# CHARACTERIZATION, ANALYSIS, AND MITIGATION OF PROCESS, VOLTAGE, AND TEMPERATURE (PVT) VARIATIONS ON ELECTRICAL MASKING AND RADIATION–INDUCED TRANSIENTS

By

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## DEDICATION

This dissertation is dedicated to God, the Creator of the planets and everything in and around them (Psalm 24:1), the Giver of life (Genesis 2:7), and the Owner of cattle on a thousand hills (Psalm 50:10-12), who strategically positioned resources and helpers along the journey of my life because of His love and unlimited grace on me.

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| | |
|---|---|
| CCE | Charge Collection Efficiency |
| FinFET | Fin-Shaped Field-Effect Transistor |
| $I_{drive}$ | Drive Current |
| $I_{SET}$ | Radiation-Induced Transient Current |
| IC | Integrated Circuit |
| LET | Linear Energy Transfer |
| MFG | Most Frequent Gates |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| MTFs | Multiple Transient Faults |
| PPA | Performance, Power, and Area |
| PTM | Predictive Technology Model |
| PVT | Process, Voltage, and Temperature |
| $Q_{coll}$ | Collected Charge |
| $Q_{crit}$ | Critical Charge |
| $Q_{dep}$ | Deposited Charge |
| SCE | Short-Channel Effect |
| SEE | Single-Event Effect |
| SEMT | Single-Event Multiple Transients |
| SER | Soft Error Rate |
| SET | Single-Event Transient |
| SEU | Single-Event Upset |
| SoC | Systems On Chip |
| SRAM | Static Random Access Memory |
| SV | Sensitive Volume |
| TRM | Triple Modular Redundancy |

# CHAPTER 1

# INTRODUCTION

FinFET technology evolved to overcome the prevalent issues in bulk technology due to scaling. It offers benefits on performance, power, and area (PPA) of an electronic design. It has an improved reliability response compared to bulk MOSFET technology. In addition, it has a better short-channel effect (SCE) , increased drive current, reduced leakages, and reduced sensitive volume (SV) with less charge collection efficiency (CCE) [53]. The sensitive volume (SV) is a region in the device or circuit that, if enough charge generates within it, results in a single–event effect (SEE). SSV reduces with the technology scaling and determines the quantity of the collected charge, $Q_{coll}$, when the charge is deposited, $Q_{dep}$. Hence, planar technology has a larger sensitive volume (SV) to collect, $Q_{coll}$, the deposited charge, $Q_{dep}$, than FinFET technology node [34].

The critical charge, $Q_{crit}$ , which is the minimum charge that causes an upset, also continues to reduce. The reduction in $Q_{crit}$ reduces the electrical masking of an electronic design. Masking, which can be electrical, logical, or temporal (or timing window), is an error-prevention mechanism in logic circuits. It suppresses the propagating radiation-induced single-event transient (SET) pulse. If the propagating transient is not masked, the radiation-induced fault leads to an error when the propagating transient pulse latches at the storage element or memory cell [55].

The performance of FinFET technologies depends on their physical models and the structure of the fins [28]. A reduced sensitive volume (SV) that leads to a reduced charge collection efficiency (CCE) [52] has an impact on the resulting transient pulse. The charge accumulation/deposition is limited around the fins compared to the bulk technology body [84], as shown in Fig. 1.1. In the radiation environment, the devices with wider fins collect more charge when exposed to heavy ions [29]. Therefore, the technology is radiation-tolerant due to the reduced area (SSV) to collect deposited charges compared to bulk technology. Also, it has a parasitic capacitance interconnect [37]. The capacitive network creates resilience that increases the nodal capacitance and generates a transient pulse with smaller width compared to planar devices [83]. An increase in the drive current, $I_{drive}$ , which is an opposing current to the induced transient current, $I_{SET}$, also contributes to a small

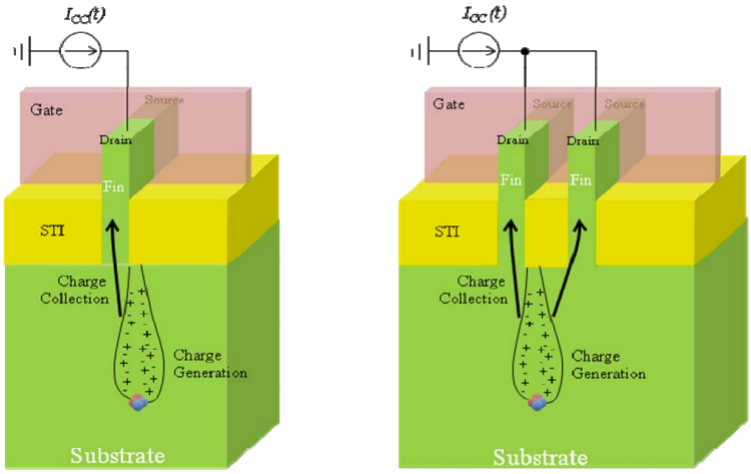



Figure 1.1: Illustration of a simulation for the charge collection efficiency between (a) single-fin and (b) double-fin structures as shown in [39]. The charge collection efficiency depends on the sensitive volume and the number of fins.

pulsewidth of the propagating transient pulse in designs implemented using FinFET technologies.

However, as the technology scales and continues to adhere to Moore's law [47], there are reliability issues in newer technologies such as FinFET. It is challenging for scaled silicon designs to sustain particle strikes because *the source of the particle strikes does not scale as the technology does*. When radiation particles impact the technology, it leads to the emergence of radiation-induced transient dependent on the quantity of collected charge, $Q_{coll}$, from the deposited charge, $Q_{dep}$. The capability of the scaled critical charge, $Q_{crit}$, is not enough to suppress the impact of the accumulated charge, $Q_{coll}$. Then the radiation-induced transient flips the node's value. Although multi-gate designs, such as FinFET technology, are still susceptible to radiation-induced soft errors, they have better vulnerability responses than bulk MOSFET technologies because of significantly reduced sensitive volume (SV). The amount of charge collected, $Q_{coll}$, from the deposited charge, $Q_{dep}$, depends on the sensitive volume (SV).

An electronic design's operation involves the process, voltage, and temperature (PVT) variations. Therefore, the variation is vital in determining the design's possible deviation from the reliability and output expectation. With variations, there is an increased probability that the radiation-induced transient, initially with no severe threat, causes reliability issues [57]. These conditions make the radiation-induced transient pulse in nanometer technologies experience propagation-induced

pulse broadening [25]. The impact continues to manifest as the technology scales. For instance, Ding *et al.* [18] presented process variation modeling using the Monte Carlo method and made comparisons to the worst-case analysis. Also, authors in [38, 60] reported the effect of process variation, and the combined results of temperature and voltage variation are presented in [15] with an increase in SET–induced error cross–sections at high temperatures, even with high supply voltage. The worst-case corners of PVT variations expose the impact of scaling on the nanometer design's reliability. Therefore, analysis and implementation of today's design require consideration of the effect of variations as the uncertainty in multi-stage design flows continues to be challenging to understand and analyze.

Mitigation saves the design from failing from the impact of radiation particle strikes and variations. An appropriate mitigation methodology leads to a fault-tolerant operation of an electronic design. The silicon designs implemented with nanometer technologies require new mitigation techniques to prevent eroding the benefits of scaling. Mitigation increases the electrical masking of the designs to minimize or eliminate the propagation of radiation-induced transient pulse. The electrical masking increases when the design's node capacitance or voltage increases. Different ideas from the circuit-level [33, 41] to the cell layout/placement approaches [82, 36, 20] have been presented as mitigation techniques for creating a robust design. Often, there is a high cost when individual gates are hardened during mitigation procedures. However, when the selected path approaches [57, 68] are implemented, the penalty reduces because only the vulnerable gates are identified and replaced with the gates of higher nodal capacitance [41, 68]. Also, sizing the gates and carefully selecting the gate dimensions [85] strengthened the gates' electrical masking capability with reduced overhead.

Since mitigation comes with an overhead penalty, developing a data-driven approach to select various techniques/options based on the trade-off between cost and reliability is necessary to minimize design reliability issues. Furthermore, the technique avoids high mitigation costs impacting the design's area and power. Hence, the dissertation analyzed a fault-tolerant design approach using a front-end flow of RTL2GDSII to mitigate the combined impact of radiation-induced transient pulses and PVT variations. The approach focuses on reducing performance-related overhead to limit reliability issues by characterizing a data-driven mitigation strategy and assessing a cost-to-reliability trade-off for several benchmark logic designs. Applying the trade-off mitigation data-driven approach affects the robustness by minimizing or eliminating radiation-induced transient

pulsewidth/amplitude of low LET.

## 1.1 Research Contributions

The contributions of this research are summarized as follows:

1. The research characterized the radiation-induced transient pulses using advanced technologies (e.g., FinFET) to evaluate the resilience and vulnerability to fault injection.

2. The research analyzed a fault-tolerant design approach that mitigates the combined impact of radiation-induced transient pulses and PVT variations.

3. The research implemented a cost-to-reliability trade-off mitigation strategy with selected options of a reduced penalty and better reliability response compared to the traditional means of mitigation.

## 1.2 Dissertation Organization

The research work described in this dissertation is organized as follows:

1. Chapter 1 gives background information, motivation, contributions, and organization of this work.

2. Chapter 2 provides and explains the single-event effect mechanisms in silicon designs. It entails the description of the event that leads to the charge generation, deposition, and collection process in silicon. In addition, the basic mechanisms of linear energy transfer (LET), critical charge, radiation-induced faults, and soft errors are also discussed.

3. Chapter 3 explains the types of masking principles. Then, the effects of the voltage and temperature variations on the electrical masking on silicon designs implemented using MOSFET and FinFET technology are discussed. The work on electrical masking is part of a published study in [54]. Finally, the chapter validates the technology used by validating with the experimental data published in [23].

4. Chapter 4 explains the effect of uncertainty in a different stage of the multi-stage design flow. The chapter discusses the impact of the process, voltage, and temperature (PVT) variations on transient pulse propagation in synthesis gates. The mechanisms of pulse broadening in

combinational circuits are also explained. The work on pulse broadening in synthesis gates is part of a published study in [57]. As FinFET technologies show the slightest increase with the temperature variation, the effect on compensating relationship between the threshold voltage, $V_{TH}$, and current drive, $I_{drive}$, is analyzed in pulse broadening. Finally, the technology is validated by comparing the simulation data to the experimental data published in [27].

5. Chapter 5 explains the impact of particle strikes and advanced technologies on memory cells. It examines the vulnerability of SRAM using FinFET technology. A model-based approach for estimating a memory cell's Soft Error Rate (SER) is discussed. When validated with the experimental data, the modeling process can be used for additional analysis of similar technologies without the expense of laser beam or heavy ion testing. The work extends a published study in [56]. The approach is validated with the experimental data published in [71].

6. Chapter 6 explains the principle for mitigating the propagating radiation-induced transients. In addition, it explores different mitigation techniques earlier presented in previous publications. Previously published studies [55, 56, 57] on mitigating induced transients with PVT variations in bulk and FinFET technologies are also discussed. Finally, the technology models are validated using the experimental data published in [71].

7. Chapter 7 entails the cost-to-reliability trade-off techniques for improving the robustness of electronic designs while minimizing the performance-related overhead cost. Most Frequent Gates (MFG) and fanout mitigation approaches are discussed. The techniques provide data-driven techniques with options that minimize the cost of creating resilience designs. The flow of identifying the logic gates with fanout in a synthesis file using Python scripts is also discussed and presented.

8. Chapter 8 summarizes the dissertation work by providing information about the contribution of this dissertation work.

# CHAPTER 2

# SINGLE-EVENT EFFECTS (SEE) MECHANISMS

Single-Event Effects (SEE) are random and localized occurrences in a device or circuit. They are caused by high-energy particles hitting the sensitive region of the electronic device or circuit, known as the sensitive volume (SV).

## 2.1 Generation, Deposition, and Collection of Charge in Silicon Devices

The charge generated, deposited, and collected in a silicon device depends on various factors, such as the type and sources of the radiation particle strike. The charges are generated through direct and indirect ionization. The indirect ionization of charge occurs when secondary particles created from the nuclear interaction between energetic particles and the semiconductor device lead to the generation of electron-hole pairs in the semiconductor device. In direct ionization, the energetic charged particles generate electron-hole pairs in the sensitive volume (SV) and lose energy as they travel through the material [7].

The deposition process creates a cloud of electron-hole charge collected at the sensitive OFF-state p-n junction within the material. The quantity of charge collected, $Q_{coll}$, depends on the type of material. Therefore, the percentage of collected charge, $Q_{coll}$, is lower than the deposited charge, $Q_{dep}$ as the technology and the sensitive volume (SV) of the technology scale. For instance, as shown in Table 2.1, the value of generated charge using TRIM shows that an average of 34% of the total deposited charges were collected based on the experimental data reported for five different ions in a 180 nm non-epitaxial bulk CMOS process featuring dual wells [48]. SV determines the extent to which deposited charges, $Q_{dep}$, are collected, $Q_{coll}$. Therefore, more charges are collected, $Q_{coll}$, when technology has a high sensitive volume (SV). The collected charges, $Q_{coll}$, in the reversed-based p-n junction cause a state change that involves drift, diffusion, and recombination of electron-hole pairs. The built-in electric field causes charge transport during the drift process, and the charge concentration gradients are responsible for charge transport during diffusion. Finally, the charged particles (holes and electrons) combine in the recombination phase. Fig. 2.1 shows the processes during charge collection.

Table 2.1: The experimental data from [48] with an average charge collection efficiency, $\frac{Q_{coll}}{Q_{gen}}$ of 34% of the total charge deposited.

| **Ion** | $Q_{gen}(pC)$ | $Q_{coll}(pC)$ | $\frac{Q_{coll}}{Q_{gen}}$ |
|---|---|---|---|
| **Ne** | 3.90 | 0.70 | 0.20 |
| **Ar** | 7.00 | 2.10 | 0.30 |
| **Y** | 15.20 | 6.00 | 0.40 |
| **Ag** | 18.50 | 6.50 | 0.40 |
| **Ta** | 28.00 | 10.10 | 0.40 |

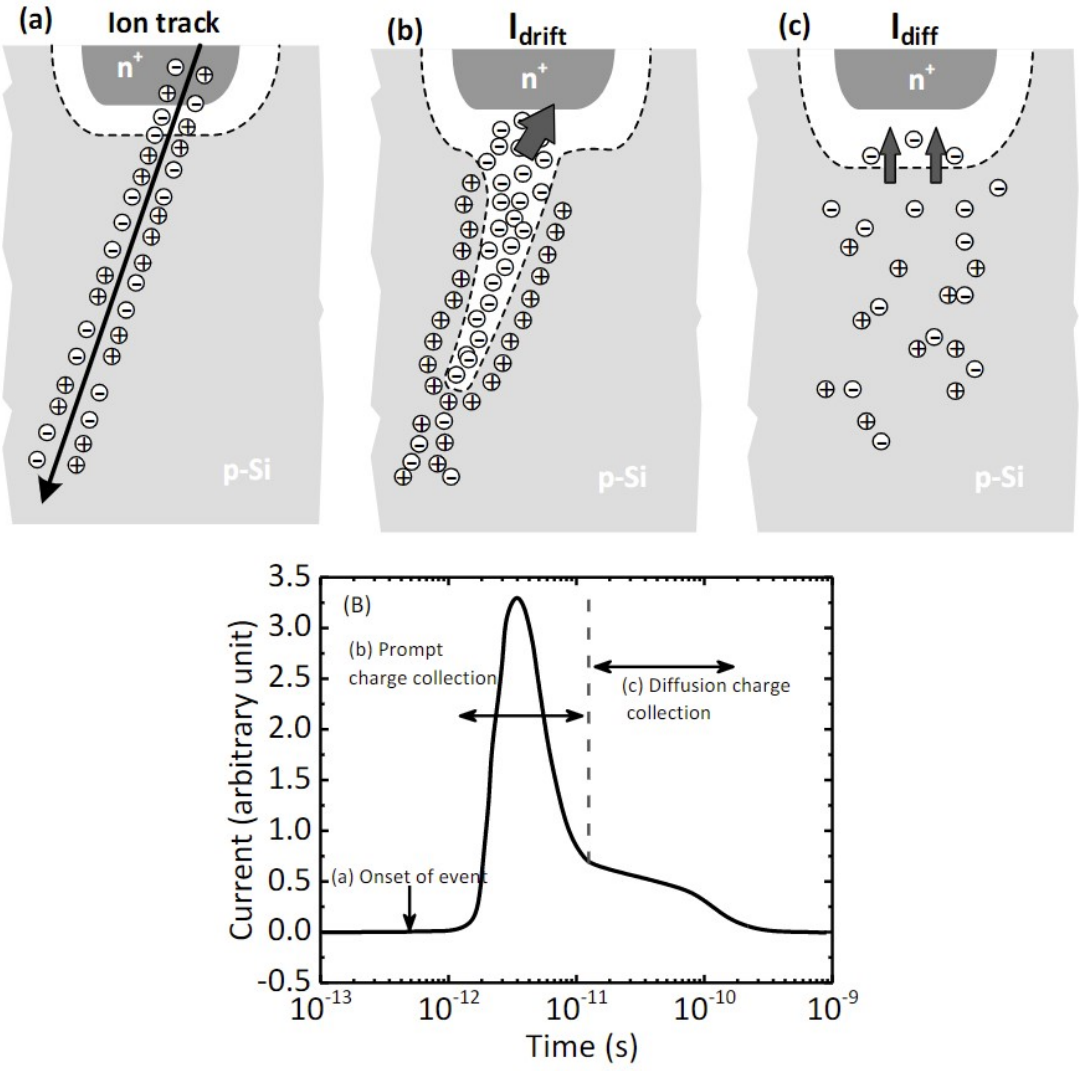



Figure 2.1: Charge generation and collection in a reversed pn junction and resulting current transient caused by the movement of high-energy particle ions. [7]

## 2.2 Linear Energy Transfer (LET)

The ionizing particle strikes on CMOS technology cause the creation of electron-hole pairs that lead to the generation of a radiation-induced transient current, $I_{SET}$ . The quantity of deposited charge depends on the LET. LET is the average energy loss rate to the generated electron-hole pair during particle strikes. The conversion between an ion's LET and charge deposition per unit of path length through the device is provided by Massengill in [44]. Eq. 2.1 shows the relationship between the LET and the quantity of deposited charge, $Q_{dep}$, per 1 $\mu m$ penetration length, L, in silicon technology:

$$Q_{dep}[\frac{pC}{\mu m}] = LET[\frac{MeV - cm^2}{mg}] \times 1.035x10^{-2} \tag{2.1}$$

The LET value estimates the corresponding quantity of charge deposited that causes a single-event upset (SEU) in the sensitive node. Hence, a LET of 1 MeV-cm$^2$/mg deposits an approximate 0.01 $pC/\mu m$ charge. Double exponential waveform does not fully account for data in circuit modeling, but it is mainly used as the based function for modeling SEE [35, 46]. The equation is shown as follows:

$$I_{SET}(t) = \frac{Q_{dep}}{\tau_f - \tau_r}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right) \tag{2.2}$$

where $Q_{dep}$ is the charge deposited due to particle strike, $\tau_f$ is the collection time constant, and $\tau_r$ is the ion-track time constant. It is usually connected to the output of the affected gate and used in SPICE simulations to capture an approximate response of the circuit to fault injection.

## 2.3 Critical Charge

Critical charge, $Q_{crit}$, is the minimum charge that results from fault injection or particle strikes to cause an upset or flipping of a stored digital bit. The higher the critical charge, $Q_{crit}$, the better the design response to the radiation particles' impact. As the technology scales, the critical charge, $Q_{crit}$, reduces the recovery ability of the storing node from the particle strikes or fault injection. If the value of the collected charge, $Q_{coll}$ from the deposited charge, $Q_{dep}$ exceeds the critical charge, $Q_{crit}$, of the sensitive node, then the stored value in a memory cell or combinational logic gate flips. Fig. 2.2 [65] shows experimental data of how the critical charge, $Q_{crit}$, reduces as the technology

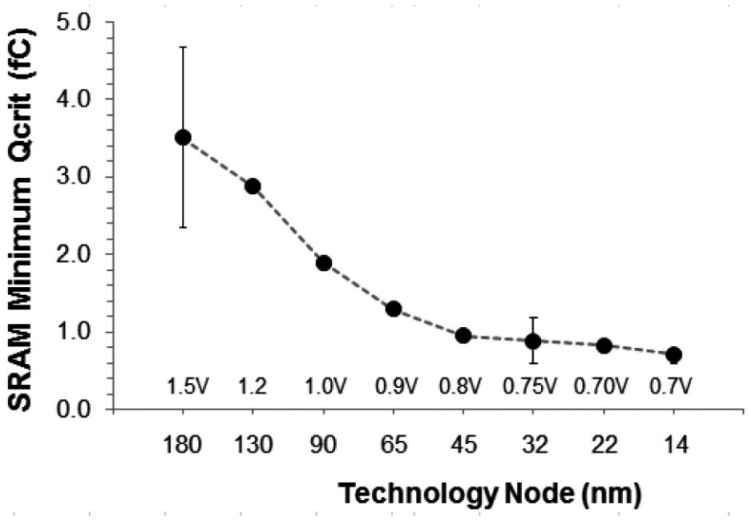



Figure 2.2: The experimental data of the minimum critical charges for SRAM devices at nominal technology voltages reported in [65].

scales with the nominal operating voltage. The results indicate that the scaled SRAM cell and a scaled operating voltage lead to a significantly low critical charge, $Q_{crit}$, that impacts the soft error rate (SER). The scaled critical charge, $Q_{crit}$, causes a reduction in the masking ability of the storing node of a memory cell. Since the technology scaling impacts these parameters, the vulnerability of the designs implemented in advanced technology nodes would also be affected. The vulnerability of the SRAM cells can be estimated using a soft error rate (SER). The common equation for estimating SER modeled by Hazucha & Svensso [32], and referenced by different authors [10, 59, 66] shows that SER depends on the critical charge ($Q_{crit}$), collected charge ($Q_{coll}$), and diffusion area ($A_{diff}$) of the technology as shown in the Eq. (2.3):

$$SER \sim A_{diff}\ exp\ (-\frac{Q_{crit}}{Q_{coll}}) \tag{2.3}$$

Though the data reported by Hazucha & Svensso [32] is based on neutrons, the data can give a reasonable judgment about the vulnerability of a memory cell.

## 2.4 Faults and Errors

Particle strikes on a silicon device or circuit deposit charge, $Q_{dep}$, in the device as the ionizing

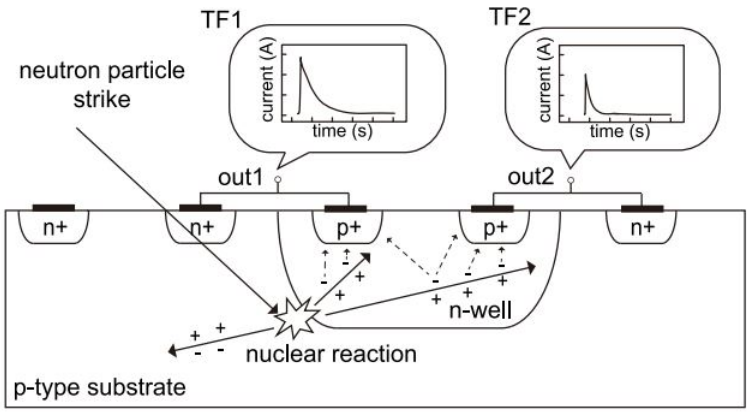



Figure 2.3: Illustration of MTFs induced by a single neutron strike [33]. The impact of particle strikes on multiple logical nodes leads to MTFs.

particles pass through semiconductor devices. The energy depositing movement leads to a fault due to the charge collected, $Q_{coll}$. The error can be permanent (hard) or transient (soft) [9]. Permanent errors are also known as hard errors because of their destructive nature. They are not correctable. They lead to failures that cause permanent damage to the circuit. Examples include single–event (SE)–burnout (SEB) and single–event (SE)–gate rupture (SEGR) in power transistors. The scope of this work does not focus on these types of errors.

On the other hand, soft errors occur when the radiation-induced fault latches into the memory cell. They can be corrected with no damage to the circuit. For example, the single energetic particle event leads to a single-event transient (SET) occurring at a node in combinational logic, and a single–event upset (SEU) in the circuit's logic state relates to memory elements [9]. Resetting or powering off and on a design can quickly eliminate soft errors. Technology scaling offers more transistors to enable system-on-a-chip (SoC) integration, but it also means more transistors are affected by radiation-induced faults. The impact of those faults increased the concern for the reliability of designs of newer technologies. Although not all particle strikes lead to radiation-induced transients, the scaling causes the radiation-induced faults in integrated circuits (ICs) from Single–Event Transient (SET) faults to Multiple Transient Faults (MTFs) [33]. This is because the density of the design's logic gates increases as the technology scales. As a result, MTFs affect many cells within the particle strike radius [22, 21, 12], as illustrated in Fig. 2.3, thereby increasing the error rate [19]. Hence, radiation-induced transients of sufficient amplitude and pulsewidth may be a con-

cern since the propagating transients have high amplitude and pulsewidth to flip the digital value of combinational circuits.

## 2.5 Chapter Summary

An overview of single-event effects (SEE) as it relates to silicon devices and the circuit is presented in this chapter. The mechanisms that lead to charge generation, deposition, and collection are also discussed. The linear energy transfer (LET) for circuit modeling of charge deposition is also reviewed as it applies to major work completed in this dissertation. The impact of the critical charge, the type of faults, errors, sensitive volume (SV), and the effect of scaling as it leads to Multiple Transient Faults (MTFs) from Single–Event Transient (SET) faults are also discussed.

# CHAPTER 3

## MASKING PRINCIPLES AND VARIATIONS

A Single Event Transient (SET) induced from radiation strikes on an integrated circuit (IC) can be masked electrically by logic gates while propagating through the circuit towards a storage element (e.g., flip-flop). With the continuous scaling of the silicon technology, there are simultaneous reductions in voltage, cell size, and internal capacitances that impact the properties of the logical gates of the electronic design. Scaling reduces the design's critical charge ($Q_{crit}$) and the gates' electrical masking capability. Reduction in $Q_{crit}$, which accompanies technology scaling, causes the silicon design implementations to be susceptible to radiation-induced soft errors. A soft error is a reliability issue in modern silicon technologies, and its prevention or mitigation largely depends on the technology features. Hence, radiation-induced transients are more likely to reach the storage elements. In addition, the induced transient fault may lead to an error if its propagation latches in the memory element.

The propagation of an induced transient depends on the energy of the particle strike and other operating conditions. Older technology models, such as 90 nm and 45 nm, tend to attenuate the propagating transients. The technologies have operating voltages ($V_{DD}$), with an increase in drive currents, $I_{drive}$, that reduce radiation-induced currents. Fig. 3.1 depicts the impact of technology scaling on the critical charge, $Q_{crit}$, and the nominal voltage, $V_{DD}$, of the technology models [1] as part of the results published in [54]. A scaled technology, such as 16 nm with reduced operating voltage and size, caused an induced transient to traverse through additional gates before being fully attenuated. *Note that fabrication technology has continued to follow Moore's law [47], while the radiation sources remain the same and even worse in some situations [8].* The number of affected nodes increases with the density of gates on the fabricated die. Although not all particles strike, translate to faults [33], any fault of sufficient amplitude may become a source of concern since the amplitude is enough to flip the digital value of combinational circuits and a stored bit of memory cell.

Also, voltage and temperature variations affect transient pulse propagation. The worst corner cases of the PVT variations potentially aid the transient pulse propagation due to an increase in

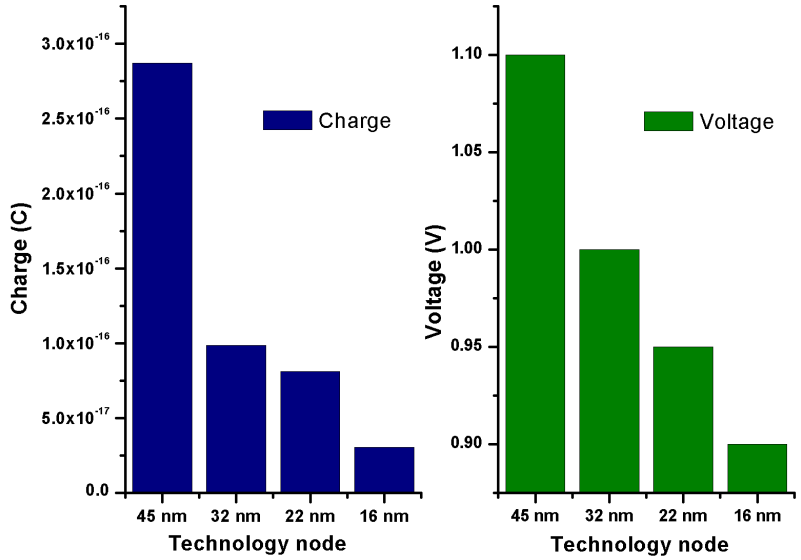



Figure 3.1: The effect of scaling on the critical charge and the nominal voltage of 45 nm, 32 nm, 22 nm, and 16 nm technologies from the Predictive Technology Model (PTM) of Arizona State University (ASU) [1]. The critical charge and the nominal voltage reduce as technologies scale [54].

pulsewidth and amplitude [54, 57]. In those cases, the induced transient pulse propagates farther than expected and aids the latching of the propagating induced transients in the storage elements. The amplitude of the radiation-induced voltage transient determines whether the transient pulse will be sustained or masked. Under nominal or typical simulations $(tt)$, if the amplitude is more than $\frac{1}{2}V_{dd}$ or close to $\frac{3}{4}V_{dd}$, then there is a tendency for the transient masked in older technologies, such as 90 nm, to propagate in newer technologies such as 22 nm and 16 nm. In the presence of the worst cases of variations, a transient that poses no threat initially [55] can flip a digital bit with high amplitude and pulsewidth increased by variations. Hence, with multiple cells placed in a small die space, Multiple Transient Faults (MTF) affect cells within the particle strike radius [12, 21, 22] that increase the error rates.

## 3.1 Types of Masking

The masking principle is an error prevention mechanism that weakens or mitigates the propagation of radiation-induced transients before latching on the memory elements or causing any error at the primary outputs. The ability of the logical gates within the logic depth to mask the propagating

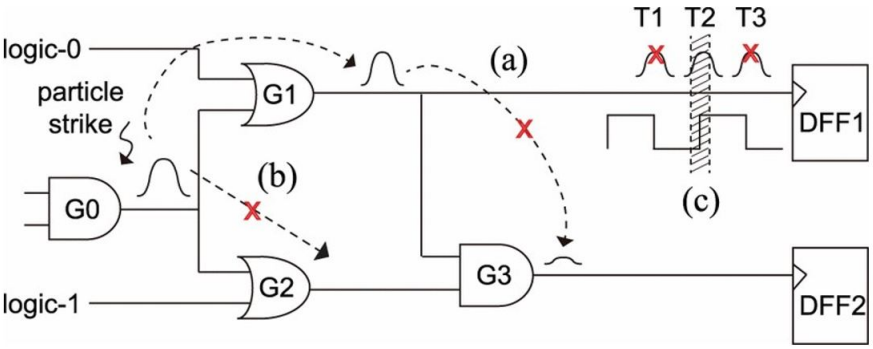



Figure 3.2: Logic circuit implementation used to explain the logical, timing, and electrical masking principles. Gates *G0* is the source of the impact. Radiation-induced transients traverse to other gates through its fanouts [17]. The tendency of the induced transient to propagate through the gates varies with the masking under consideration.

transients depends on the nodal capacitance of the logical nodes. The logic nodes continue to lose the capacity to weaken or suppress the propagating transients as the technology scales. Therefore, a logical gate with better electrical masking suppresses the radiation-induced faults from causing the error. There are three basic masking principles. These include logical, timing (latching window), and electrical masking.

1. **Logical masking**: In a logical masking principle, other inputs with controlling values block the propagating transients. The input combination dictates the transients' propagation. By applying controlling input vectors, the propagating radiation-induced transients are hindered from propagating through the input of a logic gate. For example, the input *logic–1* of gate *G2* in Fig. 3.2 is a controlling input that prevents the radiation-induced transient from the gate, *G0*, from propagating.

2. **Latching window or timing masking**: The timing masking principle uses the propagating transients' inability to meet the latching window (set-up and hold time) requirements to mask the transients. Fig. 3.2 shows the transient *T2* meets the set-up time and hold time requirements; hence, *T2* can cause an error on the flip–flop *DFF1*. Neither transients *T1* nor *T3* meet the timing requirements; hence the errors can be masked. As the scaling continues, an increase in the clock frequency of the design impacts the latching window.

3. **Electrical masking**: In electrical masking, the property of the traversing gates determines if

the propagating radiation-induced transients would be masked or not. The reduction in gate dimensions leads to reduced nodal capacitance and causes a reduction in the critical charge. The effect makes the gates more vulnerable to radiation-induced faults. For example, in Fig. 3.2, the propagation of the transient, from gate *G0* through gate *G1* to the primary output of gate *G3*, shows that the properties of gates *G1* and *G3* weaken or reduce the propagating transient. The ability of logic gates to reduce the properties of the propagating transient depends on the type of technology and the operating conditions.

The research activities in this dissertation only consider electrical masking as a significant area of focus. The principle has been studied and effectively attenuates the transient pulses. Feng and Xie [76] proposed a model for transient pulse generation and propagation for accurate soft error rate analysis using a look-up table approach based on a drain current model. An approach proposed by Watkins and Tragoudas in [78] used an analytical electrical masking approach to show improvement in Single Event Multiple Transient (SEMT) and Multiple Event Multiple Transient (MEMT) error simulations. Finally, Ramakrishnan *et al.* [61] explained how temperature affects the electrical masking and the latched window masking property for soft error rate (SER) estimations of different benchmarks and 70 nm Predictive Technology Model (PTM). The effectiveness of electrical masking depends on the nodal capacitance of a design.

## 3.2 Effect of Technology, Voltage, and Temperature Variations on Electrical Masking in *sub*-65-nm bulk MOSFET Nodes

In the era of technology scaling, the worst corner cases of variations continue to impact the technology's performance-related features, even complicating the impact of the existing transients. This section discusses results published by Olowogemo et al. [54].

### Methodology - Simulation Environments for the Inverter Chain and the Logic Circuit

To demonstrate the impact of technology scaling, voltage, and temperature variations, the inverter chain and the logic circuit are used for the implementation. Table 3.1 shows that the simulations involved six models. Two cases show the effect of technology scaling: technology-dependent and technology-independent pipeline depth. In a technology-dependent case, the number of logic gates implemented for the design increases as the technology scales from generation to genera-

Table 3.1: Technology models and the number of inverters in the technology-dependent pipeline depth. The technology modes are obtained from Arizona State University's (ASU) Predictive Technology Model (PTM).

| t | Nom. voltage | Tech. mode | No. of inverter | $c_t$ (fF) |
|---|---|---|---|---|
| 0 | 1.25 | 90 nm | 10 | 2.00 |
| 1 | 1.10 | 65 nm | 14 | 1.40 |
| 2 | 1.05 | 45 nm | 20 | 0.98 |
| 3 | 1.00 | 32 nm | 29 | 0.69 |
| 4 | 0.95 | 22 nm | 42 | 0.48 |
| 5 | 0.90 | 16 nm | 60 | 0.33 |

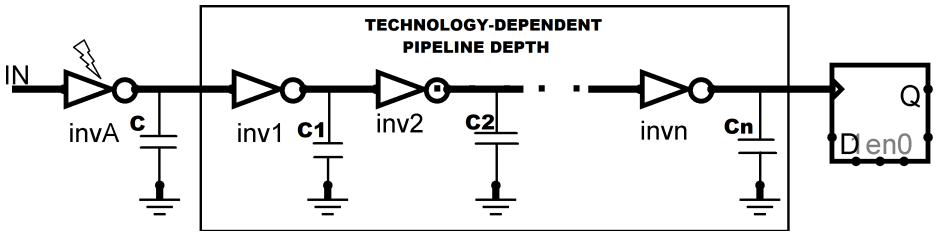



Figure 3.3: Technology-dependent pipeline depth for inverter chain simulations. The number of inverters depends on the technology, as shown in Table 3.1. The minimum length corresponds to the technology, and the number of inverters is determined using the scaling factor $k = 0.7$. In a technology-dependent pipeline depth, the number of gates increases.

tion. On the other hand, the number of logic gates for technology-independent is fixed. The cases show the impact of technology scaling on the technology nodes. Fig. 3.3 shows the technology-dependent pipeline depth set-up approach. In this case, the SPICE file of each model is prepared using the scaling factor of $k = 0.7$. The minimum length corresponds to the technology, and the number of inverters is determined using the scaling factor. Table 3.1 shows the details of the models and the number of gates simulated for each model. The capacitive loads in the output of each inverter are determined using the following:

$$c_t = k^t c_{load} \tag{3.1}$$

where $t = 0,1,2,3,4,5$ corresponding to each technology and $c_{load} = 2fF$. For example, the output capacitive load of each inverter in 32 nm technology-dependent pipeline simulation requires

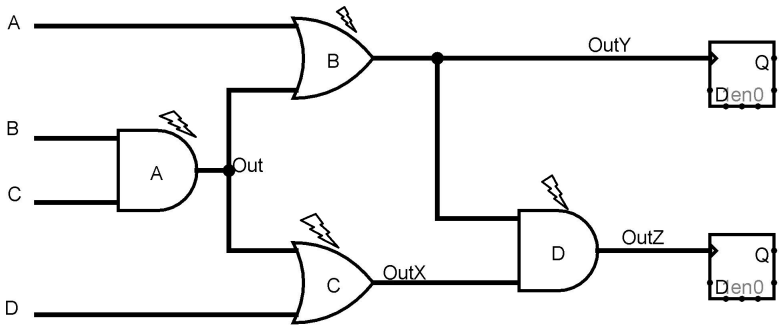



Figure 3.4: Logic implementation to show the effects of different technologies and electrical masking under variations of voltage and temperature [33]. Logic gates with better nodal capacitance and electrical properties weaken the propagating radiation-induced transient.

$c_t = c_1 = c_2 = c_3 ... = c_{29} = 0.7^3 * 2 = 0.69fF$. The same number of gates (i.e., a 10-inverter chain) is used for the technology-independent simulation pipeline depth case. The capacitive loads in the outputs of each inverter are the same ($c_{load} = c_1 = c_2 = c_3 ... = c_n = 2fF$). Fig. 3.4 shows the logic circuit implementation. The *AND Gate A* is selected for injecting the transient fault with the outer cell (*NMOS* or *PMOS*) as the primary target location for the simulation. The type of cell considered depends on the input vector and the expected output of each logic gate. The output of *Gate D* is the main target in this simulation to estimate the amplitude and pulsewidth of the propagation of the induced transient from the injected fault. Each technology model is simulated using voltage *(V)* variation chosen within $\pm 20\%$ of the nominal value, and the temperature *(T)* variation is from $T$ = -$20^0C$ to $T$ = $100^0C$ with a step size of $T$ = $60^0C$.

**Results and Discussions**

- **Effect of Technology Scaling**: Technology scaling increases the density of logic gates. Hence the number of gates transverse by the propagating radiation-induced transients increases. The effect of single–event effect (SEE) on silicon designs is more pronounced in the newest scaled technology compared to older technologies. The scaled technology has a reduced nodal capacitance, critical charge, and a scaled voltage, $V_{DD}$, that leads to a scaled drive current, $I_{drive}$, in each technology. The expression in Eq. 3.2 shows the relationship between the drive current, $I_{drive}$, of a transistor and the operating voltage, $V_{DD}$.

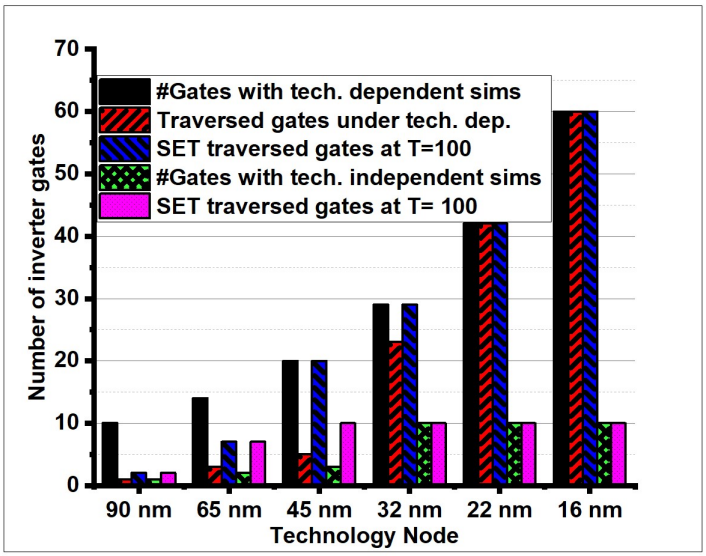



Figure 3.5: The effect of technology and temperature on the number of inverters required for masking the injected fault. For easy analysis, the same transient fault is applied. With an increase in temperature, the number of inverters traverses by the propagating transient increases in 22 nm and 16 nm nodes in a technology-dependent case.

$$I_{drive} = K\mu \frac{(V_{DD} - V_T)^2}{2} \tag{3.2}$$

As the $V_{DD}$ increases, the drive current, $I_{drive}$, which can be classified as an opposing current to the induced transient current, also increases. With the technology scaling, the value of $V_{DD}$ and the value of the opposing drive current, $I_{drive}$, reduces. Fig. 3.5 shows the results of both technology-dependent and technology-independent pipeline depth simulations. The transient pulse is masked in the 90 nm model in both cases before the output of the second inverter. However, the number of gate traverses by induced transient depends on technology models. It traverses more gates in the 22 nm and 16 nm models. As the technology scales and the operating voltage, $V_{DD}$, reduces, the number of gates traversed by the induced transient increases.

Fig. 3.6 shows the effect of the same fault injection on the technology models. Because of technology scaling that causes a reduction in critical charge, the minimum deposited charge in the 90 nm model may be challenging for the 16 nm model to sustain. Herefore,

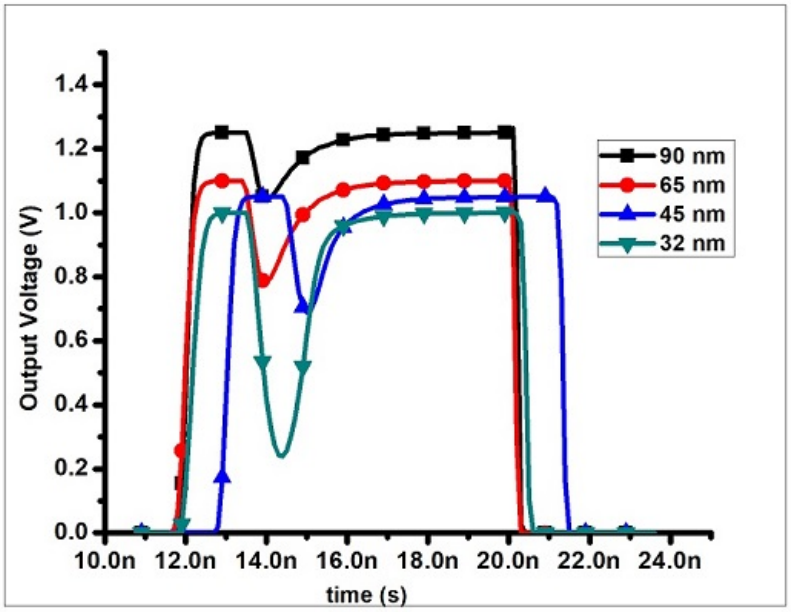



Figure 3.6: The technology models exposed to the same sources of radiation. The figure shows the effect of the same quantity of charge deposition on different technologies. With the sources of particle strikes remaining unchanged, the SET pulse is more pronounced in the scaled technologies considered in this study.

similar fault injection is difficult to be sustained for scaled technology models in the study. Since the source of particle strikes cannot be scaled, the effects of the injected fault are more pronounced in *sub*-65 nm technology. Compared to older technologies, they show a weaker capability to attenuate or mitigate the transient pulse as it traverses across more gates. As shown in Fig. 3.7, the simulation reports of the logic circuit show that 45 nm and 32 nm nodes masked out the transient pulse due to an increase in nominal voltage. For 22 nm and 16 nm, the nominal voltage reduces. As a result, the transient pulse propagated to the output gate $D$ of the circuit in 16 nm and 22 nm models, with the former having wider pulse width. A reduced $V_{DD}$ leads to less drive current.

- **Effect of Temperature**: Eq. 3.2 shows the relationship between the drive current, $I_{drive}$, of a transistor, the mobility, $\mu$, of charge carriers, and the threshold voltage, $V_{th}$. The mobility, $\mu$, and the threshold voltage, $V_{th}$, through a flatband voltage, $\phi_F$, are functions of temperature. If the temperature increases, the mobility of the electrons reduces and leads to a reduction in the drive current of the device. The effect of such a reduction in the drive current of the

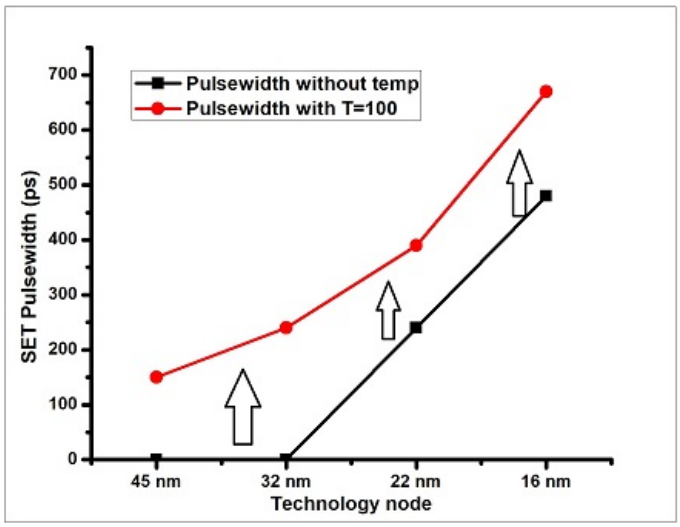



Figure 3.7: Effect of different technology on induced transient propagation of a logic circuit implementation in Fig. 3.4. While it is fully masked in 45 nm and 32 nm due to an increase in nominal voltage, $V_{DD}$, the transient propagates with an increase in pulsewidth in 22 nm and 16 nm nodes. With T = $100^0C$, there is an increase in the pulsewidth for all the technology models. Increased temperature causes charge carriers' lower mobility, leading to a lower drive current.

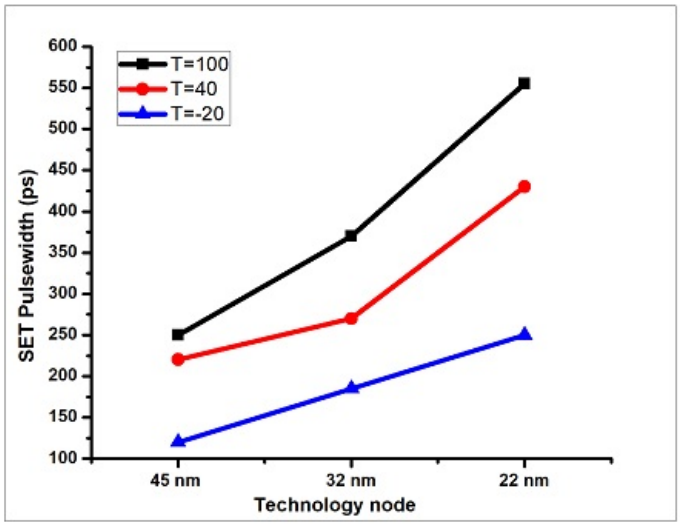



Figure 3.8: Effect of temperature on induced transient propagation using different technology. Since the temperature affects the charge carriers, the variation leads to different responses. The reduction in temperature increases the drive current due to an increase in charge mobility, leading reduction in the amplitude and pulsewidth of the propagating transient under low temperatures. As the temperature increases, the pulsewidth for all the technology models increases due to a lower opposing drive current from reduced charge mobility.

transistor gives rise to an increase in the radiation-induced current that generates a proportional induced voltage. Considering the effect of temperature on the technology-dependent and technology-independent pipeline depth, as shown in Fig. 3.5, an increase in temperature leads to an increase in transient pulse propagation with an increase in the number of gates that the transient pulse traverses. As the temperature increases, carrier mobility and thermal voltage [23] reduce and lead to a reduced drive current, $I_{drive}$, of the transistor. Hence, the induced transient current increases in amplitude. Fig. 3.8 shows the effect of temperature variations on different technology models. There is a widening or broadening of the pulsewidth as it propagates through the gates [24] as shown in Fig. 3.9. Even without a temperature increase or a reduction in nominal voltage, the broadening effect causes the induced transient to traverse through many gates in 22 nm and 16 nm nodes. The transient pulse propagates, and it may eventually latch at the storage elements if the case of MTFs is included for consideration. Since the mobility of the electrons reduces with an increase in temperature, the drive current, $I_{drive}$, will affect how the technology responds to radiation-induced transient from a particle strike (fault injection). With these results, the number of gates traversed by the transient pulse before masking increases.

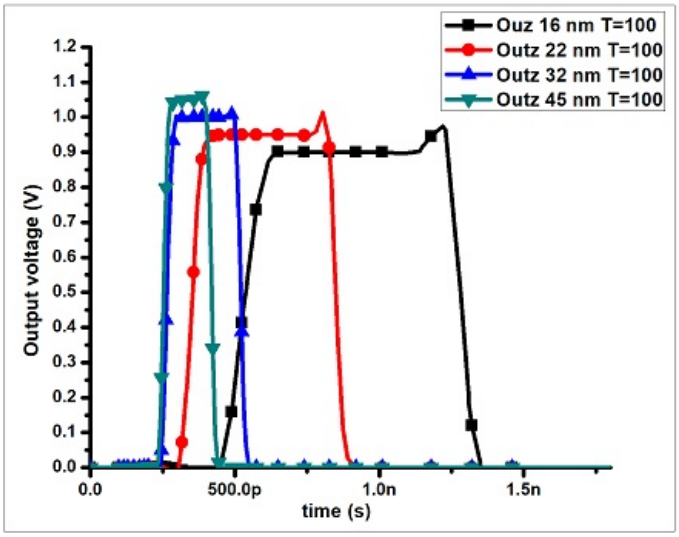



Figure 3.9: Effect of temperature on different technology nodes on the Fig. 3.4. At T = $100^0C$ with reduced charge carriers and low opposing drive current, the induced transient propagates in all the technologies but with different pulse widths due to different operating voltages. It is wider in both 16 nm and 22 nm technology nodes.

- **Effect of voltage**: Eq. 3.2 indicates that the operating voltage, $V_{DD}$ has a direct relationship with the drive current, $I_{drive}$. An increase in $V_{DD}$ leads to an increase in the drive current. Since the value differs from technology to technology, as shown in Table 3.1, the technology expects to respond differently to the impact of fault injection under different operating voltages. For instance, 90 nm with the highest $V_{DD}$ attenuates the transient more than other technology models, as shown in Fig. 3.5. Fig. 3.7 shows that 45 nm and 32 nm attenuate the propagating transient due to an increase in the operating voltage, $V_{DD}$. Likewise, in Fig. 3.9, the output gate $D$ of Fig. 3.4 depends on the type of the technology, and that dictates the operating voltage, $V_{DD}$. The technology models with high nodal capacitance and high voltage have better electrical masking capability. Hence, the models with low voltage cannot prevent the propagation of radiation-induced transient due to the continuous reduction in drive current that accompanies the scaled operating voltage, $V_{DD}$.

Technology scaling affects the electrical masking of the logic nodes through the reduction of critical charges. When node capacitance and critical charge are high, the designs of older technologies, such as 90 nm, have the sufficient electrical masking capability to minimize/eliminate the propagating transients. The logic gates have little or no resistance to limit/stop the propagation of the transients. The worst temperature and voltage variations cases increase the transients' pulsewidth and amplitude, leading to unhindered propagation of the radiation-induced transient.

### 3.3 The Impact of Scaling on the FinFET Technology

The effect of technology scaling on the electrical masking is not limited to only bulk technologies; it cuts across all the scaled technologies. In this section, the dissertation activities look at the impact of scaling on the FinFET technology nodes. The analysis explores 7-nm and 15-nm technology nodes as case studies. The critical challenges of technology scaling on SEE of 3D multi-gate technology include complicated charge–collection volume, ion tracks larger than device sizes [74], and one event affecting multiple cells. The electronic designs with multi-gate nanometer fabrication technologies have reduced dimensions, low voltages, increased frequency, and less critical charge. All these affect the design's electrical masking capability [54]. They are vulnerable when operating in an environment not free from radiation particles since the radiation sources do not scale down as the technology does, and even worse, in some cases [8].

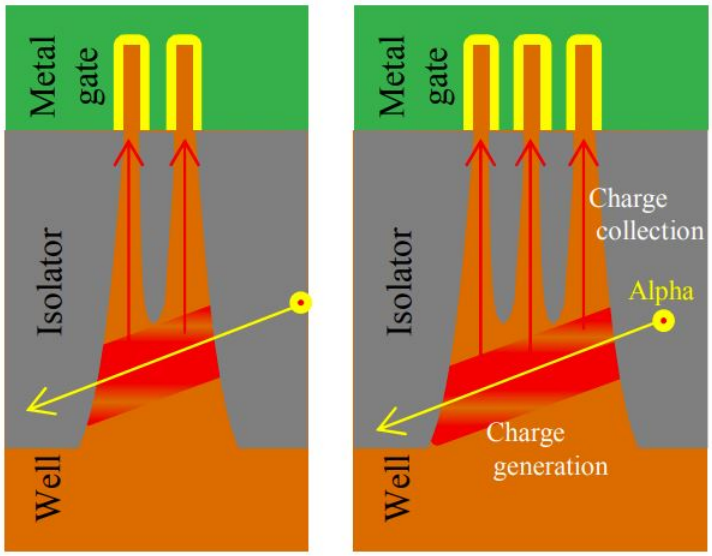



Figure 3.10: Charge generation and collection image in FinFET technology with 2 and 3 fins. The charge generation and collection efficiency in 3 fins are larger than that in 2 fins [74].

Though multi-gate technology designs have propagating transients, the 3D multi-gate technology generates transient with reduced metrics compared to bulk technology because of the high drive current, $I_{drive}$. The reduction in the sensitive volume reduces the collected charge and the transients' properties [74]. Fig. 3.10 shows the effect of the number of fins on charge generation and collection efficiency [74]. The number of fins contributes to the parasitic interconnects of the technology [37]. That makes the propagating transient with FinFET designs have induced transient with reduced amplitude and pulsewidth compared to MOSFET. An increase in fins increases the cost in terms of area and power. Transitioning from bulk MOS to multi-gate technology increases the number of gates

| **LET = 1** $Mev-cm^2/mg$ | | **NAND (mV)** | **NOR (mV)** |
|---|---|---|---|
| **Input Vector** | **00** | 10.10 | 37.20 |
| | **01** | 20.30 | 17.40 |
| | **10** | 20.20 | 17.30 |
| | **11** | 34.50 | 9.20 |

Table 3.2: Impact of the input vector on the design output. (00, 01, 10, 11). The estimated amplitude of the radiation-induced transient is in mV. The vector with a larger drain surface gives a high amplitude.

on a logic design. The probability of single–event multiple transients (SEMT) and errors are high [36] since the number of gates implemented with advanced technology increases.

### 3.3.1 Sensitive Volume

The sensitive volume is the most sensitive part of silicon design. It is significantly reduced due to technology scaling. It is a region that collects the portion of the deposited charge, leading to a fault in silicon technology. In this simulation, the location with an induced highest fault in both 2-input NOR and NAND gates is determined using 15-nm technology nodes with different input vectors at LET = 1 $Mev - cm^2/mg$. This is necessary to determine the input vectors that generate the higher induced amplitude of the transient. The simulation results of NAND and NOR with the input vectors that give a larger surface when logically connected are shown in Table 3.2. The amplitude of the induced fault is significantly less when compared to the bulk MOSFET considered in the previous section. The reduction in amplitude is due to a reduced sensitive volume of the FinFET technology that affects the quantity of charges collected from the deposited charge.

### 3.3.2 Critical Charge

The impact of scaling is not limited to sensitive volume alone. However, because the scaled FinFET technology nodes have low critical charges, a low quantity of deposited charge may give an induced radiation-induced transient with high amplitude. Fig. 3.11 shows a simulation result between 7-nm and 15-nm FinFET technology nodes. Because of the reduced critical charge in 7-nm, it generates an induced transient with higher amplitude than 15-nm. Other factors that contribute to reduced amplitude in 15 nm include operating voltage. The voltage at 15 nm is higher compared to 7-nm. It means that 15-nm has a higher drive current than 7-nm, which shows that the technology provides a higher opposing drive current to the induced current. Hence, critical charge plays an important role in the electrical masking of an electronic design.

## 3.4 Validation of Simulation Results With the Experimental Data - Estimation of Static Current as a Function of Temperature

The temperature affects the drive current through the mobility of the charge carriers. In this section, 7-nm and 15-nm FinFET technology models are validated using the experimental data. The

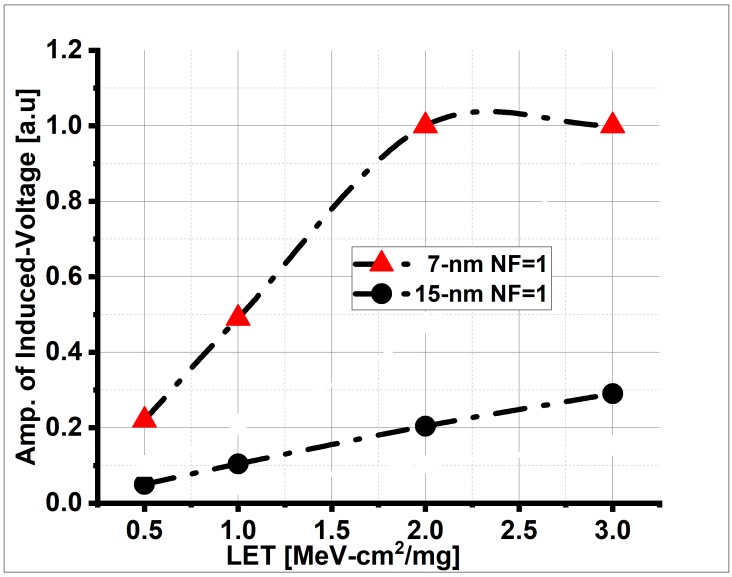



Figure 3.11: The LET increases as the amplitude of the radiation-induced voltage transient increases. In 7-nm, the amplitude of the radiation-induced transient is higher since the technology has a lower critical charge that dictates the electrical masking of the design.

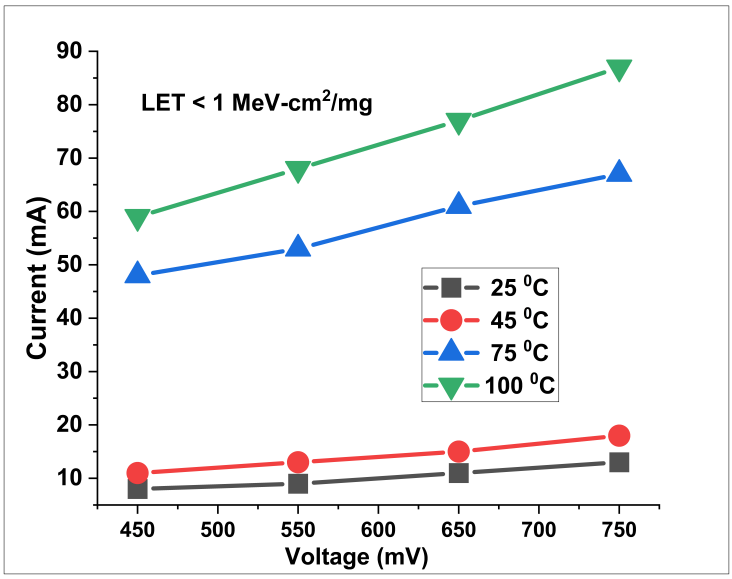
estimated static current as a function of voltage and temperature was compared and validated to the experimental data presented in [23].

### 3.4.1 Design Approach

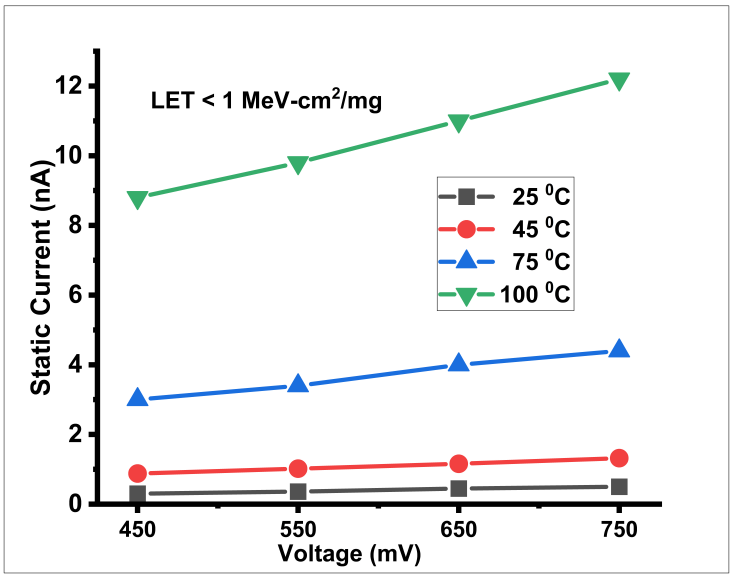
As a function of voltage and temperature, the static current is estimated using a simulation of 20-chain inverters. The static current can be estimated when the circuit is not switching. The significant current flows through either of the transistors when $V_{DD} = 0$ or $V_{DD} = V_{DD}$, and the values is the nearly the same.

### 3.4.2 Discussions of results

Fig. 3.12 (b) shows the simulation results. There is an increase in leakage current as the voltage increases, but with low and insignificant differences, even at a higher temperature. These simulation results represent the impact of temperature on the leakage current of ring oscillators under fault injection. FinFET technology has a minimal temperature change due to a competing relationship between the carrier mobilities, thermal voltage, and charge collection, leading to insignificant differences as the temperature changes [23, 11]. An increase in temperature in FinFET technology




(a)




(b)

Figure 3.12: The plot in (a) shows the experimental data of Static IC-level current as a function of temperature and supply voltage reported in [23] and (b) shows the simulated static IC-level current as a function of temperature and supply voltage using FinFET 7-nm technology.

does not increase the drive current like that of MOSFET nodes because of the compensating relationship between the carrier mobility and threshold voltage [11]. In addition, the compensating saturation current relationship between the NMOS transistor and PMOS transistor causes a reduction in the leakage current since the transistors have a reduced threshold voltage [23]. The published results in [23, 11] show an exciting response from the simulated and experimental data. The plot in Fig. 3.12 (a) is consistent with the reported data in [23] after the alpha particles' exposure. As the temperature increases, the leakage currents increase, and the collection charges reduce in FinFET technology [23]. The reported data of 16-nm and 7-nm technology models show insignificant differences.

## 3.5 Chapter Summary

Technology scaling reduces the electrical masking of logic gates. Hence, the logic gates cannot attenuate the transient pulse from being propagated toward the storage elements. With multiple transients and denser placement of transistors on a chip, cells will be prone to strikes and generate transient pulses that traverse more gates before latching on the memory cell. The effect of technology scaling, temperature, and voltage on electrical masking of *sub*-65 nm combinational logic circuits and FinFET technologies manifest as the scaling continues. In bulk MOSFET, temperature changes show a huge impact compared to those noticed under FinFET technology. The competing and compensating relationship between the charge collection, carrier mobility, and thermal voltage leads to an insignificant difference in FinFET technology. As the technology scales, the drive current and mobility reduce, leading to a reduction in the electrical masking of electronic designs.

# CHAPTER 4

# THE EFFECTS OF PROCESS, VOLTAGE, AND TEMPERATURE VARIATIONS ON PULSE PROPAGATION IN SYNTHESIZED DESIGNS

As fabrication technology advances for semiconductor and system technology, the probability of device failure increases because the sources of variation and failure become too complex to be fully understood [13]. Using advanced technology nodes requires a complex fabrication approach that adds uncertainty throughout the multi-stage process flow. For instance, factors like reduced device reliability, increased parameter uncertainty, increased capacitive coupling, and die packaging, become more complex as the technology scaling trend continues [13, 67]. As a result, uncertainty exists across the multi-stages of a design, from technology fabrication to design implementation. The inability to fully capture the issues introduced due to these complexities and needing more knowledge to address them leads to uncertainty. These uncertainties in an electronic system design's hierarchical flow reduce the design's reliability. The success of an electronic system design depends on developing a robust design that performs an intended function while minimizing or eliminating issues with reliability. However, uncertainty occurs at every stage of an electronic system. Variations, aging, and operating environment factors can also cause uncertainty [67]. They introduce uncertainty into the multi-stage design phase of the flow. For instance, as the technology scales, the process variation related to device fabrication becomes challenging. Process variation is a significant source of uncertainty. Other variations, such as operating voltage, $V_{DD}$, and temperature, may be introduced due to operation and environmental factors.

In this dissertation work, the variations are simulated across different design corners, which give solutions that differ from nominal simulations. As stated in [13], adding a data-driven decision that is informed by data collected may be of help to reduce the issue of uncertainty. In that case, uncertainty can be characterized and optimized using statistical methods such as stochastic-based design and optimization methods [67]. These are techniques used to characterize uncertainty and its mitigation. Hence, the sources of uncertainty in design can be managed.

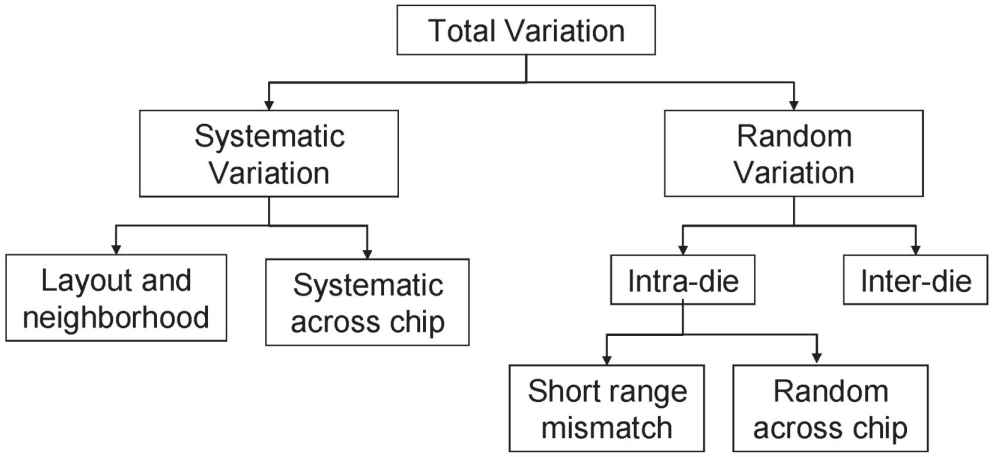



Figure 4.1: Types of variation as described in [64].

## 4.1 Process, Voltage, and Temperature Variations

Variations can be categorized into random or non-systematic sources, and systematic sources of variation [64]. Systematic variations are deterministic and estimated by applying the deterministic function. Random variations can only be characterized by distributions due to their stochastic nature [72]. Fig. 4.1 shows the variation classification based on the differences in the root causes of the types of variation [64]. It is a concern as the technology scales, and the impact of variation in the process, voltage, and temperature (PVT) continues to manifest as the technology scales. It introduces a deviation in the operating factors and alters the design's output [25, 57] due to an introduction into the design phase. The effect of variations depends on the corners of considerations. The best corners provide a situation that reduces and weakens the amplitude and pulsewidth of a propagating transient. The worst corners of variation aid the propagation of the transient with high amplitude and pulse width that aid the traversing of more gates during propagation. Since the logic gates respond differently to the particle strikes or fault injected, the type of gates also dictates the radiation-induced transients. The PVT variation issue is prevalent with an integrated circuit (IC) design. It is an area of interest during electronic designs because it affects the design's switching speed (timing). This problem worsens as technology scales and increases the variation of design-related parameters [79].

### 4.1.1 Process variations

Process variation is one of the primary sources of uncertainty, and it remains challenging to address as the scaling trend continues [13]. The process variation is related to issues caused during the lithography step of the fabrication process [72, 87]. Classification of process variations depends on the spatial scales, and their nature [72]. It can be classified as systematic and random variations based on their nature. Regarding spatial scales, they can be classified as inter-die (global) and intra-die (local) variations. Global variation is related to the device parameters that affect the transistors equally. Examples include oxide thickness and dopant concentration. Local variation has a different effect on the transistor. It can be classified as the mismatch of random uncorrelated variations [79]. Inter-die process variation is regarded as a die-to-die variation. It is a variation that occurs between different chips on the same wafer. Intra-die process variation is known as within-die variation. It is a variation between elements in the same die or chip. It accounts for variations within the same chip [2, 31].

Simulations with process variation help quantify the extent to which the design deviates or behaves under different technology process corners. In the published work by Ding *et al.* [18], the authors presented process variation modeling using the Monte Carlo method and made comparisons to the worst-case analysis. The authors showed the dependence of $Q_{critical}$ variation on gate length variations and threshold voltage, $V_{TH}$. Also, the impact of process variation on the reliability and performance of 32-nm 6T SRAM is highlighted in [38]. In today's design, PVT variation cannot be neglected. The variation needs to be considered during design, analysis, and simulations; otherwise, such designs may fail when exposed to similar variations during applications. Therefore, extreme corner cases present an ideal consideration during design phases. The process corners include *fast (ff), typical or nominal (tt)*, and *slow (ss)* corners. The corners *(tt, ff, ss)* are based on features of the technology models tailored for specified corner simulations. For instance, a fast corner case increases the design drive current and maximizes speed. Slow corners provide the opposite results. Apart from the three *(tt, ff, ss)* corners considered in this work, *slow-fast (sf)* and *fast-slow (fs)* corners are other additional corners as the scaling effect continues to fluctuate design-related parameters.

### 4.1.2 Operating voltage

The operating voltage, $V_{DD}$, is one of the most impacted metrics of silicon technology. Reducing $V_{DD}$ leads to lower power consumption and increases path delay in logic design. However, as the $V_{DD}$ value reduces, the reduction leads to reliability issues that affect the electrons' mobility and cause a reduced transistor drive current. If the drive current is lower than the radiation-induced transient current, it leads to a transient voltage with high amplitude and pulsewith with propagating potentials. Therefore, an increase in $V_{DD}$ is an excellent mitigation strategy for radiation-induced transients. While increasing $V_{DD}$ helps the gates' masking ability, low $V_{DD}$ causes the transient with sufficient amplitude and pulsewidth to propagate. The combined impact of low $V_{DD}$ of operation and the radiation-induced transient leads to pulse broadening [25, 26].

### 4.1.3 Effects of temperature

Temperature is another critical operating factor that requires urgent consideration during the design, analysis, and implementation phase of electronic designs. A reliable electronic design will operate without failure in different weather conditions of varying temperatures. Eq. 3.2 shows a relationship between the drive current, $I_{drive}$, carriers mobility, $\mu$, threshold voltage, $V_{TH}$ and operating voltage, $V_{DD}$. The current drive, $I_{drive}$, of a transistor, is determined by the carrier mobility, $\mu$. Carrier mobility, $\mu$, is affected by temperature. Temperature also affects the design's threshold voltage, $V_{TH}$, since it affects the thermal voltage. An increase (a decrease) in temperature increases (reduces) the thermal voltage. This leads to a reduction (increase) in $V_{TH}$. A lower (an increase) in $V_{TH}$ leads to an increase (a decrease) in drive current, $I_{drive}$. From the compensating relationship between the threshold voltage and carrier mobility [11, 23], the resultant drive current, $I_{drive}$, of the transistor determines the status of the induced transient, $I_{SET}$. If the resulting drive current, $I_{drive}$, increases (reduces), then the induced transient decreases (increases) in pulsewidth and amplitude. Each technology in Fig. 3.8 operates at a different operating voltage, $V_{DD}$, with 22 nm as the lowest $V_{DD}$. At $100^0C$, the pulsewidth increases since the transistor drive current, $I_{drive}$, reduces. Hence, in bulk technology, the estimated pulsewidth of propagating transient shows a gradual dependence on temperature. This increases the number of gates traversed by the propagating transient before masking [54].

In old bulk generations, the compensating relationship is not fully manifested with temperature

variations since voltage, and the technology's size dominate and control the drive current, $I_{drive}$. The compensating relationship is exposed as the technology scaling transits to advanced technology processes. Hence, the value of transistor drive current, $I_{drive}$, is determined and controlled by either threshold voltage, $V_{TH}$, or carrier mobility, $\mu$, as the temperature varies under different operating voltages, $V_{DD}$. As the temperature varies, induced transients using FinFET technology give different responses. As previously stated, planar technology shows a gradual dependence of the technology on the temperature. However, FinFET technology shows a minimal change when the temperature varies in 16-nm, and 7-nm FinFET technology nodes [11, 23]. Using 7-nm FinFET nodes, as the temperature varies, the drive current, $I_{drive}$, is not strongly shown to depend on the temperature. The compensating relationship between the carrier mobility, $\mu$, of the transistor and threshold voltage, $V_{TH}$, affects the transistor drive current, leading to the most negligible increase with temperature variations in 7-nm FinFET technology nodes. This relationship affects designs implemented using newer processes, such as 7-nm and 16-nm FinFET nodes, and has been shown in other known phenomena, such as pulse broadening in the 7-nm FinFET technology node.

### 4.2 Pulse Broadening in Combinational Circuits with Standard Logic Cell Synthesis

Broadening or widening [24] of transient pulsewidth in scaled technology is another concern as the channel distance reduces. The logic gates in scaled nanometer technologies experience propagation–induced pulse broadening [25]. Newer technologies are prone to broadening effects as they operate under higher clock frequency. The propagating transients traverse the gates and broaden, leading to unhindered propagation. Fig 4.2 shows the broadening of the transient as it traverses the chain of inverters. Pulse broadening continues to persist as the technology scales. The transient pulsewidth broadening during propagation across logic gates may satisfy the timing conditions for the latching window. However, the effect could cause an error on the storage element if transient propagation latches on the memory elements. This depends on meeting the conditions outlined in [45] as shown in Fig. 4.3. Widening of the transient pulsewidth can also trigger bipolar amplification during exposure to radiation sources [24, 45].

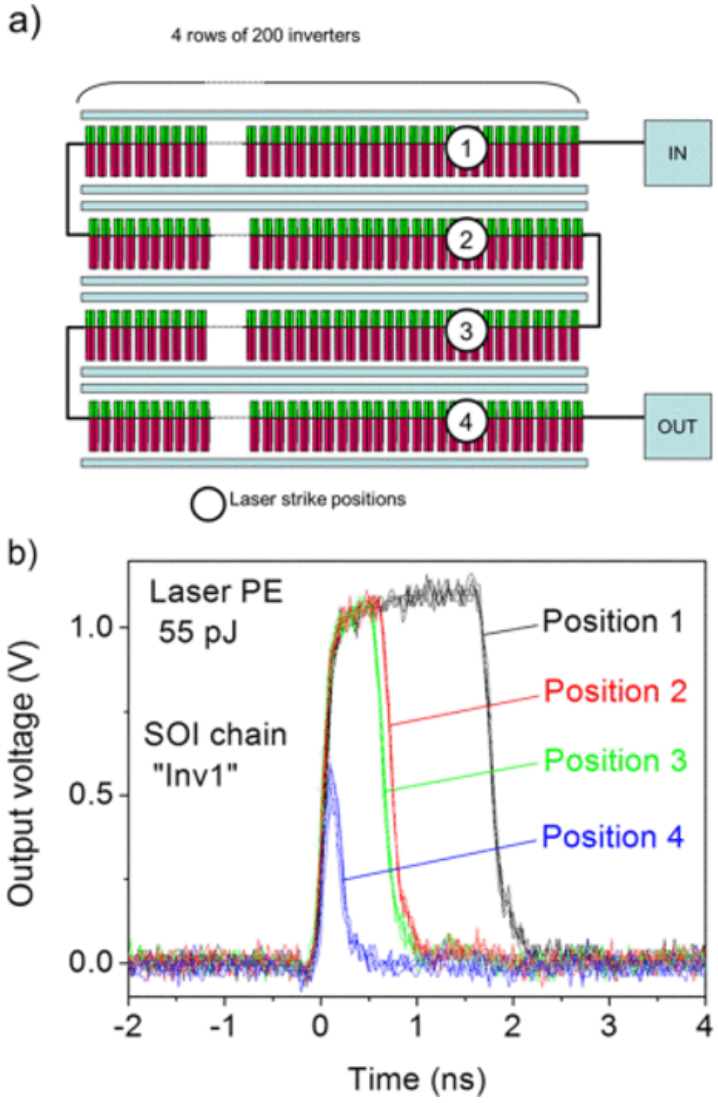



Figure 4.2: The experimental data captured when laser injection is used on the chain of the bulk inverter. SET pulse broadening as it propagates through the gates [24]

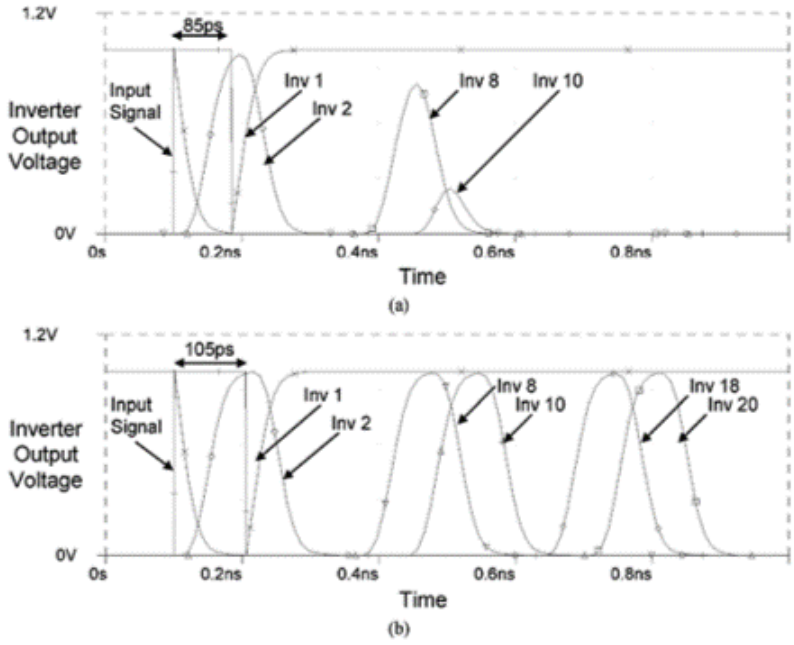



Figure 4.3: SET pulse (a) conditions not met (b) conditions are satisfied [24][45]. The SET pulse with conditions in (b) will propagate unhindered since the conditions for propagation are met.

### 4.2.1 PVT Variations on the Transient Pulses that Initially Pose no Significant Threat in Planar Technology

Since not all particles strike translate to faults [33], there are faults with no error-impacting activities. Nevertheless, these low-threat radiation-induced transients are of serious concern in the presence of PVT variations. Silent or low-threat transients are without threat because of reduced amplitude and pulsewidth under nominal cases. While the best corners mitigate such transient, the worst corners increase the amplitude and widen the pulsewidth [57]. This scenario makes a transient with no serious threat, initially masked electrically, traverse more gates due to pulse broadening [25]—the scaling and variation aid transient propagation [63] and affect the average error propagation. With sufficient amplitude and pulsewidth, the propagating transient broadens and propagates. However, the overall impact of variation and fault injection depends on the type of gates, the number of gates, the location/intensity of the particle strikes, and each gate's input vectors.

#### Methodology

This section analyzes pulse broadening due to PVT variation on transient faults with no se-

Table 4.1: EPFL benchmark circuits with the information about the reference number, number of gates, and the area of synthesized circuits

| *Circuit* | $\#Ref$[a] | $\#gates$[b] | $Area(\mu m^2)$ |
|---|---|---|---|
| Adder | 4 | 131 | 544.77 |
| Barrel shifter | 11 | 1752 | 2020.54 |
| Divisor | 68 | 31,731 | 34,880.31 |
| Log2 | 40 | 12,031 | 17,731.03 |
| Max | 22 | 2,138 | 2,248.76 |
| Multiplier | 34 | 8,660 | 14,767.26 |
| Sine | 41 | 2,292 | 3,068.84 |
| Square-root | 70 | 21,290 | 25,096.83 |
| Square | 28 | 5,917 | 10,719.80 |

[a] The number of gate references in each benchmark
[b] The number of gates after synthesis
[c] The percentage of vulnerable gates before mitigation

rious threat. The implementation procedure starts with the generation of the gate-level netlist of the *Arithmetic EPFL Combinational Benchmark Suite* [3] circuits using Synopsys Design Compiler (DC) [69]. The tool accepts the Verilog RTL netlist, design constraints, and the standard cell library as the inputs for the RTL to gate-level synthesis. Table 4.1 shows the *Arithmetic EPFL Combinational Benchmark Suite* [3] circuits used for the implementation. The logic gates of a randomly selected path were first identified using synthesized benchmark circuits. The paths from the primary input (PI) to the primary output (PO) of the gate-level netlist are arranged in ascending order of slack and then partitioned into four bins. In each bin, a path is randomly selected for simulation. Next, the gates of the randomly selected path are converted to circuit-level HSpice files. The transient pulse, modeled with a double-exponential waveform, is injected on the gates in the design [40]. Finally, each randomly selected path is simulated with and without PVT variations using the NanGate 45 nm [49] technology model.

The transient fault is modeled to give an equivalent transient pulse with an amplitude less than 15% of $V_{dd}$ to ensure that initial simulations do not lead to pulse broadening. All the gates with multiple input ports are provided with appropriate input signals to prevent logical masking. The

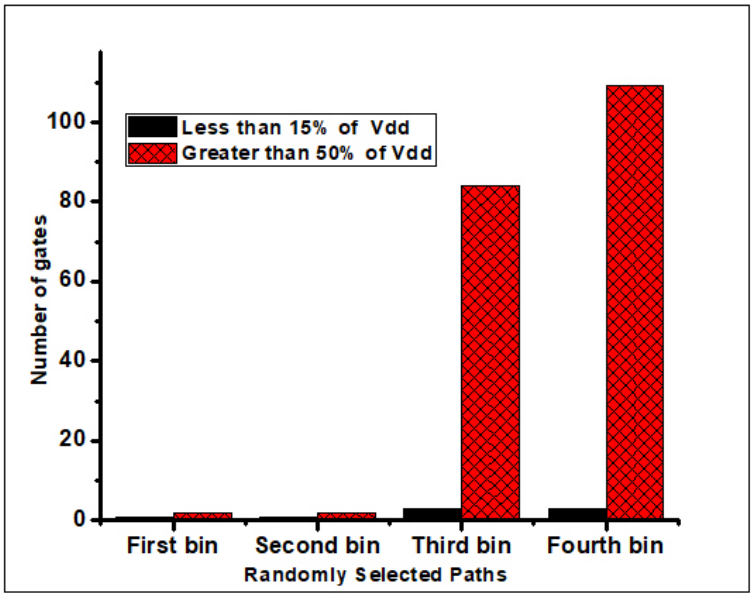



Figure 4.4: Number of gates traverses by a transient pulse in each randomly selected path when the amplitude is less than 15% of $V_{dd}$ and higher than $\frac{1}{2}V_{dd}$. The transient fault is injected on the most vulnerable gate, and the propagation is traced to either gate that masks it or to the PO.

voltage (V) variation is chosen within $\pm$15% of the nominal value, and the temperature (T) variation is from T = -20$^0C$ to T = 100$^0C$ with a step size of T = 60$^0C$. The slow (ss), nominal (tt), and fast (ff) process corners are used, respectively. The vulnerable gates are selected if the amplitude of the generated transient pulse at the output of the gate is more significant than 15% of $V_{dd}$. The gates that generate the transient pulses of high amplitude and pulsewidth are identified to mitigate the possibility of pulse broadening.

**Results and Discussions**

The *sine* circuit is used as a representative sample for the simulation. After synthesis, the gate-level netlist has 2,292 gates from 41 references (instances). Randomly selected paths in the *sine* circuit have 3, 4, 88, and 113 gates from the primary input (PI) to the primary output (PO). As shown in Fig. 4.4, the number of gates traversed by the transient pulse increases as the amplitude and pulse width increase. The observation indicates that a transient pulse with no significant propagation tendency propagated due to the effect of the worst corners of PVT variation. The plot in Fig. 4.5 shows the number of gates that experience pulse broadening at worse cases (slow corners, low

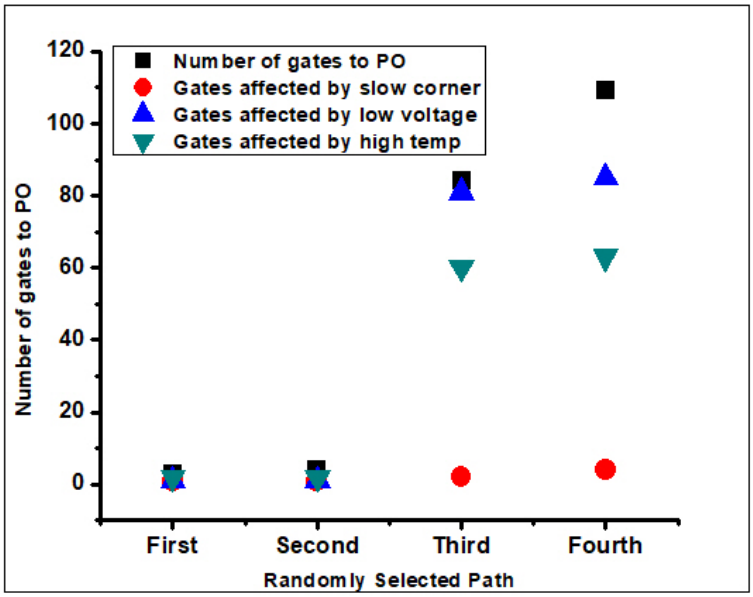



Figure 4.5: Worse cases (slow corners, low voltage, and high temperature) effect of PVT variations on vulnerable gates in selected paths of the *Sine circuit* of the EPFL benchmark suite.

voltage, and high temperature) of PVT variation in the randomly selected paths. The effects of low voltage and high temperature generate a concern for silent or low-threat transients. The results showed that the variations increase the amplitude and pulsewidth of low-threat radiation-induced transients, leading to pulse broadening. The logic gates of newer technology with less masking ability would find it difficult to stop the propagating transients.

- **Process corners**: The process variation initially affects the existing transient pulse with no significant threat. The results in *Fig. 4.5* shows the worst case of the process corner (i.e., the slow corner). The slow corner causes an increase in the number of gates as the transient pulse traverses additional gates. For instance, the slow corner (ss) increases the transient pulse amplitude of less than 15% of $V_{dd}$ by 38.5%, and the faster corner (ff) reduces it by 17.3% during propagation in a randomly selected path in the third bin. The drive current opposes the radiation-induced voltage transient under a fast process, but a slow corner causes a decrease in the drive and speed of the design. A randomly selected path within the second bin shows a 5.4% increase and 4.3% decrease for slow (ss) and faster (ff) corners, respectively. The most vulnerable gates identified, *NAND2_X1* and *NOR3_X1*, as shown in Table 4.2, show more than

Table 4.2: The digital logic gates simulated to identify the most vulnerable gates based on the resulting radiation-induced voltage waveform amplitude. The worst cases of PVT variations on the vulnerable gates in the *Sine circuit* are reported in this table.

| Gates | P (ss) | V (low) | T (high) |
|---|---|---|---|
| $BUF\_X1$ | 340 | 320 | 380 |
| $CLKBUF\_X1$ | 340 | 320 | 380 |
| $CLKBUF\_X2$ | 350 | 400 | 560 |
| $INV\_X1$ | 320 | 450 | 550 |
| $INV\_X2$ | 400 | 500 | 480 |
| $NAND2\_X1$ | 650 | 1130 | 1300 |
| $NOR2\_X1$ | 450 | 880 | 1150 |
| $NOR3\_X1$ | 890 | 950 | 1410 |
| $OR2\_X1$ | 260 | 460 | 1120 |
| $XOR2\_X1$ | 360 | 710 | 780 |

50% deviation with the slow (ss) corner.

- **Operating voltage**: The operating voltage is varied in a randomly selected path. The worst cases occur at low voltage since low voltage decreases the drive current. While increasing in voltage helps the masking ability of the gates, low voltage causes the transient pulse at the output of the subsequent gates to have significant amplitude and pulsewidth to propagate unhindered. Vulnerable gates in randomly selected paths, such as *NAND2_X1*, *NOR3_X1*, *NOR2_X1*, and *XOR2_X1*, as shown in Table 4.2, have transient with an increase in amplitude and pulsewidth with over 40% deviation with low voltage. The plot in *Fig. 4.5* shows the number of gates that experience pulse broadening at a low operating voltage, $V_{DD}$, in the randomly selected paths.

- **Temperature**: At temperature T = -20$^0C$, the effect of the resulting transient pulse is reduced, low, and masked by the next gate. Temperature affects the mobility, $\mu$, of charge carriers. When T = 40$^0C$ increases the amplitude and pulsewidth of the transient pulse, the transient pulse traverses more gates, and the situation worsens with T = 100$^0C$. The outputs at the *NAND2_X1*, *NOR3_X1*, *NOR2_X1*, and *OR2_X1* gates, as shown in Table 4.2, have wider

pulsewidths and increased amplitudes. This result causes pulse broadening as the transient pulse traverses additional gates. As shown in Fig. 4.5, the transient pulse traverses additional gates at high temperatures, broadening the transient pulse initially with reduced amplitude and pulsewidth.

## 4.3 Evaluation of the Impact of Voltage and Temperature Variations on 7-nm FinFET Technology Nodes

Impact of PVT variations in FinFET technology does not follow the same pattern as planar technology. Instead, as the FinFET technology nodes scale to 16-nm and 7-nm, the impact of PVT variation shows a slight increase [11, 23] compared to results reported under bulk technology [54].

### Methodology

In this procedure, 20 chain inverter is simulated using ASAP 7-nm Predictive PDK. The technology is simulated using typical (tt), slow (ss), and fast (ff) process corners. The simulation's voltage is similar to that reported in [23, 11]. The fault is injected, and the output of the induced voltage transient is estimated.

### Discussion of Results

The simulation results are shown in Figs. 4.7, 4.6 and 4.8. The plots show negligible differences between the technology models. As reported in [11, 23], the compensating relationship between the charge carriers and threshold voltage, $V_{TH}$, affects the transistor currents and is responsible for the negligible values. The SET has a higher amplitude at low voltage and across all the temperature variations because the mobility of charge carriers, $\mu$, reduces as the operating voltage, $V_{DD}$, reduces. Reduction in the $V_{DD}$ reduces the drive current as it affects the carrier mobility, $\mu$. The resulting transient waveform has a higher amplitude than other operating voltages in the simulation. The models show a close result across all the process corners and the temperature variation, as shown in Figs. 4.7, 4.6 and 4.8, but the impact of operating voltage, $V_{DD}$, still manifests.

## 4.4 Analysis of Pulse Broadening in 7-nm FinFET Technology Nodes

The issue of broadening continues to manifest in both the MOSFET and FinFET technology nodes, but a different pattern of pulse broadening is experienced under FinFET technology. The

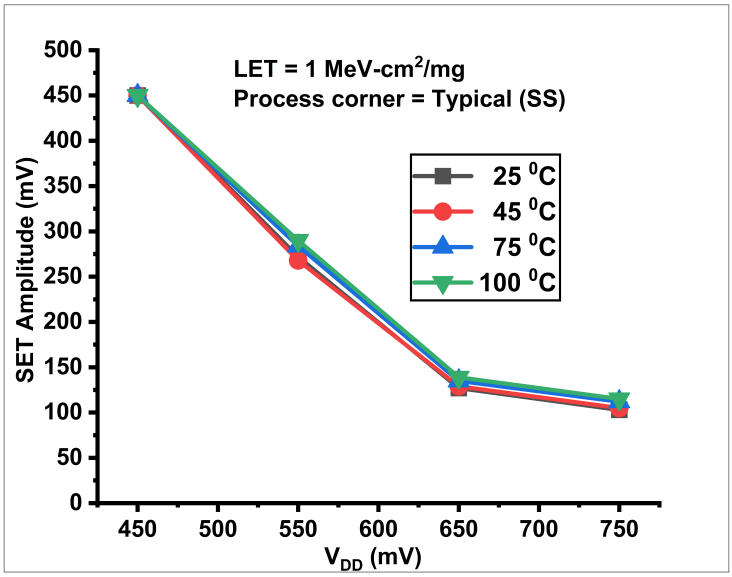



Figure 4.6: Effects of temperature variation on 7-nm FinFET with slow (ss) corner simulations. As the voltage increases, the amplitude of the propagating transient reduces. At low voltage, the amplitude increases.

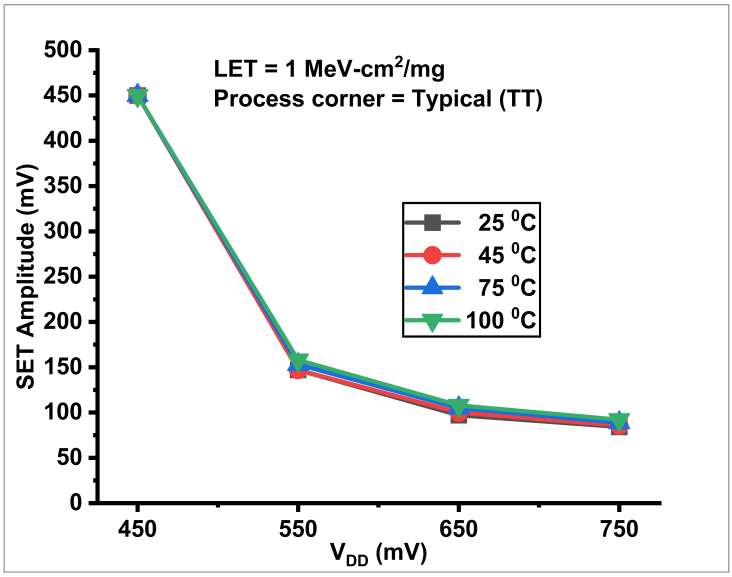



Figure 4.7: Effects of temperature variation on 7-nm FinFET with typical (tt) simulations. As the voltage increases, the amplitude of the propagating transient reduces. At low voltage, the amplitude increases.

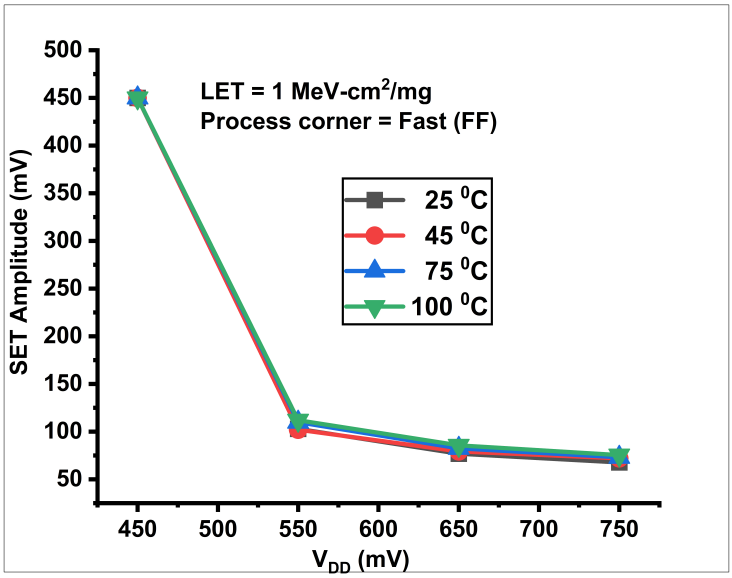



Figure 4.8: Effects of temperature variation on 7-nm FinFET with fast (ff) corner simulations. As the voltage increases, the amplitude of the propagating transient reduces. At low voltage, the amplitude increases.

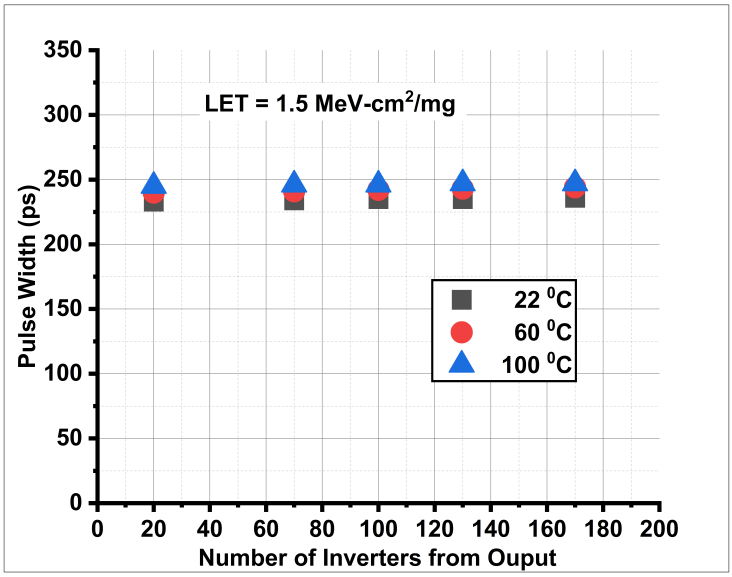



Figure 4.9: Estimated SET pulse width in 7-nm as a function of temperature at $V_{DD}$ = 500 mV. There are the least values as the temperature varies.

compensating relationship also affects the broadening effect in a chain of inverters implemented using FinFET technologies. The simulation task designed 200-chain inverters using 7-nm FinFET technology nodes and injected them at different locations, and output SET was measured and plotted against the injected location to the chain's output. The fault injection has the same delay to ensure that the same simulation condition is used for all the injected locations. The duty cycle for the simulation is 2 *ns*, the fault injection delay is 0.8 *ns*, and the simulation time is 10 *ns*. The estimated LET used is 5.26 MeV-cm$^2$/mg.

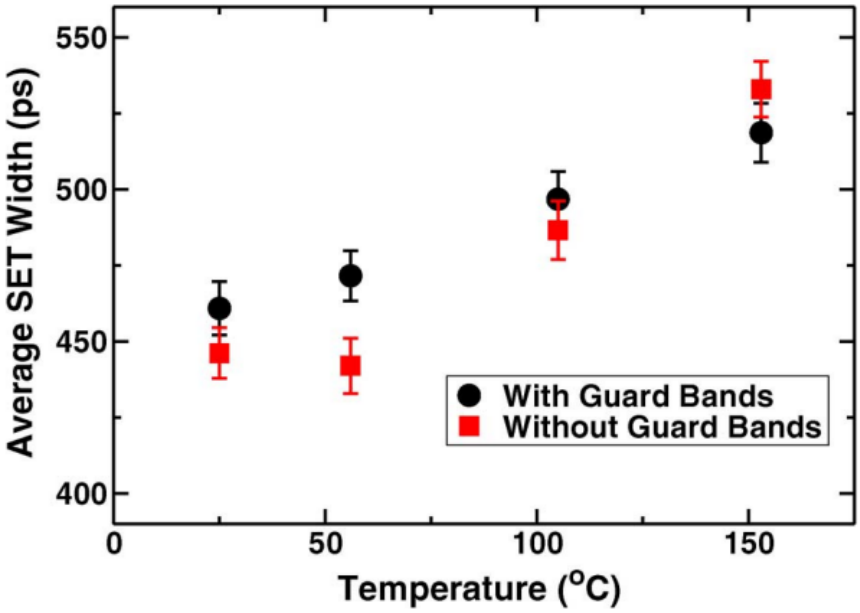
As shown in Fig. 4.9, the propagating transient pulsewidth has a low and minimal increase as the number of inverters estimated from the output of the chain changes. However, the estimated pulsewidth is so close that the difference between the pulsewidth of the first and last inverter is a single-digit difference. For instance, as shown in Fig. 4.9, the estimated percentage difference between the pulsewidth of the first and last inverter in the chain at 22 °C, 60 °C, and 100 °C is approximately 1.3%, 1.7%, and 0.82%, respectively. This results from compensating relationship between carrier mobility, $\mu$, and threshold voltage, $V_{TH}$, as the temperature varies [11, 23]. The pattern differs from reported data for bulk [24] and FDSOI technologies [27].

## 4.5 Validation of Simulation Results With the Experimental Data - Estimation of Pulsewidth due Elevated Temperature

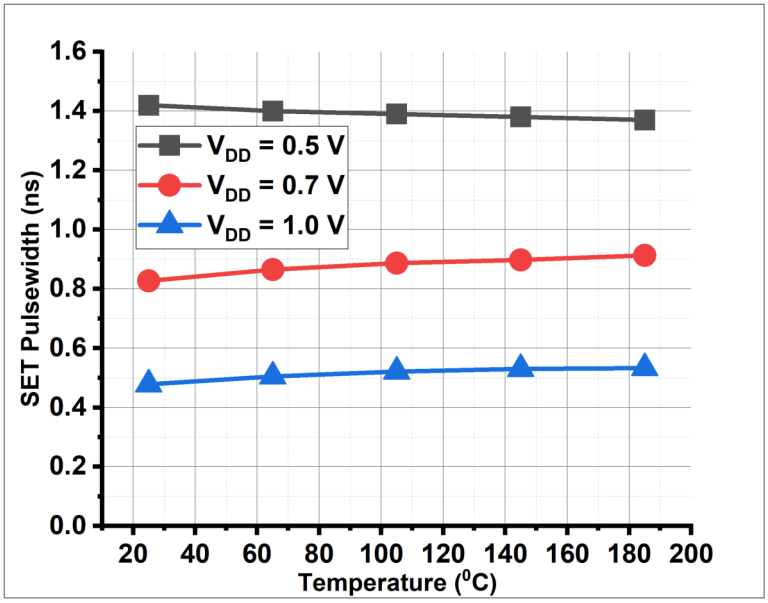
The research activities in this section were conducted to determine the correlation between the simulation results and the experimental data. In addition, the simulation results were compared to experimental data presented in [27] to validate the technology for the simulation activities.

### 4.5.1 Design Approach

To validate the technology with previously published data, a chain of 200 inverters was designed using the 7-nm FinFET technology node. The simulation task injected fault at Stage 189 to assess the impact of the fault injection as the propagating transient traverse the chain of inverters. The SET was measured at the output of the chain of inverters and plotted against the different elevated temperatures. The simulation activities used the details stated with Eq. 2.2. The duty cycle for the simulation is 2 *ns*, the fault injection delay is 0.8 *ns*, and the simulation time is 10 *ns*. The estimated LET used is 5.26 MeV-cm$^2$/mg. The simulated results were validated with the experimental data




(a)




(b)

Figure 4.10: (a) Elevated temperature heavy-ion testing of bulk 130-nm test circuits [27]. The experimental data show that the average SET pulsewidth increases as the elevated temperature increases for the test circuit without guard bands. (b) Estimated SET pulsewidth with elevated temperature using 7-nm. At $V_{DD}$ = 0.5 V, the pulsewidth reduces as the temperature increases. But there is an increase in pulsewidth with an elevated temperature at $V_{DD}$ = 0.7 V and $V_{DD}$ = 1.0 V.

reported. The experimental data involved heavy-ion testing of bulk 130-nm test circuits [27].

### 4.5.2 Discussion of Results

With and without guard bands in Fig. 4.10 (a), the average pulsewidth increases as the temperature increases in four measurements when 130-nm bulk test circuits are exposed to Krypton ions with LET of 30.9 MeV-cm$^2$/mg [27]. However, in Fig. 4.10 (b), at $V_{DD}$ = 0.5 V, the estimated pulsewidth reduces as the temperature increases. Low $V_{DD}$ leads to a low drive current, $I_{drive}$. When the temperature increases, mobility, $V_{TH}$, reduces, and the threshold voltage, $V_{TH}$, reduces. These compensating relationships lead to induced transients with a reduced or high amplitude and pulsewidth since the resulting drive current from the relationship is lower than an induced transient current.

When $V_{DD}$ increases to 0.7 V and 1.0 V, respectively, the pulsewidth increases as the temperature increases. An increase in operating voltage, $V_{DD}$, increases the drive current, $I_{drive}$. However, an increase in temperature reduces the carrier mobility, $\mu$, and the drive current, $I_{drive}$. In this case, the drive current due to carrier mobility, $\mu$, dictates the overall drive current, $I_{drive}$, from the compensating relationship between carrier mobility, $\mu$, and threshold voltage, $V_{TH}$. Hence, since an increase in temperature affects the charge carriers' mobility, $\mu$, the estimated pulsewidth of the induced transient increases, as shown in Fig. 4.10 (b). The changes in the estimated pulsewidth of induced transient are insignificant compared to the experimental data reported in [27]. This results from the compensating relationship between the carrier mobility, $\mu$, and threshold voltage, $V_{TH}$, similar to experimental data reported for 16-nm and 7-nm FinFET technologies in [11, 23]. The estimated transient has a smaller increase as the value of temperature increases. Only estimated results at $V_{DD}$ = 0.7 V and $V_{DD}$ = 1.0 V show a similar trend as the reported experimental data in [27].

## 4.6 Chapter Summary

The impact of PVT variations cannot be neglected as the effect of scaling continues to manifest in designed-related parameters. Radiation-induced transient with reduced amplitude and pulsewidth broadens when the worst cases of PVT variation are included in the simulation cases. The effect of PVT variations on vulnerable gates with transient faults (with no severe threat) increases the amplitude and pulsewidth of the transient pulse. It broadens and traverses more gates toward the

primary output (PO). The pulse broadening also happens in FinFET technology nodes. The impact of scaling exposed the hidden impact of temperature on compensating relationship between the mobility of charge carriers, $\mu$, and the threshold voltage, $V_{TH}$, of the transistor. The relationship gives a pulse broadening effect with a minimal difference in pulsewidth of the propagating transient as it traverses the chain of inverters. Also, the compensating relationship leads to an insignificant value as the temperature varies in the pulsewidth of the propagating transient under elevated temperature.

# CHAPTER 5

# THE IMPACT OF ADVANCED TECHNOLOGIES ON SRAM DESIGN

FinFET technologies have a better electrical performance than planar MOSFET technology models. SRAMs implemented using FinFET technologies show a reduced soft error rate (SER) due to a reduction in the sensitive volume of the designs [34, 50] with a reduced charge collection efficiency [52]. The reduction in the sensitive volume causes a substantial decrease in the collected charge, leading to a reduced estimated threshold linear energy transfer (LET) in FinFET designs [34]. Even with design benefits and electrostatic channel control with better reliability than a planar node [53], FinFET technologies have new reliability-related issues due to technology scaling [50]. Per-bit SER increases as the FinFET technology scales down to 5 nm. Since the critical charge of a storing node reduces as the technology scales, SRAM memory cells implemented in the newest advanced technologies would be vulnerable to radiation-induced upsets. The equation of critical charge [39] of the sensitive node is expressed as:

$$Q_{crit} = C_N.V_{DD} + I_{DP}.T_F \tag{5.1}$$

where $C_N$ is the capacitance of the storage node, $V_{DD}$ is the operating voltage, $I_{DP}$ is the drain current of the PFET, and $T_F$ is the flipping time of the cell. The parameters in this equation have a direct and indirect relationship with scaling. Thus, the critical charge and operating voltage follow the same trend as the nodal capacitance. As a result, they all reduce with scaling.

## 5.1 SRAM Cell

A typical SRAM cell is a six-transistor (6-T) cell with two cross-coupled inverters with two NMOS cells as access transistors, as shown in Fig. 5.1. The two access transistors are controlled by wordline, WL, and connected to bitline, *BL*, and its complement, *BLB*. Conventional 6-T SRAM operation includes read, write, and hold. Each operation depends on the status of the bitline, *BL/BLB* and wordline, *WL*. A bit is written into the storing node, *Q/QB* by driving either bitline, *BL/BLB*, to $V_{DD}$ and then precharge the wordline, *WL*, to $V_{DD}$. A read operation is done by precharging both bitlines, *BL/BLB*, to $V_{DD}$ while wordline, *WL*, ramps up to $V_{DD}$. Static Noise Margin (SNM) eval-

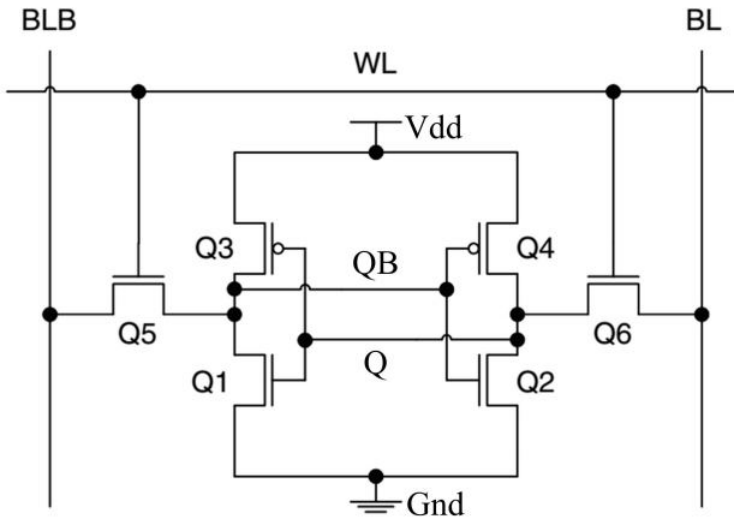



Figure 5.1: The schematic of a conventional six-transistor (6T) SRAM cell.

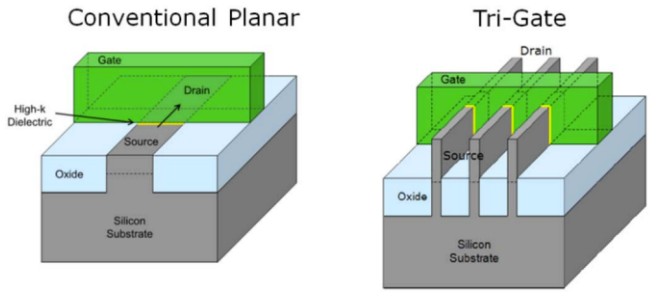



Figure 5.2: Structure of conventional planar technology and multi-fin FinFET technology [65]. The FinFET has a less sensitive volume compared to planar technology.

uates the stability of the SRAM cell. SNM measures the minimum noise voltage necessary to flip the cell state at each storing node. The operating voltage, size of the gates, and types of technology influence SNM. The higher the SNM, the better the SRAM [77]. Write and read operations must be stable enough to avoid flipping the stored bits. This is prevented by appropriately sizing the access, pull-up, and pull-down transistors to avoid metastability. For instance, during the read operation, the cell ratio $\frac{Q1}{Q5} \ggg 1$. The ratio prevents the storing node, $QB$, from flipping the stored bit. Also, sizing of Q5 and Q3 during write operations must be $\frac{Q5}{Q3} \gg 1$ for writability and suppressing the impact of the feedback inverter [75].

### 5.1.1 Single-Event Upset (SEU) in SRAM Cell

A single-event upset (SEU) occurs in an SRAM cell when the radiation-induced collected charge from the deposited charge flips the stored bit on the sensitive node [43]. As technology scales and impacts the design size, the quantity of charge needed to flip a storing bit decreases. In a sensitive design like SRAM implemented in advanced nodes, such as FinFET technologies, only a fraction of the deposited charge, compared to the older designs, is required to flip the stored bit in a sensitive node. The ability of the sensitive node to recover or suppress the radiation-induced transient depends on factors such as the type of technology, the critical charge, the operating voltage, and the quantity of charge collected from the deposited charge. SRAM cell has active feedback with the back-to-back inverters. When a radiation particle strikes the sensitive node, it affects the reverse-biased drain junction of the "OFF" NMOS transistor, $Q2$, resulting in a transient current due to the charge collected by the node. The induced current will be countered and potentially restored by finite current from the "ON" PMOS cell, $Q4$. The voltage drop at the restoring transistor drain results in a transient that upsets the sensitive node. Since the SRAM cell is significantly impacted by scaling, RC delay, which determines the amplitude of induced transient voltage, also reduces [58]. Due to the sensitivity of the storing node, a slight increase in the induced collected charge from the deposited charge can cause the node to lose its recovering potential, i.e., the ability to minimize the amplitude of induced voltage transient (Fig. 5.3) [43].

The recovery time depends on the cell write time in the $RC$ delay, and the value dictates the SRAM SEU sensitivity. The smaller the RC delay, the faster the SRAM responds to the upset and the higher the probability of the SRAM being vulnerable to SEU [58]. Since scaling dictates the

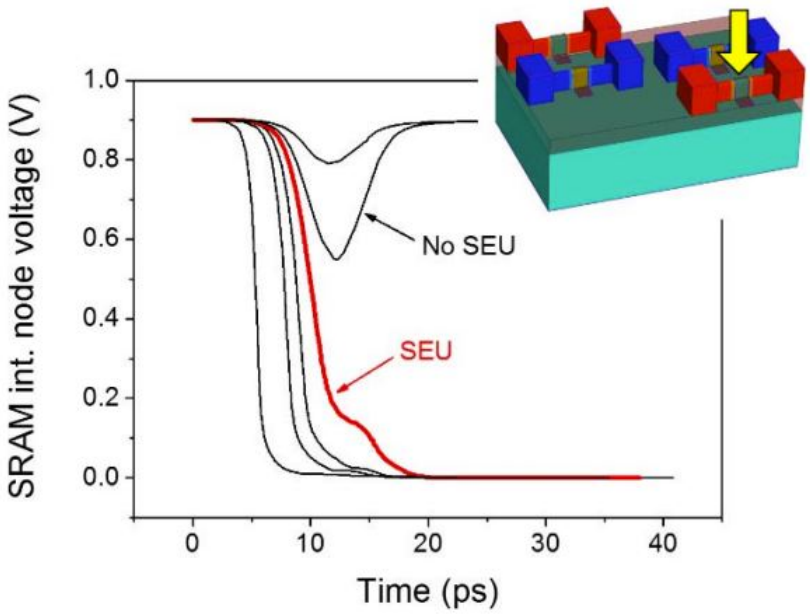



Figure 5.3: Cases of ”No SEU” and ”SEU.” The node with ”No SEU” recovers with no upset, while the plot with ”SEU” fails to recover [43]. Recovery ability reduces as the technology scales.

size of the technology, the RC delay reduces, and the recovery potential differs from technology to technology. The recovery limit can be described as the maximum amplitude of induced transient caused by the deposited charge that the SRAM cell recovers or suppresses without an upset. For example, Fig. 5.3 shows a storage node with cases of a single event upset (SEU) when the node fails to overcome the radiation-induced voltage transient due to a substantial collected charge from the deposited charge. The plot labeled ”No SEU” indicates that the node recovers since the radiation-induced voltage transient from the collected charge is still within the sensitive node’s recovery limit. In this case, the difference between the ”No SEU” and ”SEU” depends on the quantity of charge collected from the deposited charge and the critical charge of the storing node. When the collected charge from the deposited charge is higher than the critical charge ($Q_{dep}$) of a node, the node flips to cause SEU [43].

## 5.2 Simulation of the Impact of Scaling on Noise Margin, Threshold LET, and Critical Charge of an SRAM Cell

The memory cell’s static noise margin (SNM) values at different voltages and technology are simulated and estimated for reading and writing operations. SNM is a function of voltage and tech-

nology. Each back-to-back inverter remains in either logic-1 or logic-0 stable states. The transfer characteristics curve, known as the "butterfly curve," is used to describe the stable states of the cell. To ensure the conditions for writability and readability, sizing of the access ($Q1$), pull-up ($Q3$), and pull-down ($Q5$) transistors is 3:1:4.

### 5.2.1 Simulation Approach

The ionizing particle strikes on silicon technology cause the creation of electron-hole pairs that lead to the generation of a transient voltage. The amount of charge deposited depends on the LET, which determines the energy loss rate to the generated electron-hole pair during particle strikes. The conversion between LET of the ion and charge deposition per unit of path length through the device is provided by Massengill in [44]. The sensitive node is injected using the double exponential current waveform with Eq. 2.2. A double exponential current waveform is used for modeling the radiation-induced transient. In this simulation, the rise time, $\tau_r$, is 0.5 $ps$ and the fall time time, $\tau_f$, is 70 $ps$ chosen after data in [35]. The double-exponential fault modeling is injected into the storing node during the read operation. Both bitlines are precharged to $V_{dd}$, and the wordline ramps up to $V_{dd}$. Finally, one bitline goes to the ground, and the other remains at $V_{dd}$ equivalent to logic-1. The upset limit was chosen where the radiation-induced voltage transient is more than $\frac{1}{2}V_{DD}$. In this simulation, each technology is simulated with different values of $I_{SET}$ since the design of the technologies has different critical charges with separate RC delays. Therefore, the maximum voltage at which the storing node recovers the impact of the collected charge from the deposited charge is obtained by parametrically varying $Q_{dep}$, and the equivalent threshold LET is estimated. The effect of voltage on the critical charge of the designs is compared to the experimental data presented in [65]. The simulation activities were performed using HSpice version Q-2020.03 [70] on a CentOS Linux64 server. $W/L = 10\ nm/15\ nm$ is used for $W/L$ of 15-nm, and $W/L = 27\ nm/20\ nm$ for nFET and pFET of 7-nm.

### 5.2.2 Discussion of Results

The results of the noise margin, the threshold LET, the impact of scaling on charges (collected and deposited), and SER are discussed in this section.

- **Noise Margin (NM)**: Fig. 5.4 shows the Write Noise Margin (WNM) for both 7-nm and

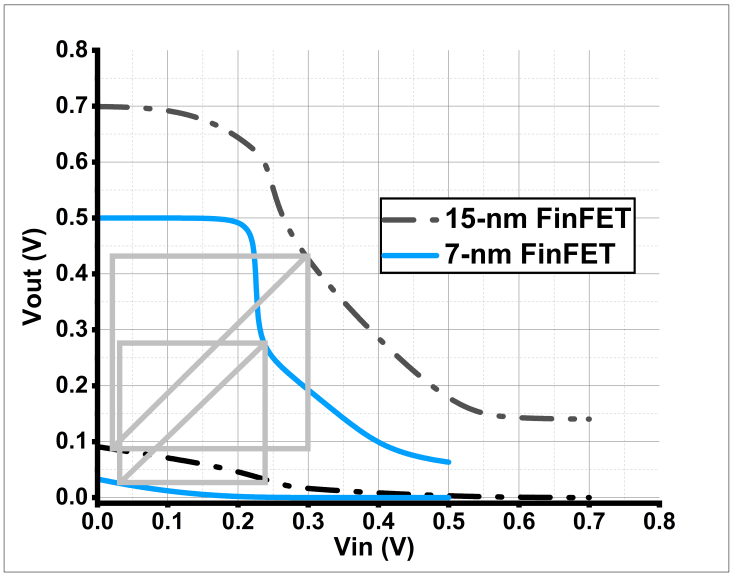



Figure 5.4: Write Noise Margin (WNM) of 7-nm FinFET and 15-nm FinFET estimated at 700 mV and 500 mV, respectively. The 7-nm FinFET has lower WNM as the technology scales from 15-nm to 7-nm.

15-nm technologies. The value of WNM is 280 $mV$ for 7 nm and 390 $mV$ for 15 nm, which is a 28.2% reduction. Also, as shown in Fig. 5.5, to estimate the impact of voltage on the SNM, 15-nm simulated at 500 $mV$ and 700 $mV$ show that SNM reduces. It shows approximately 20% from 15-nm to 7-nm FinFET technologies as the voltage reduces. The simulated results align with results in [77], which show that SNM at the different hold stage voltages reduces as voltage reduces. As shown in both Figs., SNM and WNM are voltage functions influenced by technology scaling. Since SNM determines the stability of the SRAM cell, the higher the SNM, the better the SRAM exhibits tolerance to upsets. The greater the perimeter of the square, the stronger the SNM, contributing to the overall SRAM performance.

- **Threshold LET and the impact of particle LET**: The storing node recovers from the deposited charge without an upset if the resulting transient is within the recoverable region of the storing node. For this analysis, any radiation-induced voltage transient less than $\frac{1}{2}V_{DD}$ was selected as recoverable, and any value higher than $\frac{1}{2}V_{DD}$ was selected as an upset. The maximum deposited charge with successful recovery without an upset is shown in Fig. 5.6. This is used to estimate the threshold LET. Since the sensitive volume differs in each tech-

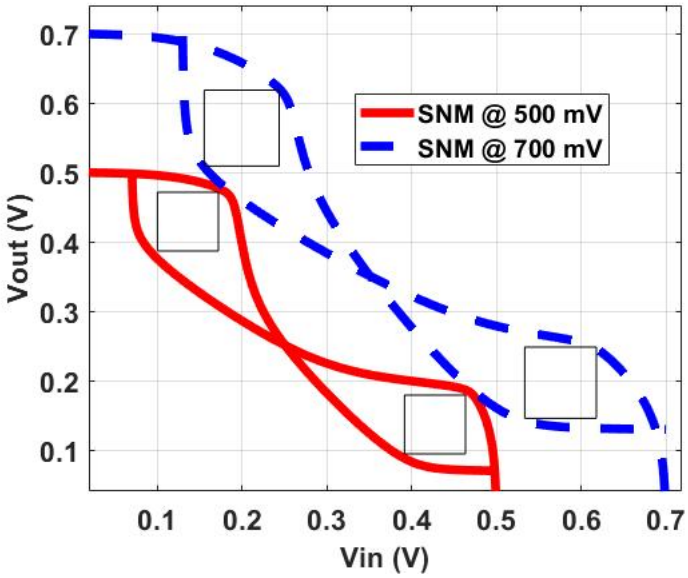



Figure 5.5: SRAM Read Static Noise Margin (SNM) of 15-nm FinFET simulated at 500 mV and 700 mV to show the impact of voltage. A larger SNM provides better read stability of the SRAM cell. The SNM is 150 mV in 15-nm FinFET with 0.7 V and 120 mV at 0.5 V, respectively.

nology, the threshold LET differs, as shown in Fig. 5.6. Since the diffusion area of FinFET 7-nm is lesser than 15-nm, the 7-nm has a lesser value of threshold LET, and the amount of the charges to be collected is proportional to the sensitive volume of the designs. The 15-nm FinFET design has a threshold LET of 5.92 times that of the 7-nm FinFET design at 0.75 V. It indicates that 15-nm will collect more charges. The simulation results are estimated when each technology's design successfully recovers from the transient voltage without an upset.

- **Impact of Critical Charge and Deposited Charge**: The critical charge reduces as the technology scales with the nominal operating voltage. The estimated values in this simulation are 0.035 $fC$ for 7-nm FinFET and 0.82 $fC$ for 15-nm FinFET. These values are the minimum estimated value on all the nodes within the sensitive regions of the SRAM cell when the nodes are injected with a fault with no upset. The values are compared to the experimental data reported in [65]. The simulation results show a similar reducing critical charge and voltage pattern as the technology scales. Also, the results published in [50] show that the critical charge reduces as the technology scales from 7 nm to 5 nm, decreasing the per-bit SER from 7 nm to 5-nm FinFET process. As estimated, the critical charge of 7 nm is lower than 15 nm,

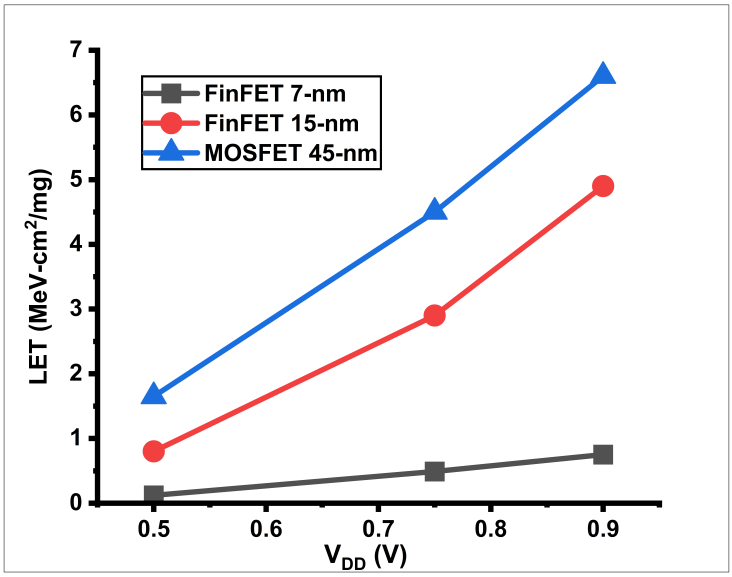



Figure 5.6: Estimated maximum threshold LET with no upset recorded as the radiation-induced transient remains less than $\frac{1}{2}V_{DD}$. The value of LET was estimated based on the Massengill equation in 2.1. The threshold LET at 15 nm is an average of 6.30 times of threshold LET at 7 nm. It is highest at 45-nm due to its sensitive volume.

and exposing both to the same radiation sources yields different responses. The simulation results show that both technologies have reduced and different critical charges ($Q_{crit}$).

The estimated threshold LET for 7-nm and 15-nm FinFETs are shown in Fig. 5.6. The minimum threshold LET occurs at 500 mV and is estimated as 0.19 MeV-cm$^2$/mg (0.0020 $pC/\mu m$ of deposited charge) for 7-nm and 0.80 MeV-cm$^2$/mg (0.008 $pC/\mu m$ of deposited charge) for 15-nm. A low critical charge in 7-nm is assumed responsible for the low threshold LET. As the voltage increases from 500 mV to 900 mV, there is a gradual increase in the threshold LET. The simulation results show that the quantity of deposited charge is determined by the type of technology since the technologies, in most cases, have different sensitive volumes.

## 5.3 Validation of Simulation Results with Experimental Data - Estimation of SER Using a Model-Based Approach

The following simulation results are compared to experimental data presented in [50]. When

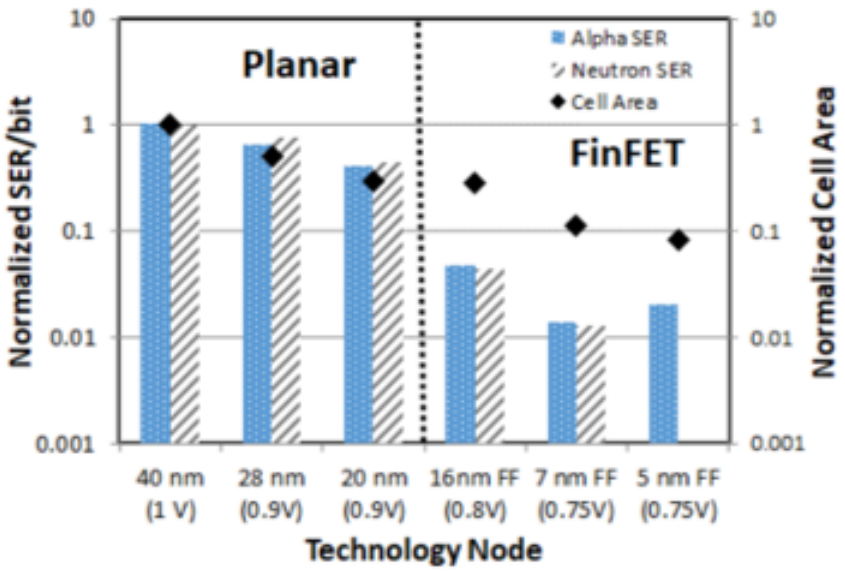
validated with the experimental data, the modeling process can be used for additional analysis of similar technologies without the expense of laser beam or heavy ion testing. The dissertation evaluates SRAM cells' vulnerability to single-event upsets (SEUs) using the NCSU FreePDK 15-nm and the ASAP 7-nm Predictive PDK models. The research activities were used to determine the correlation between the simulation results and the published experimental data. The amount of the collected charges differ from technology to technology, impacting the SER. Since a single term cannot be used to conclude the vulnerability of the SRAM cell, the most common approach is to estimate the SER using Eq. (2.3). The model was simulated with the voltage range (0.50 V to 1.0 V) selected based on the experimental data used for validation.

### 5.3.1 Design Approach

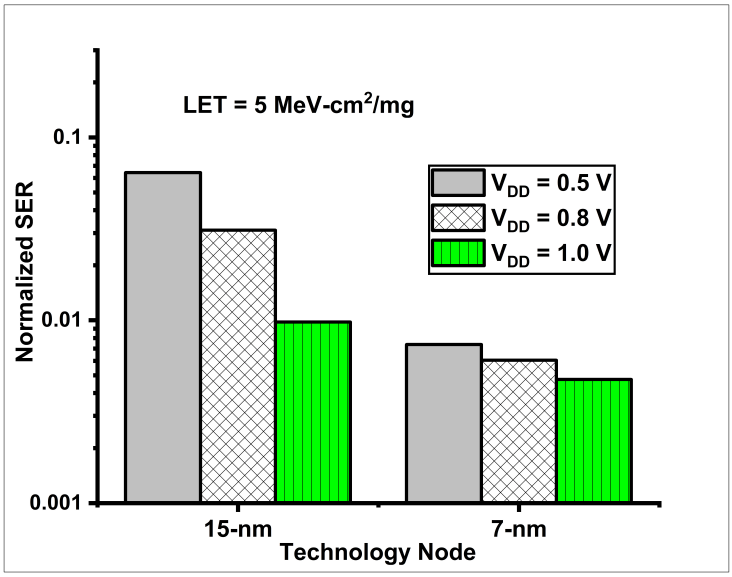
SER is a good metric for estimating the vulnerability of the SRAM designs. SER depends on the critical charge ($Q_{crit}$), collected charge ($Q_{coll}$), and diffusion area ($A_{diff}$) of the technology as shown in Eq. (2.3). Although the circuit simulation alone cannot accurately estimate the collection charge ($Q_{coll}$), such information can be sourced from available experimental data. The estimated value of the deposited charge ($Q_{dep}$), a constant diffusion area ($A_{diff}$) of the technology from the PDK, and the extraction of either charge collection efficiency or collection charge from the experimental data will give sufficient information to make a valid judgment about the vulnerability of the SRAM. This validation process estimates SER based on the published experimental data [48]. The information is used to quantify the collected charge for each FinFET technology used for the simulation. The experimental data shows that the average charge collection efficiency is 34%. It means an average of 34% of the total charge deposited is collected. The diffusion areas are obtained from the PDK information of each technology [16, 51]. Then, using Eq. 2.3, the SER was estimated and plotted in a logarithmic scale in Fig. 5.7 (b) and compared to the experimental data shown in Fig. 5.7 (a).

### 5.3.2 Discussion of Results

Due to scaling, SRAM cells designed and fabricated in advanced technologies such as 7-nm and 15-nm technology processes have reduced critical node capacitances and are vulnerable to radiation sources because of the cell's corresponding critical charge. Also, the scaling reduces the diffusion area of the technology. As a result, 7-nm has a reduced diffusion area and causes the technology to




(a)




(b)

Figure 5.7: (a) Normalized scaling trends in the per-bit alpha and neutron SER of SRAMs as a function of technology node [50]. The experimental data of 16-nm and 7-nm is the focus for comparing the SER. (b) Estimated Soft Error Rate (SER) for the SRAM implemented with 7-nm and 15-nm technologies. 15-nm FinFET technology is more vulnerable than 7-nm FinFET technology.

collect less quantity of the deposited charge. Therefore, 7-nm has a low SER overall. Fig. Fig. 5.7 (b) shows that 15-nm is more vulnerable to upset when compared to 7-nm. The experimental data of 16-nm and 7-nm in Fig. 5.7 (a) are the main focus for comparing the SER. As shown, the SER decreases from 16-nm to 7-nm FinFET generations [50]. Though the estimated SER between the two technologies may not be quantitatively close to the experimental data, factors such as simulation and fault-injection setup may lead to these differences. However, the estimated SER shows a similar pattern as the experimental data.

## 5.4 Chapter Summary

The impact of technology scaling also affects a sensitive memory cell such as SRAM. This chapter presents simulation activities to assess the impact of technology scaling on SNM; threshold LET, and critical charge of SRAM cells. The simulation activities analyzed the SER of the SRAM cells and compared it to previously published experimental data. Although FinFET 7-nm generated an induced waveform with higher amplitude under the same voltage and LET, the FinFET 15-nm has a higher vulnerability regarding threshold LET and the estimated SER, which align with experimental data used in this study. In addition, 7-nm FinFET has a lower threshold LET, which can be traced back to the reduced sensitive volume created by scaling. The modeling procedures estimate the SER of FinFET technologies without the expense of laser beam or heavy ion testing.

# CHAPTER 6

# MITIGATION TECHNIQUES FOR MINIMIZING OR ELIMINATING THE RADIATION-INDUCED TRANSIENTS

In the era of nanometer technologies, the design created with advanced silicon technology needs an appropriate mitigation approach to perform the intended function without losing its integrity. The reliability of integrated circuits (ICs) has become a significant concern in computing systems' development as the technology scales. Mitigation techniques minimize or eliminate the reliability issue created by particle strikes (fault injection) and PVT variation, as well as those caused due to scaling. The worst cases of process, voltage, and temperature (PVT) variations increase the vulnerability of the designs to soft errors. Considering the effects of variation helps to model a fault-tolerant design that mitigates or minimizes the effect of the worst corners of variation on the reliability issues created by particle strikes (fault injection). Therefore, a fault- and variation-tolerant design that can operate in the presence of PVT variations without losing the design's integrity must be a priority.

## 6.1 Approaches to Mitigate Propagating Transients

Over the years, different mitigation techniques have been proposed and implemented to mitigate a propagating radiation-induced transient. The mitigation techniques implemented under the following methods minimize the properties of the propagating transient:

1. Standard Cells Strength Approach
2. Selective Hardening Approach, and
3. Layout Placement Approach

### 6.1.1 Standard Cell Strength Approach

The standard cell strength approach increases the individual logic gates' capacitance to increase the design's resilience. Though the properties of the propagating transient are mitigated, this approach incurs a penalty. Propagating radiation-induced transients can be eliminated when the

vulnerable cells that generate transient of increased amplitude and pulsewidth are replaced [41] and when the individual cells are hardened [62]. Employing a hardening-by-design technique to develop a radiation-hardened design using guard gates [6] also weakened the propagating transient. In addition, sizing the gates and carefully selecting the gate dimensions [41, 85] increases the electrical masking of the logic gates. Finally, temporal, spatial, and triple modular redundancy (TMR) [73] techniques provide mitigation against soft errors with an increase in logic strength and density. All these implementations reduce the transient propagation and help the design's robustness. However, since the individual gates are hardened with an additional gate that increases the number of logic nodes, the implementations lead to an increase in power and area penalty.

### 6.1.2 Selective Hardening Approach

The selective hardening approach has an advantage over the standard cells strength technique. While only vulnerable gates are selected for mitigation in the former, individual gates are selected and hardened in the latter. The approach generally involves adopting a path by focusing on the vulnerable gates. When the vulnerable cells are identified and replaced with alternative cells or logical functions of higher strength, the vulnerability of the logic gates of the circuit reduces [41]. In addition, the overall transient impact reduces since the properties of the propagating transient reduce. Srinivasan *et al.* [68] presented hardening of the datapath by identifying the sensitive nodes. The elected paths are chosen based on a pre-defined design metric to create the radiation-hardened design. Since only vulnerable gates are selected for mitigation, the approach has a reduced penalty in power and area compared to the standard cells strength technique.

### 6.1.3 Layout Placement Approach

The layout placement approach focuses on reducing the sensitive volume (SV) since it is an area impacted by particle strikes. Different implementations indicate that the effects of propagating transients can be mitigated using the layout approach. The pulse quenching approach uses layout [5, 21] approach to lessen the pulsewidth based on the reduction in a sensitive area. The technique ensures that the impact of propagating transients is reduced or mitigated. Kiddie et al. [36] used alternative standard cell placement methods to mitigate Single-Event Multiple-Transients (SEMT). The work increases the reliability of the design through charge-sharing techniques to minimize the

transient. The author in [22] used a layout approach to identify vulnerable adjacent cells and increase their physical distance without imposing any area or performance penalty. Layout mitigation techniques such as P-hit and N-hit SET also weaken the transient pulse width [14]. A transistor folding mechanism [81] can be explored, as well, as a mitigation strategy for reducing SRAM SEU vulnerability. The layout approach has an advantage over the standard cell, and selective path approaches. While many implementations under layout techniques are without penalty, standard cells and selective approaches incur penalties. It resolves issues around cost and reliability.

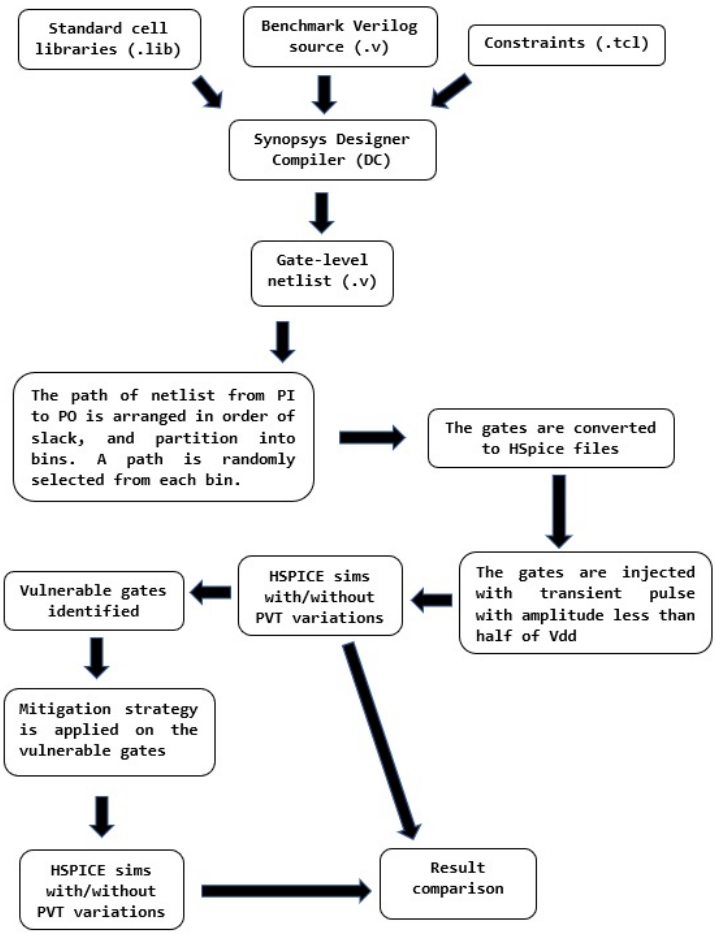



Figure 6.1: The ASIC flow for generating gate-level netlist from standard library cells, EPFL benchmark verilog cells, and the constraint files. The vulnerable gates are identified and mitigated along randomly selected paths in EPFL benchmark circuits using the HSpice simulation.

## 6.2 Improvement of Masking Ability of Logical Gates Using 45nm Bulk Technology

Suppressing the impact of the worst corners of PVT variation may be a suitable mitigation strat-

egy. It is necessary to prevent design failure caused by the worst cases of variation. For example, in [42], a self-adjusting mechanism that involves the dynamic configuration of the delays of adjustable delay buffers (ADBs) is used to reduce the effect of PVT variations on clock skew. Also, the robustness evaluation of a FinFET technology [86] showed the effect of PVT variations on the OFF current. This work's mitigation approach focuses on standard cell drive and selective hardening techniques.

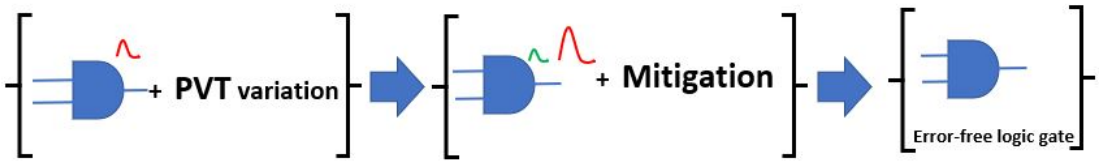



Figure 6.2: The flow to obtain an error-free logic gate. An error-free logic gate is free from the impact of both radiation-induced transient and PVT variation. The selection and hardening of an individual gate to create an error-free logic gate lead to overhead costs in terms of area and power.

This section discusses the effects of worst corners of PVT variations on vulnerable gates with propagating transient pulses and on those that initially pose no significant threat. The Synopsys Design Compiler (DC) [69] was used to synthesize the 74182 (carry look-ahead (CLA)) and selected arithmetic benchmark circuits from the EPFL benchmark suite [3] to generate the gate-level netlist. The synthesis tool requires a Verilog netlist of the benchmark, design constraints, and the standard cell library. Finally, the gate-level netlists were translated to circuit-level HSPICE descriptions for simulations. The simulation analysis uses Synopsys HSPICE [70] and NanGate 45-nm technology models [49]. In addition, a double-exponential waveform [54] in Eq. 2.2 is used for modeling the faults to analyze:

1. Mitigation of Pulse Broadening Amplified by PVT Variations

2. Electrical Masking Improvement with Standard Logic Cell Synthesis

### 6.2.1 Mitigation of Pulse Broadening Amplified by PVT Variations

As the technology scales, the node capacitance reduces. Hence the critical charge of the logical node reduces. Scaling leads to design improvement in electronic design's power, area, and speed but causes reliability concerns in newer technologies. For example, different bulk technology nodes

Table 6.1: Worst cases of PVT variations on the vulnerable gates in the *Sine circuit* using 45nm bulk technology. Vulnerable gates aid the propagation of radiation-induced transient by increasing the properties of the propagating transient.

| | **Before mitigation (mV)** | | | **After mitigation (mV)(%)** | | |
|---|---|---|---|---|---|---|
| Gates | P (ss) | V (low) | T (high) | P (ss) | V (low) | T (high) |
| $BUF\_X1$ | 340 | 320 | 380 | 79 (76.8) | 59 (81.6) | 71 (81.3) |
| $CLKBUF\_X1$ | 340 | 320 | 380 | 79 (76.8) | 59 (81.6) | 71 (81.3) |
| $CLKBUF\_X2$ | 350 | 400 | 560 | 79 (77.4) | 59 (85.3) | 71 (87.3) |
| $INV\_X1$ | 320 | 450 | 550 | 62 (80.6) | 56 (87.6) | 80 (85.5) |
| $INV\_X2$ | 400 | 500 | 480 | 78 (80.5) | 58 (88.4) | 75 (84.4) |
| $NAND2\_X1$ | 650 | 1130 | 1300 | 150 (76.9) | 145 (87.2) | 160 (87.7) |
| $NOR2\_X1$ | 450 | 880 | 1150 | 125 (72.2) | 95 (89.2) | 195 (83.0) |
| $NOR3\_X1$ | 890 | 950 | 1410 | 179 (79.9) | 93 (90.2) | 145 (89.7) |
| $OR2\_X1$ | 260 | 460 | 1120 | 69 (73.5) | 89 (80.7) | 185 (83.5) |
| $XOR2\_X1$ | 360 | 710 | 780 | 118 (70.6) | 118 (83.4) | 155 (80.1) |
| **Average** | | | | **76.5** | **85.5** | **84.4** |

impacted by the same particle sources lead to a different response. Although a scaled technology has a lower sensitive volume for charge collection, technology with a better nodal capacitance (critical charge) will generate an induced transient with reduced properties. In the presence of worst cases of process corners (P), operating voltage (V), and temperature (T) variations, the propagation of transient pulse, initially with no serious threat, which would be masked electrically, leads to pulse broadening. When temperature increases and voltage reduces, the charge carrier's mobility reduces. The effect reduces the drive current and causes an increase in the transient current. Also, existing vulnerable gates are not exempted from the impact of the worst corners of PVT variations. This effect causes the propagating transient traverses more gates toward a storage element.

The pulse broadening effect can be minimized by reducing the effect of variations on those gates. The design implementation is explained in chapter 4, and the implementation flow is shown in Fig. 6.1. Each vulnerable gate is replaced with gates in the standard cell library of higher strength that adds nodal capacitance value to the design. The approach is applied on the vulnerable gates of the *sine* circuit of EPFL benchmark circuits [3]. For example, the worst gate *NOR3_X1*

Table 6.2: The EPFL benchmark circuits with synthesized and vulnerable gates. The simulation column shows the percentage changes in the area after the mitigation approach is applied.

| | | Synthesis | | Sims | |
|---|---|---|---|---|---|
| Circuit | #Ref[a] | #gates[b] | Area($\mu m^2$) | %V.g[c] | %$\Delta$[d] |
| Adder | 4 | 131 | 544.77 | 2.29 | 0.54 |
| Barrel shifter | 11 | 1752 | 2020.54 | 29.50 | 37.99 |
| Divisor | 68 | 31,731 | 34,880.31 | 53.41 | 56.83 |
| Log2 | 40 | 12,031 | 17,731.03 | 34.06 | 24.32 |
| Max | 22 | 2,138 | 2,248.76 | 61.37 | 56.92 |
| Multiplier | 34 | 8,660 | 14,767.26 | 39.41 | 23.92 |
| Sine | 41 | 2,292 | 3,068.84 | 44.94 | 36.16 |
| Square-root | 70 | 21,290 | 25,096.83 | 49.13 | 48.35 |
| Square | 28 | 5,917 | 10,719.80 | 50.63 | 24.48 |

[a] The number of gate references in each benchmark
[b] The number of gates after synthesis
[c] The percentage of vulnerable gates before mitigation
[d] The percentage change in the area after mitigation is applied

is replaced with *NOR3_X4*, and the standard cell mitigation approach applied on the vulnerable logical gates of the *sine* circuit reduces the pulsewidth and amplitude of the transient to an average of 86.6%. The mitigation helps the robustness of the design by reducing the amplitude of the propagating transient on average by 76.5% for process corner variation, 85.5% for operating voltage variation, and 84.4% for temperature variation, as shown in Table 6.1. The approach reduces the ability of vulnerable gates to generate a transient of sufficient amplitude in the presence of the worst cases of PVT variation. The technique is extended and repeated to other selected arithmetic benchmark circuits from the EPFL benchmark suite [3] as shown in Table 6.2. Table 6.2 shows the percentage of vulnerable gates before mitigation and the percentage change in the area after applying the mitigation technique in each benchmark circuit. The electrical masking of the logic nodes increases to prevent the propagation of radiation-induced transient pulse [33, 45, 76]. The broadening effect increased by the worst corners of PVT variations is mitigated.

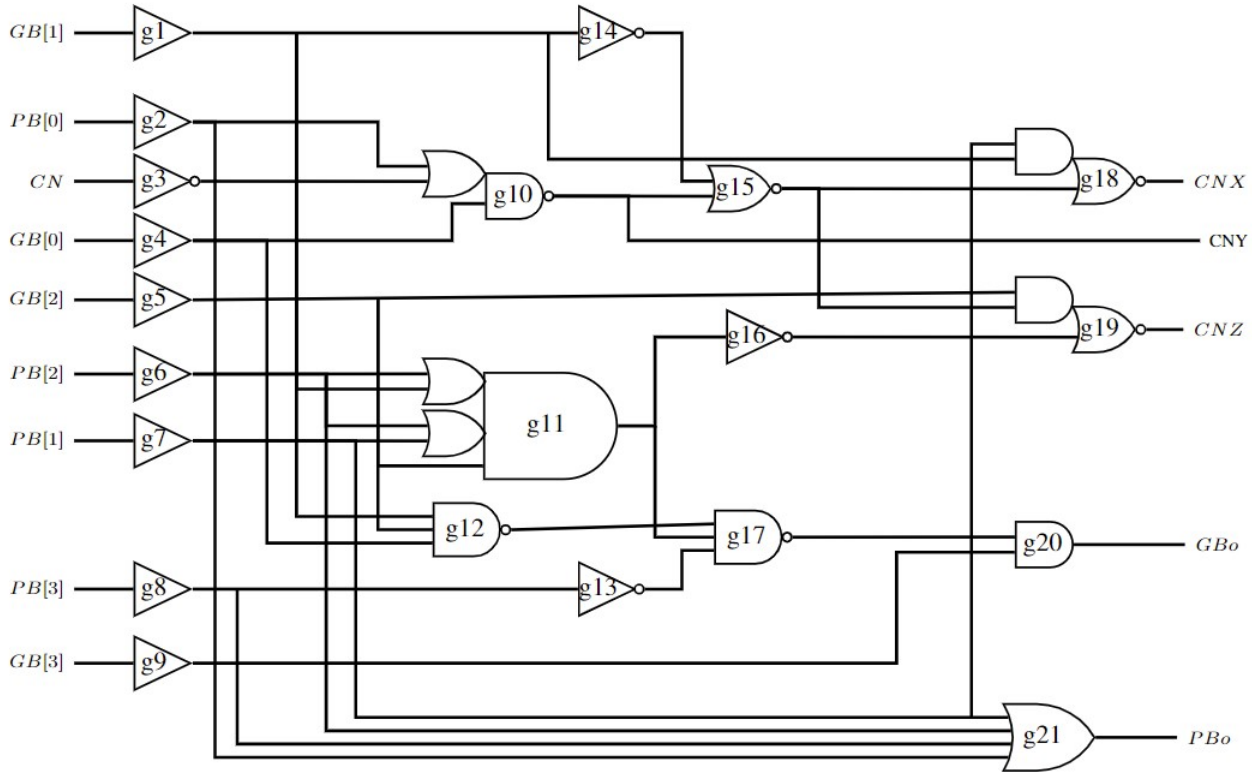



Figure 6.3: Gate-level netlist of 74182 benchmark circuit generated using Design Compiler (DC) [70], and the gate-level netlists were converted to HSpice for simulation.

### 6.2.2 Electrical Masking Improvement with Standard Logic Cell Synthesis

The electrical masking of a circuit changes when the logical gates along the path of vulnerability and the primary outputs are replaced with gates with increased strength. This approach weakens the worst cases of low-voltage and high-temperature variations using the 74182 (carry look-ahead (CLA)) benchmark circuit. The effect of the process (P), voltage (V), and temperature (T) variations are simulated with and without the mitigation strategy. The process simulations involve slow (ss), nominal (tt), and fast (ff) corners, respectively. The voltage (V) variation is $\pm 0.2$ of $V_{dd}$, and the temperature (T) variation include $-20°C$, $40°C$ and $100°C$. The gates at the primary inputs (PIs) are injected with a double-exponential waveform. The simulation is used to identify the paths easily traversed by the transient pulse from the point of a particle strike to the primary outputs (POs). During the HSPICE simulations, all the PIs can propagate the signals by applying input vectors that allow transient propagation. This ensures that the injected transient pulse propagates unhindered through the gates to the POs.

**Discussion of Results**

The simulation results help identify the vulnerable path and the gates along it, determine the worst cases during simulation involving PVT variations, and apply mitigation strategy to vulnerable gates.

1. **Identification of path of vulnerability**: The path of vulnerability is needed to identify the vulnerable gates [68]. The *typical* simulation results of PVT variation, as shown in Fig. 6.4, Fig. 6.5, and Fig. 6.6, show that the output of the gate, *g18*, has a transient pulse of sufficient amplitude and pulsewidth. The response of the logic gates depends on their logical operations, sources of the transient pulse, and the type of the gates. As shown in Fig. 6.3, two input pins of gate, *g18*, receive signals directly from the primary inputs, *GB[1]* and *PB[1]*. The logical operation of these signals increases the transient pulse with sufficient amplitude and pulsewidth. Hence the gate, *g18*, is selected as a vulnerable gate, and the paths through gates, *g15* and *g10*, from inputs *PB[0]*, *CN*, and *GB[0]* are chosen as the vulnerable paths. The logical gates on this path generated propagating transients with higher amplitudes and wider pulsewith than other logical gates because they have a reduced masking capability. The results of *typical* simulation of PVT variations at the POs *CNY*, *CNZ*, and *GBo* showed

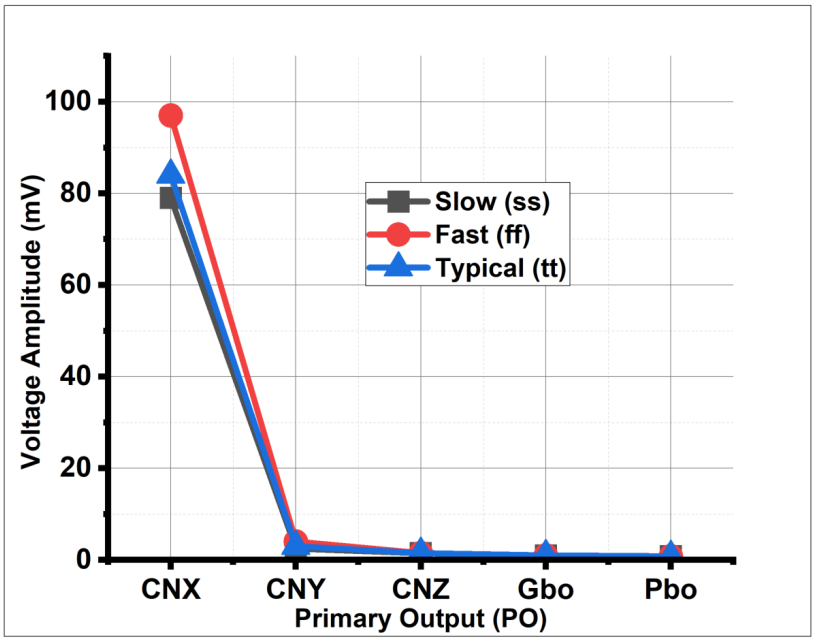



Figure 6.4: The plot shows the simulation results of the logical circuit in Fig. 6.3 estimated at the primary output (PO). The fault injection is simulated at different process corners (ss, tt, and ff). The values estimated at the PO *CNX* showed an increase in the amplitude of the transient pulse across all the process corners considered.

insignificant and reduced transient pulses. The pulses were sufficiently masked and reduced as they traversed the internal gates. The gate, *g21*, also produced a reduced transient pulse at its output, *PBo*, due to the size (area) of the gate that masked the transient pulse. The results of *typical* simulations used to select the paths and gates for mitigation.

2. **Process, Voltage, and Temperature variation**: The propagating transient pulse through the output, *CNX*, requires the mitigation technique because the path aids the propagation of the transient with sufficient amplitude and pulsewidth. As shown in Fig. 6.5 and Fig. 6.6, the worst cases were recorded at a low operating voltage and high-temperature [54], signifying a considerable impact of temperature and operating voltage on newer technologies. The charge carrier's mobility reduces as the temperature increases. Also, as the operating voltage reduces, a reduction in the drive current leads to an increase in the amplitude and pulsewidth of the induced transient current. The two conditions weaken the electrical masking capability of the logical gates of the design. These conditions aid the propagation of transient pulses from the

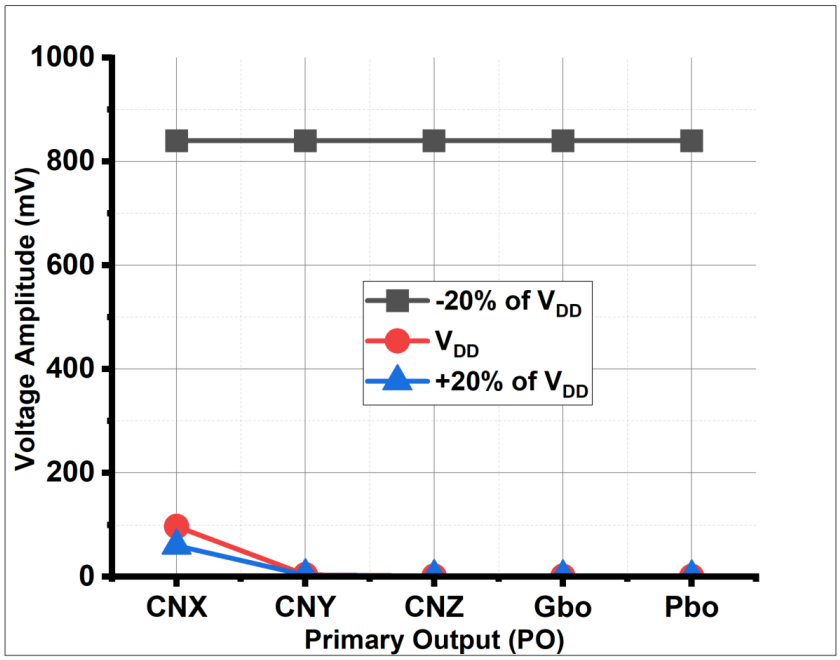



Figure 6.5: The simulation result shows the amplitude of the propagating transient estimated at the outputs of the logical circuit in Fig. 6.3. At -20 % of $V_{DD}$, the amplitude of the propagating transient at all the outputs of the logical circuits equals $V_{DD}$ since the drive current reduces as the operating voltage reduces.

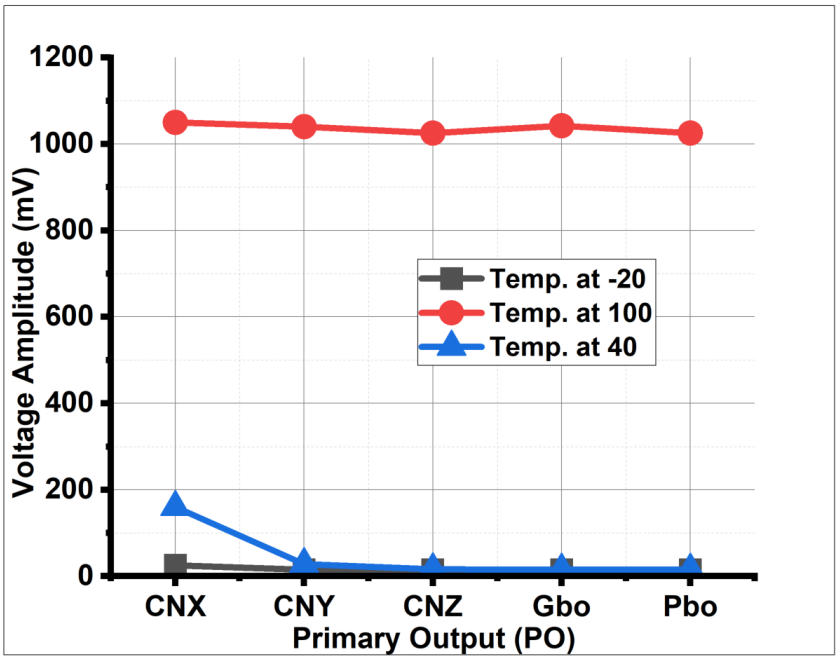



Figure 6.6: Temperature variation results at $-20°C$, $40°C$ and $100°C$. High temperature increases the amplitude of the transient pulse. As temperature increases, the charge carrier's mobility reduces, which reduces the drive current and increases the transient current.

PIs to the POs. Hence, there is a need to consider the gates at the POs for mitigation.

3. **Mitigation Strategy**: The mitigation approach helps the simulated circuit by minimizing or eliminating the propagating transient pulse. It is achieved using standard cells that increase the nodal capacitance of the logic gates on the design. Since the worst cases occur at low voltage and high temperature, the mitigation simulation only focuses on those cases. The vulnerable gates are identified and replaced with gates with higher drive strength to boost the design's overall electrical masking. For instance, due to the worst cases recorded under high temperatures and low voltage, the gates at the primary outputs are replaced with higher drive gates in the library. For instance, *AOI21_X4* gate for gates, *g18* and *g19*. *AND2_X4* gate for *g20* gate, and *OR4_X4* gate for *g21* gate. Fig. 6.7 depicts the difference between the mitigation strategies before and after considering the worst cases of PVT variations. The effects of low operating voltage and high temperature reduced to an average of 7% and 10% of the initial amplitudes, respectively, with 51% area overhead.

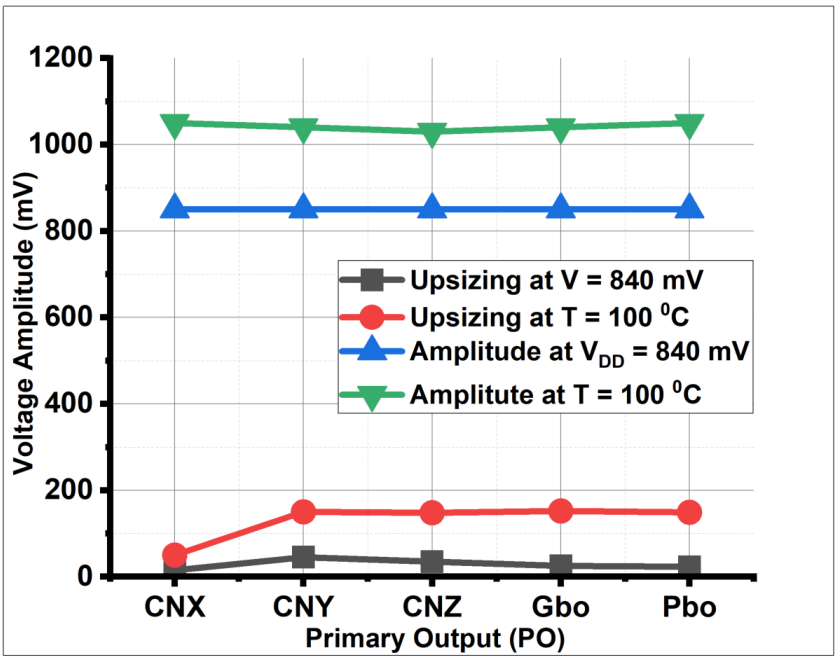



Figure 6.7: The worst cases of low voltage and high temperature are mitigated using higher-strength gates to replace the selected vulnerable gates.

The vulnerable gates aid the propagation of radiation-induced transients. With variation, the propagating transient traverses more gates along the path of vulnerability. However, by replacing the vulnerable gates with gates of higher strength in the library, the electrical masking increases, and the impact of vulnerable gates reduces.

### 6.2.3 Minimize the Single Event Upset in SRAM

In the era of nanometer technology, understanding the technology's reaction to a particle strike (fault–injection) helps develop appropriate mitigation techniques for the designs implemented in such advanced technologies. With the continuous scaling of the technology, the radiation-induced transients' waveform and propagation are greatly affected. The metrics of the transients, such as amplitude, Full Width at Half Maximum (FWHM), time constants ($t_{rise}$, $t_{fall}$), and duration, change as technology transits from MOSFET to FinFET technology nodes. The reported works in [4, 37, 84, 83] gave findings of reduced pulsewidth, pulse quenching, and parasitic capacitances with the FinFET technologies. As an example of design implemented using advanced technology, SRAM is sensitive to particle strikes. The stored bit on the node can flip since the scaling reduces the node

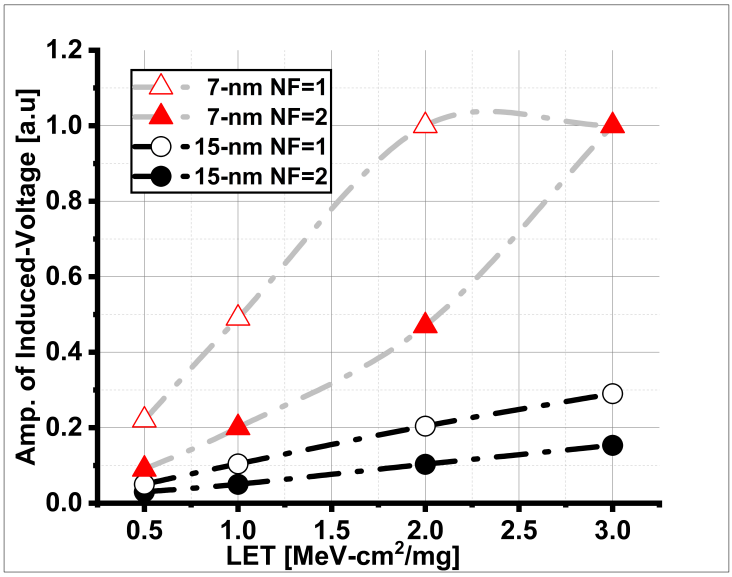



Figure 6.8: The impact of particle LET on 7-nm and 15-nm FinFET technologies. As the value of LET increases, the amplitude of the radiation-induced voltage transient increases. 7-nm generates transient with a higher amplitude since it has a reduced critical charge. The amplitude of the transient reduces as the number of fins increases.

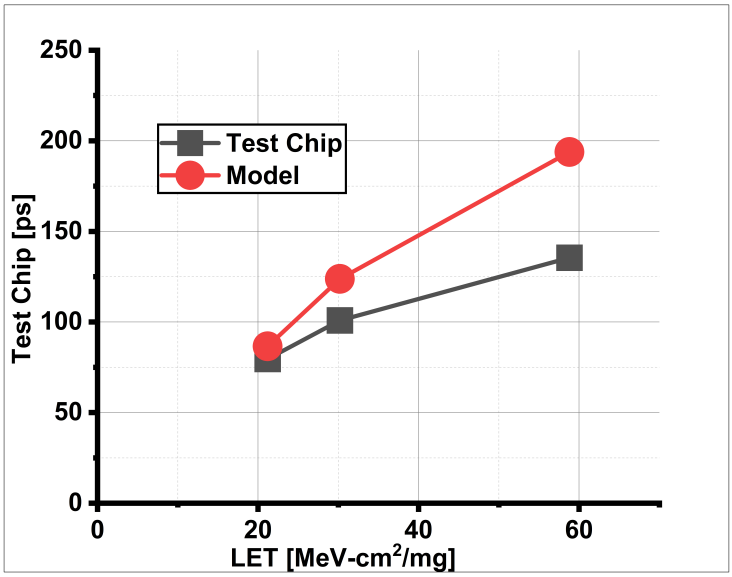
capacitances. Fig. 6.8 shows the response of 7-nm FinFET and 15-nm FinFET technology nodes to particle LET. When subjected to the same LET, the 15-nm FinFET has reduced amplitude compared to the 7-nm FinFET since 7-nm has a reduced critical charge than 15-nm. As the particle LET increases, the amplitude of the radiation-induced voltage transient increases. However, increasing the number of fins increases the node capacitance. Therefore, as the fins of the design increase, the transient amplitude reduces significantly, as shown in the figure.

## 6.3 Validation of Simulation Results With the Experimental Data - Estimation of Pulsewidth as a Function of LET

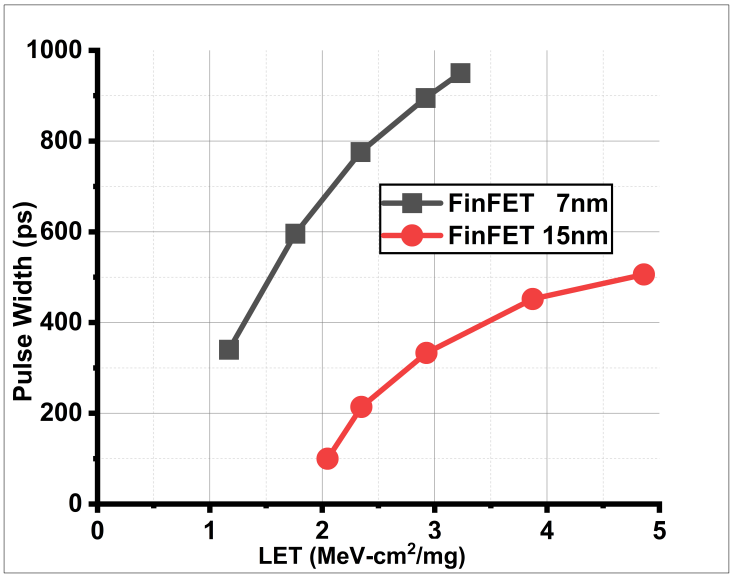
The validation approach uses the experimental data reported in [71] to validate the FinFET technology models used in this chapter.

### 6.3.1 Design Approach

Twenty-one chains of inverters were designed to validate the 7-nm and 15-nm FinFET technology nodes used in this chapter. The corresponding LET value of the injected fault at the first




(a)




(b)

Figure 6.9: (a) Experimental data for 65nm inverters reported in [71]. As the value of LET increases, the estimated pulsewidth of the SET pulse of the test chip and model implemented in [71] increases. (b) An estimated SET pulsewidth in 7-nm and 15-nm technology nodes when the value of the injected fault varied from 0 to 5 LET. As the value of the LET increases, the pulsewidth increases. Since 15-nm has a higher critical charge, the pulsewidth of the propagating transient is reduced compared to 7-nm.

inverter's output varied from 0 to 5. At the output of the chain's last inverter, the pulsewidth of the propagating transient was estimated.

### 6.3.2 Discussion of Results

Fig. 6.9 (b) shows the estimated pulsewidth as the value of LET increases. As the value of LET increases, the pulsewidth increases in both technology models. The response of each technology node to an injected fault differs since the critical charge and the sensitive volume in each technology differ. For example, the pulsewidth of 7-nm is higher than 15-nm since the critical charge in 7-nm is significantly lower than 15-nm. Lower critical charge leads to less electrical masking. Therefore, there is an increase in the pulsewidth as the value of LET increases. The plot is compared to the experimental data reported in [71] as shown in Fig. 6.9 (a).

## 6.4 Chapter Summary

The mitigation principle is essential for the successful operations of the technology operating in a radiation environment. The steps uplift the robustness of the design within radiation environments. This chapter looks at the different mitigation approaches for minimizing or eliminating the propagation of radiation-induced transients. The approach minimizes the effect of the worst cases of PVT variations on induced transient initially with reduced amplitude and pulsewidth.

# CHAPTER 7

# COST-TO-RELIABILITY TRADE-OFF TECHNIQUES FOR IMPROVING THE ROBUSTNESS OF ADVANCED TECHNOLOGY DESIGNS

Mitigation techniques help the electrical masking of the logical gates by increasing the node capacitance. However, high penalty costs should be avoided when implementing a mitigation approach since it will affect the overall benefits of technology scaling. The penalty for increasing the robustness or resilience of a design varies depending on the applications. For example, electronic design for space applications requires a different mitigation approach from consumer electronics. Therefore, ensuring that the penalty does not overshadow the technology's benefits is critical for a reliability design. Adding additional nanowatts of power to existing power consumption on a die with billion of gates cannot be allowed in mission-critical applications. This chapter analyzes mitigation approaches involving ASIC front–end design flow to improve electrical masking. In chapter 4, the impact of the process, voltage, and temperature (PVT) variations on scaled technology have been explored. Also, the impact of fins, gate strengths, and logic gates as mitigation techniques for improving the electrical masking and design's robustness are discussed in Chapter 6. The chapter uses previous results to analyze and recommend a cost-to-reliability trade-off technique with options to reduce the penalty for improving resilience or robustness.

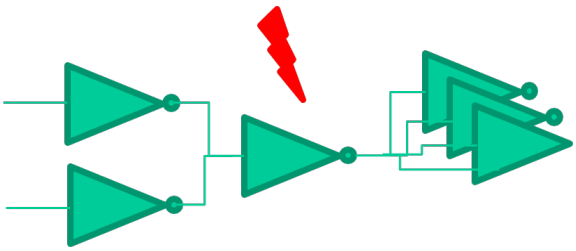


Figure 7.1: The gates within the logical path respond to fault injection differently than a standalone logic gate. The impact of fault injection on the gate with fan-out can affect the gates on its fan-out.

## 7.1 Analysis of Electrical Masking of Gate(s) Within Netlists

Understanding the mechanisms of charge deposition, sharing, and quenching related to Fin-

FET technology helps to choose/recommend an appropriate mitigation approach for the design implemented in the latest nanometer technology nodes. Charge-sharing induced single-event transient (SET) pulse quenching with bulk FinFET using TCAD has been reported [84]. Modeling the physical mechanisms requires understanding how the technology responds to the impact of particle strikes. The work in [4] discussed the impact of parasitic capacitances and also [83] discusses that the SET pulses width in FinFET technology is smaller compared to bulk technology with parasitic capacitances [4, 37]. As earlier reported [84], the charge accumulation/deposition is limited around the fin compared to the bulk technology body. Hence, the fin's structure dictates the performance of the technology [28]. The dissertation activities characterize the impact of radiation-induced transient using FinFET technologies. The characterization results help understand the influence of process, voltage, and temperature (PVT) variations on the propagating transient in FinFET technology nodes.

### 7.1.1 Impact of Fan-in and Fan-out on Synthesis Gates Using FinFET Technology Nodes

The dissertation analyzes the impact of surrounding gates on the electrical masking capability of the gate(s) within a network of gates in a logical path or depth using the 7-nm and 15-nm FinFET technologies.

#### Design Approach

The study analyzes the impact of reduced electrical masking on fan-in and fan-out gates. The fan-in and fan-out simulation arrangement for INV, NOR, and NAND gates is shown in Fig. 7.1. The fan-out is varied as 1, 2, 4, 6, 8, and 10 using the HSpice simulation. The input vector is limited to two for gates with more than one input, such as NOR and NAND. Finally, the simulation process is simulated with LET of 0.5, 1, 2, 5, and 10 to obtain the amplitude of the resulting voltage transient.

1. **Case 1-Gate with fan-outs**: The simulation focuses on the worst-case input vector since it generates a high amplitude transient.

2. **Case 2-Fan-in gates with different LET**: The simulation follows a similar procedure as case 1 but focuses only on the preceding gate before the gate with the fan-outs.

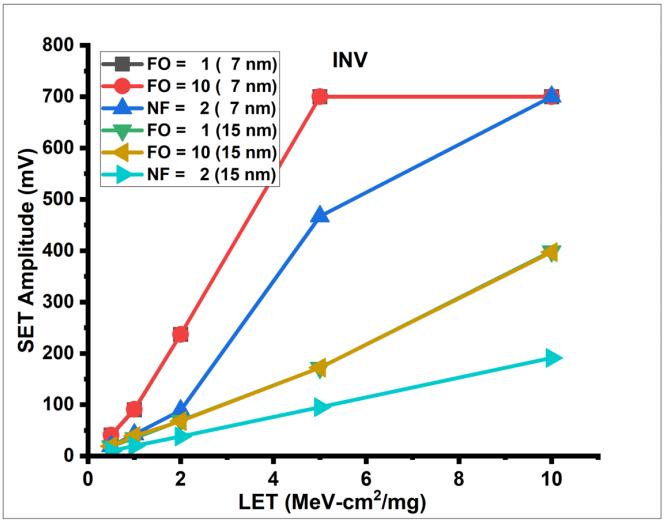



Figure 7.2: Amplitude of propagating transient at the output of the gate with fan-out using INV gates. The transient has a sufficient amplitude to propagate when the LET value equals or exceeds 10. When the number of fins increases to two, the amplitude reduces.

**Discussion of Results**

The amplitude of the induced transient in both cases shows similar simulation results for 15-nm (INV, NAND, and NOR) and 7-nm (INV, NAND, and NOR) as shown in Fig. 7.2, Fig. 7.3 and Fig. 7.4. The simulation results categorize them into low LET (0 - 2) and high LET (4 and above) cases. A low LET effect is noticed in the simulation results. As reported in [59], technology impacted with a low LET of less than 10 shows a low response due to a reduced charge deposition in the small fin area of the FinFET. Hence, in this simulation, at low LET (0 - 2), the propagating transient has reduced amplitude and pulsewidth with no significant effect on the fan-out gates. Hence, the next gate on the fan-out efficiently mitigates the propagating transient of low LET (0 - 2). However, the induced transient propagates unhindered at high LET, and the amplitude reaches the voltage rail as early as LET of 5. This is common among the gates with fan-outs [27], but as the number of fan-out gates changes, there is a difference in pulsewidth [80]. The transient propagation depends on the intensity of fault injection, the type and size of gates, and the injection timing. As the number of fins increases, the amplitude and pulsewidth of the propagating induced transient reduce.

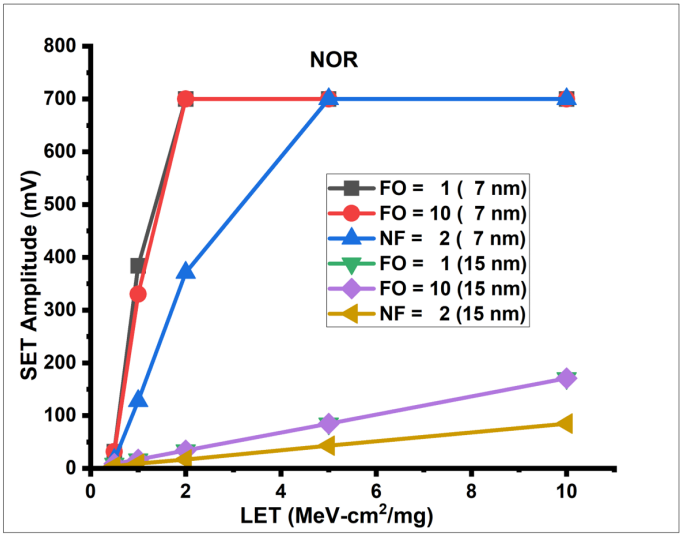



Figure 7.3: Amplitude of propagating transient at the output of the gate with fan-out using NOR gates. The transient has a sufficient amplitude to propagate when the LET value equals or exceeds 10. When the number of fins increases to two, the amplitude reduces.

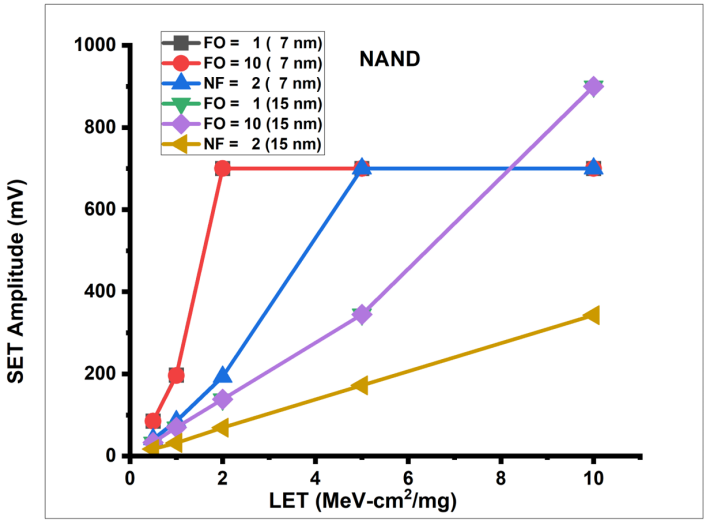



Figure 7.4: Amplitude of propagating transient at the output of the gate with fan-out using NAND gates. The transient has a sufficient amplitude to propagate when the LET value equals or exceeds 10. When the number of fins increases to two, the amplitude reduces.

Table 7.1: The ISCAS85 benchmark circuits used in this dissertation work. Each circuit is synthesized to gate-level netlists using 7-nm FinFET, 15-nm FinFET, and 45-nm MOSFET technologies.

| **ID** | *Circuit* | *In* | *Out* |
|---|---|---|---|
| **c432** | 27-channel interrupt controller | 36 | 7 |
| **c499** | 32-bit SEC circuit | 41 | 32 |
| **c880** | 8-bit ALU | 60 | 26 |
| **c1908** | 16-bit SEC/DED circuit | 33 | 25 |
| **c2670** | 12-bit ALU and controller | 233 | 140 |
| **c3540** | 8-bit ALU | 50 | 22 |
| **c5315** | 9-bit ALU | 178 | 123 |
| **c6288** | 16x16 multiplier | 32 | 32 |
| **c7552** | 32-bit adder/comparator | 207 | 108 |

### 7.2 RTL-to-Gate Synthesis

ISCAS85 benchmark circuits [30], as shown in Table 7.1, were synthesized to a gate-level netlist using Synopsys Design Compiler (DC) [69] with NanGate 45-nm standard cell library based on the FreePDK45 PDK [49], NCSU FreePDK 15-nm [51], and ASAP 7-nm Predictive PDK [16] models. During the RTL-to-gate Synthesis, RTL is mapped to technology using Synopsys Design Compiler (DC) to produce technology-dependent gate-level netlists. The Design Compiler (DC) or any other synthesis tool performs the following tasks:

- Performs high-level RTL optimizations
- RTL to unoptimized Boolean logic
- Technology independent optimizations
- Technology mapping to available technology

The timing, area, and gate-level netlist output reports can be viewed using Design Vision (DV). As shown in Fig. 7.5, library and environment set-up are crucial during the synthesis flow. Gate-level netlist, cell, and area information were extracted as needed for further research activities.

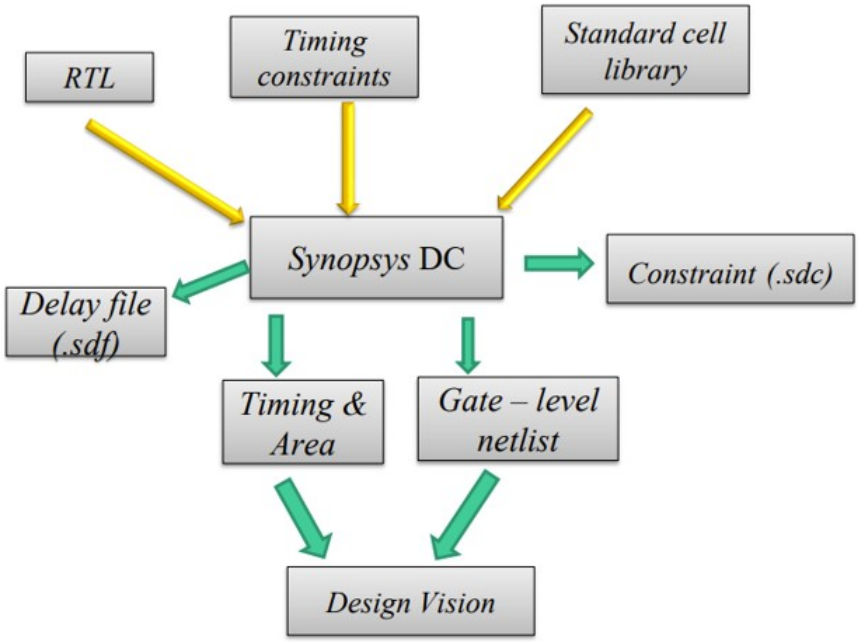



Figure 7.5: The synthesis flow to create gate-level netlist. The synthesis approach uses RTL verilog files, standard cell library, and constraints as the inputs.

## 7.3 Analysis of Cost-to-Reliability Trade-Off

The prior simulation results have established that in 15-nm and 7-nm FinFET technology nodes, the transient of low LET $\leq 2$ can easily be mitigated by the next gate in the logical path or depth. Replacing the gate with another gate of higher strength or changing the number of the fin mitigate the transient of low LET $\leq 2$. Hence the analysis focuses on low LET cases. Furthermore, the cost-to-reliability trade-off approach is considered to minimize the performance overhead. There are two approaches presented in this dissertation:

- Most Frequent Gates (MFG) Approach
- One-to-Many Fan-out Approach

### 7.3.1 Most Frequent Gates (MFG) Approach

Technology scaling increases the density of gates on the fabricated die and increases the possibility of multiple gates being affected by particle strikes. The most frequent gates (MFG) approach

Table 7.2: The frequency of gates based on the percentage of instances in the c1908 gate-level netlist.

| **Reference** | Unit area $\mu m^2$ | Count | Total area $\mu m^2$ | Gate % | New area $\mu m^2$ |
|---|---|---|---|---|---|
| *XNOR2xp5_ASAP7_75t_L* | 0.13122 | 39 | 5.11758 | 11.93 | 6.82344 |
| *INVx1_ASAP7_75t_L* | 0.04374 | 34 | 1.48716 | 10.40 | 1.98288 |
| *NAND2xp5_ASAP7_75t_L* | 0.05832 | 34 | 1.98288 | 10.40 | 2.97432 |
| *AND2x2_ASAP7_75t_L* | 0.08748 | 26 | 2.27448 | 7.95 | 2.27448 |
| *XOR2xp5_ASAP7_75t_L* | 0.13122 | 25 | 3.2805 | 7.65 | 3.28050 |
| *INVxp33_ASAP7_75t_L* | 0.04374 | 19 | 0.83106 | 5.81 | 0.83106 |

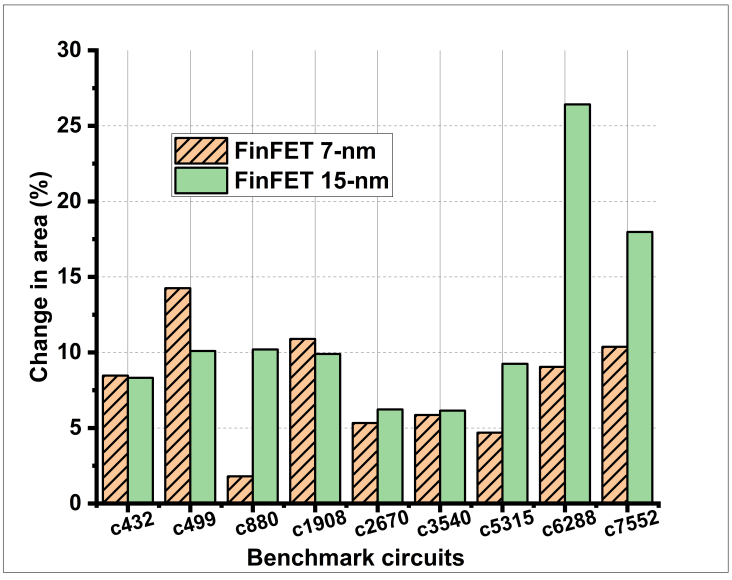



Figure 7.6: MFG of 10% and above selected for mitigation. The frequency of the gates is chosen as a mitigation strategy. Focusing on the most frequent gates in the design helps the mitigation strategy.

analyzes the synthesized gate-level netlists using FinFET 7-nm and 15-nm technologies with ISCAS85 benchmark circuits. Since single-event effects (SEE) on silicon technology affect the multiple gates on a scaled design, the probability of higher frequency for SER is very high. Therefore, applying a mitigation strategy using the frequency of gates can be a reasonable means of reducing the transient's propagation. The approach analyzes 7-nm and 15-nm synthesis files to identify the most frequent gate with 10% and above, as shown in Table 7.2, as a means for a possible mitigation strategy. Fig. 7.6 shows the cost of using MFG in each benchmark circuit.

### 7.3.2 One-to-Many Fanout Approach

The data-driven approach with a range of techniques/options to reduce the reliability concerns of a design implemented with newer technology is explored in this section. The fan-out relationship between the gates can be explored as a possible means of mitigation. The analysis focuses on early PVT variation simulation results in Figs. 4.7, 4.8 and 4.6. Also, the simulation results in section 7.1 have established that, in 15-nm and 7-nm, the transient with LET $\leq 2$ can easily be mitigated by the next gate in the logical path or depth. Hence, in synthesized gate-level netlists, a location within the logic path or depth with better nodal capacitance will ultimately weaken the propagation of radiation-induced transients [55] of low LET. The work analyzes transient propagation and introduces mitigation strategies that protect against PVT variation and induced transient while minimizing performance overhead. The idea is to reduce the number of gates considered for mitigation. The flow of the approach is shown in Fig. 7.7. The approach uses a fan-out of *three* and above for the MOSFET 45 nm, and a fan-out of *four* and above is used for both 7-nm and 15-nm technology nodes. However, if the cost of mitigation is not an issue, lower fan-out can be considered using FinFET technologies. The lower the number of the fan-out, the higher the cost.

- **Identification of Gates with Fan-out**: The gate, *inva*, with fan-outs, as shown in Fig. 7.8, can propagate the radiation-induced transient to other gates on its fan-out. If a transient waveform of high amplitude and wider pulsewidth is generated, the fan-out gates would be impacted by receiving the induced transient of propagating potential. However, if gate, *inva*, is identified for hardening, the propagation of the induced transient can be mitigated from affecting the gates on its fan-out. Though an increase in fan-out adds to the output capacitance between the gates and weakens the propagated radiation-induced transients, the value of output ca-

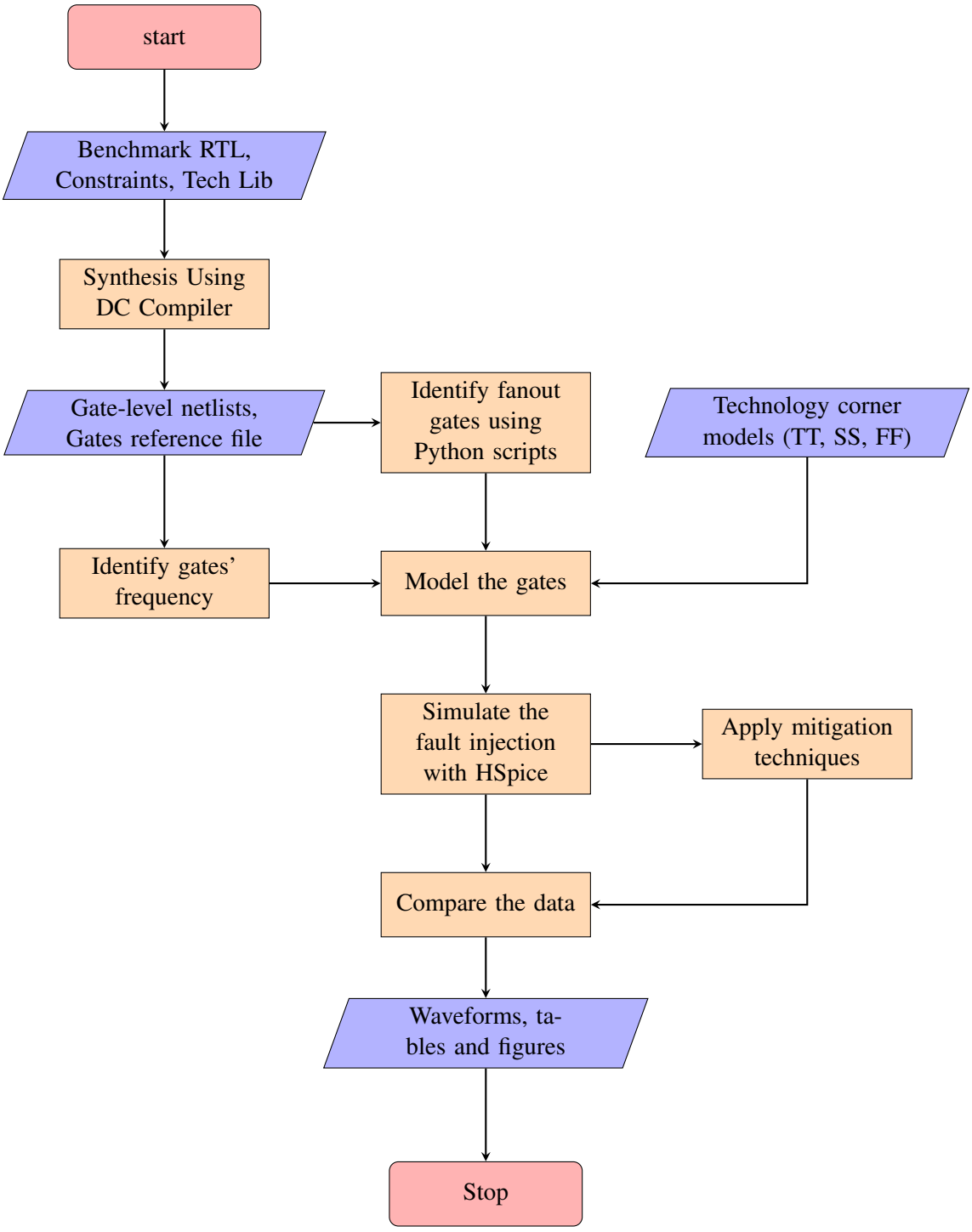



Figure 7.7: The flow of the proposed research work. The flow gives results of traditional ASIC front–end flow and modified flow. The Latex for implementing the flow is added in Appendix A

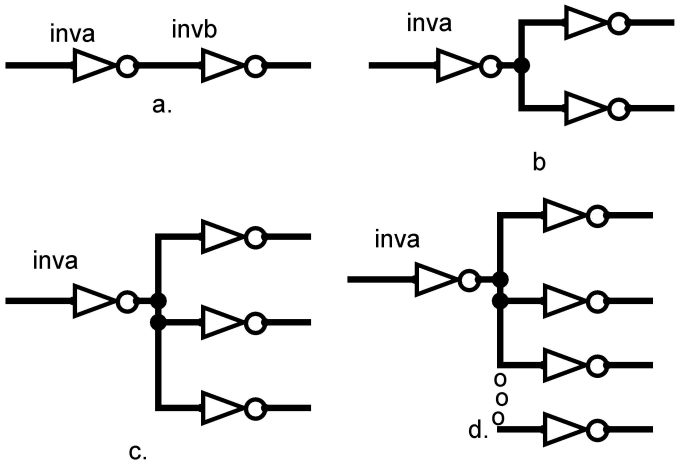



Figure 7.8: Fan-out arrangement with gate and its fan-outs. The induced propagating transient from the gate, *inva*, can impact the fan-out gates. The higher the number of fan-out gates, the higher the number of gates the propagating transient pulse can impact.

```
#########################################################################################################
########################## THE SCRIPT ACCEPTS GATE-LEVEL NETLIST FILE OF BENCHMARK CIRCUIT    ###################
#########################################################################################################
########################## Select one of the codes below as netlist_key ##################################
#########################################################################################################
##                                                                                                     ##
##                 0 -c17 ## 1 - c432 ## 2 - c499 ## 3 - c880 ## 4 - c1908 ## 5 - c2670              ##
##                          6 - c3540 ## 7 - c5315 ## 8 - c6288 ## 9 - c7552                          ##
##                                                                                                     ##
#########################################################################################################
#########################################################################################################

Pick a netlist code number: 1

Total number of gates in selected c432.vh gate-level netlist is: 196

c432.vh is identified for further processing.

#FO is less than  4

#FO is less than  4

#FO is less than  4

For FO of  4
1       AND2_X2
1       INV_X2
2       NAND2_X1
1       OR3_X1

For FO of  5
1       NAND2_X2
1       OAI21_X2

For FO of  9
1       INV_X16
```

Figure 7.9: The prescreen shows a typical output from the Python codes. The codes have the option of selecting the benchmark circuit to analyze. Python codes are in this document's Appendix B

**Algorithm 1:** The algorithm shows the flow used to determine the number of gates with fan-outs. The Python script implementation based on the Algorithm flow is available in Appendix B.

```
Result: Mapping of ISCAS85 to gate-level netlist
Read the netlists;
while for each net do
    Identify the gates and their instance;
    if net and gate in netlist then
        Determine the number of gates with a similar number of fan-out ;
        List out the gates and their instances;
    end
end
```

pacitance also reduces with scaling. The python script is implemented to identify the gate(s) with fan-out in synthesized files of the three technology files considered for this dissertation work. The script identifies the gates with different fan-outs, determines the number and the type of gates, and groups the gates according to the number of fan-outs. A typical output from the Python script is shown in Fig. 7.9, and the Python code for identifying the gates on the fan-out is added to the Appendix B section of this document. The distribution of the gates with their various fan-out arrangement is shown in Table 7.3. The algorithm flow for implementing the selection of gate(s) with fan-out is shown in Algorithm 1. Depending on the benchmark circuits, the synthesis of benchmark circuits can generate gate-level netlists that may be manually challenging to analyze. Using Python script reduces the time to identify gates with their respective fan-outs.

- **Mitigation Strategy**: The mitigation strategy focuses on reducing the number of gates selected for the design resilience or robustness improvement. The approach aids the resilience of the design by mitigating the propagating transient of low LET with less overhead. To limit the overhead cost, the dissertation chooses gates of fan-outs of *three* and above for MOSFET technology or *four* and above for FinFET technologies. For example, as shown in Table 7.3, if an option of fan-out of *four* and above is selected for mitigation in the c499 benchmark circuit using FinFET technologies, the mitigation requires twenty-one gates (8.14%) in FinFET 7-nm and twenty-one gates (8.40%) in FinFET 15-nm. On the other hand, using the fan-out of *three* and above in 45-nm requires fifty-two gates (20.96%) in MOSFET 45-nm gate-level

Table 7.3: Gates with fan-out (s) in gate-level netlists of ISCAS'85 benchmark circuits using 7-nm FinFET, 15nm FinFET, and 45-nm MOSFET technologies.

| | | FinFET 7-nm | | | | | | FinFET 15-nm | | | | | | MOSFET 45-nm | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | Inp/Out | #Gates | 4 | 5 | 6 | 7 | ≥7 | #Gates | 4 | 5 | 6 | 7 | ≥7 | #Gates | 3 | 4 | 5 | ≥5 |
| **c432** | 36/7 | 212 | 2 | 1 | 0 | 0 | 0 | 196 | 5 | 2 | 1 | 0 | 0 | 241 | 12 | 1 | 2 | 0 |
| **c499** | 41/32 | 258 | 15 | 2 | 1 | 2 | 1 | 250 | 15 | 3 | 3 | 0 | 0 | 248 | 31 | 13 | 5 | 3 |
| **c880** | 60/26 | 468 | 14 | 10 | 3 | 0 | 0 | 200 | 11 | 4 | 1 | 0 | 0 | 328 | 17 | 10 | 5 | 6 |
| **c1908** | 33/25 | 327 | 6 | 3 | 5 | 3 | 5 | 306 | 16 | 1 | 2 | 0 | 3 | 400 | 21 | 10 | 4 | 2 |
| **c2670** | 233/140 | 400 | 8 | 3 | 1 | 2 | 4 | 413 | 18 | 2 | 1 | 1 | 2 | 503 | 27 | 11 | 5 | 10 |
| **c3540** | 50/22 | 901 | 37 | 22 | 5 | 4 | 25 | 805 | 25 | 19 | 9 | 9 | 18 | 1429 | 73 | 18 | 17 | 33 |
| **c5315** | 178/123 | 949 | 41 | 21 | 9 | 14 | 23 | 968 | 23 | 19 | 2 | 3 | 17 | 1319 | 75 | 21 | 30 | 49 |
| **c7552** | 207/108 | 1337 | 42 | 20 | 10 | 6 | 9 | 1063 | 33 | 13 | 8 | 2 | 11 | 1565 | 162 | 33 | 13 | 21 |
| **c6288** | 32/32 | 2901 | 141 | 33 | 8 | 5 | 27 | 1990 | 18 | 0 | 0 | 0 | 6 | 7254 | 535 | 137 | 33 | 42 |

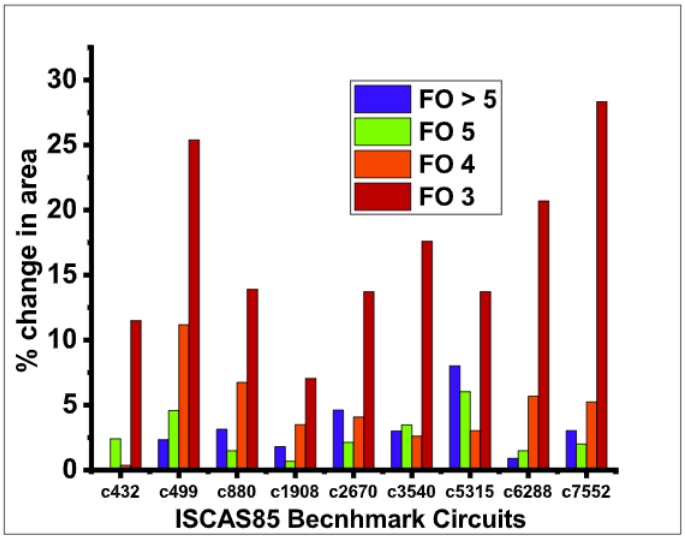



Figure 7.10: The percentage change in area in 45-nm MOSFET after applying the mitigation technique to different fan-outs. Since the 45-nm has a large surface area with high dimensions, the cost of mitigating the gates will be high compared to 7-nm and 15-nm FinFET technologies.

netlists as the fan-out of *three* produces the additional gates. The number of gates with fan-outs will increase as the number of fan-outs is lowered. Since the number of gates selected for mitigation is proportional to the area and power overhead, the approach gives a reduced penalty when the number of fan-out is increased.

- **Cost/Reliability Relationship**: The cost of implementing the mitigation approach differs from one technology to another. Since bulk technology has a huge sensitive volume (SV), the characterization results differ from the FinFET technologies. It means bulk technology collects more deposited charges. Hence, mitigating the radiation-induced transients in 45-nm technology designs incurred a higher penalty. The penalty is higher than FinFET technologies because a fan-out of *three* is included in the gates selected for mitigation. Also, the technology cells have a larger dimension than a scaled FinFET technology. This creates transients of wider pulsewidth and amplitude. Mitigating such transients requires a higher-strength cell to weaken the propagating transients at 45 nm. For instance, reducing the induced transient in $INV\_X1$ to a transient of insignificant amplitude and pulsewidth requires $INV\_X16$. The gate with fan-out under 45-nm must be replaced with the highest library cell to eliminate the propagating transient. Fig. 7.10 shows the cost incurred by implementing the approach

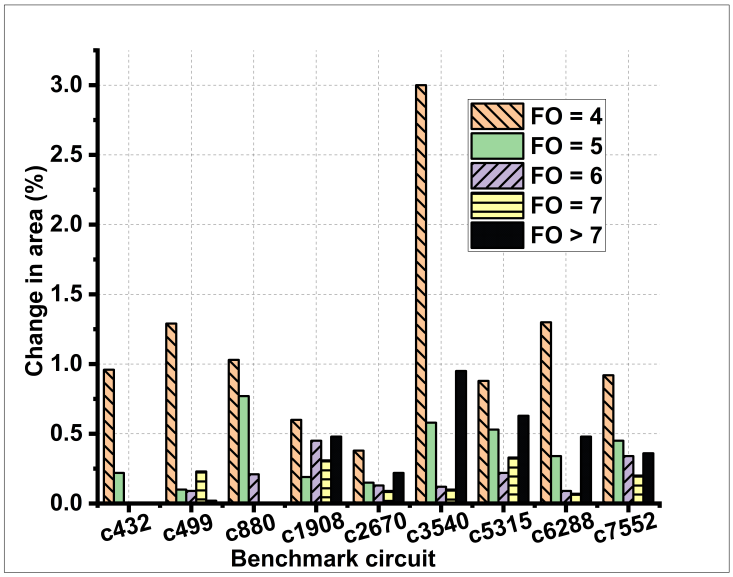



Figure 7.11: Percentage change in area in 7nm FinFET after applying the mitigation technique to different fan-outs. The higher the resilience or robustness of the design, the higher the cost. Using the fan-out of four reduces the cost.

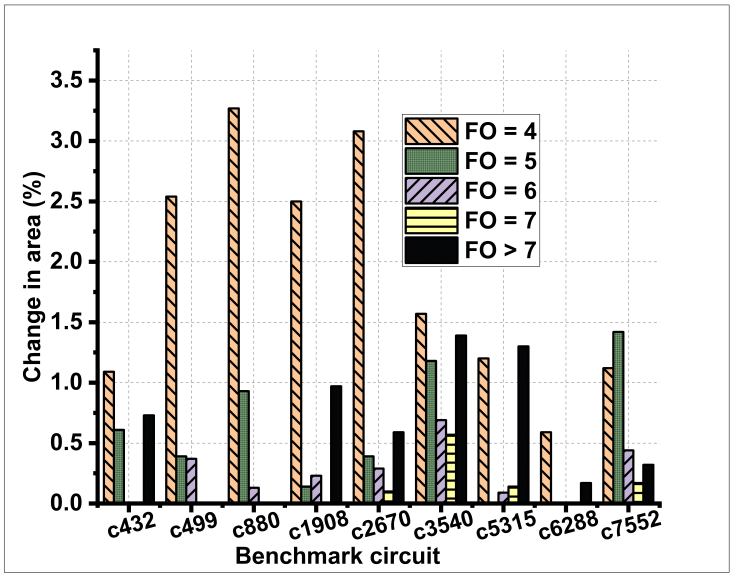



Figure 7.12: Percentage change in area in 15nm FinFET after applying the mitigation technique to different fan-outs. The number of gates selected for mitigation reduces when compared to hardening all gates on the electronic designs.

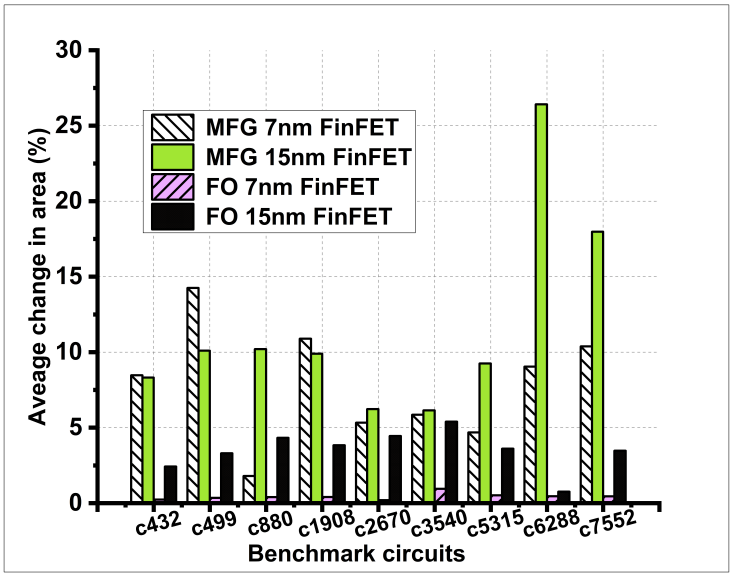



Figure 7.13: Comparison in percentage change in area overhead between the Most-Frequent Gates and Fan-out techniques using 7-nm and 15-nm technology nodes. The overhead cost reduces in FinFET 7-nm than in FinFET 15-nm, and the fan-out approach provides reduced overhead.

using 45-nm MOSFET. For FinFET technologies, the approach focuses on LOW LET (0-2), as earlier explained. The next or higher gate can eliminate transient propagation under low LET and PVT variations in the library. Fig. 7.11 and Fig. 7.12 show the areas incurred by each ISCAS85's benchmark circuit using 7-nm and 15-nm FinFET technology nodes. The fan-out approach still has low gates for mitigating or eliminating the propagating transients under the influence of PVT variation.

As shown in Fig. 7.13, comparing both methods using FinFET 7-nm and 15-nm technology nodes, the fan-out approach has a low overhead cost since the number of gates selected for mitigation focuses on the gate(s) with fan-outs for mitigation.

## 7.4 Chapter Summary

There is a need to analyze a mitigation strategy with a cost-to-reliability (resilience/robustness) trade-off to implement a robust design that eliminates the combined impact of variations and radiation-induced transients. The dissertation work characterizes the radiation-induced transients using FinFET technologies by investigating the effect of fan-in and fan-out gates on the electrical

masking within a logical path using the 7-nm and 15-nm FinFET technologies. Finally, it analyzes a fault-tolerant design to select various techniques/options for cost-to-reliability trade-offs. Two primary mitigation techniques were considered. The optional data-driven approach presents mitigation techniques that reduce the overhead in terms of area. These mitigation options/approaches are necessary to avoid overshadowing the technology's benefits.

# CHAPTER 8

## Summary

Technology scaling has increased the density of logic gates impacted by a single particle strike, affecting the reliability of digital designs. Also, process, voltage, and temperature (PVT) variations augment even low-threat transient pulses caused by particle strikes, leading to pulse broadening. The combined impact intensifies the propagation of a radiation-induced transient toward the storage elements. In a preferred case, the favorable corners of the variations show an improvement in the design's reliability response, while the worst corners show an impact that extends the reliability issues.

Moore's law has led to the 3D multi-gate technology with a significantly reduced critical charge. The impact leads to reduced electrical masking that initially struggles with existing radiation sources. The effects of surrounding gates on the electrical masking of the gate(s) within a logical path are analyzed in this study. The scaling effect within FinFET technology leads to the propagation of transients that broaden with a low, insignificant difference.

As advanced technology is now adopted for the development of ICs, there is a need to analyze a mitigation strategy for implementing a fault-tolerant design approach that eliminates the combined impact of variations and radiation-induced transients on the new emerging scaled integrated circuits (ICs). Major mitigation approaches only complete with cost, which is sometimes more significant than expected. Therefore, the dissertation analyzed fault-tolerant design techniques to mitigate the combined impact of radiation-induced transients and PVT variations. Furthermore, the dissertation used a data-driven approach to select various techniques/options to reduce the design reliability issues based on a reduced critical charge that affects the electrical masking capability of the logic nodes implemented in newer technologies. Data-driven approaches provide an opportunity for a reduced penalty since the number of logic gates selected for mitigation reduces compared to hardening all the logic gates on the design. The cost-to-reliability approaches provide reduced penalty mitigation strategies with better reliability.

The contributions provided in this dissertation include the following:

1. Evaluation of the resilience and vulnerability to fault injection of the designs implemented

using FinFET technology based on the characterization results of the radiation-induced transients.

2. Characterization and analysis of the response of 7-nm FinFET technology under pulse broadening with an insignificant difference in the pulsewidth from the point of fault injection to the output of the chains.

3. Analysis of fault-tolerant design approaches. The approaches mitigate the combined impact of radiation-induced transients and PVT variations.

4. Established that compensating relationship between the threshold voltage, $V_{TH}$, and current drive, $I_{drive}$, affect the pulsewidth and amplitude of propagating radiation-induced transient under pulse broadening and elevated temperature in an inverter chain.

5. Development of a model-based approach validated with the experimental data to estimate the SER of memory cells without the expense of laser beam or heavy ion testing. The model can be used to project the SER of the memory cells.

6. Development of Python scripts that accept gate-level netlist files to identify gates with fan-out more quickly than the manual approach.

7. Analyzed mitigation approaches for increasing the design's resilience or robustness by implementing cost-to-reliability trade-off techniques with optional penalty reduction. Vulnerable gates with fan-outs are selected for mitigation to avoid the propagation of induced transients to gates on the fan-outs.

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# Appendix A

# Latex script

The script is used to create the design flow as shown in chapter 6.2.

## A.1 Latex script for creating the flow of the dissertation work in chapter 7

```
\begin{figure}
%\centering
\begin{tikzpicture}[node distance=2cm]
\node (start) [startstop] {Start};
\node (in1) [io, below of=start] {Benchmark RTL, Constraints, Tech Lib};
\node (pro1) [process, below of=in1] {Synthesis Using DC Compiler};
\node (out1) [io, below of=pro1] {Gate-level netlists, Gates reference file};
\node (proc2) [process, right of=out1, xshift=3.0cm] {Identify fanout gates
    using Python scripts};
\node (proc3) [process, below of=out1, yshift=-0.50cm] {Identify gates'
    frequency};
\node (proc4) [process, right of=proc3, xshift=3.0cm] {Model the gates};
\node (in2) [io, right of=proc2, xshift=3.0cm] {Technology corner models (TT, SS
    , FF)};
\node (proc5) [process, below of=proc4, yshift=-0.5cm] {Simulate the fault
    injection with HSpice};
\node (proc6) [process, right of=proc5, xshift=3.0cm] {Apply mitigation
    techniques};
\node (proc7) [process, below of=proc5, yshift=-0.5cm] {Compare the data};
\node (out2) [io, below of=proc7] {Waveforms, tables and figures};
\node (stop) [startstop, below of=out2, yshift=-0.5cm] {Stop};

\draw [arrow] (start) -- (in1);
\draw [arrow] (in1) -- (pro1);
\draw [arrow] (pro1) -- (out1);
\draw [arrow] (out1) -- (proc2);
\draw [arrow] (out1) -- (proc3);
\draw [arrow] (proc2) -- (proc4);
```

```
\draw [arrow] (in2) |- (proc4);
\draw [arrow] (proc3) -- (proc4);
\draw [arrow] (proc4) -- (proc5);
\draw [arrow] (proc5) -- (proc6);
\draw [arrow] (proc6) |- (proc7);
\draw [arrow] (proc5) -- (proc7);
\draw [arrow] (proc7) -- (out2);
\draw [arrow] (out2) -- (stop);
\end{tikzpicture}
\caption{}
\end{figure}
```

# Appendix B

# Python script

## B.1 Python script to identify the fanout gates in a synthesis file shown in Table 7.3

```
## Select the netlist to analyze
print()
netlist_code = int(input("Pick a netlist code number: "))

print()

if netlist_code >= 10:
    print("You're wrong! You need to choose between 0 and 9. \n")
elif netlist_code < 0:
    print("It must be positive number and between 0 and 9. \n")
else:
    if netlist_code == 9:
        netlist_filename = "c7552.vh"
        ### range of = (internal nets), (output nets), (input nets), and (
    netlists)
        p1, p2, p3, p4, p5, p6, p7, p8 = 65, 160, 53, 65, 35, 53, 220, 1282
    elif netlist_code == 8:
        netlist_filename = "c6288.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 20, 221, 16, 20, 13, 16, 222, 2212
    elif netlist_code == 7:
        netlist_filename = "c5315.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 63, 149, 50, 63, 34, 50, 172, 1140
    elif netlist_code == 6:
        netlist_filename = "c3540.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 =  22, 97, 19, 22, 14, 19, 101, 906
    elif netlist_code == 5:
        netlist_filename = "c2670.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 82, 126, 66, 82, 43, 66, 230, 643
    elif netlist_code == 4:
        netlist_filename = "c1908.vh"
```

```
        p1, p2, p3, p4, p5, p6, p7, p8 = 19, 45, 16, 19, 13, 16, 46, 352
    elif netlist_code == 3:
        netlist_filename = "c880a.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 22, 37, 19, 22, 14, 19, 49, 249
    elif netlist_code == 2:
        netlist_filename = "c499.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 20, 40, 17, 20, 13, 17, 41, 291
    elif netlist_code == 1:
        netlist_filename = "c432.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 15, 33, 14, 15, 11, 14, 34, 230
    else:
        netlist_filename = "c17.vh"
        p1, p2, p3, p4, p5, p6, p7, p8 = 10, 11, 9, 10, 8, 9, 12, 20
    ##### Step 3. List out the total number, types, and instances of gates
    ####Determine the number of gates in the netlist##############################
    #print("The netlist filename identified is",netlist_filename,"\n")
    vector_doc = open(netlist_filename, 'r')
    lines2 = vector_doc.readlines()
    gate_type = []
    Total_gates = 0

    for gate in lines2[p7:p8]:
        gate_type.append(gate[2:25].strip().replace(' U5', '').replace(' U8', ''
    ).replace(' U', '').replace(' U7', ''))
        Total_gates = Total_gates + 1
                #break
                #for gate in gate_type:
        #print(gate_type, "\n")
    print("Total number of gates in selected "+netlist_filename+" gate-level
    netlist is: "+str(Total_gates),"\n")

    print(netlist_filename,"is identified for further processing. \n")
    #print("\t\t Benchmarrck circuit \t\t #FO/#Gates\n")
    def file_identity(netlist_filename, fanout_no):
        ##### Step 1. Read the mapped gate-level netlist
        vector_doc = open(netlist_filename, 'r')
```

```
64        lines = vector_doc.readlines()
65
66        ##### Step 2. Identify all the nets that connect the gates.
67        ########For list the nets that connect the gates###########
68        list_wire = []
69        list_input = []
70        list_output = []
71
72        my_string = ""
73        my_string2 = " "
74        for line in lines[p1:p2]:
75            my_string += line.strip()
76            less_string = my_string[6:]
77        new_string=less_string.replace(';', '')
78        my_list = new_string.split(",")
79        for x in my_list:
80            list_wire.append(x.strip())
81        #print("Internal wire(s) includes: ",list_wire,"")
82        #print()
83
84        oup_to_string = ""
85        for out_item in lines[p3:p4]:
86            #print(out_item)
87            oup_to_string += out_item.strip()
88            less_string = oup_to_string[6:]
89        new_string=less_string.replace(';', '')
90        my_list2 = new_string.split(",")
91        for x in my_list2:
92            list_output.append(x.strip())
93        #print("Output net includes: ",list_output)
94        #print()
95
96        inp_to_string = ""
97        for inp_item in lines[p5:p6]:
98            inp_to_string += inp_item.strip()
99            less_string = inp_to_string[6:]
```

```
100         new_string=less_string.replace(';', '')
101         my_list3 = new_string.split(",")
102         for x in my_list3:
103             list_input.append(x.strip())
104         #print("Input net includes: ",list_input)
105         #print()
106 
107 
108         miti_gate = []
109         line_string1 = ""
110         sum_fan_gate = 0
111         count = 0
112         gates_inv  = []
113 
114         ##### These codes are responsible for fanout  ###################
115 
116         num = 0
117         for x in list_wire:
118             for line in lines[p7:p8]:
119                 line_string1 = line.split(" ")
120                 for y in line_string1:
121                    # print(y)
122 
123                     #num = 0
124                     #if "AOI21_X1" in y:
125                     #   print(line)
126                     #    num = num + 1
127 
128                     ##### Step 4a. If a net is in line, identify the gates with
    it
129                     if x in y:
130                         for a in range(6,10):
131                             if y[4:a] in y and len(y[4:a])==len(x) and y[4:a+1].
    endswith(")") and y[4:a] == x \
132                                 or y[3:a-1] in y and len(y[3:a-1])==len(x) and y
    [3:a].endswith(")") and y[3:a-1]==x:
```

```
                                count = count + 1
                                ####Step 4a.i. count the number of gates connect to a gate and store them separately
                                while x:
                                    #print(line, y)
                                    miti_gate.append(line)
                                    #print(miti_gate)
                                    break

        ##### Step 5. Determine the number of gates and their instances with a similar number of fanouts
        gate_same_net = []
        # gates_inv  = []
        #gates_inv2 = []

        if count == fanout_no:
            for m in miti_gate:
                #print("m1: ",m, miti_gate)
                if x in m:
                    gate_same_net.append(m)

                    if "Y("+x+")" in m or "YN("+x+")" in m or "Z("+x+")" in m or "ZN("+x+")" in m:
                        #print("x: ",x , m)
                        sum_fan_gate = sum_fan_gate + 1

                        #if count < 6:

                        gates_inv.append(m[2:10].strip().replace(' (', '').replace(' U', ''))
                        #print(gates_inv)


            #### This line prints information about fanouts gate
            countg = 0
            for item in gate_same_net:
```

```
                countg = countg + 1
        miti_gate = []

        #gate_string = ""

        ##### Step 6: Reset the count. This is very important to reset the count
        count = 0

    if gates_inv != []:
        sumg = 0
        counta = 0

        seta =list(set(gates_inv))
        #print(seta)
        target_FO = 4
        if fanout_no-1 >= target_FO:
            print("For FO of ", fanout_no-1)
        else:
            print("#FO is less than ", str(target_FO))
        for a in range(len(seta)):
            for m in gates_inv:
                while m==seta[a]:
                    counta = counta + 1
                    break
            sumg = sumg + counta
            if fanout_no-1 >= target_FO:
                print(str(counta) + "\t" +seta[a])
                file = open(netlist_filename+"_fo_gates","a")
                file.write("\n")
                #file.write("For FO of " + str(fanout_no-1))
                file.write("#FO is " + str(fanout_no-1) + "\t"  + str(counta) + "\t" +seta[a])
                file.close()
                #print("Total is ", sumg)
            counta=0
```

```
199
200             print()
201     for p in range(2, 50):
202         file_identity(netlist_filename, p)
```