EFFECTS OF TOTAL-IONIZING DOSE ON CARBON NANOTUBE FIELD-EFFECT TRANSISTORS

By

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CHAPTER 1

Introduction

Today's population has grown accustomed to new computers and phones consistently getting smaller and faster. All of this is possible because of the doubling in the number of transistors that fit on an integrated circuit every year or two, as observed by Gordon Moore [1]. Moore's Law is not a natural inevitable phenomenon. It was originally presented as an observation and continued to be made true by the hard work of engineers over the five decades since it was observed. Moore's Law scaling would not have been possible without changes to device architecture and fabrication processes, such as using high-k gate dielectrics and moving to a finFET[1] architecture, which have enabled devices to continually shrink [2][3][4]. However, now that silicon transistors are approaching the 3nm technology node, warnings about the end of Moore's Law are growing [5][6]. Integrated circuits are facing a "Power Wall," where the required power for an integrated circuit is no longer scaling, and a "Memory Wall," where processors spend most of their time accessing data instead of performing computations Researchers have been studying alternatives to silicon transistors for decades, searching for technology that can perform and scale better than the silicon complementary metal oxide-semiconductor (CMOS) integrated circuits. Meanwhile, engineers are continuing to develop alternate architectures to address problems like the Power Wall and Memory Wall to increase performance.

One interesting alternative transistor technology that may improve both transistor performance and architecture is carbon nanotube field effect transistors (CNTFETs). CNTFETs use carbon nanotubes (CNTs) as an alternative channel material between the drain and the source. CNTFETs offer several advantages over silicon CMOS technology. By way of example, CNTFETs have excellent electrostatic

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[1] A finFET is a MOSFFET where the drain/source channel is raised above the plane of silicon and the gate wraps around that channel. This allows for greater control over the channel by the gate and increases the effective width resulting in higher transistor drive current and superior short channel behavior compared with planar MOSFETs[3].

control and high carrier transport [7]. Additionally, the higher drive strength of CNTFETs offers an energy efficient solution, promising a nine times lower energy delay product (EDP) when compared with silicon finFETs [8]. Another advantage is that CNTFETs can be fabricated at lower temperatures than CMOS, which allows multiple layers to be fabricated on top of each other [9].

The ability to fabricate layers of heterogeneous circuitry in a monolithic stack is the idea behind the DARPA 3DSoC program. The Three Dimensional Monolithic System-on-a-Chip (3DSoC) program seeks to improve memory access time by including logic and memory circuitry together in layers on a single die stack. The System-on-a-Chip (SoC) will combine CMOS, resistive-RAM (RRAM), and CNTFETs into one 3D chip [10]. This new 3D architecture utilizes CNTFETs' lower fabrication temperatures, allowing the stacking of many layers. The program seeks to include up to 4 GB of memory in the SoC, which will allow the logic to access the data faster and with less energy to decrease the memory access power to less than 2 pJ/bit [11]. These improvements result in increased performance without increased density scaling, and a 90nm CNTFET/RRAM 3D process is predicted to exceed the performance of a current 7nm CMOS process [12].

The 3DSoC program aims to create these monolithic stacked integrated circuits for government and DoD customers, including as an area of interest the technology's application in radiation environments. For electronics to operate in space, or other radiation environments, they must continue to function after being subjected to a total-ionizing dose (TID) of radiation. Exploratory testing is necessary to determine how a given technology will perform in a radiation environment and to plan for mitigation of radiation effects. In addition, low-frequency noise (LFN) testing both before and after TID irradiation can provide insight into the nature and density of defects in the oxides used in the transistors and can inform on the mechanisms of the TID response. In doing so, testing will elucidate the response to dose and reveal the underlying mechanisms. The goal of the research described in this thesis was to perform a TID testing campaign on the CNTFETs developed for the 3DSOC program. TID response data were collected for three different generations of CNTFETs, providing an initial understanding of the TID hardness of this technology.

CHAPTER 2

Background

2.1. Total-Ionizing Dose

Total-ionizing dose (TID) refers to the amount of energy deposited by ionizing radiation per unit mass and is typically measured in rad, which measures energy absorbed per unit mass of a specific material. TID can cause electrical performance degradation that impacts the operation of semiconductor devices. The ionizing dose comes from the interaction of high energy photons or charged ions (protons, electrons, or heavy ions) with an insulator. When an oxide used in a semiconductor device is subjected to ionizing radiation, electron-hole pairs can be generated [14][15], as shown in Fig. 2.1 (1). The electrons, which have higher mobility than holes, are quickly swept out of the oxide [16], Fig 2.1(1), while the holes are left to slowly move through the oxide [14], Fig 2.1 (2).

Imperfections in the oxide can cause some of the mobile holes to become trapped in the oxide in what are called oxide traps [17], Fig 2.1 (3). The positive charge of the trapped holes in the oxide degrades the performance of the semiconductor device. Additionally, during irradiation, hydrogen ions can be released and travel to the interface, where they may become trapped by dangling bonds at the semiconductor-insulator interface [18], shown in Fig 2.1 (4). This is known as an interface trap. A third type of trap is a border trap, which occurs in the near inter-facial oxide but otherwise behaves like an interface trap [19]. In traditional silicon CMOS, the dominant defect that causes oxide and border traps is an oxygen vacancy, and the dominant defect that causes interface traps is a dangling Si bond [14][20].

The charge located in the oxide trap shifts V_{GS} negatively while the interface and border traps cause the subthreshold swing to increase [21]. As modern transistors became smaller, the gate oxides also shrunk and the TID effects lessened significantly [22]. However, more recent technologies, including CNTFETs, use high-k dielectrics for the gate oxide instead of SiO_2. The TID response of transistors with these gate stacks became more complex [22], and the effects more pronounced, than previous technologies using

silicon dioxide. Initial studies of high-k dielectrics demonstrated high defect densities relative to SiO_2 and increased susceptibility to the effects of TID [23].

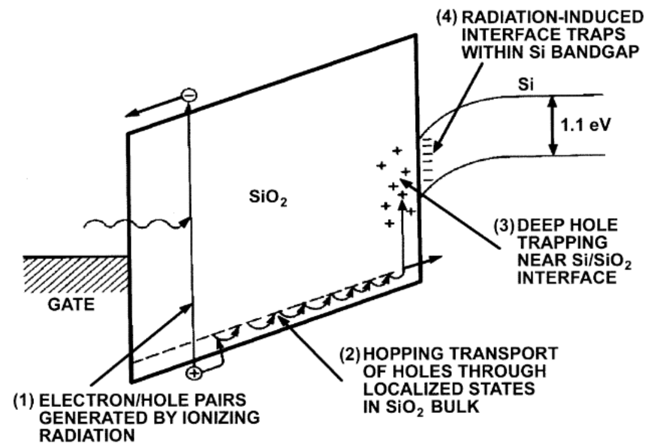


Figure 2.1 – Diagram showing the mechanisms of TID in SiO_2. Electron/hole pairs are generated from radiation. The electrons are quickly swept away leaving holes to move relatively slowly to the oxide/semiconductor interface. A fraction of the holes become trapped in the oxide bulk. Other holes are trapped in the interface border region. As the holes move, some Hydrogen ions are released and travel to the interface, where they interact with dangling Si bonds [14].

2.2 Low-Frequency Noise

Measuring low-frequency noise in devices can provide an estimate on the density of border traps and insight on the nature of the defects in an oxide [37]. 1/f noise is observed in a number of physical systems including biased electronic devices [37][38]. A. L. McWhorter modeled 1/f noise in semiconductors as charge carrier number fluctuations [65]. Later, Duta, Dimon, and Horn developed a model to infer defect energy distributions from LFN measurements [38]. The Dutta and Horn model was originally used to describe noise of thin metal films [38] but was eventually used to characterize MOS devices [39] and has since been used with other emerging semiconductor technologies such as SiC and GaN [40][41].

In the context of CMOS devices, a significant amount of experimental and theoretical work on 1/f noise has shown the dominant defect in SiO_2 is an O vacancy [42]. Similarly, modern transistors, which

often use high-k dielectrics such as HfO_2, have demonstrated the dominant defect is also an O vacancy [43][44]. Past studies have shown that the measured room temperature 1/f noise is correlated to the post-irradiation threshold voltage shift in MOS devices [56]. Low-frequency noise testing on CNTFETs therefore has the potential to give first order estimates of defect densities in the oxides and combined with further theory calculations can facilitate the identification of the defect microstructures.

2.3. Carbon Nanotube Field Effect Transistor Construction and History

Carbon nanotube field effect transistors (CNTFETs) are gate-controlled field effect transistors that use single walled carbon nanotubes (SWCNT) as an alternative channel material between the source and drain. The SWCNTs are graphene sheets rolled into tubes with a diameter of ~1 nm. The SWCNTs in the channel form a Schottky contact with a metal source/drain and the gate controls the current flow through the CNTs. To date, CNTs have formed single transistors [24], simple logic gates [25], simple circuits [26], and small microprocessors [27]. Historically, however, there have existed several issues with CNTs that have made VLSI circuits containing CNTFETs difficult to fabricate.

First, CNTFETs are inherently PFETs, and previous efforts to create NFETs from CNTFETs have been unsuccessful [28]. One solution utilizes low work function metals for the source/drain contacts to lower the Schottky Barrier, which enables electron transport through the CNTs, as shown in Figure 2.2. In addition, surrounding the CNTFETs with different oxides—hafnium oxide for NFETs or silicon oxide for PFETs—further modifies the Schottky barrier and allows for tunability of the transistors [29].

Next, carbon nanotubes have a material defect in which a certain percentage of CNTs will be metallic instead of the desired semiconducting CNTs. The metallic CNTs have little to no bandgap and degrade performance of CNTFETs by increasing off-state leakage current, worsening noise margins, and resulting in incorrect logic functionality [30]. For example, metallic CNTs can affect logic stages differently depending on how they are implemented in both the schematic and layout, and certain implementations can result in a worse static noise margin (SNM) [27]. One potential solution developed by the Massachusetts Institute of Technology is called DREAM (designing resiliency against metallic CNTs). The DREAM

process overcomes the presence of metallic CNTs by using standard EDA tools that account for the possibility of metallic CNTs during the design flow. DREAM works during logic synthesis to create logic functionality by avoiding combinations that are most susceptible to metallic CNTs [27].

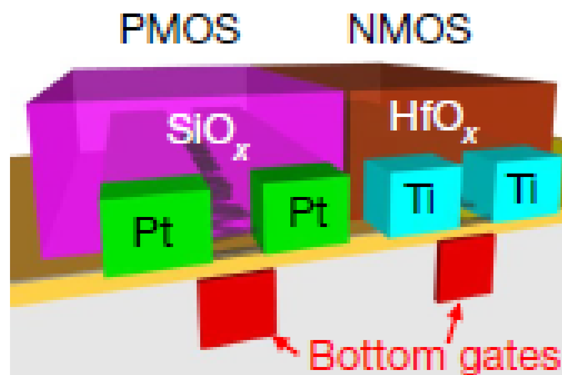


Figure 2.2 – Illustration showing a relative depiction of the structure of the CNTFETs used in this research. The transistors are comprised of a bottom metal gate with the CNTs in the channel above connecting a metal source and drain. The CNTFET is then surrounded with a non-stoichiometric oxide to electrostatically tune the transistor. Note the PMOS vs NMOS differences with the different Drain/Source metals and surrounding oxides [27].

2.4 MIT CNTFETS

Three different lots of transistors were tested during the research described in this thesis. The initial Lot 1 CNTFETs were received in December 2020, Lot 2 transistors were received in April 2021, and the Lot 3 transistors were received in August 2021. All three lots of CNTFETs contain a metal bottom gate with the gate dielectric above, which is a mixture of Al_3O_2 and HfO_2 [27]. A layer of CNTs is then deposited and etched away, except for the area over the gate. For Lot 1 and Lot 2 transistors, the metal used for the PMOS source and drain is primarily titanium while the metal in NMOS source/drains is primarily platinum. Surrounding the transistor is the oxide layer of either SiO_X around the PMOS or HfO_X around the NMOS, for electrostatic tuning of the threshold voltage [29]. The use of the non-stochiometric oxides, SiO_X and HfO_X, enables control of the Schottky Barrier height by controlling the stoichiometry of the oxides [29]. A

basic illustration of the Lot 1 and Lot 2 transistors is show in Figure 2.2, and an illustration of the fabrication process for those first two lots is shown in Figure 2.3.

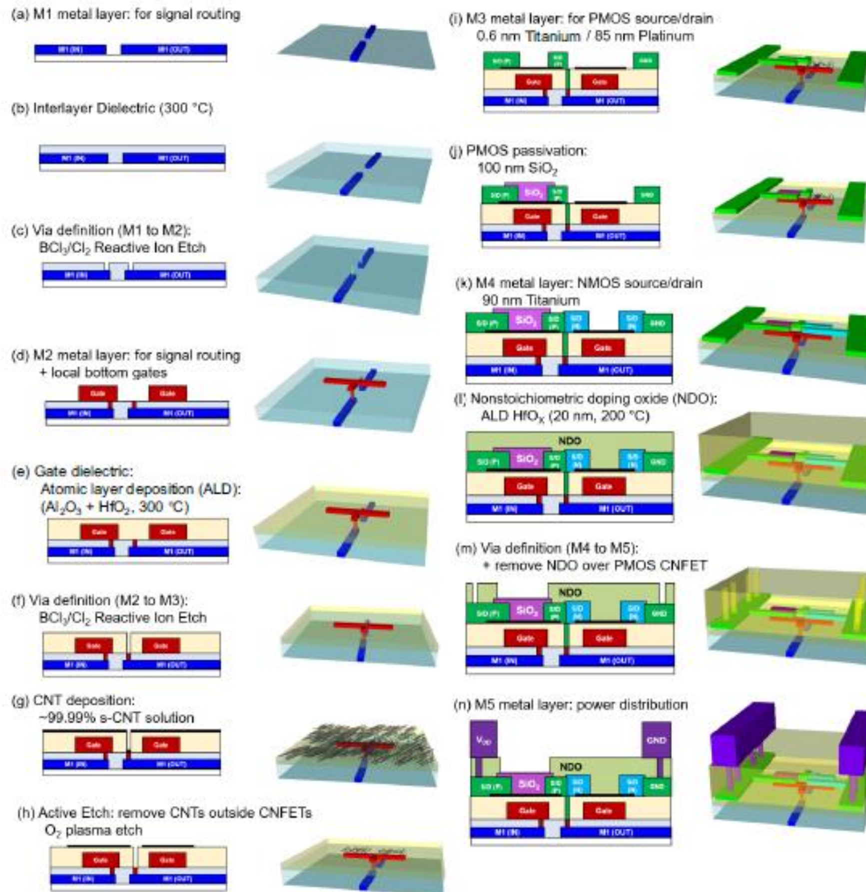


Figure 2.3 – Illustration depicting the fabrication flow constructing Lot 1 and Lot 2 CNTFETs [27].

The Lot 3 transistors are similarly constructed, except that the metal for the source and gate is deposited using a lift-off-free process which makes it compatible with current CMOS tools used in modern fabs [32][33]. The original CNTFETs used a non-standard metal evaporation and lift-off to remove the CNTs outside the channel and create the metal source/drain contacts. This was done because traditional plasma etching will destroy the CNTs in the channel. However, the lift-off procedure has a reduced yield and results in reduced transistor performance. In the lift-off-free process, an Al_2O_3 mask covers and protects the CNTs in the channels during plasma etching.

Another difference in the new process is the source and drain metals—Ti/TiW and W for NMOS and PMOS respectively. Both variations are then surrounded by the same AlO_X oxide. In Lot 3, the NFETs and PFETs are created entirely through the work function engineering in the contact between the SWCNTs and the metal drain/source, rather than through electrostatic tuning using surrounding oxides. An illustration of the Lot 3 transistor is shown in Figure 2.4.

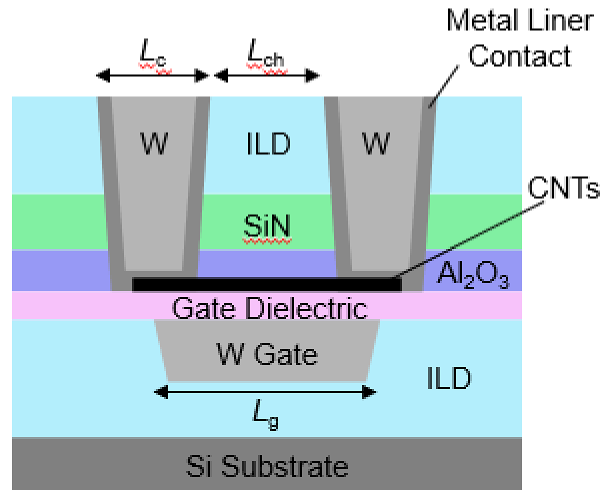


Figure 2.4 – Illustration depicting the cross section of Lot 3 transistors [32]. The bottom gate is made of tungsten and the gate dielectric is a mix of hafnium oxide and aluminum oxide. The ILD is a low-k interlayer dielectric surrounding the rest of the CNTFET. The Al_2O_3 is deposited via atomic layer deposition and is a hard mask used to protect the CNTs during dry etching of the contact holes.

2.5 CNTFET Response to TID

Past TID testing on CNTFETS has shown some potential susceptibility to TID-induced voltage shift [34]. TID in CNTFETs affects the surrounding materials, causing device degradation through trapped charge or Schottky barrier height modification [35]. Cress et al. show CNTFETs exhibiting 0.8 V shift at 2 Mrad (SiO_2) [34]. Other testing has shown various amounts of I-V curve shift depending on the specific CNTFET architecture [35][36].

CHAPTER 3

Pre-radiation Electrical Characterization

A series of electrical characterization tests were performed to separate transistor I_{DS}-V_{GS} curve differences caused by either TID or operational/testing stress.

3.1 Electrical Characterization Testing Setup

In all tests, the CNTFETs were connected to an HP4168B Parameter Analyzer, pictured in Figure 2.3 (a). The parameter analyzer was used to measure current and voltage (I_{DS}-V_{GS}) characteristics before irradiation and between each irradiation step. The parameter analyzer was also used for all bias voltages. For all I_{DS}-V_{GS} sweeps, the gate voltage was swept from negative 1.8 V to positive 1.8 V, and each sweep occurred at a set drain voltage, dependent on the lot of CNTFET being tested. All Lot 1 and Lot 2 transistors were swept from a V_D of 0.1 V to a V_D of 1.8 V, while all Lot 3 transistors were swept from a V_D at 50 mV to a V_D at 800 mV. The initial Lot 1 experiments were performed by probing the pads of the transistor on the die, and later, Lot 1 experiments were performed with the pads wire-bonded to a package for testing. The picture in Figure 3.1 shows the surface of a Lot 2 die with the columns and rows of probing pads visible. Figure 3.2 shows the electrical probing station that was used for all probe testing on the three lots.

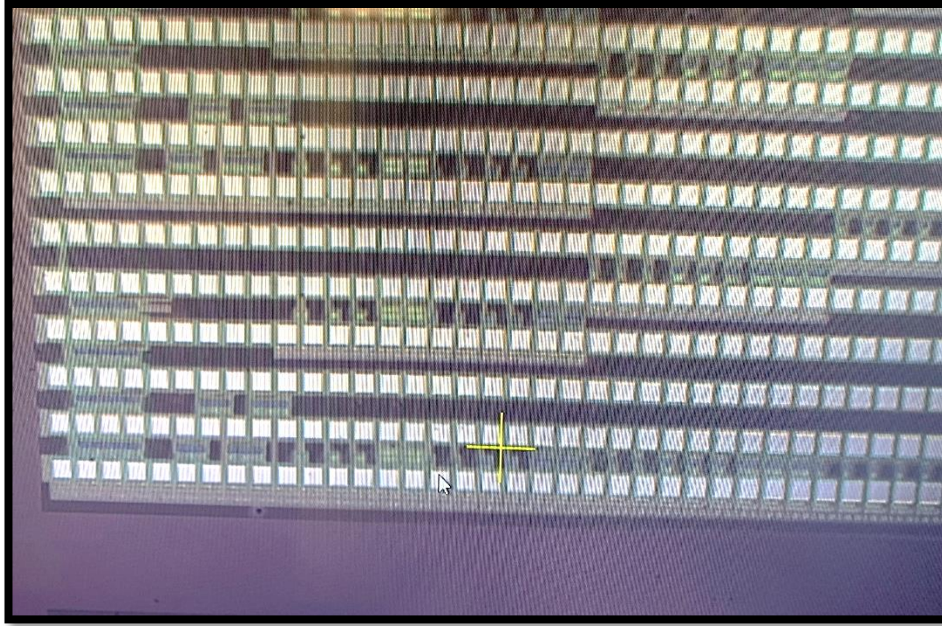


Figure 3.1 – Image of Lot 2 die surface. Each column contained different types of test devices. Each individual transistor had three probe pads for the gate, drain, and source. The probe pads are the large square surfaces in rows and columns on the die.

Upon receipt of the CNTFETs, I_{DS}-V_{GS} data were obtained to establish a baseline prior to radiation testing. These experimental transistors show variability in I_{DS} vs V_{GS} curves between transistors and between different sweeps of the same transistor.

Figure 3.2 – Electrical probing station used to characterize the CNTFETs before bonding and irradiation. Metal tips were used to contact the probe pads of a transistor to connect to the HP4168B Parameter Analyzer for measurement and biasing.

Before any testing took place, the transistors were baked in an attempt to anneal out any contamination that may have accumulated from being stored in air and humidity during transportation to Vanderbilt. The Lot 1 transistors were baked at 100°C in a vacuum overnight for 14 hours. For Lot 2 and Lot 3, an updated procedure was used: these lots were baked in nitrogen at 300 degrees Celsius for five minutes to anneal out any moisture. The transistor I_{DS}-V_{GS} curves before and after bake were compared, and the results are shown in Chapter 3.2.

The next test required biasing the transistors for the same amount of time as the transistors would be biased during irradiation in either a simulated ON state or negative gate bias state. This test aimed to find any degradation in current-voltage characteristics from electrical stress. I_{DS}-V_{GS} sweeps were taken at

1, 3.3, 6.6, 9.9, 16.5, and 33 minutes of total time biased. These times correspond with the amount of time the device would be biased for the six TID levels used in irradiation testing.

Additionally, multiple IDS-VGS sweeps were performed on the devices in rapid succession to delineate stress caused by time under bias from stress caused by the I-V sweeps. The multiple sweep tests served to determine if the control stress was caused by the time under bias or the stress from the seven I-V sweeps.

A hysteresis test was performed, where the I_{DS}-V_{GS} was swept from a negative gate voltage to a positive gate voltage, and then from a positive gate voltage to a negative gate voltage. Hysteresis is a known effect in CNTFETs [45][46][47] and this test quantified the amount in the transistors used in this research.

3.2 Characterization Results

3.2.1 Vacuum / Nitrogen Bake

The vacuum bake used on the Lot 1 transistors showed a small change in I_{DS}-V_{GS} characteristics, depicted in Fig. 3.3. The nitrogen bake used on Lot 2 and Lot 3 devices showed similar results, depicted in Fig 3.4. These negligible changes suggest that results from the other tests will be relatively free of the effects of contamination from the air and moisture.

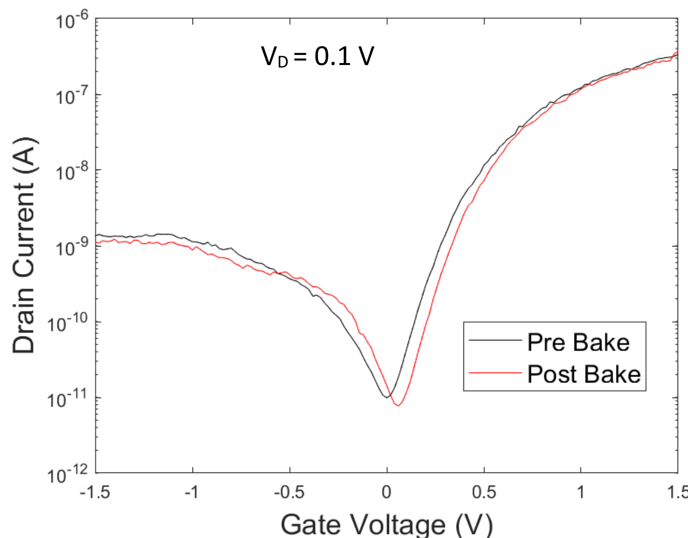


Figure 3.3 – Lot 1 vacuum bake results showing a single transistor's I-V curves both before and after the bake. The vacuum bake did not cause a noticeable change in the I-V curves of the Lot 1 transistors.

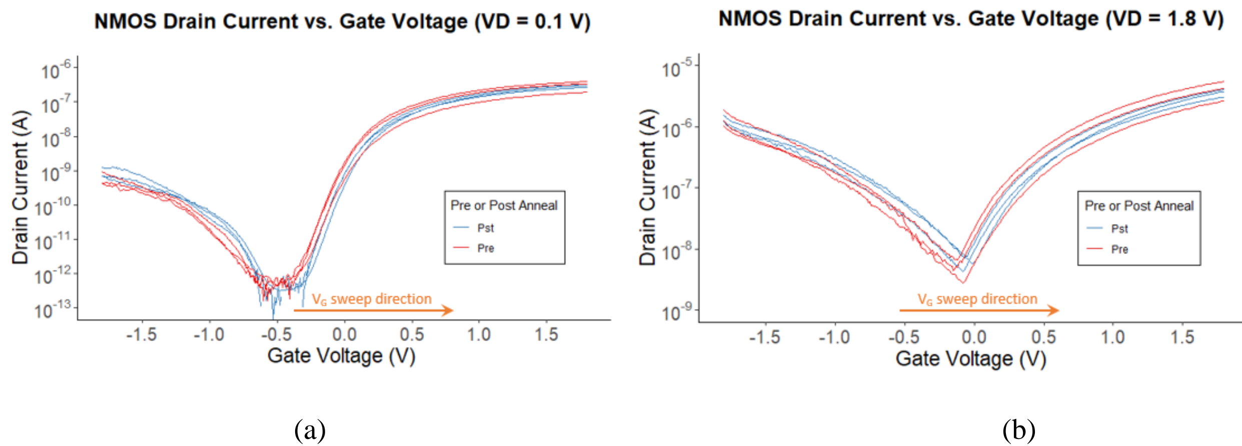


Figure 3.4 – Lot 2 nitrogen bake results. These graphs show several I-V sweeps on a transistor both before and after the bake. (a) shows the V_G sweep at a V_D of 0.1 V and (b) is a V_D of 1.8 V. The nitrogen bake did not cause a change in I-V curves of the Lot 2 transistors.

3.2.2 Sweeps

Multiple consecutive sweeps showed no trend in the Lot 2 transistors, depicted in Fig. 3.5. By contrast, the ten consecutive sweeps on the Lot 3 transistors, Fig. 3.6., showed a slight shift of the I-V curves to the left by about 0.2 V.

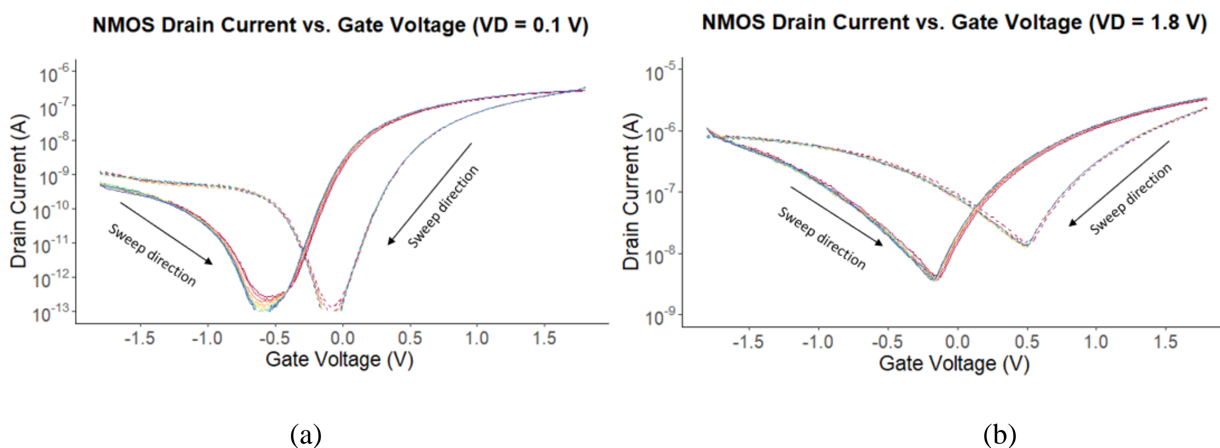
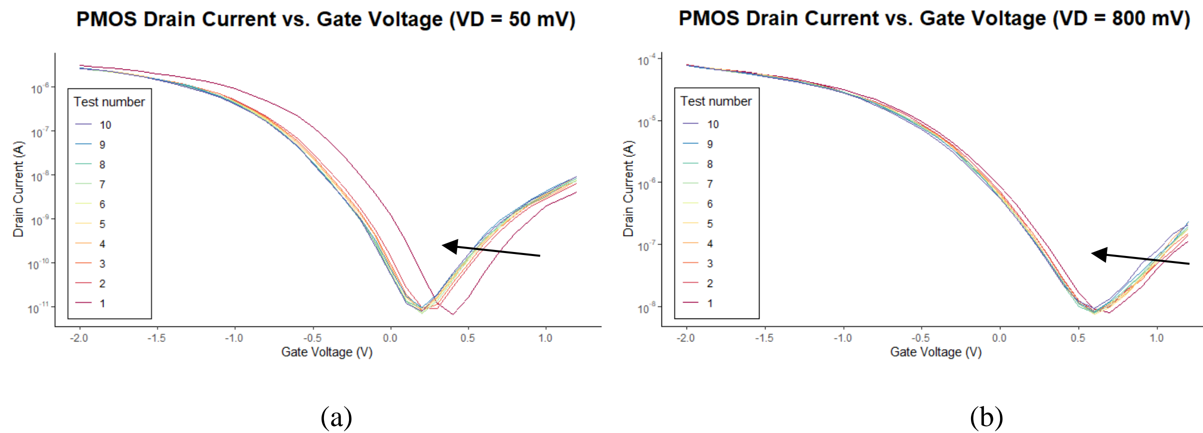


Figure 3.5 – Lot 2 consecutive sweep testing. The transistor was swept ten times in the negative to positive V_G direction and ten times in the positive to negative V_G direction. The lot 2 transistors did not show any change from the multiple sweeps.



(a) (b)

Figure 3.6 – Lot 3 transistors were also swept ten consecutive times. However, these newer tranisistors exhibited some shift to the left after ten sweeps.

3.2.3 Hysteresis

Fig. 3.7 shows Lot 2 CNTFETs exhibited a shift of around 0.5 V in the I_{Ds} vs V_{GS} curves, dependent on whether the gate voltage sweep was positive to negative or negative to positive.

This hysteresis in CNTFETs is a known problem, caused by interface traps and surface traps [47]. The interface traps are located at the interface between the CNT (semiconductor) and dielectric (insulator). Surface traps are similar, but they are at the surface of the dielectric that is not in contact with the CNTs. These two types of traps charge or discharge depending on the sweep direction, affecting the I_{DS} vs V_{GS} curves. Previous research has estimated that the number of interface traps at the CNT/oxide interface is higher than other semiconductor/insulator pairs resulting in the high level of hysteresis shift [45].

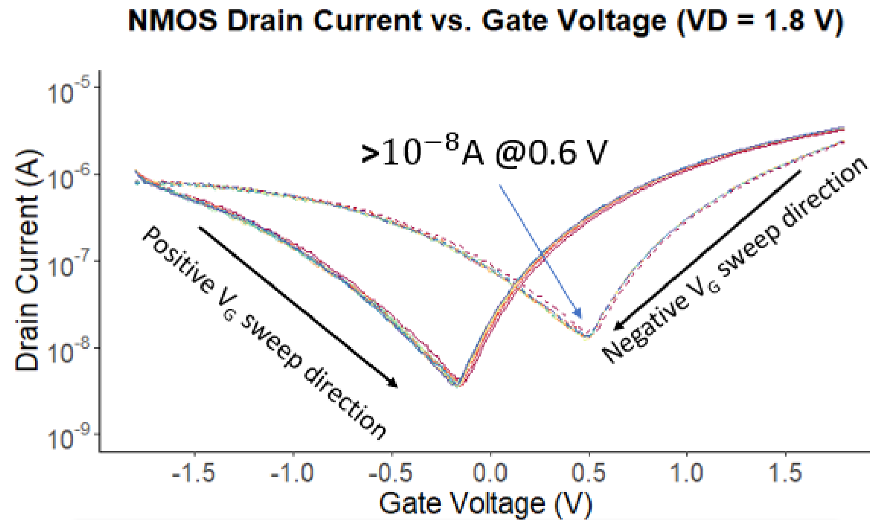


Figure 3.7 – Lot 2 transistors exhibiting hysteresis. Note the 0.5 V difference between a negative to positive sweep and a positive to negative sweep.

Comparing Lot 2, Fig. 3.7, with Lot 3, Fig. 3.8, the newer transistors exhibited approximately 0.5 V less of a hysteresis shift than the earlier lots of transistors. All control and TID tests for Lot 3 transistors will show curves taken with V_G swept from negative to positive.

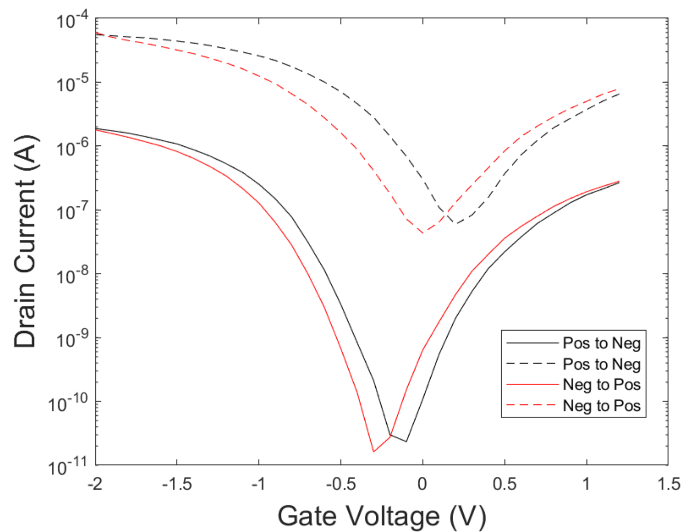


Figure 3.8 – Lot 3 transistors exhibited less hysteresis compared to Lot 2.

3.2.4 Control Stress Test

3.2.4.1 Lot 1

The Lot 1 control test, Fig. 3.9, showed the CNTFETs were affected by being biased in the ON state for the duration of a TID test. The voltage shift to the positive indicates electrons trapped in interface traps [51] or in oxide traps formed from oxygen vacancies in the dielectric [54]. HfO_2 has a propensity to form oxygen vacancies that trap carriers (electrons or holes) [57]. The electrons arrive in the traps through hot carrier injection, where electrons accelerated in the channel obtain enough energy to inject into the gate dielectric [51].

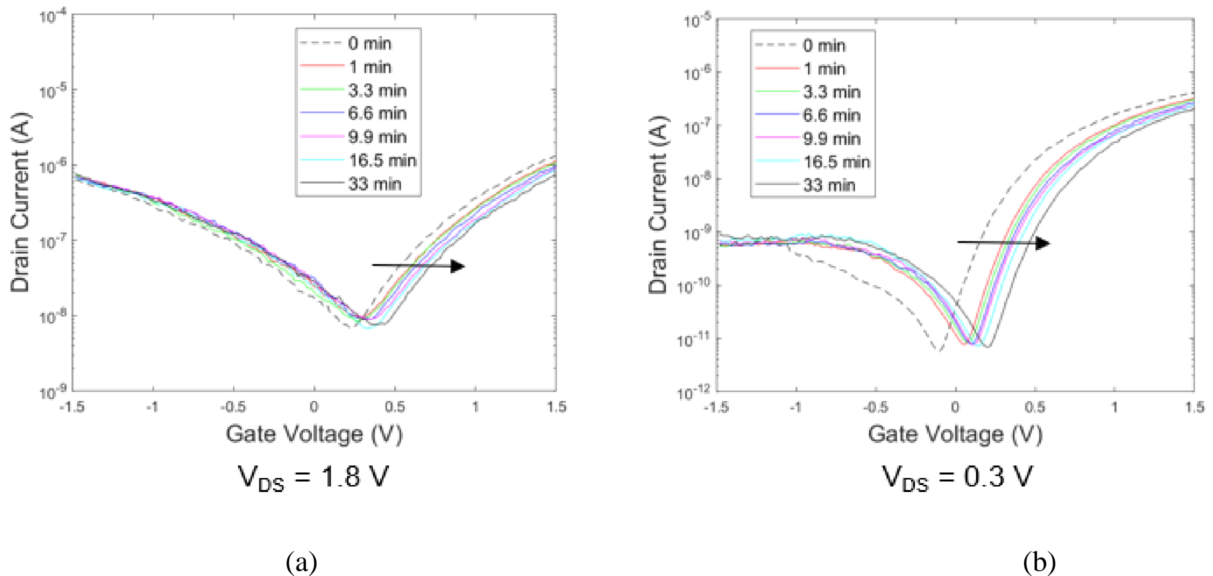


Figure 3.9 – Lot 1 control stress test. (a) is the plot of I-V curves taken at a V_{DS} of 1.8 V and (b) is the plot of I-V curves taken at a V_{DS} of 0.3 V. This test shows a positive voltage shift from being biased in the ON state for a total of 33 mins.

3.2.4.2 Lot 2

Lot 2 shows similar results, with the I_{DS} vs V_{GS} curves positively shifting when the gate is under a positive bias, shown in Fig. 3.10. This positive I_{DS}-V_{GS} shift is caused by the positive voltage on the gate leading to electron trapping in the gate dielectric [54], similar to the Lot 1 results. Fig. 3.11, depicts the

results of Lot 2 transistors with a negative gate bias. The negative voltage on the gate caused the I-V curves to shift to the left caused by holes trapped in the oxide [55].

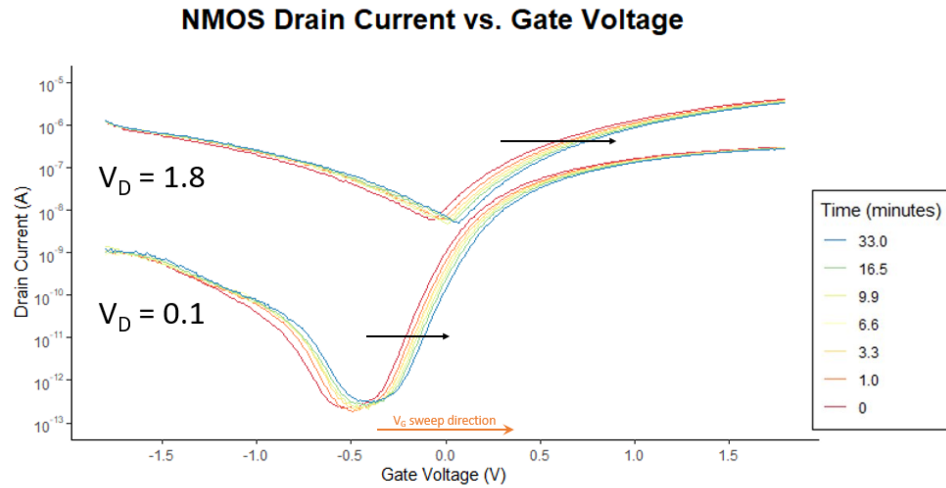


Figure 3.10 – Lot 2 Control stress testing with gate biased at a positive voltage. The positive I-V curve shift is due to electron trapping in the gate oxide.

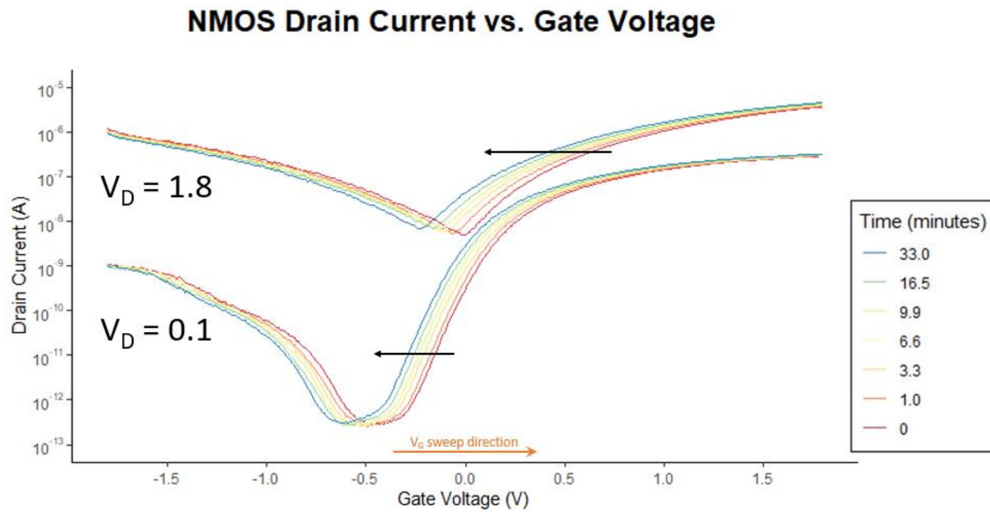
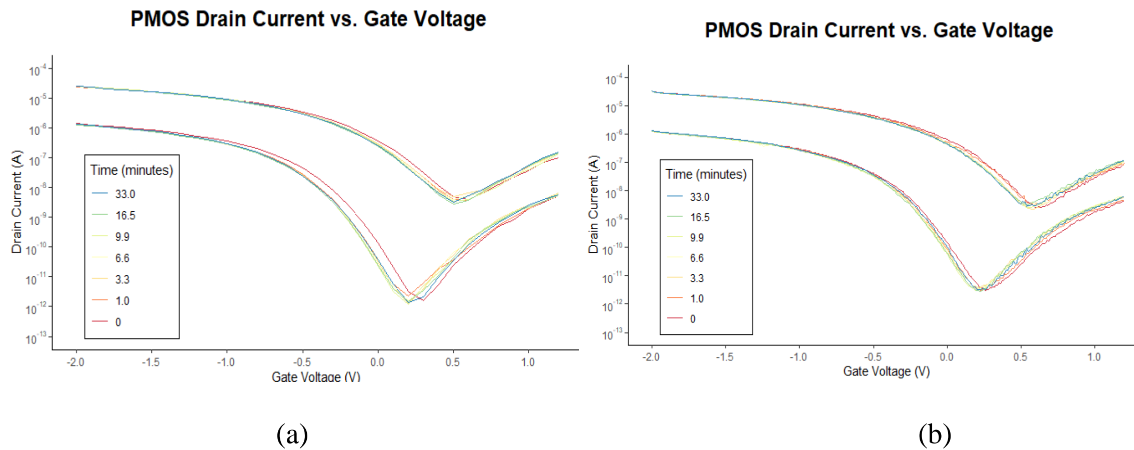


Figure 3.11 – Lot 2 Control stress testing with gate biased at a negative voltage. The negative I-V curve shift is due to hole trapping in the gate oxide.

3.2.4.3 Lot 3

The Lot 3 control test shows no noticeable curve shifts compared with the first two lots. Both the positive gate bias, Fig. 3.12(a), and the negative gate bias, Fig 3.12(b), showed no trend in the I_{DS}-V_{GS} curves over the 33-minute test. This is potentially a result of a maturing fabrication process between the different lots.



(a) (b)

Figure 3.12 – Lot 3 control test showing no shift from the gate biased for 33 minutes with a (a) negative voltage and a (b) positive voltage.

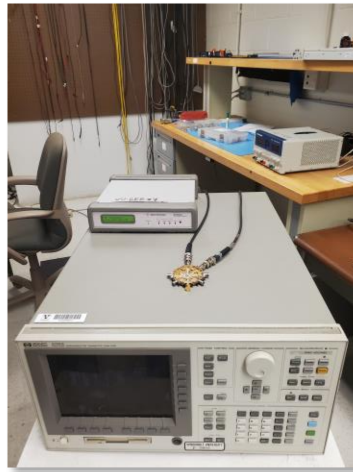
All the electrical characterization tests combined to show how these transistors were affected by normal operation and testing stress. This allowed the effects of TID to be extracted from the testing data. Additionally, the results of the control stress test and the hysteresis test indicate a large number of defects in the oxides that can trap charge. This suggests that these CNTFETs will be susceptible to the effects of TID-induced charge trapping.

CHAPTER 4

Total-Ionizing Dose Characterization

4.1 Total-Ionizing-Dose Experiment Setup

The devices were biased and measured with the HP4168B, Fig. 4.1(b), exactly as in the electrical characterization test. Lot 1 TID testing was performed with the die pads probed, Lot 2 TID testing was performed with the die bonded, and Lot 3 testing was performed with probes because the tungsten pads precluded bond wires from successfully adhering to the pads. All TID experiments were performed with the ARACOR X-ray machine in Figure 4.1(b). During irradiation, the parameter analyzer was used to bias the device in one of several bias conditions. In the OFF-Bias condition, the Drain was biased high, and the Gate was biased low. In the ON Bias condition, the Gate was biased high, and the Drain was biased low. This was done to measure the difference that an electric field across the gate oxide has on the TID response. In the TID experiments, the transistors were irradiated at a rate of 30.3 krad (SiO_2)/min to a level of 30 krad (SiO_2), 100 krad (SiO_2), 200 krad (SiO_2), 500 krad (SiO_2), and 1000 krad (SiO_2). Since the threshold voltage (V_{TH}) was unknown, a voltage at a fixed current was used to compare I_{DS} vs V_{GS} curves.



(a) (b)

Figure 4.1 – (a) is a picture of the HP4168B Parameter Analyzer used to set the voltages and measure the drain current; (b) is the ARACOR 10 keV X-Ray source used to deliver ionizing radiation in TID testing.

4.2 CNTFET Response to TID

The following sections show the data from TID testing on all three lots in the different bias configurations.

4.2.1 Lot 1 Results

The Lot 1 CNTFETs show significant I_{DS}-V_{GS} curve shift in response to total-ionizing dose. This shift is seen in both the OFF-bias test, Fig. 4.2, and the ON-bias test, Fig. 4.3, and suggests radiation-induced hole trapping in the gate dielectric and surrounding oxides [42][55].

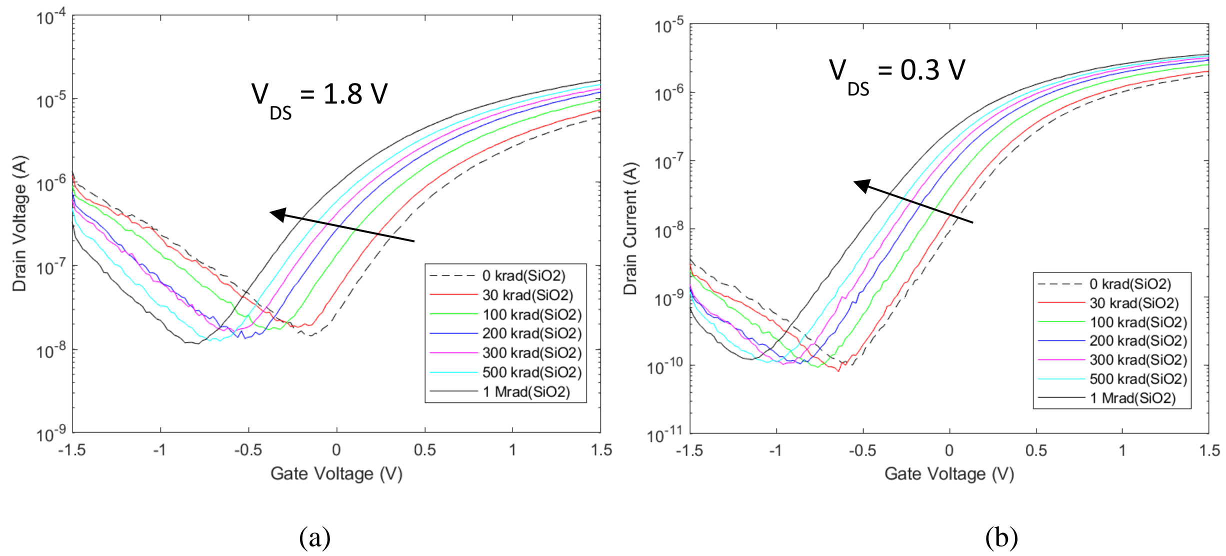


Figure 4.2 – TID results for Lot 1 CNTFETs in the OFF bias condition.

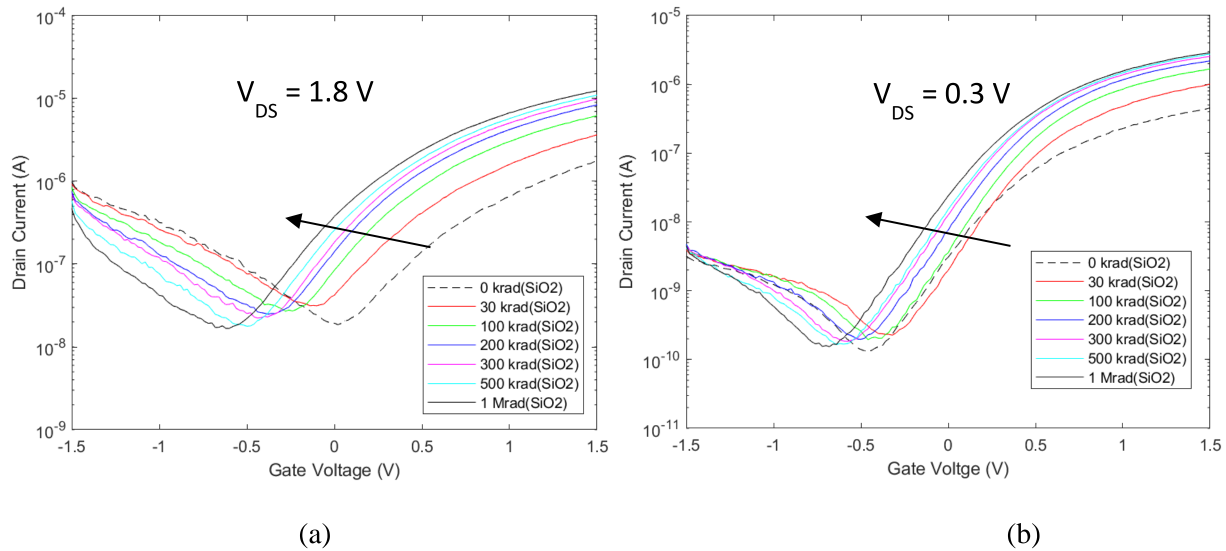
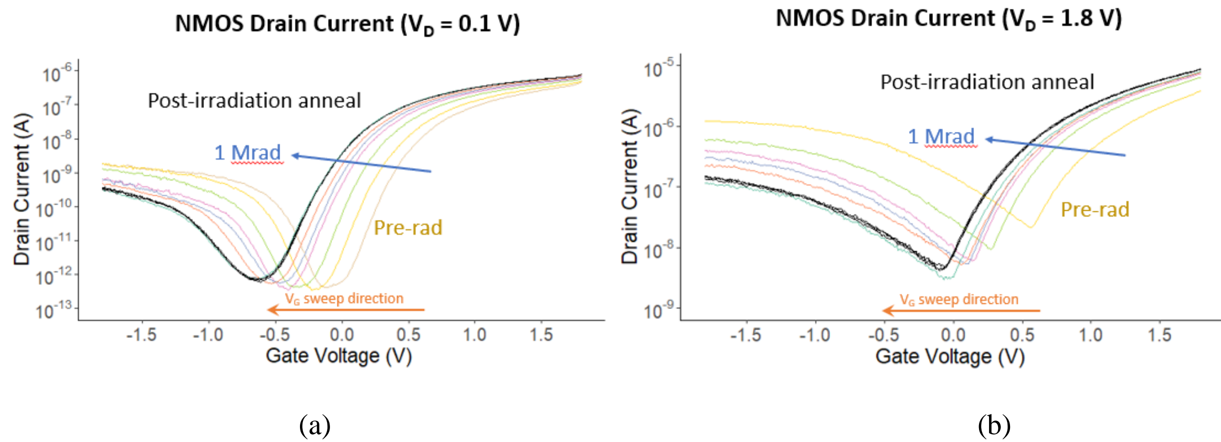


Figure 4.3 – TID results for Lot 1 CNTFETs in the ON bias condition.

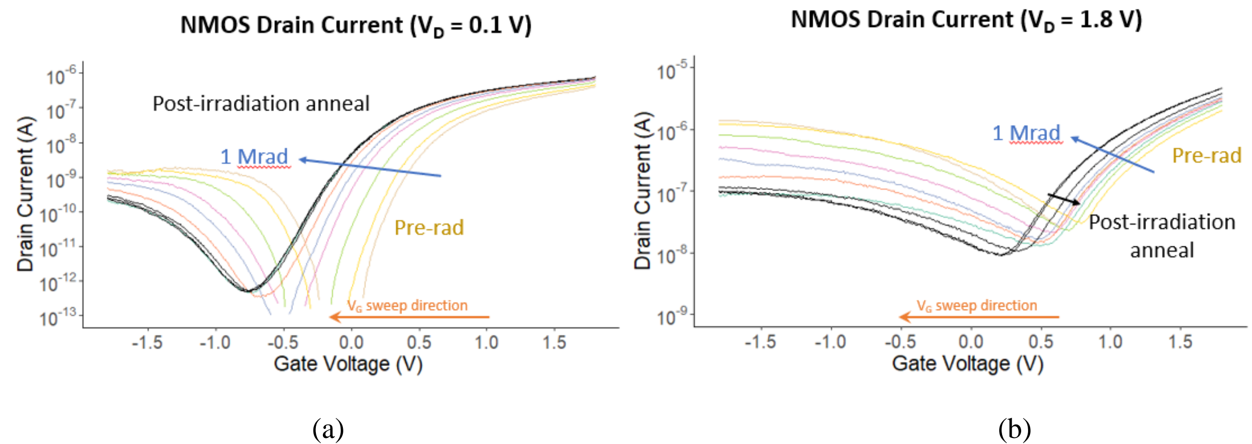
4.2.2 Lot 2 Results

The Lot 2 CNTFETS also show significant negative threshold voltage shift with dose, depicted in Fig. 4.4 and Fig. 4.5. These results are similar to the Lot 1 results.



(a) (b)

Figure 4.4 – TID results for LOT 2 CNTFETS in the OFF Bias.

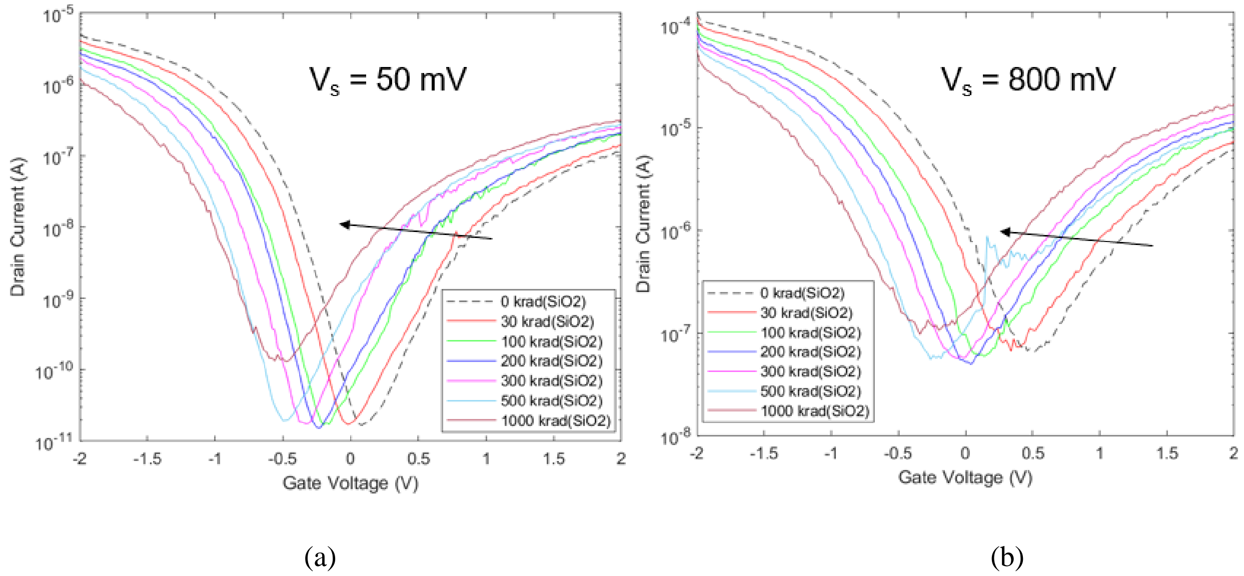


(a) (b)

Figure 4.5 – TID results for LOT 2 CNTFETS in the ON Bias.

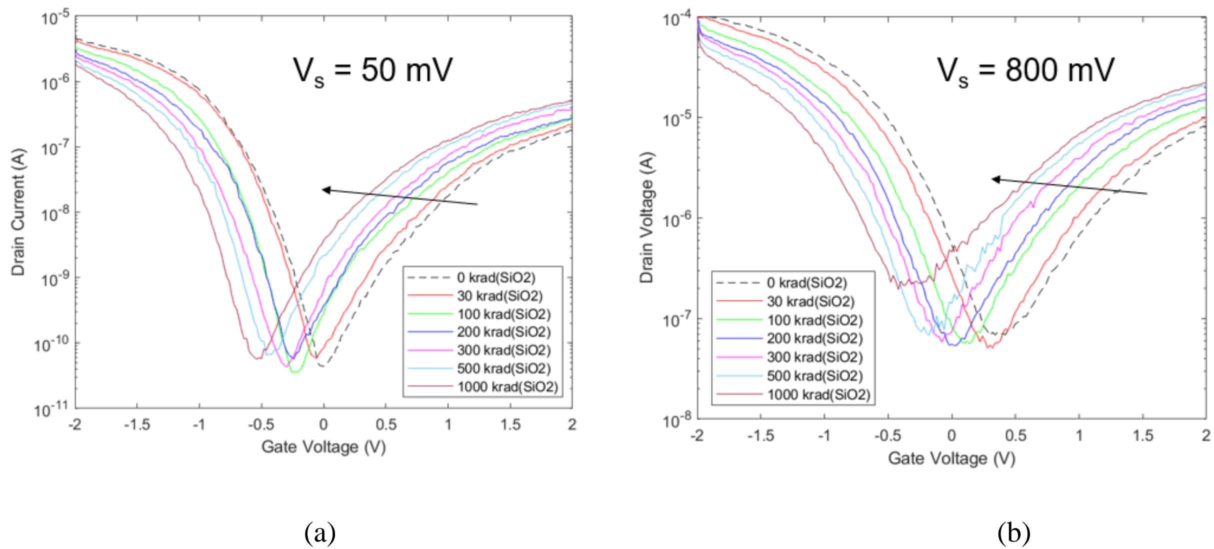
4.2.3 Lot 3 Results

Lot 3 TID testing also showed a similar negative I_{DS}-V_{GS} curve shift in both the ON-bias, Fig. 4.6, and the OFF-bias, Fig. 4.7, test conditions.



(a) (b)

Figure 4.6 –TID results for Lot 3 CNTFETS in the On Bias condition.



(a) (b)

Figure 4.7 – TID results for Lot 3 CNTFETs with the gate biased in an OFF-bias condition.

4.2.4 Summary of TID Results

The three lots cover three different generations of fabrication processes and both NFETs and PFETs. All the lots show similar significant susceptibility to TID. The range of V_T shifts is 0.6 V to 0.8 V at a dose of 1 Mrad (SiO_2), depicted in Fig 4.8 and Fig. 4.9. After the irradiation to 30 krad (SiO_2), the

CNTFETs had a V_{TH} shift percent change of 10-50%. The average percent change of the V_{TH} over all lots at 1 Mrad (SiO_2) was 155%. The TID voltage shift values were consistent across the three lots even though they represent different manufacturing processes.

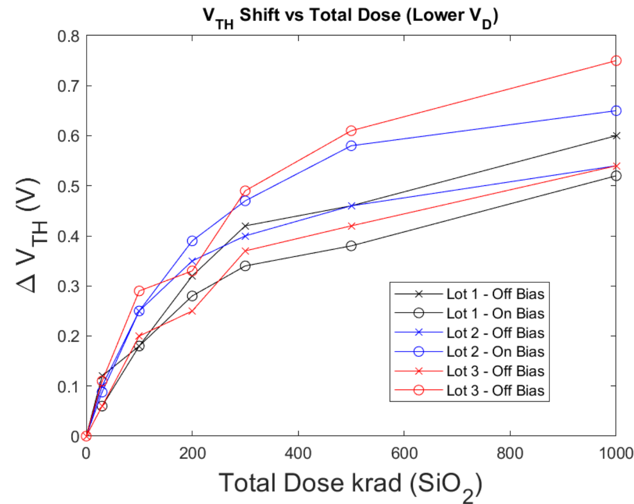


Figure 4.8 – Comparison of total change in threshold voltage for each TID level for all lots and bias configurations. This plot compares all the I_{DS} vs V_{GS} curves taken at the lower V_D, which was 0.1 V for Lot 1 and Lot 2, and 50 mV for Lot 3.

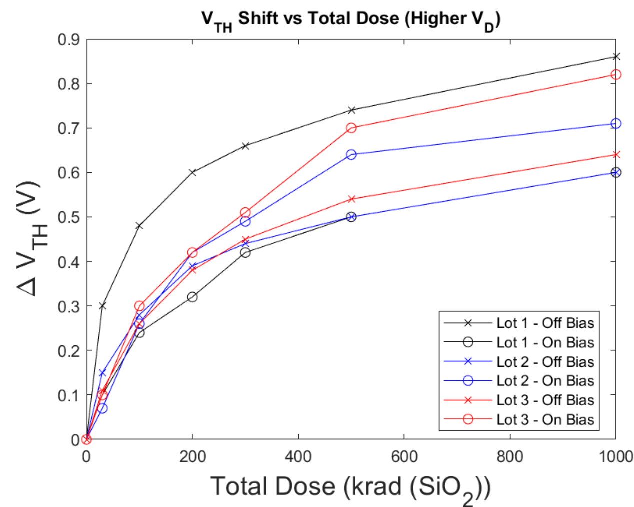


Figure 4.9 - Comparison of total change in threshold voltage for each TID level for all lots and bias configurations. This plot is comparing all the I_{DS} vs V_{GS} curves taken at the higher V_D. Which was 1.8 V for Lot 1 and Lot 2, and 800 mV for Lot 3.

The three lots also showed similar increase in the current at 0 V V_G, as shown in Figure 4.10. The Lot 1 and Lot 3 transistors had approximately a 1 order of magnitude increase in current and the Lot 2 CNTFETs had a three order of magnitude increase in the current.

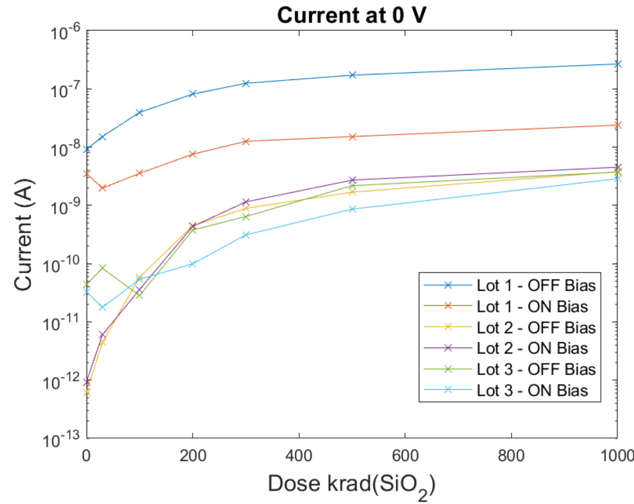


Figure 4.10 – Current at 0 V Gate Bias vs Dose for all three lots. All values are from the low V_D I_{DS}-V_{GS} curves.

These results concur with previous research on the effects of TID on electronic devices including CNTFETs [34][35][36]. In addition, the results agree with the findings from the pre-radiation electrical characterization tests that show the presence of a high number of oxide defects. Previous research indicates the source of hysteresis in CNTFETs is the defects in the oxides [45][66]. Although the channel material used in CNTFETs is relative to CMOS, the CNTFET device still has a gate dielectric and oxides surrounding the entire transistor, and TID response depends on the oxides used in the devices. The structure of the CNTFETs in this research is similar to a full-depleted silicon-on-insulator (FDSOI) MOS transistor. Figure 4.11 shows a cross section illustration of a FDSOI transistor. The channel is lightly doped silicon, which is analogous to the undoped carbon nanotube semiconductors in the channel of the CNTFET. The drain, source, and channel all sit on top of the buried oxide (BOX) which is structurally similar to the CNTFETs' layout. Instead of sitting on a BOX, the CNTFETs have oxides above the undoped CNT channel

and a spacer oxide below the bottom gate. FDSOI devices have shown increased sensitivity to TID effects due to charge trapping in the BOX [62]. This charge causes threshold voltage shift, in contrast to modern FinFETs where the primary TID effect is an increase in leakage current [64]. This is similar to the CNTFET results showing a large V_{TH} shift with dose, indicating the oxide above the CNTs is trapping charge.

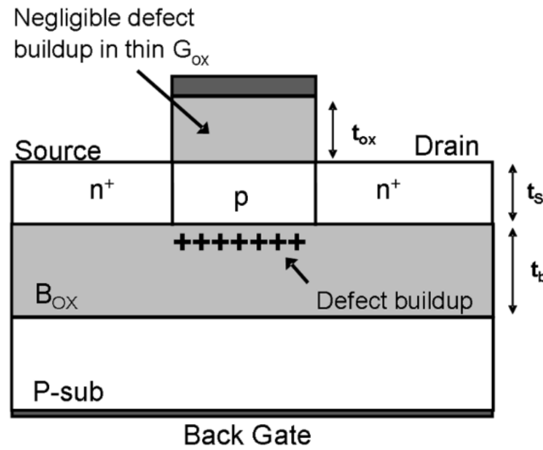


Figure 4.11 – Cross section illustration of a FDSOI transistor. The image depicts a lightly doped p-channel between the source and drain and on top of the buried oxide (BOX). Also depicted are more defects to trap charge in the larger BOX than in the gate oxide [62].

In comparison, Figures 4.11, 4.12, and 4.13 show I_{DS} vs V_{GS} curves for FDSOI transistors before and after TID. An older 45nm FDSOI transistor, shown in Figure 4.11, had less than a 0.2 V V_{TH} shift after 1 Mrad (SiO_2) of TID exposure [60]. Figure 4.12 shows results from a 22nm FDSOI Charge Trap Transistor, where the total V_{TH} shift at 500 krad (SiO_2) was 0.12 V [63]. Another 22nm FDSOI transistor showed a similar shift of 0.139 V in Figure 4.13 [61]. These three FDSOI transistors exhibited less than 0.2 V shift at 500 krad (SiO_2) compared to a shift 0.37 V to 0.6 V for the CNTFETs at the same dose. This shift is at least two to three times less than the shifts exhibited by all three CNTFET lots.

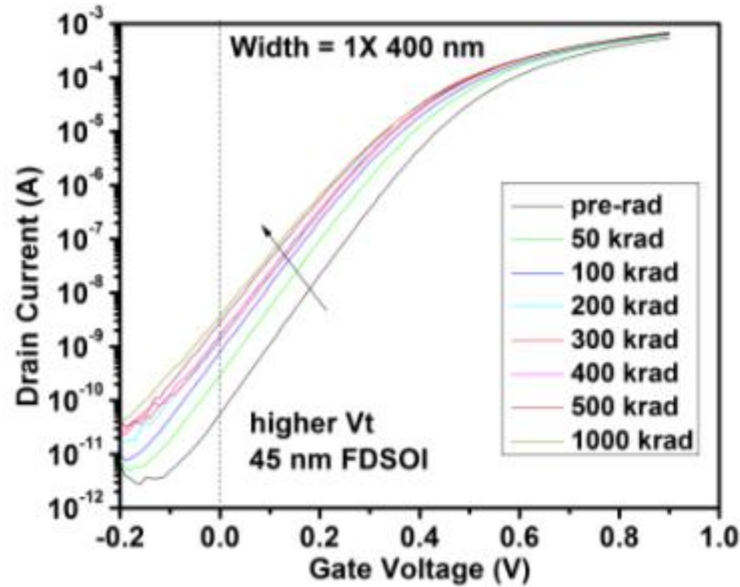


Figure 4.12 – TID testing results on 45nm FDSOI transistor. The total V_{TH} shift after 1 Mrad (SiO_2) was less than 0.2 V [60].

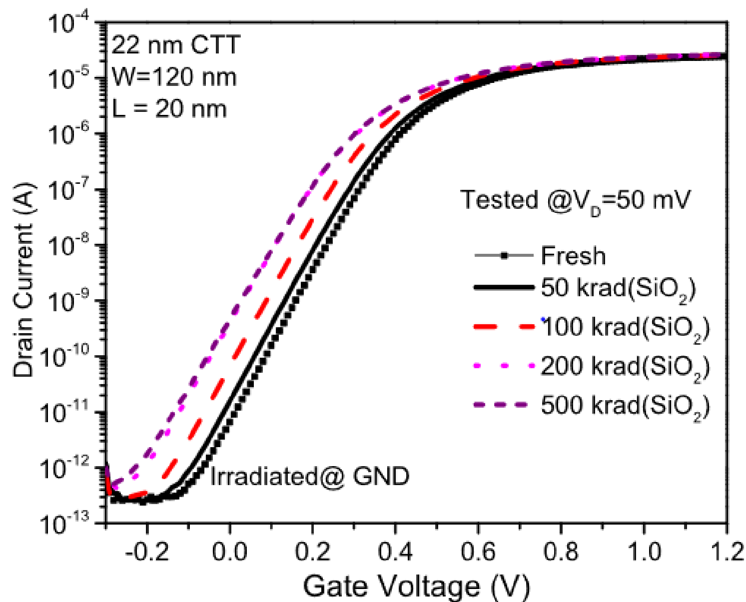


Figure 4.13 – I-V curve results of a 22nm FDSOI charge-trap transistor irradiated to 500 krad (SiO_2). The total V_{TH} shift was 120 mV [63].

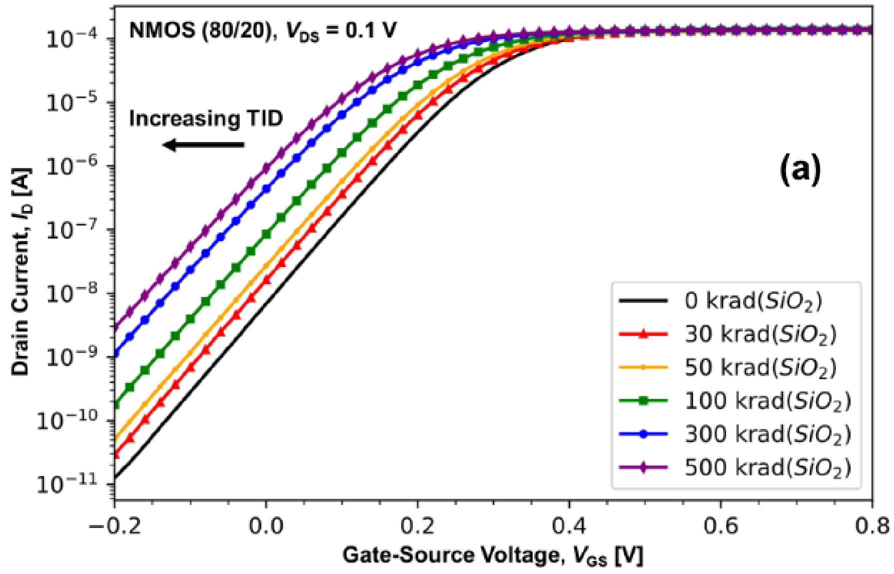


Figure 4.14 – TID test results from irradiating a 22nm FDSOI transistor to 500 krad (SiO_2). The total V_{TH} shift was 139 mV [61].

The CNTFETs' greater shift in V_{TH} when compared to FDSOI is caused by the increased number of defects in the oxides that surround the transistors. Like previous changes in oxides [42], these CNTFETs are fabricated with a new process and rely on newer, immature oxides to surround the transistors. The specific SiO_X and HfO_X used for Lot 1 and Lot 2 electrostatic tuning or the AlO_X used in surrounding Lot3 transistors likely have a higher number of defects compared to modern CMOS.

CHAPTER 5

Low-Frequency Noise Characterization

5.1 Low-Frequency Noise Experiment Setup

1/f noise experiments were performed on Lot 2 transistors both before and after TID irradiation. The setup used for these experiments is depicted in the block diagram pictured in Figure 5.1. As before, the V_{TH} was defined as a voltage at a fixed current. The low-frequency noise-power spectral density, S_{VD}, was measured using the setup in Figure 3.4, at 295 K at a range of frequencies from f = 1 Hz to 2000 Hz with correction for background noise [48][49]. During the low-frequency noise measurements, the drain was biased at 0.1 V with source and substrate terminals grounded; noise measurements were taken at gate voltages V_G from 0.1 V to 0.8 V above the calculated $V_{TH.}$

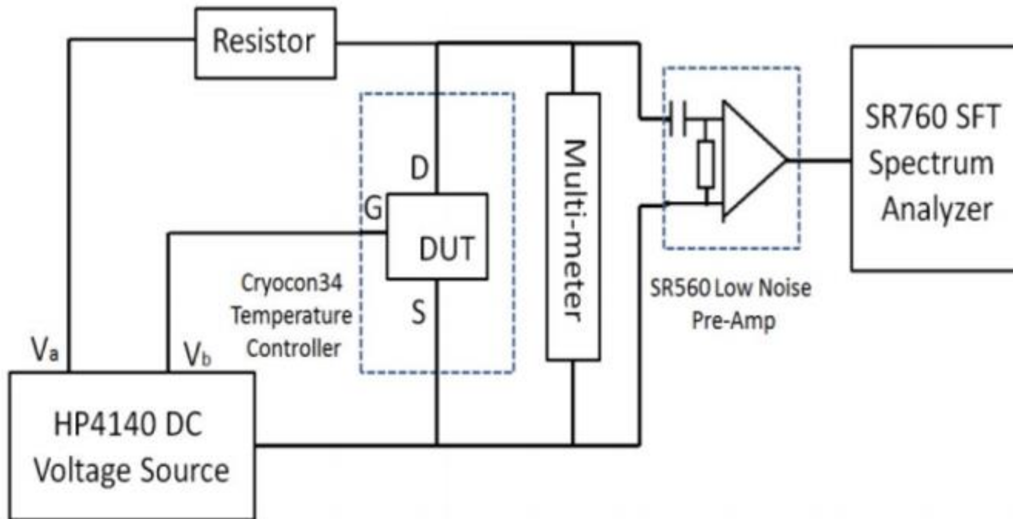


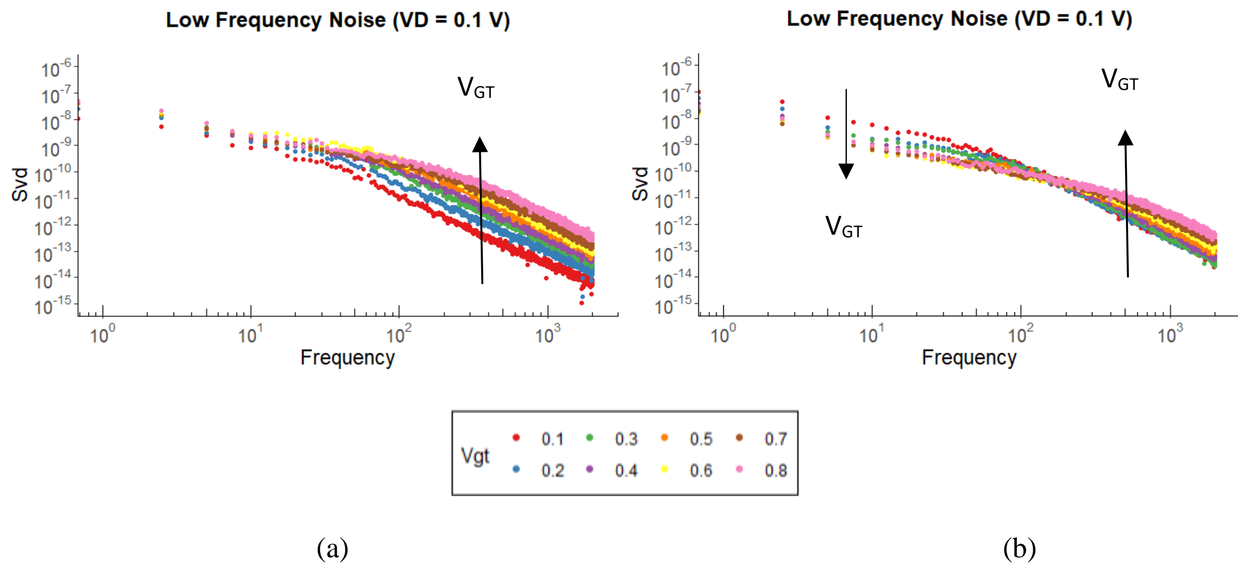
Figure 5.1 – Low-frequency noise testing setup [50].

5.2 Impact of Total-Ionizing Dose on $1/f$ Noise

Figure 5.2(a) and 5.3(a) show the power spectral density (S_{VD}) for the Lot 2 CNTFETs before irradiation. The slope of the frequency dependence of the noise, α, is calculated using equation (1):

$$\alpha = \frac{\partial \ln(S_{VD})}{\ln(f)} \quad (1)$$

A plot of α vs V_{GT} is located in Figure 5.4, which shows that the α at frequencies below 50 Hz is ~2, which is consistent with random telegraph noise [37] caused by prominent individual defects. At higher frequencies α increases above 2 and the noised magnitude has a greater dependence on V_{GT}. This suggest that percolation-path switching in the CNT mesh comprising the channel is a source of the noise magnitude[27]. Figure 5.2(b) and 5.3(b) show that after irradiation the lower frequency noise decreases with increasing gate voltage, which is consistent with an increased role of border traps in the noise.



(a) (b)

Figure 5.2 - LFN testing results from (a) pre-irradiation and (b) post-irradiation to 1 Mrad (SiO_2) in the ON-bias configuration. These plots show the power spectral dependency (S_{VD}) on frequency.

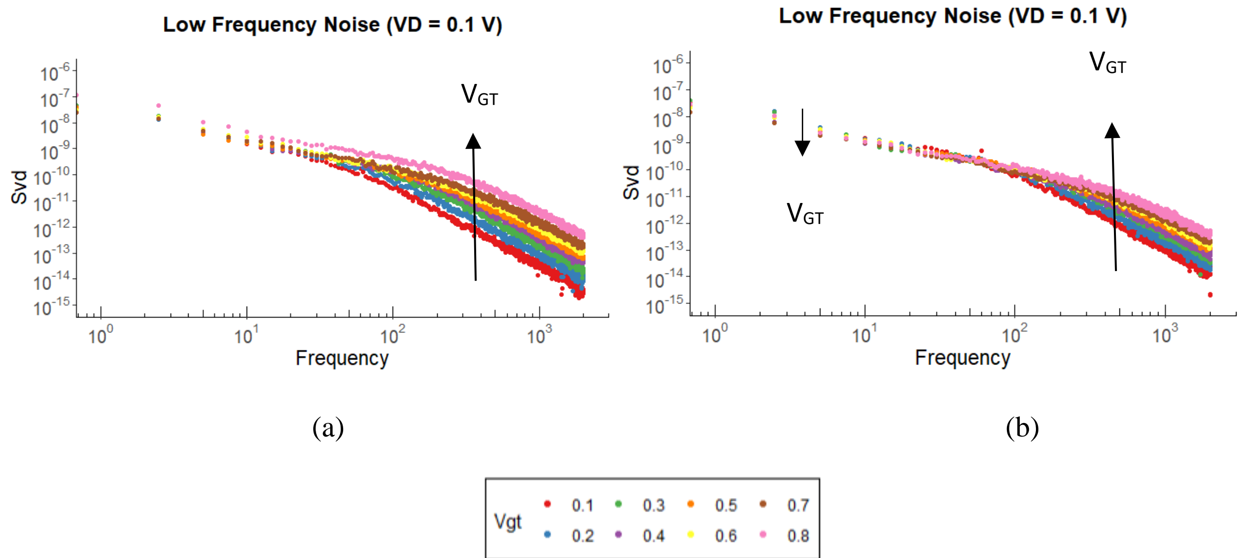


Figure 5.3 – LFN testing results from (a) pre-irradiation and (b) post-irradiation to 1 Mrad (SiO_2) in the OFF-bias configuration. These plots show the power spectral dependency (S_{VD}) on frequency.

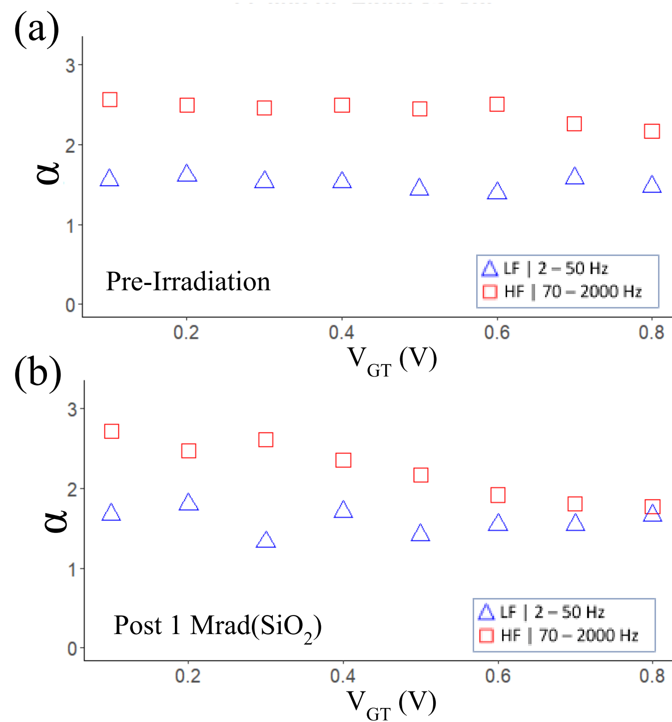


Figure 5.4 – α versus V_{GT} (a) before irradiation and (b) after 1 Mrad (SiO_2) of TID.

The noise magnitude in these CNTFETs is significantly higher than contemporary MOS transistors. While percolation path switching is a significant source of the noise, higher defect densities in the oxides also contribute to the noise magnitude. Figure 5.5 depicts LFN results from both a 30nm bulk FinFET and a 30nm SOI FinFET [59]. The CNTFET S_{VD} at 10 Hz in Figs 5.2 and 5.3 is 2-3 orders of magnitude larger than the two types of 30nm FinFETs. Previous studies have shown that the noise of SOI transistors can be higher than bulk transistors due to higher defect densities from the BOX and sidewall oxides [58]. While the structure of the CNTFETs is analogous to FDSOI, CNTFETs exhibit orders of magnitude more noise than some SOI transistors [59], which indicates that CNTFETs have much higher defect densities in the oxides. Previous research has shown that the measured room temperature 1/f noise correlates to the post-irradiation threshold voltage shift in MOS devices [56], which is consistent with what is seen in the CNTFETs.

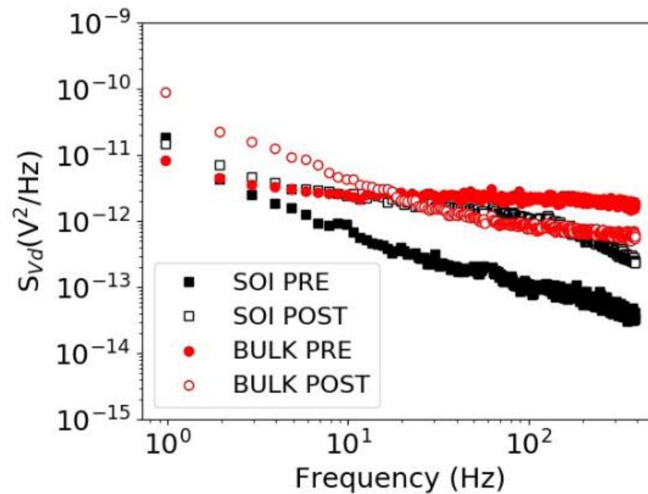


Figure 5.5 – LFN testing results showing S_{VD} vs Frequency for 30nm bulk and SOI FinFETs [59].

CHAPTER 6

Conclusion

CNTFETs exhibit significant response to TID effects. The testing described in this paper—the control stress test I-V curve shift, hysteresis, TID induced threshold voltage shift, and 1/f noise before and after irradiation—all indicate that a larger number of defects in the oxides, when compared with mature CMOS, is the cause of the degradation. All three lots showed a similar 0.6 V to 0.8 V threshold voltage shift and had orders of magnitude higher current, at 0 V, after irradiation. This voltage shift after irradiation up to 1 Mrad (SiO_2) would cause the transistor to always be turned ON, resulting in incorrect circuit functionality. The increase in the off-state current raises the static power consumption, which could effectively negate CNTFETs' promised energy efficiency advantages.

Although the CNTFETs' transistor structure is similar to that of silicon FDSOI transistors, the CNTFETs had at least three times increase in threshold voltage shift. The larger voltage shift is caused by more charge trapped in the oxide around the CNTFET. This is corroborated by the low-frequency noise testing, which demonstrates the CNTFETs have 3 orders of magnitude more noise than modern MOS SOI transistors. This higher noise level suggests that CNTFETs have more defects in the oxides surrounding the transistor [58], which would trap charge and in turn cause the large voltage shifts seen in this research.

CNTFETs are a new and emerging technology, and the fabrication process is rapidly changing. Therefore, continued testing of their TID susceptibility will be essential to developing an understanding as to how these devices will respond in radiation environments.

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