TOTAL-IONIZING-DOSE EFFECTS ON CHARGE-TRAPPING NAND MEMORY DEVICES

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1. INTRODUCTION

1.1. NAND Flash memory

THE NAND Flash technology has become a leading technology in the nonvolatile (NV) memory market that has proven to largely overcoming hard-disk drive technology [1]. This is due to the capability of the NAND Flash solution to address quite a variety of applications better than any other storage technology, thanks its successful tradeoffs between reliability, performance, and cost [2]-[4]. The rapid evolution of the technology makes it possible to steadily increase the integration density of the NAND array. This is proved in Fig. 1.1 in terms of gross

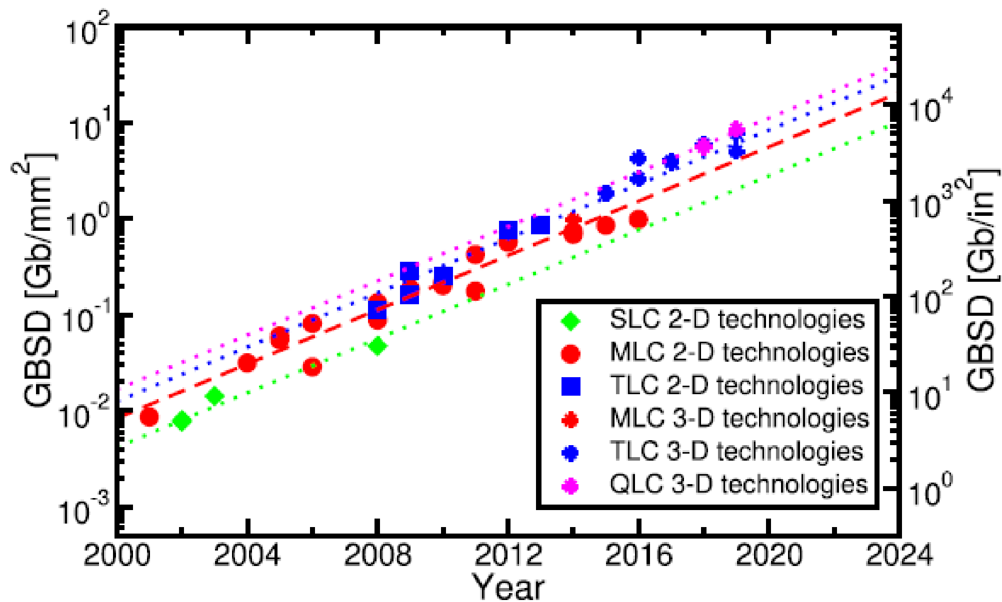


Fig. 1.1. GBSD of the single-level cell (SLC), multi-level cell (MLC), and triple-level cell (TLC) 2D and MLC, TLC, and QLC 3D NAND Flash chips presented at the IEEE ISSCC since 2001 [after3].

bit storage density (GBSD), for example, the ratio between the storage capacity and the total chip area of the NAND Flash chips [4]-[6].

With technology development, the improvements of the 2D NAND Flash technology over the years is achieved by increasing in process and system complexity [7]. Vertical-channel 3D NAND arrays came as a relief to that challenge of the NAND Flash technology. They allowed to use conventional single-patterning ArF immersion lithography, reducing the need for double-patterning techniques [8]. Meanwhile, owing to their much larger cell size, 3D NAND show

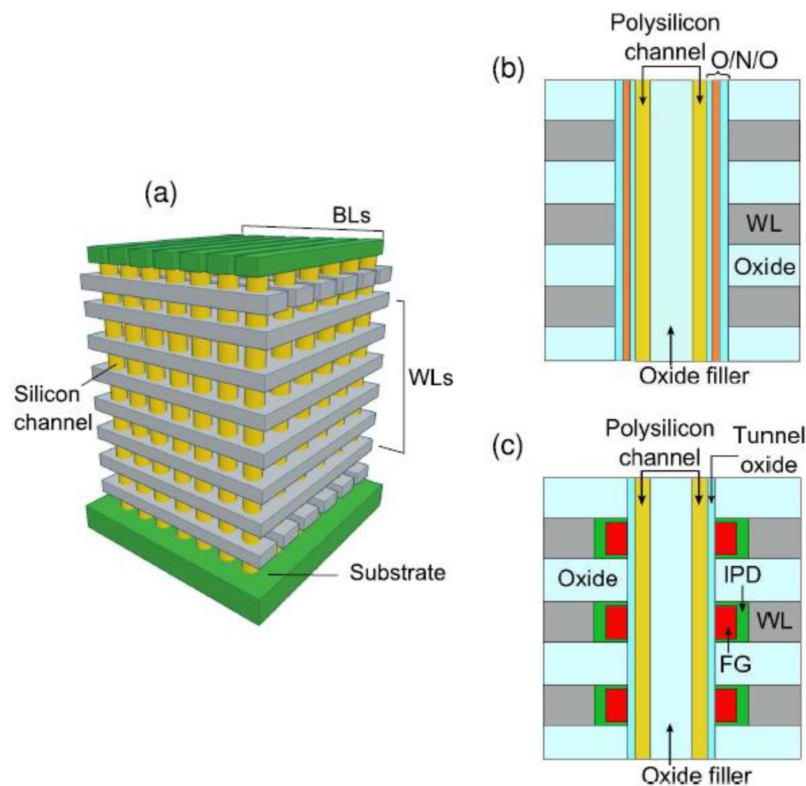


Fig. 1.2. (a) Schematic picture of a vertical-channel 3D NAND Flash memory array. Vertical cross section of a 3D NAND Flash memory array based on (b) charge-trap storage and (c) floating-gate storage. IPD is inter-poly dielectric and O/N/O stands for oxide/nitride/oxide [after4].

reduced impact on device reliability and performance of the main physical issues that constrained the performance of 2D technologies [9], [10]. Fig. 1.2 (a) shows the schematic structure of a vertical-channel 3D NAND Flash array. Different vertical-channel 3D NAND Flash array technologies have been developed nowadays. The main difference among them is the material adopted to store charge in the memory cells, which can be either conventional polysilicon [10] or a dielectric layer with a high density of trap centers, typically silicon nitride [11], [12]. Fig. 1.2 (b) and (c) shows the schematic cross section of the NAND string in the two cases, offering benefits and drawbacks in terms of program/erase performance, reliability, and integration complexity [3].

1.2. Main operations of NAND Flash memory

Fig. 1.3 schematically depicted a planar NAND Flash array consists of floating-gate transistors. Floating-gate transistors can store information in terms of charge in their floating gate, such transistors are connected in series along strings and are driven by shared wordlines (WLs). Additional service elements other than the memory cells are required in order to store and access data safely for memory technologies. For NAND Flash technology, the number of the service elements is relatively low, which is another key advantage of this storage solution [4]. For example, all of the memory cells in a NAND string are addressed by a single drain select transistor driven by a drain select line (DSL) and a single source select transistor driven by a and a source select line (SSL), as shown in Fig. 1.3. And then the source select transistors are

connected to a source line and the drain select transistors are connected to the bitlines (BLs). The upper and lower cells in the strings are dummy cells [13], driven by dummy lines (DULs).

Storing data in a NAND Flash array is achieved by changing the floating-gate charge of the memory cells to set their threshold voltage (V_{th}) to a certain level. And the information stored in the memory cell is determined by the level of its V_{th}. Program, erase and read operations are required for NAND Flash array to store and access data in their memory cells. The schematic description of the voltages applied to the NAND string for those operations is shown in Fig. 1.4.

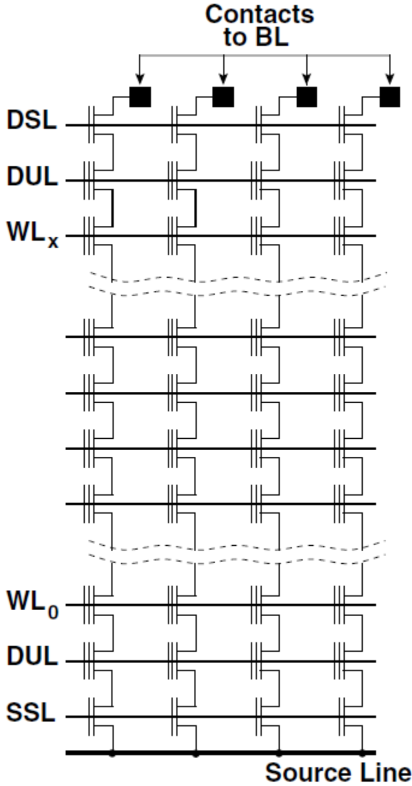


Fig. 1.3. Schematic description of a NAND Flash array. Strings are selected by means of a drain select transistor, connecting the string to a BL and driven by a DSL, and a source select transistor, connecting the string to an implanted source line and driven by an SSL [after 4].

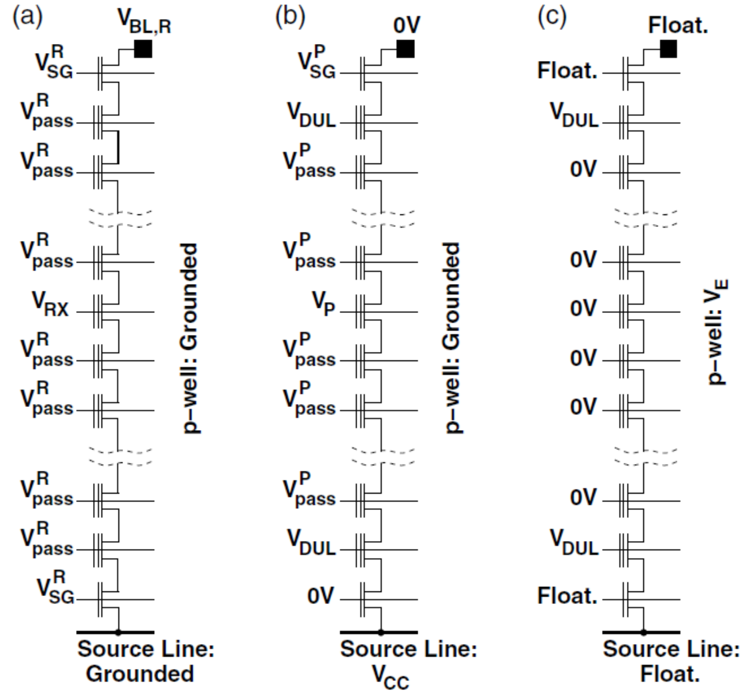


Fig. 1.4. Schematic description of the voltages applied to the NAND string to (a) read, (b) program a selected memory cell in the string and (c) erase the entire NAND block. V_{SG}^{R} and V_{SG}^{P} are the voltages applied to the gates of the biased select transistors during read and program, respectively [after 4].

For the read operation, a read voltage V_{RX} is applied to a selected cell's control gate and all of the other cells and the two selectors in the same string are acting as pass transistors, to sense the current flowing through the selected cell [14], [15]. The voltages applied to the NAND array are depicted in Fig. 1.4(a): the voltage of the WL of the selected cell is raised to V_{RX} and that of unselected cells is raised to V_{pass}^{R}. The string is connected to the BL (biased at $V_{BL,R} > 0$ V) and the grounded source line by positively biased DSL and SSL. V_{pass}^{R} must be set higher than the maximum V_{th} level so that all of the unselected cells in the string are highly conductive irrespective of their memory state. These operating conditions lead to a current flow through the

string that is mainly limited by the selected cell. A sense amplifier allows then to assess if the cell V_{th} level is lower or higher than V_{RX} from the integration of this current [16], and from that, the information stored in the cell can be read.

For the program operation, uniform Fowler-Nordheim (FN) tunneling of electrons from channel to floating gate through the tunnel oxide has become the elective physical mechanism to program the memory cells in a NAND Flash array [17], [18]. Fig. 1.4(b) shows the voltages applied to the NAND array for program operation. A program voltage V_P is applied to the WL of the selected cell, with all of the other WLs biased at a pass voltage V_{pass}^{P}). The SSL is grounded so that all the source select transistors are kept off. A positive voltage V_{SG}^{P} is applied to the gate of drain select transistor, so that the string is connected the grounded BL. In order to reduce the electric field in the dielectric material isolating the DSL/SSL and the DUL, the DUL lines are biased at a voltage V_{DUL} lower than V_{pass}^{P} [19], [20]. By applying such voltage to the NAND string, a high electric field is created in the tunnel oxide of the selected cell by V_P, electrons can therefore uniformly tunnel from the channel of the memory cell to its floating gate, change their V_{th} to a programmed level. To achieve a fine placement of the V_{th} levels among the memory cells, an incremental step-pulse programming (ISPP) technique is used on the program voltage V_P [21], in which fast pulses of increasing amplitude are used to inject a constant, controlled amount of charge onto the floating gate at each step, follow with program verify operation in which V_{th} is monitored.

For the erase operation, the voltages applied to the NAND array is depicted in Fig. 1.4(c): a

high positive voltage V_E is applied to the p-well of the array with all of the WLs grounded, leading to a uniform Fowler-Nordheim tunneling of electrons from the floating gate to the channel of the memory cells [17], [18]. All the BLs, the source line, the DSL, and the SSL are left floating to reduce the electrical stress on the other parts of the block. A positive voltage V_{DUL} is applied to the DUL, similar to the program operation, to reduce the electric field in the insulators between these lines and the DSL/SSL [20]. After the erase pulse, a verify operation will check whether the V_{th} of all the cells in the block is below 0 V. An additional erase pulse will be applied with higher V_E if this condition is not met.

1.3. Radiation effects and reliability issues of NAND device

The microelectronic components in space are exposed to various types of radiation such as protons and electrons, which interact with the semiconductor material to cause ionizing damage, atomic displacement, and/or single event effects. Total-dose irradiation is a significant concern for the long-term reliability of MOS devices. It is extremely important to understand radiation effects on semiconductor devices for the application of advanced technologies and materials in space environments. This section will first discuss the basic effects of radiation-induced charge buildup in MOS devices, including oxide, interface, and border traps.

Fig. 1.5 shows a schematic energy diagram of a MOS structure under positive bias applied to the gate and indicates four major physical processes that contribute to the radiation response of a MOS device. For MOS devices, the most total-dose radiation-sensitive parts are the oxide

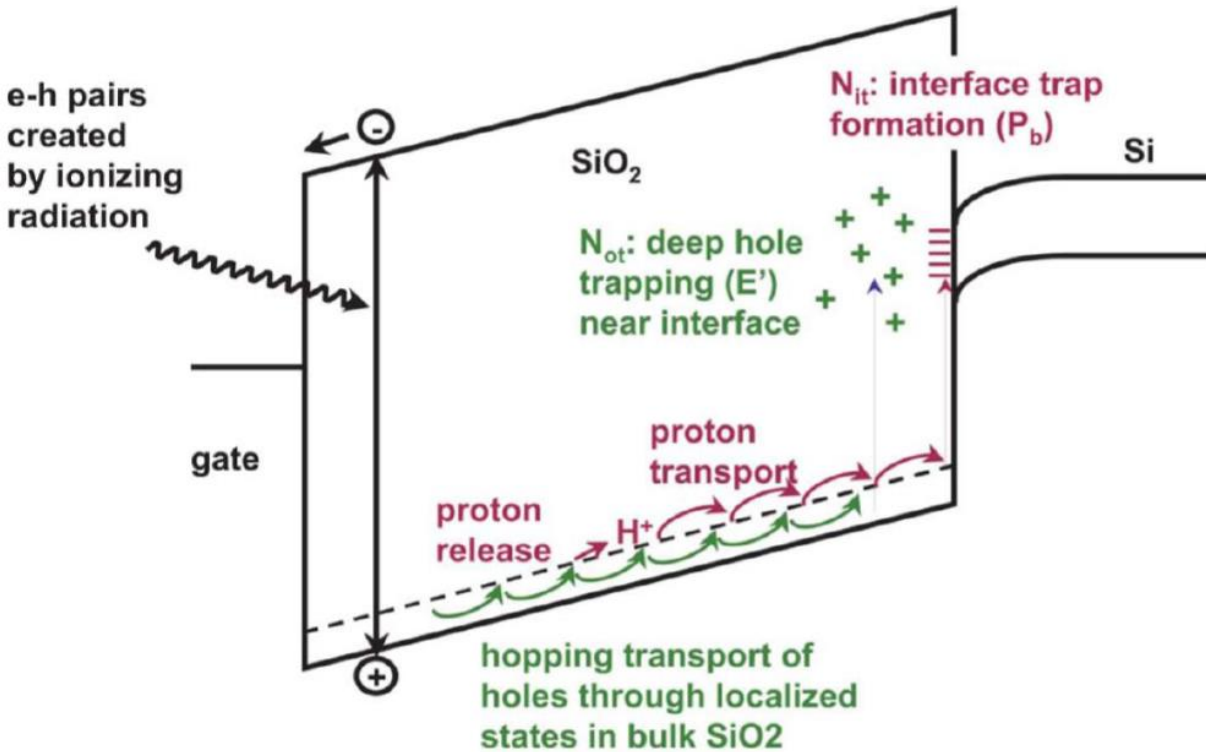


Fig. 1.5. Schematic energy band diagram for MOS structure under positive bias, indicating major physical processes underlying radiation response. [after 22].

insulators. Electron-hole pairs are created in the oxide by the deposited energy when a MOS device is exposed to high-energy ionizing radiation. Because the electrons are much more mobile (20 cm^2/V sec at 300 K in fused quartz [23]) than the holes (~4×10^{-9} cm^2/V sec at 300 K) in SiO_2, most of the electrons are swept out of the oxide rapidly, and the remaining holes are trapped in micro-structural defects and pre-existing traps. However, some of the electrons will recombine with holes before they leave the oxide. The fraction of electron-hole pairs that escape recombination is called the charge yield. The fraction depends significantly on the energy of the incident particle and the strength of the electric field in the oxide. The generation and

recombination of electron-hole pairs are the first processes shown in Fig 1.5. Those holes that escape initial recombination will further transport toward the Si/SiO_2 interface by hopping via localized states in the oxide [24]. This process typically takes less than a second, but may take place over many decades in time. Because hole transport in SiO_2 is highly dispersive [25], as a result, the "tail" of the transport extends over several decades in time.

When the holes approach the Si/SiO_2 interface, some of the holes will be neutralized by electrons thermal emission from the trapping sites or tunneling from silicon, while others get trapped at relatively deep trapping states, forming positive oxide trap charges. These oxide trapped charges can lead to threshold voltage shift as well as an increase of radiation-induced leakage current (RILC) in these devices [26]-[28]. RILC is often attributed to an inelastic tunneling process assisted by neutral traps in the oxide. The neutral electron trap likely originates as radiation-induced holes trapped at E' centers in the oxide. The Electron Spin Resonance (ESR) measurements performed by P. M. Lenahan et al. have shown a link between E' centers and RILC [29].

Meanwhile, as holes transport toward the interface through the oxide, hydrogen ions (protons) can be released in the oxide bulk. Under positive gate bias, those protons can drift to the Si/SiO_2 interface, where they may react with Si-H to form H_2, leaving silicon dangling bonds at the interface. These dangling bonds can act as interface traps, which are localized states in the Si band-gap. Their occupancy is determined by the Fermi level, leading to a change of threshold voltage and a decrease of carrier mobility [31].

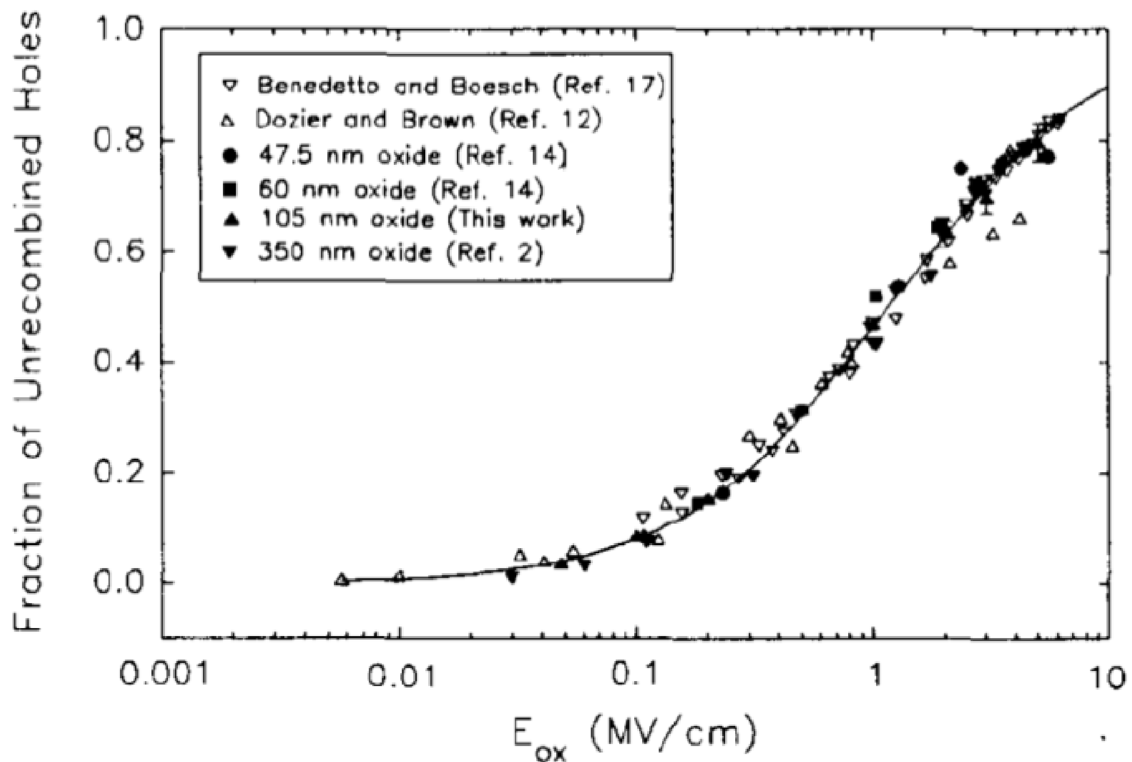


Fig. 1.6. Fraction of holes which escape recombination for 10-keV x-ray irradiations as a function of oxide field. The solid line is a fit to data. [after 30].

As previously mentioned, some fraction of the radiation-induced holes will recombine with the electrons before the electrons are swept out of silicon dioxide. The fraction of holes escaping initial recombination depends significantly on the magnitude of the electric field through the oxide. When an electric field is applied across the oxide of a MOS device, the radiation-induced electron-hole pairs will immediately be separated and begin to transport in opposite directions. As the electric field strength increases to separate pairs more efficiently, the probability that a hole will recombine with an electron decreases, and the charge yield increases. Fig. 1.6 plots the fraction of holes that escape recombination for 10-keV x-ray irradiation as a function of the

electric field. When the electric field is higher than 4 MV/cm, more than 80% of radiation-induced holes escape initial recombination.

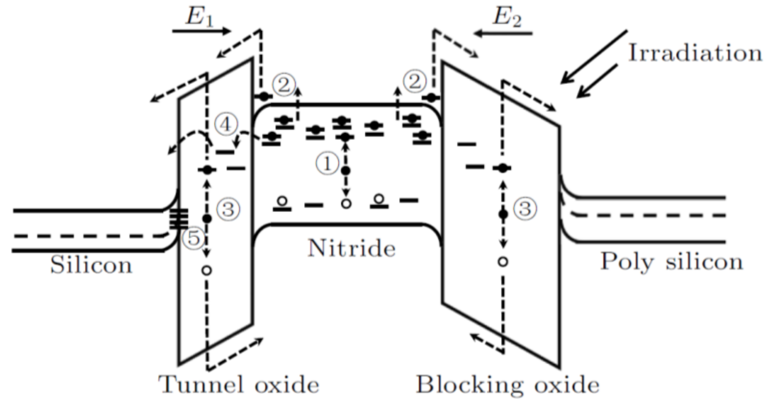


Fig. 1.7. Physical mechanisms involved in the programmed SONOS device under TID irradiation: (1) electron-hole pairs are generated in the nitride layer; (2) electrons emission over the nitride/oxide barriers; (3) electron-hole pairs are generated in the tunnel oxide and blocking oxide; (4) traps existing in the tunnel oxide assist electrons conducting from the nitride layer to silicon; and (5) the interface states are generated at the silicon/tunnel oxide interface (channel region) [after 36].

NAND Flash technology has become the leader in the NV memory market [1], [3]. NAND Flash memory devices are based primarily on 3D architecture because they overcome the density limits inherent to planar NAND devices and have become effective solutions for high density storage [32],[33]. Conventional floating-gate (FG) structures face fundamental scaling limits [33]. Thus, silicon-oxide-nitride-oxide-silicon (SONOS) structures have become appealing alternatives for NV memory applications due to their process simplicity, economy of power, film scalability, and radiation tolerance [34],[35]. Total ionizing dose (TID) effects are an important consideration in the use of NV memories in space and other high-radiation

environments [36]-[38]. SONOS NOR-based NV memory devices are more radiation-tolerant than FG memories [39]-[45]. Fig. 1.7 shows the physical mechanisms involved in the programmed SONOS device under TID irradiation [36].

Electron-hole pairs are generated in the nitride layer during TID radiation, which will recombine partially afterwards. And then the remaining electrons will be swept out of the nitride layer by the build-in electric field induced by trapped electrons, remaining holes in the nitride will either recombine with the trapped electrons or captured by the trapping sits, owing to the higher trapping probability for holes than electrons in nitride [39],[44]. Trapped electrons can also emit from traps in the nitride and transport out of the dielectric layer during irradiation by absorbing energy from radiation [39]. The radiation introduced electron-hole pairs in the tunnel/blocking oxide recombine partially afterwards. And then the remaining electrons will be swept away toward the channel and the poly-silicon gate by the build-in electric field, remaining holes are attracted to the SiN layer and eventually trapped in the near-SiN regions of the blocking and tunnel oxides [39], [46]-[49]. Traps existing in the tunnel oxide assist electrons conducting from the nitride layer to silicon [36]. The interface states can also be generated at the silicon/tunnel oxide interface by high electric field or radiation, which can result in an increase in the subthreshold slope (SS). These reasons explain that radiation can significantly impact the performance and the storge information of the memory cells, which can eventually lead to failure.

Reliability of a NV memory represents its capability to store data and allow for their correct retrieval after a relatively long stretch of time. 3D memory relieves the need of scaling the cell

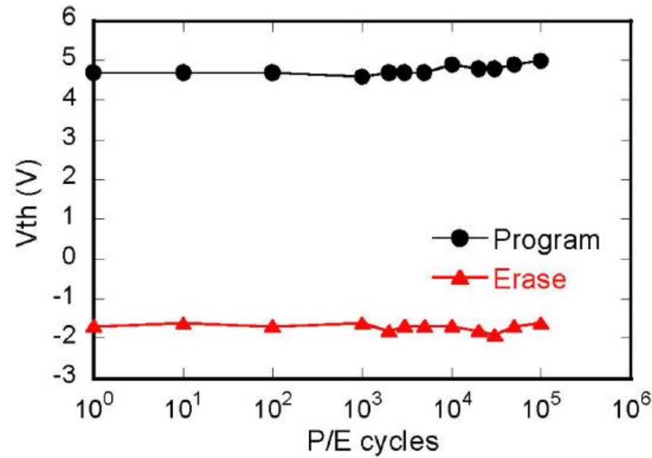


Fig. 1.8. Endurance performance for a 3D NAND [54].

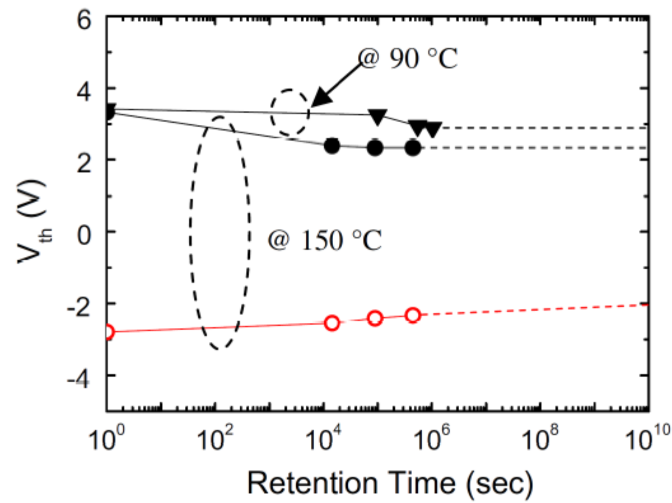


Fig. 1.9. Retention performance for floating-gate based 3D NAND and different temperatures [63].

retention still present in 3D devices [2],[3],[50].

area by placing it onto the increase in the number of stacked layers, and as a consequence, achieved a better reliability performance. However, reliability issues such as endurance and data retention still exist.

Endurance specifies the maximum number of program/erase (P/E) cycles that the memory chip can tolerate. The endurance of a memory cell can be observed by repeating P/E operations on it and monitoring the resulting V_{th} change. For planner cells it has been proved that their V_{th} levels will experience an increase for high values of P/E cycles, eventually leading to a read failure [2]. This phenomenon is one consequence of the electron flow through the oxide during FN tunneling, which will generate oxide traps and fixed charge in the devices [51]-[53]. Fig. 1.8 shows the endurance performance of a 3D NAND cell as a function of P/E cycles [54]. Because of the larger cell size compared to their planar counterpart, 3D NAND are reported to have better endurance performance [55]-[59]. based 3D NAND design. Reliability issues other than endurance and retention, such as RTN noise, charge detrapping, cell-to-cell electrostatic interference will also affect the performance of 3D NAND [8], [64]-[66].

Floating-gate based NAND devices suffer from stress introduced leakage current (SILC) after heavy P/E cycling, such effect has also been reported in 3D NAND technologies, though it is not expected to be the main cause of retention loss [59], [60]. SILC shows much less significant impact for charge-trap based memories, due to the localized nature of storage [61]. However, it has been reported that defect build-up in the tunnel oxide will enhance the trap assist tunneling effect which will eventually lead to retention loss for charge-trap based memories [62]. Fig. 1.9 shows retention performance for 3D NAND and different temperatures [63], suggest that a good intrinsic retention can be achieved for a floating-gate memory device.

Random telegraph noise in MOS transistors is an abrupt two-level fluctuation in drain

current following trapping and release of a single electron by an oxide defect. This well-known phenomenon has been observed and studied since the 1980s [2]. For a NAND Flash memory cell, the defects located in oxide layer and oxide/channel interface can trap and release single electron. When a single electron is trapped by the defect, the current of the device will decrease and therefore the V_{th} of the device will increase. On the contrast, when a single electron is released by the defect, the current of the device will increase and the V_{th} of the device will decrease. Those phenomena together will lead to V_{th} fluctuation in the memory cell, and since the storge information is dependent on the device threshold voltage, RTN could lead to Flash memory

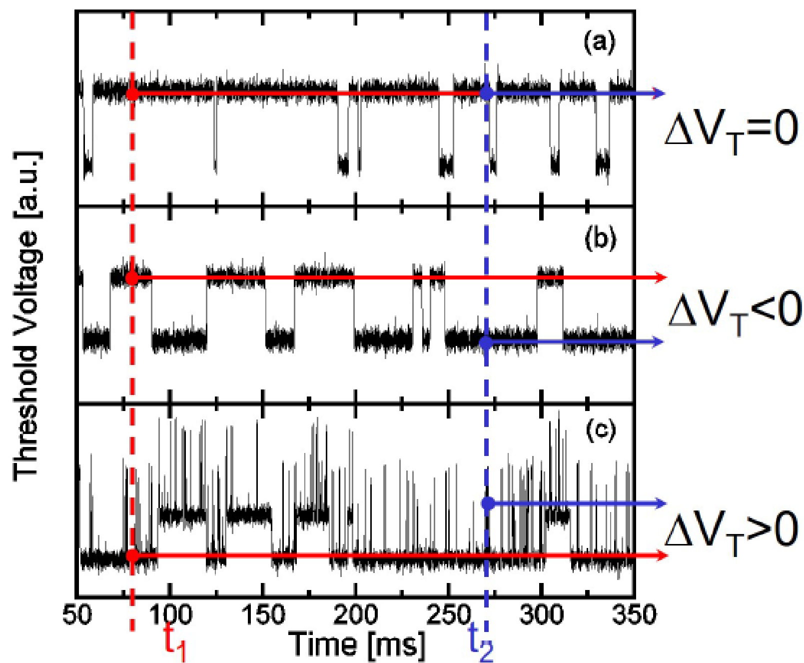


Fig. 1.10. Time dependence of V_{th} for three Flash cells affected by RTN. V_{th} is sampled at times t_1 and t_2 and the RTN amplitude is defined as the threshold voltage difference. Note that (a) null, (b) negative and (c) positive ΔV_{th} can result [After 2].

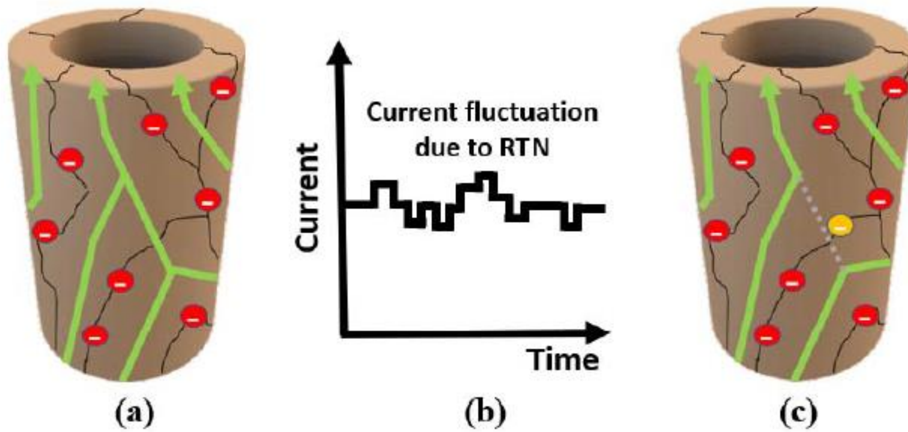


Fig. 1.11. (a) Percolative conduction in polysilicon thin cylindrical channel amidst GB potential barriers and trapped charges. (b) Current fluctuations due to RTN. (c) Large RTN impact of single electron trapping (orange) located along percolation path [After 66].

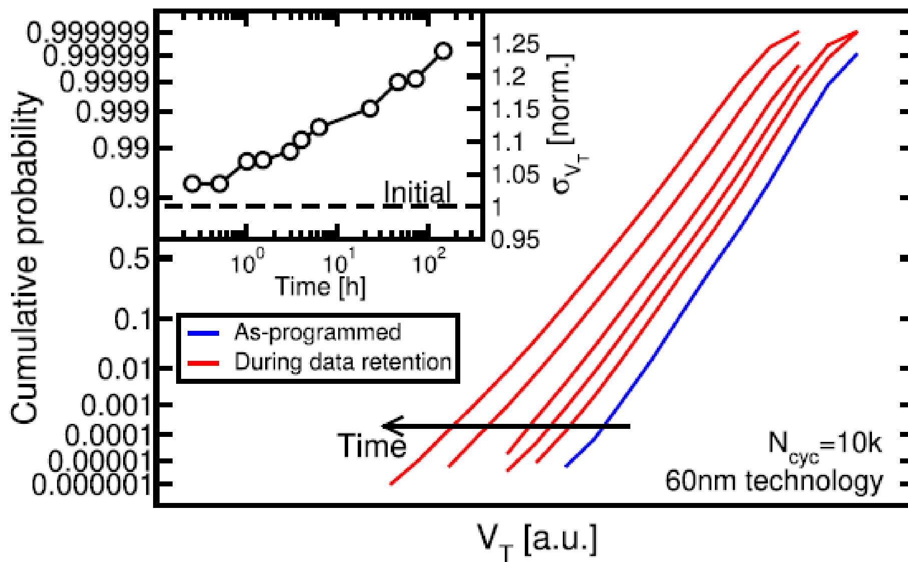


Fig. 1.12. Measured cumulative V_{th} distribution of a page of a NAND Flash array as resulting from the program operation and after increasing time during data retention at room temperature [after 3].

program failure, read error and other issues. Therefore, such noise mechanism should be paid special attention to during the NAND Flash memory investigation, especially for 3D NAND devices. A Time dependence of V_{th} for Flash cells affected by RTN is reported in Fig.1.10. As

shown RTN can cause V_{th} fluctuation in the memory cell. This measurement will return the actual RTN amplitude distribution that matters under real operating conditions, when a cell is read after being programmed.

For 3D NAND devices, the mechanism for RTN is different from planer NAND devices. Instead of defects in the tunnel oxide, the electrons trapping/de-trapping happens at defects locate at the grain boundary is leading to the RTN in 3D devices. Unlike the crystal Si channel 2D Flash memory devices, 3D NAND devices have a ploy-Si channel. When an electron is trapped in the defect located at the grain boundary, the current percolation path will be blocked. as a result, the current flow through the channel will decrease and lead to V_{th} increase. On the contrast, when electron is de-trapping from those defects located along percolation path, the current of the device will increase and the V_{th} of the device will decrease. Those phenomena together will lead to V_{th} fluctuation in the 3D NAND memory cell. The RTN in 3D NAND cell due to larger impact of single electron trapping/de-trapping located in proximity to a percolation path is shown in Fig. 1.11. This current/threshold voltage noise has a direct and significant impact on read window margin especially at lower temperature, therefore the research related to RTN in 3D NAND devices is needed and will face brand new challenges.

Charge detrapping is a transient process that owing to the healing of some charged defects located at device tunnel oxide [9, 10]. Usually, those defects are negatively charged after the programming of the memory cell. And the detrapping will lead to a V_{th} reduction over the logarithmic timescale during data retention. Measured cumulative V_{th} distribution of a NAND

Flash array as resulting from the charge detrapping after program operation is shown in Fig. 1.12 [3]. Due to the different number of defects per cell, the V_{th} distribution is affected by a relevant statistical dispersion.

1.4. Dissertation Organization

In this dissertation, radiation effects and reliability performance on vertical charge-trapping 3D NAND memory devices with different tunneling layers are explored. This dissertation is organized as follows:

Chapter 1 describes the background and motivation of this work. The development and structure of 3D NAND device are discussed. Then, the basic operations of NAND array have been explained and the mechanism of radiation effects and reliability issues of NAND devices have been discussed.

Chapter 2 describes the radiation effects of poly-crystalline Si channel vertical charge trapping NAND devices with SiON and SiO_2 tunneling layers. The V_{th} shifts during and after irradiation for pre-programmed and pre-erased devices have been investigated and the related physical mechanisms are discussed based on charge separation.

Chapter 3 covers the effects of geometry and cycling on the radiation response of charge-trapping NAND memory devices with SiON tunneling layers. Scaling to smaller dimensions

enhances programmability, endurance, and radiation tolerance. Retention performance is evaluated before and after irradiation.

Chapter 4 summarizes the major finding and research contributions of this work.

2. Total-Ionizing-Dose Effects on Vertical-Charge-Trapping NAND devices

In this chapter, total-ionizing-dose effects are evaluated in vertical-charge-trapping NAND devices with silicon oxynitride (SiON) and SiO_2 tunneling layers. Processing splits include SiON tunneling layers with and without H_2/D_2 high-pressure annealing. Programmed devices were irradiated to 500 krad(SiO_2) with 10-keV X-rays and annealed for 30 min. A second programming after annealing does not fully restore the original, programmed state. Radiation-induced trapped holes compensate deeply trapped electrons that are injected into the dielectric during device programming. Throughout the full irradiation and annealing sequence, threshold voltages remain large enough to enable successful NV memory application.

2.1. Experimental details

A schematic band diagram of a SONOS memory element is shown in Fig. 2.1 under erase

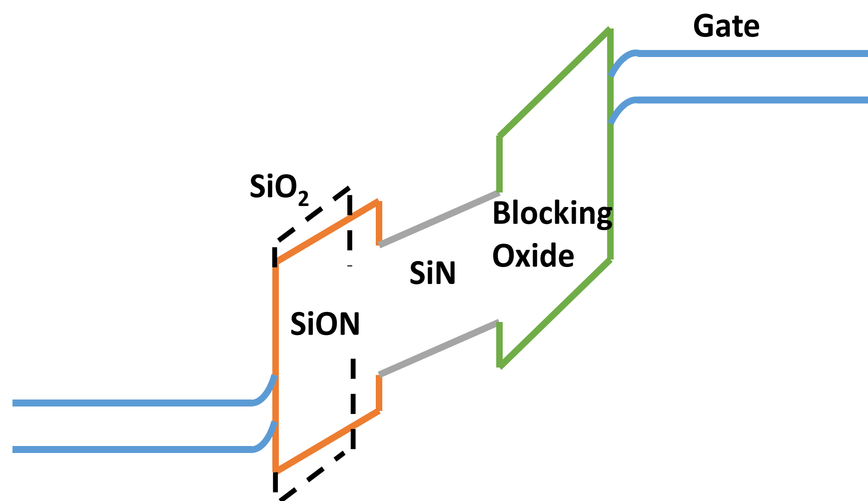
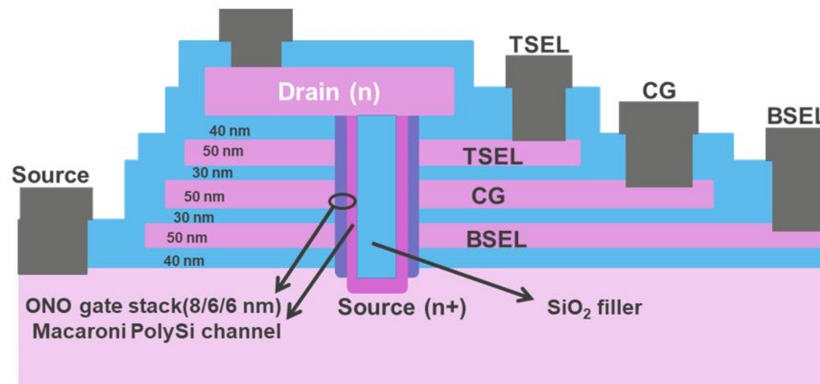
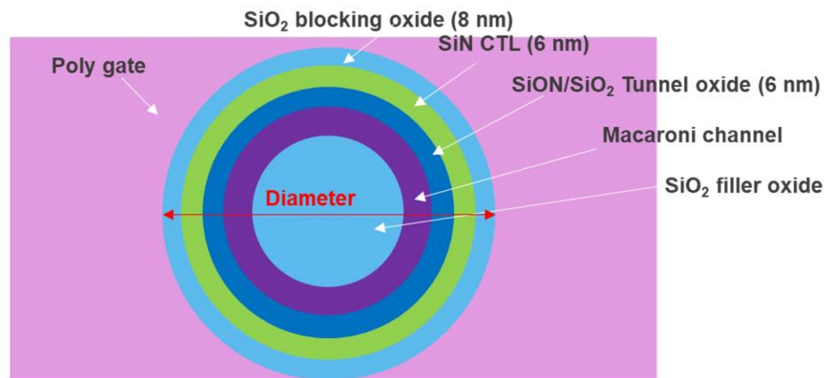


Fig. 2.1. Band diagrams under erase conditions for polycrystalline-Si channel vertical-charge-trapping NAND devices with SiON and SiO_2 tunneling layers. (After [68].)

conditions for devices with SiON and conventional SiO_2 tunneling layers. The deeper valence band of SiO_2, compared with SiON, reduces the hole tunneling current. The increased hole tunneling for SiON leads to enhanced speed and efficiency of the erasure process [67].



(a)



(b)

Fig. 2.2. (a) Lateral cross section and (b) top-view cross section of polycrystalline-Si channel vertical-charge-trapping NAND devices with SiON and/or SiO_2 tunneling layers.

Lateral and top view cross sections of 3-gate vertical charge trapping NAND devices are shown in Fig. 2.2. Circular cylindrical holes with ~70 nm diameters are etched vertically in the

substrate to serve as source junctions for the memory stack. The ONO gate stack is deposited along the outer circumference of the hollow cylinder that is formed. Then poly-crystalline Si is deposited to form the channel and the remaining inner volume of the cylinder is filled with SiO_2. This fabrication process forms three gates: the top selector (TSEL), control gate (CG), and bottom selector (BSEL), with equal channel lengths of 50 nm and 30 nm SiO_2 inter-gate spacing. The tunneling layer consists of SiON or SiO_2 [68]. The charge trapping layer is silicon nitride (SiN).

I_D-V_G characterization and program/erase testing is performed using a Keithley 4200A-SCS semiconductor parameter analyzer. Using incremental step pulse programming (ISPP), 100 μs pulses with increasing amplitude of 12-28 V are applied to the CG. During programming, the BSEL and TSEL gates are biased in pass mode at 7 V with source and drain grounded. During erasure, the CG bias is incremented from -12 V to -21 V with pulse times of 1 ms. The BSEL and TSEL gates are biased in pass mode at -10 V with source and drain grounded. I_D-V_G curves are measured by sweeping the CG from -2 V to 11 V with both TSEL and BSEL biased at 7 V and the drain biased at 0.5 V. The threshold voltage V_{th} is calculated as $V_{GS\text{-}int} - V_{DS}/2$; point of maximum first derivative [69]. Threshold-voltage shifts due to oxide- and interface-trap charge, ΔV_{ot} and ΔV_{it}, are estimated via the midgap method of Winokur et al. [70].

TID irradiation is performed at a dose rate of 30.3 krad(SiO_2)/min in an ARACOR Model 4100 ~10-keV X-ray irradiator [46]. All terminals are grounded during irradiation, corresponding

to the storage condition. Programmed and erased devices are irradiated up to 500 krad(SiO_2). After irradiation, devices were annealed with all terminals grounded for 30 min at room temperature. Devices were then erased and reprogrammed using the ISPP process. Reprogrammed devices were annealed at room temperature (RT) for at least four days to test retention. For each type of device and condition, results were obtained from at least three devices; average values and error bars denoting standard deviations are shown.

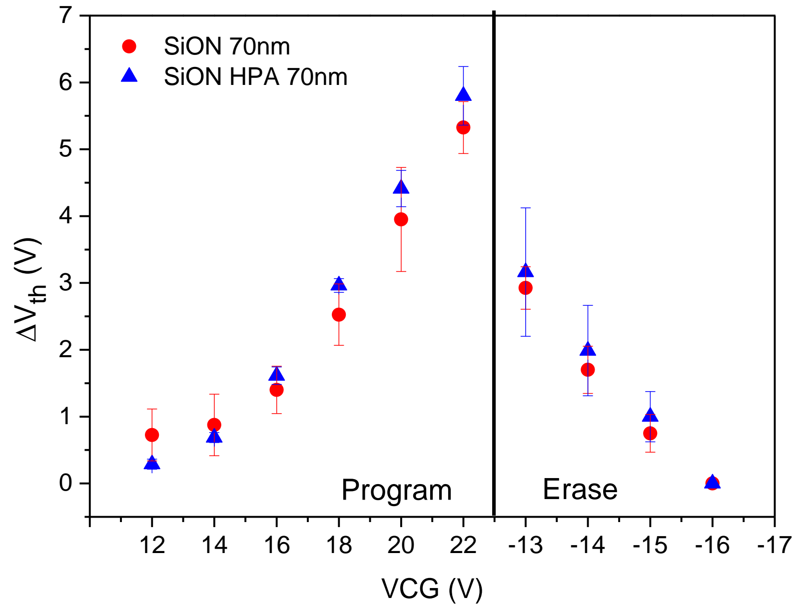
2.2. Experimental results and analysis:

2.2.1. Program/erase and retention characteristics

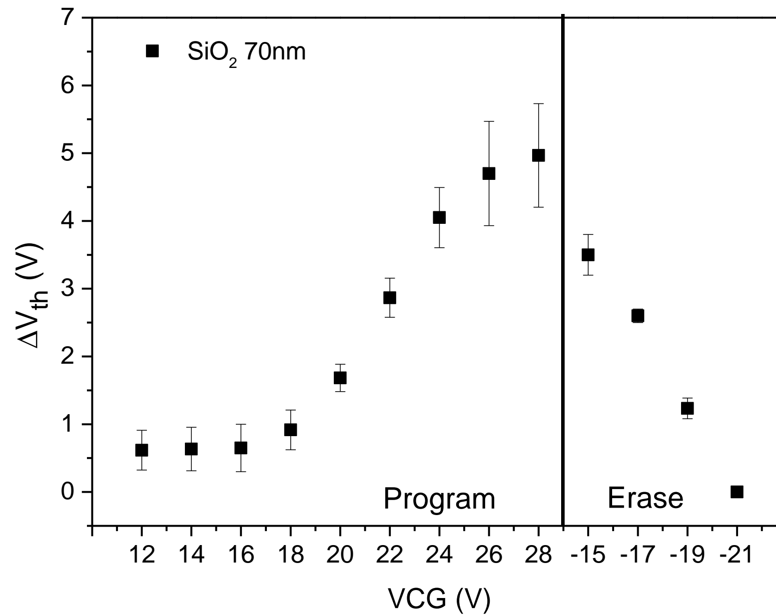
Fig. 2.3 shows V_{th} shifts for various program and erase voltages for devices with SiON tunnel layers with and without high pressure annealing in H_2/D_2 ambient (HPA) [71], and with SiO_2 tunnel layers. The V_{th} shift is defined relative to that of devices erased with the lowest CG voltage. Using ISPP, SiON devices were programmed with CG voltages from 12 V to 22 V and erased with CG voltages from -13 V to -16 V. Programming the devices produces a V_{th} shift of about +5 V. This shift is evidence of significant electron trapping in the SiN layer of the SONOS device [33], [35], [39], [46], [68]. SiO_2 devices were programmed using ISPP with CG voltages from 12 V to 28 V and erased with CG voltages from -15 V to -21 V to provide similar V_{th} shifts. These results confirm that devices with SiON tunnel oxides are programmed and erased more easily than devices with SiO_2 tunnel oxides [68].

The retention characteristics of the programmed devices were also investigated; results for

SiON devices are shown in Fig. 2.4. The I_D - V_G curves in Figs. 2.4 (a) and values of

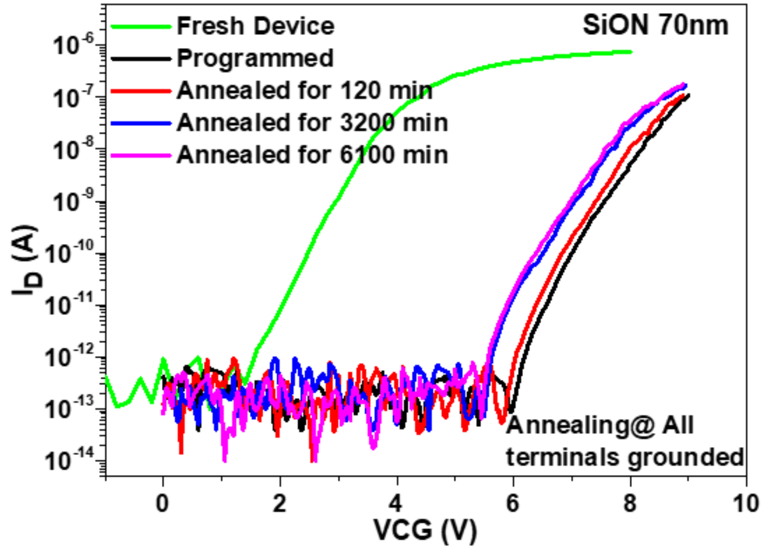


(a)

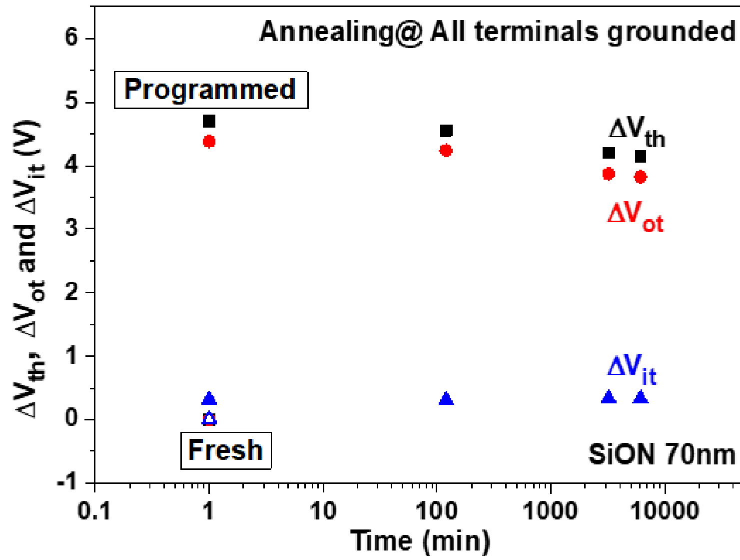


(b)

Fig. 2.3. V_{th} shifts under various program and erase voltages for 3D NAND devices with (a) SiON and (b) SiO_2 tunneling layers.

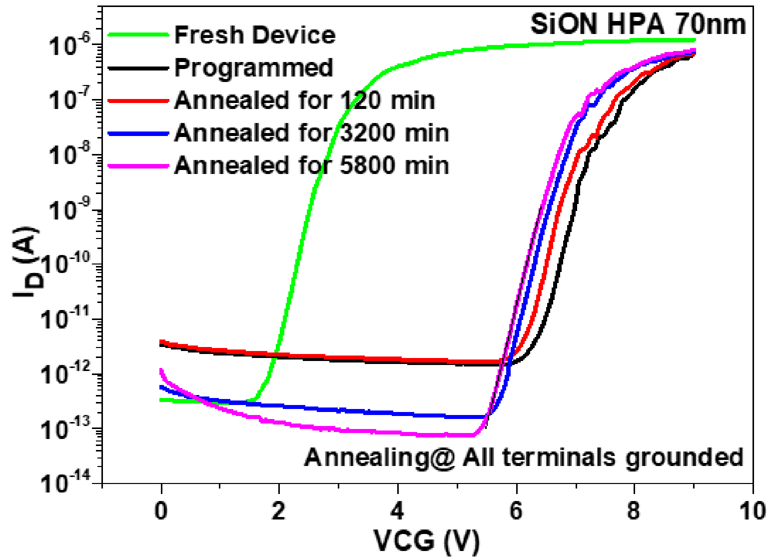


(a)

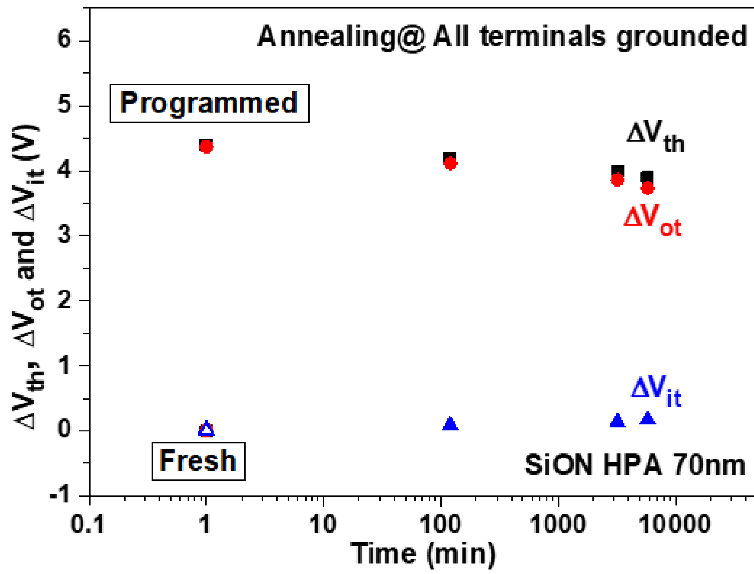


(b)

Fig. 2.4. (a) I_D-V_G curves, (b) V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through programming and RT annealing for SiON devices. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.

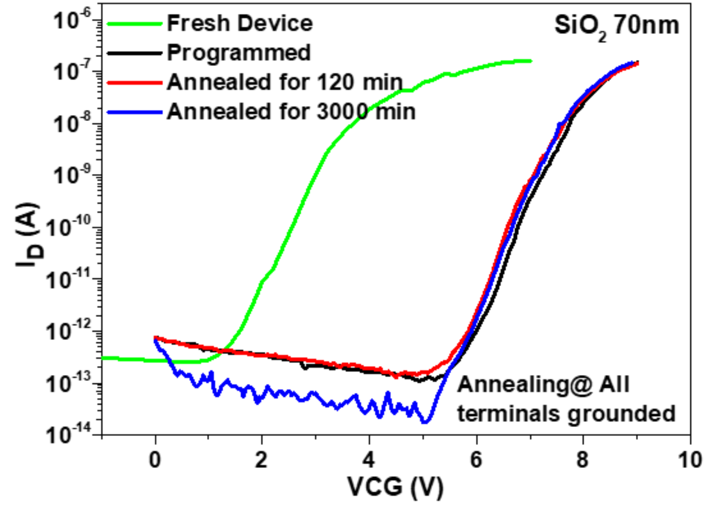


(a)

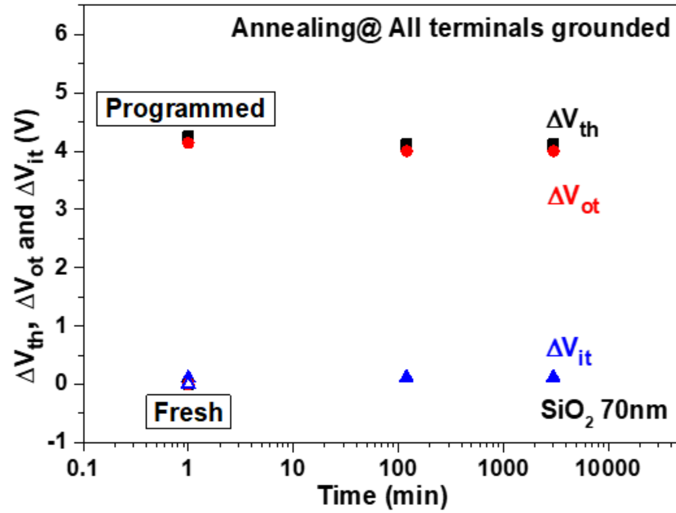


(b)

Fig. 2.5. (a) I_D-V_G curves, (b) V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through programming and RT annealing for SiON devices with HPA. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.



(a)



(b)

Fig. 2.6. (a) I_D-V_G curves, (b) V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through programming and RT annealing for SiON devices with HPA. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.

ΔV_{ot} and ΔV_{it} in Figs. 2.4(b) show that negative trapped charge in the silicon nitride (SiN)

contributes most to V_{th} during programming, with minimal stretch-out due to interface-trap charge buildup at the Si/tunnel-oxide interface during or after device programming.

The retention characteristics of the programmed devices were also investigated; results for SiON devices with HPA are shown in Fig. 2.5. The I_D - V_G curves in Figs. 2.5 (a) and values of ΔV_{ot} and ΔV_{it} in Figs. 2.5(b) show that negative trapped charge in the silicon nitride (SiN) contributes most to V_{th} during programming, with minimal stretch-out due to interface-trap charge buildup at the Si/tunnel-oxide interface during or after device programming, similar to SiON devices.

The retention characteristics of the programmed devices were also investigated; results for SiO_2 devices are shown in Fig. 2.6. The I_D - V_G curves in Figs. 2.6 (a) and values of ΔV_{ot} and ΔV_{it} in Figs. 2.6(b) show that negative trapped charge in the silicon nitride (SiN) contributes most to V_{th} during programming, with minimal stretch-out due to interface-trap charge buildup at the Si/tunnel-oxide interface during or after device programming, similar to SiON devices, in all cases, the V_{th} shift caused by the retention charge loss is not significant, sufficient charge retention is demonstrated to enable successful NVM operation.

2.2.2. Total-ionizing-dose results

V_{th} shifts of pre-programmed devices are plotted vs. total ionizing dose in Fig. 2.7. After irradiation, devices were annealed for 30 min at room temperature and then reprogrammed and annealed again. A significant memory window can be maintained in both SiON and SiO_2 devices

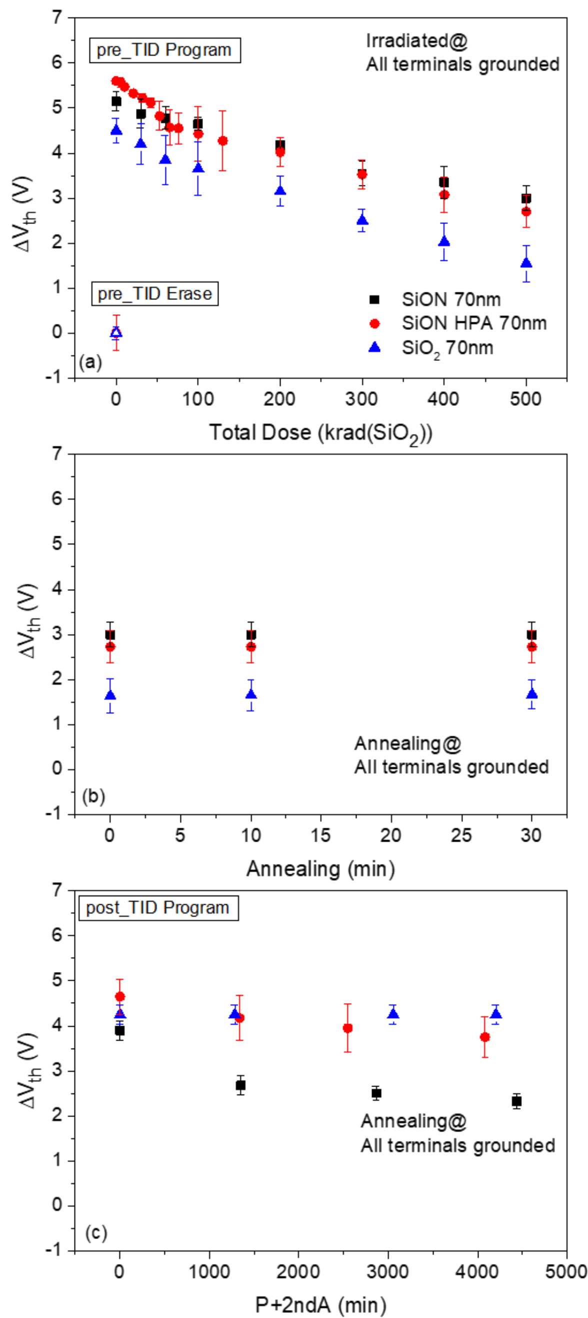


Fig. 2.7. Irradiation, RT annealing, and retention results for pre-programmed devices with SiON and SiO_2 tunneling layers. In (a), devices show V_{th} shifts, relative to pre-programmed values, of ~4.5 V to ~5.5 V after programming and ~1.5 V to ~3 V after TID exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 minutes of RT annealing after TID. (c) shows responses of devices after reprogramming. V_{th} increases but does not fully return to initial programmed values.

having these threshold voltage levels during the entire sequence. Programmed devices show V_{th} reductions of ~2 V at 500 krad(SiO_2). This reduction occurs because (1) trapped electrons are emitted from traps in the nitride and transport out of the dielectric layer during irradiation [39] and (2) radiation-induced positive charges in the SiN or near-SiN tunnel oxide recombine with or compensate a fraction of the electrons stored in the SiN layer [39], [46]-[48], [70], [71]. After irradiation, devices were annealed at room temperature for 30 minutes; recharging electron traps in the SiN during post-irradiation programming more difficult than during the original programming of as-processed (fresh) devices. Reprogrammed devices were annealed at room temperature for at least four days to test retention characteristics. As shown in Fig. 2.7, SiO_2 devices and SiON devices with HPA have superior retention characteristics to SiON devices without HPA after the second programming.

V_{th} shifts of pre-erased devices are plotted vs. total ionizing dose in Fig. 2.8. The sequence of results is similar to Fig. 2.7. Significantly less net radiation-induced trapped positive charge is observed in the SiON devices with HPA than for other types of tunnel oxides, as evidenced by the V_{th} shifts in Fig. 2.8, panel 1. These differences indicate that either fewer radiation-induced holes are trapped or more compensating electrons are trapped in devices with SiON tunnel oxides with HPA than in devices with SiON tunnel oxides without HPA or in devices with SiO_2 tunnel oxides. After irradiation, devices were annealed at room temperature for 30 minutes; V_{th} values do not change significantly during annealing. Reprogrammed devices were annealed at room temperature for at least four days to test retention characteristics. SiO_2 devices and SiON

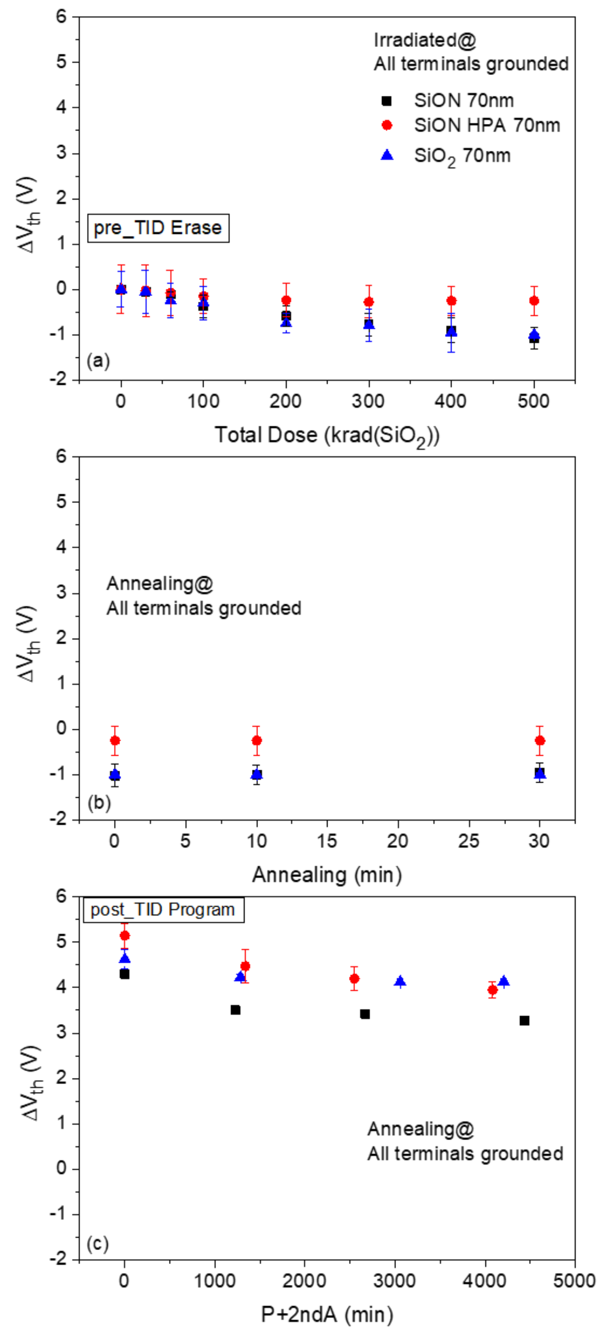
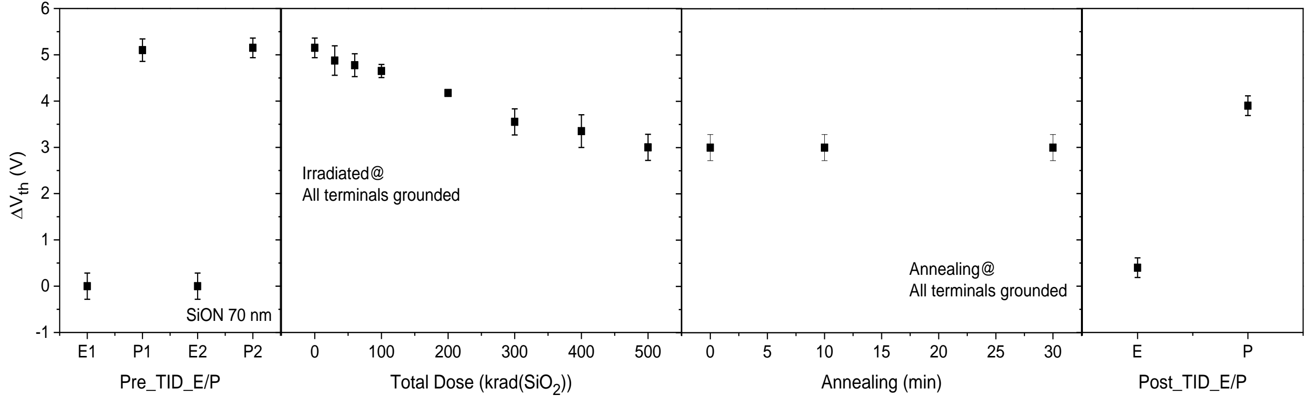
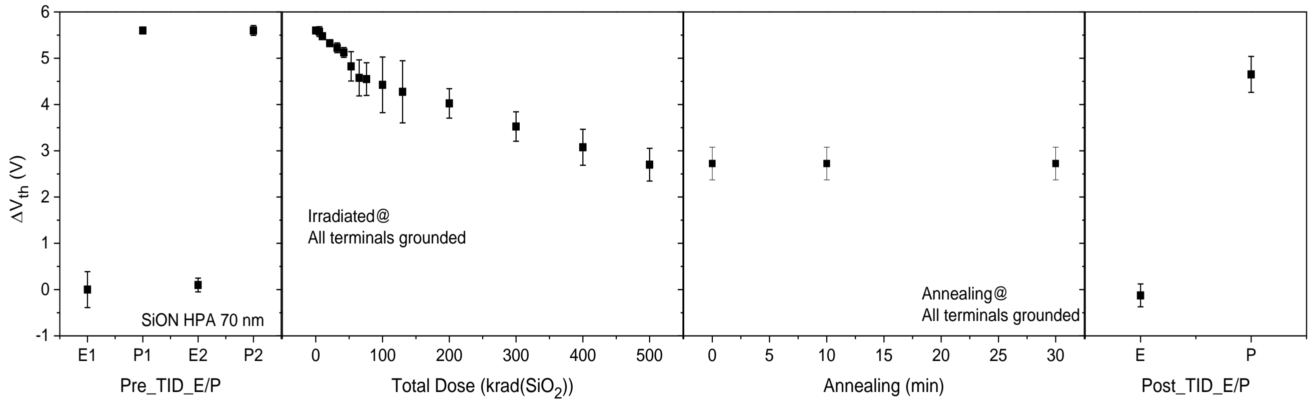


Fig. 2.8. Irradiation, RT annealing, and retention results for devices with SiON and SiO_2 tunneling layers, irradiated in the erased-state. In (a), devices show V_{th} shifts, relative to pre-erased values, of ~0.25 V (SiON HPA) and ~1.0 V (SiON, SiO_2) after exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 min RT annealing. (c) shows responses of devices after reprogramming. V_{th} increases but does not fully return to initial programmed values.



(a)



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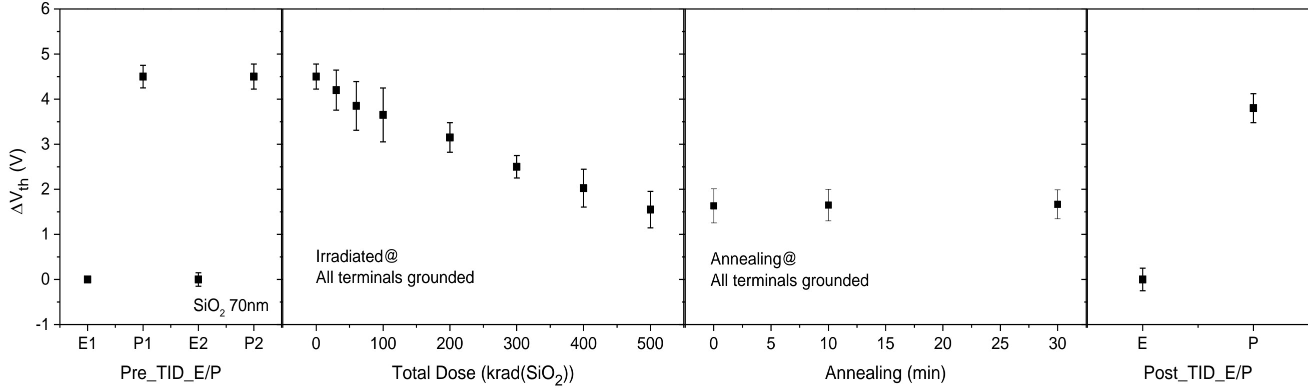


(c)

Fig. 2.9. Threshold voltage shifts during program/erase cycles (Panels 1 and 4) before and after TID irradiation (Panel 2) and annealing (Panel 3) for (a) SiON devices, (b) SiON devices with HPA, and (c) SiO_2 devices.

devices with HPA have superior retention characteristics to SiON devices without HPA after programming, consistent with trends in Fig. 2.7.

Fig. 2.9 shows how threshold voltages shift during multiple program/erase cycles before and after TID. Repeatable programming and erasing are illustrated in the leftmost panel for each device. Decreases in V_{th} are observed in the second panels during TID exposure. Little change is observed during post-irradiation annealing in the third panels. In the right-most panels, devices are successfully erased, but reprogrammed devices do not reach the original levels. Again, a

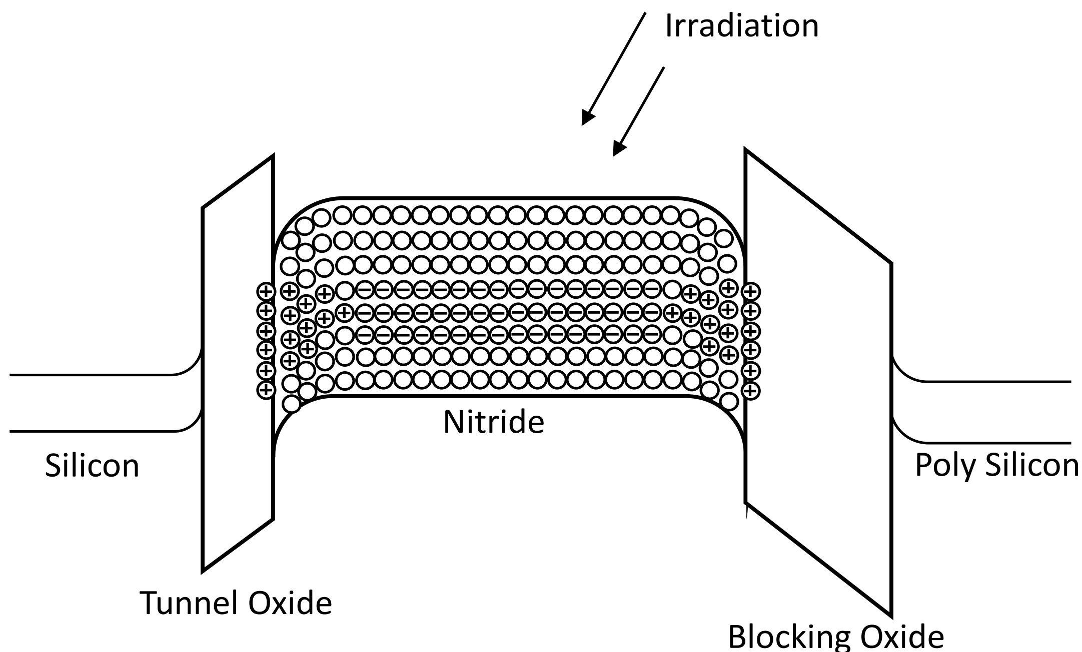


Fig. 2.10. Schematic band diagram for devices that are programmed and irradiated. Empty sites in SiN are represented by circles; trapped electrons and holes are represented by "-" and "+". During irradiation, electron emission primarily depopulates sites near the conduction band edge. Some deeper electron traps are neutralized via hole capture; some programming-induced charge in the SiN is compensated by hole trapping in SiN or the near-SiN tunnel or blocking oxides.

significant memory window can be maintained in NVMs having devices with these threshold voltage levels during the entire sequence.

The charge distribution of devices that are programmed and then irradiated is shown schematically in Fig. 2.10. Holes generated in blocking and tunnel oxides are attracted to the SiN layer by the high negative charge density in programmed devices [39], [46], [49]. Because of the high density of hole traps in silicon nitride [39], [46] and the potential to trap holes in the near-SiN tunnel oxide, many are captured before they can recombine with trapped electrons. Thus, irradiation leads to the emission of trapped electrons from sites near the conduction band edge [39], the neutralization of some deeper traps via hole capture [37], and hole trapping in the near-SiN regions of the blocking and tunnel oxides [39], [46]-[49]. The compensating holes reduce the V_{th} shift without emptying a significant fraction of the deep electron traps [46]. In both Si_3N_4 and SiO_2 layers, a significant fraction of the dipoles formed by compensating trapped charges are highly thermally and electrostatically stable during subsequent irradiation and/or annealing [72]-[75]. Thus, many of the deeper trapping sites populated during the original programming cycle are no longer available when devices are reprogrammed, and the second programming cycle preferentially populates shallower trapping sites in the SiN. Hence, these newly trapped electrons are more easily removed during post-irradiation annealing [72], [73].

Fig. 2.11 – Fig. 2.13 shows I_D-V_G curves through irradiation (a) and post-TID annealing (b), and corresponding values of ΔV_{ot} and ΔV_{it} (c), for devices with SiON tunnel oxide that did not receive H_2/D_2 HPA (Fig. 2.11), SiON tunnel oxides with HPA (Fig. 2.12), and devices with SiO_2

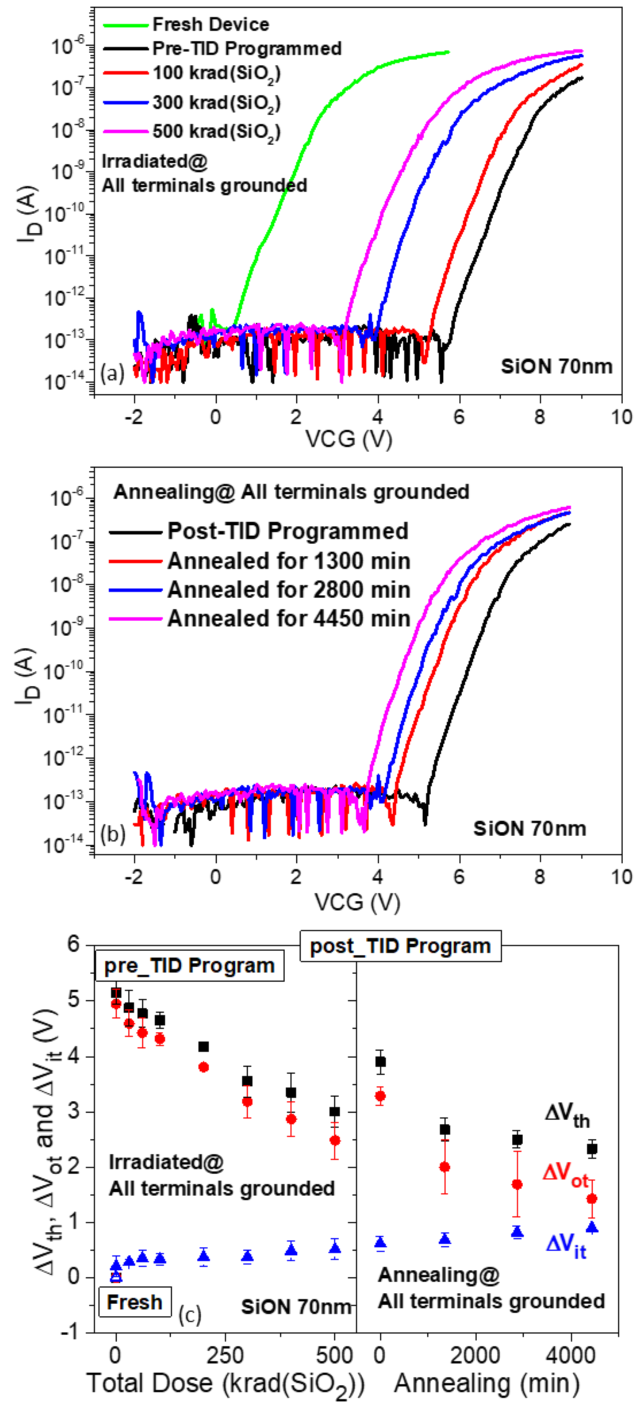


Fig. 2.11. (a) and (b) I_D-V_G curves, and (c) V_{th} shifts and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through irradiation (a) and post-TID retention testing (b) for SiON devices. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.

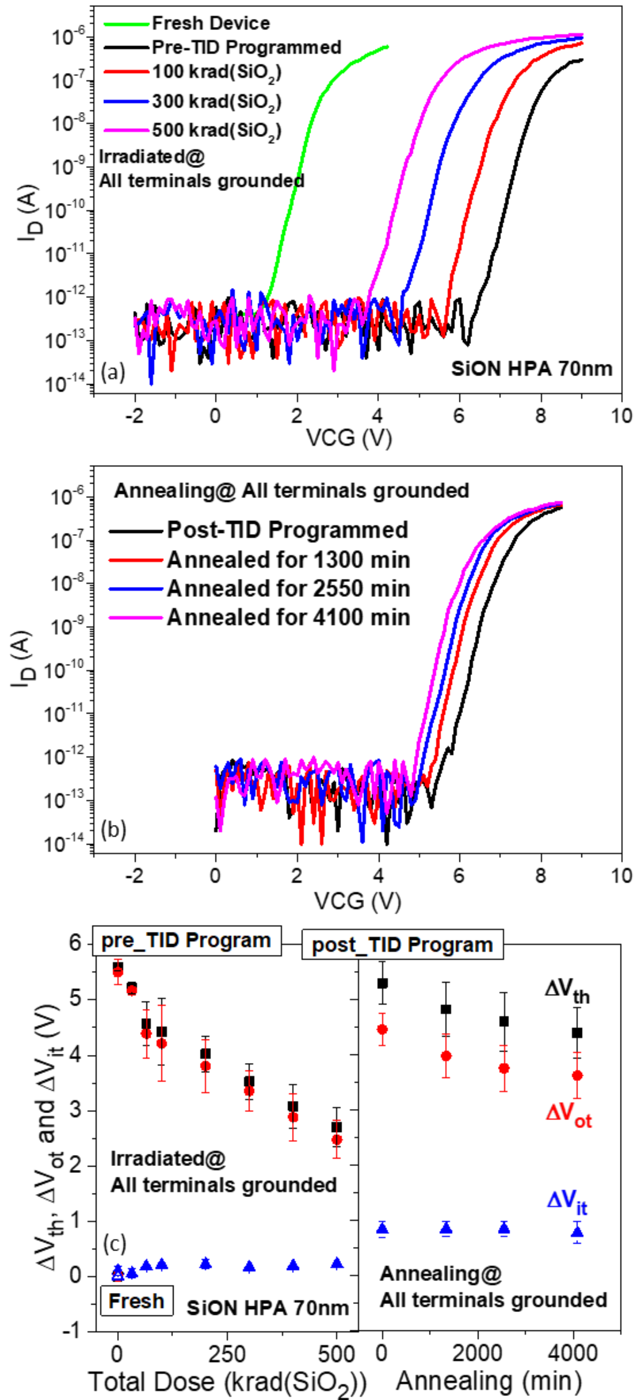


Fig. 2.12. (a) and (b) I_D-V_G curves, and (c) V_{th} shifts and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through irradiation (a) and post-TID retention testing (b) for SiON devices with HPA. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.

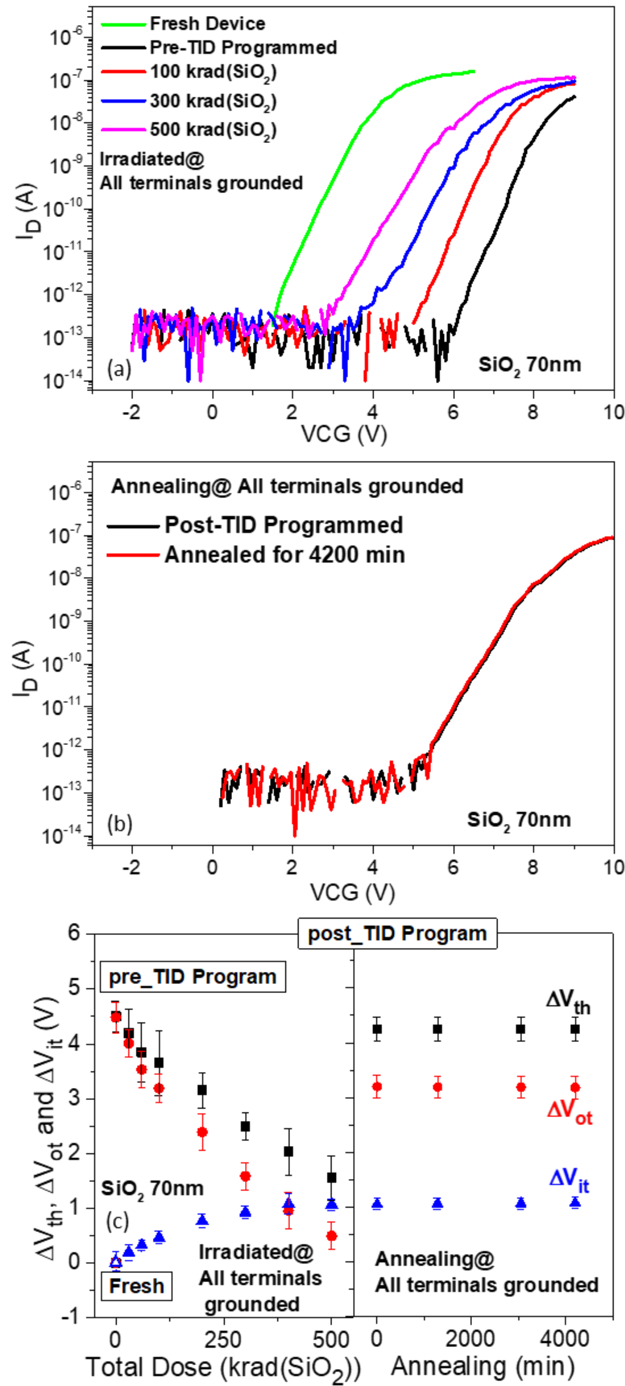


Fig. 2.13. (a) and (b) I_D-V_G curves, and (c) V_{th} shifts and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through irradiation (a) and post-TID retention testing (b) for SiO_2 devices. Values of ΔV_{th}, ΔV_{ot}, and ΔV_{it} are defined relative to those of fresh devices.

tunnel oxides (Fig. 2.13). The I_D-V_G curves of the SiO_2 devices show more significant increases in subthreshold stretch-out with irradiation compared to SiON devices with or without HPA, and thus a higher density of interface traps at the Si/tunnel-oxide interface. Nitrogen incorporation can passivate the silicon dangling bonds and release the strain at the interface of SiON devices [76], [77]. The formation of strong Si-N bonds at the interface also reduces interface-trap formation in programmed [78], [79] and/or irradiated [80], [81] SiON devices. As a result, fewer interface traps are generated during irradiation for devices with SiON tunnel oxides than for devices with SiO_2 tunnel oxides.

The similarity in total interface-trap densities in SiON devices that received HPA treatment in a H_2/D_2 environment and SiON devices that did not receive HPA is due most likely to the negative field that exists in the tunnel oxide during irradiation and annealing as a result of the large negative charge density in the SiN [39], [73]. This negative field causes excess protons that may be released during hole transport in the SiON tunnel oxide with HPA to drift away from the Si/SiO_2 interface, instead of drifting toward the interface and causing additional interface-trap formation [46], [82]-[86]. The post-TID I_D-V_G curves in Fig. 2.13(b) show that values of V_{th} for the SiO_2 device shift very little after annealing for 4200 min. However, the V_{th} of SiON devices shifts significantly after annealing. These differences in annealing response are due to the lower tunneling barrier in SiON devices than for SiO_2 devices. However, even after this reduction of V_{th}, SiON devices that received HPA in H_2/D_2 ambient show the best overall response in this study. These devices (Fig. 2.12(b)) show less charge loss than devices with SiON tunnel oxide

with no HPA annealing (Fig. 2.11(b)), and much less subthreshold stretch-out than devices with SiO_2 tunnel oxides (Fig. 2.13(b)).

2.3. Summary and conclusion

The radiation effects of poly-crystalline Si channel vertical charge trapping NAND devices with SiON and SiO_2 tunneling layers are investigated. Devices show ~ +5 V V_{th} shifts during programming and approximately −2 V V_{th} shifts when irradiated to 500 krad(SiO_2). Irradiated devices cannot be programmed back to original programming levels after irradiation, most likely because trapped holes in the nitride layer compensate deeply trapped electrons, rather than recombining with them. Hence, deep electron trapping sites are not available when irradiated devices are reprogrammed. Programmed devices are still able to be erased successfully after irradiation. In all cases we have considered, devices show sufficient V_{th} shifts after programming, irradiation, and annealing to enable successful operation as NVM devices. Under the programming and irradiation conditions of this study, the devices with SiON tunnel oxides that received HPA treatment in H_2/D_2 ambients show the best overall response.

3. EFFECTS OF GEOMETRY ON THE RADIATION RESPONSE OF NAND MEMORY DEVICES

In this chapter, we have investigated the dimension dependence of TID effects on 3D NAND devices built in a SONOS architecture with SiON tunneling layers. Scaling the channel hole dimension are effective approaches to improve the storage density and reduce cost for NAND applications [87], however the cylindrical geometry has a significant impact on the oxide capacitance and the electrical field cross the oxide and channel [88], [89], therefore will affect the radiation effects and reliability performance of memory devices. Device dimension become more and more critical, but the dimension dependence on their radiation effects is still lack of investigation. Experimental results show that programmed devices show excellent performance up to at least 500 krad(SiO_2) with different dimensions. The dimension dependence of retention performance of devices before and after irradiation are also investigated.

TID effects are an important consideration for the use of nonvolatile memories in high-radiation environments [1], [3]. Nowadays NAND Flash memory devices are based primarily on 3D NAND architecture due to their advantages for high density storage [32]-[34]. Vertical NAND stacks with SONOS type memory cells are the most adopted structure for 3D NAND memories [35], which generally are more radiation-tolerant than floating-gate Flash memories [36]. Scaling channel dimensions can improve storage density and reduce cost for NAND applications [51]; however, the cylindrical geometry associated with modern, vertical

NAND stacks has a significant impact on oxide capacitance and oxide/channel electric field [36], [37]. Thus, it is important to determine the effects of device dimension scaling on the properties of these devices.

We have investigated the effects of channel area on TID effects on 3D NAND devices built in a SONOS architecture with SiON tunneling layers. Programmed and erased devices show excellent performance up to at least 500 krad(SiO_2). Smaller devices show enhanced programmability and greater TID tolerance than larger devices. Devices show worse retention performance after irradiation owing to increased trap assist tunneling. Excellent endurance is observed in pre- and post-irradiation cycling tests.

3.1. Experimental details

Fig. 2.2 shows lateral and top-view cross sections of the SONOS-based 3D NAND devices used in this study [90]. Circular cylindrical holes with 70 to 90 nm diameters are etched vertically in the substrate to serve as source junctions for the memory stack [78], [90]. An ONO gate stack is deposited along the outer circumference of the core hollow cylinder. The charge trapping layer is silicon nitride (SiN). The channel is poly-crystalline Si; the inner volume of the cylinder is filled with SiO_2. This process forms the top selector (TSEL), control gate (CG), and bottom selector (BSEL), with equal channel lengths of 50 nm and 30 nm SiO_2 inter-gate spacing [90].

I_D-V_G characterization and program/erase (P/E) testing are performed using a Keithley

4200A-SCS semiconductor parameter analyzer. To program the devices, 100 μs pulses with increasing amplitudes of 12-24 V are applied to the CG with the BSEL and TSEL gates biased in pass mode at 7 V; the source and drain are grounded. During erasure, the CG bias is incremented from -12 V to -20 V with pulse times of 1 ms. The BSEL and TSEL gates are biased in pass mode at -10 V with source and drain grounded. I_D-V_G curves are measured by sweeping the CG from 0 V to 10 V with the TSEL and BSEL biased at 7 V and the drain biased at 0.5 V [90]. The threshold voltage V_{th} is calculated from the intercept of the drain current with the gate-voltage axis, $V_{GS\text{-}int} - V_{DS/2}$, with the extrapolation taken from the point of maximum first derivative [46], [70].

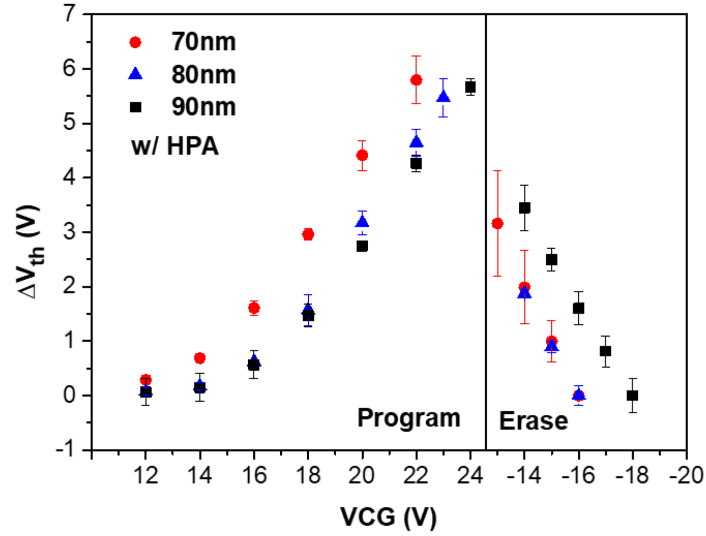
TID irradiation is performed at a rate of 30.3 krad(SiO_2)/min using ~10-keV X-rays [17]. All terminals are grounded during irradiation, corresponding to the storage condition. In this study, devices with different dimensions are (1) programmed and annealed at room temperature for at least four days to test retention, (2) irradiated up to 500 krad(SiO_2) and annealed with all terminals grounded for 30 min at room temperature, and/or (3) subjected to P/E cycling before and after irradiation. For each type of device and condition, results were obtained from at least three devices; average values and error bars denoting standard deviations are shown.

3.2. Experimental results and discussion:

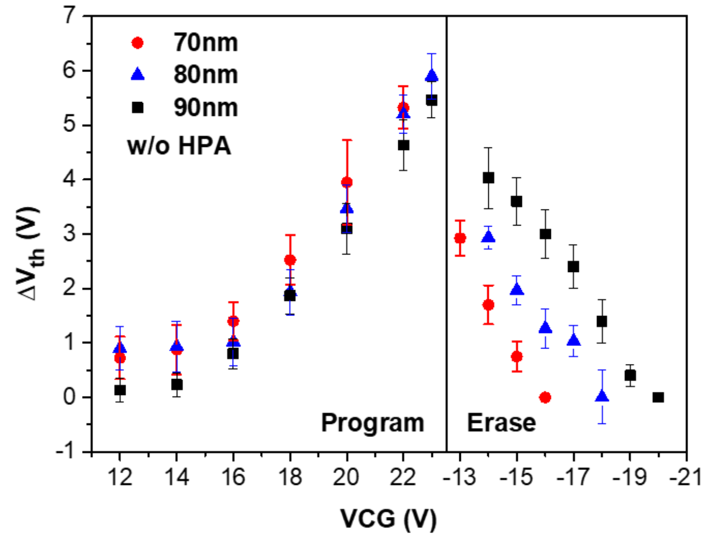
3.2.1. Program and erase characteristic

Fig. 3.1 shows V_{th} shifts for various program and erase voltages for devices with and without

high pressure annealing in H_2/D_2 ambient (HPA) [71], [90]. Devices with hole diameters of 70 nm, 80 nm, and 90 nm are tested. The V_{th} shifts are defined relative to those of devices erased



(a)



(b)

Fig. 3.1. The V_{th} shift under various program and erase voltages for 3D NAND devices with and without HPA and with different dimensions.

with the lowest CG voltage. The programming sequence described in Section 3.1 produces a V_{th} shift of about +5 V due primarily to electron trapping in the SiN layer [39], [47], [90]. These results show that devices with smaller dimensions are programmed and erased more easily than devices with large dimensions, because the increased electric fields during programming in devices with small dimensions increase both the program and erase efficiency of SONOS-based memory devices [88], [89]. The geometrical effects in Fig. 3.1 are more significant than the effects of whether HPA is performed or omitted.

3.2.2. Total ionizing radiation results

Figs. 3.2 and 3.3 show V_{th} shifts for devices programmed before irradiation through a sequence that includes: (1) P/E cycles, (2) irradiation to 500 krad(SiO_2), (3) RT annealing, and (4) post-annealing erasure and programming (Fig. 3.2) with and (Fig. 3.3) without HPA. Figs. 3.4 and 3.5 show similar cycling, irradiation, annealing, and programming sequences for devices (Fig. 3.4) with and (Fig. 3.5) without HPA that were erased without programming before irradiation (pre-erased). All devices are easily and reproducibly programmed and erased before and after irradiation and annealing [90].

Irradiation to 500 krad(SiO_2) neutralizes up to ~60% of the stored electrons [46],[47], [71],[90],[91]. The highest neutralization percentages are observed for the largest diameter devices in Figs. 3.2 and 3.3. Thus, programmed devices with smaller dimensions exhibit higher radiation tolerance than larger-dimension devices. This is due primarily to the effectively thinner

oxides of the more highly scaled (smaller) memory elements [46]. Moreover, the gate-all-around structure of these memory elements provides increasing gate control as the volume of the device decreases [92]-[94].

V_{th} shifts during irradiation are similar for devices with and without HPA, as shown in

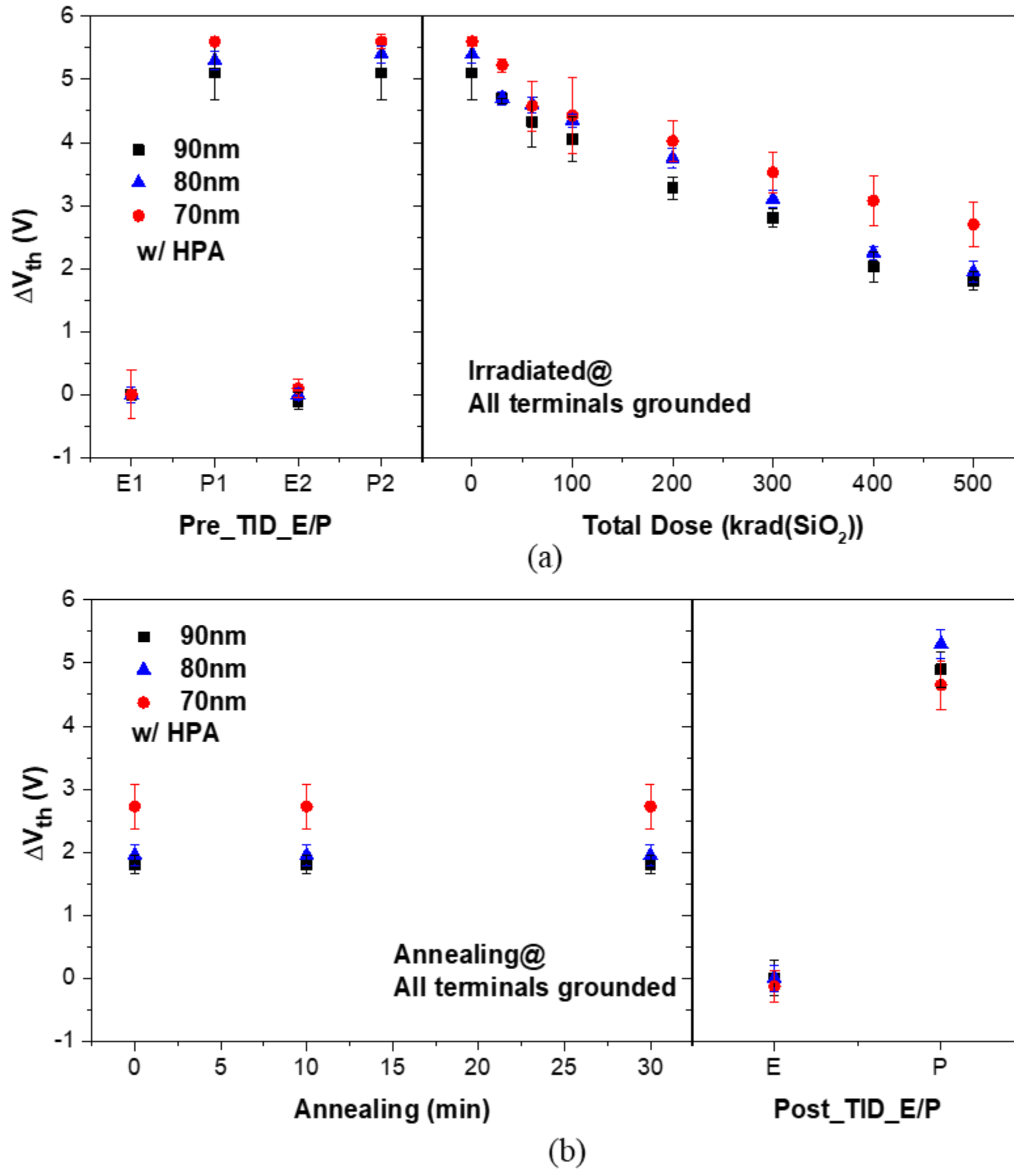


Fig. 3.2. Program/erase cycles before and after irradiation, V_{th} shift during irradiation and RT annealing results for pre-programmed devices with HPA. In (a), pre-programmed devices show V_{th} shifts, relative to

pre-programmed values, of ~5 V to ~5.5 V after programming and ~2 V to ~3 V after TID exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 minutes of RT annealing after TID and devices can be successfully erased and reprogrammed after irradiation.

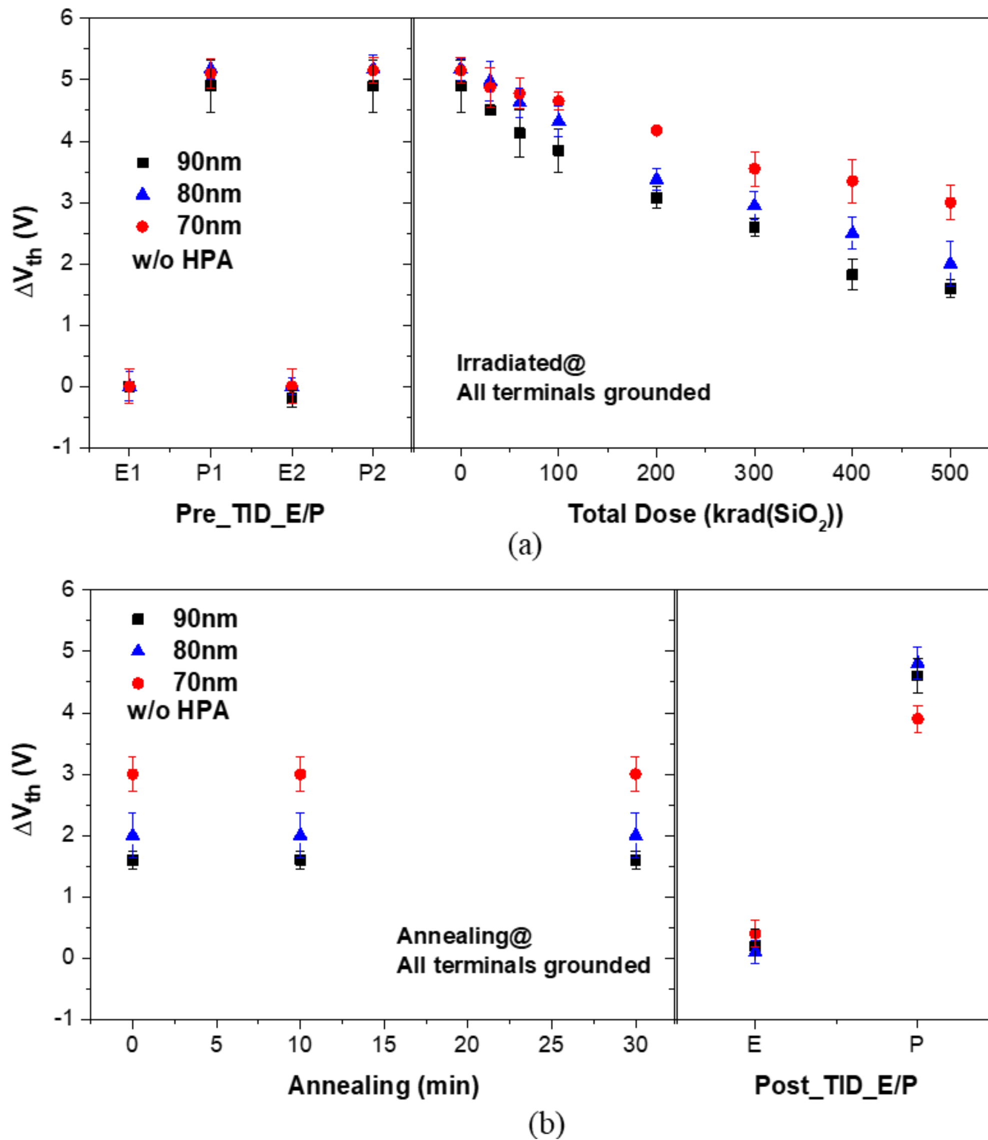
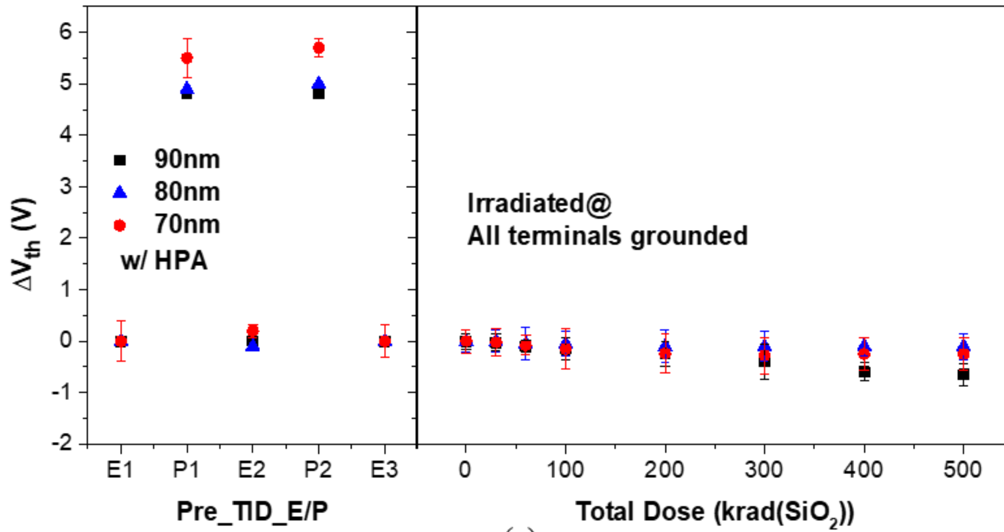
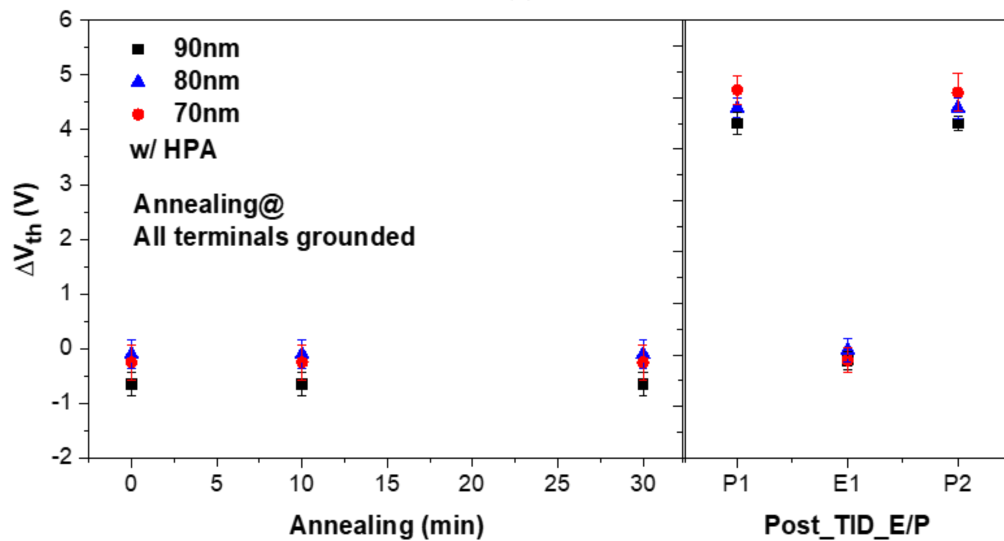


Fig. 3.3. Program/erase cycles before and after irradiation, V_{th} shift during irradiation and RT annealing results for pre-programmed devices without HPA. In (a), pre-programmed devices show V_{th} shifts, relative to pre-programmed values, of ~5 V to ~5.5 V after programming and ~2 V to ~3 V after TID exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 minutes of RT annealing after TID and devices can be successfully erased and reprogrammed after irradiation.

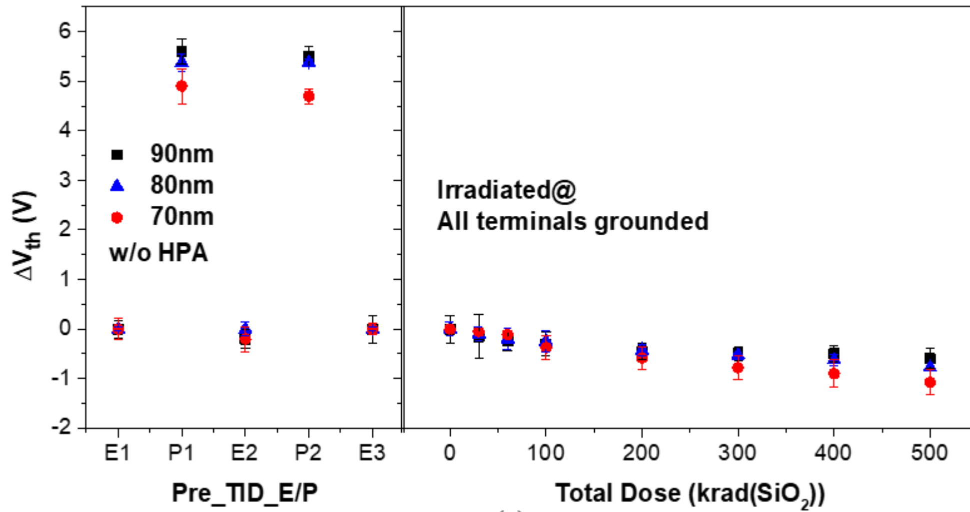


(a)

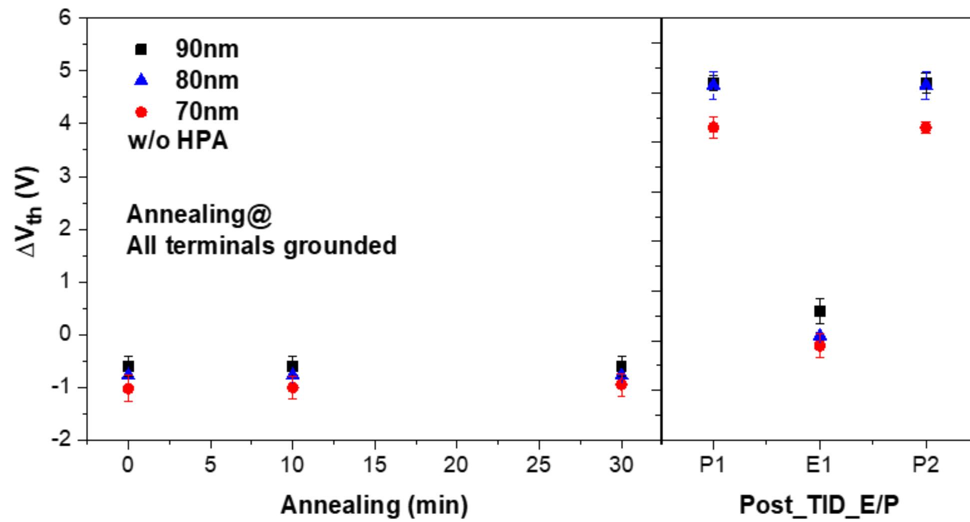


(b)

Fig. 3.4. Program/erase cycles before and after irradiation, V_{th} shift during irradiation and RT annealing results for pre-erased devices with HPA. In (a), pre-erased devices show memory window of ~5 V to ~5.5 V before irradiation and V_{th} shifts of ~0.5 V to ~1 V after TID exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 minutes of RT annealing after TID and devices can be successfully erased and reprogrammed after irradiation.



(a)



(b)

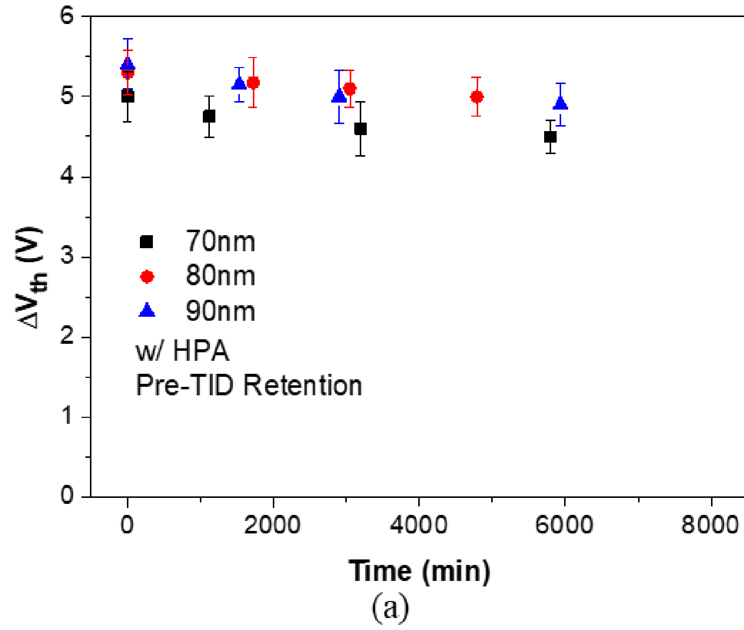
Fig. 3.5. Program/erase cycles before and after irradiation, V_{th} shift during irradiation and RT annealing results for pre-erased devices with HPA. In (a), pre-erased devices show memory window of ~5 V to ~5.5 V before irradiation and V_{th} shifts of ~0.5 V to ~1 V after TID exposure to 500 krad(SiO_2). In (b), V_{th} does not change significantly during 30 minutes of RT annealing after TID and devices can be successfully erased and reprogrammed after irradiation.

Figs. 3.2 and 3.3, respectively. In Figs. 3.4 and 3.5, pre-erased devices show less significant V_{th} shifts during TID irradiation than devices programmed before irradiation (pre-programmed), owing to reduced trapped charge densities and correspondingly lower electric fields during irradiation. For all cases in Fig. 3.2 - 3.5, V_{th} values do not change significantly during 30 min. room-temperature annealing.

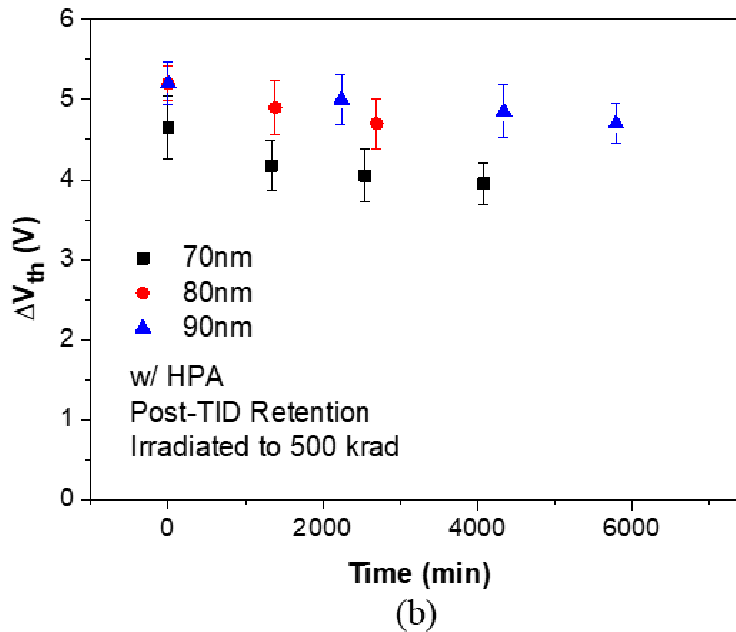
3.2.3. Retention performance results

We also performed retention tests on devices before and after irradiation. Results are shown in Fig. 3.6 for devices with HPA and Fig. 3.7 for devices without HPA. The retention characteristics of unirradiated, programmed devices are shown in (a) of Figs. 3.6 and 3.7. The V_{th} shifts are defined relative to those of erased, unirradiated devices. V_{th} shifts of about 0.5 V occur during RT post-irradiation annealing. In contrast to the programming results in Fig 3.1, the device dimensions do not significantly affect retention performance. This is because the electric fields during programming are determined primarily by the applied voltages, while the electric fields during the retention test are determined entirely by trapped charge densities. So, the differences among electric fields for devices of different geometries during the retention test are smaller than differences during programming. In addition, charge loss during retention testing is determined primarily by trap-assisted tunneling via variable range hopping and/or thermal emission, which depend more weakly on oxide electric field than device programming [3], [39], [95]. After the retention test, devices were irradiated up to 500 krad(SiO_2), fully erased, and reprogrammed with

the same process as before irradiation, and then put into retention testing again. Post-irradiation

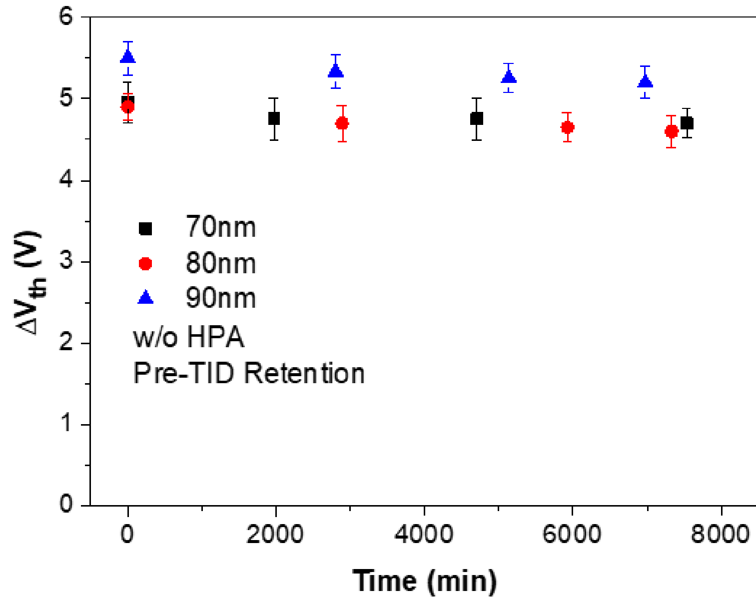


(a)

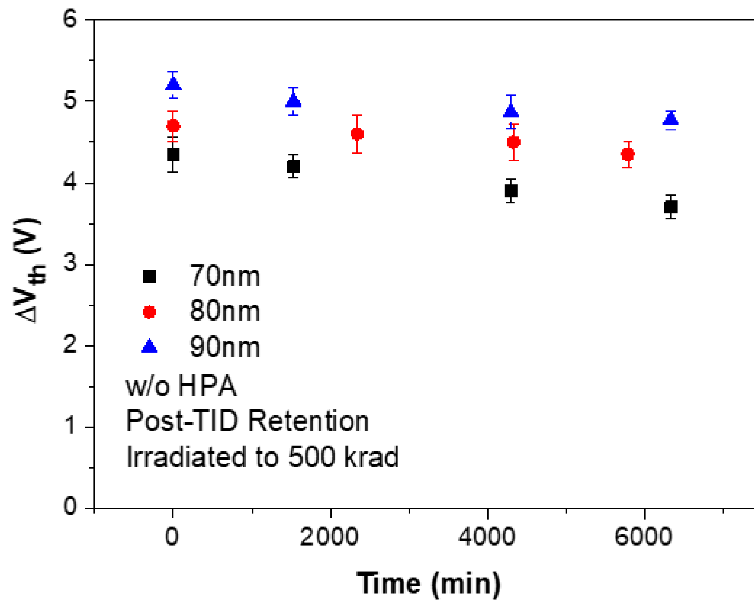


(b)

Fig. 3.6. Retention for devices with HPA. Retention test are carried out during room-temperature storage with all pins grounded for (a) unirradiated devices, and (b) devices that were irradiated to 500 krad(SiO_2) with all pins grounded, fully erased, and reprogrammed before being put onto retention test.



(a)



(b)

Fig. 3.7. Retention for devices without HPA. Retention test are carried out during room-temperature storage with all pins grounded for (a) unirradiated devices, and (b) devices that were irradiated to 500 krad(SiO_2) with all pins grounded, fully erased, and reprogrammed before being put onto retention test.

test results are shown in (b) of Figs. 3.6 and 3.7. Devices show V_{th} shifts of about 0.5 V to 1 V during the post-irradiation retention test. The faster rate of post-irradiation charge loss, compared with unirradiated devices, occurs because radiation-induced charge trapping in the tunnel oxide enhances the rate of trap-assisted tunneling significantly [3], [39]. The HPA process does not have a significant impact on retention. These results show that hydrogen treatments have less impact on charge loss mechanisms in these devices than on interface-trap buildup [39], [86], [90].

3.3. Cycling Test Results

Fig. 3.8 shows the cycling endurance performance for devices with HPA, including: (a) as-processed devices, (b) devices irradiated to 500 krad(SiO_2), (c) devices irradiated to an additional 500 krad(SiO_2), so that the cumulative dose is 1 Mrad(SiO_2). Fig. 3.9 shows the cycling endurance performance for devices without HPA, including: (a) as-processed devices, (b) devices irradiated to 500 krad(SiO_2), (c) devices irradiated to an additional 500 krad(SiO_2), so that the cumulative dose is 1 Mrad(SiO_2). V_{th} shifts of about 5 V were achieved with the first P/E cycle for unirradiated devices, relative to that of the erased state. As-processed devices that received HPA treatments show V_{th} shifts of about –0.5 V for the programmed state and about +0.5 V for the erased state [5], [35], [36]. For as-processed devices without HPA the V_{th} shift with cycling is not as significant. After irradiation, V_{th} does not shift significantly with cycling for devices with and without HPA, as shown in panels Fig. 3.8 and Fig.3., (b) and (c). Only about 0.1 V ~ 0.2 V V_{th} was observed for programmed and erased state with cycling.

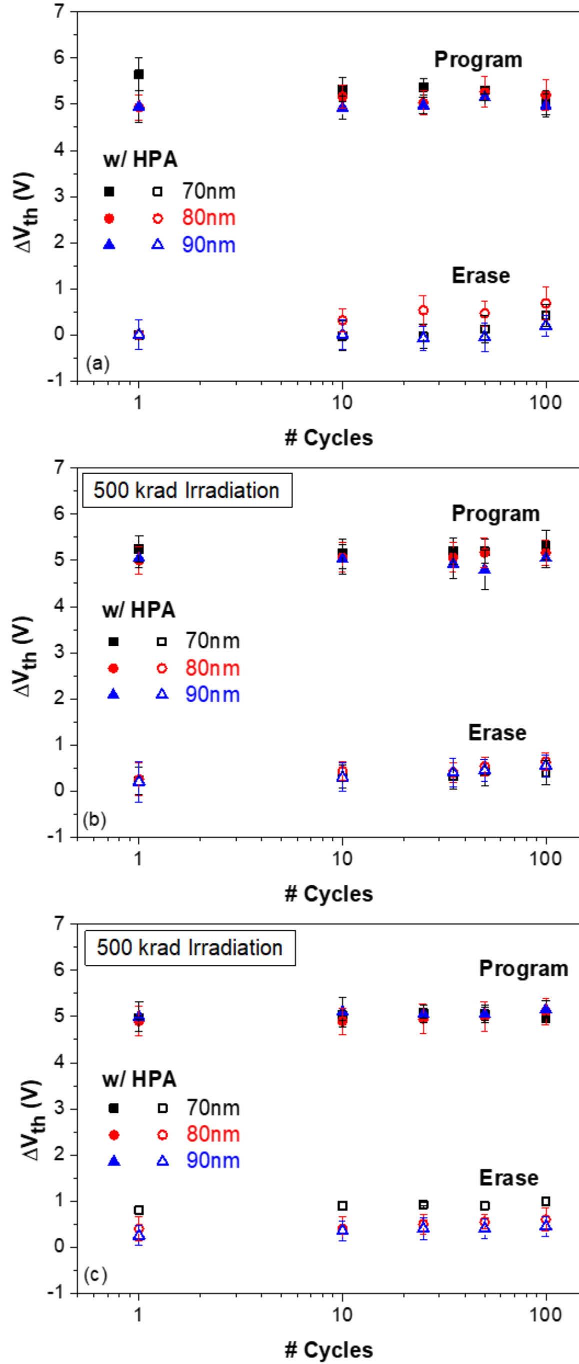


Fig. 3.8. Cycling endurance performance for devices with HPA before and after irradiation. Left to right, (1) as-processed devices are programmed with 22 V ~ 24 V and erased with -17 V ~ -19 V for 100 cycles, (2) devices are irradiated to 500 krad(SiO_2) and then cycled 100 times, and (3) devices are irradiated to 500 krad(SiO_2) again (total 1000 krad(SiO_2)) and then cycled an additional 100 times. All V_{th} shifts are defined relative to those of the erased state that is established after the first P/E cycle for the unirradiated devices.

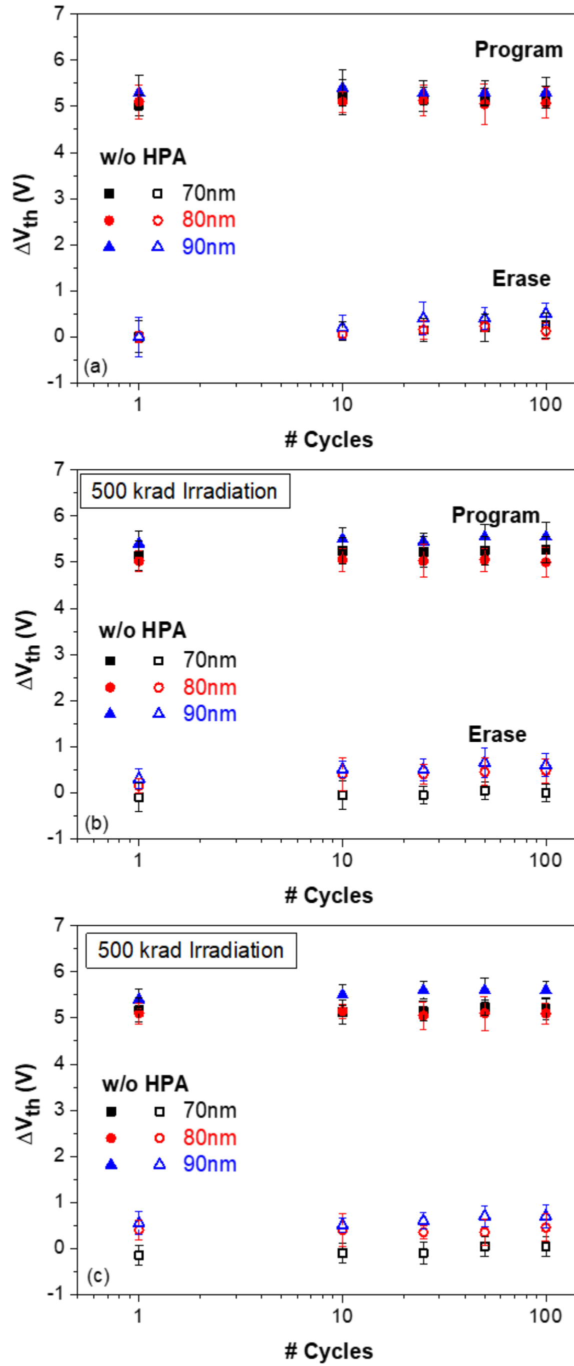


Fig. 3.9. Cycling endurance performance for devices w/o HPA before and after irradiation. Left to right, (1) as-processed devices are programmed with 22 V ~ 24 V and erased with -17 V ~ -19 V for 100 cycles, (2) devices are irradiated to 500 krad(SiO_2) and then cycled 100 times, and (3) devices are irradiated to 500 krad(SiO_2) again (total 1000 krad(SiO_2)) and then cycled an additional 100 times. All V_{th} shifts are defined relative to those of the erased state that is established after the first P/E cycle for the unirradiated devices.

The I_D-V_G curves through the entire cycling sequence for programmed state and erased state of 70nm devices with HPA are shown in Fig. 3.10 – Fig. 3.12 (a) and (b), respectively. And corresponding values of ΔV_{th}, ΔV_{ot} and ΔV_{it} are shown in Fig. 3.10 – Fig. 3.12 (c) for programmed state and Fig. 3.10 – Fig. 3.12 (d) for erased state. The I_D-V_G curves through the entire cycling sequence for programmed state and erased state of 70nm devices without HPA are shown in Fig. 3.13 – Fig. 3.15 (a) and (b), respectively. And corresponding values of ΔV_{th}, ΔV_{ot} and ΔV_{it} are shown in Fig. 3.13 – Fig. 3.15 (c) for programmed state and Fig. 3.13 – Fig. 3.15 (d) for erased state. Values of ΔV_{th}, ΔV_{ot} and ΔV_{it} are defined relative to those of fresh devices. From the charge separation results, the V_{th} shift for the programmed state in as-processed devices decreases during cycling due primarily to the loss of electrons in the trapping layer [39], [95], [96]. The V_{th} shift for the erased state of as-processed devices increases during cycling owing to the buildup of interface traps and negatively charged oxide traps. As shown in Fig. 6 for the 70 nm devices with HPA that were irradiated to a cumulative dose of 1 Mrad(SiO_2), the differences between V_{th} values for the programmed and erased states decrease by about 1.5 V, relative to the responses of unirradiated devices. The decrease in the effective memory window results from three factors: (1) net radiation-induced hole trapping in the tunnel oxide, (2) charge loss from the SiN layer due to electron emission and/or charge neutralization via hole capture during irradiation, and (3) the buildup of interface traps at the tunnel oxide/channel interface [39], [90], [96].

V_{th} shifts during TID irradiation for uncycled and cycled devices with HPA are shown in

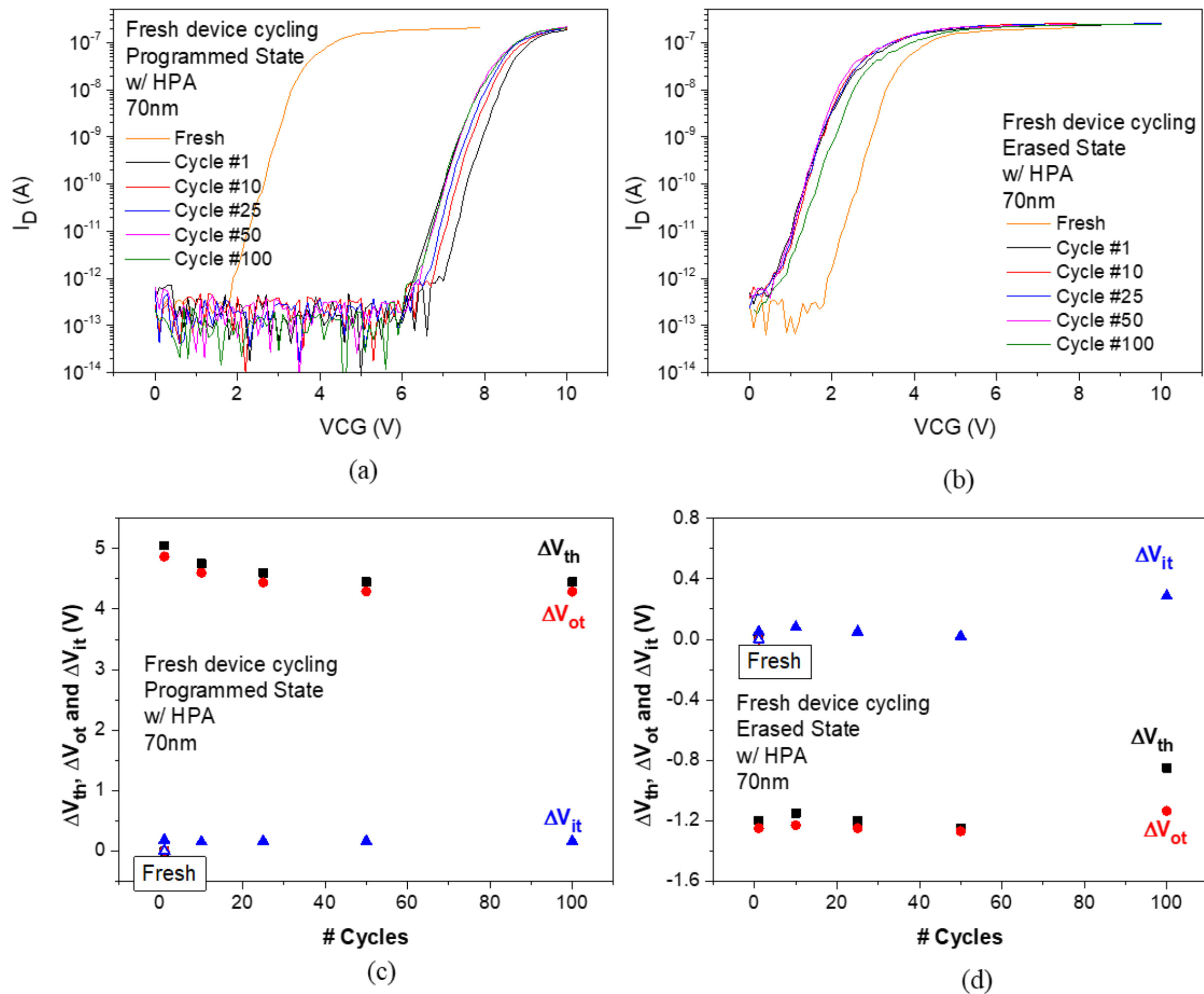


Fig. 3.10. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of as-processed 70nm devices with HPA. Devices show about 0.5 V V_{th} decrease for programmed-state and about 0.5 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

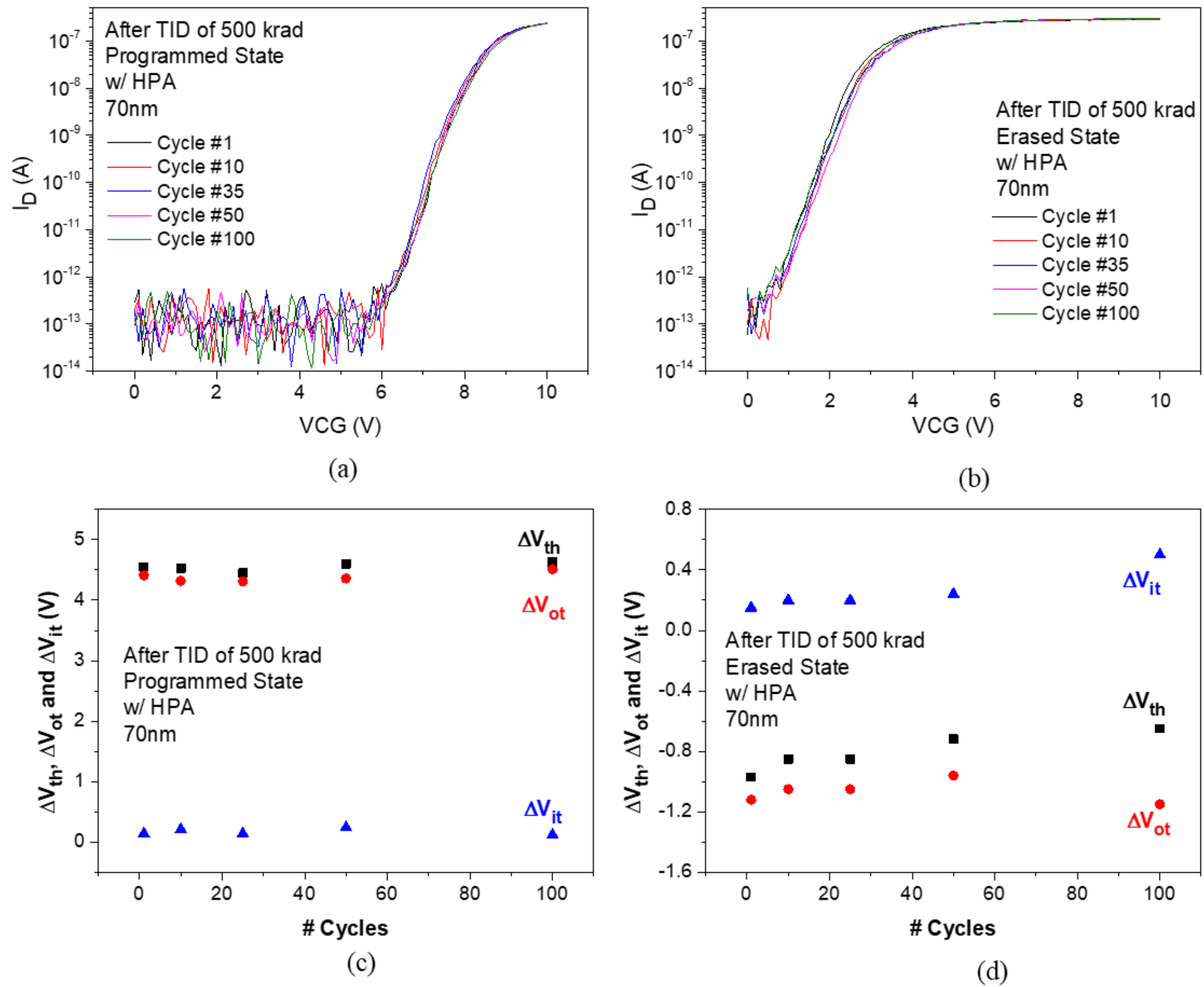


Fig. 3.11. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of 70nm devices with HPA irradiated to 500 krad(SiO_2). Devices show about 0.1 V V_{th} decrease for programmed-state and about 0.3 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

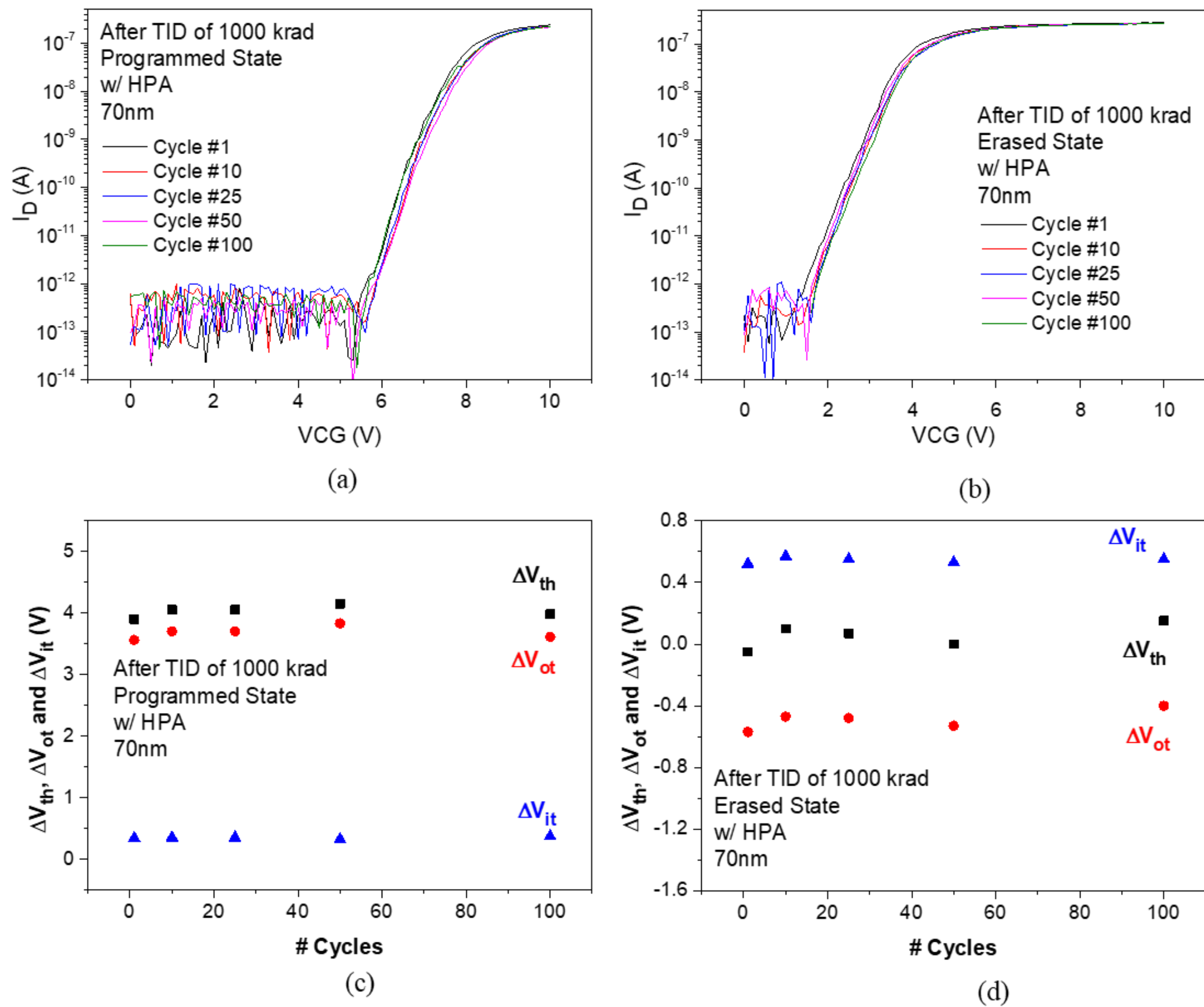


Fig. 3.12. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of 70nm devices with HPA irradiated to a cumulative dose of 1 Mrad(SiO_2). Devices show about 0.1 V V_{th} decrease for programmed-state and about 0.2 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

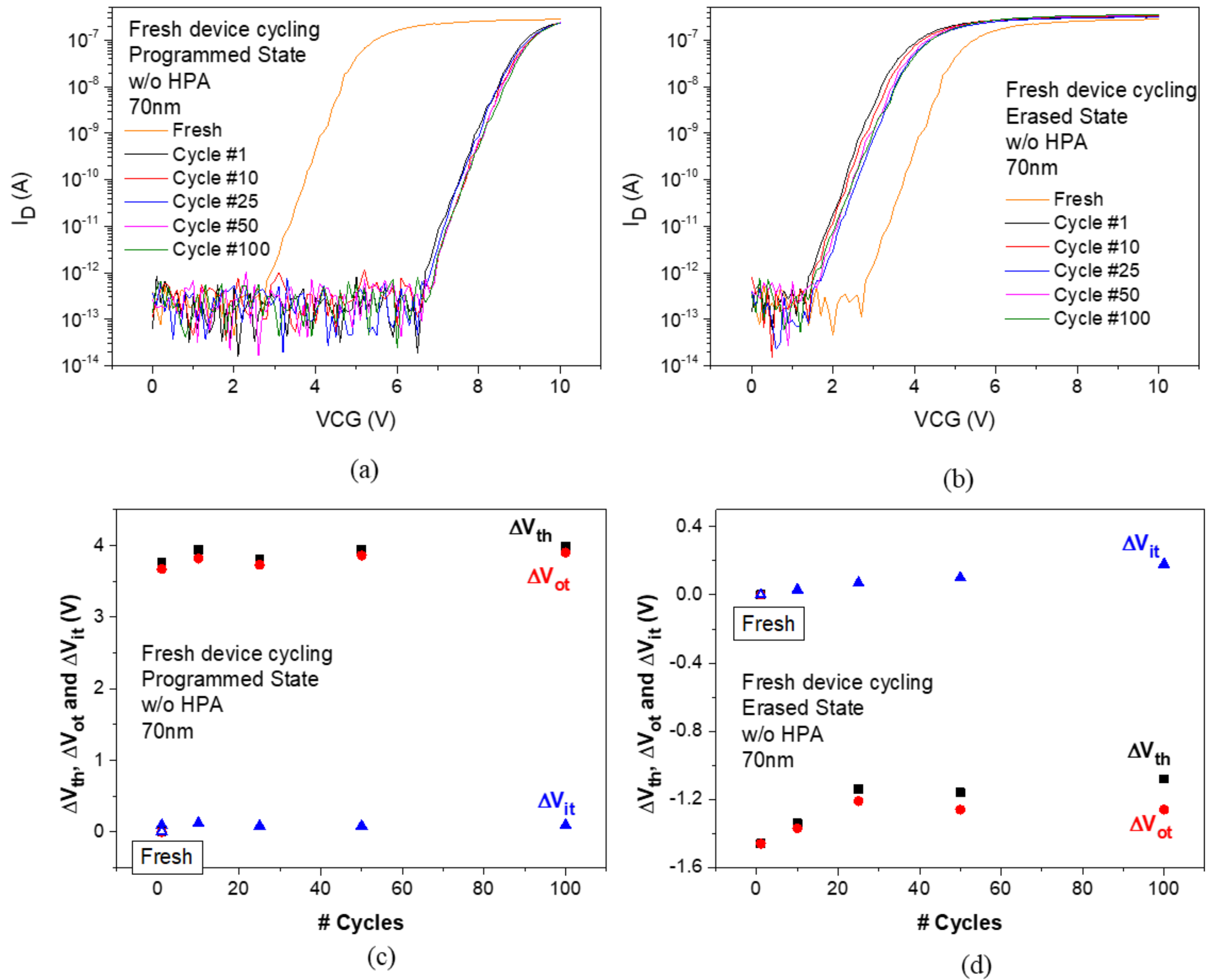


Fig. 3.13. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of as-processed 70nm devices without HPA. Devices show about 0.1 V V_{th} increase for programmed-state and about 0.5 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

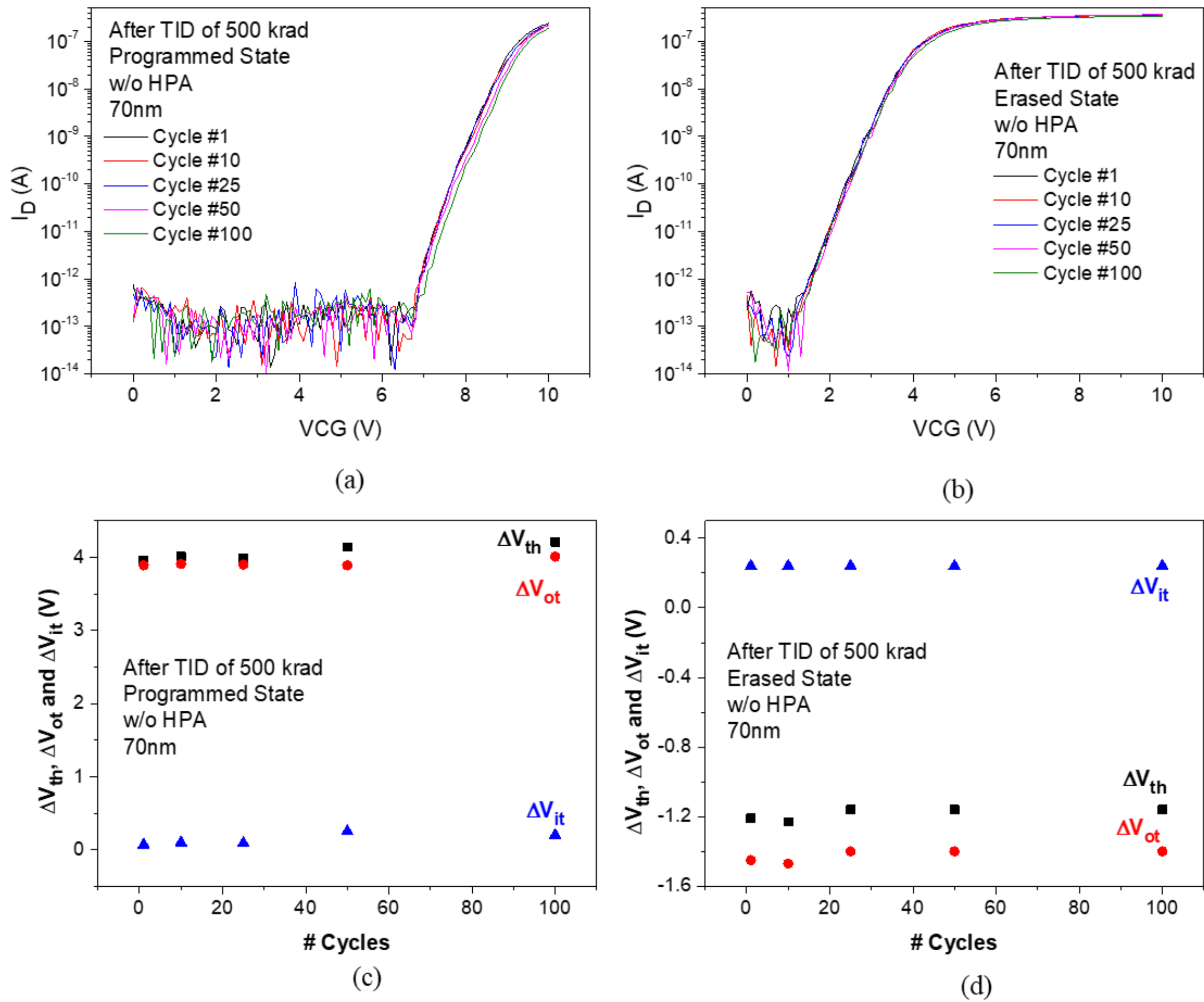


Fig. 3.14. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of 70nm devices without HPA irradiated to 500 krad(SiO_2). Devices show about 0.1 V V_{th} increase for programmed-state and about 0.1 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

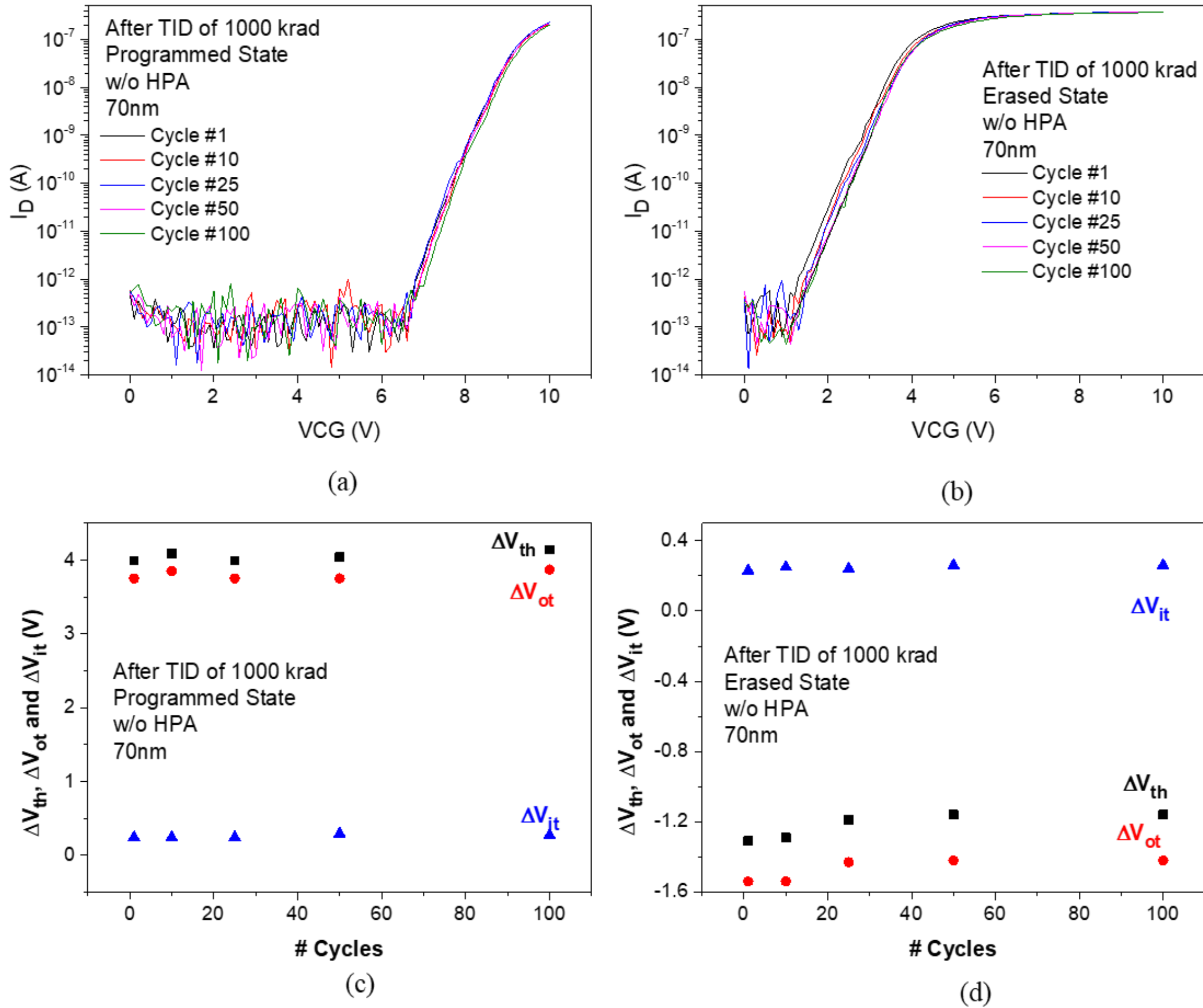


Fig. 3.15. I_D-V_G curves, V_{th} shifts, and components due to oxide and interface-trap charge, ΔV_{ot} and ΔV_{it}, through the cycling endurance test sequence for (a) and (c) programmed state, and (b) and (d) erased state of 70nm devices with HPA irradiated to a cumulative dose of 1 Mrad(SiO_2). Devices show about 0.05 V V_{th} increase for programmed-state and about 0.1 V V_{th} increase for erased-state, owing to the buildup of interface traps and oxide traps, as well as the charge loss in the trapping layer, as show in (c) and (d).

Figs. 3.16(a) and 3.16(b); results for uncycled and cycled devices without HPA are shown in Figs. 3.16(c) and 3.16(d). For both splits, as-processed and cycled devices were irradiated to

500 krad(SiO_2). Even though the P/E cycling are known to introduce oxide and interface traps [97],[98], the results of Fig. 3.16 show that modest P/E cycling does not significantly add to the radiation-induced charge loss for these devices under these irradiation and cycling conditions.

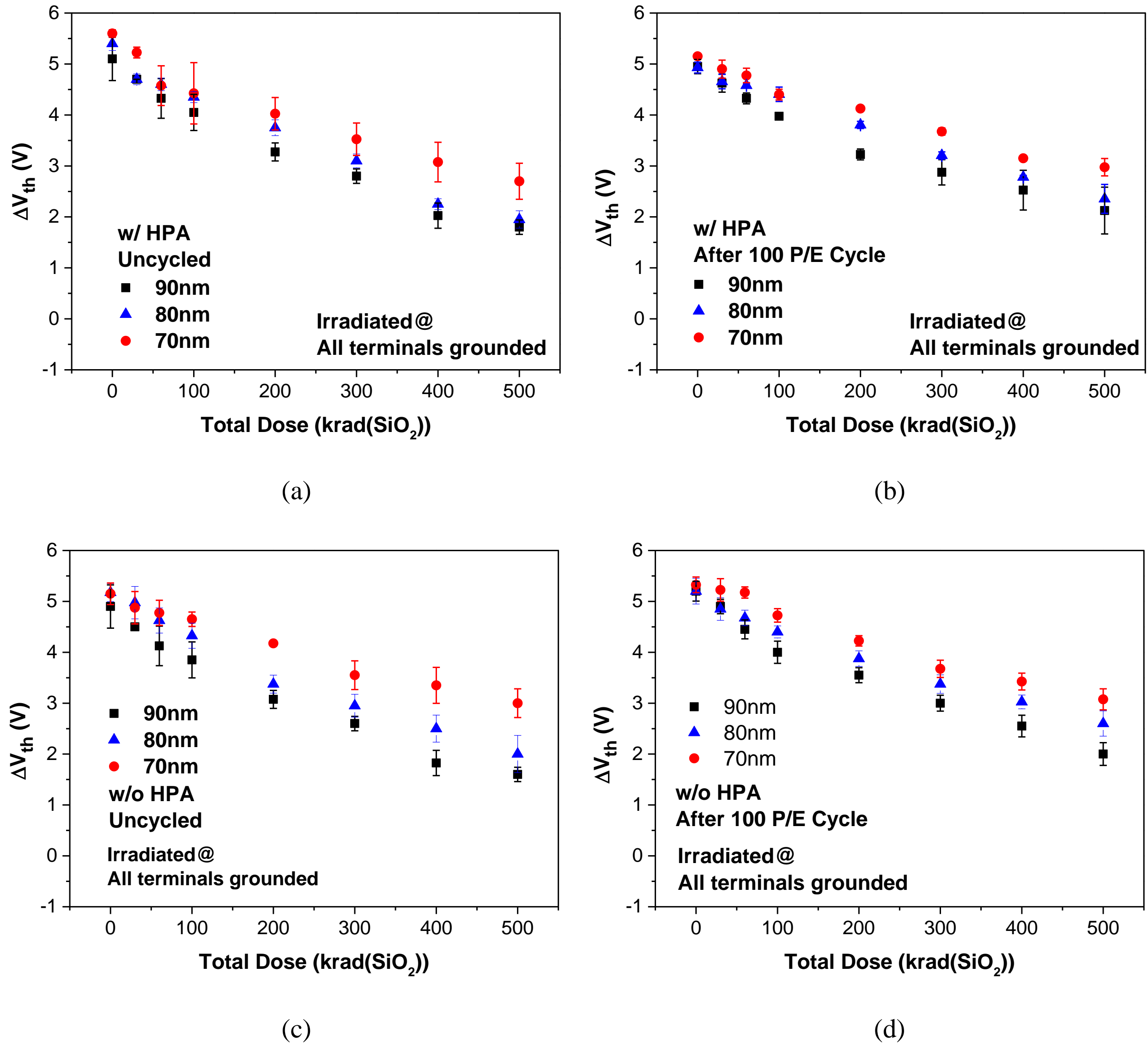


Fig. 3.16. Threshold voltage shifts during TID irradiation for (a) uncycled and (b) cycled devices with HPA and (c) uncycled and (d) cycled devices without HPA.

3.4. Summary

The effects of channel area on the total-ionizing dose response of 3D NAND devices built in a SONOS architecture with SiON tunneling layers were evaluated. Programmed and erased devices show excellent radiation response and endurance up to at least 500 krad(SiO_2). Smaller devices show enhanced programmability and greater TID tolerance than larger devices, which is a very positive trend for future size scaling of charge-trapping NAND memories. Devices at all dimensions tested are able to be erased and programmed successfully after irradiation. Retention performance of irradiated devices is worse compared to unirradiated devices, owing to radiation-induced oxide- and interface-trapped charge buildup. Excellent endurance is observed during cycling tests performed before and after irradiation. Devices irradiated to a cumulative dose of 500 krad(SiO_2) exhibit a decrease in maximum possible memory window of up to 1.5 V, owing to the charge loss from the SiN layer and buildup of interface traps at the tunnel oxide/channel interface, but remain capable of operation as NV memory elements.

4. CONCLUSION

This work focuses on evaluating TID effects and reliability issues in vertical-charge-trapping NAND devices with SiON and SiO_2 tunnel layers. We test devices with three different processes: devices with SiON tunnel layer and without HPA; devices with SiON tunnel layer and with HPA; devices with SiO_2 tunnel layer and without HPA. We evaluated the devices pregame/erase efficiency, the TID test were carried out for both programed and erased devices with different dimensions. And the reliability performance such as endurance and retention of those devices are investigated before and after irradiation. The overall performance of devices with different tunnel layers and different annealing processes are compared. And detailed analysis of the underlying mechanism is provided for the experimental results, which will be useful for future device performance improvement.

The program/erase efficiency are evaluated for 70 nm devices with different tunnel layers, devices with SiO_2 tunnel show less efficiency due to their larger band barrier height. Devices show ~ +5 V V_{th} shifts during programming and approximately −2 V V_{th} shifts when irradiated to 500 krad(SiO_2), because radiation-induced positive charge either recombines with or compensates a fraction of the stored electrons in trapping layer during irradiation. It's interesting to note that irradiated devices cannot be programmed back to original programming levels after irradiation, because trapped holes in the nitride layer compensate deeply trapped electrons, rather than recombining with them. For all the devices under testing, their V_{th} shift caused by the

retention charge loss is not significant, sufficient charge retention is demonstrated to enable successful NVM operation. Under the programming and irradiation conditions of this study, the devices with SiON tunnel oxides that received HPA treatment in H_2/D_2 ambients show the best overall response.

The effects of channel area on the TID response for devices with SiON tunneling layers were also evaluated. Programmed and erased devices with different dimensions show excellent radiation response and endurance up to at least 500 krad(SiO_2). Smaller devices show enhanced programmability and greater TID tolerance than larger devices, owing to the increased electric fields and gate control ability in devices with small dimensions, which is a very positive trend for future size scaling of charge-trapping NAND memories. Devices at all dimensions tested are able to be erased and programmed successfully after irradiation. Retention performance of irradiated devices is worse compared to unirradiated devices, owing to radiation-induced oxide- and interface-trapped charge buildup. Excellent endurance is observed during cycling tests performed before and after irradiation. Devices irradiated to a cumulative dose of 500 krad(SiO_2) exhibit a decrease in maximum possible memory window of up to 1.5 V, owing to the charge loss from the SiN layer and buildup of interface traps at the tunnel oxide/channel interface, but remain capable of operation as NV memory elements.

5. REFERENCES

[1] R. E. Fontana Jr and M. D. Gary, "Moore's law realities for recording systems and memory storage components: HDD, tape, NAND, and optical," *AIP Adv.*, vol. 8, no. 5, pp. 056506-1-056506-5, 2018.

[2] A. S. Spinelli, C. M. Compagnoni and A. L. Lacaita, "Reliability of NAND flash memories: Planar cells and emerging issues in 3D devices," *Computers*, vol. 6, no. 2, pp. 1-55, Apr. 2017.

[3] C. M. Compagnoni and A. S. Spinelli, "Reliability of NAND flash arrays: A review of what the 2-D–to–3-D transition meant," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4504-4516, Jun. 2019.

[4] C. M. Compagnoni, et al., "Reviewing the evolution of the NAND flash technology." *Proceedings of the IEEE,* vol. 105, no. 9, pp. 1609-1633, Mar. 2017.

[5] S. Lee et al., "A 1Tb 4b/cell 64-stacked-WL 3D NAND Flash memory with 12 MB/s program throughput," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 340-341, Feb. 2018.

[6] D. Kang, et al., "A 512 Gb 3-bit/cell 3D 6th -generation V-NAND Flash memory with 82 MB/s write throughput and 1.2 Gb/s interface," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 216-217, Feb. 2019.

[7] J. Hwang, et al., "A middle-1X nm NAND Flash memory cell (M1XNAND) with highly manufacturable integration technologies," *International Electron Devices Meeting (IEDM)*, pp. 199-202, Dec. 2011.

[8] H. Kim, S.-J. Ahn, Y. G. Shin, K. Lee, and E. Jung, "Evolution of NAND Flash memory: From 2D to 3D as a storage market leader," *2017 IEEE International Memory Workshop (IMW)*, pp. 7-10, May. 2017.

[9] J. Lee, J. Jang, J. Lim, Y. G. Shin, K. Lee, and E. Jung, "A new ruler on the storage market: 3D-NAND Flash for high-density memory and its technology evolutions and challenges on the future," *International Electron Devices Meeting (IEDM)*, pp. 284–287, Dec. 2016.

[10] K. Parat and C. Dennison, "A floating gate based 3D NAND technology with CMOS under array," *International Electron Devices Meeting (IEDM)*, pp. 48–51, Dec. 2015.

[11] H. Tanaka, et al., "Bit cost scalable technology with punch and plug process for ultra-high density Flash memory," *2007 IEEE Symposium on VLSI Technology*., pp. 14–15, Jun. 2007.

[12] R. Katsumata, et al., "Pipe-shaped BiCS Flash memory with 16 stacked layers and multi-level-cell operation for ultra-high density storage devices," *2009 Symposium on VLSI Technology*, pp. 136-137, Jun. 2009.

[13] K. Kanda, et al., "A 120 mm 2 16 Gb 4-MLC NAND Flash memory with 43 nm CMOS technology," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 430-431, Feb. 2008.

[14] F. Masuoka, M. Momodomi, Y. Iwata, and R. Shirota, "New ultra-high density EPROM and Flash EEPROM with NAND structure cell," *International Electron Devices Meeting (IEDM)*, pp. 552-555, Dec. 1987.

[15] M. Momodomi, et al., "New device technologies for 5 V-only 4 Mb EEPROM with NAND structure cell," *International Electron Devices Meeting (IEDM)*, pp. 412-415, Dec. 1988.

[16] R. Micheloni and L. Crippa, "Multi-bit NAND Flash memories for ultra-high density storage devices," *Advances in Non-volatile Memory and Storage Technology*, pp. 75–119, Jun. 2014.

[17] R. Kirisawa, S. Aritome, R. Nakayama, T. Endoh, R. Shirota, and F. Masuoka, "A NAND structured cell with a new programming technology for highly reliable 5 V-only Flash EEPROM," *IEEE Symposium on VLSI Technology*, pp. 129–130, Jun. 1990.

[18] R. Shirota, et al., "A 2.3 μm^2 memory cell structure for 16 Mb NAND EEPROMs," *International Electron Devices Meeting (IEDM)*, pp. 103–106, Dec. 1990.

[19] K.-D. Suh, et al., "A 3.3 V 32 Mb NAND Flash memory with incremental step pulse programming scheme," *IEEE J. Solid-State Circuits*, vol. 30, no. 11, pp. 1149–1156, Nov. 1995.

[20] T. Tanaka, et al., "A quick intelligent program architecture for 3 V-only NAND-EEPROMs," *IEEE Symposium on VLSI Technology*, pp. 20–21, Jun. 1992.

[21] G.J. Hemink, et al., "Fast and accurate programming method for multi-level NAND EEPROMs," *1995 Symposium on VLSI Technology. Digest of Technical Papers*, pp. 129–130, Jun. 1995.

[22] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet and V. Ferlet-Cavrois, “Radiation effects in MOS oxides,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[23] R. C. Hughes, “Charge-carrier transport phenomena in amorphous SiO_2: Direct measurement of the drift mobility and lifetime,” *Phys. Rev. Lett.*, vol. 30, pp. 1333-1336, Jun. 1973.

[24] R. C. Hughes, “Hole mobility and transport in thin SiO_2 films,” *Appl. Phys. Lett.*, vol. 26, no. 8, pp. 436-438, Apr. 1975.

[25] H. E. Boesch, Jr., F. B. McLean, J. M. McGarrity, and G. A. Ausman, Jr., “Hole transport and charge relaxation in irradiated SiO_2 MOS capacitors,” *IEEE Trans. Nucl. Sci.*, Vol. 22, no. 6, pp. 2163-2167, 1975.

[26] A. Scarpa, et al., “Ionizing radiation induced leakage current on ultra-thin gate oxides,” *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 1818-1825, Dec. 1997.

[27] M. Ceschia, et al., “Radiation induced leakage current and stress induced leakage current in ultra-thin gate oxides,” *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2375-2382, Dec. 1998.

[28] G. Cellere, et al., “Radiation induced leakage current in floating gate memory cells,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2144-2152, Dec. 2005.

[29] P. M. Lenahan, J. P. Campbell, A. Y. Kang, S. T. Liu, and R. A. Weimer, “Radiation-induced leakage currents: Atomic scale mechanisms,” *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 2101–2106, Dec. 2001.

[30] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, “Charge yield for cobalt-60 and 10-keV x-ray irradiations of MOS devices,” *IEEE Trans. Nucl. Sci.*, vol. 38, no. 6, pp. 1187–1194, Dec. 1991.

[31] J. F. Conley and P. M. Lenahan, “Room temperature reactions involving silicon dangling bond centers and molecular hydrogen in amorphous SiO_2 thin films on silicon,”. *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 2186-2191, Dec. 1992.

[32] A. Subirats, et al., “Impact of discrete trapping in high pressure deuterium annealed and doped poly-Si channel 3D NAND macaroni,” *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, pp. 5A-2.1-5A-2.6, Apr. 2017.

[33] K. Wu, et al. “SONOS device with tapered bandgap nitride layer,” *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 987-992, May 2005.

[34] J. W. Hill-Lindsay and J. T. Yuen, “Ultra-high impact resistant digital data recorder for missile flight testing,” *IEEE Trans. Compon. Packag. Manuf. Technol. A*, vol. 17, no. 3, pp. 398-403, Sep. 1994.

[35] M. H. White, Y. Yang, A. Purwar, and M. L. French, “A low voltage SONOS nonvolatile semiconductor memory technology,” *IEEE Trans. Comp. Packag. Manufact. Technol. A*, vol. 20, pp. 190-195, June 1997

[36] J. Bi, “Radiation effects of floating-gate (FG) and charge-trapping (CT) Flash memory technologies,” *2019 International Conference on IC Design and Technology (ICICDT)*, Suzhou, China, Jun. 17-19, 2019, pp. 10.1.1-10.1.3, 2019.

[37] J. S. Bi, Y. N. Xu, G. B. Xu, H. B. Wang, L. Chen and M. Liu, "Total ionization dose effects on charge-trapping memory with $Al_2O_3/HfO_2/Al_2O_3$ trilayer structure," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 200-205, Jan. 2018.

[38] M. Bagatin, et al., "Total ionizing dose effects in 3-D NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 48-53, Jan. 2019.

[39] P. J. McWhorter, S. L. Miller, and T. A. Dellin, "Radiation response of SNOS nonvolatile transistors," *IEEE Trans. Nucl. Sci.*, vol. 33, no. 6, pp. 1413-1419, Dec. 1986.

[40] F. Qiao, et al., "TID radiation response of 3-D vertical GAA SONOS memory cells," *IEEE Trans. Nucl. Sci*., vol. 61, no. 2, pp. 955-960, Apr. 2014.

[41] E. Chatzikyriakou, K. Morgan and C. H. Kees De Groot, "Total ionizing dose hardened and mitigation strategies in deep submicrometer CMOS and beyond," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 808-819, Mar. 2018.

[42] S. Libertino, et al., "Ionizing radiation effects on non volatile read only memory cells," *IEEE Trans. Nucl. Sci*., vol. 59, no. 6, pp. 3016-3020, Dec. 2012.

[43] C. X. Zhang, et al. "Electrical stress and total ionizing dose effects on graphene-based non-volatile memory devices," *IEEE Trans. Nucl. Sci*., vol. 59, no. 6, pp. 2974-2978, Dec. 2012.

[44] H. Puchner, P. Ruths, V. Prabhakar, I. Kouznetsov, and S. Geha, "Impact of total ionizing dose on the data retention of a 65 nm SONOS-based NOR flash," *IEEE Trans. Nucl. Sci*., vol. 61, no. 6, pp. 3005-3009, Dec. 2014.

[45] F. Qiao, et al., "Total ionizing radiation effects of 2-T SONOS for 130 nm/4 Mb NOR flash memory technology," *Sci. China. Inf. Sci*., vol. 57, no. 6, pp. 1-9, Jun. 2014.

[46] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate sensitive linear-bipolar devices," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1706-1730, Jun. 2013.

[47] D. M. Fleetwood, "Radiation-induced charge neutralization and interface-trap buildup in metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 67, no. 1, pp. 580-583, Jan. 1990.

[48] G. X. Duan, et al., "Bias dependence of total ionizing dose effects in SiGe-SiO_2/HfO_2 pMOS FinFETs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2834-2838, Dec. 2014.

[49] D. M. Fleetwood, "Total-ionizing-dose effects, border traps, and 1/f noise in emerging MOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1216-1240, July 2020.

[50] K. Parat and C. Dennison, "A floating gate based 3-D NAND technology with CMOS under array," *2015 International Electron Devices Meeting (IEDM)*, pp. 48–51, Dec. 2015.

[51] M. Itsumi, "Positive and negative charging of thermally grown SiO_2 induced by Fowler-Nordheim emission," *Journal of Applied Physics,* vol. 52, no. 5, pp. 3491-3497, Jan. 1981.

[52] J. Maserjian and N. Zamani, "Behavior of the Si/SiO_2 interface observed by Fowler-Nordheim tunneling," *Journal of Applied Physics,* vol. 53, no. 1, pp. 559-567, Sep. 1982.

[53] I.C. Chen, S. Holland and C. Hu, "Electron-trap generation by recombination of electrons and holes in SiO_2," *J. Appl. Phys*., vol. 61, no. 9, pp. 4544-4548, Jan. 1987

[54] Y. Fukuzumi, et al., “Optimal integration and characteristics of vertical array devices for ultra-high density, bit-cost scalable Flash memory,” *2007 International Electron Devices Meeting (IEDM)*, pp. 449–452, Dec. 2007.

[55] K.T. Park, et al., “Three-dimensional 128 Gb MLC vertical NAND Flash memory with 24-WL stacked layers and 50 MB/s high-speed programming,” *IEEE J. Solid-State Circuits,* vol. 50, no. 1, pp. 204-213, Sep. 2014.

[56] J. Choi and K. S. Seol, “3D approaches for non-volatile memory,” *2011 Symposium on VLSI Technology*, pp. 178–179, Jun. 2011.

[57] E.S. Choi and S.K. Park, “Device considerations for high density and highly reliable 3D NAND Flash cell in near future,” *2012 IEEE International Electron Devices Meeting (IEDM)*, pp. 211–214, Dec. 2012.

[58] J. W. Im, et al., “7.2 A 128Gb 3b/cell V-NAND flash memory with 1Gb/s I/O rate,” *2015 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 130-132, Feb. 2015.

[59] H. Yang, et al., “Reliability issues and models of sub-90nm NAND flash memory cells,” *Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 760-762, Oct. 2006.

[60] A. Chimenton, et al., “New Statistical Data and Modeling of Stress-Induced Leakage Current in 3D-NAND Floating Gate Non-Volatile Flash Memories,” *IEEE Electron Device Letters,* vol. 43, no. 1, pp. 29-31, Dec. 2021.

[61] M. Janai and E. Boaz, "The kinetics of degradation of data retention of post-cycled NROM non-volatile memory products," *2005 IEEE International Reliability Physics Symposium*, pp. 175-180, Apr. 2005.

[62] M. C. Lee and H. Y. Wong, "Investigation on the origin of the anomalous tail bits on nitrided charge trap flash memory," *Microelectronics Reliability*, vol. 55, no. 2, pp. 337-341, Feb. 2015.

[63] S. Aritome, et al., "A novel three-dimensional dual control-gate with surrounding floating-gate (DC-SF) NAND flash cell," *Solid-state electronics*, vol.79, pp. 166-171, Jan. 2013.

[64] D. Resnati, G. Nicosia, G. M. Paolucci, A. Visconti, and C. M. Compagnoni, "Cycling-induced charge trapping/detrapping in Flash memories—Part I: Experimental evidence," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4753-4760, Dec. 2016.

[65] D. Resnati, A. Goda, G. Nicosia, C. Miccoli, A. S. Spinelli, and C. M. Compagnoni, "Temperature effects in NAND Flash memories: A comparison between 2-D and 3-D arrays," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 461-464, Apr. 2017.

[66] G. Nicosia, et al., "Characterization and modeling of temperature effects in 3-D NAND Flash arrays—Part II: Random telegraph noise," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3207–3213, Aug. 2018.

[67] C. J. Yim, et al., "Effect of incorporated nitrogen on the band alignment of ultrathin silicon-oxynitride films as a function of the plasma nitridation conditions," *J. Korean Phys. Soc.*, vol. 58, no. 5, pp. 1169-1173, May 2011.

[68] L. Breuil, et al., “Impact of SiON tunnel layer composition on 3D NAND cell performance,” *Proc. IEEE 11th Int. Memory Workshop (IMW)*, pp. 152-155, May 2019.

[69] S. Bonaldo, et al., “Total-ionizing-dose effects in InGaAs MOSFETs with high-k gate dielectrics and InP substrates,” *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1312-1319, Jul. 2020.

[70] P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, “Correlating the radiation response of MOS capacitors and transistors,” *IEEE Trans. Nucl. Sci.*, vol. 31, no. 6, pp. 1453-1460, Dec. 1984.

[71] L. Breuil, et al., “Passivation of poly-Si channel vertical NAND devices by high pressure annealing,” *Proc. 8th International Memory Workshop (IMW)*, Paris, France, May 15-18, 2016, pp. 88-91.

[72] P. J. McWhorter, S. L. Miller, and T.A. Dellin, “Modeling the memory retention characteristics of silicon-nitride-oxide-silicon nonvolatile transistors in a varying thermal environment,” *J. Appl. Phys.*, vol. 68, no. 4, pp. 1902-1909, Aug. 1990.

[73] Y. Wang and M. H. White, “An analytical retention model for SONOS nonvolatile memory devices in the excess electron state,” *Solid-State Electronics*, vol 49, no. 1, pp. 97-107, Jan. 2005.

[74] D. M. Fleetwood, P. S. Winokur, O. Flament, and J. L. Leray, “Stability of trapped electrons in SiO2,” *Appl. Phys. Lett.*, vol. 74, no. 20, pp. 2969-2971, May 1999.

[75] D. M. Fleetwood, P. S. Winokur, L. C. Riewe, O. Flament, P. Paillet, and J. L. Leray, "The role of electron transport and trapping in MOS total-dose modeling," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1519-1525, Dec. 1999.

[76] T. Kim, D. He, K. Morinville, K. Sarpatwari, B. Millemon, A. Goda, and J. Kessenich, "Tunnel oxide nitridation effect on the evolution of Vt instabilities (RTS/QED) and defect characterization for sub-40-nm flash memory," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 999–1001, Aug. 2011.

[77] S. Chakraborty, P. T. Lai, and P. C. K. Kwok, "MOS characteristics of NO-grown oxynitrides on n-type 6H-SiC," *Microelectron. Reliab.*, vol. 42, no. 3, pp. 455–458, Mar. 2002.

[78] K. Jonghan, et al., "Scaling down of tunnel oxynitride in NAND flash memory: Oxynitride selection and reliabilities," *Proc. 35th IEEE Annu. Rel. Phys. Symp.*, pp. 12–16, Apr. 1997.

[79] H. Fukuda, A. Uchiyama, T. Kuramochi, T. Hayashi, and T. Iwabuchi, "Heavy oxynitridation technology for forming highly reliable flash-type EEPROM tunnel oxide films," *Electron. Lett.*, vol. 28, no. 19, pp. 1781– 1783, Sep. 1992.

[80] G. J. Dunn and P. W. Wyatt, "Reoxidized nitrided oxide for radiation-hardened MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 2161-2168, Dec. 1989.

[81] D. M. Fleetwood and N. S. Saks, "Oxide, interface, and border traps in thermal, N_2O, and N_2O-nitrided oxides," *J. Appl. Phys.*, vol. 79, no. 3, pp. 1583-1594, Feb. 1996.

[82] P. S. Winokur, H. E. Boesch, J. M. McGarrity, and F. B. McLean, "Two-stage process for buildup of radiation-induced interface states," *J. Appl. Phys.*, vol. 50, no. 5, pp. 3492-3494, May 1979.

[83] F. B. McLean, "A framework for understanding radiation-induced interface states in SiO_2 MOS structures," *IEEE Trans. Nucl. Sci.*, vol. 27, no. 6, pp. 1651-1657, Dec. 1980.

[84] P. S. Winokur, F. B. McLean, and H. E. Boesch, Jr., "Physical processes associated with radiation-induced interface states," HDL-TR-2081, https://www.osti.gov/biblio/5585869-physical-processes-associated-radiation-induced-interface-states-technical-report, accessed Jun. 18, 2021.

[85] N. S. Saks, R. B. Klein, and D. L. Griscom, "Formation of interface traps in MOSFETs during annealing following low-temperature irradiation," *IEEE Trans. Nucl. Sci.*, vol. 35, no. 6, pp. 1234–1240, Dec. 1988.

[86] D. M. Fleetwood, "Effects of hydrogen transport and reactions on microelectronics radiation response and reliability," *Microelectron. Reliab.*, vol. 42, no. 4/5, pp. 523-541, Apr./May 2002.

[87] D. Jiang et al. "Impact of critical geometry dimension on channel boosting potential in 3D NAND memory," *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1248-1250, Oct. 2016.

[88] F. Lime, O. Moldovan and B. Iñiguez, "A compact explicit model for long-channel gate-all-around junctionless MOSFETs. Part I: DC characteristics," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3036-3041, Aug. 2014.

[89] G. M. Paolucci, et al., "A semi-analytical model for macaroni MOSFETs with application to vertical Flash memories," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1871-1876, Apr. 2016.

[90] J. Cao, et al., "Total-ionizing-dose effects on polycrystalline-Si channel vertical-charge-trapping NAND devices," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 314-320, Mar. 2022.

[91] M. Bagatin, et al., "Effects of total ionizing dose on the retention of 41-nm NAND flash cells," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2824-2829, Nov. 2011.

[92] E. S. Comfort et al., "Intrinsic tolerance to total ionizing dose radiation in gate-all-around MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4483–4487, Dec. 2013.

[93] M. Gaillardin et al., "Total ionizing dose response of multiple-gate nano-wire field effect transistors," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2061-2068, Aug. 2017.

[94] M. Gorchichko et al., "Total-ionizing-dose response of highly-scaled gate-all-around Si nanowire CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 687-696, May 2021.

[95] M. J. Powell, "Charge trapping instabilities in amorphous silicon-silicon nitride thin film transistors," *Appl. Phys. Lett.*, vol. 43, no. 6, pp. 597-599, Sep. 1983.

[96] M. J. Marinella, "Radiation effects in advanced and emerging nonvolatile memories," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 546-572, May 2021.

[97] K. H. Lee, et al., "Assessment of tunnel oxide and poly-Si channel traps in 3D SONOS memory before and after P/E cycling," *Microelectronic Engineering*, vol. 147, pp. 45-50, Nov. 2015.

[98] D. Jiang, et al., "A study of cycling induced degradation mechanisms in Si nanocrystal memory devices," *Nanotechnology*, vol. 22, no. 25, pp. 254009, May 2011.