RADIATION EFFECTS AND NEGATIVE BIAS-STRESS IN Ge-CHANNEL FinFET & NANOWIRE DEVICES

By

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Alhamdulillah

Dedicating to my loving parents and my lovely wife. Nothing would have been possible without their struggle and continuous support.

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CHAPTER 1

Introduction

Semiconductor devices are the fundamental building blocks of microprocessors. A modern-day microprocessor performs its task using billions of transistors. The continuous scaling of these transistors enhanced the performance of the processors by increasing the transistor density, reducing the cost of microelectronics significantly. This revolution in semiconductor industry is best described by Moore's law [21–24] even in the present days. According to Pat Gelsinger, CEO of Intel Corporation, "Moore's law is alive and well" as shown in Fig. 1.1.

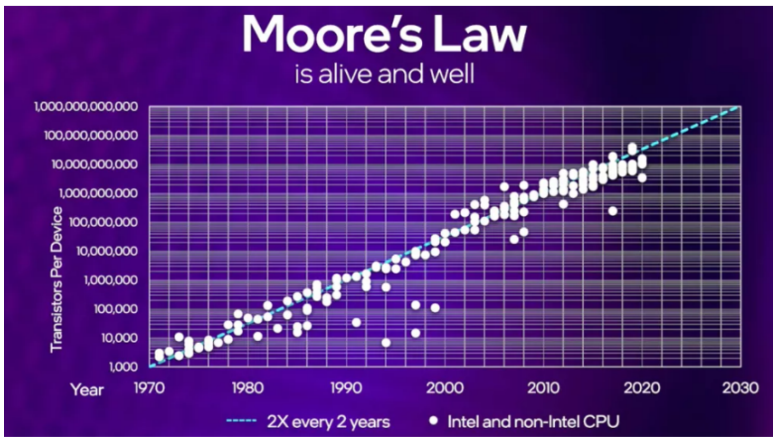

Figure 1.1: Moore's Law is alive and well (Source: Intel Corporation, Oct. 2021)

Following this challenging road map has never been easy as the transistor feature size moves to the nanometer region. Newer semiconductor materials and transistor architectures have been explored to maintain the MOSFET downscaling efforts. Electron and hole mobility [25] was increased by introducing strain engineering in 90 nm technology. Introducing metal-gate/high-k gate stack in 45 the nm node reduced the gate leakage current and poly-silicon depletion [26], [27]. Increasing short channel effects were significantly diminished by introducing FinFET technology in the 22 nm node.

Despite introducing newer materials and significant architectural changes, the miniaturization of semiconductor devices has faltered as research and manufacturing grow ever more expensive. Chip elements are reaching atomic scales, and power consumption problems limit the clock speeds

that keep chip processing steps marching in lockstep. As a result, vertically stacked ribbonFET transistors (Intel corporation, Oct. 2021) and gate-all-around (GAA) nanowire MOSFETs (Fig. 1.2) are introduced to continue progress in performance and power consumption as well as the ability to pack more transistors more densely on a chip. Introduction of GAA provides excellent electrostatic control and reduces gate leakage in 5 nm nodes [2, 28, 29].

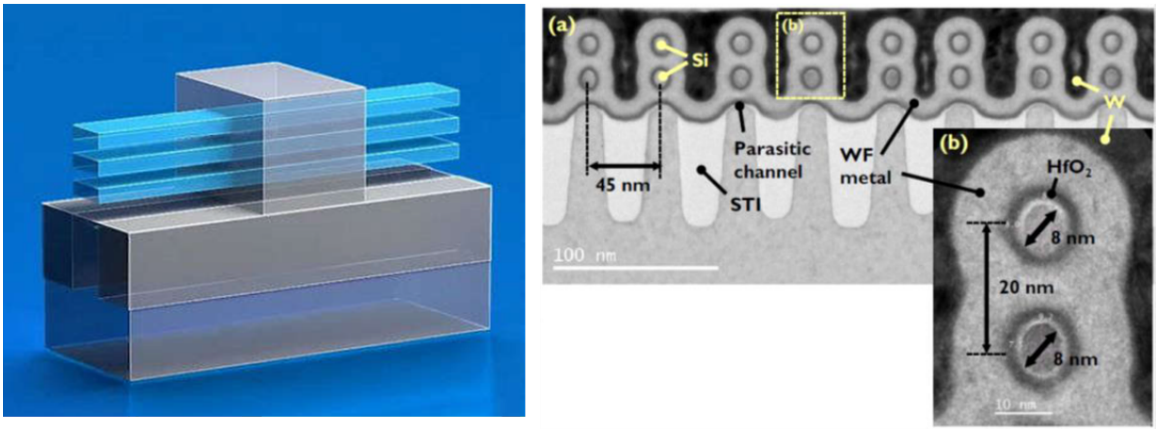

Figure 1.2: Intel RibbonFET transistors are a key part of the chipmaker's recovery plan, Intel news, Oct. 2021, TEM images of an NMOS GAA Si NWFET (LG = 70 nm): (a) overview of the Si NW array, and (b) detailed view of two stacked Si NWs. The rounded NW shape, the narrow NW size distribution, and the con-formally deposited HK/MG layers are visible [2]

1.1 Ge as a channel material in MOS devices

Several challenges exist to incorporate novel materials within the current Si process technology. The device performance will be affected by the ballistic transport mechanism in the channel. As a result, the ultimate carrier speed in the channel will depend on the carrier injection velocity on the source side [30], [31]. It has been shown experimentally that the higher injection velocity can be achieved by using channel material with higher carrier mobility [32].

Various high mobility materials have been explored beyond Si as shown in Fig. 1.3. Among them, germanium (Ge) has been found to exhibit the most balanced hole and electron mobilities with the benefit of simpler process integration in the current Si technology. Unlike other compound semiconductors which are sensitive to their stoichiometry, the mono-atomic nature of germanium also draws attention to the researchers. Besides high mobility, the density of the states also makes germanium more favorable since the density of states in the channel is relevant to determining the channel current as it is directly related to gate capacitance [33]. However, despite the debate of

using Ge only for p-MOSFETs and III–V compounds for n-MOSFETs [34], [35], Ge appears to be the most promising candidate for CMOS technology beyond Si-CMOS scaling. Table 1.1 shows the carrier mobility, effective mass, and energy bandgap in bulk Si, Ge, and typical III–V compound semiconductors. A very high hole mobility in Ge is far ahead of others.

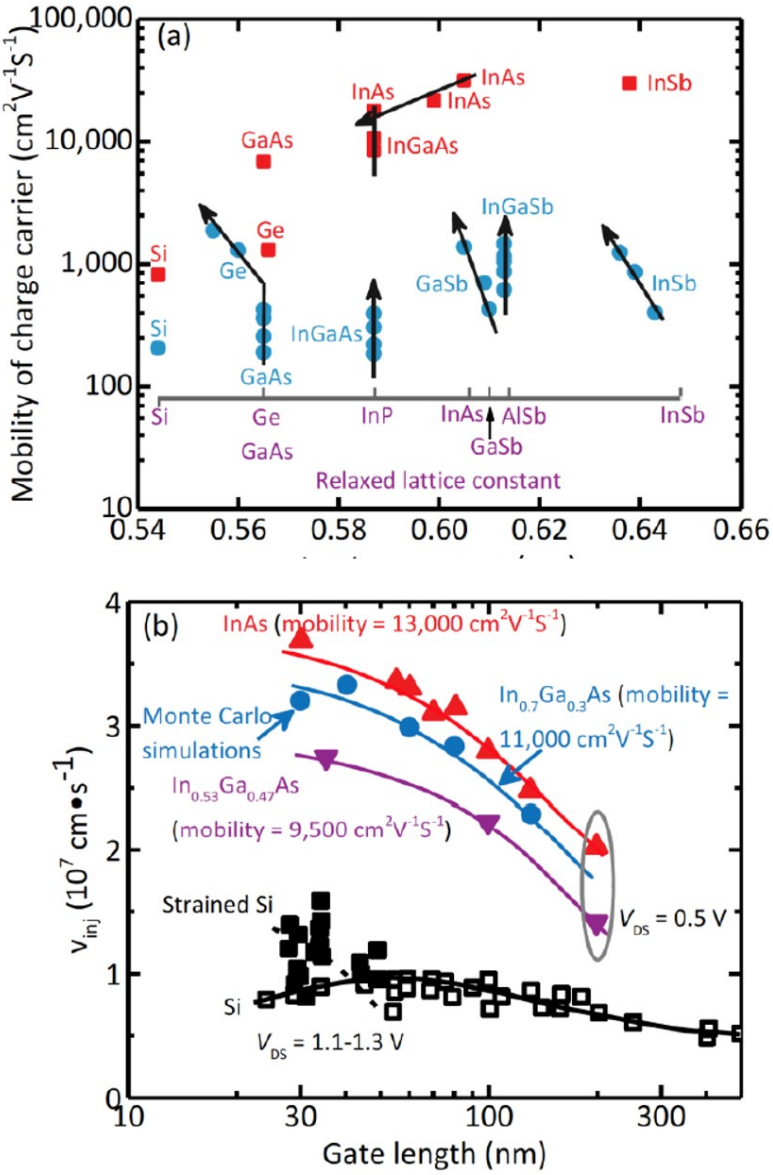

Figure 1.3: (a) Electron and hole mobility of group III-V compound semiconductors. Electron mobility is marked red and hole mobility is in blue. The arrow indicates the increase of biaxial compressive strain. (b) Electron injection velocity in III-V compound semiconductors [3]

Table 1.1: Carrier mobility, effective, mass and energy bandgap in bulk Si, Ge, and typical III–V compound semiconductors. A very high hole mobility in Ge is far ahead of others [1]

	Si	Ge	GaAs	InP	InAs	InSb
Electron mobility ($cm^2 V^{-1} s^{-1}$)	1600	3900	9200	5400	40000	77000
Electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0.916	m_t: 0.082 m_l: 1.467	0.067	0.082	0.023	0.014
Hole mobility ($cm^2 V^{-1} s^{-1}$)	430	1900	400	200	500	850
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
Energy band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17

However, it is important to understand and solve many critical issues that are responsible for the successful and reliable integration of Ge devices. Firstly, the critical inherent properties of Si, such as the Clarke number make it abundant on earth and the energy bandgap makes the operation temperature range wider. Likewise, Ge is not a rare material if it is not used for all purposes. On the other hand, a smaller bandgap in Ge compared to Si provides a higher junction leakage current at room temperature which is a big concern for any MOS device. Secondly, the crystal purity of Ge is not more than that of Si crystal. This factor is related to the defect control of the channel material and the crystal purity is improving with the evolution of recent technology. Thirdly, the wafer size of Ge is not a concern since Si is being used as the bottom substrate and single-crystalline Si is produced on an industrial scale. Last but still the most serious challenge in the Ge fabrication process is to control the hetero-interfaces of GeO_2/Ge for high-performance devices as shown in Fig. 1.4.

The GeO_2/Ge gate stack is not as stable as SiO_2/Si [36] because of significant GeO desorption from GeO_2/Ge [4], [37] as shown in Fig. 1.4. Thus, Ge gate stack and passivation challenges need to be overcome when Ge is considered as an alternative channel material. Several efforts [5], [6] have been carried out to improve the performance of the Ge gate stack by using an epitaxially grown thin Si-cap, mainly using a SiO_2/Si/Ge stack. This method facilitates the use of existing Si process technology without having the reaction at GeO_2/Ge suppressed as shown in Fig. 1.5.

After the discovery of Ge in 1886 [38], the first transistor and the integrated circuits (ICs) on Ge have been demonstrated in 1947 and 1958, respectively [39]. Despite the long history of Ge as an electron device, it has been widely used only for radiation spectrometers and IR detectors. Nowadays, researchers are investigating the challenges involved in Ge channel devices for space

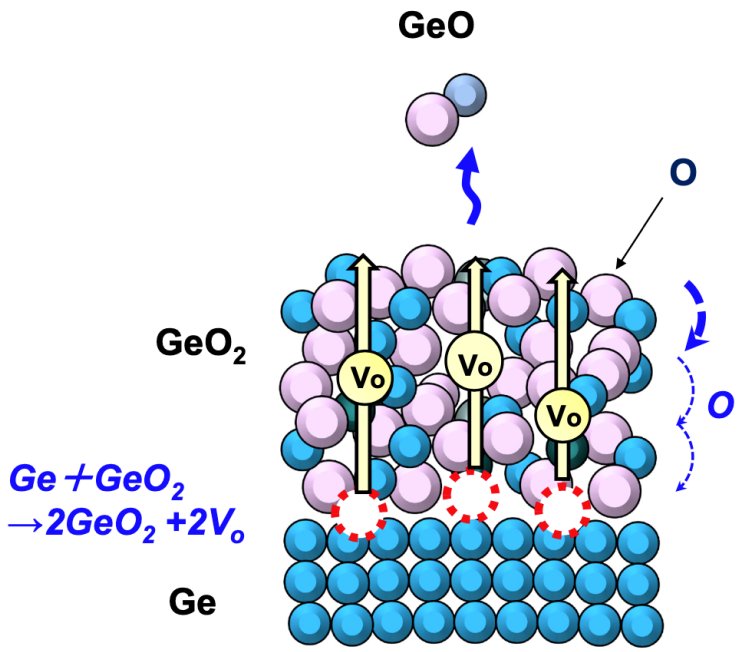

Figure 1.4: A kinetic model proposed for the GeO desorption. For understanding the above experimental results, it is most probable that V_o diffusion from the $GeO_2 = Ge$ interface triggers GeO desorption at the top surface [4]

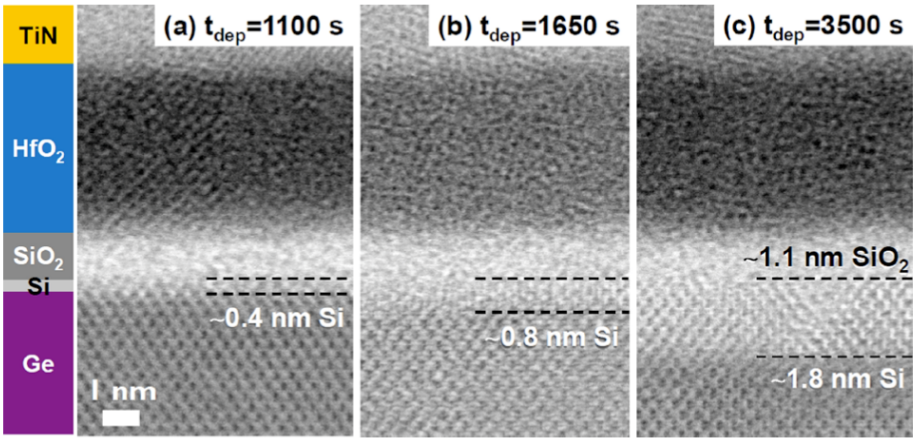

Figure 1.5: Cross-sectional TEM images of Si-passivated Ge gate stacks made using various Si deposition [5], [6]. A very thin Si layer epitaxially grown on Ge is observed.

applications, based on present understandings of device physics and technological development. Fig. 1.6 shows the electronic band diagram and the electron configuration of Ge. It is important to notice that the direct bandgap in Ge at the Γ-point is significantly lower than in Si, which is very important for optical applications of Ge [4]. Table 1.2 shows the typical material properties of Ge

and Si. All of the properties listed in this table in addition to carrier mobility should be considered for designing real electron devices.

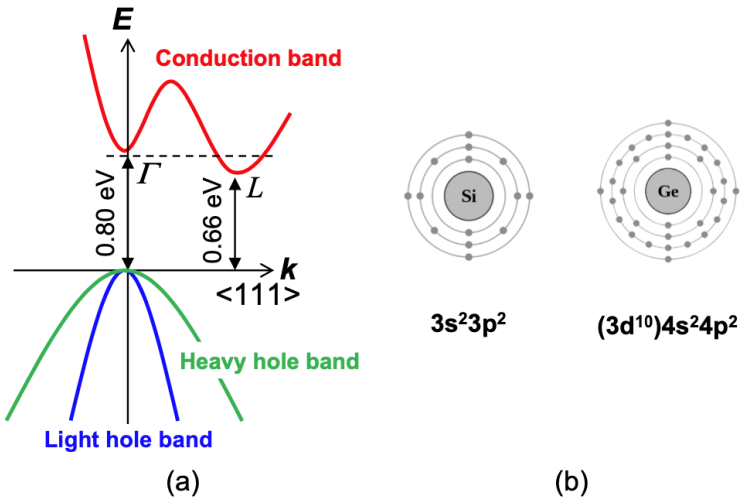

Figure 1.6: Electronic structure of Ge. The conduction band minimum is located at L-point with an indirect energy bandgap of 0.66 eV. The direct energy bandgap at the Γ-point is about 0.80 eV, which is rather close to the indirect one. This is in striking contrast to the Si case. (b) Schematic electron configurations of Si and Ge atoms. The 4s state of Ge is rather deep compared with the 3s state of Si because of the insufficient screening by 3d electrons [1].

Table 1.2: Typical material properties of Ge and Si. All of this listed in this table in addition to carrier mobility should be considered for designing real electron devices [1]

	Ge	Si
Density (g/cm^3)	5.327	2.328
Young's modulus (N/m^2) $\langle 100 \rangle$ direction	1.3×10^{11}	1×10^{11}
Thermal conductivity ($W\,cm^{-1}\,K^{-1}$) at 300 K	0.6	1.5
Dielectric constant	16.0	11.9
Refractive index at 633 nm	5.48	3.88
Lattice constant (Å)	5.64613	5.43095
Clarke number (%)	0.00065	25.8

As technology scales down and the material/architecture of the devices changes, the reliability of microelectronics becomes one of the most important issues. Moreover, the semiconductor devices or ICs used in space applications need to withstand radiation exposure, changing the device behavior

in an unexpected way. The objective of this work is to explore two broad categories of radiation effects; total ionizing dose (TID) and single event effects (SEE) in Ge channel devices. In addition to that, negative bias-stress in Ge channel devices have also been explored.

Chapter-II describes the background of this work. The development of highly scaled advanced semiconductor devices necessitates an extensive study of radiation effects in Ge-channel FinFET and GAA nanowire devices. The future scope of Ge as a channel material has been discussed at the beginning of this section. Then, the background of radiation effects (SEE & TID) and negative bias-stress in modern semiconductor devices are discussed. A detailed literature review of previous work on SEE, TID, and negative bias-stress in MOS devices is also included in this section.

Chapter-III presents the Single-Event-Induced Charge Collection in Ge-Channel pMOS FinFETs. Peak transient currents due to pulsed-laser or heavy-ion irradiation of Ge pMOS FinFETs are nearly independent of gate bias. This is because the prompt photocurrent is due primarily to a transient source-drain shunt. In contrast, longer-term diffusion charge collection is strongly gate-bias dependent. This bias dependence results from hole injection from the source in response to the transient increase in electron concentration in the channel. The transients measured at the source terminal change polarity when the strike location moves from source to drain, but this effect does not occur for the transients measured at the drain terminal. Charge collection mechanisms are studied using TCAD simulations.

Chapter-IV reports on Geant4-based Monte Carlo simulation results of the interaction of high energy protons with various target materials used in Ge channel pFinFET devices. Our results demonstrate that maximum Linear Energy Transfer (LET) values of the order of 23 $\mathrm{MeVcm_2}/mg$may need to be accounted for in heavy-ion testing of Ge channel devices. The presence of high-Z materials (such as tungsten) in interconnects extends the maximum Linear Energy Transfer (LET) values to approximately 40. Moreover, the relative impact of recoil ions on charge deposition is also calculated and described in this chapter.

Chapter-V illustrates the negative bias-stress and total-ionizing-dose (TID) effects in deeply scaled Ge-GAA nanowire devices, which are characterized for different biasing conditions. negative bias-stress-induced degradation in Ge GAA device originates primarily from the interface- and border-trap generation. Devices stressed at high gate voltage show rapid initial degradation and quick saturation dominated by interface-trap generation. Radiation-induced off-state leakage cur-

rent in Ge GAA nanowires increases with dose due to enhanced band-to-band tunneling caused by charge trapping in the shallow trench isolation (STI).

Chapter-VI summarizes the conclusions of the dissertation.

CHAPTER 2

Background

2.1 Radiation Environment

The effects of the radiation environment on semiconductor devices and the resultant damages can be divided into ionization effects and displacement damages. The ionization effects include the effects caused by a single ionizing particle defined as Single Event Effects (SEE) or Total Ionizing Dose (TID) effects from charges deposited by accumulated dose over time. On the other hand, Displacement Damage (DD) is non-ionizing which is caused by a particle targeting the semiconductor lattice. The main sources of energetic particles in space environments are particles trapped in the Earth's radiation belts and cosmic rays. The particle distributions in Earth's radiation belt are illustrated in Fig. 2.1 [7]. The cosmic rays, which include the galactic cosmic rays and the solar cosmic rays contain protons and heavy ions. However, the galactic cosmic rays consist mostly of alpha particles and protons. Fig. 2.2 shows the distribution of the elements in galactic cosmic rays [8]. A similar distribution is also observed in solar cosmic rays [8].

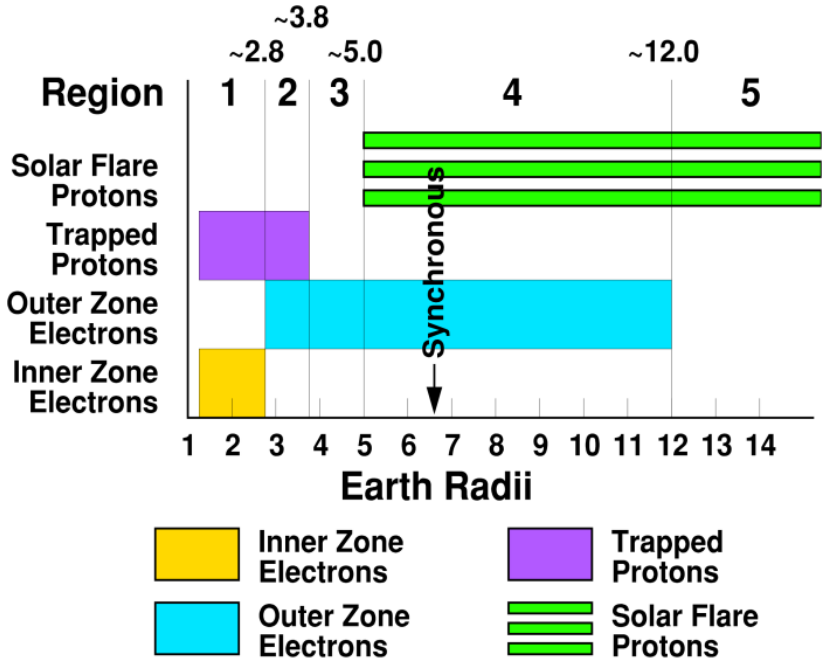

Figure 2.1: The charged particles trapped by Earth's magnetosphere [7]

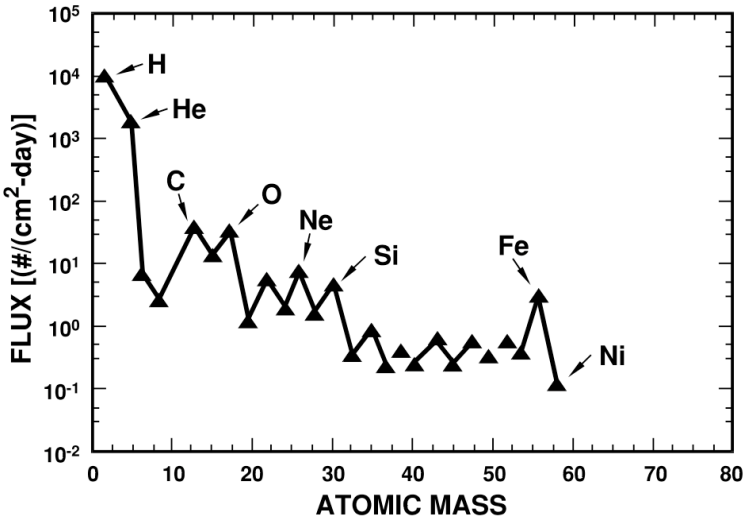

Figure 2.2: Relative abundance of the elements from hydrogen to the iron group [8]

The cosmic rays interact with nitrogen and oxygen atoms in the Earth's atmosphere and shower a lot of secondary particles including electrons, protons, heavy-ions, neutrons, muons, and pions [40], among which neutrons can affect avionics through nuclear interactions and induce SEEs. The neutron-induced SEE is a strong function of altitude and latitude [41].

2.2 Single-Event Effects in Semiconductor Devices

Single Event Effects (SEEs) are one of the most important radiation effects that need to be considered for modern technology nodes. When a highly energetic particle (e.g., neutrons, protons, alpha particles, or other heavy ions) strike sensitive regions of a microelectronic circuit [42], it may cause nondestructive single-event-induced effects such as single-event transients (SET), single-event upset (SEU), or potential destructive effects such as single-event latch-up (SEL). The physical origin of SEE comes from the charge deposition and collection mechanism.

2.2.1 Charged carriers generation and deposition

The charge deposition occurs when an energetic particle passes through a semiconductor material and loses energy through a different scattering processes. The energy loss liberates excess electron-hole pairs throughout the ion track length in the target material. The electron-hole pairs are generated via different mechanisms.

The Rutherford or coulomb scattering characterizes the interaction of incident particles (protons,

ions or, electrons) with free electrons in the conduction band and bound electrons in the lattice, producing electron-hole pairs by Coulomb attraction and/or repulsion. Direct ionization produces a free carriers along its track by the incident particles with energies lower than 100 keV. When the particle energies are higher than 10 MeV [43], [44], the ion-nuclei interactions dominate the energy deposition and charge creation. Energetic particles are more likely to interact with an atomic nucleus and deposit energy through elastic and inelastic scattering mechanisms.

An elastic collision can displace an atom from its original position by transferring kinetic energy, resulting in secondary isotopes of the mother atom. The recoiled isotopes act as a heavy-ion in the lattice and further generate electron-hole pairs through ionization. Moreover, the relocated atom's vacancy generates displacement damage by modifying the local lattice potential. The displaced atom can also transfer the received energy to the lattice in the form of phonons (heat). On the other hand, the in-elastic process is a nuclear reaction that occurs when an energetic ($\geq$ 50 MeV) particle interacts with the nucleons of the target atom [45]. As a result, wide ranges of secondary recoils are generated that further deposit energy and ionize neighboring atoms, producing electron-hole pairs.

Generally, the loss of energy is defined by linear energy transfer (LET) [12] as

$$LET = \frac{1}{\rho}\frac{dE}{dx} \qquad MeV.cm^2/mg \tag{2.1}$$

Where, ρ is the density of the target material. In silicon, a LET of 100 MeV.cm2/mg corresponds to a charge deposition of 1 pC/μm. The distance traveled by an incident particle is defined as the range of the particle and it entirely depends on the initial kinetic energy, atomic number of the particle, and the density of the target materials. Some of the incident particles and generated secondary recoils travel through the target material when the range of ions is larger. When the penetration depth of the incident particles is smaller than the target materials, the incident particle eventually loses all of its energy. The maximum energy loss per unit distance occurs at the Bragg peak [46], immediately before the particle stops.

There is another efficient way of generating electron-hole pairs in semiconductor materials through the absorption of photons. Generally, single photon absorption (SPA) occurs when the photon energy is above the semiconductor bandgap [47], or two-photon absorption occurs when the photon energy is sub-band [48]. Fig. 2.4 depicts the SPA process of exciting an electron from the

valence band and leaving behind a hole.

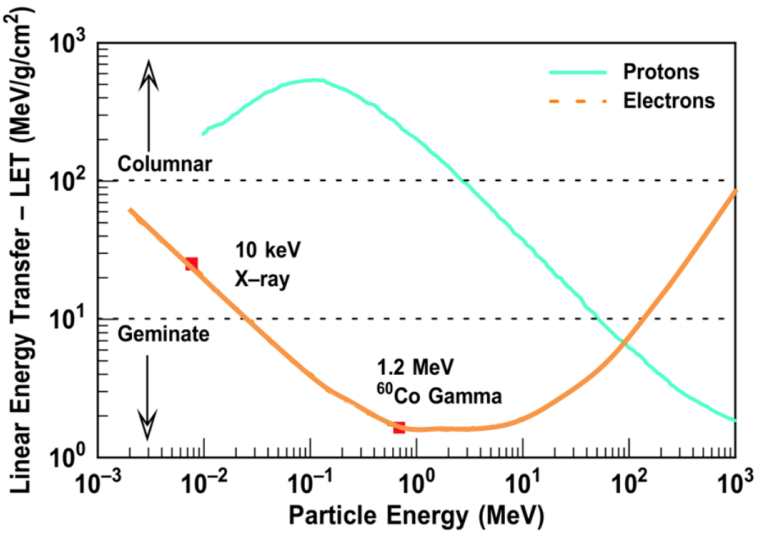

Figure 2.3: LET in SiO_2 versus particle energy for electrons and protons, and secondary electrons generated by 10-keV X-rays and 1.25-MeV Co-60 gamma rays [9]

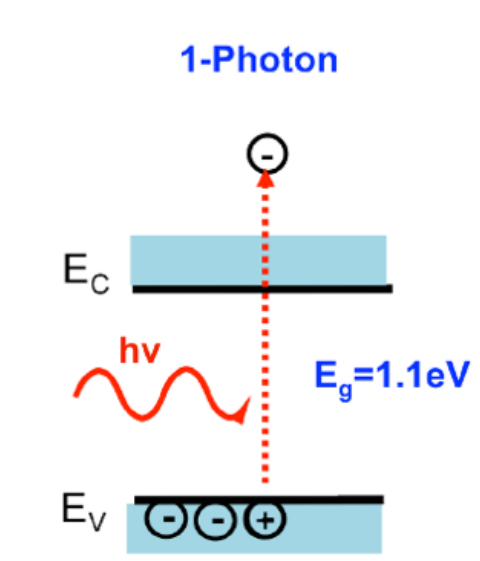

Figure 2.4: Energy band diagram for silicon illustrating the single photon absorption. hν is the energy of the incident photon.

Each photon is absorbed to create a single electron-hole pair, hence the SPA nomenclature. This process of photon absorption is ruled by Beer's law [10] which explains that the intensity of light passing through a material decreases exponentially with distance into the material at a rate determined by the linear absorption coefficient. Thus, the charge generation through the SPA

process is well characterized for a precise location at a specific time.

$$I(z) = I_0 exp(-\alpha z) \tag{2.2}$$

Where I_0 is the intensity of the incident beam, α is the linear absorption coefficient of the target material., and z is the laser penetration depth. the equation explains an exponential decrease in the beam intensity as it propagates through the target material.

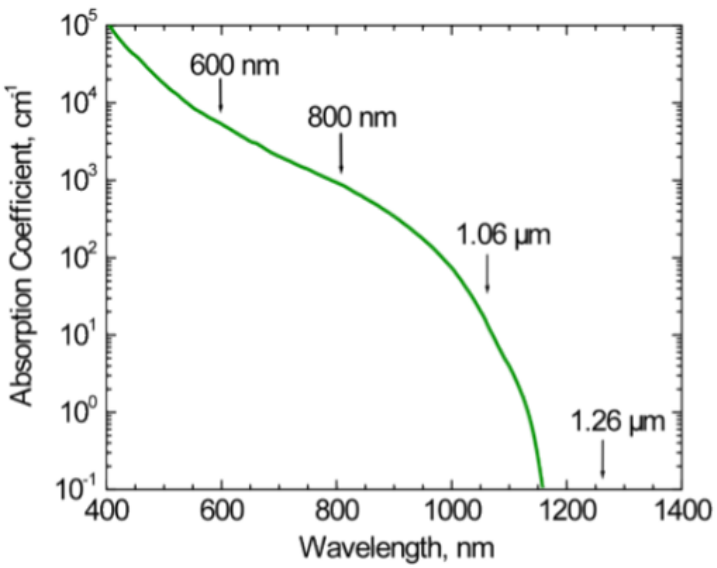

Figure 2.5: Absorption coefficient as a function of the wavelength for silicon [10]

The absorption coefficient as a function of wavelength for silicon is illustrated in Fig. 2.5. There is an inverse relationship between the absorption coefficient of the laser through a material and the penetration depth ($\alpha = 1/e$). α is the penetration depth at which the intensity decreases to $1/e$ [49]. Thus, the penetration depth in silicon can be varied up to 10 μm by choosing the wavelength of the light [10]. In contrast to ions, laser pulses cannot pass through metal layers. This is why the semiconductor devices are usually irradiated with laser pulses from the backside to avoid reflections from top metal layers. The sensitive region is typically located near the channel region which is hundreds of μm from the substrate. Therefore, the thick substrate modulates the amount of incident light and the amount of charge collected by the device, producing a serious absorption problem in the SPA process. As indicated in Fig. 2.5, there is a very low absorption in the sub-band region. However, the laser pulses with sufficiently high intensities can penetrate thick layers and

deposit two-photons simultaneously to generate a single electron-hole pair.

In TPA, a very high photon density is required and carrier generation is quadratic with laser irradiance [50]. As a result, TPA-induced charges are bound to a limited region [50], [51]. Therefore, 3-D mapping of SEE charge generation is possible using the TPA process. The light propagation in a material is governed according to the equation [10],

$$\frac{dI(z)}{dz} = -\alpha I(z) - \beta I^2(z) \tag{2.3}$$

where $I(z)$ is the laser intensity propagating in the material, α is the single-photon absorption coefficient and β is the two-photon absorption coefficient (cm-s/Joule). This equation describes two distinct regimes of absorption, the linear regime for single-photon absorption and the nonlinear regime for two-photon absorption. The nonlinear photon absorption requires α to be very small which corresponds to a wavelength longer than 1.2 μm according to Fig. 2.5. A wavelength of 1.2 μm corresponds to a photon energy of 1 eV, smaller than the Si bandgap. Therefore, two-photons are required to generate one electron-hole pair, hence the nomenclature of two-photon absorption (TPA).

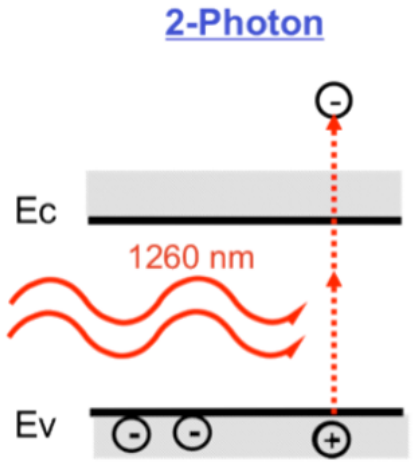

Figure 2.6: Energy band diagram for silicon illustrating the two-photon absorption

Fig. 2.6 illustrates the two-photon absorption mechanism with each photons having a wavelength of 1260 nm. With sufficient intensities, two-photons are absorbed to excite an electron form the valence band to the conduction. The carrier generation equation highlights the influence of

intensity on the two-photon absorption process [10],

$$\frac{dN(z)}{dt} = \frac{\alpha I(z)}{h\nu} + \frac{\beta I^2(z)}{2h\nu} \tag{2.4}$$

Where N(z) is the density of free carrier , h is the Plank's constant and ν is the photon frequency (c/λ). Since the Ge has bandgap (0.67 eV) lower than that of photon energy corresponding to a wavelength of 1260 nm(0.98 eV), the charge generation in Ge by TPA is not well-characterized [52].

2.2.2 Charge collection mechanism

When an energetic particle strikes an electronic component, it ionizes the lattice atoms and generates excess electron-hole pairs. The transport of the generated carriers is described by the drift diffusion process. As a result, the charged carriers move towards a sensitive node [11] (reverse-biased p-n junction, drain of a MOS device) and collected to produce a transient current. Fig. 2.7 illustrates the charge generation and collection places in a reverse-biased junction [11]. Sometimes, the charge collection can be enhanced by the field funneling process if the electric field in the reversed biased depletion region is disturbed [53] as shown in Fig. 2.8.

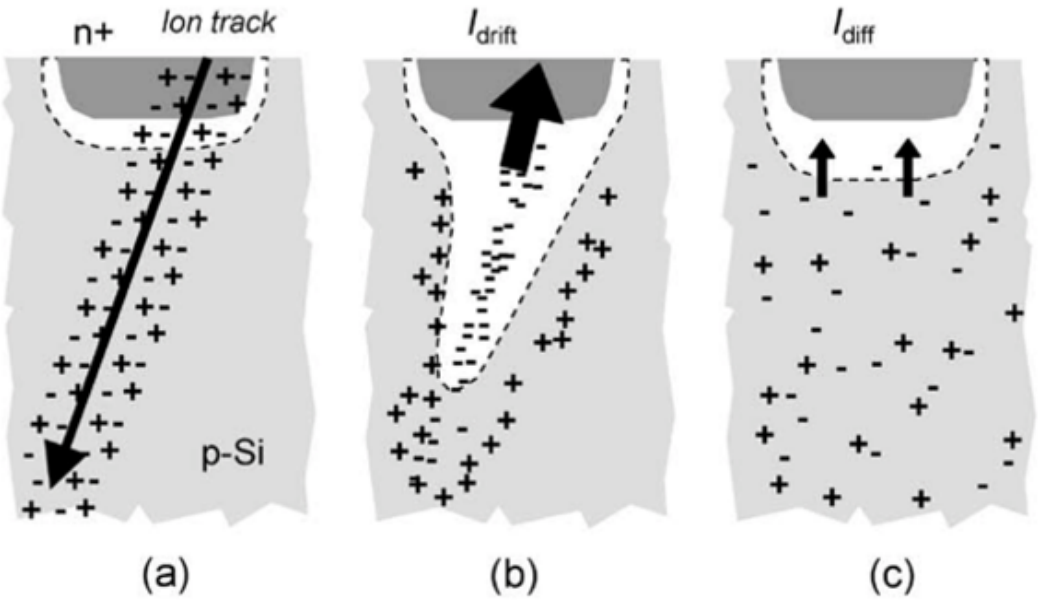

Figure 2.7: Charge generation and collection phases in a reverse-biased junction [11]

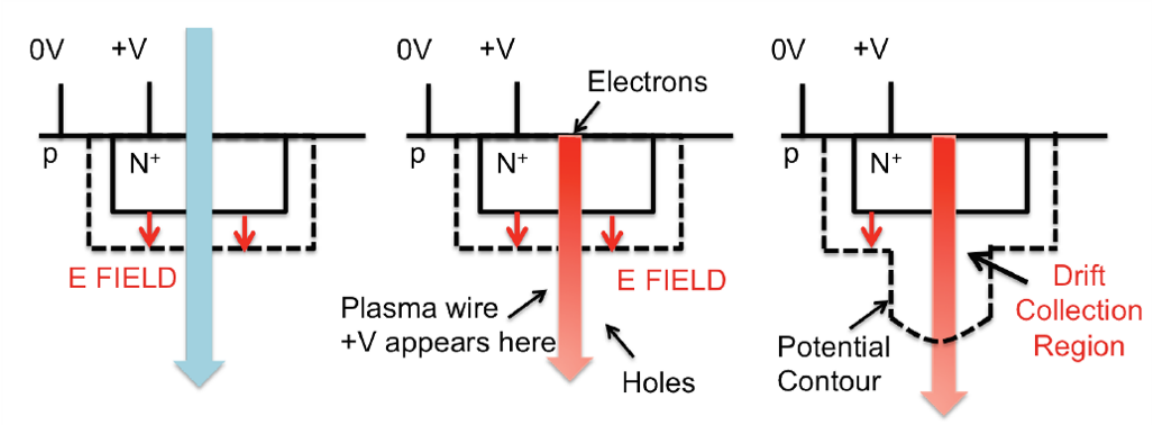

Figure 2.8: Progress of funneling from the plasma track creation (on the left) to the funnel build up (on the right) [12]

The funneling effect extends the sensitive region deep into the substrate and allows more charge collection. The transient current has a fast component resulting from the drift collection from the depletion layer and filed funnel region and secondly, a slow component resulting from the diffusion process. Recombination of electrons and holes also occurs at the same time through Shockley Read Hall recombination (SRH) or Auger recombination when the electron-hole pair density is high. Fig. 2.9 illustrates a short-term charge collection process dominated by drift, which contributes to the peak transient current and a relatively slow process dominated by diffusion, which contributes to the tail.

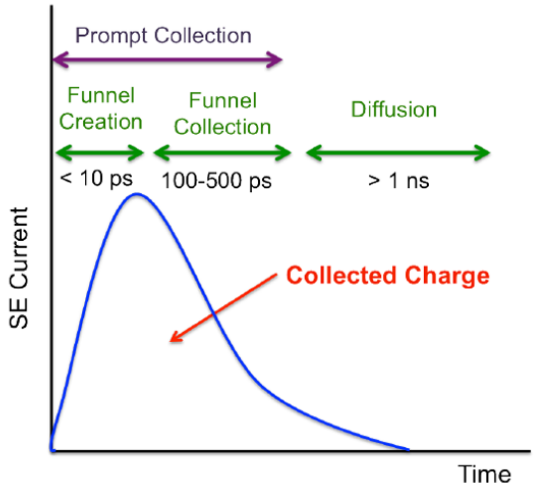

Figure 2.9: Shape of a representative single event pulse measured at a struck p-n junction [12]

2.2.3 Shunt effects

As technology scales down, multiple junctions in a semiconductor device can be disturbed by energetic particles or photons, and the high density of generated carriers can create a transient and highly conductive path that connects two adjacent junctions. This phenomenon is defined as a single-event-induced shunt effect [13]. The energetic ion track perturbs and penetrates into both junctions, forming a highly conductive ohmic-like region. As a result, the junction charge collection cannot be treated independently. In advanced semiconductor devices the shunt effect will create a lateral conductive path along the channel from source to drain, causing transient current [54–61]. Fig. 2.10 depicts an ion track shunt effect in a multi-layer structure.

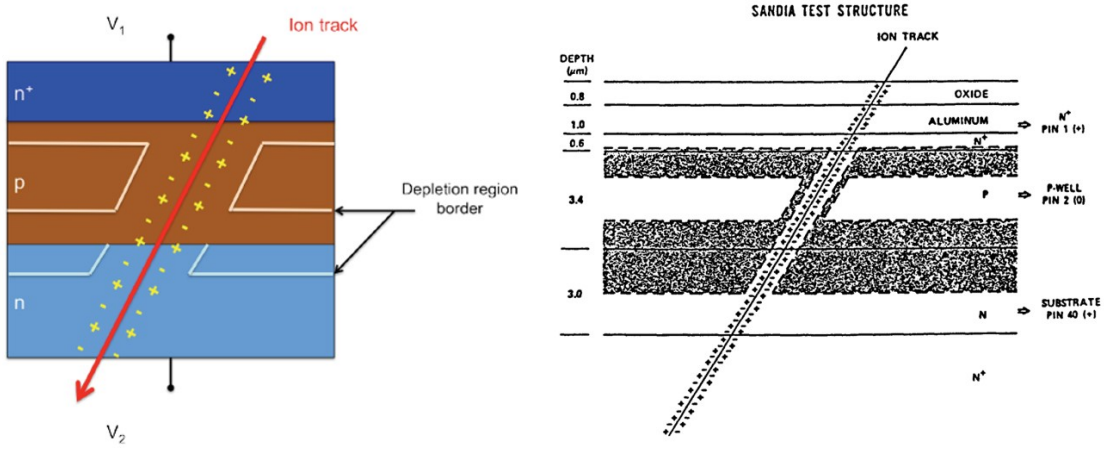

Figure 2.10: Diagram of a multi-layer structure exhibiting shunt effect [13], [12] and an illustration of ion track shunt effect in two-junction experimental structure [13]

2.2.4 Bipolar amplification effect

Single event induced charge collection enhancement through bipolar amplification effect have been explored a significant number of studies [58], [59], [14, 62–68]. A high density of electron-hole pair is created along the ion track during a heavy ion strike. Because of the lighter effective mass, electrons are swept away immediately after the generation. On the other hand, holes remain in the active region because of their larger effective mass and get accumulated near the reverse biased source-body junction. As a result, the source-body barrier gets reduced and forces the source to eject electrons into the body, and collect them by the drain terminal. This mechanism is similar to the forward active mode operation of bipolar transistors. This enhanced charge collection mechanism

is known as the bipolar amplification effect, which allows more charges to be collected than was generated. The bipolar amplification process dominates the charge collection mechanism as long as the excess hole density is present. The charge collection enhancement mechanism ins GaAs is illustrated in Fig. 2.11. [14].

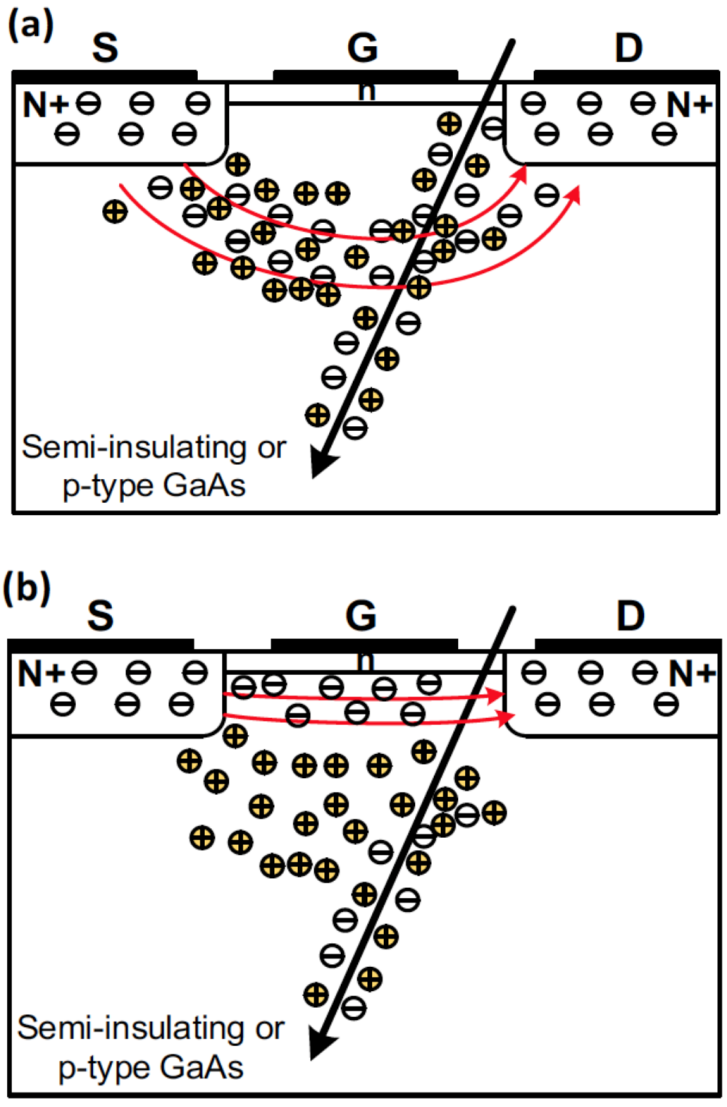

Figure 2.11: Schematic diagram illustrating (a) the bipolar gain and (b) channel-modulation charge enhancement mechanisms that contribute to the charge collection processes of GaAs FETs [14].

2.3 Total Ionizing Dose (TID) effects in MOS devices

Total Ionizing Dose (TID) effects is referred to as parametric degradation and possible functional failures in electronic devices caused by the cumulative process of energy deposition and

charge generation by incident ionizing radiation [15]. In general, the oxide layers are the most sensitive parts in MOS systems. When a MOS device is exposed to a radiation environment, the incident energetic particle generates electron-hole pairs caused by the deposition of energy in the oxide layer of the device. Under the influence of an electric field these excess electrons and holes will immediately drift in opposite directions, the electron in the direction of higher potential and holes in the direction of lower potential. The highly mobile electrons are swept out of the oxide immediately (within picosecond) after the generation. On the other hand, the transportation of holes is much slower than the electrons and they get trapped in the microstructural defects and pre-existing traps in the oxide. However, a fraction of electrons will recombine with holes before leaving the oxide which is defined as initial recombination [15]. The number of holes escaping the initial recombination known as charge yield drift towards the oxide interface. This charge yield is a strong function of the electric field present in the oxide and the energy of the incident particle as shown in Fig. 2.12.

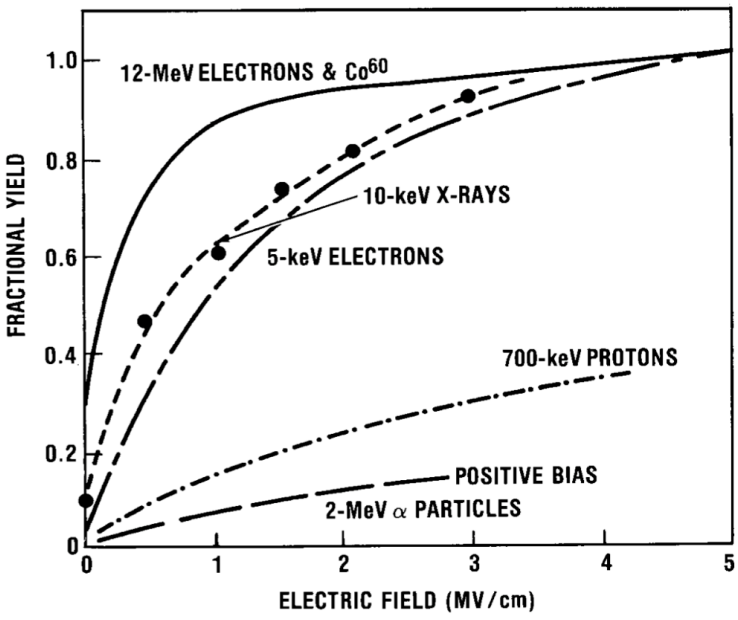

Figure 2.12: Charge yield as a function of electric field present in the oxide and the energy of the incident particle [15].

The unrecombined holes will further transport towards the oxide/semiconductor interface through the polaron hopping process between localized states in the oxide [69]. This hopping process typically takes less than a second but also may take decades [70]. As the holes travel near the Si/SiO_2

interface, some of the holes are trapped in the oxygen vacancies, forming positive oxide traps. These trapped charges can modulate the inversion layer of a MOS device and cause a shift to the threshold voltage and an increase in radiation-induced leakage current. These oxides trapped charges are generally neutralized with time through electron tunneling and thermal emission. Fig. 2.13 shows the major physical processes underlying radiation response that happens in MOS systems following ionizing radiation [71].

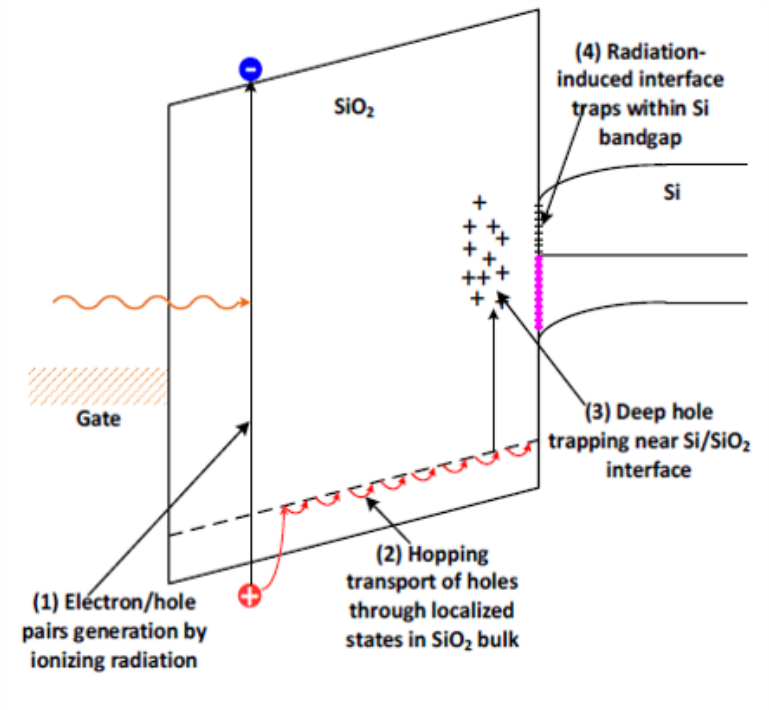

Figure 2.13: Schematic energy band diagram for MOS structure under positive bias, indicating major physical processes underlying radiation response. After [15]

Furthermore, the hole transport through SiO_2 via the hopping process causes an energy exchange in the oxide lattice, resulting from the release of hydrogen ions (protons). These protons travel towards the interface in the presence of an electric field and react with Si-H to form H2, leaving behind a silicon dangling bond at the interface. As a result, these dangling bonds act as interface traps localized in the Si bandgap. Their occupancy is determined by the Fermi level, resulting in a change in threshold voltage and mobility degradation. The near interfacial oxide traps are called the border traps [72]. Since it is difficult to identify border traps separately, the defect sites within 3 nm of Si/SiO_2 interface are considered as border traps [71].

The TID effect due to accumulated charge causes three primary changes in MOS device per-

formance: threshold voltage shift, transconductance degradation, and increase in leakage current. Typically, the voltage shift results from both the oxide trap charge and interface trap charge. In modern MOS devices, a positive oxide trap charge will have a negative threshold voltage shift in both n- and p- channel MOS devices. On the other hand, the positive interface trap charges cause a negative threshold shift in PMOS devices, and the negative interface traps in NMOS devices to cause a positive threshold voltage shift. Therefore, the effect of TID-induced oxide and interface trap charge compensate threshold shift in NMOS and add up together in PMOS devices. The relationship is given by:

$$\Delta V_{TH} = -\frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{x_0} x \,.\rho_{ox}(x)\, dx \tag{2.5}$$

where Q_i is the interface charge, ρ_{ox} is the volume charge density, x_0 is the oxide thickness and ε_{ox} is the oxide dielectric constant.

For relatively thick oxides, the threshold-voltage shift caused by trapped holes in the oxide can be defined by:

$$\Delta V_{ot} \propto x_0^2 \tag{2.6}$$

Equation 1.6 suggests that the TID effects due to oxide/interface trap charges are becoming less significant for advanced technology nodes with the continuing CMOS scaling. The ultra-thin gate oxide layer thickness is now approximately 1 nm, which is too thin to trap charges and cause noticeable TID effects. Contrarily, the thick oxide regions in CMOS devices such as the buried oxide in the silicon-on-insulator (SOI) and the shallow trench isolation (STI) are increasingly causing reliability problems, for example, leakage current increases [73].

2.4 Negative Bias Temperature Instabilities in MOS devices

Negative Bias-temperature Instabilities occurs when a negative bias is applied to the gate terminal at elevated temperatures. It degrades the device performance by creating an oxide trap charge and interface traps at the Si/oxide interface. Despite the advantages of FinFET and GAA devices, the novel architecture introduces new reliability concerns. Such as, multi-gate devices are more susceptible to NBTI than planar devices due to the higher number of Si-H bonds at the interfaces.

Incorporating a high-κ gate stack and new channel material also affects the interface quality; changing the response to NBTI induced degradation. However, a number of models have been proposed to explain the NBTI mechanism.

2.4.1 Reaction-Diffusion model

NBTI has often been considered as a form of reaction-diffusion (RD) model, as proposed by Jeppson and Svensson [74]. The RD model infers that the Si-H bond at the semiconductor/oxide interface is separated at higher temperature and electric field, allowing some hydrogen species to be released from passivated interface defects and diffused into the oxide.

Another RD model proposed by L. Tsetseris et al. [75], considers the dopant depassivation from silicon and subsequent movement of hydrogen species to the interface as the origin of NBTI. According to first-principles calculation, a direct depassivation reaction is possible,

$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si\bullet + H_2$,

where $Si_3 \equiv SiH$ is a hydrogen-passivated interface trap and $Si_3 \equiv Si\bullet$ is an interface trap with the dot is the representation of the dangling bond. It is assumed that the hydrogen released from P-H bonds because of the depletion region biasing condition in n-type Si surface at elevated temperature. Hols get trapped and subsequently create positively charged (H^+). As a result, negative bias drives the H^+ towards the interface and subsequently accelerates the reaction with the Si-H bond to form H_2, leaving behind a positively charged Si dangling bond (or Pb center). Eventually, the H_2 diffuses from the interface into the oxide.

However, it has been found by the recent researchers [76], [77] that the interface trap creation is not the only reason for NBTI induced degradation. A major hole trapping also occurs when the electric field at the gate oxide approaches or exceeds 10 MeV/cm. Moreover, a large number of studies [77], [78] investigated the recovery of NBTI, published in the last decade does not fully get convinced by the reaction-diffusion model.

2.4.2 Two-stage model

Tibor Grasser et al. [16], developed and proposed a comprehensive quantitative two-stage model in 2009, inferring that the NBTI degradation is due primarily to interface trap creation and/or oxide charge buildup. it is assumed that the degradation proceeds in two coupled stages. The NBTI

induced degradation process is initiated (stage 1) when an E' precursor site, e.g., a neutral oxygen vacancy captures an inversion layer hole. The hole capture results in a positively charged E' centers (paramagnetic defects observable with ESR) in the oxide layer, thereby creating a switching trap, as illustrated in Fig. 2.14. As a result of a the Si–Si bond break, positively charged E'$_\gamma$ center is created (state 2). After that, electron capture (hole emission) neutralizes the positively charged E'$_\gamma$ center (state 3). Now it can fall back to state 2 by capturing a hole again or the structure can return back to its initial equilibrium configuration (state 1). In the second stage, oxide silicon dangling bonds (E' centers) created in the stage one process exchange hydrogen with a P_b center at the interface and trigger the creation of P_b centers.It has been further confirmed that E' centers recover very quickly upon removal of the stress [79]. During zero oxide bias at elevated temperature or negative oxide bias at room temperature the E' defect density does not change, further supporting hole capture at an E' precursor site and the creation of interface traps.

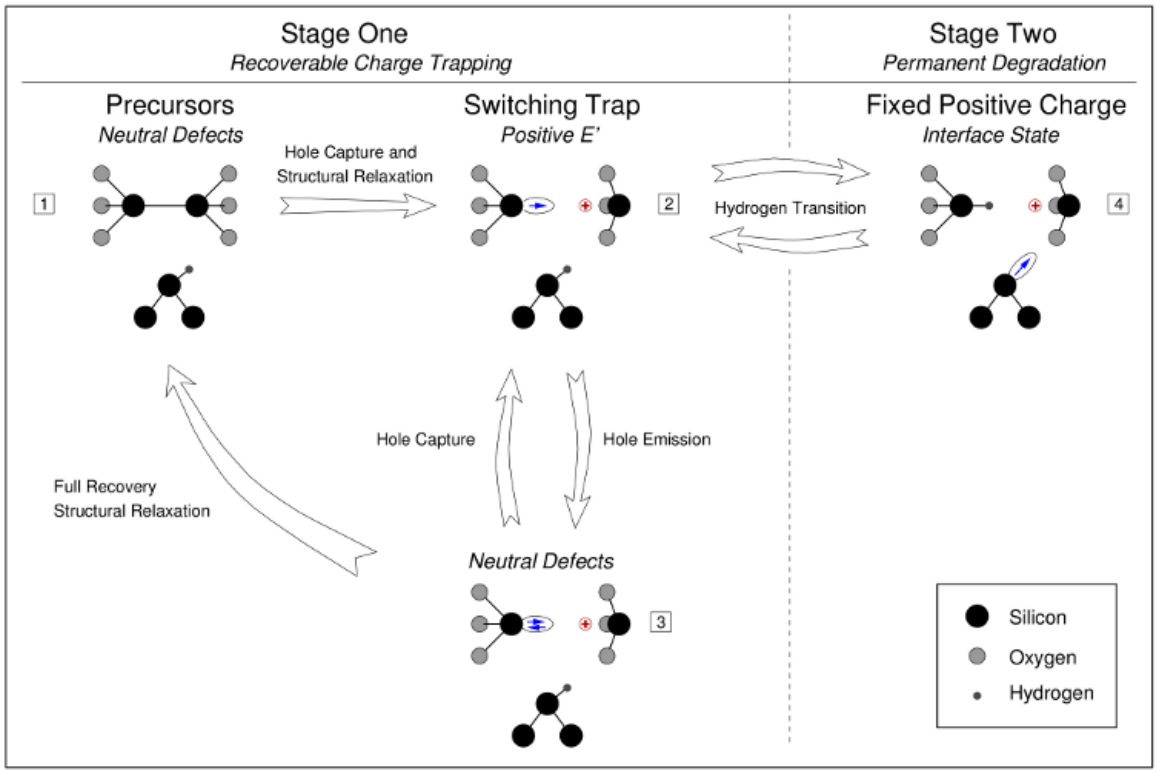

Figure 2.14: Switching oxide trap model, After [16]

Recently Grasser et al. [80–82] have also extended the study and included hydrogen-related centers associated with NBTI. Complexes that incorporates oxygen and hydrogen (e.g., the hydrogen

bridge, a hydrogen atom at a dimer O vacancy in SiO_2 [80–82], and the hydroxyl E center, a strained O bonded to a hydrogen atom [83], [84]) may also affect NBTI. Compared to the E'$_\delta$ centers, these defects are modified structurally and/or chemically via NBTI. Moreover, the hydrogen-related defects increase in density as a result of NBTI.

2.5 Previous work on SEE in bulk and FinFET devices

The material properties, complex gate stacks, and device architecture can strongly impact ion-induced charge collection of semiconductor devices [56, 58, 60, 61, 67]. F. El-Mamouni et al. and H. Gong et al. extensively explored the drain bias dependence of SET-induced charge collection in bulk and FinFET devices [56], [60]. It has been shown that increasing the drain bias reduces the transient current rise time in Si/InGaAs bulk FinFET devices which is a signature effect of substrate, unlike SOI devices. Gate bias dependence of SEE has been performed in [60], [61] for InGaAs FinFET devices. It has been reported that there is no gate bias dependence for InGaAs FinFET devices while the peak transient current is reduced for planar devices. A reduced excess carrier density in the channel when the device is biased in the inversion results in a reduced transient current [67]. On the other hand, a thin channel in the FinFET devices is completely depleted and no gate bias dependence is observed in the FinFET devices [60], [58]. The radiation responses of bulk Ge pMOSFETs and SiGe FinFETs also have been evaluated in a number of studies [85–89]. Pulsed laser tests can provide important information about the strike location dependence of SET-induced charge collection [10, 48, 90]. Previous work on single-event transients (SETs) in SiGe- and Ge-channel planar devices demonstrates that the peak transient current magnitude and polarity depend on strike location [52], [19].

2.6 Previous work on TID and NBTI in MOS devices

Historically, GAA devices appear to provide more Total Ionizing Dose (TID) tolerance compared to planar devices [91–93] and FinFETs [94]. Si and III-V semiconductor-based GAA devices have been shown to be resistant to radiation-induced charge and parasitic channels [95–97]. Likewise, the radiation responses of bulk Ge pMOSFETs and SiGe FinFETs have been evaluated in a number of studies [85–89] but very few attempts have been made to investigate the TID response of Ge GAA devices. The NBTI [76] reliability appears to be process and architecture-

independent [98]. However, GAA NW devices may exhibit faster initial NBTI degradation and longer saturation time [99], [100]. Although a number of studies demonstrated that Ge may improve NBTI robustness [101–103], only a handful of studies investigated NBTI in Ge GAA NW pFETs [104].

CHAPTER 3

Single-Event-Induced Charge Collection in Ge-Channel pMOS FinFETs

3.1 Introduction

Scaling of CMOS technologies led to the introduction of FinFETs, in which the enhanced electrostatic control significantly improves off-state leakage (and thus power consumption), subthreshold slope, and short-channel effects [105]. III-V materials can provide enhanced electron mobility, but also can lead to manufacturing complications and reduced hole mobility [106]. Germanium has shown promise for p-channel devices, owing in part to the higher hole mobility of germanium and its potential alloys. As a Group IV elemental semiconductor, germanium is more easily compatible with silicon CMOS technology and can be manufactured to significantly greater purity standards than III-V compounds. Thus, the integration of SiGe and Ge technology with CMOS is an active area of research and development [29]. Ge-based FinFETs have been shown to maintain compatibility with conventional Si integration processes [17, 102, 107] with reduced short channel effects, reduced bias temperature instabilities, and increased hole mobility over Si.

The material properties, complex gate stacks, and device architecture can strongly impact ion-induced charge collection of non-Si channel FinFET devices. The radiation responses of bulk Ge pMOSFETs and SiGe FinFETs have been evaluated in a number of studies [85–89]. Pulsed laser tests can provide important information about the strike location dependence of SET-induced charge collection [10, 48, 90]. Previous work on single-event transients (SETs) in SiGe- and Ge-channel planar devices demonstrates that the peak transient current magnitude and polarity depend on strike location [52], [19].

In this work, Ge channel pFinFETs are irradiated with heavy-ions and a pulsed laser. Heavy-ion and laser test data suggest that the total collected charge strongly depends on applied gate bias, but the peak transient current shows little variation with gate bias. The effects of strike location on the polarity of the peak transient current are also explored using pulsed-laser irradiation. Unlike the SiGe pFinFETs and planar Ge devices examined in previous studies [52], [19], the change in the polarity of transient current that occurs when the strike location moves from source to drain is observed only for source transients in the ultra-thin quantum well devices examined here, and not

for drain transients. The mechanisms responsible for the dependence of charge collection on applied bias and strike location are investigated using 3-D TCAD simulations.

3.2 Experimental Details

3.2.1 Device structure

Germanium-channel p-type FinFETs were fabricated on 300-mm Si wafers by imec [17], [6]. The foundation of the device fin is n-type silicon, upon which a $Si_{0.25}Ge_{0.75}$ buffer is grown. A scanning transmission electron microscope (STEM) image of the device is shown in Fig. 3.1. Nominally undoped germanium is then grown on top of the SiGe layer to form the device channel. The base of the buffer layer is angled. This angle is formed because of the crystal lattice mismatch between the Si and SiGe layers and encourages dislocations resulting from the mismatch to propagate toward the side of the fin rather than toward the active area of the device. A thin silicon cap layer is grown on top of the Ge channel for passivation. SiO_2, HfO_2, and TiN are then deposited to form the gate oxides and gate metal, respectively. The active device is formed by growing a thick ($\sim$200 nm) layer of germanium on the silicon substrate [17], [6]. The raised source and drain are formed by depositing $Si_{0.25}Ge_{0.75}$ onto the Ge layer and implanting the SiGe with boron. Measured DC characteristics of the devices are shown in Fig. 3.2 and a band diagram of the structure is shown in Fig. 3.3. For the results discussed in this paper, the device gate length (as drawn) L_G = 120 nm, fin length L_F = 1 μm, fin width W_F = 100 nm, fin height F = 15 nm, and number of fins N_F = 4.

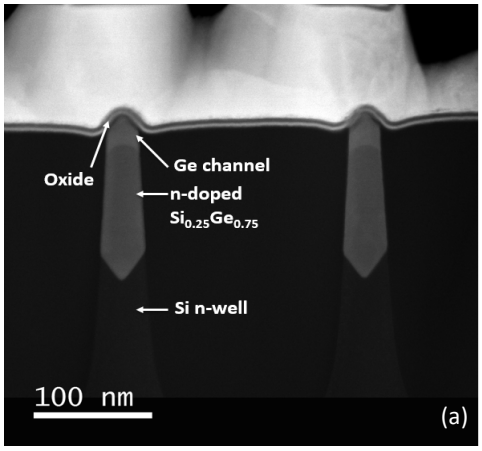

Figure 3.1: STEM cross-section of Ge-channel device, looking along the fin from source to drain. The gate stack consists of a Si buffer layer, SiO_2/HfO_2 dielectric, and TiN gate [17], [6]

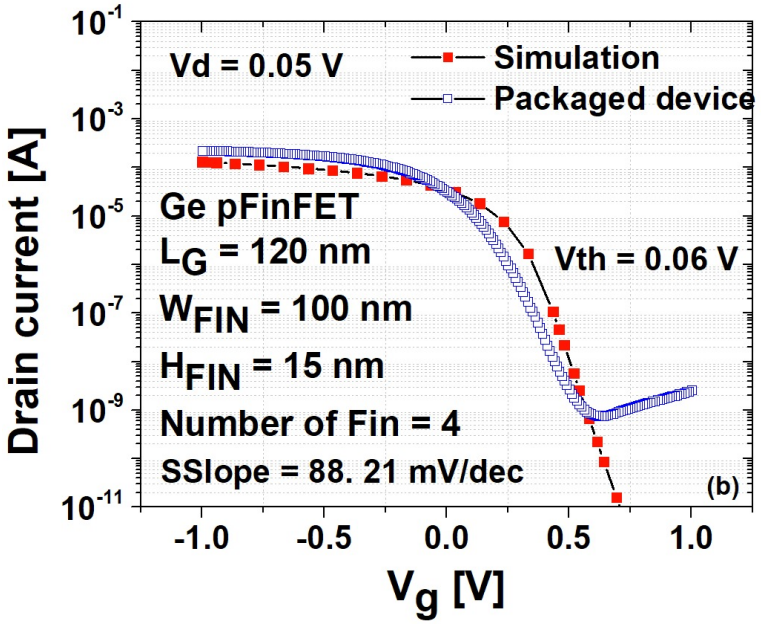

Figure 3.2: DC characteristics of Ge-channel p-FinFETs with gate length LG = 120 nm, fin height = 120 nm, fin width = 100 nm, and number of fins = 4 [18].

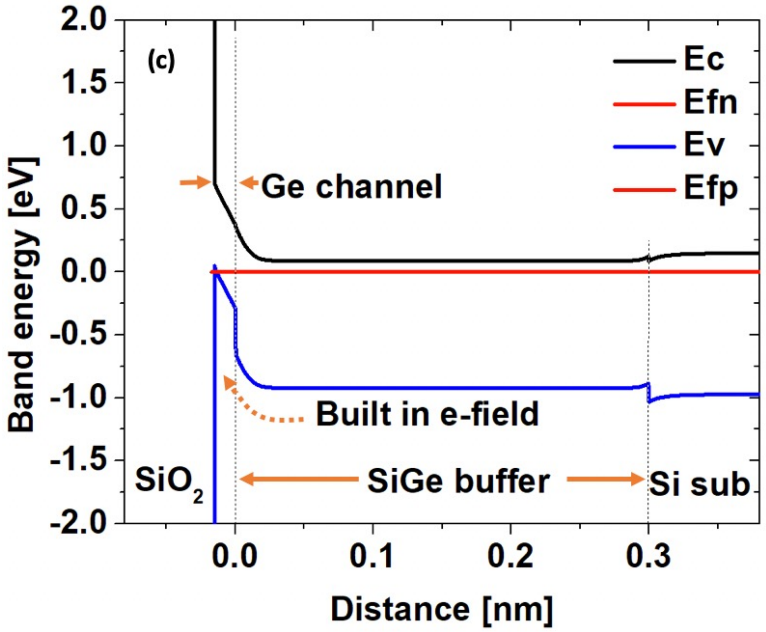

Figure 3.3: Vertical energy band diagram at equilibrium condition. The small built-in potential at the channel-buffer heterojunction contributes negligibly to the charge collection in these devices [18].

3.2.2 Experimental setup

Laser-induced single event transient (SET) tests were performed using the pulsed-laser system at Vanderbilt University, which generates 150 fs pulses with 1 kHz repetition rate [58]. This laser

system can be optimized both for the two-photon (TPA) and single-photon (SPA) absorption tests. Laser irradiation was performed with a wavelength of 1260 nm (energy of ∼0.98 eV) and spot size of ∼1.2 μm [48]. The sensitive regions of the Ge FinFETs are composed of Ge and SiGe. The SPA [48], [19] process dominates charge generation in the Ge channel (band gap ∼0.67 eV). SPA also dominates charge generation in SiGe, since the band gap of $Si_0.25Ge_0.75$ is ∼0.8 eV, derived through quadratic approximation [108], [109]. Two-photon absorption dominates carrier generation in the silicon (band gap ∼ 1.1 eV) regions of the device. Laser energies reported in the paper are for the incident beam at the surface of the device. Reflected energy from the silicon surface (∼30%) and energy converted into electron-hole pairs due to non-linear absorption are not considered when determining this value.

For pulsed-laser tests, DC bias was supplied by a semiconductor parameter analyzer (HP 4156A) through bias tees with 50-GHz bandwidth, allowing intermittent ID-V_G measurements to monitor the health of the devices and look for changes in characteristics. Transients are monitored by a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36-GHz front-end bandwidth and 80 GS/s sampling rate, as shown in Fig. 3.4 [108], [109]. Devices under test are mounted in a custom-milled brass package [110] designed for high-speed transient testing, as shown in Fig. 3.5. Device terminals are wire-bonded to impedance-matched strip lines and terminated with SMA- or K- connectors. A hole is drilled in the center of the package to permit the laser to strike the backside of the wafer, thus avoiding metal over-layers [19]. The laser spot is focused on active device areas by observing the reflected image that is transmitted through the microscope objective used to deliver laser pulses to the device. It is possible to see the metal layers from both reflected and transmitted illumination sources to determine the best focus, as confirmed by minimum observed laser spot size in the reflected image [48].

For the heavy-ion-induced SET experiments, devices were irradiated using the 88-Inch Cyclotron at Lawrence Berkeley National Laboratory (LBNL). The results shown are for irradiations with 1955 MeV Xe (LET = 49 MeV-cm^2/mg). SETs were measured using the high-speed pulse-capture setup shown in Fig. 3.4. These FinFETs have a total surface fin area of 0.048 μm^2 (channel length×fin width×no. of fins) per device, the small geometry of the device prevented timely measurement of a sufficient number of SETs when using the typical LBNL beam flux of ∼10^5 cm^{-2} s^{-1}. To solve this problem, the beam was focused from a spot-size on the order of a few inches

down to ∼1 cm in diameter, increasing the flux to an estimated value of ∼10^7 cm^{-2} s^{-1}. Tuning the beam in this manner prevented direct monitoring of flux and fluence; knowing these quantities to high accuracy is not important to the conclusions of this study.

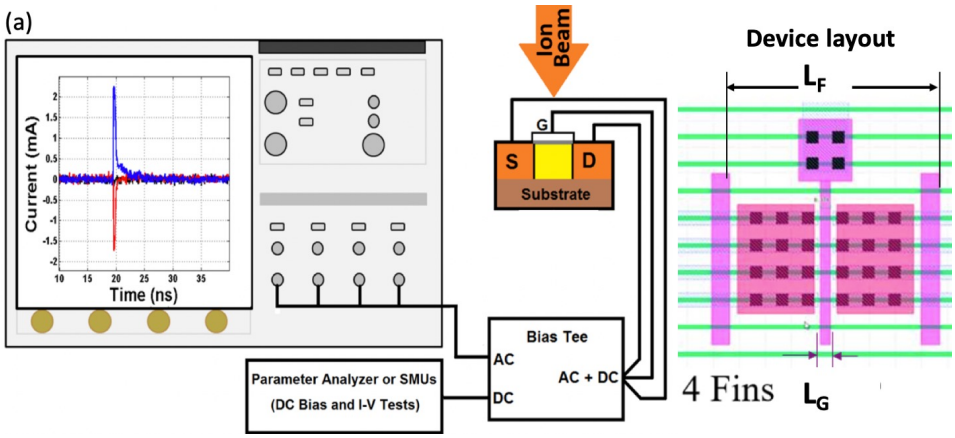

Figure 3.4: Block diagram of pulse-capture setup. High-speed bias tees decouple the AC transient signal from DC bias. Transients were recorded using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope [19].

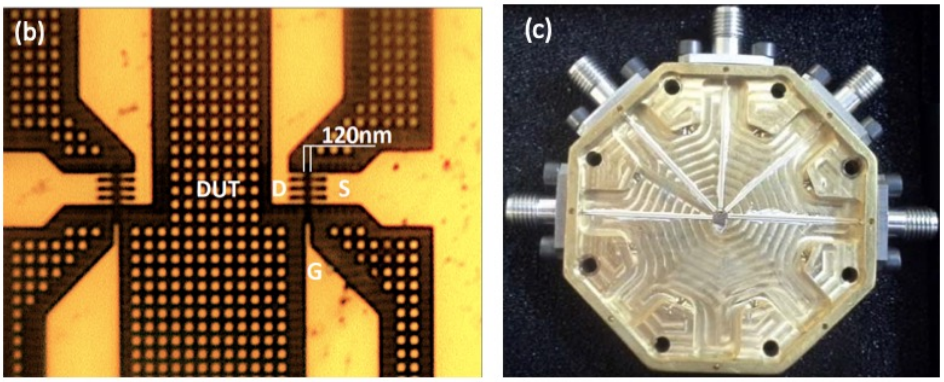

Figure 3.5: Microscopic view of DUT from the top showing contact pads of different terminals and the gate length, [18] and the packaged device [19].

3.2.3 SEE Simulation methods

3-D TCAD simulations of single event transients were performed by using the heavy-ion model in Sentaurus TCAD [111]. The models included Boltzmann statistics, bandgap narrowing, doping-dependent mobility, Shockley Read Hall (SRH) recombination, and avalanche generation. The carrier generation function is modeled as a Gaussian radial distribution both in space and time with a radius of 50 nm and a characteristic width of 2 ps. A normally incident heavy-ion with a

track length of 8 μm and a linear energy transfer of 49 MeV-cm^2/mg is considered to illustrate the relevant mechanisms. Fig. 3.5 shows a truncated structure and cross-sectional view of the investigated device. The simulation structure has the same gate length, fin width, and fin height as the actual DUT but the XYZ dimensions of the simulated volume have been extended to 5 μm, 5 μm, and 20 μm, respectively, to avoid effects associated with carrier reflection at the boundaries. The simulated structure is based on a rectangular fin geometry for efficiency, while the actual device has a triangular shaped fin. The triangular fin shape introduces non-uniform carrier distribution along the vertical direction, improves leakage performance, and modulates carrier mobility [112–114], but none of these factors has a significant impact on SET induced pulse width. Fig. 3.7 shows the transients generated by the calibrated TCAD model. The x-axis is re-scaled to compare with experimental results.

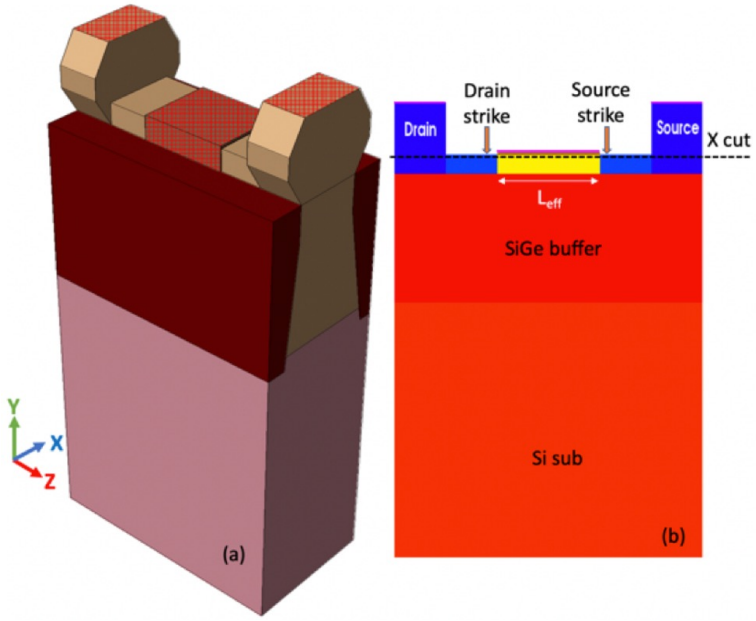

Figure 3.6: (a) Truncated 3-D structure of simulated device model. The actual model has the same gate length, fin width, and fin height as the real device but the simulated structure has an overall thickness of 20 μm, length of 5 μm, and width of 5 μm to avoid unexpected results due to the carrier reflection from the boundary; (b) cross-sectional view of the simulated device [18].

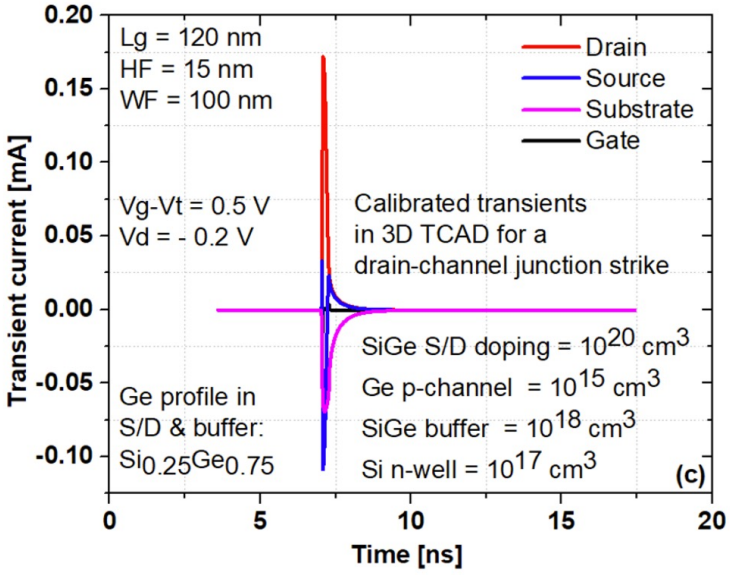

Figure 3.7: Transients generated by the calibrated TCAD model. The x-axis is re-scaled to compare with experimental results [18]

3.3 Results and discussion

An area scan using the pulsed laser for a 120 nm Ge channel FinFET device is depicted in Fig. 3.8. This contour plot outlines the epicenter of charge collected by the drain terminal during a laser strike within an area of 100 μm^2 around the device. The inset diagram of the device position implies that the positive drain transient current flows only when a laser strike occurs near the drain terminal.

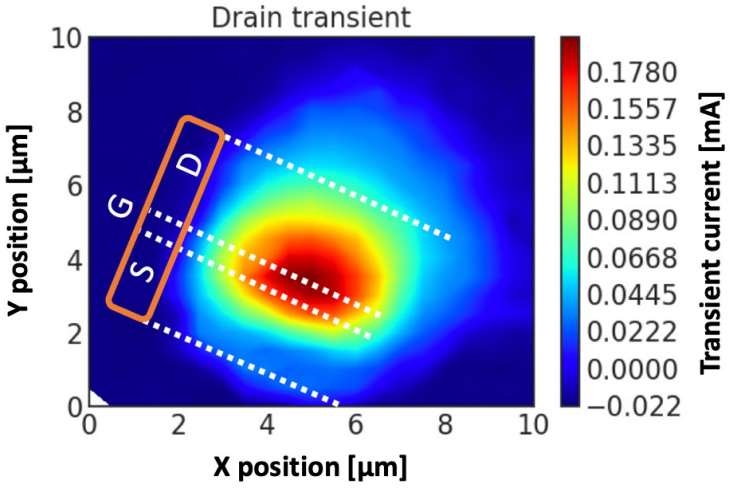

Figure 3.8: Experimental results of an area scan of a 120 nm device within an area of 100 μm^2 around the device showing the regions sensitive to the pulsed-laser strike. Experimental device position shows the terminals during the SPA test [18].

To explore the position dependence, a pulsed-laser line scan from source to drain is plotted in Fig. 3.9. It represents peak transient currents at the source and drain terminals as a function of strike location during the SPA pulsed-laser test. With a step size of 0.1 μm, transient currents from 100 laser pulses were averaged to extract the resulting current at each location.

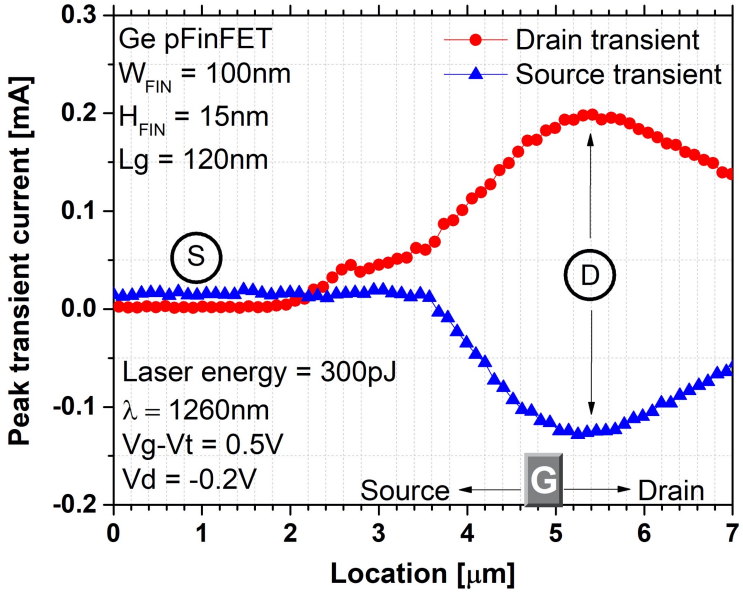

Figure 3.9: Experimental results of peak transient current on drain and source as a function of laser strike location along the channel length during SPA irradiation [18].

These data show that the strike position determines the polarity of the source transient current and that the drain transient current polarity is independent of strike position. The polarity of the source transient inverts as the strike location transits from source to drain. On the other hand, the lack of position dependence of polarity for drain transient contrasts with the trends observed in SiGe-channel and Ge-channel planar devices [52], [19].

The data in Fig. 3.9 show that the pulse magnitudes for drain strikes are larger than for source strikes, because the source-substrate bias is 0 V and the drain-substrate reverse bias is 0.2 V. Peak transients for source strikes are quite small in both these Ge FinFETs and planar devices [19]. This is due to the quantum well that is characteristic of the structure [52], [19], [115], as well as increased carrier recombination [52] during a channel strike. With higher channel resistance, a quantum well device responds to a strike as if the drain and source are nearly independent junctions. Studies of SiGe quantum well devices in [52] showed that the lack of field funneling [116] and increased

recombination dominate charge collection for a source strike. As a result, there is much less charge collection below the channel or source.

Representative single-event transient pulses for two different strike locations are plotted in Figs. 3.10 and 3.11. For these events, the device was biased in the hard-off state ($V_G - V_{TH}$ = 0.5 V; V_D = -200 mV; V_S = 0 V) during the pulsed-laser test. In Fig. 3.10, the laser-induced transient pulses resulting from a source strike, indicated by 'S' in Fig. 3.9, shows that the positive-going source transient current is accompanied by a negative-going transient current produced on the substrate contact. The drain transient for a source strike is positive and much smaller than the source and substrate transients, which indicates the dominant current path is source-substrate during a source strike. In contrast, for SiGe-channel and Ge-channel planar devices in [52], [19], a laser strike at the source terminal results in significant source-drain current. This difference occurs because the enhanced gate control of the FinFET structure is more capable than planar devices of maintaining complete depletion of the channel and therefore, blocking hole injection by the drain when an event occurs on the source.

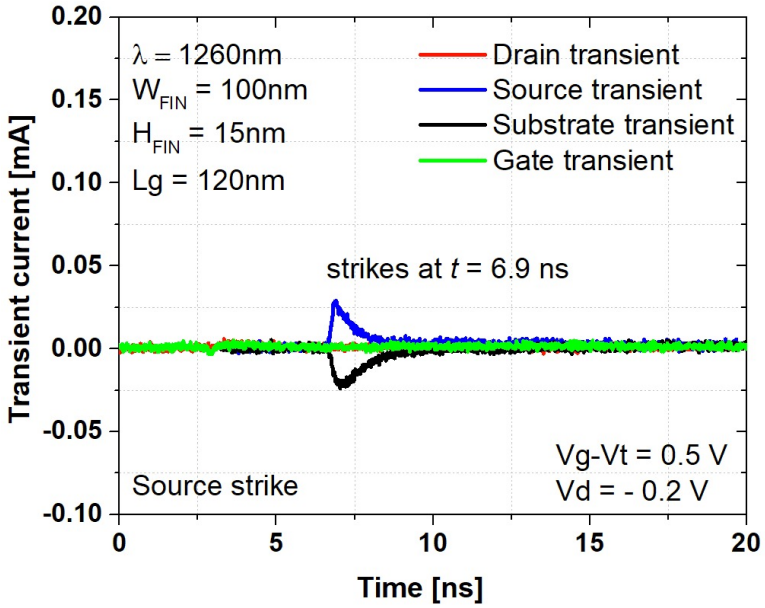

Figure 3.10: Experimental results of transient pulse resulting from pulsed-laser strike on the source terminal with the bias condition of V_G-Vt = 0.5 V, V_D = -0.2 V and Vs=Vsub = 0 V. The strike location is indicated by 'S' in Fig. 3.9 [18].

Fig. 3.11 shows transient pulses for a drain strike, indicated by 'D' in Fig. 3.9. Here, a negative going substrate transient current along with a positive going drain transient current indicates

that the dominant current path is drain-substrate. Moreover, the negative going source current becomes positive at t = 7.3 ns, as indicated by the circle in Fig. 3.11. This bipolar nature of source transient current indicates that there are two distinct processes associated with the charge collection mechanism, as also observed in planar Ge channel devices [52], [19].

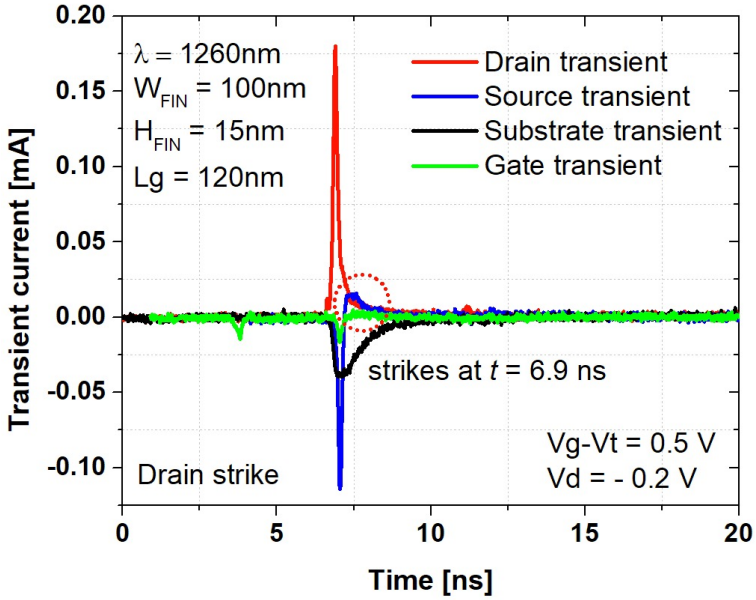

Figure 3.11: Experimental results of transient pulse resulting from pulsed-laser strike on the drain terminal with the bias condition of V_G-Vt = 0.5 V, V_D = -0.2 V and Vs=Vsub = 0 V. The strike location is indicated by 'D' in Fig. 3.9. The circle indicates the small current polarity inversion that occurs only for the source terminal for drain strikes [18].

3.4 Charge collection mechanism

The position dependence of a heavy-ion strike becomes a significant issue for deeply scaled devices, where multiple cells can be affected by shared charge deposition [117–120]. Since the strike position determines the polarity and the magnitude of the transient pulses, it is important to understand the underlying physics of the charge collection mechanism. The transient pulses resulting from a laser strike at the source terminal (depicted by 'S' in Fig. 3.9) are quite small in magnitude, as shown in Fig. 3.10. This is mainly because the strike location is away from the active channel region. Also, there is no secondary carrier generation mechanism involved since the impact ionization rate is small for a source strike. The majority of holes generated in the depletion region drift towards the zero-biased source terminal by a weaker electric field in the source-body depletion region. As a result, the drain terminal collects a small number of carriers and the resulting drain

transient current is very small for a source strike (Fig. 3.10).

When the laser strikes near the drain terminal, as shown in Fig. 3.11, the high density of generated carriers [13], [57] creates a transient conductive path between source and drain. This highly conductive path can result in a lateral shunt that accelerates prompt charge collection [13], [57]. The transient drift current leads to a sharp peak immediately after the laser strike at t = 6.9 ns. The differences in peak source and drain transient occur because the drain is biased negatively and the source and body are grounded during the SPA test. As a result, the increased electric field in the drain/channel depletion region or drain/body depletion region increases the velocity of carriers drifting towards the drain terminal, reducing the recombination rate and increasing the collected charge magnitude.

The slower charge collection process begins to dominate after the prompt charge collection subsides. This is due to the collection of carriers generated in the SiGe buffer layer. Excess electrons generated in the buffer region travel towards and forward-bias the source junction [52], [19]. As a result, the source injects holes into the body. These holes are collected by the drain terminal. Hence, the polarity of the source transient is reversed at t = 7.3 ns in Fig. 3.11. A similar bipolar effect leading to transient current polarity reversal occurs in bulk Ge-channel devices [52], [19]. This slower charge collection occurs as long as excess electrons remain at levels of significant density.

3.4.1 Gate bias dependence

Fig. 3.12 illustrates the total charge collected along a pulsed-laser line scan from source to drain for different gate biases. The peak charge collection depends strongly on gate bias. Maximum charge collection appears when a laser strike occurs near the drain/channel junction. The horizontal position dependence of charge collection is not spatially symmetric since a laser strike on the reverse-biased drain side of the channel leads to higher peak current and charge collection compared to hitting the source region where there is a field only due to built-in potential and there is high doping.

Fig. 3.13 plots the integral of drain transient pulses for a drain strike. The initial charge collection is quite rapid, regardless of gate bias. After the initial quick growth, charge collection increases linearly with time as a result of the “stretching out” of the exponential tail of the transient signal, as shown in Fig. 3.11. The long tail that results from the slower diffusion charge collection processes

is a strong function of gate bias. This mechanism dominates when the ultra-thin body becomes de-biased and the bipolar amplification becomes significant.

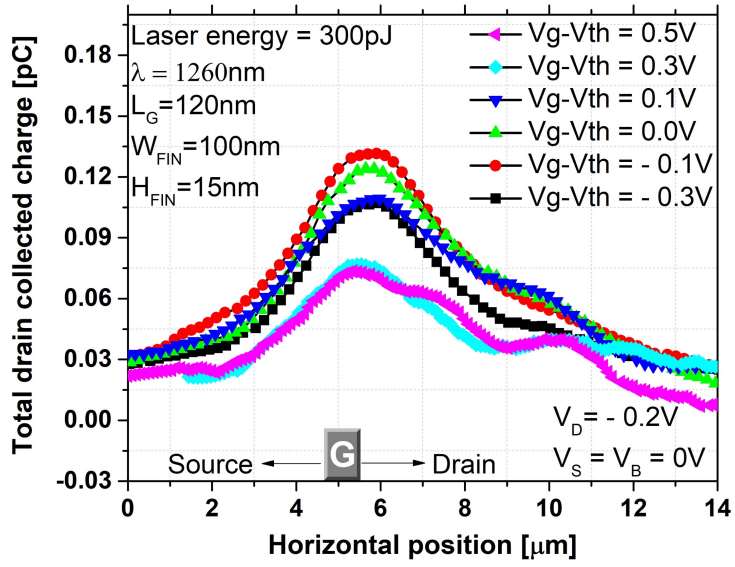

Figure 3.12: Experimental results of charge collected as a function of gate bias along the distance traversed by the laser from source to drain at V_D = -0.2 V [18].

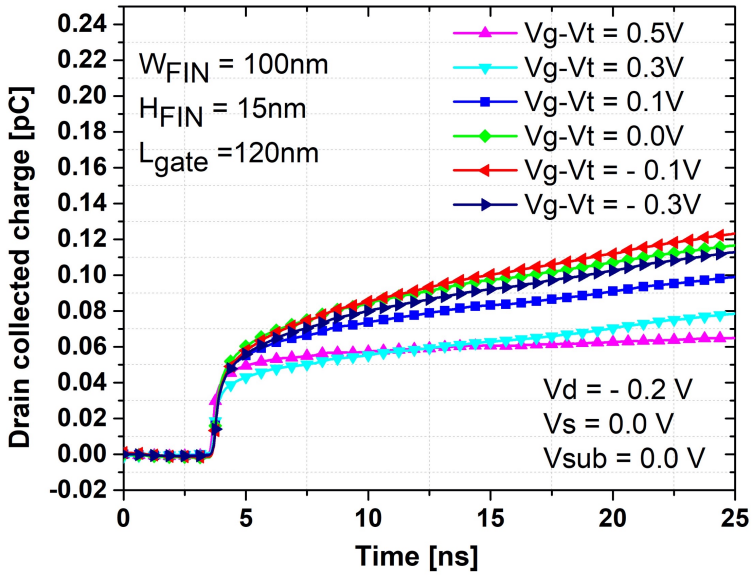

Figure 3.13: Experimental results of integral charge collected at the drain terminal for a drain strike as indicated by 'D' in Fig. 3.9 shows charge collected by the bipolar amplification process after the prompt charge collection [18].

Peak drain transient currents are plotted as a function of gate bias in Fig. 3.14. The bias de-

pendence of peak transient currents measured at the drain terminal under peak charge collection conditions is similarly weak for the heavy-ion and pulsed-laser data. TCAD simulations of the electrostatic potential barrier along the channel are shown as a function of gate bias in Fig. 3.15. These results confirm the weak gate-voltage dependence and formation of a transient shunt from source to drain [57], as inferred from the results of Figs. 3.9-3.11. This source-drain shunt mechanism is a significant issue for single-event-induced charge collection for any highly-scaled device for which the dimensions of the ion track are comparable to or greater than the device lateral dimensions [121–123].

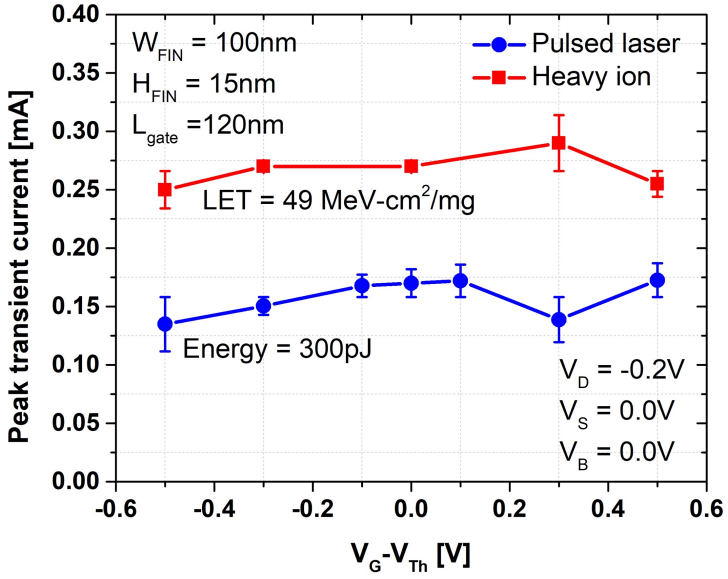

Figure 3.14: Experimental results of peak drain transient current as a function of gate bias. Error bars correspond to one standard deviation [18].

Fig. 3.16 plots the total collected charge at the drain terminal (positive-going peak drain transient current, as shown in Fig. 3.11) for heavy-ion and pulsed-laser tests as a function of applied gate bias. Trends in charge collection are similar for the laser and heavy-ion data. The total collected charge at the drain terminal depends strongly on gate bias, with peak charge collection occurring when the device is biased in inversion. The charge collection decreases slightly in strong inversion.

Fig. 3.17 shows TCAD simulations of the electrostatic potential distribution in the channel under conditions corresponding to the data of Fig. 3.16. After the prompt charge collection is essentially complete (at t = 8 ns), the potential barrier between the source and drain terminals now varies significantly with gate bias. The off-state (positive overdrive voltage) potential distribution

in the channel is re-established at this point. Since bipolar amplification primarily affects slower charge collection processes, the charge collection now becomes a strong function of gate bias.

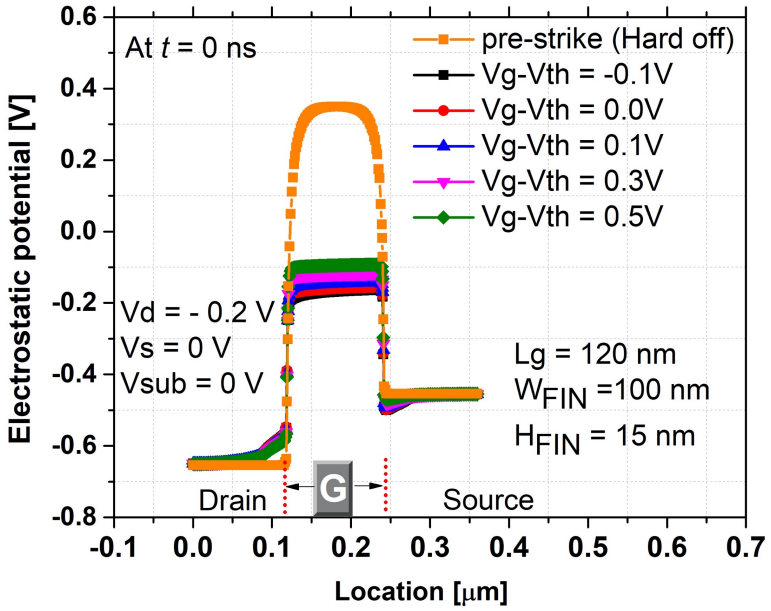

Figure 3.15: 3D TCAD simulation results of electrostatic potential as a function of gate bias immediately after the strike in a cutline of 2 nm below the oxide interface (X-cutline in Fig. 3.6). The potential barrier is a weak function of gate bias at $t = 0$ ns [18].

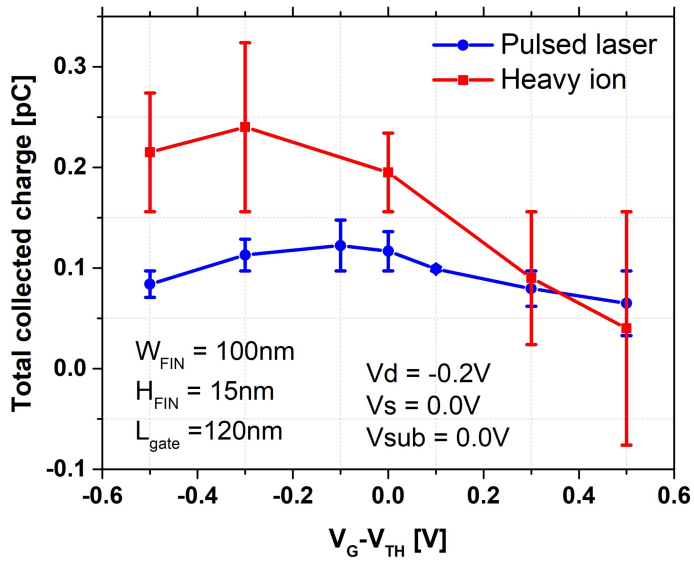

Figure 3.16: Experimental results of total collected charge with positive-going peak current measured at the drain terminal versus gate bias. Error bars correspond to one standard deviation [18].

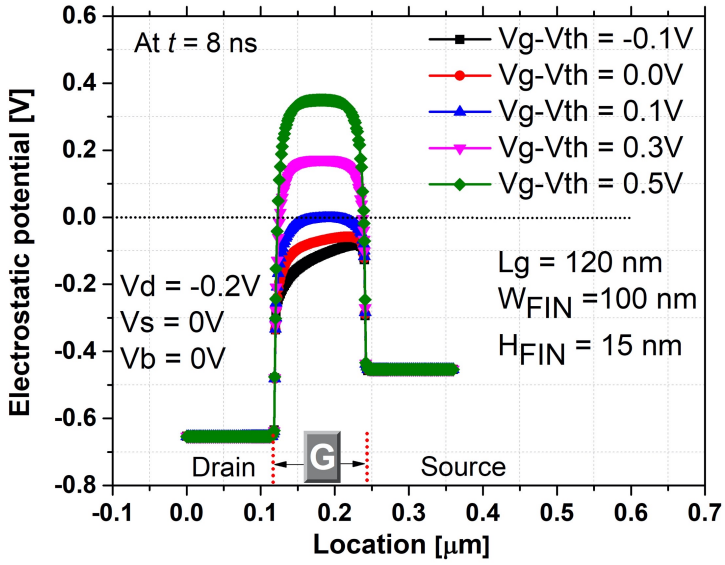

Figure 3.17: 3D TCAD simulation results of electrostatic potential vs. gate bias after a heavy-ion strike in a cutline of 2 nm below the oxide interface (X-cutline in Fig. 3.6). At t = 8 ns, diffusion charges are collected and the potential barrier varies strongly with gate bias [18].

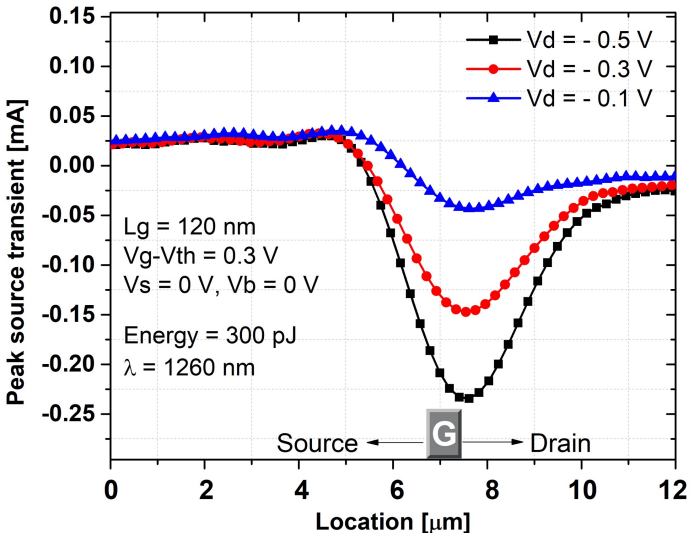

Figure 3.18: Experimental results of peak transient current at the source for laser strike locations from source to drain during the SPA irradiation as a function of drain bias [18].

3.4.2 Drain bias dependence

The peak transient currents at the source and drain terminals are plotted in Figs. 3.18 and 3.19, respectively, as a function of drain bias and strike location. Fig. 3.20 plots the collected charge from source to drain. The peak transient current and total charge along a line collection observed for a

drain strike are sensitive to the drain bias. On the other hand, significant drain-bias dependence is not observed for channel and source strikes.

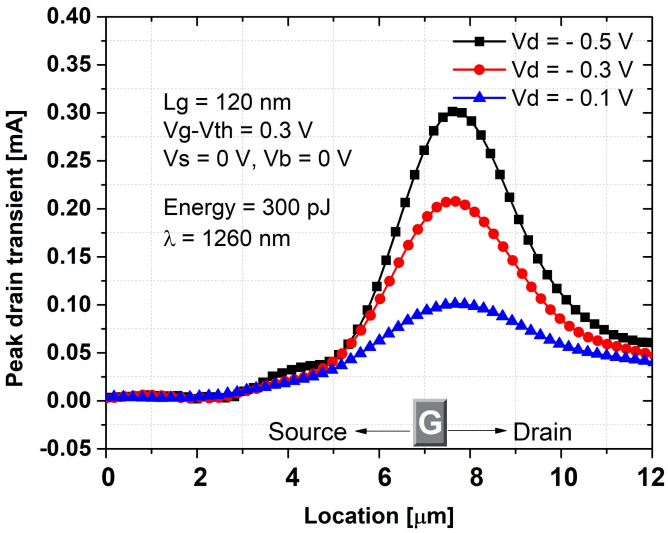

Figure 3.19: Experimental results of peak transient current on the drain for different laser strike locations from source to drain during the SPA irradiation as a function of drain bias [18].

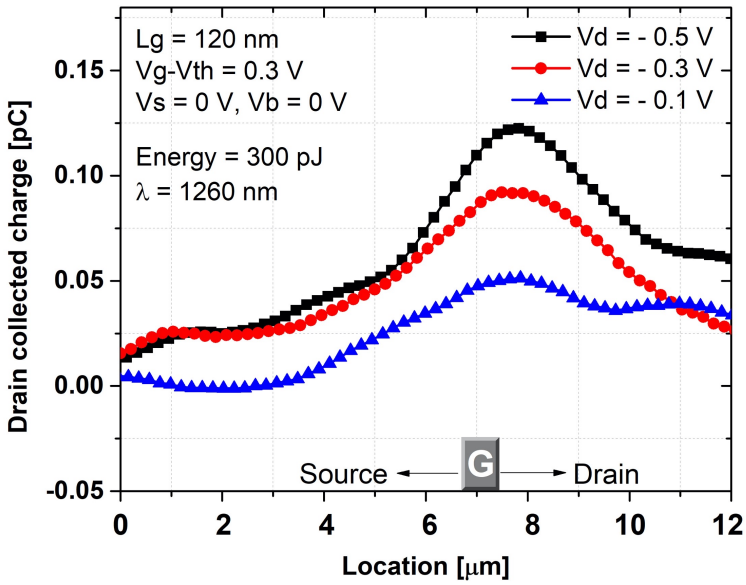

Figure 3.20: Experimental results of total charge collected at the drain terminal along a line scan from source to drain as a function of drain bias [18].

The higher channel electric field increases carrier velocity and decreases carrier recombination [124], [125], leading to increasing current with increasing drain bias, as shown in Fig. 3.19.

The magnitudes of Shockley-Read-Hall (SRH) recombination and impact ionization in the channel region are shown in Figs. 3.21 and 3.22 for different drain biases when the charge generation is maximum (t = 5 ps). These simulations illustrate the increase in impact ionization rates (Fig. 3.21) and decrease in recombination rates (Fig. 3.22) occur with increasing drain bias in these devices. The peak value of impact ionization occurs when the electric field is highest near the drain junction. In this region, the SRH recombination decreases strongly as the carriers approach the drain, and impact ionization leads to the generation of additional charge carriers and thus a further increase in collected charge. Increasing the drain bias may lead to an increased drain-induced barrier lowering (DIBL) [126–128]. However, the relatively small effects of DIBL on charge collection in these devices is negligible compared to the barrier lowering induced by the charge generation caused by the ion strike, shown in Figs. 3.15 and 3.17.

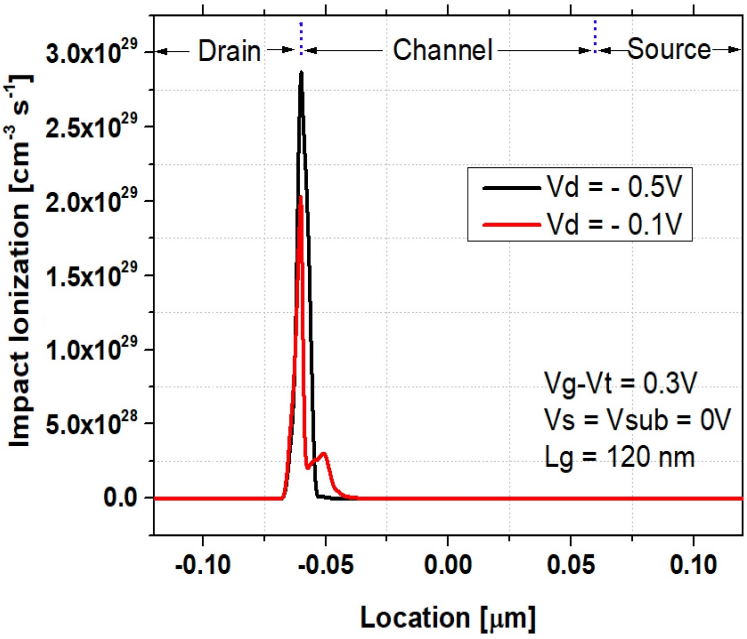

Figure 3.21: 3D TCAD simulation results of impact ionization rate from drain-to-source regions as a function of drain bias for a cutline of 2 nm below the oxide interface (X-cutline in Fig. 3.6), after an ion strike (t =5 ps) [18].

3.5 Summary and conclusion

Single-event charge collection behavior in Ge-channel p-type FinFETs depends strongly upon gate bias, as well as on heavy-ion or pulsed-laser strike location. The “fast” portion of the transient signal is due to a transient source-drain shunt effect. Hence, the peak transient current is nearly

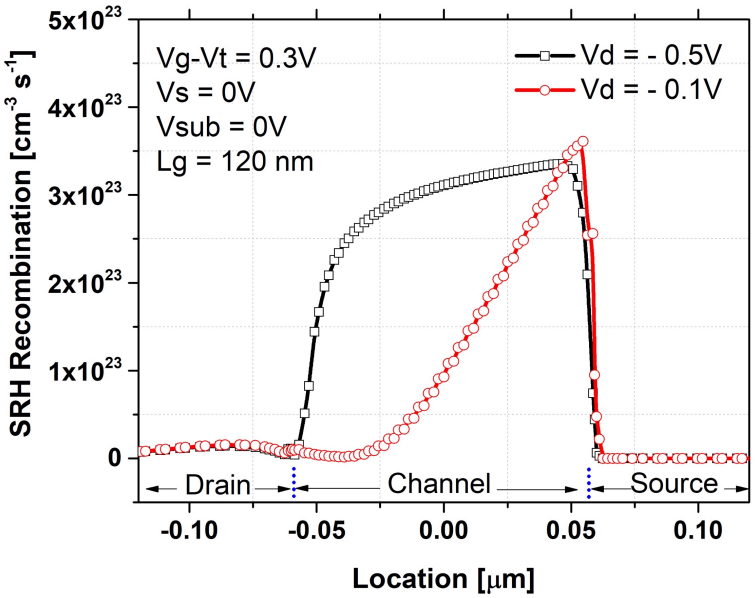

Figure 3.22: 3D TCAD simulation results of SRH recombination rate as a function of drain bias for drain-to-source regions in a cutline of 2 nm below the oxide interface (X-cutline in Fig. 3.6), after the ion strike (t =5 ps) [18].

independent of gate bias. After the drift current in the channel is "quenched" by the gate, increased charge collection comes only from the slower tail of the transient. As a result, the total collected charge changes dramatically with gate bias. Unlike SiGe pFinFETs and planar Ge devices in previous studies [52], [19], the change in polarity of transient current that occurs when the strike location moves from source to drain is observed only for source transients in this ultra-thin quantum well device, and not for drain transients. The differences between the charge collection on the Ge pMOS FinFETs in this work and that of previous work on planar SiGe and Ge pMOS devices are due primarily to the significant improvement of gate control of Ge-FinFETs over planar devices.

CHAPTER 4

LET distribution of Proton Induced Recoil Ions in Ge-channel pFinFET Devices

4.1 Introduction

Ge channel devices exhibit reduced short channel effects, improved robustness to bias temperature instabilities, and increased hole mobility over Si, which makes them a promising candidate for p-channel devices. Furthermore, germanium is more easily compatible with silicon CMOS technology [17, 102, 107] and can be manufactured to significantly greater purity standards than III-V compounds. Thus, the integration of SiGe and Ge technology with CMOS technology [29] for space flight electronics requires extensive study of radiation hardness for Ge-channel devices. Space flight electronics mostly experience single event effects due primarily to high energetic heavy-ion bombardment, coming from galactic cosmic rays. Typically, lower energy ions are available in a lab setting and are widely used to test single event effects. Although it is possible to reliably predict the radiation hardness using this handful of heavy-ion test facilities around the world, a more commonly used method is to use energetic protons/neutrons [129]. Various studies investigated the underlying mechanisms of proton/neutron irradiation to understand the linear energy transfer (LET) of different heavy ions in silicon devices [130–132]. The results were fruitful explaining many questions about SEE effects in Si technologies, but the radiation hardness studies based on proton/neutron-induced nuclear recoils in Ge channel devices remain unexplored.

Proton irradiation causes single event effects in semiconductor devices by interacting with target material nuclei. The incident particles create ionizing nuclear recoils through elastic and inelastic scattering, which deposit energy and generate electron-hole pairs eventually. On the other hand, the direct ionizing events resulting from energetic particles and light particles such as protons, neutrons, and alpha particles do not deposit enough local energy to generate minimum charges required to cause an upset, unless the devices are extremely sensitive [130]. The energy loss to charge generation due to secondary recoils generation from the interaction of the ion with a material depends on the target material, incident ion species, and energy. Therefore, the type and number of generated secondary elements, their contribution to the LET spectrum, and their range in target materials are expected to be different as compared to silicon devices. Hiemstra and Galimov [130], [133] have

shown that the secondary recoils generated in silicon comprise the species with atomic number Z = 14 and below. A recoil phosphorus nucleus is produced due to the rare occasion of an inelastic collision between a proton and a silicon nucleus.

Fig 4.1 shows the distance traveled by an energetic particle before stopping (range) as a function of energy loss per unit length (LET) of various nuclei in Silicon [134]. It shows that the maximum LET that can be produced by proton/neutron-induced secondary recoils is about 14.9 MeVcm^2/mg. For Ge, it is expected to be more than 14.9 since the generated secondary recoil ions will have an atomic number as high as 33 (Arsenic) resulting from an inelastic collision between a Ge (Z=32) nucleus and a proton/neutron. Fig. 4.2 shows the LET versus the energy of various nuclei in silicon bulk. The energy range of secondary recoils includes the energies produced by 500 MeV proton irradiation. Depending upon the complex gate stack materials used in semiconductor devices and the material used for local and global interconnects, the maximum LET in the sensitive region, and the energy of the recoils could reach even higher, making the study more crucial for the devices containing Ge like high-Z elements. Therefore, the LET threshold in test facilities needs to be clearly higher than the maximum LET generated by secondary recoils, to estimate the robustness of the device under test (DUT) against radiation.

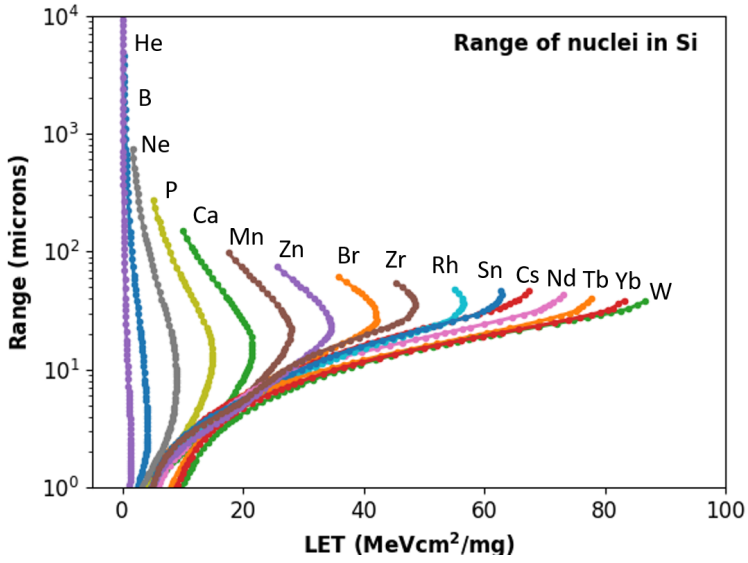

Figure 4.1: Range in Si of recoil ions resulting from proton bombardment as a function of recoil ion energy for ions Z=1-75.

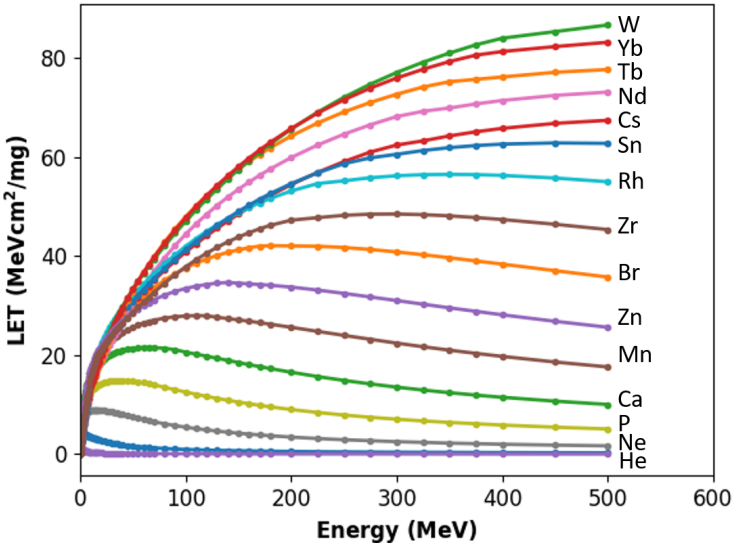

Figure 4.2: LET of recoil ions in Si resulting from proton bombardment as a function of recoil ion energy for ions Z = 1-75.

This chapter investigates the secondary recoils generation in Ge channel FinFET devices as a function of the incident proton energies from 50 to 500 MeV, based on the Geant4 simulation setup and the methodologies developed at Intel Corporation [135]. The results presented in this study illustrate the distribution of generated recoils in various regions of the device, the number of recoils generated somewhere in the device but depositing energies in the sensitive channel region, and the calculation of their LET distributions. In addition, to highlight the differences in Si and Ge materials' behavior under irradiation, we also investigate the contributions from metallization that include the effects of using tungsten as a local interconnect in Ge channel FinFET devices. It appears that the presence of high-Z material in semiconductor devices or in the interconnections such as tungsten (W) results in LET values well beyond those generated in Si when reacting with high-energy protons.

4.2 Simulation setup:

The multi-layered detector geometry of the Germanium-channel p-type FinFET device used in Geant4 Monte Carlo simulations was fabricated on 300-mm Si wafers by imec [17], [6]. The foundation of the device fin is n-type silicon, upon which a $Si_{0.25}Ge_{0.75}$ buffer is grown. Nominally

undoped germanium is then grown on top of the SiGe layer to form the device channel. The base of the buffer layer is angled. This angle is formed because of the crystal lattice mismatch between the Si and SiGe layers and encourages dislocations resulting from the mismatch to propagate toward the side of the fin rather than toward the active area of the device. A thin silicon cap layer is grown on top of the Ge channel for passivation. SiO_2, HfO_2, and TiN are then deposited to form the gate oxides and gate metal, respectively. The active device is formed by growing a thick (200 nm) layer of germanium on the silicon substrate [17], [6]. The raised source and drain are formed by depositing $Si_{0.25}Ge_{0.75}$ onto the Ge layer, and implanting the SiGe with boron. For the results discussed in this paper, the device gate length (as drawn) LG = 120 nm, fin length LF = 1 μm, fin width WF = 100 nm, fin height HF = 15 nm and the number of fins NF = 4. A scanning transmission electron microscope (STEM) image of the device is shown in Fig. 4.3 along with the simulated structure.

Geant4 Monte Carlo simulations [133], [136] are facilitated by taking the cross-section (dotted lines in Fig. 4.3) of the material stack used vertically in this device, rendering the methodologies developed in [135]. The target material stack contains a layer of tungsten interconnect, TiN gate, HfO_2/SiO_2/Si gate stack, Ge channel, SiGe buffer, and Si substrate, with the Ge channel defined as a sensitive volume. The thicknesses (not drawn to scale) of the individual material layers and the order are illustrated in Fig. 4.4. The cross-section area of all eight layers has been extended to 1 cm^2 to ensure that the generated secondary recoil ions stay within the boundary. It also improves the efficiency of data collection and analysis to calculate differential fluence per cm^2without compromising the accuracy of the statistics. Furthermore, the geant4 code has been customized to have a random position of the particle at normal incidence to the top surface of the first layers and penetrating through the detector layers. Since the radiation environment contains energetic particles with various energies, a range of proton energies from 65 MeV to 500 MeV have been simulated. The effects of the NYC terrestrial neutron spectrum have also been explored to cover the environment that may be appropriate for different space electronics. After having the detector geometry setup, 1×10^{10} protons/neutrons were shot to the top surface, and the generated recoils were monitored for each individual event. The geant4 source code has been modified to record the individual recoil ion species produced in other layers and entering the SV, including their energy and population information. Finally, the LET spectra of all recoil nuclei are calculated using the SRIM table and then summed up together to get an overall LET spectrum.

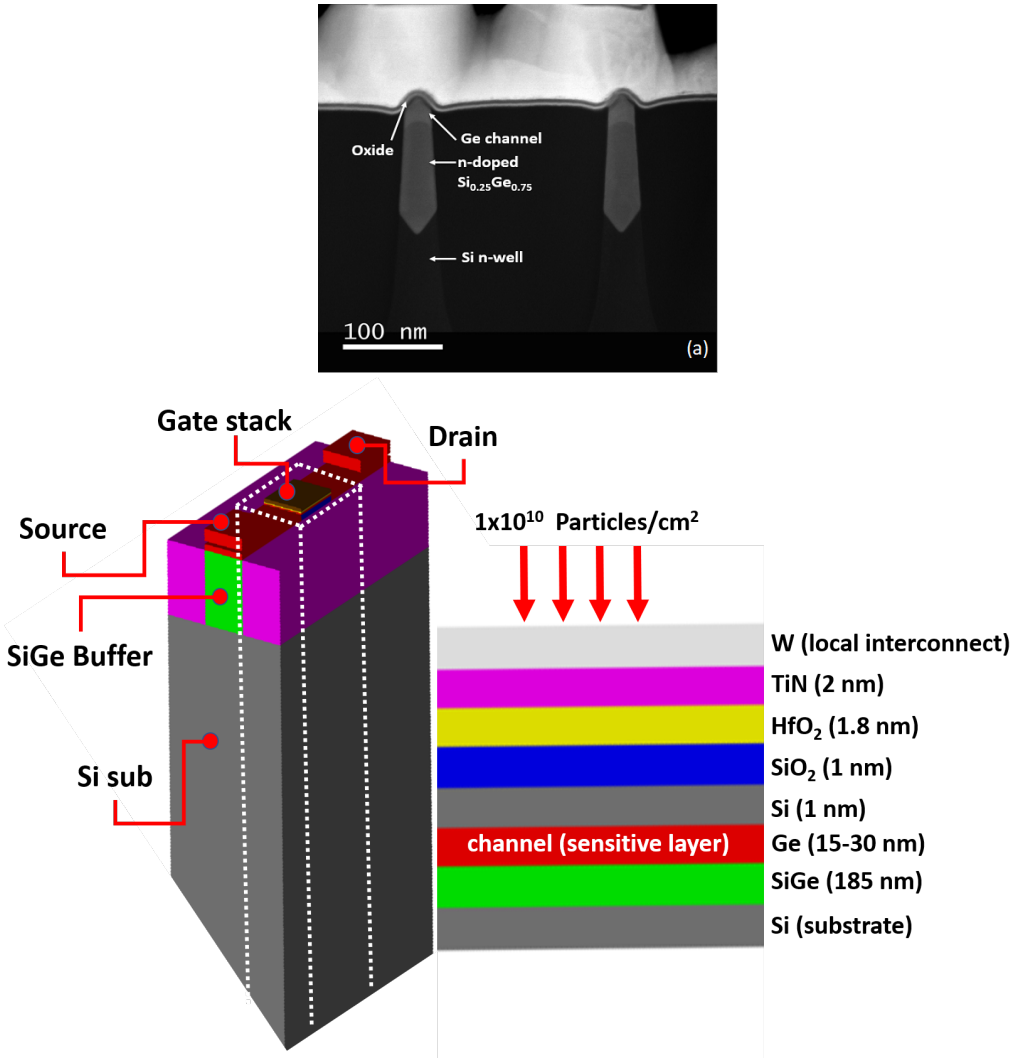

Figure 4.3: STEM cross-section of Ge-channel device, looking along the fin from source to drain. The gate stack consists of a Si buffer layer, SiO_2/HfO_2 dielectric, and TiN gate [17], [6], and the Genat4 simulation setup.

4.3 LET calculation methodology

Average LET convention [135] as illustrated in Fig. 4.4, has been used to calculate the LET of a secondary recoil ion. This convention defines the initial kinetic energy ($kinE_{initial}$) of a recoil ion as the kinetic energy of the recoil at the moment it enters the SV, or it is generated in the SV as indicated in Fig. 4.4. On the other hand, the final kinetic energy ($kinE_{final}$) is defined as the kinetic energy when the recoil ion leaves the SV. After that, the distribution of $kinE_{initial}$ and $kinE_{final}$ have been recorded from Geant4 Monte Carlo simulations with normally incident protons. Since the secondary recoil ion in SV can experience scattering, the energy deposition in each incremental

chord length may result in different LET values before the recoil ion finally leaves the SV. Final LET is calculated as the average of all LET values are given by the SRIM table corresponding from $\text{kinE}_{initial}$ to kinE_{final}.

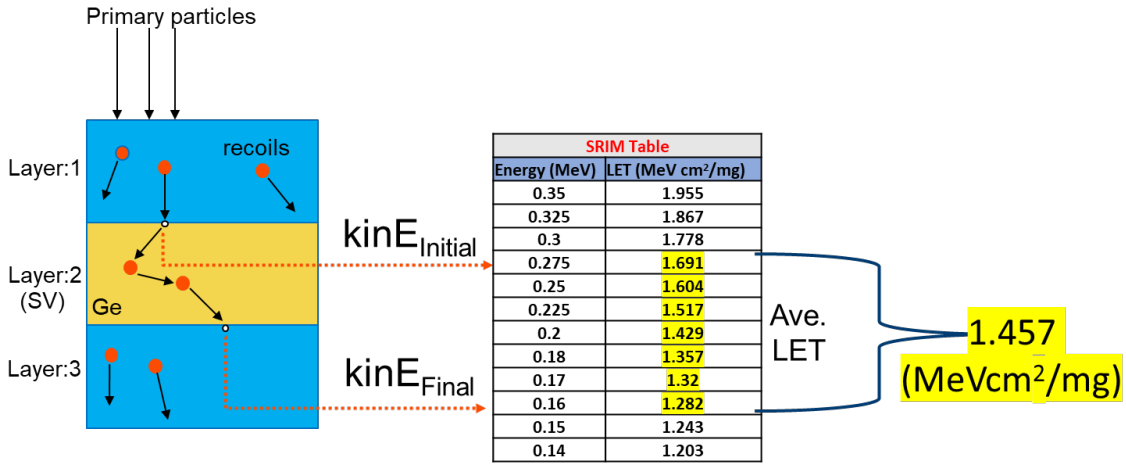

Figure 4.4: Illustration of average LET convention

4.4 Results and discussion

To validate the simulation model and highlight the difference in secondary recoil generation in Si and Ge under proton irradiation, a bulk Si and Ge layer of 10 um are irradiated with 200 MeV protons. Each target material has a cross-section area of 1 cm^2, making sure that the generated secondary recoils stay within the sample. As a result, a better statistic gives a more accurate estimation of the LET distribution of the recoils. The number of secondary recoils generated in a particular material depends on the material and the thickness of target nuclei. In general, the incident protons undergoing an inelastic scattering process can generate any secondary recoils with a lower atomic number than the heaviest target nuclei. On the other hand, the elastic scattering process dislocates the target nuclei, and finally, the displaced atoms can create a recoil ion with atomic number one higher than the target nuclei due to the neutron capture process [137]. It is worth noting that the mass and energy of the recoil ions determine their LET and range.

Fig. 4.5 illustrates the frequency of individual secondary recoils generated in bulk Si and germanium under proton irradiation. As indicated earlier, in Si the highest-Z atoms present are phosphorus (Z=15), similar to what other studies found [130–132]. In Ge the highest-Z atoms present are selenium (Z = 34), indicating the presence of higher LET recoil atoms during proton irradia-

tion. Moreover, the population of higher-Z recoils in Ge clearly dominates the overall distribution as compared to the lower-Z recoil atoms in Si.

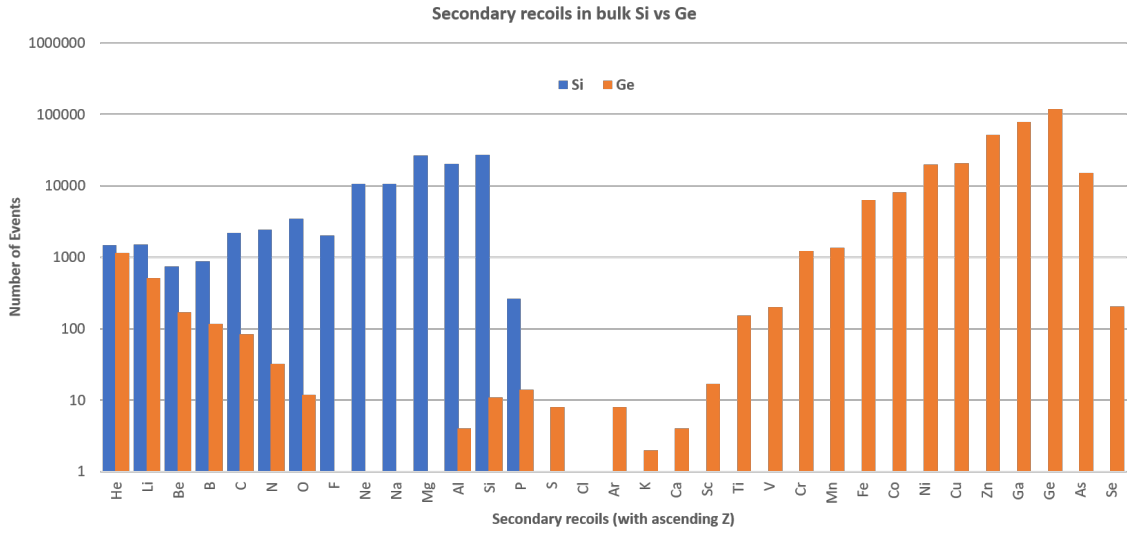

Figure 4.5: Comparison of secondary recoil ions generated in bulk Si and Ge

Generally, heavier ion possesses higher LET and potentially can cause SEE during proton irradiation. Therefore, it is important to investigate the LET distribution of recoil ions besides their population distribution. Since the LET of recoil ions are energy-dependent, geant4 source code has been customized to record the energies of each individual recoil ion produced from elastic and inelastic collisions. With appropriate post-processing, the energy data have been used to calculate the LET of each recoil ion using SRIM [134], and the LET spectrum of each energy level is plotted in Fig. 4.6. The results illustrate the number of events per cm^2, defined as the differential fluence as a function LET with a bin width of 1 MeVcm^2/mg. It can be noticed that the highest LET of recoils resulting from 200 MeV protons on Ge is 23 MeVcm^2/mg, much higher than that of the highest LET in Si (13 MeVcm^2/mg). This finding clearly indicates that the higher-Z recoil ions from Ge have LET values of $>$13 MeVcm^2/mg, contributing to the high end of the LET distribution. The LET distribution of Si has also been compared with previously found results for 200 MeV protons, validating the accuracy of the model in this study. The small difference in the LET distribution of Si between this work and the literature comes from the difference in detector geometry.

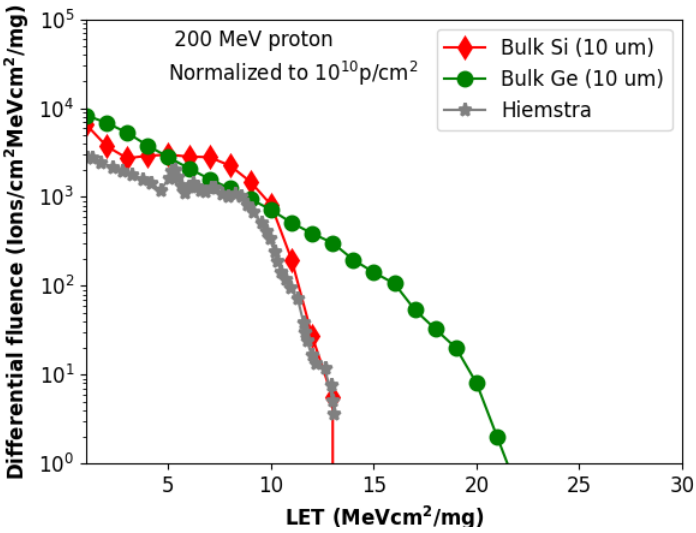

Figure 4.6: LET distribution of secondary recoil ions generated in bulk Si and Ge. Bin labels shown reflect the upper bound on LET of each bin

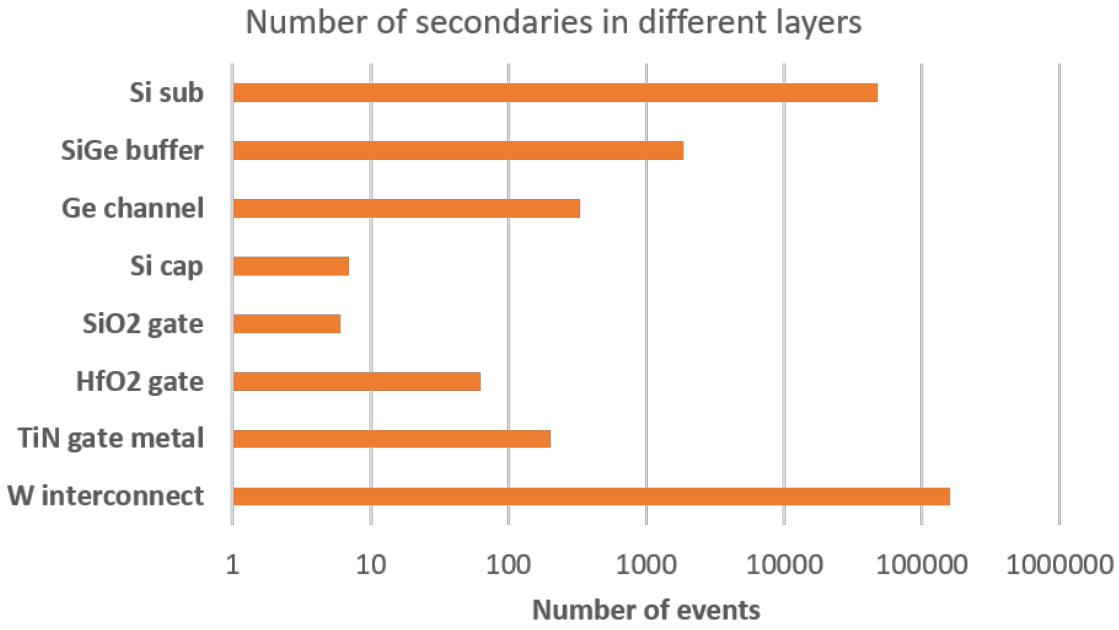

Figure 4.7: Number of secondary recoil ions generated in different layers of material used in Ge FinFET devices for 200 MeV proton.

4.5 Effects of local interconnect and gate stack

The result presented in Fig. 4.7 illustrates the number of recoil ions produced in different layers of material in Ge channel FinFET devices for 200 MeV proton irradiation. In this simulation, a

local interconnect of tungsten with a thickness of 2 um has been included. Therefore, the tungsten interconnects layer generates a larger number of secondary recoils, being the heaviest target nuclei in the target material. Some of the secondary recoils are also generated in the thin layers of Ge channel, Si/SiO_2/HfO_2 gate stack either through elastic scattering or inelastic scattering of recoils coming from other layers.

Fig. 4.8 illustrates the frequency of individual secondary recoils generated in all 8 layers of the material stack due to proton irradiation. It can be noticed that the secondary recoil ions range from Z = 2 to Z = 76, indicating the presence of high-Z (such as W) material in the device. The heaviest recoil ions generated from 200 MeV proton irradiation is Osmium, which has an atomic number of 76, two more than that of the heaviest target Tungsten nuclei. Technically, it indicates a subsequent inelastic collision of Rhenium, a secondary recoil generated from inelastic scattering of dislocated tungsten nuclei. As mentioned earlier, the high-Z recoil ions are mostly coming from local interconnect W, TiN gate. On the other hand, Si substrate mostly generates the secondary recoil ions from helium (Z = 2) to phosphorus (Z = 15).

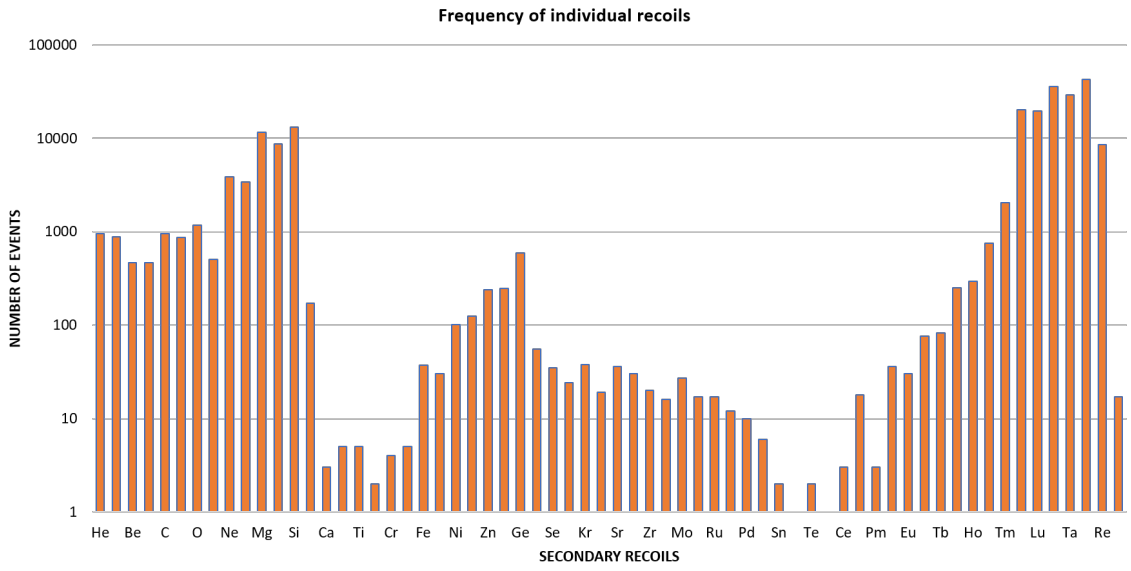

Figure 4.8: . Frequency of secondary recoil species generated in different layers of Ge FinFET devices for 200 MeV proton.

The previous study [18] demonstrated that the Ge channel region is very sensitive to SEE-induced charge collection in Ge channel pFinFET devices. Since protons do not contribute to SEE by direct ionization, it is important to identify the species of the secondary recoils and their popula-

tion which are depositing energy to the sensitive channel region. Fig. 4.9. shows the histograms of the contribution from each secondary recoil to the energy deposition into the channel. Although, the species of secondary recoils depositing energy into the channel have Z = 2 to Z = 74, the population of recoil ions is significantly lower compared to the total number of secondary recoils generated (Fig. 4.8), not necessarily all secondaries deposit energies into the sensitive volume. It can be inferred that the high-Z recoil ions striking the sensitive channel region and depositing energies are coming from the W interconnect and the TiN gate. In addition to that, only a small number of secondary recoils generated in the ultra-thin channel layer (Fig. 4.3), deposit energy, and contribute to the LET distribution. While the population of species detected in the channel layer provides valuable information about the particles that may cause SEE, investigating the LET spectrum of those recoils will give significant insight about their contribution.

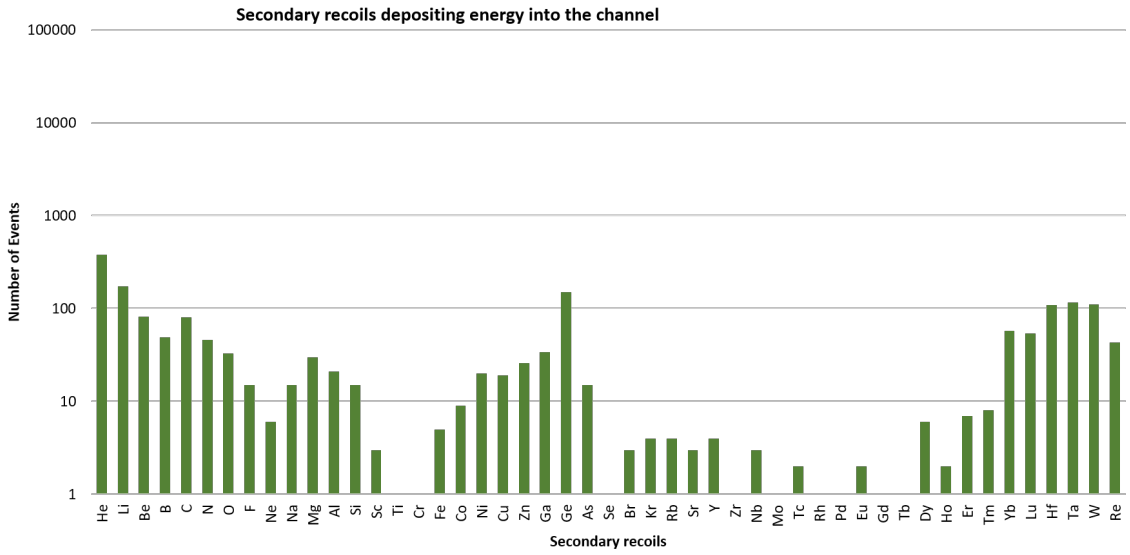

Figure 4.9: Frequency and species of secondary recoil ions detected in the channel of Ge FinFET device for 200 MeV proton.

The LET distribution of secondary recoil ions depositing energy into the sensitive volume is depicted in Fig. 4.10. Surprisingly, the LET spectrum for Ge channel FinFET exhibits weak dependence of Ge channel layer but a strong dependence on other high-Z materials used in this device. Two different spectra of LET distribution have been observed namely, the first spectrum ranges from 0 to 14 MeVcm^2/mg and the second spectrum ranges from 20 to 34 MeVcm^2/mg. This could imply that the test standards for Ge channel devices with tungsten interconnect and TiN gate needs to be

re-evaluated. Instead of 23 MeVcm^2/mg which was found for bulk germanium, the maximum LET of 34 MeVcm^2/mg needs to be considered, much higher than that of a silicon device. Otherwise, the full susceptibility might not be possible to identify experimentally.

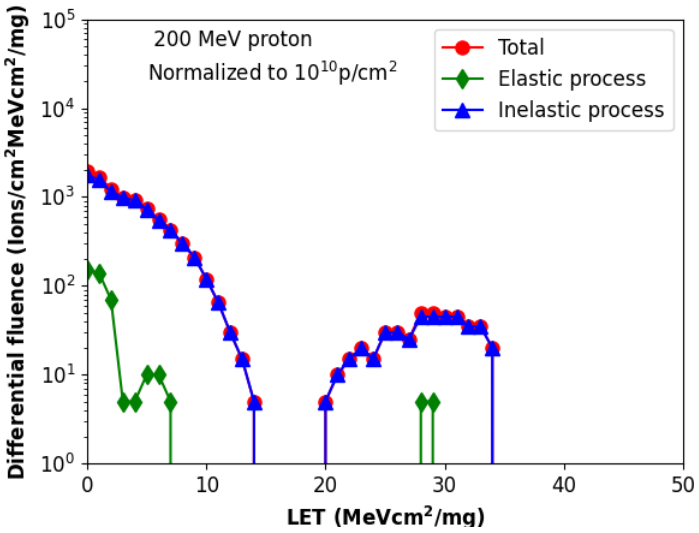

Figure 4.10: LET distribution of secondary recoil ions generated in Ge FinFET device. Bin labels shown reflect the upper bound on the LET of each bin.

Furthermore, the comparison between the LET spectrum resulting from elastic and inelastic processes confirms an insignificant contribution from elastic Ge recoils. The gap in the mid-range LET can be explained using the individual contribution of recoils to the LET spectrum as plotted in Fig. 4.11a. This plot illustrates the LET spectrum as a function of the atomic number of recoil ions. A similar plot has been generated for a Ge channel FinFET device without the W/TiN layer and plotted in Fig. 4.11b. Comparing these two plots it can easily be explained that the presence of a thin layer of Ge in the channel produces recoil ions with Z $<$ 33 which have a maximum LET of 20 MeVcm^2/mg (Fig. 4.11b). Recoil ions with Z $<$ 15, mostly generated in Si/SiGe layers have a maximum LET of less than 15 MeVcm^2/mg. On the other hand, the recoils ions with Z $>$34 entirely come from the spallation in the W layer. Surprisingly, only the recoil ions with Z = 34 to 50 contributes to the upper spectrum of LET with a maximum LET of 35 MeVcm^2/mg, whereas the recoil ions with Z $>$ 60 have a maximum LET of less than 15 MeVcm^2/mg which is similar to smaller-Z elements. None of these recoil ions contribute to the LET range from 15 to 20 MeVcm^2/mg.

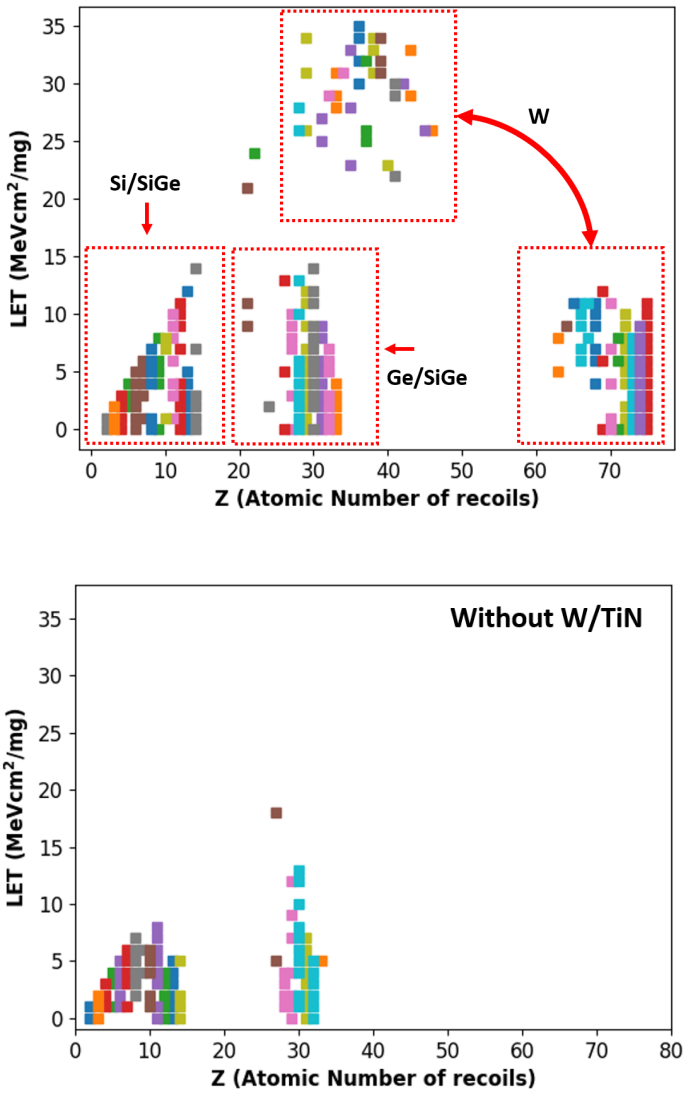

Figure 4.11: Mapping of individual recoil species contribution to LET as a function of atomic number for 200 MeV proton. Colors represent different species but overlap in colors may happen since the number of different species- is large.

The energy map of recoil ions depositing energy into the sensitive channel as plotted in Fig. 4.12, shows that the maximum kinetic energy of recoil ions is less than 160 MeV for 200 MeV proton irradiation. Generally, the LET of an ion reaches a maximum at the Bragg peak, immediately before it stops at a target material. The heavier recoils ions ($Z > 60$) have a maximum kinetic energy of < 10 MeV, far off from the Bragg peak. Although these heavier ions have higher LETs, the LET of these high-Z recoil ions does not reach beyond 15 MeVcm^2/mg because of their smaller kinetic

energies as illustrated in Fig 4.12. On the other hand, the recoil ions with Z = 29 to 50 strike the channel with sufficient kinetic energy and slow down there, resulting in higher LETs as they reach close to the Bragg peak before getting stopped or passing through.

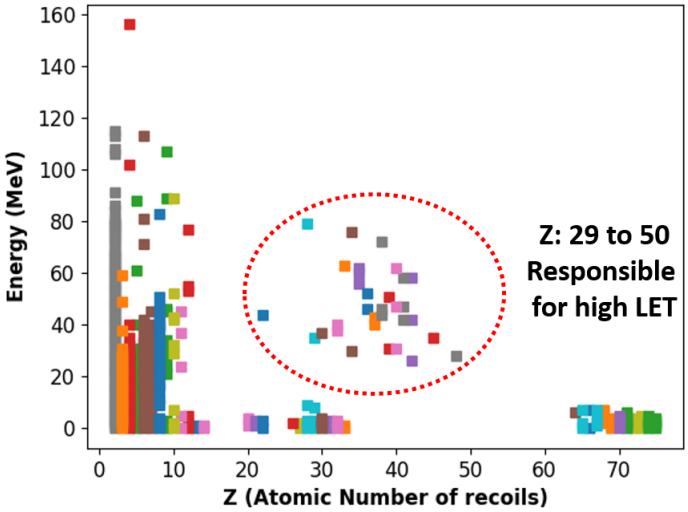

Figure 4.12: Energy mapping of individual recoil species as a function of atomic number for 200 MeV proton. Colors represent different species but overlap in colors may happen since the number of different species is large.

4.6 Charge deposition of recoil ions in SV

Recoil ions deposit charges through ionizing energy loss (LET) which largely depends on the ionization efficiency of recoil ions on a target material. Previous literature provides the experimental ionization efficiency of various species on Si and Ge [138], [139]. Besides experimental data, there are few methods to calculate the ionization efficiency for different species [140–147]. The Lindhard method [140] uses Robinson's analytical approximation [142] to calculate the partition of the deposited energy, where two different analytical equations are used based on whether the incoming recoil ion is the same as the target medium or not. The ionization efficiency of recoil ions also can be calculated using the transport of ions in matter (TRIM) Monte Carlo simulation [134], [148]. The Monte-Carlo method of calculating ionization efficiencies is applicable to different species and different target materials including compound semiconductor materials. By means of these one can estimate the energy deposited to create atomic displacement [147] and ionization. A modified expression of Robinson's analytical approximation, proposed by Akkerman and Barak

[144] is found to be more consistent with the experimental data as shown in Fig. 4.14. Fig. 4.14 illustrates the ionization efficiencies of various species in Ge calculated using modified expression of Robinson's analytical approximation. Throughout this study, ionization efficiency or recoil ions depicted in Fig. 4.14 has been utilized to calculate the charge deposition in Ge.

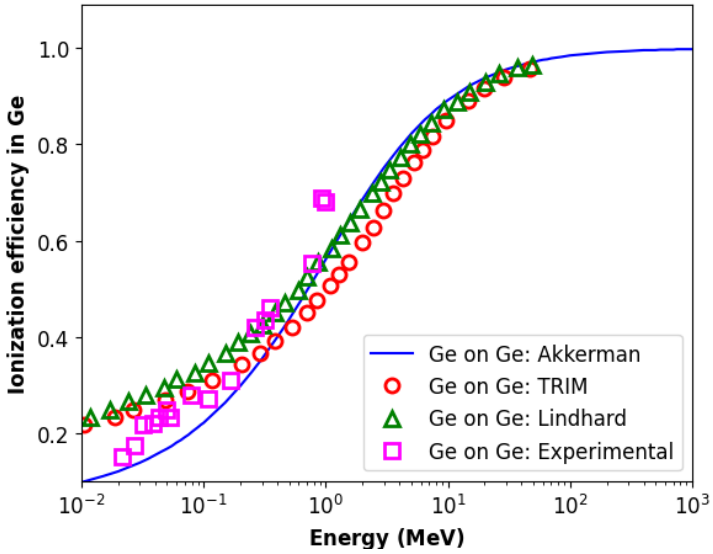

Figure 4.13: Experimental, TRIM, Lindhard, and Akkerman ionization efficiencies for Ge on Ge.

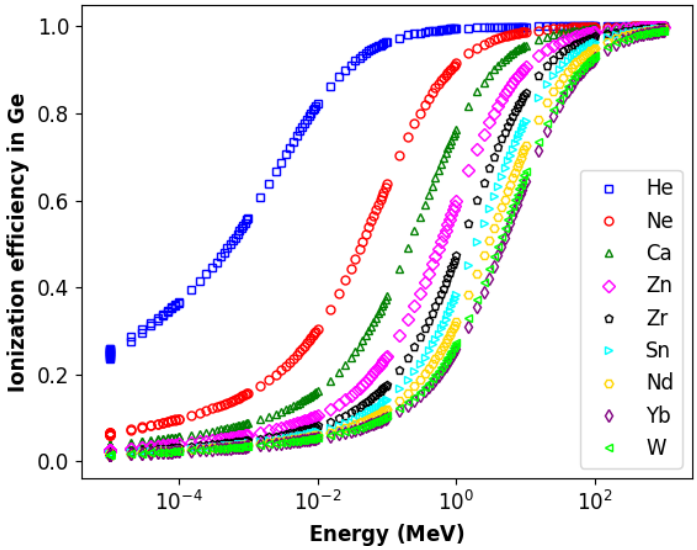

Figure 4.14: Akkerman ionization efficiencies of various recoil ions on Ge.

The charge deposition in a sensitive layer by recoil ions can be calculated using the simple

equation expressed by Eqn. 4.1. kinE$_{initial}$ is the initial kinetic energy when the recoil ion enters the SV, kinE$_{final}$ is the final kinetic energy when the recoil ion leaves the SV, $\sigma(E)$ represents the ionization efficiency at a kinetic energy E, and ε is the average energy required to create an electron-hole pair. For Ge, it is 2.9 eV.

$$Q_{dep} = \frac{kinE_{initial} \times \sigma(kinE_{initial}) - kinE_{final} \times \sigma(kinE_{final})}{\varepsilon} \tag{4.1}$$

The charge deposition in the sensitive channel layer by each individual recoil ion is calculated using Eqn. 4.1 and the Qdep$_{max}$ is plotted in Fig. 4.15 for 200 MeV proton irradiation. It can be seen that the maximum charge deposition occurs due to high-Z recoil ions. It can also be noticed that Ge recoil ion also deposits significant charges into the sensitive channel layer. If there were no W layer in the FinFET device, the Ge layer itself would be responsible for most of the charge deposition. As the proton energy increases, the production of recoil ions through the inelastic process also increases, giving more charge deposition. As a result, total Q$_{dep}$ increases significantly as shown in Fig. 4.16.

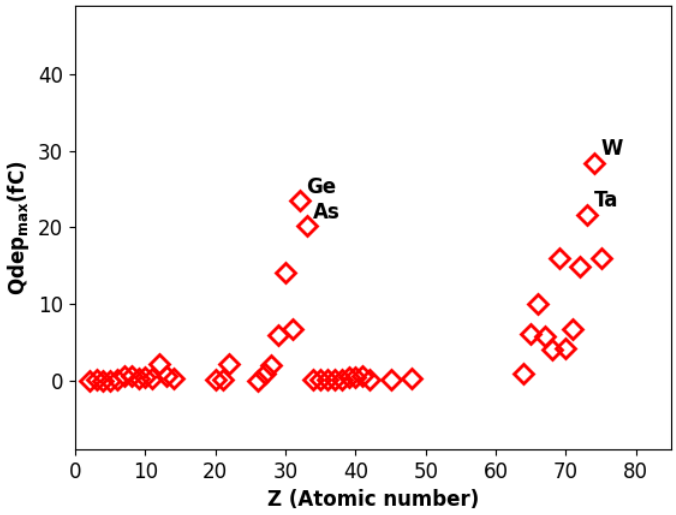

Figure 4.15: Maximum charges deposited (Qdep$_{max}$) into the channel as a function Z for 200 MeV proton. Ge, As, W, and Ta have been labeled for easy understanding of their charge depositions. It can be seen that the Qdep$_{max}$ for heavier recoil ions that are coming from the W layer is considerably higher than other recoil ions, signifying the effects of high-Z materials. Surprisingly, the Qdep$_{max}$ for Ge and its neighbors is also higher.

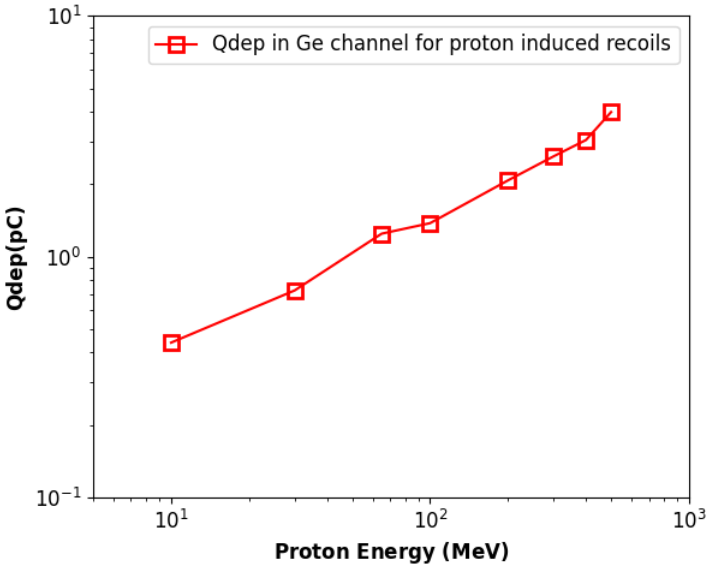

Figure 4.16: Total charge deposition into the channel layer as a function of proton energies.

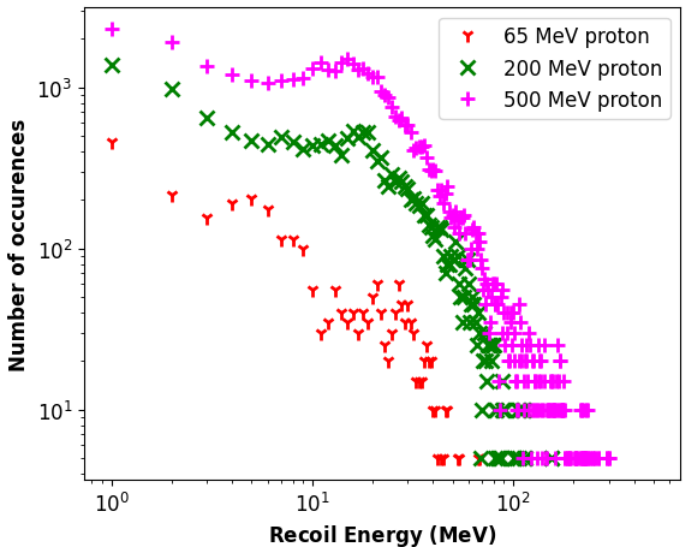

Figure 4.17: (a) Energy distribution plot of recoil ions depositing energies into the channel for different proton energies.

The energy distribution plot of generated recoil ions in Fig. 4.17 shows that increasing the energy of protons increases the maximum kinetic energy and the population of recoil ions. As a result, the production of higher LET recoil ions also increases and eventually contributes to the LET bin range from 15 to 20 MeVcm^2/mg. Most of the high energetic (>80) recoil ions fall within

the range of Z = 2 to 15, which has a maximum LET of less than 15 MeVcm^2/mg. As a result, the maximum LET shows insignificant change with increasing protons energies as depicted in the proton energy dependence of LET distribution plot for Ge channel FinFET devices in Fig. 4.18.

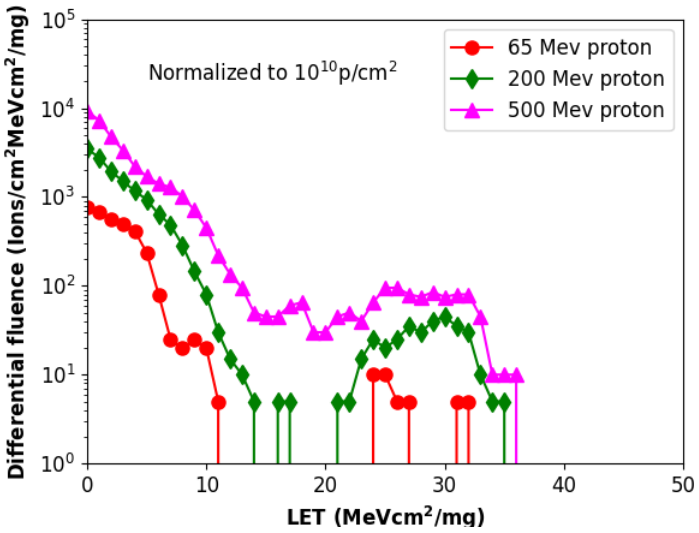

Figure 4.18: LET distribution of recoil ions depositing energies into the channel for different proton energies.

4.7 Effects of interconnect thickness on LET distribution

Tungsten is widely used as a local interconnect in semiconductor devices because of its low resistivity and conformal characteristics. However, the presence of tungsten in Ge channel FinFET devices produces high-Z recoil ions due to proton irradiation. Depending upon their kinetic energies, these recoil ions can have maximum LET values of the order of 35 MeVcm^2/mg. To understand the sensitivity of different thicknesses of tungsten and identify the worst-case LET distribution, the geant4 simulation model has been extended for 3 different thicknesses of tungsten. As plotted in Fig. 4.19, the variation in tungsten layer thickness does not bring a significant change in the LET distribution of recoil ions in the sensitive channel layer. There is an insignificant change in both the population of recoil ions and the maximum LET value for tungsten layer thicknesses of 2, 5, and 10 um.

The range vs LET plot in Fig. 4.1 shows that the majority of the recoil ions generated in the tungsten layer have ranges on the order of 10 μm with a maximum kinetic energy of 50 MeV. In-

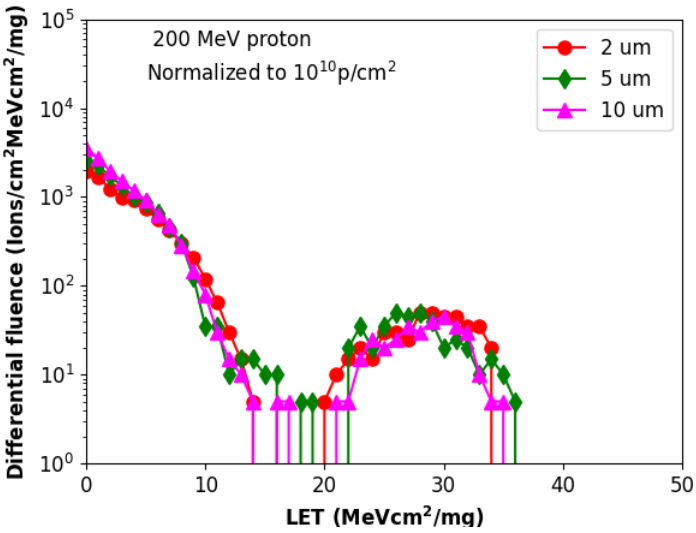

Figure 4.19: LET distribution of secondary recoil ions in the channel due to 200 MeV proton irradiation for different thicknesses of the tungsten layer.

creasing the target material thickness increases the total number of recoil ions but a thicker tungsten layer may restrict most of the high-Z low-energetic recoil ions from reaching the channel layer, as can be seen in table 1. Comparison of the total number of recoil ions vs. the number of recoil ions in the channel layer for different tungsten layer thicknesses is depicted by the histogram plot in Fig. 4.20. The percentage of the recoils detected in the ultra-thin Ge channel layer decreases abruptly with an increase in the total number of recoils as the thicknesses increase, keeping the change in the total number of recoils in the channel layer insignificant. As a result, the LET spectrum in Ge channel FinFET devices due to proton irradiation shows negligible dependence on tungsten layer thickness.

Table 4.1: Number of total recoil ions vs. recoil ions in Ge channel

W layer thickness	Total number of recoils	Number of necoils in Ge channel	% of recoils in Ge channel
2 um	209190	1772	0.84707682
5 um	453354	2188	0.482625057
10 um	860477	2565	0.298090478

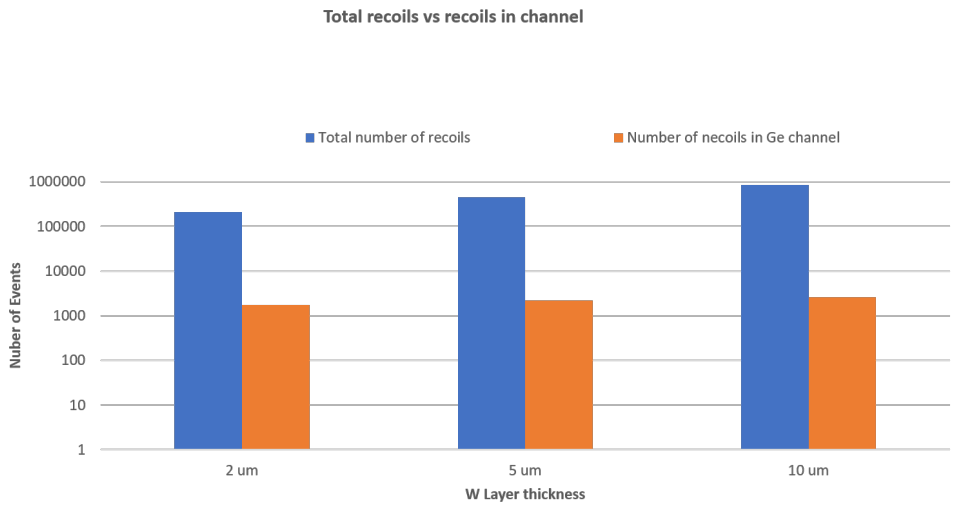

Figure 4.20: Histogram plot of the total number of secondaries generated vs the recoils striking the sensitive channel volume for 200 MeV proton irradiation.

4.8 Conclusions

The simulation results presented in this work demonstrate the key differences in LET of proton-induced recoil ions in Ge with Si. The population and the species of secondary recoil ions in Ge significantly vary. Moreover, the charge deposition profile of recoil nuclei as a function of proton energies provides a clear understanding of the processes undergone during proton irradiation in Ge channel FinFET devices that may lead to SEE. Space industries are mostly relying on test campaigns with LET thresholds we used to see in Si with proton energies below 300 MeV. In this lower energy regime, the highest LET recoil nuclei resulting from proton irradiation in Ge gives a LET value of 23 MeVcm^2/mg, exceeding the maximum LET observed for Si (15 MeVcm^2/mg). The presence of high-Z elements (W) Ge channel devices extends the maximum LET value up to 35, resulting from high-Z recoil ions generated in W and depositing energy into the Ge channel.

CHAPTER 5

Negative Bias-Stress and Total-Ionizing-Dose Effects in Deeply Scaled Ge-GAA Nanowire pFETs

5.1 Introduction

Vertically stacked gate-all-around (GAA) nanowire (NW) transistors [28,29,149–151] are among the most promising device solutions beyond the 5-nm node. They offer excellent electrostatics [104], [105] without requiring large changes in technology [152]. The ultimate carrier speed in nanowire devices largely depends on the carrier injection velocity on the source side [30], [31]. Materials with higher-than-Si hole mobility such as SiGe/Ge [29], [104], [20], [153], [32] in the channel increase the injection velocity and provide higher drive current. Including Ge in the channel requires optimization of key process steps [17, 102, 107] and integration of high-k dielectrics [154], [155], making Ge GAA pFETs serious con-tenders for post-Moore nodes [123]. Moreover, the improved drive current per unit area reduces the numbers of nanowires within the vertical stack, and thus reduces parasitic resistance and capacitance [156]. However, negative bias-stress and total-ionizing-dose (TID) effects may influence the performance and long-term reliability of GAA nanowire devices, influenced by both the structural nature and the high-K metal gate (HKMG) gate stacks [157], [158].

NBTI degradation is exacerbated by the increased electric field (Eox) that occurs with technology scaling since the supply voltages are not scaled by the same factor as the geometry [76]. Multi-gate technology introduces low channel/fin doping and the use of close-to-midgap work function metals in the HKMG stack, thereby reducing NBTI by reducing Eox [157], [159]. Unlike FinFETs or planar devices [99], [100], GAA NW devices can exhibit faster initial NBTI degradation and longer saturation times [99], [160]. However, incorporating Ge into the channel may improve NBTI robustness [101–103], which has been found to be a process and architecture-independent property of Ge channel devices [98]. Several experimental studies have been carried out to evaluate the impact of device dimensional scaling on NBTI [161–165]. NBTI evolution kinetics for nanowire devices have been explored using a conventional reaction-diffusion (RD) model in [166]. However, simulation results appear to be inconsistent with recent experimental results that show the

time evolution of the degradation is similar to planar and FinFET devices [158], [167], [168].

Previous reports suggest that GAA devices may have higher TID tolerance compared to planar devices [91–93] and FinFETs [94]. Si and III-V semiconductor-based GAA devices have been shown to be resistant to radiation-induced charge buildup and formation of parasitic channels [95–97]. Radiation-induced trapped charge and trap generation under the gate spacer in sub-100 nm GAA devices is shown to be the dominant factor causing device degradation [97]. In [169], [170], it has been found that no leakage current increase or subthreshold slope degradation in GAA-based memory devices up to 1 Mrad(Si). Recent studies have pointed out the improved radiation responses of Ge/SiGe bulk pMOSFETs and FinFETs [18, 85–89], but very few attempts have been made to investigate the TID responses of Ge GAA devices.

In this chapter, we explore negative bias-stress and TID effects in deeply scaled strained Ge GAA nanowire pFETs [171]. The negative bias-stress-induced degradation in Ge GAA devices mainly originates from interface-trap and border-trap generation. Due to the cylindrical nature of GAA devices, faster initial trap generation and rapid saturation are observed. In the recovery stage, oxide hole de-trapping is observed. The devices exhibit excellent TID tolerance with small variations in threshold voltage (V_{Th}), peak transconductance (G_m), and subthreshold slope (SS). However, the off-state leakage current increases with TID, due most likely to radiation-induced gate-induced drain leakage (GIDL) current.

5.2 Experimental details

5.2.1 Device structure

Development-stage Ge GAA pFETs were fabricated at imec on a 300 mm $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer (SRB) [172], [173] by adapting a FinFET process flow [174] with high-pressure-annealing (HPA) [20]. The fabrication process includes the formation of a SiGe/Ge/SiGe stack followed by wet etching of a SiGe sacrificial layer [175], leaving behind Ge NWs [104]. To improve interface quality, a thin Si cap layer of 6 monolayers [153] is epitaxially grown on Ge using Si_3H_8 or Si_4H_{10} precursor at 350 °C. Wet oxidation is used to passivate a SiO_2 interface layer (IL), followed by ALD HfO_2 deposition, leading to an effective oxide thickness (EOT) of 0.8 nm. Fig. 5.1 schematically illustrates a fully processed 70-nm strained Ge GAA. The high angle annular dark-field (HAADF) STEM image in Figs. 5.2 and 5.3 show a Ge NW (11 nm) surrounded by

a conformal Si-cap based gate stack and TiAl-based workfunction metal. The gate length of the devices was Lg = 70 nm. Each device has four fins with two vertically stacked NWs per fin, with a diameter of ∼11 nm. Effects of the parasitic $Si_{0.3}Ge_{0.7}$ fin under the Ge NW are addressed by setting V_{Th} sufficiently lower than for the Ge NW [104].

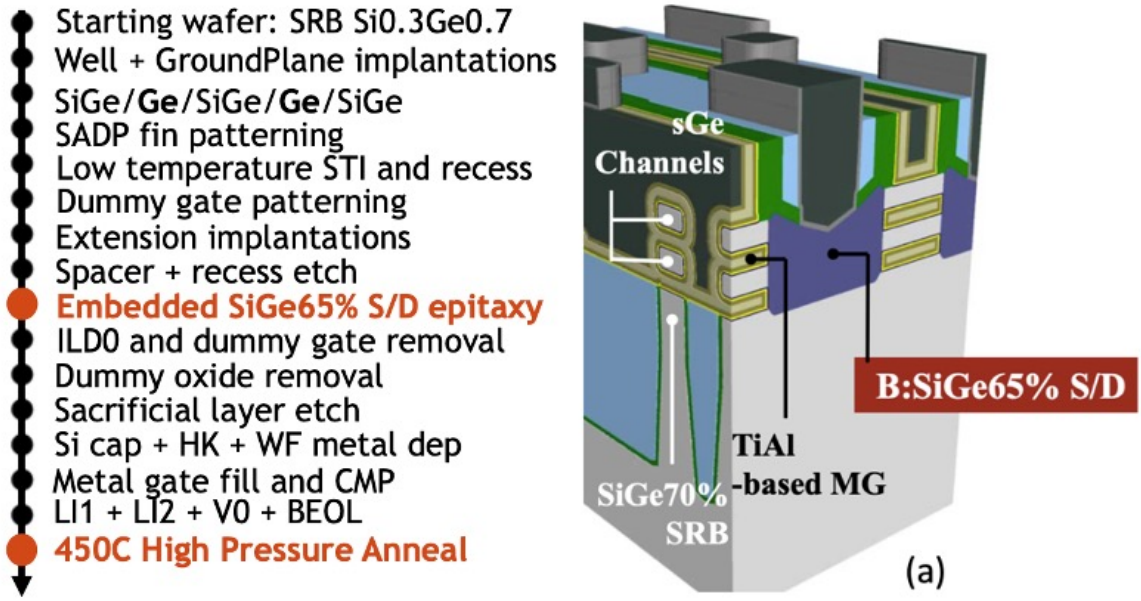

Figure 5.1: Process flow for the development-stage devices used in this work, without S/D stressors, mimicking a device with aggressively scaled gate pitch (for 7 nm and beyond) and a 3D illustration of Ge GAA NW pFET transistor from Coventor SEMulator3D [20].

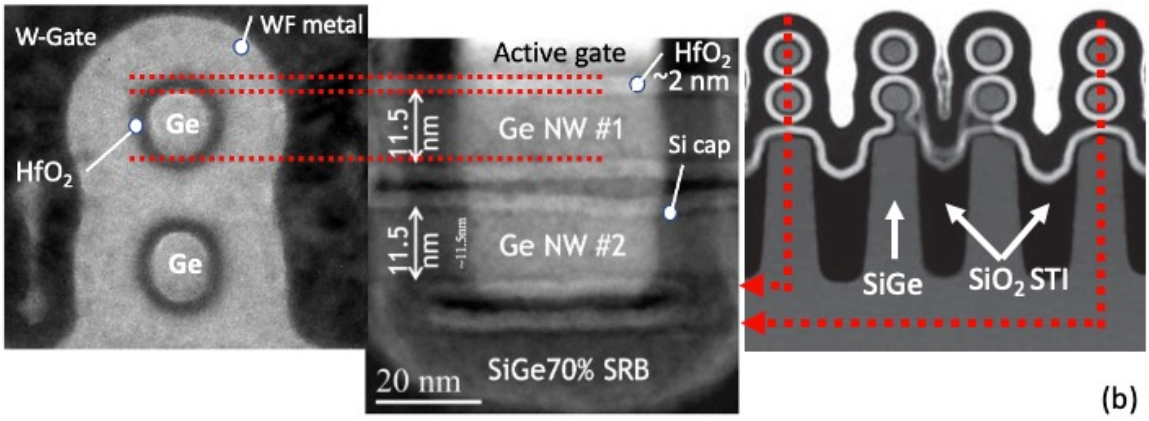

Figure 5.2: HAADF-STEM images of a Ge GAA device. The Ge NW is surrounded by HfO_2/SiO_2/Si gate stack and TiAl-based WF metal [20].

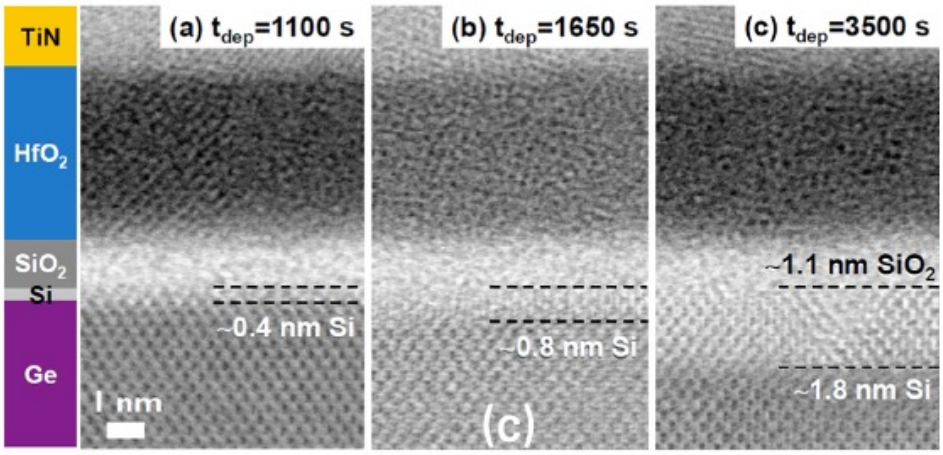

Figure 5.3: Cross-sectional TEM images of Si-passivated Ge gate stacks from [5], [6]. A very thin Si layer epitaxially grown on Ge is observed.

5.2.2 Experimental setup

Applied negative gate-bias stress voltages were V_G = +1 V, 0 V, 1 V, 2.0 V, and 2.5 V. Agilent 4156A/B semiconductor parameter analyzers were used to measure the $I-V$ characteristics with drain bias $|V_D|$= 50 mV. Each device was stressed up to 75 min. I_D–V_G and I_G–V_G characteristics were monitored at regular intervals to confirm that devices under test were operational and that high voltages did not compromise the integrity of the gate oxides. In TID experiments, devices were irradiated using a ∼10 keV ARACOR X-ray source [176] at room temperature at a rate of 30.3 krad(SiO_2)/min up to 1 Mrad(SiO_2) for gate biases (V_G = -1 V, 0 V, +1 V) with the drain, source and body at 0 V. Negative bias stress and TID experiments were performed using wafer probes at room temperature. At least three devices of each type were tested under the same conditions; error bars in plots represent standard deviations of measurements.

5.3 Results and Discussion

5.3.1 Negative bias-stress

Under negative bias-stress [98], interface traps and positive oxide charge generation may lead to degradation in semiconductor devices. Figs. 5.4 and 5.5 show typical I_D-V_G characteristics for Ge GAA devices at different stress biases and different stress duration, respectively. The devices were stressed at V_G = 0 V, -1 V, -2 V, and -2.5 V at room temperature. The negative bias-stress-induced degradation is smaller and builds up less rapidly at lower gate voltages.

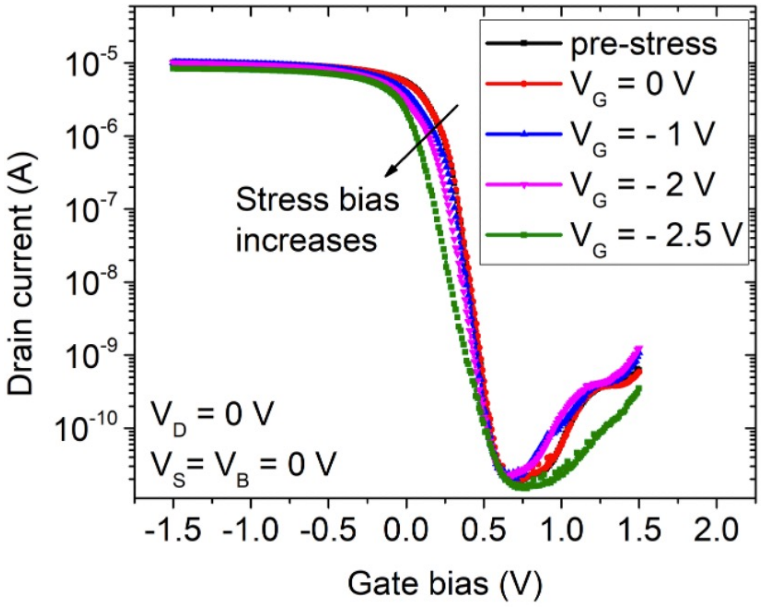

Figure 5.4: $I_D - V_G$ characteristics measured at V_D = 50 mV at different gate stress biases. Devices were stressed for 4900 s to record the representative negative-bias stress-induced degradation in drain current as a function of gate bias [171].

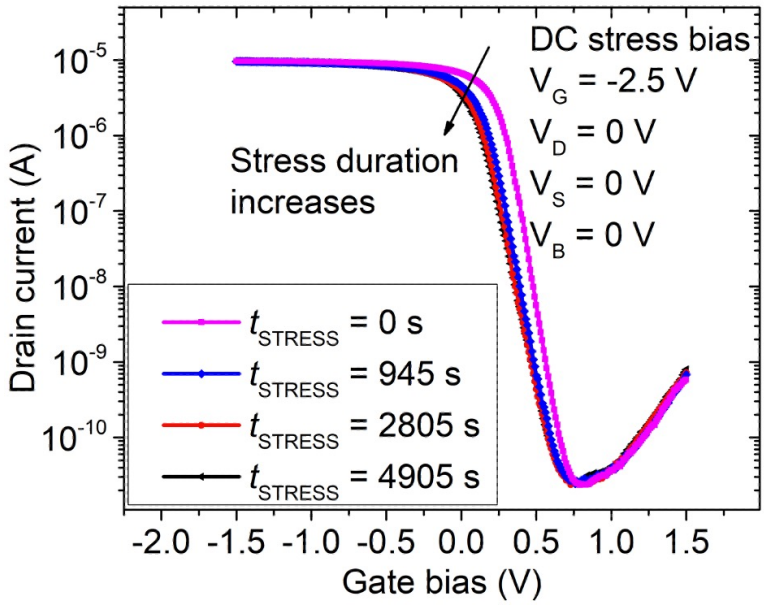

Figure 5.5: $I_D - V_G$ characteristics measured at V_D = 50 mV at different stress times. Devices were stressed at V_G = -2.5 V to capture the representative negative-bias stress-induced degradation in drain current as a function of stress time [171].

The negative bias-stress-induced V_{Th} degradation is plotted in Fig. 5.6 as a function of stress and annealing time. In the stress stage, the worst-case V_{Th} degradation occurs at V_G = -2.5 V.

This initial quick degradation and longer saturation time [99] is typical of nanowire structures. This response is due to the geometry dependence of hydrogen diffusion, which allows faster trap generation at the initial stage of degradation [99], [160]. Moreover, the concentric curvature of the cylindrical capacitance for these devices increases the electric field, thereby increasing the hole density near the interface. As a result, accelerated trap generation is observed due to the increased rate of the reaction-diffusion (RD) process. Also, the self-limiting oxidation process during the nanowire thinning and shaping stage can enhance the oxide trap generation by introducing gate-strain [177], [178]. On the other hand, the limited number of Si-H bonds and a small number of defects in the small gate-area of the thin gate oxide lead to fast (¡ 1000 s) saturation in the V_{Th} shift [160].

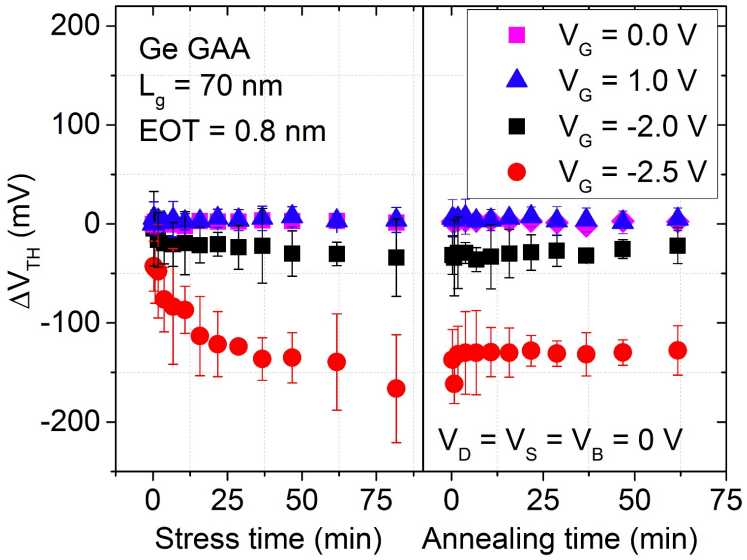

Figure 5.6: V_{Th} shifts at different gate stress as functions of stress and annealing time. The threshold voltages are calculated from $I_D - V_G$ characteristics measured at V_D = 50 mV. Error bars correspond to one standard deviation [171].

There is a small V_{Th} shift for V_G = -2 V, contrasting with larger shifts previously observed in Si, Ge, SiGe, and SiNW devices [99], [101–103, 160], [98], [179]. This improved robustness is attributed to the intrinsic behavior of Ge channel devices with Si/SiO_2/HfO_2 gate stacks [86], [87], [89], [179–181]. Both the increased concentration of Ge in the channel and the smaller thickness of the QW channel push up the Fermi level with respect to the defect band and reduce the negative-bias stress sensitivity. Higher Ge segregation is observed at the Si/SiO_2 due to the thinner Si cap layer in

these devices, relative to those in previous studies [98], [5], due to higher temperature processing. A thin Si cap layer also introduces a larger misalignment of the channel Fermi level with respect to the pre-existing oxide defect energy levels [98]. As a result, fewer defect levels are available for the channel holes confined in the Ge quantum well (QW). Negligible quantum confinement effects were observed in these devices or reported on devices with similar dimensions [182–184].

Negligible V_{Th} shift at $V_G = \pm 1$ V (approximately double the nominal operating voltage $|V_{DD}| = 0.5$ V) demonstrates the device stability during normal operation, indicating no significant leakage current within the operating range. The higher temperature processing increases the interface quality of the as-processed devices; hence, precursor defect (P_{b0}) densities in the thin Si cap layer are reduced. As a result, fewer interface traps (ΔN_{it}) are created during negative bias stress [46]. The reduction in ΔN_{ot} is attributed to an improvement of SiO_2/HfO_2 material quality with increasing process maturity.

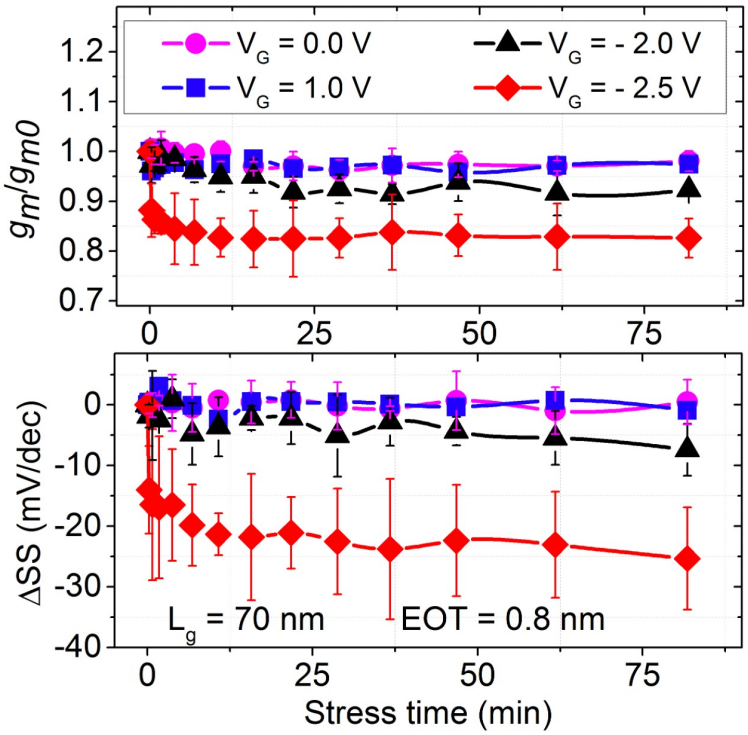

Figure 5.7: Normalized transconductance (G_m) and subthreshold swing (SS) variation at different gate stress as a function of stress time. The G_m and SS are calculated from $I_D - V_G$ characteristics measured at $V_D = 50$ mV. Error bars correspond to one standard deviation [171].

Fig. 5.7 shows the negative bias-stress-induced transconductance and sub-threshold swing degradation obtained from the $I_D - V_G$ curves in Figs. 5.4 and 5.5. When the devices are stressed

with V_G = -2.5 V, the peak G_m decreases by 20% and saturates quickly. This is due primarily to surface scattering events in the channel caused by increased interface and border trap generation [185–187] in the initial stage of degradation. This is consistent with the large initial shift in subthreshold swing *SS* (25 mV/dec) shown in Fig. 5.7.

The contributions of interface traps and oxide trapped charge to the V_{Th} shifts were separated using the subthreshold swing and mid-gap voltage techniques [176]; results are plotted in Fig. 5.8 as functions of stress and recovery time. The NBTI degradation in these Ge GAA nanowire devices is due mainly to interface and border traps (ΔN_{it}) [71], [188], with a small contribution from oxide trapped charge (ΔN_{ot}), unlike results observed in Si/Ge/SiGe devices [99], [101, 102, 160], [98], [189], where contributions from oxide-trap charge are more significant. In the recovery stage, rapid trapped hole annealing and relatively small interface trap passivation are observed. An increasing rate of trapped-hole neutralization is observed, consistent with previous reports on similar dielectric layers [98].

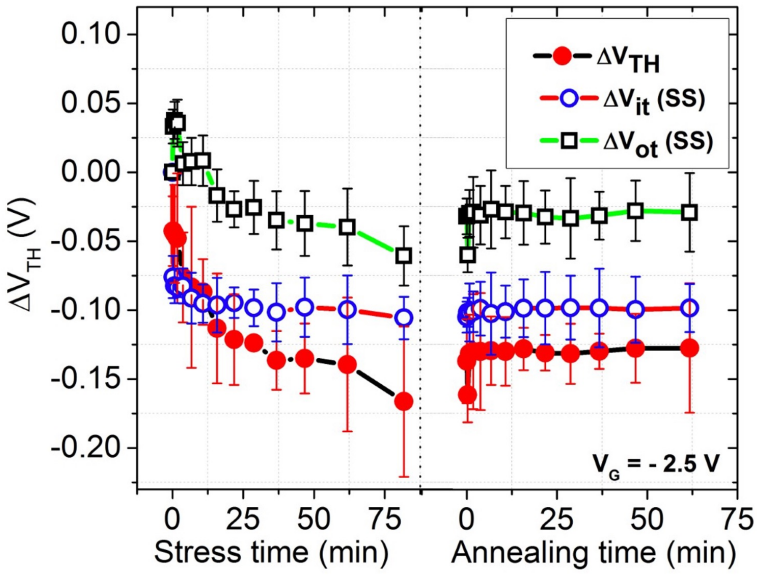

Figure 5.8: Contributions of oxide traps (ΔV_{ot}) and interface traps (ΔV_{it}) to the total V_{Th} shifts, calculated using both the mid-gap voltage shift and *SS* stretch-out techniques and plotted as functions of stress and annealing time. The devices are stressed at V_G = -2.5 V and the V_{Th} shift is calculated from $I_D - V_G$ characteristics measured at V_D = 50 mV. Error bars correspond to one standard deviation [171].

In Fig. 5.9, the time dependencies of trap buildup are illustrated. A time exponent of n $\sim$ 0.25 indicates that interface trap creation due to hydrogen-induced depassivation of Si dangling bonds

dominates the longer-time component of NBTI [98], [189]. The inset shows the estimated stress time required for a 30 mV threshold voltage shift as a function of gate voltage. This quantity is often equated with time to failure (TTF) for a maximum lifetime of 10 years [102]. Further optimization of the gate stack will be required to extend device lifetimes under projected operation conditions of ~ 0.5 V.

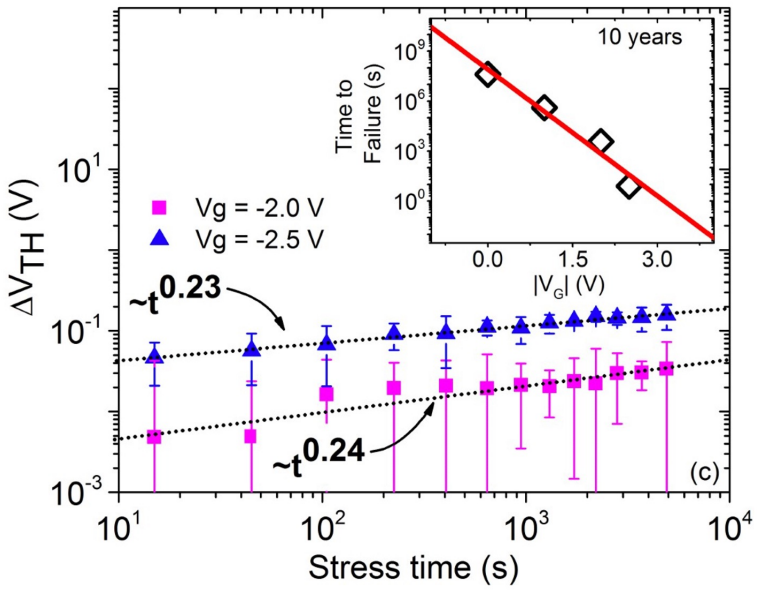

Figure 5.9: Threshold-voltage shift vs. time at two different stress bias conditions. The inset shows the stress time needed to reach a 30-mV threshold voltage shift, often equated with time to failure (TTF). Error bars correspond to one standard deviation [171].

5.3.2 Total ionizing dose effects

Figs. 5.10 and 5.11 illustrate the $I_D - V_G$ characteristics measured at V_D = 50 mV for irradiation biases of V_G = 1 V and -1 V, respectively, for doses up to 1 Mrad(SiO_2). The drain current changes insignificantly after irradiation for both bias conditions, consistent with the changes observed in SiGe/Ge FinFETs [89], [190], and Si GAA NWs [191]. This TID robustness results primarily from the excellent electrostatics and thin dielectric layers in these devices. These factors effectively attenuate the TID-induced charge build-up in the gate dielectric layers. However, the off-state leakage increases due to radiation-induced trapped charges in the shallow trench isolation (STI), which is also observed in SOI bulk and Si FinFET devices [192–195].

An enlarged view of the radiation-induced off-state leakage current is illustrated in Fig. 5.12.

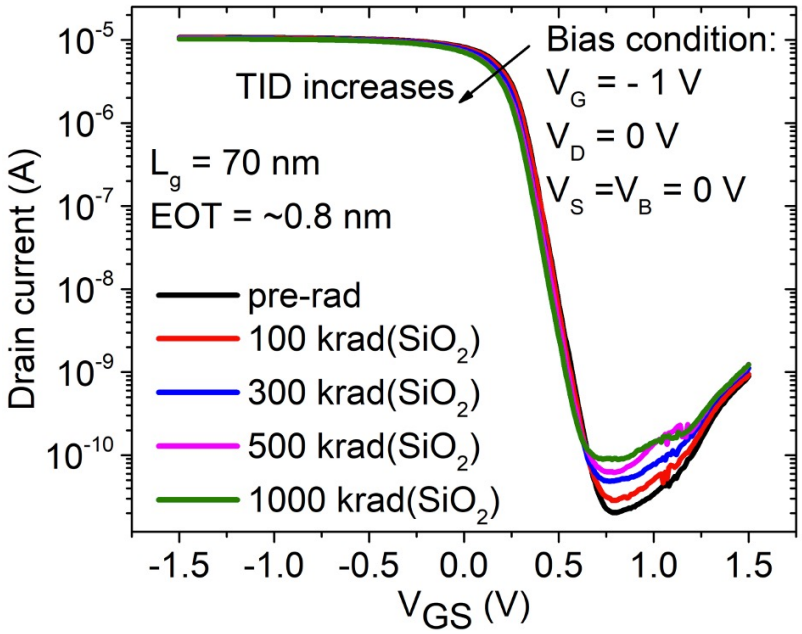

Figure 5.10: Pre- and post-irradiation $I_D - V_G$ characteristics measured at V_D = 50 mV as a function of gate biases. The devices are irradiated with V_G = -1 V and other terminals are grounded [171].

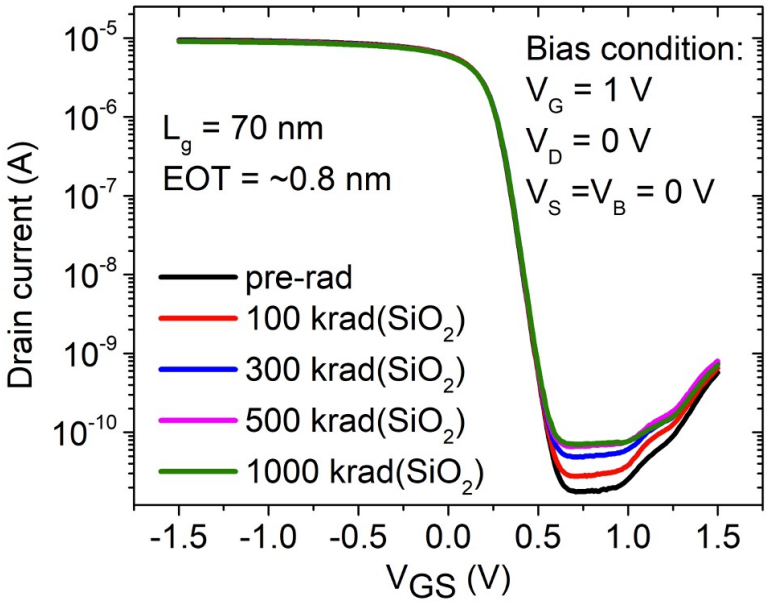

Figure 5.11: Pre- and post-irradiation $I_D - V_G$ characteristics measured at V_D = 50 mV as a function of gate biases. The devices are irradiated with V_G = 1 V and other terminals are grounded [171].

The increase in off-state leakage current contrasts with the relatively constant values exhibited by Ge FinFETs and Si GAA NW devices [190], [191]. This sub-threshold leakage current is due most likely to barrier lowering or gate-induced-drain leakage current (GIDL) as previously noticed in

FDSOI planar [192], [193] devices and bulk-drain junction barrier lowering. In general, the GIDL in nanowire devices originates from the longitudinal band-to-band tunneling near the drain-body junction, which is enhanced by the gate field coupling to the depletion region [196]. This is a characteristic of nanowire conduction since the carriers generated in the gate-overlap region have no conduction path to the substrate. Consequently, the current flow only can pass through the source terminal, as in SOI devices [28]. Bulk-drain junction barrier lowering occurs due to wrapped around gate field coupling near the bulk-drain edge [87].

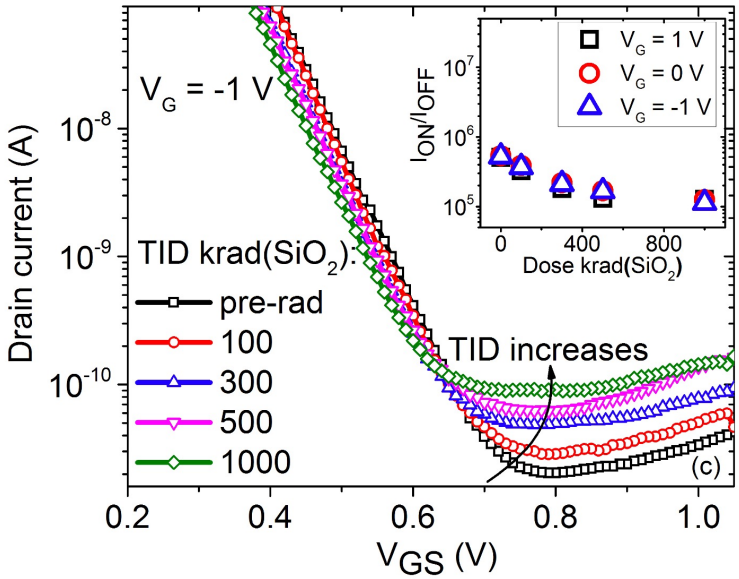

Figure 5.12: Drain current measured at V_D = 50 mV as a function of gate biases for an irradiation bias V_G = -1 V, showing the drain leakage in-creases with increasing total dose. The inset shows the variation of ON/OFF current ratio as a function of TID [171].

In Ge GAA nanowire devices, the increase in charge trapping in the nearby shallow-trench isolation (STI) with increasing TID modulates the channel electric field by electrostatic charge coupling effects [197–201] and bends the energy band sufficiently to accelerate the longitudinal band-to-band (LBTBT) tunneling current [192], [193]. Owing to the larger band gap in Si material compared to Ge, similar band-to-band tunneling does not occur in Si GAA nanowire devices [191]. The TID response due to charge trapping in the STI also depends on the proximity of trapped charges to the active channel, oxide coverage near the trench corner, strength of the lateral gate field effect and sidewall doping [195], [202–207]. The modulated gate field also lowers the bulk-drain junction barrier, enhancing radiation induced junction leakage current. The inset in Fig. 5.12 depicts the

ON/OFF current ratio as a function of total dose, due primarily to the increase in off-state leakage current during irradiation.

Fig. 5.13 shows TID-induced V_{Th} shifts as a function of total dose and annealing time with gate biases of 0 V and ±1 V. Devices were irradiated up to 1 Mrad(SiO_2) and annealed at room temperature for 30 min. The largest V_{Th} shift is observed (less than 30 mV) for negative gate bias during irradiation. This response is comparable to shifts reported for Ge FinFETs [190] and Si GAA NW devices [191]. The extremely thin dielectric gate stack (EOT = 0.8 nm) in the Ge GAA devices decreases the rate of hole trapping by electron tunneling and subsequent neutralization of trapped holes in the oxide and interface [176], [15, 208, 209]. As a result, minimal buildup of radiation-induced oxide, interface, and border traps [71], [188] is observed in these devices. For irradiation under positive gate bias, the small positive shift in V_{Th} is due most likely to electron trapping in the HfO_2/SiO_2 dielectric stack [89], [176], [197], [210]. Negligible V_{Th} recovery occurs during annealing.

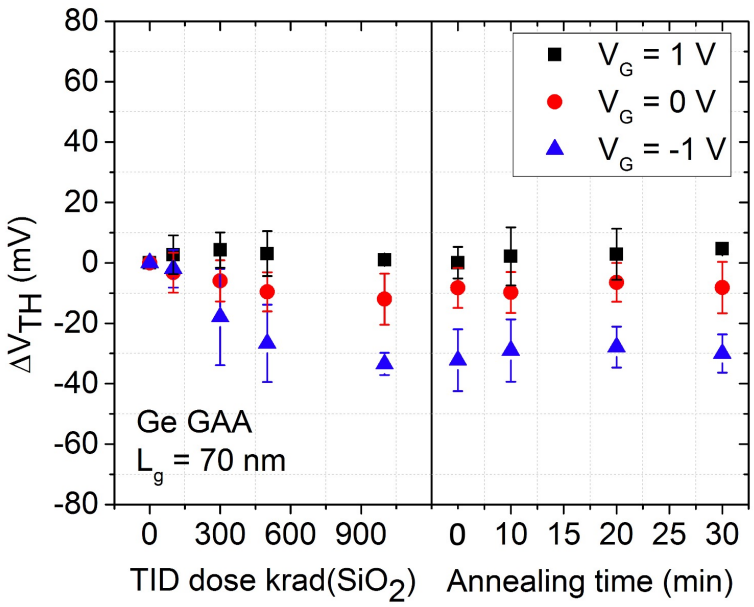

Figure 5.13: Threshold voltage shift ΔV_{Th} as a function of irradiation dose and annealing time. The devices were biased with V_G = 1 V, 0 V, and -1 V during the irradiation. Error bars correspond to one standard deviation [171].

Figs. 5.14 and 5.15 illustrate the degradation of transconductance G_m and subthreshold swing SS (± 2.5 mV/dec) as functions of total dose and annealing time at three different gate biases V_G = +1 V, 0 V, -1 V. For negative gate biases when the devices are irradiated up to 1 Mrad(SiO_2),

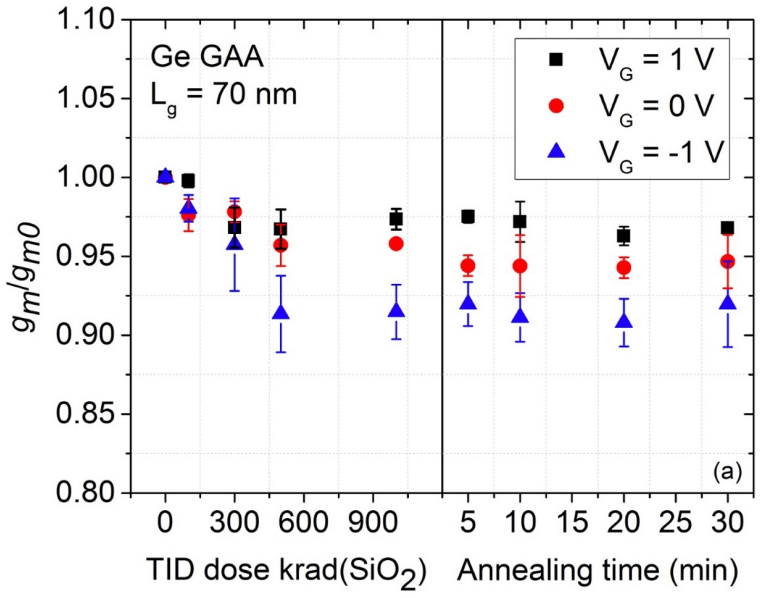

Figure 5.14: Transconductance degradation as a function of irradiation dose and annealing time. The devices were biased with V_G = 1 V, 0 V, and -1 V during the irradiation. Error bars correspond to one standard deviation [171].

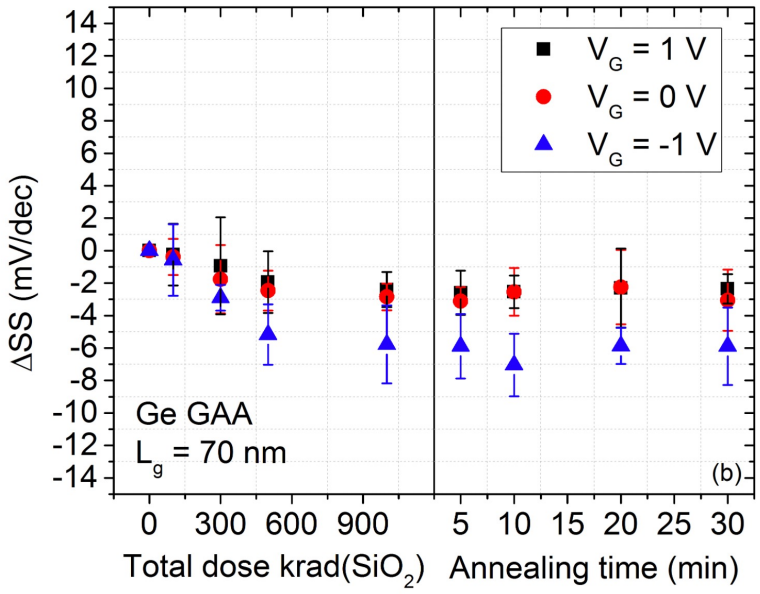

Figure 5.15: Subthreshold slope degradation as a function of irradiation dose and annealing time. The devices were biased with V_G = 1 V, 0 V, and -1 V during the irradiation. Error bars correspond to one standard deviation [171].

the peak transconductance decreases by ∼8%, indicating increased scattering at the surface due to interface and border trap generation [185–187]. The peak transconductance degradation in these Ge

GAA devices is consistent with the shifts observed in Ge FinFET and Si GAA devices [190], [191]. The channel conductance shift affects the subthreshold swing [211]. The *SS* degradation is plotted in Fig. 5.15, showing a shift of ∼5 mV/dec for negative gate bias. For positive gate bias, there are almost no changes in peak G_m and *SS* due to negligible interface and border trap formation. No peak G_m and *SS* shift recovery occur during annealing.

5.4 Summary and Conclusions

The Ge GAA nanowire devices examined here have improved negative bias-stress responses compared to previous generations of Ge/SiGe pMOS and pFinFETs; the observed degradation is due primarily to interface and border traps. The excellent electrostatic control over the channel and the ultra-thin gate oxide reduces radiation-induced charge trapping in the dielectric layers of these devices, but the off-state leakage current increases, most likely because of gate-induced drain leakage current. These results are highly encouraging for the future use of Ge GAA devices in space and other high-radiation environments.

CHAPTER 6

Conclusion

This dissertation investigates the response of Ge-channel devices to radiation effects and illustrates new findings. Firstly, it focuses on understanding the single-event-induced charge collection in Ge-channel FinFET devices. The Ge-FinFET devices are fabricated by imec with complex high-k gate stack and metal gate architecture, which motivates to choose this device. Large feature size device with gate length (as drawn) L_G = 120 nm, fin length L_F = 1 μm, fin width W_F = 100 nm, fin height H_F = 15 nm, and number of fins N_F = 4, were tested to get a better idea about the SE-induced charge collection mechanisms. Both heavy-ion experiments and pulsed laser tests were used in this work. In general, heavy-ion experiments allow energetic ions similar to ions found in space environment, to strike the devices. Therefore, people are more interested in heavy-ion results. On the other hand, pulsed laser-induced single event transient (SET) tests are nondestructive and low-cost methods to study SEE in semiconductor devices and circuits. Despite the difference in charge generation and deposition mechanism compared to heavy-ion tests, laser tests are widely used to characterize SEE in devices. Moreover, laser sources also can be optimized both for two-photon (TPA) and single-photon (SPA) absorption tests. 3-D TCAD simulations of single event transients were also performed by using the heavy-ion model in Sentaurus TCAD. Boltzmann statistics, bandgap narrowing, doping-dependent mobility, Shockley Read Hall (SRH) recombination, and avalanche generation have been included in the model to investigate different phenomena of charge collection by varying the bias conditions, heavy-ion profiles, and carrier lifetime, etc.

The experimental results and the simulation data confirm that the single-event charge collection behavior in Ge-channel p-type FinFETs depends strongly upon gate bias, as well as on heavy-ion or pulsed-laser strike location. The resultant transient is a combination of a sharp peak coming from drift current and a slower tail resulting from diffusion current. The sharp peak occurs immediately after the heavy-ion strike due to a transient shunt effect which does not depend on the gate bias. As a result, the peak transient current does not show any gate bias dependence. After the drift current in the channel is "quenched" by the gate, increased charge collection comes only from the slower tail of the transient. As a result, the total collected charge changes dramatically with gate bias.

Unlike SiGe pFinFETs and planar Ge, the strike location dependence of transient current polarity inversion was not observed for drain transient. The improved SE robustness of Ge pMOS FinFETs compared to planar SiGe and Ge pMOS devices are due primarily to the significant improvement of gate control of Ge-FinFETs over planar devices.

The LET distribution of proton-induced recoil ions in Ge-channel pFinFET devices is also explored in this thesis using Gean4 simulation. The multi-layered gate stack is irradiated with different proton energies and the key differences in LET of proton-induced recoil ions in Ge with Si are illustrated. The representative results show that the population and the species of secondary recoil ions in Ge vary significantly, giving a LET value of 23 MeVcm^2/mg, exceeding the maximum LET observed for Si (15 MeVcm^2/mg). The presence of high-Z elements (W) in Ge channel devices extends the maximum LET value up to 35, resulting from high-Z recoil ions generated in W.

Finally, this work investigates the negative bias-stress and TID effects in deeply scaled strained Ge GAA nanowire pFETs using accelerated stress test and X-ray irradiation respectively. The Ge GAA pFinFETs were fabricated at imec on a 300 mm $Si_{0.3}Ge_{0.7}$ strain relaxed buffer (SRB) by adapting the FinFET process used for SE-induced charge collection experiments. Each device has four fins with two vertically stacked NWs per fin, with a diameter of 11 nm. The experimental results and comprehensive analysis reveal that the negative bias-stress-induced degradation in Ge GAA devices mainly originates from interface-trap and border-trap generation. Because of the cylindrical nature of GAA nanowire devices, the electric field is more concentrated. As a result, trap generation occurs rapidly, and quick saturation is observed. During the recovery stage, hole de-trapping is also noticed. The GAA nanowire devices exhibit excellent electrostatic control over the gate as compared to other counterparts. Therefore, their TID robustness improves significantly. Moreover, the ultra-thin gate oxide reduces radiation-induced charge trapping in the dielectric layers of these devices. Unlike Si GAA nanowire devices, the off-state leakage current in Ge channel pFinFET devices most likely results from gate-induced drain leakage current. These results are highly encouraging for the future use of Ge GAA devices in space and other high-radiation environments.

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