BIAS AND THRESHOLD-VOLTAGE DEPENDENCIES OF SINGLE-EVENT UPSETS IN A 7-NM BULK FINFET TECHNOLOGY

By

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CHAPTER 1

Introduction

Power consumption is a perennial concern for integrated circuit (IC) designers, and this has only become more true since the end of Dennard scaling [2]. Without the ability to rely on constant power density in MOSFETs, designers must carefully consider issues related to power dissipation accompanying smaller sizes and faster clock frequencies. This dilemma is especially apparent in space-bound systems, where power dissipation is restricted due to limited resources. Even in terrestrial applications, heat dissipation can be significant (latest ASIC design with 19 billion transistors dissipates approximately 700 watts in a 1 cm^2 area) and requires designers to use low-power approaches whenever possible. One possible solution to this problem is reducing the supply voltage for noncritical paths or whenever high performance is not a primary concern, as doing so decreases both dynamic and static power consumption [3]. Another common approach is to provide multiple threshold-voltage (V_T) options for any given fabrication process so that designers can compromise between performance and power as necessary. Raising the threshold voltage only decreases static power consumption, but static power becomes a more daunting concern with each new technology node due to the increasing contribution from subthreshold leakage, so most modern commercial processes offer these options.

While these techniques may help alleviate power concerns in many cases, they cannot be naïvely used in all designs. In addition to performance tradeoffs, if ionizing radiation is a concern, as it is for advanced technologies and in many space and medical applications, the matter of power consumption cannot be considered in a vacuum because both supply voltage and V_T can impact a circuit's single-event (SE) response. For space applications, this challenge has historically been

accounted for by using parts specifically qualified for use in space, made with carefully designed circuitry and often using specialized process nodes that were typically a few generations behind the cutting edge, but that is not always the case anymore. The rapid growth of the private space industry has driven demand for faster and cheaper spacecraft development, which in turn has led to an increasing interest in the use of commercial-off-the-shelf (COTS) parts due to their superior performance and lower cost compared to space-grade parts [4] [5] [6]. These parts are not made in a specialized, radiation-hard process, but their SE response must be investigated in order to gauge their suitability for use in space. In medicine, radiotherapy has similar requirements for radiation-hardened circuitry, although total dose is typically more of a concern than single-event effects (SEEs), as most radiotherapy uses photons rather than ions [7]. Yet this too may be changing, as there is an interest in increasing the availability of heavy-ion-based treatment options [8] [9], which would require an analysis of SEE vulnerability.

Previous research has shown that lowering supply voltage increases a circuit's susceptibility to single-event upsets (SEUs) and that this effect has been exacerbated by the introduction of multi-gate transistor architectures [10] [11] [12] [13] [14]. Previous works have also analyzed the impact of V_T options on SEU response for 28-nm planar, 20-nm planar, and 16-nm FinFET technologies [15] [16], but the scaling trend is not as clear-cut as the supply voltage trend. These results show that SE response of identical flip-flop (FF) designs can vary greatly between different technologies, requiring similar analysis with the advent of each new technology node.

This work presents one such analysis on the SE responses of D-flip-flop (DFF) designs with all available V_T options in a commercial 7-nm bulk FinFET technology node as a function of supply voltage and particle Linear-Energy-Transfer (LET) values. Alpha-particle and heavy-ion

results show that, unlike in older FinFET processes, V_T options have practically no effect on SEU response in this technology under nominal conditions; however, the inclusion of supply voltage variation reveals that, when subject to lower biases and higher-LET particles, SEU vulnerability is proportional to threshold voltage. This trend can be explained most easily by a limitation on the efficiency of charge collection from the substrate resulting from the structure of bulk FinFETs, a mechanism predicted and simulated in other works [17] [18]. In the subsequent chapters, after an explanation of relevant background information, the experiment from which these results were obtained is detailed, followed by supporting simulations, and finally the results themselves and an analysis of them.

CHAPTER 2

Background

2.1. Single-Event Transients and Upsets

When a semiconductor material is struck by electromagnetic radiation, it can absorb energy, which can excite an electron from the valence band to the conduction band, leading to the generation of electron-hole pairs (EHPs). The threshold energy required for EHP creation depends on the bandgap energy of the irradiated material. The bandgap of silicon is approximately 1.1 eV, but some of the energy from the incident particles is absorbed as heat, so the threshold energy to create an electron-hole pair in silicon is about 3.6 eV [19].

A simple example of this type of charge generation is a solar cell. A solar cell can be modeled as a simple diode exposed to light. Photon strikes on the diode's p-n junction generate EHPs as described above, which in turn generates current flow [20]. This current has two components: (1) a prompt component resulting from the drift of carriers generated in the depletion region due to the built-in potential of the junction, and (2) a delayed component resulting from the diffusion of carriers generated outside the depletion region to the junction [21]. Drift refers to the movement of charge carriers due to an electric field, and diffusion refers to the movement of charge carriers due to against the gradient of the carrier concentration. Although this current is desirable in a solar cell, all reverse-biased p-n junctions are sensitive to this effect, and it is usually undesirable in turned-off transistors. The similarity in structure between a solar cell and a regular planar MOSFET is illustrated in Figure 2.1.

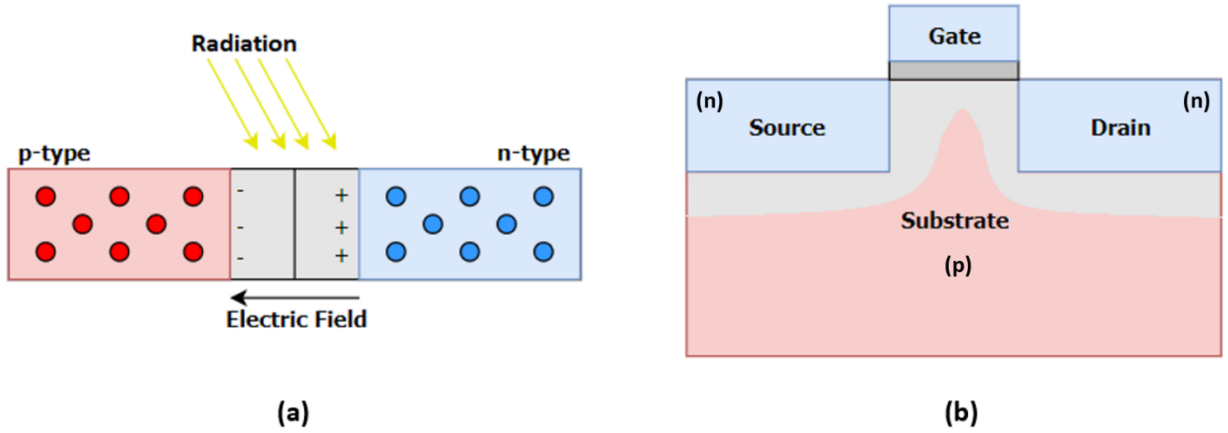


Figure 2.1: Illustration of the similarities between (a) a solar cell and (b) a transistor. The n-type semiconductor is shown in blue, the p-type in red, and the depletion region in gray.

The same charge-collection mechanism can be observed if a semiconductor material is struck by a single energetic particle rather than by light, in which case the resulting voltage transient is called a single-event transient (SET), and the associated current transient is called the ion-hit current or SET current. The EHPs can be generated either directly or indirectly by the particle. In the case of direct ionization, a charged particle penetrates the material, imparting its energy to trapped electrons as it travels, which in turn forms a charge track of free EHPs [22], as shown in Figure 2.2. In the case of indirect ionization, a particle penetrates the material and collides with the nucleus of an atom within the device; this collision causes a nuclear reaction, the charged products of which may cause direct ionization [23]. Regardless of whether they form from direct or indirect ionization, the EHPs generated by an ion-strike may be collected by the p-n junctions within a transistor via drift and diffusion exactly as described for solar cells. Figure 2.2 shows the ion-hit current waveform corresponding to an SET caused by direct ionization and an illustration of the associated charge collection mechanisms. SETs only last at a node for a very short time (on the order of picoseconds in modern devices), but their effects are not necessarily as short-lived.

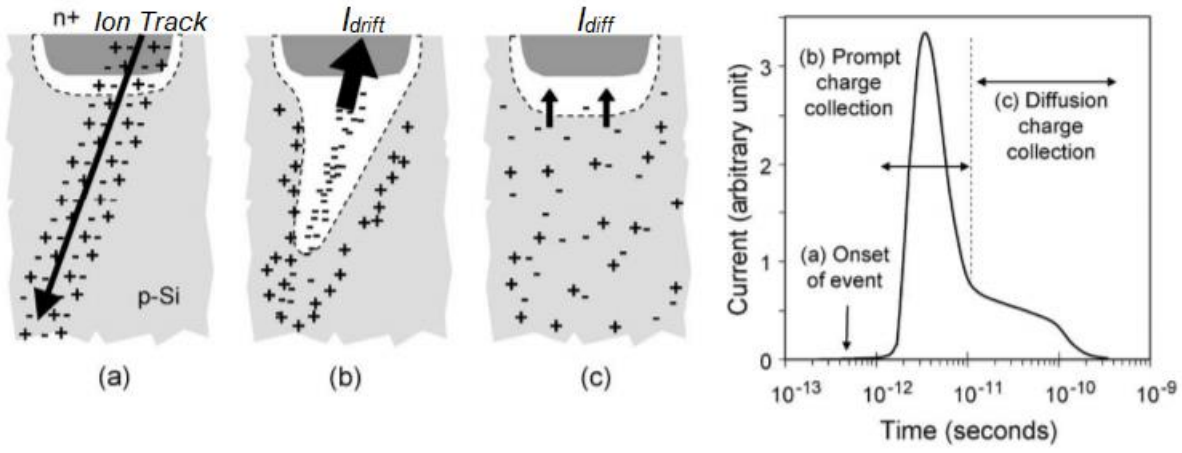


Figure 2.2: Illustrations of the steps of SET generation and the resulting SET waveform. (a) Charge track left behind by a heavy ion. (b) Drift/prompt current. (c) Diffusion/delayed current. From [24].

Transient voltages are not errors in and of themselves, but they can possibly cause errors if they change the state of the circuit in some way. For instance, if an SET occurs at a vulnerable combinational logic node and has sufficient magnitude, it is possible that it will cause an erroneous voltage value to propagate to a latch. If a latch error occurs due to the storage of an SET pulse or a single particle strike to a semiconductor region contained within the latch itself, it is called a single event upset (SEU). In a digital system, SET pulse propagation can be impeded in various ways, such as attenuation as it passes through logic gates (electrical masking), missing a latch's setup and hold time requirements (temporal masking), and the rejection of the erroneous signal at a logic gate as the result of the gate's other inputs (logical masking) [25]. If the voltage pulse is not masked by one of the above methods, it may be stored in the latch as erroneous data. As a general rule, an SET with a pulse width (PW) greater than the feedback-loop delay (FD) of a latch will cause an SEU, assuming the generated voltage transient has sufficient amplitude to be stored in the latch. FD is the time required for a signal to propagate through the feedback loop of a latch,

and it is typically equal to two inverter delays (2τ) for standard DFFs, as illustrated in Figure 2.3. FD will be different for different FF designs.

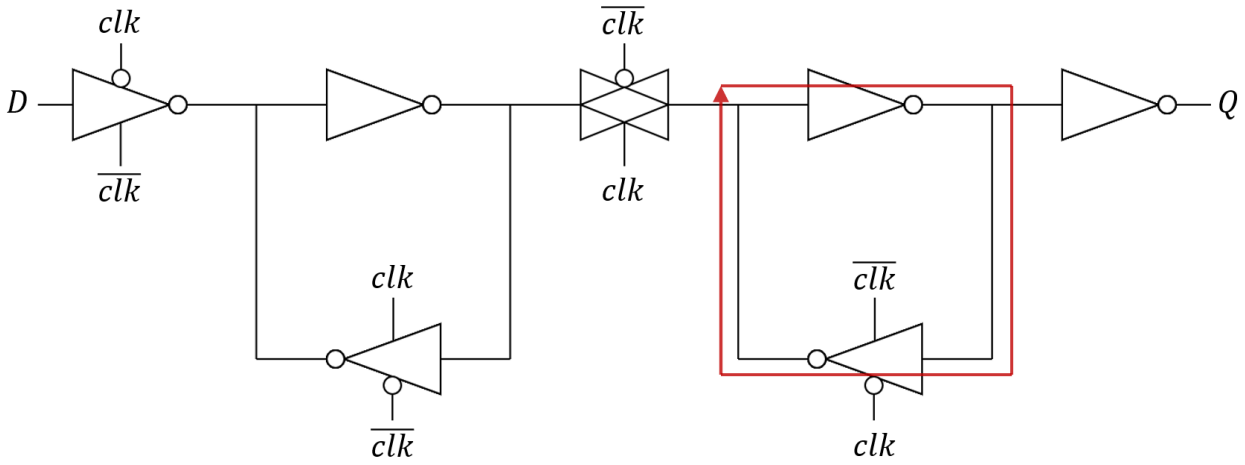


Figure 2.3: Illustration of feedback-loop (red) in a DFF. If an incorrect voltage at the input of one of the inverters in this loop lasts long enough, it can cause an incorrect output that propagates to and through the second inverter, causing the initial incorrect voltage to be maintained.

2.2. FinFET Structure

A key aspect of the technology analyzed in this work is that it is a bulk FinFET node, rather than a planar MOSFET node. A FinFET is a multi-gate transistor in which the channel is formed within a narrow fin of silicon that is surrounded by the gate [26], rather than beneath the gate as in a planar transistor. Figure 2.4 shows these two types of transistors side-by-side for comparison. By wrapping the gate in this way, the channel is controlled on three sides, allowing for excellent current control. This additional current control translates to increased drive current, improved switching characteristics, lower leakage, and superior performance at lower supply voltages compared to planar transistors [27] [28]. This structural difference between FinFETs and planar

transistors also impacts SE mechanisms. In a bulk FinFET, the only path to the substrate is through a narrow neck region, which makes charge collection much less efficient than in planar MOSFETs, where the source and drain are fully within the substrate/well [17]. This is illustrated in Figure 2.4, which shows how charge deposited in the substrate can freely diffuse to the drain in the in planar structure, but charge must diffuse through the neck region in the FinFET structure because all other paths are blocked by the shallow trench isolation (STI).

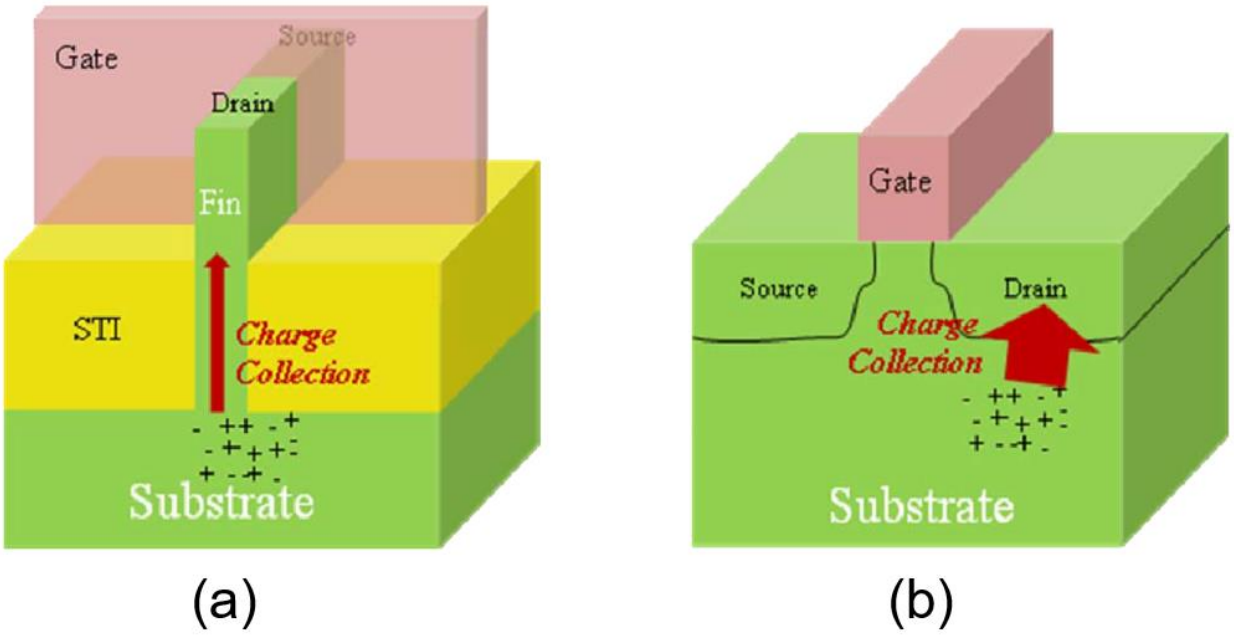


Figure 2.4: Comparison of (a) FinFET and (b) planar structures. From [29].

2.3. Designing for Low-Power

As mentioned previously, minimizing power dissipation is paramount in modern circuit design, but before one can do so, power dissipation must be clearly defined. The total power dissipation for a device (P_{tot}) is estimated by the following equation [30]:

$$P_{tot} = P_{dyn} + P_{stat} + P_{dp}$$

where P_{dyn} is the dynamic power consumption due to capacitance charging and discharging, P_{stat} is the static power consumption due to leakage current, and P_{dp} is the direct-path power consumption due to the brief short-circuit between power and ground during switching. Assuming full rail swing, these terms can be further broken down as follows [30] [3]:

$$P_{dyn} = A \cdot f \cdot C_L \cdot {V_{DD}}^2$$

$$P_{stat} = I_{LEAK} \cdot V_{DD} \approx I_{sub} \cdot V_{DD}, \qquad I_{sub} \propto e^{\frac{-V_T}{nKT/q}}$$

$$P_{dp} = t_{sc} \cdot f \cdot I_{SC} \cdot V_{DD}$$

where A is the probability of a clock signal causing a power-consuming event, f is the clock frequency, C_L is the load capacitance, V_{DD} is the supply voltage, I_{LEAK} is the leakage current, I_{sub} is the subthreshold leakage, $\frac{nKT}{q}\ln(10)$ is the subthreshold swing, V_T is the threshold voltage, t_{sc} is the time period of the switching short, and I_{SC} is the short-circuit current.

With these equations as reference, the power benefits of lowering supply voltage and raising V_T become clear. P_{dyn} depends quadratically on supply voltage, and P_{dp} shows a linear dependence. As for P_{stat}, subthreshold conduction tends to dominate leakage current in modern circuits, and it decreases exponentially as V_T increases. Of course, there are limits as to how much these values can be controlled. The saturation/drive current of a field-effect transistor can be given as [30]:

$$I_D = \frac{1}{2} k' \frac{W}{L} (|V_{GS}| - |V_T|)^2$$

where k' is a process parameter, $\frac{W}{L}$ is the size ratio, and V_{GS} is the gate-to-source voltage. $|V_{GS}|$ is often just V_{DD}, especially in digital circuits, so by decreasing supply voltage and increasing V_T, the current available for charging and discharging capacitors in CMOS circuits also decreases, leading to increased delays. Oftentimes, this tradeoff can be addressed locally, and one can use lower supply voltages and higher threshold voltages in subcircuits with relatively lenient timing requirements. In the case of FinFETs, this option is very appealing due to their excellent performance at low supply voltages, which in turn provides enhanced design flexibility.

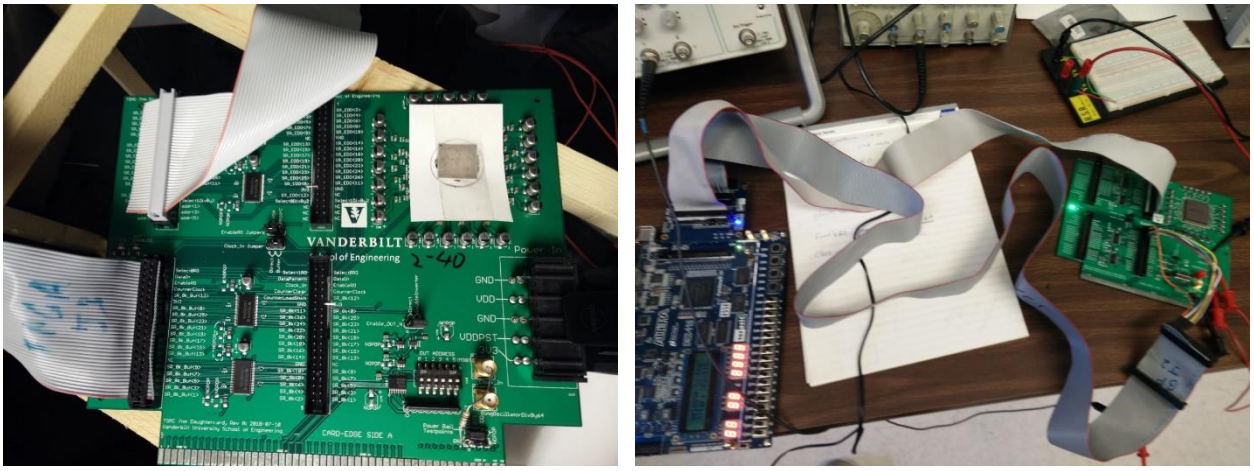
In addition to power consumption, SET PW and FF FD are also strongly related to the chosen V_T option for a logic gate. When an SET occurs at the output of a standard CMOS logic gate, at least one transistor should be biased on, acting as a pull-up or pull-down transistor trying to restore the perturbed node to its proper value. How effectively the node can be restored depends on the how quickly this transistor can sweep away excess charge carriers, and the rate at which this occurs is the transistor saturation current. As drive/saturation current increases, PW decreases because the node is restored more quickly. This relates V_T and SE cross-section because increasing V_T decreases drive/saturation current, as shown by the I_D equation above, resulting in an increase in SET PW and a corresponding increase in SE cross-section. Increasing V_T also increases FF FD due to the heightened gate delays, resulting in a decrease in SE cross-section. These two competing factors are typically the main determinants of the overall SEU response for a given V_T option [31]. If average PW increases faster than FD as V_T increases, SEUs should become more likely because it becomes more likely that the SET PW will be longer than FD; the opposite is true if average FD increases faster.

CHAPTER 3

Experimental Details

3.1. Test Circuit

The test circuit consists of three separate 1 mm × 2 mm die, each fabricated in a commercial 7-nm bulk FinFET technology. Each die contains shift registers with either 24K or 32K stages, and each stage of these shift registers contains one DFF design. For this study, shift registers consist of identical DFF layout and schematic designs but use different V_T options. All transistors used in these designs were two-fin transistors. The V_T options available at this technology node are standard threshold voltage (SVT), low threshold voltage (LVT), and ultra-low threshold voltage (uLVT). This test circuit is shown on a test board in Figure 3.1.



(a) **(b)**

Figure 3.1: Images of (a) a close-up of the test board and (b) the test board connected to an FPGA for alpha-particle testing.

The overall design for the test circuit applies the Circuit for Radiation Effects Self-Test (CREST) [32] architecture, as shown in Figure 3.2. Whenever a DFF in one of the shift registers is upset, the flipped bit propagates through the register and is tallied by the error counter when it does not match the output expected from the input data source. On-chip error checking and clock generation was used during tests to minimize external error. All circuitry that is not part of the shift registers utilizes triple-modular redundancy (TMR) to guard against the counting of spurious errors. All error bars in this paper were calculated using either Gaussian standard error [33] corresponding to a double-sided Poisson confidence interval of 1 σ or, in cases where less than ten errors were counted, Poisson counting statistics. This approach is reasonable because if the error count is larger than ten, then the 1-σ Gaussian-statistics limit approximates both the upper and lower Poisson-statistics limits with at least single-digit-percent accuracy [34].

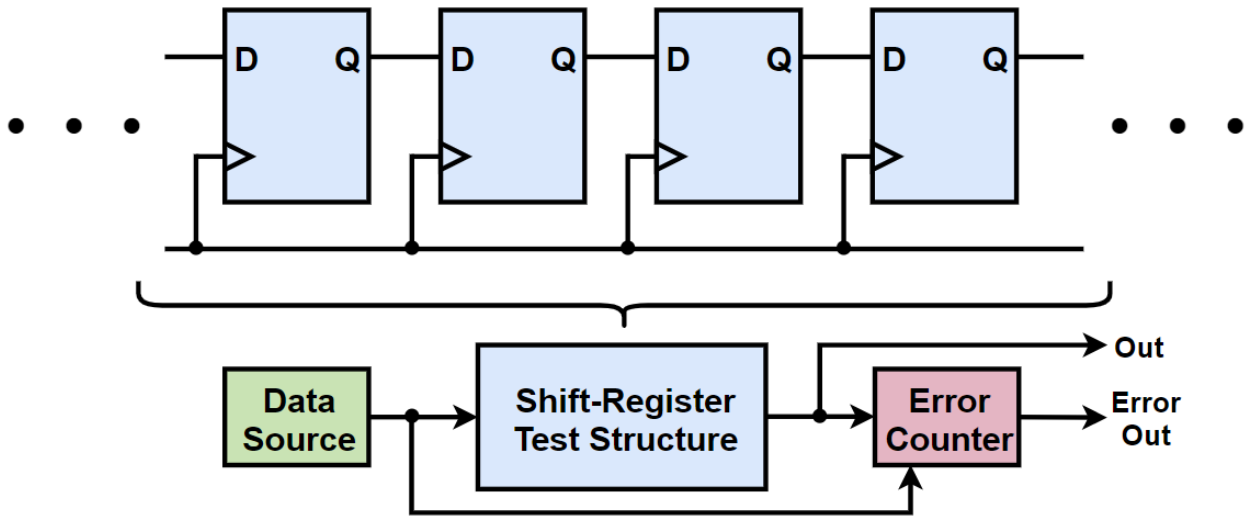


Figure 3.2: Block diagram of CREST configuration used in SEU test circuit. After [35].

3.2. Heavy-Ion Tests

All heavy-ion tests were performed at the Lawrence Berkeley National Laboratory (LBNL) with a 16 MeV/nucleon cocktail, the components of which are shown in Table 3.1, with values calculated using SRIM. The particle LET values ranged from 1.16 MeV-cm^2/mg (Nitrogen) to 24.98 MeV-cm^2/mg (Krypton). Particle fluence ranged from 4×10^7 to 9×10^7 particles/cm^2.

These tests were carried out in vacuum, at normal incidence, and at room temperature. During the tests, the shift registers were given an input of "0" and clocked at a frequency of 2.5 MHz. Keeping the input voltage for the shift registers at 0 V during the tests prevents ion hits within the clock tree from resulting in upsets because a high value cannot be written to a flip-flop due to a spurious high clock signal, ensuring that all upsets observed are due to ion hits within a latch cell. Choosing 2.5 MHz for the frequency reduces probability of an upset due to ion hits on transparent stage of the FF. For different tests, supply voltage was varied from 750 mV (nominal value) to 450 mV.

Table 3.1: 16 MeV/Nucleon Cocktail Components [36]

Ion	Energy (MeV)	LET (MeV-cm^2/mg)	Range$_{Max}$ (μm)
$^{14}N^{+5}$	233.75	1.16	505.9
$^{20}Ne^{+7}$	321.00	2.39	347.9
$^{29}Si^{+10}$	452.10	4.58	274.3
$^{40}Ar^{+14}$	642.36	7.27	255.6
$^{78}Kr^{+27}$	1225.54	24.98	165.4

3.3. Alpha Tests

Alpha particle tests were performed at Vanderbilt University using a 1 cm × 1 cm ^{241}Am foil source positioned less than 1 mm away from the die, in accordance with the JESD89 standard [37]. The results in this paper come from tests conducted at room temperature with particle flux of 1000 alpha/mm^2/s. These particles were estimated to have an LET value of 0.5 MeV-cm^2/mg. As with the heavy-ion tests, the shift registers were given an input of "0" and clocked at a frequency of 2.5 MHz. Supply voltage was varied between 750 mV and 350 mV.

CHAPTER 4

Simulations

4.1. Schematic Simulations

Single-event transient (SET) pulse width (PW) and DFF feedback-loop delay (FD) were estimated for different V_T options and supply voltages using simulations with a 7-nm process design kit (PDK). The simulations used a double-exponential current pulse to represent an alpha-particle-induced SET pulse. As mentioned earlier in Section 2.1, it can generally be assumed that an SET with PW greater than the FD will cause an upset in a latch if the transient voltage is of sufficient magnitude. As further discussed in Section 2.3, increasing V_T tends to increase both SET PW and FF FD, resulting in conflicting effects on SE cross-section. Which of these factors changes faster typically determines how SE response varies across different V_T options. For the 7-nm node, Figure 4.1 shows the relative comparison of SET PWs for different V_T options along with FD as a function of supply voltage. The figure shows that both SET PW and FD change significantly with V_T, but both factors scale relatively similarly.

Compared to the 16-nm simulation results (from [16]) for nominal supply voltage (Table 4.1), these results not only have relatively smaller differences between the rates with which PW and FD increase as a function of V_T, but also which rate is higher is inconsistent across V_T options. These results suggest that all three V_T options should show similar SE cross-section values, which is consistent with the alpha data, shown in CHAPTER 5. While these schematic-level simulations are useful for modeling first-order circuit effects, a basic current source does not account for other factors that can affect the SET's characteristics, such as volatile bias conditions during an SE and

structural effects of the FinFET geometry. For a better understanding of the physical and temporal effects of a bulk FinFET processes, additional simulations are necessary.

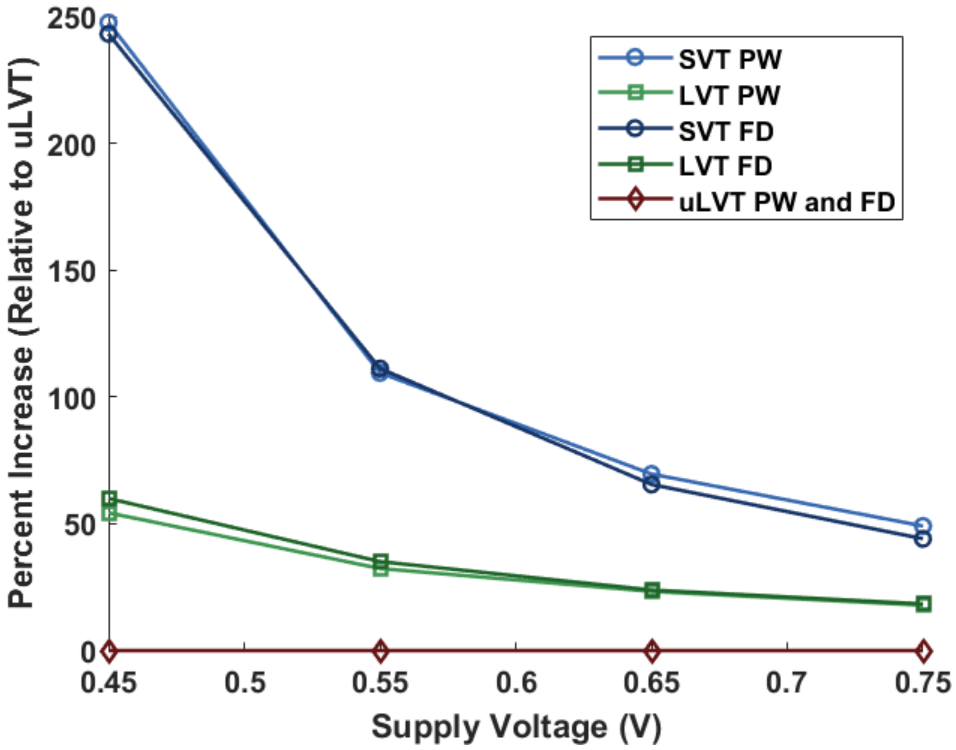


Figure 4.1: Simulated percent increase (relative to uLVT) in pulse width and feedback-loop delay for V_T options as a function of supply voltage.

Table 4.1: Simulated Percent Increase in Pulse Width and Feedback-Loop Delay Relative to uLVT at Nominal Voltage

7-nm	SVT	LVT	uLVT
PW	49.1%	17.9%	0%
FD	44.1%	18.4%	0%

(a)

16-nm	SVT	LVT	iLVT	uLVT
PW	116.5%	61.6%	37.0%	0%
FD	78.9%	36.0%	15.6%	0%

(b)

4.2. TCAD Simulations

A 3D technology computer-aided design (TCAD) model of a 7-nm bulk FinFET inverter, shown in Figure 4.2, was developed in the Synopsys Sentaurus suite of TCAD tools, version K-2015.06 [38], based on material described in published literature for the fin dimensions and WELL dopings [39] [40] [41].

Mixed-mode ion-strike simulations were run for two variants of the inverter, a uLVT and an SVT, for supply voltages of 0.45 V and 0.75 V. The ion-strikes simulated were direct strikes at the center of one fin in the OFF-NMOS transistor and indirect strikes at a location 100 nm away from this fin. Both types of strikes were at normal incidence, and the ion charge deposition model is Gaussian both spatially (10 nm radius) and temporally (0.5 ps) [42]. The simulated SETs for a particle with a low LET value of 1 MeV-cm^2/mg are shown in Figure 4.3(a)(b), and the SETs for a particle with a high LET value of 25 MeV-cm^2/mg are shown in Figure 4.3(c)(d); the drain currents of the NMOS transistor and the restoring saturation currents of the PMOS transistor (dotted lines) for the same simulations are shown in Figure 4.4.

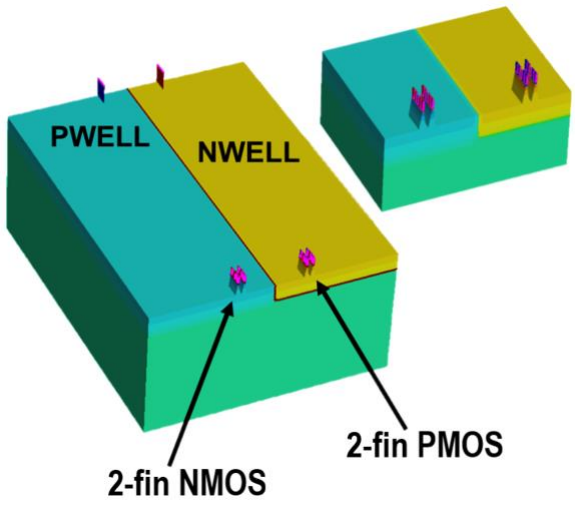


Figure 4.2: 3D TCAD model of a 7-nm bulk FinFET inverter used for SET simulations. The strike location for all simulations was the center of one of the NMOS fins.

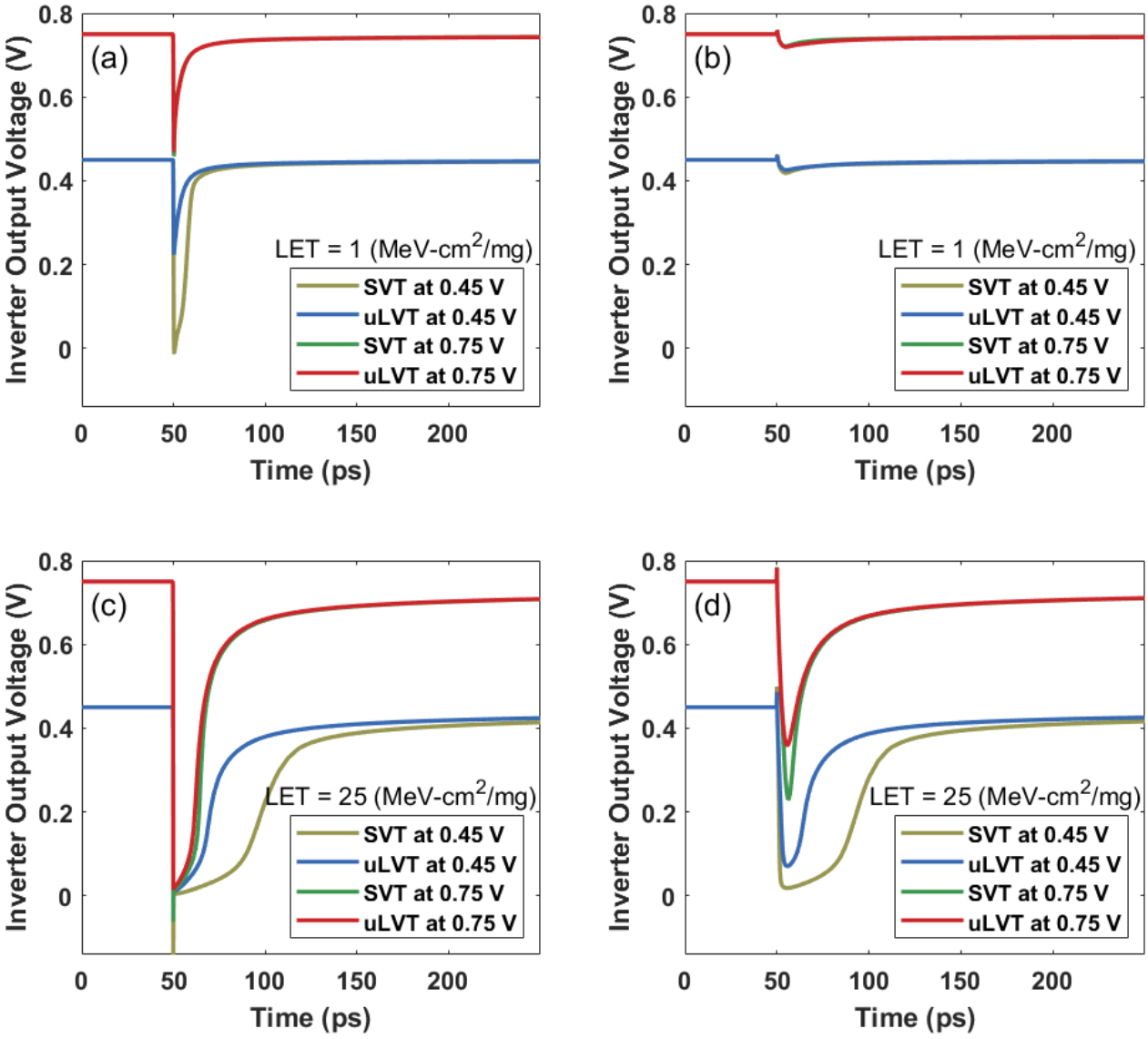


Figure 4.3: Output voltage of inverter from TCAD simulations of SET pulses generated by particle strikes located (a & c) directly at center of fin and (b & d) 100 nm away from fin. Simulations were performed for particles with (a & b) LET = 1 MeV-cm^2/mg and (c & d) LET = 25 MeV-cm^2/mg. Each simulation tested high and low V_T options as well as nominal (0.75 V) and reduced (0.45 V) supply voltages.

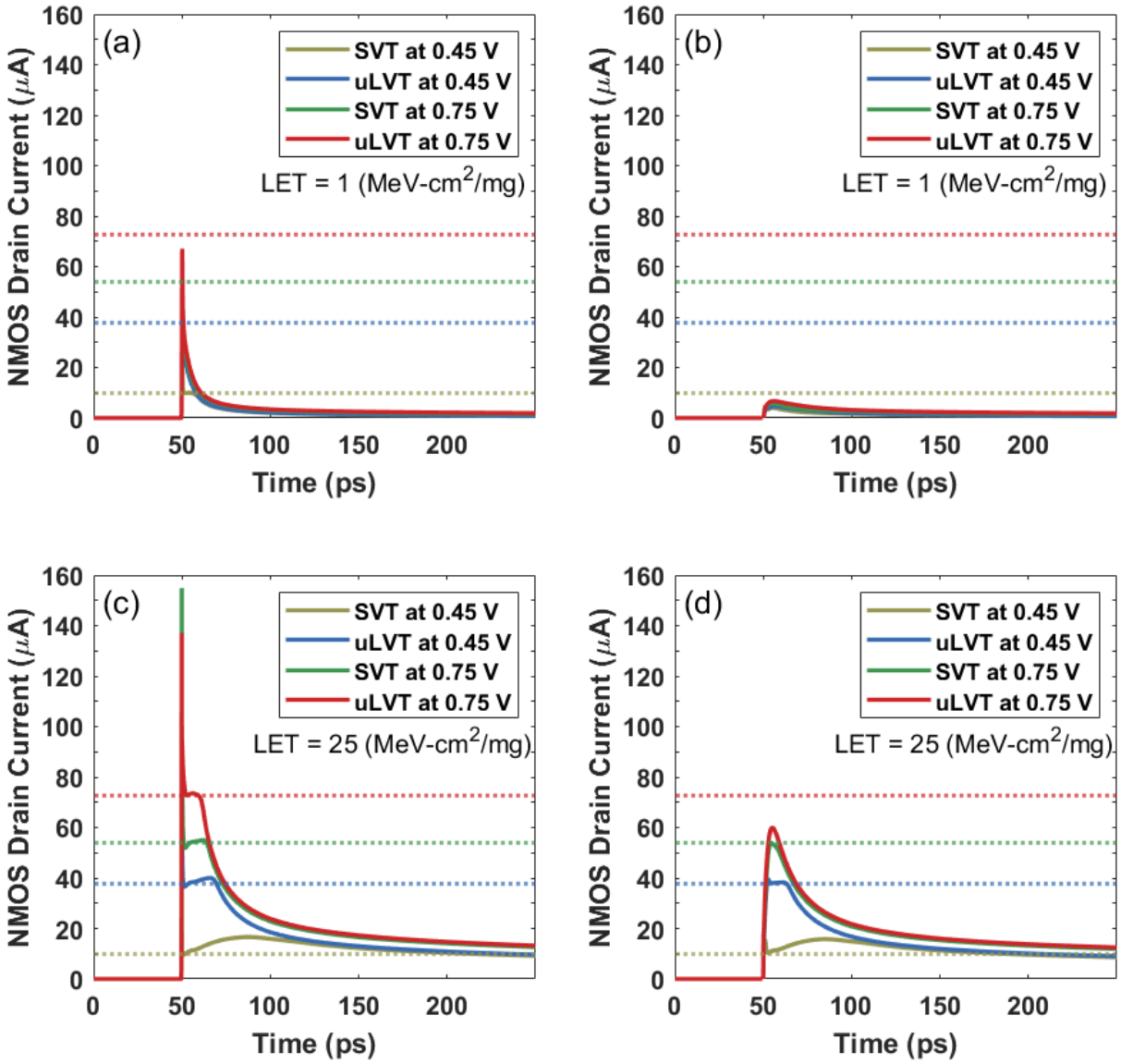


Figure 4.4: NMOS drain current from TCAD simulations of SET pulses generated by particle strikes located (a & c) directly at center of fin and (b & d) 100 nm away from fin. Simulations were done for particles with (a & b) LET = 1 MeV-cm^2/mg and (c & d) LET = 25 MeV-cm^2/mg. The dotted lines indicate the corresponding PMOS drive current for each threshold voltage and supply voltage combination.

In the low-LET cases, the ion-induced SETs in Figure 4.3 are virtually identical when comparing the uLVT and the SVT inverters at nominal supply. At reduced supply voltage, the SET waveforms are clearly different, but the output voltages are restored at approximately the same time. Perhaps more importantly, when the strike position is moved 100 nm away, there is no noteworthy voltage transient, and the curves for SVT and uLVT look almost identical at both voltage levels. In the high-LET case, even when the strike location is 100 nm away from the fin, SETs clearly occur. Not only that, but at 0.45 V supply voltage, the pulse widths of the SVT and uLVT versions are significantly different for both direct and indirect strikes, and the nodal voltage of the SVT option is, in both cases, restored a relatively long time after that of the uLVT option. The nominal-supply-voltage results still have similar pulse widths and restoration times, but the output voltages drop to different amplitudes in the case of indirect strikes.

The voltage pulse characteristics are most easily explained by looking at the current pulse characteristics in Figure 4.4 to better understand the flow of charge. In this case, given that the input to the inverter is held low, the drive of the PMOS pull-up transistor acts as restoring current that tries to pull the output of the inverter to its proper high value when it is perturbed by the transient pulse from the NMOS, as described in Section 2.3. If the restoring current is higher than ion-hit diffusion current, as it is in the low-LET indirect hit case, it is unlikely that diffusion current will cause an upset because charge carriers will be swept away faster than they can be supplied from the substrate [23]. Consequently, at low LET values, SEUs are unlikely to result from indirect strikes, where the SE current is caused mostly, if not entirely, by charge collection from the substrate. Examining the output voltages from this perspective, the voltage transients are nearly identical in the parts of the curves where the diffusion current is less than its respective PMOS drive current.

Because it depends on carrier concentration, diffusion current increases with LET, but it has only a small dependence on supply voltage and is independent of threshold voltage. More specifically, particles with higher LET values can generate more free carriers, and substrate doping is independent of V_T and supply voltage. Therefore, for particles with high LET values, reducing drive current by reducing the supply voltage and increasing threshold voltage can greatly affect SEU cross-section. This is true because while normal-incidence direct fin strikes almost guarantee upsets, whether cells upset due to strikes away from fins depends on the amount of charge collection from the substrate and the magnitude of the restoring drive current. The charge collection in the inverter is heavily influenced by the sub-fin and WELL dopings. If enough charge is collected such that the SET current amplitude surpasses the restoring drive current, then a current "plateau" forms when the output node is discharged and all of the SET current passes through the pull-up transistor [43] [44] [45] [46]. When this plateau occurs, restoration depends on WELL potentials being restored rather than on the drive current of the pull-up transistor because the pull-up drive cannot recharge the output node voltage until the amount of excess charge carriers collected from the substrate decreases. Therefore, when the restoring current and the diffusion current have similar magnitudes, as they do in the high-LET case, the diffusion current can contribute to SEUs. As one can see in Figure 4.4(d), the PMOS drive current level (where the current plateaus) is less than the diffusion current in the low-supply, high-V_T case. This means that an SET can occur due to ion-hit diffusion current alone under those conditions.

For older bulk CMOS technologies, the transistor sizing was significantly large enough that each transistor can be considered "isolated" from another with respect to an ion strike. A similar concept applies to silicon-on-insulator (SOI) technologies, which truly limit the restoration of a floating node to a pull-up (or pull-down) transistor by means of an insulating layer between

the fin and the substrate. However, in advanced bulk planar and FinFET technologies, high-LET particle strikes can lead to enough charge collection in the WELL/substrate region to dominate the response of the transistor. This is indicated by the large magnitudes of the diffusion currents in Figure 4.4 (c & d).

For low-LET particles strikes, pull-up transistor drive still dominates voltage restoration, as the diffusion current is generally much less than the pull-up current, though this is more due to inefficient charge collection from the substrate rather than actual isolation, as the sub-fin neck region does still connect to the substrate. Figure 4.5 clearly illustrates the role of the neck region in charge collection. One can see that for the SOI FinFET, diffusion current from adjacent node strikes is practically nonexistent because there is no bridge connecting the substrate to the fin, while the diffusion current for bulk FinFETs is almost identical for direct drain strikes and strikes to adjacent nodes because the neck region allows for some diffusion from the substrate. This mechanism will be addressed further in CHAPTER 6.

As an expository tool, these TCAD simulations provide valuable insight, but quantitatively they do not merit the same credence that the experimental data do. It is important to recognize that these simulations could not be tuned exactly to the technology in this paper due to the unavailability of some process parameters in published literature. Thus, the value in them comes from their ability to model mechanistic behaviors and not from their ability to accurately estimate SET parameters. The basic mechanisms exhibited by these simulations are consistent with those observed in previous works [18] and the trends in the 7-nm experimental data, but using TCAD models to numerically describe the SET response of this specific 7-nm process is beyond the scope of this work.

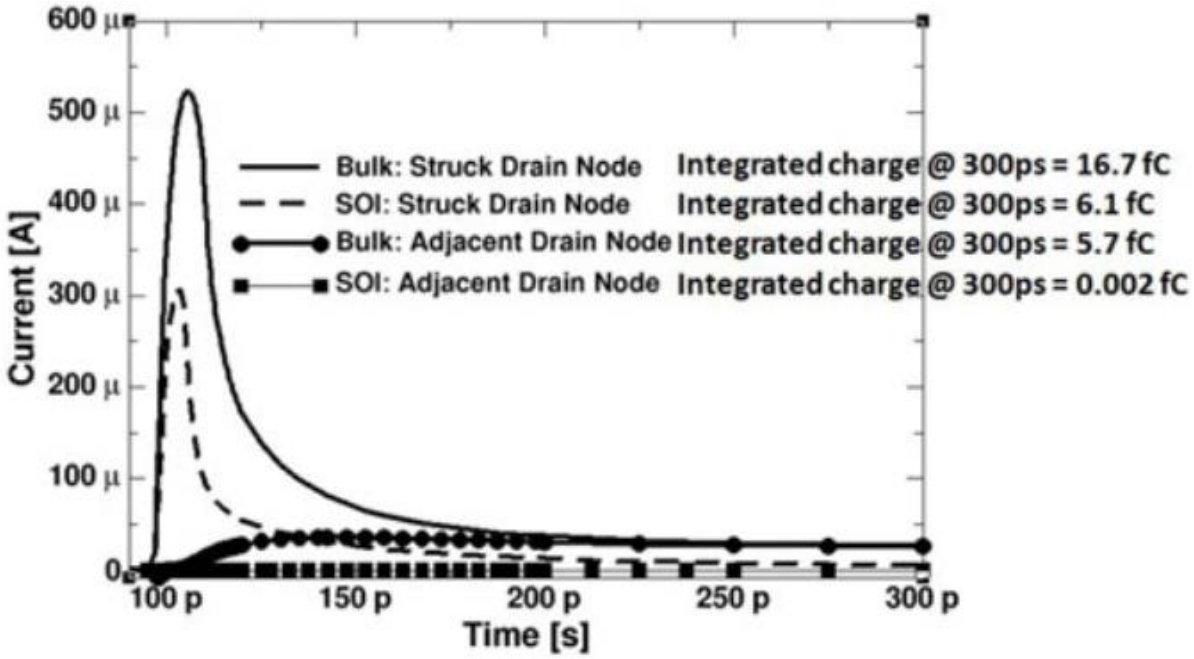


Figure 4.5: SRAM TCAD simulation results comparing the drain current transients and collected charge values for bulk and SOI FinFETs from both direct strikes and strikes to adjacent nodes. Generated charge = 50 fc/µm. From [47].

CHAPTER 5

Experimental Results

Experimental SEU cross-sections for each V_T option are shown as a function of supply voltage in Figure 5.1. At a supply voltage of 0.75 V (nominal), all designs show very similar SE cross-section for alpha particles (Figure 5.1(a)). As the supply voltage is reduced, results for all three options remain similar, but there are some slight differences at the lowest biases. In these results, the much stronger dependence on supply voltage, indicated by the almost 25× increase in cross-section for SVT as the supply voltage is lowered from nominal to 0.45V, completely overshadows any dependence of SEU cross-section on V_T choice. For heavy ions, although all V_T options show similar results at nominal supply voltage, particles with LETs less than 5 MeV-cm^2/mg produced inconsistent results as supply voltage decreased. At higher LET values, a more coherent trend emerges. Figure 5.1(b) shows the SE cross-section for Krypton with an LET value of 24.98 MeV-cm^2/mg.

At this LET value, clear differences between different V_T options are visible at below-nominal supply voltages; the SVT design has the highest SE cross-section and the uLVT design has the lowest SE cross-section. At a supply voltage of 0.45 V, the point of greatest difference between the SVT and uLVT cross-sections, the SVT cross-section is only about 2× larger than the uLVT cross-section. For high-LET particles, SE cross-section is subject to the transistor drive current trend —increasing drive current leads to decreasing SE cross-section.

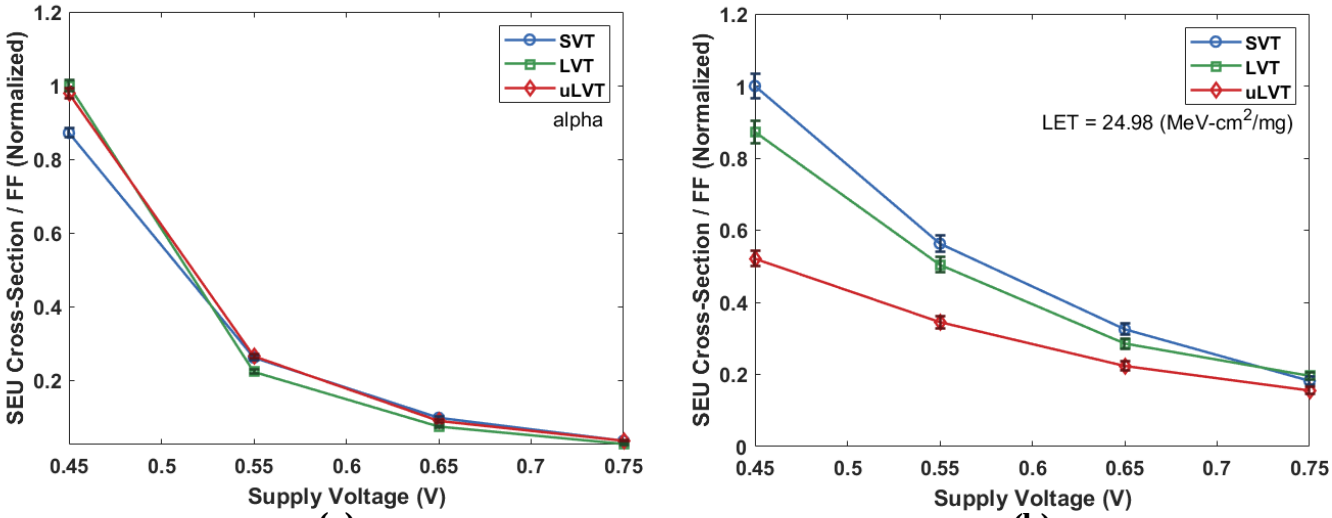


Figure 5.1: Normalized experimental SEU cross-section per flip-flop as a function of supply voltage for 7-nm DFFs with all three VT options. (a) shows alpha-particle results. (b) shows high-LET (24.98 MeV-cm^2/mg) results.

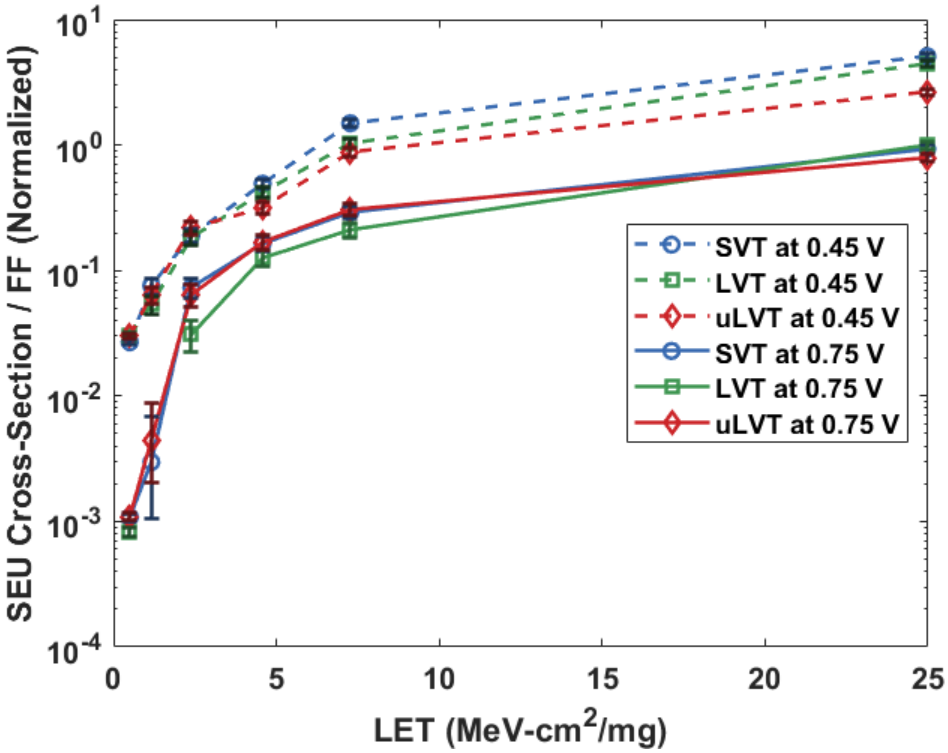


Figure 5.2: Normalized experimental SEU cross-section per flip-flop as a function of LET at nominal supply voltage for all available VT options.

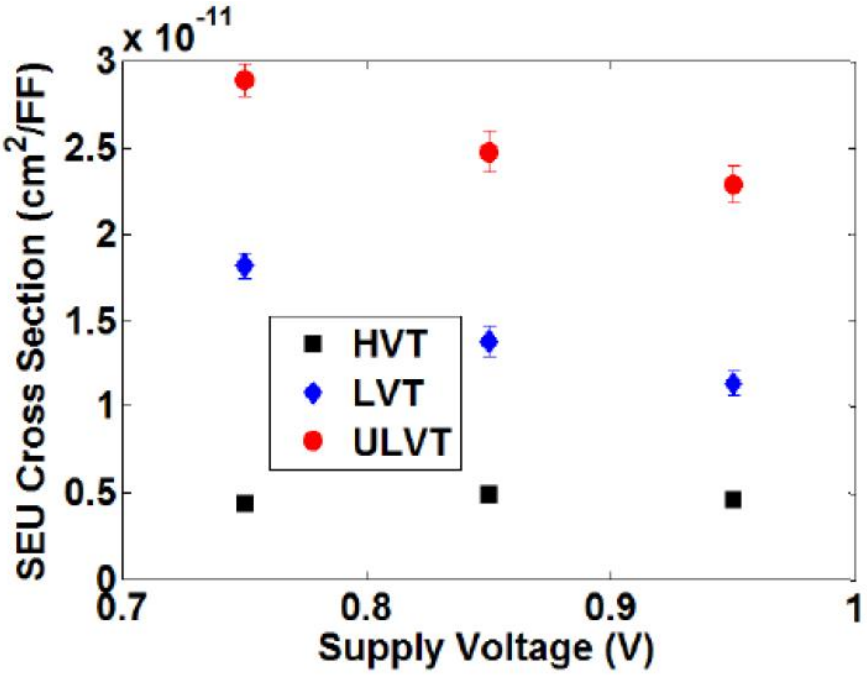
A key result from both the high-LET and the low-LET data is that at close-to-nominal supply voltage, there is no clear distinction between the SEU cross-sections of DFFs using the V_T options available in this technology, as shown by the data for 0.75 V in Figure 5.2. Comparing these results with the data for 0.45 V, also in Figure 5.2, although there is a noticeable difference between results for the different V_T options, the difference between highest and lowest supply voltages for a given V_T option is greater. At an LET value of 24.98 MeV-cm^2/mg, the average SVT cross-section at a supply voltage of 0.45 V is more than 5× larger than the average SVT cross-section at nominal supply. Not shown in Figure 5.2, the SVT cross-sections for 0.55 V and 0.65 V are, respectively, about 3× and about 2× larger than the 0.75-V SVT cross-section. For particles with low LET values, this dependence is even stronger, with uLVT cross-section increasing by about 25× as supply voltage decreases from 0.75 V to 0.45 V.

CHAPTER 6

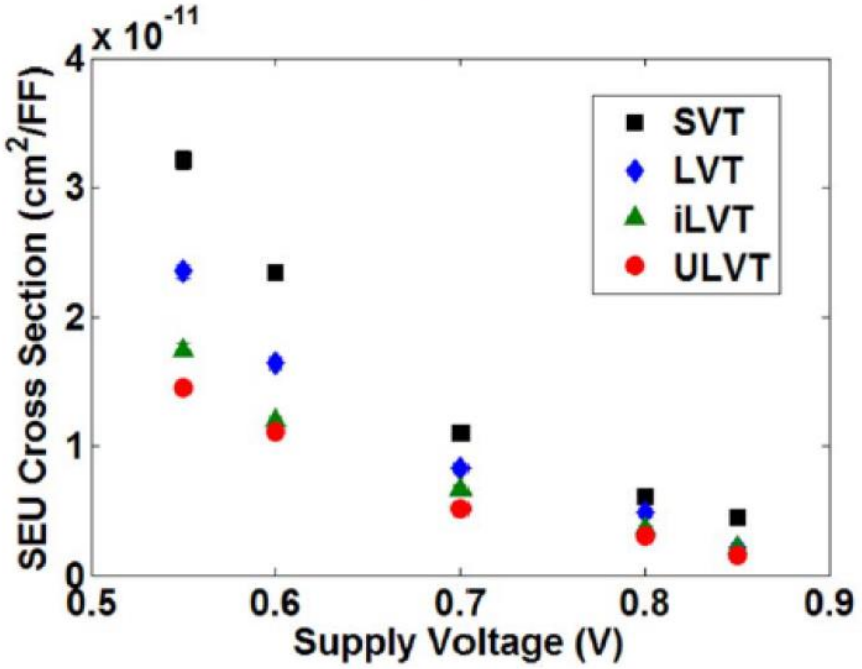
Discussion

The results from these experiments differ drastically from those for similar DFF designs at the 20-nm planar node and 16-nm FinFET node, as shown in Figure 6.1. For alpha particles, 20-nm and 16-nm circuits show opposite trends, with the 20-nm data showing SEU cross-section decreasing with V_T and the 16-nm data showing SEU cross-section increasing with V_T, whereas the 7-nm circuit shows no trend at all. These three distinct behaviors clearly illustrate the point that the effects of V_T options on SEU cross-section must be evaluated for each new technology node. Other works [16] [18] [29] explore why trends may be different between planar and FinFET technologies, but even comparing the 16-nm and 7-nm results, which are both bulk FinFET technologies and thus ostensibly subject to similar charge-collection mechanisms, the alpha results are still quite different. It is worth noting, however, that for higher LET values and lower-than-nominal biases, the 7-nm heavy ion results do follow the same trend as the 16-nm alpha results do, which is that SEU cross-section increases with threshold voltage.

SE cross-section as a function of particle LET is possibly related to mechanistic differences in how particle strikes cause upsets at different LET values. For FinFET technologies, it has been shown that the charge-sharing between transistors is weaker than that of planar nodes for low-LET ions [48]. This is mainly due to the narrow neck region connecting the channel region to substrate, which restricts charge diffusion from substrate to drain regions [17]. As a result, significant charge collection for low-LET particles occurs only when a particle directly hits the drain region [48].



(a)



(b)

Figure 6.1: Alpha-particle SEU cross-section per flip-flop as a function of supply voltage with all available VT options for (a) 20-nm DFFs and (b) 16-nm DFFs. In the 20-nm technology, SEU cross-section decreases as V_T increases, whereas in the 16-nm technology, SEU cross-section increases with V_T. Reproduced from [16].

Therefore, the sensitive region for a transistor in a DFF design is limited to just the drain region unless the transport limitations imposed by the narrowness of the neck region are overcome by sufficiently large charge generation in the substrate. This mechanism has been observed and modeled in a similar 16-nm bulk FinFET node [18], so it is reasonable to infer that it occurs in this technology as well. Figure 6.2 shows TCAD simulations illustrating this mechanism in the 16-nm node. For the low-LET strikes, only the direct hit causes an SET because there is not enough substrate charge collection for the non-direct hit to contribute to an SET. For the high-LET strikes, significant charge is collected from the substrate, and this charge dominates the SET response, leading to nearly identical pulses between the direct strike and the strike between fins.

For particles with lower LET values, this plentiful-charge condition is not met, so usually only strikes to the fin/drain are able to cause upsets, and the drain regions for the 7-nm DFF designs in this study are identical; moreover, critical charge (the amount of charge required to cause an upset) is extremely low at this node, so any normal-incidence direct hit in the drain region can cause an upset, yielding similar SE cross-sections for all V_T options. At higher LET values, however, significant charge is deposited in the substrate and enough diffusion charge collection occurs to cause an upset [18]. This is consistent with previous data showing that charge-sharing can indeed occur in FinFETs subjected to high-LET ion strikes [49]. Consequently, small differences in critical charge for different V_T options become substantial in determining SE cross-section. Since the critical charge is inversely proportional to V_T values, the uLVT design shows the lowest SE cross-section and the SVT design shows the highest SE cross-section.

This explanation agrees well with the earlier discussion of the TCAD simulations from Section 4.2. From Figure 4.3(b), it is clear that non-direct strikes will not cause an upset at low

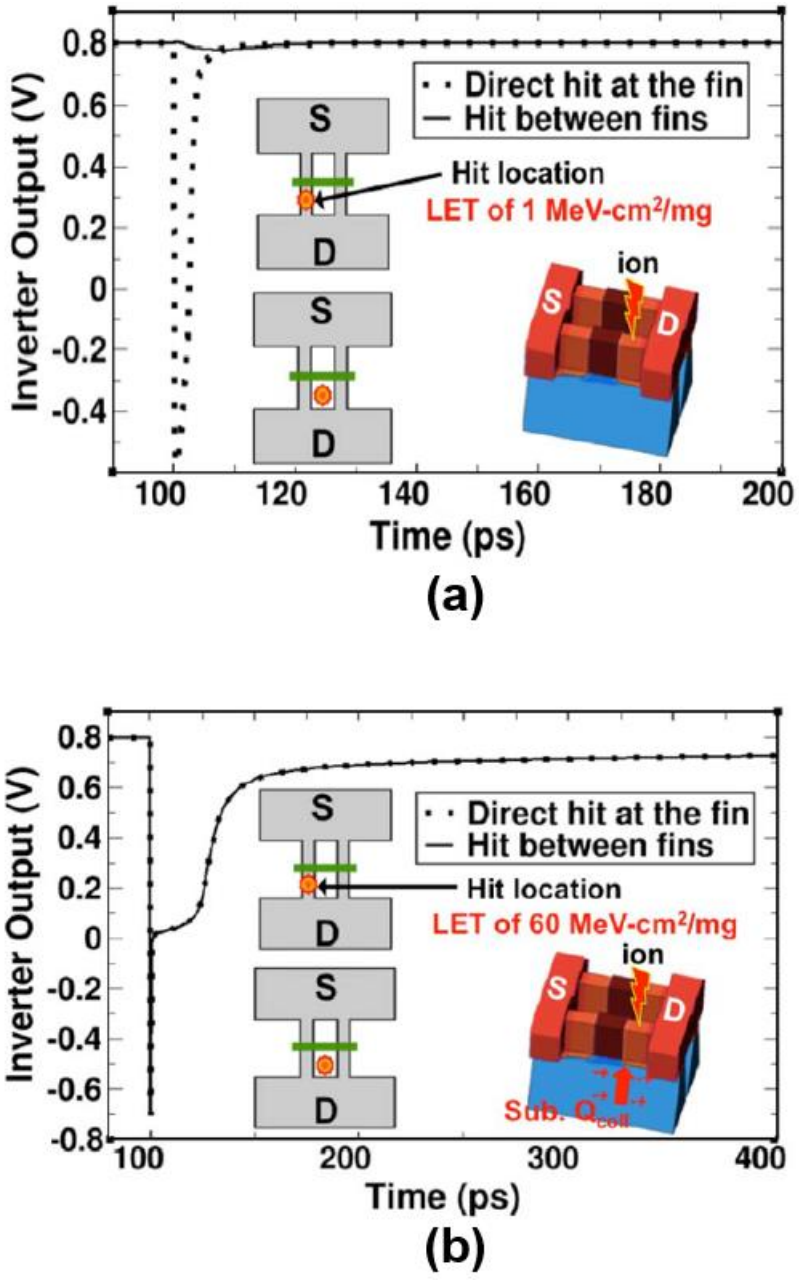


Figure 6.2: 16-nm TCAD simulations showing that the relative importance of strike location to SET response depends on particle LET. (a) shows low-LET (1 MeV-cm^2/mg) results. (b) shows high-LET (60 MeV-cm^2/mg) results. From [18]

LET values, and one can infer from the lack of a visible voltage transient that any NMOS drain current flowing from the output node into the substrate due to diffusion is completely overpowered by the PMOS pull-up transistor's restoring current. This is clearly not the case in Figure 4.4(a)(c)(d), where the presence of plateaus in the current waveforms indicate that the SET current amplitude seen at the drain is bottlenecked by the pull-up current [46], which is of the same order of magnitude as the diffusion current. The voltage at the output node cannot be restored while the restoring current and charge collection current are balanced. The presence of SETs for only direct strikes at low LET values but for both direct and indirect strikes at high LET values is what one would expect from the discussed mechanism, and this is exactly what the simulations showed. This is also consistent with the 16-nm TCAD simulation shown in Figure 6.2.

Regarding this explanation, it is appropriate to consider why there is such a stark disparity between the alpha results for the 16-nm and 7-nm nodes if they do, in fact, depend on the same mechanism. If this mechanistic explanation is correct, one could expect it to be generally applicable to all bulk FinFET technologies, since the entire idea is framed around a trait of their basic transistor structure. While it is possible that this explanation is incorrect, that is not necessarily the case. Another possibility, and the one favored in this work, is that the incongruity of these two trends is not due to distinct mechanisms, but rather to dissimilarities between the processes; even if the basic structure is the same, there are several process parameters that can affect the amount of charge collected from a particle strike, like doping density, fin height, minimum feature size, etc. [50]. In the 16-nm node, the critical charge and the collected charge from an alpha strike were similar, so small differences in critical charge due to differing drive currents between V_T options were more apparent [16]. In the 7-nm node, even if there is less average collected charge than there is in the 16-nm node and similar critical charge [14], the

amount of charge collected from drift for worst-case, normal-incidence, direct strikes to fins, which are taller in the 7-nm process than 16-nm process, can be adequate to cause an upset. Moreover, given how consistent this theory is with the TCAD results from Section 4.2, attributing the observed results to this mechanism is reasonable.

The speed of these transistors is critical in this argument because the response times of the 7-nm DFFs may be as quick as or quicker than the drift component of charge collection, making the shape of the SET current pulse more important than the total amount of charge collected [23]. In cases like this, the critical and collected charges cannot be treated as fixed values that are independent of time [51]. For the 7-nm node specifically, the diffusion current from low-LET particle strikes is too low and too slow to overwhelm the restoring drive current and lead to an upset, so the charge collected during the initial drift current pulse is more important than the total charge collected over the course of the event. This initial charge collection is still dependent on process parameters, so both observed trends can be explained if the initial charge collection is relatively larger when compared to the critical charge in the 7-nm node than in the 16-nm node for direct fin strikes at normal incidence. The overall sensitive area is smaller in the 7-nm process than in the 16-nm process, so these worst-case strikes happen less frequently, but when they do occur, they may be relatively more likely to cause an upset. Small differences in critical charge should not matter if the collected charge from the initial drift current is high enough to cause an upset for all V_T options.

Due to the proprietary nature of commercial technologies, the specifics of the 7-nm process are not available for calibration, precluding the possibility of finely tuned device simulations that directly compare these two technologies. The more generic, literature-based TCAD simulations shown earlier in Figure 4.3 and Figure 4.4 seem to support the importance of charge collection

timing, but simulations calibrated to this specific 7-nm technology would be required to support the claim that the taller 7-nm fins collect more charge initially than the 16-nm fins do for direct normal-incidence strikes. Whatever the cause may be, the fact remains that alpha-particle SEU cross-section depends on V_T in the 16-nm node but not in the 7-nm node, and this point is significant in and of itself; just knowing what the trends are and that the performance will not be the same as other technologies is enough for a designer using a new technology to assess the threat posed by SETs and plan accordingly.

These charge-collection-efficiency and temporal explanations may account for the effects of V_T options on SEU response, but in order to fully describe the presented results, other factors must be considered. The authors of [14] have already shown that the SE response to alpha particles in this technology has an exponential dependence on supply voltage, and these results show a similar dependence for heavy-ion irradiation, albeit weaker. This dependence is quantified for all V_T options and both low-LET (alpha particle) and high-LET (Krypton) particles in Table 6.1, which shows the ratios of SEU cross-section at given supply voltages to the corresponding SEU cross-section at nominal supply. Supply voltage is especially important for low-LET particles both because bias dependence is more pronounced at low LET values [10] and because the effects of V_T are less pronounced at low LET values in this technology. As for high-LET particles, even though the dependence of SEU cross-section on supply voltage is weaker than it is for low-LET particles, the presence of the V_T trend is contingent on supply voltage being lowered. The emergence of a V_T dependence can be attributed to a combination of the supply voltage dependence and the mechanistic explanations above.

As described earlier in Section 2.1, if an SET current pulse surpasses the restoring drive current of an inverter, the output will flip, and an upset occurs if this erroneous value can propagate

Table 6.1: Ratios of SEU Cross-Section at Given V_{DD} to SEU Cross-Section at Nominal Supply

	Alpha Particle Results			Krypton Results (LET ≈ 25 MeV-cm2/mg)		
V_{DD}	SVT	LVT	uLVT	SVT	LVT	uLVT
0.65 V	2.8±0.17	2.8±0.20	2.5±0.16	1.8±0.13	1.5±0.10	1.4±0.11
0.55 V	7.4±0.40	8.3±0.53	7.5±0.41	3.1±0.20	2.6±0.15	2.2±0.16
0.45 V	24.7±1.27	37.4±2.26	27.6±1.41	5.5±0.34	4.5±0.25	3.4±0.23

through the feedback loop of a latch before being rectified. Diffusion current magnitude depends only very weakly on supply voltage, and it is practically independent of V_T, but it depends strongly on LET. Conversely, drive current depends on both V_T and supply voltage but is independent of LET. From the discussion above, one can expect a trend to emerge after decreasing the supply voltage sufficiently lowers the drive currents of the V_T options such that they are of similar magnitude to the diffusion current. For particles with low LET values, this is unlikely because the limitation on charge collection efficiency leads to very small diffusion currents. For particles with higher LET values, however, substrate diffusion current is of great enough magnitude to affect SEU likelihood, and drive current can be lowered to the point where the two currents are of similar scale. Because drive current has a roughly quadratic dependence on the difference between the supply voltage and V_T (from the saturation current equations), the percent difference between the drive currents of different V_T options will also be larger when the supply voltage is lower, which in turn leads to larger differences in SEU cross-section.

Another factor worth considering is process variation. Process variation has been shown to have a large effect on the SEU response for flip flops in older planar technologies [52], and this has only gotten worse with size scaling. For newer FinFET technologies, simulations have

estimated almost a 20% impact on majority voter circuit SEU sensitivity [53] and almost a 50% increase in soft error rate (SER) for SRAM cells [54] due to process variations using a predictive 7-nm PDK. Moreover, FinFET devices are often operated at low supply voltages due to their excellent gate control mitigating some of the accompanying performance drawbacks, but supply voltage can be very close to the threshold voltage in these cases, leaving very little margin for error due to process variation. Exactly how close these voltages are for this specific 7-nm node cannot be disclosed at this time due to the proprietary nature of this technology.

Even though process variation was not an original topic of analysis for this work, it is worth considering because its presence was suggested by some of the data. In the worst case, a difference larger than 75% exists between two experimental SEU cross-sections obtained during alpha particle testing using different dies but otherwise identical conditions. It is infeasible to collect enough experimental data across separate dies to exhaustively examine the full impact of die-to-die variation on the results presented in this paper, but this examination could perhaps be accomplished using simulations as a subject of future research, once more information about this technology is publicly available. While the possibly that weak dependencies could be overshadowed by die-to-die variations cannot be ignored, the palpability of the trends exhibited in this work suggest that they are too strong for this to occur.

Regardless of their cause, based on these results in this work, the optimal choice of V_T depends on the environment and bias conditions for which the system is being designed. In environments where alpha particles or low-LET particles are the main concern, designers can safely use SVT transistors to reduce power with little-to-no increase in SEU cross-section. The same is true for devices that can be guaranteed to operate at or near their nominal supply voltage.

In general, the tradeoff between SEU cross-section and V_T must be considered for designs that must endure high-LET particle strikes at below-nominal supply voltages.

CHAPTER 7

Conclusions

Many circuit designers are accustomed to evaluating threshold voltage options in the context of leakage-performance tradeoffs, but evaluating effects on reliability can be just as important. In particular, for environments where radiation is a concern, it is imperative that designers properly account for any effects on SE response due to changing V_T, and since these effects are inconsistent across different technology nodes, the best way to do this is often by looking at experimental data. For the 7-nm technology used in this paper, SEU cross-section is largely independent of threshold voltage. Only when supply voltage is low and particle LET is high does a trend appear, which is that SEU cross-section is directly related to threshold voltage. In keeping with these results, is it is generally safe to reduce power consumption by choosing a higher V_T option for scenarios in which voltage levels are nominal because SEU responses at different values of V_T remain similar. Even at sub-nominal biases, as long as particle LET values remain low, supply-voltage effects and process variation are probably larger concerns, but environments with high-LET particles may require using lower threshold voltages.

An important implication of these results is that similar experiments must be performed for each new technology node that may see use in a radiation environment, which may be all nodes, given the increasing interest in ion radiation therapy and the use of COTS parts in spacecraft. Indeed, if even the 16-nm and 7-nm nodes, two similar bulk FinFET processes, can have starkly different results, one cannot assume that behaviors similar to those in existing nodes will manifest in future nodes. Future research in this topic will be especially important for implementations of new types of transistors, such as gate-all-around FETs (GAAFETs)[55], as these will likely be

subject to entirely different charge-collection mechanisms. As alluded to in the previous chapter, performing more rigorous simulations to characterize the effects of process variation on SE response could also prove to be insightful, as process variation can often be an especially large concern in highly scaled technologies such as this one.

The main purpose of this work is to provide an analysis of the effects that V_T has on the SEU response of a 7-nm bulk FinFET technology. The results of this analysis are described above, along with a possible mechanism to explain these results and further analysis of how the influence of V_T is affected by other factors, such as supply voltage. Although the data is normalized to protect proprietary details, the shown trends should still be immensely helpful to any circuit designer planning to use this technology in a radiation environment.

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