TECHNIQUES TO MITIGATE DIGITAL BIT CORRUPTION IN SILICON-ON-INSULATOR FLASH ANALOG-TO-DIGITAL CONVERTERS

By

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Chapter 1

INTRODUCTION

Signal processing systems, such as software-defined radios, often use digital circuits to efficiently analyze data produced from analog signals. Analog-to-digital converters (ADCs) translate continuous-time analog signals into discrete digital values. This is achieved by sampling the continuous time signal at predetermined intervals and generating representative digital values at each sample point. ADCs are used in a wide range of signal processing applications, including medical, space, and defense electronics [1]. Each application may have significantly different design constraints, requiring various area, power consumption, sampling rate, and resolution specifications, resulting in a wide range of ADC designs.

For space and defense applications the reliability of key components, such as an ADC, is critical when exposed to ionizing radiation environments. Ionizing radiation can cause electrical errors in digital circuits [2]. Data corruption created by electrical errors in ADCs lead to invalid data conversions, which can result in data corruption. For circuits to function properly when operating in a radiation environment, they must be resistant to these inflicted electrical errors. One way to improve circuit response is to apply radiation-hardened by design (RHBD) methods. RHBD methods use additional circuitry to improve radiation response. This approach inflicts design penalties, e.g. reducing circuit performance for an increase in radiation hardness. In an ADC this will decrease sample rate, while increasing circuit area and power consumption.

In this work, an ADC is designed for applications within silicon-on-insulator (SOI) CMOS technology nodes. The design maximizes sample rate and provides adequate signal resolution, while functioning within a radiation environment. Sample rate requirements are met using a flash

analog-to-digital converter (FADC) design that utilizes parallel comparison to maximize sample rate. It is important to note that in this work a nontraditional FADC is applied because it is assumed stable reference voltages are available. To ensure functionality in a radiation environment, RHBD methods have been applied to the FADC. Conventional RHBD FADC designs are focused on eliminating all radiation-induced errors [3], incurring significant design penalties. In this work, a novel most significant bit (MSB) hardening technique protects data conversions from radiation errors while reducing design penalties.

Chapter 2

ANALOG-TO-DIGITAL CONVERTER DESIGN

2.1 Analog-to-Digital Conversion

Analog signals are continuous values, which vary over time. Signal processing circuits rely on information from analog voltages but require digital values to complete data analysis. This creates the need for an Analog-to-Digital Converter (ADC) circuit to convert analog voltages to representative digital binary vectors. The idea of representing a continuous signal with binary vectors is illustrated in Figure 2.1. This example uses a continuous sinusoidal input starting at time T=0 and ending at time $T=T_m$. For each time increment T, the value of the sine wave is converted into a representative 4-bit binary vector. In Figure 2.1 a portion of the representative vectors are displayed in the quantized vector table. These vectors are then used to recreate a representative plot of the sinusoidal input.

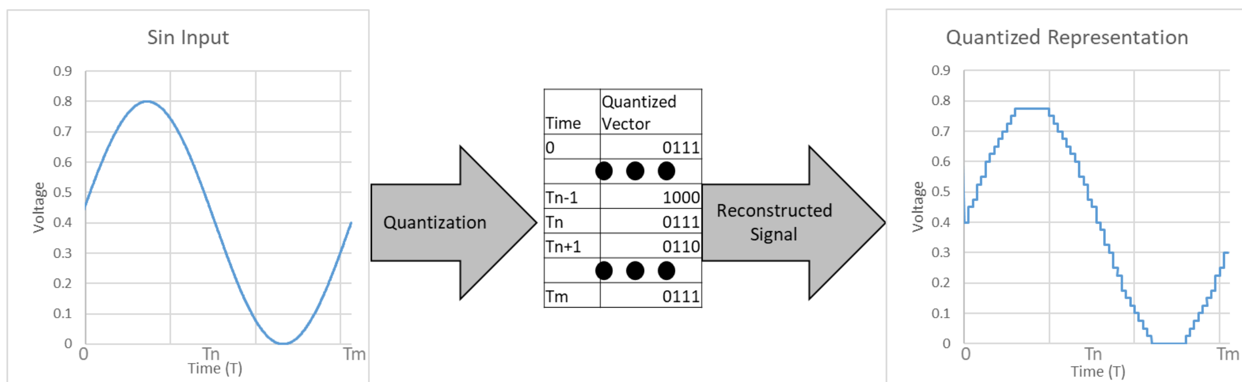


Figure 2.1. Illustration of ADC methods, a sinusoidal input is created, this input is converted into 4-bit binary vectors and these vectors are used to recreate a representative graph of the input

2.2 Analog-to-Digital Converter Design Tradeoffs

In ADC design, various circuit topologies are applied for different design applications. These designs are optimized for various parameters such as sample rate, resolution, circuit area, and power consumption. Optimizing a circuit for one or more of these parameters will often incur

design penalties in other circuit performance characteristics. For example, successive approximation ADCs conserve power and circuit area, but incur conversion speed penalties due to the iterative method used to determine the representative digital value [4]. This iterative method compares the analog input voltage to a predetermined value. Then using this comparison, the representative voltage range is narrowed. When repeating this process over multiple comparison periods, the digital value converges on the analog input voltage. Once a given tolerance is met, the representative voltage is determined. This use of successive comparison allows for a reduction in ADC circuitry because the same circuitry is used in each comparison period, reducing power consumption and circuit area. However, because it takes multiple comparison periods to determine the representative value conversion time is increased.

2.3 Analog-to-Digital Converter Motivation and Topology Selection

In this work an ADC is developed for use in the single-event radiation environment, which maximizes sample rate. This must be done while limiting design penalties in terms of circuit power consumption and footprint. Achieving this allows for the ADC to be used in a variety of signal processing applications such as communication and measurement circuits. A flash analog-to-digital converter (FADC) topology is applied to maximize sample rate, which incurs design penalties in terms of circuit footprint and power consumption. When applying this FADC design to the single-event radiation environment, it is important to reduce radiation hardening design penalties, while preserving radiation hardness. ADC sample rate, area, and power consumption design penalties are reduced when compared to a fully hardened FADC design. These methods are demonstrated using a 16 level, 4-bit ADC.

2.4 Flash Analog-to-Digital Converter Design

Before discussing the specifics of the FADC developed in this work, it is important to discuss the underlying FADC design principles. These ideas are illustrated using a 3-bit FADC as shown in Figure 2.4.1. It is important to reiterate that in this work a 4-bit FADC is developed, but the design principles remain the same when discussing a 3-bit or 4-bit FADC. Furthermore, these design principles are better illustrated using a 3-bit FADC.

A high-speed FADC design applies parallel comparison to maximize conversion speed. As shown in Figure 2.4.1, stacked impedance sources create evenly spaced reference voltages. In this work it is assumed that stable reference voltages are provided. These reference voltages are used for parallel comparison to an analog input voltage in a comparator bank. Each comparator determines one level of resolution by comparing the input voltage to a unique reference voltage. Comparison conversion times vary depending upon the input voltages. For this reason, these digital outputs are read into a D Flip-Flop (DFF) circuit at regular intervals to remove this temporal effect. After the DFF stage, the digital vector created by the comparators is converted to a binary output using an encoder. These output voltages are read into a second synchronization DFF stage, which provide the final output vector.

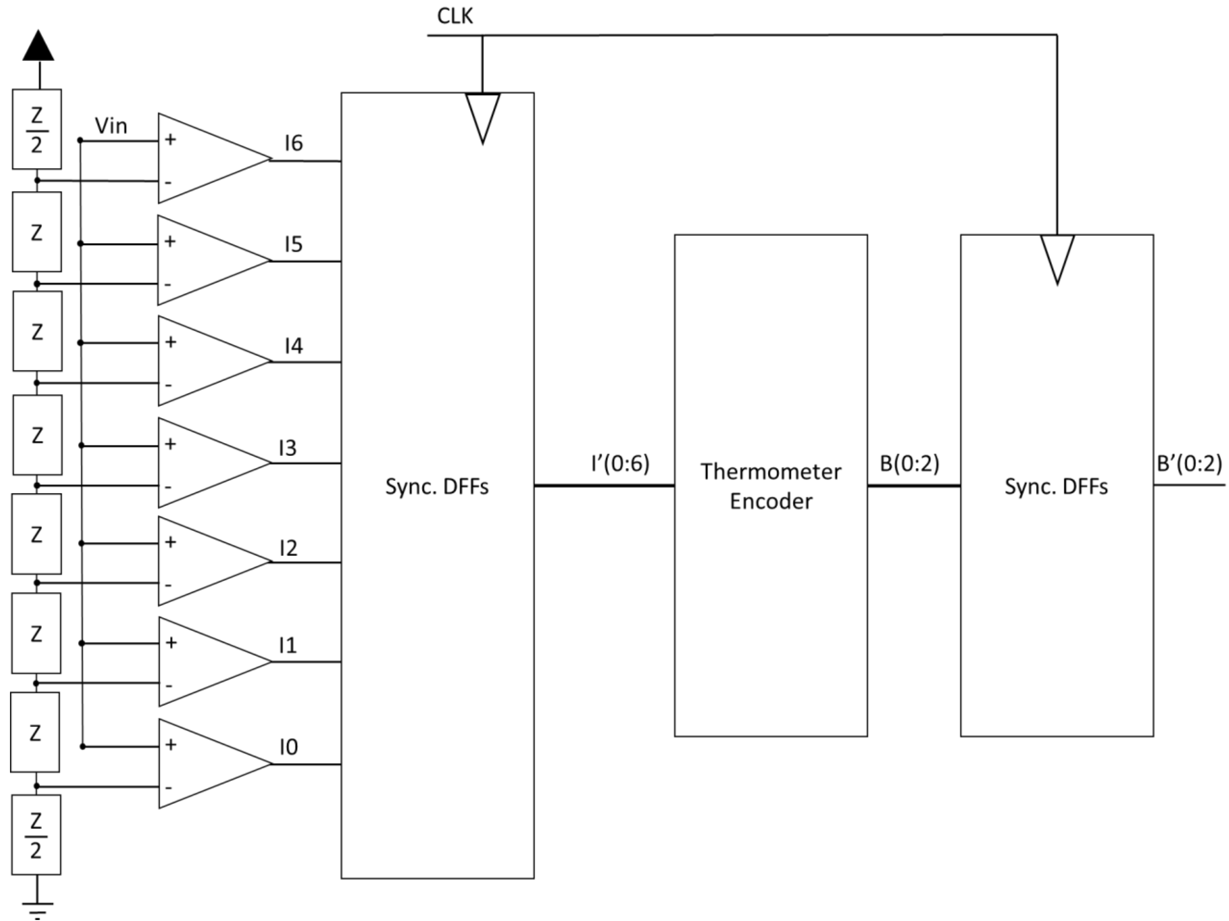


Figure 2.4.1. Illustration of sample FADC impedance ladder creates reference voltages for the comparator bank. The comparator bank creates a digital vector that represents the analog input and is then encoded into binary. DFF circuits used for signal synchronization.

To provide adequate sample resolution, design penalties are incurred in terms of circuit space and power consumption when compared to other ADC topologies. This is illustrated by comparing a successive approximation ADC to a FADC. To provide additional sample resolution, the successive approximation ADC requires more conversion periods, because the same circuitry is continually used. FADCs replace this temporal redundancy with spatial redundancy, using 2^n-1 comparators to complete an n-bit FADC conversion. This leads to large circuits with increased power consumption. However, it only takes one clock cycle to determine the digital output, maximizing ADC sample rate.

The FADC design discussed in this work is a modified topology of [5]. It is represented with a block diagram consisting of three sub-circuits and two D Flip-Flop (DFF) stages to provide data synchronization. Going from left to right in Figure 2.4.2, the first sub-circuit is the reference voltage circuit, which creates evenly spaced reference voltages between ground and V_{dd} using stacked impedance sources. These reference voltages are used in the second sub circuit: the comparator ladder. For each reference voltage, V_{ref}, a unique comparator is used to compare the V_{ref} to Vin and determine which has the greater value. These parallel comparisons determine a representative quantized value encoded in unary, which is often referred to as "thermometer code" in FADC design. Because comparison speed is not equal, DFFs are placed at the output of each comparator to synchronize output data. The final sub-circuit is the thermometer encoder, which is a digital logic circuit that uses the attributes of thermometer code to create a corresponding binary output. DFFs are again placed at the output of the thermometer encoder for data synchronization.

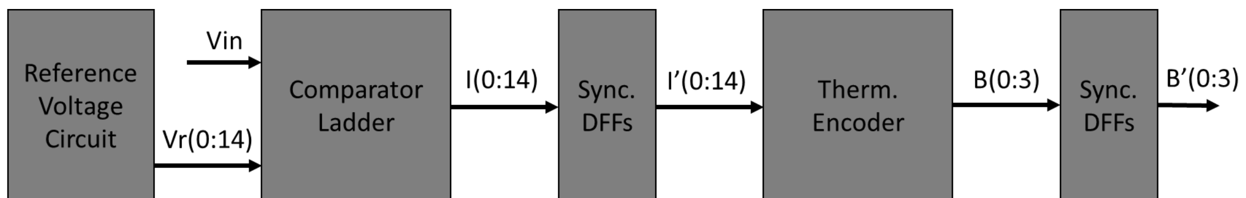


Figure 2.4.2. Flash Analog-to-Digital Converter Block Diagram, where reference voltages are created and used for conversion in the comparator ladder and encoded into binary using a thermometer encoder

2.5 Thermometer Code

The concept of thermometer code is important to understand when analyzing a FADC. Thermometer code is created by the comparator stage and is the quantized value representing the analog input. A valid thermometer code conversion consists of every bit before a transition point being a 1 and then every bit after a transition point being a 0. The number of 1s represents the value of the code because every digital 1 bit represents a comparison where V_{in} is greater than V_{ref}.

Vertically picturing all 1s before a transition point and 0s after a transition point looks like an analog thermometer, leading to the name “thermometer code”. This idea is illustrated in Figure 2.5, where on the left an analog thermometer is displaying a value, which is then represented in thermometer code and binary code. This figure also highlights the inefficiencies of thermometer code: it requires 2^n-1 bits of thermometer code to represent the same value as n bits of binary code. To create an efficient output, it is necessary to convert thermometer code to binary code within the FADC.

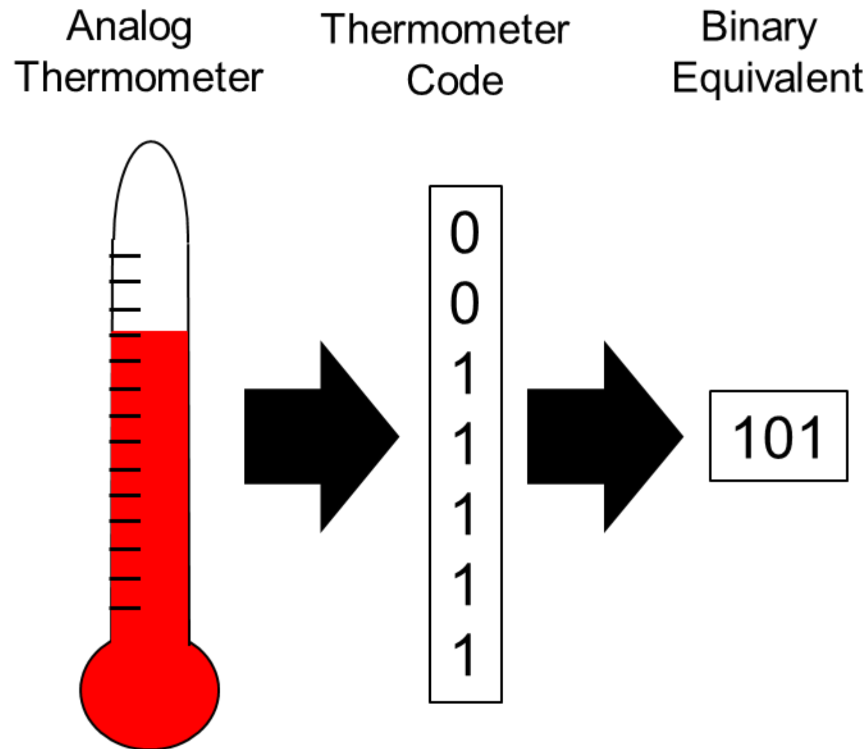


Figure 2.5. 7-bit thermometer code illustration. The value of an analog thermometer is represented first by thermometer code and then by the binary equivalent.

2.6 Silicon-On-Insulator Technologies

An integrated circuit uses about 0.1% of a silicon wafer for active electrical operation that is typically occurring within the top few microns of silicon in a bulk CMOS technology. The remaining portion of the silicon substrate is typically hundreds of microns thick providing

mechanical support for the die. As shown in Figure 2.6 [6], Silicon-On-Insulator (SOI) technologies isolate the functional integrated circuit from the inactive portion of the silicon wafer by introducing a non-conductive oxide layer between the active silicon and the substrate [7]. In bulk planar CMOS, the capacitance associated with the drain/body depletion region can be significantly large to affect the speed of the circuit. The application of SOI methods provides a buried oxide layer that truncates the depletion region, decreasing the drain/body capacitance, resulting in faster circuits.

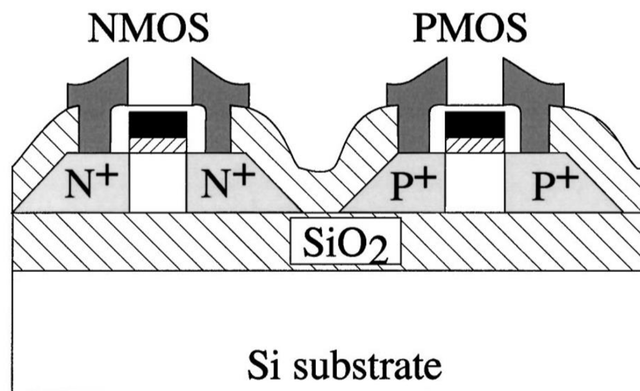


Figure 2.6. Silicon-On-Insulator cross section. NMOS and PMOS with the bodies of the transistors isolated from the substrate using an insulated layer (in this case silicon dioxide) [6].

Chapter 3

FLASH ANALOG-TO-DIGITAL RADIATION VULNERABILITIES

3.1 Single-Event Radiation Environment

When an energetic particle, such as an ion, interacts with silicon, electron-hole pairs (EHPS) are created. If an electric field is present in the silicon (as a result of a reverse-biased P-N junction), the EHPS can separate, leading to current flowing through the P-N junction. Due to the relationship between voltage, resistance, and current, a voltage perturbation referred to as a single-event transient (SET) is created if the current flow has sufficient magnitude. SETs can alter the output state of circuit nodes leading to electrical errors. For example, if the output node of an inverter is biased high and an ion strike results in the node being pulled low, then an opportunity for an electrical error due to ionizing radiation is created.

The probability of an electrical error taking place within a circuit is dependent on the amount of energy deposited by the incident particle per unit path length and is measured by Linear Energy Transfer (LET) MeV/cm/mg. LET normalizes the energy deposited to the density of the target material. Generally, the more charge that is lost correlates to a higher LET which leads to more deposited charge. As a particle deposits charge in a target material it loses energy and slows, potentially stopping in the target material. The LET during this process is not constant because the particle loses energy at a different rate as it slows. This change in energy loss is described by the Bragg Curve, which plots energy loss in terms of path length with the maximum energy loss at the Bragg Peak. The amount of charge deposited is altered by the funnel effect [8], [9], where collected charge is increased by perturbing the electric field of a p-n junction through an increase in the area of depletion region, which leads to an increase in collected charge due to drift mechanisms.

A Single Event Upset (SEU) occurs if an electrical error is created by an incident particle. SEUs occur through two main mechanisms: direct alteration of a latched state [10] and SET propagation to a storage circuit [11]. Many storage circuits use feedback to store a digital state. For example, SRAM cells use an inverter pair. When an incident particle strikes the storage node a SET is created and leads to a SEU if it is fed through the feedback inverter before the circuit node recovers from the ion strike [10]. The minimum amount of charge needed to alter the digital state is referred to as the critical charge and is denoted as Q_{crit}. SETs create SEUs by propagating through the circuit and becoming latched in a storage node. SETs are generally created in logic; the incident ion deposits charge and temporarily changes the output state. If the output of this logic is being latched while the SET is occurring, then a SEU is created.

3.2 SOI in the Radiation Environment

As discussed in Chapter 2, adding a buried oxide layer results in isolation of the active silicon from the substrate for electrical operation. Similarly, when an ion passes through the active region in an SOI technology, charge that is deposited in the substrate is unable to transport through the buried oxide layer which in turn reduces collected charge because of a reduction in the sensitive volume. However, radiation induced turn-on of a parasitic bipolar transistor (BJT) can amplify the collected charge [12]. As shown by Kauppila in [13], this amplification can impact the width of a single event transient voltage pulse but has minimal effect on SEU in sub-50nm CMOS due to the short time frames. While the parasitic BJT can be important for SETs and total charge collection on a node, typically the parasitic BJT does not directly impact SEU in an inverter pair because the SEU has occurred before the parasitic BJT has turned on.

3.3 Upset Mechanisms

As previously discussed, an energetic particle interacting with silicon may create a SET potentially leading to a SEU. This SEU corresponds to a loss of data and potentially an invalid data conversion within the FADC circuit. To identify the cause of this data loss due to single events, it is important to identify the upset mechanisms of individual circuit components, which are denoted in Figure 3.3. In this FADC design, the key upset mechanism of the D Flip-Flops (DFF) and clocked comparator circuits is a single event perturbing a latched state creating a SEU, denoted by a red box in the block diagram below. In the logic circuit the key upset mechanism is a SET becoming latched into a SEU in subsequent circuitry, denoted by an orange box in the block diagram. In previous work and simulated circuit analysis, it has been shown that the comparators and DFFs within FADCs are the most vulnerable to SETs creating SEUs, while logic circuits are less vulnerable [14]. Regardless of the upset mechanism, if uncorrected, an SEU can potentially reach an output node and cause an incorrect data conversion, thus degrading system performance.

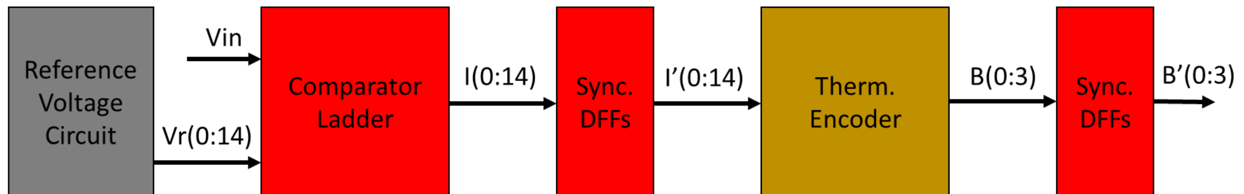


Figure 3.3. Flash Analog-to-Digital Converter Block Diagram highlighted to emphasize single event vulnerabilities: Grey uninvestigated, Red single events perturb a latched state leading to an SEU, Orange single events create SETs, which become SEUs if latched in subsequent circuitry.

3.4 Bubble Error

Upsets within the FADC often manifest as "bubble error", where a SEU corrupts an otherwise valid thermometer code. A "bubble", as illustrated in Table 3.4 manifests as a "1 bubble" defined by an erroneous 1 in the 0 sequence, or a "0 bubble" defined by an erroneous 0 in the 1

sequence. It is described as a bubble error because the erroneous 0 or 1 resembles a bubble in an analog thermometer.

The 1 to 0 transition point determines the representative value of the FADC conversion because it indicates all V_{ref} voltages which are less than V_{in}. If the bubble error does not take place near the 0 to 1 transition point, the type of bubble error, a 0 bubble or 1 bubble, can be determined. Thus leading to the correction of the erroneous bit and recovery of a valid data conversion.. As displayed in Table 3.4, the 1 bubble and 0 bubble are easily identified meaning that they can be corrected.

TABLE 3.4 ILLUSTRATION OF BUBBLE ERROR

Illustration of 1 bubble and 0 bubble.1 bubble is a 1 after the 1 to 0 transition. 0 bubble is a 0 after the 0 to 1 transition.

Bit	No Bubble	1 Bubble	0 Bubble
I14	0	0	0
I13	0	0	0
I12	0	**1**	0
I11	0	0	0
I10	0	0	0
I9	0	0	0
I8	0	0	0
I7	1	1	1
I6	1	1	1
I5	1	1	**0**
I4	1	1	1
I3	1	1	1
I2	1	1	1
I1	1	1	1
I0	1	1	1

When a bubble error takes place within one bit of the transition point, the error can be detected but not corrected, because the true transition point is lost. To illustrate this idea first consider the bubble errors in Table 3.4. It is relatively easy to determine the bit, which is in error, meaning that additional logic can detect and correct the bubble. Now consider Figure 3.4, a bubble

takes place near the transition point and it cannot be determined if this is a 0 bubble or a 1 bubble. In this case additional logic can only detect that the bubble error exists, but the true transition point cannot be determined.

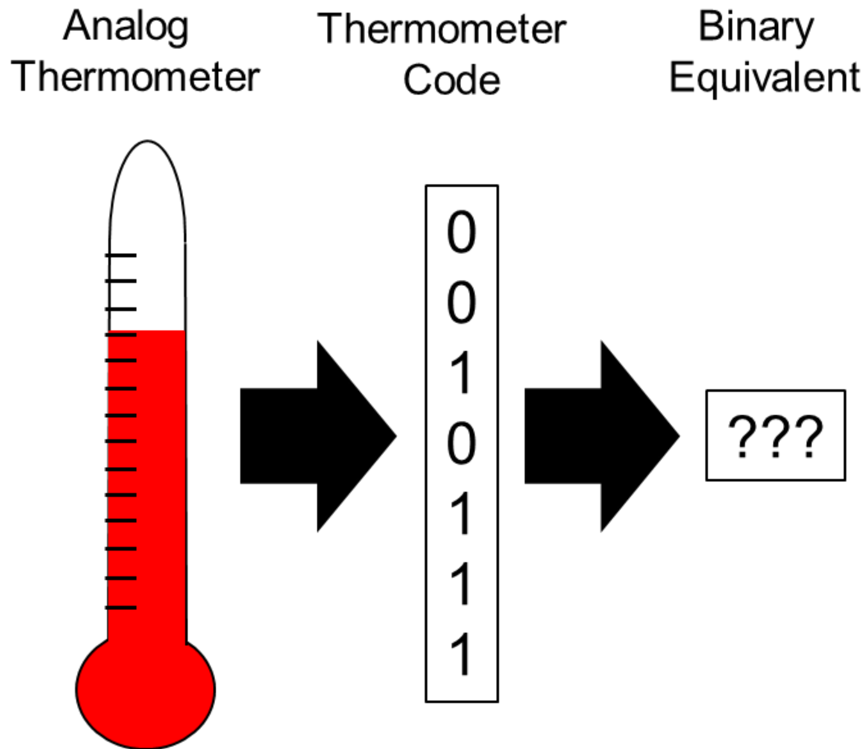


Figure 3.4. An illustration of bubble corrupted thermometer code, where a bubble error in the thermometer code will possibly lead to an incorrect binary output

3.5. Radiation Hardened by Design

One way to protect circuits from the effects of ionizing radiation is by adding material to stop particles before interactions can take place, a method referred to as shielding. However, as particle energy increases, shielding requires significantly more material to remain effective, leading to significant design penalties in terms of physical design, weight and area. An alternative approach is Radiation Hardening by Design (RHBD), which uses additional circuitry to protect from ionizing radiation and incurs circuit level design penalties instead of increasing physical weight and area.

As summarized in Figure 3.5, two RHBD methods are used to mitigate SEU errors in comparator and DFF circuits, denoted in green, and error correction is applied to the most significant bits of the thermometer encoder, denoted in blue. SEU is mitigated through the application of dual interlocked storage cells (DICE) [15] and device stacking [16], [17]. DICE saves the digital state at multiple nodes to provide redundancy. When an ion creates an electrical error in a single node, the other circuit nodes will use feedback to correct the error. Device stacking replaces a single transistor with two in series to effectively ignore SETs at input nodes. This is applied to protect sensitive transistors from a bias perturbation due to ionizing radiation. Error correction codes use additional encoder logic circuitry to detect and correct errors. This reduces the number of corrupted data conversions. Combining these techniques provides an efficient RHBD FADC circuit.

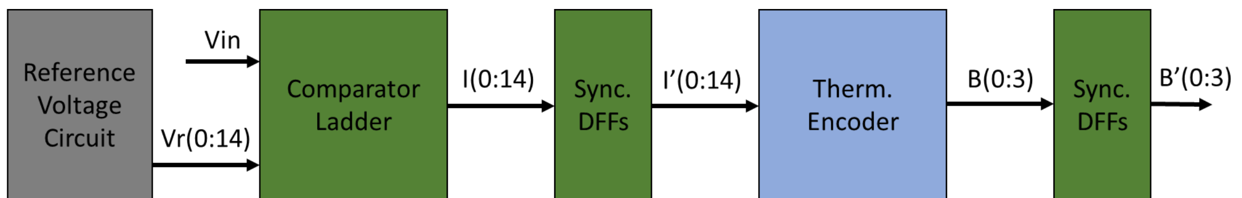


Figure 3.5. Flash Analog to Digital Converter Block Diagram highlighted to emphasize hardening approach: Grey uninvestigated, Green circuit level protection from SEU, Blue application of MSB correction

Chapter 4

SIMULATION METHODOLOGY

4.1 Overview

Circuit level simulations are used to create comparisons between various circuit topologies. These circuit level simulations are used to quantify the design tradeoffs between the presented FADC, a fully radiation hardened FADC, and an unhardened FADC design to verify that the design preserves radiation hardness while conserving design penalties.

4.2 Single-Event Simulation Methodology

A framework for using single-event simulations to design a circuit which mitigates single event phenomena is given in [18] and follows three steps: 1) define an upset metric and identify transient propagation paths, 2) use single event simulations to create single events in every sensitive node and review propagation paths plus identify additional paths, and 3) identify SEU sensitive circuit components and determine their vulnerabilities. This allows for single event resistant circuits to be designed using verified circuit level single event simulations rather than physical testing and multiple implementations of silicon circuits, thus allowing for more efficient RHBD circuit design.

In this work, this design method is applied to the FADC using data verified compact models for Partially Depleted Silicon-on Insulator Technologies (PD-SOI) at sub-50nm technology nodes [13]. These single-event models allow for a specific transistor to be struck with control of particle, strike time, LET and angle of incidence. Applying these models to circuit simulations allows for the detection of vulnerabilities and verification of hardening techniques. This leads to the creation

of a RHBD FADC, which mitigates key SEU vulnerabilities producing a resistance to corruption from single event phenomena.

4.3 Circuit Performance Simulation Methodology

Performance comparisons for the unhardened and hardened circuits were completed using parasitic-extracted circuit netlists within the Cadence Virtuoso environment, at sub-50nm PD-SOI technology nodes. Propagation delay was measured by comparing the amount of time it takes for the digital state to change from ground to mid-rail or V_{dd} to mid-rail. Maximum dynamic power was compared by finding the maximum current flow and using it to calculate the consumed power. Similarly, average static power consumption was determined through measuring the average current flow. Circuit area was determined by measuring the physical circuit layout size. These measurements on the hardened and unhardened circuits create performance comparisons in terms of circuit power consumption, speed, and area.

Chapter 5

COMPARATOR DESIGN AND HARDENING

5.1 Comparator Ladder Design

As discussed previously, the comparator ladder creates a quantized representative value corresponding to the magnitude of the input voltage. To complete this task, an n-bit FADC uses 2^n-1 comparators with each comparator creating a quantization level, providing 2^n data levels. For example, in this work a 4-bit FADC uses 15 comparators to create 16 output quantization levels. When V_{in} is less than all V_{ref} levels the zero-quantization level is the result.

To optimize the FADC sample rate, a high-speed clocked comparator design, as shown in Figure 5.1.1, [19] was selected, which can complete data conversions on the order of tens of picoseconds and allow the FADC to function in the gigahertz range. The comparator functionality consists of two phases: a reset phase (clock low) and evaluation phase (clock high). During the reset phase the output comparator nodes are invalid because nodes P0 and P1 are pulled to V_{dd} through M7 and M10, which in turn applies a bias on M3 and M6 pulling both output nodes to ground. During the evaluation stage P0 and P1 discharge proportionally to the input voltages applied on the gates of M11 and M12. This determines the magnitude of the bias on M3 and M6, which controls the latched state of the inverter pair, indicating if V+ or V- is larger. This digital result is stored in the cross-coupled inverter pair until the next reset phase.

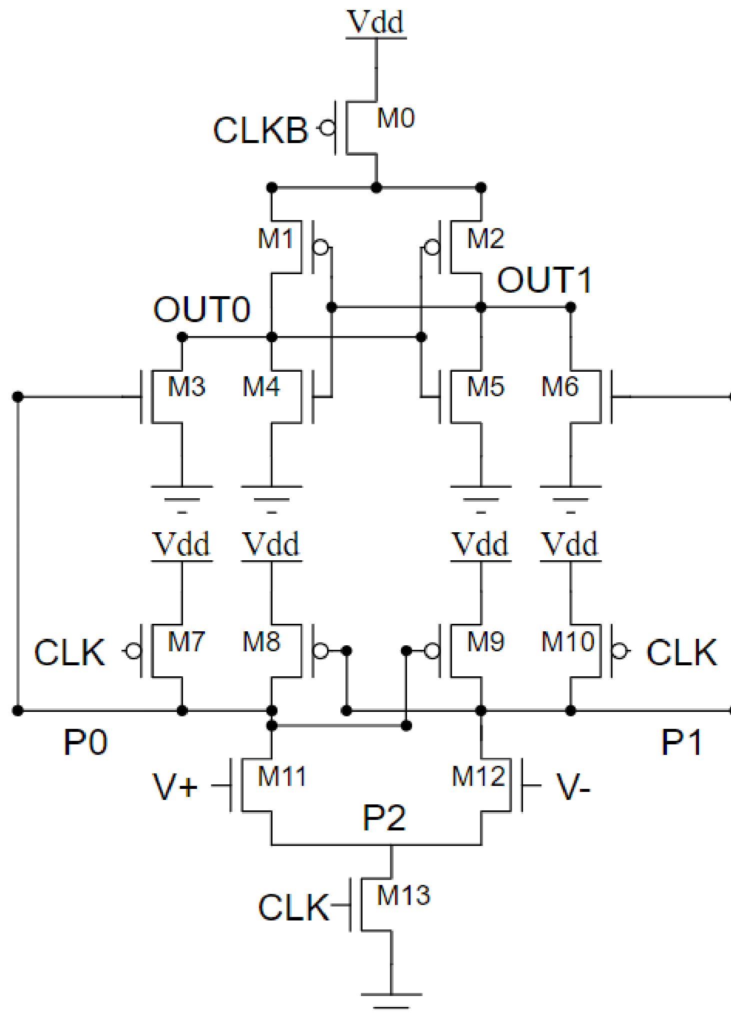


Figure 5.1.1 Baseline comparator design consisting of two stages. During reset phase (clock low) output voltages go low. During evaluate phase (clock high) the output voltages correspond to the values of V+ and V-, indicating, which voltage is of greater value [19].

To function within the given FADC system the comparator circuit must be able to quickly and reliably compare voltages. To do this, transconductance of key transistors is altered by increasing channel widths by several times more than the technology minimum. This in turn increases the transistor W/L ratio. These transistor sizing ratios are summarized in Table 5.1. The minimum technology W/L ratio is normalized to 1. The increased channel widths are illustrated by showing the multiplication factor from the technology minimum. Sample rate maximization is done through increasing the discharge rate of P0 and P1 to ground by increasing the channel widths

of the tail transistors, M11, M12, and M13, which reduces the resistance to ground and increases current flow. To ensure correct latching, P0 and P1 must not have a voltage offset when the evaluation stage begins. This is achieved by increasing the channel width of M7 and M10 to tie P0 and P1 to V_{dd} with no offset. To ensure correct conversion the drive strength of M8 and M9 must be increased to supply enough current to the tail transistors through an increase in channel width.

TABLE 5.1 COMPARATOR TRANSISTOR SIZING CHART

Sizing Chart	
Transistor	W/L Ratio
M0	4
M1	1
M2	1
M3	1
M4	1
M5	1
M6	1
M7	4
M8	6.25
M9	6.25
M10	4
M11	4
M12	4
M13	8

As the bias applied on V+ and V- decreases, the current flowing through M11 and M12 also decreases. When a minimal threshold is reached M11 and M12 enter cut-off and nodes P0 and P1 stop discharging through the tail transistors, which means that the comparator is no longer completing a voltage comparison. This effectively limits the input voltage range. To counter this, a second comparator design, Figure 5.1.2, is implemented. This design controls the latching of the inverter pair by charging P0 and P1 through PMOS transistors, rather than P0 and P1 discharging through NMOS transistors. Due to the use of NMOS and PMOS input gates a full rail-to-rail input

voltage range has been achieved. With the PMOS comparators handling voltages from ground to mid-rail and the NMOS comparators handling voltages from mid-rail to V_{dd}.

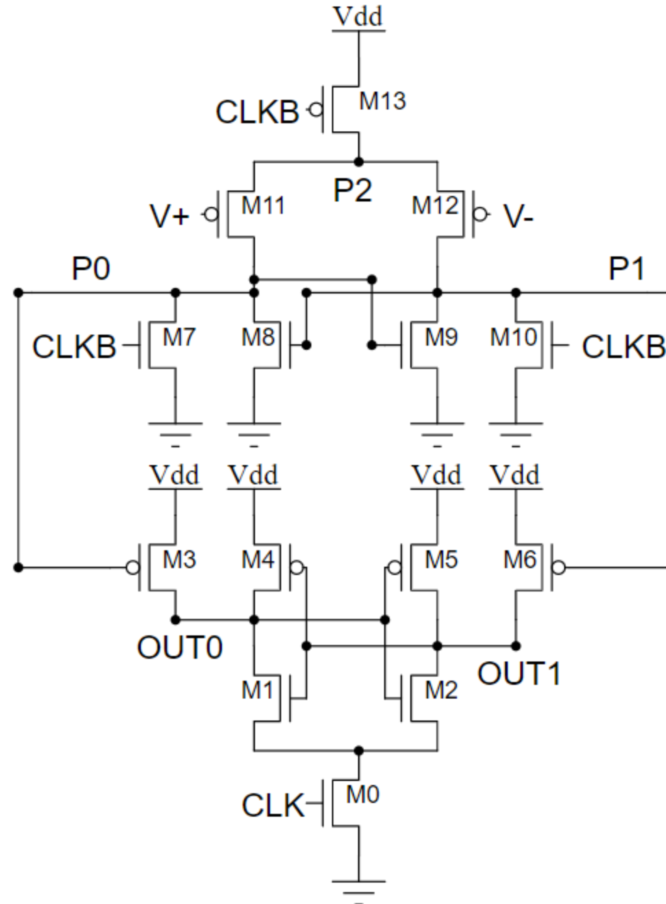


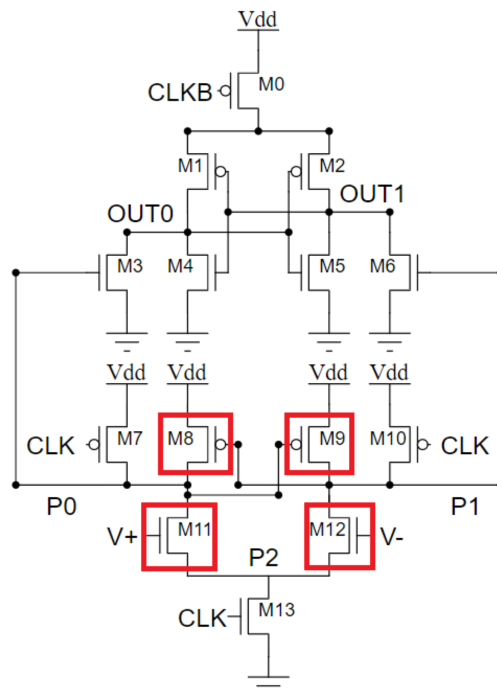
Figure 5.1.2. PMOS comparator design where current charges P0 and P1 to control latching rather than discharging. Rail-to-rail input voltage is created through the combination of these two designs because the NMOS comparator functions for input voltages from mid-rail to V_{dd} and the PMOS comparator functions from ground to mid-rail.

5.2 Clocked Comparator Vulnerabilities

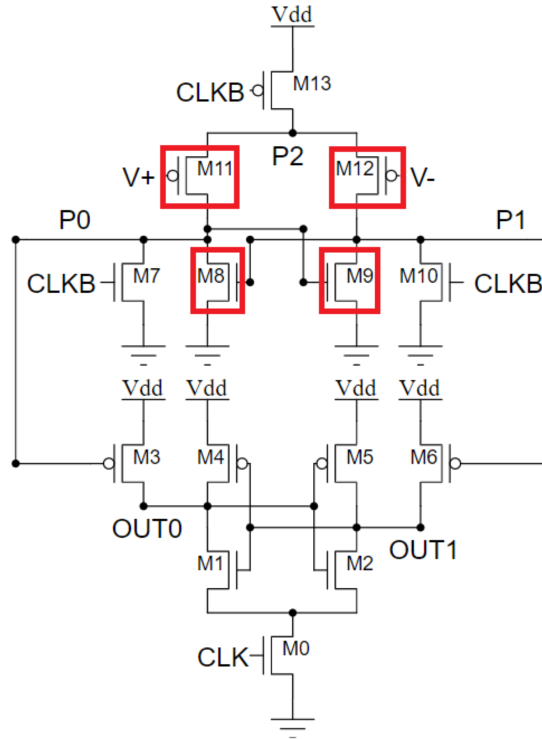
Single event analysis of the baseline comparator design has identified vulnerabilities due to ion strikes on transistors M1-M6, M8-M9 and M11-M12. An ion strike taking place on M1-M6 triggers a response like that of a SET taking place in an SRAM cell where the ion strike creates incorrect latching of data. However, in this case, when a SET takes place the voltages on nodes P0 and P1 provide redundancy and restore the digital states of OUT0 and OUT1; a SEU will only take

place if the output nodes are read into a DFF while the output perturbation is occurring, which is short (tens of picoseconds) compared to the clock cycle. This means that a SET taking place in the inverter pair does not present a significant vulnerability to ionizing radiation and is not mitigated.

When an ion strike takes place on transistors M8 or M9, charge is added to internal nodes P0 or P1 respectively for the NMOS topology and charge is removed for the PMOS topology. Similarly, P0 or P1 lose charge when an ion strike takes place on M11 or M12 for the NMOS topology and gain charge for the PMOS topology. In each case the biasing on transistor M2 or M5 is perturbed, which changes the digital state saved in the cross-coupled inverter pair leading to a SEU. This upset mechanism provides a significant vulnerability to ionizing radiation and must be mitigated. This vulnerability is illustrated by red boxes denoting the sensitive transistors for the NMOS and PMOS design shown in Figure 5.2 (a) and Figure 5.2 (b) respectively.



(a)



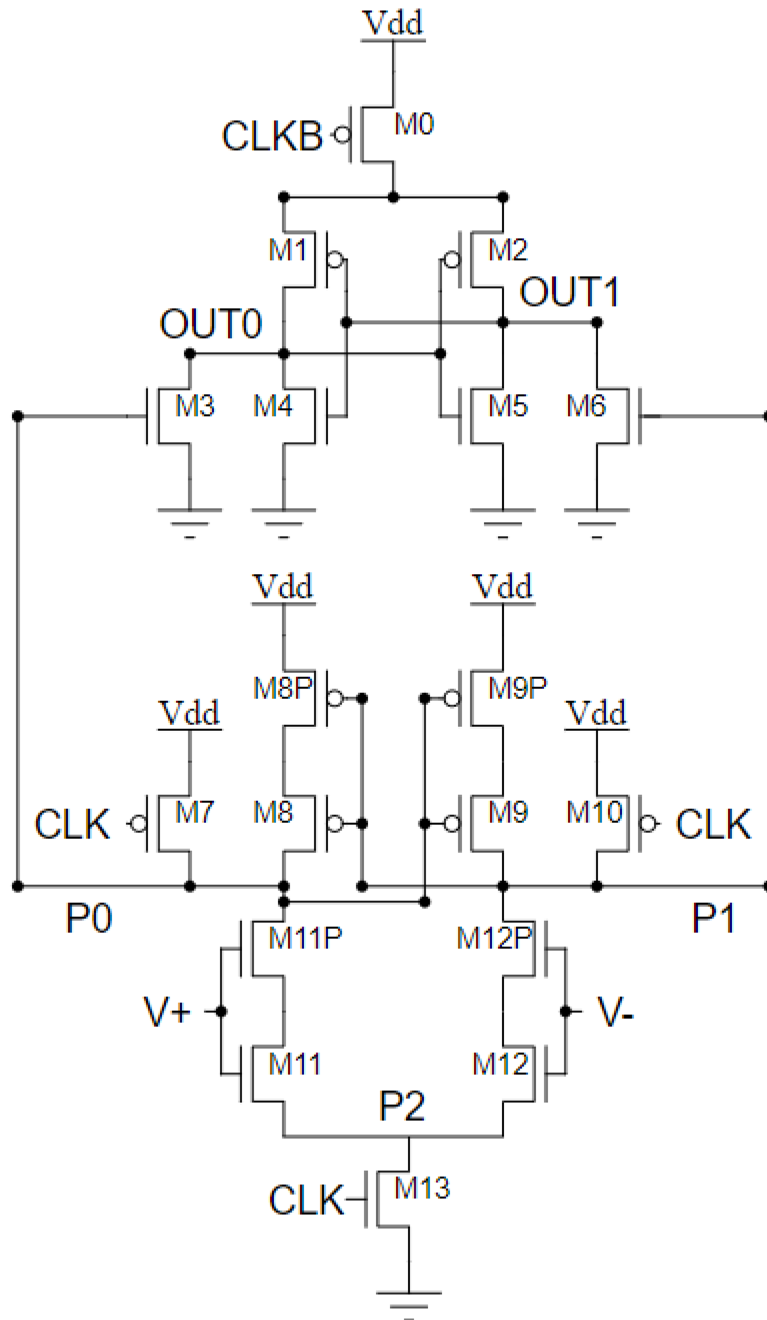
(b)

Figure 5.2. Ion strike taking place on boxed transistors M8, M9, M11, or M12, perturbs the bias on M3 or M6 leading to a SEU in the cross coupled inverters. (a) NMOS comparator topology (b) PMOS comparator topology

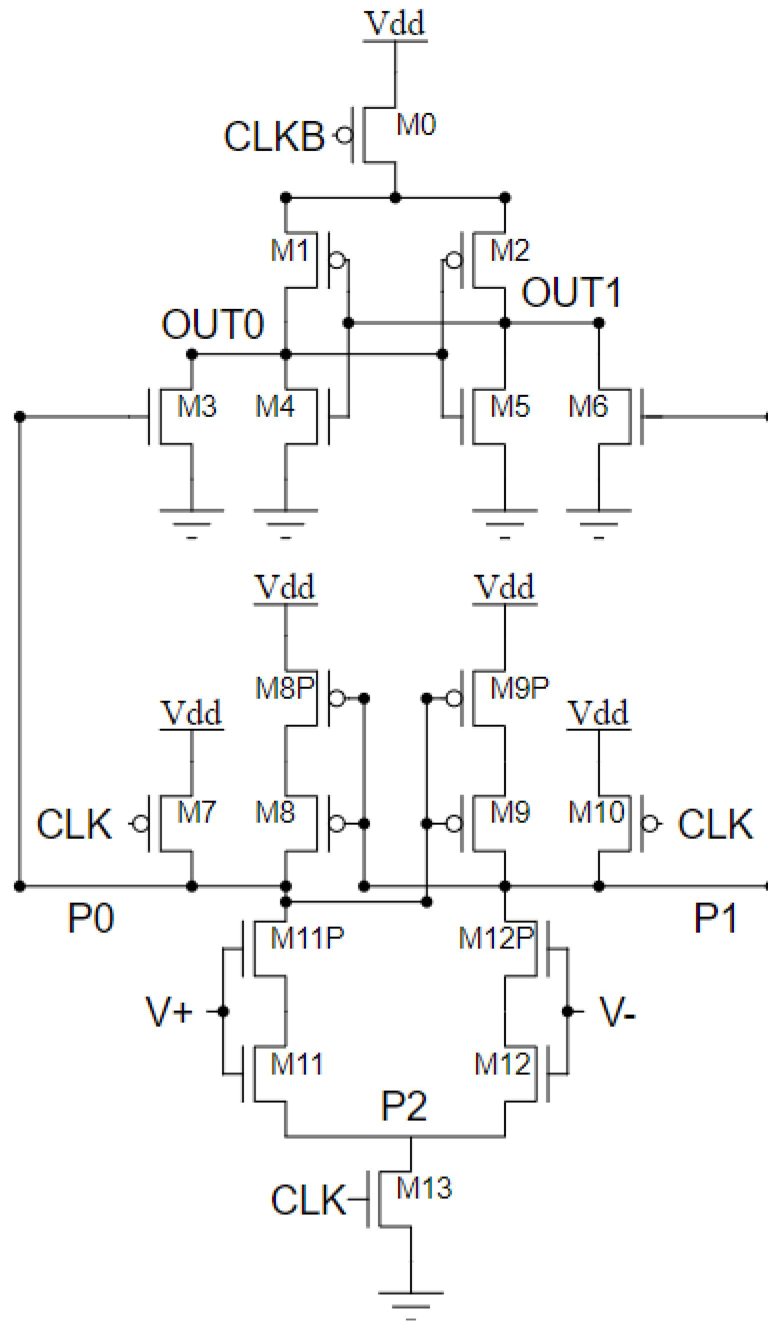
5.3 Clocked Comparator Hardening

The previously discussed vulnerability is mitigated through the application of device stacking [16], [17], which adds a redundant node by replacing a single transistor with two in series. In most cases if a single transistor is struck, the voltage will not be significantly altered. To create a SET with sufficient magnitude to generate a SEU, the energetic particle must intersect both transistors. When device stacking is applied to DFFs in the 32-nm SOI CMOS technology node, a several orders of magnitude decrease in cross section has been shown [20]. This technique is applied to M8, M9, M11, and M12 as shown in Figure 5.3 (a) for the NMOS topology and Figure 5.3 (b) for the PMOS topology. If a single-event strike takes place on any of the stacked transistors, the hardening method will create a circuit resistant to a voltage perturbation on P0 or P1, which

preserves the biasing on M3 or M6. If this biasing remains unperturbed, the upset mechanism which leads to a SEU has been eliminated.



(a)

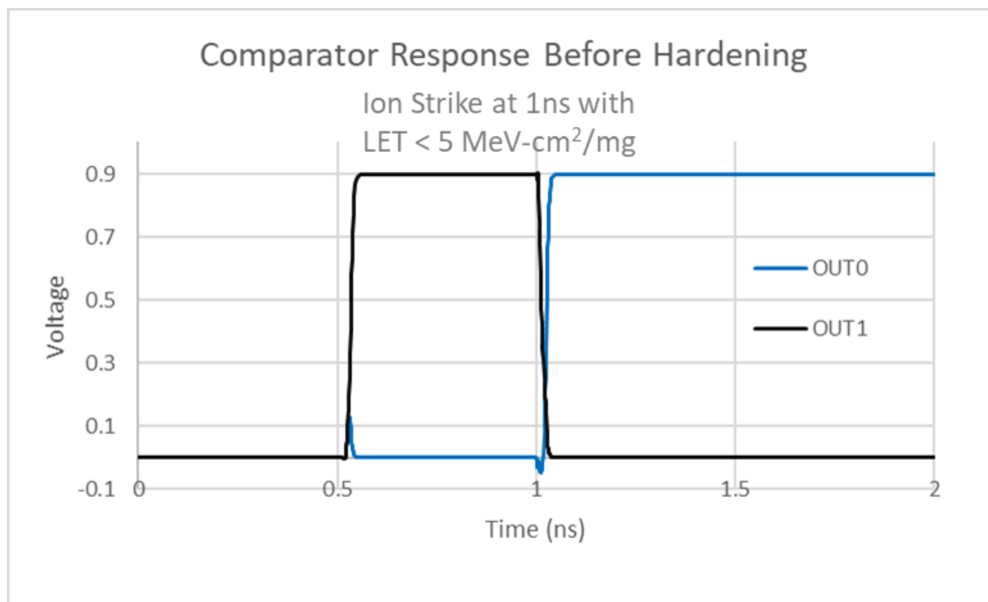


(b)

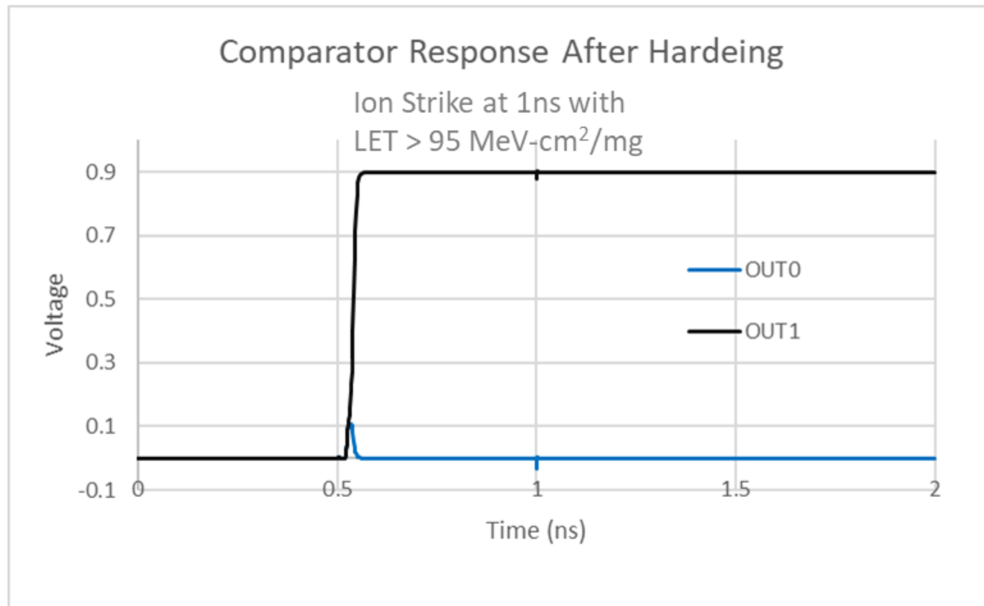
Figure 5.3. RHBD comparator design utilizing device stacking, addition of M11P and M12P, to mitigate an ion strike on M11 or M12, which affects biasing of M3 or M6 potentially creating a SEU. (a) NMOS stacked comparator topology (b) PMOS stacked comparator topology

5.4 Clocked Comparator Hardening Results

As illustrated in Figure 5.4, device stacking comparator hardening methods have shown a significant increase in radiation hardness to the effects of ionizing radiation. At time T0 the comparator is in the reset phase and both outputs are invalid. The evaluate stage begins at 0.5ns and the outputs display the voltage comparison result. An ion strike is simulated at 1ns as shown in Figure 5.4 (a). Before hardening a LET of less than 5 MeV-cm^2/mg upsets the comparator circuit. After hardening, as shown in Figure 5.4 (b), an ion strike with an LET above 95 MeV-cm^2/mg does not create an SEU. This corresponds to a significant increase in radiation hardness.



(a)



(b)

Figure 5.4 (a) Unhardened comparator response to a single-event strike with LET = 5 MeV-cm^2/mg (b) Radiation-hardened comparator response to a single-event strike with LET = 95 MeV-cm^2/mg

When analyzing speed, power consumption, and area, as summarized in Table 5.4, it is important to consider the effect of additional tail transistors on current flow. The additional stacked transistors are the same size as the original transistors, which increases the resistance to ground. However, the amount of charge, which must flow to ground for comparison remains the same. This reduces current flow, power consumption, and transistor switching speed, while increasing circuit area. If speed is a significant design consideration, the tail transistors can be scaled up to increase current flow and thus increase switching speed and power consumption. This would also further increase circuit area, which is why the additional transistors were kept at the same size, in order to conserve circuit footprint. The application of device stacking already incurs a significant design penalty in terms of area. Scaling the tail transistors would further increase this penalty.

Furthermore, even with the increased propagation delay the comparator circuit can still function at more than 500 MHz

TABLE 5.4 COMPARISON OF CLOCKED COMPARATOR PERFORMANCE ATTRIBUTES

Comparator Performance Attribute	Comparator Circuit	
	Unhardened	*Hardened*
Max Propagation Delay	1	2.63
Static Power Consumption	1	0.69
Dynamic Power Consumption	1	0.69
Circuit Space	1	2.10
Upset Threshold MeV-cm^2/mg	<5	>95

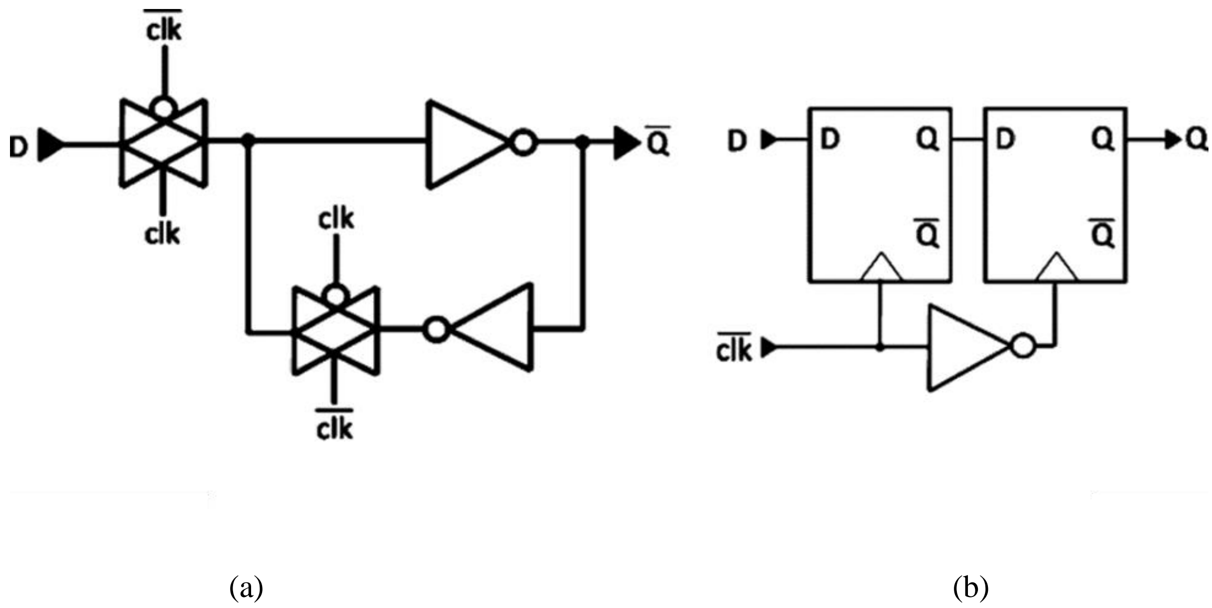
Chapter 6

LATCH DESIGN AND HARDENING

6.1 Latch Design

After completion of the comparator ladder and thermometer encoder stages, master-slave DFFs are placed to provide signal synchronization. This is due to variation in propagation delay between circuits. Propagation delays between the comparator circuits differ because propagation delay depends upon the applied gate voltage, which is different for each comparator. In the thermometer encoder circuit, the larger logic circuit of the Least Significant Bits (LSBs) creates propagation delays higher than that of the Most Significant Bits (MSBs), leading to a time delta between the output of the MSB and LSB circuits. To remove these temporal effects, DFFs use a 90-degree phase shifted clock, which synchronizes the data after the longest propagation delay has taken place.

The specific DFF design applied is a transmission gate D flip-flop (TG DFF). An example of a TG DFF is shown in Figure 6.1 (a) and (b) [21]. The basic latch design, Figure 6.1 (a), functions in two operational phases: clock high and clock low. When the clock is high the digital input at D propagates though the pass gate. When the clock goes low the digital state of D is isolated from the internal circuit node. The inverter pair stores the state of D at the clock edge, leading to $\overline{Q}$ being equal to the inverse of the clocked input state. When hooking these up in a master-slave configuration, as shown in Figure 6.1 (b), the output of the first latch circuit is connected to the input circuit of the second latch. This creates a memory circuit which stores the digital input state D in the first clock cycle and displays this state at Q in the next clock cycle.



(a) (b)

Figure 6.1. Transmission gate D flip-flop (a) basic latch design (b) two latches in master-slave configuration [21]

6.2 Latch Vulnerabilities

The master-slave TG DFF design has a similar upset vulnerability to that found in a SRAM cell, where a SET creates a voltage perturbation, which latches into a SEU. This vulnerability is best illustrated using Figure 6.1 (a). If a single-event takes place in the inverter pair, a SEU can be created which corrupts the digital value stored at node $\overline{Q}$. When this error propagates through the DFF to the output, Q will also be corrupted. When these circuits are applied to the FADC design, this error within the DFF can ultimately create an invalid data conversion.

6.3 Latch Hardening

This vulnerability is mitigated through the application of DICE latches. This idea is illustrated using Figure 6.3 [15]. This style of latch functions similarly to the latch design discussed in Section 6.1. During clock high, D propagates to the internal circuit nodes and during clock low the input state D at the clock edge propagates to the circuit output Q. The difference between the two circuits is in the response to ionizing radiation. The DICE design provides redundant storage

nodes which preserve the stored digital state when a single event takes place. Consider the situation where Q is high and $\overline{Q}$ is low and an ion strike takes place on N0. Charge will be pulled off Q leading to a voltage perturbation. However, after the strike, the redundant feedback paths from the other storage nodes will preserve the digital state and prevent a SEU from occurring. These additional nodes mitigate the SEU vulnerability.

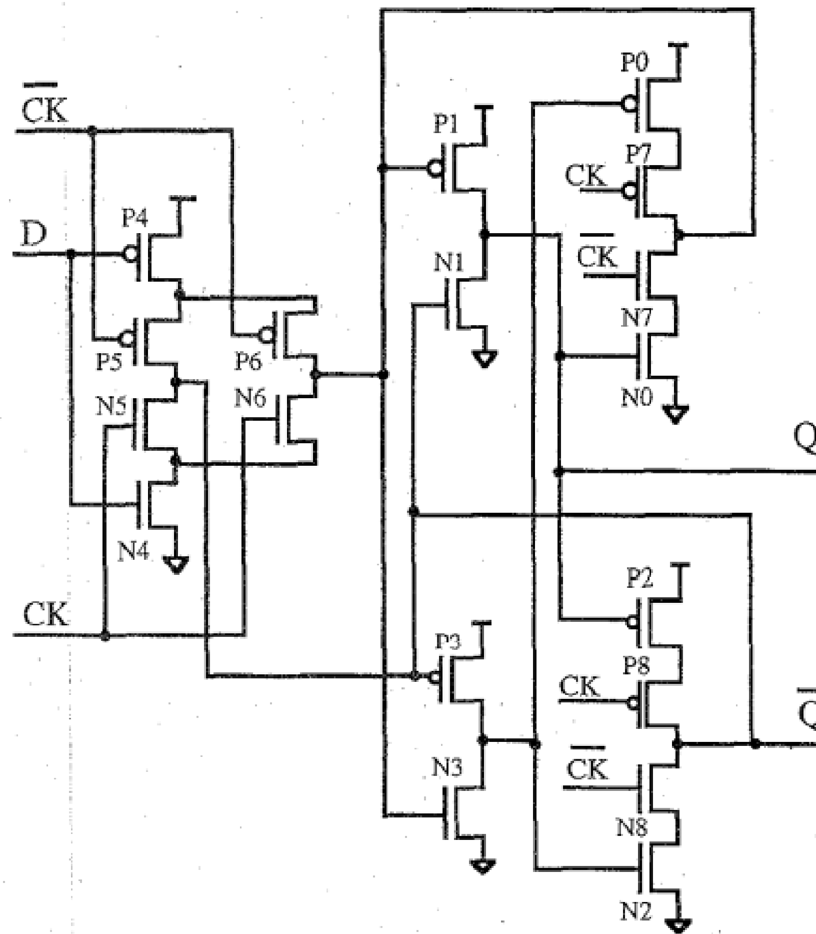


Figure 6.3. DICE latch cell that uses additional nodes to preserve stored data in the case of a single-event strike [15].

6.4 Latch Hardening Results

DICE flip-flop designs in sub 50-nm SOI technologies have provided a several order-of-magnitude reduction in SEU cross-section when compared to TG DFFs. This is shown in

Figure 6.4 using 32nm SOI DICE flip-flops [22]. These in silicon results were generated at Lawrence Berkeley National Laboratory (LBNL) and Texas A&M University (TAMU) using a perpendicular angle of incidence. The key comparisons are between the TG DFF noted by a red square and DICE DFF noted by the green circle. This experiment illustrates the advantages of DICE FFs within advanced SOI technology nodes and highlights why DICE designs have been applied in this work.

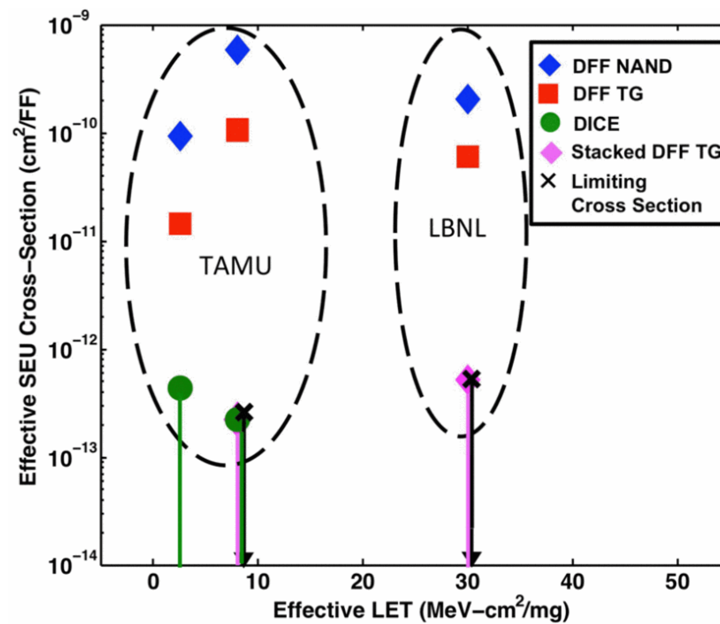


Figure 6.4. SEU cross section comparison for varying flip-flop designs. The key comparison is between the TG DFF and DICE design, highlighting a several order of magnitude improvement in effective cross section [22].

A simulated comparison using laid out DFF and DICE flip-flop circuits, developed at Vanderbilt, has shown tradeoffs between circuit performance and radiation hardness. The unhardened DFF design has SEUs occurring at LETs below 5 MeV-cm^2/mg, while the hardened DICE Flip-Flop design does not have SEUs occurring above 95 MeV-cm^2/mg. However, hardening techniques incur design penalties in terms of power consumption, speed, and area as displayed Table 6.4 below. The maximum design penalty is incurred upon circuit area with circuit

hardening making the flip-flop circuit around 2.5 times bigger. Speed is also significantly affected with the hardened circuit having about 2 times the propagation delay as compared to the unhardened circuit. Lesser penalties are incurred in terms of power consumption, with static and dynamic power consumption increased by about 38% and 75% respectively.

TABLE 6.4 COMPARISON OF FLIP-FLOP PERFORMANCE ATTRIBUTES

Flip-Flop Performance Attribute	Flip-Flop Circuit	
	Standard FF	*DICE FF*
Max Propagation Delay	1	2.13
Static Power Consumption	1	1.38
Dynamic Power Consumption	1	2.13
Circuit Space	1	2.81
Upset Threshold cm^2/mg	<5	>95

Chapter 7

THERMOMOTER ENCODER DESIGN AND HARDENING

7.1 Thermometer Encoder Design

The thermometer encoder translates the inefficient data representation of thermometer code to binary code using CMOS And-or-Invert Logic blocks which have been simplified using De Morgan's Theorem. The logical inputs I0-I14 come from the comparator ladder with each Ix representing one bit of thermometer code. The binary logical output is represented by Bit0-Bit3 for each bit is shown in Equations (1)-(4), with Bit3 representing the Most Significant Bit (MSB) and Bit0 representing the Least Significant Bit (LSB).

$$Bit0 = I0 \cdot \overline{I1} + I2 \cdot \overline{I3} + I4 \cdot \overline{I5} + I6 \cdot \overline{I7} + I8 \cdot \overline{I19} + I10 \cdot \overline{I11} + I12 \cdot \overline{I13} + I14 \quad (1)$$

$$Bit1 = I1 \cdot \overline{I3} + I5 \cdot \overline{I7} + I9 \cdot \overline{I11} + I13 \quad (2)$$

$$Bit2 = I3 \cdot \overline{I7} + I11 \quad (3)$$

$$Bit3 = I7 \quad (4)$$

7.2 Thermometer Encoder Vulnerabilities

When an energetic particle interacts with the logic nodes of the encoder circuit a SET is created, which temporarily perturbs the output state but does not create a SEU unless it becomes latched in subsequent circuitry. As these transient events do not permanently affect the encoder output state, they are not mitigated. The true vulnerability within the thermometer encoder is SEUs propagating to it from previous comparator or latch circuitry and creating an incorrect thermometer to binary code conversion. It is important to target these errors because even with comparator and latch hardening a SET can create a SEU in the latch and comparator circuits due to ions affecting

multiple transistors [23] or high LET incident ions. The key error propagation paths create bubble errors leading to data corruption in the most significant binary bits. Therefore, most significant bit correction is used to mitigate the most serious of these potential errors.

7.3 Thermometer Encoder Most Significant Bit Correction

When a SEU causes a bit flip to take place the affected bit may control one of the LSBs or MSBs. For example, if I14 is flipped, Bit0 which is an LSB, will become corrupted. This causes one data level to be lost. However, if I7 is flipped, Bit3 which is an MSB, will become corrupted. This causes half of the data levels to be lost. Hardening I14 has the same design penalty as hardening I7 but provides much less protection from level loss. Furthermore, LSBs are controlled by more thermometer encoder bits than MSBs. For example, Bit3 is controlled by 1 thermometer encoder bit, but Bit0 is controlled by 15 thermometer encoder bits. Hardening Bit3 requires significantly more hardening circuitry but provides a fraction of the radiation response. This means that relatively few bits can be hardened and provide a substantial improvement in radiation response. For this reason, MSBs were hardened by adding additional logic as displayed in Equations (5) and (6) to correct the most serious bubble error by comparing the value of Ix to I(x-1) and I(x+1). The application of this method to the MSBs reduces radiation hardening design penalties while providing substantial radiation hardness.

$$Bit2 = (I2 \cdot I3 + I2 \cdot I4 + I3 \cdot I4) * (\overline{I6 \cdot I7 + I6 \cdot I8 + I7 \cdot I8}) + (I10 \cdot I11 + I10 \cdot I12 + I11 \cdot I12) \quad (5)$$

$$Bit3 = I6 \cdot I7 + I6 \cdot I8 + I7 \cdot I8 \quad (6)$$

7.4 Thermometer Encoder Hardening Results

The performance of the following three encoder circuits are compared to quantize the effects of RHBD methods, 1) Baseline Design, which contains no additional circuitry to correct

bubble error, 2) MSB Correction, which contains circuitry to correct the most serious bubble error affecting the most significant bits, and 3) Full Correction, which has additional circuitry to correct bubble errors on all bits. The effects of bubble errors were simulated on each design. This was done through injecting predetermined vector inputs containing bubble errors. Then recording and comparing the output vectors as illustrated in Figures 7.4.1-7.4.4.

The first vector displayed in Figure 7.4.1, does not have a bubble error. The input thermometer code vector is summarized by I0-I14 and the binary code for each of the designs is then displayed after conversion from each thermometer encoder. Finally, a decimal number representative of the binary code value is displayed. When no error takes place all the thermometer encoder designs provide the same binary output.

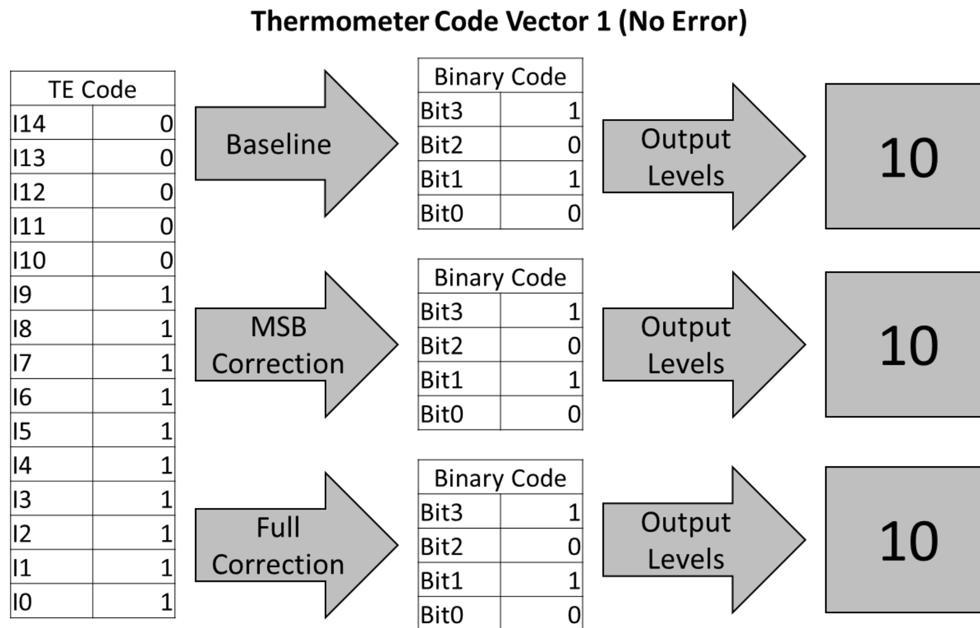


Figure 7.4.1. Comparison of thermometer encoder response with no error for Baseline, MSB Correction, and Full Correction designs. Displaying input thermometer code, resultant binary code, and correlating decimal output. All encoders complete a correct conversion.

The second vector, displayed in Figure 7.4.2, creates a bubble error affecting the most significant output bit. This example best displays the advantages of error correction. When no error correction takes place half of the output data levels are lost as shown by the Baseline design. However additional circuitry provided by the MSB Correction and Full Correction designs corrects this error and produces a correct data conversion saving half of the data levels.

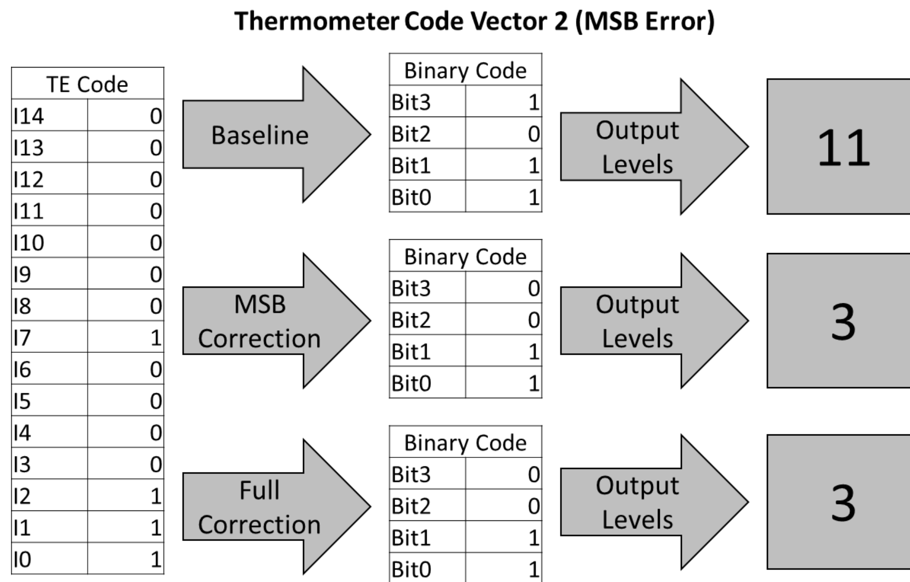


Figure 7.4.2. Comparison of thermometer encoder response with MSB error for Baseline, MSB Correction, and Full Correction designs. Displaying input thermometer code resultant binary code and correlating decimal output.

The third vector creates a bubble on the least significant bit, as displayed in Figure 7.4.3. In this case both the baseline and the MSB correction encoder designs lose one data level. Comparing the output results of the second and third vectors reveals the advantages of MSB correction. The second vector creates error which results in the loss of half the data levels when uncorrected. The third vector creates error which results in the loss of only one level if uncorrected. This demonstrates that the MSB correction encoder protects against the most serious errors.

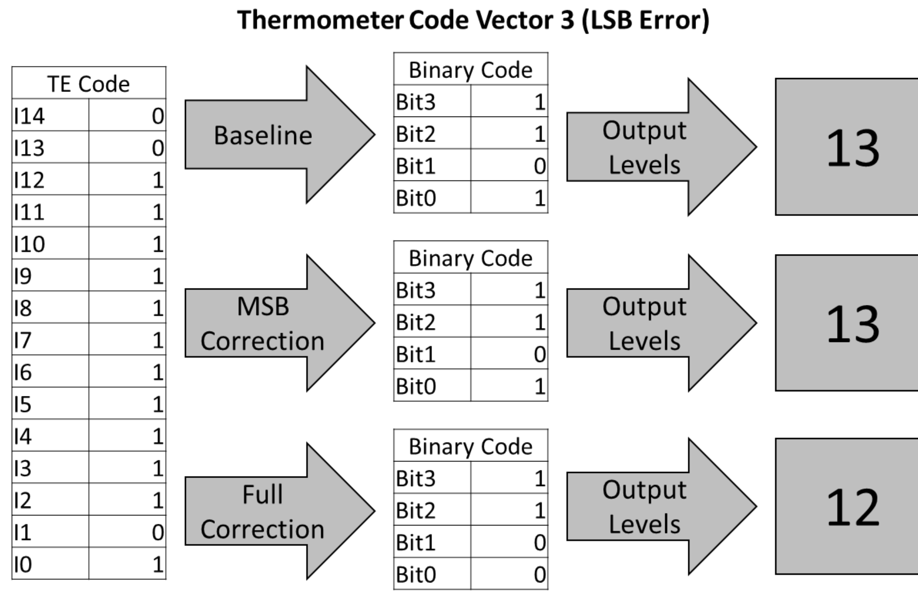


Figure 7.4.3. Comparison of thermometer encoder response with LSB error for Baseline, MSB Correction, and Full Correction designs. Displaying input thermometer code resultant binary code and correlating decimal output. Both the Baseline and MSB Correction design lose one data level while the Full Correction loses no data levels.

The final vector, displayed in Figure 7.4.4, creates a bubble error at the transition point, where the true value cannot be recovered. The fully hardened design detects a bubble and attempts to correct it, while the unhardened design does not attempt to detect or correct the bubble. Both either determine the intended value or lose one level of data, depending on what the true value is. However, the MSB encoder performs worse than the other two encoders, because the MSB encoder detects and attempts to correct the error in the upper bits but not the lower ones. This creates a situation where the maximum potential error of the MSB bubble encoder is the sum of the unprotected bits. Even though the MSB encoder performs worse than the baseline design in this situation, when all possible bubble error is simulated, on average the MSB design performs better than the baseline design.

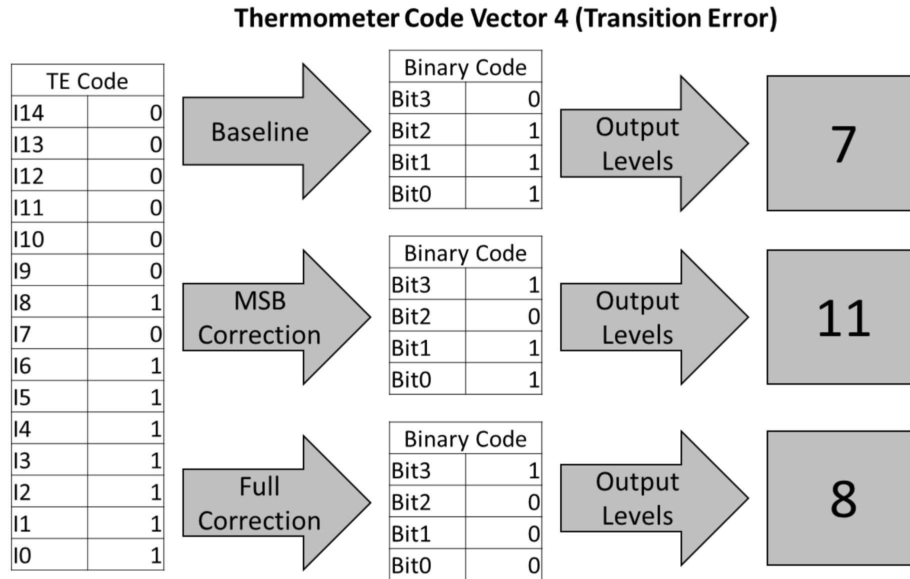


Figure 7.4.4. Comparison of thermometer encoder response with transition error for Baseline, MSB Correction, and Full Correction designs. Displaying input thermometer code resultant binary code and correlating decimal output. The true value cannot be recovered and the MSB Correction encoder has the worst performance.

There are situations where the MSB encoder performs worse than the unhardened encoder. To fully evaluate this operation, a program was written which simulates bubble error on every bit for each thermometer code input state. This program was applied to the logic of each encoder design and error detection and correction statistics were generated. These statistics verify that on average the MSB correction encoder design performs better than the baseline design. presented in Table 7.4.1, comparisons between the three encoder designs were created. It is important to note that errors in the full correction circuit are created through bubbles taking place at the 0 to 1 transition, which is an unrecoverable error state as discussed in Section 3.4. When a bubble error takes place, the output value is corrupted; this leads to a given number of quantized output levels being lost. The MSB correction circuit performs better than the baseline encoder, but worse than the fully hardened design for average data loss due to bubble error. For the maximum data loss, the number of lost levels is reduced from half to a quarter of the levels. If bubble error is masked,

the error does not reach an output node and does not result in an error in the final output. Without any correction a bubble will be masked 50% of the time. The MSB correction encoder only provides minimal improvement, but the 6% that is corrected is in the most significant bits.

TABLE 7.4.1 COMPARISON OF THERMOMETER ENCODER ERROR CORRECTION PERFORMANCE

Encoder Performance Attributes			
Correction Scheme	Avg. # of Levels Lost	Max Level Loss	Masked
No Correction	1.12	8	50%
MSB Correction	.8	4	56%
Full Correction	.32	1	81%

Circuit performance comparisons are displayed in Table 7.4.2. Maximum propagation delay is not significantly affected by additional hardening. Dynamic switching power consumption is affected with the MSB correction circuit drawing about 10% more power and the Full Correction circuit drawing around 30% more power. The main advantage of selected hardening is in terms of circuit area: the MSB correction circuit is about 1.25 times bigger while the Full Correction circuit is over 2.5 times bigger.

TABLE 7.4.2 COMPARISON OF THERMOMETER ENCODER PERFORMANCE ATTRIBUTES

Encoder Performance Attribute	Thermometer Encoder Circuit		
	Design	*MSB Correction*	*Full Correction*
Max Propagation Delay	1	1	1.08
Static Power Consumption	1	1	1
Dynamic Power Consumption	1	1.11	1.33
Circuit Space	1	1.26	2.56

Chapter 8

FLASH ANALOG-TO-DIGITAL CONVERTER HARDENING AND RESULTS

8.1 Flash Analog-to-Digital Converter Hardening

When constructing the final RHBD FADC it is important to note which hardening method is applied to each sub circuit as summarized in Figure 8.1.1. In this work, the voltage reference circuit is not targeted for hardening and is colored grey. Green colored sub circuits have additional circuitry to protect from electrical errors due to incident ions. This method is applied to the comparator ladder and synchronization DFFs. The thermometer encoder uses MSB error correction as indicated by blue coloring.

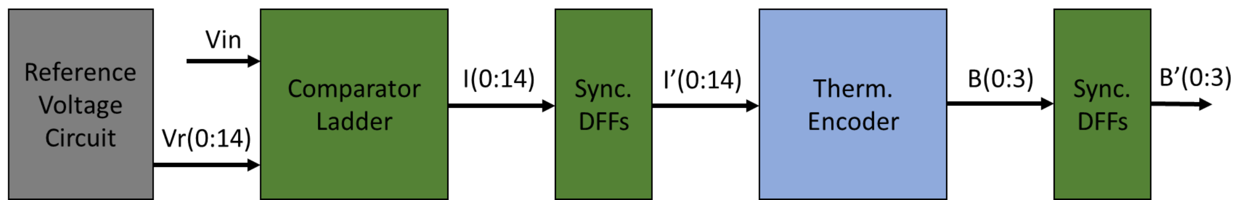


Figure 8.1.1. Flash Analog-to-Digital Converter Block Diagram highlighted to emphasize hardening approach: Grey uninvestigated, Green circuit level protection from SEU, Blue application of MSB correction.

The MSB FADC circuit schematic, as shown in Figure 8.1.2 closely resembles the FADC schematic provided in Figure 2.4.1. The MSB FADC provides an additional bit of resolution which requires added circuitry. Not all this additional circuitry is displayed in the schematic below. Instead a condensed representative resistor and comparator ladder is shown. The synchronization flip-flops read the outputs of key circuits using a 90-degree phase shifted clock. The application of selective hardening to protect the MSBs has also altered this FADC design. Within the comparator ladder and DFF stages, both hardened and unhardened circuit components are applied. In the thermometer encoder, implemented using And-or-Invert logic, additional circuitry exists to correct the most serious radiation errors.

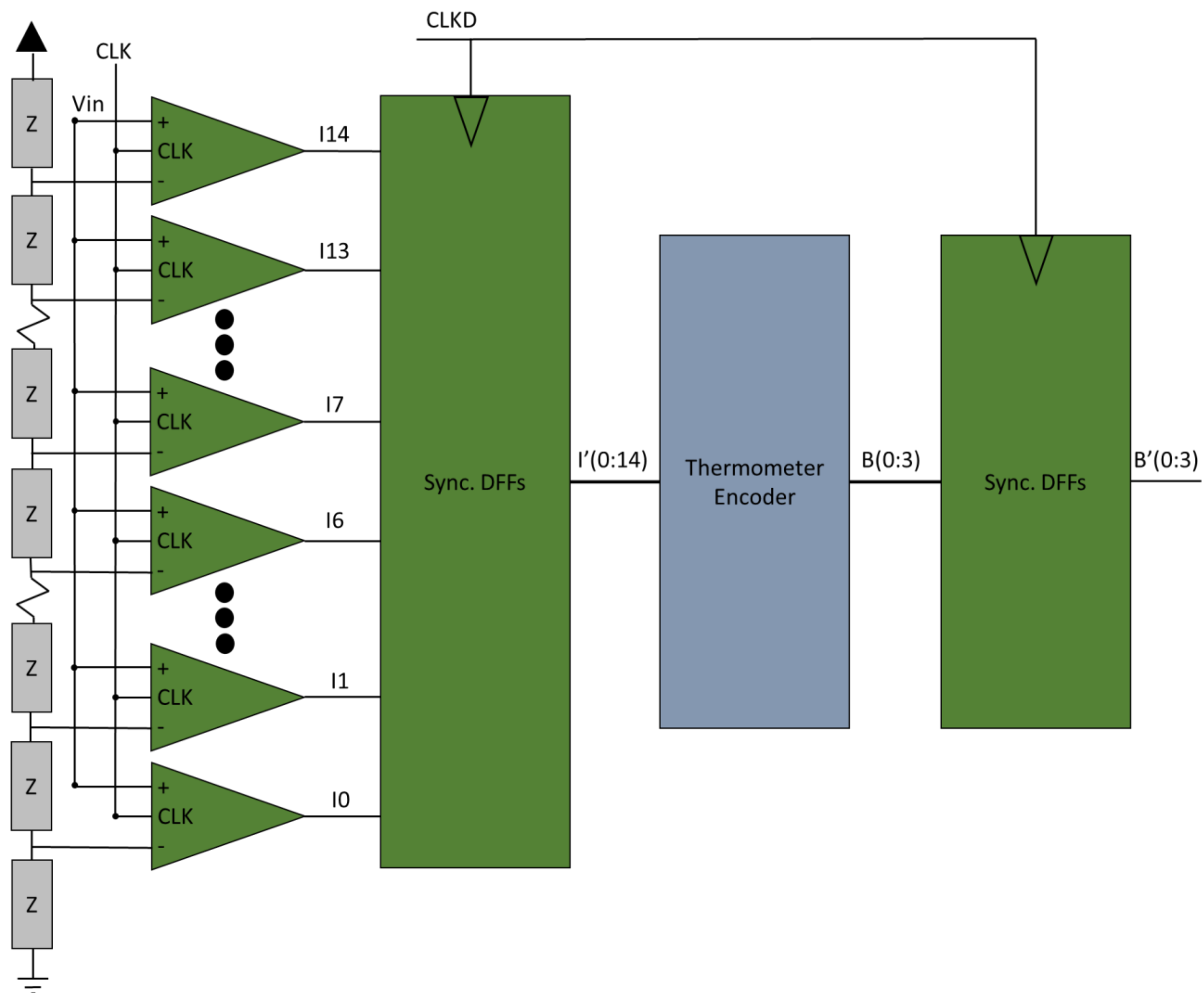


Figure 8.1.2. Schematic of MSB FADC

The MSB FADC Design focuses on protection and correction of the most significant bits. Protection of the most significant bits is done by applying the hardened comparators and latches to the circuits which determine the most significant bits and using the unhardened topologies for the other portions of the circuit. The application of this method is illustrated in Table 8.1. Each stage of the FADC is summarized. For each stage the left column denotes the circuit which controls a given thermometer code or output bit and the right column denotes the circuit topology. For example, in the comparator stage each thermometer code bit I0-I14 is in the left column and the

comparator type is in the right column. This application of hardening protects the circuit from the most significant radiation error while reducing the number of hardened circuit components.

TABLE 8.1 APPLICATION OF HARDENED AND UNHARDENED CIRCUIT COMPONENTS

FADC Stage					
Comparator Ladder		TE Clocking Stage		Output Clocking Stage	
TE Code	Type	TE Code	Type	Output Bit	Type
I14	Unhardened	I14'	DFF	Bit 3	DICE FF
I13	Unhardened	I13'	DFF	Bit 2	DICE FF
I12	Stacked	I12'	DICE FF	Bit 1	DFF
I11	Stacked	I11'	DICE FF	Bit 0	DFF
I10	Stacked	I10'	DICE FF		
I9	Unhardened	I9'	DFF		
I8	Stacked	I8'	DICE FF		
I7	Stacked	I7'	DICE FF		
I6	Stacked	I6'	DICE FF		
I5	Unhardened	I5'	DFF		
I4	Stacked	I4'	DICE FF		
I3	Stacked	I3'	DICE FF		
I2	Stacked	I2'	DICE FF		
I1	Unhardened	I1'	DFF		
I0	Unhardened	I0'	DFF		

The circuit layout was constructed in the Cadence Virtuoso environment. This layout resembles the block diagram for the FADC circuit, Figure 8.1.1. The first block is the comparator ladder which was constructed by placing the comparators in rows of four creating a roughly square layout. Next, the first set of synchronization flip-flops were placed on top of one another to clock the output of the comparator ladder. To the right of the synchronization flip-flops, the thermometer encoder was placed. The output of the thermometer encoder was again fed into vertically stacked flip-flops. This created a layout with a rectangular footprint. This design was done for the simplicity of interconnections between circuit nodes and was not optimized for space as it is being used for demonstration purposes.

8.2 Flash Analog-to-Digital Converter Results

This section provides verification that the MSB FADC meets design requirements: maximizing sample rate, providing adequate sample resolution and providing resistance to the effects of ionizing radiation. As can be seen in Figure 8.2, the FADC functions at a clock frequency of 500MHz while providing 16 levels of data resolution. This is demonstrated by creating a sine wave input and recording the resultant binary output vectors. These vectors are used to reconstruct the sine wave in post processing. This reconstructed sine wave has been laid over the original input function. The representative value from the FADC output closely matches the input sine wave value. It is important to note that the representative signal is directly reconstructed from analog outputs which results in perturbations due to phenomena such as clock feed through.

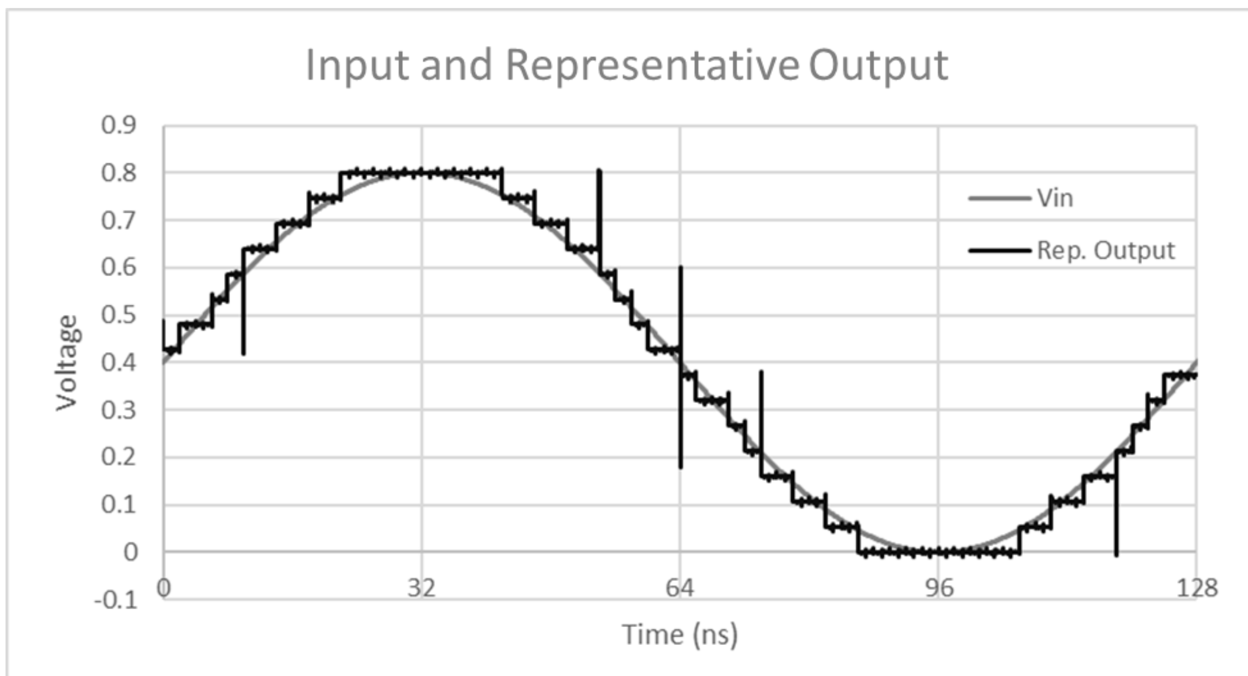


Figure 8.2 Input and Representative Voltage output plotted, shows functionality of FADC with 16 voltage levels functioning at 500MHz.

Results in Table 8.2 compare the performance attributes between three FADC designs: 1) “Baseline Design”, the design without hardening applied, 2) “MSB Correction”, the design which

implements selectively hardened circuit components and MSB correction, and 3) “Fully RHBD”, the fully radiation hardened design applying hardened comparators, flip-flops and error correction on every bit. These results were generated using data from parasitic extracted circuit components. Maximum propagation delay was determined by finding the largest propagation delay from the components within a FADC. Power consumption and circuit area were calculated by summing the attribute value for all FADC sub circuits. Selected radiation response data is tabulated from previous sections.

The maximum propagation delay is determined by the comparator circuit, which increases this metric for both the MSB fully RHBD circuit by about 2.5 times over the baseline design. Average power consumption is dominated by the clocked comparators, because they consume substantially more power than the rest of the circuit components. The MSB design performs between the other two designs drawing about 20% less power than the baseline design but drawing about 10% more power than the fully hardened circuit. This is due to the increased resistance to ground within the comparator circuit as discussed in Section 5.4. Every circuit component contributes to circuit space, with the MSB correction circuit using 60% more space than the unhardened design, while the fully hardened design uses more than double the space. It is important to note that changing the tail transistor sizing, as discussed in section 5.4, will alter these results. If the comparator design was modified to use larger tail transistors, current flow would increase and maximize switching speed. However, power consumption and circuit area would also increase. In this work, this additional scaling was not applied to conserve circuit area design penalties as the FADC can still function at more than 500MHz. Radiation response of the MSB correction design also performs between the other two designs. With the number of data levels lost and protected circuit components falling between the other two topologies.

TABLE 8.2 COMPARISON OF FADC PERFORMANCE ATTRIBUTES

FADC Performance Attribute	FADC Circuit Performance		
	Baseline Design	*MSB Correction*	*Fully Hardened*
Max Propagation Delay	1	2.63	2.63
Static Power Consumption	1	0.81	0.69
Circuit Space	1	1.63	2.19
Max % Data Loss From Bubble Error	50%	25%	6%
% SEU Protected Comparators	0%	60%	100%
% SEU Protected DFFs	0%	58%	100%

Chapter 9

CONCLUSIONS

Ionizing radiation creates SETs in FADC circuits, which can become latched resulting in SEUs. This ultimately leads to incorrect analog-to-digital conversions. Previous work has focused on comprehensive RHBD methods [1], creating large correction circuits. This work presents an efficient method for mitigating SEU errors with reduced circuit complexity through protecting only the circuitry related to the most significant bits and correcting the most significant errors. These circuits have been simulated using data verified models and show increased radiation hardness with less impact upon circuit performance. This radiation hardening technique is also scalable to FADCs using more bits. As the number of ADC output bits increase, the number of comparators will also increase but comparator design will remain unchanged. The thermometer encoder design is also scalable because the principles of MSB error correction remain the same even when a larger FADC is used. This provides a robust FADC, scalable to various ADC output bits, for use in the single-event radiation environment.

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