Electrical Engineering

SE Response of Guard-Gate FF in 16-nm and 7-nm Bulk FinFET Technologies

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Dissertation under the direction of Professor Bharat Bhuva

With scaling of CMOS technology, single event effect (SEE) has become more and more significant due to the increasing packing density and the reducing supply voltage and node capacitance. Therefore, radiation hardened by design (RHBD) technology become even important for design engineers working at advanced technology nodes. In this work, a Guard-Gate Flip-Flop (GG-FF) design with improved single event reliability (SER) has been investigated. Design was implemented with conventional D-FF in 16-nm and 7-nm bulk FinFET technologies. Tests were carried out with alpha particles, neutrons and heavy ions with different supply voltages, operating frequencies and linear energy transfer (LET) of particle. The GG-FF design did not show any upset with alpha particles at nominal supply voltage for both technology nodes. The SE performance of GG-FF show improved performance compared to D-FF at both 550 mV and 750 mV for 7-nm node with fast neutron. Heavy-ion test results show that even at high operating frequency, the SER of Guard-Gate (GG) design is more excellent than conventional D-FF design. The heavy-ion test results have also been used to evaluate the single-event transient (SET) pulse with distribution at different technology nodes.

Approved:
Bharat L Bhuva, Ph.D.

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SE RESPONSE OF GUARD-GATE FF IN 16-NM AND 7-NM BULK FINFET

TECHNOLOGIES

By

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1. INTRODUCTION

Following Moore's Law in the past few decades, the integrated circuit (IC) industry has made significant progress to accomplish the goals of lower cost, better performance and higher efficiency. The number of transistors in a dense integrated circuit doubles roughly eighteen months [1]. Fig. 1.1. shows the Moore's 1965 prediction of the doubling of the number of "minimum cost" components on a chip each year.

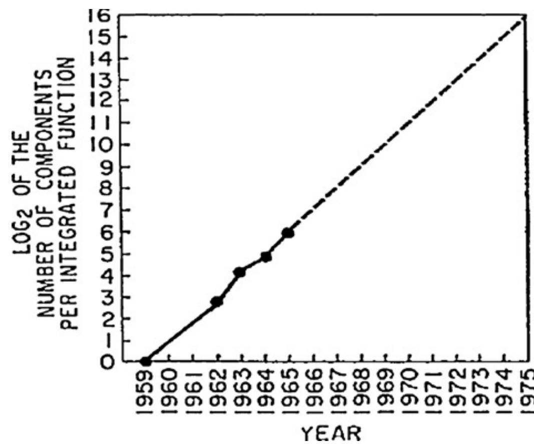


Figure 1.1: Moore's 1965 prediction of the doubling of the number of "minimum cost" components on a chip each year, based on historical data and extrapolated to 1975 [1].

Scaling down of CMOS technology is considered the key to sustain Moore's Law. With scaling down of CMOS technology, the IC supply voltage is steadily decreasing associated with reduction in the critical charge of a cell. Meanwhile the packing densities are increasing due to scaled geometry. Therefore, IC designs are

getting more susceptible to single-event upsets (SEU) [2-4]. With scaling of minimum geometries and supply voltages on an integrated circuit (IC), the critical charge of a storage cell is steadily decreasing. Meanwhile the packing densities are increasing due to scaled geometry. These factors have made electronic systems highly susceptible to single-event upsets (SEU) [2-4]. Mitigation of these upsets requires performance penalties in terms of increased power, cell delays, and/or area. Depending on the target environment (and design specifications), designers manage these performance penalties by employing appropriate mitigation techniques. For space environment, designers use spatial redundancy-based hardening approaches, such as Dual Interlocked Cell (DICE), or Triple Modular Redundancy (TMR) based FF. Such designs reduce single-event error rates (SER) to extremely low levels [5-9]. Improvement in SER to such levels comes at a steep increase in performance penalty, making them unsuitable for applications with more relaxed specifications, such as those for terrestrial applications.

Unlike space applications, where SER needs to be extremely low, terrestrial applications only need to lower SER to a manageable level. Designers are also cognizant of the need for lower power and speed penalties. As a result, many FF designs, such as Schmitt-trigger-based FF, GG-based FF, Recombinant-Collected-charge-based FF, Hysteresis-based FF, etc. have been proposed with improved SE performance at a reduced level of performance penalties [8, 10-14]. SE performance of these FF designs vary with scaling of FinFET nodes due to changes in the physical

structure of transistors and the resultant changes in charge collection after an ion hit. As a result, it is important to evaluate SE vulnerability of these FF designs at each technology node as TCAD simulations are not sufficiently accurate. The main focus of this paper is to compare SE performance of D-FF and GG-FF designs at each technology node.

This work mainly focusses on the SEE on 7-nm and 16-nm bulk FinFET FF designs. Therefore, having a thorough understanding of the charge deposition and collection mechanism in transistor and SEU mechanisms in FF is of great importance.

Due to Coulomb scattering, when an energetic particle pass through a semiconductor device, excess electron-hole pairs in the semiconductor will be generated. When a particle strikes a microelectronic device, the most sensitive regions are usually reverse-biased p/n junctions [3]. Fig. 1.2 illustrates the SET induced by energetic ions injection and the subsequent charge collection by drift and diffusion in a reverse biased p-n junction [15]. Fig. 1.2(a) shows the generation of a cylindrical track of electron-hole pairs along the energetic ion passage. Fig. 1.2(b) shows after an ion strike, the carriers generated in the drain region will be quickly collected by charge drift, creating a large current transient at first place. Fig. 1.2(c) shows that after the collection of charge in the drain, the charge generated in device subtract will transport to the p-n junction by diffusion and be collected due to the electric field. In such condition, diffusion dominates the carriers' collection process,

which usually takes a longer than charge drift. Generally, the farther the event occurs away from the depletion region, the less charges will be collected. It is also concluded that the reverse-biased junction is the most charge-sensitive part of

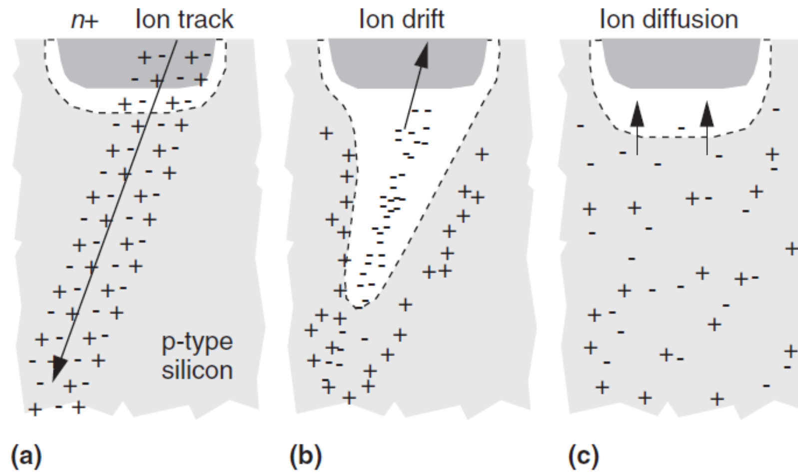


Figure 1.2: Charge generation and collection in a reverse-biased junction: (a) formation of a cylindrical track of electron-hole pairs, (b) funnel shape extending high field depletion region deeper into substrate, (c) diffusion beginning to dominate collection process [15].

circuits, because a high electric field is created in this region. The charge collection after an ion strike in FinFET structure is shown in Fig. 1.3. For a FinFET node, however, charge collection for ion hits outside drain region is different than that for a planar node. For a FinFET drain region, an ion hit away from the drain region will deposit charge in the substrate region below the isolation oxide. This substrate region is connected to the drain region through a narrow neck region that restricts charge transport, resulting in a decrease in charge collection from the substrate

region (FinFET nodes have been shown to experience diminished charge-sharing effects compared to that for planar nodes [16, 17]).

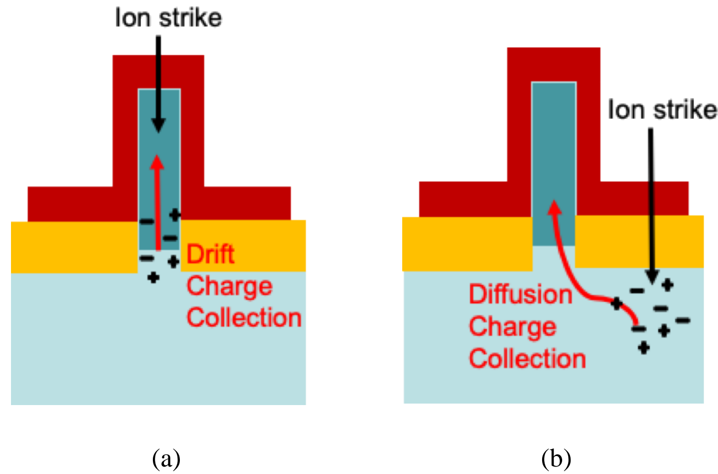


Figure 1.3: Charge collection mechanisms in FinFET structure. (a) Charge collected by charge drift when ion strike directly on the drain, (b) Charge collected by charge diffusion when ion strike away from the drain.

In this work, SER for alpha particles, fast neutron and heavy-ion exposures for GG-FF and conventional D-FF at the 16-nm and 7-nm bulk FinFET nodes are presented. Tests were carried out under a wide range of supply voltages, frequencies, and particle LET values. Results for low-LET particle exposures for GG-FF at 16-nm and 7-nm nodes show better SE performance than that for D-FF. For high-LET particles, results for 16-nm node show comparable SE performance for GG-FF and D-FF, but results for 7-nm node show better SE performance for GG-FF than D-FF. Since all the transistors on the IC were fabricated in the same progress, the charge collection are identical for the sensitive nodes of both D-FF and GG-FF is assumed. The main reason for their performance difference is due to the increased percentage

of short SET pulses at the 7-nm node across the tested particle LET range. The difference in D-FF and GG-FF SE cross-section is used to estimate the number of short pulses as a function of particle LET value. The SER performance of different designs was also evaluated with respect to power consumption and operating frequency to allow design engineers to optimize radiation resiliency.

2. GUARD-GATE FF

Guard-gate (GG) (or C-element or Mueller cell) has been used in logic circuits to compare two digital signals [13,14,18-23]. For this cell, both input signals must match for the output to switch. If inputs do not match, the output is left in floating condition (for CMOS circuits, this means the output will retain its value for a short time). Previously, researchers have used this configuration in a conventional D-latch by replacing one of the inverters by a GG with a delay cell on one of the inputs [14,18-24]. For such a latch design (shown in Fig. 2.1), the presence of an SET at the input of GG

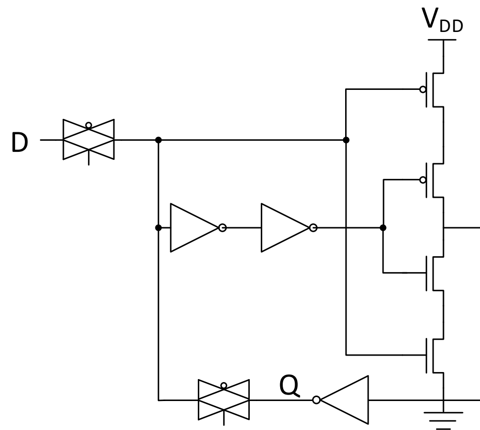


Figure 2.1: Schematic design of a GG-latch.

results in mismatched inputs for the GG as long as the SET pulse-width is shorter than the delay of the delay cell. Under such a scenario, the output of the GG floats

for the duration of the SET pulse, thereby preventing the SET from propagating through the latch. Same scenario results for any SET generated within the delay cell. Similar designs have been used at the outputs of combinational logic circuits also to eliminate SET pulses [14]. As the GG eliminates all SET pulses shorter than the delay of the delay cell and the number of short SET pulses is significantly higher than that for long SET pulses, significant improvement in SER is observed for GG-based FF over conventional D-FF designs. The improvement in SER will be proportional to the percentage of short SET pulses for a given technology. For FinFET technologies, the narrow neck region connecting drain with substrate results in reduced charge collection after an ion hit, and subsequently shorter SET pulses compared to planar technologies [25]. As a result, the improvement in SE performance for GG-FF over D-FF will be better for FinFET nodes compared to planar nodes.

GG-FF used in this study is shown in Fig. 2.2. For this latch design, all sensitive

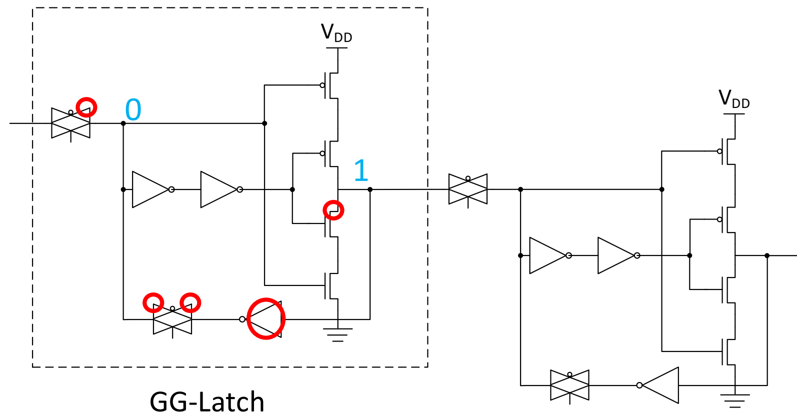


Figure 2.2: Schematic design of a GG-FF.

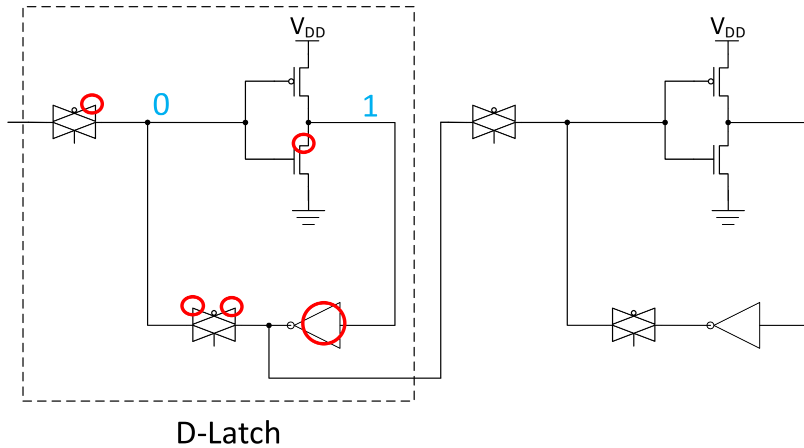


Figure 2.3: Schematic design of a conventional D-FF.

regions for input 0 are shown. Similarly, Fig. 2.3 shows sensitive regions for input 0 for a conventional D-latch. The sensitive regions in GG-latch consist of three regions in the pass gate (both source and drain of the PMOS in the opened pass gate and the drain of the PMOS in the closed pass gate), one region in the feedback inverter, and one region in the GG, as shown by red circles in Fig. 2.2. Similarly, for

the D-latch, the sensitive regions are shown in Fig. 2.3. Assuming similar size transistors (similar size drain and source regions), total sensitive area for both of these designs will be similar. However, SE upset cross-section will be different because GG-latch will eliminate more SET pulses compared to that for D-latch.

The difference in measured SE cross-section between these two designs can also be used to estimate the number of SET pulses that are shorter than the feedback-loop delay of the GG-latch. Additionally, by varying the supply voltage (and subsequently the delay of the delay cell and SET pulse widths), researchers will be able to estimate relative increases in gate delays and SET pulse widths. Such an estimation will allow designers to understand the effects of reducing power supply on effectiveness of GG-based mitigation approaches in logic circuits [14].

Table I: Normalized performance, transistor number and delay comparison for the conventional D-FF and GG-FF designs at different technology nodes. (Performance data normalized to the D-FF at nominal V_{DD} at 7-nm node, transistor number and delay data normalized to the D-FF).

<table>
<tr><th colspan="3"></th><th>D-FF</th><th>GG-FF</th></tr>
<tr><td rowspan="4">Power Consumption (n. u.)</td><td rowspan="2">Nominal V_{DD}</td><td>16-nm</td><td>1.66</td><td>2.78</td></tr>
<tr><td>7-nm</td><td>1.00</td><td>1.34</td></tr>
<tr><td rowspan="2">Reduced V_{DD}</td><td>16-nm</td><td>0.59</td><td>0.88</td></tr>
<tr><td>7-nm</td><td>0.28</td><td>0.41</td></tr>
<tr><td colspan="3">Number of Transistors (n. u.)</td><td>1</td><td>1.33</td></tr>
<tr><td colspan="3">Clock-to-Q delay (n. u.)</td><td>1</td><td>2.14</td></tr>
</table>

The performance of GG-FF and D-FF was simulated with the 7-nm FinFET transistor models from the Arizona State University Predictive Technology Model.

Table I shows the normalized performance comparison for the conventional D-FF and GG-FF designs at both technology nodes, and the transistor number and delay comparison for those designs at 7-nm node. Simulation results are normalized to nominal V_{DD} power consumption for conventional D-FF at the 7-nm node. Comparing performance, the GG-FF costs about 30% more power and 30% more area compared to conventional D-FF when operating at nominal V_{DD} at the 7-nm node.

3. EXPERIMENTAL DETAILS

Test chips were fabricated in 16-nm and 7-nm bulk FinFET technologies at a commercial foundry. Shift registers with different FF designs were implemented in Circuit for Radiation Effects Self-Test (CREST) configuration [26]. The test structure consists of 24K stages for D-FF and 16K stages for GG-FF for the 7-nm test chip and 8K stages for D-FF and GG-FF for the 16-nm test chip. Support circuits (such as clock generation, error detection, error counting, etc.) were also designed on-chip. The overall design approach for both the test ICs is shown in Fig. 3.1. All sub-circuits other than shift registers were designed with Triple Modular Redundancy (TMR) to eliminate all errors from support circuits. The size of the test die was 2 mm × 2 mm for the 16-nm node and 2 mm × 1 mm for the 7-nm node.

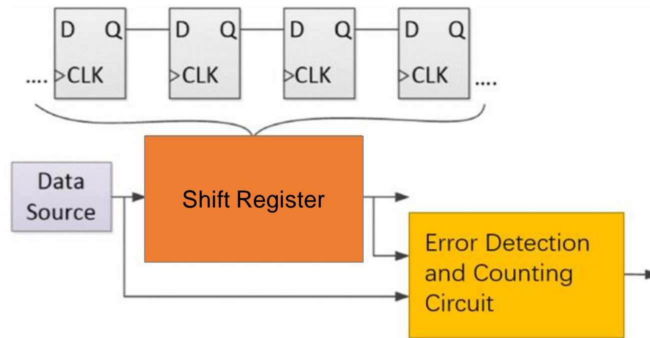


Figure 3.1: CREST block level design used for evaluating SEU response of FF cells [26].

Heavy-ion exposures were carried out at Lawrence Berkeley National Laboratory (LBNL) with 10 MeV/nucleon cocktail for the 16-nm designs and with 16 MeV/nucleon cocktail for the 7-nm designs. The range of particle LET values used for tests were from 1~25 MeV-cm^2/mg for the 7-nm node design and from 1~47 MeV-cm^2/mg for the 16-nm node design. All heavy-ion experiments were carried out at room temperature and in vacuum with normal incidence. The input signal of shift registers was set to logic zero. The supply voltage ranged from 450 mV~750 mV for the 7-nm node (for this technology, nominal V_{DD} is 750 mV) and 500 mV ~ 800 mV for the 16-nm node (for this technology, nominal V_{DD} is 800 mV). The operating frequencies of shift registers was varied from 2.5 MHz to 1.8 GHz for heavy-ion tests.

Alpha particle exposures were carried out at Vanderbilt University using a 1 cm × 1 cm size 10 μCi ^{241}Am foil button source with the energy of emitted alpha particles ~5.4 MeV (flux = 1000 particles/mm^2) in air. The size of the alpha source compared to die size ensures uniform alpha flux. At 5.4 MeV energy, assuming less than 1 mm of air and 20 μm of overlayers, the particle LET will be less than 1 MeV-cm^2/mg when it reaches active-Si area. Tests were performed for supply voltage values of 850 mV, 800 mV (nominal), 700 mV, 600 mV, and 550 mV for the 16-nm node designs, and at 750 mV (nominal), 650 mV, 550 mV, and 450 mV for the 7-nm node designs. All tests were carried out at room temperature.

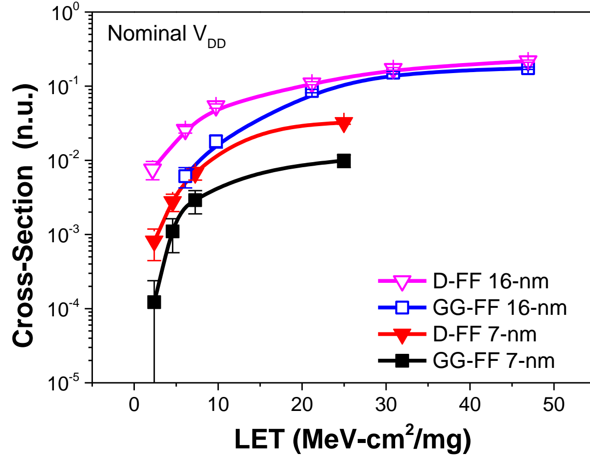
Fast neutron experiments were performed at the ChipIR facility at the Rutherford Appleton Laboratory (RAL) in Didcot, UK. ChipIR provides a spectrum that is very similar to atmospheric spectrum for neutron energies between 10 and 750 MeV. Tests were performed for supply voltage values of 750 mV and 550 mV for the 7-nm node designs. All tests were carried out at room temperature.

4. Experimental and Simulation Results

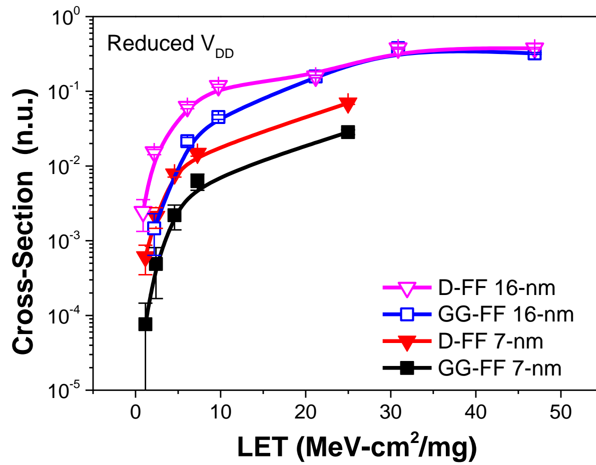
4.1. Heavy-Ion Experimental Results

Fig. 4.1 shows the heavy-ion result for conventional D-FF and GG-FF as a function of particle LET for two different supply voltage values. Results show that for the 16-nm node, at nominal V_{DD}, GG-FF shows about ~3× SER improvement compared to conventional D-FF design for low-LET particles as well as comparable SER performance for high-LET particles. Similar trend is observed for the 16-nm node designs at reduced V_{DD} values, as shown in Fig. 4.1(b). For the 7-nm node, at nominal V_{DD}, the GG-FF shows about ~3× SER improvement compared to conventional D-FF design for particle LET values of 1~25 MeV-cm^2/mg. At reduced V_{DD} values, the measured improvement ratio in SER is also ~3× for the 7-nm node. For high-LET particles at the 16-nm node, GG-FF and D-FF show similar SE cross-section. But the 7-nm node designs show consistently better SE performance for GG-FF over D-FF. The main reason behind this difference is the percentage of short SET pulses at these nodes.

The GG-FF eliminates all SET pulses that are shorter than the delay of the delay circuit (in this case, the delay circuit was two minimum-size inverters). For low-LET ions, the number of short SET pulse will be high for FinFET nodes. As a result,



(a)



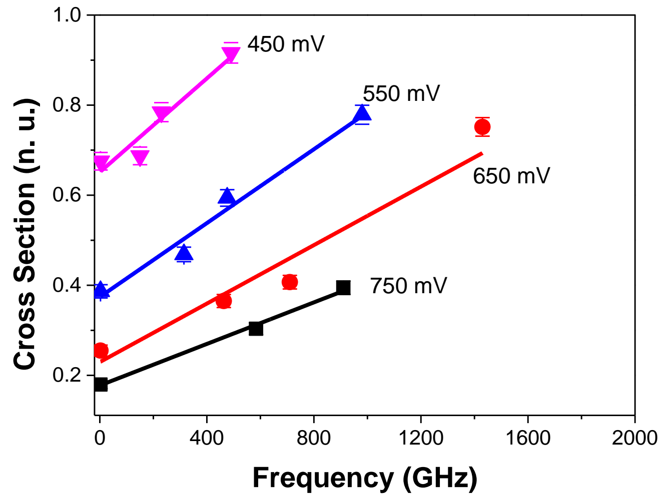
(b)

Figure 4.1: Heavy-ion test result for GG-FF and conventional D-FF in 7-nm and 16-nm technology nodes for different particle LET values at (a) nominal supply voltage and (b) reduced supply voltage.

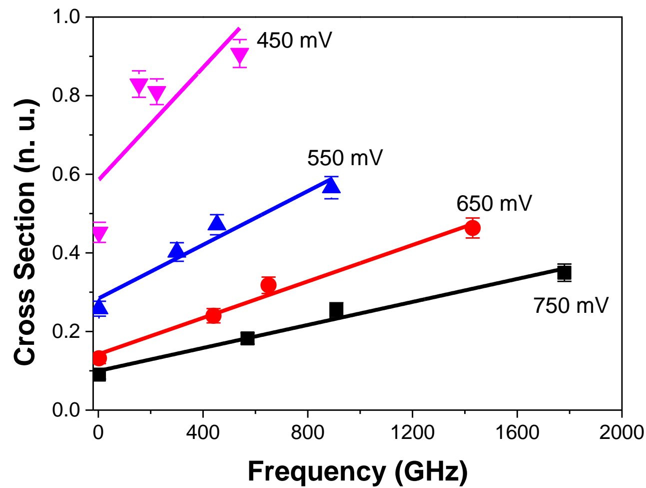
the difference between D-FF and GG-FF SE cross-sections will be significant, as seen in Fig. 4.1. For High-LET particles, direct hits on drain regions will generate

long SET pulses. Ion hits nearby a drain region will deposit charges in the substrate region which will be collected through diffusion process, yielding shorter SET pulses. For the 16-nm node, the percentage of short SET pulses for high-LET particles is small, resulting in very small differences between D-FF and GG-FF SE cross-sections. However, for the 7-nm node, the percentage of short SET pulses does not drop off as dramatically, resulting in significant differences in SE cross-section between D-FF and GG-FF. Percentage of short SET pulses for both of these technologies and reasons for the differences are explained in the Short SET Pulses section below.

Most ICs fabricated at these technology nodes will operate in GHz range of frequencies. At these frequencies, contribution of the logic SE cross-section is comparable to latch SE cross-section. As a result, it is important to include such frequency dependence in SE performance evaluations. For a shift register, the transparent stage of the FF will act like a logic circuit [27]. Fig. 4.2 shows the heavy-ion test result for conventional D-FF and GG-FF as a function of operating frequency. Results show that for the 7-nm node, at nominal V_{DD}, the GG-FF shows about ~2.5× SER improvement compared to conventional D-FF design over a wide range of operating frequencies. At reduced V_{DD}, the GG-FF shows about ~1.5× SER



(a)



(b)

Figure 4.2: Heavy-ion test result for (a) conventional D-FF and (b) GG-FF in 7-nm technology nodes for different operating frequencies. The ion we used for this test is Kr (25 MeV-cm^2/mg).

improvement compared to conventional D-FF. The slopes of these curves also show that the rate of increase in SE cross-section with frequency is smaller for the GG-FF

compared to that for the D-FF. As the overall sensitive area for both the FF designs is similar (as shown in Fig. 2.2 and Fig. 2.3), the consistently better performance of GG-FF over D-FF is solely due to the elimination of short SET pulses in GG-FF design. Reducing V_{DD} has been an effective way to reduce the power consumption of the IC. However, as shown in Fig. 4.2, the slope of SE cross-section vs. frequency curve increases when V_{DD} is reduced for both conventional D-FF and GG-FF. These test results indicate that at the 7-nm node, the GG-FF has better SER performance compared to D-FF over a wide range of particle LET values and operating frequencies at both nominal and reduced V_{DD}.

From a design perspective, operating frequency for GG-FF will be lower compared to D-FF due to the increased setup-&-hold time requirement. Increasing V_{DD} will increase power consumption and lower FF SER. Increasing frequency will increase logic SER. Logic SER and latch SER are comparable at GHz range of frequencies. For a designer to meet power and SE specifications, compromises must be made between V_{DD}, frequency, and SER. For such an optimization, SE cross-section as a function of power consumption per clock cycle may be a good metric for a fair comparison across frequency and V_{DD} values. Such a metric can be used to optimize SE cross-section as a function of frequency and V_{DD}. Power consumption per clock cycle is super-linearly related to V_{DD} and linearly related to frequency. Fig. 4.3 provides the same data set as that in Fig. 4.2 with three

dimensions (SER, frequency and power consumption) for conventional D-FF and GG-FF at the 7-nm node. Results shown in Fig. 4.3 were

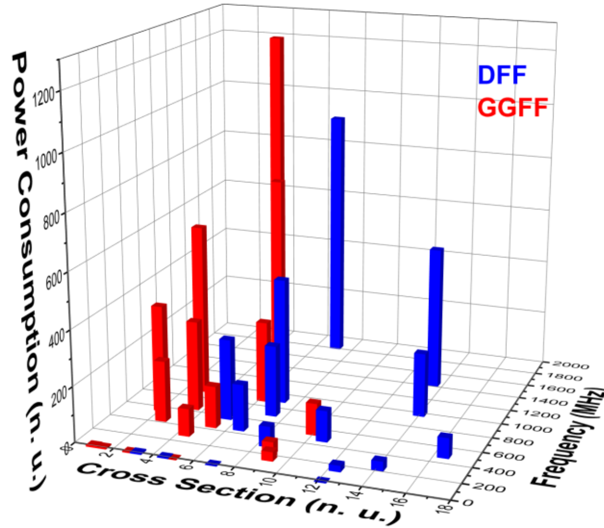


Figure 4.3: Data set with three dimensions (SER, frequency and power consumption) for conventional D-FF and GG-FF at 7-nm node. Test data were collected from heavy-ion test with Kr.

collected from heavy-ion test with Kr (LET = 25 MeV-cm^2/mg). For a given power budget, designers can either increase V_{DD} and operate at a lower frequency to meet SER specifications or reduce V_{DD} and increase frequency. Increasing V_{DD} will reduce latch SER and increasing frequency will increase logic SER. Such options allow designers to optimize the operating conditions for a circuit. For example, for operation at 400 MHz with SE cross-section lower than 12 (arbitrary units used in Fig. 4.3), conventional D-FF with V_{DD} equals to 550 mV will give the lowest power consumption among all the selections while meeting the other two criteria

(frequency and SE cross-section). Such figures for multiple FF designs at a given technology node will allow designers to optimize overall circuit performance.

It is important to evaluate the effect of changing power budget on SE cross-section. Rate of increase in SE cross-section as a function of power consumption per clock cycle is shown in Fig. 4.4. For this Figure, the X-axis was normalized to GG-FF's power consumption per cycle at nominal V_{DD}. The slope of GG-FF's SE cross-section shows a super-linear trend when V_{DD} is reduced, compared to a linear trend for conventional D-FF. Designer must take all such results into consideration before selecting the optimum operating conditions for a given SE specifications.

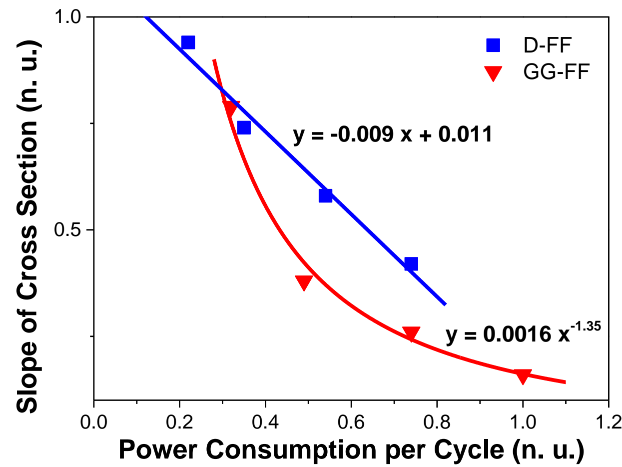


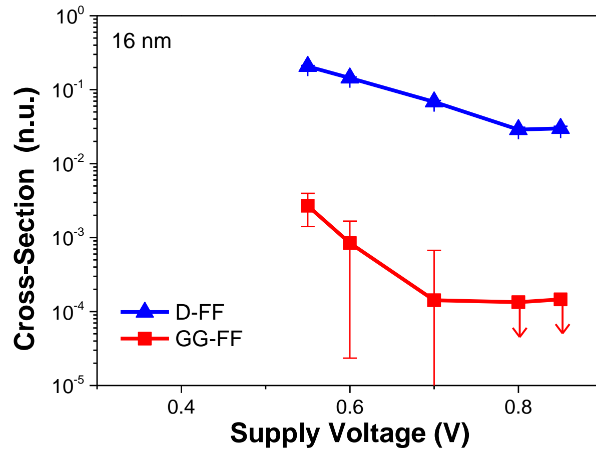
Figure 4.4: The slope of SE cross-section calculated based on Kr heavy-ion frequency test for conventional D-FF and GG-FF. X-axis was unified to GG-FF's power consumption per cycle at nominal V_{DD}.

4.2. Alpha Particles Experimental Results

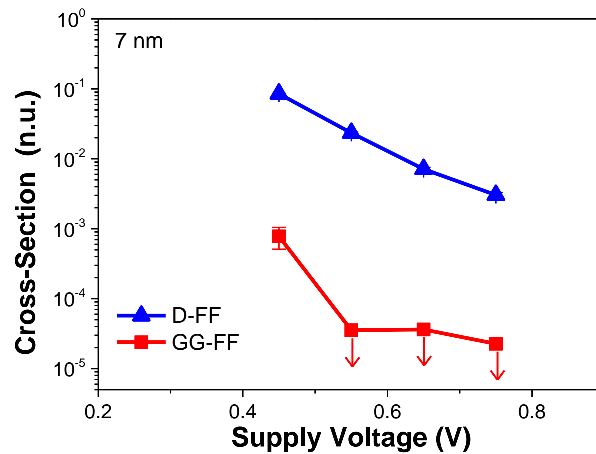
The alpha particles test results are shown in Fig. 4.5. The SE performance of GG-FF and conventional D-FF at different supply voltages were evaluated for both 16-nm and 7-nm technology nodes. The GG-FF did not upset to the tested fluence of alpha particles in both 16-nm and 7-nm designs at nominal supply voltages. For the 7-nm node, GG-FF design showed upset only when supply voltage was reduced to 450 mV. At both technology nodes, GG-FF shows at least 100× SER improvement compared to conventional D-FF design over a wild range of supply voltages.

4.3. Fast Neutron Experimental Results

The fast neutron test results for conventional D-FF and GG-FF at 7-nm node are shown in Table II, the SE performance of GG-FF show improved performance compared to D-FF at both 550 mV and 750 mV. The improvement is not as much as that for heavy-ions and alpha particles. One of the reasons for this discrepancy in improvement may be due to the very few upsets observed in all neutron tests.



(a)



(b)

Figure 4.5: Alpha particles test result for GG-FF and conventional D-FF in (a) 16-nm and (b) 7-nm technology nodes at different supply voltages.

Table II: Fast neutron test results for conventional D-FF and GG-FF for V_{DD} of 750 mV and 550 mV at 7-nm node. (Data normalized to the D-FF at V_{DD} = 750 mV).

FIT (n. u.)	**D-FF**	**GG-FF**
750 mV	1 ± 0.35	0.56 ± 0.32
550 mV	1.92 ± 0.61	0

5. SHORT SET PULSES

SET pulse width and feedback-loop delay of a latch are two factors that determine the overall SER of FF designs [24, 25]. To a first degree, an SEU will occur only if the SET pulse width is longer than the feedback-loop delay of the latch. SET pulse width is strongly related to the transistor current, which varies with technology and supply voltage [24]. The presence of the delay cell in the GG-FF essentially increases the feedback-loop delay, thereby rep0utechnologies scale, the effectiveness of GG-FF is not seen to diminish. GG-FF is as effective at the 16-nm node as it is at the 7-nm node. This improvement is retained even when supply voltage is reduced.

For a D-latch, the feedback-loop delay can be approximated as equal to 2-inverter delay. For GG-latch, the feedback-loop delay can be estimated as 4-inverter delay (delay of the delay-cell + 2-inverter delay). D-latch will eliminate all SET pulses shorter than 2-inverter delay (or will have no upset if the SET pulse is shorter than ~2-inverter delay). Similarly, GG-latch eliminates all SET pulses shorter than ~4-inverter delay for the design shown in Fig. 2.1.

The difference in measured SE upset cross-section for these two designs can be used to estimate the number of SET pulses that are between 2-inverter delay and 4-inverter delay. Comparing these SE upset cross-sections as a function of supply voltage will provide an insight into how the SET pulse width distribution changes

(it must be kept in mind that feedback-loop delay of D-latch and GG-latch will also change).

Table III shows the percent of total SE transient that are between 2-inverter delay and 4-inverter delay for a range of supply voltages for the 16-nm node. Similarly, Table IV shows same results for the 7-nm node. These results show that for the 16-nm node, at nominal supply voltage, the percentage of short transients (shorter than 4-inverter delay) ranges from 100% to 11% when particle LET varies between 1-47 MeV-cm^2/mg. For the 7-nm node, however, the percentages vary between 85% to 57% when particle LET value varies between 1-25 MeV-cm^2/mg for nominal supply voltage.

At some particle LET value, both of these nodes show a reversing trend in this percentage value (for the 16-nm node, this percentage value is smallest at 31 MeV-cm^2/mg and for the 7-nm node, it is smallest at 7 MeV-cm^2/mg from the list of tested LET values. This implies that beyond a threshold value, the percentage of SET pulses shorter than (for example) 4-inverter delay increases with increasing particle LET values. For particles with low-LET values, the charge deposited and collected will be small resulting in short SET pulse widths for most ion hits – yielding higher percentages as shown in Table III and IV. As the particle LET increases, the SET pulse width will increase due to higher deposited/collected charge for ion hits on the drain region. Any ion hits away from the drain region will collect less charge (compared to ion hits within the drain region), resulting in shorter SET pulses [28].

Table III: Percentage of Short Transients for Different Particle LET and V_{DD} at 16-nm Node

		V_{DD} (mV)			
		800	**700**	**600**	**550**
Particle LET (MeV-cm²/mg)	**0.89**	100	100	100	100
	2.19	100	100	97.8	90.5
	6.09	76.4	68.5	56.7	65.5
	9.74	66.2	52.0	38.0	61.9
	21.17	21.6	4.1	0	7.7
	30.86	11.4	0	0	0
	46.92	19.8	0	0	14.9

Table IV: Percentage of Short Transients for Different Particle LET and V_{DD} at 7-nm Node

		V_{DD} (mV)			
		750	**650**	**550**	**450**
Particle LET (MeV-cm²/mg)	**1.16**	100	100	87.5	100
	2.39	85.0	94.4	76.9	63.8
	4.58	60.3	53.2	71.9	57.8
	7.27	56.8	41.0	57.6	62.8
	24.98	69.3	68.4	59.2	59.1

For a FinFET node, however, charge collection for ion hits outside drain region is different than that for a planar node. For a FinFET drain region, an ion hit away from the drain region will deposit charge in the substrate region below the isolation oxide. This substrate region is connected to the drain region through a narrow neck region that restricts charge transport, resulting in a decrease in charge collection from the substrate region (FinFET nodes have been shown to experience diminished charge-sharing effects compared to that for planar nodes [16, 17]). As a result, SET pulses will either be long SET pulses due to direct ion hits on the drain region, or

short SET pulses for ion hits away from the drain regions. Depending on the particle LET value, the amount of charge collected for ion hits away from the drain region may not be enough to cause an upset. Under such conditions, increasing particle LET value will yield lower percentages of short SET pulses initially (higher LET value will yield longer SET pulses for direct ion hits). Ion hits away from the drain will result in short SET pulses. With the overall percentage of short SET pulses declining with increasing particle LET value. Beyond a threshold value of particle LET value, enough charge will be deposited in the substrate such that SET pulse widths again start to increase for ion hits outside the drain region. This will increase the percentage of short SET pulses – similar to what is shown in Table III and IV.

6. CONCLUSIONS

In this work, SE performance of GG-based FF designs at 16-nm and 7-nm FinFET technology nodes is compared to that for D-FF for heavy-ions, fast neutron and alpha particles. Results clearly show the applicability of such a design for applications that require lower SER at a slightly higher performance penalty. Frequency test result show that GG-FF's SE cross-section shows a super linear increasing trend with reducing power consumption, and such slope would result in higher SER for GG-FF than that of conventional D-FF if they both are operating at a low power consumption level. Heavy-ion results are also used to calculate the percentage of short SET pulses that cause an upset in D-latch but not in GG-latch for a range of supply voltages and particle LET values. The percentage of short transients decreases with increasing particle LET values. However, this trend reverses at high particle LET values. Characterization of GG-FF and SET pulse widths as a function of supply voltage presented in this paper will allow designers to develop solutions to meet SE specifications with acceptable performance penalty.

References

[1] Moore, G. E. (1965). Cramming more components onto integrated circuits.

[2] R. C. Baumann, “Single event effects in advanced CMOS Technology,” in *Proc. IEEE NSREC Short Course Text*, 2005.

[3] P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 583–602, Jun. 2003.

[4] T. Heijmen, B. Kruseman, R. van Veen and M. Meijer, “Technology scaling of critical charges in storage circuits based on crosscoupled inverter-pairs,” in *Proc. IEEE Int. Rel. Phys. Symp*., pp. 675–676, Jul. 2004

[5] T. Calin, M. Nicolaidis and R. Velazco, “Upset Hardened Memory Design for Submicron CMOS Technology,” *IEEE Trans. Nucl. Sci*., vol. 43, pp. 2874-2878, Dec. 1996.

[6] P. Hazucha et al., “Measurements and analysis of SER tolerant latch in a 90 nm dual-Vt CMOS process”, Proceedings of *IEEE Custom Integrated Circuits Conference*, pp. 617-620, 2003.

[7] D. G. Mavis and P. H. Eaton, “SEU and SET Modeling and Mitigation in Deep Submicron Technologies”, proceedings of the *IEEE International Reliability Physics Symposium*, pp. 293-305, 2007.

[8] N. Seifert et al., “On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies,” *IEEE Intl. Rel. Phy. Symp. Proc*., pp. 188-197, 2010.

[9] H. H. K. Lee, K. Lilja, M. Bounasser, I. Linscott and U. Inan, “Design Framework for Soft-Error-Resilient Sequential Cells,” *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 3026-3032, Dec 2011.

[10] B. Narasimham, K. Chandrasekharan, Z. Liu, J. K. Wang, G. Djaja, N. J. Gaspard, J. S. Kauppila, B. L. Bhuva, “A Hysteresis-Based D-FlipFlop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead,” *IEEE Trans. Nucl. Sci.*, pp. 2847 – 2851, 2012.

[11] B. Narasimham, K. Chandrasekharan, J. K. Wang, K. Ni, B. L. Bhuva, R. D. Schrimpf, “Charge-Steering Latch Design in 16 nm FinFET Technology for Improved Soft Error Hardness,” *IEEE Trans. Nucl. Sci.*, vol. 64, pp. 353-358, 2017.

[12] J. P. Kulkarni, K. Kim, and K. Roy, “A 160 mV robust Schmitt Trigger based subthreshold SRAM,” *IEEE J. Solid-State Circuits,* vol. 42, no. 10, pp. 2303–2313, Oct. 20

[13] Y. Li, H. Wang, S. Yao, Z. Gao, and J. Xu, “Double node upsets hardened latch circuits,” *J. Elect. Testing*, vol. 31, nos. 5–6, pp. 537–548, 2015.

[14] A. Balasubramanian, B. L. Bhuva, J. D. Black, and L. W. Massengill, “RHBD techniques for mitigating effects of single-event hits using guard-gates,” *IEEE Trans. Nucl. Sci*, vol. 53, no. 6, pp. 2531–2535, Dec. 2005.

[15] Baumann, R. (2005). Soft errors in advanced computer systems. *IEEE Design & Test of Computers*, 22(3), 258-266.

[16] H. Zhang et al., "Angular effects of heavy-ion strikes on single-event upset response of flip-flop designs in 16-nm bulk FinFET technology." *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 491-496, 2017.

[17] B. L. Bhuva, N. Tam, L. W. Massengill, D. Ball, I. Chatterjee, M. McCurdy, and M. L. Alles, “Multi-cell soft errors at advanced technology nodes,” *IEEE Trans. Nucl. Sci.,* vol. 62, no. 6, pp. 2585–2591, Dec. 2015.

[18] R. L. Shuler, A. Balasubramanian, B. Narasimham, B. L. Bhuva, P. M. O’Neill, and C. Kouba, “The effectiveness of TAG or guard-gates in SET suppression using delay and dual-rail configurations at 0.35 μm,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3428–3431, Dec. 2006.

[19] Shuler R. L., C. Kouba, and P.M. O’Neill, “SEU Performance of TAG Based Flip-Flops,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, Dec. 2005.

[20] S. Mitra, M. Zhang, S. Waqas, N. Seifert, B. Gill, and K. S. Kim, “Combinational logic soft error correction,” in *Proc. IEEE Int. Test Conf.*, 2006, Paper No. 29.2.

[21] S. Mitra, N. Seifert, M. Zhang, Q. Shi, and K. S. Kim, “Robust system design with built-in soft-error resilience,” *Computer*, vol. 38, no. 2, pp. 43–52, Feb. 2005.

[22] J. Furuta et al., "A 65 nm bistable cross-coupled dual modular redundancy flip-flop capable of protecting soft errors on the c-element", *Proc. VLSI Circuits Symp*., pp. 123-124, 2010-Jun.

[23] M. Zhang et al., "Sequential element design with built-in soft error resilience", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*., vol. 14, no. 12, pp. 1368-1378, Dec. 2006.

[24] H. Zhang et al., "Temperature dependence of soft-error rates for FF designs in 20-nm bulk planar and 16-nm bulk FinFET technologies." *2016 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2016.

[25] H. Zhang, H. Jiang, B. L. Bhuva, J. S. Kauppila, W. T. Holman, and L. W. Massengill., "Frequency dependence of heavy-ion-induced single-event responses of flip-flops in a 16-nm bulk FinFET technology." *IEEE Trans. Nucl. Sci*., vol. 65, no. 1, pp. 413-417, Dec. 2018.

[26] P. Marshall, M. Carts, S. Currie, R. Reed, B. Randall, K. Fritz, K. Kennedy, M. Berg, R. Krithivasan, C. Siedleck, R. Ladbury, C. Marshall, J. Cressler, G. Niu, K. LaBel, and B. Gilbert, “Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5 AM SiGe circuit for radiation effects self test (CREST),” *IEEE Trans. Nucl. Sci*., vol. 52, no. 6, pp. 2446–2454, Dec. 2005.

[27] S. Jagannathan, T. D. Loveless, B. L. Bhuva, N. J. Gaspard, N. Mahatme, T. Assis, S. J. Wen, R. Wong, and L. W. Massengill, “Frequency dependence of alpha-particle induced soft error rates of flipflops in 40-nm CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 2796–2802, Dec. 2012.

[28] K. M. Warren, R. A. Weller, B. D. Sierawski, R. A. Reed, M. H. Mendenhall, R. D. Schrimpf, L. W. Massengill, M. E. Porter, J. D. Wilkinson, K. A. LaBel, and J. H. Adams. "Application of RADSAFE to Model the Single Event Upset Response of a 0.25 μm CMOS SRAM." *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 898-903, 2007.