EFFECTS OF MOISTURE EXPOSURE AND TOTAL DOSE IRRADIATION ON MOS LOW FREQUENCY NOISE

By

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CHAPTER I

INTRODUCTION

The low frequency ($1/f$) noise of semiconductor devices has been a source of interest for decades. Extensive theoretical and experimental research has been performed in order to better understand the physical properties responsible for the noise, and to develop useful models to describe them. In recent years, $1/f$ noise has been used as a tool to characterize changes in MOS behavior and reliability due the effects of ionizing radiation and aging [1]-[5].

Radiation effects in microelectronics has become a highly active field of research today, especially in the space and nuclear weapons industries, as technologies are continually becoming more and more advanced. Consequently, hardness assurance and reliability testing have become central and critical issues for electronics operating in radiation-harsh environments, and, as a result, a vast amount of resources has been invested in testing and qualifying parts for these environments. The most effective way to test these parts for hardness and reliability is to subject them to the conditions they would encounter during their deployment, namely, by exposing them to ionizing radiation. While significant insight can be gained about device performance, these tests are typically destructive, and therefore the devices cannot be used afterwards. Furthermore, devices that are tested form a limited sample (and consequently a limited representation) of a specific lot, which introduces a degree of uncertainty, since device responses from these tests may or may not differ from responses of the actual fielded devices. As a result,

much effort has been exerted in finding nondestructive, reliable tests for radiation hardness in microelectronics.

Over the last 20 years, 1/*f* noise measurements have emerged as an insightful and potentially nondestructive test for radiation hardness in MOS devices [1]-[4]. Work has been done that links characteristics of MOS 1/*f* noise with characteristics of the device radiation response. Scofield and Fleetwood have found that the pre-irradiation low frequency noise of MOS transistors correlates strongly with the post-irradiation threshold voltage shifts due to oxide-trap charge [1]. Further studies have shown the significance of bias and temperature conditions during irradiation and annealing on MOS 1/*f* noise and radiation response [2], [3], particularly the differences observed between n-channel and p-channel devices.

Recent work has shown that MOS radiation response can degrade with aging, and strongly suggests that moisture is a primary agent in the aging process [6], [7]. This can have a significant impact on the reliability and radiation hardness of devices employed for long periods of time or used after long-term storage in non-hermetic environments. In particular, in [6] it was shown that devices that had been stored for 17 years in room temperature conditions exhibited a much larger increase in threshold-voltage rebound during post-irradiation annealing than devices from the same wafer that were tested in the original study in 1988; in [7] it was shown that exposure to moisture at elevated temperatures could cause a significant increase in interface trap buildup during post-irradiation annealing. It has also been shown that the 1/*f* noise of MOS devices can change significantly with storage time [5]; however, moisture exposure appears to affect nMOS and pMOS noise differently.

These areas of study continue to evolve as more is understood about the relationship between low frequency noise and radiation response, and how aging affects both. While research continues to provide valuable insight into MOS low frequency noise, especially the differences between nMOS and pMOS devices, the microscopic origins of the 1/*f* noise are still not well understood, or at best, are still under debate. Two schools of thought have emerged to explain the origin of 1/*f* noise in MOS devices. One attributes the noise of nMOS and pMOS devices to two different mechanisms: a surface trapping mechanism for nMOS devices and a bulk mobility fluctuation mechanism for pMOS devices. The second school of thought attributes the noise of both nMOS and pMOS devices primarily to trapping. The observed differences in gate-voltage dependences of the 1/*f* noise for nMOS and pMOS devices have been a dividing line for these two cases, and extensive studies on nMOS and pMOS noise have been interpreted as weighing in favor of one theory or the other.

In this thesis, we explore the effects of moisture exposure at elevated temperature on MOS 1/*f* noise and radiation response, and report the different effects observed between n-channel and p-channel transistors. The gate-voltage dependence of the noise is studied in detail for both types of devices throughout the experiments. Results show that moisture exposure has a more significant impact on pMOS noise and radiation response than for nMOS devices; furthermore, gate-voltage noise measurements indicate that changes in the defect energy distributions are responsible for the observed gate-voltage dependence for our nMOS and pMOS devices, which supports the carrier-number fluctuation theory. Chapter II describes the models used to characterize 1/*f* noise in MOS devices, and gives an overview of the radiation and aging effects on MOS response and

reliability. Chapter III describes the devices used in this study, the experimental setup for measuring $1/f$ noise, the moisture exposure and irradiation experiments, and ensuing analyses. Chapter IV presents and discusses the results from these experiments, and Chapter V provides a summary and conclusion of this work.

CHAPTER II

BACKGROUND

This chapter contains background information about low frequency noise in MOS devices, radiation effects, and aging and reliability issues. 1/*f* noise in metals is discussed, because this provides useful background information on characterization of the temperature and energy dependence of the noise. In addition, we describe the two models most commonly used to describe 1/*f* noise in MOS devices, along with their relevance to this work. The effects of total dose radiation exposure on MOS devices are then recounted, followed by a discussion of aging effects and reliability.

Low Frequency Noise in MOS Devices

Many physical systems exhibit fluctuations with spectral densities that vary approximately as 1/*f* over a large range of frequencies. We are particularly interested in these 1/*f*-like fluctuations in metals and semi-conducting materials, due to the information they can reveal about the physical structures of these systems and the physical processes involved in the 1/*f* noise that is characteristic of each system. Dutta and Horn developed a model that describes the 1/*f* noise in metals, by investigating the fluctuations in the voltage drop across a sample resistance through which current is flowing [8]. The instantaneous voltage drop across the resistance, $V(t)$, fluctuates about it its average value $\langle V \rangle \equiv V_{DC}$ when in steady state, or when the current I_{DC} is constant. When $I_{DC} = 0$, $V_{DC} = 0$ and the fluctuations in the voltage drop $S_V(f)$ are known as Johnson or Nyquist noise.

Over a limited frequency range, Johnson noise can be defined as

$$S_V(f) = 4k_B TR(f), \tag{2.1}$$

where k_B is the Boltzmann constant, T is the temperature, and R is the sample resistance. In the steady-state condition, when I_{DC} is non-zero, $S_V(f)$ is observed to increase over the equilibrium value given by Eq. (2.1), and at sufficiently low frequencies exhibits 1/*f*-like noise behavior.

In most cases, the observed noise spectra are not exactly proportional to 1/*f*, but have a frequency dependence of the form f^{α}, where $0.8 \leq \alpha \leq 1.4$. Dutta and Horn showed that 1/*f* noise can be obtained from a distribution of activation energies $D(E)$ that are not constant, but vary slowly compared to $k_B T$. When $D(E)$ varies slowly over any range $\Delta E \sim k_B T$, the energy distribution of defects causing the noise can be related to the noise spectral density through

$$D(E_0) \propto \frac{\omega}{k_B T} S(\omega, T), \tag{2.2}$$

where $\omega = 2\pi f$. The defect energy E_0 is related to the temperature and frequency by

$$E_0 \approx k_B T \ln(\omega, \tau_0), \tag{2.3}$$

where τ_0 is the characteristic time for the defect. Dutta and Horn also derived an expression for the frequency and temperature dependence of the noise, given by

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\delta \ln S(\omega, T)}{\delta \ln T} - 1\right), \tag{2.4}$$

where the frequency exponent α is defined as

$$\alpha = \frac{\delta \ln S}{\delta \ln f}. \tag{2.5}$$

The equations defined above are valid for the following conditions:

1. The noise is due to random processes with thermally activated characteristic times.
2. The distribution of activation energies $D(E_0)$ varies slowly over any interval, $\Delta E \cong kT$.
3. The attempt-to-escape frequency for the defect, $f_0 = 1/\tau_0$, is much larger than the frequency at which the noise is measured.
4. The total noise magnitude is independent of temperature.

A variety of models have been used to explain the 1/*f* noise in MOSFET devices [9]-[18]. It has been generally accepted that the 1/*f* noise in the conduction channel of the device is primarily associated with the capture and emission of charge carriers from trap sites in the oxide, at or near the Si/SiO_2 interface. Fluctuations in the oxide-trap charge couple to the channel, both directly through fluctuations in the inversion layer charge density, and indirectly through fluctuations in scattering associated with fluctuations in trap occupancy. These fluctuations in inversion charge are referred to as carrier-number fluctuations. At variance with this mechanism, carrier-mobility fluctuations are described as fluctuations in carrier mobility due to phonon scattering. In general, studies tend to show that n-channel MOSFET noise is primarily dominated by number fluctuations, while p-channel noise is frequently interpreted to be due both to number and mobility fluctuations. The most widely accepted models for describing the two different mechanisms attributed to MOS 1/*f* noise are based on models originally proposed by McWhorter [19], and Hooge [20], [21].

Arguments in favor of number fluctuations often use experimental data showing an increase in 1/*f* noise through degradation (by hot carriers or irradiation) as evidence of

the theory; however, the majority of the results obtained on homogenous p-channel devices is consistent with Hooge's relationship. Hooge contended that 1/*f* noise was a bulk effect, rather than a surface effect, and that the fluctuating drain current arose from fluctuations in the mobility of the channel carriers as they collided with the crystal lattice, resulting in noise that was inversely proportional to the total number of carriers in the system. Hooge developed an empirical relation to describe the spectral density of the 1/*f* noise in the conductance *G* of a homogenous sample, given by

$$\frac{S_G}{G^2} = \frac{S_I}{I^2} = \frac{\alpha_H}{Nf}, \tag{2.6}$$

where S_I is the current noise in the sample, I is the current flowing through it, α_H is the Hooge parameter, and N is the total number of charge carriers. When lattice scattering prevails, $\alpha_H \approx 2 \times 10^{-3}$. If impurity scattering is present also, then α_H becomes

$$\alpha_H = \left(\mu / \mu_{latt}\right)^2 (2 \times 10^{-3}), \tag{2.7}$$

where μ is the observed mobility, and μ_{latt} is the value the that the mobility would have had if only lattice scattering had been present [21], [22].

In order to compare experimental results of MOS transistors with the empirical relation given by equation (2.6), the following form is derived (for devices operated in the linear region) by using $N = C_{ox}(V_g - V_t)WL/q$, and rearranging terms to obtain

$$S_{I_d} = \frac{q\alpha_H}{C_{ox}WL} \frac{I_d^2}{(V_g - V_t)f}, \tag{2.8}$$

where S_{I_d} is the MOS drain current noise, I_d is the drain current, q is the electron charge, C_{ox} is the gate oxide capacitance, and L and W are the length and width of the device

channel, respectively [23]. For a constant drain voltage, fluctuations in the channel current vary inversely with $(V_g - V_t)$, or $S_{I_d} \propto (V_g - V_t)^{-1}$.

McWhorter developed a simple model that attributes the noise to charge trapping at trap sites located at a distance from the oxide-semiconductor interface, facilitated by a tunneling mechanism in the surface oxide of the material. To obtain a $1/f$ noise spectrum, a wide distribution in the capture time, or time constant, τ of these traps must be present, with a distribution proportional to $1/\tau$. The time constants in the tunneling process are given by

$$\tau = \tau_0 \exp(\alpha x), \tag{2.9}$$

where x is the distance between the trap and the oxide-semiconductor interface, α is a tunneling parameter, and τ_0 is the time constant for a trap at the surface [24]. If x varies between 0 and 40 Å, τ will vary over many orders of magnitude, from very small to very large time constants. The traps that are most effective in the process are those with energies near the Fermi level of the oxide, since those energies more than a few kT above the Fermi level are empty and those more than a few kT below it are filled. The filling and emptying of these traps alter the conductivity of the device channel, thus leading to changes in the majority carrier concentration. As a result, the noise predicted by this model should be proportional to the density of traps near the Fermi level.

Following McWhorter's proposal, others have developed models to account for the tunneling mechanism and charge trapping responsible for $1/f$ noise in MOS devices [4], [10], including carrier-number fluctuation models that account for mobility fluctuations caused by carrier trapping [25], [26]. However, in this discussion, we will use a model that describes MOS $1/f$ noise primarily due to number fluctuations, assuming

that any scattering due to trapped carriers produces a less significant fluctuation in mobility.

In this model, the oxide traps that exchange charge with the device channel are assumed to exist uniformly in space (throughout the oxide) and in energy (in the silicon band gap). Charge carriers tunnel directly into and out of these traps, with a mean trapping time governed by Eq. (2.9). The power spectral density of fluctuations in the total number of trapped charges N_t is given by

$$S_{N_t}(f,T) = \frac{k_B T D_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f}, \tag{2.10}$$

where $D_t(E_f)$ is the oxide trap density at the Fermi level E_f, L and W are the device channel length and width, respectively, and τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [4]. Thus, the level of the noise spectrum is determined by the density of traps near the Fermi level, which depends on T, at a distance from the interface that depends on f. For a MOS transistor operated in strong inversion, the fluctuations in trapped charge result in a fluctuation in the effective gate voltage, and under constant drain current conditions, causes a fluctuation in the drain voltage, given by

$$S_{V_d}(f,T,V_d,V_g) = \frac{q^2}{C_{ox}^2} \frac{V_d^2}{(V_g - V_t)^2} S_{N_t}(f,T)$$

$$= \frac{q^2}{C_{ox}^2} \frac{V_d^2}{(V_g - V_t)^2} \frac{k_B T D_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f}, \tag{2.11}$$

where C_{ox} is the gate oxide capacitance, V_d and V_g are the drain voltage and gate voltage, respectively, and V_t is the threshold voltage of the device [4]. For a fixed drain voltage, $S_{V_d} \propto (V_g - V_t)^{-2}$. Any non-uniformity in $D_t(E_f)$ would show up in the gate-voltage

dependence, temperature dependence, and/or frequency dependencies of the noise in Eq. (2.11). These dependencies frequently are coupled through mechanisms similar to those described in Eq. (2.4) above, in the discussion of the Dutta-Horn model. According to this model, given a significant deviation from a uniform distribution of traps in energy, the gate-voltage, temperature, and frequency dependencies must reflect this departure from uniformity. This will be discussed further in Chapter IV.

The observed correlation between oxide trap density and 1/*f* noise in MOS devices is often used as evidence for the number fluctuation model; however, as stated earlier, many argue against its acceptance as a general model for MOS 1/*f* noise due to its inconsistency in describing pMOS data. Likewise, arguments against the Hooge model have also been presented [27]. The differences between the observed gate-voltage dependence of the 1/*f* noise for n-channel and p-channel MOS devices have reinforced the two different schools of thinking [23], [28]-[31]. In particular, the noise S_{V_d} has been found to scale with $V_d^2/(V_g - V_t)^2$ for nMOS devices, which is considered strong evidence for the number fluctuation model; for pMOS devices, however, $S_{V_d} \propto V_d^2/(V_g - V_t)$, which is often interpreted as evidence that noise is dominated by mobility fluctuations.

Radiation Effects in MOS Devices

Ionizing radiation is known to cause damage in solid-state devices. Exposure to ionizing radiation can alter the physical microstructure of the device, temporarily or permanently, causing changes in device properties and operating characteristics. This is obviously a major concern for microelectronics operating in radiation environments, particularly for military and space applications. As such, much time and resources have

been devoted to understanding as much as possible about radiation effects in microelectronics, the short-term and long-term damage, time-dependent responses, and mitigation techniques. Sources of radiation in the space and weapons environment include x-rays, energetic electrons, protons, and heavy ionized particles, the effects of which can be observed and studied on the material level, device level, circuit level, and chip level, and can be separated into two different areas of study: total dose effects and single event effects. Total dose effects entail the damage and degradation accumulated over time from radiation exposure, while single event effects include device or circuit response to interaction with a single ionizing particle. For this study, we focus on total dose effects in MOS devices, which are described next in detail.

For MOS devices, the oxide is the most radiation-sensitive part. Figure 1 below shows a schematic energy band diagram of a MOS structure, and illustrates the four main physical processes responsible for the radiation response of the device [32]. A positive bias is applied to the gate electrode so that electrons flow toward the gate and holes move to the silicon substrate.

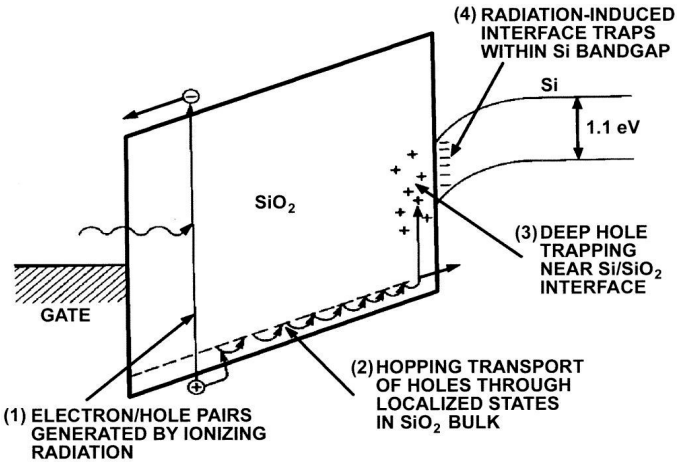

Figure 1: Band diagram of a MOS system with a positive gate bias. After [32].

When a MOS device is exposed to ionizing radiation, electron-hole pairs are created in the oxide (1). Because electrons have a much higher mobility than holes in SiO_2, the majority of the electrons are swept out of the oxide, under the influence of the gate bias. Some fraction of the electrons and holes will recombine after the initial exposure, the amount of which depends on the strength of the electric field in the oxide and the energy of the incident irradiation. The holes that escape recombination are relatively immobile and remain in the oxide as positive charge. The holes then transport through the oxide to the Si/SiO_2 interface (2), where some fall into deep trap states (3). The fourth major process in MOS radiation response is the buildup of interface traps at the Si/SiO_2 interface (4). As the holes transport through the oxide, they free hydrogen, in the form of protons, which then migrate to the interface to react with the Si-H bonds, creating interface traps [32]. The charge state of these traps depends on the gate bias.

Radiation-induced trapped charge and interface traps are a significant concern for MOS transistors, particularly because of their effects on device operating parameters. The positive oxide trapped charge generated by ionizing radiation causes a negative shift in the threshold voltage of MOS transistors. Interface trapped charge depends on the gate bias. For an nMOS transistor (gate biased positively), the interface trapped charge is negative, which causes a positive shift in threshold voltage; for a pMOS transistor (gate biased negatively), the interface trapped charge is positive, causing a negative shift in threshold voltage. The oxide charge buildup is greatest after initial irradiation, and anneals with time, while interface trap buildup typically continues to increase with time. This leads to a further reduction in the negative threshold voltage shift for pMOS devices, and can lead to a more positive threshold voltage shift, or threshold rebound, in nMOS

devices [33]. Depending on the radiation-tolerance of the oxide, radiation-induced damage can be quite severe for MOS transistors, even causing device failure.

In addition to an increase in charge density within the oxide and trap density at the oxide-silicon interface, radiation exposure increases the low frequency noise levels of MOS devices [1]-[3], [34]-[36]. The pre-irradiation 1/*f* noise of MOS devices has been found to correlate strongly with the post-irradiation threshold voltage shift due to oxide trapped charge. In particular, Scofield *et al.* showed a nearly linear relationship between the pre-irradiation normalized noise magnitudes of devices and ΔV_{ot}, with the noisiest devices exhibiting the largest ΔV_{ot} [1]; much less correlation was found to exist between the noise and threshold voltage shift due to interface traps, ΔV_{it}. Furthermore, in [3], the 1/*f* noise was observed to increase with increasing oxide trapped charge during irradiation for both nMOS and pMOS devices, but no significant correlation was found between the 1/*f* noise and ΔV_{it}. These studies led to the conclusion that oxide traps within a few nanometers of the Si/SiO_2 interface were responsible for the 1/*f* noise in MOS devices. These traps were termed 'border traps' [36].

Aging and Reliability

In addition to radiation exposure, harsh operating and storage conditions, as well as the normal aging process, all degrade device performance, with moisture absorption affecting these significantly. If water is introduced into devices during processing, water molecules can also diffuse into the gate oxides of MOS devices during long-term storage in non-hermetic environments.

Rodgers *et al.* showed that the irradiation and annealing responses of nMOS transistors could change significantly after 17 years of room-temperature storage [6]. These devices experienced a much larger increase in threshold-voltage rebound during post-irradiation annealing than devices from the same wafer that were tested in the original study in 1988. They attributed these shifts in threshold voltage to an increase in interface trap generation during irradiation and annealing, and found that baking these devices prior to irradiation reduced the shifts significantly. They concluded that the aging-related changes observed in these devices were likely due to water molecules absorbed during non-hermetic storage.

Work done by Batyrev *et al.* with devices from the same lot as in [6] showed that exposure to moisture at elevated temperatures significantly increased the interface trap buildup during post-irradiation annealing, as compared to devices that were not exposed to moisture, and devices that were baked prior to irradiation [7]. All devices in the study showed an increase in interface trap buildup compared to devices irradiated in the original study.

These studies demonstrate the importance of aging-related effects on MOS response. In particular, MOS response and reliability does not remain constant over time, but instead degrades, with the extent of degradation greatly influenced by the storage and operating conditions. Furthermore, these studies highlight the critical role water absorption plays in MOS radiation and aging response.

CHAPTER III

EXPERIMENTAL DETAILS AND MEASUREMENT TECHNIQUES

Devices

The nMOS and pMOS transistors used in this study were fabricated in 1984 at Sandia National Laboratories, and packaged in 1987. These transistors have poly-crystalline silicon gates and come from two different process lots, lot G1916A (wafer 10) and lot G1928A (wafers 16 and 28). Devices from wafer 10 have oxide thicknesses of 37 nm, and received a 30-minute, 1100 °C N_2 post-oxidation anneal. This type of processing is known to greatly increase the density of oxygen vacancies and vacancy complexes in SiO_2, making it a "radiation-soft" device [3]. Devices from wafer 16 have an oxide thickness of 25 nm, and devices from wafer 28 have an oxide thickness of 68 nm. Devices were passivated with p-glass, and experienced a full CMOS manufacturing flow. The nMOS transistors have a doping concentration of ~ 2.7×10^{15} cm^{-3} and the pMOS transistors have a doping concentration of ~ 4×10^{16} cm^{-3}. These parts were stored for 20 years before noise measurements.

The devices presented here were exposed to 85% relative humidity at 130 °C for one week at Sandia National Laboratories. Exposed parts were delidded during the one-week process, while the control parts remained hermetically sealed, or were not exposed at all.

Experimental Setup and Measurement Techniques

Noise measurements

Excess noise measurements were performed on n- and p-channel MOSFET transistors operating in strong inversion in their linear regimes using the apparatus shown in Figure 2. A constant voltage source V_A in series with a 20 kΩ resistor was connected to the MOSFET drain. A second, constant voltage source V_B was connected directly to the gate. Both the source and substrate were grounded. The constant voltage sources were supplied by a Hewlett Packard (HP) model 4140A constant voltage source/picoammeter. The drain voltage noise was amplified by a Stanford Research (SR) model 560 low-noise preamplifier. The preamplifier's low- and high-pass filters were set to pass frequencies between 0.3 Hz to 1 kHz, and the gain was set at 100. The output of the preamplifier was connected to the input of an SR760 FFT spectrum analyzer for calculating the power spectral density spectrum.

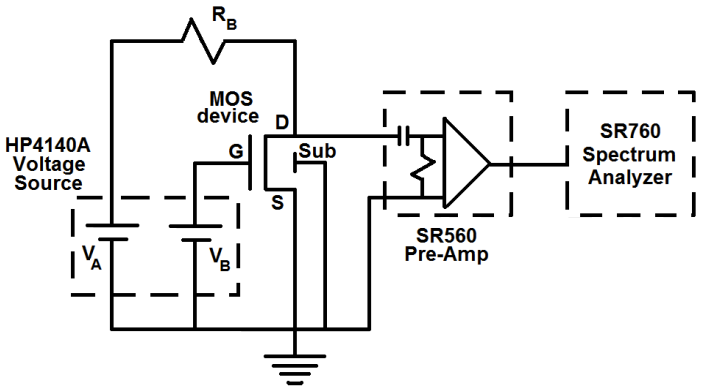

Figure 2: 1/f noise measuring circuit diagram.

Both the HP 4140A voltage source and the SR760 FFT spectrum analyzer were controlled with a personal computer using the IEEE-488 general purpose instrument bus

(GPIB). To reduce the interference of outside noise sources during the 1/*f* noise measurements, the device and circuit were enclosed in a shielded circuit box, and the preamplifier was operated in battery mode, to reduce the noise contribution from the 60 Hz pick-up in the power lines.

Figure 3 shows a log-log plot of typical measured drain voltage noise spectra S_{Vd} versus frequency for an nMOS transistor. The lower trace was measured with the drain biased at 0 V and represents the background noise for the system. The background noise is mainly due to three effects: the random thermal motion of the charge carriers in the channel, the noise of the preamplifier, and the pick-up from the 60 Hz power lines. The upper trace was measured with the drain biased at 100 mV. The 1/*f* noise spectrum of the device was determined by subtracting the background noise from the non-zero biased noise spectrum. The spikes in the noise spectrum due to the 60 Hz pick-up were ignored during the noise curve fitting and subsequent analysis.

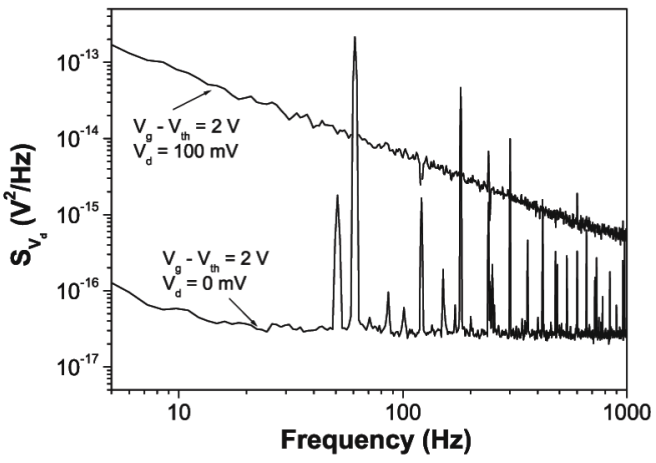

Figure 3: 1/f noise power spectral density for an unirradiated n-channel transistor. The lower trace represents the background noise.

All noise measurements in this work were performed while operating the devices in their linear regime in strong inversion. During the noise measurements, the drain voltage V_d was held at a constant ±100 mV ('+' for nMOS devices, '-' for pMOS devices). The gate-to-threshold voltage V_g-V_t was held at ±1 V during the measurements, unless specified otherwise.

Threshold voltage measurements

Threshold voltage measurements were carried out using HP 4156A and HP 4156B semiconductor parameter analyzers. A constant voltage of ±100 mV was applied to the drain of the device while the gate was swept from subthreshold to inversion. The threshold voltage was extracted from the linear plot of the measured drain current I_d versus gate voltage V_g in the linear region of operation, by determining the extrapolated x-axis intercept of the linear part of the curve (after subthreshold, when the device begins conducting).

Irradiation experiments

Irradiations were performed using an ARACOR Model 4100 10-keV X-ray irradiator. During all irradiations, the gate was biased at +6 V and all other leads were grounded. Devices were irradiated at a dose rate of 31.5 krad(SiO_2)/min.

CHAPTER IV

MOISTURE EXPOSURE AND RADIATION EFFECTS ON MOS LOW FREQUENCY NOISE

In this section, we present low frequency noise data on n-channel and p-channel devices from lot G1916A, wafer 10, and lot G1928A, wafers 16 and 28, before and after moisture exposure and irradiation, and describe the effects of moisture exposure on the total dose radiation response and the 1/*f* noise and MOS characteristics.

Low Frequency Noise and Moisture Exposure

Low frequency noise measurements were made on nMOS and pMOS transistors before and after the one-week exposure to humidity at 130 °C. Figure 4 shows the excess drain-voltage noise spectrum S_{Vd} versus frequency f for 3 μm x 16 μm (L x W) n-channel and p-channel devices from a wafer 10 part prior to irradiation, which was not exposed to moisture (control). The drain voltage V_d was held at a constant ± 100 mV and V_g-V_t was held at 1 V.

The dependence of the excess noise on frequency, drain voltage, and gate voltage can be approximated by the equation

$$S_{V_d}(f, V_d, V_g) = \frac{K}{f^{\alpha}} \frac{V_d^2}{(V_g - V_t)^2}, \tag{4.1}$$

where K is the normalized noise magnitude of the device and α represents the frequency dependence [1], [3].

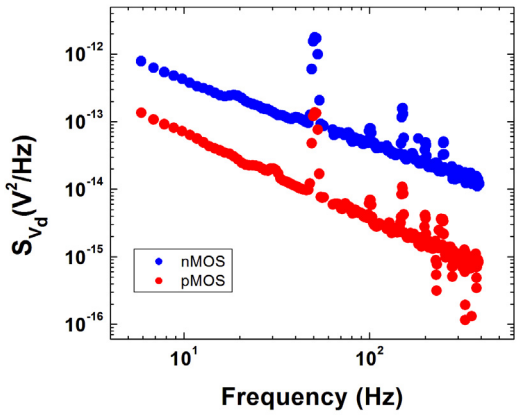

Figure 4: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm nMOS and pMOS transistors prior to radiation exposure.

For the nMOS device, α (determined by the best fit to S_{Vd} over the entire frequency span) was close to unity, indicating a relatively uniform border trap energy distribution [8], while for the pMOS device, α = 1.3. These frequency dependences are consistent with nMOS and pMOS devices from similar parts, and are typical of 1/*f* noise associated with defects (border traps) in the near-interfacial SiO_2 [1]-[4].

The 1/*f* noise magnitude is significantly larger in the nMOS device than it is in the pMOS device. Similar results were observed in other similarly processed devices, and are in agreement with previous studies done on these types of parts [2]. In general, for as-processed MOS devices, larger noise magnitudes are typically observed in n-channel transistors than in p-channel transistors, indicating a difference in which the majority carriers interact with the defects in the oxide for both types of devices. For electrons, the energy barrier into SiO_2 is 3.1 eV, and for holes it is 4.8 eV [37]. Therefore, it is more difficult for a p-channel device, where holes are the majority carrier, to exchange charge with the oxide, leading at least in part to the observed decrease in noise.

After the one-week exposure to moisture, low-frequency noise and threshold voltage measurements were made on the devices, and were compared to previous measurements. Much larger increases in noise were observed for pMOS devices exposed to moisture than for nMOS devices. Nearly all of the pMOS devices exposed exhibited a significant increase in noise. The nMOS results were more diverse, with some experiencing small to moderate increases or decreases in noise, and some changing relatively little. The control devices experienced negligible change in noise.

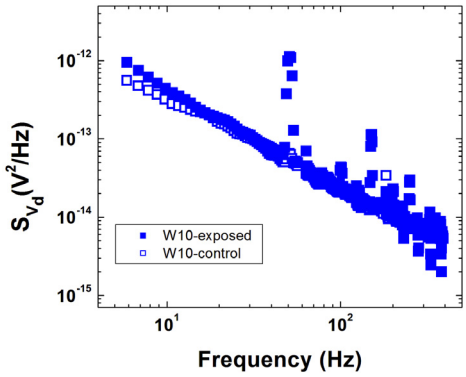

Figure 5: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 2 µm x 16 µm nMOS transistors from the control and moisture-exposed parts from wafer 10, prior to radiation exposure.

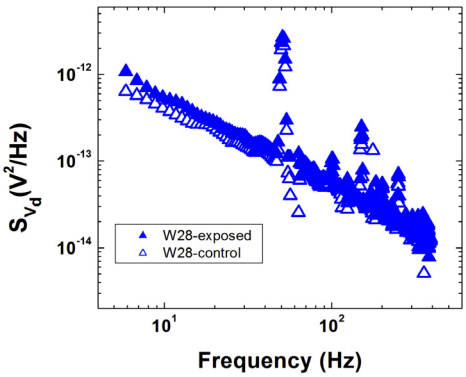

Figure 6: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 2 µm x 16 µm nMOS transistors from the control and moisture-exposed parts from wafer 28, prior to radiation exposure.

Figures 5 and 6 show S_{Vd} versus f for 2 µm x 16 µm (L x W) n-channel moisture-exposed and control transistors from wafers 10 and 28, prior to irradiation. There is negligible difference in the noise between the control and exposed devices of wafer 10, and the noise of the exposed wafer 28 device of is slightly larger than that of the control device.

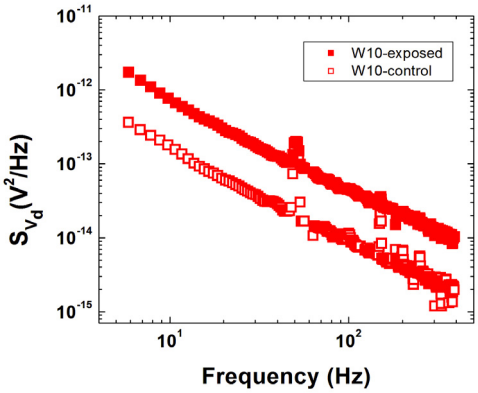

Figure 7: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 2 µm x 16 µm pMOS transistors from the control and moisture-exposed parts from wafer 10, prior to radiation exposure.

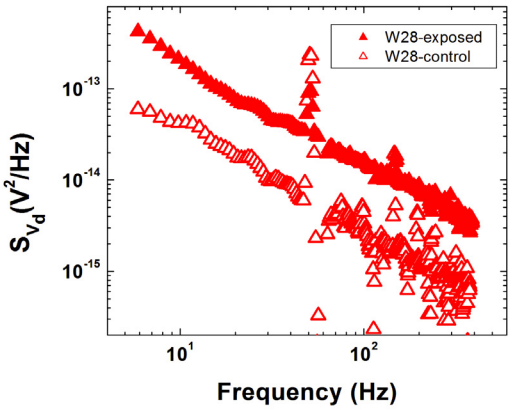

Figure 8: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 2 µm x 16 µm pMOS transistors from the control and moisture-exposed parts from wafer 28, prior to radiation exposure.

Figures 7 and 8 show S_{Vd} versus f for 2 μm x 16 μm (L x W) p-channel moisture-exposed and control transistors from wafers 10 and 28. The noise of the exposed pMOS device is much larger than that of the control device in both cases. Similar results were observed for the other transistors on these parts, and in general for devices exposed to moisture in this study.

These results show that moisture exposure can cause a significant increase in the defects responsible for the 1/f noise in MOS devices (thought to be oxygen vacancy centers near the interface [36], [38], [39]), and indicate a difference in the way the water molecules interact in nMOS and pMOS devices, leading to the observed differences between the noise for each type of exposed device. It has been suggested that these differences may be related to the inhibited diffusion of moisture to the gate oxides in nMOS devices due to phosphorus incorporation in the field oxide regions that are adjacent to and/or overlie the sources and drains. Phosphorus inhibits moisture diffusion; in contrast, boron can enhance moisture diffusion in the gate oxides of pMOS devices. [40], [41].

In addition to an increase in noise, some pMOS devices exposed to moisture experienced significant shifts in threshold voltage. Figure 9 shows threshold voltage curves for 3 μm x 16 μm pMOS transistor from moisture-exposed and control parts from wafer 10. The threshold voltage for these transistors was measured prior to and following moisture exposure, and approximately a month and a half later. The threshold voltage for the exposed transistor continued to shift after the initial exposure. Charge separation techniques indicated a nearly equal buildup of N_{ot} and N_{it} over the measured time span.

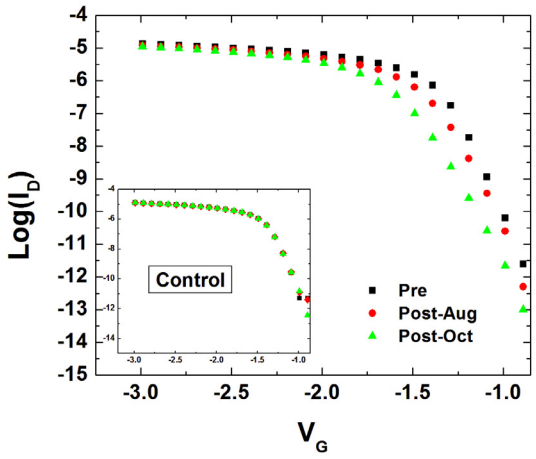

Figure 9: Drain current as a function of gate voltage before and after moisture exposure for a 3 µm x 16 µm pMOS transistor from a moisture exposed part and from a control part.

Gate-Voltage Dependence of 1/*f* Noise

Figures 10 and 11 show S_{Vd} versus f for V_g-V_t = 1, 2, 4, 6, and 8 V for the 3 µm x 16 µm control nMOS and pMOS devices from wafer 10, respectively, prior to irradiation. The noise magnitude of the devices decreases with increasing gate voltage.

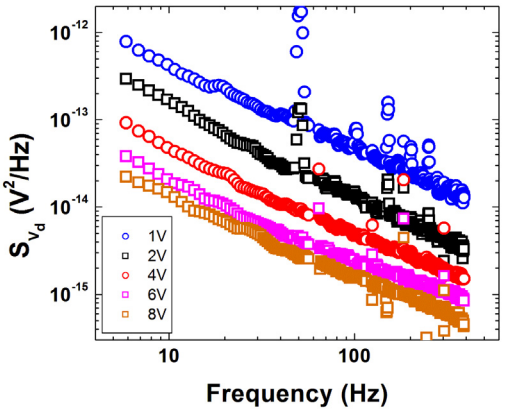

Figure 10: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm nMOS transistor prior to radiation exposure for Vg-Vt = 1, 2, 4, 6, and 8 V.

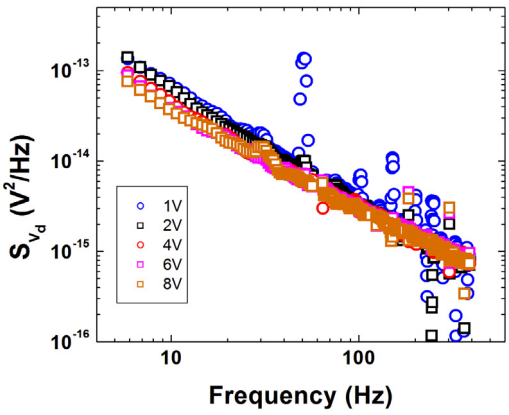

Figure 11: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm pMOS transistor prior to radiation exposure for V_g-V_t = 1, 2, 4, 6, and 8 V.

At a given temperature, to first order, only traps near the Si/SiO_2 interface and whose energy levels are within a few kT of the quasi-Fermi level contribute to the measured 1/*f* noise, as illustrated in Figure 12 below.

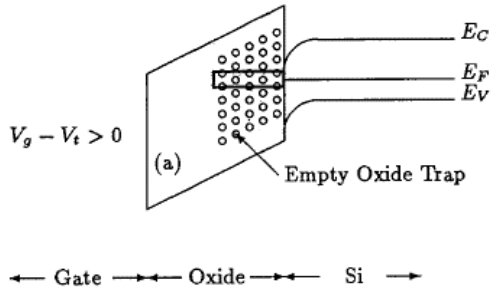

Figure 12: Energy band diagram of an nMOS transistor biased into strong inversion.

The Fermi level changes with temperature, while the trap energy levels move (relative to the Fermi level) with gate voltage, or the silicon energy band edges. As the gate voltage increases, the number of carriers in the device channel increases, making the impact of any trapping or detrapping less significant, resulting in a decrease in the measured noise.

There is a significant difference between the nMOS and pMOS noise shown in Figures 10 and 11. In Figure 10, the frequency exponent, α, is approximately equal to unity for the pre-irradiation nMOS noise, and remains relatively constant with increasing V_g-V_t, indicating a relatively uniform $D_t(E_f)$ [8]. For the pMOS device, however, α is larger than unity at V_g-V_t =1, and decreases as V_g-V_t is increased.

In addition to the different frequency dependences, these devices exhibit markedly different gate-voltage dependences, as illustrated in Figures 13 and 14.

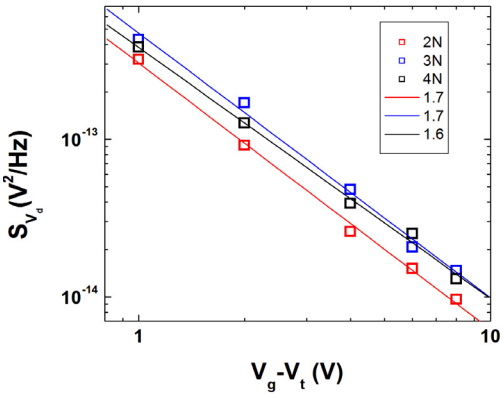

Figure 13: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for nMOS transistors prior to radiation exposure.

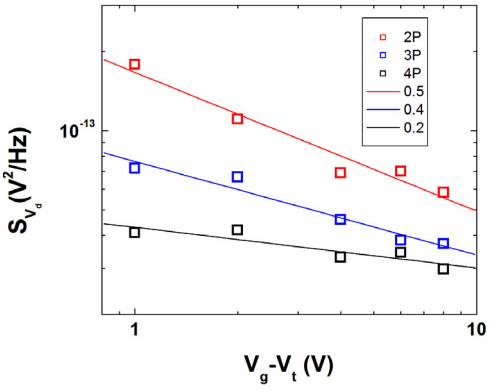

Figure 14: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for pMOS transistors prior to radiation exposure.

Figure 13 plots S_{Vd} at ~10 Hz as a function of V_g-V_t for 2-µm, 3-µm, and 4-µm channel-length nMOS transistors from the wafer 10 control part, prior to irradiation, and Figure 14 plots the gate-voltage dependence data for the wafer 10 pMOS transistors. The solid lines are a best fit to the data, where the slopes of the lines are denoted here as β, and $S_{V_d} \propto (V_g - V_t)^{-\beta}$. For the nMOS devices, β ranges from ~ 1.6 to 1.7, which agrees reasonably well with Eq. (2.11), suggesting a nearly uniform trap distribution [1], [28]. However, for the pMOS device, β ranges from ~ 0.2 to 0.5. This smaller gate voltage dependence suggests a significantly non-uniform trap energy distribution [28]. Similar results were seen for other n- and p-channel devices in this study, prior to irradiation. For the nMOS transistors, β typically ranged from ~ 1.4 to 1.8, while for the pMOS transistors, β ranged from ~ 0.2 to 1.

The gate-voltage and frequency dependences shown in Figures 10-14 are quite consistent with previous reports of nMOS and pMOS devices. For nMOS devices, as fabricated, the gate-voltage dependence generally trends closer to a $(V_g\text{-}V_t)^{-2}$ dependence, while for the pMOS devices, as fabricated, the gate-voltage dependence generally trends more closely to a $(V_g\text{-}V_t)^{-1}$ dependence.

Many studies on MOS 1/*f* noise conclude that the observed differences in gate-voltage dependence for nMOS and pMOS devices result from differences in the mechanisms responsible for the noise in each type of device (i.e., surface effect in nMOS, bulk effect in pMOS). Particularly, a dependence of $\sim(V_g\text{-}V_t)^{-2}$ is often interpreted as evidence for noise dominated by carrier-number fluctuations (Eq. 2.11), [23], [28], [29], [31], while a $\sim(V_g\text{-}V_t)^{-1}$ dependence is often interpreted as evidence for noise dominated by mobility fluctuations (Eq. 2.8), [23], [28]-[31].

Some researchers, however, have suggested that the observed frequency and gate-voltage dependences are directly related to a non-uniform trap energy distribution, one that increases toward the valence band edge [28], [43], [44]. In [28], 1/*f* noise measurements were made on unirradiated nMOS and pMOS transistors as a function of temperature and gate voltage, in order to gain insight into the energy dependence of the defect distributions responsible for the noise. For their nMOS devices, Scofield *et al.* found the noise to be only weakly dependent on temperature, consistent with the expected linear dependence in Eq. (2.11) for a uniform $D_t(E_f)$, resulting in $S_{V_d} \propto V_d^2/(V_g - V_t)^2$. For their pMOS devices, however, they found a much stronger temperature dependence, and concluded that the observed $S_{V_d} \propto V_d^2/(V_g - V_t)$ scaling resulted in a non-uniform $D_t(E_f)$, one that increased rapidly toward the valence band edge. At lower temperatures, where $S_{V_d} \propto T$, they found that $S_{V_d} \propto V_d^2/(V_g - V_t)^2$ for both nMOS and pMOS devices, and that the gate-voltage dependence of the noise deviated from the relation whenever the temperature dependence was much stronger (as was the case with the pMOS devices). With these results, they concluded that both nMOS and pMOS noise could be described with the trapping model given by Eq. (2.11), and that the observed differences in gate-voltage dependence arose from a non-uniform $D_t(E_f)$.

While the researchers in [28] used gate-voltage and temperature measurements to probe and characterize $D_t(E_f)$, the frequency dependence of 1/*f* noise, in a similar manner, can reveal characteristics about the trap energy distribution. In particular, Dutta and Horn showed that the frequency exponent has dependencies on frequency and temperature (Eq. 2.4). For a constant distribution of defect energies (or one that varies slowly with k_BT),

we would expect $S_{V_d} \propto f^{-\alpha}$, with $\alpha \approx 1$ (Eq. 2.2) [8]. However, any non-uniformities in $D_t(E_f)$ would show up in the frequency dependence of the measured noise, i.e., $\alpha \neq 1$ (as shown for the pMOS device in Figure 11). As a result, the gate-voltage dependences of these devices, coupled with their frequency dependences, can reveal significant insight into the nature of the defect energy distributions responsible for the noise.

Radiation Response

The control and moisture-exposed parts were irradiated after all low frequency noise and threshold voltage measurements were made. During irradiation, +6 V was applied to the gates of the devices, and all other pins were grounded. Noise and threshold voltage measurements were made after each dose (with bias conditions the same as described previously), and gate-voltage dependence measurements were made after total dose irradiation, for each transistor.

Figure 15 shows S_{Vd} versus f for 3 µm x 16 µm n-channel exposed and control transistors from wafer 10 before and after total dose irradiation.

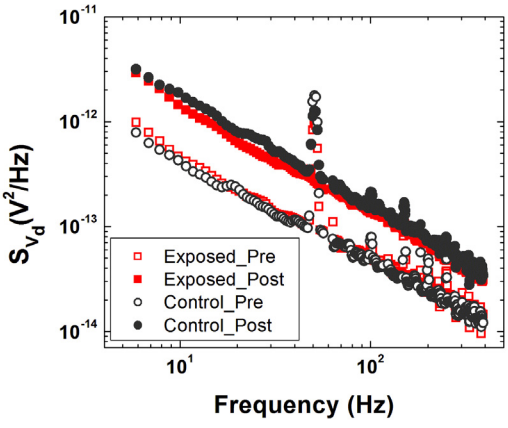

Figure 15: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm nMOS transistors from the control and moisture-exposed parts from wafer 10, before and after500 krad(SiO_2) total dose irradiation.

There is negligible difference between the pre-irradiation noise for the nMOS control and exposed devices, but the post-irradiation noise for the control device is slightly larger than that for the moisture-exposed device. For both the control and exposed devices, α was close to unity before and after irradiation.

Figure 16 shows S_{Vd} versus f for 3 µm x 16 µm p-channel exposed and control transistors from wafer 10 before and after total dose irradiation. The pre-irradiation and post-irradiation noise for the exposed pMOS device is much higher than that for the control pMOS device. For the control pMOS device, prior to irradiation, α = 1.3, and for the exposed device α = 1.2. After irradiation, α = 1.1 for the control device and α = 0.9 for the exposed device, indicating a change in the trap energy distribution [8].

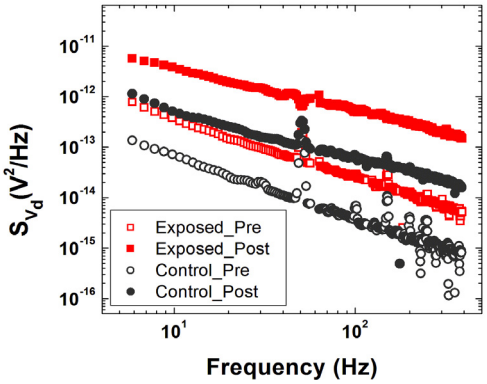

Figure 16: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm pMOS transistors from the control and moisture-exposed parts from wafer 10, before and after500 krad(SiO_2) total dose irradiation.

For the control part, the nMOS device experienced a greater increase in noise than the pMOS device with total dose irradiation; however, for the exposed part, the pMOS device experienced a greater increase in noise.

Figure 17 plots S_{Vd} versus f for V_g-V_t = 1, 2, 4, 6, and 8 V for the 3 µm moisture-exposed nMOS device of Figure 15 after total dose irradiation. $\alpha \approx 1$ for the post-

irradiation noise, and remained relatively constant with increasing V_g-V_t. These results are reflected in Figure 18, where S_{Vd} at ~10 Hz is plotted as a function of V_g-V_t for this device and the 3-µm control nMOS transistor from wafer 10 before and after total dose irradiation.

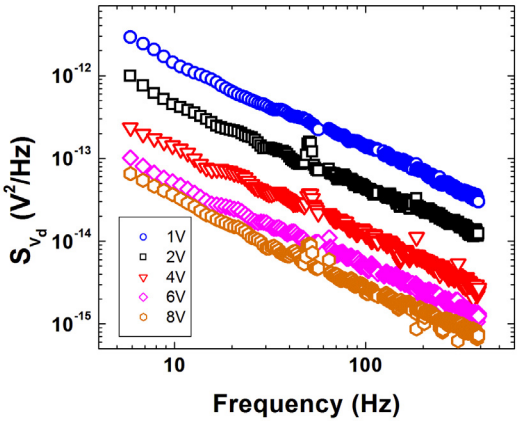

Figure 17: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm nMOS transistor from the moisture-exposed wafer 10 part after 500 krad(SiO_2) total dose irradiation, for V_g-V_t = 1, 2, 4, 6, and 8 V.

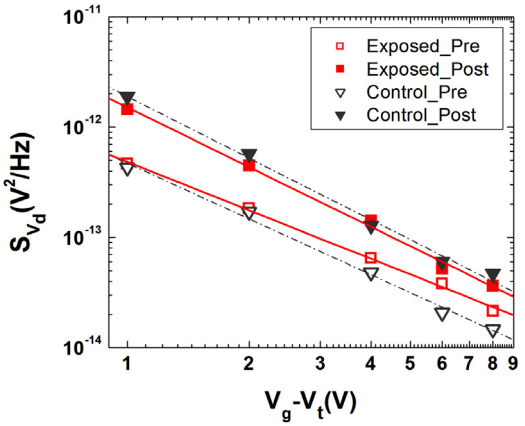

Figure 18: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of V_g-V_t for 3 µm x 16 µm nMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO_2) total dose irradiation. For the control device, prior to irradiation, β = 1.7 and after irradiation β = 1.9; for the exposed device, prior to irradiation, β = 1.5 and after irradiation β = 1.8.

There is relatively little change in the gate-voltage dependence of the noise for each nMOS device after irradiation, with $\beta \approx 2$ for both devices, indicating a uniform $D_t(E_f)$ before and after irradiation.

Figure 19 shows S_{Vd} versus f for V_g-V_t = 1, 2, 4, 6, and 8 V for the 3 µm x 16 µm moisture-exposed pMOS device from Figure 16. In contrast to the pre-irradiation noise of Figure 6, $\alpha \approx 1$ for V_g-V_t = 1 and increases with increasing V_g-V_t. This change in gate-voltage dependence is illustrated again in Figure 20, where $\beta \approx 2$ for the moisture-exposed device after total dose irradiation.

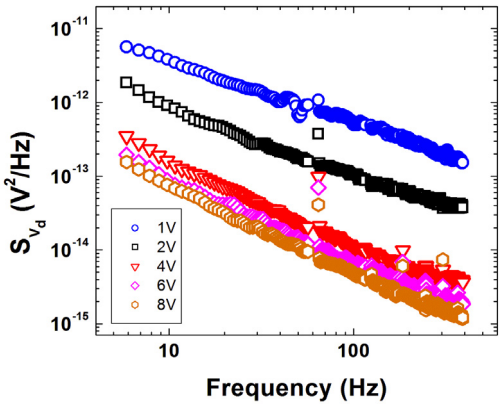

Figure 19: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm pMOS transistor from the moisture-exposed wafer 10 part after 500 krad(SiO_2) total dose irradiation, for V_g-V_t = 1, 2, 4, 6, and 8 V.

Figure 20 shows S_{Vd} at ~10 Hz as a function of V_g-V_t for the moisture-exposed and control pMOS devices from wafer 10 before and after irradiation. For the pMOS devices, there is a significant change in the gate-voltage dependence, signified by the increase in α after irradiation. These results, along with those in Figure 19, suggest a change in the trap energy distribution with irradiation.

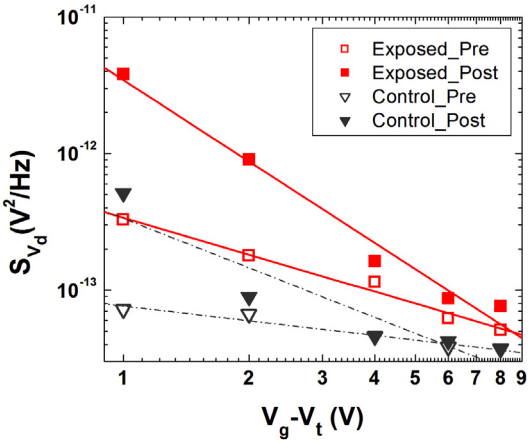

Figure 20: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for 3 µm x 16 µm pMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO_2) total dose irradiation. For the control device, prior to irradiation, β = 0.4 and after irradiation β = 1.2; for the exposed device, prior to irradiation, β = 0.9 and after irradiation β = 2.0.

Figures 15-20 clearly demonstrate the different frequency and gate-voltage dependences observed for nMOS and pMOS devices, especially the complexity of these dependences and the difficulty it has presented in the past in analyzing MOS 1/*f* noise. From our results, relatively little difference was observed between the S_{Vd} curves of the exposed and control nMOS devices, and the frequency exponent α remained close to unity before and after irradiation. For the pMOS devices, however, there is a change in slope of the S_{Vd} curves after irradiation, corresponding to a decrease in α, suggesting a change in the trap spatial or energy distributions [8], [40], [42].

The pre-irradiation gate-voltage dependences of the nMOS and pMOS devices presented here are consistent with trends reported by others, and with the room temperature results reported in [28]. However, after irradiation, the gate-voltage dependence of the pMOS devices changes significantly, trending closer to a dependence of ~$(V_g\text{-}V_t)^{-2}$. While it is possible that the pre-irradiation noise of these devices is dominated by mobility fluctuations and the post-irradiation noise is dominated by number

fluctuations, it seems much more likely, and more consistent with the noise frequency exponent changes in Figure 16, that irradiation has changed not only the defect density in these devices, but also its energy distribution [45], [46]. Particularly, before irradiation, the frequency exponent is greater than unity and the gate-voltage dependence is significantly less than $(V_g\text{-}V_t)^{-2}$, signifying a trap energy distribution that most likely is strongly increasing as it approaches the valence band edge. However, after irradiation, the frequency exponent is close to unity, with a gate voltage dependence of $\sim(V_g\text{-}V_t)^{-2}$, consistent with a more uniform defect energy distribution [8], [27], [28]). This reinforces and extends the conclusions of [28], which focused only on the temperature and gate-voltage dependences of devices that were neither exposed to moisture nor irradiated.

Results from other transistors from this wafer, and from different wafers in this study, confirm this behavior. Figures 21 and 22 show S_{Vd} at ~10 Hz as a function of $V_g\text{-}V_t$ for 2-µm nMOS and pMOS transistors, respectively, from the control wafer 28 part before and after 100 krad(SiO_2) total dose irradiation.

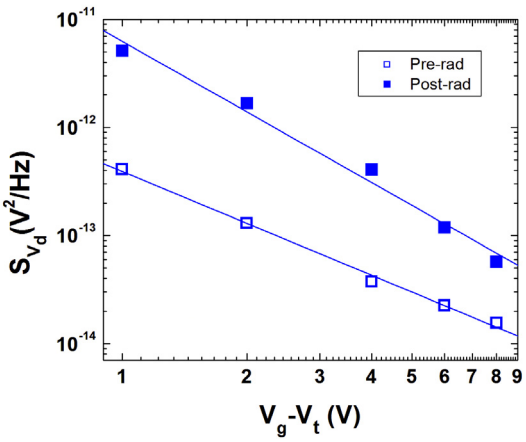

Figure 21: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for 2 µm x 16 µm nMOS transistor from the control part from wafer 28, before and after 100 krad(SiO_2) total dose irradiation. Prior to irradiation, β = 1.6 and after irradiation β = 2.2.

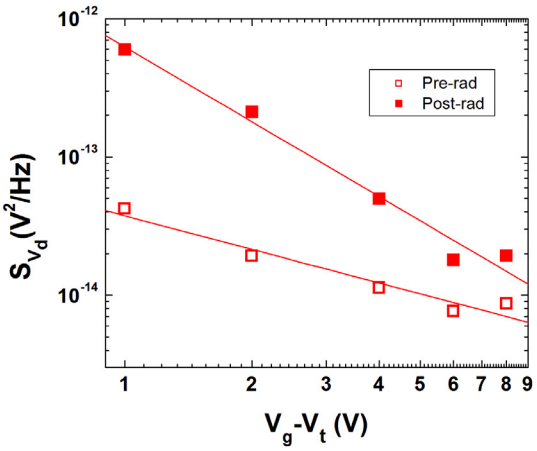

Figure 22: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for 2 µm x 16 µm pMOS transistor from the control part from wafer 28, before and after 100 krad(SiO_2) total dose irradiation. Prior to irradiation, β = 0.8 and after irradiation β = 1.8.

There is a more pronounced change in the gate-voltage dependence of the nMOS device with irradiation. Here, β = 1.6 before irradiation, and after β = 2.2, where $S_{V_d} \propto (V_g - V_t)^{-\beta}$, in reasonable agreement with Eq. (2.11), and with previous results. For the pMOS device, prior to irradiation, β = 0.8, and after irradiation, β = 1.8.

Devices from different wafers and process lot, control and moisture-exposed, were also studied, and similar results were observed. However, in some cases, the observed gate-voltage dependence was more complicated. For some of the exposed devices, the change in gate-voltage dependence after irradiation was much larger than those presented previously; in fact, many of these devices exhibited a post-irradiation β value closer to 3. Gate-voltage measurements were repeated on one of the devices, approximately two weeks later, to determine if annealing during the original measurements had affected the observed gate-voltage dependence. However, there was no appreciable change in α between the second measurements and the initial ones.

Figure 23 shows the gate-voltage dependence of moisture-exposed pMOS devices from wafer 16 after 500 krad(SiO_2) total dose irradiation.

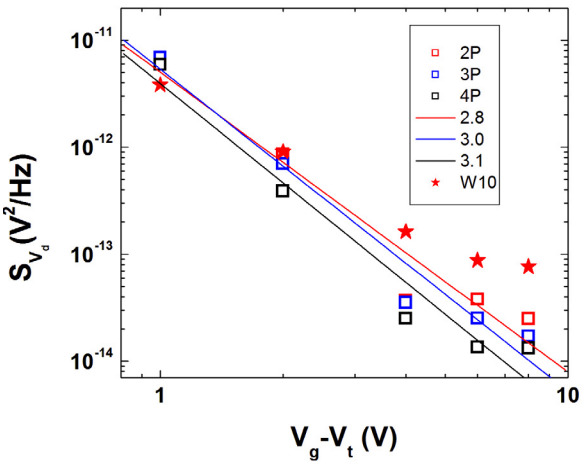

Figure 23: Excess drain-voltage spectrum S_{Vd} at ~10 Hz as a function of Vg-Vt for moisture-exposed pMOS transistors from wafer 16 after radiation exposure; pMOS data from wafer 10 plotted for comparison.

For the all three transistor channel lengths, $\beta \approx 3$ over a significant fraction of the voltage range. To the best of our knowledge, this behavior has not been reported in the literature. One possible explanation is that irradiation has completely altered the trap energy distributions for these moisture-exposed devices in a manner similar to that reported previously using capacitance-voltage and AC conductance measurements [45], [46], but which to our knowledge has not been studied in this kind of detail previously using noise measurements. In particular, the trap energy distribution is now decreasing toward the valence band edge (opposed to increasing toward E_V with $\beta \approx 1$ prior to irradiation, or more uniform throughout the band gap with $\beta \approx 2$), resulting in the larger than expected disparity between S_{Vd} with varying gate voltage. For comparison, the gate-voltage dependence of the pMOS device from wafer 10 (post-irradiation, $\beta \approx 2$) has been

plotted with this data, represented by the solid star symbols. The frequency exponent α of these devices changes significantly with irradiation, as shown in Figure 24 for the 3-µm device. For V_g-V_t = 1, α is much less than unity, but increases with increasing V_g-V_t, which is consistent with results from the other irradiated pMOS devices in this study.

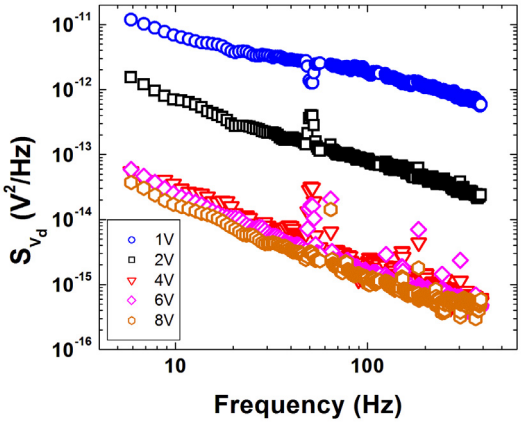

Figure 24: Excess drain-voltage spectrum S_{Vd} as a function of frequency for 3 µm x 16 µm pMOS transistor from the moisture-exposed wafer 16 part after 500 krad(SiO_2) total dose irradiation, for V_g-V_t = 1, 2, 4, 6, and 8 V.

CHAPTER V

CONCLUSIONS

Exposure to humidity at elevated temperatures clearly impacts MOS 1/*f* noise and radiation response, and does so differently for n-channel and p-channel transistors; these differences may be related to the inhibited diffusion of moisture in the nMOS devices due to the presence of phosphorus in the field oxide regions. The effects of moisture exposure on 1/*f* noise are more significant for pMOS devices than nMOS devices. For parts that were exposed to moisture, the pMOS devices experienced a significant increase in noise overall, while the effects on nMOS noise were more mixed. Additionally, it was observed that the threshold voltage of some of the exposed pMOS devices could change with time after the initial exposure, indicating a continuing build-up of charge. After irradiation, the moisture-exposed pMOS devices experienced a greater increase in noise than the exposed nMOS devices.

Prior to irradiation, the gate-voltage dependences of the noise of the nMOS and pMOS devices were consistent with those reported by other researchers. For the nMOS devices, a dependence of $\sim(V_g\text{-}V_t)^{-2}$ was generally observed, while for the pMOS devices the dependence was significantly reduced. The former results are often cited as evidence for noise dominated by number fluctuations, while the latter are often cited as evidence for noise dominated by mobility fluctuations. After irradiation, there was no significant change in the gate-voltage dependence of the noise for the nMOS devices. However, the pMOS devices showed a much greater change after irradiation, with an observed gate-

voltage dependence of $\sim(V_g\text{-}V_t)^{-2}$. We conclude that these results can be explained by a simple trapping model (Eq. 2.11), and that the $1/f$ noise of both nMOS and pMOS devices originate from fluctuations in the channel carriers of each device. Differences in the gate-voltage dependence of the noise for nMOS and pMOS devices are attributed to a non-uniform trap energy distribution that increases toward the valence band edge, leading to a $\sim(V_g\text{-}V_t)^{-1}$ dependence for pMOS devices. Irradiating the devices not only increased the defect density in both devices (corresponding to the observed increase in noise), but also altered its energy distribution, leading to a much more uniform trap distribution for pMOS devices (corresponding to the observed $\sim(V_g\text{-}V_t)^{-2}$ dependence and change in frequency exponent). Furthermore, we conclude that the frequency and gate-voltage dependencies of the noise can provide a valuable means of revealing changes in the trap energy distribution of these devices before and after radiation exposure.

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