

THE RADIATION RESPONSE AND LONG TERM RELIABILITY OF HIGH-K
GATE DIELECTRICS

By

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CHAPTER I

INTRODUCTION

Space systems rely on advanced microelectronic devices to perform functions including communication, control, imaging, and power conversion. While in space, the electronics are exposed to various forms of radiation, including electrons, protons, neutrons, and heavy ions. The radiation may produce effects in the electronics ranging from temporary loss of data to catastrophic failure. Device failure can occur because of long-term degradation caused by continuous exposure to the space-radiation environment (total dose effects) or as a result of transient, high energy particle radiation (single event effects). The specific effects produced depend strongly on the specific technology and the radiation environment. Most space systems are designed conservatively using electronic parts that are at least several generations behind the current state of the art. However, the demand for higher performance and reduced time from design to flight has increased the pressure to use advanced technologies in space. The effects of radiation in some advanced technologies are poorly understood, or in some cases, completely unknown. At present it is not clear that it will be possible to use some advanced technologies in space, no matter how impressive the performance they promise. In addition, highly scaled devices may be sensitive to the naturally occurring radiation at the earth's surface, even though the atmosphere provides significant protection.

Scaling has enabled IC manufactures to increase production exponentially, while decreasing cost at nearly the same rate [1]. For the past ~ 30 years devices have been scaled such that performance doubled as the cost was cut in half every 2-5 years, resulting in a four order of magnitude increase in processor speed and throughput since 1970 [1, 2]. However, modern complementary metal oxide semiconductor (CMOS) devices are rapidly approaching the intrinsic physical scaling limit for Si/SiO₂. Therefore, to keep pace with Moore's Law, which says the number of transistors on a chip should double every two year, IC manufacturers are considering new materials for devices in the near future. The current practice in the semiconductor industry is to manufacture devices with SiO₂ or nitrided SiO₂ gate oxides that are only a few monolayers thick [3, 4]. For example, Intel's transistors for the upcoming 90 nm technology node are projected to have 50 nm gate lengths and 1.2 nm gate oxides [5–7], corresponding to only about 4 mono-layers of SiO₂. If one assumes that two of these layers are actually suboxide interfacial layers at the substrate and the gate, there are really only two atomic layers of stoichiometric "SiO₂" in these transistors. According to Dennard's

constant field scaling method, the operating voltages should be scaled in conjunction with the device dimensions [8, 9]. However, in practice, device operating voltages have been scaled less aggressively than the device dimensions. Hence, devices with ultra-thin oxides operate at rather large electric fields [10, 11]. This has raised concerns about the long-term reliability of devices with highly scaled gate oxides. Furthermore, devices with oxides thinner than $\sim 4\text{-}5$ nm also exhibit large off-state leakage currents (i.e., 1 to 10 A/cm²) since carriers are able to tunnel directly between the substrate and gate electrode [12–14]. This is a significant concern for space systems and mobile electronics where power conservation is essential. To reconcile the need for reduced off-state leakage currents in highly scaled devices, several high dielectric constant (high- κ) alternative gate dielectrics to SiO₂ are being investigated for incorporation into future ICs [14–23].

Finding a material to replace silicon dioxide is a formidable challenge because SiO₂ is a nearly perfect gate dielectric. Some of the most notable properties of silicon dioxide, which will likely be difficult to match with alternative gate dielectric materials are: (1) it is amorphous and remains thermodynamically stable on Si to temperatures exceeding 1100 °C, (2) it has a wide band gap (9 eV) with large (> 2.5 eV) conduction and valence band offsets for Si, (3) it is nearly insoluble in water, (4) it has a high breakdown strength (ultra-thin oxides can maintain electric fields of up to ~ 15 MV/cm), and (5) it can be processed with low ($\sim 10^{10}$) densities of bulk and interfacial defects. Indeed, the only notable drawback to SiO₂ is that it has a relatively low dielectric constant (3.9). Some of the high- κ materials being considered for integration into future IC technologies are Al₂O₃, HfO₂, ZrO₂, Y₂O₃, TiO₂, and Ta₂O₅ and/or the silicates and aluminates of some of these materials [13–15, 17, 22, 24, 25]. Each of these materials has advantages and disadvantages, but none of them are currently at the material quality level of SiO₂. Still, all of these alternative gate dielectrics have a larger dielectric constant than SiO₂. Therefore it is possible to manufacture a gate stack that is physically thicker, yet electrostatically shows a capacitance that is similar to an ultra-thin SiO₂ layer. The increased physical thickness significantly reduces the probability of tunneling across the insulator, and therefore reduces the amount of off-state leakage current [14, 15, 17, 19–21, 24, 26, 27]. However, an increased dielectric constant comes at the expense of a smaller band gap and smaller conduction and valence band offsets between the substrate and the gate dielectric [14, 17, 28]. With the exception of Al₂O₃, most high- κ materials have a conduction band offset of only $\sim 1.5\text{-}2$ eV [29, 30]. Because leakage current increases exponentially with decreasing film thickness and barrier height [31, 32], this trade-off between dielectric constant and barrier height will limit the relative advantages an alternative dielectric offers in terms of reduced

leakage current compared to devices with standard thermal gate oxides. Still, the initial data in the literature are promising, and most high- κ gate dielectrics exhibit ~ 5 orders of magnitude less leakage current than electrically equivalent SiO_2 [17, 20, 23, 26].

An alternative gate dielectric ideally needs to be integrated into standard CMOS processes without major restructuring of the process flow. Many high- κ gate dielectrics have exhibited encouraging electrical and materials characteristics, but there are still problems that need to be solved before high- κ gate dielectrics can be incorporated effectively into commercial ICs. Interfacial layer formation is one of the largest obstacles to high- κ integration. For maximum capacitance, it is best to have the high- κ material in direct contact with the Si substrate. However, it is currently difficult to create high quality direct interfaces between high- κ materials and Si. Therefore, to improve interface quality it is common practice to use interfacial barrier layers (oxides or oxynitrides). The purpose of an interfacial layer is to take advantage of the natural Si-SiO₂ interface while also incorporating a high- κ material to increase the capacitance and thickness and thereby reduce the direct tunneling probability. Nitrided interfacial layers are also used to limit dopant diffusion into the channel. In a standard polysilicon CMOS process, the gate electrodes are implanted with dopants such as phosphorous and boron [33]. The devices are then annealed at temperatures close to 1000 °C to activate the dopant and distribute it throughout the polysilicon. If the dopants are able to diffuse through the gate insulator into the channel, they can change the threshold voltage of the device, or in large quantities, can increase drain to source leakage current. The problem is that a low permittivity interfacial layer reduces the capacitance of the gate stack and ultimately limits the effectiveness of the high- κ material. Even if it is possible to create a clean interface between silicon and a freshly deposited alternative gate dielectric, it is difficult to maintain that interface throughout a standard process flow because most high- κ materials are not good oxygen diffusion barriers [14, 21, 34]. Oxygen uptake is slowest for Al_2O_3 , but even modest oxygen pressures are enough to cause significant interfacial oxidation [34]. In practice, interfaces that are nearly free of oxidized silicon have been achieved in a few systems, most notably as deposited $\text{Al}_2\text{O}_3/\text{Si}(001)$ [35]. Still, avoiding silicon oxidation has been difficult in other materials systems. For Group IV metal oxides (HfO_2 and ZrO_2) there is typically an unintentional interfacial layer of SiO_2 that is ~ 0.5 nm thick [35–37].

In contrast to SiO_2 , most high- κ materials experience a phase change from amorphous to crystalline at relatively low temperatures (~ 400 °C to 800 °C) [15, 33, 37]. The crystallization temperature can be increased by adding SiO_2 (silicates) or Al_2O_3 (aluminates) to the metal oxide (HfO_2 ,

ZrO₂, etc.) to form alloys [25,28]. However, for these materials to stay amorphous at temperatures near 1000 °C, the composition must be configured strongly toward pure SiO₂ or Al₂O₃, and will therefore have a significantly reduced dielectric constant. The issue is that with film crystallization comes an increase in leakage current. However, polycrystalline yttrium oxides have shown relatively low leakage levels [15], so it is unclear whether an amorphous film is absolutely necessary.

Furthermore, it is important to understand the stability and long-term reliability of these materials to ensure the problems associated with ultra-thin SiO₂ are not simply traded for an even larger set of problems with alternative dielectrics. Moreover, before these materials can be used for space applications, it is equally important to understand their radiation response. In this thesis the radiation response and long term reliability of several high- κ materials is evaluated. Chapter II is an introduction, which provides a brief overview of total dose and single event radiation effects in microelectronics and a discussion of radiation effects in nitrated gate oxides. Chapter III is a discussion of the radiation response of aluminum oxide capacitors and transistors and chapter IV covers hafnium based dielectrics. Chapter V describes how to compare the relative material qualities and radiation responses of high- κ dielectrics by calculating an effective charge trapping efficiency. The long term reliability of these materials is discussed in chapter VI, and chapter VII provides the summary and conclusions of this work.

CHAPTER II

EFFECTS OF RADIATION

Total Dose Radiation Effects

Ionizing radiation degrades a CMOS integrated circuit by producing electron hole pairs (EHPs) in the gate and isolation dielectrics. Some of the radiation-induced charge recombines and does not affect the device. The percentage of EHPs that escape initial recombination (i.e., the charge yield) depends on the oxide electric field [38, 39]. A large electric field will separate the charges more efficiently, leading to fewer recombination events [38, 40]. A significant fraction of the remaining radiation-induced charge can become trapped at micro-structural defects in the dielectric. The mechanism for radiation-induced charge generation and charge trapping in SiO₂ gate dielectrics is shown by the energy band diagram in Fig. 1. This figure shows a metal gate, p-substrate MOS capacitor, irradiated under positive gate bias. For this bias condition, the electrons are swept out toward the gate electrode, while the holes transport toward the Si/SiO₂ interface via defect sites in the oxide [39]. Some of the unrecombined holes will become trapped in the oxide, forming a positive oxide trapped charge density. As shown in Fig. 1, protons are released during hole transport to the interface and as holes are trapped near the Si/SiO₂ interface. These protons have been linked to radiation-induced interface trap formation in devices with SiO₂ gate oxides. Although Fig. 1 only shows hole trapping in the oxide, most gate dielectrics can also trap a significant density of electrons. Indeed, some HfO₂ films have exhibited more electron trapping than hole trapping after exposure to ionizing radiation [41]. However, the radiation-induced oxide trapped charge in SiO₂ and alternative dielectrics is generally net positive [42–44].

Historically, the gate oxides of CMOS devices were relatively thick and radiation-induced charge buildup in gate oxides was a major concern. Fortunately, as an IC technology is scaled and the gate oxide thickness is decreased, the radiation hardness of thermally grown gate oxides (SiO₂) can improve dramatically. Figure 2 is a plot of the threshold-voltage shifts due to interface-trap and oxide-trapped charge for dry and steam grown (wet) oxides [45]. The threshold-voltage shifts due to both types of charge decrease with slightly less than a t_{ox}^2 thickness dependence ($t_{ox}^{1.5}$ to $t_{ox}^{1.8}$). Thus, excellent total-dose hardness is a supplementary benefit of aggressive gate oxide scaling. For very thin oxides (<20 nm), there is evidence that the amount of radiation-induced

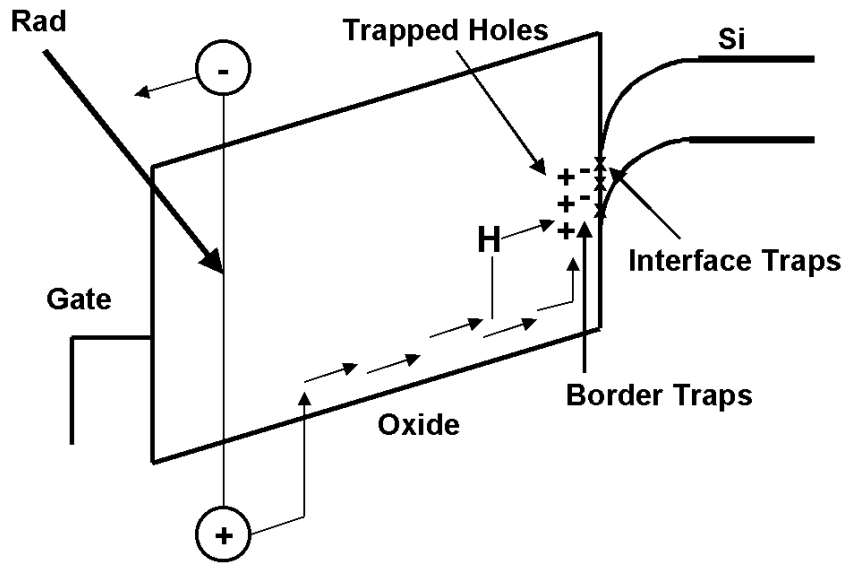


Figure 1: Energy band diagram showing ionizing radiation creating electron-hole pairs in the SiO₂ layer of a MOS capacitor under positive gate bias. After [39].

oxide-trap charge decreases with an even faster dependence on oxide thickness [46]. Because of the improvement in hardness with decreasing thickness, thermally grown gate oxides in advanced commercial technologies can be extremely radiation hard, withstanding accumulated doses in excess of 1 Mrad(SiO₂) with little threshold voltage shift. With high- κ gate materials, much thicker dielectrics can be used to obtain the equivalent capacitance of much thinner SiO₂ gates. This raises the concern that gate oxide radiation response could be degraded if high- κ dielectrics are used in place of ultra-thin SiO₂.

Oxide Traps

Oxide-trapped charge is net positive charge located in the bulk and near interfacial region of the gate dielectric, which forms as holes become trapped at defect sites in the dielectric. The precursor trap densities for high- κ devices reported in the literature are typically \sim 1-2 orders of magnitude larger than is usually achieved for high quality thermal SiO₂ [13, 14, 47]. The density of oxide-trapped charge is greatest immediately following radiation exposure with some annealing occurring slowly over time due to electron tunneling from the Si or thermal emission of holes from the trap sites [48–50]. Positive charge trapping in the gate oxide can invert the channel interface for nMOS devices causing leakage current to flow in the OFF state condition ($V_{GS} = 0$ V). This will result in an increase in the static power supply current of an IC and may cause IC failure. In

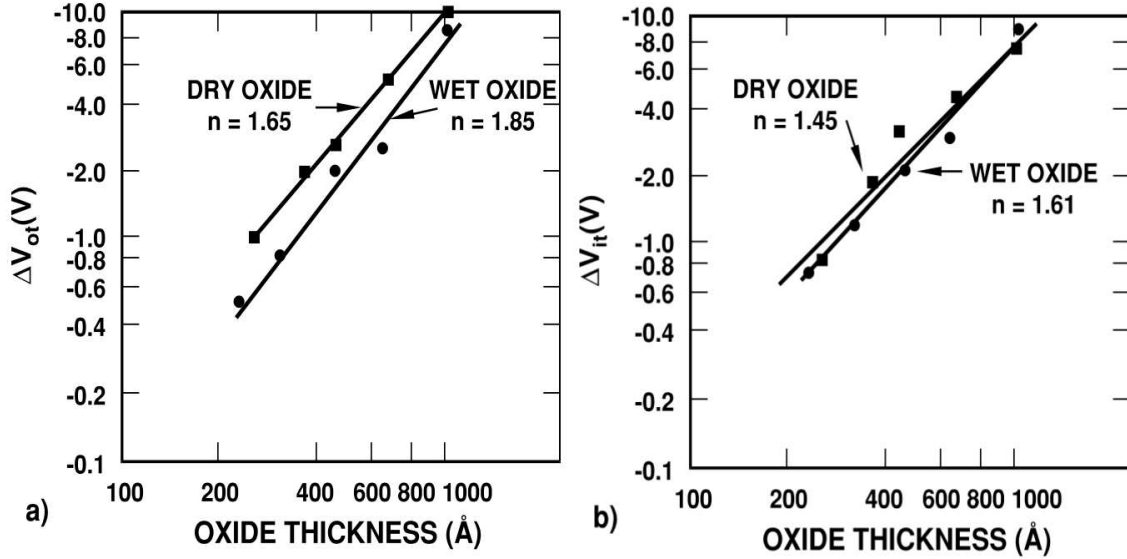


Figure 2: The dependence of the threshold-voltage shift due to a) oxide-trap and b) interface-trap charge on oxide thickness. After [45].

a similar fashion, positive charge buildup in isolation oxides (field oxides and silicon-on-insulator (SOI) buried oxides) can cause large increases in IC static power supply leakage current.

The most widely accepted precursor leading to the formation of oxide-trap charge in SiO_2 is the E' center or oxygen vacancy [51–54]. An oxygen vacancy can result from implantation damage or from out-diffusion of oxygen during a post-oxidation, high temperature, annealing cycle [55]. The number of oxygen vacancies in a given technology is therefore dependent on the process. As discussed in detail in chapters III and IV, high- κ gate dielectrics show significant changes in trapping properties with processing variations. In 1992, Warren *et al.* discussed several possible structures for E' centers in amorphous SiO_2 [51]. Since then, it has been determined that the E'_γ center is the most probable precursor to oxide-trapped charge formation in SiO_2 [52–54]. Fig. 3 shows a diagram of the E'_γ trapping center with part (a) representing the precursor to the oxide trap ($\text{O}_3 \equiv \text{Si}-\text{Si} \equiv \text{O}_3$) and part (b) showing a hole trapped by the precursor site ($\text{O}_3 \equiv \text{Si}^\uparrow + \text{Si} \equiv \text{O}_3$).

For alternative dielectrics, there has been little work done to understand defect microstructure. However, it is likely that a defect similar to an E' center exists in most high- κ films in addition to other possible defect centers related to the stoichiometry of a particular high- κ material. Charge trapping in alternative gate dielectrics is a significant concern [56–62]. Researchers at IBM have shown that the probability of bias induced charge trapping in high- κ gate dielectrics is extremely

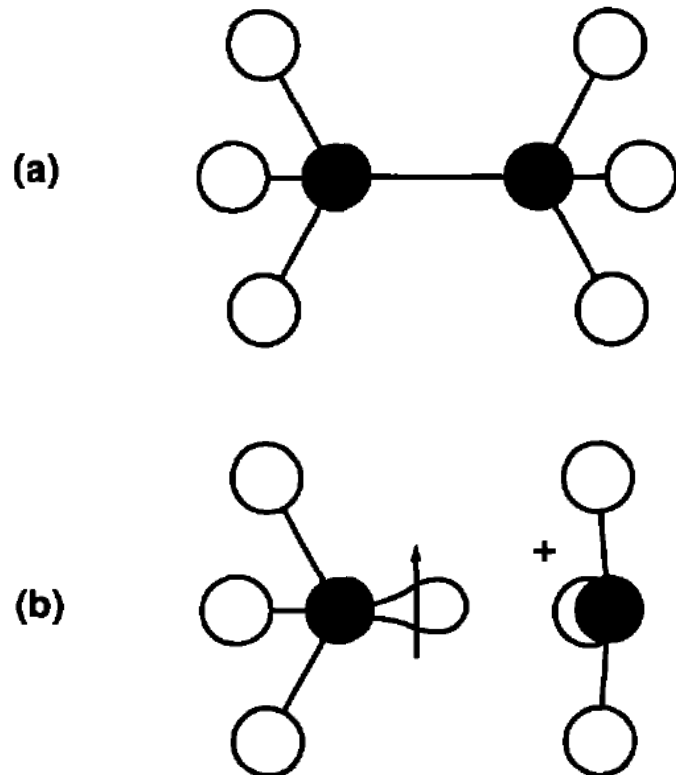


Figure 3: Schematic diagram of an E'_γ center, showing the characteristic strained Si-Si bond precursor state and the charged EPR active state. After [51].

high due to the large densities of intrinsic defects [56–59]. This is different than the behavior of SiO_2 , which generally has very few “as grown” defects, and defects are created during stressing [56].

Interface Traps

In addition to oxide trapped charge buildup, ionizing radiation can also change the interface trapping properties of devices. Interface traps are located directly at the interface with energy levels that exist within the silicon band gap [45]. Traps in the lower half of the band gap are donor like, meaning they are neutral when filled and positively charged when empty [45]. In contrast, interface traps in the upper portion of the band gap are acceptor like, meaning they are neutral when empty and negatively charged when filled [45]. Trap sites with energies a few kT below the Fermi level (determined from Fermi statistics) are filled, and trap sites with energies a few kT above the Fermi level are empty. The number of occupied or unoccupied trap sites at the interface is therefore bias dependent because the amount of band bending determines the number of interface traps above and below the Fermi level. Thus, when a device is biased at midgap, interface traps are neutral [63,64]. Interface trapped charge causes negative threshold voltage shifts in p-channel transistors, positive

threshold voltage shifts in n-channel transistors, and channel mobility degradation [65,66]. These effects can decrease the drive of transistors and degrade the timing parameters of an IC. In contrast to oxide traps, interface trap density is at a minimum immediately following radiation exposure and slowly builds up with time [65,67]. In circuits, interface traps decrease the noise margin and increase the switching time.

The underlying mechanisms for interface trap formation in SiO₂ and in alternative gate dielectrics is not completely understood. The most widely accepted model of interface trap formation in SiO₂ is that hydrogen species, released during hole transport in the oxide, migrate to the Si/SiO₂ interface and react with silicon dangling bonds to form interface traps [65,67–69]. Much work is still being done to study both hydrogen motion in SiO₂ and the detailed microstructure of interface traps. However, a dangling Si bond that is passivated by a hydrogen atom (H-Si≡Si) is currently considered the most likely precursor to interface trap formation in SiO₂ [52–54, 70]. Interfacial defect microstructure in alternative gate dielectrics is still largely unknown.

Border Traps

The term border trap was first suggested by D.M. Fleetwood in 1991 [71]. Simply put, border traps are oxide traps that are able to exchange charge with the silicon on the time scale of the electrical measurements. This property of being able to exchange charge with the silicon during the measurement causes border traps to look like interface traps electrically; however, these defects are in the oxide and not at the interface. There is still some debate as to the underlying microstructure of border traps, and it is likely that there is not a single defect for all border traps in all materials and devices [71]. In this work low frequency ($1/f$) noise measurements are used estimate the border trap density in Al₂O₃/oxynitride transistors.

Single-Event Effects

In addition to total dose ionization damage, energetic particles such as protons, alpha particles, and heavy ions associated with space environments can also cause single-event effects (SEE). As a single high-energy particle (e.g., energetic heavy ion, proton, alpha particle, or neutron) strikes a material, it generates a dense plasma of electron-hole pairs along the path of the particle, which can trigger a variety of SEE. Single-event effects are classified into two types: soft errors, which cause no permanent damage and may be correctable, and hard errors, which result in permanent damage to the device. A single event upset (SEU) is an example of a soft error, where only the logic state of the circuit is changed. SEUs were first observed in space in 1975 [72]. Soft errors can generally be corrected by reloading the original information into a memory element or by restarting an algorithm

in a CPU. If the error rate caused by single-event upsets is too high, performance degradation and even system failure can result. Hard errors are observed in circuits where large electric fields are present across insulating layers, such as nonvolatile memories and thin gate oxides. For example, permanent damage can be induced by energy deposition in a small region of the dielectric after the passage of a high-energy particle. This effect is known as single-event gate rupture (SEGR). Protons and heavy ions may also trigger high-current conditions that can result in permanent circuit failure. Examples of this type of hard error are single-event latchup (SEL) in CMOS and bipolar ICs, single-event snap-back (SESB) in nMOS devices, and single-event burnout (SEB) in power transistors [73].

Radiation-induced hard breakdown

A major consideration for designers of space systems is a catastrophic failure known as radiation-induced hard breakdown (RHB) (also called single event gate rupture (SEGR)) [74–76]. This effect can occur under conditions of high field, such as during a write or clear operation in a nonvolatile SRAM or E²PROM. It has recently become a concern for advanced technologies as oxide thicknesses scale below 10 nm and oxide fields increase above 5 MV/cm [77]. As a heavy ion passes through the dielectric, a highly conductive plasma path is formed, which allows the capacitor formed by this structure to discharge. If sufficient energy is stored on the capacitor due to high electric fields, excessive heating during discharge can create a thermal runaway condition [74]. Temperatures can be high enough to cause the dielectric to melt and the overlying conductive layers to evaporate.

The industry trend toward increasing electric fields as oxide thickness and feature size scale down in advanced technologies has raised concern that RHB may be a limiting factor for integrated circuits (ICs) in space applications. It was suggested that, as devices scaled to 0.25 μm and below, RHB by Fe ions will occur, leading to a large increase in catastrophic failures in space hardware. Sexton, *et al.* [77] found that, as oxide thickness decreased below 10 nm, the increasing breakdown strength of the oxides resulted in a higher than expected gate voltage for rupture, contrary to earlier predictions. Their results suggest that advanced technologies will be more RHB resistant at a given electric field than expected. They cautioned, however, that RHB will continue to be a significant concern for devices that operate with gate oxide electric field above 5 MV/cm.

Massengill *et al.* found that for highly scaled (ultra-thin) gate oxides and alternate high- κ dielectrics, RHB should not be a limiting factor in advanced technologies [78]. Figure 4 is a plot of the voltage to breakdown for capacitors versus dielectric thickness for several different nitrided and high- κ dielectrics, as well as for SiO₂. These capacitors were exposed to 342-MeV gold ions.

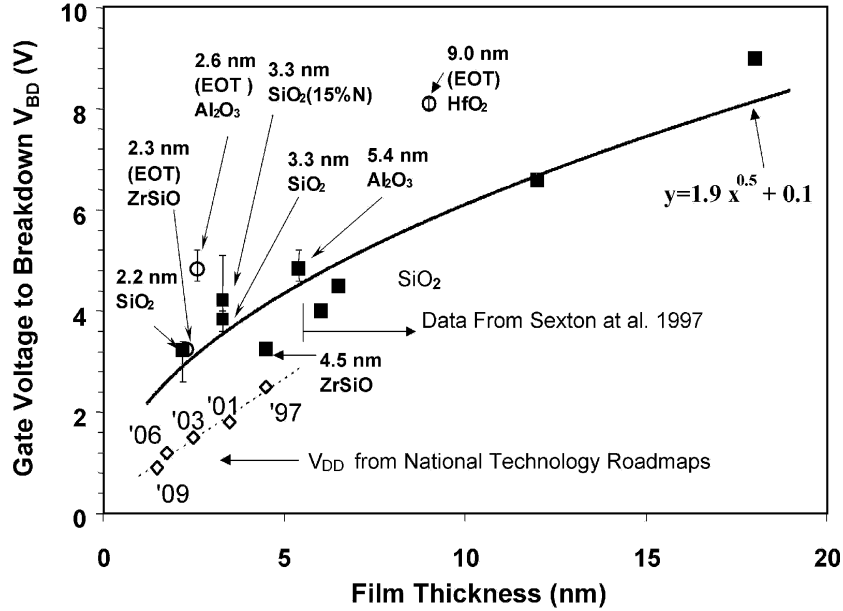


Figure 4: Gate voltage to breakdown versus physical film thickness for several different alternate high- κ dielectrics and ultra-thin SiO₂ gates. The capacitors were exposed to 342-MeV gold ions. After [78].

The critical voltage to hard breakdown scales with the square root of the physical thickness of the insulator. The data of Fig. 4 show the breakdown data for thin oxides can be fit by a power threshold model [79] as opposed to an energy dissipation model as has been applied to high voltage devices with thick oxides [80,81]. Also shown in the figure (dashed line) is the V_{DD} scaling trend suggested by the SIA National Technology Roadmap [82]. Although there is considerable variation in the voltage to hard breakdown in the devices of Fig. 4, all of the breakdown voltages are above the power supply voltages that will be seen in future highly scaled commercial technologies. Therefore, it does not appear that RHB will be a significant problem for future highly scaled commercial technologies which incorporate alternative gate dielectrics.

Radiation-induced soft breakdown

It is possible for energetic ions to degrade a device without causing permanent damage such as SEGR. Two examples of this are radiation-induced leakage current (RILC) [83–85] and radiation-induced soft breakdown (RSB) [78, 86–88]. Both RILC and RSB are characterized by increased oxide leakage current after ion exposure. RILC is the result of radiation-induced trap-assisted tunneling current, similar to SILC observed after constant voltage stress [83, 84]. Massengill *et*

al. [78] and Ceschia *et al.* [89] showed that RSB in high- κ and SiO₂ gate oxides results as the ions create random conductive paths in the oxide proportionally with ion fluence. In contrast to RHB, there does not appear to be a critical electric field for the onset of RSB [78,89], but rather a critical threshold ion LET [77,78,89]. Choi *et al.* [90] showed that oxide damage leading to RSB is a function of dielectric film thickness, ion LET, and total fluence. RSB can increase the gate current by $\sim 1 \mu\text{A}$, which increases the power consumption in the device by $\sim 1 \mu\text{W}$ [87]. Thus, RSB is most significant in low power applications like space electronics. However, it has also been shown recently that the combination of ion irradiation and electrical stress can affect the long term reliability of devices with ultra-thin gate oxides [87,90–92]. Suehle *et al.* [92] showed that capacitors irradiated with ¹²⁹Xe ions to a fluence of 10^7 ions/cm² had a time to failure in constant voltage time dependent dielectric breakdown (TDDB) tests that was reduced by approximately three orders of magnitude relative to unirradiated devices. Similar premature failures during TDDB testing have also been observed in devices irradiated with Au, Br, I, and Si ions [91]. Therefore, although ion exposure may not always cause a catastrophic failure like RHB, it can significantly reduce the operational lifetime of a device. This is a concern for space electronics, which are generally designed to have ~ 10 year lifetimes. Moreover, since devices with alternative gate dielectrics often have shorter operational lifetimes (based on low Weibull slope TDDB results) than ultra-thin SiO₂ for a given operating voltage [22,93–95], RSB and latent ion damage could pose a serious problem for qualifying devices with alternative gate dielectrics for use in space.

Nitrided Oxides

One alternative dielectric that has been previously explored (by others) in some detail is reoxidized nitrided oxides (RNO) [96–101]. In general, nitrided oxides have a lower pin-hole density than SiO₂, can be grown at high temperatures, permitting better uniformity and less compressive stress and fixed charge, and can slow the diffusion of dopants through the insulator, which can affect the channel resistivity [97]. Furthermore, RNO oxides have been shown to be superior to thermal oxides in hot-carrier degradation [102]. Thus, nitrided and RNO dielectrics are attractive for ultra-thin gate oxides for commercial and radiation hardened devices [97]. However, because the dielectric constant of these materials is very similar to SiO₂, nitrided oxides are only a viable alternative dielectric for near-term replacement (1-2 generations) of SiO₂.

The primary difference between thermal SiO₂ and RNO dielectrics in ionizing radiation environments is the nearly total lack of interface-trap buildup for RNO dielectrics [103]. RNO dielectrics can be fabricated such that there is no measurable interface-trap buildup for transistors irradiated



Figure 5: The change in midgap voltage measured on 37 nm RNO and thermal oxide transistors versus dose. The midgap voltage shift corresponds to the threshold-voltage shift due to oxide-trapped charge. After [103].

to total doses in excess of 50 Mrad(Si) [103]. This makes RNO gates attractive for space applications. For those cases where some interface-trap buildup was observed, the number of interface traps does not increase in time after irradiation [104]. This likely occurs because hydrogen released in the bulk of the dielectric or near the interface (which is responsible for interface-trap buildup in thermal oxides), cannot penetrate the nitrogen rich oxynitride layer near the interface and create interface traps [104].

RNO dielectrics can be fabricated so that the amount of oxide trapped charge buildup is less than or comparable to that of a thermal oxide. Figure 5 is a plot of the threshold-voltage shift at midgap for p-channel transistors fabricated with a hardened oxide and with a RNO oxide versus dose [103]. The oxide and RNO dielectric thicknesses were 37 nm and the pre-irradiation fixed charge levels were $\sim 3 \times 10^{10}$ and 10^{11} cm², respectively. At midgap, interface-trap charge is neutral, thus the threshold-voltage shift at midgap corresponds to the threshold-voltage shift due to oxide-trap charge. The bias during irradiation for the hardened thermal oxide was +5 V and the bias for the RNO oxides was either +5 or -5 V. After irradiation to 10 Mrad(SiO₂), the amount of oxide-trap charge buildup in the hardened thermal oxides is more than twice that for the RNO oxides. Note that for the RNO oxide transistors, the shifts are nearly equal for biases of +5 and

-5 V. Based on the results of Fig. 5, the radiation hardness of ultra-thin RNO dielectrics should be extremely good.

CHAPTER III

ALUMINUM OXIDE DIELECTRICS

Aluminum oxide is a candidate for short-term replacement (2-3 generations) of SiO_2 because of its larger dielectric constant and its compatibility with high temperature CMOS processing [15]. The aluminum oxide capacitors studied here were 0.0011 cm^2 Al gate devices fabricated at IBM's Thomas J. Watson Research Center on n-type Si(100) wafers with a doping concentration of $\sim 10^{16} \text{ cm}^{-3}$. The gate dielectric stack consisted of an Al_2O_3 layer on an interfacial oxynitride. Sixteen different process splits (~ 500 devices per wafer) were fabricated within one wafer lot with 4 variations in Al_2O_3 thickness, 2 SiO_xN_y thicknesses, and 2 different annealing conditions. The physical thickness of the Al_2O_3 was 10 nm, 7.5 nm, 5.0 nm, or 2.5 nm, while the physical thickness of the oxynitride was either 2.5 nm or 1.1 nm as measured ellipsometrically. The interfacial oxynitrides were thermally grown on HF-last Si(100), resulting in $\sim 10\%$ - 15% N incorporation. The Al_2O_3 layers were deposited by atomic layer deposition (ALD) at 300°C using standard $\text{Al}(\text{CH}_3) + \text{H}_2\text{O}$ surface chemistries [15–17]. After deposition, the dielectrics were subjected to either a forming gas (5-10% H_2 in N_2) anneal (FGA) at 550°C or an O_2 anneal and a FGA at 550°C . The accumulation capacitance of the O_2 annealed devices was consistently $\sim 5\%$ to 10% smaller than the devices that received a FGA only, suggesting they had an oxygen rich oxynitride, or a small amount of SiO_2 at the interface [16,105]. After annealing, the Al gate electrodes were evaporated at room temperature. The relative dielectric constant of as-deposited Al_2O_3 is ~ 8 and the relative dielectric constant of silicon oxynitride is ~ 4 - 5 for this concentration of N. The equivalent oxide thicknesses (EOTs) of the dielectrics studied here are 7.4 nm, 6.2 nm, 5.1 nm, and 3.4 nm for the devices with the 2.5 nm oxynitride and 6.3 nm, 5.2 nm, 4.0 nm, and 2.6 nm for the devices with the 1.1 nm oxynitride.

Prior to irradiation the capacitance-voltage (CV) and breakdown characteristics of several (~ 40) capacitors from each sample were measured using equipment at Sandia National Laboratories. These wafer level measurements were made using an Electroglass automated prober and a HP 4062 characterization system controlled by HP's ICMS wafer test control utility. Fig. 6 is a plot of representative (a) CV curves and (b) breakdown characteristics for ~ 20 of these devices. Fig. 6a shows that these capacitors have well behaved CV characteristics with a flatband voltage (V_{fb}) of $\sim 0 \text{ V}$ and very little part-to-part variation. The devices that received only a FGA showed

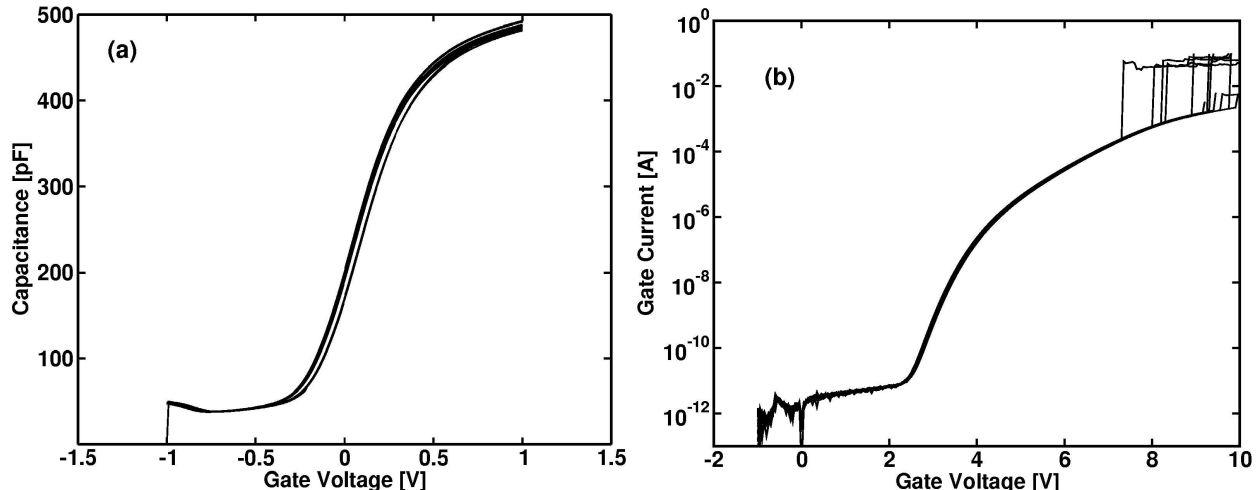


Figure 6: Pre-irradiation (a) CV and (b) breakdown characteristics for 0.011 cm^2 devices with $10 \text{ nm Al}_2\text{O}_3$ on $2.5 \text{ nm SiO}_x\text{N}_y$ which received a FGA after Al_2O_3 ALD. The corresponding EOT of these samples is $\sim 7.4 \text{ nm}$.

no measurable hysteresis, whereas most of the devices which received an O_2 anneal and FGA showed $\sim 20\text{-}30 \text{ mV}$ of hysteresis (not shown here). The bias dependence of the hysteresis suggests that it is related to electron movement into and out of border traps in the near interfacial region of the oxide [106]. However, due to the thin oxynitride layers present in these devices, the possibility of an additional contribution from traps at the $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ interface cannot be ruled out. Fig. 6b shows that these devices have low gate leakage currents ($\sim 1 \text{ pA}$ or 10^{-8} A/cm^2) for gate voltages less than $\sim 3 \text{ V}$. Similar $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ gate dielectrics exhibit a factor of ~ 100 reduction in leakage current compared to electrically equivalent SiO_2 [16]. Overall, the breakdown field E_{bd} did not depend significantly on processing conditions or Al_2O_3 thickness. However, my results showed that the interfacial oxynitride plays an important role in the breakdown of the dielectric stacks for these devices. The samples with the 2.5 nm interfacial layer had an average breakdown of $\sim 6 \text{ MV/cm}$ with a standard deviation of ~ 0.5 , whereas the devices with the 1.1 nm oxynitride broke down at an electric field of $\sim 4.7 \text{ MV/cm} \pm 0.6$. This result is in good agreement with initial data in the literature that suggests high- κ dielectric breakdown is determined by the interfacial layer [93,107]. In comparing the electric fields in each of the layers at breakdown, it was found that the fields in the oxynitrides were $\sim 8\text{-}9 \text{ MV/cm}$ whereas the fields in the Al_2O_3 were $\sim 4\text{-}5 \text{ MV/cm}$. Therefore, the breakdown strength in these $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ dielectric stacks is really limited by the SiO_xN_y . When the oxynitride breaks down, all of the gate potential is suddenly dropped across the Al_2O_3 , and since it cannot maintain as large an electric field, it too breaks down.

Charge pumping is more precise than CV or subthreshold current-voltage (IV) stretchout

analysis for measuring interface trap densities [108]. Thus, high- κ transistors with similar gate dielectric stacks were also examined as part of this work. These devices were $100\ \mu\text{m} \times 100\ \mu\text{m}$ nMOSFETs with n^+ poly-Si gates fabricated on p-type Si(100) wafers with a doping concentration of $\sim 3 \times 10^{17}\ \text{cm}^{-3}$. The Al_2O_3 and SiO_xN_y layers were deposited in the same manner as the capacitors discussed above. The physical thickness of the Al_2O_3 was 20 nm, and the interfacial oxynitride was ~ 0.7 nm, corresponding to an EOT of ~ 8.0 nm. These transistors received different post deposition thermal cycles than the capacitors, including a $1000\ ^\circ\text{C}$ dopant activation anneal in Ar for ~ 5 seconds, a standard FGA at $550\ ^\circ\text{C}$, and a second FGA anneal at $400\ ^\circ\text{C}$ after deposition of the metal interconnects [16,24]. It is known that variations in post deposition anneal conditions can significantly impact the radiation response of SiO_2 [109]. As discussed in detail below, similar effects of processing are also observed for the radiation response of the nMOSFETs relative to the capacitors.

Capacitor Radiation Results

The capacitors were irradiated incrementally to a total dose of 10 Mrad(SiO_2) with 10-keV X-rays at a dose rate of 1667 rad(SiO_2)/s. Several types of radiation experiments were performed to determine the effects of radiation bias, dielectric film thickness, and processing conditions. The effects of the radiation were characterized using standard 1-MHz high frequency *CV* analysis [63], and the results of these experiments are discussed in detail below.

Bias dependence

The effects of bias during irradiation of high- κ devices are not well understood. However, prior work has shown that radiation-induced midgap voltage shifts (ΔV_{mg}) have a weak dependence on radiation bias for some alternative dielectric materials [42, 43]. Therefore, these $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ capacitors were irradiated using several electric fields between -1.0 and 2.0 MV/cm. For fields larger than ~ 2.3 MV/cm, these gate dielectrics begin to conduct enough current that any radiation results reported in this range could be skewed, resulting from trapped positive charge neutralization due to the injected charge. Fig. 7 is a plot of the absolute value of ΔV_{mg} after a total dose of 2.0 Mrad(SiO_2) as a function of oxide electric field during irradiation. The bias dependence in these devices is similar to that observed in standard thermal oxides [38], although somewhat different than the bias dependence for hafnium silicate gate dielectrics as discussed in the next chapter. In Fig. 7, the magnitude of the radiation induced voltage shift increases monotonically from ~ 0.1 V

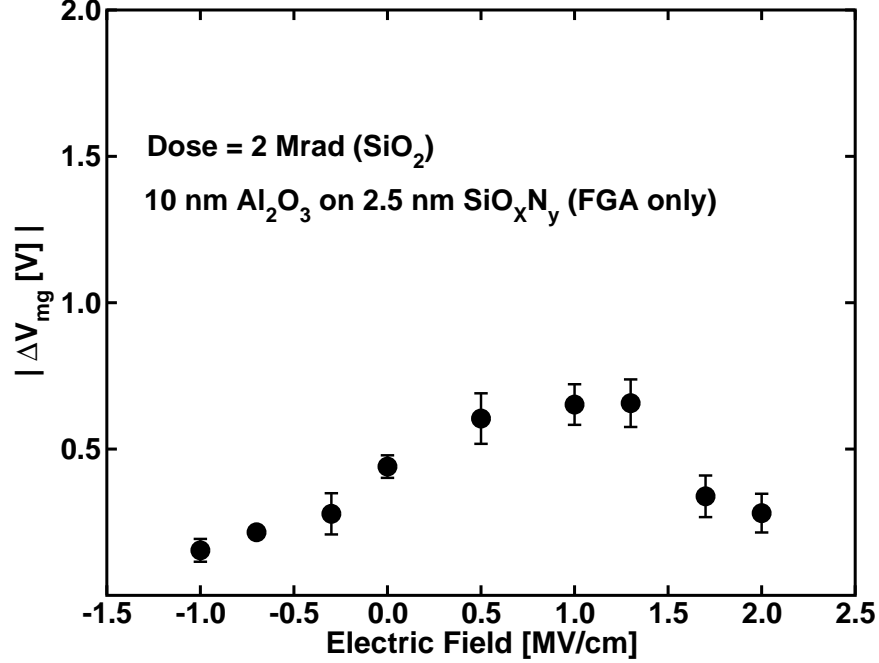


Figure 7: Absolute value of ΔV_{mg} versus electric field for $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ capacitors irradiated to 2 Mrad(SiO_2). These devices were processed with a FGA only after Al_2O_3 ALD. The data points represent the average of at least four devices and the error bars represent the standard deviation.

at -1.0 MV/cm to ~ 0.75 V for fields of 1.0-1.3 MV/cm. The observed drop-off at larger fields is consistent with an approximate $E^{-0.5}$ dependence and is likely related to a decrease in effective capture cross section with increasing field as has been observed in SiO_2 [38, 110, 111]. In some thermal oxides, negative bias exposures lead to larger voltage shifts than irradiations at 0 MV/cm due to an increase in charge yield. However, in making these types of comparisons, it is necessary to consider the effects of both charge yield and location of the charge centroid. For increasing negative fields, there is an increase in charge yield corresponding to a decrease in the initial recombination of radiation-induced electron-hole pairs, which will tend to increase the amount of radiation induced voltage shift [38, 112]. However, larger negative fields tend to move the charge centroid toward the gate, which reduces the measured ΔV_{mg} [113]. Thus, charge yield and centroid motion are competing mechanisms for negative bias exposures. Since the data of Fig. 7 show the magnitude of ΔV_{mg} decreases for decreasing field, the location of the centroid appears to be the dominant factor determining the irradiation bias dependence in these devices.

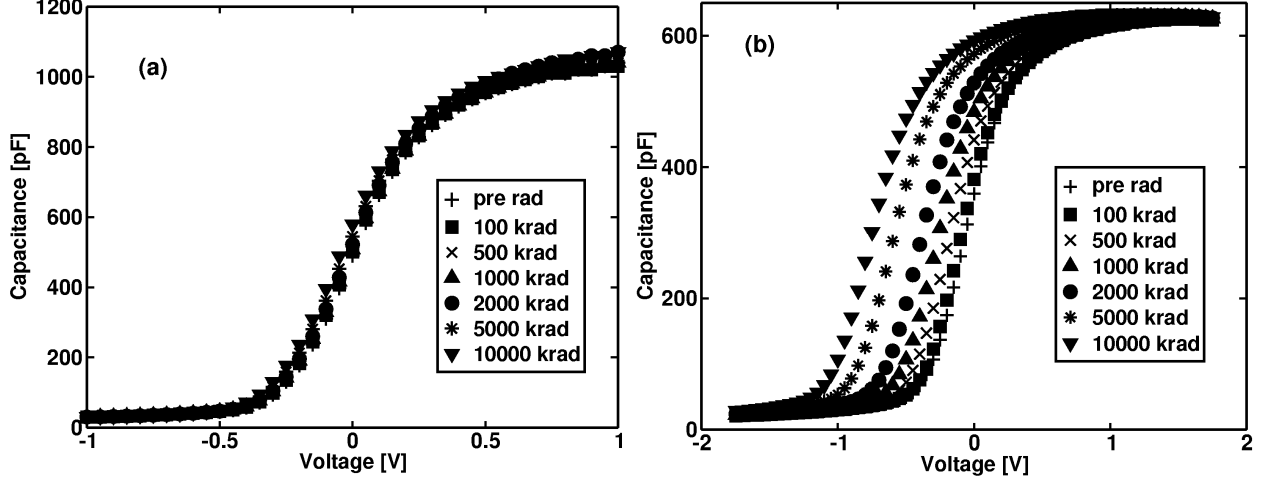


Figure 8: Pre and post irradiation 1 MHz CV measurements on 0.0011 cm^{-2} capacitors that received a FGA after Al_2O_3 deposition, with an EOT of (a) 3.4 nm and (b) 6.2 nm, irradiated to total doses from 100 up to 10,000 krad(SiO_2) at an electric field of +1.0 MV/cm.

Al_2O_3 and SiO_xN_y thickness dependence

The amount of midgap voltage shift in these devices depends strongly on gate dielectric film thickness. Fig. 8 shows representative 1 MHz CV data for devices with (a) a 2.5 nm Al_2O_3 and (b) a 7.5 nm Al_2O_3 layer on a 2.5 nm interfacial oxynitride, which received only a FGA, for incremental doses up to 10 Mrad(SiO_2) at an electric field of 1.0 MV/cm. After 10 Mrad(SiO_2), the device in Fig. 8a has a midgap voltage shift (ΔV_{mg}) of -52 mV, and the device in Fig. 8b shows a ΔV_{mg} of -735 mV. Using these values for ΔV_{mg} , net oxide trap charge densities can be estimated by [114]

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \quad (1)$$

where ΔN_{ot} is the radiation induced net oxide trap charge density projected to the interface, C_{ox} is the oxide capacitance measured in accumulation, $-q$ is the electronic charge, and A is the area. Using equation 1 the net oxide-trapped charge densities projected to the interface (ΔN_{ot}) are estimated to be $2.98 \times 10^{11} \text{ cm}^{-2}$ and $2.65 \times 10^{12} \text{ cm}^{-2}$, respectively. Similarly, the flatband voltage shifts (ΔV_{fb}) for these devices at the same total dose are -50 mV and -720 mV. The interface-trap charge densities (ΔN_{it}) can be estimated from midgap-to-flatband stretchout of 1 MHz CV curves by [63]

$$\Delta N_{it} = \frac{C_{ox}(\Delta V_{fb} - \Delta V_{mg})}{qA}. \quad (2)$$

Therefore, the irradiation has no measurable effect on the interface trap density (as estimated from the midgap to flatband stretch-out) to within the accuracy of the measurement. This result is consistent with radiation results for hafnium oxide and hafnium silicate dielectric materials [41,42].

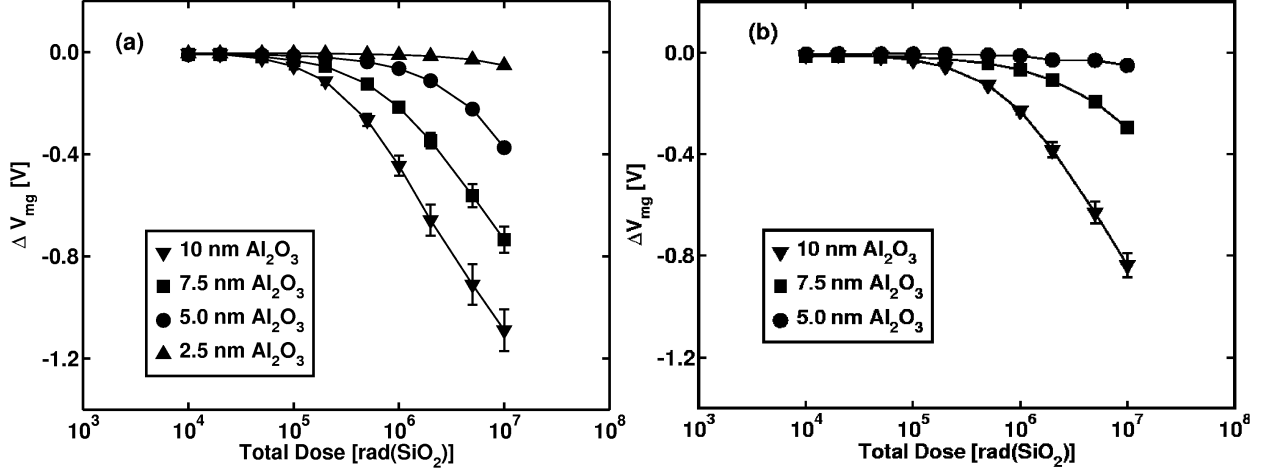


Figure 9: A complete summary of midgap voltage shifts as a function of total dose for exposures from 10 krad(SiO₂) to 10,000 krad(SiO₂) for devices with (a) a 2.5 nm and (b) a 1.1 nm interfacial oxynitride.

A more precise analysis of the interface trapping properties of similar Al₂O₃/SiO_xN_y gate dielectric stacks using *CP* analysis on nMOSFETs is discussed below.

Fig. 9 is a plot of ΔV_{mg} versus dose for 1.0 MV/cm biased exposures from 10 krad(SiO₂) to 10 Mrad(SiO₂) for devices with (a) a 2.5 nm oxynitride and (b) a 1.1 nm oxynitride that received only a FGA after Al₂O₃ deposition. For total doses up to 50 krad(SiO₂), none of the samples trap a significant amount of charge. After additional exposure, there is a clear difference in the amount of trapped charge for each Al₂O₃ film thickness at a given dose. By comparison of Figs. 9a and 9b, a significant reduction in the amount of radiation damage is observed for a given Al₂O₃ film thickness for the devices with a 1.1 nm oxynitride layer relative to devices with 2.5 nm SiO_xN_y. These shifts are larger than would be observed in high-quality thermal SiO₂ of equivalent electrical thickness [46, 115–117]. However, it is evident that total-dose degradation will not be a major concern for Al₂O₃/SiO_xN_y gate stacks of most interest to modern CMOS manufacturing processes (< 4 nm EOT), as there is only ~ 50 mV shift after a total dose of 10 Mrad(SiO₂).

It is interesting to consider why there is such a large difference in the amount of radiation induced trapped charge for a given Al₂O₃ thickness for the two separate interfacial layers. One would expect to see less trapping in the films with the thinner oxynitride since there is less volume in these films within which to generate electron-hole pairs (EHPs). However, for a given Al₂O₃ thickness, the difference in ΔV_{mg} between Fig. 9a and 9b is more than that expected based on a volume argument alone. Thus it is necessary to consider additional mechanisms to understand

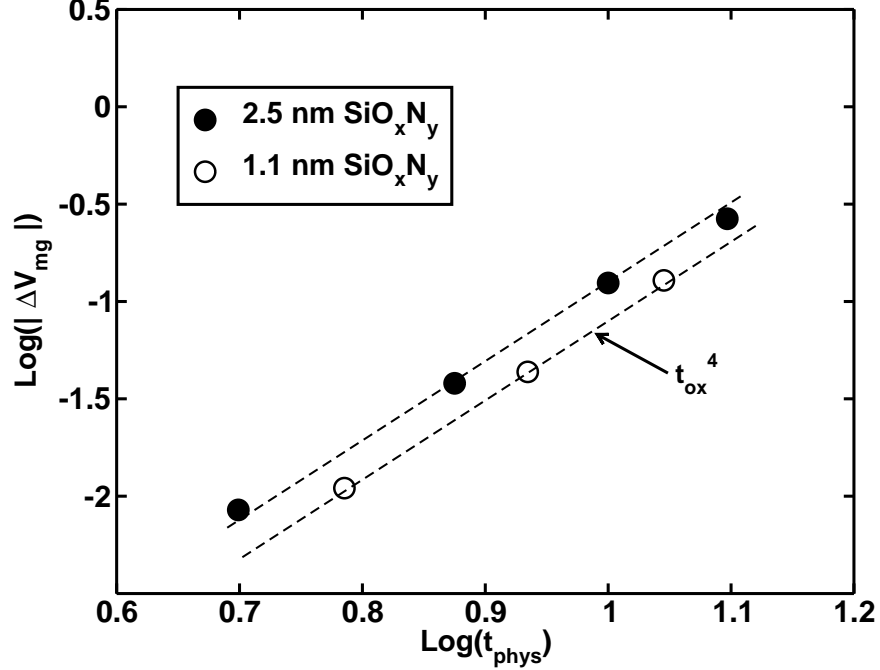


Figure 10: Logarithm of the absolute value of ΔV_{mg} data from Fig. 9a (filled symbols) and Fig. 9b (open symbols) versus the logarithm of the physical thickness of the films. These 500 krad(SiO_2) data are well correlated to a linear regression model (dashed lines) that shows a t_{ox}^4 thickness dependence.

these data completely. Since these devices were processed in the same manner, they should exhibit similar trapping properties. Fig. 10 is a plot of the logarithm of the absolute value of the ΔV_{mg} data from Fig. 9a and Fig. 9b as a function of the logarithm of the total physical thickness ($t\text{-Al}_2\text{O}_3 + t\text{-SiO}_x\text{N}_y$) for a total dose of 500 krad(SiO_2). A linear regression model of the data (dashed lines)

indicates there is a good correlation between the measured voltage shifts and the total film thickness; the ΔV_{mg} in these devices is proportional to $\sim t_{ox}^4$. For SiO_2 films thinner than ~ 20 nm, there is a similar deviation from the $\Delta V \propto t_{ox}^2$ relationship that is expected and typically observed for thick oxides that are otherwise processed similarly [46,115–117]. The physical reason one expects to see a t_{ox}^2 dependence is to account for charge generation throughout the entire volume of the oxide, and to account for the moment arm effect resulting from the spatial distribution of the charges in the oxide projected to the interface [113]. Deviation from a t_{ox}^2 thickness dependence is the result of charge removal via tunneling from a thin layer near the interface and the gate electrode [46,117,118]. This reduces the effective thickness of the dielectric by the region over which the charge is removed. For thick films (> 20 nm), this is relatively insignificant, but it becomes an important consideration for films like those being discussed here. Saks, et al. successfully used a similar model to fit data on

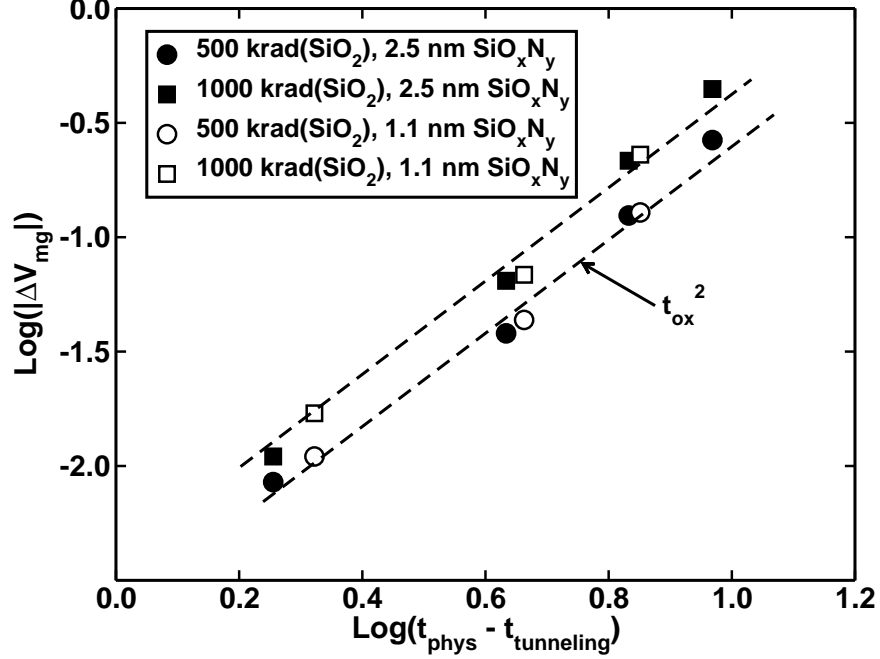


Figure 11: The data of Fig. 10, as well as 1000 krad(SiO_2) data, plotted with the effects of tunneling taken into account. The data for both the 2.5 nm (solid symbols) and 1.1 nm (open symbols) are well correlated to a linear regression model (dashed lines) showing a t_{ox}^2 thickness dependence.

ultra-thin SiO_2 capacitors [46]. For these $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ devices, $\Delta V_{mg} \propto t_{\text{ox}}^2$ if the devices with the 2.5 nm oxynitride are thinned by ~ 3 nm due to tunneling, and the devices with the 1.1 nm oxynitride are thinned by ~ 4 nm due to tunneling. This result is consistent with an increased electron tunneling probability for the thinner SiO_xN_y films. Fig. 11 is a plot of the data in Fig. 10, as well as data for exposures to 1000 krad(SiO_2), with the effects of tunneling taken into account. In Fig. 11, the data for both the 2.5 nm oxynitride and 1.1 nm oxynitride devices fall on the same curve, and show a $\sim t_{\text{ox}}^2$ dependence. Hence, most of the measurable trapping in these devices occurs in the Al_2O_3 since the charge trapped in the oxynitride is removed due to tunneling. As expected, more trapping is observed for thicker Al_2O_3 films due to their larger volumes. However, for a given Al_2O_3 thickness, the devices with a 1.1 nm oxynitride show less trapping than a 2.5 nm oxynitride due to a greater tunneling probability for the thinner interfacial layer.

Consistent with the above interpretation, consider Fig. 12 in which ΔV_{mg} is plotted versus dose for the 10 nm Al_2O_3 devices of Fig. 9a and Fig. 9b, as well as data for devices from these same splits irradiated at -1.0 MV/cm. Under negative bias there should not be any significant electron tunneling effects since the Si surface is in inversion. Therefore, since the Al_2O_3 thickness is the

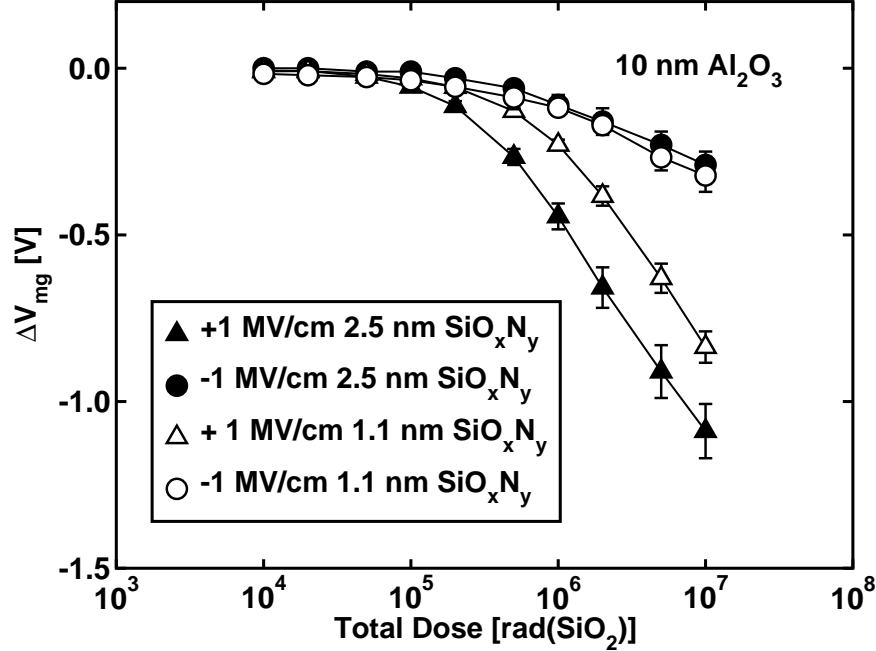


Figure 12: Midgap voltage shift versus total dose for 10 nm Al_2O_3 devices with 2.5 and 1.1 nm interfacial oxynitrides irradiated at +1.0 MV/cm (triangles) and -1.0 MV/cm (circles).

same, the radiation responses of the 1.1 nm SiO_xN_y and the 2.5 nm SiO_xN_y samples should match more closely than for positive bias exposures. As shown in Fig. 12, for negative bias exposures there is a nearly identical radiation response for devices with the same Al_2O_3 thickness, independent of the interfacial oxynitride.

Effects of processing

Fig. 13 is a plot of ΔV_{mg} versus total dose for devices with 10 nm, 7.5 nm, and 5.0 nm Al_2O_3 layers deposited on a 1.1 nm interfacial oxynitride for devices that received either a FGA or an O_2 anneal and FGA. The data of Fig. 13 show the devices which received the additional O_2 anneal also have a significantly improved radiation response as seen previously for thermal oxides in [119]. For doses greater than ~ 1 Mrad(SiO_2) the 10 nm and 7.5 nm O_2 annealed devices have $\sim 50\%$ less voltage shift than the devices which received a FGA only. The 5.0 nm devices show almost no shift with dose up to 10 Mrad(SiO_2), and there is no measurable difference between the FGA and O_2 +FGA processed devices. Therefore, the significant processing dependence shown in Fig. 13 essentially vanishes for film thicknesses of most relevance to commercial use. The large differences seen in the 10 nm and 7.5 nm devices suggests that the O_2 anneal either decreases the density of hole trap precursors or increases the density of electron trap precursors in the near SiO_xN_y interfacial

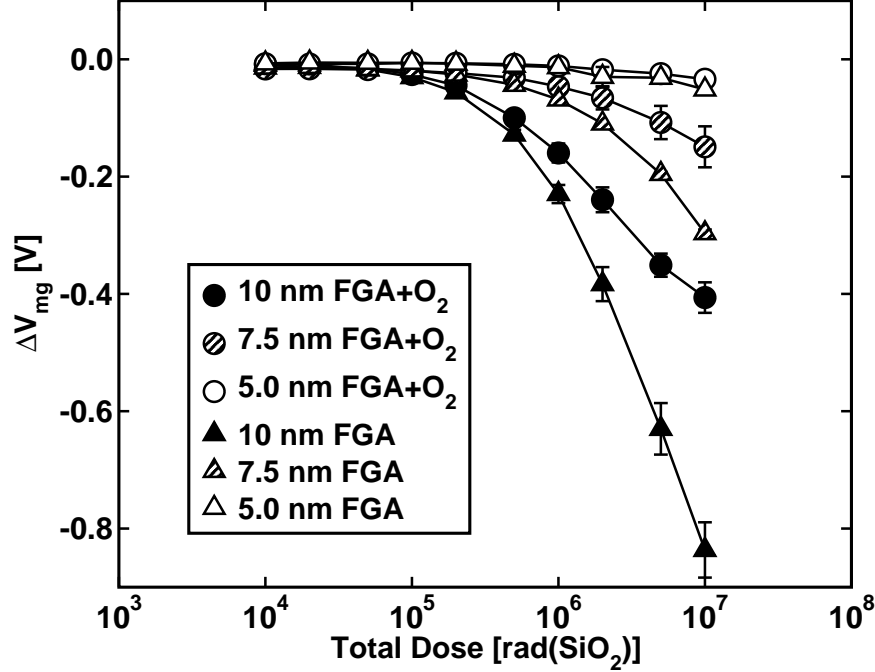


Figure 13: Midgap voltage shift versus dose for 6.3 nm (solid symbols), 5.2 nm (striped symbols), and 4.0 nm (open symbols) EOT devices annealed with either a FGA or an O₂ anneal and a FGA after Al₂O₃ ALD.

region of the Al₂O₃ or at the Al₂O₃/SiO_xN_y interface. It has been shown that the electron trap

density in SiO₂ can be significant (on the same order as hole traps) and is dependent on device processing [120]. Electron traps are classified as either “deep” or “shallow” depending on their energy distribution. Deep electron traps are very stable, and will compensate some of the trapped holes, thereby reducing the net oxide-trapped charge density measured using the midgap *CV* shift method [120]. Shallow trapped electrons can move easily in and out of the gate dielectric, producing effects such as *CV* hysteresis [120]. Recall that for these capacitors, only the O₂ annealed devices showed a measurable hysteresis. Thus, these data may be evidence of significant electron trapping in the Al₂O₃/SiO_xN_y dielectric stacks that received the O₂ anneal. This result is consistent with early work on Al₂O₃ gate dielectrics, which showed those aluminum oxides had a significant density of electron traps [118]. Previous work often found that Al₂O₃ exhibited good total-dose radiation hardness because it trapped a significant amount of electrons, which compensated the trapped holes [118, 121, 122]. Furthermore, it was shown that Al₂O₃ contains several trap levels in the band gap, making it easy for electrons to tunnel between the dielectric and the substrate [123, 124]. Therefore, although the apparent reduction in ΔV_{mg} observed in Fig. 13 for the O₂ annealed devices

may be the result of less hole trapping, the possibility of compensation via trapped electrons cannot be ruled out.

Transistor Radiation Response

Polysilicon gated transistors with similarly processed $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ dielectrics were characterized using a combination of low frequency $1/f$ noise, subthreshold IV and variable base CP measurements. All measurements were done using devices from a single wafer. Some devices were packaged to facilitate the $1/f$ noise measurements [125], while the radiation, IV and CP data were taken using wafer level measurements. The irradiations were performed at a dose rate of $1000 \text{ rad}(\text{SiO}_2)/\text{s}$ using a 10 keV X-ray source. These devices, with gate stacks consisting of 20 nm Al_2O_3 on 0.7 nm SiO_xN_y were irradiated incrementally to a total dose of 1 Mrad(SiO_2). During irradiation, the gate was biased at +1.0 MV/cm or -1.0 MV/cm with all other terminals grounded. Prior to irradiation, and after each incremental dose, the IV and CP characteristics were measured *in situ*. The IV measurements were performed by sweeping the gate from -2 V to +5 V with 150 mV on the drain. During the CP measurements, the gate was pulsed using a 4.5 V square wave with a 10 ns rise and fall time at a frequency of 500 kHz, while the source and drain were reverse biased at 500 mV. The $1/f$ noise of the packaged devices was measured as a function of both drain voltage (V_{ds}) and gate voltage (V_{gs}). It is known that $1/f$ noise measurements are a sensitive test for probing the effects of near interfacial oxide defects (i.e., border traps) on channel carriers. Indeed, $1/f$ noise in MOS devices is the result of number and/or mobility fluctuations of channel carriers resulting from interactions with border traps [68,106,126]. Thus, the combination of $1/f$ noise measurements with IV and CP analysis offer a complementary toolset for examining the interface properties of these nMOSFETs before and after exposure to ionizing radiation.

Fig. 14 is a plot of the excess-voltage noise power spectral density S_{Vd} as a function of frequency for (a) several drain voltages at a constant V_{gs} of 5 V and for (b) varying V_{gs} with a constant V_{ds} of 100 mV [125]. These data show that the $1/f$ noise in these devices increases with increasing drain voltage and decreases with increasing V_{gs} . In Fig. 15, the data of Fig. 14 are combined and plotted as S_{Vd} versus $V_{ds}^2/(V_{gs}-V_{th})^2$, which are the expected drain and gate voltage dependences for noise due primarily to number fluctuations. Arranging the data in this way makes it possible to extract the density of border traps D_{bt} by [106]

$$D_{bt} = \left(\frac{A}{qkT} \right) \ln \left(\frac{\tau_1}{\tau_2} \right) \left(\frac{\epsilon_{ox}}{t_{ox}} \right)^2 K \quad (3)$$

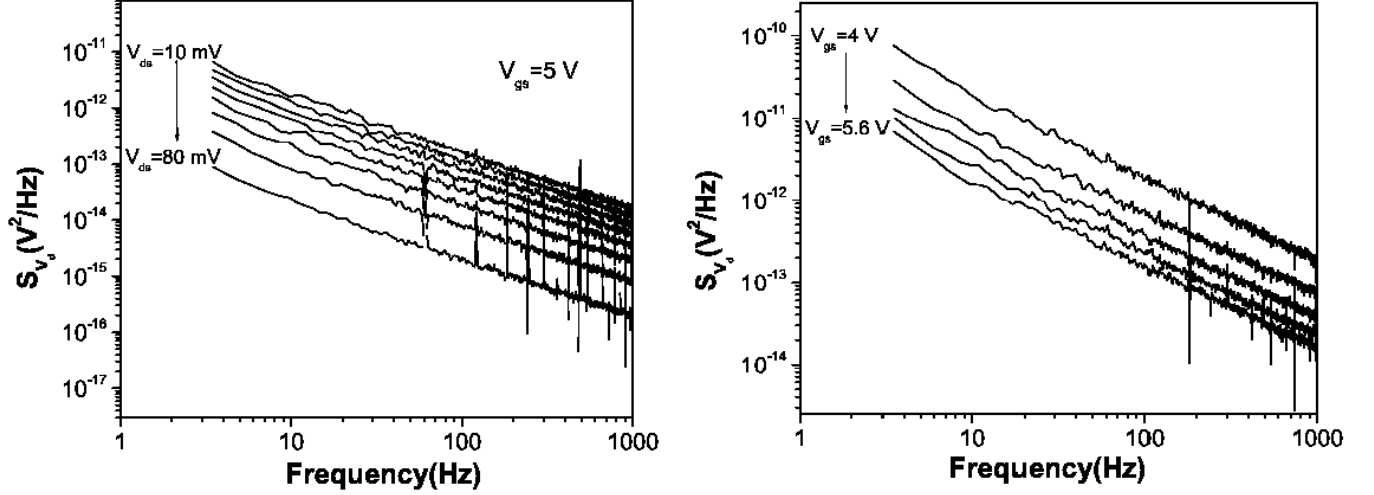


Figure 14: Pre-irradiation noise power spectral density for a $2 \mu\text{m} \times 20 \mu\text{m}$ transistor for (a) several values of V_{ds} at a constant V_{gs} of 5 V as well as for (b) several values of V_{gs} for a constant V_{ds} of 100 mV. The spikes are the result of 60-Hz pickup and are ignored in the fitting and analysis of the data.

where A is the gate area of the transistor, q is the magnitude of the electronic charge, k is the Boltzmann constant, T is the absolute temperature, t_{ox} is the (equivalent SiO_2) oxide thickness, ϵ_{ox} is the dielectric constant of SiO_2 , τ_1 and τ_2 are “cutoff” times associated with the tunneling and thermally activated processes that lead to the observed noise [127, 128], and K is the normalized $1/f$ noise magnitude as found from the slope of a fit to the data in Fig. 15. For these devices, K

$\sim 3 \times 10^{-9} \text{ V}^2$ and the pre-irradiation D_{bt} from equation 15 is found to be $\sim 2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. This number is larger than is commonly seen in SiO_2 [106], but may not be too surprising as it likely includes contributions from defects both in the near interfacial layer of the Al_2O_3 and at the $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ interface, which is $\sim 0.7 \text{ nm}$ away from the $\text{SiO}_x\text{N}_y/\text{Si}$ interface.

Fig. 16 shows the sub-threshold IV characteristics ($S \sim 150 \text{ mV/dec}$) of these transistors for incremental irradiations up to 1 Mrad(SiO_2) at a gate bias of 1.0 MV/cm. The shifts seen in Fig. 16 are due to the net positive charge buildup in the gate insulator with dose [63]. As a guide to the eye, a set of parallel lines has been added to the pre-irradiation and 1 Mrad(SiO_2) curves to show that, just like for the CV curves of the capacitors, there is no measurable stretchout due to interface traps in these devices. Fig. 17 is a summary of ΔV_{th} for irradiations at $\pm 1.0 \text{ MV/cm}$. After a total dose of 1 Mrad(SiO_2), $\Delta V_{th} \sim -1.3 \text{ V}$ corresponding to $\Delta N_{ot} \sim 2.1 \times 10^{12} \text{ cm}^{-2}$ with no significant dependence on the bias polarity during irradiation. This result differs from the bias

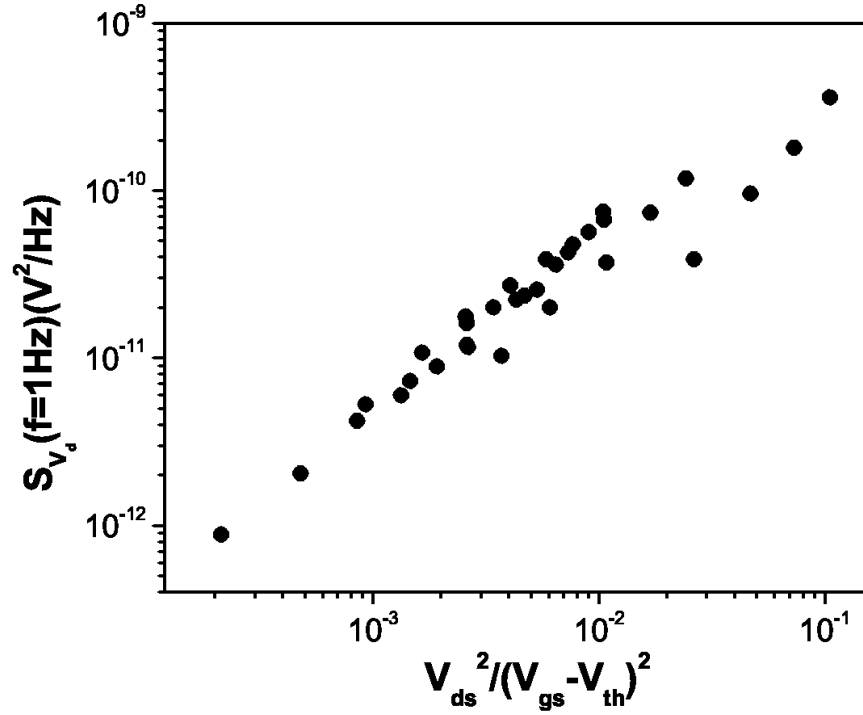


Figure 15: Log-log plot of the noise power spectral density versus $V_{ds}^2/(V_{gs}-V_{th})^2$ for the data of Fig. 14

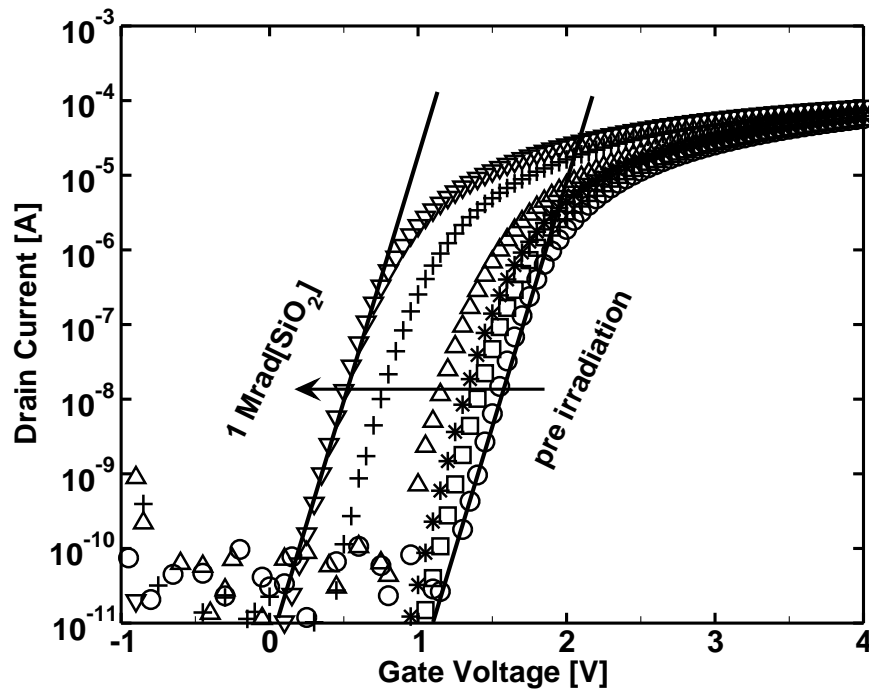


Figure 16: Subthreshold IV data for a $100 \mu\text{m} \times 100 \mu\text{m}$ $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ transistor irradiated at $+1 \text{ MV/cm}$ from $10 \text{ krad}(\text{SiO}_2)$ to $1 \text{ Mrad}(\text{SiO}_2)$. The transistors examined here received a $1000 \text{ }^\circ\text{C}$ dopant activation anneal and two FGAs.

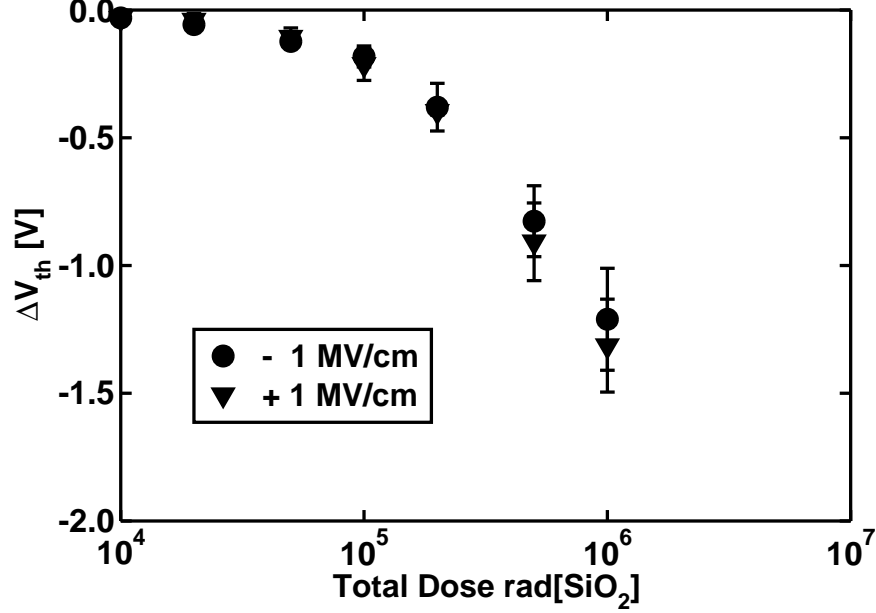


Figure 17: Summary of ΔV_{th} for $100 \mu\text{m} \times 100 \mu\text{m}$ nMOSFETs after irradiation with 10-keV X-rays for both positive and negative bias conditions.

dependence observed for the capacitors in Fig. 7. However, since the dielectrics in these FETs were annealed at much higher temperatures than the capacitors, this is not an equal comparison. It has been shown that high temperature processing can significantly alter the trapping properties of thermal oxides [109,119]. Additionally, since Al_2O_3 begins to crystallize at $\sim 900 \text{ }^\circ\text{C}$ [16,17,105] it is likely that the dielectric in the transistors is poly-crystalline, and amorphous in the capacitors. Thus, considering the differences in film thickness and post deposition processing is not surprising that an increased voltage shift with dose and variation with radiation bias is observed for the Al_2O_3 transistors relative to the Al_2O_3 capacitors.

Fig. 18 is a plot of the CP characteristics of these devices. The pre-irradiation peak charge pumping current was $\sim 0.9\text{-}1.3 \mu\text{A}$, which corresponds to a D_{it} of $\sim 1.0\text{-}1.6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. A pre-irradiation D_{it} of 10^{12} is ~ 100 times larger than the D_{it} expected for thermal SiO_2 , but is in good agreement with interface trap densities reported in the literature for high- κ devices [13,14,47]. This interface trap density is also comparable to the border trap densities in these devices measured using $1/f$ noise. Fig. 19 is a summary of ΔD_{it} for irradiations with $+1.0$ or -1.0 MV/cm on the

gate. These data indicate there is a monotonic reduction in D_{it} for both bias conditions for doses up to $500 \text{ krad}(\text{SiO}_2)$. For additional exposure, there is not a significant reduction in D_{it} , perhaps

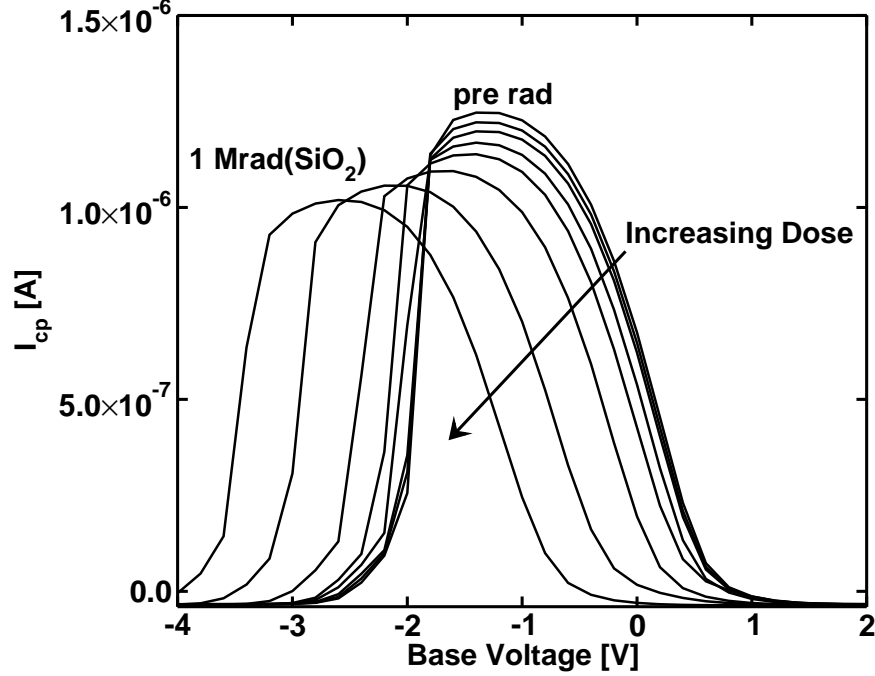


Figure 18: *CP* characteristics of a $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ transistor irradiated at $+1 \text{ MV/cm}$ from $10 \text{ krad}(\text{SiO}_2)$ to $1 \text{ Mrad}(\text{SiO}_2)$.

suggesting that this process is beginning to saturate. Overall, there is a $\sim 25\%$ reduction in D_{it} for exposures at $+1 \text{ MV/cm}$, and a $\sim 15\%$ reduction for exposures at -1 MV/cm . This result is somewhat surprising because D_{it} generally increases with dose in silicon-dioxide films. It should be noted that radiation-induced neutralization of oxide-trap charge has been observed in SiO_2 , but typically only under negative or zero bias irradiation conditions following an initially positive bias exposure [129,130]. Hence, these results differ significantly from prior experience on the radiation response of the Si/thermal SiO_2 system.

Based on the data in Figs. 17 and 19 it can be hypothesized that the surprising results of Fig. 19 are related to hydrogen passivation of some of the border traps and/or interfacial defects in these devices. To understand this, consider the following two points. (1) There are recent data in the literature which suggest that some alternative dielectric materials can reduce hydrogen diffusion to the interface, making standard FGAs less effective on high- κ devices than on devices with thermal oxides [131–133]. Furthermore, this effect is enhanced in large area devices where lateral hydrogen diffusion is essential for uniform passivation of the entire interface [132,133]. (2) These transistors were large area ($100 \mu\text{m} \times 100 \mu\text{m}$) devices, which contained a significant amount of hydrogen (due to the two FGAs), but still had a large density of interface traps and border traps as measured by

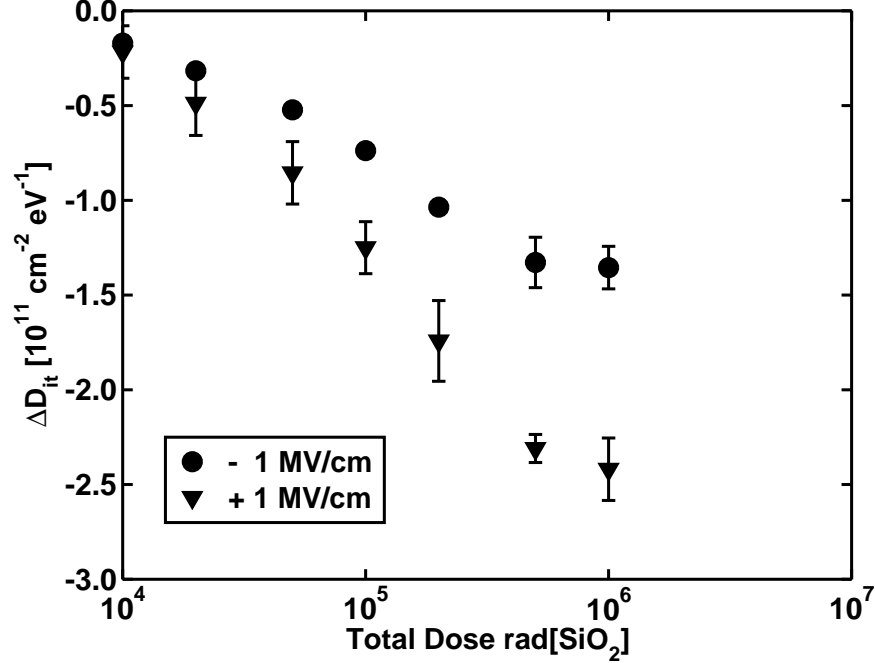


Figure 19: Interface trap density as a function of dose for both positive and negative bias irradiations.

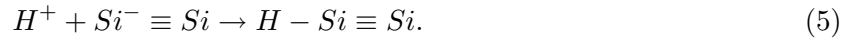
CP (Fig. 18) and $1/f$ noise. Thus, it is possible that some of the hydrogen in these films could be released during the irradiation and passivate defects at or near the interface [68, 134–136]. Defects passivated by hydrogen can no longer communicate with the Si or contribute to the *CP* current, thereby reducing the measured interface trap density. As shown in Fig. 17 positive and negative bias exposures generate the same amount of net-positive charge in these dielectrics, however H^+ drift to the interface is hindered under negative bias. Therefore, if this argument is correct, it is not surprising that a greater reduction in D_{it} is observed for positive electric fields. Furthermore, these devices had a relatively large $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ pre-irradiation density of interface traps and border traps [43]. Thus, only $\sim 12\%$ of these defects would need to be passivated to account for the ΔD_{it} shown in Fig. 19.

Interface trap formation and passivation in these devices may be a concentration limited reaction. In standard thermal oxides the interfacial defect density is generally two orders of magnitude less than in these $\text{Al}_2\text{O}_3/\text{SiO}_x\text{N}_y$ films, and hydrogen is generally thought to create interface traps by the following mechanism [68, 137, 138].



However, since there are so many defects (e.g., dangling bonds) in the near interfacial regions of these films, hydrogen released during the irradiation may actually passivate some of the defects.

Therefore, instead of the reaction shown in equation 4, it is possible that the mechanism for interface passivation in these devices could be something like



Equation 5 shows a potential mechanism by which, hydrogen released during the irradiation could passivate a dangling bond and reduce the measured interface trap density. Indeed, the decrease in D_{it} begins to saturate after 500 krad(SiO_2), suggesting this process is relatively inefficient, and may only be observed in devices where the pre-irradiation interfacial defect density is extremely large. Nevertheless, additional work is required to determine whether this type of hydrogen passivation or some other mechanism is responsible for this effect.

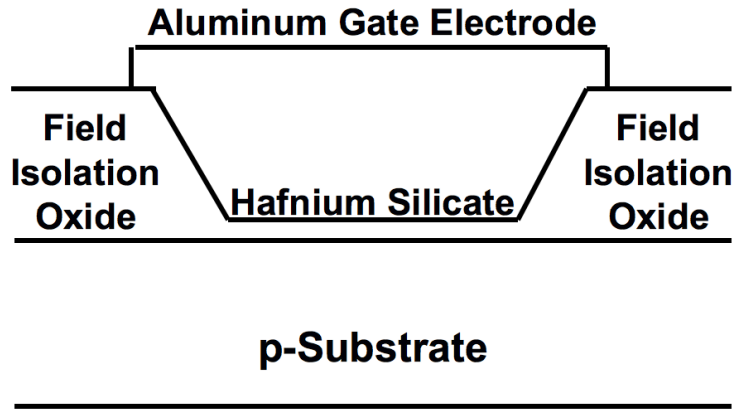


Figure 20: Schematic diagram showing the cross section of the hafnium silicate devices.

CHAPTER IV

HAFNIUM-BASED DIELECTRICS

Hafnium silicate has a relatively high dielectric constant (~ 20) compared to Al_2O_3 and SiO_2 , is less reactive with polysilicon than many of the other dielectrics being pursued, and has shown encouraging results in measurements of reliability such as TDDB and mean time to failure [14, 20, 22, 23, 42]. These characteristics make hafnium based dielectrics strong candidates for future (~ 4 -5 generations) IC technologies.

The devices used here were $1 \times 10^{-4} \text{ cm}^2$ and $2.5 \times 10^{-5} \text{ cm}^2$, aluminum gate, MIS capacitors with 4.5 nm EOT hafnium silicate gate insulators and 200 nm field isolation oxides, as shown in Fig. 20. The physical thickness of the films is $\sim 29 \text{ nm}$ and the dielectric constant is ~ 24 . The capacitors were built at North Carolina State University on 2 in., p-type Si(100) wafers with a doping concentration of $\sim 10^{18} \text{ cm}^{-3}$. The hafnium silicate gate dielectric was deposited using CVD following a wet etch of the field isolation oxide. The deposition temperature and pressure were $200 \text{ }^\circ\text{C}$ and 300 mTorr. The CVD precursors were O_2 , hafnium t-butoxide ($\text{Hf}[\text{CO}(\text{CH}_3)_3]_4$), and silane (SiH_4). The resulting film composition was approximately $\text{Hf}_8\text{Si}_{25}\text{O}_{67}$. Following deposition the devices were given a rapid thermal anneal (RTA) in argon for thirty seconds at $700 \text{ }^\circ\text{C}$. The backside of the wafer was then sputtered with aluminum to allow electrical contact to the substrate. Test chips from each wafer were prepared and packaged in 40 pin ceramic DIPs at Sandia National Laboratories.

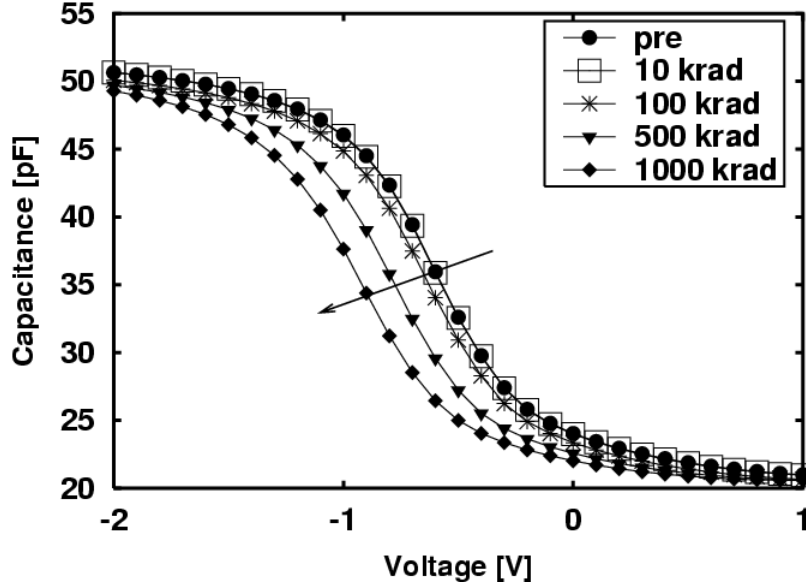


Figure 21: Pre and post irradiation 1 MHz CV measurements on a $1 \times 10^{-4} \text{ cm}^2$ hafnium silicate capacitor with an EOT of $\sim 4.5 \text{ nm}$, irradiated to total doses of 10, 100, 500 and 1000 krad(SiO_2) at 2 V.

Irradiations were performed at a dose rate of $\sim 525 \text{ rad}(\text{SiO}_2)/\text{s}$ using an ARACOR 10-keV x-ray source. The capacitors were irradiated incrementally to a total dose of either 500 krad(SiO_2) or 1000 krad(SiO_2). A total of ~ 30 capacitors were irradiated at biases ranging from -1 V to 2 V. These capacitors did not receive any post-processing baking treatments or bias stress prior to irradiation to be certain the effects discussed below in chapter VI did not influence the radiation results. Additionally, all irradiation biases were evaluated on supplementary parts from the same wafer to confirm there was no charge injection due to the applied field. All irradiation data reported in this thesis for hafnium silicate devices were obtained from capacitors with leakage currents of less than 10 pA, capacitance within $\pm 10\%$ of the theoretical value, and no hysteresis in the CV characteristics.

Radiation Response

Fig. 21 shows representative 1 MHz CV data after total dose exposure to 10, 100, 500, and 1000 krad(SiO_2) at a gate bias of 2 V. There is a monotonic increase in net oxide trap charge density with increasing dose. After total doses of 500 and 1000 krad(SiO_2), these devices exhibit midgap voltage shifts of $\sim -0.24 \text{ V}$ and $\sim -0.4 \text{ V}$, respectively. For these same total doses the flatband voltage shifts are $\sim -0.24 \text{ V}$ and $\sim -0.4 \text{ V}$. Therefore, ΔN_{ot} is estimated (using equation 1) to be \sim

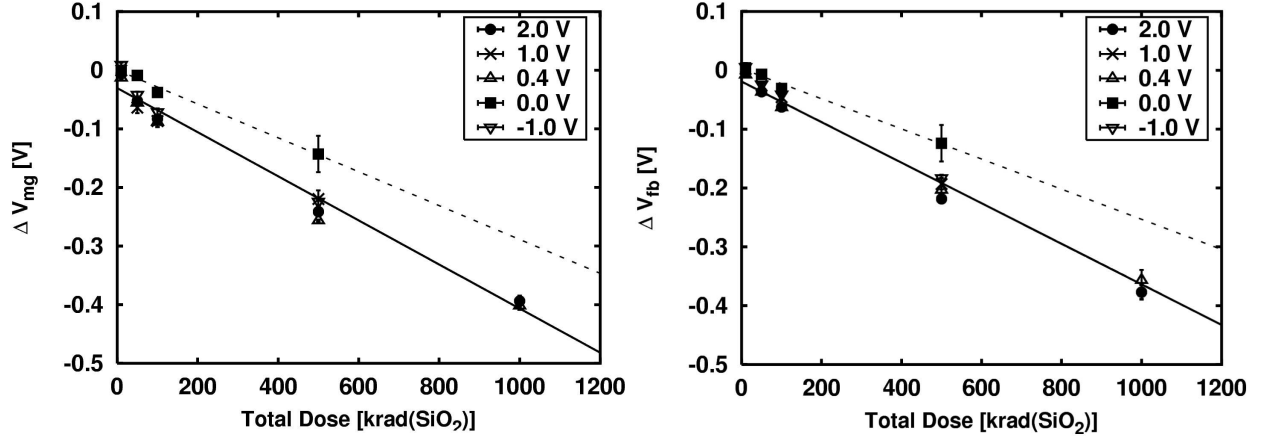


Figure 22: A summary of a) midgap voltage shifts and b) flatband voltage shifts for total dose irradiations at biases of -1 V, 0 V, 0.4 V, 1 V, and 2 V for hafnium silicate capacitors with 4.5 nm EOT insulators.

$7.5 \times 10^{11} \text{ cm}^{-2}$ after 500 krad(SiO_2) and $\sim 1.2 \times 10^{12} \text{ cm}^{-2}$ after 1000 krad(SiO_2). Since $\Delta V_{mg} \approx \Delta V_{fb}$ there is no measurable interface trap build-up with ionizing irradiation for these devices to within the accuracy of the measurement. For these hafnium silicate devices this result may be due to the large pre-irradiation density of interface charge ($\sim 2 \times 10^{12} \text{ cm}^{-2}$, as calculated by comparison to the theoretical CV characteristics of these devices) [139]. The effect of these charges can be seen by the relatively large stretchout of the pre-irradiation curve in Fig. 21 [140].

Figs. 22a and 22b show ΔV_{mg} and ΔV_{fb} for all total doses and bias conditions. The data in these figures represent the average of the results from ~ 5 capacitors for each bias condition.

These data indicate the radiation induced midgap and flatband voltage shifts are nearly the same for all radiation biases shown here except 0 V. The solid line is a linear fit of the -1 V, 1 V, 0.4 V, and 2 V irradiation data, and the dashed line is a linear fit of the 0 V data. The lack of a significant bias dependence in these data at low electric fields has also been observed in thermal SiO_2 [38]. In this limited bias range, this may result from the competition between an increase in charge yield and a decrease in effective hole capture cross section with increasing electric field [38]. Since both positive and negative biased irradiations result in the same amount of damage, these data suggest that the radiation induced charge centroid is not strongly affected by the radiation bias. This may be consistent with a low mobility or a large capture cross section for holes in the bulk of these films. The shifts seen in Figs. 22a and 22b are much larger than would be expected for high-quality radiation-hardened thermal oxides [46, 115–117]. Although the

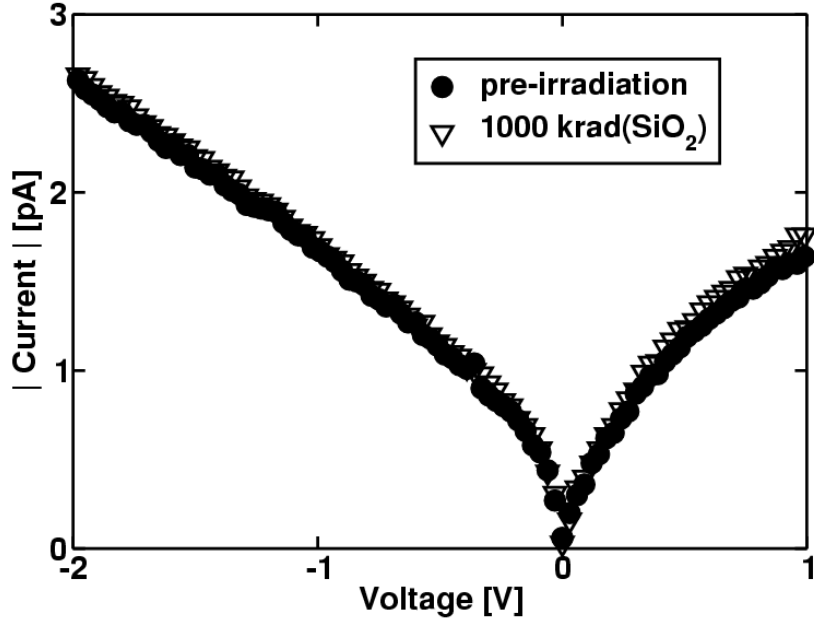


Figure 23: Absolute value of leakage current as a function of gate voltage during current-voltage measurements of the devices of Fig. 21

radiation hardness of these hafnium silicate dielectrics is much worse than for radiation-hardened thermal oxides of the same thickness, these results are still promising for the use of hafnium silicate dielectrics in advanced radiation-hardened MOS technologies. Assuming that the buildup of oxide-trapped charge in hafnium silicate dielectrics also follows a t_{ox}^4 thickness dependence as observed for stacked Al_2O_3 dielectrics, for practical EOT hafnium silicate dielectric thicknesses (<2 nm EOT or physical thicknesses <12 nm), the midgap voltage shift would be approximately 50 times lower or approximately 8 mV at 1 Mrad(SiO_2).

Fig. 23 is a plot of leakage current measured as a function of gate bias for the devices of Fig. 21. These data show that there is no noticeable increase in leakage current with radiation exposure up to 1000 krad(SiO_2). The currents shown in Fig. 23 are low enough that devices like these could

be used in applications that require low power or standby operation. However, these currents are about a factor of ten too large to allow characterization of these devices via alternative techniques such as thermally-stimulated-current [114, 141, 142].

Processing Dependence

Fig. 24 is a plot of ΔV_{mg} for 7.5 nm Al_2O_3 (same data as Fig. 13) and HfO_2 layers on 1.1 nm interfacial oxynitrides which received various anneals (no anneal, FGA, or O_2 anneal + FGA) after

high- κ atomic layer deposition. The hafnium oxide/oxy-nitride gate stacks in Fig. 24 were processed in a similar manner as the Al_2O_3 /oxy-nitride gate stacks discussed in chapter III. The HfO_2 devices that received no anneal show almost no shift at 10 Mrad(SiO_2), whereas the annealed devices shift ~ -200 mV. The HfO_2 devices in Fig. 24 had a hysteresis that varied with processing just like the Al_2O_3 devices of Fig. 13. For all of the devices in Fig. 24 the amount of CV hysteresis was inversely proportional to the magnitude of the radiation induced voltage shift. Thus, the non-annealed devices show the best radiation response, and have the most CV hysteresis, whereas the Al_2O_3 devices annealed in forming gas have the worst radiation response and have no measurable CV hysteresis. It is interesting to note that the Al_2O_3 and HfO_2 devices that received an O_2 anneal and FGA show similar amounts of CV hysteresis and have nearly identical radiation responses. This processing dependence certainly warrants follow-on study, and may crucially depend on the relative amounts of hole and electron traps in the near-interfacial region of the gate dielectrics. To quantitatively separate the effects of processing on electron and hole trapping in gate dielectrics, it is necessary to use techniques such as thermally stimulated current (TSC) [142]. Unfortunately, due to the stringent current and bias/temperature requirements for TSC, it has not yet been possible to use this method for devices with high- κ gate dielectrics [114, 141, 142].

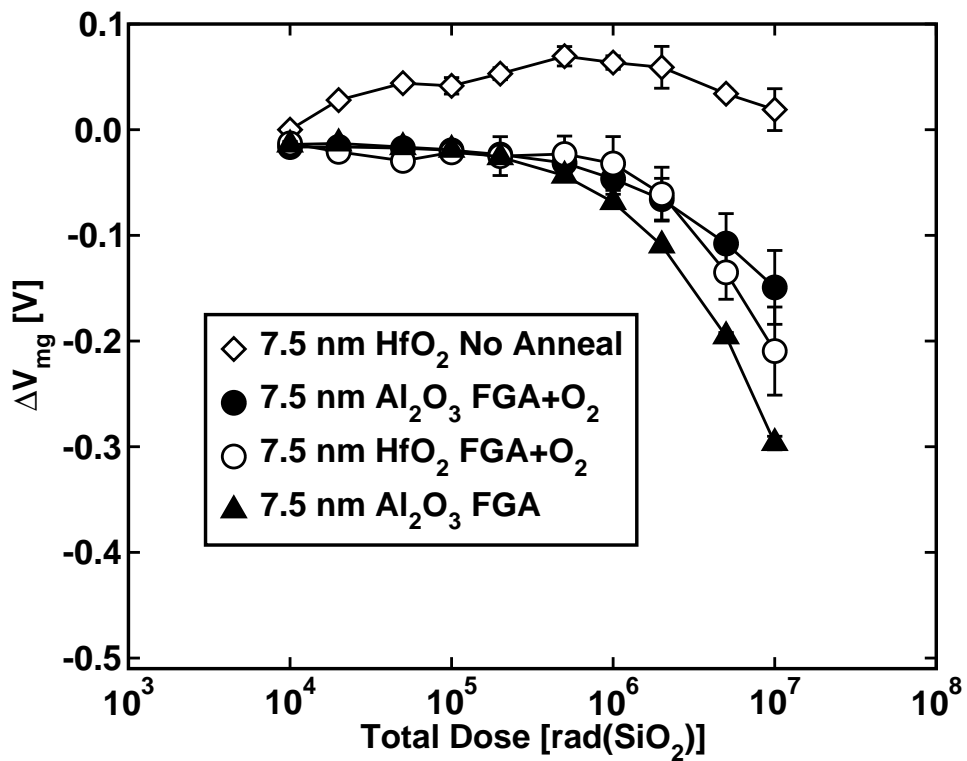


Figure 24: Midgap voltage shift versus dose for 7.5 nm HfO₂ and Al₂O₃ ALD deposited on a 1.1 nm oxynitride for several annealing conditions.

CHAPTER V

CHARGE-TRAPPING EFFICIENCY

To understand the physical significance of the trapped charge densities illustrated by Figs. 9 and 22, it is possible to estimate an effective trapping efficiency for these devices. Trapping efficiency is a dimensionless quantity used to approximate the intrinsic “trappiness” of the insulator [143]. The effective trapping efficiency of an alternative dielectric is defined here as what the trapping efficiency would be if the gate dielectric were SiO₂ instead of an alternative dielectric. This definition is consistent with the concept of EOT, which describes what the thickness of the dielectric would be if it were SiO₂ instead of an alternative dielectric, based on the measured capacitance value. Neglecting possible dose enhancement effects, the effective trapping efficiency can be estimated for an alternative dielectric film using

$$f_{ot} = -\frac{\Delta V_{mg}\epsilon_{ox}}{q\kappa_g f_y t_{eq} t_{phys} D} \quad (6)$$

where f_{ot} is the effective trapping efficiency, ΔV_{mg} is the midgap voltage shift, ϵ_{ox} is the dielectric constant of SiO₂ ($\sim 3.5 \times 10^{-13}$ F/cm), $-q$ is the electronic charge, κ_g is the number of electron-hole pairs (EHP) generated per unit dose, f_y is the charge yield, t_{eq} is the equivalent oxide thickness, t_{phys} is the physical thickness of the alternative dielectric, and D is the total dose [143].

The effective trapping efficiency calculated using equation 6 is a figure of merit that can be used to compare radiation responses of high- κ materials, and it is important to understand the assumptions and approximations built into this calculation. Some of the quantities in equation 6 such as κ_g and f_y are not well known for many alternative dielectrics. However, the idea of equation 6 is to leverage the extensive knowledge for SiO₂ to get a reasonable estimate of the effective trapping efficiency for these new materials [42]. For charge yield (f_y) it is possible to use the value in SiO₂ for the same oxide electric field during irradiation [144]. To get an estimate for charge generation κ_g it is possible to use the known value for SiO₂ ($\sim 8.1 \times 10^{12}$ cm⁻³rad⁻¹(SiO₂)) [144] scaled by the ratio of the band-gap of SiO₂ to the band gap of the high- κ material [30]. This is a first order approximation to account for the increase in EHPs generated per unit dose in the high- κ dielectric compared to SiO₂, due to the difference in band gap energies. Equation 6 includes a term for the physical and electrical thickness of the high- κ material. In similar equations for SiO₂, both of these effects are accounted for by a single t_{ox}^2 term [143]. However, since equation 6 incorporates dielectric constant of SiO₂, it is necessary to distinguish between the electrical thickness and the

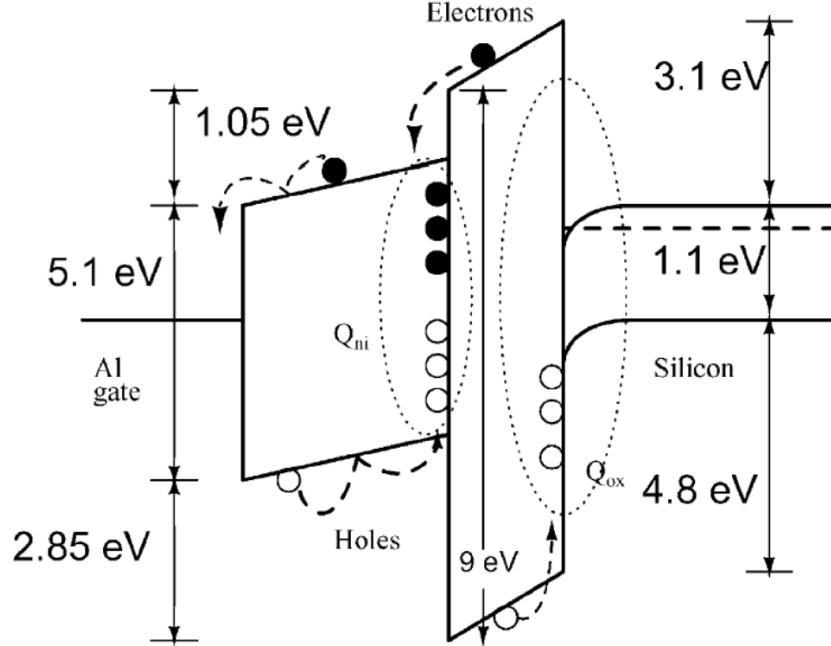


Figure 25: An energy band diagram for nitride-oxide MOS gate stacks during irradiation with positive bias on the gate electrode. After [145]

physical thickness of the alternative gate dielectric [42]. In equation 6, the t_{phys} term accounts for charge generation throughout the entire volume of the oxide. As mentioned in chapter III, charge in the near interfacial region of the dielectric can be removed via tunneling, which effectively thins the gate dielectric by the tunneling distance into the gate dielectric. If desired it is possible to account for this effect by replacing t_{phys} with $(t_{phys} - t_{tunneling})$. The t_{eq} term is to account for the moment arm effect that results from projecting the spatial distribution of the charges in the oxide to the interface [113]. This ensures that all comparisons are made for charge in the same location (at the Si/high- κ interface). However, it also means it possible to underestimate the effective charge trapping efficiency. To understand this, it is important to realize that one charge at the interface has the same effect (electrically) as two charges in the middle of the dielectric. Therefore, if it location of the charge centroid was known, it would be appropriate to add a scale factor (i.e., 2 if the centroid is in the middle of the dielectric) to the numerator of equation 6.

Several high- κ devices have a gate stack structure rather than a single dielectric. In some instances this is by design (e.g., the devices of chapter III) to improve interface quality, but there is also the possibility of unintentional surface oxidation of the Si substrate during processing. This creates a “parasitic” SiO₂ layer at the interface, which leads to an overall reduction of the

capacitance. It is important to realize that the effects of dielectric stacks are not accounted for in equation 6. There are several differences in the way charges move and are trapped in stacked structures relative to standard single material gate dielectrics. For example, consider Fig. 25 which shows an energy band diagram of a nitride-oxide gate stack during irradiation with positive gate bias. Comparing this with Fig. 1 it is possible to see that stacked structures can have barriers which can hinder or stop charge motion to the Si interface. Furthermore, it is possible for charge to build-up at the interfaces between the dielectrics. Hence the trapping properties of stacked structures can be significantly different than single material gate dielectrics. Raparla *et al.* [145] have modeled charge transport and trapping in stacked nitride-oxide dielectrics, however, the difficulty of this problem increases significantly when the band offsets and band gaps are not well known. Robertson [29] has calculated the band gaps of several high- κ materials as well as the band offsets of these materials with Si. However there is not much information available about how these materials line up with each other, and therefore trying to include effects of having a gate stack in the calculation of effective trapping efficiency would involve making a series of additional assumptions.

The location of the oxide trapped charge centroid after exposure to ionizing radiation is dependent on the irradiation bias conditions [146, 147]. For large positive fields the charge centroid will tend to be toward the substrate interface, and it will tend to be toward the gate interface for large negative fields. For low electric field and zero volt biased exposures, the charge centroid will tend to be toward the middle of the dielectric. Fleetwood [147] has developed a method to calculate the location of the charge centroid using *TSC* and *CV* analysis. Looking more closely at hole and electron trapping efficiencies and calculating charge centroid locations could be an interesting topic of follow-on research to this work when high- κ devices are able to meet the stringent current requirements for TSC analysis. As mentioned previously, there are several assumptions and approximations built into equation 6. For these reasons, this figure of merit is called an effective trapping efficiency rather than the trapping efficiency. In order to calculate the true trapping efficiency of a high- κ material, it is necessary to perform more rigorous studies determine factors such as κ_g and f_y , and it is also important to account for effects such as the location of the charge centroid and dielectric stack structures. Research in the area of high- κ gate dielectrics is currently at a point where several materials are being examined, and it is not clear which material or materials will be used in future commercial ICs. Although it may be possible to calculate a true trapping efficiency for several of these new materials, this type of in depth analysis is very tedious and time consuming and therefore defeats the purpose of using the effective trapping efficiency as a quick first order

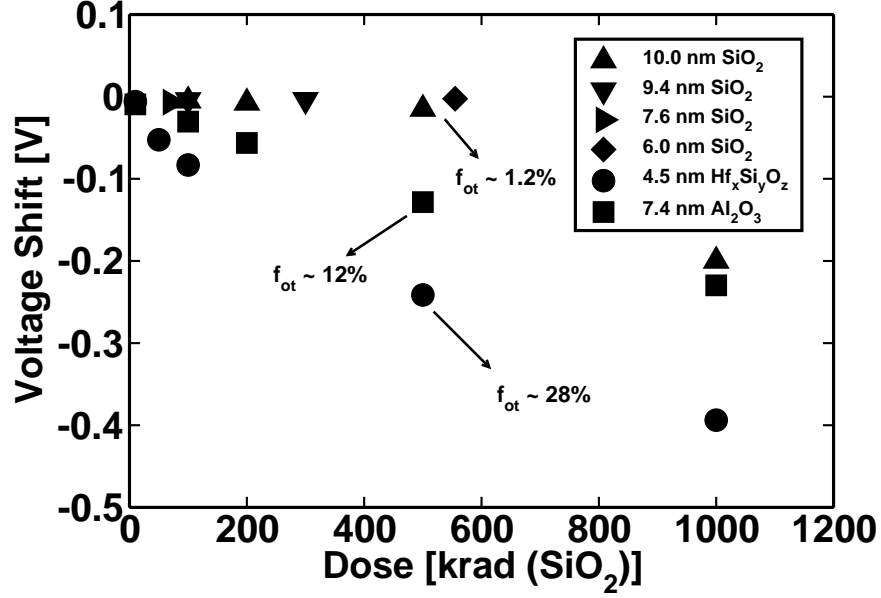


Figure 26: Voltage shift versus dose for several ultra thin thermal oxides and high- κ dielectrics. For similar electrical thicknesses, the intrinsic quality of the thermal oxides is much better than the high- κ films.

comparison of material quality and trapping properties. Nevertheless, it would be beneficial to develop techniques, such as ways to model complex dielectric stacks, especially if these types of structures become prevalent in future technologies.

Fig. 26 is a plot of the radiation induced voltage shift for the high- κ devices of Figs. 9 and 22 as well as several thermal oxides [46, 116, 148, 149]. These data show that alternative dielectrics trap significantly more charge than thermal oxides of similar electrical thickness. Some of the difference is due to the increased physical thickness of the high- κ films relative to the SiO_2 , but the high- κ films also have a much larger trapping efficiencies than the thermal oxides. For a total dose of 500 krad(SiO_2) the effective trapping efficiencies of the hafnium silicate and Al_2O_3 /oxynitride capacitors are $\sim 28\%$, and $\sim 12\%$ respectively [42,44]. The trapping efficiency of the Al_2O_3 /oxynitride transistors (not shown in Fig. 26) was larger at $\sim 38\%$ [44]. However, at this same total dose the trapping efficiency of the thermal oxides in Fig. 26 is only $\sim 1.2\%$. Therefore, the intrinsic material quality of the thermal oxides is ~ 16 to 23 times better than these alternative gate dielectrics.

The trapping efficiency of these hafnium silicate devices ($\sim 28\%$) is larger than the trapping efficiency ($\sim 1.2\%$) of the SiO_2 devices by a factor of ~ 23 . In contrast, the difference in voltage shifts in Fig. 26 between the hafnium silicate and 10 nm SiO_2 films is only a factor of ~ 16 . To better understand the relationship between midgap voltage shift and trapping efficiency, consider

the ratio of the parameters in equation 6 for hafnium silicate to the parameters for SiO₂. The values of these ratios (hafnium silicate to SiO₂) are as follows: $f_{ot} \sim 23$, $\kappa_g = 3/2$, $f_y = 1/3$, $t_{eq} = 1/2$, $t_{phys} = 3$, and q , ϵ_{ox} , and D all equal one. Therefore, the factor of 16 difference between the hafnium silicates and thermal oxides in Fig. 26 is because there is half as much trapping in the hafnium silicate due to differences in charge generation and charge yield, 3 times more trapping in the hafnium silicate since it is physically thicker, half as much moment arm effect because it is electrically thinner, and ~ 23 times more trapping because the hafnium silicate films have a higher defect density than the SiO₂.

Additionally, it is interesting to note that the Al₂O₃/oxynitride nMOSFETs and the hafnium silicate capacitors have similar effective trapping efficiencies and radiation bias dependences. In chapter IV it was suggested that the lack of radiation bias dependence in these devices could be due to a large trapping cross section or a low hole mobility in the bulk of these dielectrics. The trapping efficiency calculation has shown us the intrinsic material quality of both of these sets of devices is similar, and they are both much more likely to trap charge than either the Al₂O₃ capacitors or the thermal oxides.

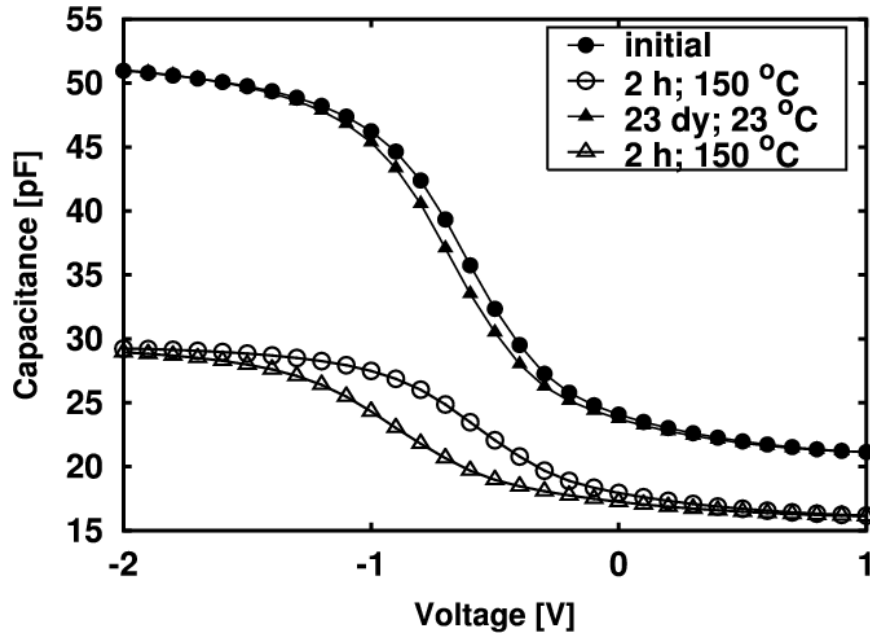


Figure 27: Capacitance-voltage curves for $1 \times 10^{-4} \text{ cm}^2$ capacitors with 4.5 nm EOT, which were baked in room ambient at $150 \text{ }^\circ\text{C}$ for 2 hours without bias, annealed in room ambient at $\sim 23 \text{ }^\circ\text{C}$ for 23 days, then baked again at $150 \text{ }^\circ\text{C}$ for an additional 2 hours.

CHAPTER VI

RELIABILITY

Gate oxide reliability has been studied intensively; particularly as commercial gate oxide thickness has moved to the ultra-thin oxide regime, generally interpreted as sub 2-5 nm. Some common types of reliability screens used to evaluate long term devices reliability are elevated temperature bias stress or “burn-in” tests [150,151] and TDDB tests [152,153]. It has been shown that “burn-in” screens can alter the radiation response of SiO_2 [150,151], and that ion exposure can reduce lifetimes in TDDB tests [87,91,92]. Therefore, it is important to determine how alternative gate dielectrics perform in common reliability screens.

Effects of Baking

Fig. 27 is a plot of representative CV curves for the hafnium silicate devices of Fig. 22 that shows the effect of baking these devices, unbiased, in room ambient at $150 \text{ }^\circ\text{C}$ for 2 hours. After the baking treatment, a $\sim 40\%$ decrease in the accumulation capacitance and a $\sim 24\%$ decrease in the depletion capacitance is observed for these capacitors. In addition to a reduction in capacitance,

after baking the devices exhibit a hysteresis of > 100 mV in the CV characteristics (not shown). After being stored in anti-static foam for ~ 3 weeks in room ambient, the hysteresis recovered, and the capacitors returned, almost completely, to their initial state (solid triangles). However, as shown by the open triangles, the effect was reproduced by subjecting the parts to a second baking treatment. Similar changes in the CV curves of hafnium silicate were commonly observed in the devices tested. However, large and reversible changes like those shown in Fig. 27 were not always seen, presumably depending on variations in device and metal characteristics from device to device. One possible cause of this effect is that the reduction and subsequent recovery of the capacitance in these devices could be due to water vapor being baked out and re-absorbed by these films [151]. To further explore this idea, the devices were stored in a vacuum desiccator at room temperature for another ~ 3 weeks following the second baking treatment. The devices were then measured again to see if the capacitance had returned to the original state in the absence of water vapor. After ~ 3 weeks of storage in the desiccator the parts did not recover, suggesting that water vapor may well be responsible for the baking effect observed in these devices.

In order to see a significant change in capacitance, either the capacitor area, dielectric thickness, or dielectric constant must change. The changes seen in Fig. 27 are not likely due to a change in area or in dielectric thickness. However, the reduction in capacitance might be due to a change in the dielectric constant. To understand this, recall that the dielectric constant of a material, defined as one plus the electric susceptibility ($1 + \chi_e$), is directly proportional to the dipole moment per unit volume [154]. Therefore, a change in the dipole moment of a material can alter the dielectric constant. Although the devices were baked at a relatively low temperature (150°C) for a short time (2 hours), perhaps enough water vapor was removed from the film to cause a noticeable change in the dielectric constant of these hafnium silicate devices. Indeed, it appears that a chemical change takes place in these devices in the absence of water vapor; however, a more detailed baking study is still necessary to determine completely the cause of the baking effect observed in Fig. 27. Similar baking effects (though often not as dramatic, and not always reversible) have also been observed on other high- κ devices. Indeed Zafar *et al.*, [58] have also observed significant effects on the charge trapping properties of Al_2O_3 gate dielectrics resulting from moisture absorption. They showed that moisture absorbed by the aluminum oxide reduced the amount of charge trapping and moved the V_{fb} closer to the calculated ideal value. Fully processed devices will be passivated to prevent moisture absorption and/or release. Still the results of Fig. 27 and [58] suggest that effects related to water vapor or hydrogen could be a significant reliability issue for future devices with alternative

gate dielectrics [68, 151].

Effects of Bias Stress

Some recent studies have determined the conduction and the valence band offsets between Si and most alternative gate dielectrics are much smaller than the band offsets between Si and SiO₂ [29, 30]. Therefore, there is a smaller barrier to electrons tunneling into the high- κ material. Hence applying large biases to these devices can cause increased charge injection from the substrate into the dielectric. Charge injection and trapping affects device reliability, by degrading device parameters such as the threshold voltage and drive current. Bias induced charge trapping in alternative gate dielectrics is generally more severe than in conventional SiO₂ gate dielectrics [17]. Trapping occurs as pre-existing traps are filled by the injected charge [56]. This is different than observed in SiO₂ where the concentration of pre-existing traps is very low ($\sim 10^{10}$ cm⁻² or less) and trap creation is the dominant mechanism [56]. Gusev *et al.* [56, 105] have shown that significant injected charge trap densities can lead to threshold voltage shifts of > 0.1 V. They have also shown that the amount of trapping can be reduced by improvements in processing. Still, trapping densities in high- κ dielectrics are unacceptable compared to SiO₂.

Charge injection and trapping could also cause a misinterpretation of the radiation response of an alternative gate dielectric. To see this, consider Fig. 28, which shows the effect of applying 3.4 V to the gate of a 2.5×10^{-5} cm² hafnium silicate capacitor for ~ 15 minutes. This is the same amount of time that it took to do the 1000 krad(SiO₂) irradiation described in chapter IV. The bias applied to the devices in Fig. 28 corresponds to an electric field of only ~ 1 MV/cm. This is not an unreasonably large field; however, in practice these devices would most likely never be operated at a bias greater than ~ 1.5 V. The midgap and flatband voltage shifts in Fig. 28 are ~ 0.4 V. Comparing this value with the 1000 krad(SiO₂) irradiation data in Figs. 22a and 22b, it is observed that they are equal and opposite. Therefore, it is possible that one could drastically overestimate the radiation hardness of an alternative dielectric if electron injection due to the applied bias compensates the radiation induced trapped charge. Thus, radiation testing must be performed at biases which do not inject charge into the dielectric (i.e., the *CV* characteristics of a devices should not change due to the radiation bias alone).

Time Dependent Dielectric Breakdown

TDDDB accelerated life tests are used to construct reliability models that allow one to extrapolate the lifetime to use conditions. This extrapolation assumes that the physics of oxide wear-out does

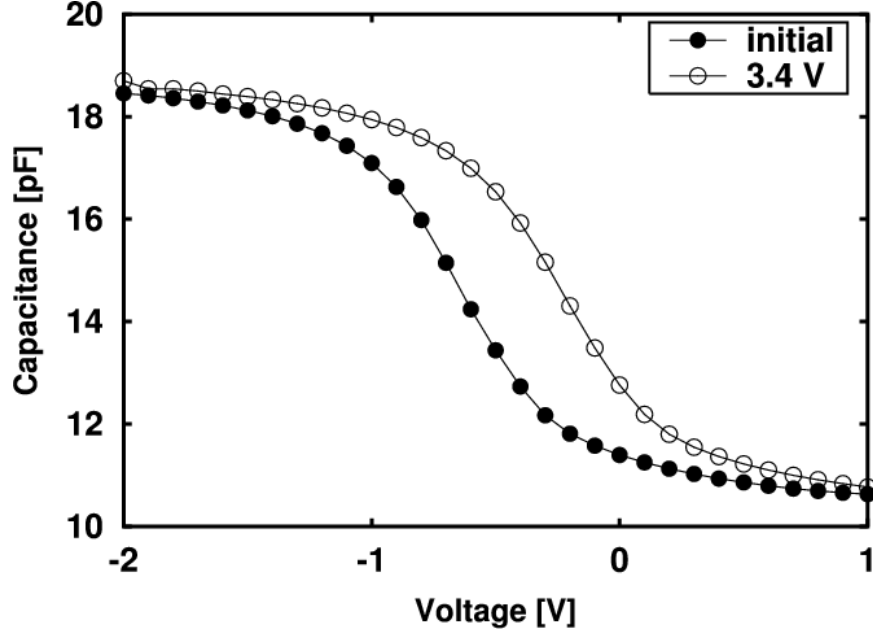


Figure 28: Capacitance-voltage curves for $2.5 \times 10^{-5} \text{ cm}^2$ capacitors with 4.5 nm EOT showing the changes observed due to a physical electric field of $\sim 1 \text{ MV/cm}$ applied for ~ 15 minutes.

not change between the test conditions and use conditions, which is an issue of continuing debate for conventional SiO_2 gate oxides. The failure of gate oxides is usually modeled using a Weibull cumulative distribution function (CDF) given by [155]

$$F(t) = 1 - e^{-\left(\frac{t}{\alpha}\right)^\beta} \quad (7)$$

where α is a scale factor and β is a shape factor, sometimes called the “Weibull slope.” $F(t)$ is a measure of the percentage of oxides that will fail by a time t . The scale parameter, α , determines the 63.2 percentile of the Weibull distribution, since $F(\alpha) = 63.2\%$ independent of β . The characteristic time $t = \alpha$ is often referred to as “ T_{63} .” The experimental lifetime of oxides subjected to constant electric fields large enough to cause oxide breakdown at laboratory time scales is typically determined by making Weibull probability plots of the data, i.e., plots of $W_f(t) = \ln(-\ln(1-F(t)))$ versus $\ln(t)$. It is important to note that changing the area or the test field will change the characteristic breakdown time $t = T_{63}$, but not the Weibull slope, β . Indeed, if the breakdown mechanism is consistent across all devices tested, data taken at different areas and fields should exhibit a constant Weibull slope. A reliability study extracts T_{63} (using $W_f(T_{63}) = 0$) where the time to failure has been accelerated by increasing the field. A model that describes the breakdown time as a function of temperature, field and area is used to extrapolate T_{63} to the use conditions. The dependence of T_{63} on oxide area can be analytically described when the correlation

between defects is controlled and understood. If the distribution of defects in the insulator is random and the defects are uncorrelated the data can be described by Poisson statistics. This condition is met in mature technologies where all processing variables are controlled and subject only to random fluctuations [156–159].

The functional form of the dependence of T_{63} on electric field and temperature has been controversial, especially with regard to the form of the electric field acceleration parameter. The field and temperature dependence of the time to breakdown has been modeled by McPherson [152, 153] as

$$\ln(T_{bd}) = \frac{\Delta H_o}{kT} - \gamma(T) \cdot E \quad (8)$$

where ΔH_o is the enthalpy of activation for Si-Si bond breakage (activation energy), $\gamma(T)$ is a field acceleration factor, and E is the electric field. In this model (known as the “E” model) oxide wear-out is driven by the field-assisted, thermal breakage of Si-Si bonds that occur at oxygen vacancies (E' centers in SiO_2) [152, 153]. An alternate model where E is replaced by $1/E$ in equation 8 has also been proposed [160]. The “1/E” model describes wear-out resulting from degradation induced by Fowler-Nordheim charge transport through the oxide film. Both the E model and the 1/E model have been used successfully to fit a wide range of experimental data [152, 153, 161, 162]. Both models have been the subject of debate over the past three decades since there is a large discrepancy in the lifetime projection for electric fields close to use conditions. The 1/E model give a much more optimistic prediction of dielectric lifetime at low fields [153, 163]. It has been difficult to validate these models since both fit experimental data at large fields (i.e., > 7 MV/cm) equally well [163]. However, results from substrate hot-electron injection studies [161, 164] and polysilicon gate electrode doping experiments [165, 166] suggest that tunneling electrons with energy related to the applied gate voltage are the driving forces for defect generation and breakdown in ultrathin oxides. Furthermore, McPherson *et al.* [153] have recently showed that elements of both models are required to fully describe breakdown in ultra thin gate oxides. This may also be true for alternative gate dielectrics as well because they are susceptible to increased charge injection relative to SiO_2 (due to reduced band offset energies).

Fig. 29 is a plot of Weibull failure distributions for aluminum oxide gate dielectrics subjected to constant voltage TDDB stress. Breakdown times that are controlled by a single failure mechanism should exhibit a straight line on this type of plot. Therefore, the 5.5 MV/cm and 5.0 MV/cm data in Fig. 29 exhibit a single failure mode. Intrinsic failures result from oxide wear-out (i.e.,

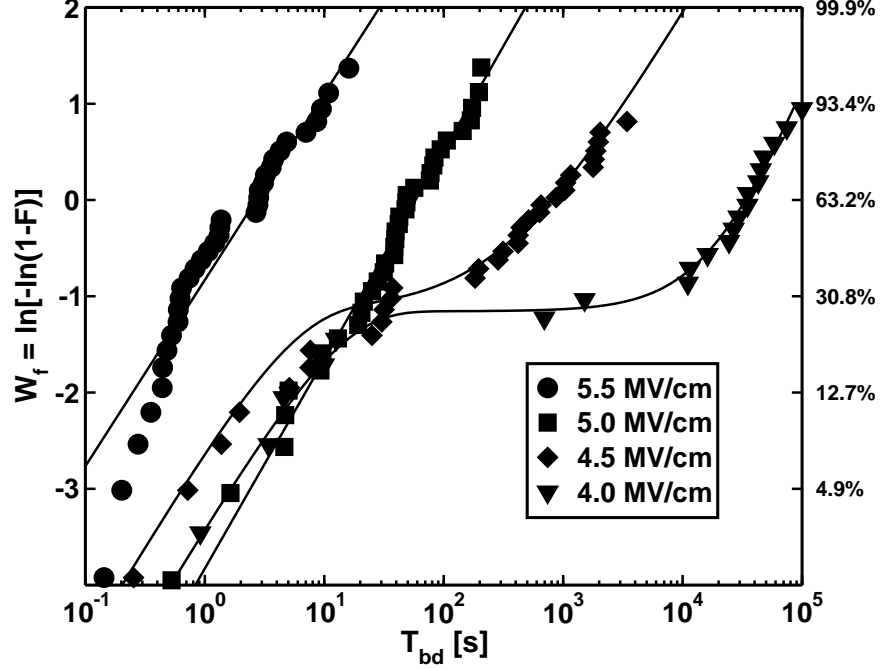


Figure 29: Time dependent dielectric breakdown test results for 7.5 nm aluminum oxide gate dielectrics deposited on a 1.1 nm interfacial oxynitride. The devices were stressed at electric fields from 4 MV/cm to 5.5 MV/cm.

bond breaking). Extrinsic failures are due to local oxide damage from an external source such as a chemical contaminant or a particle from the fabrication process. Extrinsic failures typically occur much earlier than intrinsic failures. Examples of two mode (intrinsic and extrinsic) dielectric breakdown where the extrinsic portion of the distribution is visible are shown in the 4.0 MV/cm and 4.5 MV/cm data in Fig. 29. In the case of two failure modes, the Weibull probability plot appears S-shaped. In the two-failure mechanism mode, the cumulative failure probability, $F(t)$, can be written as the weighted sum of two independent failure probabilities, $F_A(t)$ and $F_B(t)$, each described by equation 7 with independent values of α and β . If we assume that a percentage, P_A of the samples will fail by the first mechanism and $(1-P_A)$ percent of the samples will fail by the second mechanism, the total cumulative failure probability will be

$$F(t) = P_A F_A(t) + (1 - P_A) F_B(t). \quad (9)$$

Eq. 9 can be combined with Eq. 7 to allow one to calculate a total failure probability resulting from two independent failure mechanisms. Actually, it is possible that each of the distributions in Fig. 29 have intrinsic and extrinsic failures. However, these trends may not be obvious from the data because the intrinsic failure time is shorter than the extrinsic failure time for the largest electric fields. It is not clear whether the early failures in the large electric field data result from

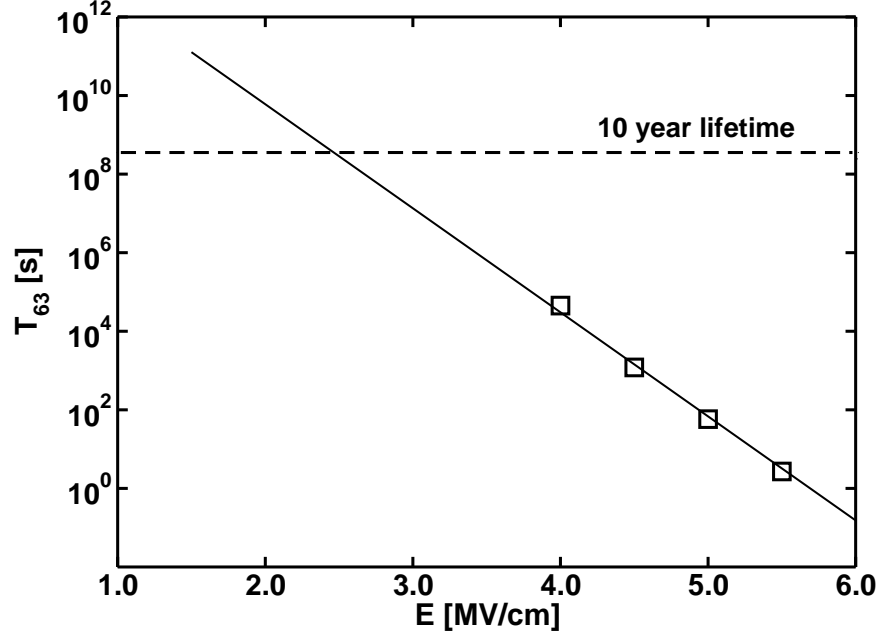


Figure 30: Lifetime extrapolation versus electric field based on the T_{63} data from the TDDB failure distribution of Fig. 29

the same mechanism as the intrinsic wear out or extrinsic failure. It is clear, however, that any early failures will result in a serious reliability problem for these devices. By looking at Fig. 29, it is possible to see that the extrinsic failure population accounts for almost 30% of the total sample set for the two lowest electric fields.

For single-mode failures, the Weibull parameters α and β were obtained using the method of maximum likelihood, generalized for use with a small number of samples [167]. The maximum likelihood method is preferred over a least-squares method of fitting since it properly accounts for limited sample statistics. The 5.5 MV/cm and 5.0 MV/cm distributions have a Weibull slope of 0.9. A Weibull slope of ~ 1 is in good agreement with high- κ TDDB data in the literature [22,93–95], but is much smaller than Weibull slopes from commercial gate oxides of comparable physical thickness ($\beta \sim 4$) [156]. A low Weibull slope indicates there are significant process variations across the wafer. The two mode failure distributions were fit manually using equation 9. The manual fit was done by forcing the intrinsic portion of the distribution to have the same slope (0.9) as the single mode failure data, while varying the other Weibull parameters until the fit appeared to match the data.

Fig. 30 shows the lifetime extrapolation of the T_{63} data of Fig. 29 versus electric field. Also shown is Fig. 30 is the duration equivalent to a 10 year operational lifetime (dotted line). Assuming

the extrapolation is accurate to first order, it can be seen that these devices have to be operated below 2.5 MV/cm in order to achieve an operational lifetime of > 10 years. That being said, there are some assumptions behind this extrapolation. First, it is necessary to assume that the physics of breakdown do not change from test fields to operational fields. This is still under debate, but here it will be assumed that this method is valid, since it is the most common method used for lifetime extrapolations of conventional SiO₂ gate oxides. Furthermore, the accuracy of the extrapolation in Fig. 30 is questionable due to the low Weibull slope and the large population of extrinsic failures. Therefore, these data do not suggest that it would be safe to pick any random part out of this lot and assume it would operate reliably for > 10 years at 2.5 MV/cm. Still, the extrapolation is a good figure of merit, and should become more valid with improvements in processing these materials. There is a lot of room for significant improvements in the processing methods used to make high- κ devices, and therefore future production high- κ oxides may not have the same problems as these devices. Indeed, initial life testing of gate oxide reliability for a new SiO₂ radiation hardened technology found significant extrinsic failures, but this percentage has been reduced in more recent test lots as the process was improved [168]. Therefore, process improvements may not significantly change the lifetime prediction of Fig. 30, but rather make this prediction more accurate.

CHAPTER VII

SUMMARY AND CONCLUSIONS

In this thesis, the effects of radiation bias, film thickness, and device processing conditions on the radiation response of high- κ alternative gate dielectric stacks have been discussed. The midgap voltage shifts for future high- κ films of most interest to industry (i.e., < 2.0 nm) are projected to be on the order of a few millivolts at total doses of 1 Mrad(SiO_2) or more. Therefore, as is the case for ultra thin SiO_2 , charge trapping in the gate oxide after exposure to ionizing radiation will not likely be a major concern for future devices which incorporate alternative gate dielectrics. Still, high- κ device fabrication is very much in the research phase, and there are currently no well defined standard processes for making devices with alternative gate dielectrics. Indeed, there is still debate as to which high- κ material is best suited for use in future ICs. Therefore, it is important to continue to research these materials and determine how variations in processing and device design effect radiation response. For the high- κ /oxynitride gate stacks examined here, it was shown that the interfacial oxynitride plays an important role in the device radiation response. For ~ 1.4 nm decrease in SiO_xN_y thickness, there was not only a reduction in E_{bd} of more than 1 MV/cm for the aluminum oxide capacitors, but also a $\sim 31\%$ reduction in ΔV_{mg} for a given Al_2O_3 thickness. The radiation responses of these high- κ devices is also strongly dependent on post-high- κ deposition anneals. The amount of radiation-induced oxide trapped charge was found to be inversely proportional to the amount of CV hysteresis. The aluminum oxide capacitors that received an O_2 anneal followed by a FGA showed a small amount of pre-irradiation CV hysteresis and a $\sim 50\%$ reduction in ΔV_{mg} , relative to the capacitors that received a FGA only. Similar trends were also shown for hafnium oxide/oxynitride gate stacks and an even larger variation in trapping was observed in the Al_2O_3 nMOSFETs, probably due to the 1000°C dopant activation anneal. The variations in radiation response with processing could be the result of changes in either the hole or the electron trapping properties of these materials. These results warrant follow-on study when the leakage current levels in these devices are suitable for analysis with other measurement techniques that make it possible to separate the effects of positive and negative charge trapping (i.e., TSC).

It is unlikely there will be one single high- κ material that will replace SiO_2 for all applications. Each alternative gate dielectric has advantages and disadvantages for a specific application, but

currently none of the high- κ dielectrics have been able to achieve all of the properties of SiO₂ outlined in chapter I. Therefore, it is important to be able to easily compare different materials and film compositions in order to make engineering decisions about which process changes lead to the highest quality final product. For this purpose effective trapping efficiency was developed as a tool to compare the intrinsic trapping properties of alternative gate dielectrics and SiO₂ gate oxides. Calculating effective trapping efficiencies makes it possible to compare the trapping properties of several materials without having to know all of the material properties of each new material. Instead, it is possible to test a group of various devices/dielectrics and leverage the extensive knowledge of SiO₂ to compare their relative material qualities. In this work, it was shown that the effective trapping efficiencies of alternative gate dielectrics are significantly larger than for SiO₂ gate oxides. The Al₂O₃/oxynitride nMOSFETs and the hafnium silicate capacitors exhibited effective trapping efficiencies of > 30%, and the Al₂O₃/oxynitride capacitors had an effective trapping efficiency of \sim 12%. However, the thermal oxides showed a trapping efficiency of only \sim 1%. An increase in trapping efficiency from 1% to 12% or 30% means that the alternative gate dielectrics will trap \sim 11% to 29% more of the initial charge than thermal SiO₂ of comparable electrical thickness.

An initial look at the long term reliability of alternative gate dielectrics was also presented. Burn-in baking treatments were shown to degrade the device characteristics, presumably as water vapor was removed from the film. It has also been demonstrated that radiation testing at large gate biases may lead to excess bias induced charge trapping and a potential overestimation of the radiation hardness of an alternative dielectric. TDDB accelerated life tests showed that the high- κ materials have failure distributions with unacceptably low Weibull slopes and a large (\sim 30%) probability of extrinsic failure. These obstacles, most likely related to processing inconsistencies, make it difficult to qualify these parts for use in long duration missions. It was projected that the devices examined here would need to be operated below 2.5 MV/cm to achieve a 10 year operational lifetime. To put this in perspective, an aluminum oxide device with an EOT of \sim 2 nm that had a failure distribution like the devices in chapter VI could only be used in technologies that operated at voltages of \sim 1 V or less. According to the SIA roadmap [82], V_{DD} will not scale to \sim 1 V until at least 2006. Furthermore, since the failure distribution of these devices is so broad, it would be impossible to guaranteed that any given part would actually operate reliably for that duration. Therefore, before TDDB life tests can be used to accurately and reliably predict operational lifetime for alternative gate dielectrics, there must be significant process improvements which yield tighter

failure distributions and eliminate the high probability of extrinsic failures.

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