HOT-CARRIER RELIABILITY SIMULATION IN AGGRESSIVELY SCALED MOS TRANSISTORS

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CHAPTER I

INTRODUCTION

Hot-Carrier Degradation in MOSFETs

Advances in semiconductor manufacturing techniques and ever increasing demand for faster and more complex Integrated Circuits (ICs) have driven the associated Metal Oxide Semiconductor Field Effect Transistor (MOSFET) sizes close to their physical limits. On the other hand, it has not been possible to scale the supply voltage used to operate these ICs proportionately due to factors such as compatibility with previous generation circuits, noise margin, power and delay requirements, and non-scaling of threshold voltage, subthreshold slope, and parasitic capacitance. While the consequent increase in internal electric fields in aggressively scaled MOSFETs comes with the additional benefit of increased carrier velocities, and hence increased switching speed, it also presents a major reliability problem for the long term operation of these devices. As devices are scaled the benefits of higher electric fields saturate while the associated reliability problems get worse.

The presence of large electric fields in MOSFETs implies the presence of high energy carriers, referred to as "hot-carriers", in such devices. The carriers that have sufficiently high energies and momenta can get injected from the semiconductor into the surrounding dielectric films such as the gate and sidewall oxides as well as the buried oxide in the case of Silicon-On-Insulator (SOI) MOSFETs (Fig. 1). The presence of mobile carriers in the oxides triggers various physical processes that can drastically change the device characteristics during normal operation over prolonged periods of time eventually causing the circuit to fail. Such degradation in device and circuit behavior due to injection of energetic carriers from the silicon substrate into the surrounding dielectrics will be referred to as "hot-carrier degradation" in the rest of this document. It is clear that the presence of large electric fields has major influence on the long term operation of modern ICs. These Hot-Carrier (HC) related device instabilities have become a major reliability concern in modern Metal Oxide Semiconductor (MOS) transistors and are expected to get worse in future generation of devices. The study of the fundamental physical processes that result in device parameter variation due to HC injection is essential to provide guidelines for avoiding such

problems in future ICs.

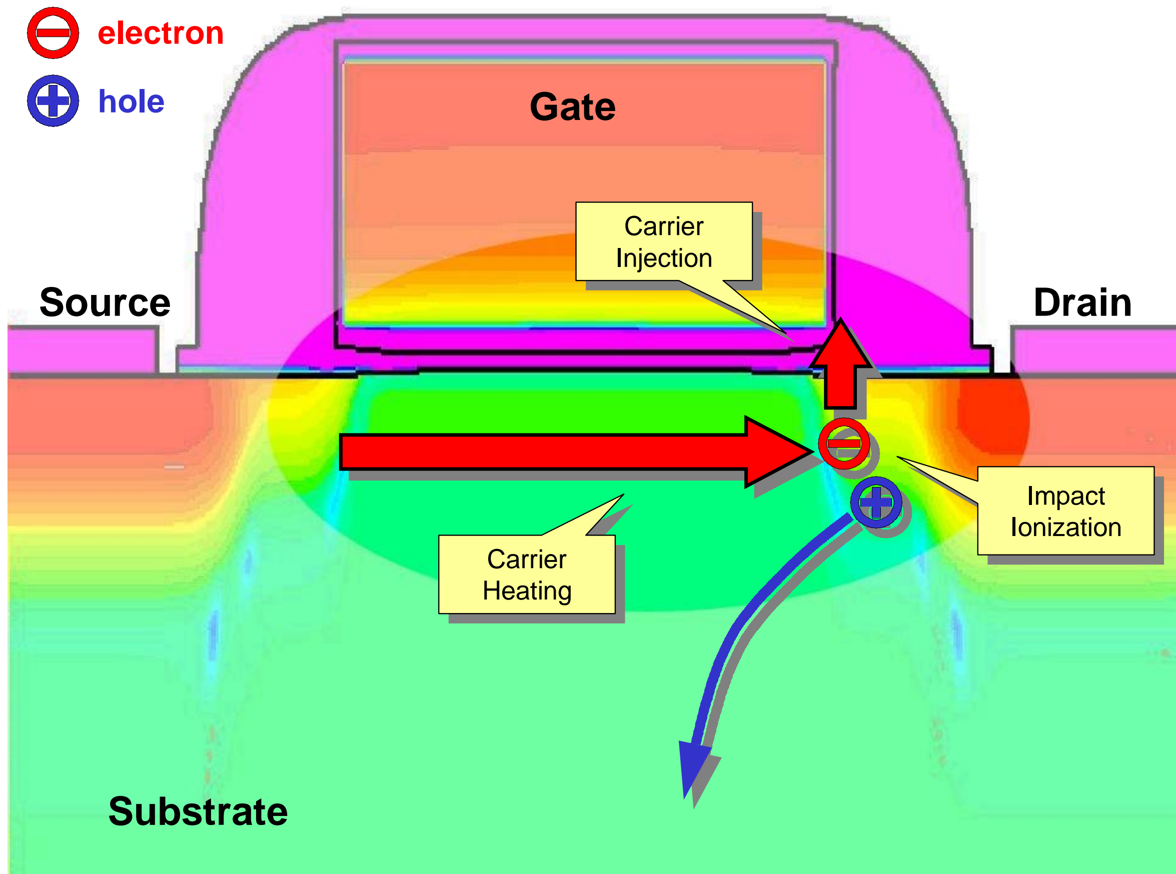


Figure 1: The basic processes leading to HC injection in MOS transistors. The color contours in the MOS substrate and polysilicon gate regions represent the net doping concentration.

Motivation: Modeling Requirements

HC-induced device degradation has been the subject of numerous studies over the past several decades. The effect of carrier heating has been observed in a variety of applications and device structures [1, 2, 3]. In fact, certain carrier heating processes have been utilized as the basis of operation of circuits such as Electrically Erasable Programmable Random Access Memory (EEP-ROM) cells. As soon as the potential detrimental influence of HC injection on the circuit reliability was recognized, several fabrication strategies were devised to reduce it without compromising the circuit performance [4]. In spite of the vast amount of research performed to understand the HC

degradation phenomenon, little agreement exists on the exact nature of the physical processes involved in HC degradation to this date. These studies have, however, provided useful insights into the physical mechanisms involved in device degradation and have aided the development of several fabrication and design techniques to mitigate the associated reliability problems. As the push to scale the semiconductor devices continues, we are beginning to run out of these fabrication "tricks" due to the limited knowledge of the sources of the degradation mechanisms and their dependence on the process and geometrical parameters associated with the devices.

In the past, methods for the evaluation of HC reliability have been based on physical models for long-channel transistors. These approaches have been remarkably successful in predicting the time-dependence of HC degradation on factors such as channel length, channel doping, and supply voltage in long-channel devices. Even though the limitations in their application to deep sub-micron devices have long been recognized [5], as devices are scaled, the same techniques continue to be applied to short-channel devices. In short-channel devices, however, several assumptions made in the conventional approaches break down and hence the parameters associated with most of these models lose their physical meaning. These model parameter are usually extracted by fitting the model to experimental data. Such empirical approaches, though useful for qualitative evaluation of existing technologies, provide little insight into the physical mechanisms responsible for the device degradation. Furthermore, the semi-physical model parameters extracted from a given set of experiments on a particular technology are not able to predict the device behavior under process modifications essential to meet circuit performance requirements as the devices are scaled. Hence such approaches cannot be used for predictive modeling and/or to aid the semiconductor industry in designing manufacturing processes to overcome the relevant reliability problems. The presence of novel physical mechanisms such as short-channel effects, non-local carrier heating, and quantum effects in aggressively scaled devices further complicates the modeling process and requires the use of more comprehensive modeling techniques for such structures.

In view of these limitations of the conventional modeling techniques, the semiconductor industry is witnessing a rapid evolution of modeling approaches based on information extracted from a hierarchy of simulation tools (Fig. 2). *Ab initio* and Molecular-Dynamics (MD) simulation

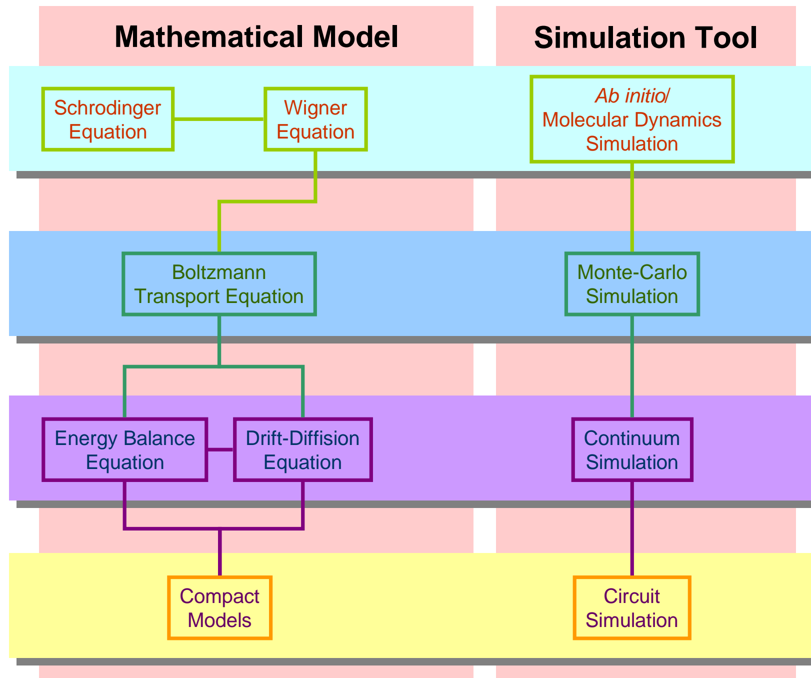


Figure 2: Hierarchy of simulation tools available for modeling fundamental physical mechanisms in semiconductor devices.

tools provide information about the most basic physical processes in the materials being modeled by solving an equivalent of the Schrodinger equation (for example, the Wigner Equation in the case for semiconductors [6]). The results of these simulations provide parameters for particle interactions that are typically modeled using Monte-Carlo (MC) simulations. At this point, several quantum effects are typically neglected resulting in the solution of the equivalent Boltzmann Transport Equation (BTE). Simulation of semiconductor devices using MC simulations can be prohibitively time consuming for routine simulation. In cases where the field and material properties are varying slowly over the domain being simulated, certain averaging techniques can be used to obtain simplified models for use in continuum device simulations. In particular, the balance equations for carrier flux and carrier energies can be obtained from the BTE by integrating over the momentum subspace. Numerical device simulation based on Drift-Diffusion (DD) equations thus obtained has become a standard practice in studying the physical mechanisms involved in the device operation and for performance optimization using Technology Computer Aided Design (TCAD) [7, 8, 9]. Finally, the device simulation tools provide parameters essential for circuit

level design of the ICs.

HC degradation mechanisms, in particular the processes active in dielectric regions of the devices, have not been traditionally modeled by device simulators. The 2002 Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) [10] clearly states the need to develop such modeling tools to meet the near and long term technological needs of the semiconductor industry. The modeling of these processes in continuum simulation tools is the primary focus of the work presented here. We have developed a simulation tool aimed at predictive modeling of HC degradation phenomena in aggressively scaled MOSFETs. The transport of HCs injected into the oxides has been modeled along with the interaction of the carriers with defects in the oxide that result in instabilities in the devices.

Thesis Outline

The current understanding of the basic physical mechanisms that result in HC injection and subsequent device degradation is presented in Chapter II. This chapter highlights the processes that need to be modeled in device simulation tools in order to be applicable to predictive simulation of HC phenomena in current and future generation MOSFETs.

In Chapter III we describe the development of our modeling tool along with the choices and assumptions that were made to model the physical mechanism described in Chapter II in a practical simulation application. The details of the numerical model developed as a result of this analysis are presented.

The results of the application of these simulation tools to HC degradation in p- and n-channel MOSFET are presented in Chapters IV.

A list of symbols used in the equations throughout this document can be found Chapter while a list of acronyms used throughout the document can be found in Chapter .

CHAPTER II

BASIC PHYSICAL MECHANISMS

Introduction

The basic physical mechanism that result in HC reliability problems in MOSFETs are (Fig. 3) :

1. Under the influence of high lateral fields in short-channel MOSFETs, carriers in the channel and pinch-off regions of the transistor reach non-equilibrium energy distributions. The generation of these hot-carriers is the primary source of several reliability problems.

2. The energetic carriers lose their energy via impact-ionization resulting in high substrate currents consisting of impact-generated majority carriers. The impact-generated carriers also serve as candidate hot-carriers for injection into the oxide films surrounding the silicon substrate. The impact-generated carriers can manipulate the electric field distribution in the substrate initiating latch-up. Bremsstrahlung from high-energy electrons or electron-hole recombination can give rise to photons, which can then be re-absorbed elsewhere in the substrate. This could, for example, cause refresh degradation in Dynamic Random Access Memories (DRAM).

3. Hot-carriers can acquire sufficient energy to surmount the energy barrier at the Si-SiO_2 interface or tunnel into the oxide.

4. Injected hot-carriers interact with the oxide and "somehow" use their energy to generate defects in the oxide and its interfaces.

5. The presence of defects in the oxide induces device parameter shifts. This instability in device parameters appears as a major hurdle in the reliable long term operation of these devices.

The degradation of MOSFETs due to HC injection has been the subject of numerous studies in the past [11, 12, 13, 14, 15, 16, 17]. In particular, the physical processes occurring in the silicon

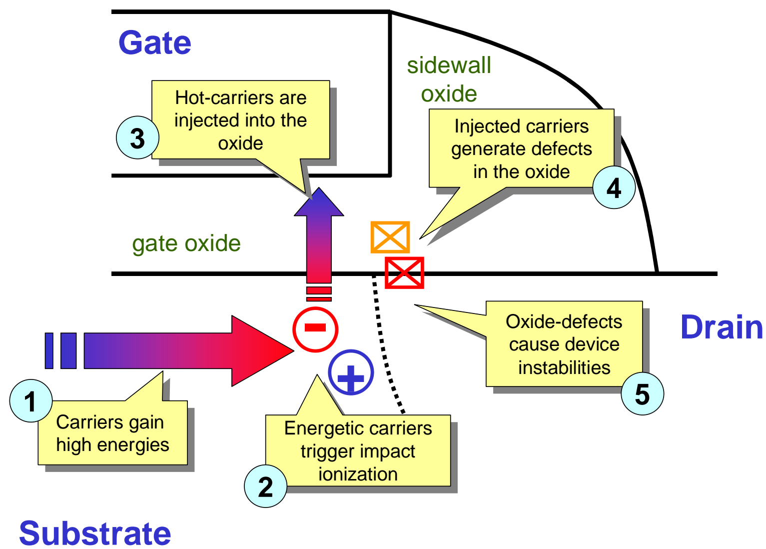


Figure 3: The sequence of physical mechanisms that contribute to HC-induced device degradation in MOS transistors. This figure shows the pinch-off region near the drain-substrate junction of a typical n-channel MOSFET.

substrate that result in the generation of energetic carriers have been extensively studied. These carrier-heating mechanisms are primarily dependent on the carrier and electric field distributions in the silicon substrate and are considered to be fairly well understood with comprehensive models available in the literature. Similarly, the nature of processes that result in the injection of energetic carriers from silicon substrate into the oxide have been also been studied and modeled [17, 18, 19, 20, 21, 22, 23, 24, 25]. The interactions between carriers with species in the oxide and at the Si-SiO_2 that result in defect formation have been studied under a variety of stress conditions, such as hot-carrier injection, high-field injection, optical injection, and radiation exposure, in the past [21, 26, 27, 28, 29, 30, 31]. However, these interactions have not traditionally been modeled numerically in hot-carrier literature. As part of this work, the current understanding of these interactions has been used to construct a set of numerical models that can be used in continuum device simulation tools. In this chapter we present a qualitative discussion of the above physical processes that play a role in HC injection and resulting device instabilities in modern MOSFETs. The numerical models for each of these physical processes will be described in Chapter III.

Carrier Heating in Silicon

During operation in a circuit, high fields appear in the silicon substrate near the drain-substrate junction due to the formation of a pinch-off region [32]. In particular, the lateral electric field exhibits a sharp peak in this region (Fig. 4). Under high drain biases, carriers traversing this high field region can exhibit non-equilibrium energy distributions[33]. As a consequence, the concentration of energetic carriers available for injection into the oxide is a strong function of the electric field distribution in the silicon substrate. Thus, the calculation of accurate electric field distributions in silicon is a primary requirement for modeling HC degradation.

Several models for hot-carrier energy distribution have been based on the assumption of a direct relationship between the average carrier energy and the local electric field:

$$\mathcal{E}_{\text{avg}} = qEl_{mf}. \tag{1}$$

The limitations of this assumption were recognized when hot-carrier injection was observed in MOSFETs even at low biases. According to the above relationship, the maximum energy obtained by a carrier cannot exceed the energy gain across the potential difference between the

drain and source electrodes of the device. As the potential barrier for electrons at the Si–SiO_2 interface is approximately 3.2 eV, no carrier injection should be observed when V_{DS} is below 3.2 V according to this model. However, significant substrate and gate currents have been observed at drain biases well below this value[34, 35].

In long channel devices, the magnitude of the electric field peak is relatively small as compared to shorter length devices. Furthermore, the length of the pinch-off region, which is a function of both the channel length and the oxide thickness [36], is also larger. As a result, long channel devices have slowly varying electric fields along the channel with a relatively lower electric field peak (Fig. 4). In such cases, the channel carriers remain in thermal equilibrium with the lattice and the average carrier energies can be calculated from the local electric field values. As devices are scaled using non-constant-field scaling, disproportionately large and highly localized electric field peaks can appear near the pinch-off region resulting in carrier energies significantly above their values under thermal equilibrium. Furthermore, Monte-Carlo simulations show that the carrier energy peak is located past the electric field peak in the direction of carrier flow along the channel under such conditions[33, 37]. In other words, the location of maximum carrier energy is separated from the location of maximum electric field. Hence, the carrier energy distribution is not a function of the *local* electric field but depends on the electric field distributions that the carriers have to traverse in order to gain high energies [38]. In general, such non-local effects have not been included in deriving models for hot-carrier degradation in MOS transistors as they were expected to be of relatively low significance in long channel transistors. However, these effects cannot be neglected in modern sub-micron devices. Such non-local dependence of carrier energy on the electric field distribution needs to be included in simulation tools to accurately model the carrier heating processes [33, 39, 40, 5, 41] especially at low biases. Besides the non-local dependence of carrier energies on the electric field distribution, high-field effects such as velocity overshoot and mobility degradation also become significant in short-channel devices [4, 42, 32].

Impact-Ionization

When carriers in silicon gain energies above a certain threshold (approximately 3.6 eV for electrons and 5.0 eV for holes in silicon), they can generate electron-hole pairs through impact-ionization [32]. An electron in the conduction band, for example, can excite an electron from the

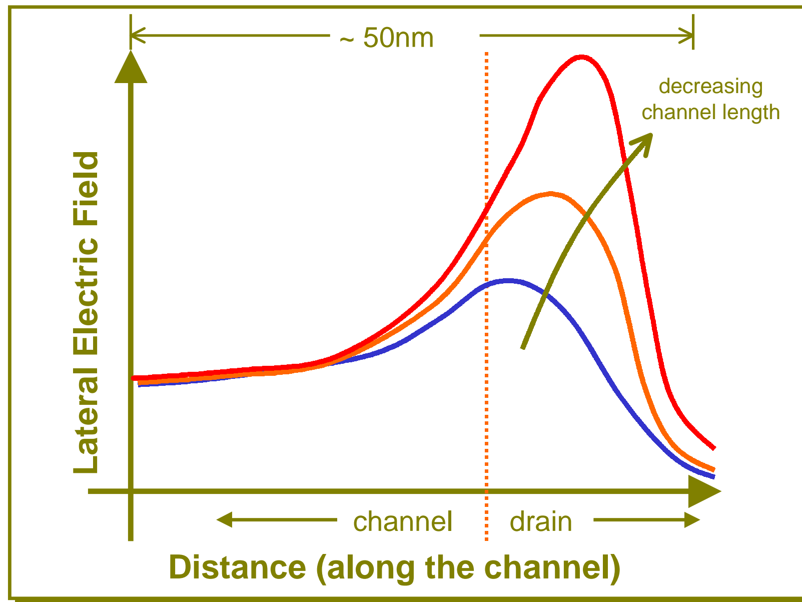


Figure 4: The maximum lateral electric field at the Si-SiO_2 interface along the channel in MOS transistors with decreasing channel lengths.

valence band resulting in two electrons in the conduction band and a hole in the valence band (Fig. 5). Both the total energy and momentum are conserved during this process.

In general, the impact ionization process itself has no dependence on the electric field. In other words, as long as the electron in Fig. 5 has enough energy it can trigger impact ionization. In continuum device simulations and analytical calculations related to hot-carrier degradation (see discussion on page 8) the carrier energy is usually expressed as a function of the local electric field. This relation is usually extended to express the impact ionization rate as a function of the electric field. However, when non-local carrier heating is in effect, these models are inapplicable for the same reasons as discussed on page 8.

Most of the majority carriers generated through impact-ionization are collected at the substrate electrode and hence the substrate current serves as a good measure of the impact-ionization rate in MOSFETs. Furthermore, electrons and holes generated due to impact-ionization in the high field region of the device can themselves gain large enough energies to be injected into the gate oxide. In other words, the generation of electron-hole pairs due to impact-ionization provides

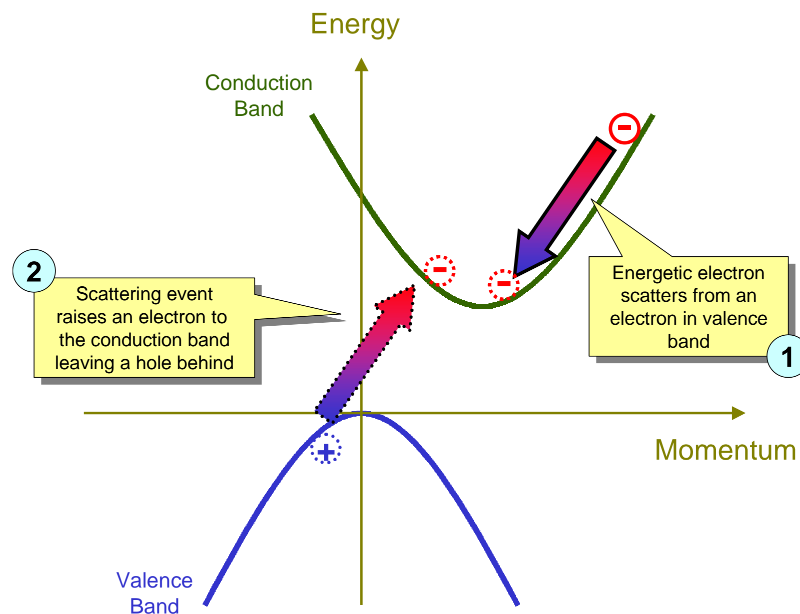


Figure 5: An illustration of the impact ionization process in silicon.

an additional source of hot-carriers besides the inversion layer. In fact, in n-channel MOSFETs these impact-generated carriers are responsible for the majority of HC degradation.

Carrier Injection into the Oxide

The carriers near the Si–SiO_2 interface in the silicon substrate of a MOSFET have to overcome an energy barrier in order to enter the oxide. Silicon dioxide has an electron affinity of 0.9 eV and a bandgap of approximately 9.0 eV. Similarly, silicon has an electron affinity of 4.05 eV and a bandgap of 1.12 eV. The band alignment at the Si–SiO_2 interface thus results in an energy barrier of about 3.1 eV for electrons and 4.8 eV for holes as shown in Fig. 6. As a result of the large difference between the energy barriers for electrons and holes, under similar conditions, electrons will be injected into SiO_2 in much larger quantities than holes. Due to these differences between electron and hole energy barriers, the hot-carrier degradation mechanisms are considerably different in n- and p-channel MOSFETs. These differences are described in detail later in the document (see page 15).

A charge carrier in silicon in the vicinity of the Si–SiO_2 interface induces an opposite charge

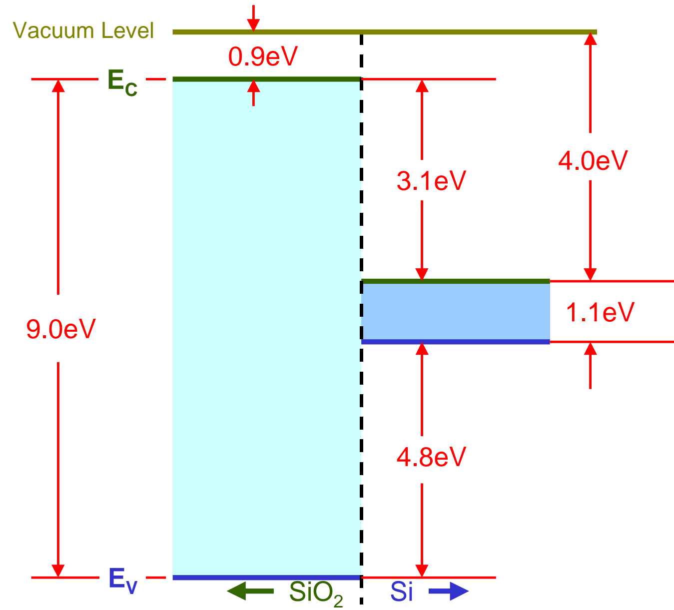


Figure 6: A band diagram showing the band alignment at the Si–SiO_2 interface and the resulting energy barriers for injection of electrons and holes from Si into SiO_2.

in the oxide. If an external electric field is applied across the oxide, this "image charge" results in the lowering of the energy barrier usually referred to as the Schottky barrier lowering (Fig. 7).

Carriers that have energies higher than the local energy barrier at the Si–SiO_2 interface have a high probability of getting injected into the oxide. The interactions of an energetic electron in silicon near the Si–SiO_2 interface with the potential distribution in the oxide are illustrated in Fig. 8. The carriers that cross the interface encounter a potential well between the interface and the location of peak oxide potential, x_m, as shown in the figure. Scattering events in this potential well can emit the carriers back into the silicon substrate – the event marked "Reflection" in Fig. 8. In spite of suffering energy loss due to scattering events, the carriers have a finite probability of injection into the oxide by tunneling across the triangular potential. Finally, carriers that do not suffer any collisions in the potential well make it over the energy barrier and enter the oxide – the event marked "Transmission" in Fig. 8 represents such processes. Clearly, the calculation of the Schottky barrier lowering and the probabilities of transmission, reflection, and tunneling as a function of the barrier height is essential for modeling hot-carrier injection fluxes.

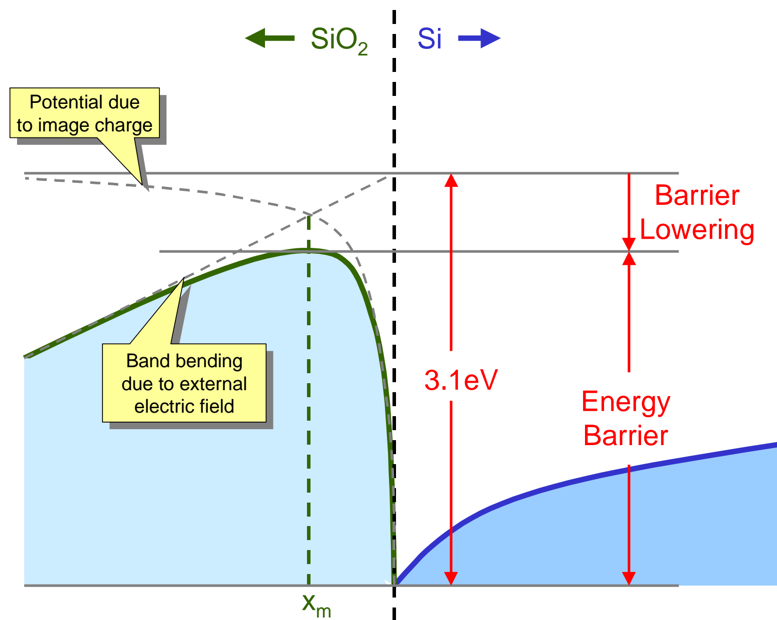


Figure 7: A schematic diagram showing the silicon and oxide conduction bands in the presence of a potential across the oxide. Electrons in the silicon region induce an image charge in the oxide that results in the lowering of the energy barrier for injection of electron from silicon into the oxide.

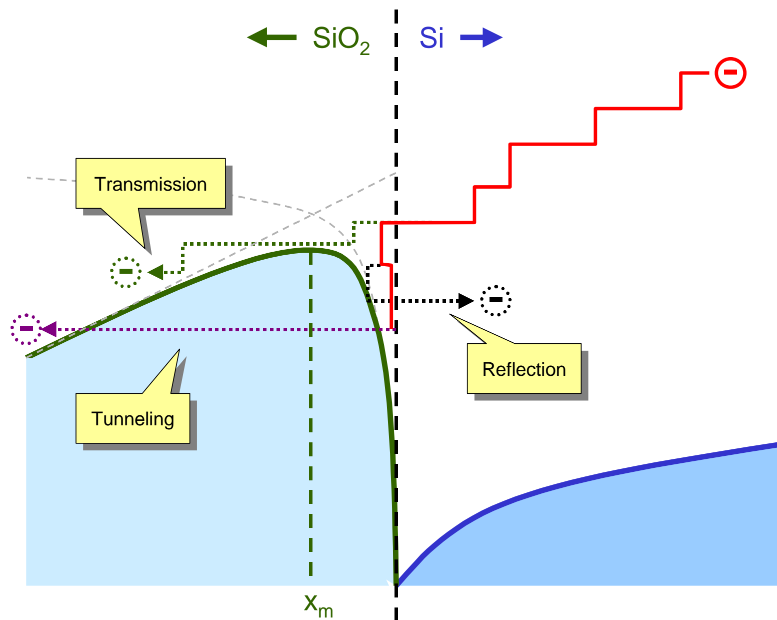


Figure 8: A schematic diagram of Si and SiO_2 conduction bands illustrating some of the mechanisms that can result in carrier injection or reflection as high energy carrier approach the Si–SiO_2 interface.

The surface potential along the Si-SiO_2 interface and hence the potential drop across the gate oxide changes as we move from the source to the drain. This variation in surface potential implies a variation in the Schottky barrier lowering along the channel. The carrier injection processes are, thus, a complex function of the applied biases, position along the channel, and the type of carrier being injected among other factors.

A simple example of this relationship can be observed in n-channel devices biased at a high drain bias and a low gate bias (less than or equal to the threshold voltage). Under this bias condition, the transverse electric field strongly favors hole injection as compared to electron injection near the pinch-off region. The electric field in the oxide near the drain results in Schottky barrier lowering for holes (but not for electrons). Furthermore, holes deeper in the silicon substrate perceive a further reduced barrier (Fig. 9) [43].

These intricate dependencies between various factors affecting the extent and location of carrier injection cannot be modeled analytically in short-channel devices. Device simulation tools for

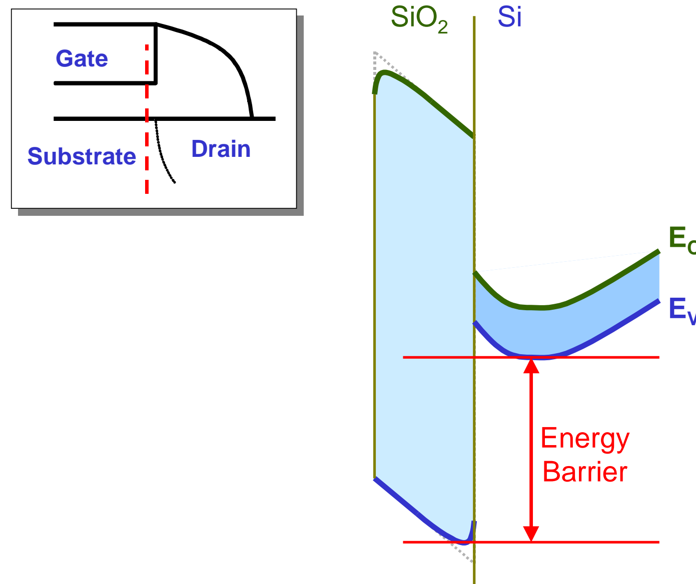


Figure 9: A combination of Schottky barrier lowering and band bending in the silicon substrate results in enhanced hole injection in nMOS devices under low gate biases.

HC degradation should include models for such dependencies to obtain an accurate understanding of the carrier injection phenomenon. Deep sub-micron devices with thin gate oxides that are subjected to high gate biases can exhibit other injection mechanisms such as Fowler-Nordheim tunneling [44, 19, 45], direct tunneling, and trap-assisted tunneling (Fig. 10). These injection mechanisms may need to be included while modeling the carrier injection phenomena in ultra-thin gate oxides [46].

Oxide Degradation

Energetic carriers that get injected into the oxide have been known to result in instabilities in device characteristics in both n- and p-channel MOSFETs through the generation of electrically active defects in the oxide and at the Si–SiO_2 interface. In the most common of these processes, the energy gained by the carriers in the high field regions of the silicon substrate is utilized to break bonds associated with extrinsic and/or intrinsic defects in the oxide. The subsequent rearrangement of the atomic structure of the oxide is responsible for the device instabilities observed during hot-carrier injection.

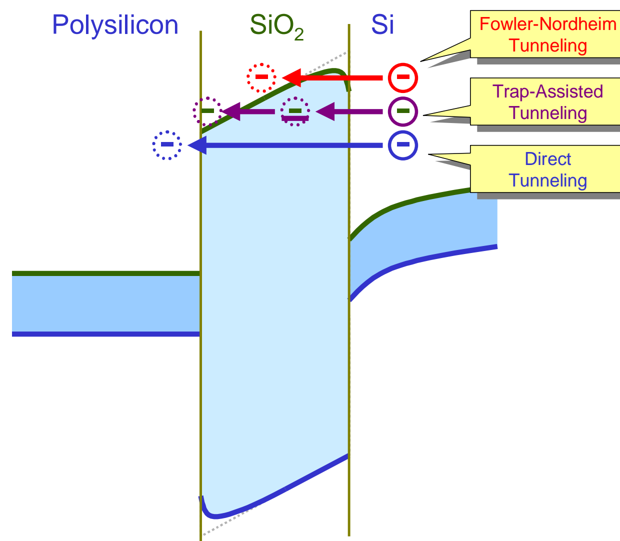


Figure 10: Various tunneling mechanism that result in injection of carriers from the silicon substrate into or across the gate oxide.

Apart from hot-carrier injection, other stress conditions can also result in the introduction of mobile charge carriers in SiO_2. One of the earliest experiments in characterizing the effects of carrier injection on MOS structures involved the injection of photo-generated carriers from the silicon substrate into the gate oxide. In these experiments, electron-hole pairs are generated by illuminating the silicon substrate with an intense low-energy-photon source (also known through the more technical term – "bulb") and accelerated toward the oxide by applying a large substrate bias. In the case of an p-type substrate, for example, a large negative substrate bias is used to accelerate the photo-generated electrons toward the Si–SiO_2 interface. The electrons approach the interface with energies exceeding the interfacial energy barrier and are injected into the oxide (Fig. 11). This process is usually referred to as Substrate Hot Electron Injection (SHEI). Similarly, ionizing radiation exposure can be used to generate electron-hole pairs directly in the oxide.

The SHEI and ionizing radiation exposure experiments result in laterally uniform populations of mobile carriers in the gate oxide of the MOS structure. Hence, the resulting degradation in the oxide is also uniform along the channel of the device. This results in simple correlations

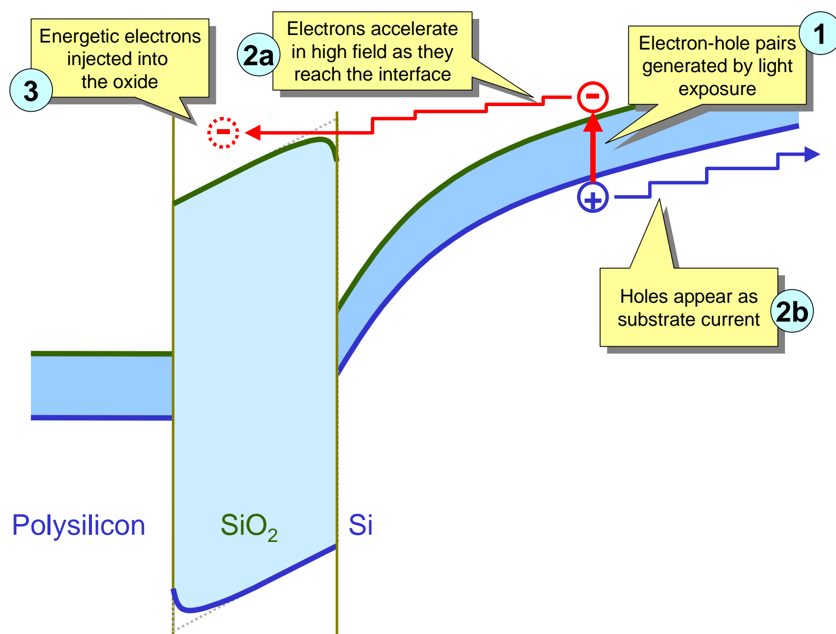


Figure 11: Photoinjection of hot-carriers from the silicon substrate into the oxide.

between the shifts in device characteristics and the population of defects formed in the oxide and at the Si–SiO_2 interface due to the presence of mobile carriers in the oxide. On the other hand, due to the localized nature of carrier injection and oxide degradation during HC injection, these correlations cannot be used to analyze HC-induced device instabilities. For example, a uniform distribution of defects in the gate oxide of a MOSFET can be easily translated into an equivalent shift in the threshold voltage of the device in SHEI and ionizing radiation experiments; such a relation does not necessarily exist for non-uniform damage caused by HC-injection. Nevertheless, the insights gained into the defect formation processes in SiO_2 during SHEI and ionizing radiation experiments can still be applied to the HC-degradation of MOS transistors. We turn to several of these studies during the model development process described in Chapter III.

During SHEI, ionizing radiation, and HC-injection experiments, two types of defect formation processes are observed to be responsible for the majority of the device parameter shifts. As the carriers transport across the oxide, their interactions with certain atomic structures in oxide result in the formation of immobile charged species with the simultaneous annihilation of the associated carriers – a process referred to as "charge trapping" as the charge associated with a carrier is converted into an immobile species with equivalent charge [47, 48, 49, 50, 51]. These trapped

charges can exist in the oxide for extended periods of time and their presence in the oxide affects the current flow in the MOSFET channel [52, 53]. Furthermore, the accumulation of these trapped charges over time is also associated with the breakdown of the dielectric properties of the oxide.

A multitude of atomic structures have been associated with charge trapping sites in SiO_2. The investigation of the effects of ionizing radiation on MOSFETs has shown that the primary defect associated with hole trapping in SiO_2 films is the Bridging Oxygen Vacancy (BOV) [54, 55, 28, 56]. This defect is observed in SiO_2 films fabricated using a variety of techniques used for semiconductor manufacturing. A hole trapping event at a BOV is illustrated in Fig. 12. The BOV is characterized by a missing oxygen atom between two silicon atoms in the SiO_2 structure. This results in a relatively weak bond between the two silicon atoms. A free hole near this structure can result in the breaking of this weak bond producing a positively charged structures called the E′-center.

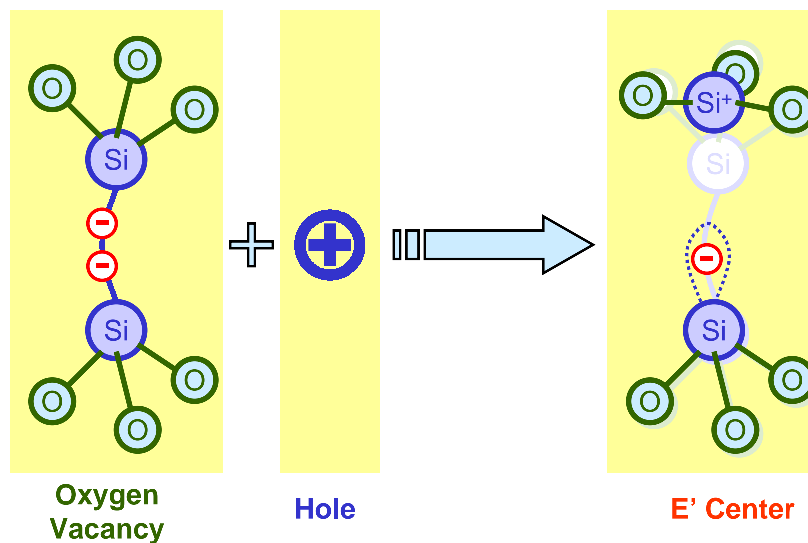


Figure 12: The oxygen vacancy has been established as the primary hole trapping site in SiO_2 films associated with semiconductor devices.

Several other hole and electron trapping mechanisms have been suggested in the literature.

Among them the trapping events that involve hydrogen-related defects are of particular interest. It has been suggested that hole-trapping at these defects can release mobile hydrogen in the oxide. The presence and transport of mobile hydrogen can trigger other defect formation processes as discussed below.

Interface traps are another type of defect associated with device degradation due to the above stresses at the Si–SiO_2 interface [57, 58, 31, 59]. These interfacial defects introduce energy states, usually referred to as "interface states", in the Si bandgap at the interface. The occupancy of these interface states depends on the local surface potential. During device operation, they get populated through the removal of minority carriers from the inversion layer resulting in a bias-dependent shift in the drain current of the MOSFET.

The atomic structure associated with interface traps in MOSFETs is believed to be a silicon dangling bond site at the interface known as the P_b-center. In fully processed MOSFETs, the dangling bonds are passivated with hydrogen and are expected to be electrically inactive. Hydrogen released by carrier trapping in the oxide, as mentioned above, can migrate to the Si-SiO_2 interface and react with the passivated dangling bonds (P_b-H). This reaction results in depassivation of the dangling bonds producing electrically active P_b-centers (Fig. 13). Besides the depassivation of P_b-H sites by hydrogen released in SiO_2, several other interface trap generation mechanisms have been suggested. Holes trapped in the vicinity of the Si-SiO_2 interface have been associated with interface trap generation in one such model [60, 61]. Similarly, channel hot-carriers have been observed to result directly in depassivation of P_b-H sites resulting in interface traps.

Hot-carrier degradation studies typically do not attempt to model the defect formation processes in the oxide that result in charge trapping or interface trap generation. In general, this requires the modeling of electron and hole transport in the oxide as well as their interactions with various defects mentioned above. Due to the amorphous nature of SiO_2 and the presence of a wide bandgap, carrier transport mechanisms in SiO_2 are significantly different from those in semiconductors. Furthermore, the transport of electrons and holes in the oxide can release other mobile species, such as atomic hydrogen or H^+, whose transport may also need to be modeled.

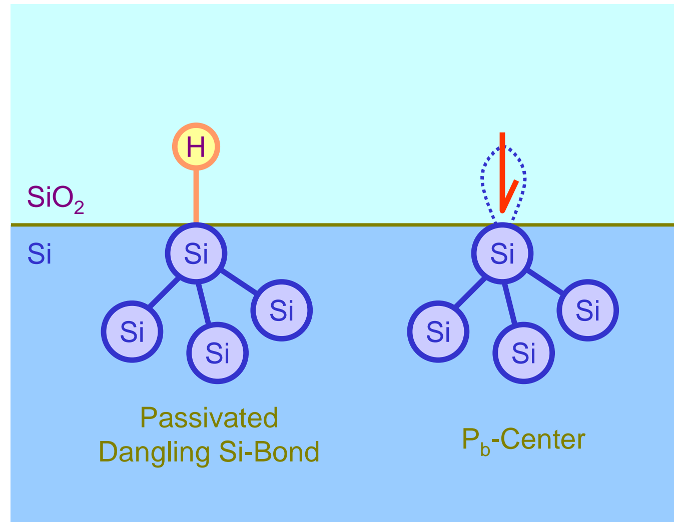


Figure 13: Atomic structure of defect structures at the interface that are primarily responsible for interface trap generation.

Device Parameter Shift

The presence of trapped charge and interface traps in the device due to HC injection directly affects the device operation. The amount of damage caused by hot-carriers is typically measured in terms of the shift in certain device-level parameters such as the threshold voltage, subthreshold slope, transconductance, and drain current obtained by performing device characterization measurements before and after HC injection. Similar techniques are also used to characterize the oxide damage resulting from other stress conditions such as high oxide fields, Fowler-Nordheim injection, and radiation exposure. However, the HC-induced device degradation differs from most of these stress conditions in the fact that the damage caused during HC injection is highly localized. On the other hand, damage caused by exposure to ionizing radiation, for example, occurs relatively uniformly throughout the oxide. The localized nature of damage caused by HC injection implies that the interpretation of shift in device parameters under such stress conditions is significantly different from cases when the damage is uniform. For example, a change in the subthreshold slope of the device is typically associated with a change in the density of interface traps if the damage is uniform. However, similar shifts in subthreshold slope can also be ob-

served through a localized increase in trapped charge density in the oxide near the drain region. Even though advanced characterization techniques such as charge pumping measurements provide better understanding of the nature of HC induced device degradation, it is often essential to utilize device simulation tools along with the characterization experiments to gain better insight into the physical processes responsible for hot-carrier induced parameter shifts. In order to aid this process, device simulation tools must be able to model the influence of hot-carrier induced trapped charge and interface traps on the device characteristics.

Summary

In this chapter, we discussed the qualitative nature of the basic physical mechanisms responsible for hot-carrier-induced degradation in MOSFETs. The physical mechanisms described here represent effects that are active during the normal operation of such devices and result in shifts in experimentally measurable device parameters such as threshold voltage and linear transconductance. In the next chapter, we present mathematical models for each of these physical mechanisms that can be used for numerical simulation of hot-carrier degradation in MOSFETs.

CHAPTER III

MATHEMATICAL MODELS

The qualitative nature of the basic physical process involved in the hot-carrier-induced device degradation has been discussed in Chapter II. In this chapter we present a discussion of quantitative modeling techniques, when available, for each of these physical processes. Furthermore, we discuss practical model choices that need to be made in order to simulate hot-carrier degradation in deep sub-micron devices. At present, device simulation tools lack quantitative models for oxide and interfacial defect generation due to carriers injected into the oxide. The development of such models has been the primary focus of the research presented here. We also develop a set of first order models for these processes so that a TCAD-based simulation toolset can be developed for predictive hot-carrier reliability simulation.

Carrier Transport and Heating in Silicon

Numerical device simulations are extensively used to study carrier transport in semiconductor devices and allow detailed analysis of the mechanisms involved in device operations. A hierarchy of approaches are available for numerical simulation of carrier transport phenomena in semiconductor devices starting from quantum mechanics based approaches to approaches based on balance equations [9] as shown in Fig. 2 on page 4.

In the absence of significant quantum effects and under relatively slow space and time variations in potential, the transport of carriers in semiconductors can be expressed through the BTE [62, 42]. The BTE is formulated in terms of the carrier distribution function, $f(\mathbf{x},\mathbf{k},t)$, which represents the probability of finding a carrier at location $\mathbf{x}$ with momentum $\mathbf{k}$ at time t. The average values of physical properties associated with carrier transport in semiconductors at any given location in space can be obtained by averaging them over momentum space by taking moments of the distribution function:

$$n(\mathbf{x},t) = \int f(\mathbf{x},\mathbf{k},t)d^3\mathbf{k} \quad \text{(Electron Density)} \tag{2}$$

$$n(\mathbf{x},t)\mathbf{v_n}(\mathbf{x},t) = \int v_n(\mathbf{x},\mathbf{k},t)f(\mathbf{x},\mathbf{k},t)d^3\mathbf{k} \quad \text{(Velocity)} \tag{3}$$

$$\mathcal{E}_n(\mathbf{x},t) = \frac{m_n^*}{2}\int v_n^2(\mathbf{x},\mathbf{k},t)f(\mathbf{x},\mathbf{k},t)d^3\mathbf{k} \quad \text{(Energy)}. \tag{4}$$

The solution of the BTE along with Maxwell's field equations allows one to numerically simulate the properties of semiconductor devices. However, the direct solution of the BTE in any but the simplest of semiconductor structures can be prohibitively time consuming. Hence, several approximate methods have been derived from the BTE. In particular, the balance equations obtained by taking moments of the BTE present a set of differential equations describing properties such as average carrier density, average momentum, and average carrier energy. These equations can be solved over fairly complex device structures and provide sufficiently accurate description of carrier transport in most applications.

In the majority of simulation studies related to MOS transistors, the effects of magnetic fields can be neglected and the electric field distribution is usually obtained by solving the Poisson's equation:

$$\boxed{\nabla \cdot (\varepsilon_{Si}\mathbf{E}) = q\left(p - n + N_D^+ - N_A^-\right) \quad \text{(Poisson's Equation)}}. \tag{5}$$

As shown in Eq. 2, the zeroth order moment of the electron distribution function gives the average electron density. A balance equation for the average electron density over the simulation domain can be obtained by taking the corresponding moment of the BTE [42, 6, 62]. This procedure results in the continuity equations for electrons and holes that are the simplest and most popular equations for simulation of carrier transport in semiconductor devices under low electric fields with no rapidly varying spatial non-homogeneities in the device structure.

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\nabla \cdot \mathbf{J_n} \quad \text{(Electron Continuity)} \tag{6}$$

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\nabla \cdot \mathbf{J_p} \quad \text{(Hole Continuity)} \tag{7}$$

The carrier current densities, $\mathbf{J_n}$ and $\mathbf{J_p}$, are obtained from the corresponding drift-diffusion equations given by:

$$\mathbf{J_n} = q\mu_n n\mathbf{E} + qD_n \nabla n \quad \text{(Electron Drift-Diffusion)} \tag{8}$$

$$\mathbf{J_p} = q\mu_p p\mathbf{E} - qD_p \nabla p \quad \text{(Hole Drift-Diffusion)}. \tag{9}$$

Under thermal equilibrium in non-degenerate semiconductors, the mobilities are related to the diffusion constants through the Einstein relationships:

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{k_B T_L}{q} \quad \text{(Einstein Relationship)}. \tag{10}$$

The quantities derived from drift-diffusion equations such as carrier energies and velocities are obtained by averaging over the local carrier distribution and electric fields. Furthermore, the drift-diffusion-based approaches use the Maxwell-Boltzmann (MB) distribution for the carrier energies assuming that the carriers are in thermal equilibrium with the lattice. Based on results of Monte Carlo simulation of carrier heating processes in silicon [63], both of these approaches have been shown to be inadequate while modeling phenomena where high energy carriers are involved and the electric field variations are highly localized. In particular, in rapidly varying electric fields the carrier energies cannot be expressed as functions of the local electric field. Similarly, the carrier energy distribution deviates significantly from the MB distribution under such conditions (Fig. 14). In order to improve the accuracy of such simulations we need to use more precise approaches from the simulation hierarchy of Fig. 2.

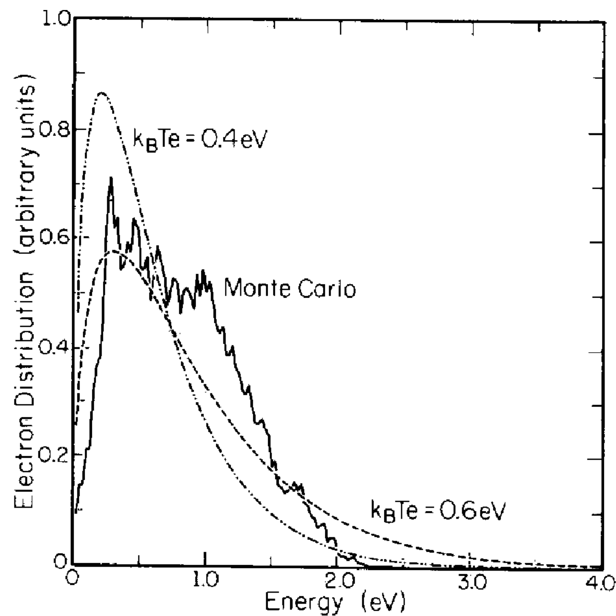


Figure 14: Comparison of hot-electron energy distribution near the drain region of an n-channel MOSFET obtained by Monte Carlo simulation with Maxwell-Boltzmann distributions at two different electron temperatures.

As mentioned before, the direct solution of Boltzmann's transport equation is prohibitively expensive and is not feasible for everyday device simulation. In view of currently available compu-

tational facilities, the energy transport based approach is most practical for routine simulations as numerical solution procedures developed for solving drift-diffusion based problems can be easily extended to solve energy balance equations. The second-order moment of the steady-state BTE is used to obtain the balance equation for the average carrier energies using a procedure similar to the one used for obtaining the carrier continuity equations (Eqs. 6 and 7) :

$$\nabla \cdot \mathbf{S_n} = \mathbf{E} \cdot \mathbf{J_n} - \frac{3}{2}\frac{nk_B}{\tau_n}(T_n - T_L) - \frac{3}{2}k_B T_n(G_n - U_n) \quad \text{(Electron Energy Balance)} \quad (11)$$

$$\nabla \cdot \mathbf{S_p} = \mathbf{E} \cdot \mathbf{J_p} - \frac{3}{2}\frac{pk_B}{\tau_p}(T_p - T_L) - \frac{3}{2}k_B T_p(G_p - U_p) \quad \text{(Hole Energy Balance).} \quad (12)$$

The carrier temperatures, T_n and T_p, are used here to simplify the expressions and are directly proportional to the average carrier energies:

$$\mathcal{E}_n = \frac{3}{2}\frac{k_B T_n}{q} \quad (13)$$

$$\mathcal{E}_p = \frac{3}{2}\frac{k_B T_p}{q}. \quad (14)$$

The electron and hole energy fluxes are also expressed in terms of the average electron and hole temperatures as:

$$\mathbf{S_n} = -\frac{5}{2}\frac{k_B T_n}{q}\left(\mathbf{J_n} + n\mu_n k_B \nabla T_n\right) \quad (15)$$

$$\mathbf{S_p} = -\frac{5}{2}\frac{k_B T_p}{q}\left(-\mathbf{J_p} + p\mu_p k_B \nabla T_p\right) \quad (16)$$

with modified drift-diffusion equations for electron and hole current densities that include terms accounting for diffusion due to gradients in carrier temperatures:

$$\mathbf{J_n} = q\mu_n n\mathbf{E} + qD_n \nabla n + q\mathcal{S}_n \nabla T_n \quad (17)$$

$$\mathbf{J_p} = q\mu_p p\mathbf{E} - qD_p \nabla p - q\mathcal{S}_p \nabla T_p. \quad (18)$$

The Soret coefficients, $\mathcal{S}_n$ and $\mathcal{S}_p$ are give by:

$$\mathcal{S}_n = \frac{k_B n\mu_n}{q} \quad (19)$$

$$\mathcal{S}_p = \frac{k_B p\mu_p}{q}. \quad (20)$$

The energy balance equations presented above are derived using the MB distribution for carrier energies. Furthermore, the energy relaxation times for electrons and holes are obtained by fitting experimental data or from MC simulations. The deviations from the MB distribution can be included in these equations through the use of an extra set of coefficients. However, a more rigorous analysis can only be performed with the aid of MC simulations as these coefficients act as fitting parameters. In this work we focus on the degradation processes taking place in the oxide regions of the MOS transistors and assume that the average energies obtained by solving the energy balance equations provide sufficiently accurate estimates of carrier energies when combined with the MB distribution.

Impact-Ionization

Under high electric fields, the generation of electron-hole pairs due to impact ionization is given by [32]:

$$G_{impact} = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q}. \tag{21}$$

The electron and hole ionization rates, α_n and α_p are defined as the number of electron-hole pairs generated by the carriers per unit distance traveled:

$$\alpha_n = \frac{1}{nv_n} \int_{BS} f(\mathbf{x}, \mathbf{k}, t) R_{ii,n} d^3\mathbf{k}. \tag{22}$$

The above integral should be carried out over the complete band structure of the semiconductor. As expected, the impact ionization rate is a function of the carrier energy. In drift-diffusion based approaches, the values of the ionization rates are calculated based on the local electric field using empirical expressions such as [5] :

$$\alpha_n = a_n \exp\left(-\frac{b_n}{E}\right). \tag{23}$$

This gives correct results as long as the carriers are in equilibrium with the local electric field. This assumption, however, breaks down during hot-carrier injection when carriers are not in thermal equilibrium with the lattice [64, 65, 66, 67]. When the average carrier temperatures

are available by solving the energy balance equations, these ionization rates can be replaced by energy dependent models [68, 67] :

$$\alpha_{n,p}(T_{n,p}, T_L) = A_{n,p} \exp\left(-\frac{B_{n,p}}{\mathcal{E}_{n,p}}\right) \quad (24)$$

where, $A_{n,p}$ and $B_{n,p}$ are semi-empirical parameters obtained from experimental data or MC simulations. We have used this approach in our simulations. However, it should be mentioned here that even the approach based on average carrier energies is not universally applicable. In general, the coefficients used in Eq. 24 are not constant over the entire energy spectrum. In general, their use introduces empirical fitting parameters in the analysis that prevents the comprehensive understanding of the underlying physics. Higher level methods such as MC simulations are expected to become essential replacements to the use of these parameters in analysis of novel aggressively scaled devices in the future [46].

Carrier Injection

The simulation of carrier injection from silicon into SiO_2 has traditionally been modeled using the lucky-electron concept originally suggested by Shockley for modeling impact-ionization in semiconductors and later applied to hot-carrier injection [17, 22, 16]. The original lucky-electron-based modeling approach is not valid for modern short channel devices. However, several modified approaches exist that have used the lucky-electron concept as the basis to construct models that can be applied to aggressively scaled MOSFETs [41, 63, 69]. We utilize one such approach in our simulations.

The lucky-electron model provides an estimate of the probability that a carrier in silicon will be transmitted to the oxide by overcoming the local energy barrier at the Si–SiO_2 interface as shown in Fig. 8. The probability of this event is expressed as a combined probability of the following events – (1) the carrier is lucky enough to traverse several mean free paths in a large electric field to acquire energy greater than the local energy barrier and retains this energy after a scattering event that directs its momentum toward the interface, P_{1n} (2) after redirection of its momentum the carrier reaches the interface without any more collisions, P_{2n} and (3) the carrier does not suffer a collision in the potential well at the interface that can result in the reflection event shown in Fig. 8, P_{3n}.

$$P_{inj,n}(\mathbf{x}, t) = P_{1n} P_{2n} P_{3n}. \quad (25)$$

Each of these probabilities was originally related to the local electric field in the lucky-electron model. Furthermore, the carrier energy distribution was assumed to be Maxwellian. As mentioned earlier, both these assumptions break down for deep sub-micron devices. In our analysis, we have utilized the energy balance equations to account for non-local carrier heating processes. The use of energy balance equations provides us with an estimate for the average carrier energies in the devices. At this point, pure thermionic emission can be assumed to obtain an estimate for the carrier injection flux into the oxide along the Si-SiO_2 interface:

$$J_{inj,n} = -q \int_{\mathcal{E}_{B,n}}^{\infty} v_{\perp,n} f_n(\mathcal{E}) g_C(\mathcal{E}) d\mathcal{E}. \tag{26}$$

This accounts for the probability terms P_{1n} and P_{2n} in Eq. 25, but neglects the probability of collision in the potential well at the interface that can result in reflection of carriers back into the silicon substrate. This probability is given by[16]:

$$P_{3,n} = \exp\left(-\frac{1}{\lambda_{n,ox}} \sqrt{\frac{q}{16\pi\varepsilon_{ox} E_{\perp,ox}}}\right). \tag{27}$$

Including this term gives the hot-electron injection current at the interface as:

$$J_{inj,n} = -q \exp\left(-\frac{1}{\lambda_{n,ox}} \sqrt{\frac{q}{16\pi\varepsilon_{ox} E_{\perp,ox}}}\right) \int_{\mathcal{E}_{B,n}}^{\infty} v_{\perp,n} f_n(\mathcal{E}) g_C(\mathcal{E}) d\mathcal{E}. \tag{28}$$

The energy distribution of hot-carriers, $f_n(E)$, is know to be non-Maxwellian. Analysis based on a single non-parabolic conduction band suggests that the energy distribution of energetic carriers has a tail that follows the relationship:

$$f_n(\mathcal{E}) = nC_n(E) \exp\left(-\chi_n \frac{\mathcal{E}^3}{T_n^{1.5}}\right). \tag{29}$$

In the case of high energy electrons, a more accurate energy distribution can be obtained using a sum of two exponentials:

$$f_n(\mathcal{E}) = nC_n(E) \left[\exp\left(-\chi_{a,n} \frac{\mathcal{E}^3}{T_n^{1.5}}\right) + C_{0,n} \left(-\chi_{b,n} \frac{\mathcal{E}^3}{T_n^{1.5}}\right)\right]. \tag{30}$$

However, this increases the number of fitting parameters in the analysis. In our simulations we have utilized the approximation given by Eq. 29. The non-parabolic nature of the conduction band is captured using the following expression for the density of states:

$$g_n(\mathcal{E}) \propto \mathcal{E}^{\frac{5}{4}}. \tag{31}$$

Finally, the perpendicular component of the carrier velocity, $v_{\perp,n}$, is approximated as [63] :

$$v_{\perp,n} \propto \mathcal{E}^{\frac{1}{4}} \tag{32}$$

Thus, the expression for electron injection current becomes :

$$\boxed{J_{inj,n} = -qnC_{inj,n} \exp\left(-\frac{1}{\lambda_{n,ox}}\sqrt{\frac{q}{16\pi\varepsilon_{ox}E_{\perp,ox}}}\right)\int_{\mathcal{E}_{B,n}}^{\infty} \mathcal{E}^{\frac{3}{2}} \exp\left(-\chi_n \frac{\mathcal{E}^3}{T_n^{1.5}}\right) d\mathcal{E}}. \tag{33}$$

The fitting parameters for this equation are $C_{inj,n}$, $\lambda_{n,ox}$, and χ_n. A similar equation for hole injection can be readily obtained.

Oxide Degradation

As mentioned in the previous chapter, device simulation tools typically do not provide models for formation of defects in the oxide that are responsible for device instabilities. The aim of this work is to develop a set of such models for hot-carrier-induced defect generation in SiO_2. This requires one to simulate not only the injection but also the transport of the injected carriers in the oxide. Finally, the interactions of mobile carriers in the oxide with atomic structures in the oxide that result in carrier trapping and interface trap generation need to be modeled. This section describes the development of models for these mechanisms.

Charge Transport

As oxide films used in semiconductor applications consist of amorphous SiO_2, the transport properties of carriers in these films are expected to be considerably different from those in silicon. As mentioned in Chapter II, exposure to ionizing radiation can generate electron-hole pairs directly in the oxide films. It becomes essential to model the transport of carriers in the oxide under such conditions. Furthermore, the uniform distribution of defects formed during radiation exposure simplifies the analysis of experiments. As a result, radiation exposure studies have provided better insights into the transport properties in oxide films as compared to hot-carrier studies[70, 71, 72, 73].

Mobile electrons and holes in SiO_2 films exhibit significantly different effective mobilities – hole mobilities range from 10^{-11} to 10^{-4} $cm^2V^{-1}s^{-1}$ depending on electric field and temperature while electrons mobilities range from 20 to 40 $cm^2V^{-1}s^{-1}$ [74]. Furthermore, hole transport in SiO_2 is observed to be dispersive in nature characterized by a decrease in the effective mobility of holes

as a function of time. On the basis of these observations, the transport of holes through the oxide is believed to be due to mechanisms such as trap-mediated valence band conduction or hopping transport by tunneling between localized trap sites in the SiO_2 bandgapz [74]. The simulation of the dispersive nature of hole transport in SiO_2 has been typically accomplished using either Continuous Time Random Walk (CTRW) [75] or Multiple Trapping and Detrapping (MTD) models [76]. However, simplified drift-diffusion-based models have been successfully used to approximate carrier transport in thin SiO_2 films[77, 73, 71]. We have used this approach to simulate carrier transport in SiO_2.

The presence of mobile charge in the oxide requires the solution of the Poisson's equation :

$$\nabla \cdot (\varepsilon_{ox}\mathbf{E}) = q\,(p - n). \tag{34}$$

The transport of electrons and holes is assumed to be governed by the current continuity equations (Eqs. 6 and 7) with the corresponding current densities obtained from the drift-diffusion equations (Eqs. 8 and 9).

Charge Trapping

As mentioned in Chapter II, the oxygen vacancy (OV) structure is responsible for the majority of hole trapping in oxides used for semiconductor applications. The resulting positively charged entity is the E'-center. We have modeled the trapping of holes at oxygen vacancies and the resulting increase in density of E'-centers using the following rate equation:

$$\left.\frac{dp}{dt}\right|_{OV} = -\frac{d[E']}{dt} = \frac{d[OV]}{dt} \quad = \quad -\sigma_{p,OV}\frac{J_p}{q}\left([OV]_0 - [E']\right). \tag{35}$$

The trapping of electrons in the oxide can be handled in a similar fashion. The rate equation used for electron trapping in the oxide is:

$$\left.\frac{dn}{dt}\right|_{N_t} = -\frac{dn_t}{dt} = \frac{dN_t}{dt} \quad = \quad -\sigma_{n,t}\frac{J_n}{q}\left(N_{t,0} - n_t\right). \tag{36}$$

The presence of trapped charge in the oxide must be included in the Poisson's equation :

$$\nabla \cdot (\varepsilon_{ox}\mathbf{E}) = q\left(p + [E'] - n - n_t\right). \tag{37}$$

Similarly, the rate equations for electron and hole trapping appear in the corresponding continuity equations :

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J_n} - \left.\frac{dn}{dt}\right|_{N_t} \tag{38}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J_p} - \left.\frac{dp}{dt}\right|_{OV}. \tag{39}$$

In the simple first order model for electron and hole trapping presented above, secondary processes, such as annealing of trapped charges, compensation of trapped charges by mobile carries, and electric field dependence of capture cross-sections, have been neglected.

Interface Trap Generation

The interface trap generation rate in MOSFETs has been observed to be a strong function of the hydrogen content in the oxide[78, 18, 28, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90]. In a majority of these reports, mobile hydrogen is released in the oxide by transporting carriers and interface traps are generated as the hydrogen reaches the Si–SiO_2 interface. The nature of atomic structures that release the mobile hydrogen, the hydrogen-liberating interactions between these defects and mobile carriers, and the nature of the mobile hydrogen species released are a subject of active debate in the literature. The energy produced through the recombination of radiation-generated electron-hole pairs, interactions between neutral excitons and hydrogen related sites, and trapping of holes at hydrogen-containing defects are some of the mechanisms that have been proposed. However, most of these models are not appropriate for numerical modeling due to lack of specific details of the associated reactions and rate equations. One of the models that is suitable for this purpose is the three-step H^+ release process suggested by Mrstik and Rendell [88]. We have adapted this model through the construction of a set of rate equations based on the reactions suggested by Mrstik and Rendell. According to this model, atomic hydrogen is released in the oxide through the trapping of a mobile hole at a hydrogen-related site, D-H :

$$h^+ + \text{D-H} \rightarrow H_0 + D^+. \tag{R-1}$$

The density of D^+ sites generated during this process is expected to contribute less than 20% of the total observed trapped positive charge in the oxide during total-dose radiation exposure [88]. On the other hand, their contribution during hot-carrier degradation is not known. In our work,

we have included the complete contribution of the D^+ sites in the net trapped positive charge in the gate oxide.

The highly reactive nature of atomic hydrogen suggests that it will dimerize rapidly as it encounters other hydrogen atoms released in the vicinity :

$$H_0 \quad + \quad H_0 \quad \rightarrow \quad H_2. \tag{R-2}$$

Experimental observations of generation of interface traps in previously irradiated MOS systems during exposure to molecular hydrogen at room temperature suggest that the D^+ sites generated by hole trapping can crack molecular hydrogen and release H^+ :

$$H_2 \quad + \quad D^+ \quad \rightarrow \quad \text{D-H} \quad + \quad H^+. \tag{R-3}$$

Under the assumption that Reactions R-2, and R-3 occur rapidly and in close proximity to the site of Reaction R-1, the three reactions can be combined into an equivalent reaction :

$$2h^+ \quad + \quad \text{D-H} \quad \rightarrow \quad D^+ \quad + \quad H^+. \tag{R-4}$$

On the basis of this net reaction, we can express the rate of trapping of holes at D-H sites and the corresponding rate of release of H^+ as :

$$\frac{1}{2}\left.\frac{dp}{dt}\right|_{\text{D-H}} = -\frac{d[H^+]}{dt} = -\frac{d[D^+]}{dt} = \frac{d[\text{D-H}]}{dt} = \frac{1}{2}\sigma_{\text{D-H},p}\frac{J_p}{q}[\text{D-H}]. \tag{40}$$

The trapping of holes resulting in D^+ and the presence of mobile H^+ require modifications to the Poisson equation and the hole continuity equation in the oxide. The Poisson and continuity equations in the oxide now become :

$$\nabla \cdot (\varepsilon_{ox}\mathbf{E}) = q\left(p + [E'] + [H^+] + [D^+] - n - n_t\right) \tag{41}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J_n} - \left.\frac{dn}{dt}\right|_{N_t} \tag{42}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J_p} - \left.\frac{dp}{dt}\right|_{OV} - \left.\frac{dp}{dt}\right|_{\text{D-H}}. \tag{43}$$

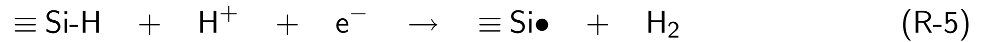
The above reactions introduce another mobile species, H^+, in the oxide whose transport needs to be modeled. The time scale associated with generation of interface traps due to interactions between hydrogen released in the oxide and defects at the Si–SiO_2 interface suggests that H^+

transport is dispersive in nature. As in the case of hole transport, in the current analysis we simplify the simulations by modeling the hydrogen transport using drift-diffusion equations :

$$\frac{\partial[\mathrm{H}^+]}{\partial t} = -\frac{1}{q}\nabla\cdot\mathbf{J}_{\mathrm{H}^+} + \frac{d[\mathrm{H}^+]}{dt} \quad (44)$$

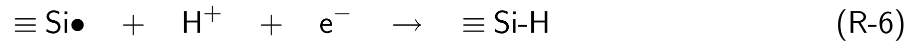
$$\mathbf{J}_{\mathrm{H}^+} = q\mu_{\mathrm{H}^+}[\mathrm{H}^+]\mathbf{E} - qD_{\mathrm{H}^+}\nabla[\mathrm{H}^+]. \quad (45)$$

As described in Chapter II, interface trap generation at the Si–SiO_2 interface results due to depassivation of $\equiv$ Si-H sites :



$$\equiv \text{Si-H} \quad + \quad \mathrm{H}^+ \quad + \quad e^- \quad \rightarrow \quad \equiv \text{Si}\bullet \quad + \quad \mathrm{H}_2 \qquad \text{(R-5)}$$

The above reaction suggests the participation of an electron from the silicon side of the interface. Recent work by Rashkeev *et al.* [91] has shown that protons reaching the Si/SiO_2 interface interact directly with Si-H and result in depassivation without the participation of an electron. However, this finding does not significantly alter the numerical model presented here due to the negligible change in the electron concentration in silicon due to the above reaction. The presence of excess H^+ can also result in a passivation reaction :



$$\equiv \text{Si}\bullet \quad + \quad \mathrm{H}^+ \quad + \quad e^- \quad \rightarrow \quad \equiv \text{Si-H} \qquad \text{(R-6)}$$

Using these reactions, the rate of generation of interface traps is expressed as :

$$\frac{dD_{it}}{dt} = \frac{d[\equiv \text{Si}\bullet]}{dt} = -\frac{d[\equiv \text{Si-H}]}{dt} = \left(k_{depass}[\equiv \text{Si-H}] - k_{pass}[\equiv \text{Si}\bullet]\right)\frac{J_{\mathrm{H}^+}}{q}. \quad (46)$$

Device Parameter Shift

The presence of fixed charge in the oxide and interface traps at the Si–SiO_2 interface results in a shift in the channel current associated with the MOSFET. This is a combined result of the perturbation in the potential distribution and surface scattering due to defect formation in the oxide. Several empirical models are available for modeling this dependences. In our simulations, we have used a simple mobility model that includes the dependence of surface mobility on the transverse electric field [69]:

$$\mu_n = \frac{\mu_0}{\sqrt{1+\gamma_n E_\perp}}. \tag{47}$$

Summary

In this chapter, we presented mathematical models for the basic physical mechanisms that were discussed in Chapter II. A variety of other numerical models for each of these physical mechanisms have been proposed in the literature. However, the mathematical models presented here represent the subset of available mathematical models that have been used in our simulation studies. These simulation studies are presented in the next chapter and illustrates the application of our approach to simulating hot-carrier degradation in MOSFETs.

CHAPTER IV

SIMULATION STUDIES

The hot-carrier modeling approach developed in Chapter III has been used to study the degradation of a set of p- and n-channel MOSFETs in this chapter. In the case of the p-channel devices used here, the primary degradation mechanism is the trapping of HC injected electrons in the gate and sidewall oxides. Hence, the simulations used for studying these devices utilize the electron trapping rate equation, Eq. (36), to model the oxide degradation. On the other hand, in the case of n-channel devices the generation of interface traps is expected to be the primary degradation mechanism. Hence, the hydrogen-mediated interface trap generation model is utilized during the simulation of the n-channel MOSFETs. The device structures used in all the simulations were obtained using SILVACO's ATHENA^{TM} [92] process simulation software. The carrier transport in oxide and the trapping rate equations, Eq. (35) and (36), have been implemented in SILVACO's ATLAS^{TM} [93] device simulator. This device simulator has been used during the p-channel HC degradation simulations presented here. The models presented in Chapter III, including the hydrogen-mediated interface trap generation model, have also been implemented into a stand-alone two-dimensional simulation code. This simulator has been used for all the n-channel device simulations presented in this chapter.

PMOS Hot-Carrier Degradation

The models presented in Chapter III have been to study the hot-carrier degradation in p-channel SOI MOSFETs with L$\times$W=0.8μm$\times$50μm and a gate oxide thickness of 15 nm. The MOSFETs were fabricated on SIMOX wafers with buried oxide thickness of 400 nm. The devices used for this study had body contacts to control the body bias and monitor the body current during the stress.

Accelerated stress experiments on p-channel transistors show that the hot-carrier-induced device parameter shift vs gate bias shift correlates well with the gate current [94]. In other words, for a given drain bias and stress period, the largest parameter shift is observed at a gate-bias that results in the largest gate current. This criterion was used to decide the stress biases during our experiments. All the hot-carrier stressing experiments were performed at V_{DS}=-10V and V_{GS}=-

0.8V for 3000 seconds. This bias condition resulted in the maximum gate current at V_{DS}=-10V. The HC-induced device degradation was monitored by measuring the I_{DS}–V_{GS} characteristics of the devices during the stress.

Process Simulation

The two-dimensional cross section of the device was simulated from the description of the process used to fabricate the test devices. The device structure produced by the process simulator is shown in Fig. 15. This figure shows the doping profile in the device as obtained from process simulation. The fabricated devices had body contacts to control the body bias and measure the body current. The modeling of devices with such body contacts requires the use of three-dimensional simulation tools. In order to reduce the simulation time, we have reduced the problem to a two-dimensional domain by approximating the effect of a body contact using an artificial "body" electrode in the silicon film as shown in Fig. 15. The size and location of this electrode were chosen to minimize its effect on the potential distribution in the device. This approximation was verified by comparing simulated I_{DS}-V_{GS} characteristics of structures with and without the artificial body contact with corresponding experimental characteristics of devices with and without body contacts.

Hot-Carrier Simulation

The experimental gate current I_{GS} vs V_{GS} plot in Fig. 16 shows that the maximum gate current occurs at a gate bias of V_{GS}=-0.8V for V_{DS}=-10V. This bias condition was chosen for hot-carrier stressing. At this bias condition, energetic carriers are generated near the drain due to the presence of a high electric field and impact ionization. The simulated spatial distribution of carrier temperatures in the device is shown in Fig. 17 while the impact generation rate is shown in Fig. 18. The carrier energies are related to the carrier temperatures through Eqs. (13) and (14). Under the influence of the high electric field the electrons move toward the gate while the holes are swept to the body. As the electrons travel towards the gate oxide, they gain energy and localized electron injection into the oxide takes place near the drain region of the device. The injected electron concentration in the gate oxide is shown in Fig. 19. The values of the electron and hole mobilities used during these simulations have been obtained from the literature to be 20 cm^2/Vs [95] and 10^{-5} cm^2/Vs [96], respectively.

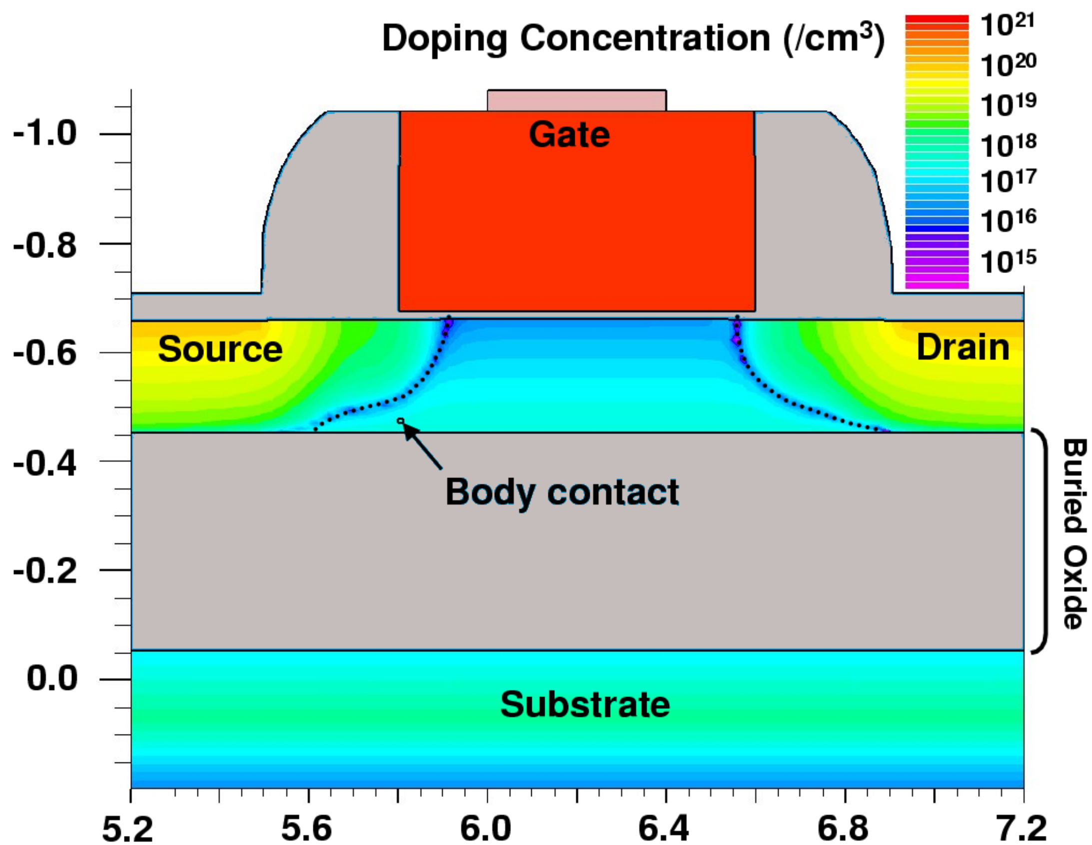


Figure 15: Structure and doping profile of the SOI p-channel transistor used for the simulations in this work. This structure was obtained from process simulation. The dotted lines indicate the locations of the source-body and drain-body junctions. An artificial body electrode contact was used to simulate the effect of a body contact. The non-symmetric nature of the source-body and drain body junction shapes is a consequence of introducing this artificial body electrode and is not a part of the fabrication process.

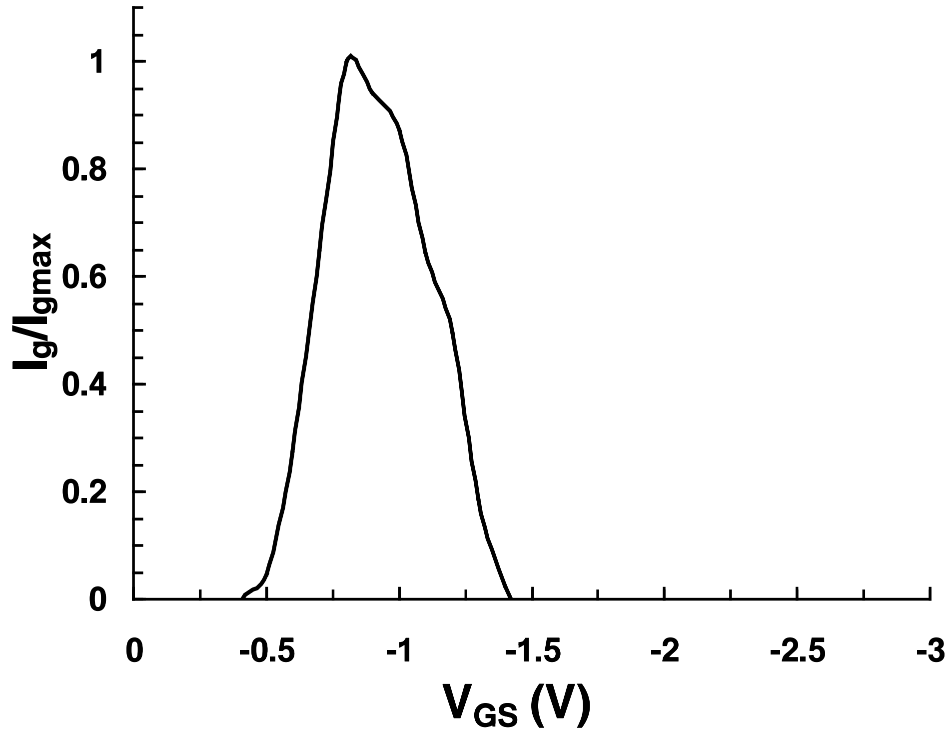


Figure 16: Experimental gate current vs gate voltage characteristics at a drain bias of -10 V. The gate current peaks at a gate bias of 0.8 V. This bias condition is used for the stress.

The volume density of trapped electrons in the oxide modeled using Eq. (36) is shown in Fig. 20. The parameters $\sigma_{n,t}$ and $N_{t,0}$ were chosen to give the best fit to experimental data ($N_{t,0} = 1.0 \times 10^{18}$ /cm^3 and $\sigma_{n,t} = 1.0 \times 10^{-18}$ cm^2). The values used in our simulations are consistent with those previously published in independent reports [97, 98]. As expected, the trapping is maximum near the drain region where maximum electron injection flux is expected. Fig. 21 compares the potential distribution under normal operating conditions of V_{GS}=-5 V and V_{DS}=-5 V before stress and after 3000s of stress. It clearly shows the effect of the trapped electrons in the oxide on the potential distribution under normal operating conditions. Fig. 22 compares the effective trapped electron density at different points along the channel at different stress times. This is calculated by converting the volume density of trapped electrons shown in Fig. 20 into an areal density at each point along the interface from source to drain. The areal

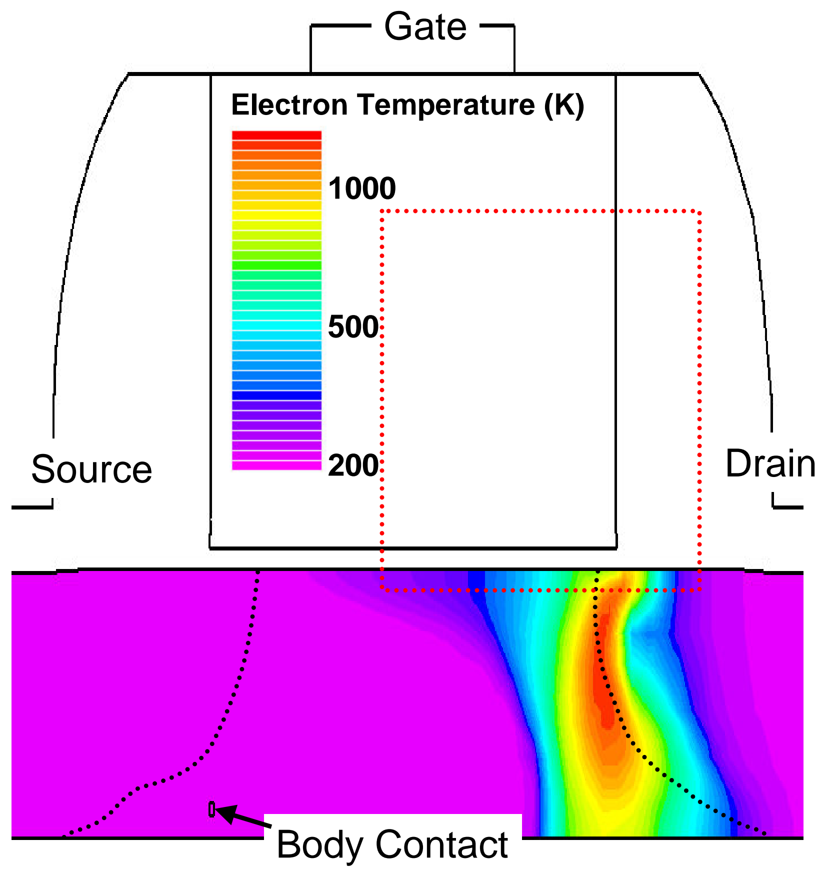


Figure 17: Electron temperature in silicon during p-MOS stressing at V_{DS}=-10 V and V_{GS}=-0.8 V.

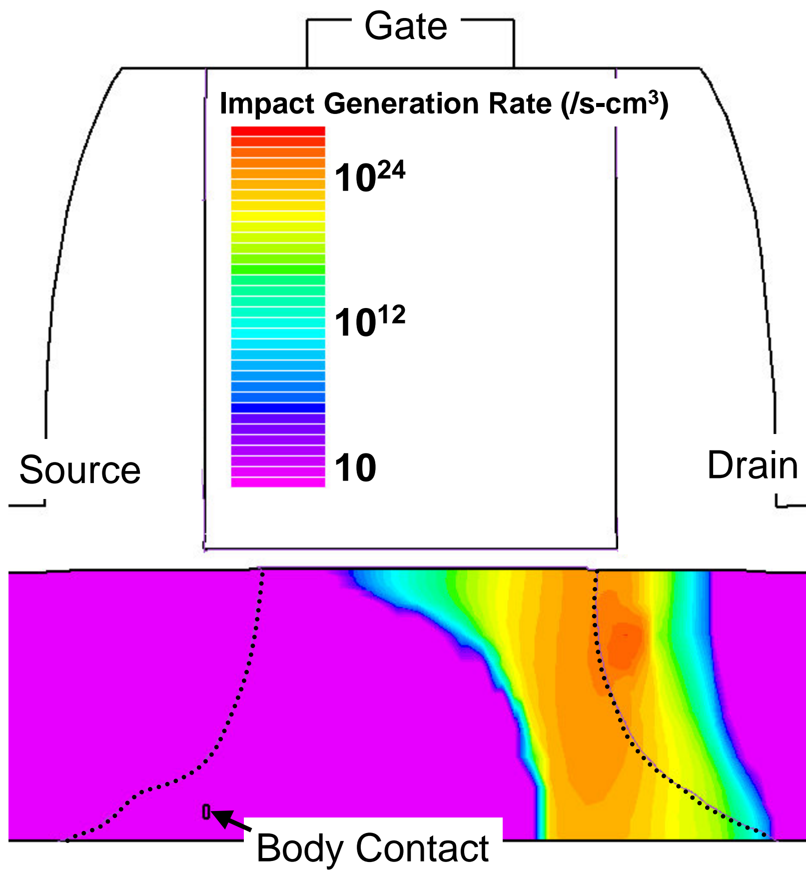


Figure 18: Impact generation rate at stress bias, V_{DS}=-10 V and V_{GS}=-0.8 V.

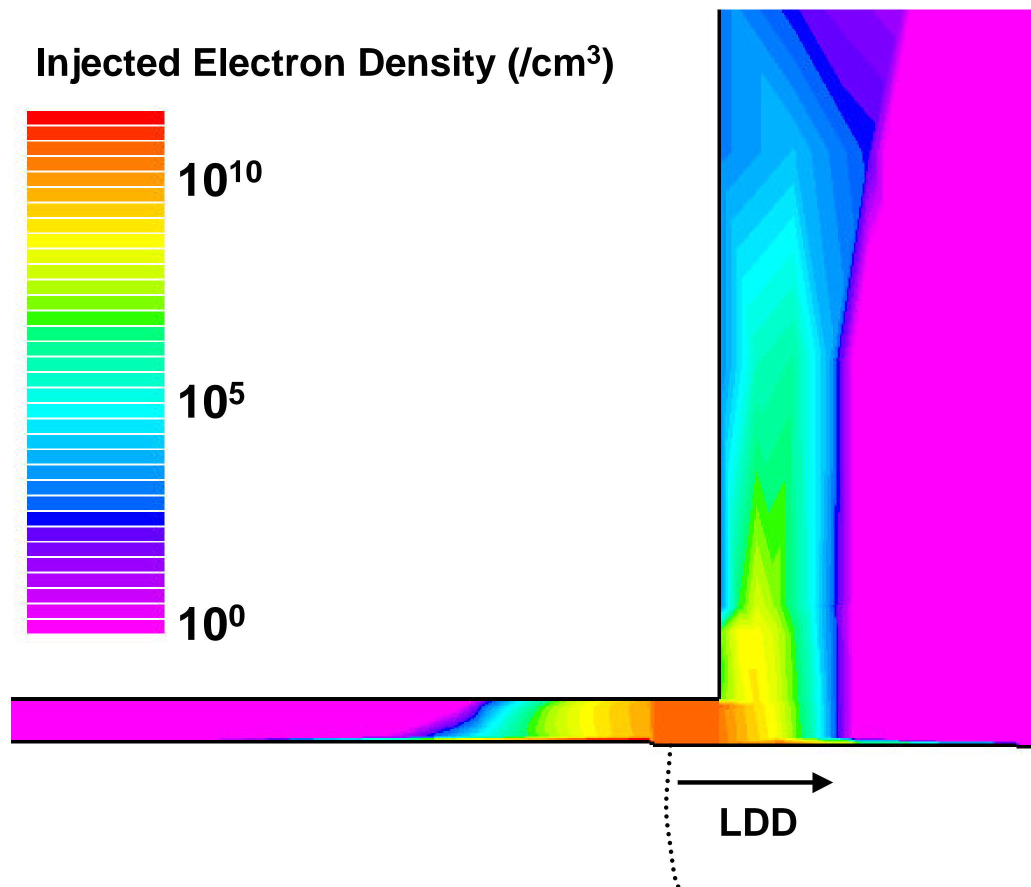


Figure 19: The concentration of injected mobile electrons in the oxide after 3000s of stress.

density is calculated by weighting the volume density of charge at a particular grid point in the oxide with the ratio of the distance of that point from the gate terminal and the thickness of the gate oxide. It clearly shows the localized charge distribution of negative charge increasing in density as we move from source to drain as well as the saturation of the trapped electron density close to the drain. This saturation behavior is expected as all the available traps become completely filled with electrons.

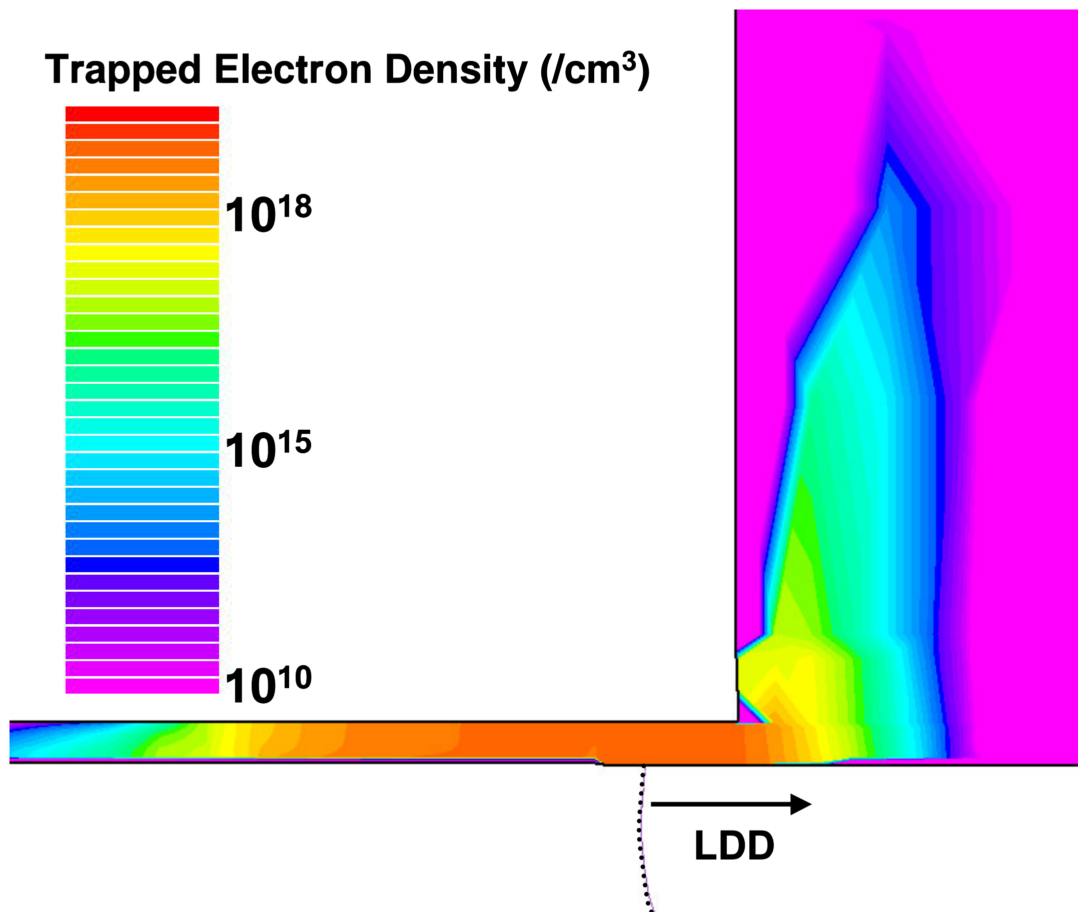
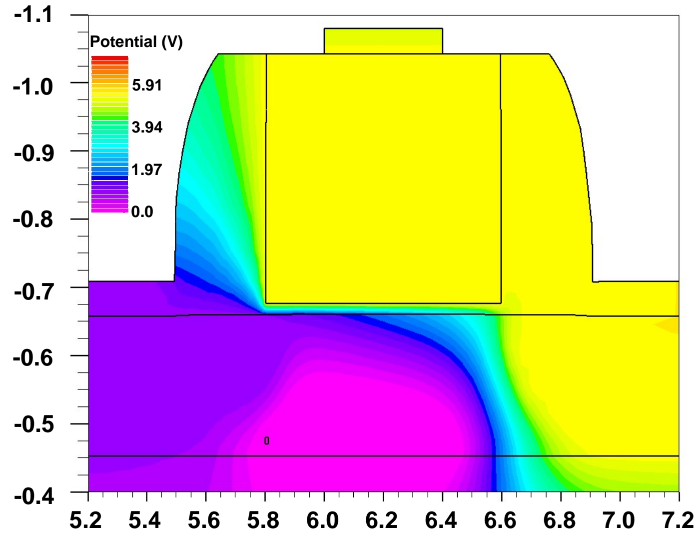
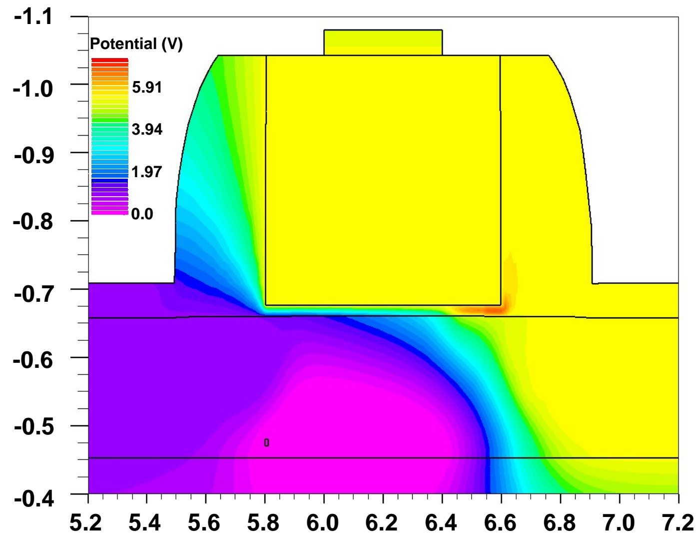


Figure 20: Trapped electron density in the oxide after 3000s of stress. Maximum electron injection occurs above the region of maximum impact generation.

In order to compare the hot-carrier simulation results with experimental data, we need to simulate the effect of trapped charge in the oxide on the device characteristics. The presence



(a) Before stress.



(b) After stress.

Figure 21: Potential distribution in the device under normal operating conditions of V_{GS}=-5 V and V_{DS}=-5 V before and after 3000s of stress.

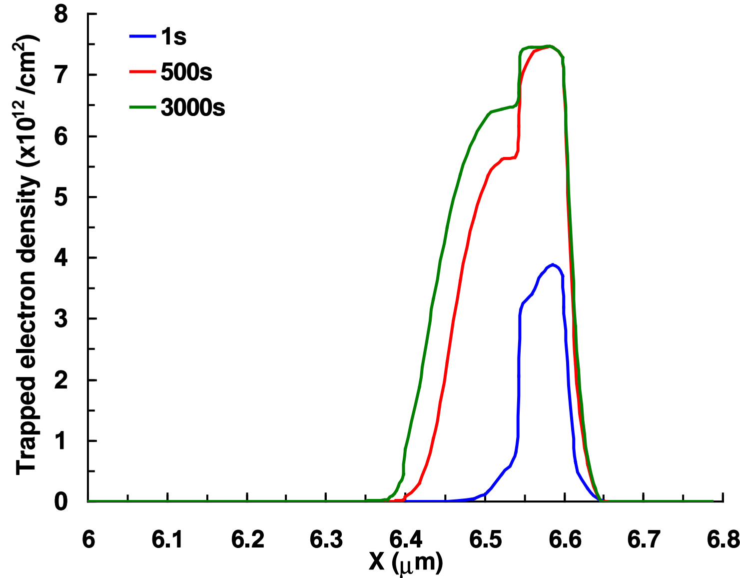


Figure 22: Effective trapped electron density as a function of lateral position.The trapped charge after 1s, 500s, and 3000s of stress are shown. X increases from source to drain.

of fixed charge in the oxide can significantly change the channel conductivity by affecting the mobility of carriers in the inversion layer. We have utilized the model presented by Lombardi *et al.* [99] to estimate the channel mobility in the presence of trapped charge in the oxide. The model parameters were adjusted to give the best fit between simulated and experimental I_{DS}-V_{GS} characteristics before hot-carrier stress. The same parameters were used to simulate the post-stress device characteristics.

The pre- and post-stress drain currents are shown as functions of the gate bias at a drain bias of -0.1 V in Fig. 23, showing an increase in the current after stress. This figure shows both experimental data and simulated results, which are in excellent agreement. The increase in the current can be explained as a result of the localized lowering of the threshold voltage due to the trapped electrons in the oxide. Fig. 24 shows a plot of the experimental and simulated relative transconductance change with respect to the initial transconductance as a function of the stress time. The increase in the transconductance is due to an apparent channel shortening as a result of the negative charge in the gate oxide. The simulation results agree closely with the experimental data. The parameter shift due to electron trapping in pMOS devices is known to have a logarithmic time dependence[100, 101]. According to the analytical model presented in [101] this logarithmic time dependence results from the “channel shortening” effect produced

due to electron trapping near the drain region of p-channel transistors. As can be seen from Fig. 24, our modeling approach is able to reproduce this well-known time dependence.

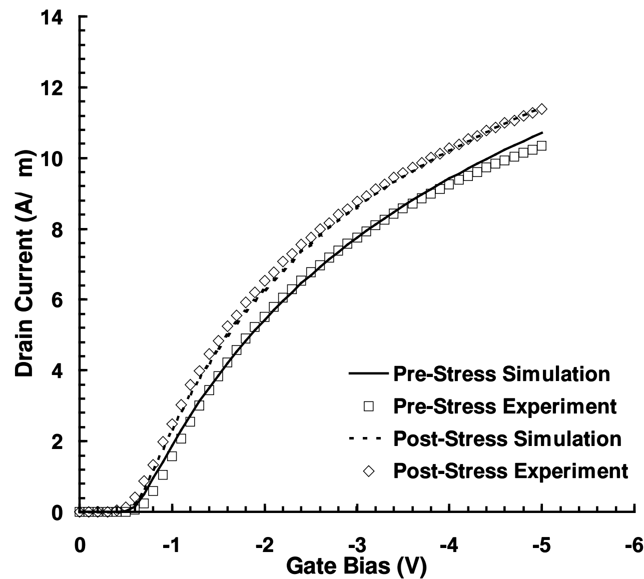


Figure 23: Drain current vs gate voltage before and after 3000s of stress. Drain currents are measured at a drain bias of -0.1 V with the gate voltage swept from 0 V to -5 V. Experimental data are shown as dots and the simulation results are shown as lines.

NMOS Hot-Carrier Degradation

Simulated Technology

The degradation of device parameters in n- and p-channel MOSFETs due to hot-carrier injection has been studied extensively in the past. The results of these studies have clearly shown certain common qualitative features associated with hot-carrier response of long channel devices. The models that have emerged from the analysis of these features have been extremely successful in predicting the dependence of hot-carrier degradation of long-channel n- and p-channel MOSFETs on parameters such as the operating bias, channel length, oxide thickness, and stress time. In this work, we compare the results of these conventional models with those obtained from our modeling approach and analyze their applicability to short-channel MOS transistors. This analysis was performed on a set of device structures obtained from a purely simulated fabrication process. The simulated fabrication process represents a typical bulk MOS process with self-aligned

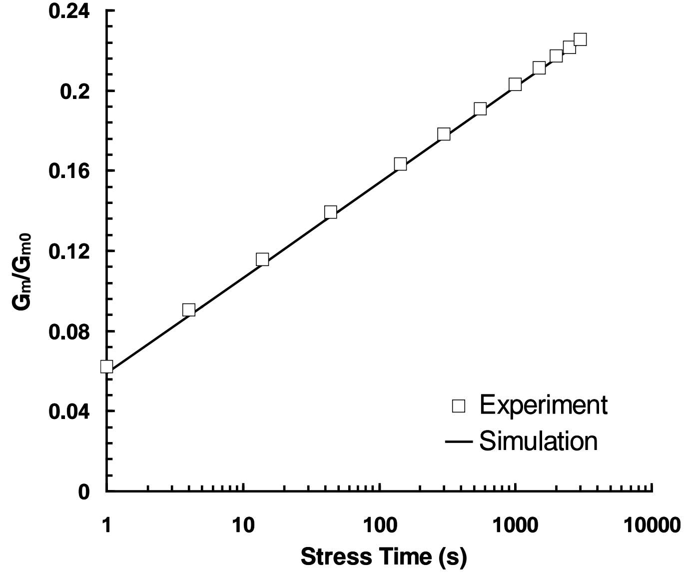


Figure 24: The relative change in the transconductance with respect to the initial transconductance as a function of stress time.

LDD source and drain. The channel lengths of devices used in this part of the study ranged from 0.10 μm to 2.0 μm with oxide thickness of 10 nm and channel width of 10 μm.

Substrate Current Characteristics

In both n- and p-channel devices, the dependence of substrate current on the bias condition provides a direct measure of the impact generation rate. The relatively slow spatial variation of electric field in long-channel devices allows one to model the impact-generation rate as a function of the local electric field. In particular, hot-carrier simulation approaches based on the lucky-electron model utilize an estimate of the maximum channel electric field, E_{max} to model the bias dependence of the substrate current using [16]:

$$I_{SUB} \propto I_D \exp\left(-\frac{\phi_i}{q\lambda E_{max}}\right) \tag{48}$$

where, ϕ_i is the impact-ionization threshold, and λ is the mean free-path of the minority carriers. The value of E_{max} is not directly measurable and hence has to be obtained from approximate methods [16] or through device simulations. The simulated value of E_{max} for a 2.0 μm nMOS device as a function of the applied gate bias for $V_{DS} = 5.0$ V is shown in Fig. 25. The substrate current values obtained for the various gate biases are used to obtain the relation

between I_{SUB} and E_{max} as shown in Fig. 26. For the 2.0 μm device, the simulated substrate current exhibits the behavior predicted by Eq. 48. Fig. 26 also shows the simulated dependence of I_{SUB} on E_{max} for a 0.1 μm nMOS device. The behavior of this short-channel device deviates significantly from Eq. 48, especially at high electric fields, due to the presence of non-local effects in the carrier-energy dependent impact-ionization model in our simulations. This behavior determines the rate of degradation of the devices as discussed in the next section.

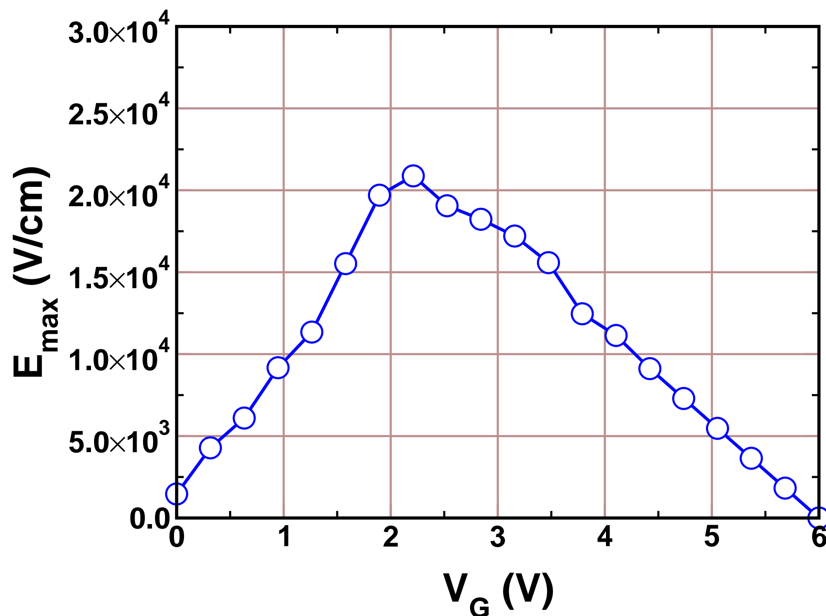


Figure 25: The simulated maximum electric field along the channel in a 2.0 μm nMOS device as a function of the gate bias at $V_{DS} = 5.0$ V.

Time Dependence of Device Degradation

In conventional modeling approaches, the time-dependence of the interface trap buildup due to hot-carrier injection in nMOS devices is typically expressed as a power-law with a technology

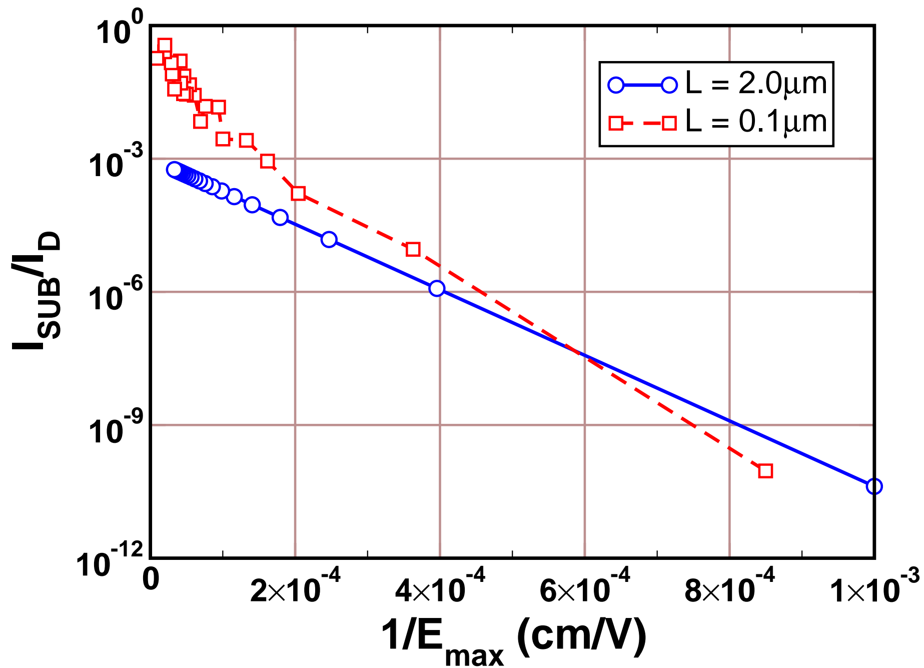


Figure 26: The simulated dependence of substrate current on the maximum electric field along the channel in nMOS devices with channel lengths of 2.0 μm and 0.1 μm

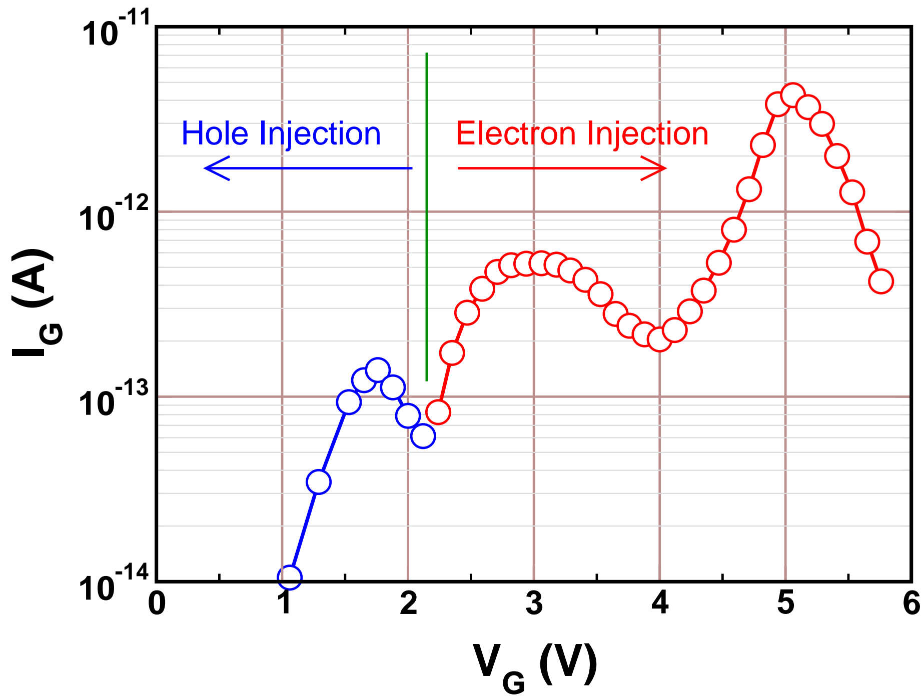


Figure 27: The simulated dependence of gate current on the gate bias in a 2.0 μm nMOS device at $V_{DS} = 5.0$ V.

dependent exponent[4]:

$$\Delta N_{it}(t) \propto \left[t \frac{I_D}{W} \exp\left(-\frac{\phi_{it}}{q\lambda E_{max}} \right) \right]^n \tag{49}$$

where, ϕ_{it} is the activation energy for the generation of interface traps and n is a process dependent parameter. The influence of hot-carrier-induced interface trap generation is typically measured in terms of variation in linear transconductance, G_m, or the drain current at a specific bias condition. In our simulations, we have used the percentage change in maximum transconductance, $\Delta G_m/G_{m0}$, obtained from $I_{DS} - V_{GS}$ characteristics at V_{DS}=0.1 V as a measure of the interface trap buildup. The simulated carrier injection current as a function of the gate bias at $V_{DS} = 5.0$ V for a device with L=2.0 μm is shown in Fig. 27. Based on Figs. 25 and 27, a gate bias of 2.0 V is expected to result in the maximum degradation in these devices at $V_{DS} = 5.0$ V. The simulated device degradation for a 0.1 μm and a 2.0 μm nMOS device during a hot-carrier stress at $V_{DS} = 5.0$ V and $V_{GS} = 2.0$ V is compared in Fig. 28.

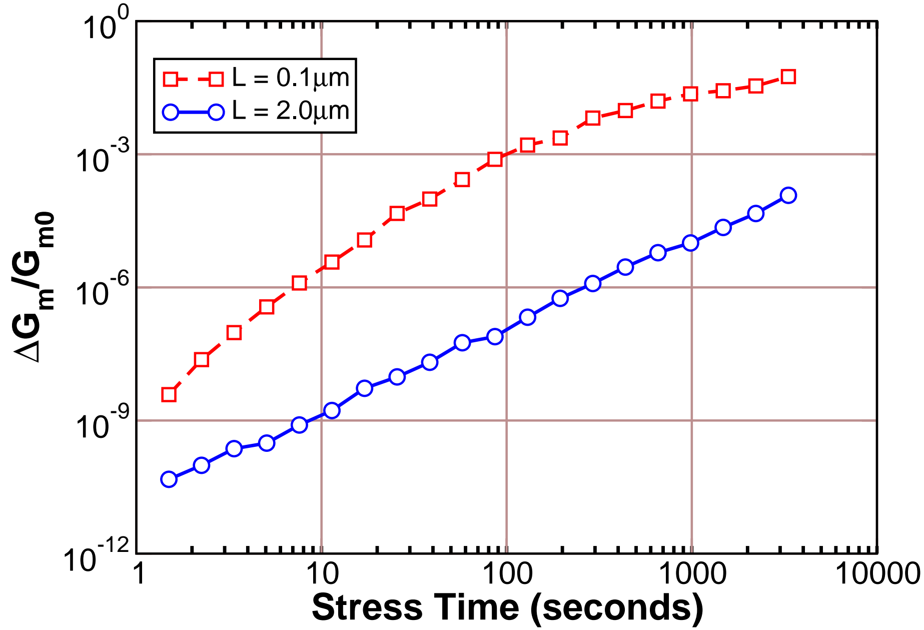


Figure 28: The simulated hot-carrier induced shift in linear transconductance of 0.1 μm and 2.0 μm devices as a function of stress time.

As seen in Fig. 28, the time dependence of interface trap buildup in the 2.0 μm device follows a power law as predicted by Eq. 49. However, in the case of the simulation 0.1 μm

device a combination of high localized fields, influence of interface traps on surface electric fields, and saturation of available interface defect precursors results in a time dependence that deviates significantly from the traditional power-law behavior. The accurate modeling of such physical mechanisms is essential in predicting the hot-carrier reliability of aggressively scaled MOS technologies.

0.17 μm Commercial Bulk Technology

In the case of n-channel MOSFETs, the majority of HC-induced parameter shift is due to generation of interface traps. In order to evaluate the hydrogen-mediated interface trap generation model presented in Chapter III, we have used a set of commercial bulk n-channel Lightly-Doped Drain (LDD) MOS transistors with different gate lengths and doping profiles. The target gate length for the technology used for fabricating the test devices was 0.17 μm. The effect of scaling on the hot-carrier reliability of this technology was evaluated using devices with gate lengths ranging from 0.17 μm to 0.35 μm. All the devices used here had an oxide thickness of 4.5 nm and a gate width of 15 μm. The normal operating bias for these devices was 2.0 V. The basic device structure and the doping profile as obtained from process simulation are shown in Fig. 29. In order to achieve the target threshold voltage in highly scaled MOS devices the well doping typically needs to be increased. However, this results in higher electric fields and HC injection currents near the drain-substrate junction. The dependence of HC reliability on the well doping was evaluated using devices with three different well implant doses – 1.0×10^{13} /cm^2, 2.0×10^{13} /cm^2, and 3.0×10^{13} /cm^2. Similarly, a halo implant is routinely used to increase punch-through voltage. However, the presence of this implant may result in increased hot-carrier vulnerability due to higher impact-generation rate. The dependence of the HC reliability on this implant was evaluated by comparing devices with three different halo implants splits (including devices with no halo implants) – no halo, 2.0×10^{13} /cm^2, and 3.6×10^{13} /cm^2.

Hot-Carrier Stressing Experiments

The hot-carrier degradation of the test structures was evaluated by performing accelerated stressing experiments at drain bias much higher than the normal operating biases for the structures. Drain biases ranging from 2.4 V to 3.2 V were used during these experiments. In n-channel devices, the maximum degradation at any given drain bias is observed at a gate bias that results

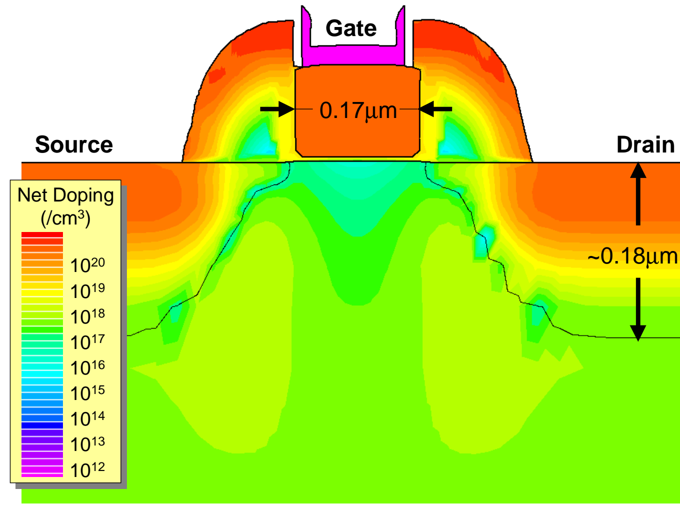


Figure 29: The geometry and doping profile of a 0.17 μm nMOS transistor used for simulating hot-carrier-induced interface trap generation.

in the maximum substrate current. As the substrate current is a direct measure of the impact ionization rate in the device, this bias condition corresponds to the maximum impact ionization in the test structures. During the hot-carrier stressing experiments, the gate bias was maintained at a value that resulted in the maximum substrate current at the corresponding drain bias.

The hot-carrier induced device degradation was characterized by monitoring various device parameters during the stress. In the results presented here, the shift in drain current at V_{DS}=V_{GS}=0.9 V is used as a measure of the device degradation. The device "lifetime" has been defined as the time to 10 % shift in the drain current measured at this bias condition.

Model Parameter Extraction

The fitting parameters associated with various models presented in Chapter III were extracted from experimental data obtained on the 0.17 μm test structures with a well implant of 2.0×10^{13} /cm^2 and a halo implant of 2.0×10^{13} /cm^2. The parameters extracted from a single set of these devices were used for all the simulations presented in this section.

We begin the modeling process by extracting parameters needed to accurately model the carrier heating in the silicon substrate. In particular, the parameters associated with the impact ionization model need to be extracted. In the case of n-channel devices, impact ionization is trig-

gered by hot-electrons in the channel and impact ionization due to hot-holes can be neglected[36]. This eliminates the impact ionization rate α_p from the analysis (see Eq. 21). The parameters A_n and B_n associated with the impact ionization rate α_n need to be extracted from experimental data. In order to extract these two parameters, we have used the measured maximum substrate current at the various drain biases used for the accelerated stressing experiments as the substrate current is a direct measure of the impact ionization rate. The simulated maximum substrate current vs drain bias curve was fitted to this data using A_n and B_n as free parameters. The results of this fitting process are shown in Fig. 30 and show that the simulated curve fits well to the experimental data on the test devices.

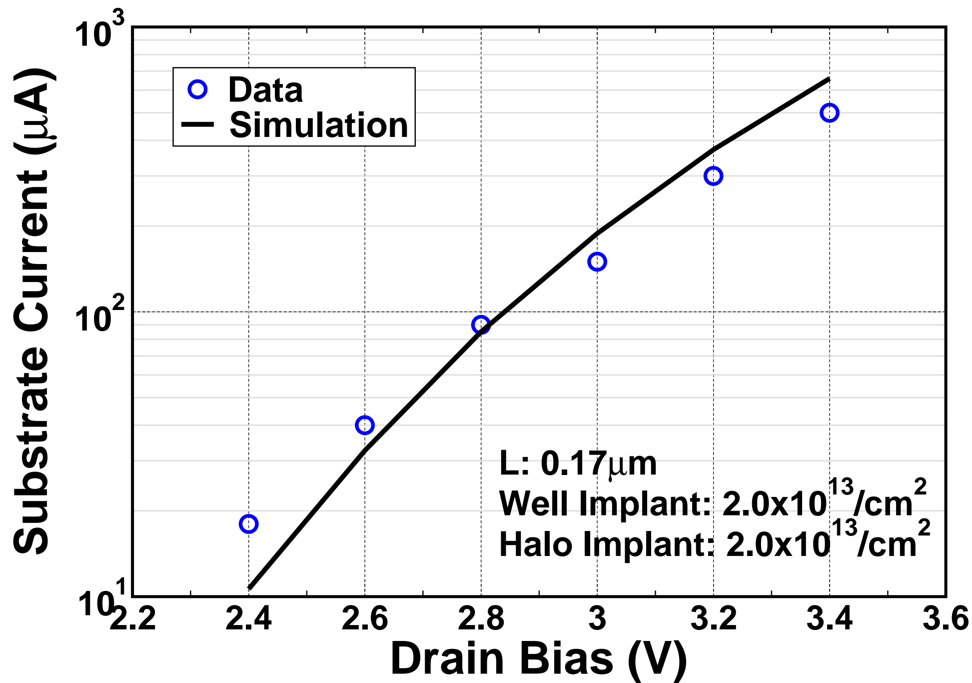


Figure 30: The maximum I_{sub} vs V_{ds} characteristics of a 0.17 μm device. The gate bias that resulted in the maximum substrate current at each drain bias was used during the stress.

The carrier injection parameter $C_{inj,n}$ (Eq. 33), the mobility parameter γ_n (Eq. 47), and the depassivation rate k_{depass} (Eq. 46) were extracted by fitting the simulated time dependence of the shift in drain current during hot-carrier stress at a drain bias of V_{DS}=3.2 V to the corresponding experimental data. The passivation reaction was neglected during this analysis (i.e., k_{pass}=0). The simulated shift in drain current during hot-carrier stress at V_{DS}=3.2 V after this fitting process

is compared with experimental data in Fig. 31. The remaining model parameters were taken from values reported in the literature and are listed at the end of this section. The carrier injection flux and the evolution of interface trap density distributions along the Si–SiO_2 interface during one these simulations are shown in Fig. 32 and 33. A uniform energy distribution is assumed for the acceptor-type interface states introduced by the interface traps in the silicon bandgap at the Si-SiOTwo interface. Furthermore, the acceptor-type interface states are assumed to be distributed entirely in the upper half of the silicon bandgap.

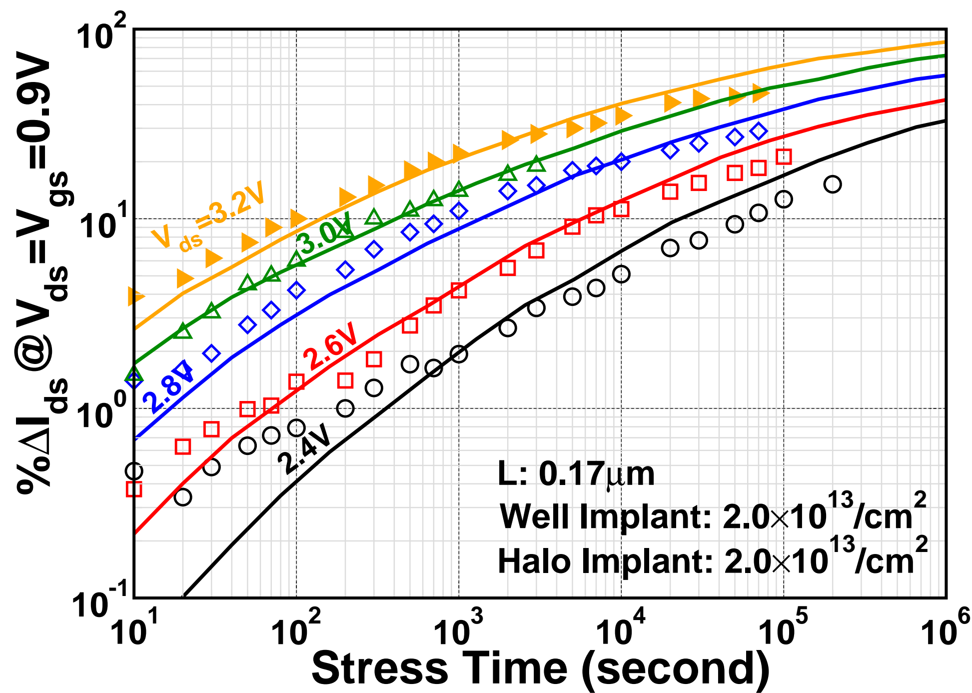


Figure 31: The percentage change in I_{ds} vs stress time for hot-carrier stress at different drain biases. The symbols represent experimental data while the solid lines represent simulation results.

Simulation Results

The parameterized models for impact-ionization, carrier injection and interface trap generation were used to evaluate the dependence of the hot-carrier lifetime on the device geometry and doping profile. The model parameters were extracted using the accelerated stress experiments

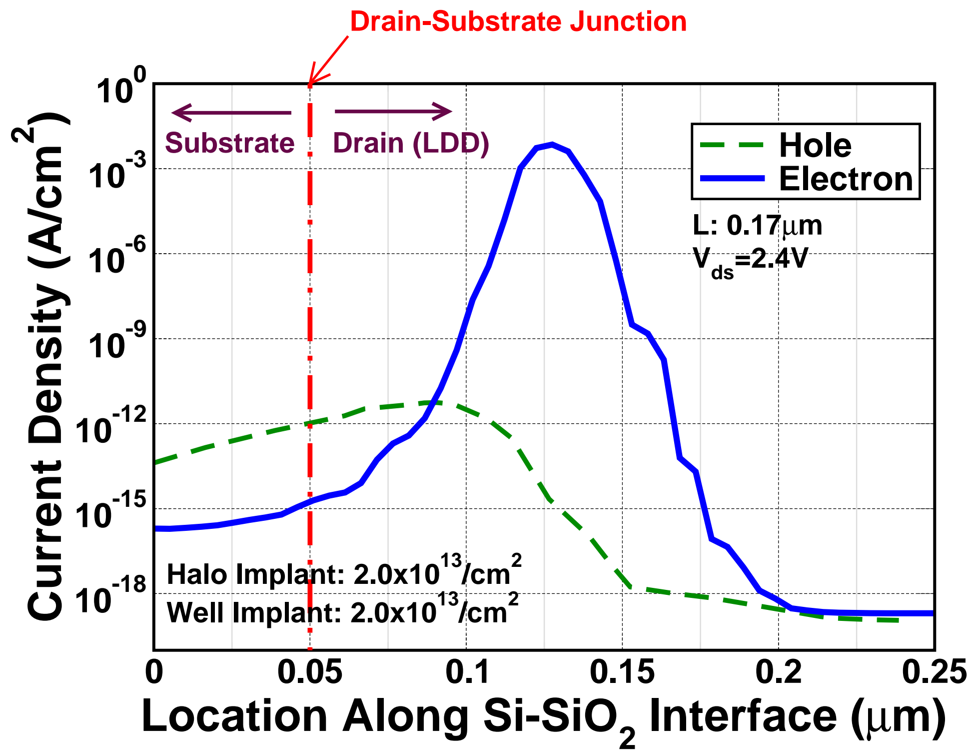


Figure 32: The carrier injection flux along the Si–SiO$_2$ interface of a 0.17 μm device as obtained from our simulation approach. The electron and hole injection current peaks are separated spatially. Most of the carrier injection happens in the oxide over the LDD region.

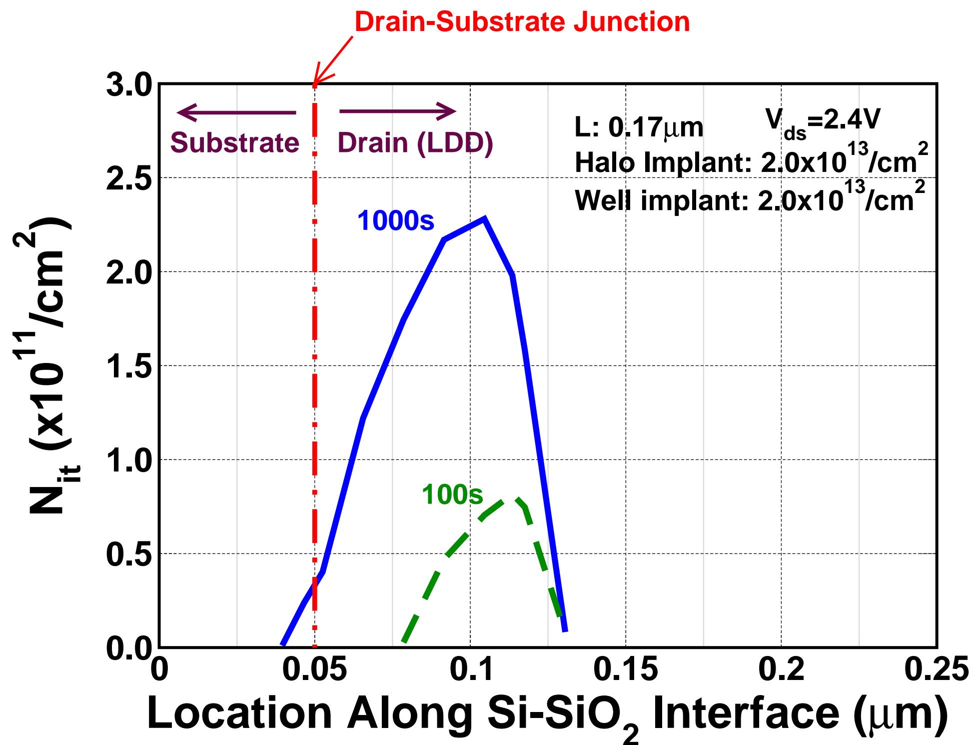


Figure 33: The interface trap density along the Si–SiO_2 interface of a 0.17 μm device during simulated hot-carrier stress.

at V_{DS}=3.2 V. These parameters were used to simulate the time-dependence of the hot-carrier-induced shift in the drain current for several lower drain biases. The results of these simulations are compared with experimental data in Fig. 31. As seen from this figure, the simulations parameterized at V_{DS}=3.2 V are able to accurately predict the drain bias dependence of hot-carrier degradation.

It has been found experimentally that the hot-carrier lifetime of n-channel MOSFETs is dependent on the supply voltage through the relation [102]:

$$\tau = A \exp\left(\frac{B}{V_{DD}}\right) \tag{50}$$

where, A and B are typically technology dependent parameters. On the basis of this empirical result, we have plotted the lifetimes, as defined above, at various drain biases as a function of $1/V_{DS}$ on a log-linear plot in Fig. 34. These values represent the same data as shown in Fig. 31. Similarly, the corresponding values obtained from simulation results shown in Fig. 31 are also plotted for comparison. As seen here, the simulations are able to reproduce the experimentally observed drain bias dependence.

A similar set of experiments and simulations have been performed on devices with gate lengths ranging from 0.17 μm to 0.35 μm. The results of this analysis are plotted in Fig. 35. The comparison between simulation and experimental data indicates that the hot-carrier degradation model scales well with respect to decrease in the gate length. The degradation for the shortest channel length device is slightly overestimated in the simulations. This is partly also an artifact of the interpolation process used to extract the device lifetime at V_{DS}=2 V from the data measured/simulated at higher biases.

The dependence of hot-carrier lifetime on the doping distribution in the devices is evaluated by comparing device with different well and halo implants. The results of hot-carrier simulations on devices with three different well and halo implants are compared in Fig. 36 and Fig. 37, respectively, as a function of the gate length. The hot-carrier degradation simulations are able to predict the dependence on variations in doping profiles for devices with varying channel lengths on the basis of parameters extracted from a single set of devices.

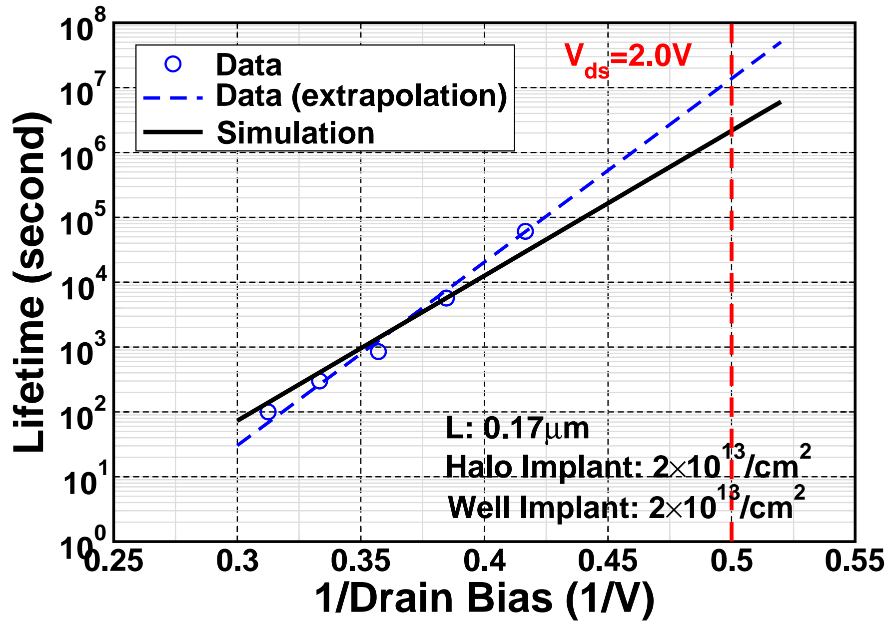


Figure 34: The hot-carrier lifetime as a function of the drain bias for a 0.17 μm device.

Summary

In this chapter, we presented several simulation studies that illustrate the application of the modeling methodology described in Chapters II and III. As seen from the results of these studies, the numerical model presented in Chapter III is able to model hot-carrier-induced charge trapping and interface trap generation in a variety of technologies.

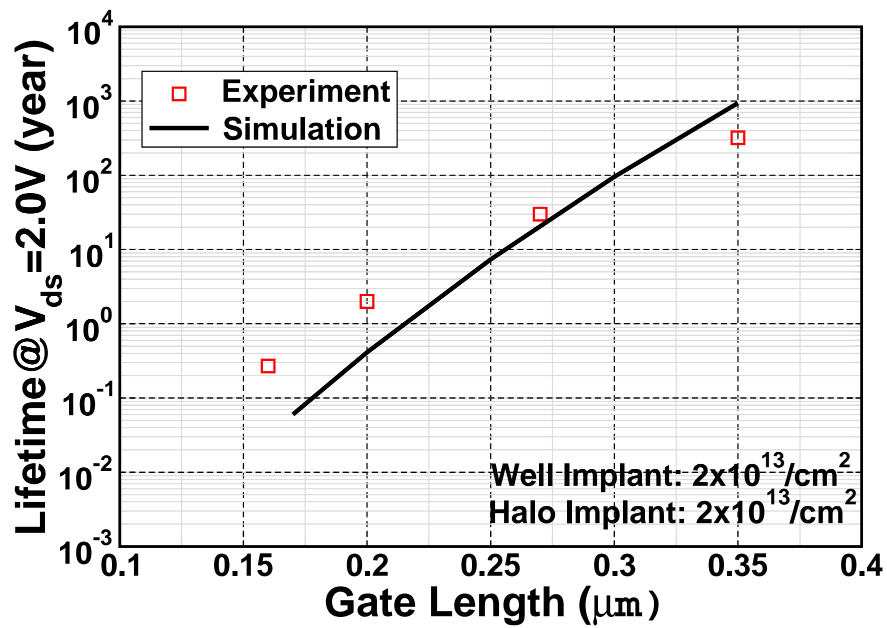


Figure 35: The dependence of hot-carrier lifetime on the gate length as obtained using the conventional approach and using our approach.

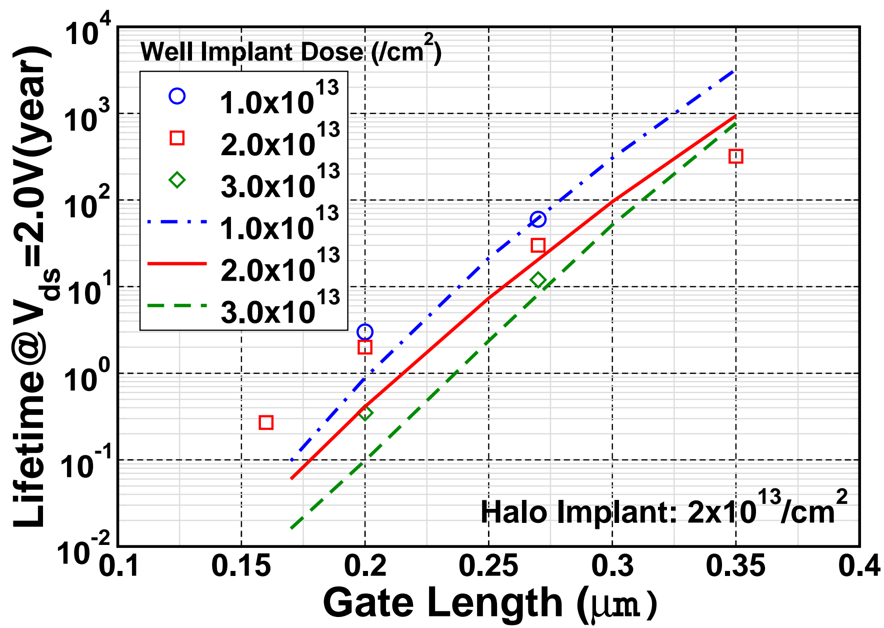


Figure 36: The hot-carrier lifetime as a function of the channel length for devices with different well implants. Symbols represent experimental data while lines represent simulation results.

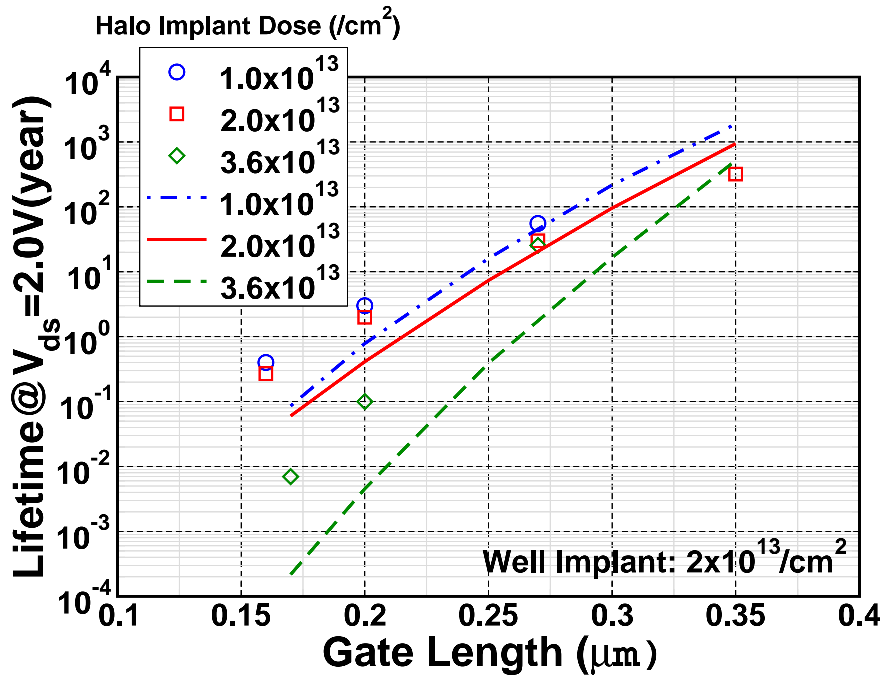


Figure 37: The hot-carrier lifetime as a function of the channel length for devices with different halo implants. Symbols represent experimental data while lines represent simulation results.

CHAPTER V

SUMMARY, CONCLUSIONS, AND FUTURE WORK

Summary and Conclusions

Hot-carrier degradation of MOS devices has been studied as a major reliability concerns for the past several decades. Empirical and semi-empirical models based on such studies have been used in the past to evaluate the hot-carrier reliability of semiconductor technologies. Some of the most widely used models are based on simplifying assumptions regarding the physical mechanisms responsible for hot-carrier generation, injection and oxide degradation. These assumptions have been known to break down in agreesively scaled semiconductor technologies. In addition, these models are not capable of predicting hot-carrier reliability variations across technologies. Finally, one of the major components that has been missing in past modeling approaches is the ability to model interactions between injected carriers and defects in the oxide.

The hot-carrier modeling approach developed in this dissertation provides a mechanism to circumvent majority of assumptions made in traditional hot-carrier modeling approaches. The use of energy-balance equations coupled with carrier-continuity and Poisson's equations allows us to account for non-local carrier-heating effects which could not be included in past models based on local electric-field values. Impact-ionization and injection models based on average carrier energies and non-Maxwellian energy distributions in our simulations provide a more accurate measure of hot-carrier injection fluxes in short-channel MOS technologies. A comprehensive model for the transport of injected carriers in the oxide and their interactions with intrinsic and extrinsics defects in the oxide has been developed. This allows us to model the trapping of injected electrons and holes at defect sites in the oxide. In addition, the release of hydrogen-species in the oxide by injected energetic carriers has been modeled for the first time. The transport of protons released in the oxide by injected carriers is modeled using drift-diffusion equations similar to those used for electrons and holes. This results in the presence of three different mobile species in the oxide. One of the most significant additions of this research has been the inclusion models for direct interactions between protons and defects at the Si/SiO_2 interface that result in generation of interface traps. The formation of interface traps due to such interactions is the

major cause of device instabilities due to hot-carrier injection. Using our model, the long-term trapping of electrons and holes as well as generation of interface traps through hydrogen-mediated mechanisms can be simulated in ultra-small geometry devices.

As illustrated in Chapter IV, we have successfully modeled hot-carrier degradation of long and short-channel bulk and SOI n- and p-channel MOSFETs using the numerical model described in Chapter III. The simulation of p-channel SOI MOSFETs illustrates the effects of electron-trapping in the gate and sidewall oxide on the device degradation. The localized lowering of threshold voltage due to trapped electrons in the oxide is shown to result in an effective channel shortening. This effects the channel current as well as the transconductance of the device. Our simulations accurately predict these phenomena as well as the experimentally observed logarithmic time dependence of device degradation. The parameterized models for impact-ionization, carrier injection and interface trap generation were used to evaluate the dependence of the hot-carrier lifetime on the device geometry and doping profile in the case of commercial technology. The model parameters were extracted using the accelerated stress experiments and used to simulate the time-dependence of the hot-carrier-induced shift in the drain current for several lower drain biases. The results of these simulations were able to accurately predict the drain bias dependence of hot-carrier degradation as well as the sensitivity of hot-carrier lifetimes on key technological parameters.

Future Work

The framework presented here represents an essential component of technological design process for building hot-carrier reliability in current and future technologies. However, the mathematical models described in Chapter III require further development to improve the predictibility of the modeling approach. Most significantly, an improved model for carrier injection mechanisms across the Si-SiO_2 interface is required. The injection model described in Chapter III does not account for several physical mechanisms such as carrier tunneling, quantum effects, and interactions with defect levels close to the interface. These physical mechanisms have been identified as some of the key reliability modeling requirements in the ITRS [10] published by SIA and may need to addressed through a hybrid Monte-Carlo simulation approach.

The modeling technique used in this research attempts to reduce the use of non-physical empirical parameters while modeling hot-carrier phenomena. While certain key parameters used

in our work have to be extracted from a set of experimental data such information may not be available on experimental technologies. In such cases, it might be possible to obtain similar information from other simulation techniques such as molecular dynamics simulations. Methodologies that allow seemless information exchange between molecular dynamics simulations and device simulations presented in this work will prove to be of utmost significance in studying emerging technologies.

Finally, even though the interface-trap generation model based on release of mobile protons close to the interface was sufficient to address the technologies investigated in this dissertation, several other hydrogen-related mechanisms have been shown to contribute to interface-trap generation in various semiconductor technologies. One or more of these mechanisms may need to be included in the future to provide a comprehensive set of models for carrier interactions with defects in the oxide.

List of Symbols

$\mathcal{E}_{\mathrm{avg}}$ Average carrier energy, see equation (1)

$[\mathrm{H}^{+}]$ Density of mobile protons, see equation (40)

$[\mathrm{OV}]_0$ Initial density of oxygen vacancies. Usually this refers to the density of oxygen vacancies at the end of fabrication, see equation (35)

$[\mathrm{OV}]$ Density of oxygen vacancies, see equation (35)

$[\mathrm{D}-\mathrm{H}]$ Density of hydrogen-containing sites, see equation (40)

$[\mathrm{D}^{+}]$ Density of trapped holes at hydrogen-related sites, D-H, see equation (40)

$[\mathrm{E}']$ Density of E′-centers, see equation (35)

α_{n} Electron ionization rate, see equation (21)

α_{p} Hole ionization rate, see equation (21)

$\chi_{\mathrm{a,n}}$ A fitting parameter introduced when using a sum of two exponentials to approximate the non-Maxwellian distribution of hot-carrier energies, see equation (30)

$\chi_{\mathrm{b,n}}$ A fitting parameter introduced when using a sum of two exponentials to approximate the non-Maxwellian distribution of hot-carrier energies, see equation (30)

χ_{n} An empirical parameter used in the model for the high energy band tail of hot-electron energy distribution, see equation (29)

$\varepsilon_{\mathrm{ox}}$ Permittivity in SiO_2 , see equation (27)

$\varepsilon_{\mathrm{Si}}$ Premittivity in silicon, see equation (9)

$\lambda_{\mathrm{n,ox}}$ Electron mean free path in SiO_2 , see equation (27)

$\mathcal{E}_{\mathrm{n}}$ Average electron energy, see equation (4)

$\mathcal{E}_{\mathrm{B,n}}$ Local energy barrier for electrons at the Si–SiO_2 interface, see equation (26)

$\mathcal{S}_n$ Soret coefficient for electrons, see equation (18)

$\mathcal{S}_p$ Soret coefficient for holes, see equation (18)

μ_n Electron mobility, see equation (9)

μ_p Hole mobility, see equation (9)

μ_{H^+} H^+ mobility in the oxide, see equation (45)

ψ Electrostatic potential, see equation (9)

$\sigma_{D\text{-}H,p}$ Hole capture cross-section at hydrogen-related sites, D-H, see equation (40)

$\sigma_{n,t}$ Electron capture cross section at electron traps in the oxide, see equation (36)

$\sigma_{p,OV}$ Hole capture cross-section at oxygen vacancies, see equation (35)

$\mathbf{E}$ Electric field, see equation (9)

$\mathbf{J_n}$ Electron current density, see equation (9)

$\mathbf{J_p}$ Hole current density, see equation (9)

$\mathbf{k}$ Momentum vector, see equation (4)

$\mathbf{x}$ Position in real space, see equation (4)

$C_{0,n}$ A fitting parameter introduced when using a sum of two exponentials to approximate the non-Maxwellian distribution of hot-carrier energies, see equation (30)

$C_{inj,n}$ A fitting parameter used in the model for hot-electron injection current, see equation (33)

$C_n(E)$ An electric field dependent parameter used by normalizing the electron energy distribution, see equation (29)

D_{H^+} H^+ diffusion constant in the oxide, see equation (45)

D_{it} Surface density of interface traps, see equation (46)

D_n Electron diffusion constant, see equation (9)

D_p Hole diffusion constant, see equation (9)

$E_{\perp,ox}$ Interfacial electric field component in the oxide perpendicular to the Si-SiO_2 interface., see equation (27)

$f_n(\mathcal{E})$ Energy distribution function for electrons, see equation (26)

G_{impact} Impact generation rate, see equation (21)

$g_C(\mathcal{E})$ Density of states in the conduction band of silicon, see equation (26)

G_n Electron generation rate, see equation (9)

G_p Hole generation rate, see equation (9)

J_{H^+} H^+ current density, see equation (45)

$J_{inj,n}$ Electron injection current density at the Si–SiO_2 interface, see equation (26)

k_{depass} Rate constant for depassivation of $\equiv$Si-H sites by H^+ flux, see equation (46)

k_{pass} Rate constant for passivation of $\equiv$Si$\bullet$ sites by H^+ flux, see equation (46)

k_B Boltzmann constant, see equation (10)

m_n^* Effective mass of an electron, see equation (4)

N_A^- Concentration of ionized acceptor atoms, see equation (9)

N_D^+ Concentration of ionized donors atoms, see equation (9)

$N_{t,0}$ Initial electron trap density, see equation (36)

N_t Density of defects that act as electron traps, see equation (36)

n_t Trapped electron density, see equation (36)

n Electron concentration ($/cm^3$), see equation (9)

p Hole concentration ($/cm^3$), see equation (9)

q Electron charge, see equation (9)

$R_{ii,n}$ Impact ionization scattering rate for electrons, see equation (22)

$R_{ii,p}$ Impact ionization scattering rate for holes, see equation (22)

S_n Electron energy flux, see equation (12)

S_p Hole energy flux, see equation (12)

T_n Electron temperature, see equation (12)

T_p Hole temperature, see equation (12)

T_L Lattice temperature, see equation (10)

t Time, see equation (4)

U_n Electron recombination rate, see equation (9)

U_p Hole recombination rate, see equation (9)

$v_{\perp,n}$ Component of electron velocity perpendicular to the Si–SiO_2 interface, see equation (26)

v_n Average electron velocity, see equation (4)

v_p Average velocity of holes, see equation (21)

l_{mf} Length of the mean free path of a carrier, see equation (1)

[$\equiv$ Si•] Surface density of $\equiv$ Si• sites at the Si–SiO_2 interface, see equation (46)

[$\equiv$ Si-H] Surface density of $\equiv$ Si-H sites at the Si–SiO_2 interface, see equation (46)

e^- Electron, see equation (45)

h^+ Hole, see equation (39)

TERMINOLOGY AND ACRONYMS

BOV Bridging Oxygen Vacancy

BTE Boltzmann Transport Equation

CTRW Continuous Time Random Walk

DD Drift-Diffusion

DRAM Dynamic Random Access Memories

EB Energy Balance

EEPROM Electrically Erasable Programmable Random Access Memory

HC Hot-Carrier

Hot-Carrier Degradation Instabilities in device and circuit behavior resulting from the injection of energetic carriers from silicon substrate into the surrounding dielectric films.

ICs Integrated Circuits

ITRS International Technology Roadmap for Semiconductors

LDD Lightly-Doped Drain

MB Maxwell-Boltzmann

MC Monte-Carlo

MD Molecular-Dynamics

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MTD Multiple Trapping and Detrapping

SHEI Substrate Hot Electron Injection

SIA Semiconductor Industry Association

SOI Silicon-On-Insulator

TCAD Technology Computer Aided Design

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