# CHARACTERIZATION OF HEAVY-ION, NEUTRON AND ALPHA PARTICLE-INDUCED SINGLE-EVENT TRANSIENT PULSE WIDTHS IN ADVANCED CMOS TECHNOLOGIES

By

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In memory of my beloved father S. L. Narasimham,

and to my beloved mother Shyamala Narasimham,

and sisters Gayathri and Priya

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# CHAPTER I

## INTRODUCTION

Astonishing technical advances in semiconductor fabrication, circuit design techniques and computer architecture have enabled an exponential increase in the performance and integration density of microprocessors. As feature size continues to shrink, more transistors can be packed into the same chip area, enabling large increases in the transistor count per chip. Fig. 1.1 shows the 2007 Semiconductor Industry Association's (SIA) roadmap for feature size scaling [ITRS-07]. The feature size is projected to decrease by a factor of 0.71 every three years. Technology scaling also facilitates a decrease in gate delay and enables clock speeds to continue to increase.

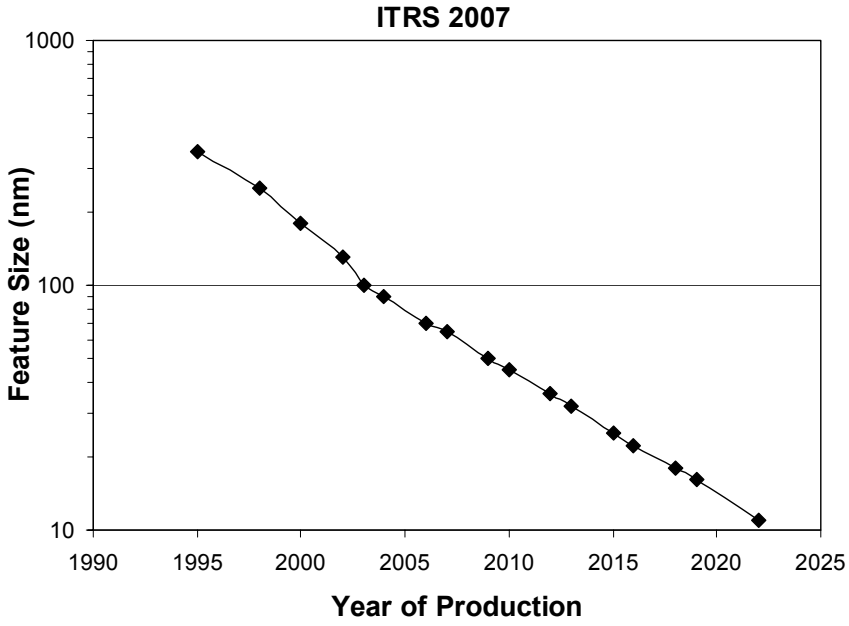



Fig. 1.1. SIA roadmap projections for feature size scaling as a function of the year of first production.

As the dimensions and operating voltages of integrated circuits (ICs) are shrunk to satisfy the consumer's ever increasing demand for lower power and higher speed, their sensitivity to radiation might increase significantly [Baum-05, Buch-01 and Dodd-03]. Deep sub-micron devices show increased susceptibility to Single-Event Effects (SEEs), which constitute a particular category of radiation effect [Buch-01]. A Single-Event (SE) occurs when an energetic particle, such as a heavy ion or neutron, strikes a device and causes a change in the device's normal operation.

SEEs encompass a multitude of different phenomena that have, as a common cause, the passage of an energetic particle through the semiconducting or insulating materials used in the manufacture of integrated circuits. The common sources of SEEs are cosmic rays and heavy-ions for space applications, and neutrons (which produce SEEs indirectly through secondary particles emitted as a result of nuclear interactions) and alpha particles for terrestrial applications. As an energetic particle passes through the IC, it excites electrons from the valence band and leaves behind a track of electrons and holes. If the track passes through or near a reverse-biased semiconductor p-n junction, the high electric field present in the region can efficiently collect the particle-induced charge through drift process. Carriers can also diffuse from locations near a p-n junction into the vicinity of the depletion region field where they can be collected, adding to the total charge collected. Charge generated along the particle track can locally extend the junction electric field due to the highly conductive nature of the charge track, leading to a field funnel region [Hsie-81]. This funneling effect can increase charge collection at the struck node by extending the junction electric field away from the junction and further into the substrate, allowing charges deposited away from the junction to be efficiently

collected through drift. In advanced CMOS processes when electrons or holes released by a particle strike are confined within the well region in which a transistor exists, charge collection may be enhanced by a parasitic bipolar effect [Dodd-03]. For example, for a PMOS transistor in an n-well process, holes induced by the particle strike may be collected at the drain or substrate junctions. However, electrons left behind in the well region lower the well potential. This lowers the source-well potential barrier and may result in injection of holes into the well from the source, which can then be collected at the drain. This adds to the original particle induced current and the effect is described as parasitic bipolar charge collection.

Some types of SEEs are also referred to as soft errors in the commercial domain. Soft errors are the primary radiation concern for commercial terrestrial applications, as opposed to parametric degradation and hard errors, which are significant concerns in space and military environment [Baum-05]. A soft error occurs when a radiation event deposits enough charge to reverse or flip the data state of a memory cell, register, latch, or flip-flop. The error is "soft" because the circuit/device itself is not permanently damaged by the radiation and the error can be corrected by writing new data [Baum-05]. In contrast, a "hard" error is manifested when the device is physically damaged and the data loss is permanent.

There are different types of effects that result in soft errors; the most important types are the Single-Event Upset (SEU) and the Single-Event Transient (SET). An SEU is a static upset in storage cells such as latches and flip-flops. The upset rate due to such an event is independent of the clock frequency [Baum-05]. For CMOS ICs, an energetic particle strike can cause a transient voltage perturbation, called a SET, that propagates

through the circuit and may become stored as incorrect data, causing disruption of the circuit operation. Upset rates due to SETs depend on the pulse width of the SET and the clock frequency [Kaul-92, Sata-94, Buch-01, Baum-05]. With increasing clock frequency there are more latching clock edges to capture an SET [Baum-05, Buch-01]. With decreasing feature sizes the charge required to represent a logic HIGH state decreases and hence may result in increased susceptibility to SETs [Buch-01]. The width of the SET is also governed by the restoring device drive strength as well as the charge collection kinematics. The reduction in the device dimensions may reduce the total amount of charge collected, reducing susceptibility to SETs. However, lower restoring drive currents with scaling may result in an increase in the SET pulse width.

SETs in digital circuits were relatively rare until the recent past. SETs were seldom observed in combinational logic circuits with minimum feature sizes larger than 0.3 μm because they were unable to propagate significant distances through the circuits and those that did reach a latch were unlikely to be captured due to lower clock frequencies. The logic gates in a combinational circuit act as low pass filters that inhibit the propagation of high frequency SET pulses. Moreover, capture in a synchronous latch requires that the SET arrive at the latch within a certain window of the clock edge for it to be latched as an error [Buch-01]. In slow circuits with relatively few clock edges, that probability is small. These two factors resulted in SETs in logic circuits making a negligible contribution to the overall error rate. As a consequence, to qualify microprocessors for space applications, radiation test engineers frequently tested only the registers for their SEU sensitivity, and completely ignored potential contributions from logic gates [Buch-01].

For feature sizes below 0.3 μm, increases in the clock frequency and reductions in the critical charge for SET creation result in increased sensitivity to SETs. With scaling the SET duration may become comparable to the of the logic transition times, enabling SETs to propagate with little attenuation and increasing their probability of getting latched as an error.

Researchers have investigated technology scaling trends in combinational logic soft errors. Such soft errors are caused by latching SETs. Shivakumar et al. have projected an increase in the combinational logic soft errors with technology scaling [Shiv-02]. Their prediction indicates that the per device logic soft errors may dominate over memory and latch soft errors for technologies beyond 65 nm. However, Seifert et al. project a slight decrease in the combinational logic SER for certain logic circuits when scaling from 90 nm to 65 nm [Seif-06]. They indicate that the slowdown in voltage and frequency scaling combined with reduction in device dimensions and charge collection efficiency may result in such a trend.

Since logic soft errors are caused by latching SETs, the logic SER depends on various masking factors associated with SETs such as electrical masking, latch window masking and logical masking, as discussed in [Shiv-02, Seif-06]. Of these, electrical masking and latch window masking depend on the width of the generated SET. Thus, for better prediction of logic SERs, knowledge of SET pulse width distributions for different radiation environments is important. The varying conclusions on logic SER trends and the relative lack of experimental measurements of logic SER indicate the importance of characterizing SETs in digital circuits.

This work presents a novel circuit technique that can be used to characterize the width of SET pulses [Nara-06]. Test chips with the SET characterization circuit have been fabricated in a range of technology nodes from 1.5-µm to 90-nm bulk through commercially available foundries. Heavy-ion, neutron and alpha particle-induced SET pulse width have been characterized. The following chapters detail the background necessary for SET generation and propagation, followed by details about the measurement technique. Heavy-ion experimental results for SET distributions in 130-nm and 90-nm processes are then presented. Technology scaling trends are explained based on experimental measurements in 130-nm and 90-nm and mixed-mode 3D-TCAD simulations. Based on the dependence of SET pulse width on different factors including the linear energy transfer of the energetic particle and the restoring device drive strength, a mathematical model is presented for SET pulse widths in the 90-nm process. Finally, neutron and alpha particle-induced SET distributions and failure-in-time (FIT) rates are presented. The neutron and alpha SET cross-sections are analyzed using Monte Carlo based simulations and these results along with scaling trends in the cross-sections are included in appendix A.

# CHAPTER II

# SETs – BACKGROUND

The formation of an SET involves three steps, namely charge generation, charge collection, and circuit response [Kaul-92, Sata-94, Buch-01, Dodd-03]. Charge generation depends on the properties of the incident particle and also on the properties of the semiconductor material that it strikes. Electrical parameters such as applied bias and the doping levels in the semiconductor will affect the charge collection [Buch-01]. This will vary widely from one circuit to another and between transistors in the same circuit. The topology of the circuit affects the circuit response [Buch-01, Dodd-03]. In the case of static combinational logic circuits, the output of the struck gate will revert back to its original state after a certain amount of time depending on the amount of charge deposited and on the restoring device drive strength. The restoring property of static gates results in a finite width transient. The duration of the transient also depends on factors such as ion LET and strike location with respect to the sensitive drain, which affect the amount of charge deposited and collected.

## *Charge Deposition*

An ionizing particle can release charge in a semiconductor device through two primary methods: direct ionization by the incident particle and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device.

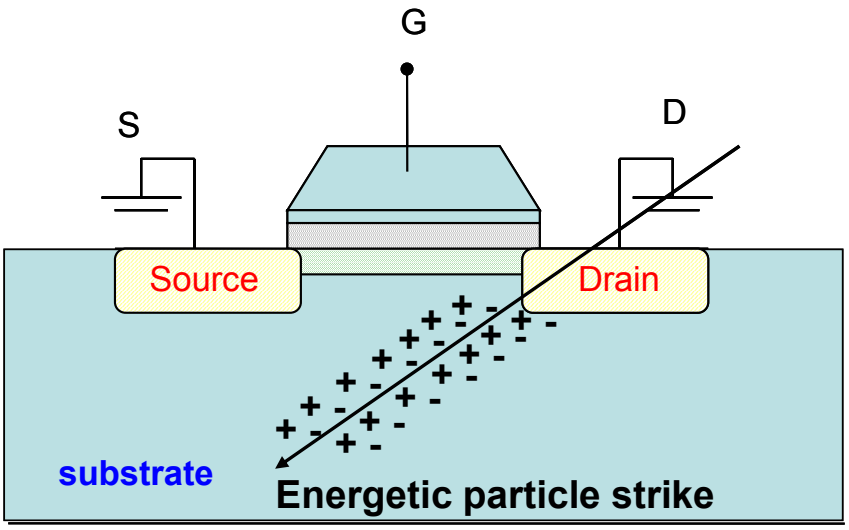



Fig. 2.1. Generation of electron-hole pairs due to an energetic particle strike

Direct Ionization: When an energetic particle such as a heavy-ion or an alpha particle strikes the semiconductor material it loses energy through Coulombic interactions with the bound electrons in the material. Energy is lost by the incident ion during the liberation of electrons. When all of the incident particle's energy is lost it comes to a rest in the semiconductor material. The distance traveled by this particle in the semiconductor is called the particle's range. The electrons stripped by the particle diffuse away from the point of generation, and may result in further Coulombic interactions, releasing addition electrons. This ionization of the material causes a dense track of electron-hole pairs to be created (Fig. 2.1). The width of this ion track depends on the energy of the incident ion [Stap-88]. The average energy required to produce an electron-hole pair in silicon is 3.6 eV. For energetic particles, one can compute the charge that will be generated in the semiconductor material from the Linear Energy Transfer (LET) [Buch-01]. LET refers to the energy loss per unit length of the particle as it passes through a material. In silicon,

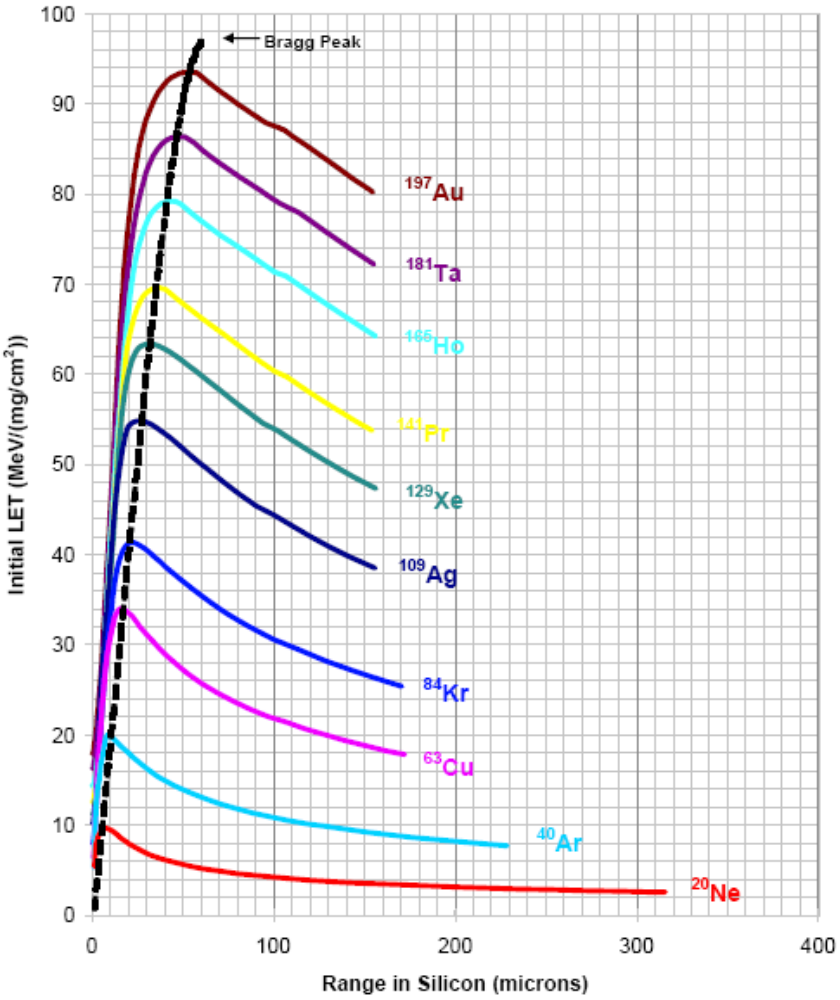



Fig. 2.2. Initial LET vs. range in silicon for different ions.

which has a density of 2.42 g/cm$^3$, the amount of electron hole pairs (Q) created along a track of length L is given by the following equation [Buch-01]:

$$Q \quad (pC) \quad = \quad 0.011 \times L\,(\mu m) \times LET\,(MeV - cm^2 / mg) \qquad (1.1)$$

The LET of a particle versus range in a material is useful in understanding the interaction of a particle with matter. Fig. 2.2 shows a curve of initial LET versus range in silicon for various ions [TAMU]. This chart is for 15 MeV/nucleon ion energy. The peak

in the charge deposition is referred to as the Bragg peak and in general occurs as the particle reaches an energy near 1 MeV/nucleon [Dodd-03].

Indirect Ionization: Protons and neutrons result in charge deposition through indirect ionization. When a high energy proton or neutron enters the semiconductor, it may undergo an inelastic collision with the target nucleus, resulting in spallation reaction products. The reaction products can now deposit energy along their paths by direct ionization. As the secondary products are much heavier than a proton or neutron, they deposit higher charge densities and hence may result in a single event [Dodd-03].

*Charge Collection*

Charge collection is the next stage in the formation of SETs. The electric field associated with a junction in a transistor causes charge separation. Efficient charge collection occurs when the charge track traverses a depletion region, or is within a diffusion length of the depletion region. Charge collection is greatest in reverse-biased junctions because of the greater thickness of the depletion region [Buch-01]. These include the drain/well and drain/substrate junctions in CMOS transistors.

Charge initially collected from the depletion layer is termed as *prompt* charge. In some cases the depletion layer may extend into the lightly doped region in the direction of the ion track. As mentioned in Chapter I, this extension of the depletion layer is described as funneling and it results in the collection of additional charge, thus increasing the sensitivity of the device to SETs [Buch-01].

As mentioned in Chapter I, in advanced CMOS technologies, charge collection may be enhanced by a parasitic-bipolar effect that is caused by the confinement of electrons or

holes within a well or body region in which a transistor is located. Some researchers have observed evidence of parasitic bipolar charge collection based TCAD simulations [Dodd-96, Dodd-03]. For example, for a p-channel transistor located in an n-well, electrons left in the well can lower the well potential and thus lower the source/well potential barrier, which may result in the source injecting holes into the channel. These holes can be collected at the drain where they add to the original particle-induced current, and hence may increase the susceptibility of the device to single events [Dodd-03]. This is described as the bipolar effect, where the source acts as the emitter, the channel as the base region, and the drain as the collector. Some researchers believe that with technology scaling, the reduced channel length increases the bipolar gain, making the effect more pronounced [Dodd-96]. The impact of the parasitic bipolar effect with scaling may also be affected by other factors including trends in the supply voltage and scaling of the contact size.

*Single Events in Logic Circuits*

In a combinational logic circuit, charge collection due to a single-event strike on a particular node will generate a low-to-high or high-to-low voltage transition or a transient. The collection of charge first results in a current spike. This current pulse is usually modeled using a double exponential current source in simulators. This current spike may momentarily flip the state of the output node, thus causing a "glitch" or transient to propagate along the combinational logic chain. The ability of this noise pulse to propagate depends not only on its magnitude, but also on the active logic paths from the node existing at that instant in time. An example of this is shown in Fig. 2.3.

In Fig. 2.3, a single-event strike generates a voltage transition on a node of this circuit. The possible propagation of this pulse to a latch (storage) element depends on several factors. First, the active combinational paths at that instant in time depend on the dynamic state of the logic. Second, assuming that an active path exists for the propagation of the

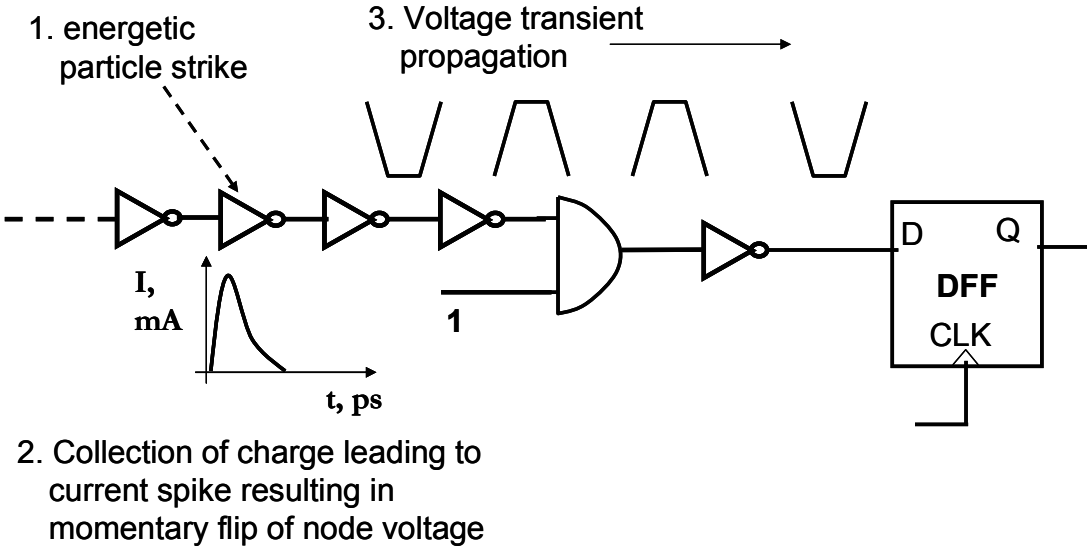



Fig. 2.3. Single event transient propagation through a combination logic chain

pulse, the pulse will be shaped and phase delayed as it propagates through the intervening gates en route to a latch. Third, the temporal characteristics of the pulse as it arrives at a latch are important. The pulse must arrive within the setup-and-hold time of the latch element to be captured. The clocking characteristics of the latch and the previous state of the latch contribute to this mechanism. If all three of the above conditions are properly met, then the SE-generated noise pulse will be captured by the latch as erroneous information.

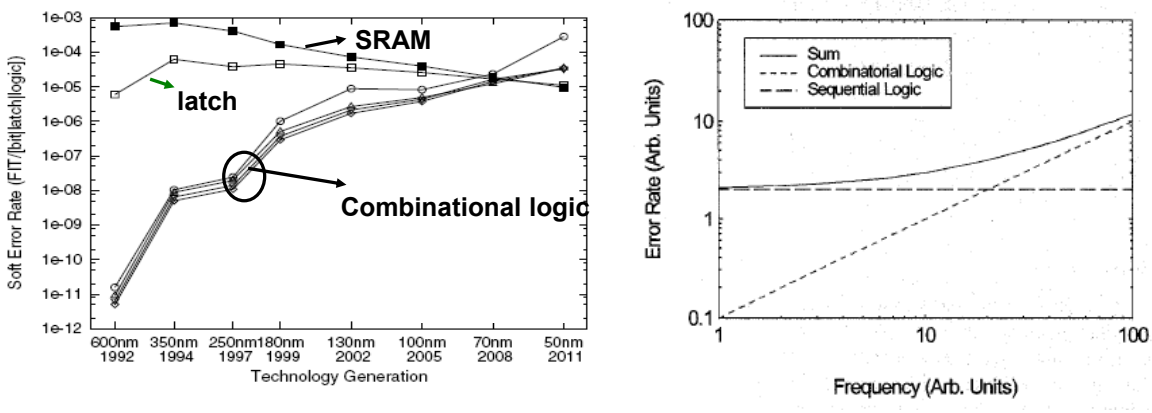
As long as an active path exists for the propagation of the single event transient pulse, its capture as an error by a latch depends on the width of the transient and on the clock frequency. An error in this context is defined as latching an incorrect logic value. Depending upon the magnitude of charge collected, the width of this transient voltage pulse varies. The pulse width of the transient (along with clock frequency) thus determines the vulnerability of the circuit to SETs [Dodd-03, Buch-97].

Single-event strikes on control logic circuitry have also been identified as a significant contributor to the overall chip-level SER [Seif-05]. Specifically SETs created in the global and local clock buffers can result in clock jitter and race conditions. Clock jitter results in differences in the clock arrival times in the same sequential circuit. Charge injected due to strikes on clock nodes at time instances close to the clock transition time can cause the clock edge to move randomly in time. This condition can result in setup time violation. A race condition can occur when a strike on the clock node results in the formation of a new clock pulse. Such a clock pulse can result in a false opening of the sequential circuit and in data racing through two consecutive pipeline stages instead of one. The width of the radiation-induced transient affects the vulnerability of a circuit to

clock jitter and race conditions. Thus it is important to understand the distribution of the SET pulse widths for a given radiation environment for prediction and mitigation of failures from clock node upsets.

For older technologies the SET could not propagate through a large number of logic gates since it usually did not produce a full output swing (due to higher nodal capacitances) and was quickly attenuated due to large load capacitances and large propagation delays [Baum-05]. In advanced technologies with lower propagation delays and higher clock frequencies, the SET can more easily traverse many logic gates, and the probability that it is latched increases [Baum-05].

Previous work has shown that combinational logic soft errors caused by latching SETs




(a) (b)

Fig. 2.4. (a) Soft error rate per logic gate for SRAM, latch and combinational logic circuits indicating and increase in the SER of logic circuits with technology scaling (after [Shiv-02] and (b) Error rates in combinational and sequential logic as a function of frequency (after [Buch-97]).

increase with technology scaling [Shiv-02, Buch-97]. Fig. 2.4(a) shows the SER per logic gate for different types of circuits. For memory and latch circuits, the per-bit SER decreases slightly with technology scaling and can be attributed to the faster scaling in

the cross-sectional area than the critical charge of the cell. However, for logic circuits, the SER is predicted to increase with scaling and for technologies beyond 65-nm it may dominate SER from memory and latch circuits [Shiv-02]. Fig 2.4(b) shows the trends in the relative contribution to error rates for combinational and sequential logic as a function of frequency, indicating an increase in combinational logic SER with increasing frequency [Buch-97]. Gadlage et al. have also observed an increase in the experimentally measured SET cross-section for combinational logic circuits with increasing frequency [Gadl-04].

A sequential element such as a latch is vulnerable to a single-event when it not driven by the inputs, i.e., during the period for which the clock is low. As stated in [Buch-97], for low frequencies, the upset rate for a given sequential element is independent of the clock frequency. However, the propagation of an upset from an upstream latch to a downstream latch depends on the number of elements between the latches and on clock frequency. Seifert et al. have shown that with increases in the clock frequency, the error rates for sequential circuits decreases [Seif-04]. In [Seif-04], the authors computed the sequential SER by striking an upstream latch at different instances of time and by observing the cases for which the next downstream latch latches an error. The window during which the downstream latch is vulnerable decreases with increasing frequency. This is because the relative contribution of propagation delay between latches becomes a larger fraction of the clock cycle, reducing the period of the clock cycle that is vulnerable to single-events. For this dissertation, the focus is mainly on combinational logic soft errors caused by SETs in logic circuits. For further details on error rates from sequential circuits the reader is urged to refer to [Seif-04, Buch-97] and references therein.

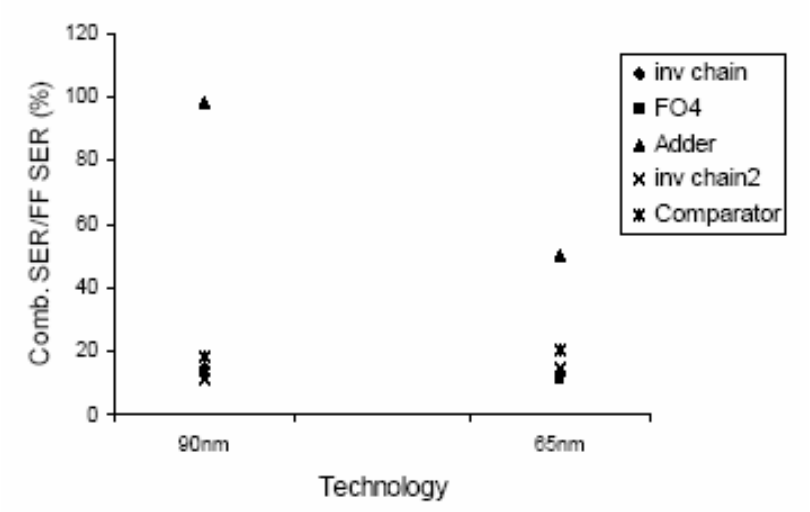



Fig. 2.5. Percent combinational logic SER for different types of logic circuits as a function of flip-flop SER for technology scaling from 90-nm to 65-nm, after [Seif-06].

As mentioned in chapter I, some researchers indicate that logic soft errors may not scale as rapidly for advanced technologies or may even reduce with scaling for sub 100-nm technologies due to a reduction in the scaling of supply voltage and clock frequencies [Seif-06]. Fig. 2.5 shows a plot of the SER for different combinational logic circuits as a function of the flip-flop SER for technology scaling from 90-nm to 65-nm [Seif-06]. While the per gate logic SER may reduce slightly depending on frequency and supply voltage scaling trends, the overall contribution to the chip level SER may still be significant especially with higher packing densities. Moreover, as pointed out in [Seif-06], the alpha particle contribution to logic SER may increase significantly with reduction in the critical charge with scaling and hence it is important to understand and characterize scaling in SETs.

Some researchers indicate that for higher frequencies, or for advanced technologies, the error rates for combinational logic circuits may begin to dominate [Buch-97, Bene-04]. An increase in clock frequency within a given technology would result in latching more

SET events due to the setup time remaining constant, increasing logic error rates. Conversely, with scaling, the reduction in the setup-and-hold times, along with an increase in clock frequency, may result in the latch window masking effects to not scale significantly. This would imply that the per logic gate SET error rates should roughly remain the same or decrease slightly with technology scaling if clock frequency and latch setup times are alone considered to impact SET error rates. However, the effect of lower charge requirements to represent a logic HIGH state with scaling and a reduction in the restoring drive strength may yield relatively wider transients, resulting in more SETs being latched as errors. Thus, it is important to understand scaling trends in SET pulse widths.

The probability that a SET will result in an error depends on the propagation distance through the combinational logic circuit and the arrival time of the SET at the latch input [Kaul-92, Sata-94, Buch-97, Mass-00, Buch-01, Seif-01, Mavi-02, Dodd-03, Bene-04]. Wider pulses have a greater probability of being present at the latching edge of the clock. Thus, characterizing transient pulse width is of paramount importance in both determining and mitigating single-event effects for advanced technologies.

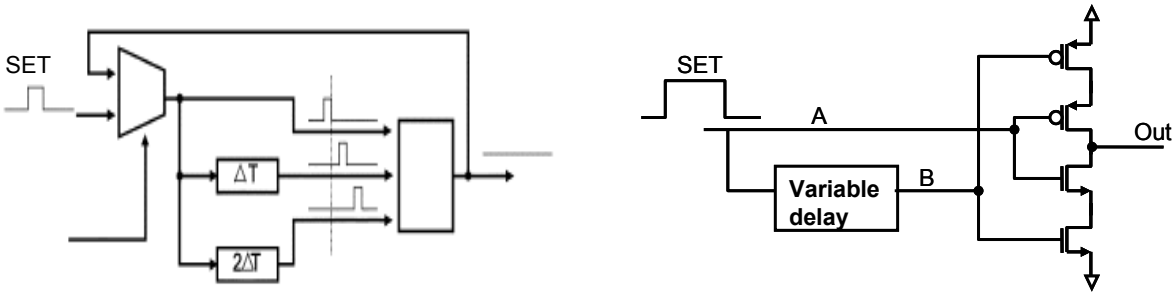
Moreover, while error-correction codes and latch-hardening designs have been developed to mitigate the effect of SEUs in memory elements, protection against SETs is quite difficult and involves considerable performance penalties [Nico-03]. A more manageable approach is to design limited protection against SETs through a targeted performance trade. Such tradeoff decisions require detailed knowledge of the SET mechanisms and attributes, specifically SET pulse widths [Nico-03].

Transient pulse width is determined by many factors, including the nature of the ionizing particle, technology used, location of the strike, and incident angle [Buch-01, Mass-93, Dodd-99, John-99 and Reed-94]. Modern sub-micron ICs are vulnerable to ionizing alpha particle and heavy-ion strikes and also to terrestrial neutrons that deposit charge through indirect ionization. Different ionizing particles interact differently with the silicon to deposit charge. Alpha particles that come from the radioactive decay of packages used for ICs have been a source of SETs through direct ionization in silicon. Energetic neutrons and protons can produce SETs indirectly through elastic scattering or a nuclear reaction in silicon. Low energy neutrons can also interact with the boron (specifically, boron-10) in a semiconductor device, producing reaction products that can cause an SET. Cosmic ray heavy ions are also a source of SETs. The charge deposited by the different ionizing species varies greatly and this may affect the transient pulse width. For example, the charge deposited by the products of neutron-induced reactions (25-150 fC/μm) is much greater in magnitude than that deposited by alpha-particles (4-16 fC/μm) and hence may pose a greater threat [Baum-05]. Likewise the angle of the incident ionizing particle also significantly affects the charge collected and hence the pulse width.

*Previous SET Characterization*

Through the use of mixed-mode simulations, Dodd et al. have characterized scaling trends in SET pulse widths for bulk and SOI technologies for processes ranging from 0.25-µm to 0.1-µm [Dodd-04]. Their results indicate transients of the order of 1 ns for bulk technologies at LETs greater than about 50 MeV-cm$^2$/mg. The simulation results presented in [Dodd-04] also suggest the presence of significant transients at LETs as low as 2 MeV-cm$^2$/mg at the 100-nm bulk process and the authors predict an increase in susceptibility to alpha particles with technology scaling beyond 100-nm.

Researchers have also experimentally characterized transient pulse widths using multiple latches with delayed signal paths [Eato-04] and/or delayed clock signals (Fig. 2.6 (a)). Guard-gate-based techniques have also been used to measure SET pulse widths as shown in Fig. 2.6 (b) [Baze-06]. In such techniques a delay element is tuned to a certain value and the circuit measures all SETs longer than the delay. The techniques thus measure the event cross section for SETs greater than a certain threshold. In such techniques the design of the delay element is critical and any variations in the delay value




(a) (b)

Fig. 2.6 (a) Variable temporal latch technique and (b) guard gate based technique for characterizing the width of SET pulses. In such techniques a delay element is tuned to match the width of the SET pulse. (after [Eato-04] and [Baze-06]).

can affect the measurement. Moreover, there has been little agreement on the range of SET pulse widths that are measured using the different techniques. For example, at the 130-nm technology node, pulse widths from a few hundred picoseconds [Baze-06] to several nanoseconds [Bene-06] have been reported. Baze et al. concluded that the majority of transients are 500 ps or shorter (with very few transients greater than 1 ns) in the 130-nm process based on SET measurements using the guard gate technique [Baze-06] while Benedetto et al. have observed transients greater than 2.5 ns long in the 130-nm process based on measurements using the variable temporal-latch technique. Furthermore, Benedetto et al. have predicted an increase in transient pulse width with technology scaling [Bene-06].

Another approach for SET pulse width measurement that has been previously reported is the use of a chain of cell copies that are monitored by latches to characterize the pulse width in terms of multiples of the individual cell delay as shown in Fig. 2.7 [Nico-03]. In this approach, the latches are clocked continuously to obtain information about the state of the cells. Since there are limitations to the maximum clock frequency that can be applied, it can be difficult to capture a very fast SET pulse using this approach. Transient current pulses have also been measured directly using oscilloscopes [Scho-98, Ferl-05].

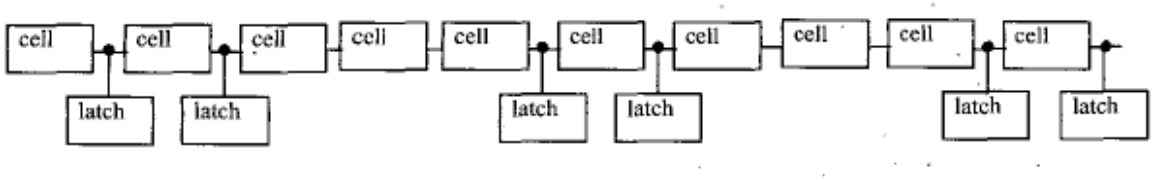



Fig. 2.7. Chain of cell copies monitored by latches that are clocked continuously to capture information of the width of an SET pulse, after [Nico-03].

Such direct measurements are difficult to perform because of pulse distortion due to the capacitance of the measurement equipment and require costly experimental setup. While such techniques are suitable for measurement of laser-induced pulses, they are much harder to use with heavy-ions. This is because such measurements are made on single transistors and they are best suited for measurements where the ion strike location can be chosen. It is difficult to make these measurements with heavy ions due to the random nature of the ion strikes.

The observable pulse width is a function of not only the base technology, but the circuit topology through which it propagates [Gadl-04], and the circuit operating parameters (such as supply voltage [Bene-06]). The measurement circuit used may even influence the measurement itself. Even if the influence of these parameters is eliminated, a fairly large statistical distribution of the collected charge has been observed based on the random nature of strike location relative to the affected node [Ferl-06]. Previous SET pulse width measurements, however, have not been able to capture the statistical distribution precisely.

In this work, a new SET test circuit is described that can complement the techniques previously proposed. This test circuit can characterize the width of SET pulses without the need for an external trigger or multiple laser strikes. The basic principle of operation of this circuit is similar to the one proposed in [Nico-03] but incorporates a *self-triggering* mechanism that does not require an outside signal to determine the presence of an SET pulse. This test circuit captures the SET pulse in a series of latches, which can be easily read out to determine the width of the pulse. This circuit technique can be used in CMOS and BiCMOS processes (including SOI technologies) regardless of feature size or

operating speed and can also be used for characterizing other spurious signals such as noise or cross-talk pulses. This circuit has been implemented in 1.5-µm, 0.35-µm, 180-nm, 130-nm, and 90-nm bulk CMOS processes and in a 180-nm SOI process and has been tested with different energetic particles. This dissertation focuses on test results from the 130-nm and 90-nm bulk CMOS processes.

# CHAPTER III

## AUTONOMOUS PULSE-WIDTH CHARACTERIZATION

### *Pulse Capture Circuit*

A common parameter for specifying the performance of a digital IC is the propagation delay associated with an inverter, designated as one inverter-delay. The test circuit described here characterizes the SET pulse width in units of inverter-delays. Pulse width is defined as the width of the pulse measured at the inverter threshold ($V_{dd}/2$). If an SET pulse of sufficient duration is input to an inverter chain, it will propagate through each inverter after a specific time delay (e.g., it will reach the third inverter after two inverter-delays, it will reach the fifth inverter after four inverter-delays, etc). This is shown in Fig. 3.1 where the leading edge of the transient pulse is shown to reach the inputs of inverters in a chain at different instances of time. As time progresses, this transient propagates through a series of inverters. Thus, at any instant of time, a certain number of inverters

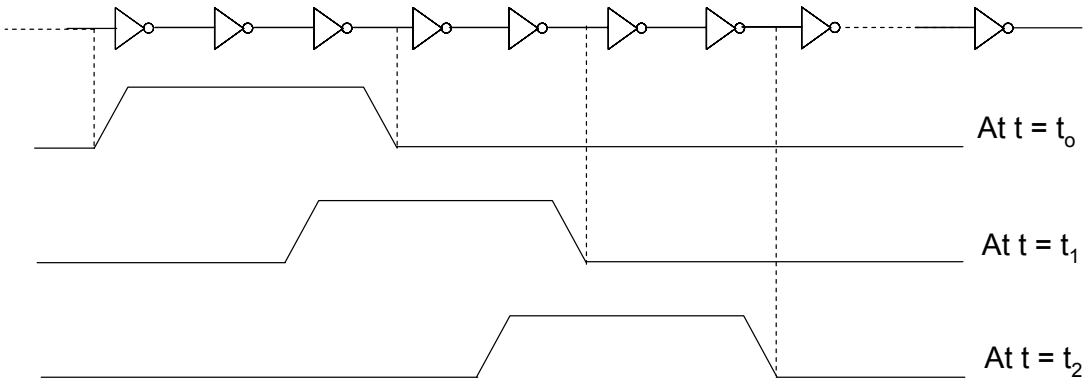



Fig. 3.1. Pulse propagation through a series of inverters. Time instances $t_0$, $t_1$, $t_2$ are 2 inverter-delays apart

have their outputs affected/switched. This number of affected inverters is proportional to the transient pulse width. For extremely short pulses, the pulse gets attenuated as it propagates through logic gates. As discussed in [Mass-08], pulses wider than the sum of the logic transition times (rise and fall) of a gate propagate through the gate without attenuation, while pulses shorter than this transition time propagate with varying attenuation. The minimum pulse width required for propagation through multiple levels of logic is discussed in more detail later in this chapter.

Fig. 3.2 illustrates an example of pulse propagation through a series of inverters when the SET pulse is three inverter-delays long. The pulse affects three inverter outputs as it propagates through the chain. If the number of such inverters whose outputs are affected by the SET pulse can be determined at any instant, the pulse width can be estimated as a multiple of inverter-delays. The number of inverters affected by the SET pulse is determined by the ratio of the SET pulse width to the individual stage delay. Let us assume that this ratio is the sum of a whole number, n, and a fraction, $f < 1$. If the fraction

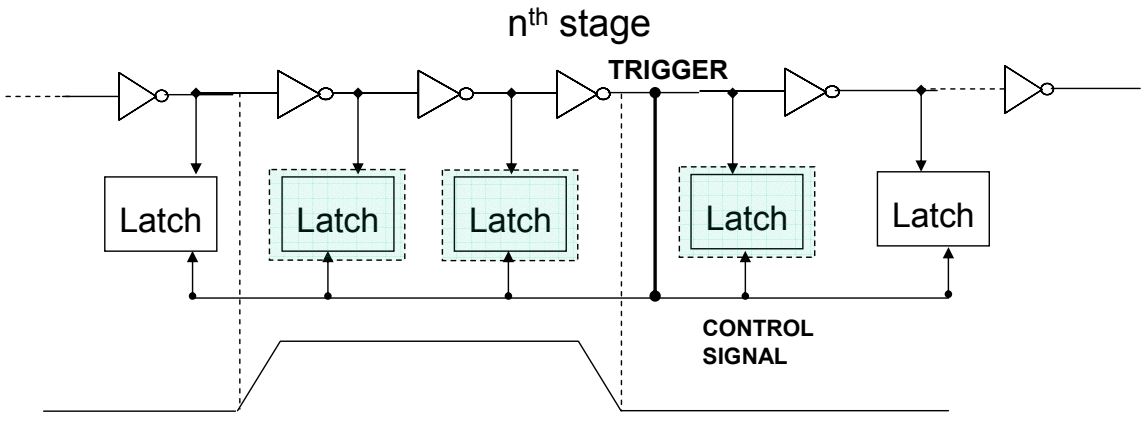



Fig. 3.2. The output of the $n^{th}$ stage can be used to provide hold signal for latches to freeze the data and the SET pulse

is zero, then the number of affected stages is just n. For $0 < f < 0.5$, the SET pulse would have just arrived at the $(n+1)^{th}$ stage, starting to switch it in the opposite direction, but the output of this stage would not be stabilized and would revert back to the original state when the trigger signal is enabled. Thus the number of affected stages would still be n. However, for $0.5 < f < 1$, the output of the $(n+1)^{th}$ stage will be nearing completion of switching to the opposite state and would latch the switched state when the trigger signal is enabled. In this case the number of affected stages would be n+1. Simulations also showed that for all pulse widths between [($n$–0.5) × stage delay] to [($n$+0.5) × stage delay], the number of affected stages is $n$. Thus the pulse width determined will be accurate to within ± half the propagation delay of an individual stage.

To measure the SET pulse originating from (for example) a target combinational logic circuit, it should first be fed to the measurement circuit composed of a chain of inverters. Next, the number of inverter stages that are affected by this SET pulse at any given instant of time must be measured. This can be accomplished if the SET pulse is frozen when it is within the measurement chain of inverters. Latches can be used to freeze the state of the inverter outputs at any given instant. Thus, to capture the affected outputs from a chain of inverters, the output of every inverter is connected to an asynchronous latch as shown in Fig. 3.2. As the SET pulse propagates through an inverter, the data stored in its respective latch will change. However, once the SET pulse passes, the inverter output and latch data will revert to their original states. (Note that the additional loading due to the latch at the inverter output will alter the pulse characteristics. Hence, capacitance at the latch input must be minimized and accounted for in the inverter delay for accurate measurement of pulse width.) If the latches are placed in a *hold* mode while

the SET pulse is within the inverter chain, each latch will retain the logic state of its respective inverter.

For laser tests, the exact instant when the hit takes place is known and the latches can be placed on *hold* after a certain delay, such that the SET pulse is guaranteed to be present within the inverter chain. However, for heavy ion testing, information regarding the hit time and hit node are usually not available. To address autonomous operation in such cases, the output of an inverter stage can be used as a trigger signal. This would cause additional loading at this inverter stage. However, as will be discussed later in this section, latches were used for both propagating the SET pulse and for its capture, and the trigger signal can be obtained from an inverter of the latch not directly in the path of the propagating SET pulse to minimize loading of the SET pulse. To make this circuit *self-triggering*, a transition at the output of the $n^{th}$ stage (due to SET) can be used to trigger the latches to hold the states of the inverters as shown in Fig. 3.2. As the output of the $n^{th}$ stage triggers the *hold* signal internally, precise information regarding the hit time (or location) is unnecessary. Any hit on stages beyond the trigger stage does not affect the trigger stage output. Thus, to latch an SET pulse, a hit must take place on a stage before the trigger stage.

The instant when the SET pulse is latched, the initial hit stage may or may not have recovered fully. If the initial stage has recovered fully when the pulse is latched, the pulse width measured is the actual pulse width (to within the accuracy of the measurement). However, if the initial stage has not recovered, it is possible that the charge collection is still continuing and the actual pulse width could be longer than the one measured. For laser tests the information regarding the state of the hit node is

available. However, for heavy ion tests, the hit stage is not identifiable, and hence it can not be ascertained whether the hit stage has fully recovered or not. To address this uncertainty, a delay is introduced in the trigger signal. In addition, more inverter stages beyond the trigger stage are added to allow the SET pulse to propagate further. Thus, the delay on the trigger signal allows the SET pulse to propagate beyond the trigger stage. When the delayed trigger signal latches the SET pulse, the SET pulse may have propagated beyond the trigger stage. How far the SET pulse travels along the inverter chain is determined by the delay in the trigger signal. The delay in the trigger signal should be equal to the maximum SET pulse width expected for measurement. If the SET pulse has moved beyond the trigger stage, one can safely say that the estimated pulse width is the actual pulse width (within the accuracy of the measurement) irrespective of the hit node. This is because a hit on a stage beyond the trigger stage can not initiate a latching process.

To increase the probability that an SET will be created in a given test environment, an array of target circuits, which functions as the source of SETs, precedes the measurement circuit as shown in Fig. 3.3. The target circuit also allows the trigger signal to be taken from the 1$^{st}$ stage of the measurement circuit and delayed in time to allow the SET to propagate completely into the measurement chain of inverters. Depending upon the designer's requirement, the target circuit can be composed of any combinational logic network. In this work, a minimum drive-strength inverter chain was used for the target since it yields SETs similar to those in standard ICs and such a chain will propagate SETs with little attenuation.

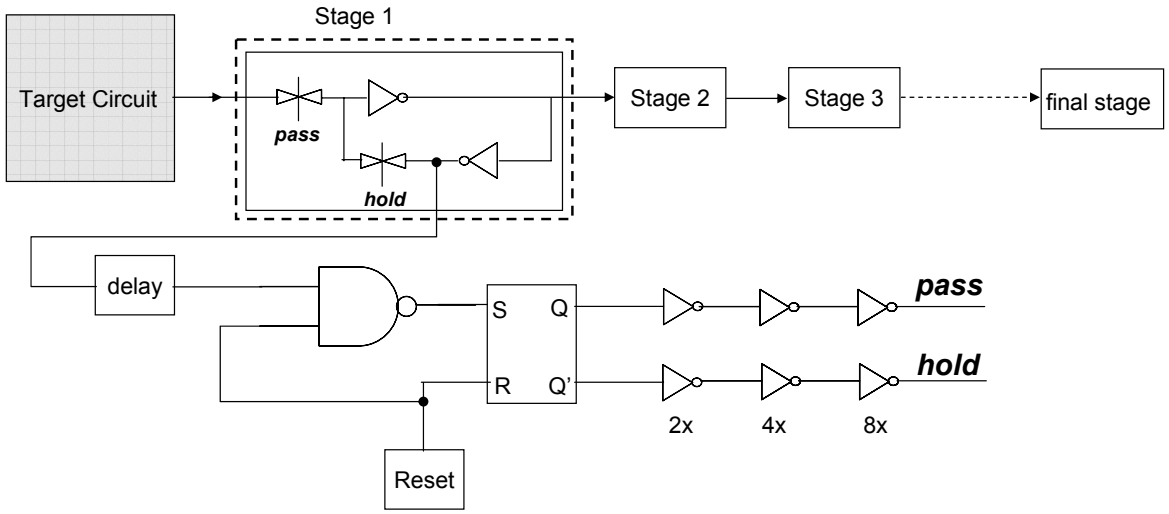



Fig. 3.3. Test structure showing individual stages along with the trigger/reset circuit. Highlighted region shows the internal circuit of individual stages

The design of the complete test circuit (composed of the target circuit and the pulse measurement circuit) is shown in Fig. 3.3. To simplify the circuit and reduce loading effects, the individual inverter stages in the measurement circuit were implemented using the inverting outputs of standard CMOS pass-gate latches. The operation of the test circuit is straightforward. An energetic particle hit in the target circuit creates an SET pulse that propagates to the measurement circuit. The measurement circuit essentially forms a series of latches that freeze the SET pulse for measurement (Fig. 3.3). The latches in the measurement circuit are initially in the SET-propagate phase. During the SET-propagate phase, the pass signal is ON and the hold signal is OFF, which allows a pulse to propagate through the measurement chain of inverters and pass-gates. When the leading edge of the SET pulse reaches the 1st stage of the measurement circuit, it creates a trigger signal that is delayed in time and hence the SET pulse continues to propagate through the inverters and pass-gates. Note that the trigger signal is obtained from an

inverter in the latch that is not directly in the SET propagation path to minimize loading of the SET pulse. When the trigger signal reaches the SR flip-flop, it turns off all pass-gates by inverting the pass signal and freezing the data in the latches by turning on the hold signal. The SET pulse width is directly proportional to the number of latches whose output is affected. Once the latch outputs have been read out, a reset signal is used to initialize the pass and hold signals and make the circuit ready for measuring the next pulse.

Fig. 3.4 illustrates measurement of an SET pulse. The chain of inverters shown in Fig. 3.4 represents the inverters in pulse capture latch stages that propagate the SET. An SET pulse that is about four times the propagation delay of an inverter stage is input to this circuit. As soon as the leading edge of the SET arrives at the output of the first stage, it triggers a control signal. Since the control signal is delayed in time, it allows the SET to propagate beyond the first stage. Finally when the control signal triggers the pulse capture latches, it causes the SET to freeze somewhere within the chain of inverters. The waveforms in Fig. 3.4 indicate that the SET pulse is between stages 16 and 19 as their outputs have a flipped state. Output of stage 15 returns back to its original state and the SET pulse has not reached stage 20. In this case the SET pulse width would be estimated as two times the propagation delay of a single latch stage which is the width of the input SET.

Latch upsets due to direct ion hits on the latches can corrupt the measurement. The total sensitive area of the target circuit was about 20 times larger than the total sensitive area of the latches in the data path. This, along with the fact that only latch upsets that occur after an SET event gets captured but before the data are read-out (and the circuit is reset)

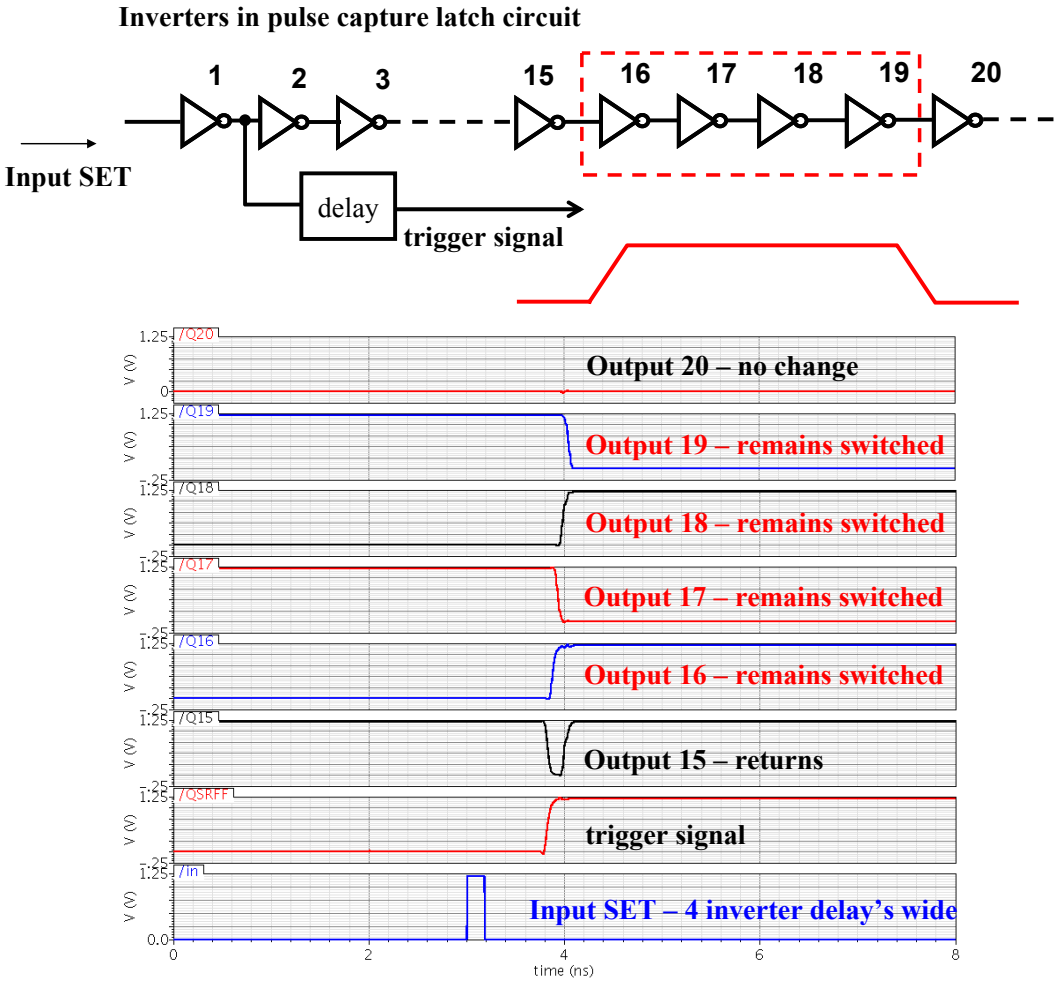



Fig. 3.4. Simulation results illustrating capture of an SET pulse. SET pulse width proportional to number of latches with a flipped state.

are a concern, implies that latch errors can be neglected. This is because the latches themselves act like a chain of inverters that propagate the SET pulse until a trigger signal causes it to latch the data. Once data are latched, they are immediately read-out and a reset pulse causes the latch to return to the pulse propagating phase during which time a latch upset would result only in an SET. Since the frequency of operation is much higher than the rate at which events are created in this process, the probability of a latch upset during the time interval when an SET is captured and before the circuit is reset is very

low. Also, most of these latch upsets can be identified by looking at the data pattern and hence can be discarded. The data pattern without any SET will be a string of thirty two alternating 1s and 0s – "101010101010…". If an SET pulse that is 5 stages wide is created, then the output looks like "10101<u>10101</u>10…". The start and end of an SET pulse is marked by two consecutive stages having the same value (except when the pulse is only a single stage wide). Latch upsets that cause the output data to read differently can easily be identified – for example if the second latch is upset during the data-read phase, then the data would read "1<u>1</u>101<u>1010</u>10…" – which does not correspond with a normal SET event and hence such data can be discarded. For the experimental measurements we did not observe even a single case where the data looked spurious.

The latches in the data path are asynchronous and do not use a clock signal. Rather they are controlled or triggered by the SET pulse. The control logic consists of an SR flip flop that provides the trigger signal to the latches and is also controlled by the SET pulse. A direct strike on this would only result in triggering a measurement. However, if no SET event has occurred, this would result in measuring the standard sequence of alternate ones and zeroes corresponding to outputs of a chain of inverters and would indicate a false measurement.

Finally, a parallel-in-serial-out shift register is used to serially output the data stored in the pulse capture latches. This shift register operates on the negative edge of an external clock signal. This shift register is also sensitive to strikes only during the time interval an SET event is captured but before the data are read out. Any strikes on the latches or on the clock buffers during such a time interval can affect the data that is read out. As

explained earlier, by examining the data pattern most of these errors can also be identified.

*Test Chip Designs*

Integrated circuits with the above test structure were designed and fabricated in 1.5-µm, 0.35-µm, 180-nm, 130-nm and 90-nm bulk CMOS processes and in a 180-nm SOI process. These designs are similar except for the number of inverters in the target circuit. This dissertation focuses on the results from the 130-nm and 90-nm bulk processes. Propagation and attenuation of SET pulses through the target and measurement circuits were analyzed using the Cadence Spectre® simulator [Spec-03]. The parasitic resistances and capacitances were extracted from the layout and were included in the circuit simulations. The delay of a single latch stage was found to be about 65 ps in the 130-nm process and about 55 ps in the 90-nm process based on circuit simulations. The delay of a single inverter stage is about 25 ps in the 130-nm process and about 21 ps in the 90-nm process. This indicates that additional loading has considerably increased the delay of the pulse measurement latch stages.

As mentioned earlier, Massengill et al. have identified the minimum pulse width for infinite propagation to be the sum of the characteristic rise and fall time of a logic gate [Mass-08]. A minimum pulse width equal to the sum of the logic transition times is required to ensure the full rail-to-rail swing that is needed for unattenuated propagation [Mass-08]. As the ratio of the logic transition time to the propagation delay of a gate is a constant, the minimum pulse width can also be expressed in units of the propagation delay time. Since ring oscillator measurements can be used to obtain the propagation

delay of a logic gate, the analysis presented here can be used to identify the minimum pulse width that would propagate through the SET pulse capture circuits. The rise and fall times for an inverter for logic swing between 10% and 90% of the supply voltage and the propagation delay times (low-to-high and high-to-low) can be expressed using the following first-order equations [Uyem-99].

$$t_{rise} = R_P \times C_L \times \ln(9)$$
$$t_{fall} = R_N \times C_L \times \ln(9)$$

$$t_{plh} = R_P \times C_L \times \ln(2)$$
$$t_{phl} = R_N \times C_L \times \ln(2)$$

where

$t_{rise}$ and $t_{fall}$ = rise, fall times

$t_{plh}$ and $t_{phl}$ = propagation delay low - to - high and high - to - low

$R_P$ = equivalent PMOS resistance

$R_N$ = equivalent NMOS resistance

$C_L$ = load capacitance

For a symmetric design, $R_N = R_P$ and hence $t_{rise} = t_{fall}$ and $t_{plh} = t_{phl}$. From the above equations, the ratio of the logic transition time to the propagation delay time is ln(9)/ln(2) which is about 3.1. Circuit simulations with higher order effects included indicate that the ratio of the logic transition time to the propagation delay time is about 2 for minimum sized inverters designed in the 130-nm and 90-nm processes. Thus the minimum pulse required for unattenuated propagation in these processes can also be expressed as follows.

$$\text{Min Pulse Width} = t_{rise} + t_{fall}$$
$$= 2 \times (t_{plh} + t_{phl})$$
$$= 4 \times t_p, \text{ assuming } t_{plh} = t_{phl} = t_p$$

Thus the minimum pulse width for unattenuated propagation through an infinite number of logic gates is about four times the propagation delay of a single logic gate. In this work, a total of thirty-two pulse capture latch stages were used for SET measurement and this was preceded by a long chain of target inverters. The propagation delay through the pulse capture latches was found to be about two and a half times that of the propagation delay through the inverter stages due to additional loading in the pulse capture latches.

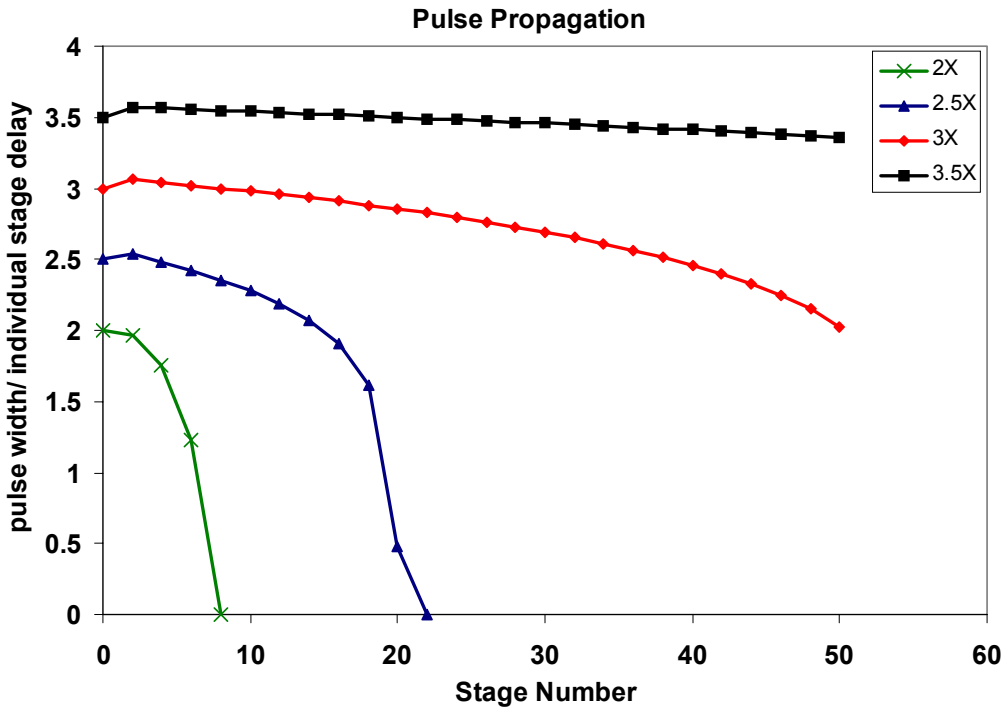



Fig. 3.5. Propagation of a transient pulse through a long chain of identical logic gates. The transient pulse width normalized to an individual gate delay is plotted as a function of the logic stage number.

Thus the minimum pulse width for propagation is determined by the pulse capture latch stages in the SET measurement circuit. Simulations showed that SET pulses greater than approximately three times the propagation delay of a single measurement latch stage propagated with less than about 10% attenuation through the thirty-two measurement

latch stages in both the 130-nm and 90-nm processes. Thus for such SETs the measured width, within the accuracy of measurement, is equal to the actual SET width. SET pulses less than this width are attenuated by greater amounts, depending on the initial pulse width. Fig. 3.5 shows a plot of the transient pulse width normalized to an individual measurement stage delay as a function of the logic stage number for propagation through fifty identical stages. The pulse width broadening effect caused by changes to the body potential of off-state devices of floating body or weakly contacted devices will be discussed in Chapter V.

A ring oscillator consisting of pulse measurement circuit latch stages was fabricated to obtain the precise delay of an individual latch stage as shown in Fig. 3.6. The design of the ring oscillator and its output waveform are shown in Figs. 11 (a) and 11 (b). This delay was measured to be about 120 ps for the 130-nm process when operating at the nominal supply of 1.2 V. For the 90-nm process, the individual stage delay was found to be about 100 ps. The nominal operating voltage for the 90-nm process used in this work is also 1.2 V. The measured delays are about a factor of two longer than the values obtained through circuit simulations. Since parasitic resistances and capacitances were included in the circuit simulations, lower drive currents for the fabricated devices may be responsible for the observed longer delays.

When the trigger signal was enabled in the measurement circuit, the leading edge of the pulse was latched at the 22$^{nd}$ stage. This enabled pulse width measurements from 120 ps (1 stage) to about 2520 ps (21 stages, excluding the first stage) for the 130-nm process. The measurement range for the 90-nm process is from 100 ps to about 2.1 ns. The accuracy of measurement is about ±½ the individual latch stage delay.

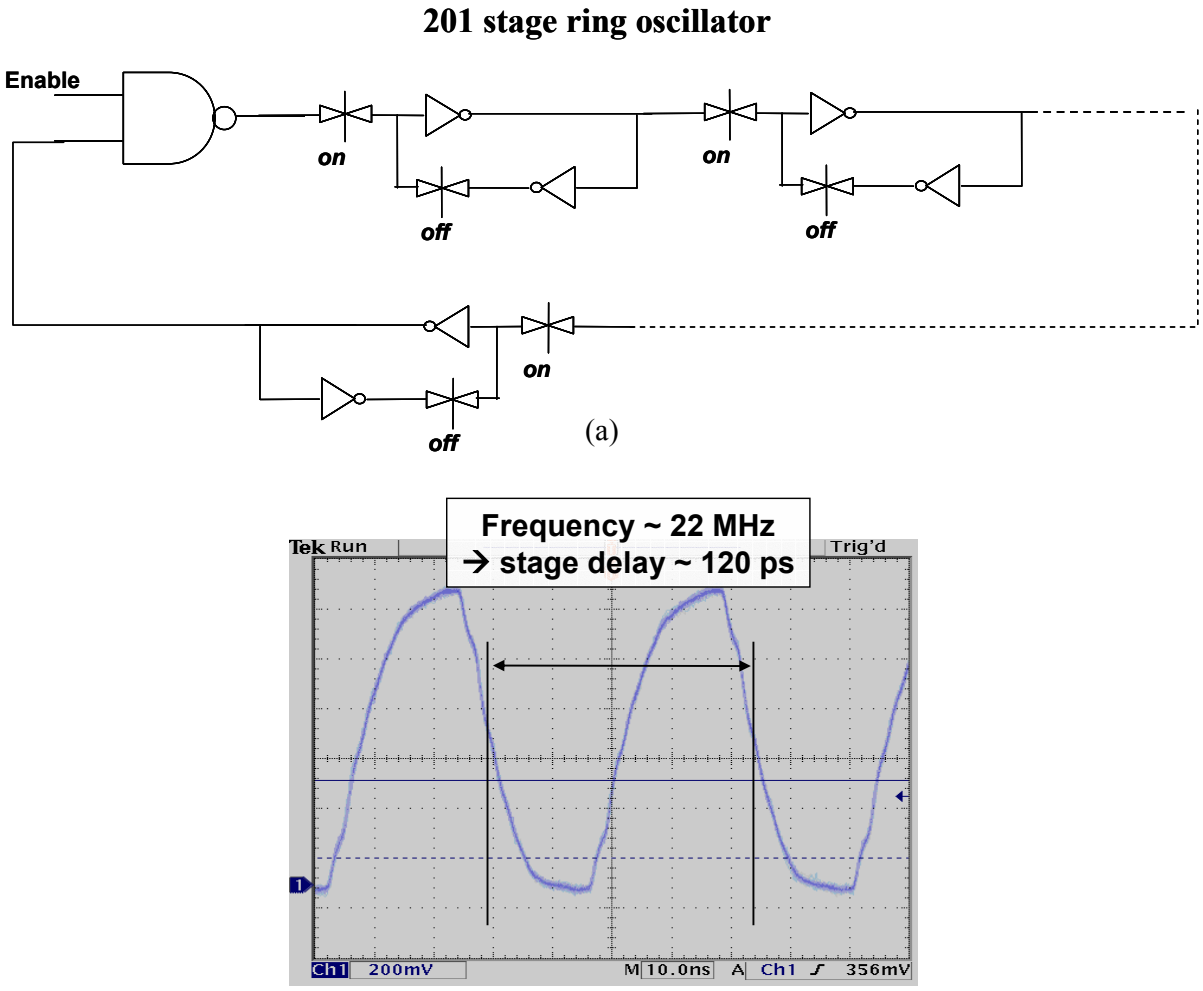



Fig. 3.6 (a) Ring oscillator design composed of the pulse measurement circuit latch stages and (b) output of the ring oscillator designed in 130-nm measured using an oscilloscope. It indicates that the delay of a single latch stage is about 120 ps.

*Experimental Verification of Pulse Capture Circuit Operation*

The operation of the pulse capture circuit was verified with the use of a pulse generation circuit, as described in [Bala-08]. Balasubramanian et al. have developed a transient pulse generation circuit that is capable of generating transients with different pulse widths with the use of current-starved inverters. An external control voltage controls the delay of the current-starved inverters. In the test chip designed in the 180-nm process, both the pulse-generation and pulse-capture circuits were included. The design enabled the output of the pulse-generation circuit to be fed to the pulse-capture circuit for measurement. In this 180-nm process, the simulated and measured delay of a single latch stage were about 135 ps and 150 ps respectively and agrees more closely than the simulated and measured delays for the 130-nm and 90-nm technologies. Fig. 3.7 shows

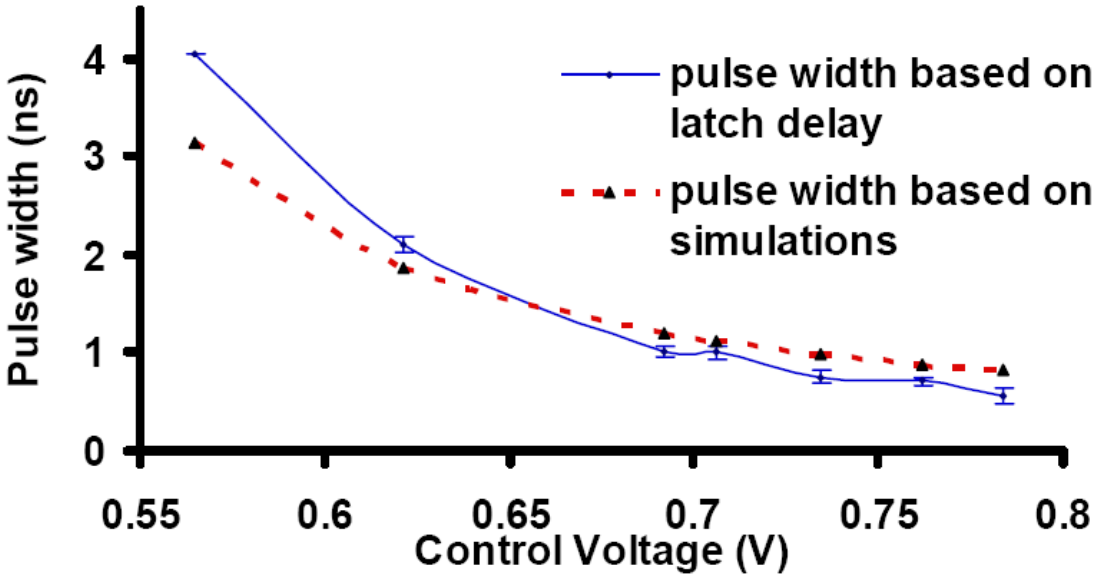



Fig. 3.7. The simulated width of the transients generated by the pulse generate circuit for various control voltage values corresponds well with the experimentally measured transient widths with the use of the pulse capture circuit outlined in this work, after [Bala-08].

plots of the simulated and measured transient widths as a function of the control voltage applied to the current-starved inverters. The transient widths were experimentally measured with the use of the pulse capture circuit. Fig. 3.7 indicates good agreement between the simulated and measured transient widths over a wide range and suggests that the pulse capture circuit provides good estimates of the actual pulse widths.

# CHAPTER IV

## HEAVY-ION TEST RESULTS

Heavy-ion tests were performed on the 130-nm and 90-nm SET test chips at different cyclotron facilities. Test results showing the distribution of SET pulse widths for various ions are reported in this chapter along with some discussions about the measured SET width distributions. The next chapter provides detailed analysis of the technology scaling trends on SET pulse widths based on experimental measurements and 3D-TCAD simulation results.

### *Heavy-Ion Tests – 130-nm*

Table 4.1. Details of the heavy-ion test – 130-nm

| Ion | Angle (deg) | Effective LET (MeV-cm$^2$/mg) | Ion Energy (MeV) |
|---|---|---|---|
| Ne | 0 | 3.45 | 216 |
| Ne | 60.5 | 7 | 216 |
| Ar | 0 | 9.7 | 400 |
| Ar | 60.9 | 20 | 400 |
| Kr | 0 | 31.2 | 886 |
| Kr | 49.3 | 48 | 886 |
| Xe | 0 | 58.7 | 1403 |
| Xe | 38.5 | 75 | 1403 |
| Xe | 54 | 100 | 1403 |

The 130-nm ICs were tested with heavy ions at the Cyclotron facility at Lawrence Berkeley National Laboratory [Nara-07]. The circuit was tested with ions at various angles to achieve an effective LET (linear energy transfer) range from about 3.5 to 100 MeV-cm$^2$/mg (see Table 4.1). At each LET, the IC was tested to a fluence of $1\times10^8$ ions/cm$^2$. At an LET of

3.5 MeV-cm$^2$/mg no SET events were measured and at 7 MeV-cm$^2$/mg only a statistically insignificant number of events were recorded. Fig. 4.1(a) is a box plot representing the average SET width, the standard deviation and the minimum and maximum SET widths for a range of LETs. The standard deviation data from Fig. 4.1(a) clearly show that most of the SET pulses created are below 1 ns. Fig. 4.1(b) shows plots of the number of SETs measured at each LET and the total SET cross section per inverter, which is the ratio of the total number of SETs measured at each LET to the fluence divided by the number of target inverters.

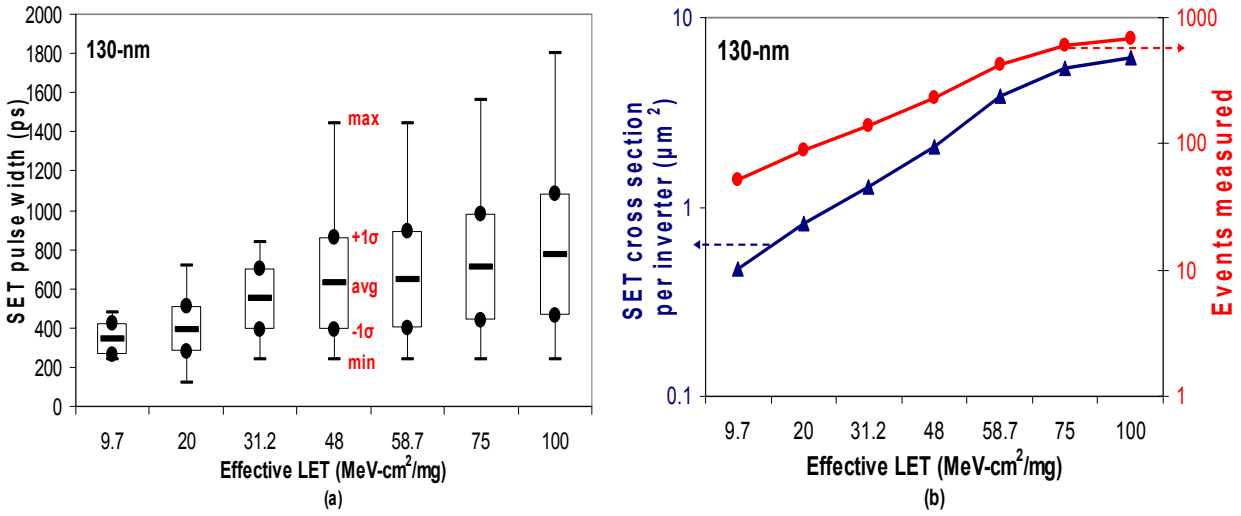



Fig. 4.1 (a) Box plot indicating the average, ± 1 standard deviation, minimum and maximum SET pulse-width as a function of LET for the 130-nm process. (b) Total SET cross section per inverter and the number of events measured as a function of effective LET.

Fig. 4.2 shows a histogram of the distribution of the event cross section per inverter as a function of LET. Event cross section per inverter is defined here as the ratio of the number of measured SET pulses with a given width to the total fluence, divided by the

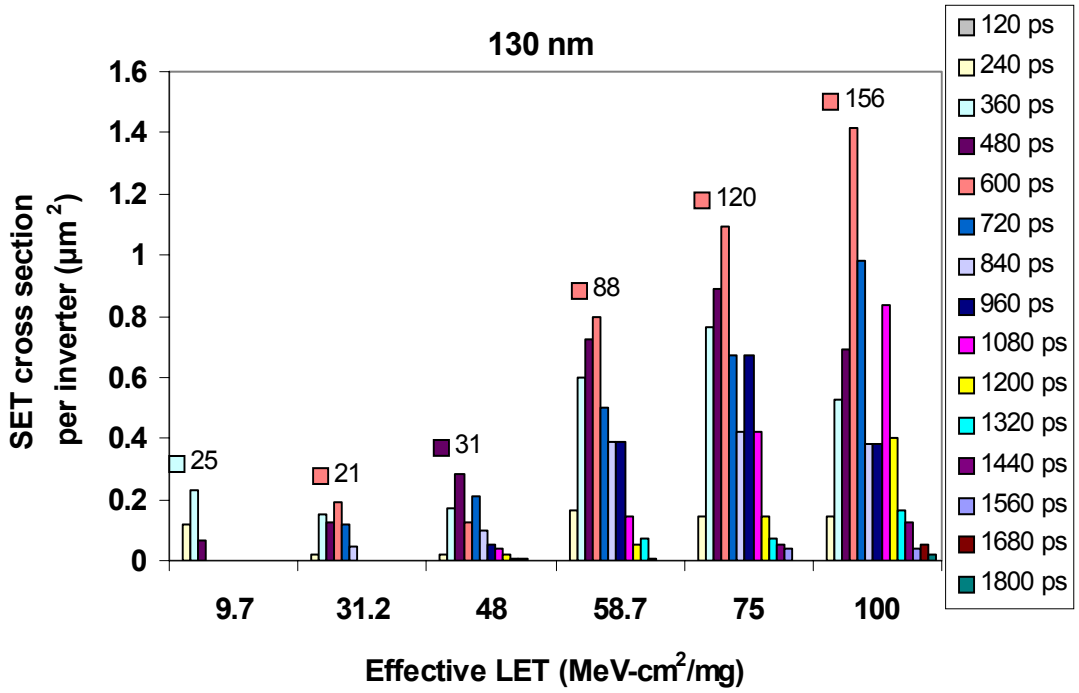



Fig. 4.2 Distribution of event cross section per inverter as a function of LET for the 130-nm process. The data labels on the chart indicate the maximum number of SET pulses of a given width measured at each LET.

number of target inverters. The SET pulse width for a given LET is not a constant and varies over a wide range. This is because the pulse width created depends on the collected charge, which varies depending on the location of the strike with respect to the sensitive drain.

Previous work indicates that the distribution of the collected charge follows a Gaussian profile (see Fig. 4.3) [Ferl-06, Hube-06]. In [Ferl-06] the collected charge by a circuit node after an ion strike was measured directly. In [Hube-06], Monte Carlo based simulations were used to show the distribution of amplitude and duration of the current transient due to charge collection for 63 MeV neutron interactions in silicon. The collected charge was then computed using the current transient waveforms and the distribution of the collected charge looks similar to a Gaussian profile. The distribution of

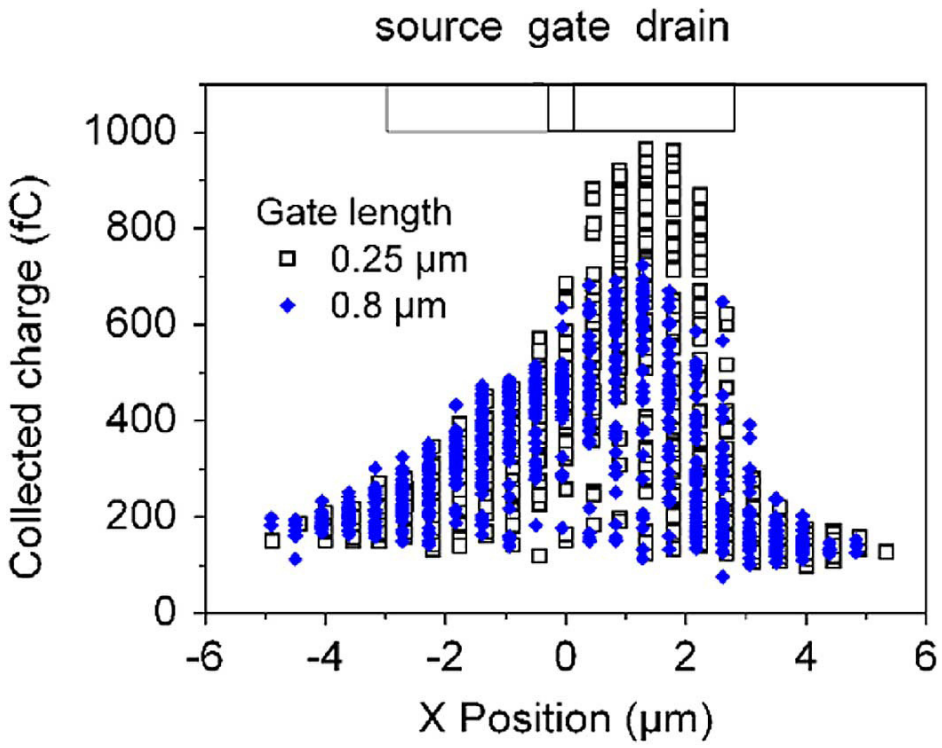



Fig. 4.3 Distribution of collected charge as a function of strike location for bulk transistors, after [Ferl-06].

collected charge correlates directly with the SET distribution observed in this work. The collected charge distribution indicates that strikes within the drain region lead to higher amounts of charge being collected and strikes further away from the drain lead to lower charge collection. Thus one may expect to see many short transients since the area around the drain region where strikes lead to relatively low amounts of charge being collected is expected to be larger than the drain region. The reason for not observing a higher number of short transients may be due to the fact that many such transients may have been attenuated completely before measurement. As discussed in Chapter III, transients that are less than about two to three times the propagation delay of a single latch stage, which corresponds to less than about 350 ps for the 130-nm process, may be partially or completely attenuated as they propagate through the measurement latch stages. Hence the

lower end of the SET pulse width distribution may extend further and may contain more events. Recent SET event cross section measurements suggest the presence of many short transients [Bala-08-1]. In [Bala-08-1], the SET event cross section was found to decrease with total dose for a measurement technique that records the total number of SET events (including some of the very short transients), while the event cross section remained approximately the same with dose for measurements using the temporal latch and the autonomous pulse capture techniques. Balasubramanian et al. have suggested that the increase in attenuation of short transients with dose, which may not be captured by the temporal latch and autonomous pulse capture circuits even for pre-dose measurements, may have resulted in the observed trends.

Based on the work of Dasgupta et al., it is also likely that parasitic bipolar charge collection may be an issue for the considered process [Dasg-07]. Such a charge collection mechanism may increase the amount of charge collected, leading to an increase in the number of wider transients. TCAD simulations showing the importance of strike location relative to the well contacts is discussed at the end of this chapter. The next chapter includes a discussion about the shape of the current pulse in the 130-nm and 90-nm processes.

The use of the autonomous pulse capture technique enables most of the created SET pulses greater than about two to three times the delay of a single latch stage to be measured (except the ones that are created when reading the data, which are negligible as the frequency of operation was much higher than the rate at which SETs were created). Moreover, while temporal latch-based or guard gate-based techniques count all SET pulses greater than a certain width, the autonomous SET characterization measures the

individual SET width and thus enables the precise estimation of event cross section for individual pulse widths greater than two to three times the delay of a latch stage at each LET.

Fig. 4.4 shows a plot of the event cross section per inverter for individual pulse widths as a function of LET (not the cumulative cross section). This chart is similar to conventional error cross-section vs. LET plots, except here it is broken down into individual contributions from each pulse width. The data point at an LET of 20 MeV-cm$^2$/mg was taken at a 60 degree angle of incidence while the one at an LET of 10 MeV-cm$^2$/mg and the one near 40 MeV-cm$^2$/mg were taken at normal incidence. It is likely that variations in the effective fluence with the angle of incidence may have resulted in a higher cross section for the data at an LET of 20 MeV-cm$^2$/mg. Using the individual SET event sections, a contour plot, shown in Fig. 4.5, was generated. The contours represent

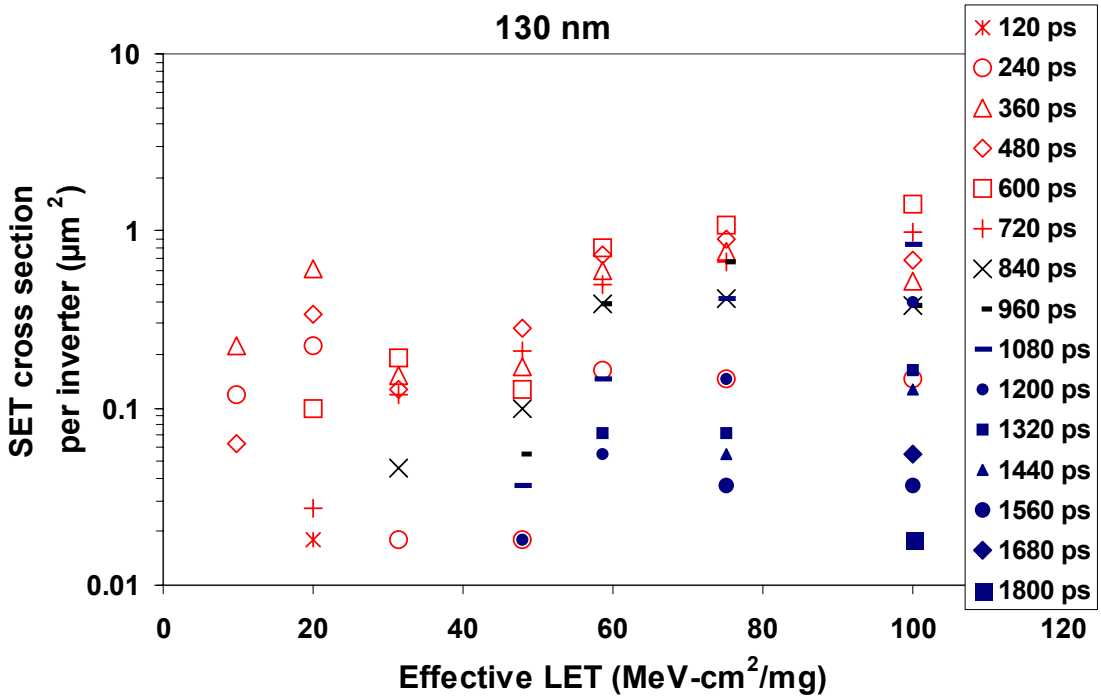



Fig. 4.4 SET cross section per inverter for individual pulse widths as a function of LET for the 130-nm process.

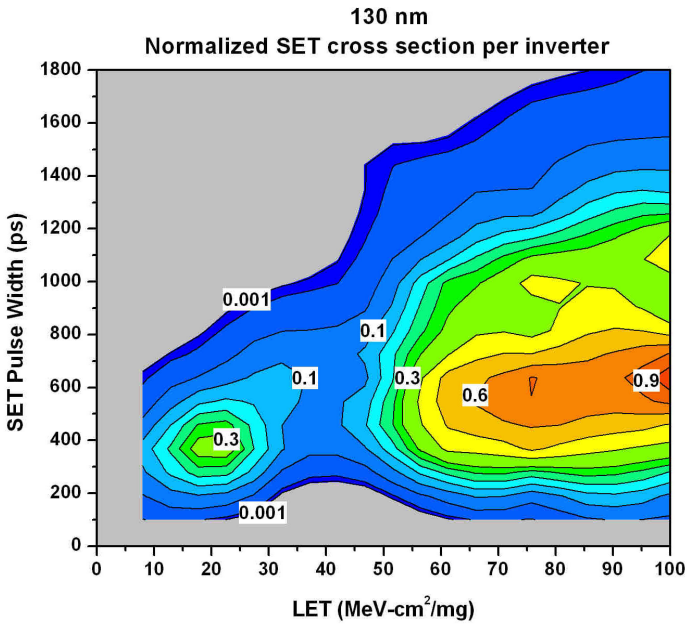



Fig. 4.5 Contour plot shows the variation in normalized, individual SET cross section per inverter as a function of both SET pulse width and LET for the 130-nm process.

the variation in the normalized, individual SET event cross section per inverter as a function of both SET pulse width and LET. From Fig. 4.5, it is evident that the event cross section is dominated by SET pulses between the range of 300 ps to about 700 ps at all LETs. Such measurements allow individual SET event rates to be incorporated into the error cross-section for better estimation of error rates.

*Heavy-Ion Tests – 90-nm*

Table 4.2. Details of the heavy-ion test – 90-nm

| Ion | Angle (deg) | LET (MeV-cm$^2$/mg) | Ion Energy (MeV) |
|---|---|---|---|
| Ne | 0 | 1.8 | 526 |
| Ne* | 0 | 3 | 263 |
| Ar | 0 | 5.7 | 929 |
| Ar* | 0 | 9 | 468 |
| Kr | 0 | 20.6 | 1858 |
| Kr* | 0 | 30 | 860 |
| Xe | 0 | 40.7 | 2758 |
| Xe* | 0 | 59 | 824 |

* Degraders used in the path of the beam to vary ion LET.

The 90-nm ICs were tested at the cyclotron facility at Texas A & M University [Nara-07]. Extensive tests with different ions, all at normal incidence, were carried out. As the ion energy and LET change with the distance traversed in a material, the LET of an ion can be modified by adding degraders in the path of the beam before it

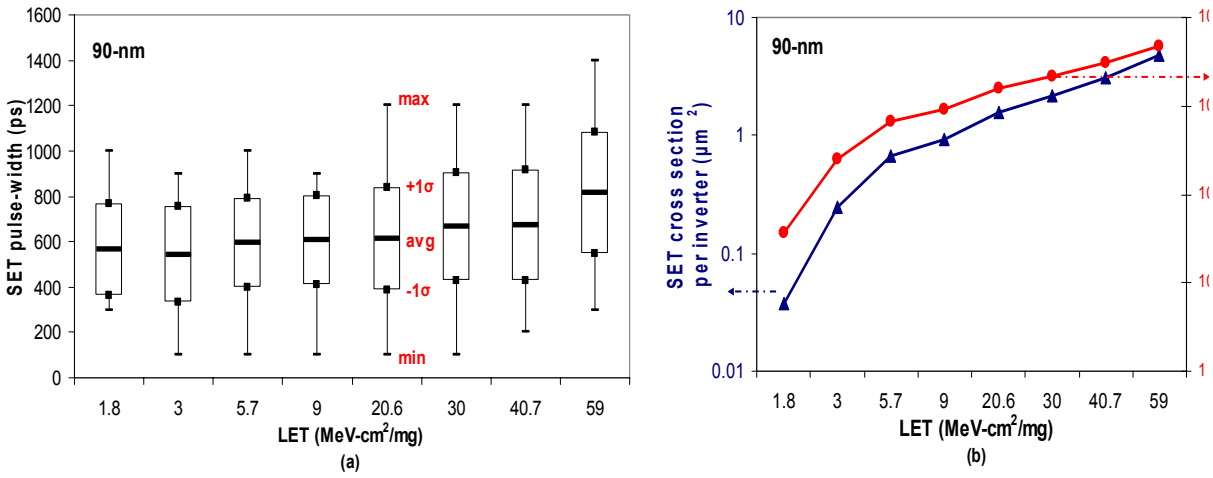



Fig. 4.6 (a) Box plot indicating the average, ± 1 standard deviation, minimum and maximum SET pulse-width as a function of LET for the 90-nm process. (b) Total SET cross section per inverter and the number of events measured as a function of effective LET.

reaches the test IC. As listed in Table 4.2, two different LETs, one obtained without using degraders and the other by using a degrader in the path of the beam, were obtained for each ion. The ICs were tested to a fluence of $1\times10^8$ ions/cm$^2$ at each LET.

Fig. 4.6(a) is a box plot representing the average SET width, the standard deviation of the SET-width population and the minimum and maximum SET widths for a range of ion LETs in the 90-nm technology. From Fig. 4.6(a), we see that the threshold for SET events in the 90-nm process is less than 2 MeV-cm$^2$/mg, compared to about 7 MeV-cm$^2$/mg for the 130-nm process. While the maximum SET width shows a slight dependence on the LET, for the most part the range of SET widths shows little dependence on the ion LET. The likely reasons for the observed distribution of SET pulse widths are discussed in the next chapter. Fig. 4.6(b) shows plots of the number of events

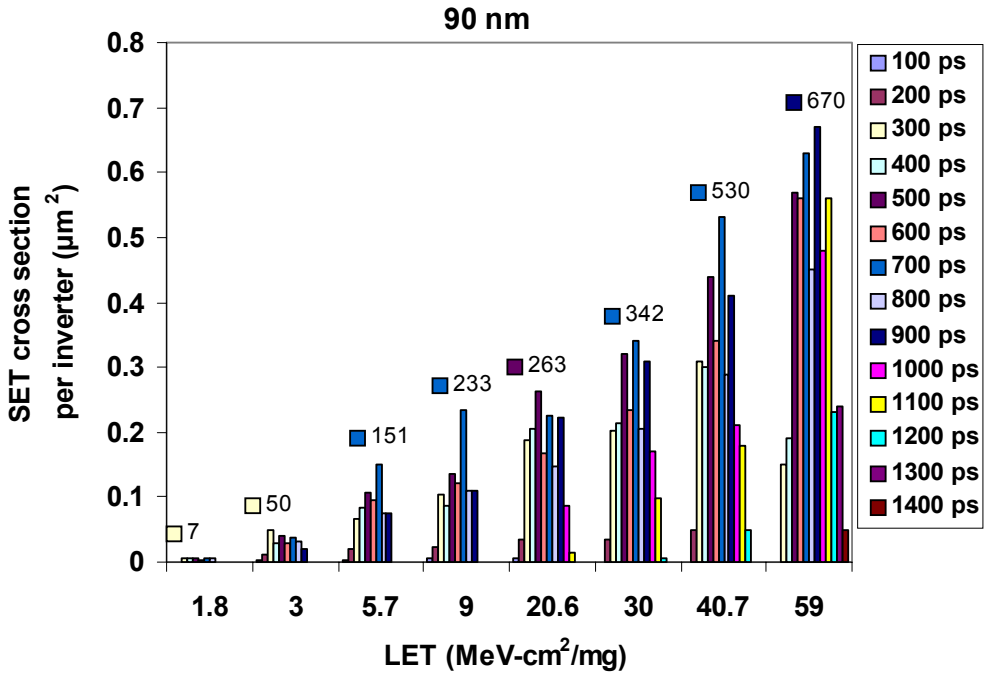



Fig. 4.7 Distribution of event cross section per inverter as a function of LET for the 90-nm process. The data labels on the chart indicate the maximum number of SET pulses of a given width measured at each LET.

measured and the total SET cross section per inverter as a function of LET. Similar to the results for the 130-nm technology, the number of SET events measured strongly depends on the ion LET. As discussed earlier, since the individual latch delay is about 100 ps for the 90-nm process, transients less than about 250 ps to 300 ps may have been partially or completed attenuated. Thus the lower end of the distribution may contain more events than those that are captured by the pulse-measurement circuit.

Fig. 4.7 shows a histogram of the distribution of the event cross section per inverter as a function of LET. As stated earlier, event cross section per inverter is defined here as the ratio of number of measured SET pulses with a given width to the total fluence, divided by the number of target inverters. The histogram of the SET distribution shows that the odd numbered bars (100, 300, 500, etc.) contain more events than the even numbered bars (200, 400, 600, etc.). This shows that the number of stages affected by the SET has a slightly higher probability of being odd than even. The total number of events in the even numbered bars was found to be about 20% to 30% lower than the number of events in the odd numbered bars. The pulse widths for strikes on devices within the well region, i.e., PMOSFETs, have been shown to be longer than the pulse width for strikes on NMOSFETs [Olso-07]. Thus a convolution of the SET width distributions for the NMOSFETs and PMOSFETs can lead to a double peaked distribution with some variations in the number of events for the bars in the middle.

Furthermore, the periodicity in the measured distributions can be created by drive current variations between the PMOSFETs and NMOSFETs. The leading edge of the SET pulse that initiates the trigger signal was always latched at the 21$^{st}$ measurement latch stage. The SET pulse width should then determine the number of stages before

stage 21 that have a flipped state. Due to the initial state of the circuit, the outputs of odd numbered latch stages are initially high and vice-versa. If the PMOSFETs have a lower drive current than the NMOSFETs, then it takes longer to transition from low-to-high than it does from high-to-low. If the SET pulse is, say, 3.55 times the individual stage delay, then it should, in theory, affect stages 21, 20, 19 and 18. In this case stage 18 is starting to recover back to its nominal state, i.e., starting to transition from high-to-low. If this transition time is faster than expected, then the output of stage 18 can cross the threshold, resulting in the SET affecting only 3 stages. Similarly, it can be argued that a slower PMOSFET can result in an SET pulse that is 4.45 times the individual stage delay to be measured as 5 stages wide. Simulations with different PMOSFET and NMOSFET drive strengths also concur with the above explanations. Thus variations in the drive currents can result in the observed periodicity in the number of measured SETs. However, such variations do not significantly affect the average and range of the SET pulse widths measured. One additional factor that can contribute to the variations in the drive currents is the amount of dose accumulated with testing the devices with heavy-ions. For these tests, a total dose of a few hundred krads was accumulated in the tested devices. The parametric degradation associated with the total dose could lead to the types of drive imbalances described above.

Based on the SET event section, a contour plot, shown in Fig. 4.8, was generated. The contours represent the variation in the normalized, individual SET event cross section per inverter as a function of both SET pulse width and LET. The event cross section is dominated by SET pulses between the range of about 400 ps to about 900 ps at all LETs for the 90-nm technology.

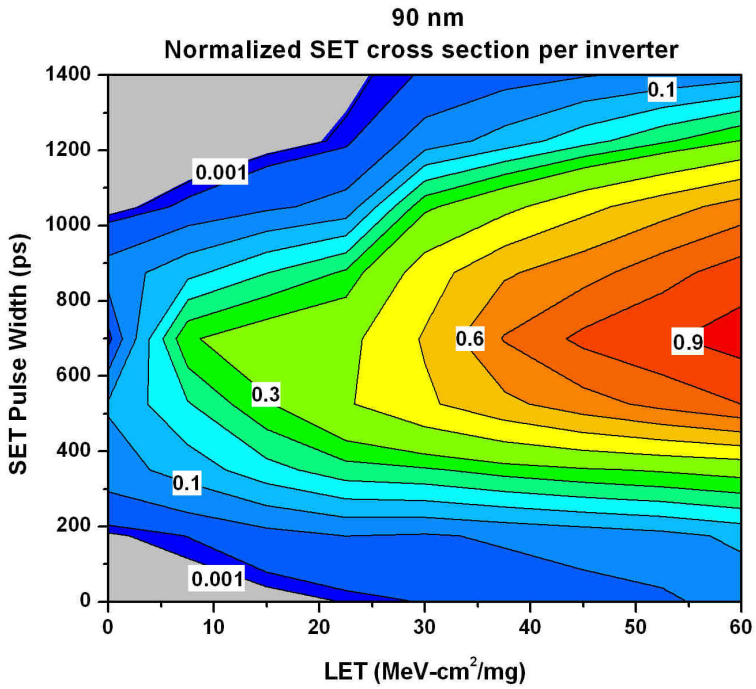



Fig. 4.8 Contour plot shows the variation in normalized, individual SET cross section per inverter as a function of both SET pulse width and LET for the 90-nm process.

*Variation in SET Pulse Width With Strike Location*

Mixed-mode simulations for a string of ten inverters designed using calibrated 130-nm and 90-nm processes were performed. These simulations are based on generic matched device sizes in these processes and do not correspond to the sizes of the circuits that were fabricated, as they are used here to only show the variation in SET pulse widths with strike location. In both cases, the off-state PMOS transistor of the second inverter was modeled using 3D-TCAD (see Fig. 4.9). Keeping the incident ion LET fixed at about 40 MeV-cm$^2$/mg, which corresponds to about 0.4 pC of deposited charge per micrometer, the strike location in the TCAD model was varied relative to the location of the well contact. Fig. 4.10 shows a plot of the width of the low-high-low pulse measured at the output of the eighth inverter for different strike locations in the TCAD model. The well contact helps in the removal of the deposited charge which in turn helps mitigate the collapse of the well potential that leads to the parasitic bipolar charge collection. The

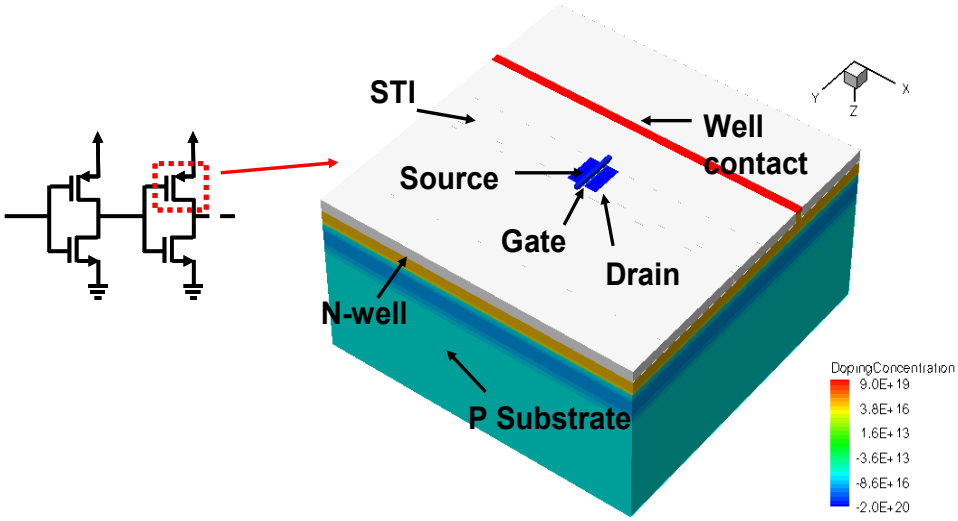



Fig. 4.9 130-nm TCAD model based on generic matched device size, used for mixed mode simulations.

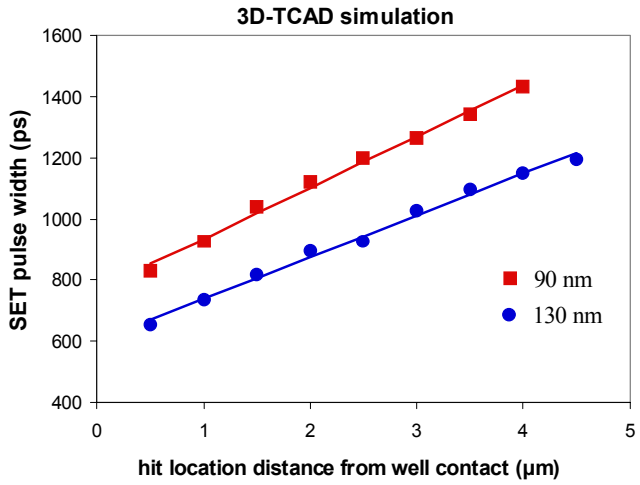



Fig. 4.10 Variation in the SET width relative to strike location from well contact.

SET pulse width is thus lower when the hit takes place closer to the contact as the deposited charges can more easily be removed by the contact [Blac-05]. These results indicate that parasitic charge collection may be an issue for these processes. The simulation results also demonstrate that the SET pulse width depends strongly on the strike location and support the statistical distribution of experimentally measured pulse widths which arises due to the random nature of ion strikes.

# CHAPTER V

# TECHNOLOGY SCALING TRENDS IN SET PULSE WIDTHS

In this chapter, scaling trends in SET pulse widths are analyzed based on the experimental data presented in the previous chapter. 3D-TCAD simulation results are used to better understand the experimentally observed trends. Discussions on SET pulse width dependence on factors such as drive current, load capacitance and contact width are included. Finally the chapter analyzes the reasons for similarity in the SET distributions in the 90-nm process across different LETs.

## *Technology Scaling Trends based on Heavy-Ion Experimental Results*

Fig. 5.1 compares the heavy-ion induced SET widths in 130-nm and 90-nm processes as a function of LET. While the ion energies are not identical for these experiments, it is still reasonable to compare the results based on LET as direct ionization events dominate over spallation secondary reaction events in this case. Only data for normal incidence are plotted in Fig. 5.1. For low to moderate LETs, the range of SET pulse widths in the 90-nm process is significantly larger than that of the 130-nm process, while they are comparable at higher LETs. A comparison of Fig. 4.5 and Fig. 4.8 indicates that in the 90-nm process, the SETs with the highest event section (~400 ps to ~900 ps) are wider than the most common events in the 130-nm process (~300 ps to ~700 ps). Assuming that the ions and LETs used for these experiments are comparable, it is evident that for this 90-nm technology, the dominant SET pulse widths have increased compared to the 130-

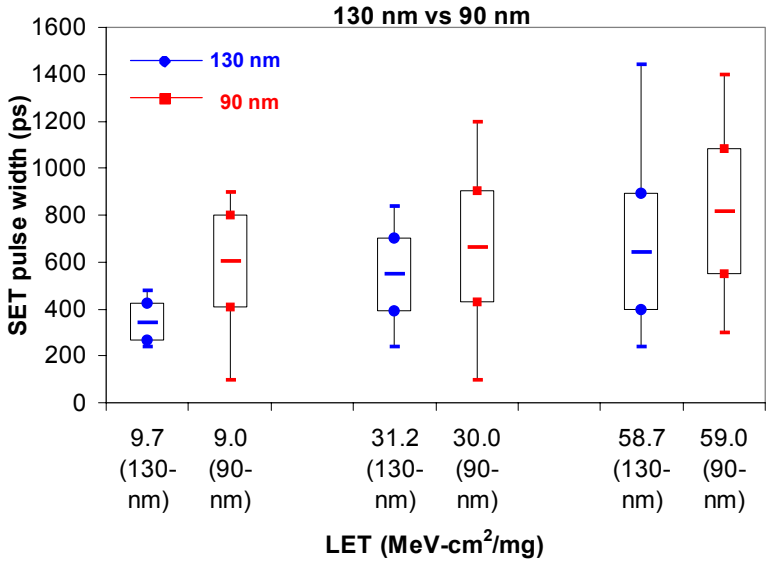



Fig. 5.1 Box plot indicating the average, ± 1 standard deviation, minimum and maximum SET pulse-width in 130-nm and 90-nm process as a function of LET. Only data for normal incidence angle are plotted.

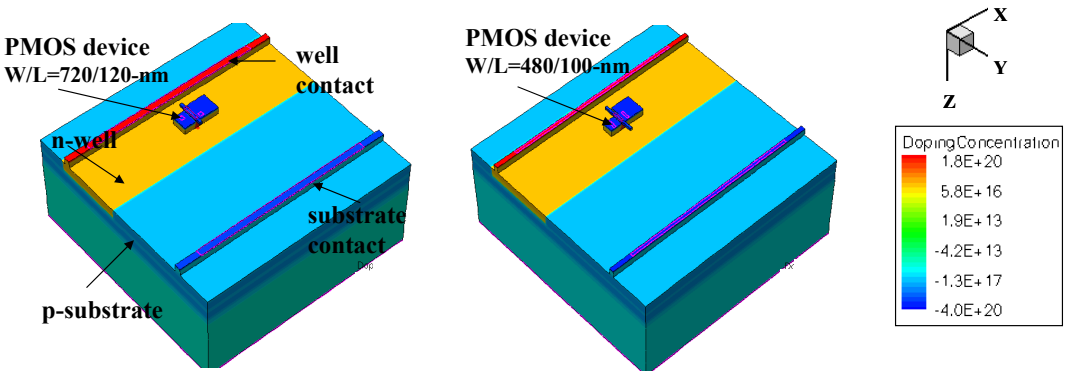
nm technology. Also, the 130-nm and 90-nm processes used in this study have the same operating voltage of 1.2 V and the circuits tested were identical except that their sizes were proportionately scaled from the 130-nm process to the 90-nm process. Since the combinational logic soft errors may increase with increasing SET pulse widths, the increase in the number of wider transients with scaling suggests higher vulnerability for future technologies.

With scaling, typically the switching speed increases and hence the argument that it should be faster to charge (or discharge) a node back to its normal state would imply that the SET pulse widths should decrease with technology scaling. However, the experimental results indicate otherwise. Mixed-mode simulations were performed using the exact device dimensions that were used in the layout of the SET test chips in the 130-nm and 90-nm processes to better understand scaling in SET pulse widths. The impact of parameters such as drive currents, load capacitance and contact widths on SET pulse

width is discussed with the use of simulations.

*Mixed-Mode TCAD Simulations to Identify Scaling Trends*

Mixed-mode 3D-TCAD simulations were performed to understand the factors that affect SET pulse widths and technology scaling trends. The simulations were performed using calibrated models in IBM 130-nm and 90-nm processes. Fig. 5.2 shows the PMOS devices modeled in 3D-TCAD used for simulating SET pulse widths in 130-nm and 90-nm processes. The TCAD structures, along with the PMOS device sizes, correspond to the PMOS devices in the target inverter layout used for obtaining the experimental results. The target inverter layout was designed with minimum sizes for the NMOS devices (a W/L ratio of 2) and with the size of the PMOS device scaled for matched current drives based on the device parameters in the appropriate process design kit (PDK).




**(a) 130-nm** **(b) 90-nm**

Fig. 5.2 3D-TCAD structures used for simulating SET pulse width in (a) 130-nm and (b) 90-nm processes. These structures are similar to the layout of the devices in the respective technologies used for obtaining the experimental results

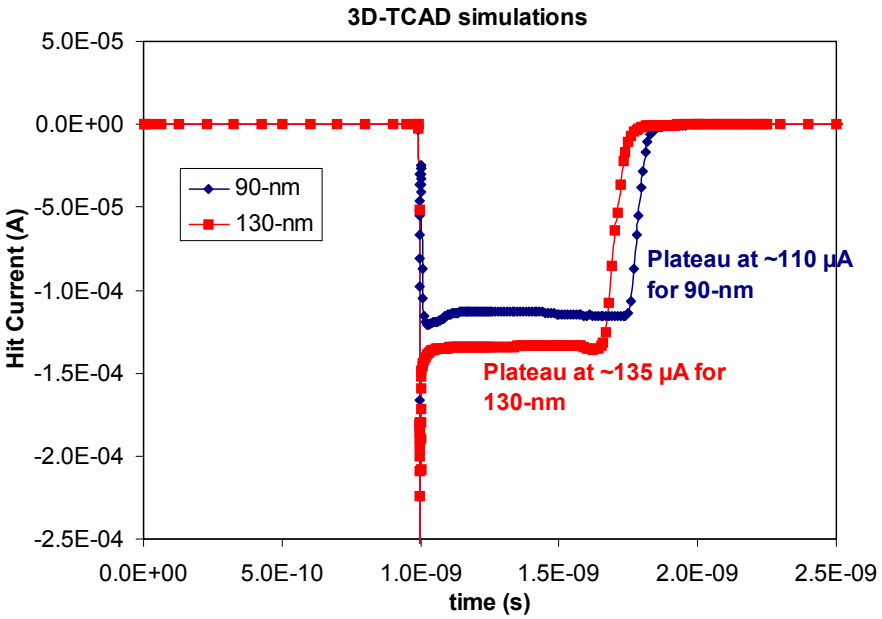



Fig. 5.3 TCAD simulated hit-node currents due to an ion-strike with an LET of 40 MeV-cm$^2$/mg in 130-nm and 90-nm processes.

The width of the contacts was chosen to be minimum in each of the technologies – 28-nm for the 130-nm process and 20-nm for the 90-nm process. The length of the contact extends from one end of each inverter cell to the other end in the layout and hence when stacking multiple inverters along a row, the well and substrate contacts form a continuous strip. The nominal supply voltage for both processes is 1.2 V.

Fig. 5.3 shows the TCAD-simulated hit-node currents in the 130-nm and 90-nm processes due to an ion strike with an LET of 40 MeV-cm$^2$/mg at the center of the drain of the off-state PMOS device. An LET of 40 MeV-cm$^2$/mg corresponds to depositing 400 fC of charge per micrometer. The hit-node current has an initial peak due to drift collection of charges followed by a plateau region where the current remains approximately constant with time and finally decays down to zero. Recent research indicates that for LETs greater than about 10 MeV-cm$^2$/mg the hit current pulse has a plateau region, as can be observed in Fig. 5.3, in addition to the standard double

exponential pulse. This plateau region can be attributed to the collapse of the well potential following a strike [Dasg-07]. The simulated current pulse shapes indicate that parasitic bipolar charge collection effects may need to be considered for some advanced CMOS processes. The plateau current corresponds to the restoring device drive current [Dasg-07]. From Fig. 5.3, the hit current is observed to plateau at about 135 μA for the 130-nm process and for the 90-nm process this occurs at about 110 μA. The SET pulse width is determined by the time at which the restoring drive current overcomes the hit

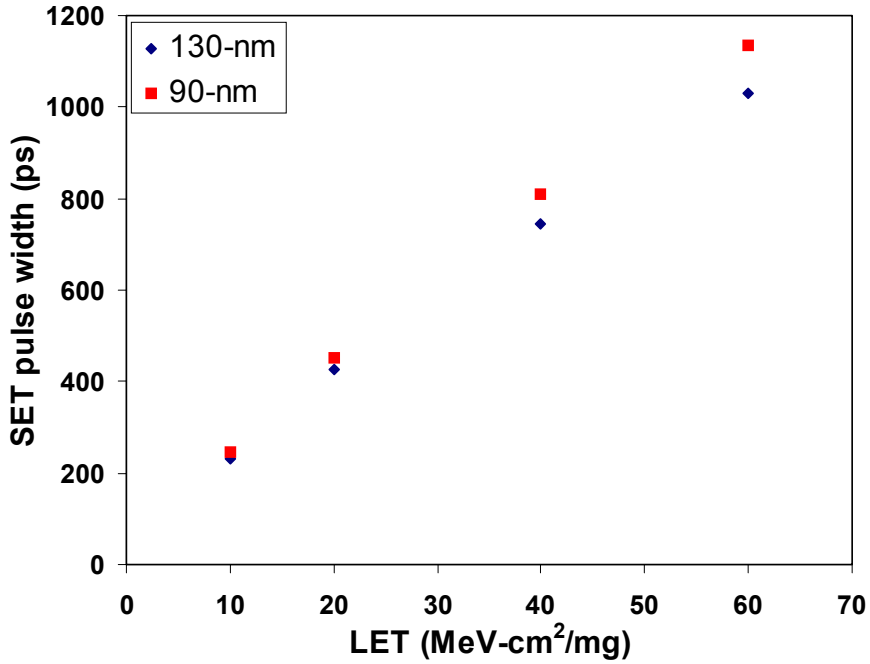



Fig. 5.4 TCAD simulated SET pulse width as a function of LET for 130-nm and 90-nm processes indicating an increase of about 10% in the SET pulse width with scaling.

current. With lower restoring drive current, the rate of charge removal is slower, which increases the SET pulse width.

Fig. 5.4 shows the TCAD-simulated SET pulse widths as a function of LET due to strikes at the center of the drain of the 130-nm and 90-nm PMOS devices shown in Fig. 5.2. The mixed-mode simulations were performed with a chain of ten inverters with the

PMOSFET of the third inverter represented using the TCAD model. As can be observed from Fig. 5.4, the TCAD results also indicate an increase in the SET pulse width when scaling from 130-nm to 90-nm. The percent increase in pulse widths is about 10% and is lower than projected by the experimental results. Moreover, the simulation results show a linear dependence on LET unlike the experimental results, which showed only a marginal dependence on LET. The likely reasons for this are analyzed in the section on long transients at low LETs. In addition to lower drive currents, the reduction in the contact sizes with technology scaling may also impact the rate of charge removal and hence the SET pulse width. TCAD simulations were also performed to identify the effect of contact width, restoring device W/L, and the power supply voltage on the SET pulse widths in the 90-nm process. Fig. 5.5 shows plots of the mixed-mode simulated SET pulse width as a function of supply voltage, restoring device W/L, contact width and the size of the loading gate. Reducing the supply voltage lowers the drive currents and hence it takes longer to restore the node back to its original state and hence increases the SET pulse width. Similarly, reducing the restoring NMOS W/L ratio has a similar effect on the drive current and thus increases the SET pulse width (or reduces pulse width if the W/L ratio is increased). Finally and more interesting is the effect of the size of the loading inverter stage on the SET pulse width.

The size of the loading gate was found to have only a minor effect on the SET pulse width. The loading inverter size was changed by factors of two and four from the minimum sizes. The primary reason for the lack of dependence on the size of the loading gate is likely due to the fact that the size of the loading capacitance determines the rise and fall time of the transient, but the duration for which a node stays affected is governed

primarily by the restoring drive current and the well contact size, both factors that help in removing the deposited charges. Since the rise and fall times of the load capacitance are significantly smaller compared to the width of the SET or the time that the node stays affected, the load capacitance has little effect on the width of the SET.

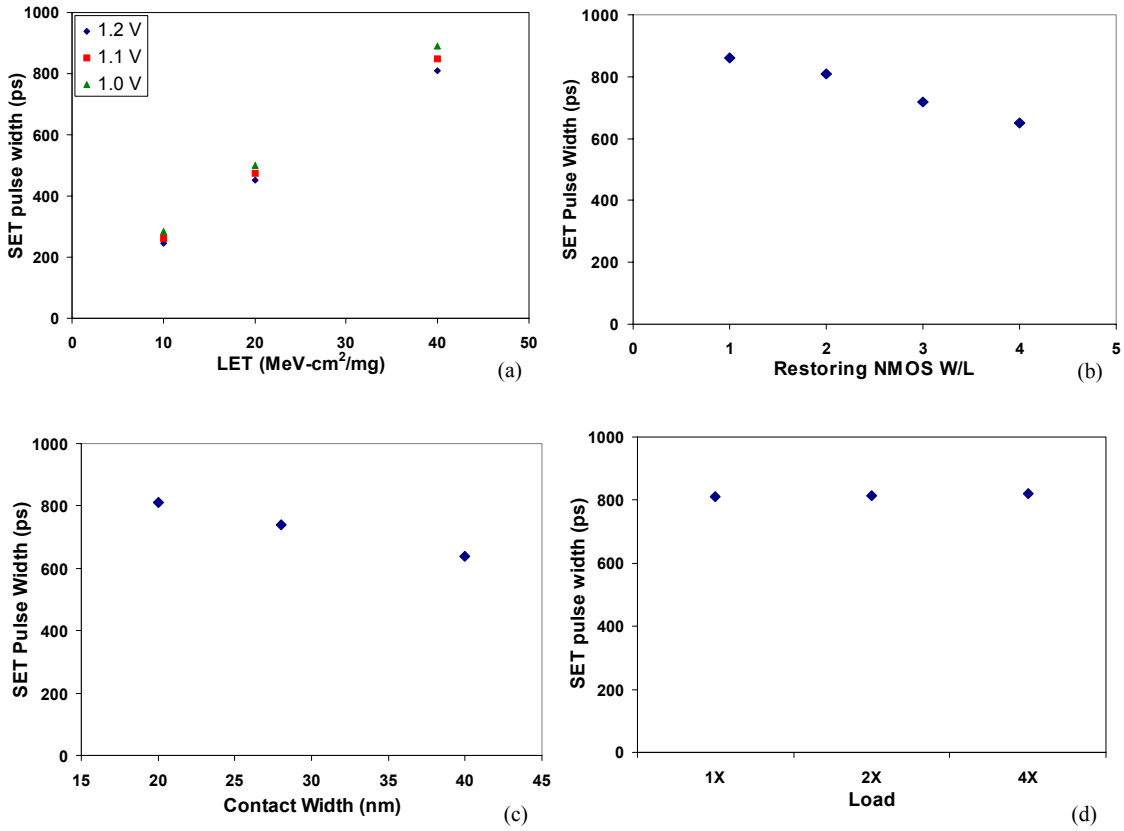
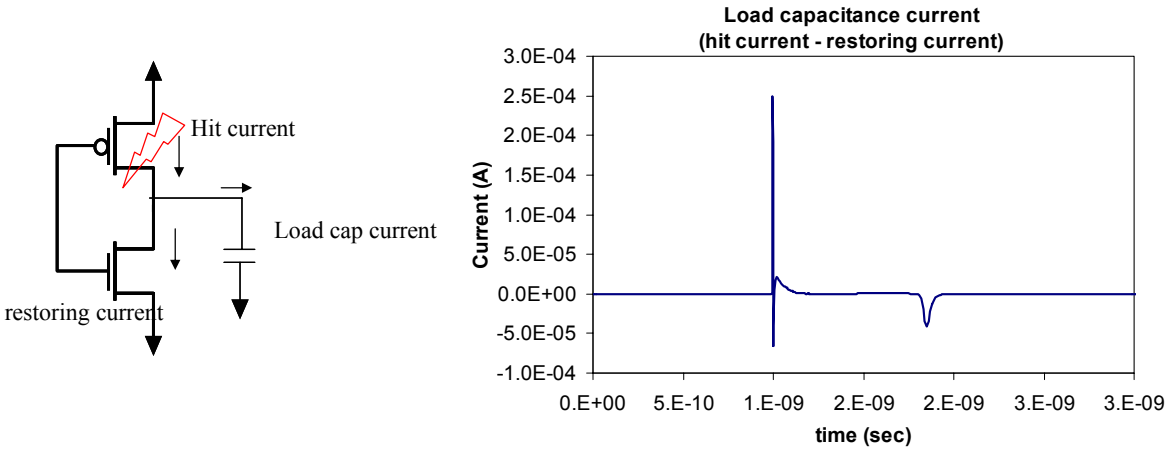



Fig. 5.5 TCAD simulated SET pulse width as a function (a) LET and supply voltages, (b) restoring NMOS W/L, (c) n-well contact width and (d) size of the loading inverter stage.

Fig. 5.6(a) shows a schematic of the inverter with the hit node, restoring device and load capacitance current components marked. The current through the load capacitance is the difference between the hit node current and the restoring device current. Fig. 5.6(b) shows a plot of the current through the load capacitor. It indicates that a current flows to charge and discharge the capacitor at the leading and trailing edge of the SET pulse, while little or no current flows through the capacitor during the rest of the period when




(a) (b)

Fig. 5.6 (a) Inverter schematic with the hit, restoring and load capacitance current components marked and (b) current through the load capacitor (hit current – restoring current) indicates that current flows to only charge and discharge the capacitor at the leading and trailing edge of the SET pulse, while little current flows through the capacitor at other times.

the node stays flipped. This validates the argument that changes to the load capacitor size should only affect the rise and fall times, while the width of the SET is determined by how efficiently the deposited charges can be removed. The size of the load should also influence the threshold for upset, however, for the LETs considered here, the deposited charge is significantly greater than the critical charge needed to cause an upset.

From the above arguments, it is clear that the drive current, supply voltages and the n-well contact sizes have an impact on the SET pulse width, while the load capacitance has a negligible effect on the SET pulse width. With technology scaling, the drive currents, the minimum contact dimensions, and the load capacitance tend to reduce. The reduction in the drive currents and contact sizes may tend to increase the SET pulse width with scaling.

*Model for SET Pulse Widths*

Based on the dependence of the TCAD-simulated SET pulse width in the 90-nm process on LET, restoring drive current, supply voltage, and contact width, a mathematical model for SET pulse width has been developed. Fig. 5.5 indicates that the SET pulse width varies linearly with each of these parameters. Thus a simple straight line equation of the form y = mx + c can be used to represent the variation of SET pulse width as a function of each of the above mentioned parameters individually. Using the mathematical modeling tool Mathcad, the dependence of SET pulse width on all the above parameters was combined in a single equation. In a simplified version this equation takes the form of

$$\begin{aligned}\text{SET pulse width} \;=\; \text{constant} + m_1 \times \text{LET} \;+\; m_2 \times (\text{restoring device W/L ratio}) \\ + m_3 \times \text{Vdd} \;+\; m_4 \times (\text{contact width})\end{aligned}$$

The equation with numerical values for all the constants is given below. This equation is valid for LET values between 1 and 100 MeV-cm$^2$/mg.

$$\begin{aligned}\text{SET Pulse Width (90 - nm in ps)} = 770\ \text{ps} &+ (18.45 \times \text{LET (MeV - cm}^2\text{ /mg)}) \\ &+ (-357.57 \times \text{Vdd}) \\ &+ (-7.704 \times \text{Contact Width (nm)}) \\ &+ (-74.58 \times \text{restoring device W/L})\end{aligned}$$

This equation has negative coefficients for supply voltage, contact width, and restoring device drive strength as the SET pulse width decreases with an increase in any one or more of these parameters. The coefficient for LET is positive, implying that the pulse width increases with increasing LET.

Fig. 5.7 compares the TCAD-simulated SET pulse widths with those calculated using the above equation. Here the model is used to compute the variation in the SET pulse width as a function of one of the variable parameters, keeping the rest as constants with

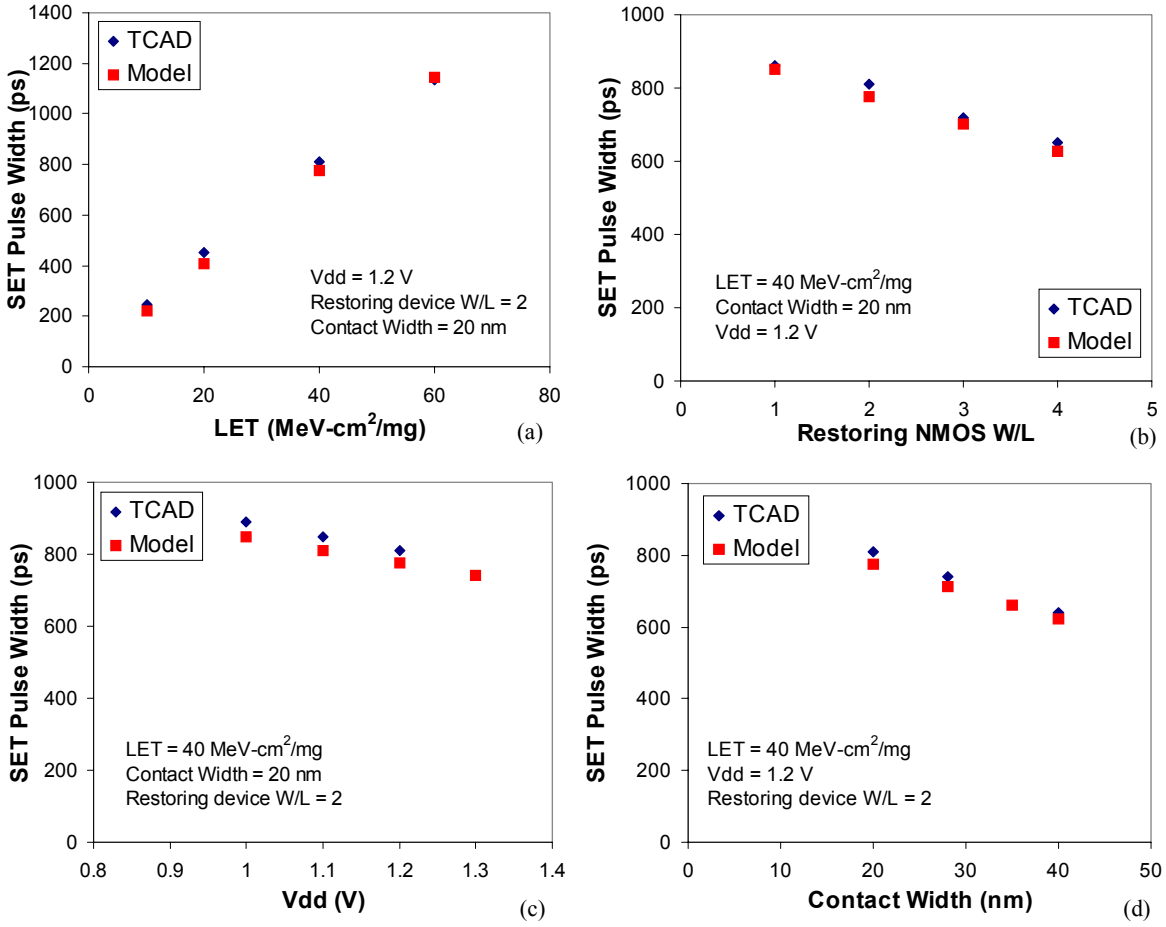



Fig. 5.7 Comparison of the TCAD simulated SET pulse widths with those computed using the model as a function of (a) LET, (b) restoring device W/L ratio, (c) Vdd and (d) contact width. The results indicate a good correlation between the simulated and modeled SET pulse widths.

values as specified in each of the plots in Fig. 5.7. The difference in the TCAD-simulated SET pulse width and that computed using the model is less than 5%, indicating good agreement between the simulated and modeled pulse widths. Such a model can be used to extrapolate the SET pulse width for different types of logic circuit designs with different restoring device currents and contact sizes.

*Experimental Evaluation of the Effect of Well and Substrate Contacts on SET Pulse Width*

The SET pulse characterization technique was used to quantify the reduction in long SET pulses for circuits with larger well contacts and guard bands compared to circuits with single well and substrate contact per inverter cell. The TCAD results suggest that larger well contacts should help mitigate the width of SET pulses by mitigating the well potential collapse effect and by enabling faster removal of the deposited charges. Two SET pulse characterization test structures were designed on the same IC in the IBM 130-nm process. Each test circuit consisted of the pulse capture circuit along with the target circuit composed of either inverters with a single well and substrate contact per cell (similar to conventional layout practice) or inverters with multiple well and substrate contacts along with guard bands surrounding each transistor. Guard bands are n+ diffusions surrounding the PMOS transistor in the n-well and they are p+ diffusions

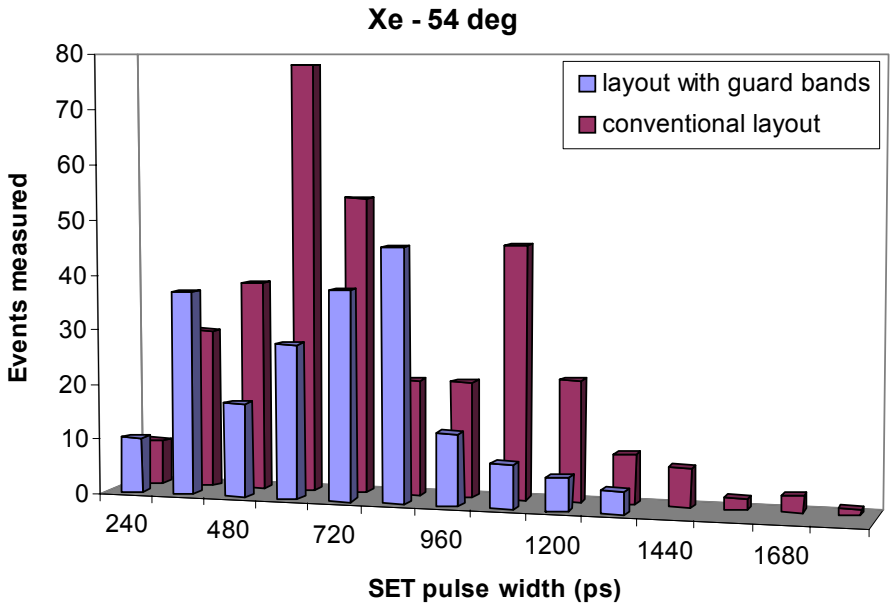



Fig. 5.8 Distribution of SET pulse widths due to Xe ions incident at 54 degrees in the 130-nm process for the conventional layout circuit and for the circuit with guard bands.

surrounding the NMOS transistor in the p-substrate. They help maintain the well potential over a larger area. The use of guard bands along with multiple well contacts per cell increases the average cell area of the inverters by about 7% for our implementation. However, the area increase would be larger for a more complex or more highly optimized cell.

Heavy-ion experiments were performed to measure the distribution of SET pulses for conventional layout circuits and for circuits with guard bands. Fig. 5.8 shows a plot of the distribution of SET pulses due to Xe ions incident at 54 degrees for the conventional layout circuit and for the circuit with guard bands. The results indicate a decrease in the number of transients longer than about 1 ns as well as a reduction in the maximum SET pulse width for circuits with guard bands. Fig. 5.9 (a) is a plot of the maximum SET pulse width for the conventional layout circuit and for the circuit with guard bands. On average the maximum SET pulse width reduced by about 20%. Since the maximum SET pulse width corresponds to the maximum amount of charge collected, it indicates a reduction in

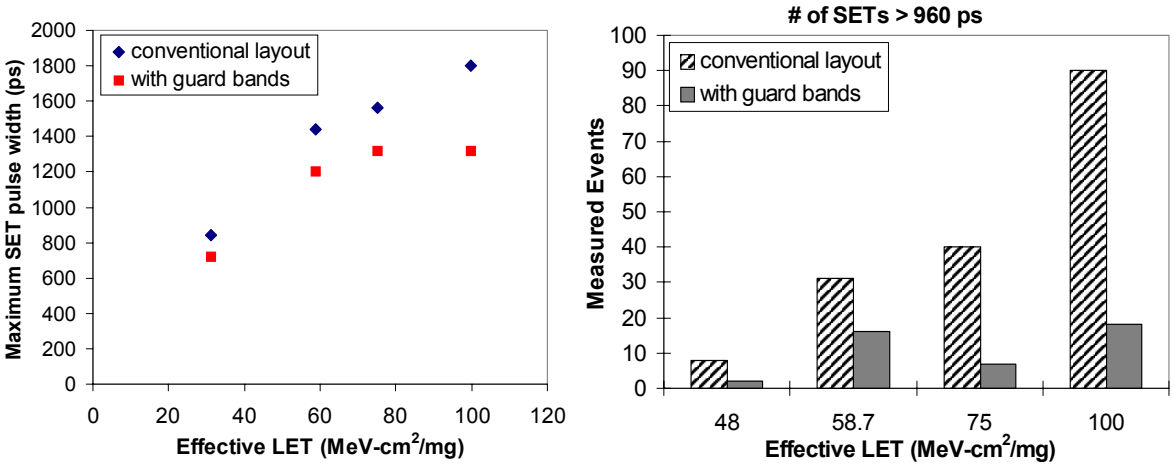



Fig. 5.9 (a) Maximum SET pulse and (b) number of SET pulses greater than 960 ps for conventional layout circuits and for circuits with guard bands.

the collected charge for circuits with guard bands. Fig. 5.9 (b) compares the number of SET events with pulse widths greater than about 960 ps for the two test circuit types. The number of longs SETs (greater than 960 ps) was reduced by about 70% for circuits with guard bands compared to the conventional layout circuit. These results indicate that stronger well and substrate contacts can help mitigate the amount of charge collected and hence reduce SET pulse widths.

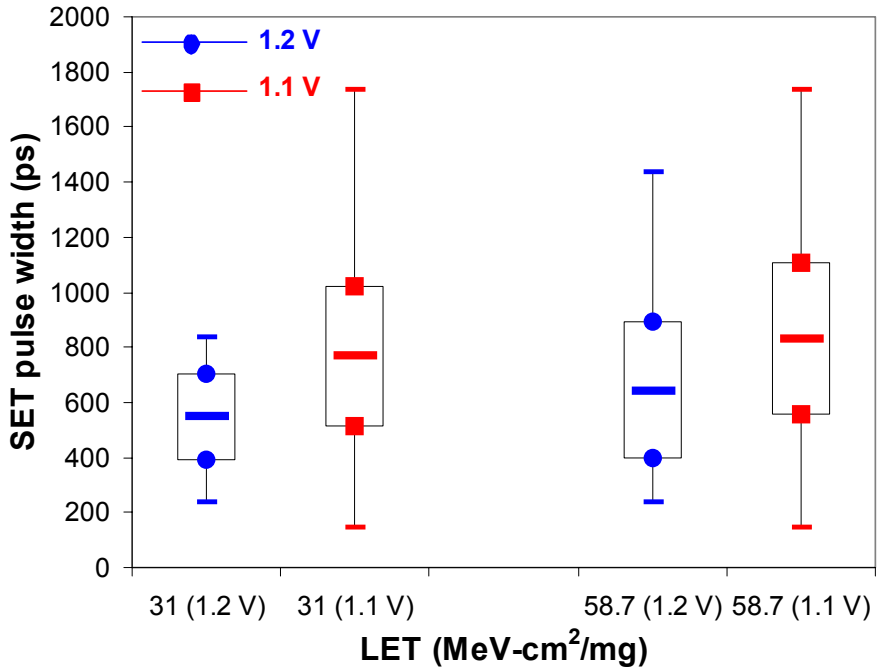



Fig. 5.10 Box chart of the minimum, average, ±σ and maximum SET pulse width in the 130-nm process for 1.2 V and 1.1 V supply voltages as a function of LET.

As discussed earlier with the use of TCAD simulations, a reduction in the drive strength of the restoring device results in increasing the SET pulse width as it takes longer for the removal of the deposited charges. Experimental verification of the effect of drive strength on SET pulse width was achieved by testing the 130-nm SET test chips at the nominal supply voltage of 1.2 V and at a reduced supply voltage of 1.1 V. A reduction in the supply voltage affects the gate overdrive or drive strength due to a reduction in the ($V_{GS} - V_T$) and ($V_{DS}$) parameters. Fig. 5.10 is a box chart of the minimum, average, ±σ and maximum SET pulse width in the 130-nm process for supply voltages of 1.2 V and 1.1 V as a function of LET. Fig. 5.10 clearly indicates an increase in SET pulse width with a reduction in the supply voltage. The average value of the SET pulse width increased by

about 25% for a 0.1 V reduction in the supply voltage. The percent increase in pulse width predicted by the TCAD simulations is much lower than the experimental results and can be partially attributed to the fact that the TCAD results are for the 90-nm process and the experimental results are for the 130-nm process. However, both the TCAD results and the experimental results indicate that restoring drive strength can significantly impact the SET pulse width.

*Possible Causes for Similarity in SET Pulse Width Distributions in the 90-nm Process at Different LETs*

The range of SET pulse widths and the average values of SET widths were found to be similar across a range of LETs, especially for LETs lower than about 10 MeV-cm$^2$/mg, in the 90-nm process. There was only a slight increase in the average and maximum SET pulse width at higher LETs compared to lower LETs. The reason for the similarity in SET pulse widths can be examined by analyzing factors that can cause long SETs at low LETs.

*Long SETs at Low LETs*

While the box chart of SET pulse widths as a function of LET for the 90-nm process (Chapter IV) indicates that there is not a significant difference in the maximum SET pulse width, the cross section for wider transients was found to be two to three orders of magnitude lower at low LETs than at high LETs. Fig. 5.11 shows the cross section for SET pulse widths greater than about 800 ps,

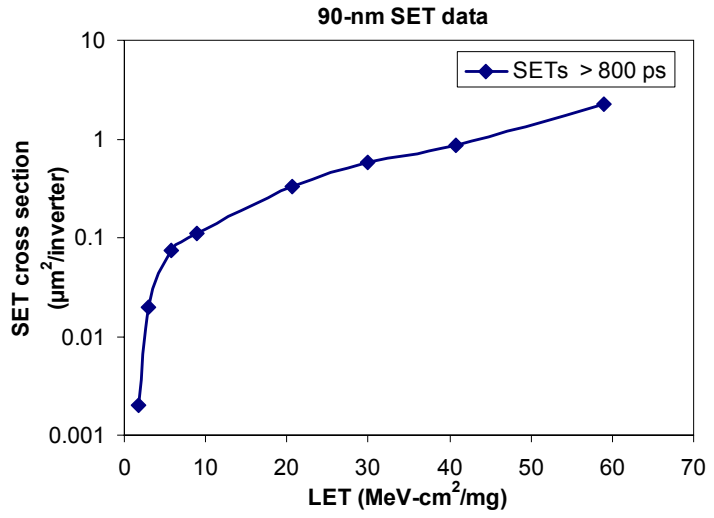



Fig. 5.11 SET event cross section per inverter for SET pulse widths > 800 ps as a function of LET. The number of wider transients are about two to three orders of magnitude lower at low LETs than at high LETs.

indicating that only a relatively few such events occur at lower LETs. A combination of many factors including lower drive currents, larger ion track radius, and secondary reaction products may be responsible for the few longer SETs at lower LETs. In addition to these effects, the length of the target inverter circuit used for the 90-nm SET test chips may also have an impact on SET propagation. The 90-nm SET test chips contain a single chain of one thousand inverters as the target circuit, while the 130-nm test chips contain only a single chain of one hundred inverters. Thus, the history or body-bias effect that is known to affect transient propagation in SOI devices is also discussed. The following discussions analyze the impact of some of these factors on SET pulse widths.

(a) Lower drive currents

As discussed in Chapter III, a ring oscillator was designed to measure the delay of an individual latch stage. However, the on-chip measured ring oscillator frequency was

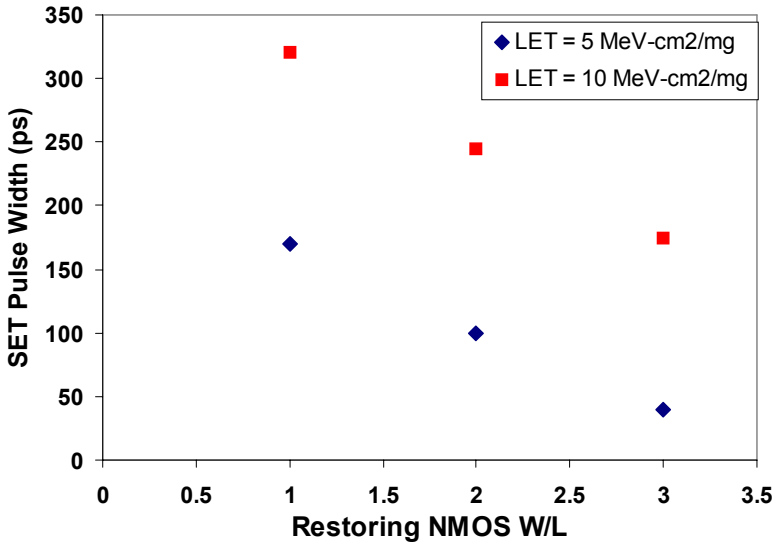



Fig. 5.12 Mixed-mode TCAD simulated SET pulse width as a function of the restoring device size for LET of 5 and 10 MeV-cm$^2$/mg. Nominal NMOS device W/L = 2.

found to be lower than the simulated value by a factor of about two. The SPICE circuit simulation-based value was also verified by simulating the extracted layout to include the RC parasitics and these values were similar. Since the layout of the ring oscillator does not have long interconnects, the capacitance is likely to be dominated by the gate capacitance of each gate. Thus assuming that the load capacitance is similar for the experimental and simulation setups, the factor of two offset in the delay of a latch stage indicates that the drive currents in the fabricated device may be lower than the simulated drive currents. Lower restoring drive currents have already been shown to increase the SET pulse width. Mixed-mode TCAD simulations were performed using the calibrated 90-nm model matched to the layout dimensions to quantify the effect of lower drive current on SET pulse widths at low LETs. Simulations were performed for LETs of 5 and 10 MeV-cm$^2$/mg. Fig. 5.12 shows the TCAD-simulated SET pulse width as a function of the restoring device (NMOS) W/L ratio. The W/L ratio of the NMOS device used in the layout of the fabricated device is two. The simulation results suggest about a 50% increase in the SET pulse width due to lowering the drive current by about a factor of two. Thus the lower drive current may have a role in the experimentally observed SET pulse width distribution. However, even with lower drive currents, the SET pulse width at an LET of 10 MeV-cm$^2$/mg is only about 325 ps, which is significantly lower than the experimental measurements. Hence, lower drive currents alone would not explain the presence of long transients.

(b) Ion track diameter

Previous research work indicates that for particles with the same LET but different energy, charge collection is higher for the higher energy particle due to wider track radius [Stap-88]. The higher energy track is more diffuse and hence may yield an increase in the charge collection as there is less initial electron-hole pair recombination [Stap-88]. The 90-nm test chips were tested at Texas A & M University with the higher energy 25 MeV/nucleon beam which may have resulted in an increase in the charge collected and hence an increase in SET widths. Mixed-mode TCAD simulations were performed with the 90-nm models for various initial ion track radii. The nominal ion track diameter used for the TCAD simulations is 50-nm. Simulations were also performed for track diameters of 200-nm and 500-nm based on the ion track diameter values reported in [Stap-88]. Fig. 5.13 shows a plot of the SET pulse width due an ion strike with an LET of 5 MeV-cm2/mg as a function of the ion track diameter. For a track diameter of 200-nm, the SET

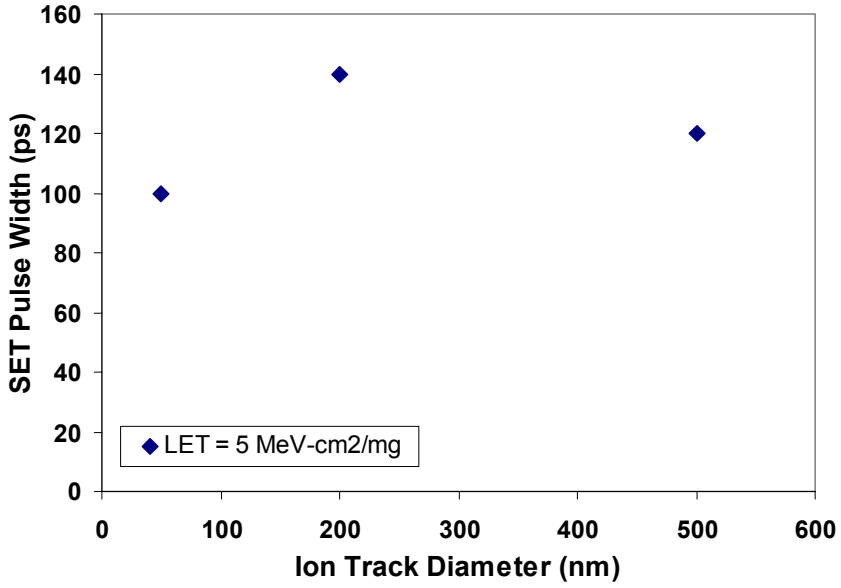



Fig. 5.13 Variation in SET pulse width as a function of ion track diameter.

pulse width was found to increase by about 40% compared to the SET pulse width for a track radius of 50-nm. However, for a 500-nm wide track radius the SET pulse width increased only by about 20%. Moreover, TCAD simulation results indicate that the effect of ion track diameter on the SET pulse width is less pronounced at higher LETs – for an LET of 10 MeV-cm$^2$/mg, only a minor increase in the SET pulse width was observed with a track diameter of 200-nm compared to 50-nm. The initial electron-hole recombination may be a smaller portion of the deposited charge for higher LETs leading to the observed trend. These results suggest that the ion track diameter can impact the SET pulse width at lower LETs.

(c) Variation in the LET of the particle and possibility of nuclear reaction products

Previous work based on Monte Carlo simulations has shown that the charge deposition profiles for an ion is Gaussian distributed around the nominal value and that a relatively few high energy nuclear reaction-induced secondary events can result in much higher charge being deposited [Warr-05]. The deposited charge due to direct ionization may vary by about 20%, while the nuclear reaction products may deposit an order of magnitude or more charge compared to the nominal charge deposition for a given ion. However, results from [Warr-05] indicate that the probability for the nuclear reaction products is about four to five orders of magnitude smaller than the direct ionization events. Dodd et al. have also analyzed the impact of the heavy-ion energy on SEU cross sections and indicate that nuclear reaction events may play a role in the SEU cross sections especially for LETs below the threshold for direct ionization [Dodd-07].

In this work, data were collected for an ion fluence of $1 \times 10^8$ ions/cm$^2$ at each of the LET. The sensitive drain area for the 90-nm SET test chip is about 1 μm$^2$/cell and the target circuit consists of one thousand inverters. This translates to a total sensitive drain area of about 1000 μm$^2$. Thus the number of particles that struck the sensitive drain region is about ($1 \times 10^8$ ions/cm$^2$) × (1000 μm$^2$) = 1000 ions. At low LETs only a few of the ions passing through the drain regions resulted in measurable SET events. Nonetheless, even a conversion of an event for every 1000 strikes in the drain region is relatively high for it to be caused by nuclear reaction events. Thus, while the possibility of some nuclear reaction events causing wider transients may not be completely eliminated, it is unlikely that such events can be used to describe the distribution of SET pulse widths at low LETs completely.

(d) History or body bias effect on SET pulse widths

Researchers characterizing SET pulse widths for SOI devices have identified a propagation-induced pulse broadening effect (PIPB) to affect the distribution of SET pulse widths [Ferl-08, Mass-08]. In SOI devices with a floating body or with weak body ties, reverse junction leakage from drain to body can result in charge getting accumulated in the body of an off-state device. This causes the threshold voltage to vary between devices of the same type in adjacent inverter stages due to the devices being alternately on or off in a chain of inverters. Massengill et al. have shown that such variations in the threshold voltage in a long chain of inverters can result in progressively broadening a transient pulse.

In the case of bulk devices charge accumulation in the body region should either be minimal or not present at all due to the presence of strong body contacts. In this work 3D-TCAD simulations were performed with PMOSFETs to identify if charge accumulates in the body region when the device is left in an off-state for a long time. If the effect is related to charge accumulation, then there should be an increase in the electron concentration in the body region with time. The electron concentration was recorded at different time instances from about 1 ns to about a second. Fig. 5.14 shows the 2D cross sections of the electron concentration in the device at time instances of 0.5 ns, 0.5 µs, 0.5 ms, and 0.5 seconds. As can be observed from the Fig. 5.14, there is little or no

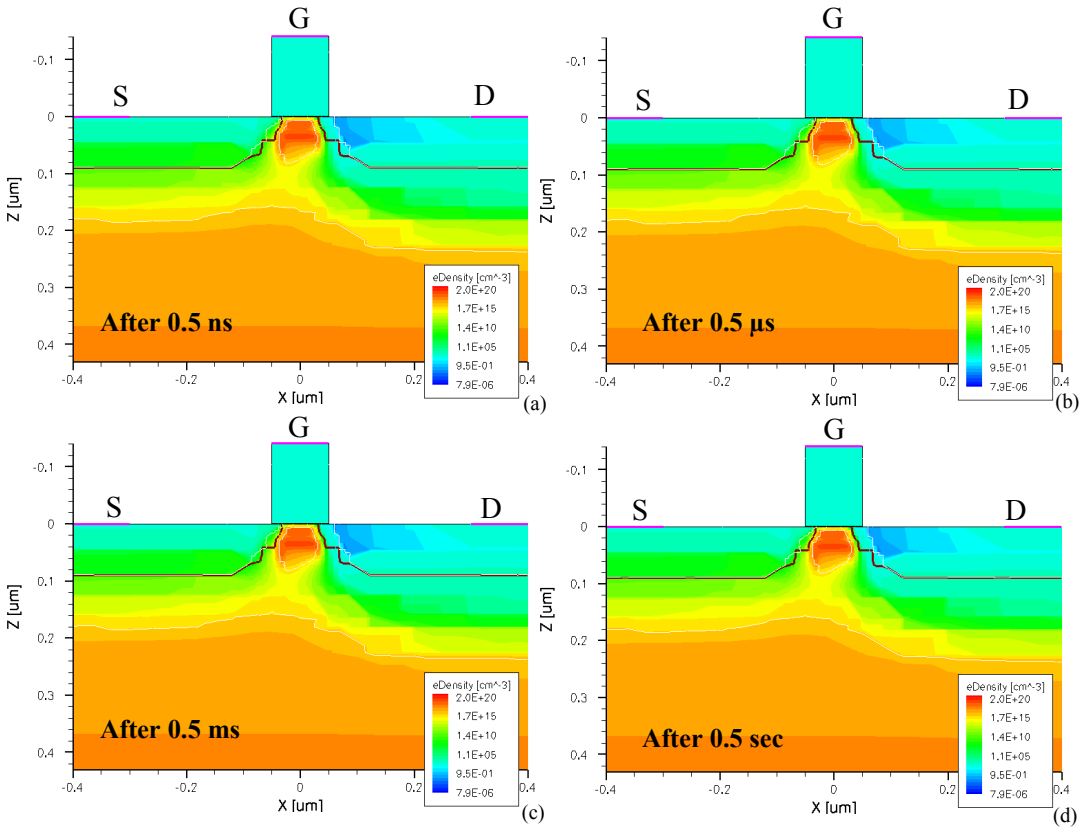



Fig. 5.14 2D cross-section views of the electron concentration in the off-state PMOS device at different time instances. These plots show little or no change in the electron concentration in the body region suggesting that leakage currents do not cause charge accumulation in bulk devices.

change in the electron concentration in the body region for the simulated bulk devices with time. The results indicate that with strong body contacts such as for bulk devices, charge does not accumulate in the body region and hence the history effects related to charge leakage should be minimal. Fig. 5.15 shows plots of the drain current versus gate voltage at 0.5 ns and at 0.5 seconds. These plots also indicate that the threshold voltage is the same regardless of the time for which the device is in the off state, indicating that

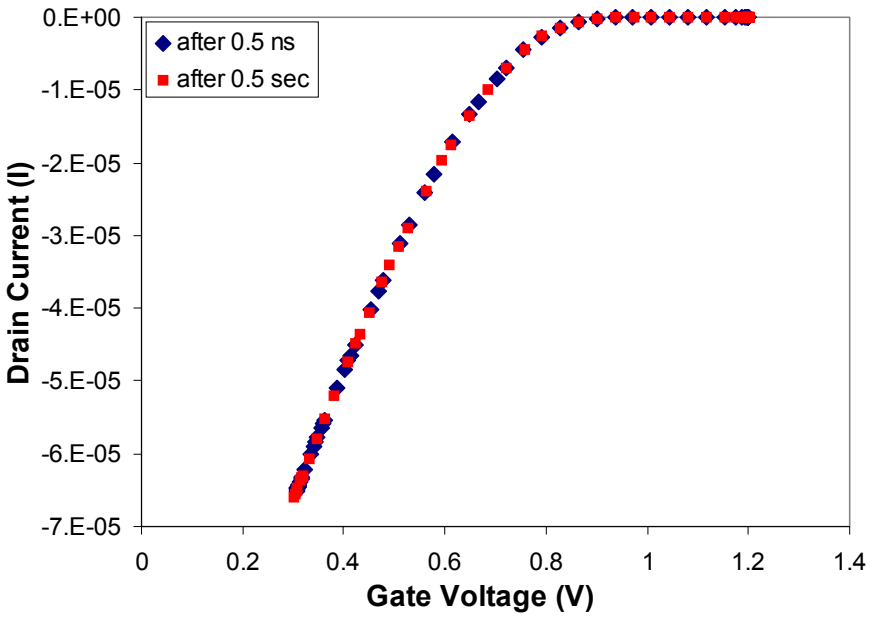



Fig. 5.15 Drain current versus gate voltage plots at 0.5 ns and at 0.5 sec indicating that the threshold voltage is not affected by the time for which a device is in the off-state.

history effects related to charge leakage are not a concern for bulk devices.

While TCAD simulations indicate that history effects may be negligible for bulk devices, recent experimental measurements by Ferlet-Cavrois et al. indicate the presence of pulse broadening in a long chain of inverters fabricated using a 130-nm bulk process, although the effect is shown to be more pronounced in SOI test structures as can be expected [Ferl-08]. Ferlet-Cavrois found that the increase in the transient width per

inverter stage depends on the input to the inverter chain and on the preset time to a given bias state. For a 0 V input to the inverter chain, similar to the input condition used for measurements in this work, the pulse broadening factor (increase in pulse width per inverter stage) was found to be between 0.3 ps to 0.4 ps per inverter for a preset time of a few ms. In [Ferl-08], circuit simulations were also performed with the body potential of off state PMOSFET and NMOSFET gates biased to mimic the history effect. They indicate that a change of about 50 mV to the body potential of off state PMOSFET and NMOSFET transistors in the circuit simulations to reproduce the experimentally observed pulse broadening.

Massengill et al. have derived the conditions for SET pulse propagation in terms of the technology and circuit parameters [Mass-08]. In [Mass-08], the authors have quantified pulse broadening based on the device hysteretic effects. The amount of alternating mismatch in threshold voltages in a chain of inverters was found to control the amount of pulse broadening. The authors point out that pulse broadening is particularly important for partially depleted SOI devices that exhibit the body-bias-induced hysteresis effect, consistent with the experimental observations made in [Ferl-08]. However, the authors also indicate that pulse broadening can occur in bulk devices with weak body ties due to parasitic capacitive coupling between gate-body and drain-body regions, which can lead to variations in the body potential.

In this work, circuit simulations are used to illustrate the impact of pulse broadening on the 90-nm test data. It is reiterated that the possibility of such an effect for bulk devices with strong well and substrate contacts is still a topic of debate and the exact causes for such an effect, if any, have not been well understood.

Circuit simulations were performed for a chain of hundred inverters designed in the 90-nm process. Simulations were initially performed with the body contacts biased with the nominal voltages, i.e., 0 V for the NMOSFETs and 1.2 V for the PMOSFETs. Simulations were then repeated to mimic history effects with the body of the off state NMOSFETs and PMOSFETs biased at 50 mV from the nominal value. A change of 50 mV is based on the value reported in [Ferl-08]. The exact change in the body bias will be different for different processes and even for designs in the same process, the effective body bias will depend on the type of layout and the contacts to the well and substrate regions. Here a change of 50 mV is used to illustrate the effect on pulse broadening and on the SET distribution. In the case of off-state NMOSFETs, the history effect leads to an increase in the body bias and in the case of PMOSFETs, it leads to a decrease in the body bias. Thus the body of the off state NMOSFETs was biased at +50 mV (instead of 0 V) and the body of the off state PMOSFETs was biased at 1.15 V (instead of 1.2 V). The changes to the body bias of both devices are equivalent in that they reduce the magnitudes of the threshold voltages of the devices.

Fig. 5.16 shows plots of the transient pulse width as a function of the inverter stage number. A 100 ps transient propagates without significant attenuation through the 100 inverter stages for the simulations without history effects. The same initial transient width increases to about 134.7 ps after 100 stages when history effects are included in the simulations. This translates to an increase of about 0.35 ps per inverter stage. Additional simulations show that the increase in the transient width is the same regardless of the initial pulse width. Furthermore, even with the inclusion of history effects, transients that are less than about three times the propagation delay of a single inverter stage are still

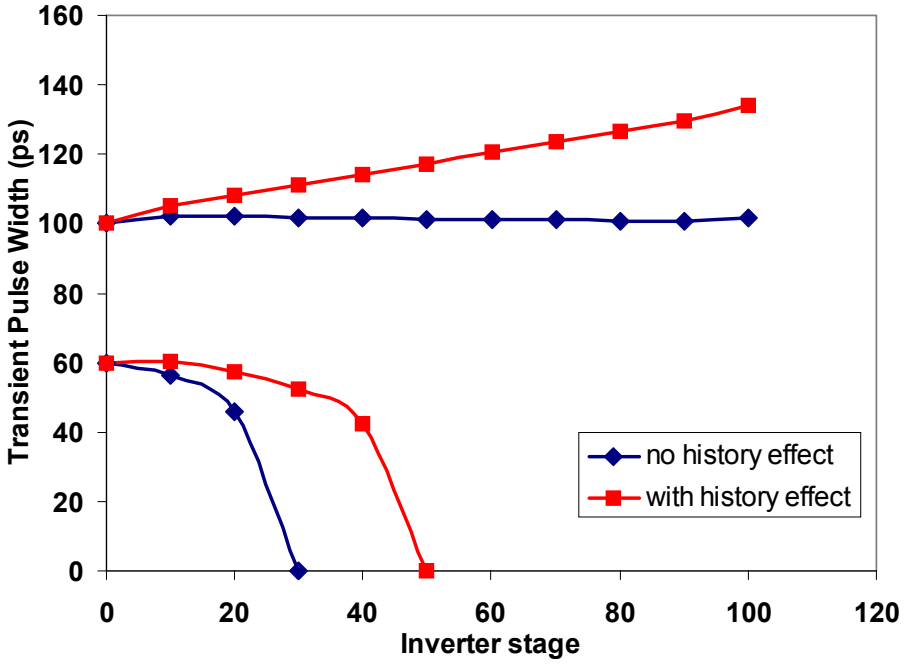



Fig. 5.16 Propagation of transients through a chain of inverters in the 90-nm process with and without the history effect.

attenuated. As shown in Fig. 5.16, a 60 ps transient is completely attenuated by about 30 stages for the normal simulation without history effects, while the same transient gets completely attenuated by the 50$^{th}$ stage when history effects are included. The attenuation of short transients was suggested as the reason the circuit does not measure many such transients. These results suggest that the presence of history effects does not increase the likelihood of measurement of very short transients.

Assuming the presence of history effects leads to a 0.35 ps increase in transient width per inverter stage, then the maximum increase in transient width for the 90-nm measurements would be about 350 ps (as the target circuit for the 90-nm test circuit is composed of a chain of 1000 inverters). Moreover the increase in the SET pulse width would vary from about 0 ps (for strikes in the target inverter chain close to the measurement circuit) to 350 ps (for strikes at the beginning of the target inverter chain).

The observed SET distribution should consist of the original distribution convolved with a linearly increasing function corresponding to the increase in transient width as a function of the location of strike in the inverter chain.

To illustrate the impact of pulse broadening on SET distribution, a Gaussian distribution of SET pulse widths at each LET was convolved with a linear function corresponding to pulse broadening caused by the history effect. Fig. 5.17 shows plots of a possible original distribution of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused history effects and the actual measured SET events. From such analysis, a likely original distribution of SETs without pulse broadening was obtained for different LETs. Fig. 5.18 is a box chart of the actual measured SET distribution and the likely original distribution adjusted for pulse broadening. The analysis indicates that with information on propagation-induced pulse

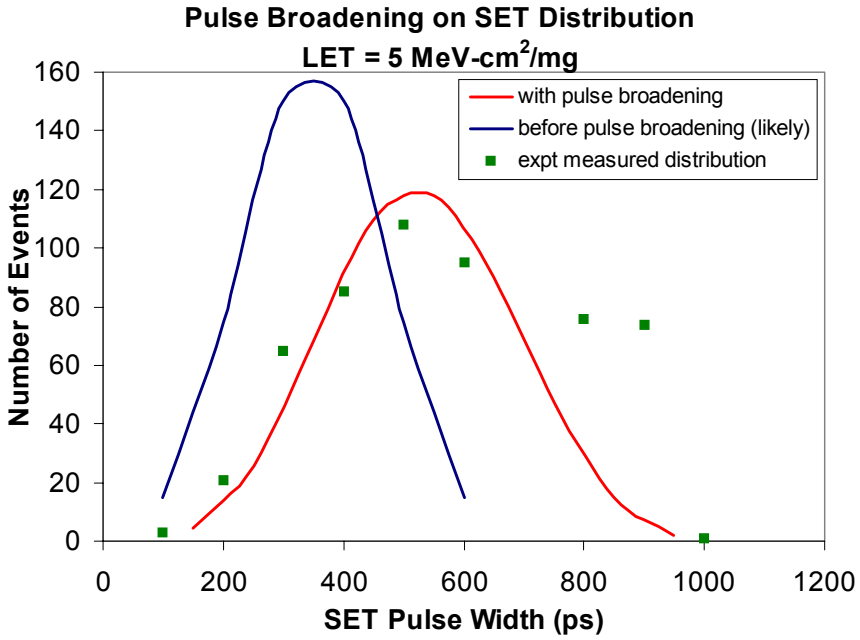



Fig. 5.17 The impact of pulse broadening on SET distribution is illustrated for a pulse broadening factor of 0.35 ps per inverter stage and for a chain length of 1000 inverters.

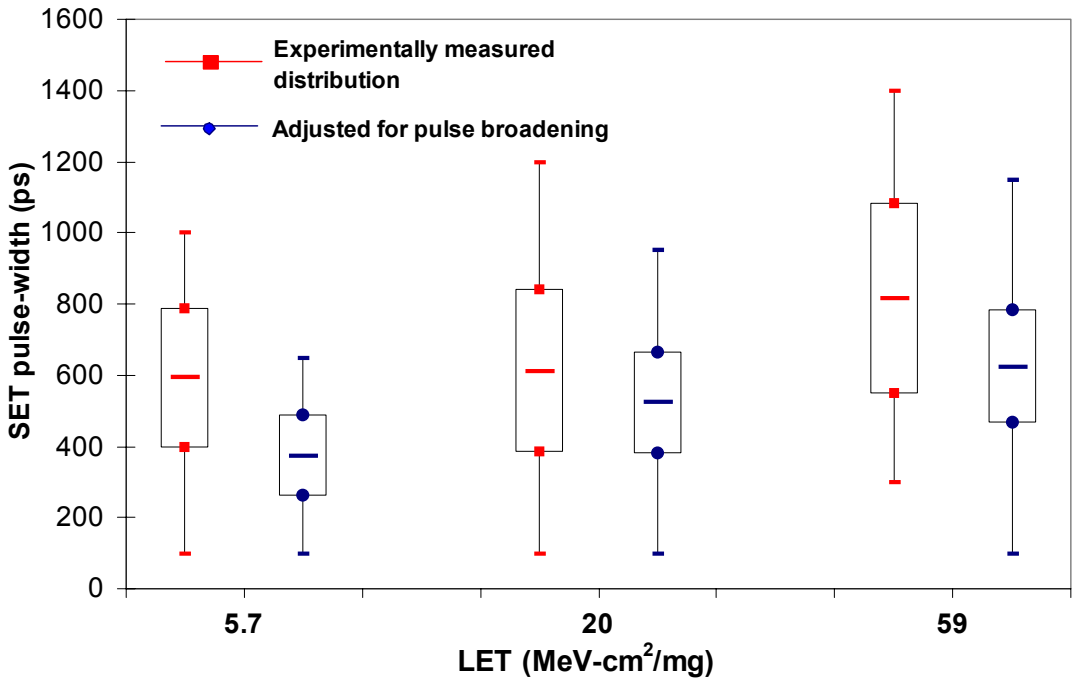



Fig. 5.18 Box plot of the original measured SET distribution and the distribution adjusted for pulse broadening assuming a broadening factor of 0.35 ps per inverter as a function of LET.

broadening, it is possible to obtain the original distribution of SET pulse widths. However, the exact mechanisms responsible for pulse broadening, particularly in bulk technologies remain to be determined.

To summarize the above discussions on long SETs at low LETs, it is likely that the SET pulse width distribution can be impacted by factors such as the mechanism of charge deposition (whether direct or indirect ionization through secondary reaction products), initial ion track diameter and circuit level effects such as drive currents. While TCAD results indicate that the history effect may be negligible for bulk devices, recent experimental evidence suggests the presence of propagation-induced pulse broadening even in bulk devices. The sources of such an effect, if any, for well-contacted bulk devices is still not well understood. However, assuming the presence of a certain amount

of pulse broadening due to history effects, an analysis to obtain the original SET distribution has been presented. A combination of one or more of these factors may result in relatively long transients at low LETs.

# CHAPTER VI

## NEUTRON AND ALPHA PARTICLE INDUCED TRANSIENTS

### *Neutron Induced SET Pulse Widths*

The 90-nm test chips were tested separately with neutrons and alpha particles [Nara-08]. Accelerated high-energy neutron tests were performed at the Weapon Neutron Research (WNR) test facility at Los Alamos Neutron Science Center (LANSCE). This neutron energy spectrum, plotted in Fig. 6.1, closely resembles the sea-level neutron spectrum for energies from 10 MeV to 500 MeV. Three circuit boards with two SET test chips per board were placed one behind another and normal to the path of the neutron beam as shown in Fig. 6.2. The center-to-center distance of the two SET test chips in each board was less than two inches and the boards were placed such that both chips were

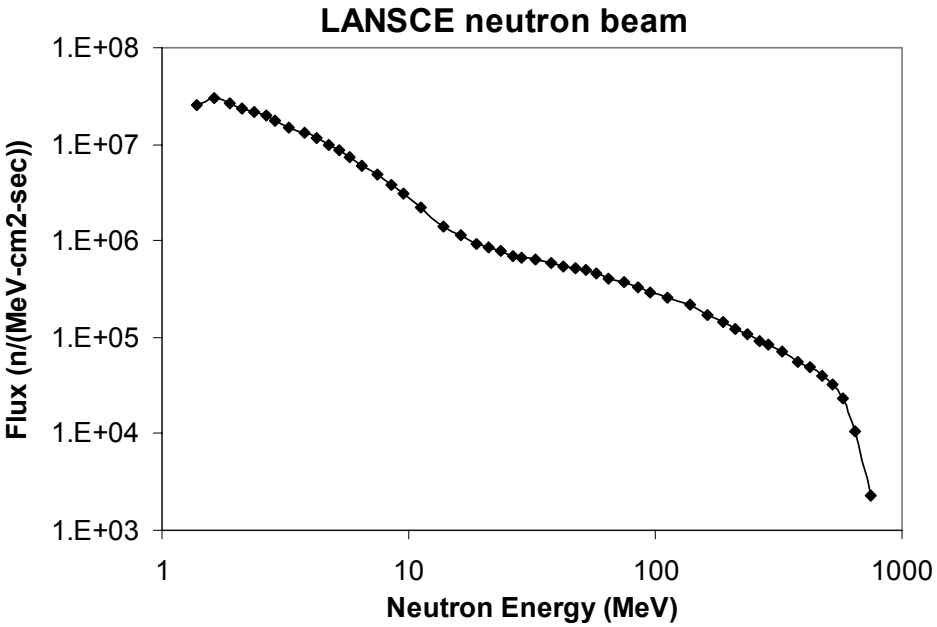



Fig. 6.1. Energy spectrum of the LANSCE neutron beam. This spectrum closely resembles the energy spectrum of terrestrial neutrons.

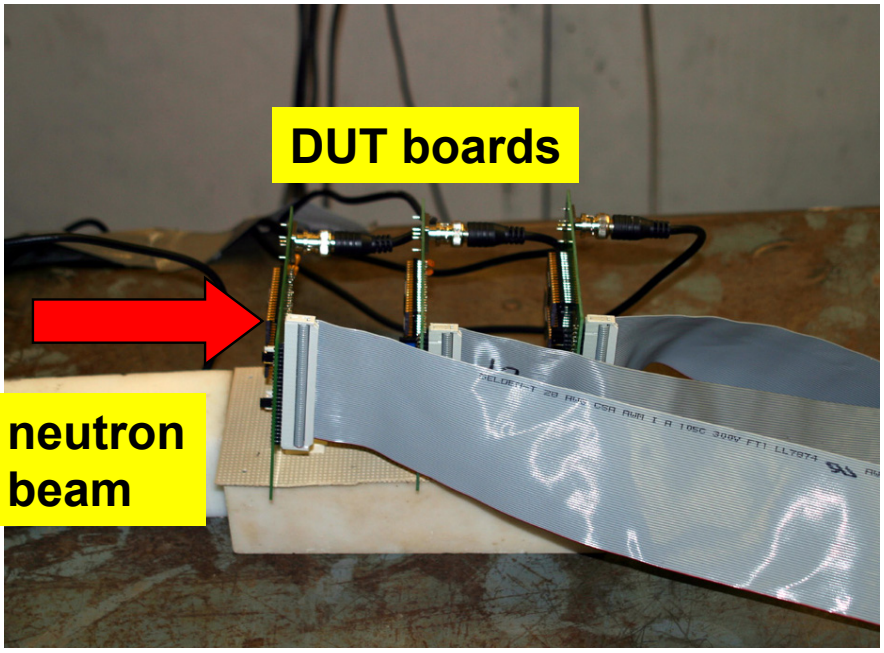



Fig. 6.2. Setup of the three DUT boards for the neutron experiments. The neutron beam direction is also indicated.

covered by the neutron beam which was 3 inches in diameter. The neutron beam penetrates through the circuit boards with minimum loss of flux, which enables testing of multiple chips at the same time. The total test time was about 102 hrs which resulted in a neutron fluence of $1.33 \times 10^{11}/cm^2$ based on the integration of neutron flux over the range of 10 MeV to 500 MeV. A total of 20 SET events ranging from about 300 ps to about 1.4 ns were measured during this test time. This converts to a neutron SET cross section of $2.5 \times 10^{-6}$ $\mu m^2$/inverter. Based on the layout, the sensitive area of an inverter used in this design is about 0.75 $\mu m^2$. The low event rate is attributed to the small area of the target circuits and to the fact that neutrons ionize indirectly through secondary reaction products. Fig. 6.3 shows the distribution of neutron-induced SET pulse widths.

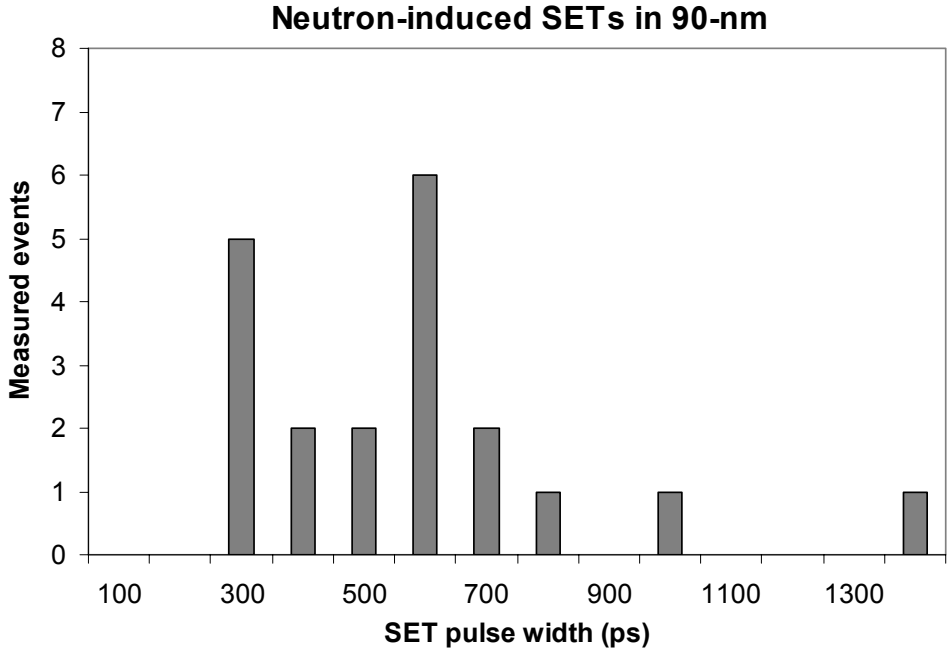



Fig. 6.3. Neutron induced distribution of SET pulses.

*Alpha-Particle Induced SET Pulse Widths*

Accelerated alpha particle tests were carried out at Texas Instruments using a foil of Americium-241 as the alpha source. The Americium-241 source was placed directly on top of the die while the device was operating and the transient pulses were recorded. The average energy of the alpha particles from this source is about 5.5 MeV. The total fluence of the alpha particles was estimated to be about $4.45 \times 10^{10}/cm^2$ and approximately 300 SET events were measured which converts to an alpha-particle SET cross section of about $6.74 \times 10^{-4}$ $\mu m^2$/inverter. Fig. 6.4 shows the distribution of alpha particle-induced SET pulses.

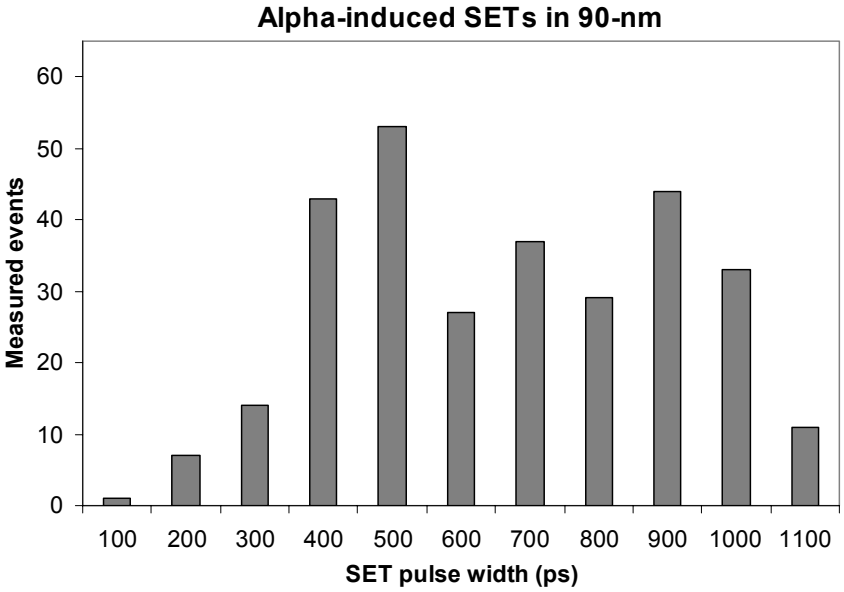



Fig. 6.4. Alpha particle induced distribution of SET pulses.

The measurement circuit attenuates most SET pulses that are less than about 250 ps, as pointed out earlier. However, transients ranging from a few hundred picoseconds to about a nanosecond or longer were measured for both alpha particles and for neutrons. While some of neutron reaction products with Si such as Mg and Al may have considerable LET to result in some longer transients, such transients were unexpected for alpha particles. The reasons outlined in the previous chapter for long transients observed with low LET heavy-ions, such as lower drive currents and the possibility of secondary reaction products, are applicable to neutrons and alpha particles as well and could have resulted in wider transients. Moreover, the angle of incidence of the alpha and neutron reaction products may have enhanced the charge deposited within the sensitive volume. With an increase in the incidence angle, the length of the path traversed by the energetic particle within the sensitive volume that collects charge increases, and may result in increased charge collection leading to wider transients. The incidence angle is not normal to the die for neutrons and alpha particles since the alpha particles from the source and

the secondary reaction products of neutron interactions can impinge on the sensitive region from different directions. Finally, propagation-induced pulse broadening effect through the long chain of target inverters may also have an impact on the observed SET pulse widths as mentioned in the previous chapter.

The distribution of neutron and alpha particle-induced SETs indicates the presence of some transients that may be wide enough to be mistaken as valid logic or clock signals in the 90-nm node. These results imply that as technology is scaled to lower voltages and higher operating frequencies SETs may become a reliability problem in the future.

A comparison of neutron, alpha and heavy-ion SET pulse width distributions is plotted in Fig. 6.5. The LET values for the ions are specified in Fig. 6.5. While the number of

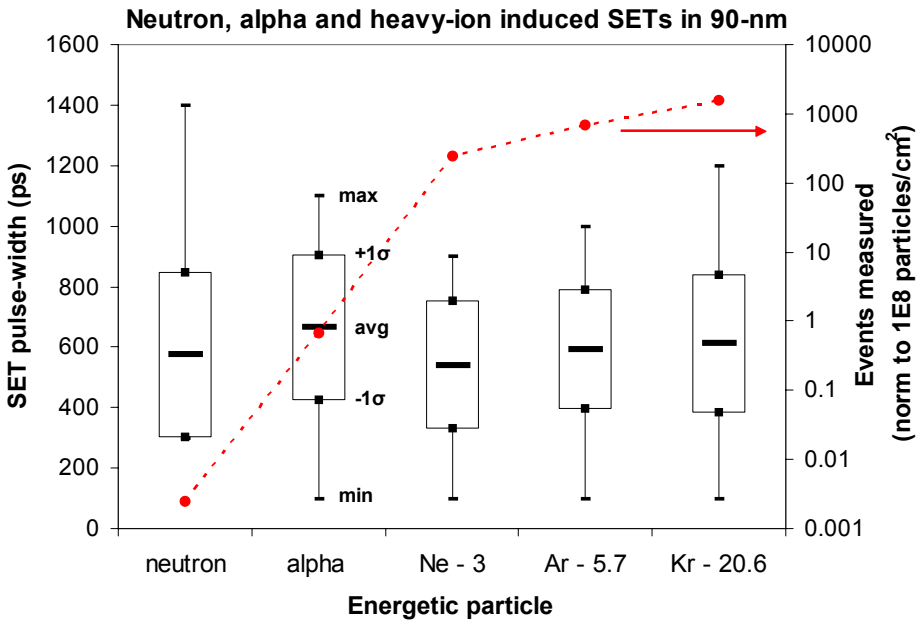



Fig. 6.5. Box plot representing the average, minimum, maximum and ±1 standard deviation in neutron, alpha and heavy-ion induced SET pulse widths along with the number of measured SET events normalized to $1 \times 10^8$ particles/cm$^2$. The ion energies for Ne, Ar, and Kr are 263 MeV, 929 MeV and 1858 MeV respectively. The ion linear energy transfer (LET) are 3, 5.7 and 20.6 MeV-cm$^2$/mg for Ne, Ar and Kr, respectively.

events varies with the particle type, the distribution of pulse widths was found to be similar for the different particle types. As expected, neutrons have the lowest event cross section as they ionize indirectly though secondary reaction products.

Monte Carlo based simulations were used to verify the experimental cross-sections and to identify scaling trends in SET cross-sections. These results are discussed in Appendix A at the end of this dissertation.

*Neutron and Alpha FIT Rates*

From the experimental SET cross section data, the failure-in-time (FIT) rate per inverter for this technology was estimated. The formula for computing the FIT rates is given by

$$\text{FIT/inverter} = \frac{\text{number of SETs measured} \times \text{particle flux} \times 10^9\,\text{hr}}{\text{total fluence} \times \text{number of target inverter cells}}$$

In this computation the number of SET events measured is derated to account for latch window and logical masking effects. This is because in a practical logic circuit design, masking effects result in only a fraction of the SET events that are created being latched as errors and hence the FIT rate computation needs to account for masking effects in order to be more accurate. Since SETs originating from a single chain of a target inverter circuit were measured in this work, the measurement does not account for logical masking. Similarly, all SETs that are not electrically attenuated are recorded and hence the measurement does not account for latch window masking effects. The measurement of the SET pulse widths, however, accounts for some electrical masking effects and hence no additional electrical derating is accounted for. The probability of latching an

SET pulse that is wider than the setup and hold times of a latch is simply given by the ratio of the SET pulse width to the clock period [Yana-08]. For this computation we assume a clock period of 1 GHz and that all SET pulses are wider than the latch setup and hold times. Logical masking may reduce the number of SET events that propagate to the latch element. Logical masking varies from circuit to circuit and even for a given circuit it depends on the inputs to the circuit. In [Nguy-05], logical masking is analyzed in detail for different circuit types and for sample computations the authors use logical masking values ranging from about 0.2 to 0.5. For this computation we choose a value of 0.5 for the logical masking.

Table 6.1. Alpha and neutron FIT per inverter.

| Particle | Total Fluence (particles/cm$^2$) | Derated FIT/inverter |
|---|---|---|
| **alpha (from package)** | $4.45\times10^{10}$ | **$1.1\times10^{-5}$** |
| **neutron (sea-level)** | $1.33\times10^{11}$ | **$4.4\times10^{-5}$** |

The drain area of the target inverter circuit designed in this work was increased to increase the probability of creating SETs for measurement. The drain area was increased by a factor of about 3× compared to a minimum drain area layout. Thus for standard layout practices, the SET cross section should be lower. The increase in the drain area is also accounted for in the computation of the FIT rates.

The average neutron flux is about 13 n/cm$^2$/hr at sea-level [Gord-04] and average alpha particle flux from package impurities is of the order of 0.01 alpha/cm$^2$/hr. Using the

derated number of SET events measured and the average flux values for neutrons and alpha particles, the FIT/inverter was calculated. Table 6.1 shows the FIT rate per inverter in this technology at sea-level for neutrons and alpha particles. The neutron FIT/inverter value computed in this work is slightly higher but comparable to the projections made in [Shiv-02]. In [Shiv-02], the authors simulated the critical charge and charge collection efficiency for logic and memory cells in different technology nodes and used an empirical model to calculate the SER based on the critical charge and charge collection efficiency. Shivakumar et al. projected the neutron FIT/logic gate to be about $10^{-5}$ for a 100-nm technology node.

In this work, error rates have not been measured for memory or latch circuits. However simulation based projections made by Shivakumar et al. indicate that the FIT/SRAM is of the order of $4\times10^{-5}$ for a similar technology node. This is very similar to the FIT/inverter value computed in this work and indicates that the chip-level soft error rate (SER) resulting from single-event transients may be a significant concern for some logic circuits. Other researchers have also characterized FIT rates for memory and latch circuits. However most reported values are based on normalized units and hence can not be directly compared with the FIT rates estimated in this work.

# CHAPTER VII

# CONCLUSIONS AND FUTURE RECOMMENDATIONS

## *Key Results and Findings*

An autonomous pulse characterization technique was developed for the first-time for single-event transient pulse width measurements. The technique measures pulse width of individual SETs and results in characterizing the distribution of SET pulse widths for a given radiation environment. Circuit designs were implemented in IBM 130-nm and 90-nm bulk CMOS processes. Heavy-ion SET measurements show a reduction in the threshold for a measurable SET from about 7 MeV-cm$^2$/mg for 130-nm to less than 2 MeV-cm$^2$/mg for 90-nm. SET pulse widths ranging from about hundred ps to over 1 ns were measured in 130-nm and 90-nm processes and the pulse widths were found to increase when scaling from 130-nm to 90-nm. Reductions in drive strength and n-well contact sizes were identified as factors that lead to the observed increase in pulse widths from 130-nm to 90-nm.

A first-ever neutron and alpha SET measurements in the 90-nm process shows most such SETs to be of the order of hundreds of picoseconds. Neutron and alpha FIT rates were found to be about $10^{-5}$ FIT/inverter. The per device FIT rates computed in this work correspond well with simulation based projections made in [Shiv-02] and are also comparable to the simulation estimates of per bit SRAM and latch FIT rates in [Shiv-02] for a similar technology node, indicating that logic SER will be an issue for certain terrestrial applications.

*Conclusions*

An autonomous SET pulse characterization technique has been developed and implemented in a range of CMOS technology nodes for measuring the distribution of SET pulse-widths. The test chips were used to measure heavy-ion, neutron and alpha-particle induced transients. The test structure was designed such that only SETs created in the target inverter circuit are measured and the measurement is not affected by hits on the measurement circuit. The minimum pulse width needed for propagation through multiple logic gates was derived in terms of the propagation delay of a logic gate. The analysis, along with simulation results, was used to show that transients greater than about three times the propagation delay of a single latch stage are able to propagate through the measurement circuit with less than 10% attenuation. Thus the measured width, within accuracy limits of measurement, is the actual width for such SETs. This ensured accurate measurement of the SET pulse widths over a wide range. As the measurement technique enables measurement of most of the SET pulses created in the target circuit that are greater than about three times the delay of single latch stage, a distribution of SET widths for every ion or energetic particle was obtained. The measurement technique, however, does not accurately capture transients that are shorter than three times the delay of a single latch stage and hence the lower end of the distribution of SET pulse widths may contain more events than those that are captured by the measurement circuit. Nonetheless, the measured SET distributions allow for precise estimation of error cross sections for combinational logic circuits over a wide range of SET pulse widths. TCAD results indicate that variations in the strike location lead to the observed variations in the SET pulse widths at a given ion LET.

Heavy-ion test results indicate that the threshold for measurable SET events has decreased from about 7 MeV-cm$^2$/mg for the 130-nm process to less than 2 MeV-cm$^2$/mg for the 90-nm process. While the number of SET events depends strongly on the ion LET for both the 130-nm and 90-nm processes, the range of SET pulse widths and the average value of the SET pulse width shows a smaller dependence on LET for the 90-nm process compared to the 130-nm process. Moreover, the SET event cross section is dominated by SET pulses ranging from about 300 ps to about 700 ps in the 130-nm process and this range increases to about 400 ps to 900 ps for the 90-nm process. A comparison of the 130-nm and 90-nm SET distributions shows that the average SET pulse width increases with scaling for these particular technology nodes.

Mixed-mode 3D-TCAD simulations were used to understand the experimentally observed trends in SET pulse widths as well as to identify causes for long transients at low LETs. The effects of parameters such as drive strength, load capacitance and contact width on SET pulse widths were simulated. Simulation results also indicate an increase in the SET pulse width with technology scaling for these technology nodes. The primary reasons for this increase were identified as a reduction in the restoring drive current for minimum sized devices and a reduction in the minimum contact sizes with scaling from 130-nm to 90-nm. Both these factors result in extending the time taken to neutralize the deposited charges, leading to an increase in the SET width. Experimental results obtained for circuits with multiple well contacts and guard bands surrounding each device compared to circuits with single well contacts per device in the 130-nm process confirm that the use of stronger contacts to the well and substrate reduce the number of long transients. SET pulse width distributions were also measured for different supply voltages

in the 130-nm process. With a lower supply voltage, the average and range of SET pulse widths was found to increase. These results confirm that a reduction in the drive strength (due to lower supply voltage) leads to longer SETs.

TCAD simulations also indicate that variations in the load capacitance have a negligible effect on the SET pulse width. This is because the load capacitance affects only the rise and fall times to charge or discharge a node due to an SET strike, but the capacitance does not directly impact the time for which a node stays affected.

The reasons for long SETs at low LETs were examined by analyzing the factors that affect the simulated and measured pulse widths. Restoring drive strength and the initial ion track diameter were found to have a significant effect on SET pulse widths at low LETs. TCAD simulations also show that the history effect caused by charge leakage into the body of off-state devices is not an issue for bulk devices. However, based on recent observations of pulse broadening for bulk devices, circuit simulations were used to illustrate the effect, assuming that the body potentials of the off-state devices depend on the bias history. An analysis to obtain the likely original SET distribution without pulse broadening was also presented. A combination of different factors, including the possibility of pulse broadening effects especially for the long inverter target circuit in the 90-nm test chips, can lead to variations between the simulated and measured width of SETs at low LETs.

With combinational logic soft errors projected to dominate the reliability issues of advanced semiconductor ICs for commercial terrestrial applications, it is essential to estimate the neutron and alpha-particle induced distribution of SET pulses for better prediction of error rates and for developing appropriate mitigation techniques. The

neutron and alpha particle-induced SET pulse width distributions were measured using the SET test chip fabricated in a 90-nm CMOS process. Results indicate that the widths of these SET pulses range from 100 ps to over 1 ns. FIT rates for alpha particles and neutron were estimated to be about $1\times10^{-5}$ and $4\times10^{-5}$/inverter, respectively. The per device FIT rates computed in this work correspond well with simulation based projections made in [Shiv-02] and are also comparable to the simulation estimates of per bit SRAM and latch FIT rates in [Shiv-02] for a similar technology node. While the overall size of memory circuits in terms of the number of cells is significantly larger than the overall size of combination logic circuits, the results indicate that logic SER will be an issue for certain terrestrial applications.

*Future Recommendations*

This work shows that the autonomous SET characterization technique can be used to obtain the distribution of SET pulse widths for any radiation environment and for any combinational logic circuit. However, as with any test circuit, the measurement circuit should have minimal impact on the measurement itself for an accurate characterization. In this work, one of the reasons for observing long transients at low LETs in the 90-nm technology node could be the use of a single chain of one thousand inverters as the target circuit compared to the chain of one hundred inverters used in the 130-nm process. The larger the target circuit area, the greater is the number of SET events measured for the same ion fluence and hence it was decided to increase the target inverter chain length for the 90-nm test chips. At the time of the 90-nm test chip design, extensive SPICE simulations were performed on both a long chain of inverters as well as the complete SET measurement circuit and they did not reveal any pulse attenuation or broadening effects for transients longer than three times the delay of a single latch stage. TCAD simulations also suggest that history effects, which are known to affect pulse propagation in SOI devices, are not an issue for bulk processes. However, based on recent measurements for bulk devices, propagation induced pulse broadening may be an issue for some bulk designs [Ferl-08]. This along with the other factors that were outlined may have resulted in some of the long transients at low LETs. It is thus recommended that future SET test chip designs use shorter chains for the target circuitry. To improve the target circuit area, multiple shorter chains may be logically ORed together.

APPENDIX A

# MONTE CARLO SIMULATION ANALYSIS OF SCALING TRENDS IN CROSS SECTIONS

To verify the experimental neutron and alpha cross sections, simulations were performed using the Monte Carlo Radiative Energy Deposition (MRED) code [Warr-05]. MRED is a simulation tool for calculating the energy deposited by radiation in microelectronic devices, based on the Geant4 libraries [Agos-03]. The MRED simulation structure is a 50 µm × 50 µm × 16.25 µm tall block, corresponding to the materials in the test structure as shown in Fig. A.1. Overlayers account for 12.25 µm of the height of the structure and consist of $SiO_2$, copper, and polyimide layers, while the remaining 4 µm at

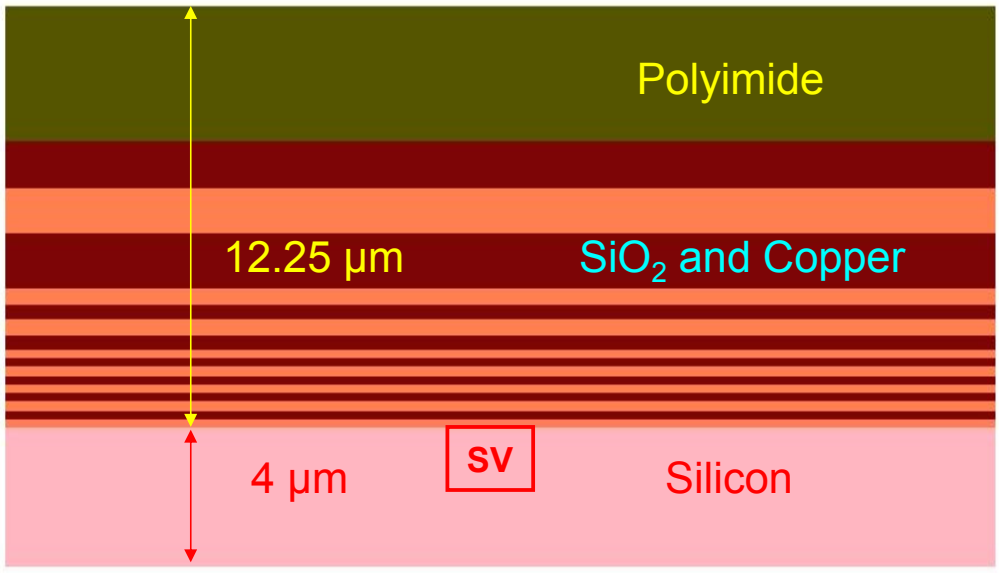



Fig. A.1. Side view of the structure used for MRED simulations

the bottom of the structure is the silicon region. Simulations were performed corresponding to the heavy ions and energies used at the Texas A&M cyclotron facility. The sensitive volume (the volume in which the charge generated is recorded by MRED) was calibrated to the heavy ion data. A critical charge of 20 fC was found to fit the experimental heavy-ion cross sections well. This indicates that a measurable SET event is created only when the generated charge within the sensitive volume is greater than 20 fC. The cross section is estimated from the number of particles that are able to generate a charge greater than the critical charge of the device within this volume.

Using the model calibrated to the heavy ion results, simulations were performed with 5.5 MeV alpha particles arriving at random angles across the top of the simulation structure. Fig. A.2 shows a plot of the integral SET cross section as a function of the generated charge. From this plot, the SET cross section was estimated to be

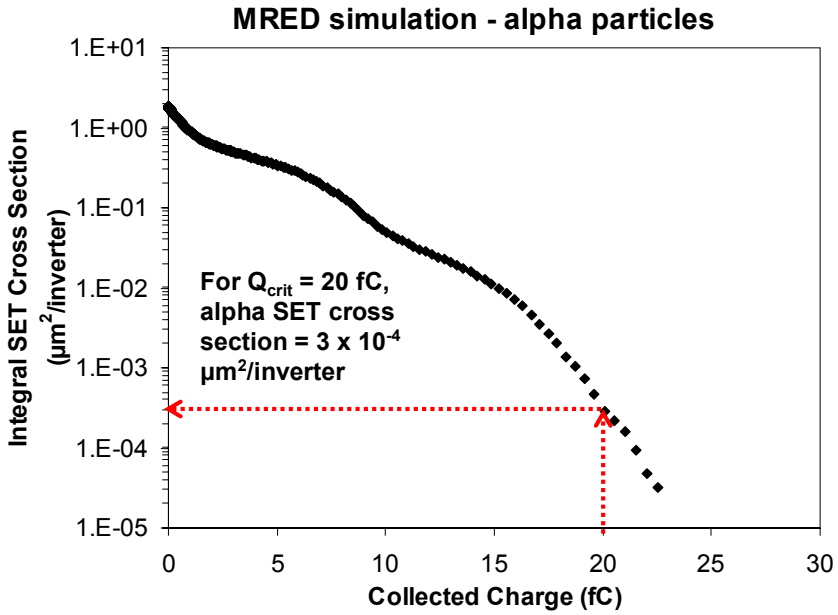



Fig. A.2. MRED simulation with alpha particles showing the integral SET cross section as a function of collected charge. The simulated alpha SET cross section for the critical charge of 20 fC closely matches the experimental value of $6.74 \times 10^{-4}$ $\mu m^2$/inverter.

$3 \times 10^{-4}$ µm$^2$/inverter for a critical charge of 20 fC. The simulated cross section compares well with the experimental cross section of $6.74 \times 10^{-4}$ µm$^2$/inverter.

MRED simulations were also performed using neutrons with energies corresponding to the LANL spectrum. The results of these simulations are plotted in Fig. A.3. From Fig. A.3, the SET cross section was estimated to be about $2.49 \times 10^{-6}$ µm$^2$/inverter for a critical charge of 20 fC. This simulated value closely matches the experimentally measured cross section, which was $2.5 \times 10^{-6}$ µm$^2$/inverter.

The simulations were also repeated by scaling the device dimensions and the sensitive volume to that of a 65-nm process to estimate the scaling in the cross-section. Fig. A.4 (a)

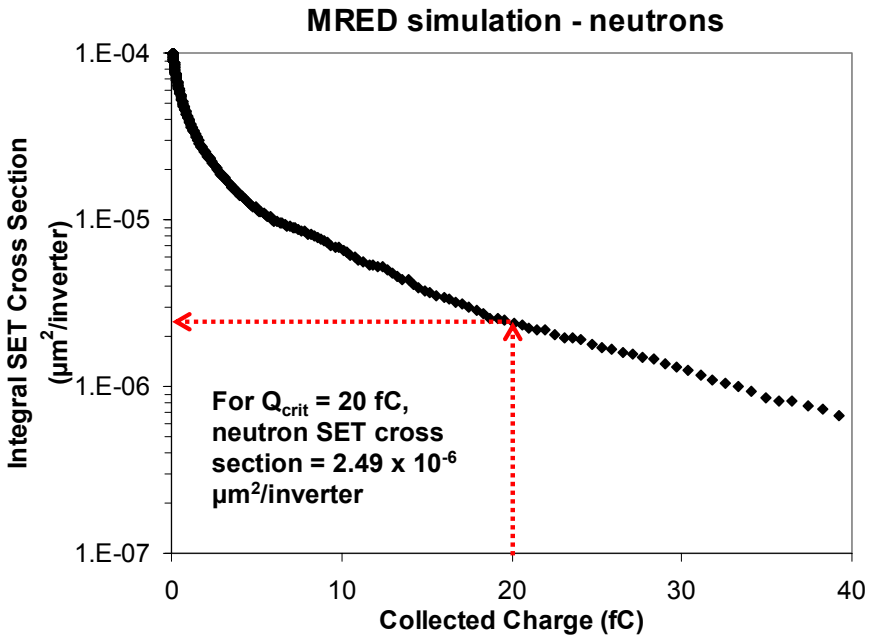
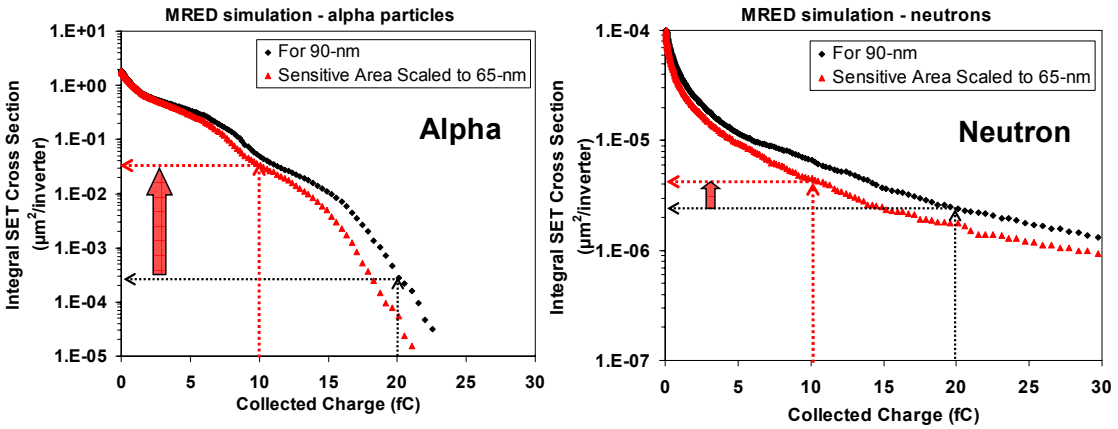



Fig. A.3. MRED simulation with neutrons showing the integral SET cross section as a function of collected charge. The simulated neutron SET cross section for the critical charge of 20 fC closely matches the experimental value of $2.5 \times 10^{-6}$ µm$^2$/inverter.

and (b) show plots of the integral SET cross section as a function of the generated charge for neutrons and alpha particles, respectively. Previous work has shown that the critical

charge reduces by a factor of about two with each new technology node [Shiv-02]. While the exact value of the critical charge may vary depending on the type of circuit, these simulation results are used to illustrate trends in the cross-section. For the 65-nm process, with reduced critical charge, the cross-section is found to increase more rapidly for alpha particles. The alpha particle-induced SET cross-section increases by close to two orders in magnitude, while the neutron SET cross-section increases by a factor of about two. Recent research has shown that for an alpha particle to create a measurable SET it has to arrive within a certain range of angles so that the Bragg peak of charge deposition occurs within the sensitive volume [Gadl-08]. The alpha particles that are emanated from, say, a point source arrive at the sensitive volume at different angles of incidence and only a fraction of these are able to create SETs. With technology scaling and the subsequent reduction in critical charge, the range of angles of incidence over which an alpha particle can create measurable events increases, increasing the SET cross-section significantly. Since the charge generated by neutron reaction products is usually greater than the




(a) (b)

Fig. A.4. Estimation of scaling trends in (a) alpha and (b) neutron SET cross sections. Results indicate alpha SET cross section may increase more rapidly than neutrons SET cross sections.

critical charge, upset rates due to neutrons do not show a significant increase with scaling. The increase in the susceptibility of circuits to alpha particles has also been observed in previous work [Seif-06]. The results indicate that alpha particle-induced error rates may become greater than neutron-induced error rates with technology scaling.

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