ON CHIP CHARACTERIZATION OF SINGLE EVENT TRANSIENT PULSE WIDTHS

By

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CHAPTER I

INTRODUCTION

As the dimensions and operating voltages of integrated circuits (ICs) are shrunk to satisfy the consumer's ever increasing demand for lower power and higher speed, their sensitivity to radiation increases dramatically [1]. Modern sub-micron devices show an increased susceptibility to single event effects (SEEs) [2]. A single event (SE) occurs when an energetic particle, such as a heavy ion or neutron, strikes a device and causes a change in the device's normal operation. Some of the single event effects (SEEs) are also referred to as soft errors in the commercial domain.

Soft errors are the primary radiation concern for commercial terrestrial applications, as opposed to parametric degradation and hard errors, which are significant concerns in space and military environment [1]. A soft error occurs when a radiation event deposits enough charge to reverse or flip the data state of a memory cell, register, latch, or flip-flop. The error is "soft" because the circuit/device itself is not permanently damaged by the radiation and the error can be corrected by writing new data. In contrast, a "hard" error is manifested when the device is physically damaged and the data loss is permanent.

There are different mechanisms by which soft errors occur and the important types are the single event upset (SEU) and the single event transient (SET). An SEU is a static upset in storage cells such as latches and flip-flops. Upset rate due to such an event is independent of the clock frequency. For CMOS ICs, an energetic particle strike can cause a transient voltage perturbation, called a single event transient (SET), that propagates

through the circuit and may become stored as incorrect data, causing disruption of the circuit operation. Upset rates due to SETs are dependent on the pulse width of the SET and the clock frequency. With increasing clock frequency there are more latching clock edges to capture an SET. With decreasing feature sizes the charge required to represent a logic HIGH state decreases resulting in an increased number of SETs. Thus the characterization of SETs in digital ICs has become more critical as clock speeds have increased and feature sizes have decreased in modern IC processes [2].

This thesis presents a novel circuit technique that can be used to characterize single event transients. Simulation results for a range of technologies from 0.13-µm to 1.5-µm are included. Test chips have been fabricated in a 1.5-µm technology through MOSIS and laser test results have been used to validate the technique.

CHAPTER II

SETs – BACKGROUND

Need for Characterization

The formation of an SET involves three steps, namely charge generation, charge collection, and circuit response [2]. Charge generation depends on the properties of the incident particle and also on the properties of the semiconductor material that it strikes. Electrical parameters such as applied bias and the doping levels in the semiconductor will affect the charge collection. The topology of the circuit affects the circuit response.

When an energetic particle strikes the semiconductor material it loses energy through Coulombic interactions with the bound electrons in the material. The subsequent ionization of the material causes a dense track of electron-hole pairs to be created (Fig. 1). The average energy required to produce an electron-hole pair in silicon is 3.6 eV. For energetic particles, one can compute the charge that will be generated in the semiconductor material from the Linear Energy Transfer (LET) [1, 2]. In silicon, which has a density of 2.42 g/cm^3, the amount of electron hole pairs (Q) created along a track of length L is given by the following equation:

$$Q \quad (pC) \quad = \quad 0.011 \times L\,(\mu m) \times LET\,(MeV - cm^2 / mg) \qquad (1.1)$$

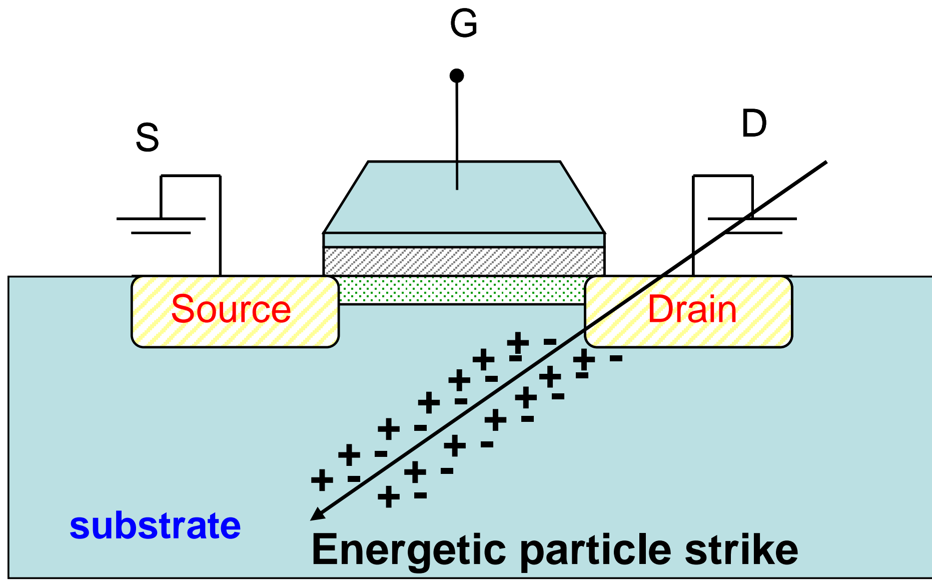

Fig. 1. Generation of electron-hole pairs due to an energetic particle strike

Charge collection is the next stage in the formation of SETs. The electric field associated with a junction in a transistor causes charge separation. Charge collection occurs when the charge track traverses a depletion region, or is within a diffusion length. Charge collection is greatest in reverse-biased junctions because of the greater thickness of the depletion region [2]. These would include the drain/well and drain/substrate junctions in CMOS transistors.

Charge initially collected from the depletion layer is termed as *prompt* charge. In some cases the depletion layer may extend into the lightly doped region in the direction of the ion track. This extension of the depletion layer is termed as funneling and it results in the collection of additional charge, thus increasing the sensitivity of the device to SETs [2].

In a combinational circuit, if enough radiation-induced charge is collected, an SET that propagates along the combinational chain will be generated as shown in Fig. 2. The

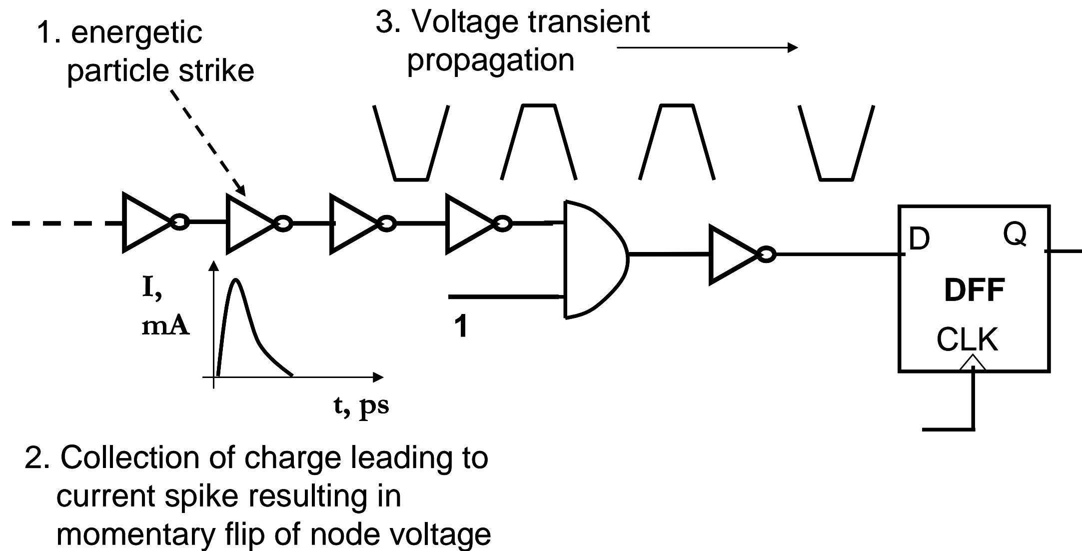

Fig. 2. Single event transient propagation through a combination logic chain

collection of charge first results in a current spike. This current pulse is usually modeled using a double exponential current source in simulators and is discussed in chapter IV. This current spike may momentarily flip in the state of the output node, thus causing a "glitch" or transient to propagate along the combinational logic chain. If this radiation-induced "glitch" propagates to the input of a latch or flip-flop during a latching clock signal, the erroneous input will be "latched" and stored. Depending upon the magnitude of charge collected, the width of this transient voltage pulse varies and it is this pulse width (along with clock frequency) that determines the vulnerability of the circuit to SETs.

For older technologies the SET could not propagate through a large number of logic gates since it usually did not produce a full output swing and was quickly attenuated due to large load capacitances and large propagation delays [1]. In advanced technologies

with lower propagation delays and higher clock frequencies, the SET could more easily traverse many logic gates, and the probability that it is latched increases [1].

Previous work has shown that errors due to SETs increase linearly with clock frequency [4]. Fig. 3 shows the relative contribution to error rates for combinational and sequential logic as a function of frequency [4]. At higher frequencies, or for advanced technologies, the error rates for combinational logic have begun to dominate [4-7]. This can be easily explained by the lower charge requirements to represent a logic HIGH state (resulting in higher number of SETs) and the increased number of clock edges for latching SETs [5]. Recent work suggests that for 0.25 μm and smaller technologies, SETs in combinational logic will dominate single-event related reliability issues [8].

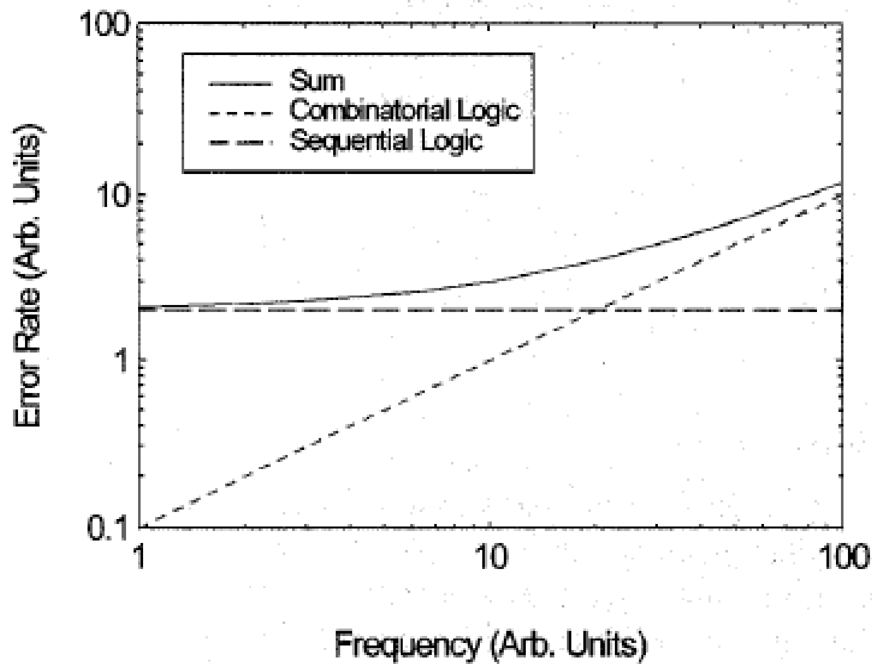

Fig. 3. Error rates in combinational and sequential logic as a function of frequency (after [4])

The probability that a SET will result in an error is dependent on the propagation distance through the combinational logic circuit and the arrival time of the SET at the latch input [2-9]. Wider pulses have a greater probability of being present at the latching edge of the clock. Thus, characterizing transient pulse width is of paramount importance in both determining and mitigating single-event effects for advanced technologies.

Transient pulse width is determined by many factors, including the nature of the ionizing particle, technology used, location of the strike, and incident angle [2, 10–13]. Modern sub-micron ICs are vulnerable to ionizing alpha particle and heavy ion strikes and also to terrestrial neutrons that deposit charge through indirect ionization [3]. Different ionizing particles interact differently with the silicon to deposit charge. Alpha particles that come from the radioactive decay of packages used for ICs have been a source of SETs through direct ionization in silicon. Energetic neutrons and protons can produce SETs indirectly through elastic scattering or a nuclear reaction in silicon. Low energy neutrons can also interact with the boron in a semiconductor device, producing reaction products that can cause an SET. Cosmic ray heavy ions are also a source of SETs. The charge deposited by the different ionizing species varies greatly and this affects the transient pulse width. For example, the charge deposited by the products of neutron-induced reactions (25-150 fC/μm) is much greater in magnitude than that deposited by alpha-particles (4-16 fC/μm) and hence poses a greater threat [3]. Likewise the angle of the incident ionizing particle also significantly affects the charge collected and hence the pulse width.

Other Characterization Methods

Previous studies indicate an increase in pulse width with the Linear Energy Transfer (LET) of heavy ions (Fig. 4) [14]. These results demonstrate the value of on-chip characterization of SET pulse widths in modern IC processes. Transient current pulses have also been measured directly using oscilloscopes [15-17]. As the SET pulse must be taken off-chip, such direct measurements are difficult because of pulse distortion due to the capacitance of the measurement (loading and line capacitance effects).

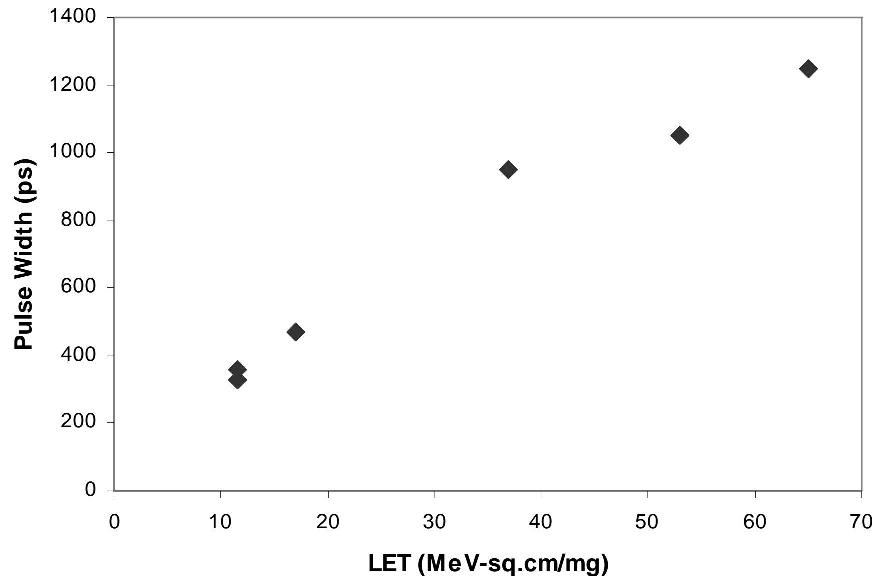

Fig. 4. SET pulse width as a function of LET for a 0.18-µm technology device (after [14])

Other researchers have characterized transient pulse widths using multiple latches with delayed signal paths [14] and/or delayed clock signals. The advantage of this method is that the delay can be continuously varied. However, multiple identical hits are needed while the delay is matched to the transient pulse width. Another approach is the use of a chain of cell copies that are monitored by latches to characterize the pulse width in terms

of multiples of the individual cell delay [19]. In this approach, the latches are clocked continuously to obtain information about the state of the cells. Since there are limitations to the maximum clock frequency that can be applied, it can be difficult to capture a very fast SET pulse using this approach.

In this thesis, a new SET test circuit is described that can complement the techniques previously proposed. This test circuit can characterize the width of SET pulses without the need for an external trigger or multiple laser strikes. The basic principle of operation of this circuit is similar to the one proposed in [19] but incorporates a *self-triggering* mechanism that does not require an outside signal to determine the presence of an SET pulse. This test circuit captures the SET pulse in a series of latches, which can be easily read out to determine the width of the pulse. This circuit technique can be used in CMOS and BiCMOS processes (including SOI technologies) regardless of feature size or operating speed.

CHAPTER III

AUTONOMOUS PULSE-WIDTH CHARACTERIZATION

Pulse Capture Circuit

A basic unit for elapsed time in a digital IC is the propagation delay associated with an inverter, designated as one inverter-delay. The test circuit described here characterizes the SET pulse width in units of inverter-delays. Pulse width is defined as the width of the pulse measured at the inverter threshold ($V_{dd}/2$). If an SET pulse of sufficient duration is input to an inverter chain, it will propagate through each inverter after a specific time delay (e.g., it will reach the third inverter after two inverter-delays, it will reach the fifth inverter after four inverter-delays, etc). This is shown in Fig. 5 where the leading edge of

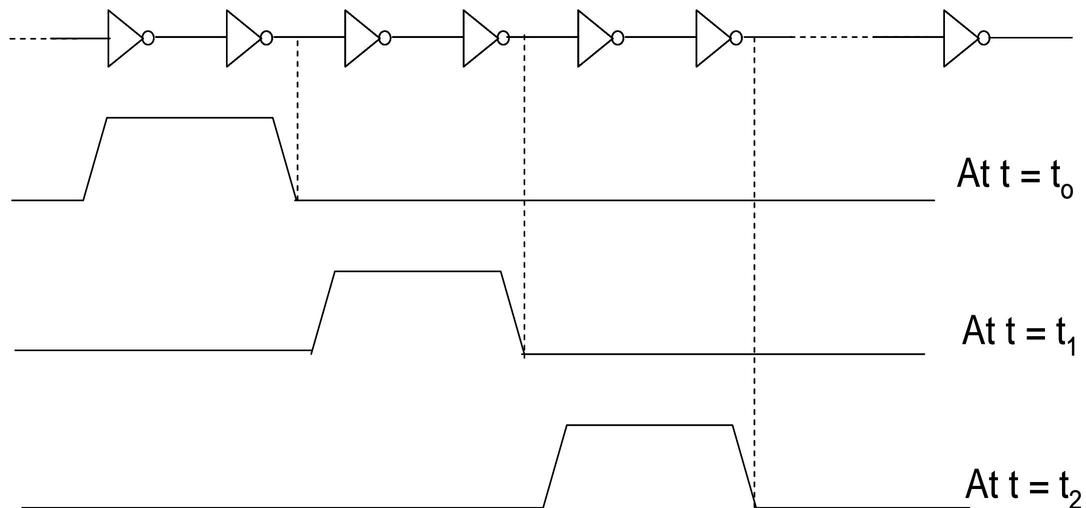

Fig. 5. Pulse propagation through a series of inverters. Time instances t_0, t_1, t_2 are 2 inverter-delays apart

the transient pulse is shown to reach the inputs of inverters in a chain at different instances of time. As time progresses, this transient propagates through a series of inverters. Thus, at any instant of time, a certain number of inverters will have their outputs affected/switched. This number of affected inverters is proportional to the transient pulse width. For extremely short pulses, the pulse gets attenuated as it propagates through logic gates. As discussed in [20], pulses wider than the logic transition time of a gate will propagate through the gate without attenuation, while pulses shorter than the transition time will propagate with varying attenuation. For each technology, simulation results showed that the minimum pulse duration (measured at the inverter threshold of $V_{dd}/2$) for propagation through multiple levels of logic is approximately equal to the delay of the logic gate in that technology. Simulations also showed that pulse shaping has a negligible effect on the pulse width when the width of the pulse is greater than the transition time of the logic gate.

Fig. 5 illustrates an example of pulse propagation through a series of inverters when the SET pulse is two inverter-delays long. The pulse will affect two inverter outputs as it propagates through the chain. If the number of such inverters whose outputs are affected by the SET pulse can be determined at any instant, the pulse width can be estimated as a multiple of inverter-delays. Simulations showed that for all pulse widths between [(n–0.5) × stage delay] to [(n+0.5) × stage delay], the number of affected stages is n. Thus the pulse width determined will be accurate to within ± half the propagation delay of an individual stage.

To capture the affected outputs from a chain of inverters, the output of every inverter is connected to an asynchronous latch as shown in Fig. 6. As the SET pulse propagates

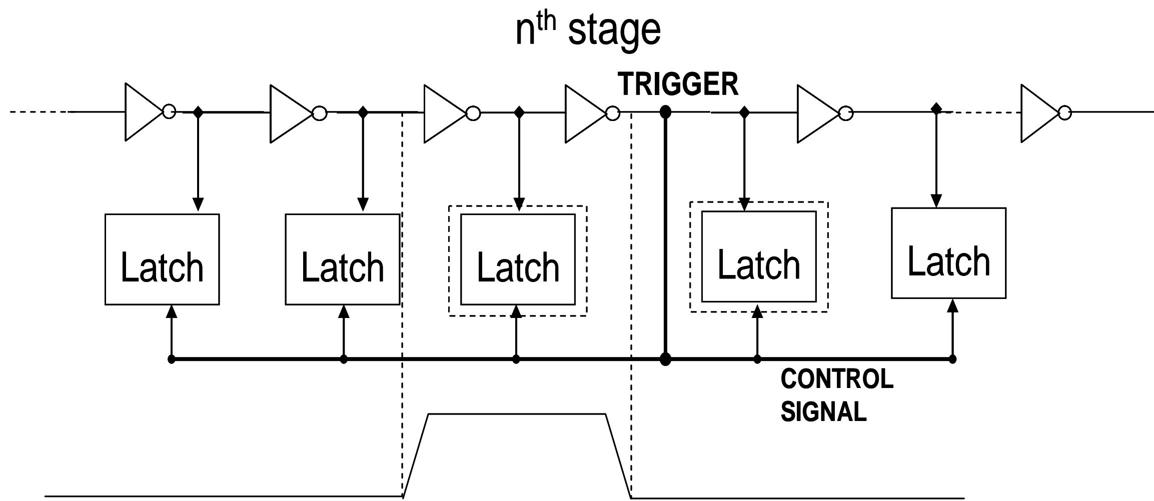

Fig. 6. The output of the nth stage can be used to provide hold signal for latches to freeze the data and the SET pulse

through an inverter, the data stored in its respective latch will change. However, once the SET pulse passes, the inverter output and latch data will revert to their original states. (Note that the additional loading due to the latch at the inverter output will alter the pulse characteristics. Hence, capacitance at the latch input must be minimized and accounted for in the inverter delay for accurate measurement of pulse width.) If the latches are placed in a *hold* mode while the SET pulse is within the inverter chain, each latch will retain the logic state of its respective inverter.

For laser tests, the exact instant when the hit takes place is known and the latches can be placed on *hold* after a certain delay, such that the SET pulse is guaranteed to be present within the inverter chain. However, for heavy ion testing, information regarding the hit time and hit node are usually not available. To address autonomous operation in such cases, the output of an inverter stage can be used as a trigger signal. To make this circuit *self-triggering*, a transition at the output of the nth stage (due to SET) can be used to

trigger the latches to hold the states of the inverters as shown in Fig. 6. As the output of the nth stage triggers the *hold* signal internally, precise information regarding the hit time (or location) is unnecessary. Any hit on stages beyond the trigger stage does not affect the trigger stage output. Thus, to latch an SET pulse, a hit must take place on a stage before the trigger stage.

The instant when the SET pulse is latched, the initial hit stage may or may not have recovered fully. If the initial stage has recovered fully when the pulse is latched, the pulse width measured is the actual pulse width (to within the accuracy of the measurement). However, if the initial stage has not recovered, it is possible that the charge collection is still continuing and the actual pulse width could be longer than the one measured. For laser tests the information regarding the state of the hit node is available. However, for heavy ion tests, the hit stage is not identifiable, and hence it can not be ascertained whether the hit stage has fully recovered or not. To address this uncertainty, a delay was introduced in the trigger signal. In addition, more inverter stages beyond the trigger stage are added to allow the SET pulse to propagate further. Thus, the delay on the trigger signal allows the SET pulse to propagate beyond the trigger stage. When the delayed trigger signal latches the SET pulse, the SET pulse may have propagated beyond the trigger stage. How far the SET pulse travels along the inverter chain is determined by the delay in the trigger signal. The delay in the trigger signal should be equal to the maximum SET pulse width expected for measurement. If the SET pulse has moved beyond the trigger stage, one can safely say that the estimated pulse width is the actual pulse width (within the accuracy of the measurement) irrespective of the hit node. This is because a hit on a stage beyond the trigger stage can not initiate a

latching process. Since the results provided in this thesis are based on laser tests, additional delay was not introduced and the chain length was kept at a minimum.

Based on the above approach, a test circuit was designed and evaluated. The lengths of all the transistors were set at the minimum allowed for the respective technology. The widths of the NMOS and PMOS transistors were chosen such that the gate has equal rise and fall times. Individual inverter stages were integrated with the latch design to reduce the loading due to latches (Fig. 7). With such integration, the logic transition time of each stage was found to be about 2.5 times the transition time of an individual inverter stage in that technology. (This was found to be true for all the technologies ranging from 1.5-µm to 0.13-µm that were used for our simulations). Thus pulses that are wider than 2.5 times the transition time of an inverter will propagate through the chain of stages without attenuation.

During the SET-propagate phase, the *pass* signal is ON and the *hold* signal is OFF. As a result, each inverter output is connected to the next stage, allowing the SET pulse to propagate through the inverters and passgates. When the leading edge of the SET pulse reaches the nth stage it triggers an SR flip-flop, which subsequently turns off all passgates by inverting the *pass* signal and freezing the data in the latches by turning on the *hold* signal. The number of latches whose output is affected will be directly proportional to the SET pulse width. Once the latch outputs have been read out, a *reset* signal is used to initialize the *pass* and *hold* signals and make the circuit ready for measuring the next pulse.

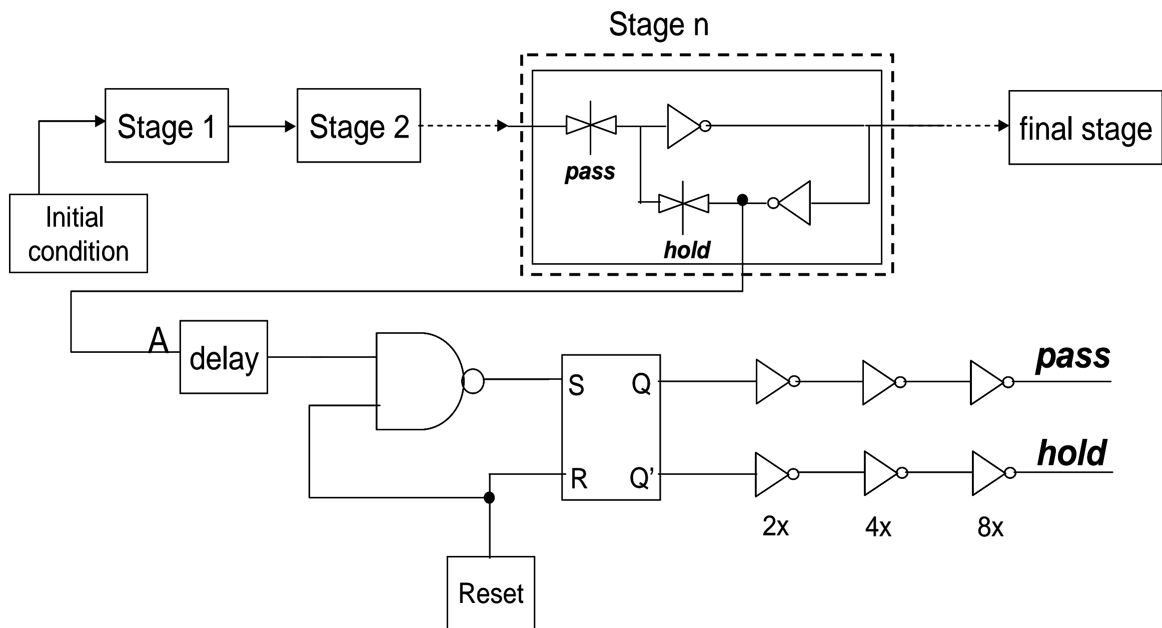

Fig. 7. Test structure showing individual stages along with the trigger/reset circuit. Highlighted region shows the internal circuit of individual stages

CHAPTER IV

SIMULATION RESULTS

Simulations were carried out for the 1.5 μm AMI technology using the Cadence Spectre® simulator [21]. The Spectre® circuit simulator is a modern circuit simulator that uses direct methods to simulate analog and digital circuits at the differential equation level. The basic capabilities of the Spectre® circuit simulator are similar in function and application to SPICE.

The designs were also simulated in three other technologies, namely the HP 0.6-μm, TSMC 0.3-μm and IBM 0.13-μm technologies. These results indicate how the measurement granularity scales with technology and are discussed in section VI.

As stated earlier, the width of the transistors were scaled to obtain equal rise and fall times. Since the mobility of holes is less than the mobility of electrons by a factor of about 3, the PMOS transistor width needs to be scaled by a factor of 3 to obtain equal rise and fall times for an inverter. Since the rise and fall times depend on the resistance of the path to V_{dd} or ground, the scaling factor will be different for different gates and will depend on the number of series-connected transistors. The widths and lengths for the different gates used in the 1.5-μm technology circuit are listed in table 1.

During simulation and experimentation, the input to the first inverter in the chain was held low, setting the outputs of odd stages high and even stages low. The 3rd stage was used to obtain the trigger signal for the 1.5 μm technology. This trigger signal was fed to the SR flip flop (SRFF).

Table 1. Width and lengths of transistors used for the 1.5-μm technology design

Gate	Transistor Type	Length (μm)	Width (μm)
Inverter	NMOS	1.6	3.2
	PMOS	1.6	9.6
Pass-gate	NMOS	1.6	3.2
	PMOS	1.6	3.2
NAND	NMOS	1.6	6.4
	PMOS	1.6	9.6

An SEE circuit simulation only requires charge to be moved between two nodes to model the charge collection event [22]. A time-dependent current source is used to model this single event-induced charge collection. To simulate a strike on the NMOS transistor (n-hit), this current source is placed between the concerned node and ground as shown in Fig. 8. In the case of a p-hit, the current source is placed between V_{dd} and the concerned

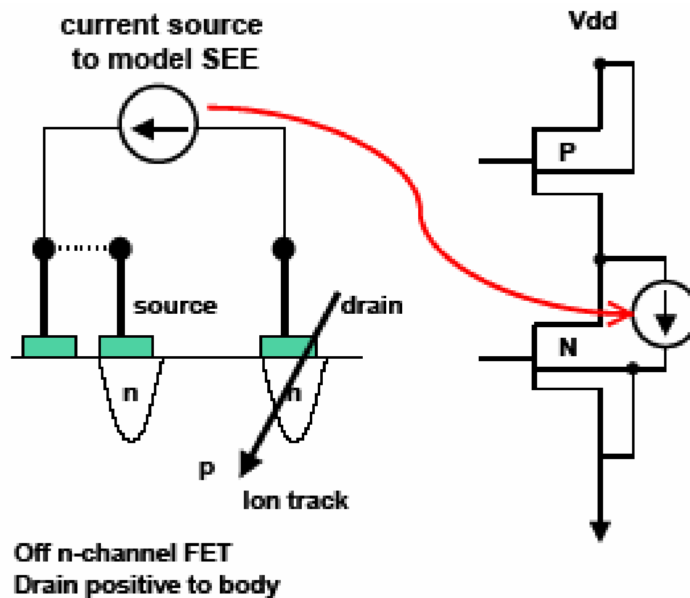

Fig. 8. Modeling a single event using current sources (after [22])

node.

The element used in the simulator to model this is a double exponential current source similar to the one proposed by Messenger [23]. Messenger developed a model for the single event generated current pulse as a double exponential given by:

$$I(t) = I_o[e^{-\alpha t} - e^{-\beta t}] \quad (1.2)$$

where α is the time constant of charge collection from the funnel region and β is the time constant for the initial formation of the funnel region [23]. This type of the SE current pulse is shown in Fig. 9 [22]. The double exponential current pulse that was used has a rise time of about 10 ps and a fall time of about 1 ns [23]. The total charge deposited will be the area under the curve. Thus the amplitude of this pulse is varied to deposit different amounts of charge.

When a strike occurs in any of the stages prior to the nth stage, it generates an SET pulse that propagates through the inverter chain and triggers the SR flip flop to change its

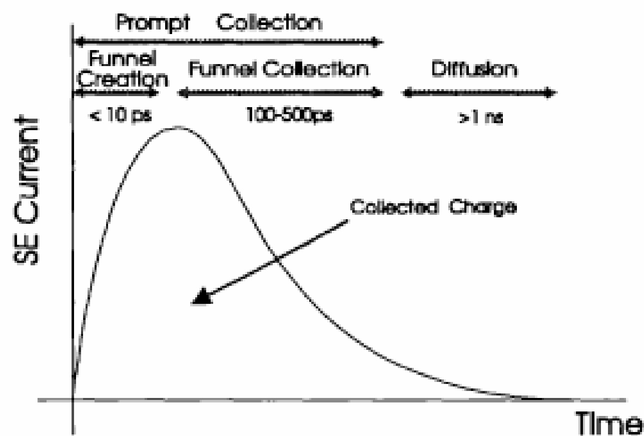

Fig. 9. Typical shape of a single event charge collection current at a junction (after [23])

state. The control signals for passgates will change states after a delay caused by the latching delay of the SRFF and the delay of the buffer stages that follow. As stated earlier, the leading edge of the SET pulse may have gone beyond the nth stage depending on this delay. As a result, additional inverters (and associated latches) beyond the nth stage are also required.

An SET timing analysis was performed for the 1.5 µm technology. Simulation results showed that the delay of an individual inverter and pass-gate stage for the 1.5 µm technology was approximately 900 ps. Since the SET pulse width is measured in units of individual stage delays, this allowed the circuit to characterize the SET pulse width in increments of 900 ps up to a maximum value of 4.5 ns (5 stages). As stated earlier, the measurements will be accurate to within ± half the individual stage delay, which would be ±450 ps for the 1.5 µm technology.

To reduce the number of I/O pins, a data shift register was designed to read the outputs of the latches serially. Fig. 10 shows the simulation results for the output of the data shift register prior to and after an SET. A double-exponential current source was used to inject charge at the output of the 1st stage. As stated earlier, the amount of charge collected, and thus the width of the SET pulse generated, is varied by modulating the amplitude of this current source. Even though the trigger pulse was taken from the 3rd stage, the delay associated with the SRFF and the buffers allowed the SET pulse to propagate to the 5th stage before the *hold* signal could freeze the latches and capture the SET pulse. Fig. 10(a) shows the clock signal used to output the latch data serially. Fig. 10(b) shows the write control signal to the data shift register. When this signal goes low, the current state of every stage in the pulse capture circuit gets stored in the data shift register and when this

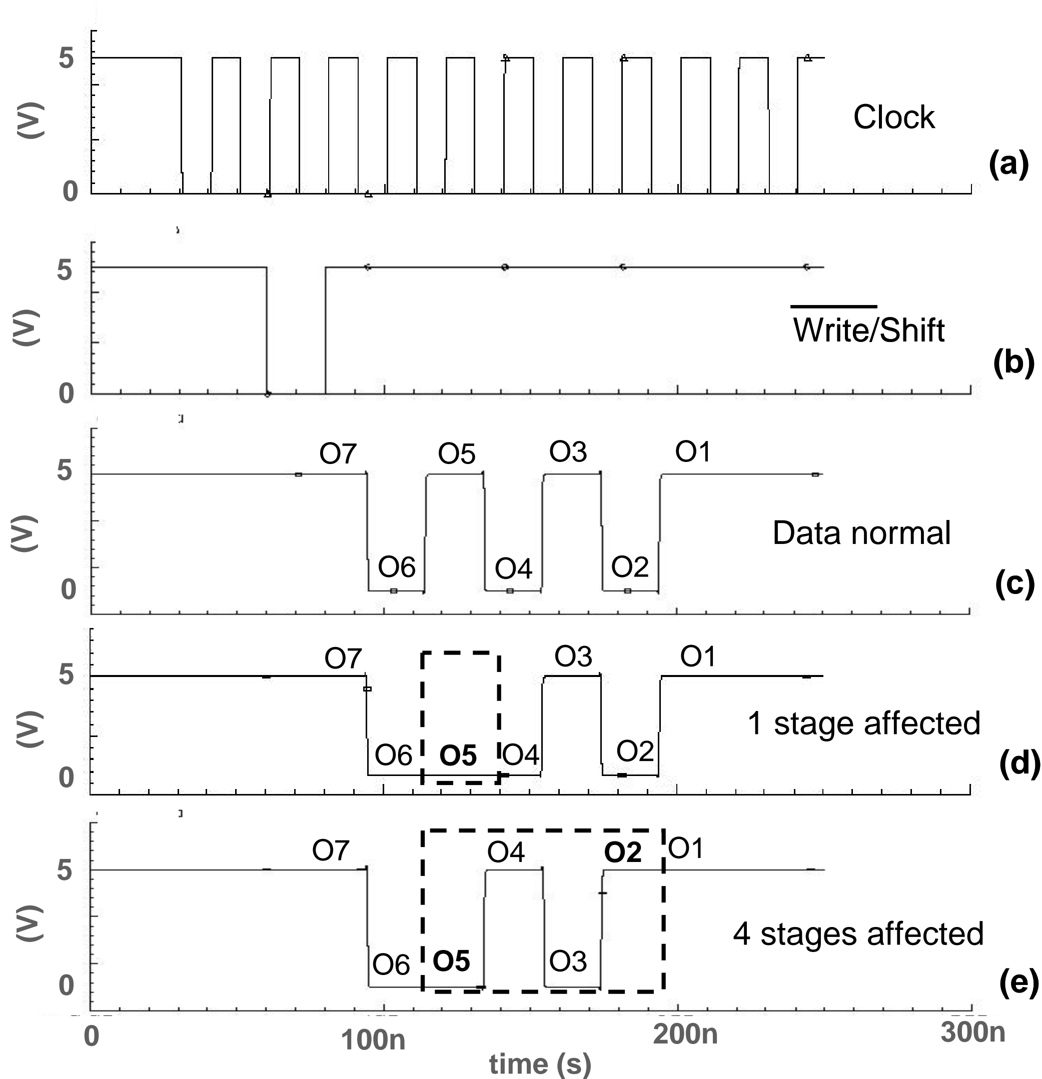

Fig. 10. Waveforms showing (a) clock to the data shift register, (b) Write/Shift control signal to the data shift register, (c) output of data shift register prior to a SET strike, (d) output with a 1.2 ns SET pulse indicating that 1 stage has a switched state and (e) output with a 3.85 ns SET pulse indicating that 4 stages have switched states

signal is high the data are serially shifted out. Fig. 10(c) shows the serial latch data in the absence of an SET pulse. Fig. 10(d) shows the latch data when the actual SET pulse was 1.2 ns. In this case, only the 5th stage is affected by the presence of the SET as evidenced by inverted values compared to Fig. 10(c). Fig. 10(e) shows the latch data for a larger SET pulse. The actual pulse width in this case was measured to be 3.85 ns. As can be

seen, the number of stages affected by the SET is four (2nd through 5th). Thus for the first case (short pulse) the pulse width is estimated to be the delay of a single stage (900 · 1 = 900 ps) ± 450 ps. For the second case in which four latches have switched states, the pulse width is estimated to lie between 3.15 ns to 4.05 ns (i.e., 3.6 ns ±450 ps).

The amplitude of the current pulse used, the charge deposited and the estimated pulse width values for different cases are summarized in Table 2. The effective LET values corresponding to the deposited charge, computed using equation 1.1, are also included in the table. These LET values are high and correspond to ions with a comparatively low flux. Still these values are reasonable for a 1.5-μm technology for which the charge deposited needs to be quite high (due to large capacitances and higher operating voltages) in order to cause SETs. Fig. 11 shows the estimated pulse width as a function of the charge deposited. The error bars on the pulse width give us an idea of the probable range for the actual pulse width. The percentage error in the estimation decreases with increasing pulse width.

Table 2. Amplitude of current pulse, charge deposited, estimated pulse width and the corresponding LET values for the 1.5-μm technology circuit

Amplitude (mA)	**Charge deposited Qc (pC)**	**Estimated PW (ps)**	**Effective LET ($MeV/cm^2/mg$)**
1.75	2.446	900	74.12
1.9	2.657	1800	80.51
2.6	3.638	2700	110.24
5	7	3600	212.12

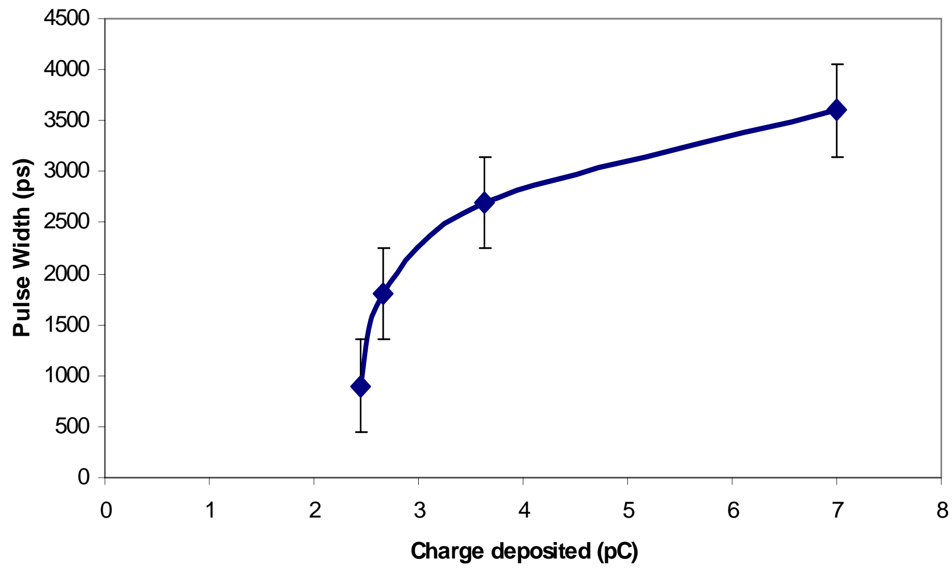

Fig. 11. Simulation results for pulse width as a function of charge deposited for the 1.5-µm technology circuit

CHAPTER V

PULSED LASER TESTING AND EXPERIMENTAL RESULTS

To provide a proof of concept, a test chip was designed using the Cadence® Virtuoso® layout tool, fabricated and tested. Details about the layout are given in appendix I. AMI 1.5 µm technology was used for the design of the test chip. Test chips were fabricated through MOSIS (www.mosis.org). Experimental results from the 1.5 µm test chip are included here to demonstrate the validity of the approach.

Fig. 12 shows a die photograph of the 1.5 µm technology test chip, indicating the 2nd stage that was hit by the laser pulses during the experiments. Laser tests were performed on these test chips at the Naval Research Lab. A good correlation between ion and laser data for the collected charge has been reported [25] validating use of laser tests to estimate the single-event sensitivity of devices.

Pulsed Laser Testing

Pulsed-laser testing is a fairly simple technique in which a short pulse of laser light is focused with a microscope objective lens to a ~1-µm-diameter spot [24, 25]. The properties of the pulsed laser are important in determining the characteristics of the SETs that are generated. The duration of the pulse must be on the order of a few picoseconds, which is longer than the time it takes for an energetic particle to generate charge, but shorter than the response time of most circuits, so that the differences between charge deposition by energetic particles and laser light are minimized. The wavelength of the

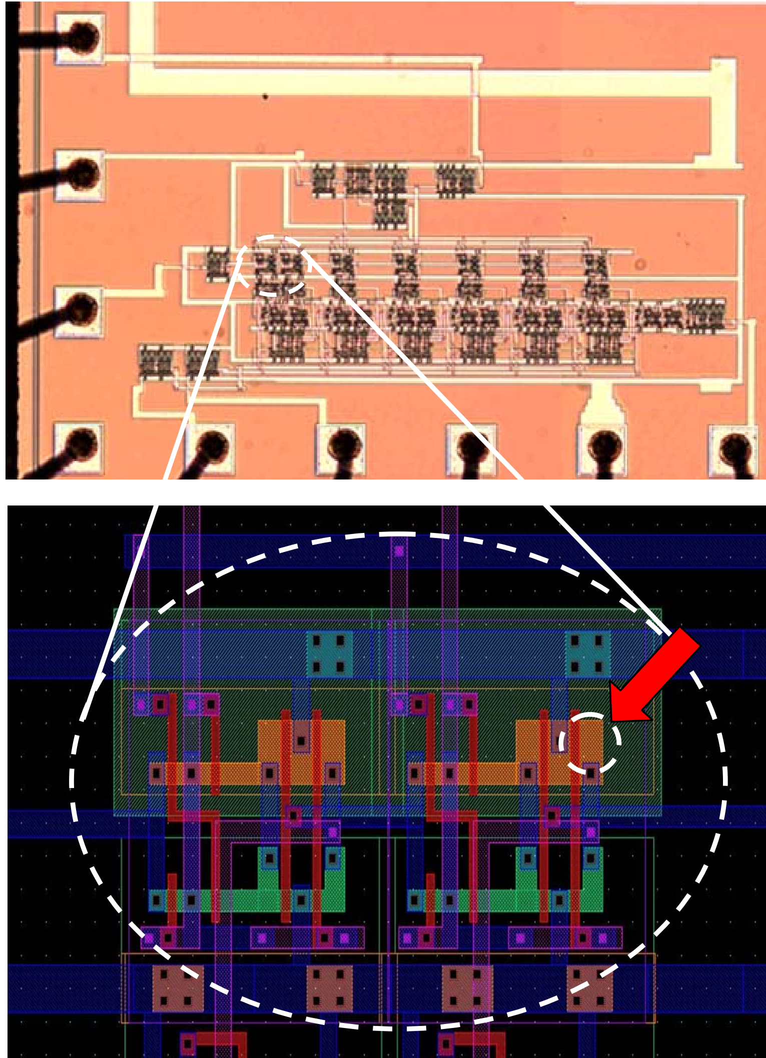

Fig. 12. (a) Die photo of 1.5um technology test chip. (b) Zoom-in picture indicating the strike location on the layout

laser determines its penetration depth into the semiconductor and also the size of the focused spot. In order to generate charge, the photon energy must be greater than the bandgap energy of the semiconductor.

The laser intensity decreases exponentially with distance as it propagates into the semiconductor [2]. Greater absorption and smaller skin depth are obtained with greater photon energy. For example, for simulating the effects of an energetic heavy ion, laser

light with a wavelength of 800 nm, which has a skin depth of about 15 mm in silicon, is commonly used [2]. Though the profile of the charge track generated by the laser may be different from that of the heavy ion, the resulting voltage transients have been found to be similar [2].

Fig. 13 shows the layout of the equipment used in pulsed laser testing [24]. The spot is positioned on a sensitive node in the circuit and the pulse energy is increased until a

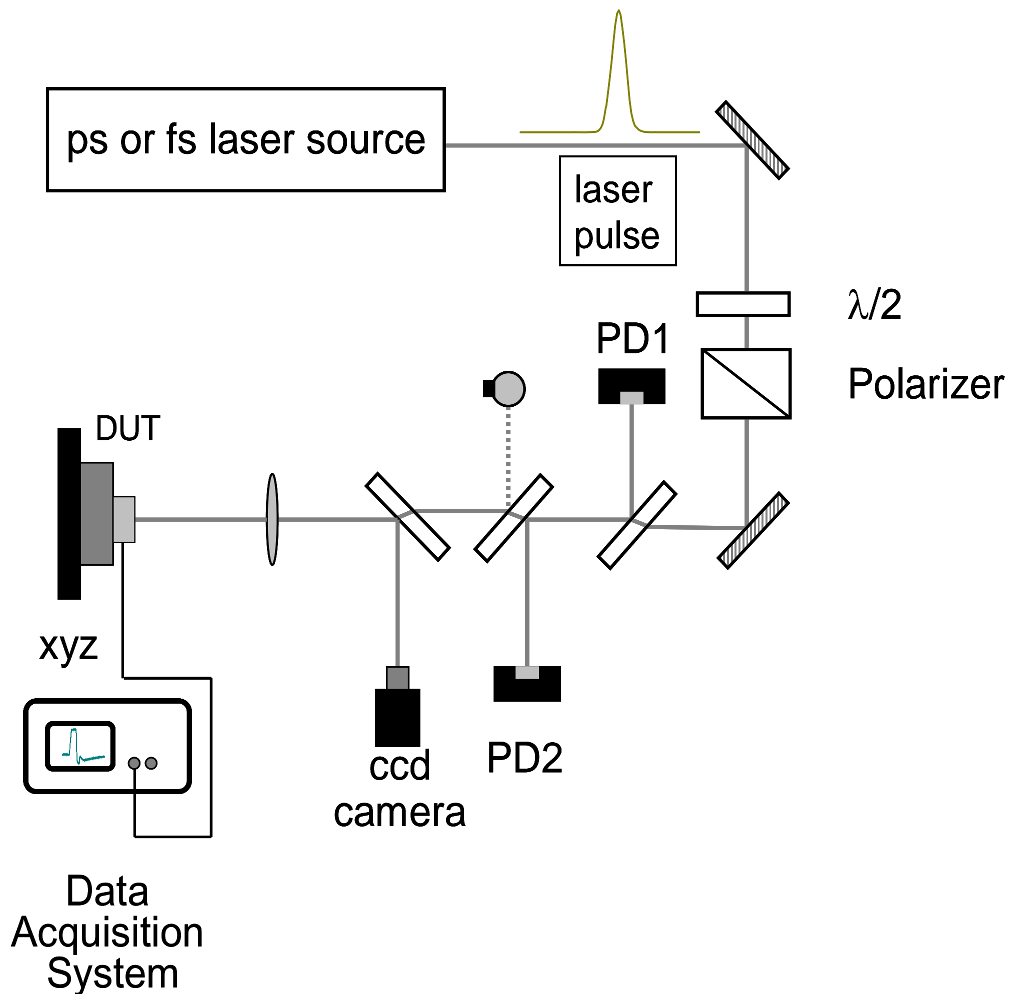

Fig. 13. Schematic of a pulsed laser test system [24]

single event occurs. The number of pulses per second can be varied from single shot to megahertz frequencies.

A portion of the beam is directed at a detector to measure the energy of each pulse at a sufficiently slow repetition rate. Neutral density filters and a polarizer are used to attenuate the pulse energy to the required value needed to produce an upset.

The light is focused to a spot with a microscope objective lens with a magnification of 100× and working distance of 3 mm. The spot size is less than a micrometer at a wavelength of 850 nm. The device is mounted on an *XY* stage that has a minimum step size of 0.1 µm. The *X* and *Y* coordinates for each location can be given relative to a fixed mark on the chip for locating sensitive nodes in complex circuits. To view the beam and the chip simultaneously, a beam splitter is inserted in the beam and the reflected light is detected with a CCD camera and monitor.

Experimental Results

In the laser tests, the collected charge can be varied as a function of the laser energy. By increasing the collected charge, the pulse width generated is also increased. For our experiments, the laser beam intensity was varied from 85 pJ to 179 pJ to deposit different amounts of charge. The lower limit of 85 pJ was the minimum energy at which at least 1 stage had a switched state. Similarly at the upper limit of 179 pJ, all stages had switched states. Based on [25], the effective LET values corresponding to these laser energies were computed to be greater than 90 MeV/cm^2/mg. Since this test chip was designed using an old technology, such high LET values were anticipated.

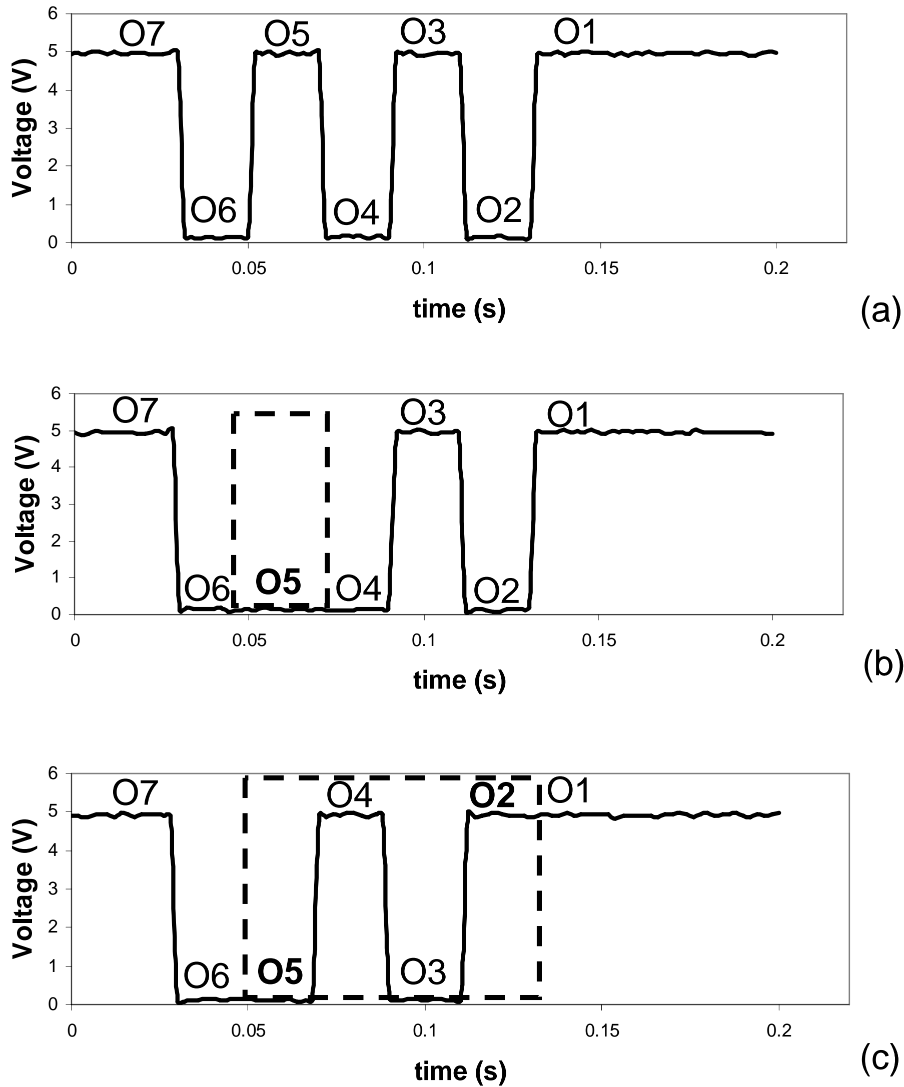

Fig. 14. Waveforms showing (a) output of data shift register prior to a laser strike, (b) with 85.1 pJ of laser and (c) with 179 pJ of laser strikes. With a lower laser energy 1 stage has a switched state, while for the higher laser energy 4 stages have switched states (outlined regions)

Fig. 14 shows the experimental results of the output of the data shift register prior to and after laser strikes with different energies [26]. These results match very well with the simulated results shown in Fig. 10. For the experimental results shown here, the second inverter in the series was struck with the laser. The SET pulse propagated until the trigger

signal caused the latches to ‘hold’ their states. For a laser pulse with about 85 pJ of energy, only 1 stage had switched its state (stage 5) as seen in Fig. 14(b). This corresponds to an SET width that lies between 450 ps and 1350ps (900 ps ± 450 ps). As the hit node has fully recovered in this case, the pulse width captured is the actual pulse width. As the laser pulse energy increased, the number of switched states also increased. When the laser pulse energy reached 179 pJ, four stages switched states, as shown in Fig. 14(c). However, in this case, the hit node has still not recovered. Thus, this result provides a lower limit of the actual pulse width. Laser energies in between these two energy levels (85 pJ and 179 pJ) would have resulted in one, two, or three stages being affected, indicating that the hit node had recovered fully. A misfire in the reset signal was found to be responsible for not being able to capture all the different waveforms. With better test board design this error can easily be avoided in future tests. The pulse widths measured when the hit node has recovered show the actual pulse width that one will see in a real circuit. As the maximum number of stages that can switch was limited to four for this design, all laser energies above 179 pJ still resulted in four stages being switched, as expected. These results provide a proof of concept that such on-chip characterization circuits can be used effectively to determine SET pulse widths. However, the granularity associated with the relatively long inverter delay of this older technology limits the resolution. Simulation results show that the resolution increases with decreasing feature size, as demonstrated in the next chapter.

CHAPTER VI

EXTENSION TO ADVANCED TECHNOLOGIES

Designs and simulations were also carried out for the HP 0.6-µm, TSMC 0.3-µm and IBM 0.13-µm technologies. For each of these technologies, the basic design was kept the same with appropriate device models and device sizes used for each simulation. The device models were obtained from mosis (www.mosis.org) for the respective technologies. As expected, the delay for individual stages decreased as the minimum feature size decreased. As the minimum pulse width that can be captured is directly related to the minimum logic gate delay, advanced technologies showed better resolution. Fig. 15 shows how the minimum pulse width, and the related measurement resolution,

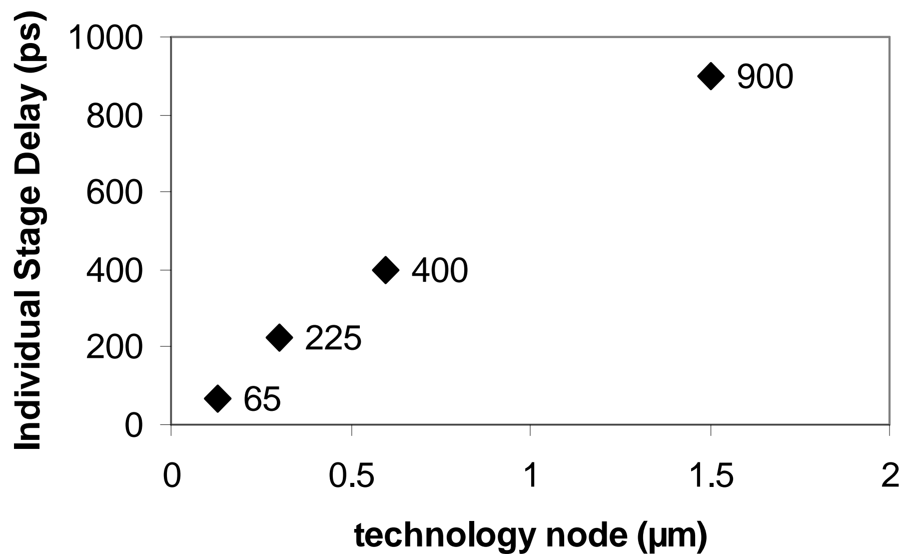

Fig. 15. Individual stage delay as a function of the technology

scales with technology. For the 1.5 μm technology, the resolution of the pulse width measurement was 900 ps. This decreased to 400 ps for 600 nm, 225 ps for 300 nm, and 65 ps for 130 nm technologies. Detailed simulation results for the 130 nm technology are discussed below. All other technologies showed similar results.

As mentioned earlier, the transistors were scaled to obtain equal rise and fall times. The widths and lengths for the different gates used in the 0.13-μm technology circuit are listed in Table 3. Simulation results showed that the delay of an individual inverter was 25 ps. However, when this inverter output was loaded with other required elements (pass-gate and another inverter for latching), the minimum delay increased to approximately 65 ps. A total of 18 stages were used for the 0.13 μm technology.

Table 3. Width and lengths of transistors used for the 0.13-μm technology design

Gate	**Transistor Type**	**Length (μm)**	**Width (μm)**
Inverter	NMOS	0.12	0.24
	PMOS	0.12	0.72
Pass-gate	NMOS	0.12	0.24
	PMOS	0.12	0.24
NAND	NMOS	0.12	0.48
	PMOS	0.12	0.72

Fig. 16 shows the simulation results for the output of the data shift register prior to and after an SET. A double-exponential current source was used to inject charge at the output of the 2nd stage. The trigger signal was taken from the 11th stage. Fig. 16(a) shows the

clock signal used to take out the latch data serially. Fig. 16(b) shows the serial latch data in the absence of an SET pulse. Fig. 16(c) shows the latch data when the SET pulse is small. In this case, the 13th and 14th stages are affected by the presence of the SET, as evidenced by inverted values compared to Fig. 16(b). Fig. 16(d) shows the latch data for

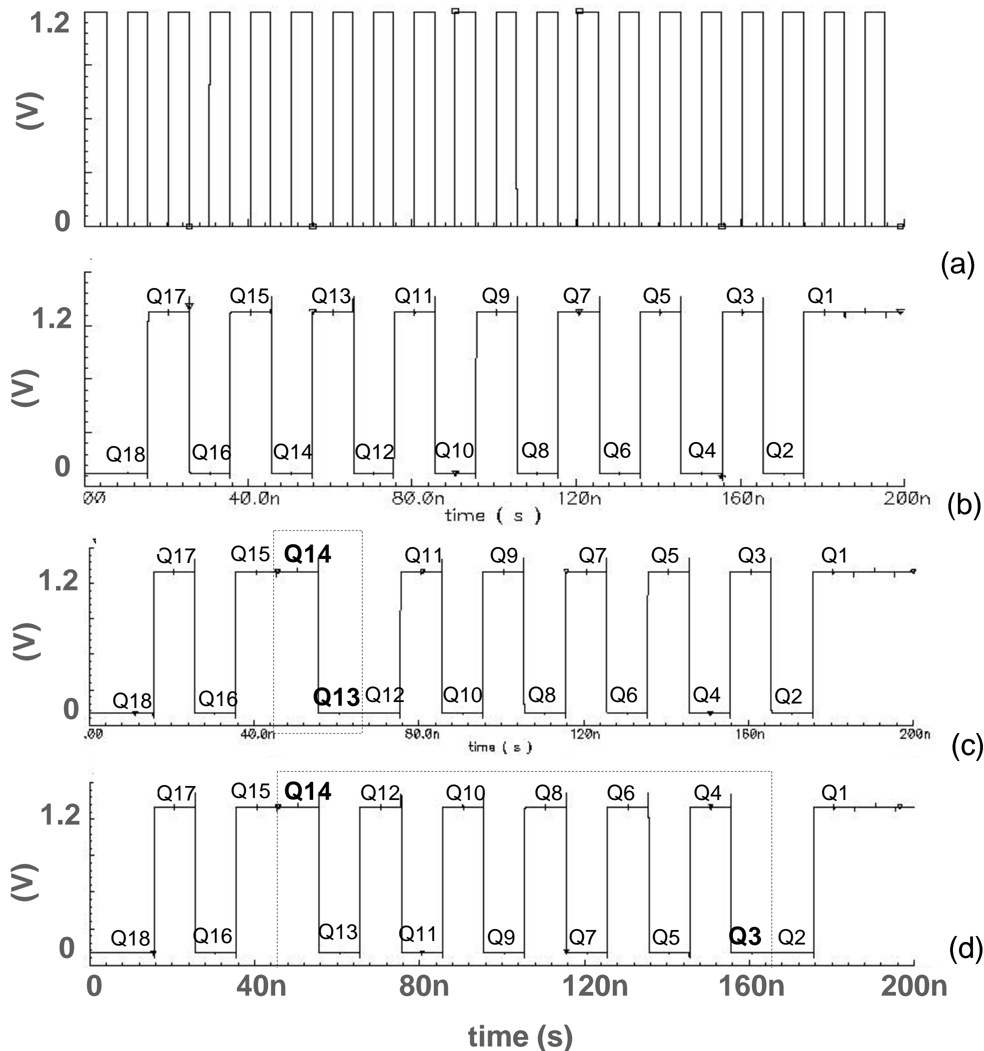

Fig. 16. Waveforms showing (a) clock to data shift register, (b) output of data shift register without any SET, (c) output with a short SET & (d) output with a wide SET. For the short SET two stages have switched states and for the wide pulse 12 stages have switched states (outlined regions)

a large SET pulse. As can be seen, the number of stages affected by the SET is twelve (3rd through 14th). Thus for the first case (short pulse) the pulse width is estimated to be twice the delay of each stage (65 × 2 = 130 ps) ± 32.5 ps. For the second case in which 12 latches have switched states, the SET pulse width is estimated to fall between 747.5 ps to 812.5 ps (65 × 12 = 780 ps ± 32.5 ps). The voltage pulses created by the current sources were plotted using the simulator and their pulse widths were measured directly to be 160 ps and 770 ps, respectively. Note that for both the simulated pulses, the hit node recovered fully before the latching of the SET pulse, thereby ensuring that the actual pulse width is captured. These simulations were carried out with a small delay in the trigger signal for ease of simulations, resulting in the presence of the SET pulse on either side of the trigger stage. In the design that would be used for heavy ion tests, one would have a longer delay in the trigger stage to ensure that the entire SET pulse has traveled beyond the trigger stage and correspondingly increase the number of stages.

The amplitude of the current pulse used, the charge deposited and the estimated pulse width values for different cases are summarized in table 4. The corresponding LET values are also given in table 4. Fig. 17 shows the estimated pulse width as a function of the charge deposited along with the error bars. Comparing this plot with the plot for the 1.5-μm technology gives us an indication of how the measurement resolution and accuracy improve with technology.

Table 4. Amplitude of current pulse, charge deposited, estimated pulse width and the corresponding LET values for the 0.13-µm circuit

Current pulse Amplitude (mA)	Deposited Charge Qc (pC)	Estimated PW (ps)	Effective LET (Mev/cm^2/mg)
0.225	0.05166	195	4.696364
0.25	0.0571	260	5.190909
0.275	0.06317	325	5.742727
0.3	0.06892	390	6.265455
0.4	0.0907	455	8.245455
0.5	0.1149	520	10.44545
0.7	0.1609	585	14.62727
0.9	0.207	650	18.81818
1.2	0.276	715	25.09091
2	0.46	780	41.81818

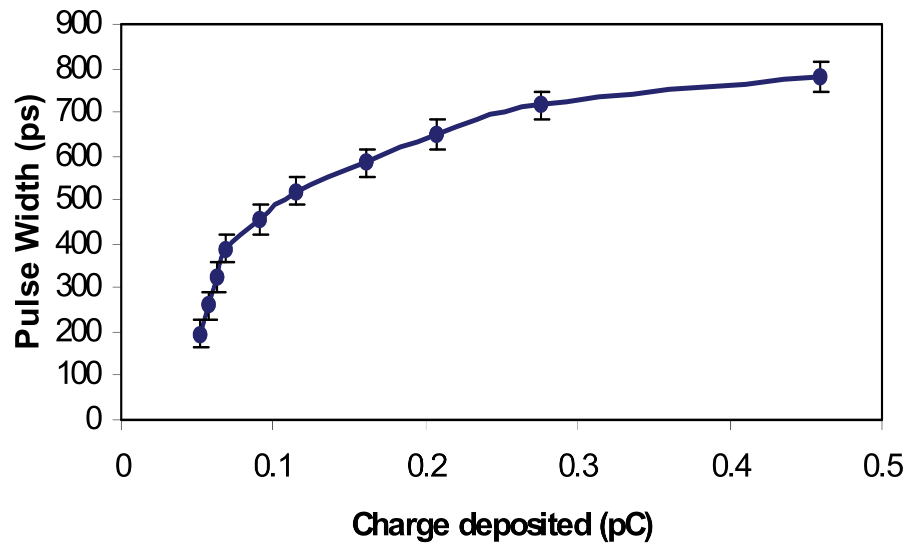

Fig. 17. Simulation results for pulse width as a function of charge deposited for the 0.13-µm technology circuit

CHAPTER VII

CONCLUSION

This thesis describes the development of a new self-triggered test structure for measuring SET pulse width in increments of one inverter delay. Simulation results from four different technologies and experimental results on test chips fabricated in a 1.5 µm technology validate the use of this method to characterize transient pulse widths. Simulation results show measurement resolution of 900 ps for a 1.5 µm technology and this scaled to 65 ps for 0.13 µm technology. Experimental pulse-width measurements from the 1.5 µm test chip indicate pulse width varying from 900 ps to over 3 ns as the laser energy at the strike location is increased from 85 pJ to 179 pJ. Longer inverter chains would permit the capture of even longer pulse width, while decreasing feature sizes (and inverter propagation delays) would improve the resolution of this technique even further.

With ever decreasing feature sizes, sensitivity to SETs will continue to increase. Even for current technologies, SETs have started to dominate error rates. SETs caused due to terrestrial neutrons are being increasingly observed in commercial electronics indicating that they are not limited only to electronics in space. Since the width of the SET determines the probability of it getting latched, knowledge of SET pulse width is important in determining and mitigating single event transients. Circuit hardening techniques can be implemented successfully only if one knows the range of transients to expect. The circuit technique described here can be implemented to determine the SET

pulse width for any technology and will continue to yield better resolution as technology advances.

APPENDIX A

LAYOUT DETAILS

Five basic steps are involved in the creation of an IC test chip. The first is to draw up a functional specification. The next step is to build a schematic based on the functional specification using a schematic editor. Such a schematic is then simulated (using simulators like SPICE, Spectre®, etc) to verify the correctness of the design. The next major task is to translate this design into a two-dimensional language of silicon – called the layout (using layout editors such as Virtuoso®). The layout is then sent to a silicon foundry for fabrication. Finally, the fabricated ICs are tested to make sure they meet the functional specifications. This appendix deals with the layout details of the test chip. More detailed information about VLSI design can be found in [27].

The layout of this test chip was obtained using Cadence Virtuoso® Layout Editor. Virtuoso® is the industry-standard base-level custom physical layout tool that supports the implementation of custom digital, mixed-signal, and analog designs at the device, cell, and block levels.

The first step in the layout is to start with the basic cells in the design. Individual cells were designed starting with the inverter. The usual practice is to have a fixed cell height for all layouts with the power rails (vdd and gnd) at the top and bottom of the cell. This approach enables easy placement of different cells together. The layouts need to adhere to certain specifications called the design rules. Design rules specify certain geometric constraints like the minimum distance between layers in the layout. Design rule check

(DRC) is performed for each individual design and any violations are immediately corrected. The next step is to check the layout of each cell with its schematic to verify the correctness of the functional behavior of the layout. Layout versus schematic (LVS) is a built-in tool in Virtuoso that performs this comparison.

Once the individual layouts are completed, the next step is to use these individual blocks to build the complete design. Automatic place and route tools help to build the complete design using the individual blocks. Since the design of this test chip was simple, automatic place and route tools were not used and the design was custom made. Based on the design, different cells are stacked one beside another and in rows. The number of cells in a row and the number of rows are chosen based on the shape and area available on the test chip. Power rails run horizontally through all the cells and are usually made using metal layer 1. Input/output connections between the cells are made using a combination of different metal layers.

The main building block of the design of this thesis work is shown in Fig. 18. Fig. 18(a) shows the schematic and Fig. 18(b) shows its corresponding layout.

Once the design is completed, it is placed inside a ring of pads. Pads connect the input, output and power pins in the design to the external pins. Thus based on its function the design of the pad differs. The complete pad structure with the different types of pads can be downloaded from mosis website (www.mosis.org). The connections from the design to the respective pads are then completed.

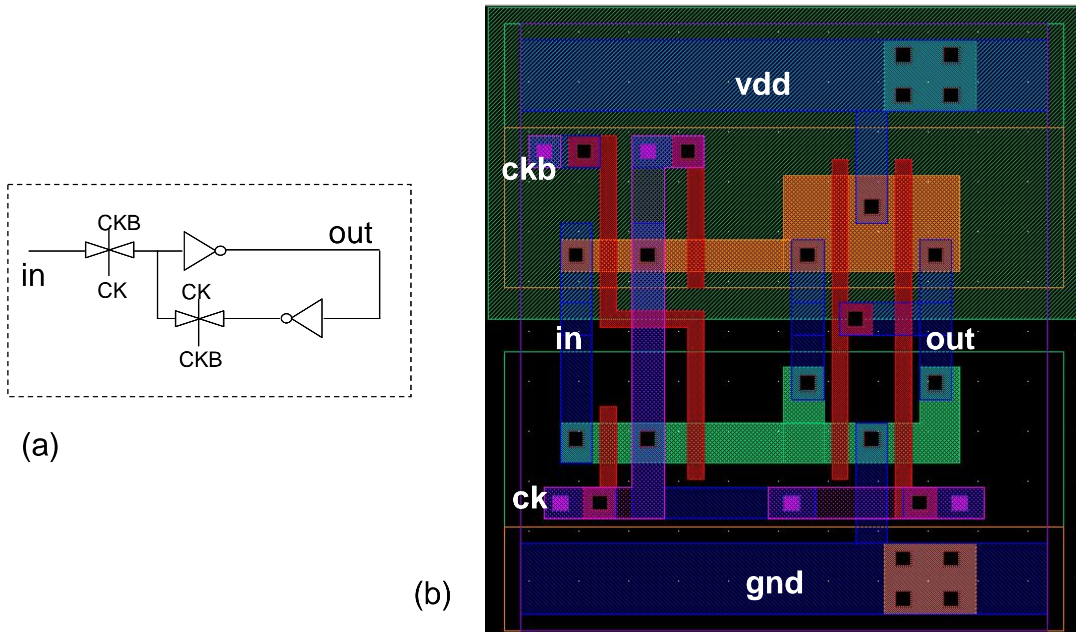

Fig. 18 (a). Latch schematic and (b) its corresponding layout

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