CHARGE TRAPPING PROPERTIES OF ALTERNATIVE HIGH-K DIELECTRICS IN MOS DEVICES

By

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CHAPTER I

INTRODUCTION

Bias temperature instability (BTI) is a degradation phenomenon that occurs mainly in MOS devices and integrated circuits (ICs) [1]-[4]. This instability is seen as an increase both in interface-trap density and oxide trapped charge density when bias is applied on the gate at elevated temperature and/or for long times [2], [5], which causes shifts in threshold voltage and a decrease in carrier mobility. The degradation of these device parameters can lead to circuit failures, both for analog and digital applications [2], [6]-[7]. BTI was not typically a reliability limiting mechanism for older generation technologies where circuits were designed to survive large threshold voltage shifts and mobility degradation levels. However, for modern MOS devices with ultrathin oxides operating at low voltages, where even small voltage shifts can jeopardize circuit performance and influence the long-term reliability, BTI becomes a major reliability issue [8].

For devices used in space systems, radiation exposure is another reliability problem. Electronics are exposed to various forms of radiation, such as electrons, protons, neutrons, and heavy ions. Total ionizing dose irradiation causes the buildup of oxide and interface trap charge. A lot of work has been done in the radiation effects community to investigate changes in MOS threshold voltage shifts after irradiation [9]. However, up till now, not much work has been devoted to studying the combined effects of irradiation and BTI on the degradation and long-term reliability of MOS devices. These combined effects are addressed in this dissertation.

Another challenging problem for modern complementary metal oxide semiconductor (CMOS) technology comes from the materials prospective. For the past 40 years, device size has decreased and device performance has increased greatly due to size scaling associated with "Moore's Law" [10]-[11]. However, modern CMOS devices are rapidly approaching the intrinsic physical scaling limit for Si/SiO_2. Devices with ultrathin oxides operate at rather large electric fields because the device operation voltage cannot be scaled more aggressively than the device dimensions. For example, devices with oxides thinner than ~4-5 nm exhibit large off-state leakage currents (1 to 10 A/cm^2) since carriers can easily tunnel directly between the substrate and gate electrode [12]-[13]. This is a big concern for satellite systems and ground-based mobile electronics where power conservation is important. To reconcile the need for reduced off-state leakage currents in highly scaled devices, IC manufacturers are considering several high-κ gate dielectrics to replace SiO_2 in the future devices [12]-[16]. The main advantage of alternative high-κ dielectrics is they can have higher dielectric constants which make it possible to manufacture a gate stack that is physically thicker than SiO_2, but which maintains electrostatically similar performance to ultrathin SiO_2 layers. The increased physical thickness significantly reduces the probability of tunnelling across the insulator, and therefore reduces the amount of off-state leakage current [15].

The high-κ materials being currently investigated for integration into future IC technologies include Al_2O_3, HfO_2, ZrO_2, Y_2O_3, TiO_2, and Ta_2O_5 and/or the silicates and aluminates of some of these materials [14]-[24]. The dielectric constant ($\varepsilon_{high\text{-}\kappa}$) is in the range of 10-40, approximately 3-10 times higher than that of SiO_2 ($\varepsilon_{SiO_2} = 3.9$) [15]. However, some of them have narrow bandgaps, which will lower the barrier height for tunnelling. Since leakage current increases exponentially with decreasing

film thickness and barrier height [25]-[26], this trade-off between dielectric constant and barrier height will determine the relative advantages that an alternative dielectric offers in terms of reduced leakage current. Initial data in the literature show that the net effect for high-κ materials is a reduced leakage current; some high-κ gate dielectrics exhibit up to ~5 orders of magnitude less leakage current than electrically equivalent SiO_2 [18], [27]-[28].

The Group IV metal oxide HfO_2 has been studied extensively for future commercial and space electronics [12], [15], [19], [21], [29]-[30] due to its high dielectric constant (~22) [31]-[32], relatively wide bandgap (~5.6 eV), sufficient band offset (> 1.4eV) [33], and thermal compatibility with Si-based processing [34]-[35]. Al_2O_3 is another promising candidate for its large conduction band offset [36] and good compatibility with high temperature CMOS processing [14]. Also, prior work found that Al_2O_3 exhibited good total-dose radiation hardness because it has a significant density of electron traps [37]-[38] to compensate the effects of radiation-induced trapped holes.

Many high-κ gate dielectrics have shown encouraging electrical characteristics as described above; however, it is difficult to establish a high quality direct interface between high-κ materials and the Si substrate. To improve the interface quality, an interfacial layer (usually oxide or oxynitride) typically is introduced [39]. The benefit of the interfacial layer is to take advantage of the natural Si-SiO_2 interface while also incorporating high-κ dielectrics to increase the capacitance and thickness and thereby reduce the direct tunnelling probability. Plus, most high-κ materials are not good oxygen diffusion barriers [16], [40]-[41]. The presence of an interfacial layer can avoid silicon oxidation to some extent and help the devices survive the standard integrated circuit fabrication process flow. Nitrogen atoms usually are introduced into

the interfacial layer to give better control of the gate leakage current, modify the interface properties, and to avoid dopant diffusion from the gate into the channel [40], [42]. Thermal annealing is a common practical nitridation process. Excess nitrogen also can provide an additional trapping site in the near-interfacial SiO_2, inhibit the motion of hydrogen, and decrease the energy barrier for some kinds of critical defect formation reactions. These can enhance charge trapping in the near-interface dielectric, to a degree determined by the concentration and distribution of nitrogen in the gate stack [5], [8].

In order to maintain a high capacitance, the thickness of the interfacial layer should be minimized since its dielectric constant (around 4-7, depending on nitrogen concentration) is less than that of the high-κ dielectrics [43]. However, the breakdown strength is also limited by the interfacial layer. For a given gate bias and assuming an initially charge free dielectric interface, D (= εE) is continuous across the interface:

$$\varepsilon_1 E_1 = \varepsilon_2 E_2 \qquad (1)$$

Here ε_1 and ε_2 are the dielectric constants of the interfacial layer and high-κ dielectric layer, respectively, and E_1 and E_2 are the electric fields of each layer. $\varepsilon_1 < \varepsilon_2$, so $E_1 > E_2$. Therefore, electrical breakdown may occur first in the interfacial layer of a typical gate stack, when a large gate voltage is applied. The thickness of the interfacial layer ultimately limits the operation voltage for the device. Interface engineers therefore need to balance between low equivalent-oxide-thickness (EOT) and high breakdown strength when integrating interfacial layers into standard commercial IC processing.

Other concerns for high-κ dielectrics include several orders of magnitude more traps found in the bulk or interface and significantly lower mobility compared with thermal SiO_2 gate devices. The probability of bias-induced charge trapping in high-κ

gate stacks is extremely high due to the large densities of "intrinsic" defects in the materials that are now available [13], [32], [39]. The charging and discharging of these traps can greatly influence the performance of the devices [44]; these can reduce the drive current due to electrostatic interaction with trapped charges, and cause threshold voltage instabilities over device operation time.

Qualification of high-κ devices for space applications may need more understanding of the charge trapping characteristics and long-term reliability of these materials. In this study, bias-temperature instabilities, radiation response, and annealing characteristics of high-κ materials (mainly HfO_2 or Al_2O_3/oxynitride gate dielectrics) were evaluated. A detailed study of the effects of switched-bias annealing on these same kinds of MOS devices following X-ray irradiation or high-field stress was reported as well. The contributions of oxide, interface, and border-trap charge are evaluated. Physical models of charge buildup and annealing are developed to account for the results. These results can provide insight into the fundamental charge trapping properties of high-κ dielectrics and help to predict the long-term radiation response and reliability of these devices. Hardness assurance implications are also discussed based on the worst-case response of devices in a combined radiation and BTS environment.

This dissertation is organized as follows. Chapter II introduces the basic concepts of different radiation-induced defects and reviews previous work on negative bias temperature stability (NBTI). Chapters III through VII present experimental results and discussion. In particular, chapter III describes experimental details and chapters IV and V present degradation due to negative bias temperature stress and irradiation separately. Then chapter VI summarizes the combined effects of these two.

Further discussion of mechanisms and detailed switched-bias experiments are interpreted in Chapter VII. Chapter VIII concludes the work.

CHAPTER II

BACKGROUND AND LITERATURE REVIEW

This chapter provides background information about radiation-induced defects including oxide, interface and border traps. The techniques used in this research to separate the threshold voltage shifts due to each type of defect are explained in detail. Furthermore, the negative bias temperature instability (NBTI) phenomenon, previous theories and models, and affecting factors are described in sequence.

Total Dose Radiation Effects and Calculation of Defect Densities

The primary effects of total ionizing dose on semiconductor devices include charge accumulation in the oxide and interface trap creation at the Si/oxide interface. Ionizing radiation creates electron-hole pairs (EHPs) in the gate and isolation dielectrics. Some of the radiation-induced charge recombines and does not affect the device performance. The EHPs that survive initial recombination (i.e., the charge yield) will be separated by the oxide electric field, as shown in Fig. 1 [45]. Electrons have a relatively high mobility in SiO_2, so they are swept to the gate in a picosecond or less at typical device operating conditions. However, holes transport slowly toward the Si/SiO_2 interface via defect sites in the oxide [45]. Some of the holes will recombine with the electrons injected from the silicon, and other holes will become trapped in the oxide, forming positive oxide trapped charges. These oxide trapped charges will cause a shift in the threshold voltage and an increase of the leakage current in integrated circuits.

Meanwhile, as holes transport to the interface, protons (hydrogen ions) can be released and react with Si-H bonds at the Si/SiO_2 interface to form interface traps. Those interface traps will lead to a change of threshold voltage and a decrease of carrier mobility, etc.

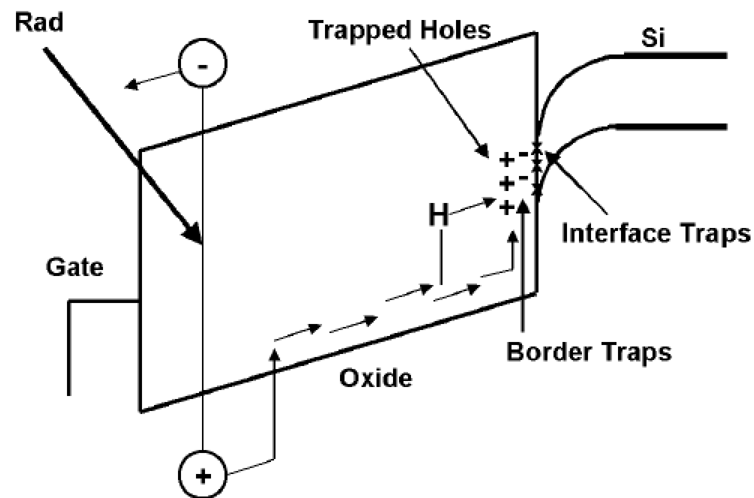


Figure 1 Energy band diagram showing ionizing radiation induced charge generation and trap creation in a metal gated, p-substrate MOS capacitor, which was irradiated under positive gate bias. After [45].

Although Fig. 1 only shows hole trapping in the oxide, most gate dielectrics can also trap a significant density of electrons. Some high-κ films have exhibited more electron trapping than hole trapping after exposure to ionizing radiation [30], [38]. The radiation-induced oxide trapped charge in SiO_2 and alternative dielectrics is generally net positive [12]-[13], [32], [36], [46]-[47].

Calculations of oxide trapped charge densities and interface trap densities typically are based on the assumption that the interface traps are charge neutral when the Fermi level is at midgap [48]-[49]. In this case, the midgap voltage shift (ΔV_{mg}) is due entirely to trapped oxide charge. The oxide trapped charges shifts the C-V

characteristics; however, the interface traps change the slope. For instance, the "stretchout" of a C-V curve is due to interface traps (ΔV_{it}). The interface traps are amphoteric. In the upper half of the silicon band gap (above midgap) they are acceptor-like while in the lower half of the silicon band gap (below midgap) they are donor-like. Interface traps usually make threshold voltage (V_t) more positive in n-channel MOSFETs and more negative in p-channel MOSFETs. Positive oxide-trap charge shifts Vt in the negative direction for both n- and p- channel MOSFETs. [50]. Note that this makes negative bias temperature instability (NBTI) a more serious reliability issue for *p*MOSFETs (on *n*-substrates) since the contributions of both oxide and interface traps to the negative threshold voltage shifts make the devices harder to turn "on". For *n*MOSFETs (on *p*-substrates), there is at least partial offset of the effects of interface and oxide traps on threshold voltage. Unless interface trap densities vary significantly across the bandgap, subthreshold measurements of MOSFETs will provide approximately equivalent information as C-V measurements of capacitors when both of them are used to extract oxide trapped charge and interface trap densities.

The changes in interface trap ΔN_{it} (midgap to flatband) and oxide trap ΔN_{ot} charge densities were determined for MOS capacitors by the following equations via the midgap charge separation method [12], [50]:

$$\Delta N_{ot} = -C_{ox} \frac{\Delta V_{mg}}{qA} \tag{2}$$

$$\Delta N_{it} = C_{ox} \frac{(\Delta V_{fb} - \Delta V_{mg})}{qA} \tag{3}$$

Here C_{ox} is the oxide capacitance, $-q$ is the electronic charge, A is the area, ΔV_{mg} is the midgap voltage shift, and ΔV_{fb} is the flatband voltage shift. Similarly, the

voltage shifts due to net-oxide trap charge ΔV_{ot} and interface trap charge ΔV_{it} can be estimated as:

$$\Delta V_{ot} = \Delta V_{mg} \tag{4}$$

$$\Delta V_{it} = \Delta V_{th} - \Delta V_{mg} \tag{5}$$

Please note that all the changes here are the differences between pre- and post-stress capacitance-voltage characteristics.

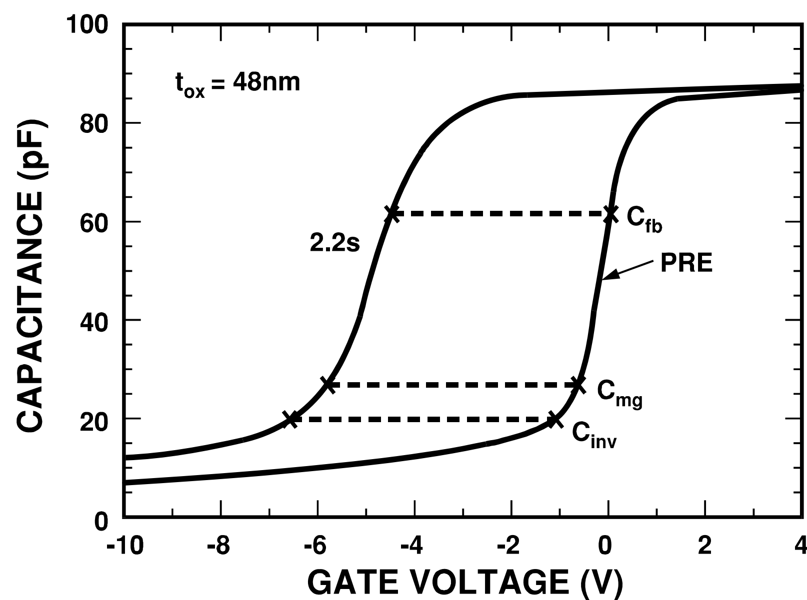


Figure 2 C-V curves for a n-substrate capacitor irradiated to 1 Mrad (SiO_2) with 10 V on the gate. After [50].

The concept of "border traps" was first proposed by D. M. Fleetwood in 1991 [51]. Border traps are oxide traps that are able to exchange charge with the Si on the timescale of the electrical measurements. The ability to exchange charge with the substrate during the measurement makes border traps looks like interface traps electrically; however, the location of these defects are in the oxide, instead of at the interface (Fig. 3) [52]. The microstructure of border traps is still under debate, with no

single defect likely responsible for all border-trap effects in all materials and devices. In some devices, border traps are apparently associated with hydrogen-related defects in the near-interfacial SiO_2 [53]-[54], or other defects not directly associated with trapped holes [55]-[56].Since border traps can sometimes be mistaken for interface traps electronically; separation of the contribution of border traps from real interface traps is performed in this study. The effective border trap density, ΔN_{bt} is obtained by measuring C-V hysteresis and integrating the absolute value of the capacitance difference [57]-[58]:

$$\Delta N_{bt} \approx (1/qA)\int \left|(C_{reverse} - C_{forward})\right| dV \quad (6)$$

$$\Delta V_{bt} = \Delta N_{bt}(q/C_{ox}) \quad (7)$$

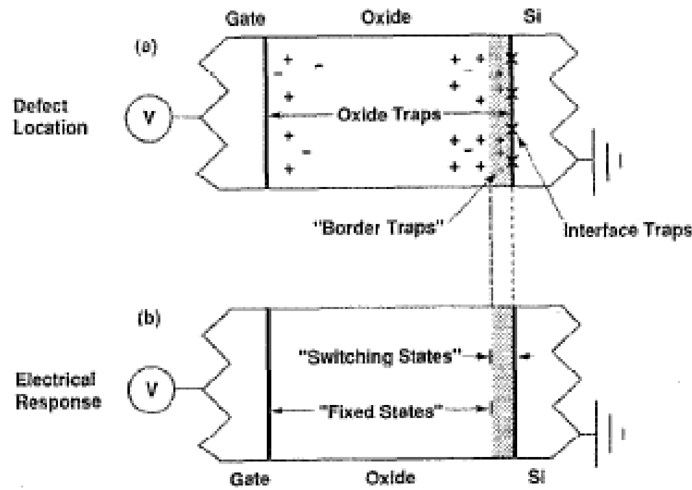
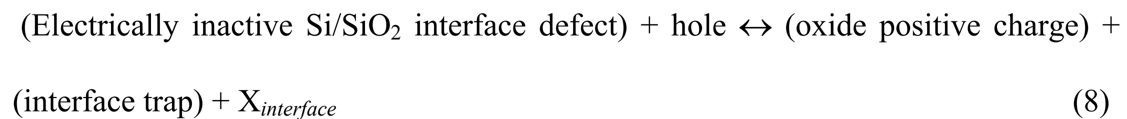


Figure 3 Nomenclature that separates terms used to identify (a) defect location from (b) measured electrical response in MOS devices. The line between an oxide trap and a border trap depends on the time scale and bias conditions of the measurements. After [52].

Review of Negative Bias Temperature Instability

Negative bias-temperature instabilities (NBTI) are associated with the generation of oxide and interface trap charge at the Si/dielectric interface, when negative bias is applied to the gate for long times and/or elevated temperatures [59]. Typical stress temperatures lie in the range of 50 °C-300 °C with oxide electric fields below 6 MV/cm [2]. Fields above this can lead to F-N degradation which is beyond the scope of the investigations in this thesis. NBTI is a long-term reliability issue for modern MOS devices with low operation voltage [60]. Although NBTI has been known for more than 30 years [61], the origins of NBTI are still under debate. In older generations of technology with thick oxides, NBTI often has been associated with water [3], [62], and/or oxygen vacancies near the Si-dielectric interface [63]. For thinner oxides, hydrogen reactions offer a more likely explanation [4], [60].

Among the numerous discussions of NBTI mechanisms, the reaction-diffusion model is the most popular one. The model is described in two steps, i.e., a reaction to create oxide and interface traps and the resulting diffusion and potential subsequent reactions of the initial reaction products. The following equations only provide one of the possible reactions:



(Electrically inactive Si/SiO_2 interface defect) + hole ↔ (oxide positive charge) + (interface trap) + $X_{interface}$ (8)

$$X_{interface} \xleftrightarrow{diffusion} X_{bulk} \quad (9)$$

Here X represents a hydrogen-related mobile species that diffuses away from the interface. Hydrogen has long been thought to be critical in NBTI and other defect formation processes in MOS gate dielectrics [2], [5], [59], [61], [64]. For thicker oxides, ΔN_{it} is governed by H_2 diffusion and

$$\Delta N_{it} = AE_{ox}^{m} t^{n} \exp(\frac{-E_a}{k_B T}) \qquad (10)$$

For thinner oxides, the devices tend to show instead a temperature-activated, E_{ox}-independent long-time ΔN_{it} increase [59], [65]-[71].The net activation energy can be expressed as a function of dissociation and annealing of Si-H bonds and the diffusion of hydrogen through the oxide [72]. Other than the electric field, temperature, thickness of oxide, and stress time are other important factors that need to be considered for developing an accurate extrapolation model for NBTI degradation to predict device lifetime. Jeppson and Svensson et al [71] proposed first a diffusion controlled mechanism to explain the time dependence of interface trap creation. Others suggested a reaction-limited mechanism [2], [4], [72]. Their assumption is that, as the reaction-limited time dependence obeys a linear relationship. The observed power-law dependence on the time (t^n) originates from the limitations on the reaction rates due to the subsequent reactions of the diffusing by-products (hydrogen-related) of the original reactions. M. A. Alam et al. proposed an "all-purpose" reaction-diffusion (R-D) model to explain the power law dependence--t^n observed in the experiments. They believe that interface trap creation is limited by a reaction (i.e., breaking of Si-H bond) at early stage. The subsequent diffusion of hydrogenated species dominates the process afterwards. The power law of time dependence applies over five interface trap generation regimes (shown in Fig. 4) [73]: (1) N_{it} increases due to Si-H bond breaking - here the system is reaction-limited with a characteristic slope of 1 (n = 1); (2) diffusion of hydrogen begins to take over (n = 0) - here the reaction is in equilibrium but the flux of hydrogen away from the interface is negligible; (3) trap creation is limited by hydrogen diffusion (n = 1/4), which is independent of the oxide field and/or the temperature but is only determined by the

nature of the diffusing hydrogenated species; (4) hydrogen diffuses in the gate with infinite diffusion velocity (n = 1/2), and (5) the maximum trap density, N_0, is reached due to the saturation of the process, and N_{it} no longer increases with time (n = 0). This is rarely observed in the experiments.

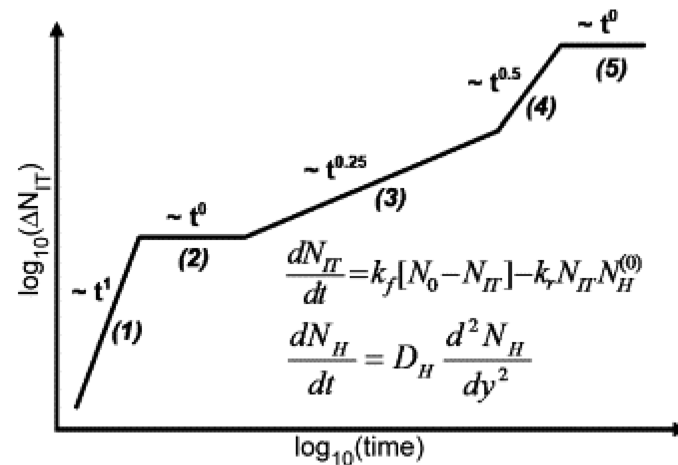


Figure 4 Classical R-D model results in five regions whose time behaviours are governed by the equations in the insert. D_H is the diffusion constant and k_f and k_r are the forward dissociation rate and reverse annealing rate of SiH bonds, respectively. After [73].

The equation in Fig. 4 can be obtained based on the diffusion control model with modified boundary conditions and Fourier transformation. Although the R-D concept is feasible, first-principle calculations based on density functional theory [74] show that direct removal of H is not energetically feasible. More details will be shown in Chapter IV; our revised R-D model will be introduced at the same time.

Empirical models are directly from experiments when NBTI degradation saturates. All the parameters are extracted from the data and the dependence of electric field (E_{ox}) on threshold voltage shifts (ΔV_{th}) is expressed as an exponential function [75]-[76]:

$$\Delta V_{th} = C \exp(\beta E_{ox}) \exp(-\gamma time^{-1/\alpha}) \quad (11)$$

C. E. Blat and E. H. Nicollian proposed a totally different model based on a first-order electrochemical reaction in the form of [2], [77]:

$$\equiv \text{Si-H} + \text{A} + p^{+} \leftrightarrow \equiv \text{Si}\cdot + \text{B}^{+} \quad (12)$$

Here A is a water-related species. Induced interface and oxide-fixed charge densities are equal and the rate of defect creation depends on the hole (p^+) concentration and electric field. Water must be present in the oxide near the Si-SiO_2 interface to initiate the reaction. They also believe that the interface trap density equals to the oxide trapped charge density which contradict with the experimental results.

Charge trapping can also be the cause of true NBTI or "NBTI-like" degradation [78]-[83]. The threshold voltage shifts are either due to the tunnelling of holes or a kinetic process initiated by hot electrons injected from the gate electrode. The latter is especially important for higher electric fields than we consider in this thesis, but often are considered NBTI in the literature. Charge transport and trapping lead to oxide and interface trap charge buildup and device degradation.

NBTI models I described so far focus on the degradation of device performance; there is a need for further study on defect formation at atomic level. J. M. Soon et al [84] suggest that released H^+ will attach to bridging oxygen atoms (Si-O-Si) near the interface. The NBTI-induced defect will weaken the bond strength of Si-O and trigger more breakdown events in the device. J. Ushio calculates the total energies of representative H positions in neutral and positive states where oxygen vacancies serve as hole trapping centers. The results show that the H migration is much easier to occur in the hole-trapping state than in the neutral state, and the activation energy change by electric field is too small to explain the experimentally observed electric-field dependence [85]. L. Tsetseris et al. (our group) suggest that the

depassivation of Si-H bonds by protons can account for the generation of interface traps. A possible source of hydrogen is from dopant sites in the depletion region of the Si-substrate [74]. More details will be discussed in Chapter IV. Although no single theory can fully explain all NBTI phenomena, such calculations provide insightful implications for the future study.

Many factors can impact NBTI sensitivity, such as chemical species (hydrogen, nitrogen, water, fluorine, and boron) which were introduced into the devices during the process, orientation of Si-substrate, temperature, the processing of the oxide layer [5], etc. Most of these effects either modify the reaction dynamics or influence the rate at which NBTI occurs within a given process and for a given device geometry. To minimize NBTI degradation, the following methods need to be considered: (1) Improve the quality of the gate oxide and interface. The passivation of traps or dangling bonds with a species more resistant to chemically or charge-induced bond breaking by hydrogen is a possible solution to minimize NBTI degradation. (2) Reduce concentration of certain chemical species. Nitrogen at the interfacial layers and water in the bulk can lower the NBTI activation energy and should be avoided or (in the case of nitrogen) used as sparingly as possible, especially at the Si/oxide interface region. (3) Minimize mechanical stress or strain at the interface. More serious NBTI degradations occur in the strained Si devices. Methods include modifying gate oxide formation temperatures and growth conditions, changes to post-oxidation annealing, and/or changing the parameters for ion implantation in the nitride layers or stress compensating layers [86]. (4) Substitute deuterium for hydrogen. Since D_2 has higher binding energies and diffuses slower than hydrogen [87]-[88]. Full understanding of the impact of these issues on NBTI can lead to more easily qualified and stable devices.

CHAPTER III

EXPERIMENTAL DETAILS

System Setup

For the bias temperature-stress experiments described in this thesis, the samples were heated with a hot chuck (Model S-1060R, Signatone) and held at a constant temperature for a period of time under bias. A HP 4140B picoammeter/DC Voltage Source served as bias source. The stress time and temperature can be controlled by program #1 in the appendix A. The changes in interface trap and oxide trap charge densities were determined from high-frequency (1 MHz) capacitance-voltage (C-V) measurements via the midgap charge separation technique described in Chapter II [50]. C-V measurements were executed on a HP 4175A Multi-frequency LCR Meter. The source control code (#2) is shown in the appendix as well. Fig. 5 shows a schematic diagram of the whole measurement process.

Irradiations were performed using an ARACOR Model 4100 10-keV X-ray irradiator. The choices of specific dose rate during irradiation do not significantly affect the results presented in this dissertation. The dose rate used in this study is 31 krad(SiO_2)/min. Different total dose levels were achieved by varying the irradiation time. The typical total ionization doses applied are 500 krad(SiO_2), 1 Mrad(SiO_2), and 2 Mrad (SiO_2).

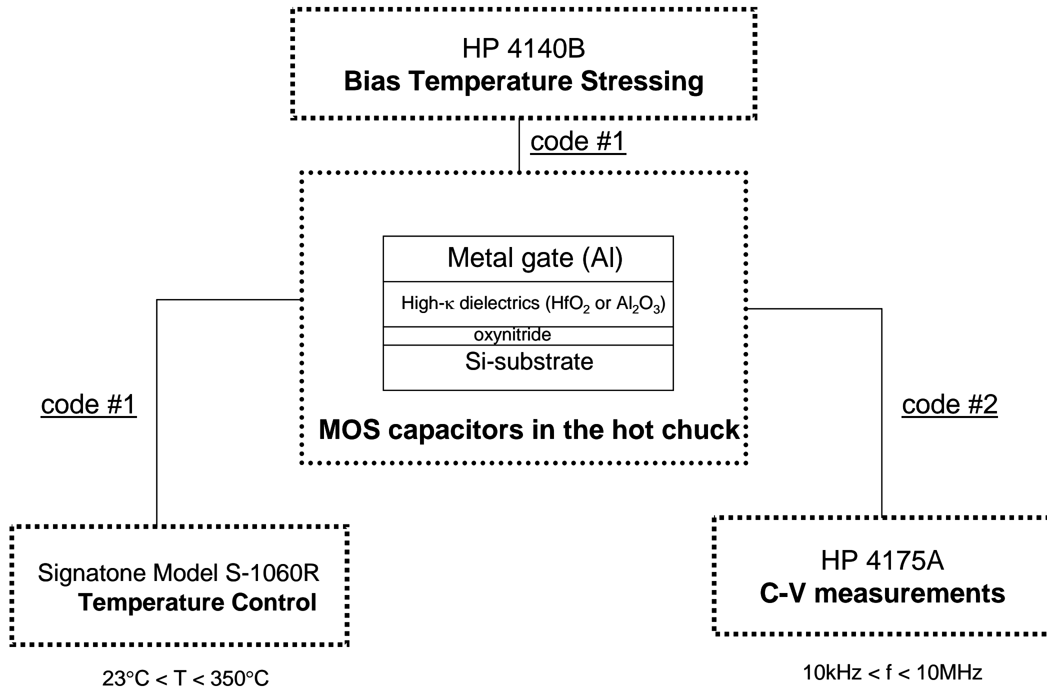


Figure 5 Schematic diagram of measurement system.

Devices

For NBTI experiments, two types of capacitors were compared. One has a thermal SiO_2 gate oxide; the other has an HfO_2 gate dielectric with a thin oxynitride layer at the Si interface. The standard thermal oxide was prepared by rapid thermal processing at 1000°C in dry O_2 to form a 6.5 nm thick SiO_2 dielectric layer on p-type Si (100) wafers. No post-oxidation annealing was performed. The SiO_xN_y/HfO_2 capacitors were fabricated on HF-last p-type Si (100) wafers with a doping concentration of ~10^{16} cm^{-3} [89]. The physical thickness of the high-κ layer was 6.8 nm as measured ellipsometrically; the interfacial oxynitride layer was 1.0 nm. The interfacial oxynitride films were thermally grown in a mixture of NO and O_2 at 900°C, resulting in ~ 10% to 15% N incorporation. The high-κ layers were deposited by atomic layer deposition (ALD) at 300°C using conventional surface chemistries.

The relative dielectric constants (ε_r) of the HfO_2 and interfacial oxynitride layer (SiO_xN_y) are ~ 20 and ~ 4, resulting in an equivalent oxide thickness (EOT) of 2.1 nm. Al gates were deposited to form gate electrodes. Atomic layer deposition (ALD) is the most promising high-κ deposition technology [15], [90]-[91]. ALD films are formed by repeating a sequence of alternating surface-reactant interactions, which are saturating and "self-limiting." This technique gives highly conformal films with monolayer control of film thickness, uniformity, and materials properties.

For the radiation experiments, two types of high-κ based MOS capacitors are compared. One has HfO_2 dielectrics and the other has Al_2O_3 dielectrics. The HfO_2 capacitors were formed on p-type (100) Si as described previously, but the Al_2O_3 capacitors were formed on n-type (100) Si. The Al_2O_3 layer was deposited by atomic layer deposition (ALD) at 300°C using standard Al (CH_3) + H_2O surface chemistries [14], [18], [92]-[93]. After deposition, the dielectrics were subjected to a forming gas (5-10% H_2 in N_2) anneal (FGA) at 550°C. 1.0-nm-thick interfacial oxynitride films between Al_2O_3 and the Si substrate were thermally grown in a mixture of NO and O_2 at 900°C, resulting in ~10% to 15% N incorporation. After the annealing, the Al gate electrodes were evaporated at room temperature. The relative dielectric constant of as-deposited Al_2O_3 is ~8 and the relative dielectric constant of silicon oxynitride is ~4-5 for this concentration of N. The equivalent oxide thickness (EOT) of the dielectrics studied here are 3.1 nm.

The combined effects of irradiation and the subsequent BTS were studied on both kinds of MOS capacitors with high-κ dielectrics. Detailed switched-bias experiments either after X-ray irradiation or constant voltage stress (CVS) were performed on Al/HfO_2+SiO_xN_y/Si *p*MOS capacitors.

CHAPTER IV

BIAS TEMPERATURE INSTABILITIES: MEASUREMENTS AND THEORY

In this chapter, experimental results of negative bias temperature stressing degradation are presented first. Experimental activation energies were extracted and compared with theoretical values based on first-principle calculations and revised reaction-diffusion (R-D) theory. The results show that excess hydrogen plays a fundamental role in the defect creation process.

Experimental Data

For the NBTI measurements, the MOS capacitors were heated with a hot chuck and held at a constant temperature under negative bias. The holding temperatures vary from 50 °C to 300 °C and the applied electric fields are between – 1 MV/cm and – 2 MV/cm. The post-stress 1-MHz high-frequency capacitance-voltage curves were taken after the samples cooled to room temperature. Voltage shifts due to net oxide-trap ΔV_{ot} and interface-trap charge ΔV_{it} were estimated via the midgap charge separation method of Winokur et al. [50].

To ensure that the measured NBTI degradation is not affected by charging effects due to high currents through the oxide [94]-[95], the gate current was monitored during all experiments with a HP 4140B picoammeter. This is particularly a concern for the SiO_xN_y/HfO_2 capacitors, as illustrated in Fig. 6. Data sets for which injected charge densities exceeded a threshold of ~ 10^{-4} C/cm^2 (above which carrier injection and trapping can dominate over NBTI) were not included in this study.

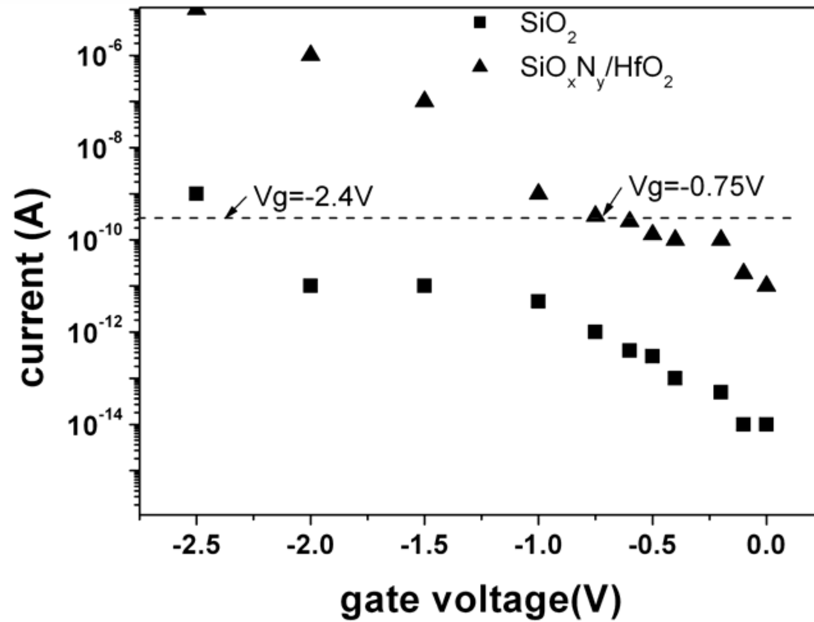


Figure 6 Leakage current vs. gate voltage for MOS capacitors with thermal SiO_2 and SiO_xN_y/HfO_2 gate dielectrics. The dashed line denotes the leakage current level above which significant charging occurs in the dielectric associated with mechanisms other than NBTI. After [89].

Despite this limitation, activation energies for NBTI from Arrhenius plots for an adequate range of temperatures and biases for both device types can still be extracted. A large number of devices were characterized for NBTI over a wide range of bias/temperature stress conditions; results under test conditions that showed maximum, reproducible (to within experimental variation) NBTI with minimum gate leakage are illustrated in Fig. 7. Here Fig. 7 shows ΔN_{ot} and ΔN_{it} for capacitors stressed for 1200 s as a function of temperature at an applied electric field of -1.54 MV/cm for the thermal oxide, and an applied field of -1.15 MV/cm for the SiO_xN_y/HfO_2 oxide. The activation energies (Ea)are listed in Table 1:

These results are comparable to the range of activation energies for NBTI that have been reported in the literature [59], [61], [64], [96].

Table 1 Activation Energies for SiO_2-based and HfO_2-based MOS capacitors

Defect Type	Ea (eV)	
	SiO_2-based MOS-C	HfO_2+ SiO_xN_y MOS-C
ΔN_{ot}	0.27 ± 0.03	0.35 ± 0.04
ΔN_{it}	0.31 ± 0.04	0.22 ± 0.03

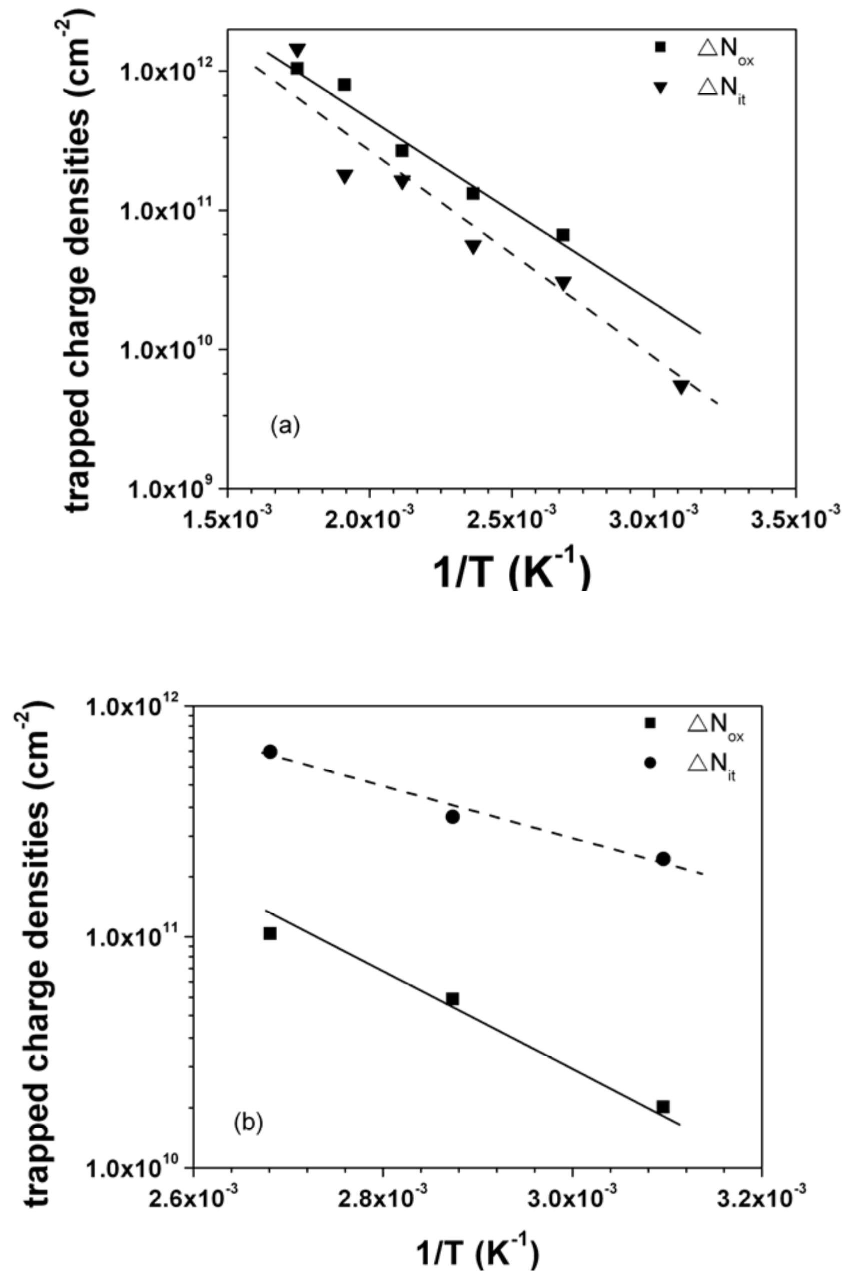


Figure 7 Oxide- and interface-trap charge densities as a function of stressing temperature for (a) SiO_2 capacitors stressed for 20 minutes at – 1.54 MV/cm; and (b) SiO_xN_y/HfO_2 capacitors stressed for 20 minutes at – 1.15 MV/cm. New devices were selected for each stress condition. After [89].

Similar activation energies for oxide-trap and interface-trap charge formation due to NBTI in MOS capacitors with SiO_2 and HfO_2+SiO_xN_y gate dielectrics were found. And these activation energies are consistent with lateral motion of protons at the interface. One possible origin for this defect formation is H^+ release from oxygen protrusions in the near-interfacial Si, its diffusion along the Si/dielectric interface, followed by its reaction with Si-H to form interface traps, or its capture at a sub-oxide bond to form positive oxide-trap charge. These oxygen protrusions can release the hydrogen as H^+ after these complex capture a hole [89], [97]-[100]. The barrier for subsequent lateral motion of H^+ along the Si/SiO_2 interface is ~ 0.3 eV [101]. At least some of the differences in the levels of defect formation between the SiO_2 and SiO_xN_y/HfO_2 devices in this study may then be explained by differences in the amount of hydrogen in the two types of devices, as well as differences in O vacancy densities in the near-interfacial SiO_2. These results are consistent with the key roles played by hydrogen in MOS defect formation in MOS radiation response and long-term reliability [102], and suggest that minimizing excess hydrogen, O vacancies, and/or oxide protrusions into Si may help to reduce NBTI.

Theoretical Calculations

Although the activation energies in Fig.7 are similar to calculated energies for processes such as lateral proton migration along the Si/SiO_2 interface, it is difficult to understand why such low-energy processes should be observed at or above room temperature. Futher theoretical calculations by L. Tsetseris et al.[74] were performed after the publication of Fig. 7 that are based on density functional theory (DFT) to provide a better understanding of NBTI on atomic scale. The DFT calculations were performed with gradient corrections for the exchange-correlation functional. Plane

waves (cutoff ~ 650 eV) were used as a basis set, utilizing untrasoft pseudopotentials [103] as implemented in the VASP code [104]. Large enough periodic supercells were used to provide realistic geometries and to ensure convergence of results.

The Si-H bond is the most typical precursor for interface traps, as the removal of the H atom leaves behind dangling bonds, which are identified in the literature as P_b centers [48]. The direct dissociation of Si-H bonds at the Si/SiO_2 interface has been suggested as a mechanism for generation of traps during NBTI when holes are present, as discussed earlier in Chapter II.

$$\text{Si-H} \rightarrow \text{Si}^{-} + \text{H} \tag{13}$$

However, DFT calculations show that the removal of the H atom from the Si-H bond to a remote Si-Si bond raises the energy of the system by ~ 1.9 eV. Adding the associated migration barrier, which is ~ 0.5 eV, results in the total dissociation activation energy of 2.4 eV [74], in agreement with experimental measurements (2.6 eV) [105]-[108]. When hole are present, as is the case for NBTI in pMOS transistors, the energy required to remove H decreases to 1.6 eV and E_a decreases to 2.1 eV. These values are well above those expected to affect NBTI, at least in the absence of high electric fields, and/or the existence of additional nearby defects. Hence, the direct dissociation mechanism is not the case for the normal operation of commerical-grade MOS devices.

Given that direct dissociation of Si-H bonds is not the cause for NBTI, the most plausible alternative is the depassivation reaction [74], [98], [100], [109]:

$$\text{Si-H} + \text{H}^{+} \rightarrow \text{D}^{+} + \text{H}_2 \tag{14}$$

First-principles DFT calculations find the reaction energy and barrier for process (14) to be 0.5 eV and 0.95 eV respectively, when the Fermi level is at the valence band maximum. This is for n-type Si under inversion. Hence this process is

energetically preferred to direct dissociation and this process can reach quasi-equilibrium for long stress times.

The mechanisms responsible for NBTI for n-type Si are described schematically in Fig. 8. The proposed mechanism for depassivation of dangling bonds (14) requires a source of H. Possible stable and metastable binding sites for H include oxygen protrusions, interstitial O in Si (Si-O-Si configurations) and dopants. These possibilities have been explored, and it is found that, in n-type Si (that is, for pMOS transistors), where H exists as H^- (due to its "negative-U" properties in Si [110]), it only binds to dopants. Calculations verify that the equilibrium H position in a p-H complex is the so-called antibonding (AB) site [111]. The energy required to move H from the AB site to a remote position (binding energy Δ_{PH}) in Si is 0.6 eV, combined with the migration barrier 0.7 eV for H^- [112], gives an activation energy of 1.3 eV for dissociation of P-H complex, in agreement with the experimental value of 1.18 eV [113]. Hence, excess hydrogen can facilitate the breaking of the Si-H bond much more easily through chemical reaction than can the direct interaction of the holes at the interface.

The stability of the P-H complex changes dramatically when the charge state of hydrogen changes to neutral (H^0). H stays neutral for a certain period of time after its release in the depletion region under NBTI stress, even though at equilibrium H exists only as H^+ or H^-. The binding energy Δ_{PH} drops from 0.6 eV to 0.2 eV for neutral H. Plus the diffusion barrier of H^0 in Si (0.1- 0.2 eV) [110] is smaller than H^+ and H^- diffusion barriers (0.48 eV and 0.7 eV[112] respectively). The resulting activation energy (E_a^0) to release H^0 from a P-H complex is only 0.3-0.4 eV. This value is in agreement with the measured E_a^0 (0.3 eV) for minority-carrier-enhanced dissociation of P-H complexes in the depletion region of Si [114].

Because of the very small activation energy, all of the H in P-H complexes in the depletion region is released and can migrate rapidly with a small barrier for H^0 (0.1-0.2 eV, shown in Fig.8 (1a)). Also at 100-200°C, some hydrogen can be released from complexes deeper in the Si substrate (illustrated as Fig. 8(1b)). Hydrogen that arrives or is released in the inversion layer becomes positively charged (H^+) by trapping a hole under negative bias; this H^+ is swept to the interface by negative bias. The inversion layer and the depassivation reaction combined act as a "sink" for hydrogen motion in Si. The whole process is depicted in Fig. 8. Because of the relatively high density of dopant atoms in the substrate, only a very small percentage of P atoms must bind a hydrogen atom prior to NBTI in order to produce the numbers of interface traps typically measured in NBTI experiments.

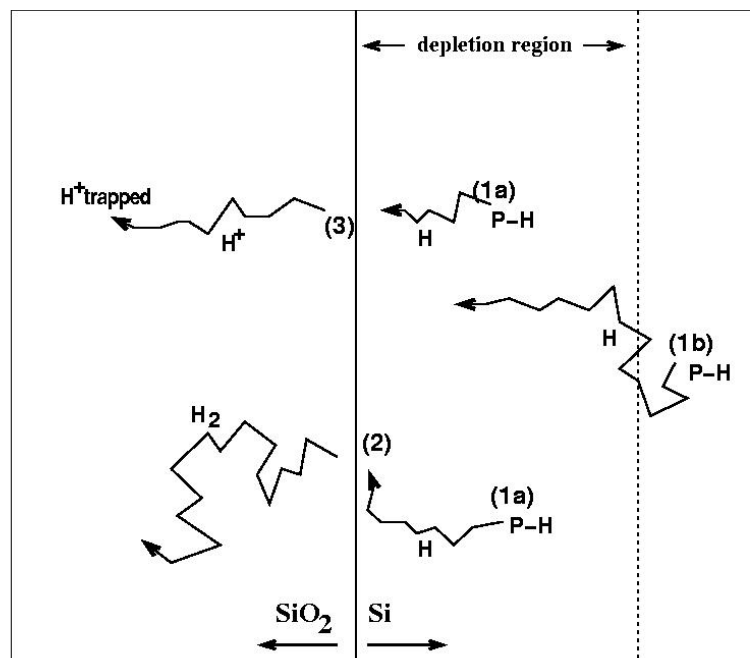


Figure 8 NBTI steps: (1a-b) release of H from P-H complexes in the depletion region (easy) or deep in Si (infrequent), (2) depassivation, or (3) entry of H^+ in SiO_2. After [74].

Protons that reach the interface encounter a large barrier of 1 eV [99] to enter SiO_2, so they first migrate rapidly along the Si side of interface. The passivation of dangling bonds by transporting protons is suppressed since both of them are of the same charge. So these protons cannot passivate pre-existing interface traps. Additionally, the energy for H^+ at the center of a Si-Si bond next to a Si-H entity is lower by 0.2 eV with respect to other sites for H^+ in Si. Therefore, hydrogen can easily find Si-H bonds and activate the reaction (14). At 100-200°C, this reaction reaches quasi-equilibrium quickly and after this point the dynamic balance is controlled by the diffusion of the products H_2. In this diffusion-limited regime, E_a is given by [4], [115]:

$$E_a = \frac{\Delta E}{2} + \frac{\Phi_D}{4} \quad . \qquad (15)$$

In Eq (15), ΔE is the reaction energy of process (14), andΦ_D is the diffusion barrier of the migrating species. According to first-principles calculations [74]: ΔE = 0.5 eV, Φ_D = 0.45 eV [116] for H_2 diffusion in SiO_2, so E_a ~ 0.36 eV which is in very good agreement with previous experimental data [59], [64], [85], [89], [96].

Protons that arrive at the interface can also eventually migrate into the oxide where they contribute to the buildup of oxide trapped charge. Significantly, oxide-trap charge in the form of a proton is much more difficult to neutralized via electron tunneling than trapped holes, leading to the relative stability of trapped H^+ in SiO_2 under NBTI stress conditions [89], [98]. In the asymptotic limit, the rate of such buildup is controlled by diffusion of the "product" H^+ in SiO_2. DFT calculations show that the diffusion barrier (Φ_D) of H^+ in SiO_2 is ~0.8 eV [102], [117], and change in energy as H^+ enters the oxide (ΔE) is 0-0.2 eV. Substituting these values in equation (15), it is found that E_a = 0.2 - 0.3 eV. For the increase of oxide trapped charge, this is consistent with measured values [64], [85], [89]. As for the formation of interface

traps, the small E_a observed in experimental studies is only an apparent activation energy, observed at the large stress time limit, after the migration of H^+ from the Si to SiO_2 reaches quasi-equilibrium.

Other experimental BTI scenarios-all consistent with current model

Other key BTI issues will now be addressed. The effect of negative bias is related to the large reduction of the P-H dissociation energy in the depletion region and the appearance of a boundary condition (sink of hydrogen) that biases the migration of H in the direction of the interface. A positive bias (PBTI) on a *p*-MOSFET can still result in degradation, but in this case the rate limiting step is the thermal dissociation of P-H complexes (barrier 1.18 eV [113]) in the accumulation region. This process may help to explain the results of Zhang and Eccleston [7] and in particular their large extracted E_a (1.23 eV) for PBTI.

Degradation can occur for p-type Si, as indicated in Fig. 8 above, however, so this degradation is typically smaller than for n-type Si. This is because the E_a for dissociation of B-H complexes (1.28 eV [118]) is larger than the P-H value. The release of H is thus more difficult in B-doped Si, leading to a less pronounanced BTI degradation.

For NBTI on p-type Si, the rate limiting step for small time is the thermal dissociation of B-H complexes, consistent with first-order reaction kinetics observed by Blat et al [2], and higher T and/or longer times [59] are required to reach the diffusion-limited regime. However, in this case, another possiblity could be the release of H from O interstitutials in the near interfacial Si region [89]. Such O atoms in the substrate have been shown to exist in certain cases in concentrations large enough to account for NBTI on p-type Si [97].

Any step that can lead to an increase of H content in the substrate, for example by annealing in H_2 or H_2O ambients [2], [7] will result in an increase for NBTI degradation. Other species, such as fluorine [119], or nitrogen in the near interfacial SiO_2 [64], [69], [72], [78], can also affect the kinetics of the depassivatin reaction and impact NBTI degradation. Fluorine has two-side effects on NBTI degrdation: on the one hand, Si-F interfacial bonds are resistant to depassivation by hydrogen species; on the other hand, an excess of fluorine can create stretched bonds, which can act as carrier traps, or disrupt an abrupt interface by cleavage of Si-Si bonds. More discussions can be found in ref [119].

In summary, NBTI induced oxide trapped charge and interface trap densities were determined at different temperatures. Activation energies were extracted from Arrhenius plots and those results are in good agreement with the therotical calculations based on our revised R-D model. The depassivation of Si-H bonds by protons as a reaction that can account for the observed generation of interface traps. The trapped protons in the oxide attribute to the oxide trapped charge buildup. The possible source of hydrogen needed to initiate depassivation is identified as such species released from dopant sites in the substrate. Finally, other key issues of NBTI are discussed briefly and those discussions are consistent with the present model.

CHAPTER V

RADIATION RESPONSE OF ALTERNATIVE HIGH-K DIELECTRICS

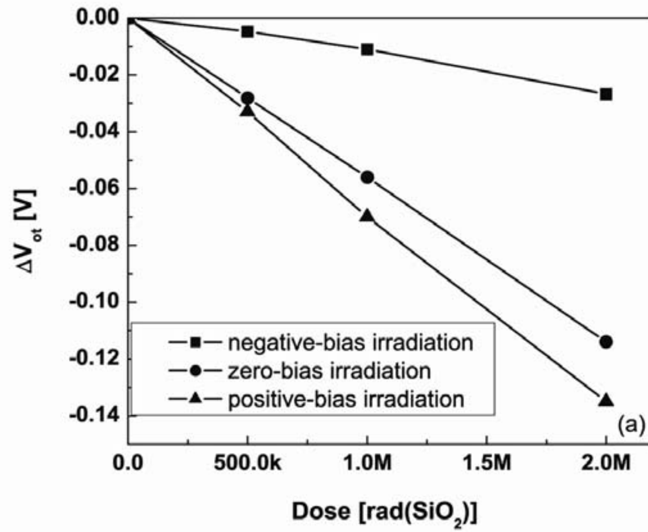
This chapter describes the radiation response of HfO_2-based and Al_2O_3-based MOS devices. Different bias conditions and total dose levels are chosen during irradiation of each group. Effective trapping efficiencies are determined from experimental results.

HfO_2-based Devices

Fig. 9 shows results for Al/HfO_2+SiO_xN_y/Si *p*MOS capacitors irradiated with 10-keV X-rays to 2.0 Mrad(SiO_2). The largest shifts in both ΔV_{ot} and ΔV_{it} are observed for positive-bias irradiation, consistent with most (but not all [120]) experience with thermal SiO_2.

Trapping efficiency is a dimensionless quantity used to approximate the intrinsic defect density of an insulator [121]-[122]. Effective trapping efficiencies (f_{ot}) of high-κ dielectrics were defined as what the trapping efficiency would be if the gate dielectrics were SiO_2 [12]:

$$f_{ot} = -\frac{\Delta V_{mg} \varepsilon_{ox}}{q \kappa_g f_y t_{eq} t_{phys} D} \qquad (16)$$



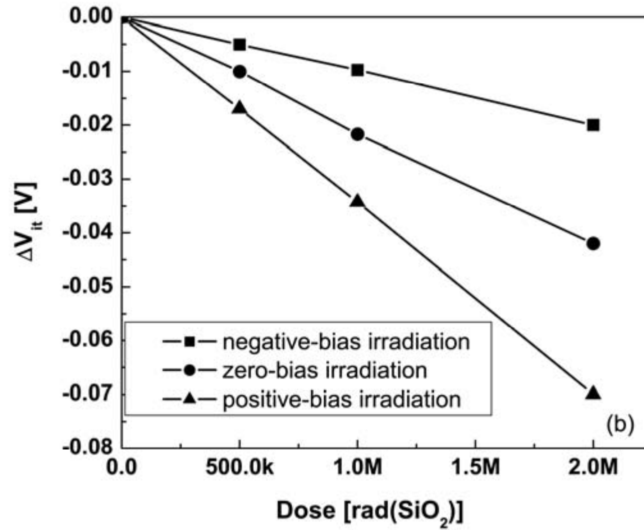


Figure 9 (a) ΔV_{ot} and (b) ΔV_{it} as a function of dose for Al/HfO2+SiOxNy/Si *p*MOS capacitors irradiated with 10-keV X-rays at a dose rate of 31 krad (SiO2)/min. The gate biases during irradiation are 0.3V (E_{ox} = 2.4 MV/cm), 0V, and - 0.3V (E_{ox}= - 2.1 MV/cm). The effective oxide thickness is 2.1 nm. All calculated electric fields include the appropriate work function differences between the Al and Si. After [92].

Here ΔV_{mg} is the midgap voltage shift, ε_{ox} is dielectric constant of SiO_2 (~ 3.5×10^{-13} F/cm), $-q$ is the electronic charge, κ_g is the number of electron-hole pairs (EHP) generated per unit dose, f_y is the charge yield, t_{eq} is the equivalent oxide thickness (EOT), t_{phys} is the physical thickness of the alternative dielectric, and D is the total dose [12], [121]. Currently, κ_g and f_y are not known for alternative dielectrics. To first order approximation, it is possible to use the known value for SiO_2 scaled by the ratio of the band-gap of SiO_2 to the band-gap of the high-κ materials since this equation (16) is used to compare with SiO_2. The t_{phys} in equation (16) is for the charge generation throughout the entire volume of the oxide, while the t_{eq} term is to account for the moment arm effect resulting from the spatial distribution of the charges in the oxide projected to the interface [123]. In similar equations for SiO_2, both of these effects are accounted for by a single t_{ox}^2 term [121]. However, for high-κ dielectrics, in order to still use ε_{ox} in equation (16), it is necessary to distinguish between the electrical thickness (EOT) and the physical thickness [12].

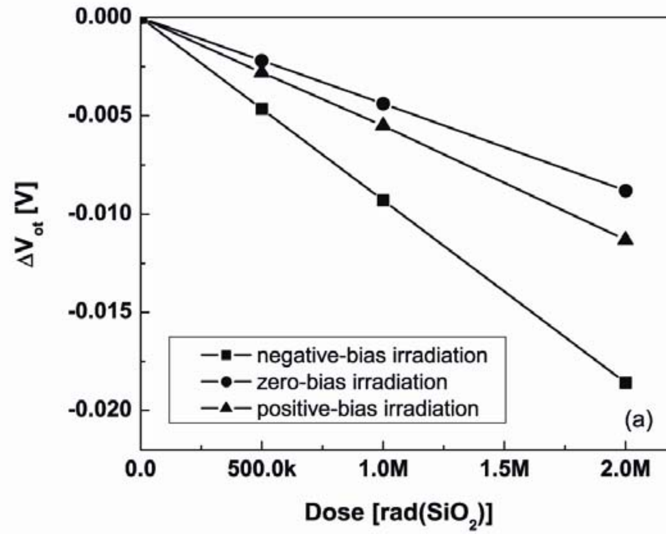
Here, $f_y = 0.45$, and $\kappa_g = 1.2 \times 10^{13}$ $cm^{-3}rad^{-1}$. This is the known charge generation value of SiO_2 (~ $8.1 \times 10^{12} cm^{-3}rad^{-1}$) scaled by the ratio of the bandgap difference between SiO_2 and HfO_2. For 1 Mrad(SiO_2) irradiation at positive bias, an effective net oxide-trap charge trapping efficiency (ignoring potential dose enhancement effects from the Hf) is estimated as ~ 22% for these HfO_2 devices, which is similar to other results for high-κ devices in the literature [12]-[13], [46]. However, at the same total dose level, the trapping efficiency of the thermal oxides can range from a few percent up to ~50%, depending on the number of oxygen vacancies in the oxide and oxide quality itself [12], [121]-[122].

Al_2O_3-based Devices

Fig. 10 shows the radiation responses of $Al/Al_2O_3+SiO_xN_y/Si$ *n*MOS capacitors irradiated with 10-keV X-rays to 2.0 Mrad(SiO_2). The largest shifts in both ΔV_{ot} and ΔV_{it} are observed for negative-bias irradiation for these step-stress experiments, in contrast to what was observed in Fig. 9 for the HfO_2 devices. In devices with thicker Al_2O_3 dielectric layers, Felix et al. observed roughly equal values of ΔV_{ot} for positive and negative bias irradiation [13].

Taken together, these results show that more charge trappings occur in the bulk of the insulators for these devices, with the relative densities of positive and negative charge varying with processing conditions and/or dielectric thicknesses. The interface-trap buildup is greatest during negative bias in these devices, and may be caused by hydrogen that is released in the Si during the irradiation [74], [89]. For 1 Mrad(SiO_2) and negative-bias irradiation, the effective net oxide-trap charge efficiency [12] is ~23% for these Al_2O_3 devices, similar to the trapping efficiency of the HfO_2-based devices discussed above.

In summary, the radiation response of MOS capacitors with HfO_2 and Al_2O_3 dielectrics were evaluated and compared with thermal SiO_2. Their calculated effective net oxide-trap charge efficiencies are comparable to values in the literature. For HfO_2-based MOS capacitors, positive bias irradiation gives the largest degradation among all the other bias radiations; however, for Al_2O_3-based MOS capacitors, negative bias irradiation has the largest voltage shifts.



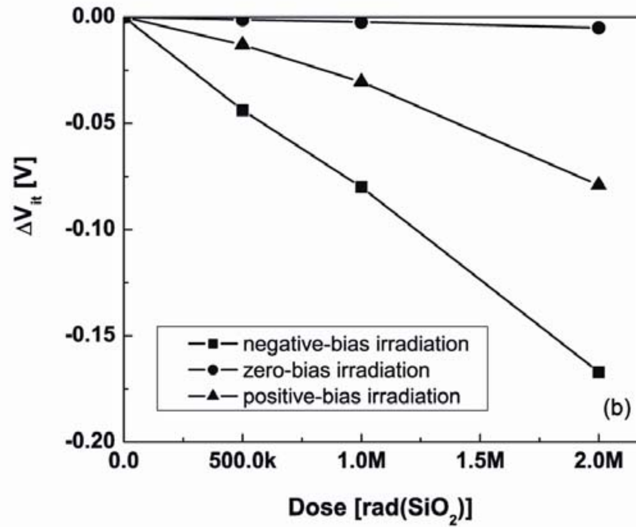


Figure 10 (a) ΔV_{ot} and (b) ΔV_{it} as a function of dose for $Al/Al_2O_3+SiO_xN_y/Si$ *n*MOS capacitors irradiated with 10-keV X-rays at a dose rate of 31 krad(SiO_2)/min. The gate biases applied during irradiation are – 0.3 V (E_{ox} = – 2.1 MV/cm), 0 V, and 0.3 V. The effective oxide thickness is 3.1 nm. After [92].

CHAPTER VI

COMBINED EFFECTS OF IRRADIATION AND BIAS TEMPERATURE INSTABILITY (BTI)

Detailed investigations of the combined effects of irradiation and bias temperature stress (BTS) for HfO_2-based MOS devices have been performed. The worst-case response of HfO_2 devices in a combined radiation and BTS environment is found to differ significantly from typical worst-case operating conditions for transistors with thermal SiO_2 gate dielectrics. For comparison, high-κ dielectric stacks incorporating Al_2O_3 were also evaluated for their combined irradiation and BTS response. Hardness assurance implications on both types of devices are discussed in this chapter.

HfO_2-based Devices

Fig. 11 shows combined effects of positive-bias irradiation and positive BTS (PBTS) on MOS devices with HfO_2 dielectrics. The combined irradiation and BTS values of ΔV_{ot} and ΔV_{it} exceed the sums of the separate irradiation and BTS results. Here the values of both ΔV_{ot} and ΔV_{it} for the combined stresses (solid circles) exceed those for the sums of the separate irradiation (Fig. 9) and pure BTS (open squares in Fig.11), denoted by the dashed curves in Fig.11. The degree to which combined stresses exceed the sums of the individual stresses increases with increasing temperature.

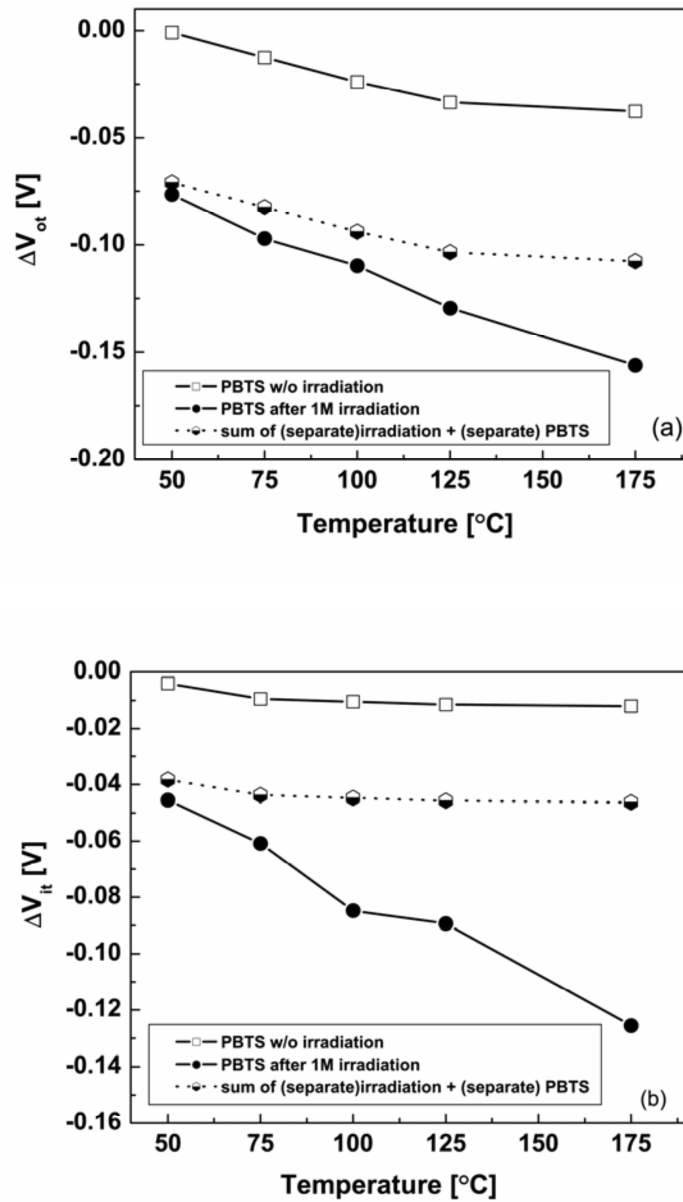


Figure 11 (a) ΔV_{ot} and (b) ΔV_{it} induced by positive bias-temperature stressing with or without positive-bias irradiation as a function of temperature for Al/HfO_2 + SiO_xN_y/Si *p*MOS capacitors. The gate bias is 0.3 V (E_{ox} = 2.4 MV/cm) for both irradiation and PBTS. The open squares represent the degradation by PBTS alone. The half open symbols represent the sum of separate 1 Mrad(SiO_2) positive-bias irradiation (Figure 9) and separate PBTS (open squares in Figure 11). The stress time was 600 seconds at each temperature. After [92].

The small increases in ΔV_{ot} and ΔV_{it} for PBTS without irradiation is likely due to the release and motion of protons within the oxide layers [124]. The enhancement of ΔV_{it} in Fig.11(b) is consistent with two-stage interface-trap buildup during irradiation and positive-bias annealing [125]-[126], but the enhancement of ΔV_{ot} differs from the reduction of net oxide-trap charge usually observed for irradiated SiO_2 with increasing anneal time at elevated temperatures [127]. This increase in ΔV_{ot} in Fig.11(b) likely is associated with radiation-enhanced H^+ motion and trapping at defect sites near the dielectric to Si interface during PBTS [5], [7], [53], [74], [89], [99], [128]-[129]. The amount of hydrogen in the films and the nature of its transport and trapping are expected to be a strong function of device processing [124].

The enhancement of ΔV_{ot} also differs from the response of Al_2O_3 under similar experimental conditions [38]. Due to high temperature forming gas annealing (FGA) processing, there are more “deep" electron trappings in the Al_2O_3 dielectrics to compensate trapped holes either through thermal annealing or tunnelling [38]. The processing dependence certainly warrants follow-on study and may crucially determine the relative amounts of hole and electron traps in the near-interfacial region of the high-κ dielectrics and impact their post-radiation responses.

In Fig. 12, HfO_2 capacitors are subjected to negative BTS (NBTS) with and without irradiation exposure. Values of ΔV_{ot} and ΔV_{it} with no irradiation are comparable to those observed in previous studies of NBTS in high-κ devices [34], [89], [130]. Values of ΔV_{ot} and ΔV_{it} after combined negative-bias irradiation and NBTS are much larger than the pure irradiation results in Fig. 9 at these doses (magnitudes of ΔV_{ot} and ΔV_{it} ~20 mV at 2 Mrad), the pure NBTS results in Fig. 12 (magnitudes of ΔV_{ot} and $\Delta V_{it} \leq$ 60 mV at 175 ºC), or the sums of the two (dashed

curves). This enhancement in combined response likely is evidence of dipolar charge trapping in the HfO_2 layers, which will be discussed in Chapter VII.

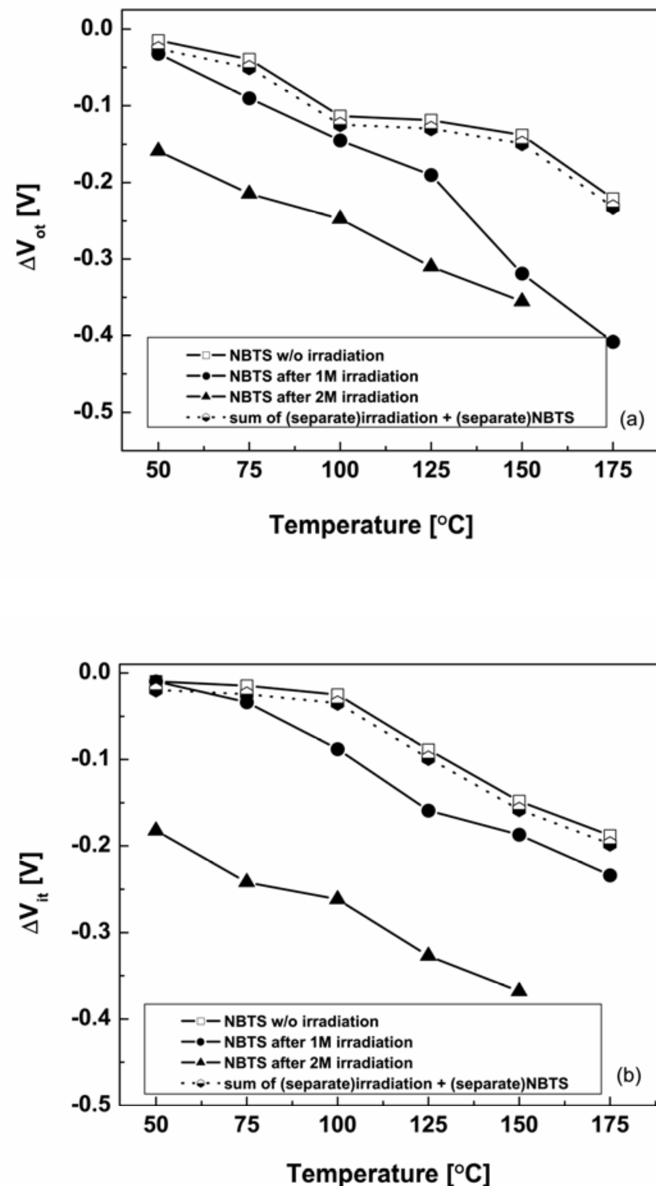
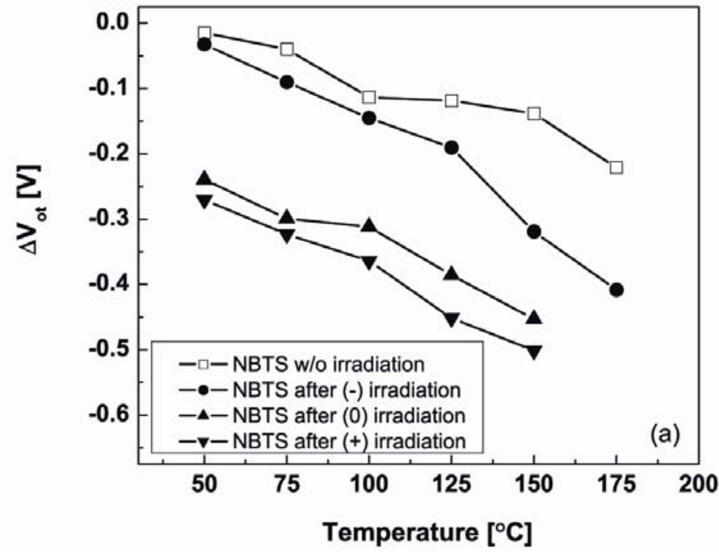


Figure 12 (a) ΔV_{ot} and (b) ΔV_{it} induced by negative bias-temperature stressing (NBTS) with or without negative-bias irradiation as a function of temperature for Al/HfO_2 + SiO_xN_y/Si *p*MOS capacitors. The gate bias is – 0.3 V for both irradiation and NBTS. The open squares represent the degradation by NBTS alone. The half open symbols represent the sum of separate 1Mrad(SiO_2) negative-bias irradiation (Figure 9) and separate NBTS (open squares in Figure 12). The 2 Mrad(SiO_2) experiment was stopped at 150 °C because the gate leakage increased above the 100 μC/cm^2 limit to avoid charging effects due to hot carriers (this current also may lead to some neutralization of ΔV_{ot}). Stress times are the same as in Figure 11. After [92].

In Fig. 13, HfO_2 capacitors are subjected to NBTS after positive bias, zero bias, and negative bias irradiation. Values of ΔV_{ot} and ΔV_{it} with and without prior irradiation are compared. Once again, combined irradiation and NBTS lead to significant enhancements of degradation over irradiation or NBTS alone. The worst case degradation here is caused by positive-bias irradiation followed by NBTS, with zero bias irradiation and NBTS causing the next worst case degradation in Fig. 13.

Fig. 14 summarizes ΔV_{ot} for the combinations of irradiation and BTS experiments performed on these HfO_2 devices; trends in ΔV_{it} are similar. The dose is 1.0 Mrad(SiO_2) in each case; the stress condition is 600 s at 75 ºC. This BTS condition is not intended to predict worst-case response at end of life for devices built in these technologies; it is instead intended to represent the kind of heating that may occur during typical device operation. Of the cases in Fig. 14, the worst-case ΔV_{ot} is positive-bias irradiation followed by NBTS. This is not a realistic pair of operating conditions for a typical circuit. However, nearly as much degradation is observed for zero bias irradiation followed by NBTS. This is a typical pair of operating conditions for a *p*MOS transistor. Moreover, the resulting voltage shifts at ~1.0 Mrad(SiO_2) in Fig. 14 are large enough to jeopardize circuit response (even before interface trap effects are considered, which will add further to the shift magnitudes), even at these 2.1 nm effective-oxide thicknesses [12]. Fig. 14 shows that, for cases in which field oxide leakage in *n*MOS transistors does not dominate the circuit radiation response [131]-[133], worst-case response for these devices likely will be for *p*MOS devices irradiated in the "off" state, and then turned on. This contrasts significantly to typical worst-case operating conditions for MOS devices with thermal SiO_2 gate oxides, in which *n*MOS transistors irradiated at positive bias usually show worst-case response [120].



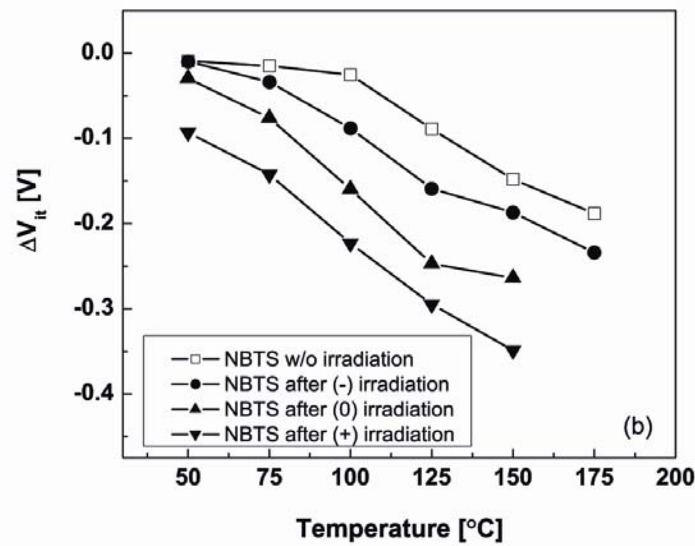


Figure 13 (a) ΔV_{ot} and (b) ΔV_{it} induced by negative-bias irradiation ($V_g = -0.3$ V), zero-bias irradiation, and positive-bias irradiation ($V_g = 0.3$ V; $E_{ox} = 2.4$ MV/cm), followed by negative bias-temperature stressing at 1 Mrad(SiO_2) as a function of temperature for Al/HfO_2 + SiO_xN_y/Si *p*MOS capacitors. The bias applied for NBTS is – 0.3 V. The total dose is 1 Mrad(SiO_2), and the stress times are the same as Figure 11 and Figure 12. After [92].

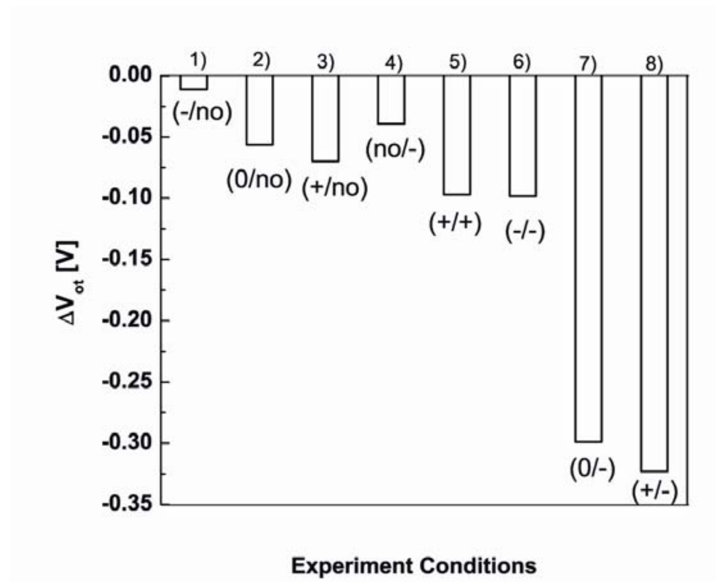


Figure 14 ΔV_{ot} at 1.0 Mrad(SiO_2) for Al/HfO_2+SiO_xN_y/Si *p*MOS capacitors for: 1) negative-bias irradiation and no BTS; 2) zero bias irradiation and no BTS; 3) positive-bias irradiation and no BTS; 4) no irradiation and NBTS; 5) positive-bias irradiation and PBTS; 6) negative-bias irradiation and NBTS; 7) zero-bias irradiation and NBTS; and 8) positive-bias irradiation and NBTS. The bias stressing temperature is 75 °C. Gate biases are ± 0.3 V or 0 V during irradiation, and ± 0.3 V during BTS. After [92].

The above effects should be possible to identify in lot acceptance testing if combined irradiation and BTS testing is performed. Indeed, although it was designed as a screen against interface-trap related failures in *n*MOS transistors, the "rebound" test in MIL-STD 883, Test Method 1019 (Fig. 15) may be well-suited for this purpose, since it includes irradiation to an additional 50% dose and a one-week, 100 ºC biased anneal [127], [134]-[135]. Suitable bias conditions would need to be chosen to match the worst-case response, which in this case would be those in which critical *p*MOS transistors were irradiated in the "off" state, and annealed in the "on" state.

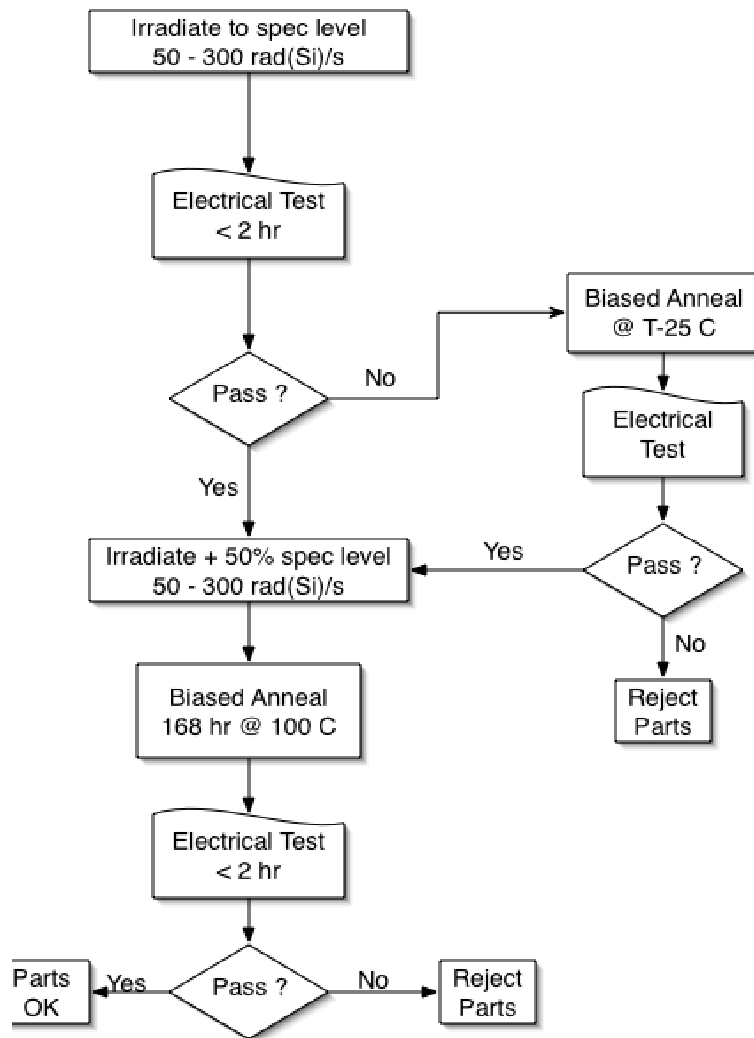


Figure 15 MIL-STD 883, Test Method 1019 flow chart. After [135].

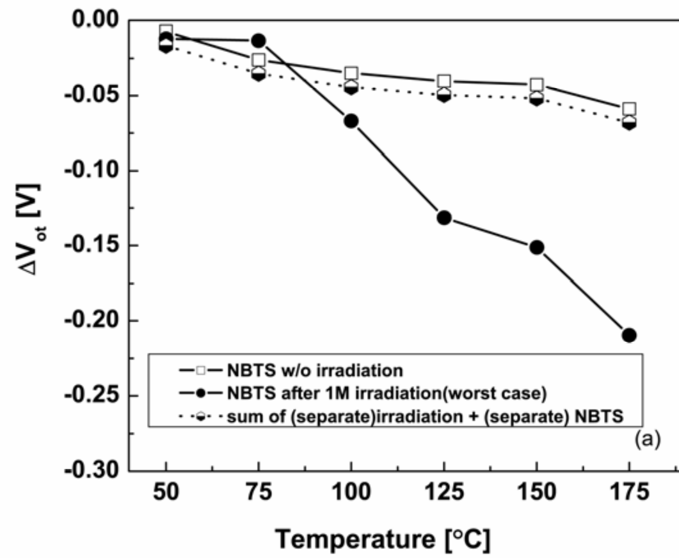
Al_2O_3-based Devices

Next, we discuss the combined effects of irradiation and BTS on MOS capacitors with Al_2O_3 dielectrics. The Al_2O_3-based devices were subjected to negative BTS after positive, zero, and negative bias irradiation exposure to 1.0 Mrad(SiO_2). Combined irradiation and NBTS values for ΔV_{ot} and ΔV_{it} are compared. The case with the largest voltage shift (NBTS after negative bias irradiation) was determined and is

shown in Fig. 16. The pure NBTS values for ΔV_{ot} and ΔV_{it} without prior irradiation are also shown. The combined irradiation and NBTS values of ΔV_{ot} exceed the sums of the separate irradiation (Fig. 10) and BTS (Fig. 16) results at higher temperatures (> 100 °C), as illustrated by the dashed curve, in comparison to the combined stresses. For example, for 1.0 Mrad(SiO_2) irradiation in Fig. 10, ΔV_{ot} = –0.01 V. After NBTS to 175 °C (Fig. 16), ΔV_{ot} = – 0.21 V for the 1.0 Mrad (SiO_2) case, as compared to the summed pure irradiation [1.0 Mrad (SiO_2), Fig. 10, - 0.01V] and NBTS (175 ºC, Fig. 16, – 0.055 V) values of – 0.065 V for ΔV_{ot}.

These increases likely are associated with the trapping of both positive and negative charge during irradiation, and the subsequent release of compensating electrons during the NBTS, as was the case for the HfO_2. However, the compensating electrons clearly are more stable in the Al_2O_3-based devices than the HfO_2 devices. Such variations in stability of compensating electrons have also been observed in irradiated SiO_2 [136]-[138], although not at relative densities as high as in these high-κ dielectrics. For these devices, worst-case irradiation response will be exhibited by *p*MOS transistors irradiated and annealed in the "on" condition.

In contrast to the ΔV_{ot}, the combined irradiation and NBTS values of ΔV_{it} generally are comparable (to within experimental uncertainty) with the sums of the separate irradiation (Fig. 10) and BTS (Fig.16) results. For example, for 1.0 Mrad(SiO_2) irradiation in Fig. 9, ΔV_{it} = – 0.07 V. After NBTS to 150 °C (Fig.16), ΔV_{it} = – 0.096 V for the 1.0 Mrad(SiO_2) case. This is quite similar to the summed pure irradiation [1.0 Mrad(SiO_2), Fig. 10, – 0.07 V] and NBTS (150 ºC, Fig.16, – 0.036 V) values of – 0.11 V for ΔV_{it}, as illustrated by the dashed curve.



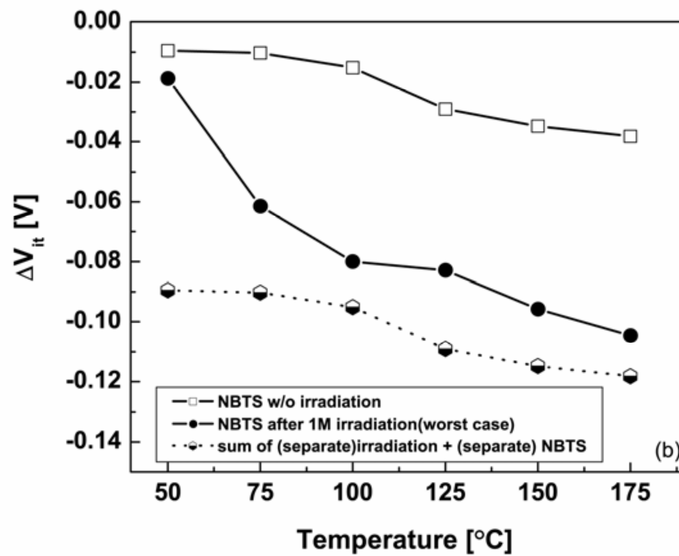


Figure 16 (a) ΔV_{ot} and (b) ΔV_{it} induced by NBTS after negative-bias irradiation (worst case) vs. NBTS without prior irradiation as a function of temperature for $Al/Al_2O_3+SiO_xN_y/Si$ *n*MOS capacitors. The dose is 1.0 Mrad(SiO_2). The gate bias is - 0.3 V (E_{ox}= - 2.1 MV/cm) for both irradiation and NBTS. The open squares represent the degradation by NBTS alone. The half open symbols represent the sum of separate 1 Mrad(SiO_2) negative-bias irradiation (Figure 10) and separate NBTS (open squares in Figure 16). The stress time is 600 seconds at each temperature. After [92].

That negative bias is worst case for these devices is evidence of bulk positive charge trapping in these SiO_2 films. An enhancement of oxide-trap charge away from the Si/SiO_2 interface has also been reported by Oldham et al. in commercial, non-radiation hardened oxides [139]. The apparent interface-trap buildup in these devices during negative bias may be caused by hydrogen that is released in the Si during irradiation, similar to what has been theorized during NBTS [8], [89], [94], [140], and observed for some bipolar base oxides [141].

In summary, the combined effects of irradiation and bias-temperature stress on capacitors with HfO_2 and Al_2O_3 based dielectrics stacks were investigated and compared to devices with thermal oxides. For each type of high-κ device, the combined effects of irradiation and BTS can be significantly greater than either alone, or than linear combinations of the two types of stresses. Worst-case responses in combined irradiation and BTS environments are positive (or zero) bias irradiation followed by NBTS for the HfO_2 based devices, and negative-bias irradiation followed by NBTS for the Al_2O_3 based devices investigated in this study. Hardness assurance tests that include irradiation and bias-temperature annealing may be used to predict the long-term radiation response and reliability of these devices, as long as worst-case conditions are properly identified and selected during device testing.

CHAPTER VII

CHARGE TRAPPING PROPERTIES DURING SWITCHED-BIAS ANNEALING

In this chapter, a series of switched-bias experiments at elevated temperatures after the irradiation was designed to investigate charge trapping characteristics during annealing. An electric field of 2 MV/cm was applied to the gate during irradiation. Alternating negative and positive bias-temperature annealing at ± 2 MV/cm was performed at temperatures ranging from 50 °C to 150 °C. The calculated applied electric fields include the appropriate work function differences between Al and Si.

For comparison, similar switched-bias annealing was performed after constant voltage stress. In this case, an electric field of ± 3.6 MV/cm was applied to the capacitors for 1200 seconds at room temperature. The resulting injected charge densities were ~ 10-12 mC/cm^2. This stress level was determined to cause equivalent damage to that produced by irradiation, to first order [57]. The contributions of oxide, interface, and border-trap charge are evaluated, and significant roles are inferred for both metastable electron traps in the near-interfacial dielectric layers and hydrogen transport and reactions at and near the Si/oxynitride interface. The results for these HfO_2 dielectrics are compared to the responses of devices with SiO_2 gate dielectrics in the literature, and physical models of charge buildup and annealing are developed to account for the results.

Post-irradiation Annealing

To explore the mechanisms that lead to the results in Figs. 11-14, alternating negative and positive BTS was applied to the worst-case device (8) in Fig. 14, starting one day after the device was irradiated and stressed at 75 ºC and – 0.3 V. Values of ΔV_{ot} and ΔV_{it} are shown in Fig. 17 for PBTS and NBTS applied first for 600 s, and then for 3600 s. Values of ΔV_{ot} change more than ΔV_{it} during the switched BTS. For NBTS, ΔV_{ot} increases in magnitude; for PBTS, ΔV_{ot} decreases in magnitude.

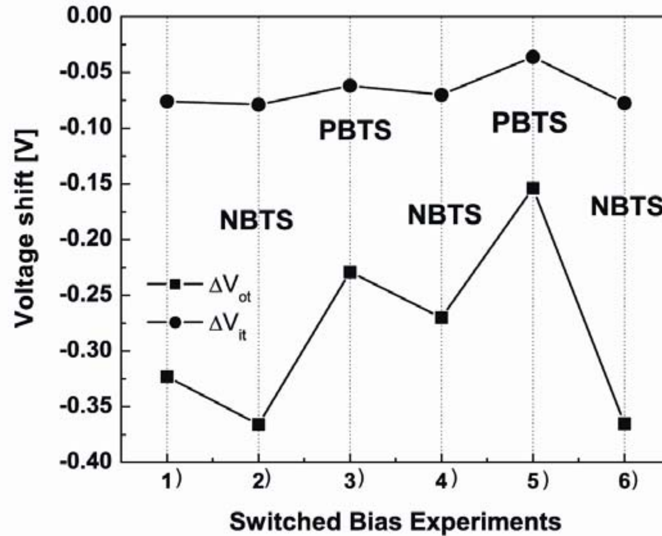


Figure 17 ΔV_{ot} and ΔV_{it} for Al/HfO_2+SiO_xN_y/Si pMOS capacitors for a series of consecutive switched bias experiments on the same devices: 1) NBTS for 600 s after positive bias irradiation to 1.0 Mrad(SiO_2); 2) a second 600 s NBTS after a 24 hour wait while the device was stored with no bias (floating) at room temperature; 3) PBTS for 600 seconds; 4) NBTS for 600 seconds; 5) PBTS for 3600 seconds; and 6) NBTS for 3600 seconds. The gate bias is 0.3 V for all PBTS and - 0.3 V for all NBTS; the stress temperature was 75 ºC. After [92].

The data of Fig. 17 are reminiscent strongly of similar bias switching experiments [52]-[53], [134], [142]-[146] for irradiated thermal SiO_2, as illustrated schematically in Fig. 18. During radiation exposure, both positive and negative charges are trapped in the bulk of the HfO_2; this is also observed in high-field stress

experiments [130]. The data of Fig. 17 show that the positive charge is trapped more stably than the negative charge, since the values of ΔV_{ot} are consistent with electrons being forced out of the oxide during the NBTS, and pulled into the oxide during the PBTS. This suggests that these electrons are located either in shallow traps in the HfO_2, at sites at the HfO_2/oxynitride interface, and/or in the oxynitride layer itself. The similarity of the responses here to those observed in SiO_2 [52]-[53], [134], [142]-[146] suggests that similar defects may be involved (e.g., O vacancies [52]-[53], [134], [142]-[146]). These results demonstrate that significant densities of dipolar defects are created during irradiation in stacks incorporating HfO_2, and that these may impact MOS postirradiation response significantly. A role for hydrogen release in the Si substrate during NBTS after radiation exposure also is likely, as discussed further below, since this process is significant for NBTI in unirradiated devices [5], [74], [88]-[89], and because bias switching effects also are observed on a smaller scale in ΔV_{it} [53], [147].

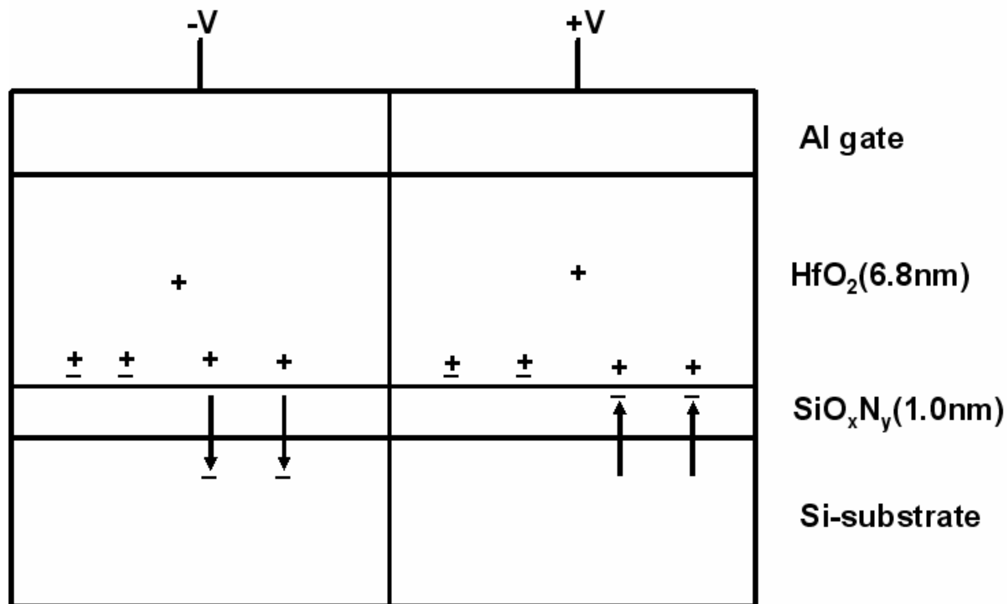


Figure 18 Schematic diagram of the gate stack used here, and electron motion during zero or positive-bias irradiation followed by positive or negative BTS. During PBTS, more electrons compensate trapped positive charge; during NBTS, fewer electrons compensate trapped positive charge. After [92].

The switched-bias annealing experiments were expanded to a fuller temperature range: 50°C ~150°C after positive bias irradiation at 1 Mrad(SiO_2), while maintaining the same stress time interval for the subsequent annealing. Fig. 19 shows results for Al/HfO_2+SiO_xN_y/Si *p*MOS capacitors. The flatband-voltage shifts due to net oxide-trap and interface-trap charge are plotted as a function of switched-bias annealing temperature. The degradation at each bias condition increases with temperature. Values of ΔV_{ot} and ΔV_{it} increase in magnitude for negative bias-temperature stress (NBTS) and decrease in magnitude for positive bias-temperature stress (PBTS). A significant fraction of the reversibility in ΔV_{ot} after irradiation is similar to switched-bias experiments for irradiated thermal SiO_2 [52]-[53], [134], [136]-[138], [142]-[146], [148]. The trend is likely associated primarily with trapping

of both positive and negative charge during the 10-keV X-ray irradiation, the subsequent release of compensating electrons during NBTS, and the return of these electrons into the oxide during PBTS [92]. In this case, the electrons are located either in shallow traps in the HfO_2, at sites at the HfO_2/oxynitride interface, and/or in the oxynitride layer itself, as discussed in Chapter VI, and consistent with previous work on SiO_2 [52], [134], [142]-[146], [148]. It is likely that different defects participate in the enhanced reversibility of charge trapping for these HfO_2 dielectrics than for high quality thermal SiO_2, but O vacancies almost certainly play a key role in the response of each type of device [52], [92], [134], [137], [142]-[146], [148].

The reversibility in ΔV_{it} after irradiation in Fig. 19(b) is more pronounced than is typical for similar irradiation and annealing sequences for thermal SiO_2 [149]-[150]. In particular, the response in Fig. 19(b) cannot be explained easily by the two-stage buildup of interface traps associated with the release of protons in the gate dielectric and their subsequent transport under bias and reaction at the Si/dielectric interface. For this case, interface traps typically are found to build up during positive bias annealing, and stay approximately constant during negative-bias annealing [149]-[150]. However, small amounts of interface-trap buildup and reversibility of interface-trap densities have been observed in switched-bias annealing experiments performed on SiO_2 devices at elevated temperatures [53]. This is seen for cases in which significant densities of trapped positive charge and hydrogenous species are simultaneously present in MOS devices, so these results are qualitatively consistent with the behavior of interface traps in SiO_2 under similar experimental conditions. The reversibility in ΔV_{it} (as well as a portion of the variability in ΔV_{ot}) is attributed to the motion, trapping, and reactions of protons near the Si/dielectric interface, as discussed in detail below. The increase in interface-trap density during negative-bias

annealing in Fig. 19(b) is much larger (relative to the post-irradiation interface-trap density) than is commonly observed in SiO_2, which reinforces that the radiation response of MOS capacitors with high-κ dielectrics can differ significantly from the response of devices with SiO_2 gate oxides.

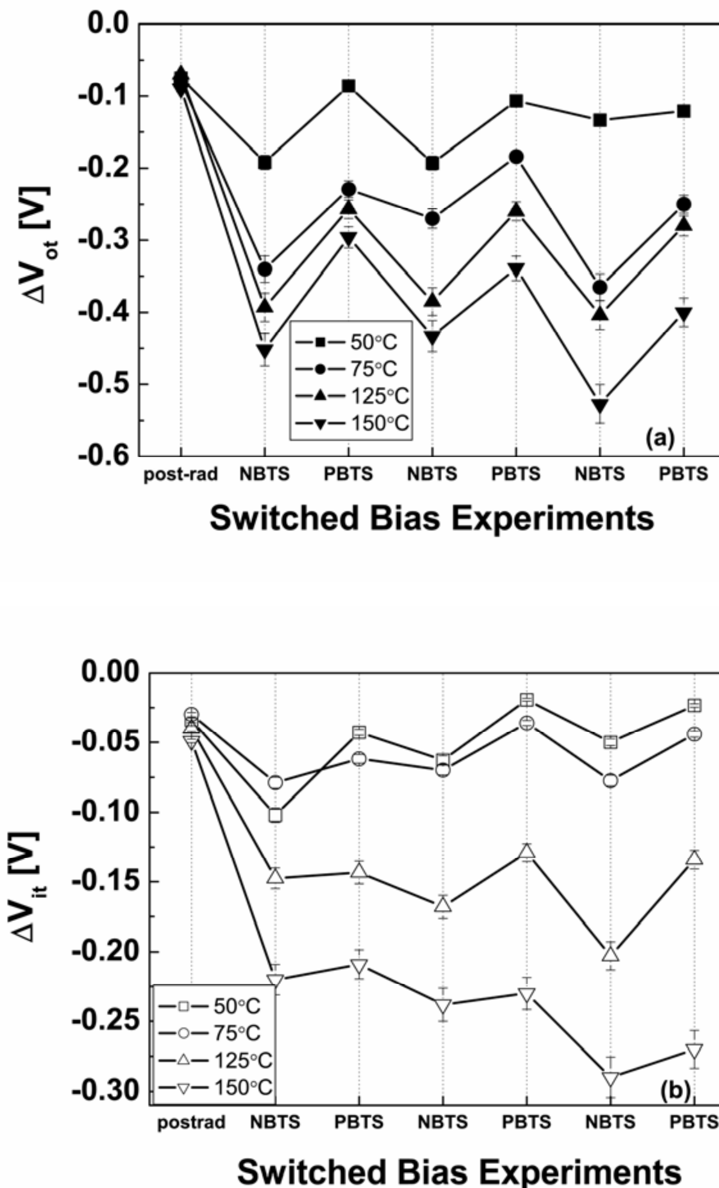


Figure 19 Induced ΔV_{ot} (a) and ΔV_{it} (b) for Al/HfO_2+SiO_xN_y/Si *p*MOS capacitors irradiated to 1.0 Mrad(SiO_2) with 10-keV X-rays, followed by a series of switched bias anneals at 50 to 150 °C. The gate bias for irradiation is 0.3 V. The switched bias anneals are ± 0.3 V (PBTS, NBTS), and the stress time was 600 s each. After [151].

In addition to the reversibility of the voltage shifts in Fig. 19, an overall increase in the magnitude of the degradation is also observed with stress time, especially for higher annealing temperatures. This likely is due to additional damage associated with the increased gate currents during the elevated temperature anneal. The cumulative gate current during the entire stress period was recorded to evaluate this effect. The total injected charge densities were determined as:

$$\frac{Q}{A} = \frac{\int I(t)dt}{A} \qquad (17)$$

Here A is the area of the MOS capacitor, I is the current through the oxide during the switched-bias anneals, and the integral is evaluated over the entire time for which the capacitor is under bias of a given polarity. The integral is evaluated separately for the positive and negative bias sequences.

Fig. 20 shows the injected charge densities during the post-irradiation switched-bias annealing sequences of Fig. 19. The injected charge densities increase with stress time for both NBTS and PBTS in Fig. 20. Injected charge densities increase with increasing temperature, demonstrating that the gate current is not due to pure tunnelling, but includes a more strongly temperature-dependent component. This likely is associated both with the lower barrier against electron injection into HfO_2 from Si than for SiO_2 [15], and to defects in the dielectric layers [152]. The injected charge at 150 °C is 0.9 C/cm^2 after four cycles of switched-bias annealing. After this sequence, the leakage current through the dielectric increases dramatically (corresponding to hard breakdown), consistent with results on thermal SiO_2 with similar defect densities [17], [57], [95], [152]. During the NBTS and PBTS cycles, the oxynitride layer is thin enough for electrons to tunnel through, enabling additional defect creation in the HfO_2, in addition to new trap creation in the interfacial oxynitride and at the interface [95], [152]. At higher temperatures, both electron

exchange and proton motion are enhanced, leading to additional defect creation. This leads to the increasing charge trapping with increasing temperature, in addition to the reversibility discussed above.

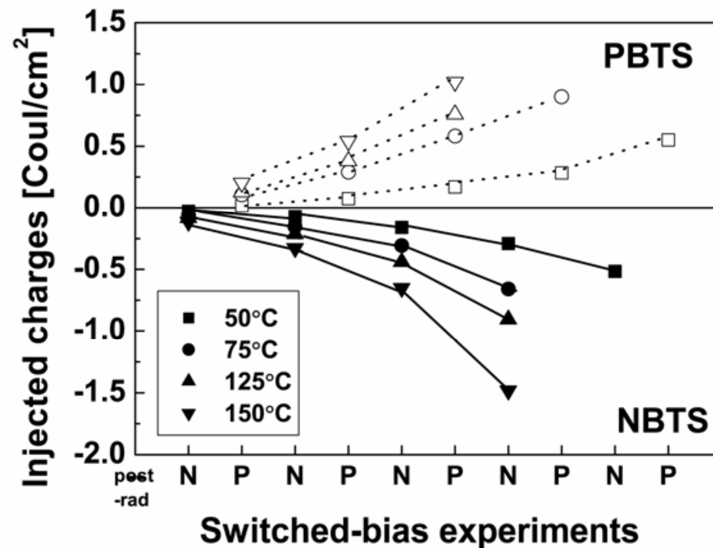
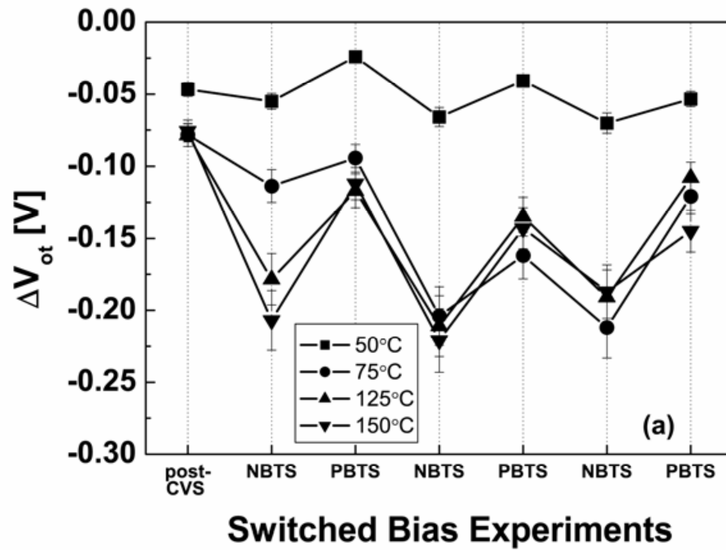


Figure 20 Cumulative injected charge densities for switched-bias annealing at elevated temperatures after irradiation. The capacitor area A = 5.6×10^{-4} cm^2. The experimental conditions are the same as Figure 18. Cumulative charge densities during PBTS are shown in the upper part of the figure, and cumulative charge densities during NBTS are shown in the lower half. These densities do not include the portions of the anneal when the device was in the opposite bias state, so the total charge is obtained by adding the charge densities in the upper and lower halves of the figure. After [151].

Post-constant voltage stress (CVS) Annealing

Fig. 21 shows results after the application of constant voltage stress (CVS) to Al/HfO_2+SiO_xN_y/Si *p*-substrate MOS capacitors. These devices were stressed with ± 2 MV/cm at elevated temperatures up to 150 °C. Although the constant voltage stress is performed at a voltage (0.5 V) that is well below the energy needed to create electron-hole pairs in the oxide, somewhat similar trends are observed in the post-CVS defect buildup and annealing as for the case of irradiation in Fig. 19. Increasing the annealing temperature enhances the buildup of the net oxide-trap charge significantly during the initial period of negative bias annealing, but the reversibility of ΔV_{ot} after this initial increase in magnitude does not depend as strongly on temperature from 75 °C to 150 °C as was the case for the X-ray irradiations in Fig. 19. The changes in ΔV_{ot} and ΔV_{it} are primarily due to proton motion and reactions in response to the applied biases, as discussed below.



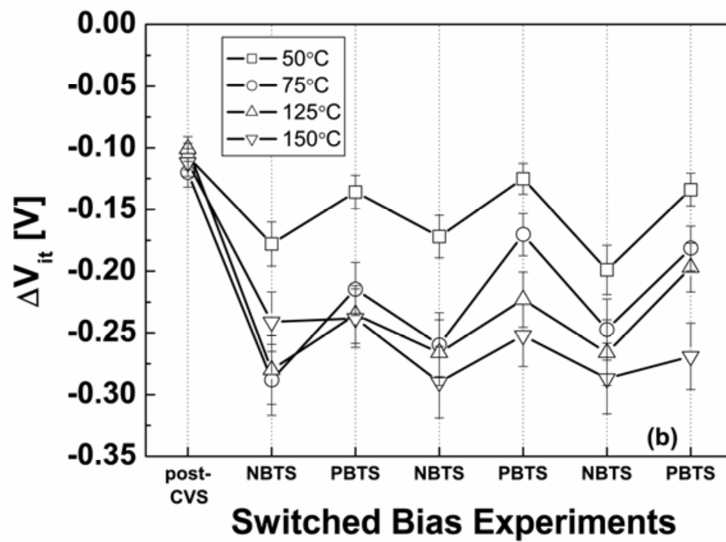


Figure 21 Induced ΔV_{ot} (a) and ΔV_{it} (b) for Al/HfO_2+SiO_xN_y/Si *p*-substrate MOS capacitors stressed at - 3.6 MV/cm for 1200 s followed by a series of switched bias experiments at 50 to 150 °C. The gate bias for constant voltage stress is – 0.5 V. The switched bias anneals are ± 0.3 V (PBTS, NBTS) and the stress time was 600 s each. After [151].

The absence of radiation-induced-hole trapping during the CVS, and the amphoteric nature of interface traps at the Si/SiO_2 interface (leading to two electrically active defect levels for each physical interface trap [48]) cause the interface trap densities to exceed the oxide-trap charge densities in Fig. 21, in contrast to Fig. 19, in which the oxide-trap charge creation dominates. This is illustrated more clearly in Fig. 22, which compares the switched-bias annealing responses at 75 °C for these high-κ devices after irradiation and CVS. More oxide-trap charge than interface-trap charge is created by radiation exposure, and more interface-trap charge than oxide-trap charge is created by CVS for these experimental conditions. Moreover, the damage levels (especially after periods of negative bias annealing) greatly exceed the damage levels immediately after irradiation, consistent with the results in ref [92]. The reversibility in ΔV_{ot} after irradiation is greater than the reversibility in ΔV_{it}; in contrast, the reversibility in ΔV_{it} after CVS is greater than the reversibility in ΔV_{ot}. Note that nearly as much reversibility is observed in the values of ΔV_{it} after CVS as is observed in ΔV_{ot} after irradiation, illustrating that, depending on the amount and type of stress to the device, significant reversibility can be observed in either oxide or interface-trap charge in these high-κ dielectrics. This contrasts with SiO_2 in which the reversibility of oxide-trap charge is typically much greater than the reversibility of interface-trap charge for irradiation or high-field stress [52]-[53], [134], [142]-[146], [148], [153].

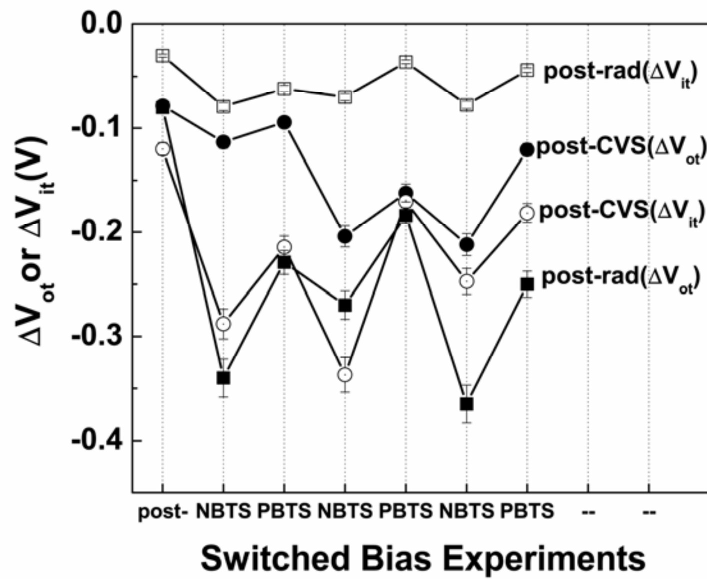


Figure 22 Induced ΔV_{ot} (solid symbols) and ΔV_{it} (open symbols) for switched-bias annealing either after irradiation (squares) or after constant voltage stress (circles). The gate bias for irradiation is 0.3 V and the dose is 1 Mrad(SiO_2). The gate bias for constant voltage stress is – 0.5 V and the stress time is 1200 s. Both irradiation and constant voltage stress were performed at room temperature. The switched biases are ± 0.3 V at 75 °C, and the stress time was 600 s for each time interval (NBTS, PBTS) for both cases. After [151].

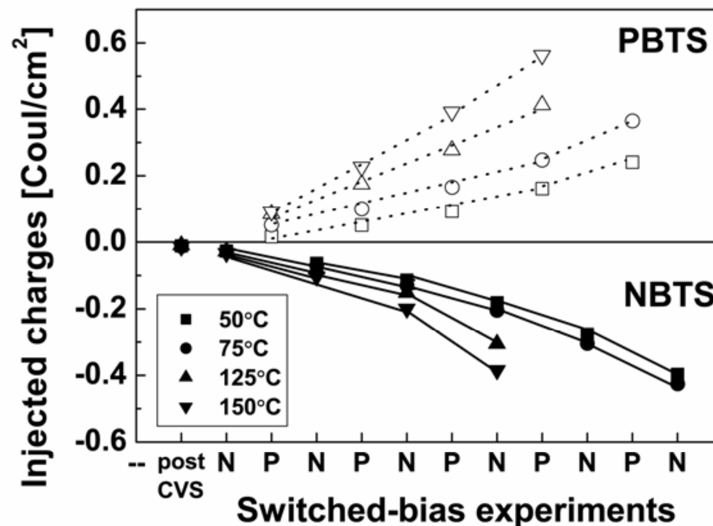


Figure 23 Injected charge densities for switched-bias annealing at elevated temperatures after constant voltage stress (CVS). The experimental conditions are the same as Figure 21. After [151].

Fig. 23 quantifies the increase in injected charge densities during the switched-bias annealing after CVS for the sequence in Fig. 21. Similar trends are observed to those in Fig. 20; that is, with increasing post-CVS switched-bias annealing time and/or increasing temperature, additional charge is injected into the dielectric layers, leading to the increase in defect density with increasing anneal time.

The above trends in charge trapping reversibility and defect growth are also illustrated nicely via multiple switched-bias annealing cycles. Fig. 24 displays a sequence of NBTS and PBTS cycles at 50 °C or 75 °C after constant voltage stress (CVS) to show the evolution in charge trapping with time at two temperatures that are fairly typical of device operating temperatures in practical applications. The same trends of reversibility in ΔV_{ot} and ΔV_{it} are found with increasing magnitudes of the voltage shifts as the switched-bias annealing continues. For example, at the data set for switched-bias annealing at 75 °C, the voltage shifts due to the first negative BTS are –0.06 V for ΔV_{ot} and –0.26 V for ΔV_{it}, respectively. These increase in magnitude to –0.18 V and –0.36 V for ΔV_{it} after 5 cycles of switched-bias annealing. The reversibility of ΔV_{it} is around two times larger than that of ΔV_{ot}. Moreover, ΔV_{ot} and ΔV_{it} are larger in magnitude for switched-bias annealing at 75 °C than 50 °C annealing. Strong reversibility in trapped charge densities occurs, consistent with the trends in Figs. 19 - 23. In addition, there is a general downward trend (upward in magnitude) in the voltage shifts due to new trap creation, associated with increasing cumulative charge injection during the annealing cycles.

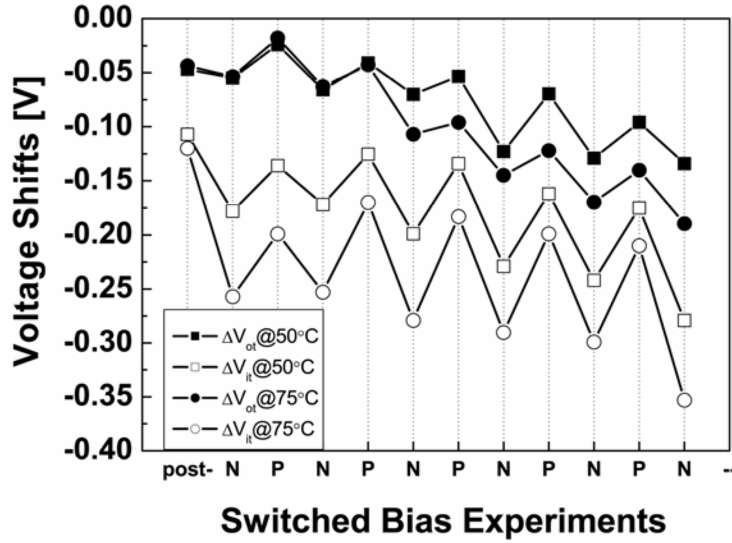


Figure 24 Induced ΔV_{ot} (solid symbols) and ΔV_{it} (open symbols) for switched-bias annealing at 50 °C (squares) or 75 °C (circles) after constant voltage stress. The gate bias for constant voltage stress is –0.5 V and the stress time is 1200 s. Both irradiation and constant voltage stress were performed at room temperature. The switched bias anneals are ± 0.3 V at 75 °C, and the stress time was 600 s for each time interval (NBTS, PBTS) for both cases. After [151].

Physical Mechanisms for Charge Trapping Reversibility

Next, we discuss physical mechanisms for charge trapping reversibility. Figs. 25(a) and (b) illustrate schematically mechanisms that are consistent with the observed degradation in Fig. 19 and Fig. 21. The reversibility in ΔV_{ot} after irradiation is greater than the reversibility in ΔV_{it}; in contrast, the reversibility in ΔV_{it} after CVS is greater than the reversibility in ΔV_{ot}. The enhanced reversibility in ΔV_{ot} for the post-irradiation case is consistent with large densities of both holes and electrons being trapped in the SiO_2 during irradiation [92], illustrated as mechanism (1) in Fig. 25. Such a high level of oxide-trap charge due to electron-hole pair generation and trapping in the insulator is absent in the CVS case, leading to the dominant role of hydrogen reactions, as illustrated by mechanisms (2)-(4).

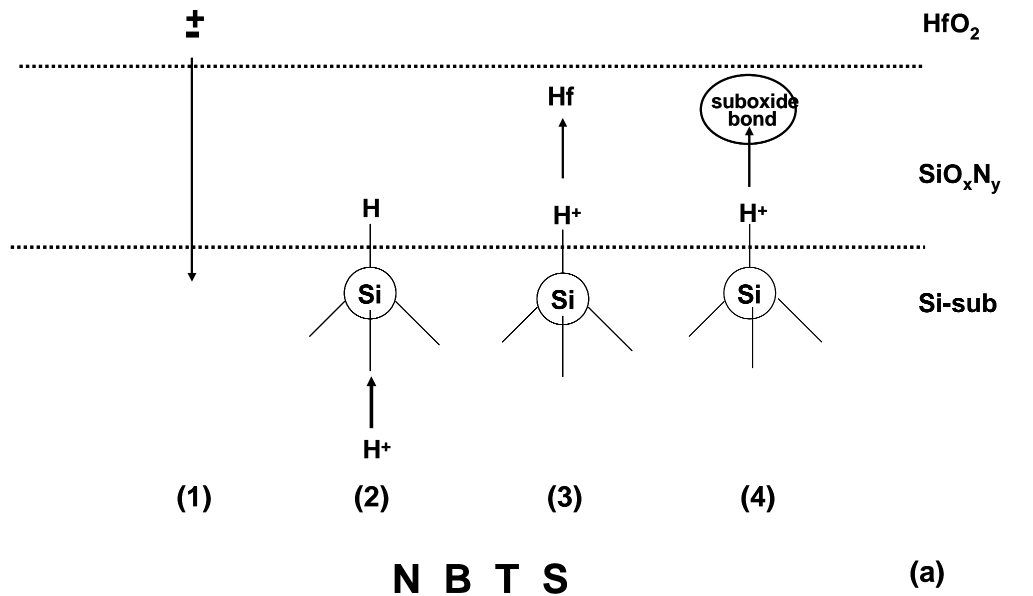
Under negative bias, H^+ drift to the interface from the oxide is inhibited by the applied electric field, and Si dangling bonds are positively charged. In this case, passivation of dangling bonds by H (reaction (18)) is suppressed, since both species are of the same charge.

$$H^+ + Si^- \rightarrow Si\text{–}H. \tag{18}$$

However, the depassivation of passivated dangling bonds can still occur via reaction (19) [100],

$$Si\text{–}H + H^+ \rightarrow Si^+ + H_2 \tag{19}$$

This reaction can lead to an increase of ΔV_{it} in magnitude during the negative bias anneal, if there is a source of hydrogen either directly at the interface or in the Si substrate. Possible sources of hydrogen in p-type Si are B-H complexes [74], [154] or oxygen protrusions [89]. Depassivation of a Si-H bond and the formation of an interface trap via the reaction (19) [98] are illustrated as mechanism (2) in Fig. 25 (a). A similar mechanism has been identified as a contributing factor to negative-bias-temperature instability in MOS devices and for enhanced low-dose-rate sensitivity in linear bipolar transistors [140].



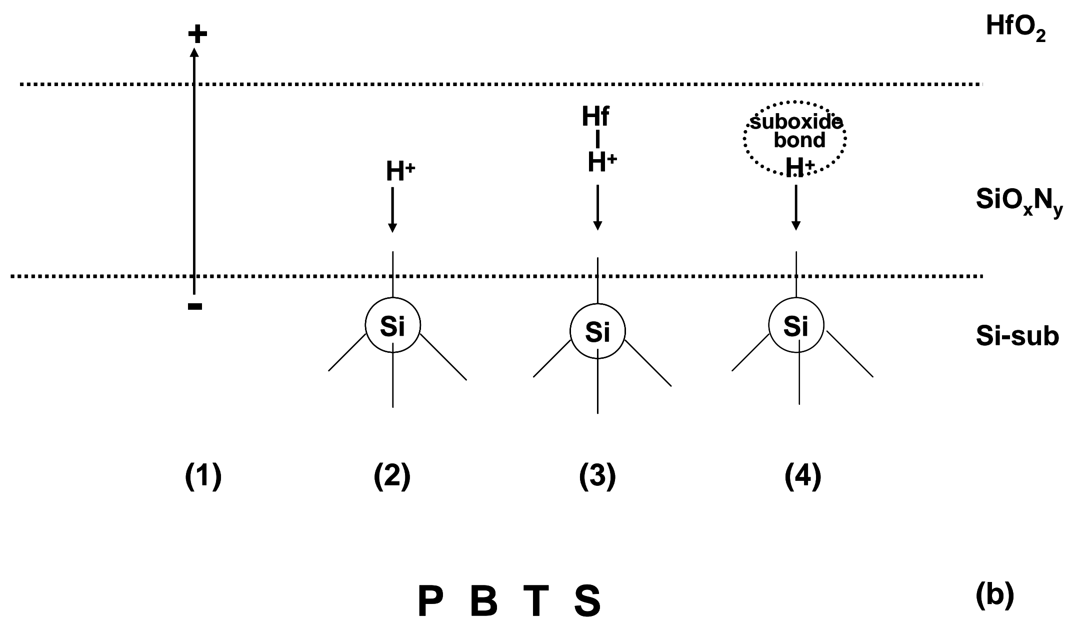


Figure 25 Schematic diagram of the gate stack and involved mechanisms. Electron exchange and proton (H^+) motion are depicted during negative BTS (a) or positive BTS (b). Mechanism (1) dominates during switched-bias annealing after irradiation, while mechanisms (2)-(4) dominate during post-CVS annealing. During NBTS, electrons are pulled back into the substrate after irradiation (mechanism 1(a)). H^+ can either depassivate a Si-H bond (mechanism (2a)) or be pulled off the Si-H bond when there is a spatially co-located suboxide bond (O vacancy), Hf atom, or other similar defect nearby that provides a trapping site for the proton, leaving behind a Si dangling bond that functions as an interface trap (mechanism (3a)-4(a)). During PBTS, electrons move into the oxide after irradiation (mechanism 1(b)). H^+ also is attracted to and passivates Si dangling bonds near the interface (mechanisms (2b)-(4b)). After [151].

Other mechanisms breaking Si-H bonds likely contribute to the increase in magnitude of oxide-trap charge and interface-trap charge under negative bias in Fig. 19 and Fig. 21, as also shown schematically in Fig. 25(a) (mechanisms (3) and (4)). If it is energetically favorable for the Si–H bond to break under negative bias, a proton can be released, which leads to the formation of an interface trap and an available H^+ that can be trapped in the dielectric layer. Density-functional-theory calculations have shown that simple thermally assisted Si–H bond breaking is highly improbable for a passivated dangling bond at an otherwise defect-free (at least in the vicinity of the Si–H bond) interface under normal device operating conditions [74]. However, at simultaneously elevated temperature and a significant, applied electric field, in the presence of a nearby defect or impurity atom, it is likely that the binding energy of the H atom would be reduced.

There are at least two plausible candidates for a defect or impurity that can both facilitate the breaking of the Si–H bond and serve as a trapping site for the proton that is released in these devices. One candidate is an impurity Hf atom in the near-interfacial oxynitride (mechanism (3) in Fig. 25(a)). Density-functional-theory calculations show that isolated Hf atoms can be incorporated into the SiO_2 interlayer between the HfO_2 gate dielectric and the Si substrate during rapid thermal annealing [155]. This phenomenon was observed in scanning transmission electron microscopy studies [156] that reveal a density of Hf atoms in the SiO_2 interlayer at a high enough level (areal density of ~ 10^{13} cm^{-2}) to contribute significantly to the processes in Fig. 25. Moreover, density-functional-theory based mobility calculations have found a significant degradation of mobility due to the large densities of neutral Hf atoms in the oxynitride interlayer [157]. The growth of HfO_2 via atomic layer deposition and the subsequent annealing process also can produce more suboxide bonds near the

interface with Si [158], owing to the effective "gettering" of a significant fraction of the O atoms in the oxynitride layer into the HfO_2. The Hf atoms (mechanism (3) in Fig. 25(a)) or suboxide bonds (mechanism (4) in Fig. 25(a)) in the near-interfacial oxynitride, can serve as proton traps under negative bias [140], and can release the protons to repassivate the Si dangling bonds under positive bias. That similar activation energies for BTS are observed in HfO_2 dielectrics with oxynitride interfacial layers and capacitors with thermal SiO_2 suggests that the suboxide bond mechanism may dominate this process [89], [101], [159]-[160].

Under positive bias, the decrease in ΔV_{it} is attributed to the passivation of negatively charged Si dangling bonds by protons. The protons can either be released and transport from the oxide, or be released from Hf-H or suboxide bonds, illustrated by mechanisms (2)-(4) in Fig. 25(b). In this case, there is a relatively large initial density of Si dangling bonds and a relatively high concentration of protons in the near-interfacial SiO_2, since HfO_2 is a weak diffusion barrier for hydrogenous species [161]. The transporting protons have a higher probability in this case to passivate a pre-existing defect (a negatively charged Si dangling bond) via the simple reaction (18) than to depassivate a Si-H bond and form an interface trap via reaction (19) [98], [100]. A similar mechanism has been observed to lead to a decrease in ΔV_{it} during irradiation for some high-κ dielectrics [13], emphasizing the plausibility of this mechanism in these kinds of devices. Once the defect is passivated by hydrogen, it no longer functions as an interface trap, therefore reducing ΔV_{it} in magnitude. This leads to an increase in magnitude of both ΔV_{ot} and ΔV_{it} during NBTS (more trapped protons in the oxide; more unpassivated dangling bonds), and a decrease in magnitude of ΔV_{ot} and ΔV_{it} during PBTS (fewer trapped protons in the oxide; fewer dangling bonds), consistent with the trends in the data of Fig. 19 and Fig. 21. Because there are two

defect levels for each interface trap [48], the measured value of ΔV_{it} during a C-V sweep can exceed that of ΔV_{ot} by up to a factor of two, consistent with the post-CVS results in Fig. 21. Hence, the results of Fig. 19 and Fig. 21 illustrate the competition that can occur between interface-trap buildup and passivation in devices with moderate to high interface-trap densities during irradiation and/or postirradiation annealing. The process that dominates is determined by the initial defect densities, concentrations of hydrogenous species, bias, time, dose, temperature, humidity, etc [38], [53], [99], [120], [147], [162]-[163].

Contributions from Border Traps

Because border traps can sometimes be mistaken for interface traps, I have checked the relative significance of border traps in these devices by measuring C-V hysteresis as a function of voltage ramp rate [53], [57]-[58]. The value of ΔV_{bt} is calculated from the following equations:

$$\Delta V_{bt} = \frac{\Delta N_{bt} q}{C_{ox}} \tag{20}$$

and

$$\Delta N_{bt} = \frac{\int \left| C_{reverse}(V) - C_{forward}(V) \right| dV}{qA} \tag{21}$$

These results are shown in Fig. 26, which were obtained after several of the irradiation and annealing sequences in Figs. 19 and 21. These border traps may be either in the HfO_2 layer or the near-interface oxynitride/Si interface. While some border traps are present, under the experimental conditions used to estimate the values of ΔV_{it}, the changes in ΔV_{it} in Figs. 19 and 21 are much larger than would be expected from at least the slower border traps that contribute to C-V hysteresis in Fig. 26.

Because similar trends in interface-trap density have been observed in previous studies of switched-bias annealing for SiO_2-based MOS transistors in studies in which the effects of border traps and interface traps were separated using charge pumping techniques [58], it appears quite plausible that the effects observed in Figs. 19 and 21 are indeed due to interface traps.

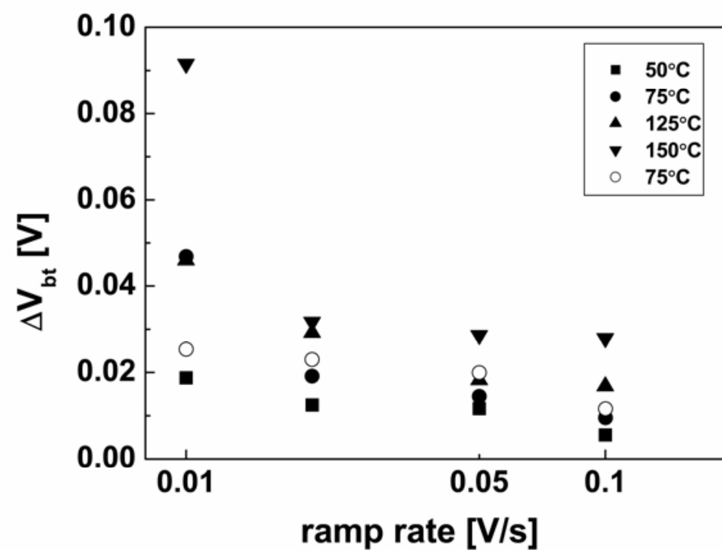


Figure 26 ΔV_{bt} for Al/HfO_2+SiO_xN_y/Si *p*-substrate MOS capacitors after post-irradiation switched-bias annealing (solid symbols) at room temperature, 75 °C, 125 °C, and 150°C for the devices of Fig. 19, at the conclusion of the measuring sequence. The open symbols represent ΔV_{bt} induced by switched bias annealing at 75 °C after constant voltage stress (same stress time as in Fig. 21). After [151].

CHAPTER VIII

CONCLUSIONS

In summary, similar activation energies for oxide-trap and interface-trap charge formation due to NBTI in MOS capacitors with SiO_2 and SiO_xN_y/HfO_2 gate dielectrics have been observed. This defect formation was originally attributed to H^+ release from oxide protrusions in the near-interfacial Si, its diffusion along the Si/dielectric interface, followed by its reaction with Si-H to form interface traps, or its capture at a sub-oxide bond to form positive oxide-trap charge. Later theoretical calculations show the activation energy based on quasi-equilibrium reactions is in agreement with the experimental values, and a possible source of hydrogen could be from dopant sites in the depletion region of the Si substrate. These results are consistent with the key roles played by hydrogen in MOS defect formation in MOS radiation response and long-term reliability, and suggest that minimizing excess hydrogen and O vacancies may help to reduce NBTI.

Detailed studies of radiation response on capacitors with HfO_2- and Al_2O_3-based MOS capacitors show that positive bias irradiation on HfO_2 and negative bias irradiation on Al_2O_3 dielectrics have largest voltage shifts and degradations when compared with other bias irradiations.

For each type of high-κ device: capacitors with HfO_2- and Al_2O_3- dielectrics, the combined effects of irradiation and BTS can be significantly greater than either alone, or than linear combinations of the two types of stresses. Significant densities of dipolar charge are trapped in the high-κ dielectric layers during irradiation, with the negative charge being less stable during bias-temperature stress than the positive charge. Worst-case responses in combined irradiation and BTS environments are

positive (or zero) bias irradiation followed by NBTS for the HfO_2 based devices, and negative-bias irradiation followed by NBTS for the Al_2O_3 based devices investigated in this study. Hardness assurance tests that include irradiation and bias-temperature annealing may be used to predict the long-term radiation response and reliability of these devices, as long as worst-case conditions are properly identified and selected during device testing.

Detailed investigations of switched-bias annealing as a function of time and temperature after irradiation and constant voltage stress were performed on capacitors with HfO_2-based MOS capacitors. For both cases, significant reversibility of oxide-trap and interface-trap charge densities is observed. After irradiation, the dominant source of reversibility in the charge trapping is metastable electron traps associated with radiation-induced trapped positive oxide charge in the near-interfacial dielectric layers. After constant voltage stress, the motion, reactions, and trapping of protons at or near the Si/oxynitride interface are much more significant to the observed device response. Much of the correlated increases and decreases in oxide-trap charge and interface-trap charge during switched-bias annealing are attributed to protons alternatively becoming trapped at a suboxide bond or a Hf atom in the near-interfacial oxynitride layer (negative bias), and passivating a Si dangling bond at the interface (positive bias). The enhanced relative importance of proton effects during the CVS stress is a result of reduced electron-hole pair creation during low-energy constant-voltage stress, as compared to the high-energy X-ray irradiation. Additional defect growth with time was observed as a result of additional charge injection through the gate stack, during the annealing process. This defect growth increases significantly with increasing stress time and temperature. These results illustrate that positive oxide-trap charge, electron traps, and protons play significant roles in the ionizing

radiation response and long-term reliability of MOS devices with high-κ gate dielectrics. While these results are qualitatively similar to effects observed in thermal SiO_2, the magnitudes of the effects are much larger in these devices, leading to a corresponding increase in their relative significance. This work confirms that combined radiation and long-term stress environments can be quite challenging for alternative high-κ dielectrics to SiO_2, and that (absent significant processing improvements in the future) additional testing margins will be required for these kinds of devices, relative to margins used for SiO_2 gate dielectrics.

APPENDIX

A Control code # 1: For bias temperature stressing

PERL is open source software and originally developed for Unix and its variants, such as Linux. It is a stable, powerful, cross-platform programming language that does not need a compiler. Below is the script written in PERL to control the bias-temperature stressing procedure. All I need to do is run .NBTI.pl under the home/xing directory.

```
#!/usr/bin/perl

# Input required experimental parameters
$TEMPINC=1;
#get user input
print "enter desired temperature (25 C to 350 C)\n";
chop($TEMP=<STDIN>);

print "enter the reset temperature (23 C)\n";
chop($RESET=<STDIN>);

print "enter a filename for the data\n";
chop($FILENAME=<STDIN>);

print "enter a bias for the sample\n";
chop($BIAS=<STDIN>);

print "enter a time to hold the bias on the sample for NBTI test
(sec)\n";
chop($HOLDTIME=<STDIN>);

$I=0;
$LOOP=0;
$CYCLES=1;
#here is the main loop
while ( $I < $CYCLES )
{
    #here is the initialization of the equipment

    #setup the 4140
    $foo=`./volt $BIAS`;
    $foo=`./read | tail -c 10`;

    #setup the temp controller
    $AMBIANT=`./write "#01R00"| cut -d C -f 1|tail -c 4`;
    $foo=`./write \"#01M01 $TEMP\"`;
    $foo=`./write \"#01M11 360\"`;
    #setup the file
    open(OUTPUT_FILE, ">./data/$FILENAME");
    $INITIME=`date +%s`;
```

```
    $DISTIME=`date +%c`;
    print OUTPUT_FILE
"$FILENAME\t$DISTIME\tbias=$BIAS\ttime=$HOLDTIME (s)\n\n";

 #  Current monitoring and temperature control
    $ITEMP=`./write "#01R00"| cut -d C -f 1|tail -c 4`;
    while ( $ITEMP < $TEMP )
    {
      $CURSUM=0;
      $TEMPSUM=0;
      while ( $LOOPTEMP < $ITEMP+$TEMPINC )
      {
          $LOOP++;
          $ONE=`./read`;
          ($ONE1,$ONE2)=split(/,/,$ONE);
          ($ONE3,$ONE4)=split(/I/,$ONE1);
          $ONE=$ONE4;
          $TWO=`./write "#01R00" |cut -d C -f 1|tail -c 4`;
          $CURSUM=$CURSUM+$ONE;
          $TEMPSUM=$TEMPSUM+$TWO;
          $LOOPTEMP=`./write "#01R00" |cut -d C -f 1|tail -c 4`;
      }
      $CURAVG=$CURSUM/$LOOP;
      $TEMPAVG=int($TEMPSUM/$LOOP);
      $CURTIME=`date +%s`;
      $COUNTIME=$CURTIME-$INITIME;
      $OUTTIME=`./sec_conv.pl "$COUNTIME"`;
      print OUTPUT_FILE "$OUTTIME\t$TEMPAVG\t$CURAVG\n";
      print "$OUTTIME   $TEMPAVG degrees C      $CURAVG amps $LOOP
samples\n";
      $CURAVG=0;
      $TEMPAVG=0;
      $ONE=0;
      $TWO=0;
      $CURSUM=0;
      $TEMPSUM=0;
      $LOOPTEMP=0;
      $LOOP=0;
      $OUTTIME=0;

      $ITEMP=`./write "#01R00" | cut -d C -f 1|tail -c 4`;
    }
    $STARTHOLD=`date +%s`;
    $STOPHOLD=$STARTHOLD+$HOLDTIME;
    while ($ITIME < $STOPHOLD)
    {
      system("sleep 5");
      $LOOP++;
      $ONE=`./read`;
      ($ONE1,$ONE2)=split(/,/,$ONE);
      ($ONE3,$ONE4)=split(/I/,$ONE1);
      $ONE=$ONE4;
      $TWO=`./write "#01R00" |cut -d C -f 1|tail -c 4`;
      $CURSUM=$CURSUM+$ONE;
      $TEMPSUM=$TEMPSUM+$TWO;
      $LOOPTEMP=`./write "#01R00" |cut -d C -f 1|tail -c 4`;
      $CURAVG=$CURSUM/$LOOP;
      $TEMPAVG=int($TEMPSUM/$LOOP);
      $CURTIME=`date +%s`;
      $COUNTIME=$CURTIME-$INITIME;
      $OUTTIME=`./sec_conv.pl "$COUNTIME"`;
```

```
      print OUTPUT_FILE "$OUTTIME\t$TEMPAVG\t$CURAVG\n";
      print "$OUTTIME   $TEMPAVG degrees C      $CURAVG amps $LOOP
samples\n";
      $CURAVG=0;
      $TEMPAVG=0;
      $ONE=0;
      $TWO=0;
      $CURSUM=0;
      $TEMPSUM=0;
      $LOOPTEMP=0;
      $LOOP=0;
      $OUTTIME=0;
      $ITEMP=`./write "#01R00" | cut -d C -f 1|tail -c 4`;
      $ITIME=`date +%s`;
    }

    #cool
    $foo=`./write \"#01M01 $RESET\"`;
    $foo=`./write \"#01M11 020C\"`;
    while ( $ITEMP > $RESET )
    {
      $ITEMP=`./write \"#01R00\" | cut -d C -f 1|tail -c 4`;
        system("sleep 2");
    }
    #Delay at the min temp
    $foo=`./volt 0`;
    system("sleep 6");

    $I++;
    $FILENAME=$FILENAME.$I;
    system("unix2dos OUTPUT_FILE");
}
```

APPENDIX

B Control code # 2: For C-V measurements:

This program is written in the C programming language and can be used to measure high-frequency (1 M Hz) C-V characteristics before pre and post-stress.

```
#include "ugpib.h"
#include <stdio.h>
#include <unistd.h>
#include <string.h>
#include <stdlib.h>

#define PAD4275a 3
#define SAD4275a 0
#define DELAY 100000

void send(int ud,char *command)
{
    ibwrt(ud,command,strlen(command));
}

int main(int *argc,char *argv[])
{
    float volt,vstart=-1,vstop=1,vstep=0.5;
    int fd, c;
    char setvolt[300],voltstr[300];
    int doutput[300],output[12],outstr[200];
    double delay;
    float freq;
    char setfreq[300],freqstr[300],numsampstr[300],setnumsamp[300];
    int bm,numsamp;
    int id,rd,handle,ud;
    short lnf;
    char readbuf[100000];
    char* charpoint,*endpoint;
    char trace[100];
    handle=ibfind("gpib0");
    ibpad(handle,0);
    ibrsc(handle,1);
    ibsic(handle);
    ibsre(handle,1);
    ud=ibdev(0, PAD4275a, SAD4275a, 13, 1, 0);

    vstart=(float)atof(argv[1]);
    vstop=(float)atof(argv[2]);
    vstep=(float)atof(argv[3]);

    /* start the meat of the code */
    /* initialize the measurement */
        send(ud,"*rst\n");
        send(ud,"*cls\n");
      send(ud,"A2B1C3D0F17H1I0M2R31S0T1");/*Frequency can be changed/
```

```
    /* do the cv loop */
    if(vstart > 0)
    {
    for (volt=vstart;volt>vstop-.0001;volt=volt+vstep)
    {
      sprintf(voltstr,"%2.2f",volt);
      strcpy(setvolt,"BI");
      strcat(setvolt,voltstr);
      strcat(setvolt,"E00V\n");
      send(ud,setvolt);
      usleep(DELAY);
      bm=0;
        strcpy(output,"                                      ");
      strcpy(readbuf,"\0");
//        ibrd(ud,&output,36);
      ibrd(ud,readbuf,36);
      printf("%f\t",volt);
//    printf("%s",output);
      charpoint=readbuf;
      while((*charpoint!='+')&&(*charpoint!='-'))
          charpoint++;
      endpoint=charpoint;
      while(*endpoint!=',')
          endpoint++;
      *endpoint='\0';
      printf("%s\n",charpoint);

    }
      send(ud,"BI000E00V\n");
    }
    if (vstart < 0)
    {
    for (volt=vstart;volt<vstop+.0001;volt=volt+vstep)
    {
      sprintf(voltstr,"%2.2f",volt);
      strcpy(setvolt,"BI");
      strcat(setvolt,voltstr);
      strcat(setvolt,"E00V\n");
      send(ud,setvolt);
      usleep(DELAY);
      bm=0;
        strcpy(output,"                                      ");
      strcpy(readbuf,"\0");
//        ibrd(ud,&output,36);
      ibrd(ud,readbuf,36);
      printf("%f\t",volt);
//    printf("%s",output);
      charpoint=readbuf;
      while((*charpoint!='+')&&(*charpoint!='-'))
          charpoint++;
      endpoint=charpoint;
      while(*endpoint!=',')
          endpoint++;
      *endpoint='\0';
      printf("%s\n",charpoint);

    }
      send(ud,"BI000E00V\n");
    }
}
```

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