Single-Event Characterization of Flip-Flops after Total Ionizing Dose Exposures for a 20-nm Bulk, Planar Technology

By

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Chapter I. Introduction

Space electronics are exposed to numerous radiation sources in the harsh environment, such as solar wind and cosmic radiation. Electrons, protons, and heavy ions are emitted from these sources and can impact the performance of the electrical systems. There are two primary ways the particles may disrupt performance of the systems, Single-Event Effects (SEE's) or Total Ionizing Dose (TID). SEE's are caused by a single energetic particle and results in an erroneous response in the electronic device. A common SEE is a Single-Event Upset (SEU), or an abrupt change in stored data, and this is the primary data point that was tracked in this study. TID measures the amount of radiation the circuitry on the system has accumulated over time. Effects of TID include increased device leakage currents and decreased functionality.

Devices, after undergoing exposure to a radiation dose, undergo a current annealing process, which is the device's attempt to return to normal operation, or operation when no TID is present. In space, however, TID exposure, SE irradiation, and annealing happen concurrently, which is difficult to model in real time experimentally. Thus, this study was modeled after a previous work where chips were exposed to different TID levels first, and the current and SEU's were tracked after the TID exposure but with an SE radiation source.

Chapter II of this thesis covers background information about SEE's and TID, current annealing, and previous work done regarding these topics. The test circuit design and the experimental setup are discussed in Chapter III. Chapter IV displays and analyzes the results, and Chapter V draws conclusions from the findings in the experiments. Appendices at the end contain tables and scripts compiled to make the results understandable.

Chapter II. Background

For older technologies, the charge trapping in the gate insulators was of paramount importance as it directly affected the threshold voltage and leakage current characteristics of individual transistors. For advanced technology nodes, the gate insulator thicknesses are usually shorter than the diffusion length, eliminating effects of trapped charges on threshold voltage of individual transistors [1]. Instead, the charges trapped in the trench isolation regions affect transistor currents by increasing leakage currents across trench oxide regions [2,3]. Single-event effects (SEE), on the other hand, are caused by individual ions traversing the semiconductor region.

Radiation Environments

The general purpose of this work is to see how the technology will be impacted by high levels of radiation in space. Electronics outside of the Earth's atmosphere are subject to various ionizing particles: protons, electrons, alpha particles, and heavy ions [4]. One source of these particles is galactic cosmic rays (GCR's), which contain the highest-energy particles in the solar system. These are emitted from outside the solar system. Another source of radiation is from the sun itself, coming from solar wind. The third source is from the Van Allen belt, which are energetic particles that come from within Earth's magnetic field [5].

Single-Event Effects

A single-event effect (SEE) is triggered by the passage of a high-energy particle through the active region of that device. Heavy ions, protons, and alpha particles are primarily responsible for SEE's. Effects range from hard, permanent damage (such as single-event related gate rupture) to soft, transient damage (such as single-event upset in memory cells) [6]. The SEE's of concern are single-event upsets (SEU's), a soft SEE.

An SEE may cause carriers to go through one of the following mechanisms: recombination, drift, or diffusion. Fig. 1 displays how the carrier can be affected in these ways because of a single event strike in a bulk silicon transistor.

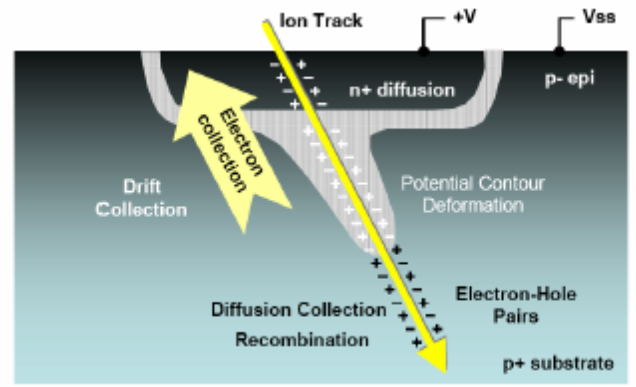


Fig. 1. A diagram of the charge collection mechanisms caused by a single event strike [6].

Rate of charge collection and the amount of charge collected by a circuit node mainly determine the impact of an SEU. Drift and diffusion processes account for charge collection at a circuit node after an ion strike. Drift processes are a strong function of electric field and electron and hole mobilities, whereas diffusion processes are determined by carrier density gradient and electron and hole mobilities.

Total Ionizing Dose Effects

Total Ionizing Dose (TID) effects are the cumulative damage done by lengthy exposure to ionized radiation. This is mainly due to electrons and protons from solar flares and the South Atlantic Anomaly (SAA), where Earth's magnetosphere dips closest to earth, resulting in more trapped radiation. Figure 2 depicts the phenomenon that is the SAA.

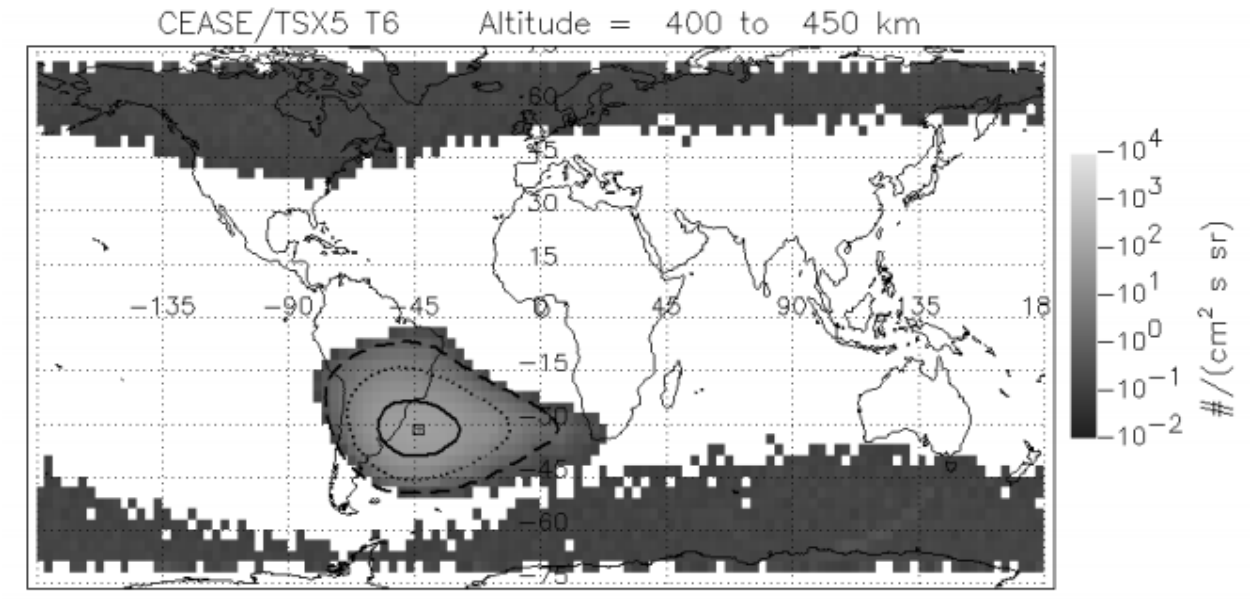


Fig. 2. This diagram of the South Atlantic Anomaly shows the flux intensity map for the > 38 MeV channel at 400 km altitude [7].

The passage of such a high-energy particle through active regions of a transistor results in electron-hole pair generation through coulombic interactions along the track [6]. Charge collection at circuit nodes due to drift and diffusion mechanisms cause voltage perturbations at circuit nodes, resulting in loss of data at those nodes. Figures 3a through 3d display the process of electron-hole pair generation in a semiconductor device.

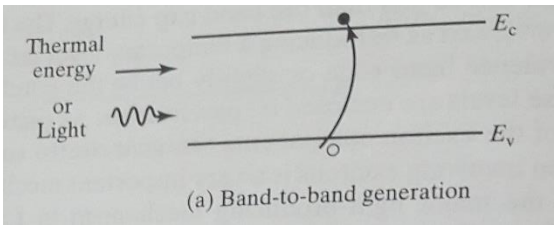


Figure 3a. Electron-hole pair generation via thermal energy or light [8].

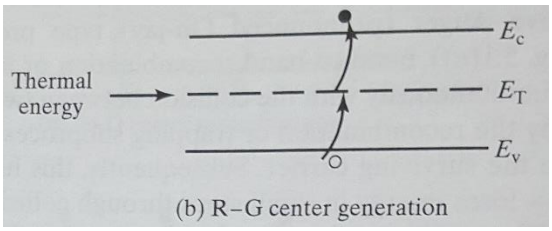


Figure 3b. Electron-hole pair generation via R-G centers acting as intermediaries [8].

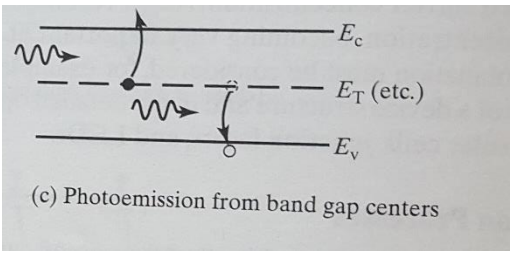


Figure 3c. Electron-hole pair generation via photoemission from band gap centers [8].

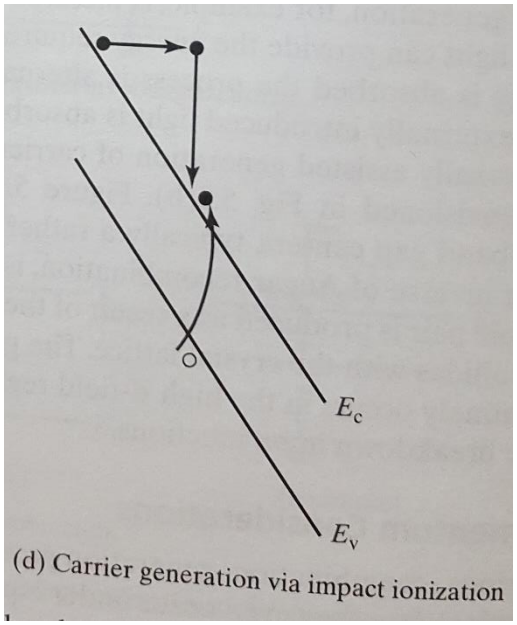


Figure 3d. Electron-hole pair generation via impact ionization [8].

Increased leakage currents across trench isolation regions due to TID exposure reduce current available for charging and discharging of nodal capacitances in logic circuits [2,3]. As a result, the circuits start to experience increased delays for logic gates. In addition, the reduced available transistor current due to TID exposure results in longer single-event transient pulse widths. Increased circuit-level delays will reduce SE vulnerability, but reduced transistor currents will increase the SE vulnerability [4]. These competing mechanisms must be evaluated for all circuits bound for space environment to ensure electronic systems meet their target specification over their lifetime.

Annealing

During and after exposure to radiation, a device will try to resume normal operating conditions, or zero-radiation conditions. During and after exposure to radiation, annealing effects will repair some damage due to total dose. Annealing may reverse increases in leakage currents. This work looks at any effects annealing may have on total dose and single-events sequentially.

Previous Experimental Work

Previous work done at Vanderbilt University looks at synergetic effects of total dose on SEU and SET performance of 40-nm sequential circuits [9]. The 40-nm technology has the same shift register design that the 20-nm technology studied in this work, discussed in the next section. The previous work also used the same methodologies, such as the same irradiation sources and input voltages. Figures 4 and 5 show typical trends in leakage current after exposure to TID and after annealing.

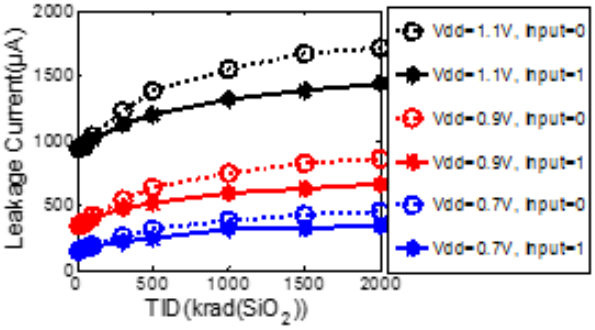


Fig. 4. Static supply leakage currents with TID are shown for 40-nm dies [9].

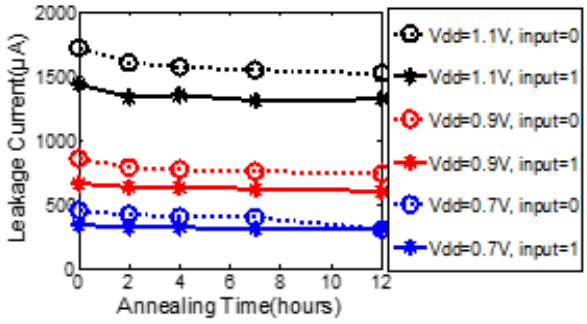


Fig. 5. Room temperature (all grounded) annealing, showed a decrease in leakage current for 40-nm dies [9].

SEU-induced soft errors versus TID were also studied, which is also looked into in this work. Not only is the general SEU over time studied, but also the SEU counts during the annealing period. As Figure 6 shows, there is a general increase in the error counts as TID increases. However, annealing does not appear to significantly impact the single-error rate (SER).

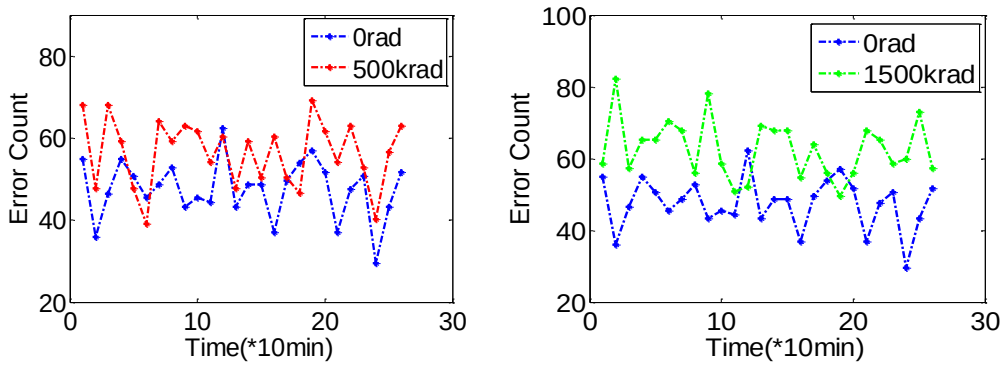


Fig. 6. SEU error count are displayed over time for two different dose exposures. There are no apparent trends over the annealing period, but there appear to be higher error counts for higher dose exposures.

Chapter III. Experimental Design

Test IC Design

A test IC was fabricated at the 20-nm bulk, planar CMOS technology node using a commercial foundry. The test IC was designed using a variety of flip-flop (FF) cells ranging from unhardened, conventional DFF to hardened DICE FF designs. These FF cells were used in a Circuit for Radiation Effects Self-Test (CREST) configuration using an 8K stage shift register, as shown in Figure 7. There were 24 different FF designs used on the test IC with varying levels of SE radiation tolerance. All support circuits other than the shift register used triple-modular redundancy (TMR) to eliminate errors due to ion hits on support circuits. Errors were detected using an on-chip error detector for high frequency operation. On-chip PLL capable of operating at 3 GHz frequency was also designed. For this technology, the nominal core supply voltage was assumed to be 900 mV and the input-output (IO) power supply voltage was assumed to be 1.8 V. Throughout the tests, the voltages used were generally 0.894 V for the core supply voltage and 1.8 for the IO power supply voltage.

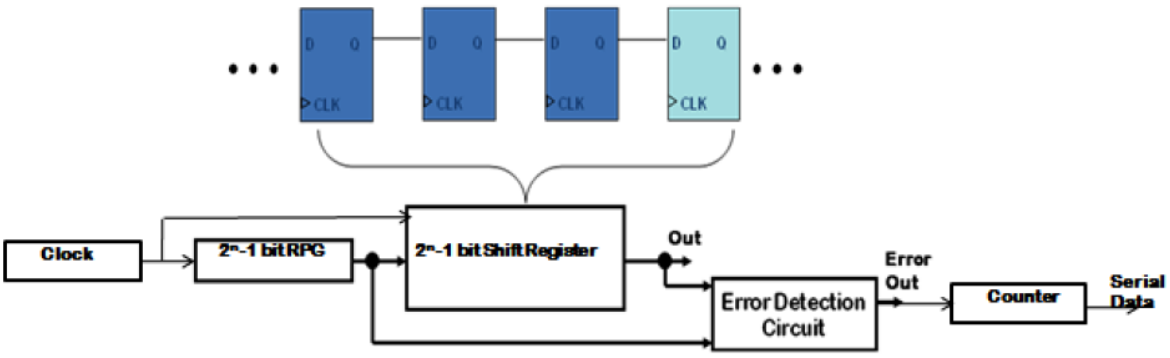


Figure 7. CREST block design of flip-flops with all sub-circuits [10].

Experimental Setup

Summary

A total of five dies were used in the experiments. Table 1 displays the die numbers associated with the radiation levels. During SE tests (and during TID exposures), the input to the shift register was fixed at a logic HIGH level. This will ensure that all ion hits on clock tree will not result in an error. The shift register was clocked from an external clock generator using 2.5 MHz frequency. This was to ensure that shifts in clock frequency due to TID effects on PLL does not affect SE results (SE cross-sections are a strong function of operating frequency [11]). A ring oscillator (RO) circuit comprising of 250 stages was also monitored to evaluate effects of TID on individual logic gate delays. During TID exposure, all power supply currents and the ring oscillator frequency were constantly monitored.

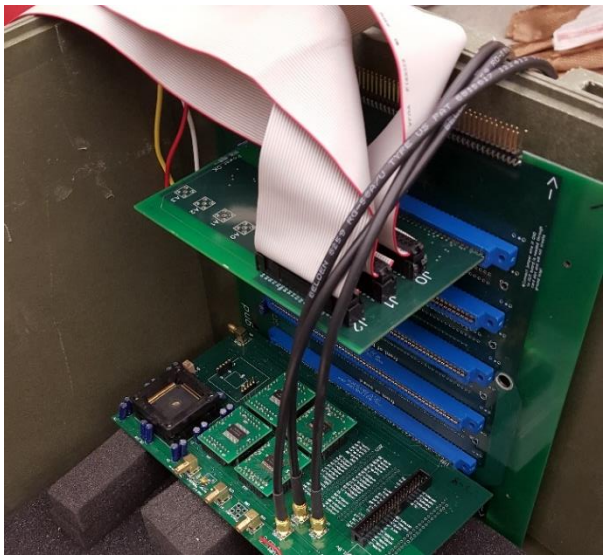
Table 1. TID Irradiation Levels for Different Test ICs.

Chip #	1	2	3	4	5
Die #	2-13	2-18	2-24	2-26	2-28
TID (krad(SiO_2))	100	200	350	500	1000

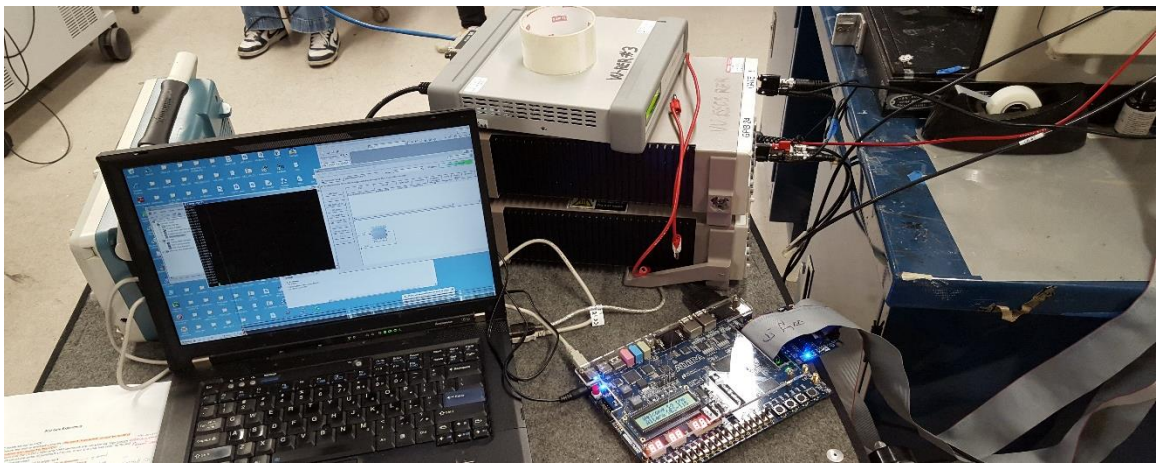
Preliminary Tests

A preliminary alpha particle test was conducted using a μCi Polonium-210 source to determine the baseline Single-Event (SE) cross section. The alpha source was about 4.8 cm^2 and the die size was 2 mm x 2 mm. The source was placed directly on top of Die 2-1, which was already inserted in the daughter board. The Device Under Test (DUT) board, daughter board and test die were placed in a large green box as to contain the radiation of the Polonium-210 source, while the power supply, FPGA board, and laptop remained outside. The power supply was set to

1.8 V for IO and 0.85 V for the core. To collect Single-Event Upset (SEU) data for each register on the Device Under Test (DUT) board, the DUT board was connected through GPIO cables to an FPGA board. The FPGA board counted the number of errors generated at 10-second intervals up to about 10 hours, and then processed and converted to ASCII text to provide readable results. The ASCII results were then sent to a laptop and logged in the terminal program Putty. A Python script (as detailed in Appendix C) was then used to generate the total upsets for each register. The data was then used to calculate single-event error rates. Figures 8a and 8b illustrate the setups described above.



(a)



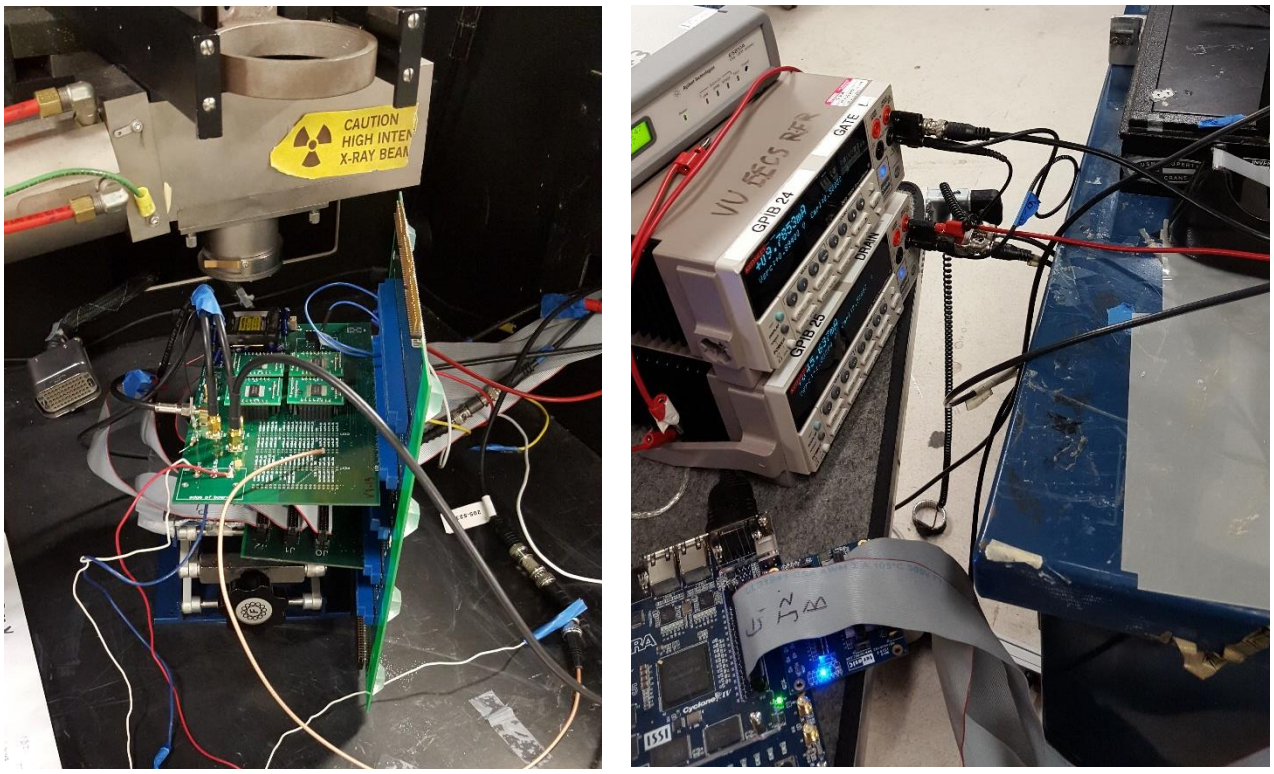
(b)

Fig. 8. (a) The daughter board is mounted horizontally by placing the vertical board vertically. The GPIO cables go into another board which is then also hooked into the bottom board. (b) The FPGA board is hooked up to the daughter board, and the computer is hooked up to the FPGA board to read the error count outputs.

Next, die 2-1 was irradiated with an ARACOR 10-keV X-ray source up to 1 Mrad(SiO_2)/min. The DUT and daughter boards were placed inside the source, while the power supply, FPGA board, and laptop remained outside. The IO supply voltage was set to 1.8 V and the core supply voltage was set to 0.894 V. The data and control inputs were all set to 0, and the clock was a constant pulse. The setup was intended so the following parameters could be monitored:

- Standby power supply current (for both IO and core)
- Functionality (reading data) at 2.5 MHz
- Leakage current at all 0-inputs
- Leakage current at all 1-inputs
- Ring oscillator (RO) waveform – RO was on during the waveform capture, off during leakage current collection

Using the above parameters, five total ionizing dose (TID) levels were determined to run the annealing tests on: 100 krad, 200krad, 350krad, 500krad, and 1 Mrad. After Die 2-1 was irradiated up to 1 Mrad, the die was then set to anneal. The leakage current was tracked continuously and ring oscillator (RO) frequency was monitored once every two hours approximately. Once the leakage current and RO frequency was stable or close to stable, an approximate time was determined for how long to collect data for the SE rates. Figures 9a and 9b show the test setup for this experiment. Figure 10 shows a block diagram of the setup used.



(a) (b)

Figure 9. (a) The daughter board is held horizontal by the bottom board so the Polonium-210 source can be placed on the die. (b) The daughter board is hooked up to voltage sources.

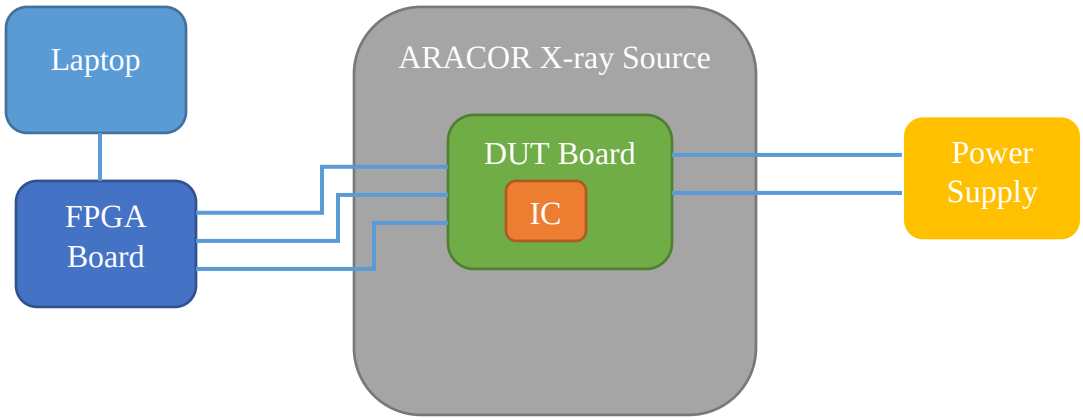


Figure 10. Block diagram of the test setup.

Primary Data collection

Before a die was exposed to the designated TID level, a pre-radiation SE test was run on the chip to ensure that there were no problems with the chip. The test dies were irradiated one at a time in the same ARACOR X-ray source within the test board. Then, the same Polonium-210 source was then placed on top of the chip with the same orientation as in the pre-radiation test, and the setup that was used in the first alpha particle testing was duplicated. Once the data was collected in Putty, the SE error counts were generated for each test using a Python script.

Chapter IV. Experimental Results

Processing Data and Change in Cross-Section Calculations

A PuTTY program was used to generate the number of single-event errors occurring in each flip-flop chain. Every ten seconds, the program produced a screen listing the number of errors for each chain during that ten-second polling cycle. Thus, a Python script was required to process all the cycles and to count the total number of errors in each shift register. The script output a file with the total time the test took and the errors for each shift register, and is shown in the appendix.

The primary data points that were analyzed were the single-event error counts, but some calculations of change in SE cross-section were done. This was done to verify the error counts were viable and to look for trends in the flip-flop chains. The following equation was used to calculate SE cross-section.

$$SE\ Cross\ Section = \frac{\#\ of\ Errors}{\#\ of\ FF \times Flux \times Time}$$

The SE cross-sections were not relied on because certain parameters were estimated throughout the experiments. Since the Polonium source activity was 13μCi, and the source was placed less than 1 cm away from the chips, the flux was estimated to be about 40000 alphas/cm^2-s. The time was taken from the Python script output in seconds. The number of flip-flops in each flip-flop chain was 250.

Preliminary Results

The data generated by the test program is formatted to display the error count for each of the twenty-eight shift registers (flip-flops) during each ten second polling cycle. This means that the recorded data requires significant processing to count the total errors from all the polling cycles. This was accomplished using a Python script, shown in the appendix, to quickly iterate through all the cycles for each shift register and accumulate the total number of errors. Table 2 shows the results of the baseline SE cross-section test over approximately 8.5 hours on chip 2-1.

This set the range of reasonable number of errors/hour to look for between about 10 and 500 to look for during a pre-radiation SE test and a TID/SE test. Anything over 500 was deemed an unreliable data point, and anything under 10 were only considered if the complementary test displayed unusual characteristics. Other factors, such as enormous discrepancies between the baseline and the SE tests, were also taken into account only for shift register analysis.

Table 2. Single-Event Upsets for All FF Chains for the Initial Baseline Test.

Shift Register	Number of SEU's
SR-1	0
SR-2	0
SR-3	0
SR-4	2012
SR-5	0
SR-6	607
SR-7	0
SR-8	1064
SR-9	752
SR-10	445
SR-11	9202
SR-12	3509
SR-13	3972
SR-14	6013
SR-15	5934
SR-16	3118
SR-17	2066
SR-18	7719
SR-19	36910
SR-20	9243
SR-21	19109
SR-22	6942
SR-23	2846
SR-24	2509
SR-25	3148
SR-26	1009
SR-27	0
SR-28	730

TID and Annealing Tests

Fig. 11 shows the changes in core supply current as a function of TID exposure level followed by changes in core current as a function of time to observe annealing effects. The data is plotted for TID exposure levels of 350 krad(SiO_2) and 500 krad(SiO_2). For the 500 krad(SiO_2) exposure level, the core current increased from 10 mA to 40 mA, with other exposure levels showing similar trend for current vs TID levels. There was very little change in core current up to 100 krad(SiO_2) TID exposure level. Beyond 100 krad(SiO_2) level, the core current increased super-linearly.

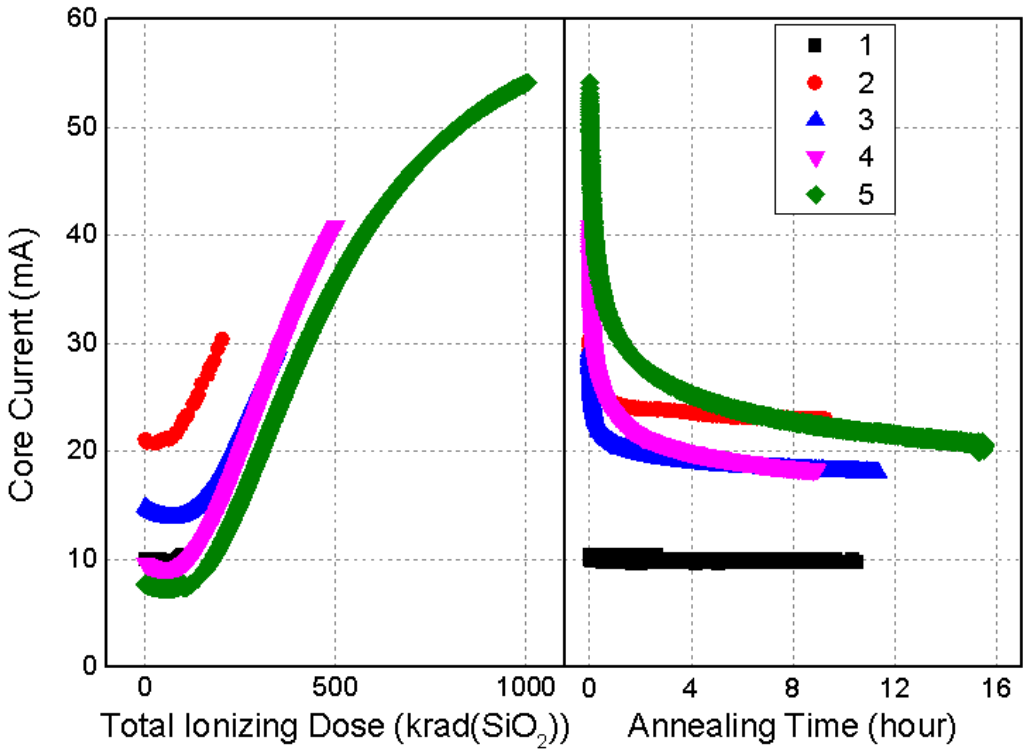


Fig. 11. The left-hand side of the curve shows delta core current versus TID level. The right-hand side of the curve shows delta core current versus annealing time. The annealing time started a few minutes after the chip was irradiated to the desired TID level. Note the change in the x-axis between the two halves of the graph.

Fig. 12 shows the data for RO frequency for the same set of exposure levels and annealing time periods. The RO frequency didn't show any significant change up to 100 krad(SiO2) TID exposure level. RO frequency decreases super-linearly after 100 krad(SiO2). For 500 krad(SiO2) TID exposure, RO frequency decreased from ~42 MHz to ~36 MHz – decrease of ~15%. For 1 Mrad(SiO2) TID exposure, RO frequency decreased from ~42 MHz to ~33 MHz – decrease of ~21%. For core current and RO frequency, the room temperature annealing resulted in significant recovery within the first 60 minutes after TID exposure ended as seen in Fig. 11 and 12. The main reason for the increase in core current and decrease in RO frequency is the leakage current in the parasitic transistors under STI in parallel with the conventional NMOS transistors in the circuit [2,3].

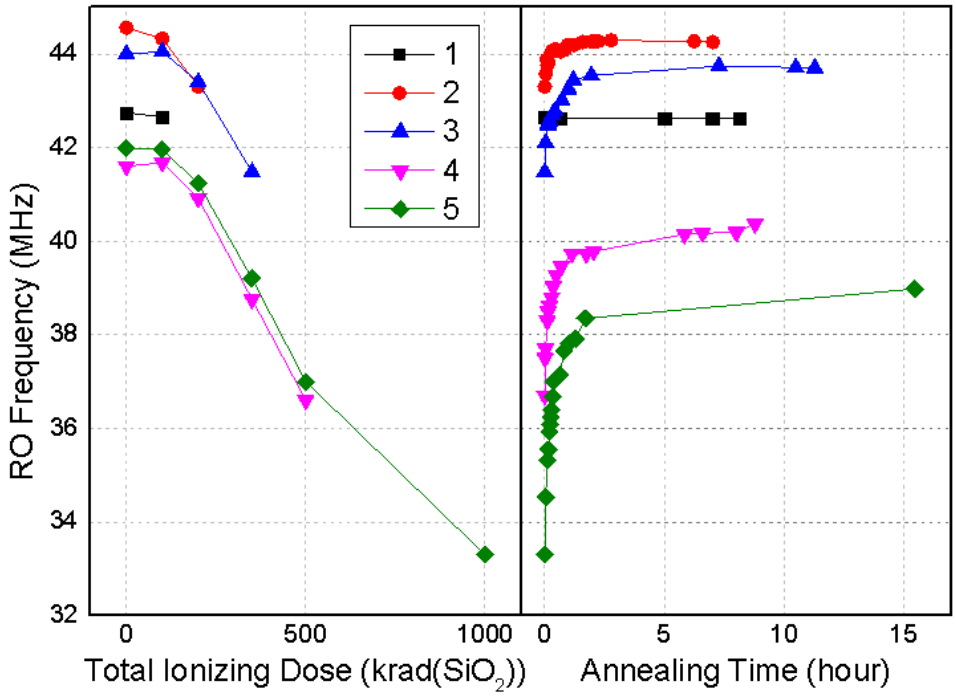


Fig. 12. The left-hand side of the curve shows RO frequency versus TID level. The right-hand side of the curve shows RO frequency versus annealing time. The annealing time started a few minutes after the chip was irradiated to the specific TID levels. The errors for each data point collected ranged between ±0.2 MHz. Note the change in the x-axis between the two halves of the graph.

Single-Event Tests

For each test IC, a pre-radiation single-event upset (SEU) test was conducted prior to any TID exposure to obtain pre-irradiation SE cross-section values. The placement of Polonium-210 source was kept identical for all tests to avoid any variations in emissivity of the alpha source. The Po-210 source was placed directly on top of each IC in the same location with the same orientation immediately after the IC had been irradiated. The input to the shift register was held HIGH for both TID and SE tests and was not changed between TID exposure and SE tests.

SE errors for all FF chains were monitored as a function of time. Fig. 13 shows the percent change in SE cross-section for five different FF designs as a function of TID exposure. These five FF's showed a consistent increase in change in SE cross-section, which is the expected result. The SE response of different FF designs is slightly different because of the relationship between feedback-loop delay of the FF design and SET pulse width.

To a first degree, an upset will occur when the SET pulse width due to an incident ion is comparable to the feedback-loop delay of a FF cell. TID exposure will reduce the available current for charging and discharging of nodal capacitances in CMOS logic circuits. As a result, logic gate delays will increase, resulting in increased feedback-loop delay of a FF cell. On the other hand, the reduced current available from a transistor (restoring current drive) will result in longer SET pulse widths. Since these two factors and their rate of change due to TID exposure will be different for different FF designs, changes in SE cross-section as a function of TID exposure will also be different. If both factors vary at the same rate, effects of TID exposure on SE cross-section will be minimal, as seen for FF #11 in Fig. 13. If SET pulse width increase at a faster rate than feedback-loop delay, SE cross-section will increase accordingly, as seen for FF #4 in Fig. 13. Similar results have been reported by others for SRAM ICs [12,13,14].

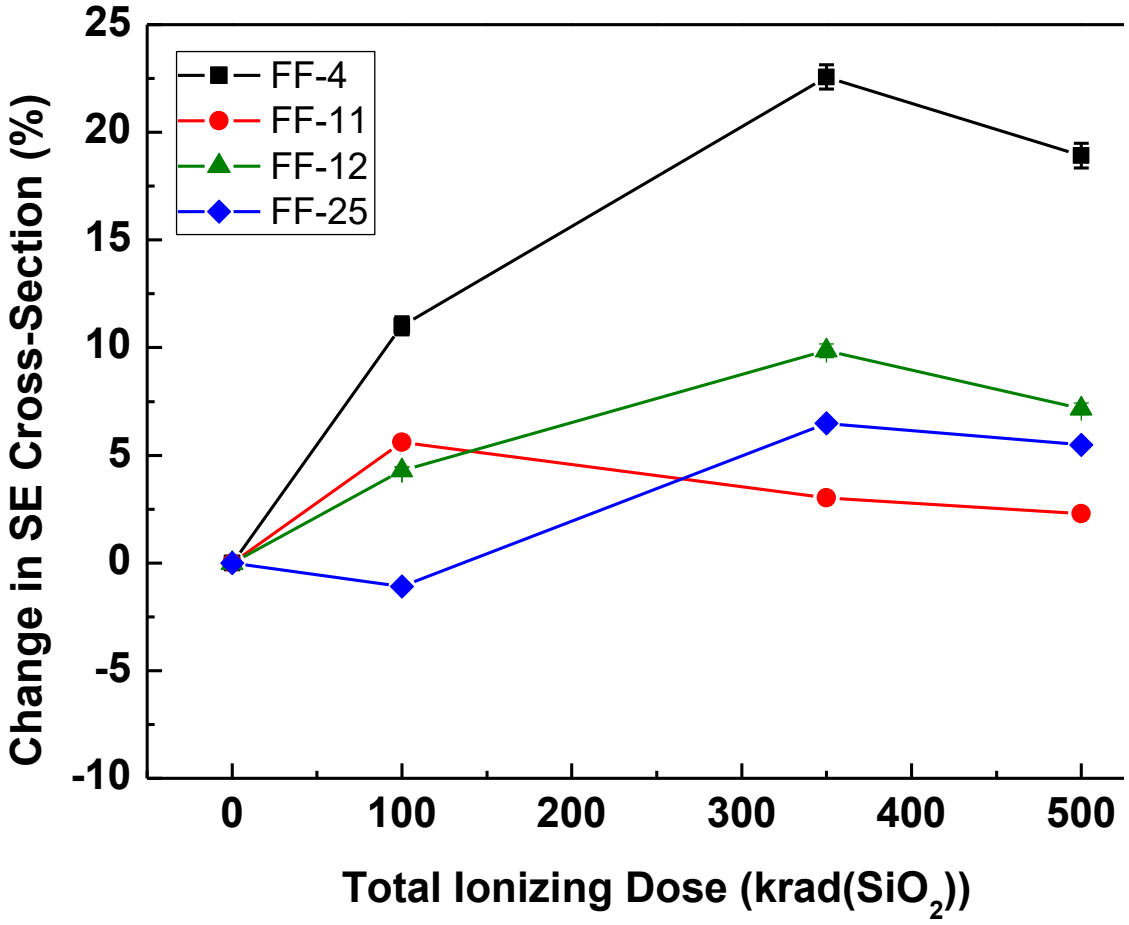


Fig. 13. The change in SE cross-section versus TID for FF's 4, 11, 12, and 25 are displayed.

Table 3. Minimum, Maximum, and Average Percent Change in SER from the Pre-Radiation Tests to the SE Tests.

TID Level (krad(SiO2))	Statistic	% Change from Pre-Radiation Test
100	Minimum	-44.093
	Maximum	9.148
	Average	-13.412
200	Minimum	-66.441
	Maximum	118.465
	Average	-6.038
350	Minimum	-98.762
	Maximum	688.620
	Average	92.615
500	Minimum	-73.488
	Maximum	787.505
	Average	111.561
1000	Minimum	-66.039
	Maximum	1852.872
	Average	242.702

Table 3 displays the minimum, maximum, and average percent changes in SE cross-section across all FF's for each TID level. The data show that 100 krad(SiO_2) TID level does not have a significant impact on the SEU rate of the chip, but 350 krad(SiO_2) and 500 krad(SiO_2) display a spike in error rates. There were certain flip-flops that generated significantly more errors during the TID/SEE test than during the pre-radiation. In general, an increase in incident TID radiation generates more errors in the 20-nm FF chains. The data shows that 100 krad(SiO_2) TID level does not have a significant impact on the SEU rate of the chip, but 350 krad(SiO_2) and 500 krad(SiO_2) display a spike in error rates. There were certain flip-flops that generated significantly more errors during the SE test than during the pre-radiation test, meaning the critical charge on those shift registers was surpassed considerably. In general, an increase in incident TID radiation generates more errors in the 20-nm FF chains.

Unusual Single-Event Test Results

Most FF designs on the test IC behaved as expected – increase in SE cross-section after TID exposure. There were some FF cells that showed a slight decrease in SE cross-section at first, followed by an increase in SE cross-section as a function of total dose. These results are shown in Fig. 14. Additionally, there were other interesting results to note among other shift registers and across the four TID levels. There were some FF's that showed zero errors during a pre-radiation test and showed multiple errors after the TID exposure.

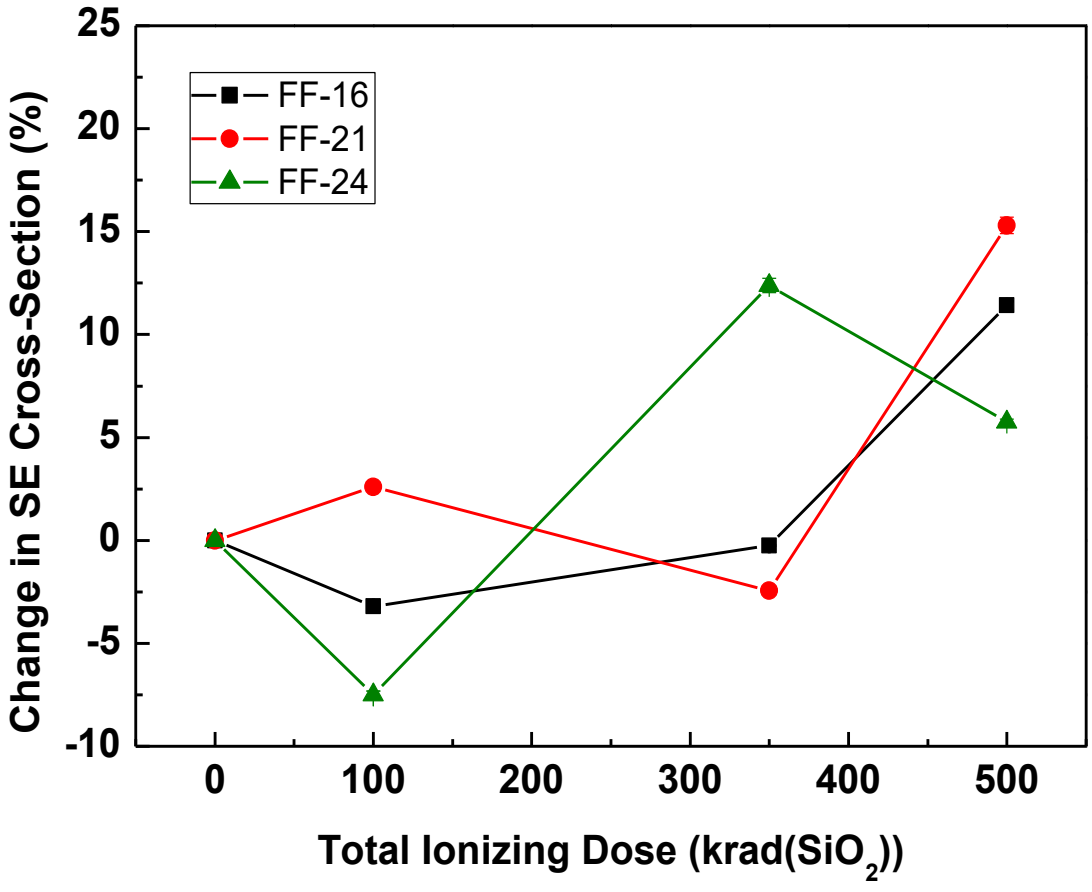


Fig. 14. The change in SE cross-section versus TID for FF's 16, 21, and 24 are displayed.

SR-7 demonstrated some unusual characteristics throughout the experiments. After having an extremely high error count during the 100 krad(SiO_2) chip's pre-radiation test, it produced 0 on the two chips during the 350 krad(SiO_2) and 500 krad(SiO_2) pre-radiation SEE tests, and around 2.5 errors/hour for 1 Mrad(SiO_2). However, for the latter three SE tests, there were a significant amount of errors induced on the flip-flop. The same happened to SR-28 during the 350 krad(SiO_2) tests, as well as several other shift registers during the 1 Mrad(SiO_2) SE tests. A simple explanation for these results is that the critical charge of the flip-flop was not reached until the Polonium-210 alpha particle source induced the required level of radiation [12]. These results show that the designs of the shift registers should be studied in order to fully understand the impact of radiation exposure on various degrees of rad-hardened flip-flops. Table 4 summarizes the unusual results found.

Table 4. Summary of Unusual SER spikes for FF's Across All TID levels

FF	TID Level (krad(SiO_2))	Pre-Radiation SER (errors/hr)	TID/SER (errors/hr)
SR-7	350	0	105.072
SR-7	500	0	5.438
SR-7	1000	2.577	28.817
SR-8	1000	0	51.855
SR-9	1000	0	113.466
SR-13	1000	0	5.403
SR-18	1000	0	94.745
SR-19	1000	2.490	2605.55
SR-28	350	0	7.400

The 200 krad(SiO_2) tests also showed an unexpected change in SE cross-section. As seen in Figures 12 and 13, the cross-section for the specific flip-flops consistently drops from the 100 krad(SiO_2) tests and is always a negative percent change from the pre-radiation tests. Looking at the data, the error rates across all shift registers varied, so there must have been an environmental

influence that impacted this SE test. In summary, different FF designs showed different trends, whereas the individual FF chains showed the same trend.

Single-Event Error Counts and Annealing

SE cross-section as a function of time was monitored to observe effects of annealing on SE cross-section. As seen in Fig. 11 and 12, the first 60 minutes after TID exposure results in significant recovery from TID damage. Fig. 15 shows results for SR-4 for SE errors per 10-minute period for the first 4 hours after different TID exposure levels. As seen for all four irradiation levels, annealing does not show a significant impact on error rates.

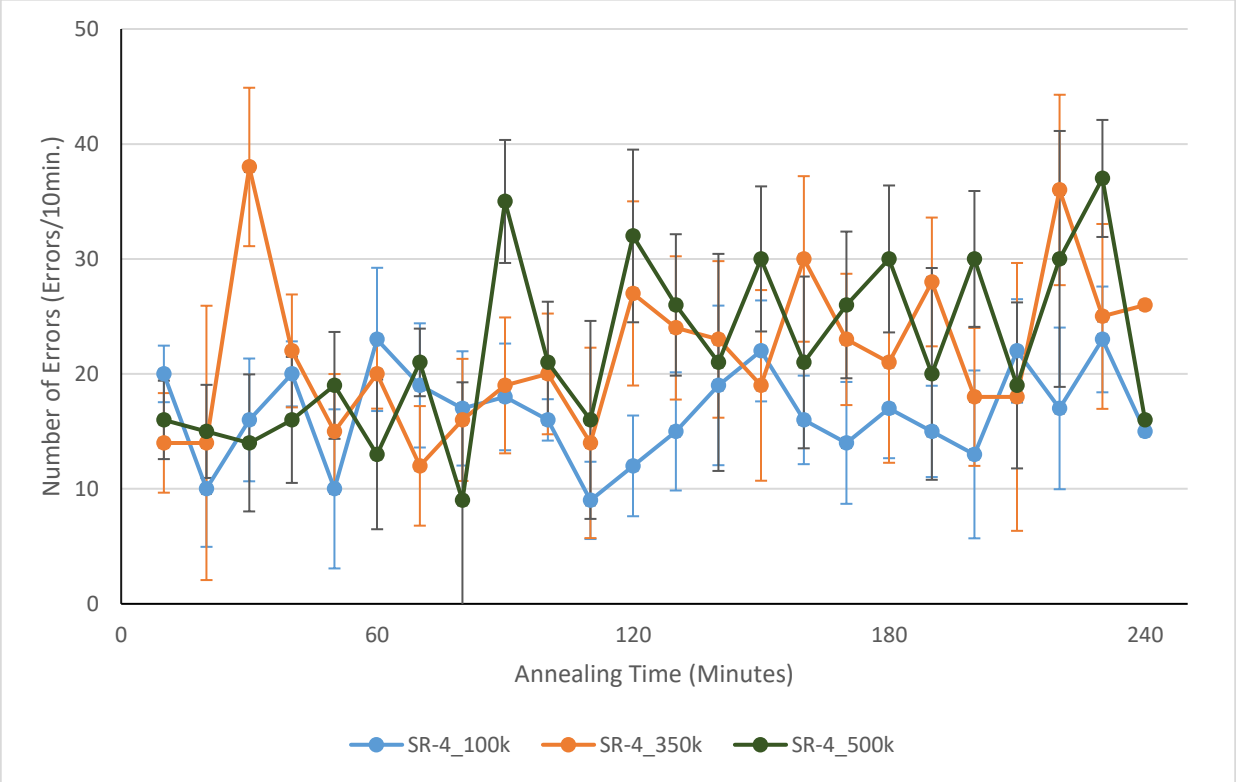


Fig. 15. The number of single-event errors versus annealing time across TID levels.

Fig. 16a and 16b complement this finding by showing the cumulative number of errors for SR-4 during the 350k pre-radiation and TID/SEE tests as a function of time. The linear trends in both curves with no obvious difference in the first two-hour window show that the error rates were not notably affected by annealing. As shown in prior data though, increasing TID rates tend to increase the presence of single-event errors. This leads to the theory that increases in SET pulse width are more impactful on the rate of SEE's than increases in feedback loop delay. Thus, annealing does reduce leakage current, but depending on the bias state, an amount of imbalance may appear between NMOS transistors on opposite sides of the FF [12]. This explains why there is no evident trend in SE counts during the annealing period across all irradiation levels.

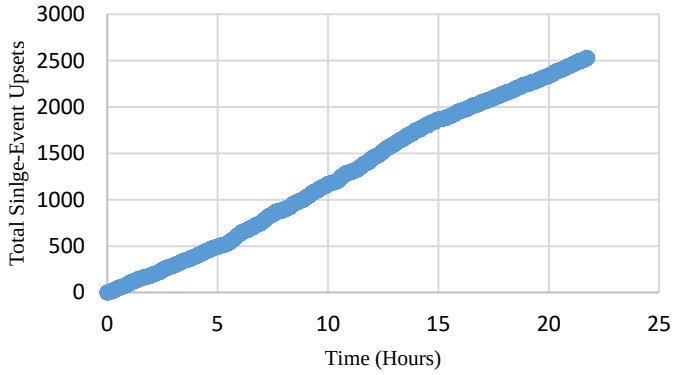


Fig. 16a. The number of total single-event upsets versus time for SR-4 during the 350 krad(SiO_2) pre-radiation test.

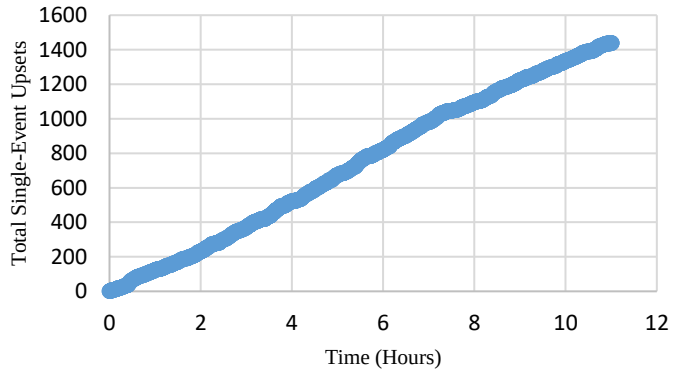


Fig. 16b. The number of total single-event upsets versus time for SR-4 during the 350 krad(SiO_2) single-event test.

V. Conclusions

Effects of combined TID and SE irradiations have been evaluated for a 20-nm bulk, planar, CMOS technology node. Custom-designed test ICs with a variety of FF cells with varying level of radiation tolerance were exposed to 10 keV X-rays and Polonium-210 alpha particle source to evaluate effects of TID on SE error rates. Results show that core current increases significantly and RO frequency decrease significantly due to TID exposures. This is primarily because of the appearance of parasitic transistors parallel to the NMOS transistors in the circuit.

SE cross-section may increase by as much as 25% after TID exposure of 500 krad(SiO_2), and SER tends to generally increase as the dose level exposures get higher. Certain flip-flop chains reacted differently and inconsistently with the varying levels of TID, so future work can study the different designs of the flip-flops and how they reacted to the different degrees of dose exposure. Room temperature annealing results in significant recovery in core current and RO frequency. However, annealing does not seem to affect SE cross-section values. Arguably, this is because that the rate of change of current annealing (along with SET pulse width) and the feedback-loop delay of a flip-flop chain are affected at the same rate.

As stated before, it is difficult to model simultaneous TID and SEE radiation, as well as the annealing process of devices in real-time. These results should help designers and users evaluate suitability of the 20-nm technology node for space and other radiation environments where TID and SE irradiations are simultaneously present.

APPENDIX

A. All Single-Event/TID Flip-Flop Data

Color	Meaning
	Reasonable data, used in calculations
	Error rates stayed at or around 0
	Semi-reasonable data, change in error rates a little high, used in calculations
	Initial error rates too high to be deemed reasonable
	Unexpected change in error rate, not used in calculations

Table 5. Color Coding of Single-Event/TID FF Data.

FF	Pre-Radiation 100k Test	100k SE Test	% Change
1	213.53	173.5	-18.75
2	0	0	
3	0	0	
4	163.89	96.96	-40.84
5	0	0	
6	627932.6	--	
7	164411.4	--	
8	0	100.43	
9	88.96	0	
10	555694.9	--	
11	675726.5	--	
12	737596.7	--	
13	2958.95	--	
14	136.43	148.91	9.15
15	152.62	152.23	-0.25
16	295.83	292.99	-0.96
17	78.97	78.03	-1.19
18	54.80	50.84	-7.22
19	741508.3	148.95	
20	311.23	224.36	-27.91
21	285.08	159.38	-44.09
22	485728.9	--	
23	23569.16	--	
24	181.26	167.24	-7.73
25	52476.7	--	
26	57.93	53.46	-7.72
27	0	0	
28	0	0	

Table 6. Single-Event/TID Data for 100 krad(SiO_2) Level.

FF	Pre-Radiation 200k Test	200k SE Test	% Change
1	0	0	
2	0	0	
3	0	0	
4	165.52	150.88	-8.84
5	0	0	
6	340.36	0	
7	246.69	83.71	-66.07
8	417.38	371.56	-10.98
9	38.11	83.25	118.46
10	17.61	11.27	-35.98
11	100.38	99.54	-0.83
12	92.65	84.38	-8.92
13	0	0	
14	145.20	146.24	0.72
15	156.82	159.21	1.52
16	294.85	331.38	12.39
17	81.67	67.02	-17.94
18	0	0	
19	0	0	
20	247.44	83.04	-66.44
21	191.95	151.60	-21.02
22	0	0	
23	20682.61	--	
24	186.47	171.37	-8.10
25	234.73	263.66	12.32
26	47.81	49.29	3.11
27	0	0	
28	0	0	

Table 7. Single-Event/TID Data for 200 krad(SiO_2) Level.

FF	Pre-Radiation 350k Test	350k SE Test	% Change
1	0	0	
2	0	0	
3	0	0	
4	122.82	138.16	12.4892
5	0	0	
6	155.30	1.92	-98.762
7	0	105.07	
8	181.33	322.22	77.6973
9	0	0	
10	1.34	3.64	171.13
11	85.27	81.92	-3.9336
12	80.36	78.43	-2.3994
13	0	0	
14	143.05	142.42	-0.444
15	181.64	172.43	-5.0686
16	303.40	297.37	-1.9881
17	80.38	77.80	-3.2125
18	0	0	
19	1.34	10.54	688.62
20	31.50	236.17	649.683
21	175.10	162.69	-7.0882
22	0	0	
23	23400	--	
24	160.09	170.01	6.19427
25	227.45	237.31	4.33352
26	59.231	56.03	-5.4072
27	0	0	
28	0	7.40	

Table 8. Single-Event/TID Data for 350 krad(SiO_2) Level.

FF	Pre-Radiation 500k Test	500k SE Test	% Change
1	0	0	
2	0	0	
3	0	0	
4	102.47	130.97	27.82
5	0	0	
6	14.96	132.78	787.51
7	0	5.44	
8	0	152.22	
9	3.20	15.42	382.08
10	2.19	9.67	340.79
11	85.63	85.35	-0.33
12	78.12	82.71	5.87
13	0	0	
14	133.15	137.44	3.22
15	142.79	194.11	35.94
16	286.74	316.88	10.51
17	73.69	82.40	11.82
18	0	0	
19	0	0	
20	212.53	56.34	-73.49
21	135.60	155.88	14.96
22	0	0	
23	31308.3	--	
24	169.17	181.28	7.16
25	232.40	250.98	7.99
26	0	0	
27	0	0	
28	0	0	

Table 9. Single-Event/TID Data for 500 krad(SiO_2) Level.

FF	Pre-Radiation 1M Test	1M SE Test	% Change
1	0	0	
2	0	0	
3	0	0	
4	77.08	104.13	35.09
5	0	0	
6	16.53	0	
7	2.58	28.82	1018.09
8	0	51.85	
9	0	113.47	
10	1.95	38.15	1852.87
11	76.02	119.52	57.23
12	74.40	121.20	62.90
13	0	5.40	
14	140.91	183.28	30.07
15	158.56	234.01	47.59
16	287.98	349.51	21.37
17	76.03	122.84	61.57
18	0	94.74	
19	2.49	2605.55	
20	0	0	
21	137.36	187.97	36.85
22	0	0	
23	27770.4	--	
24	541.87	184.03	-66.04
25	236.09	265.01	12.25
26	2.11	1.80	-14.71
27	0	0	
28	0	0	

Table 10. Single-Event/TID Data for 1 Mrad(SiO_2) Level.

B. Example Test Output

The test circuit's error counts for all shift registers were output to and processed by a PuTTY program. Fig. __ shows an example of the output during the pre-radiation and single-event tests.

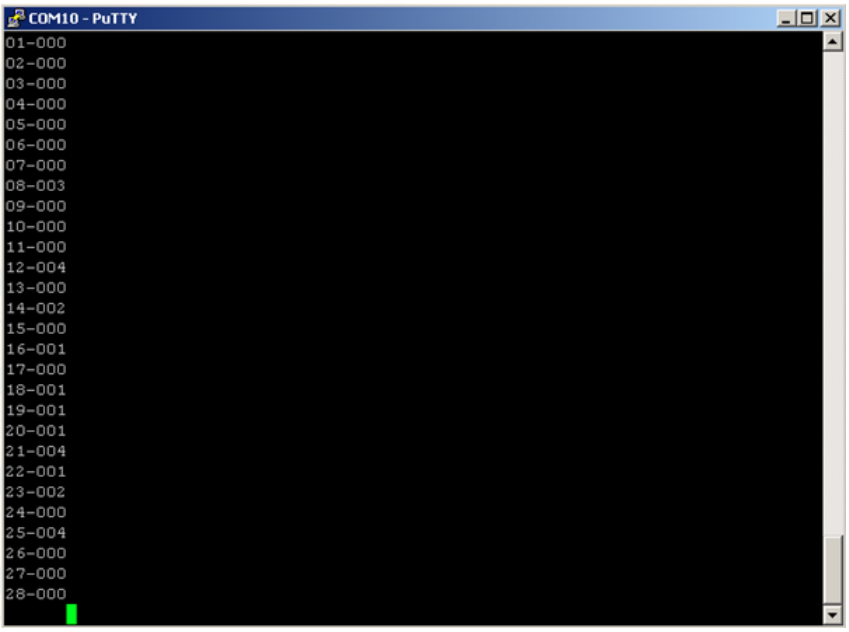


Fig 17. Typical error count data for all 28 shift registers from one polling instance of the test circuit.

C. Python Data Processing Scripts

count_total.py

The following script was used to process the PuTTY outputs to produce the total error counts for each shift register and the total time it took for the test to run. It was originally authored by Nihaar Mahatme, but some modifications were made so the script could spit out a file with all of the data rather than have the output stay in PuTTY. Note the printing to the PuTTY output screen is either commented out or put in a conditional statement, depending on if the user inputs an output file name or not.

```
#!/bin/Python
import sys
import subprocess
import os
import datetime
##check arugements
if len(sys.argv) <= 1:
  print "Python lsb)counter_process.py fileName"
  exit(0)
fileName=sys.argv[1]
outputFile = None
if(sys.argv[2]):
        outputFile = sys.argv[2]
        f = open(outputFile, 'w+')
filePointer=open(fileName,'r')
now = datetime.datetime.now()
#print "Current time is "+now.strftime("%Y_%m_%dT%H:%M")
outFile=open("processed"+now.strftime("%Y_%m_%dT%H:%M")+".txt", 'w')
total=0
sr1=0
sr2=0
sr3=0
sr4=0
```

```
sr5=0
sr6=0
sr7=0
sr8=0
sr9=0
sr10=0
sr11=0
sr12=0
sr13=0
sr14=0
sr15=0
sr16=0
sr17=0
sr18=0
sr19=0
sr20=0
sr21=0
sr22=0
sr23=0
sr24=0
sr25=0
sr26=0
sr27=0
sr28=0
for line in filePointer:
        if line.find("01-")!=-1:
                #found SR one
                #print "SR-1 add "+line.split("-")[1]
                sr1=sr1+int(line.split("-")[1],16)
                #print "SR-1 equals:"+str(sr1)+"\n----------\n"
                total=total+1
        if line.find("02-")!=-1:
                #found SR one
                #print "SR-2 add "+line.split("-")[1]
                sr2=sr2+int(line.split("-")[1],16)
```

```
                #print "SR-2 equals:"+str(sr2)+"\n----------\n"
if line.find("03-")!=-1:
                #found SR one
                #print "SR-3 add "+line.split("-")[1]
                sr3=sr3+int(line.split("-")[1],16)
                #print "SR-3 equals:"+str(sr3)+"\n----------\n"
if line.find("04-")!=-1:
                #found SR one
                #print "SR-4 add "+line.split("-")[1]
                sr4=sr4+int(line.split("-")[1],16)
                #print "SR-4 equals:"+str(sr4)+"\n----------\n"
if line.find("05-")!=-1:
                #found SR one
                #print "SR-5 add "+line.split("-")[1]
                sr5=sr5+int(line.split("-")[1],16)
                #print "SR-5 equals:"+str(sr5)+"\n----------\n"
if line.find("06-")!=-1:
                #found SR one
                #print "SR-6 add "+line.split("-")[1]
                sr6=sr6+int(line.split("-")[1],16)
                #print "SR-6 equals:"+str(sr6)+"\n----------\n"
if line.find("07-")!=-1:
                #found SR one
                #print "SR-7 add "+line.split("-")[1]
                sr7=sr7+int(line.split("-")[1],16)
                #print "SR-7 equals:"+str(sr7)+"\n----------\n"
if line.find("08-")!=-1:
                #found SR one
                #print "SR-8 add "+line.split("-")[1]
                sr8=sr8+int(line.split("-")[1],16)
                #print "SR-8 equals:"+str(sr8)+"\n----------\n"
if line.find("09-")!=-1:
                #found SR one
                #print "SR-9 add "+line.split("-")[1]
                sr9=sr9+int(line.split("-")[1],16)
```

```
                #print "SR-9 equals:"+str(sr9)+"\n----------\n"
if line.find("10-")!=-1:
                #found SR one
                #print "SR-10 add "+line.split("-")[1]
                sr10=sr10+int(line.split("-")[1],16)
                #print "SR-10 equals:"+str(sr10)+"\n----------\n"
if line.find("11-")!=-1:
                #found SR one
                #print "SR-11 add "+line.split("-")[1]
                sr11=sr11+int(line.split("-")[1],16)
                #print "SR-11 equals:"+str(sr11)+"\n----------\n"
if line.find("12-")!=-1:
                #found SR one
                #print "SR-12 add "+line.split("-")[1]
                sr12=sr12+int(line.split("-")[1],16)
                #print "SR-12 equals:"+str(sr12)+"\n----------\n"
if line.find("13-")!=-1:
                #found SR one
                #print "SR-13 add "+line.split("-")[1]
                sr13=sr13+int(line.split("-")[1],16)
                #print "SR-13 equals:"+str(sr13)+"\n----------\n"
if line.find("14-")!=-1:
                #found SR one
                #print "SR-14 add "+line.split("-")[1]
                sr14=sr14+int(line.split("-")[1],16)
                #print "SR-14 equals:"+str(sr14)+"\n----------\n"
if line.find("15-")!=-1:
                #found SR one
                #print "SR-15 add "+line.split("-")[1]
                sr15=sr15+int(line.split("-")[1],16)
                #print "SR-15 equals:"+str(sr15)+"\n----------\n"
if line.find("16-")!=-1:
                #found SR one
                #print "SR-16 add "+line.split("-")[1]
                sr16=sr16+int(line.split("-")[1],16)
```

```
                #print "SR-16 equals:"+str(sr16)+"\n----------\n"
if line.find("17-")!=-1:
                #found SR one
                #print "SR-17 add "+line.split("-")[1]
                sr17=sr17+int(line.split("-")[1],16)
                #print "SR-17 equals:"+str(sr17)+"\n----------\n"
if line.find("18-")!=-1:
                #found SR one
                #print "SR-18 add "+line.split("-")[1]
                sr18=sr18+int(line.split("-")[1],16)
                #print "SR-18 equals:"+str(sr18)+"\n----------\n"
if line.find("19-")!=-1:
                #found SR one
                #print "SR-19 add "+line.split("-")[1]
                sr19=sr19+int(line.split("-")[1],16)
                #print "SR-19 equals:"+str(sr19)+"\n----------\n"
if line.find("20-")!=-1:
                #found SR one
                #print "SR-20 add "+line.split("-")[1]
                sr20=sr20+int(line.split("-")[1],16)
                #print "SR-20 equals:"+str(sr20)+"\n----------\n"
if line.find("21-")!=-1:
                #found SR one
                #print "SR-21 add "+line.split("-")[1]
                sr21=sr21+int(line.split("-")[1],16)
                #print "SR-21 equals:"+str(sr21)+"\n----------\n"
if line.find("22-")!=-1:
                #found SR one
                #print "SR-22 add "+line.split("-")[1]
                sr22=sr22+int(line.split("-")[1],16)
                #print "SR-22 equals:"+str(sr22)+"\n----------\n"
if line.find("23-")!=-1:
                #found SR one
                #print "SR-23 add "+line.split("-")[1]
                sr23=sr23+int(line.split("-")[1],16)
```

```
                        #print "SR-23 equals:"+str(sr23)+"\n----------\n"
                if line.find("24-")!=-1:
                        #found SR one
                        #print "SR-24 add "+line.split("-")[1]
                        sr24=sr24+int(line.split("-")[1],16)
                        #print "SR-24 equals:"+str(sr24)+"\n----------\n"
        if line.find("25-")!=-1:
                        #found SR one
                        #print "SR-25 add "+line.split("-")[1]
                        sr25=sr25+int(line.split("-")[1],16)
                        #print "SR-25 equals:"+str(sr25)+"\n----------\n"
        if line.find("26-")!=-1:
                        #found SR one
                        #print "SR-26 add "+line.split("-")[1]
                        sr26=sr26+int(line.split("-")[1],16)
                        #print "SR-26 equals:"+str(sr26)+"\n----------\n"
        if line.find("27-")!=-1:
                        #found SR one
                        #print "SR-27 add "+line.split("-")[1]
                        sr27=sr27+int(line.split("-")[1],16)
                        #print "SR-27 equals:"+str(sr27)+"\n----------\n"
        if line.find("28-")!=-1:
                        #found SR one
                        #print "SR-28 add "+line.split("-")[1]
                        sr28=sr28+int(line.split("-")[1],16)
                        #print "SR-28 equals:"+str(sr28)+"\n----------\n"
if(outputFile):
                f.write("Total Runs: " + str(total) + "\n")
                f.write("Total Runtime: " + str(total*10.0/3600.0) + " hours\n")
                f.write("SR-1: " + str(sr1) + "\n")
                f.write("SR-2: " + str(sr2) + "\n")
                f.write("SR-3: " + str(sr3) + "\n")
                f.write("SR-4: " + str(sr4) + "\n")
                f.write("SR-5: " + str(sr5) + "\n")
                f.write("SR-6: " + str(sr6) + "\n")
```

```
        f.write("SR-7: " + str(sr7) + "\n")
        f.write("SR-8: " + str(sr8) + "\n")
        f.write("SR-9: " + str(sr9) + "\n")
        f.write("SR-10: " + str(sr10) + "\n")
        f.write("SR-11: " + str(sr11) + "\n")
        f.write("SR-12: " + str(sr12) + "\n")
        f.write("SR-13: " + str(sr13) + "\n")
        f.write("SR-14: " + str(sr14) + "\n")
        f.write("SR-15: " + str(sr15) + "\n")
        f.write("SR-16: " + str(sr16) + "\n")
        f.write("SR-17: " + str(sr17) + "\n")
        f.write("SR-18: " + str(sr18) + "\n")
        f.write("SR-19: " + str(sr19) + "\n")
        f.write("SR-20: " + str(sr20) + "\n")
        f.write("SR-21: " + str(sr21) + "\n")
        f.write("SR-22: " + str(sr22) + "\n")
        f.write("SR-23: " + str(sr23) + "\n")
        f.write("SR-24: " + str(sr24) + "\n")
        f.write("SR-25: " + str(sr25) + "\n")
        f.write("SR-26: " + str(sr26) + "\n")
        f.write("SR-27: " + str(sr27) + "\n")
        f.write("SR-28: " + str(sr28) + "\n")
else:
        print str(total)
        print str(sr1)
        print str(sr2)
        print str(sr3)
        print str(sr4)
        print str(sr5)
        print str(sr6)
        print str(sr7)
        print str(sr8)
        print str(sr9)
        print str(sr10)
        print str(sr11)
```

```
print str(sr12)
print str(sr13)
print str(sr14)
print str(sr15)
print str(sr16)
print str(sr17)
print str(sr18)
print str(sr19)
print str(sr20)
print str(sr21)
print str(sr22)
print str(sr23)
print str(sr24)
print str(sr25)
print str(sr26)
print str(sr27)
print str(sr28)
```

count_rate_01.py

This Python script, according to the number following the last underscore, processed the data of the separate shift registers to calculate error rates. This was also authored by Nihaar Mahatme for prior 20-nm experiments, with modifications to enable the data to be output in file format, generally a .csv file. For the rest of the shift registers, the numbers were changed in the highlighted fields to the corresponding shift register.

```
import sys
import subprocess
import os
import datetime
##check arugements
if len(sys.argv) <= 1:
  print "Python lsb)counter_process.py fileName"
```

```
 exit(0)
fileName=sys.argv[1]
filePointer=open(fileName,'r')
outputFile = None
if(sys.argv[2]):
        outputFile = sys.argv[2]
        f = open(outputFile, 'w+')
else:
        print "need output file"
        exit(0)
now = datetime.datetime.now()
#print "Current time is "+now.strftime("%Y_%m_%dT%H:%M")
outFile=open("processed"+now.strftime("%Y_%m_%dT%H:%M")+".txt", 'w')
sr1=0
sr2=0
sr3=0
sr4=0
sr5=0
sr6=0
sr7=0
sr8=0
sr9=0
sr10=0
sr11=0
sr12=0
sr13=0
sr14=0
sr15=0
sr16=0
sr17=0
sr18=0
sr19=0
sr20=0
sr21=0
sr22=0
```

```
sr23=0

sr24=0

sr25=0

sr26=0

sr27=0

sr28=0

timercounter = 0

for line in filePointer:

        if line.find("01-")!=-1:

                #found SR one

                sr1 += int(line.split("-")[1],16)

                f.write(str(timercounter) + "," + str(sr1) + "\n")

                timercounter += 10
```

REFERENCES

[1] J. R. Schwank et al., "Radiation Effects in MOS Oxides," in IEEE Transactions on Nuclear Science, vol. 55, no. 4, pp. 1833-1853, Aug. 2008.

[2] F. Faccio and G. Cervelli, “Radiation-induced edge effects in deep sub-micron CMOS transistors,” IEEE Trans Nucl. Sci., vol. 52, no. 6, Dec. 2005.

[3] M. R. Shaneyfelt, et al. “Challenges in hardening technologies using shallow trench isolation,” IEEE Trans Nucl. Sci., vol. 45, no. 6, Dec. 1998.

[4] B R. Bauman, “Single-Event Effects in Advanced CMOS Technology,” IEEE NSREC Short Course, 2005.

[5] K. Fox, "Van Allen Probes Spot an Impenetrable Barrier in Space", NASA, 2016. [Online]. Available: http://www.nasa.gov/content/goddard/van-allen-probes-spot-impenetrable-barrier-in-space. [Accessed: 03- Jun- 2016].

[6] (1997) Cosmic ray effects on microelectronics website. [Online]. Available: https://creme.isde.vanderbilt.edu/. [Accessed: 03- Jun- 2016].

[7] G. P. Ginet, D. Madden, B. K. Dichter and D. H. Brautigam, "Energetic Proton Maps for the South Atlantic Anomaly," 2007 IEEE Radiation Effects Data Workshop, Honolulu, HI, 2007, pp. 1-8.

[8] R. Pierret, *Advanced semiconductor fundamentals*. Upper Saddle River, N.J.: Prentice Hall, 2003.

[9] R. M. Chen et al., “Effects of Total-Ionizing-Dose Irradiation on SEU- and SET-Induced Soft Errors in Bulk 40-nm Sequential Circuits,” accepted for presentation at 2016 NSRE Conference.

[10] T. D. Loveless, et. al., “Neutron- and Proton-Induced Single Event Upsets for D- and DICE-Flip/Flop Designs at a 40 nm Technology Node.” IEEE Trans. On Nuclear Science, Vol. 58, No. 3, pp. 1008-1014, June 2011.

[11] C. H. Chen, P. Knag and Z. Zhang, "Characterization of Heavy-Ion-Induced Single-Event Effects in 65 nm Bulk CMOS ASIC Test Chips," in IEEE Transactions on Nuclear Science, vol. 61, no. 5, pp. 2694-2701, Oct. 2014.

[12] C. L. Axness, J. R. Schwank, P. S. Winokur, J. S. Browning, R. Koga, and D. M. Fleetwood, “Single event upset in irradiated 16k CMOS SRAMs,” IEEE Trans. Nucl. Sci., vol. 35, no. 6, pp. 1602-1607, 1988.

[13] J. R. Schwank, et al. “Issues for Single-Event Proton Testing of SRAMs,” IEEE Trans Nucl. Sci., vol. 51, no. 6, Aug. 2004.

[14] J. R. Schwank, et al. “Effects of Total Dose Irradiation on Single-Event Upset Hardness”, IEEE Trans Nucl. Sci., vol. 53, no. 4, pp. 1772-1778, Aug. 2006.

[15] L. Lantz, "Soft errors induced by alpha particles," in IEEE Transactions on Reliability, vol. 45, no. 2, pp. 174-179, Jun 1996.

[16] A. Balasubramanian, et al. “Implications of Total Dose on Single-Event Transient (SET) Pulse Width Measurement Techniques,”, IEEE Trans Nucl. Sci., vol. 55, no. 6, pp. 3336-3341, Dec. 2008.