SYSTEM-LEVEL RADIATION HARDENING OF LOW-VOLTAGE ANALOG/MIXED-SIGNAL CIRCUITS

By

Nicholas M. Atkinson

Dissertation

Submitted to the Faculty of the

Graduate School of Vanderbilt University

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

December, 2013

Nashville, Tennessee

Approved:

W. Timothy Holman

Arthur F. Witulski

Lloyd W. Massengill

T. Daniel Loveless

D. Greg Walker

ACKNOWLEDGEMENTS

I would first like to thank my advisor Professor Tim Holman for both his technical advice and his guidance through the minefield of self-doubt that seems unavoidable in the pursuit of a Ph.D. I would also like to thank Professors Arthur Witulski, Daniel Loveless, and Lloyd Massengill for the invaluable discussions and suggestions that helped shape this research. This work would also not have been possible without the support of Jeff Kauppila, who trusted me with the challenging project that blossomed into this dissertation. I would also like to acknowledge Draper and DTRA for their financial support of this research.

I want to express my deep gratitude to Dr. Enxia Zhang for bonding many parts for me and helping me out with the ARACOR. Dr. Jon Ahlbin was also a great help in mentoring me in my first few years of grad school. I also want to thank Ray Blaine for technical discussions and collaborations on several projects. I am also grateful to Nelson Gaspard for being extremely helpful technically and generally being a good guy. I want to thank Mike King for generously helping me out with the ARACOR several times, and I'm grateful to my office mates Nick Hooten and Geoff Bennett for some technical discussions but mostly for many welcome distractions. I would also like to acknowledge the rest of the RER students for their help.

Finally I want to thank my amazing family for their emotional support through these last five years. My parents—having been through the same process themselves—were always understanding and encouraging. The love of my amazing wife Stef is the one thing that kept me going through all the ups and downs of my graduate career.

TABLE OF CONTENTS

Page

ACKNOWLEDGEMENTS ... ii

LIST OF FIGURES ... v

LIST OF TABLES ... xiii

Chapter

I. INTRODUCTION ... 1

Objective of research ... 1
Organization of dissertation ... 3

II. RADIATION EFFECTS IN INTEGRATED CIRCUITS ... 5

Total ionizing dose ... 5
TID mechanisms ... 6
TID effects in analog ICs ... 8
TID mitigation ... 9
Single-event effects ... 13
SEE mechanisms ... 13
Analog single-event transients ... 15
SET mitigation ... 16

III. VOLTAGE REFERENCE CIRCUITS ... 20

Basic bandgap reference theory ... 21
Integrated low-voltage CMOS reference topologies ... 23
Temperature regulation of voltage references ... 27
Examples in industry and literature ... 28
Modeling techniques ... 33
Voltage reference designs ... 44
Test structures on first-pass 180-nm chip ... 45
Temperature-regulated reference on 40-nm chip ... 50
RHBD temperature-regulated reference on 180-nm chip ... 57
Summary ... 59

IV. SWITCHED-CAPACITOR CIRCUITS ... 61

Basic switched-capacitor (SC) theory: the integrator ... 61
Differential sample-and-hold amplifier ... 64

Overview of 45-nm sample-and-hold amplifier designs 67
Summary 73

V. RADIATION EFFECTS IN CONTINUOUS-TIME CIRCUITS 74

Total dose effects and mitigation 74
Radiation vulnerabilities in CMOS voltage reference 77
Op amp offset voltage 79
DTMOST reference devices 82
Current mirror mismatch 85
Radiation hardening of voltage reference using chopper stabilization 90
Dynamic offset cancellation: chopper stabilization 90
RHBD chopper voltage reference design 92
Simulation results: 180-nm design 98
Experimental setup 115
Experimental results 120
Radiation-hardened voltage reference using PTAT subtraction 124
PTAT subtraction topology 124
Radiation hardening using chopper stabilization 129
Simulation results: 180-nm design 132
RHBD considerations for analog circuits 135
RHBD layouts 136
Digital trimming schemes 139
Mixed-voltage interfaces 146
Single-event effects and mitigation 152
SEE mitigation in first-order voltage references 153
Differential charge cancellation (DCC) 154
Sensitive-node active charge cancellation (SNACC) 160
SEE in RHBD chopper-stabilized voltage reference 165
Conclusion 169

VI. RADIATION EFFECTS IN DISCRETE-TIME CIRCUITS 171

Total dose effects and mitigation 171
Dynamic offset cancellation: auto-zeroing 172
Switched-capacitor voltage reference with auto-zeroed op amp 174
Single-event effects and mitigation 181
The quad-path hardening technique 182
Experimental setup 192
Experimental results 193
Conclusion 198

VII. CONCLUSIONS 200

REFERENCES 206

LIST OF FIGURES

Figure Page

1. Collection of charge deposited by heavy ion in a reverse-biased junction. 14
2. Basic bandgap reference. ...22
3. Dynamic-theshold MOS transistor (DTMOST) [58]. ...24
4. DTMOST reference. ...25
5. NFET reference. ...27
6. Basic buried-zener voltage reference [101]. ...28
7. LTZ1000 components [51]. ...28
8. Temperature-regulated 7-V reference using the LTZ1000 [51]. ...29
9. Simulation of 7-V reference of Fig. 8 with and without thermal feedback. ...31
10. Temperature-regulated bandgap reference [53]. ...32
11. Functional illustration of first-order voltage reference (a) without and (b) with thermal regulation. The label 'T_{ZTC}' indicates the temperature at which the VREF tempco is zero. ...34
12. Behavioral model of thermal feedback loop using voltage sources for V_{REF} and V_{PTAT}. ...37
13. Open-loop (no thermal feedback) temperature response of model of 40-nm voltage reference using behavioral model of Fig. 12. ...38
14. Closed-loop (with thermal feedback) temperature response of model of 40-nm voltage reference using behavioral model of Fig. 12. (a) Control voltages, (b) rise in temperature and the resulting die temperature. ...38
15. Behavioral model of thermal feedback loop using Verilog-A tables for V_{REF} and V_{PTAT}. ...40
16. Open-loop (no thermal feedback) temperature response of model of voltage reference in 180-nm process using behavioral model of Fig. 15. Plot in (b) is simply zoomed in on V_{REF} in (a). ...40
17. Closed-loop (with thermal feedback) temperature response of model of voltage reference in 180-nm proces using behavioral model of Fig. 15. (a) Control voltages, (b) rise in temperature and the resulting die temperature. ...41

18. (a) DTMOST and (b) nFET reference designs fabricated in IBM 180-nm process. 45

19. Complementary folded-cascode op amp. 46

20. Effect of temperature on voltage of DTMOST reference with *R2* = 154 kΩ and *R1* = 31 kΩ. Two temperature measurements on the same reference were performed. 47

21. Temperature variation of DTMOST reference in three R1/R2 configurations. 48

22. Effect of temperature on voltage of nFET reference with *R2* = 154 kΩ and *R1* = 123 kΩ. Two temperature measurements on the same reference were performed. 49

23. Temperature variation of nFET reference in three R2/R1 configurations. 49

24. Voltage-summed DTMOST reference on 40-nm test chip (#1 in Table 1). 50

25. Current-summed DTMOST reference on 40-nm test chip (#5 in Table 1). 51

26. Trimming of V_{REF} via R2 in voltage-summed reference of Fig. 24. Digital trim code and voltage variation are indicated for each curve. 53

27. Temperature response of reference voltage across the 75—100°C range at different R2 trim codes. Digital trim code and voltage variation are indicated for each curve. 53

28. Temperature response of PTAT voltage with R3 trim codes of 0, 5, 10, 15, and 20. 54

29. Measured temperature response of reference (a) without and (b) with thermal regulation. For both measurements the trim code for V_{REF} is the maximum 31. 55

30. (a) Die temperature measured using on-chip diode when thermal regulation is active. (b) Rise in temperature as a function of power dissipated by heater. 56

31. RHBD temperature-regulated voltage reference designed in IBM 180-nm process. 57

32. Simulation results demonstrating trim functionality of (a) reference voltage and (b) PTAT voltage. 58

33. (a) A basic continuous-time integrator implemented with a resistor and capacitor. (b) A switched-capacitor integrator implemented with two capacitors and two switches operated on non-overlapping control signals ϕ_1 and ϕ_2 with frequency $f_s = 1/T_s$. 62

34. Differential sample-and-hold amplifier with switches operated on non-overlapping control signals ϕ_1 and ϕ_2 with frequency $f_s = 1/T_s$. 65

35. Differential sample-and-hold amplifier in (a) sample mode and (b) evaluation mode. 66

36. Switch implementations in (a) nFET SHA and (b) transmission-gate SHA. 67

37. (a) Non-overlapping clock generation circuit. Test chip design also includes multiplexing to overwrite the circuit-generated signals with external clocks. (b) Non-overlapping clock signals. The vertical dashed lines indicate the non-overlapping time windows of the clocks. 68

38. Schematic of nFET-input OTA used in nFET SHA. Each transistor is body-source tied. Bias voltages *v1*, *v3*, and *v4* are generated in the bias circuit of Fig. 39. The sizes of the transistors in the OTA are listed in Table 2. 69

39. Bias circuit used in both nFET-input and complementary-input OTA. The labeled nodes are referenced in the OTA schematics of Fig. 38 and 40. The size of each transistor is listed in Table 3..70

40. Schematic of complementary-input OTA used in TG SHA. Each transistor is body-source tied. Bias voltages *v1*, *v2*, *v3*, and *v4* are generated in the bias circuit of Fig. 39. The sizes of the transistors in the OTA are listed in Table 5. The common-mode voltage *vcm* is generated with a resistor divider as in Fig. 38. 71

41. Differential output of nFET and TG SHA with a voltage ramp input. 72

42. (a) DTMOST reference. (b) NFET reference. 75

43. Change in DTMOST reference output as a function of total dose. 76

44. Change in nFET reference output as a function of total dose. 76

45. DTMOST-based voltage reference. Red voltage sources indicate radiation-induced shifts. 78

46. Radiation-induced shifts in op amp offset voltage. The labels “0.5-µm” and “2-µm” indicate the channel length of the input transistors of the op amp. 80

47. Radiation-induced voltage shifts in edgeless DTMOSTs with 100 µm width and 0.5 µm length at various bias points. The voltage labels indicate the bias voltage during irradiation, and the current labels indicate the corresponding current. The voltage shift is reported as the change in voltage required to sink the amount of current indicated, which corresponds to the initial bias point. 83

48. Radiation response of pFETs with 5 μm width and 0.5 μm length. The shift in source-gate voltage required to source 5 μA with source-drain voltage of 1.75 V is plotted. All gates were biased at 0.9 V during X-ray irradiation. 86

49. Radiation-induced shift in voltage reference. The pre-rad output voltage was 484 mV. Each point is the mean of 1010 samples, with the error bars indicating the standard deviation. 89

50. (a) Chopper schematic symbol. (b) Chopper amplifier with single-ended output and low-pass filter. (c) Time-domain representation of unfiltered output V_F with and without offset voltage $V_{OS} \approx V_{OS1}$. 91

51. Radiation-hardened voltage reference design. 93

52. RHBD temperature-regulated voltage reference designed in IBM 180-nm process. R = 2.74 kΩ, R1≈ 750 Ω, R2 ≈ 3.2 kΩ, Rfilt = 10 kΩ. 99

53. Chopper OTA used in RHBD voltage reference design. Dimensions of each transistor indicated in micrometers. 100

54. Bias circuit for OTA in Fig. 53. 100

55. Effect of offset voltage (V_{OS}) of OTA input pair on (a) VREF output and (b) IPTAT bias current in the voltage reference without chopping. 102

56. Effect of offset voltage (V_{OS}) of OTA input pair on (a) VREF output and (b) IPTAT bias current in the voltage reference with chopping at 100 kHz. 103

57. Effect of shifts in DTMOSTs D1 and D2 (shown as ΔV1 and ΔV2, respectively) on voltage reference (a) output VREF and (b) bias current IPTAT *without chopping*. The blue lines show the baseline values and the red lines show the values when D1 shifts by 0.3 mV and D2 shifts by 0.2 mV. 105

58. Effect of shifts in DTMOSTs D1 and D2 (shown as ΔV1 and ΔV2, respectively) on voltage reference (a) output VREF and (b) bias current IPTAT *with chopping*. The blue lines show the baseline values and the red lines show the values when D1 shifts by 0.3 mV and D2 shifts by 0.2 mV. 106

59. Sensitivity plot of radiation-induced voltage shifts in DTMOSTs D1 (ΔV1) and D2 (ΔV2). Shaded region inside boxes indicate combinations of ΔV1 and ΔV2 that cause shifts in voltage reference less than ±0.1% of baseline value 520 mV. The maximum ΔV1 is assumed to be ±1 mV. 107

60. Effect of threshold voltage shift in pFET current source P1 on voltage reference output. 108

61. Input chopper of OTA with table showing drain-source voltages of each switch during each phase. 110

62. Single chopper switch with sidewall leakage modeled using identical transistor with gate voltage representing trapped STI charge. 110

63. Effect of threshold voltage on switch drain-source voltage as a function of the aspect ratio, using IBM 180-nm process parameters. 113

64. Effect of threshold voltage shifts in the DTMOST chopper on the voltage reference output VREF. 114

65. Chopper-stabilized op amp test circuit implemented with 180-nm test chip (the DUT) and external components on breadboard. 116

66. Fully-differential complementary folded-cascode op amp on AMP test chip (the DUT in Fig. 65). The bias circuit that generates *Vb1, Vb2, Vb3,* and *Vb4,* the common-mode feedback circuits that generate *Vcmfbp* and *Vcmfbn*, and the compensation capacitors on the cascode stage outputs are not shown....................117

67. Chopper-stabilized voltage reference test circuit. Components in gray were on the 180-nm DUT, and all other components were discrete parts. 119

68. Input-referred offset voltages of chopped and static op amps measured on AMP chip 1. 121

69. Input-referred offset voltages of chopped and static op amps measured on AMP chip 1. 122

70. Measured shifts in reference voltage for the chopped reference (VREF chip 1) and the static reference (VREF chip 2). The pre-rad voltage was 527.7 mV for the chopped reference and 528.8 mV for the static reference. Error bars indicate the minimum and maximum readings over a measurement period of 20 s. 123

71. Concept of PTAT subtraction voltage reference topology, schematic on left and temperature response on right. 125

72. Implementation of PTAT subtraction voltage reference in IBM 180-nm process. 126

73. Temperature responses of (a) PTAT currents and (b) reference voltage VREF. 128

74. RHBD PTAT subtraction voltage reference using chopper stabilization. 129

75. Transient response of voltage reference (a) without chopping and (b) with chopping to voltage shifts of 0.3 mV and 0.2 mV in D1a and D2a, respectively. The DTMOST voltage shifts occur at 3.5 ms. 132

76. Transient response of voltage reference (a) without chopping and (b) with chopping to voltage shifts of 0.3 mV and 0.2 mV in D1b and D2b, respectively. The DTMOST voltage shifts occur at 3.5 ms. 133

77. Transient response of voltage reference (a) without chopping and (b) with chopping to a shift in pFET current mirror offset voltage V_{OP}. The voltage shifts occur at 3.5 ms. 134

78. RHBD transistor layouts: (a) enclosed layout used on CMHV7SF test chip, (b) multi-finger enclosed layout used in RHBD voltage reference designs, (c) dog bone layout, and (d) edgeless dog bone layout used in RHBD voltage reference designs. 136

79. (a) Schematic and (b) trim functionality of a 5-bit programmable resistor with series trimming scheme. Rlsb ≈ 44 Ω, Rmin ≈ 2.1 kΩ, W/L = 20/0.18. 140

80. (a) Schematic and (b) trim functionality of a 5-bit programmable resistor with parallel trimming scheme. Rs ≈ 1 kΩ, Rp ≈ 2.42 kΩ, Rlsb ≈ 4 kΩ, W/L = 20/0.18. 141

81. Response of programmable resistor to nFET threshold voltage shifts with (a) series and (b) parallel trimming schemes. 143

82. Heater control in 40-nm temperature-regulated voltage reference. VREF is the reference voltage, and VPTAT is the temperature sensor voltage. 146

83. (a) VREF and VPTAT control signals and (b) chip temperature (ambient temperature + rise in temperature generated by heater) as a function of ambient temperature in a closed-loop thermal feedback simulation of heater control circuit. 147

84. (a) Current-biased and (b) voltage-biased implementations of high-voltage output stage of heater op amp. A thick gate line in the FET symbol indicates a thick-oxide (3.3-V) FET. 148

85. (a) Thermal feedback simulations using current-biased amplifier with V_{TH} shifts. (b) 3.3-V supply current at 50°C as a function of pFET threshold voltage shift. 149

86. (a) Thermal feedback simulations using voltage-biased amplifier with V_{TH} shifts. (b) 3.3-V supply current at 50°C as a function of pFET threshold voltage shift. 151

87. Voltage-summing topology of reference designed and fabricated in UMC 40-nm process. Quantities in blue have a negative tempco, and quantities in red have a positive tempco. 153

88. Effect of bias current on ASETs generated in DTMOST. (a) ASET waveforms for bias currents ranging from 1 to 15 μA. (b) ASET amplitude plotted as a function of bias current. The width of the DTMOST is scaled such that a constant current density (current/width) of 0.1 μA/μm is maintained. 155

89. Effect of DTMOST width on ASET amplitude when bias current is 10 μA. 156

90. (a) Baseline and (b) DCC layouts and schematics of D1/D2 DTMOST pair. Each drawn transistor has length 1 μm and width 3.125 μm. Each layout shown is only a quadrant of the complete layout; the complete layout is implemented with four quadrants as in (c). 157

91. Transient waveforms caused by 1-pC ion strike on (a) D1 and (b) D2. 158

92. Reference voltage ASET amplitude expressed as percentage of DC value 472 mV and plotted as a function of the fraction of charge collected by D1. The remainder of the 1 pC of deposited charge is collected by D2. 159

93. Voltage summing circuit of Fig. 87 with SNACC circuitry added. 160

94. Layout of two D3 unit cells with two D3d unit cell dummies. Channel width of each unit cell is 3.125 μm, channel lengths of D3 and D3d unit cells are 1 μm and 60 nm, respectively. Node names correspond to Fig. 93. 162

95. (a) ASETs on VREF output due to ion strike depositing a total of 200 fC of charge on P3 and P3d in Fig. 93. The extremes cases and the case of a 50/50 split are labeled. (b) Error energies of ASETs plotted as a function of the fraction of charge collected by P3, with the remainder of the 200 fC collected by P3d. 163

96. Error energies of reference voltage ASETs plotted as a function of the fraction of charge collected by D3, with the remainder of the 200 fC collected by D3d 164

97. Chopper-stabilized voltage reference with filter capacitors and three SE strike locations labeled. 165

98. SETs at VREF and VREFRC nodes when the three indicated locations in Fig. 97 are struck with ions depositing 1 pC of charge. Note: voltage and time scales are different in each plot. 167

99. Non-inverting amplifier with input-referred offset voltage V_{OS}. 172

100. Non-inverting amplifier with auto-zeroed op amp. 172

101. Operation of auto-zeroed amplifier in (a) sample phase and (b) cancel phase. 173

102. Switched-capacitor DTMOST voltage reference. 174

103. SC voltage reference with auto-zeroed op amp with clock timing diagram. 176

104. (a) AZ phase, (b) phase 1 and (c) phase 2 of operation of the auto-zeroed SC voltage reference in Fig. 103. 177

105. (a) Time-domain waveforms of SC reference output at 0, 25, 50, 75, and 100°C. (b) Voltage reference output at the end of phase 2 as a function of temperature. 178

106. (a) Time-domain waveforms of SC reference output with -10, -5, 0, +5, and +10 mV of offset voltage in the op amp. (b) Voltage reference output at the end of phase 2 as a function of offset. 178

107. The effect of shifts in the DTMOST D1 on the phase 2 output of the SC voltage reference. 179

108. Differential sample/hold amplifier. 183

109. Single-event transient in nFET SHA with input of 0.2 V and sample rate of 1 MS/s. Charge deposition of 200 fC resulted in -0.4 V sample error. 183

110. Schematic showing half of the dual-path S/H amp topology (negative half is identical) and simplified schematic of modified dual-input nFET OTA. 184

111. Schematic of fully-differential complementary folded-cascode operational transconductance amplifier (OTA). The bias circuit that generates Vb1, Vb2, Vb3, Vb4, and Vb5, as well as the two common-mode feedback circuits that generate Vcmfbp and Vcmfbn are not shown. 187

112. Schematic showing half of the quad-path S/H amp topology (negative half is identical) and simplified schematic of modified quad-input complementary folded-cascode OTA. 188

113. Layouts of (a) conventional, or baseline, TG S/H amplifier and (b) quad-path S/H amplifier fabricated in 45-nm technology with sub-circuits labeled. Layout images are on same scale. 191

114. Average sample error generated by strikes on most sensitive nFET switch. 195

115. Average sample error generated by strikes on most sensitive pFET switch. 196

LIST OF TABLES

Table Page

1. Number and description of voltage references on 40-nm test chip. 50

2. Transistor sizes of nFET-input OTA in Fig. 38. 69

3. Transistor sizes in bias circuit in Fig. 39. 69

4. Performance parameters of the nFET-input OTA in Fig. 38. 70

5. Transistor sizes of complementary-input OTA in Fig. 40. 71

6. Performance parameters of the complementary-input OTA in Fig. 40. 72

7. Performance parameters of the nFET and TG SHAs. 73

8. Effect of offset voltage in matched pairs in OTA on output (VREF) and bias current (IPTAT) of voltage reference (a) without and (b) with chopping. 104

9. Effect of each offset voltage in the PTAT subtraction reference on the output voltage expressed as the magnitude of the gain from the offset to the output. 135

10. Description of tested S/H circuits. 192

11. Comparison of 45-nm SHA designs. 198

CHAPTER I

INTRODUCTION

A. Objective of research

Analog circuits are necessary for a system-on-a-chip to interact with the outside world. Despite the advances made in high-density digital logic, analog/mixed-signal (AMS) circuits and systems will always be required for functions such as chip power management, analog-to-digital conversion, digital-to-analog conversion and a variety of signal processing of measured real-world values (e.g. temperature). However, in a radiation environment many of the more advanced AMS circuits are particularly susceptible to radiation effects, due to stringent requirements on signal integrity and precision. For example, if exposure to ionizing radiation changes the characteristics of transistors in a precision voltage reference, a shift of even one millivolt can cause the circuit to operate outside of specifications, resulting in failure. Similarly, if an ionizing particle induces a voltage transient in a sampling circuit, the incorrect sample voltage can lead to a significant digital conversion error that propagates through subsequent digital blocks.

The general objective of this research is to develop and demonstrate system-level radiation-hardened-by-design (RHBD) techniques for low-voltage analog circuits. One of the benefits of system-level techniques is that they are not directly dependent on specific mechanisms, making them portable across not only various circuit applications but across technology nodes. The techniques developed in this work are applicable—but not

limited—to low-voltage design, which is a requirement for radiation-tolerant circuits in modern complementary metal-oxide-semiconductor (CMOS) processes, due to the radiation tolerance of the thin oxides. The low-voltage nature of the designs contributes further to the portability of the presented techniques to modern processes.

To make a broad impact on the design of radiation-tolerant AMS systems, the research in this dissertation covers both continuous-time and discrete-time (sampled) circuits using specific circuits for demonstration. The circuit used as a case study for continuous-time circuits is a precision voltage reference. The voltage reference—with 10-bits, or 0.1%, of precision—provides an effective demonstration of how radiation affects sensitive analog circuitry, and how the effects can be mitigated. The techniques for mitigating radiation effects in a voltage reference are applicable to hardening analog circuits in general. Switched-capacitor circuits are used as case studies for discrete-time circuits. In particular, a switched-capacitor voltage reference and a sample/hold amplifier are used to demonstrate system-level hardening techniques that can be generally applied to switched-capacitor circuits.

The main challenges of an RHBD precision voltage reference are the temperature drift and total dose response. If 10 bits of precision are required, then the reference voltage must remain within ½ LSB (or 0.05%) of its nominal value across both temperature and radiation exposure. In this work both of these effects are addressed with a temperature-regulated voltage reference architecture. The use of an on-chip heater to maintain a constant temperature significantly reduces the temperature drift of the reference, which allows for the use of a simple first-order design. By using a first-order reference, hardening the circuit using system-level techniques becomes a viable option.

Such hardening techniques are investigated for both a conventional continuous-time voltage reference and a switched-capacitor voltage reference. Since transient perturbations can also limit the precision of a voltage reference, single-event effects are also addressed in this research.

The floating-node nature of switched-capacitor circuits makes them especially susceptible to single-event effects. Since switched-capacitor circuits are often in the analog front end of an AMS system, it is critical to ensure signal integrity in a radiation environment. In addition to single-event sensitivity, another parameter that can limit the performance of a low-voltage AMS system is the signal range. The shrinking supply voltage of modern CMOS processes makes it imperative that the front-end signal range is maximized. In this research, both of these issues are addressed by introducing and demonstrating the quad-path hardening technique for switched-capacitor circuits that offers rail-to-rail signal range.

B. Organization of dissertation

This dissertation covers total dose and single-event effects in both continuous- and discrete-time circuits. Chapter II provides background on these radiation effects. The mechanisms of total ionizing dose (TID) and single events (SEs) are covered, and a literature overview of their effects in circuits is provided. Chapter III provides background information on voltage reference circuits—the continuous-time case study—from basic design concepts to the novel use of on-chip heating for thermal stabilization in precision references. The chapter also includes overviews of voltage reference designs fabricated in commercial 180-nm and 40-nm processes. In Chapter IV the basic theory of

switched-capacitor circuitry—the discrete-time case study—is discussed, and an overview of the silicon-on-insulator (SOI) 45-nm design is presented.

Chapter V discusses radiation effects in continuous-time circuits, using the voltage reference as the demonstration circuit. An in-depth analysis of total dose effects in a precision voltage reference is presented along with experimental measurements, and novel hardening techniques utilizing chopper stabilization are demonstrated with simulation and experimental results. Design guidelines for TID hardness are presented along with a discussion on mitigation schemes for single-event effects. In Chapter VI radiation effects in discrete-time circuits are discussed. A switched-capacitor voltage reference is used to demonstrate the TID tolerance of the auto-zero offset cancellation scheme, and a sample/hold amplifier is used to demonstrate the SE tolerance of the novel quad-path hardening technique. The final chapter of the dissertation concludes the work and summarizes the presented mitigation schemes with a list of RHBD guidelines.

CHAPTER II

RADIATION EFFECTS IN INTEGRATED CIRCUITS

This chapter provides background on the radiation effects that can be detrimental to analog circuits. First, the basic mechanisms and circuit effects of total ionizing dose (TID) in CMOS and bipolar technologies are discussed. Then a brief literature overview of TID in analog circuits and voltage references is given, followed by a discussion of the basic single-event (SE) mechanisms and circuit effects in CMOS circuits.

A. Total ionizing dose

In certain environments, like space, the abundance of ionizing particles such as protons and electrons is sufficient to deposit appreciable energy in semiconductor material. The contact of ionizing radiation with a semiconductor results in charge deposition via electron-hole pair generation, and the accumulation of such charge on a device or circuit is referred to as the total ionizing dose (TID). Unlike some other radiation effects, TID is an effect of accumulation as opposed to a transient effect. Charge deposited on an integrated circuit (IC) often becomes trapped in the insulator material (primarily SiO_2) of the chip, and the trapped positive charge can alter the device characteristics and, hence, the circuit performance. In this section, the basic effects of TID on bipolar and CMOS devices are briefly discussed. [1]–[3]

TID mechanisms

The primary impact ionizing radiation can have on bipolar transistors is gain degradation. Since the charge trapped in the oxide of an IC is positive, when sufficient charge is present it can be enough to invert the surface of a p-type semiconductor. In bipolar transistors this surface inversion increases the number of recombination centers, resulting in an increase in leakage and a decrease in the current gain of the transistor. For charge trapped at the semiconductor-oxide interface, the surface recombination velocity is increased, similarly decreasing the transistor current gain. Finally, displacement damage (or bulk damage) can decrease the minority carrier lifetimes in the transistor base, decreasing the current gain. Displacement damage is particularly problematic in environments abundant in protons [4]. [3], [5]

Another important effect in bipolar transistors is the enhanced low-dose-rate sensitivity (ELDRS) effect. For an equivalent dose, a low dose rate can result in significantly more device degradation than a high dose rate. This effect has been found to be limited to bipolar devices, and it contributes to the difficulty of accurately assessing the TID susceptibility of bipolar circuits based on radiation testing. [6]–[8]

In CMOS transistors the main effects of TID are threshold voltage shifts and field-oxide leakage. A TID-induced shift in the threshold voltage of a metal-oxide-semiconductor field-effect transistor (MOSFET) is caused by charge trapping in the gate oxide or oxide/semiconductor interface. When ionizing radiation generates electron-hole pairs in the gate oxide, the high-mobility electrons either recombine or are swept out to the gate electrode via drift. The lower-mobility holes, on the other hand, remain and either recombine or drift to the Si/SiO_2 interface. The holes can tunnel into the Si and

only generate a small, transient current, or the holes can become trapped in the oxide or the interface, altering the transistor performance. The positive oxide-trapped charge causes a negative shift in threshold voltage, making nFETs harder to turn off and pFETs harder to turn on (since the threshold voltage of a pFET is negative). Interface-trapped charge increases the subthreshold swing of MOSFETs, effectively increasing the threshold voltage in nFETs and decreasing the negative threshold voltage in pFETs—making both harder to turn on. It has been found that the threshold shift due to charge buildup in oxides decreases as the gate oxide thickness decreases. In thin oxides trapped charge is greatly reduced by electrons that are able to tunnel through the oxide and liberate the trapped holes. As a result, modern deep submicron CMOS transistors are quite resistant to threshold voltage shifts caused by TID. [1]–[3], [9]–[15]

Although threshold voltage shifts are minimal in modern CMOS technologies, the isolation (or field) oxide of CMOS ICs can still cause appreciable circuit degradation. While the thickness of gate oxides may be on the order of a few nanometers, the thickness of the modern process's field oxide is on the order of hundreds of nanometers. As a result, positive charge can become trapped in the field oxide. A sufficient amount of trapped charge can cause inversion in the surface of the p-type substrate or p-well of an IC. This can result in intra- and inter-device leakage currents. The surface inversion of the p substrate between the source and drain of an nFET creates a conducting channel, increasing the drain-source current of the device, most noticeable in the sub-threshold regime of operation. Similar conduction paths can be created between adjacent nFETs or between nFETs and a nearby n-well. These effects can be particularly pronounced in the shallow-trench isolation (STI) of a modern CMOS technology. If the radiation-induced

leakage is severe enough, these leakage currents can become comparable and/or surpass the intended operating currents of devices, effectively preventing them from turning off. The general impact of increased leakage current is an increase in supply current, although it can also effect analog circuit operation by increasing the bias current of effected transistors. Recent findings, however, indicate that the effects of charge trapping in STI have decreased with CMOS scaling due to higher doping concentrations, which require more charge for surface inversion [16]. [1]–[3], [11]–[13], [15], [17]–[19]

TID effects in analog ICs

Research on the effects of TID on analog ICs has covered a wide range of circuits and systems, including both bipolar and CMOS technologies. Among the most commonly studied (and used) circuits is the operational amplifier (op amp). Since the op amp is one of the fundamental building blocks of an AMS system, it can give a general idea of the TID response of an analog circuit implemented in a particular technology. In many bipolar op amps, radiation testing often revealed catastrophic circuit failure or parametric degradation including increased input offset current, increased input bias current, increased offset voltage, or decreased open-loop gain [4], [20]–[23]. These effects were frequently attributed to the change in internal bias currents caused by TID or gain degradation caused by displacement damage. In many of these designs a single type of transistor—the lateral or substrate pnp—was identified as the most TID-susceptible [6], [23], [24]. In addition, bipolar op amps typically exhibited an enhanced sensitivity to proton radiation, as opposed to gamma radiation, due to the effects of displacement damage [4], [24], [25].

In order to avoid many of the aforementioned radiation vulnerabilities of bipolar analog circuits and take advantage of the increasing TID tolerance of scaled CMOS, this work is focused on radiation effects in CMOS. While in the past large offset voltage shifts and/or catastrophic failure have been reported in CMOS op amps [22], [26], research on the TID dependence of the analog parameters of MOSFETs at the 250-nm, 180-nm, and 130-nm technology nodes indicates that each submicron process is more resilient to TID than its predecessor [12]–[14]. The critical parameters investigated include threshold voltage, transconductance and flicker (or 1/f) noise. As mentioned in the previous section, this increased hardness is due to the thin gate oxides and high doping concentration of deep submicron CMOS processes. Implementing analog designs using the high-voltage, thick-oxide FETs available in a given CMOS process can be an attractive option due to the high voltage headroom, but the thicker oxides and lower doping concentrations—compared to the core, thin-oxide devices—make these transistors far more vulnerable to classical threshold voltage shifts and STI leakage [17], [19].

TID mitigation

The relative insensitivity of modern CMOS transistors to total dose has led to the success of radiation-hardened-by-design (RHBD) circuits. Previously, a common—and potentially expensive—approach to realizing radiation-tolerant ICs was radiation-hardening by process, wherein extra steps were added to a fabrication process to increase the intrinsic tolerance of devices [27]–[32]. With the problem of MOSFET parametric degradation largely solved by the use of thin gate oxides, it is possible to use design and layout techniques to fabricate radiation-tolerant ICs using commercial processes [2], [33].

A widely used RHBD layout technique that solves the issue of radiation-induced source-drain leakage in nFETs is the edgeless (or enclosed/annular) transistor layout. An edgeless transistor is constructed with the drain surrounded by the gate, which is in turn surrounded by the source. This layout eliminates the sidewall edge leakage path between source and drain, thereby making the transistor immune to radiation-induced leakage [17], [34]–[44]. Other layouts have been proposed to eliminate sidewall leakage in nFETs using either a two-poly process [45] or an enclosed-drain layout in which the gate surrounds the drain, but the source is only on a single side [38]. Another popular RHBD layout technique is the use of p+ guard rings to combat the surface inversion of the p substrate that leads to nFET-to-nFET and nFET-to-n-well leakage currents [2], [3], [38], [46], [47]. Some research indicates that the large area overhead associated with this layout technique may not be necessary at the 130-nm node, because significant intra-device leakage was not observed in TID experiments [15], [17].

Apart from the layout techniques that specifically address STI leakage, there are various other RHBD techniques used in analog circuits. In cases where device parameters are expected to shift, the design can be approached in a similar fashion to designing for high process variability. For example, designing bipolar circuits to avoid strong dependence on current gain β insures a certain level of tolerance to degradation [8], [48]. In addition, the use of negative feedback—as would be seen in most op amp applications—can compensate for parametric shifts of devices within the feedback loop [49]. In [23] the most TID-sensitive stages of an op amp were identified as the stages that had asymmetric or unbalanced loading, suggesting that leveraging symmetry and current-matching in an analog design can increase the circuit's hardness.

In this work voltage reference circuits are used to demonstrate radiation-hardening techniques, so it is informative to discuss total dose research on voltage references specifically. Much of the TID experiments performed on voltage references have been largely focused on commercial parts and not custom ICs. In [50], for example, Rax *et al.* published a fairly thorough comparison of the radiation response of various precision voltage references. In general the more complex precision references showed less degradation than the intermediate-precision ICs, which showed an almost linear change in VREF with respect to total dose. In fact, the reference that showed the least amount of degradation was the temperature-regulated buried-Zener reference, the LTZ1000 [51]. The only limiting factor for the LTZ1000-based reference was the use of external op amps for temperature coefficient (tempco) compensation and temperature regulation; these op amps exhibited offset-voltage degradation due to displacement damage, resulting in a significant shift in reference voltage. The resilience of the core reference circuit indicates the potential success of the use of a temperature-regulated reference in a radiation environment. Many of the other references showed appreciable output shifts at a fairly low dose of 20 krad(Si). [50]

The XFET reference by Analog Devices is another commercial, precision voltage reference that was tested for radiation-induced degradation. The circuit uses a similar tempco compensation methodology as the typical bandgap reference, but the primary reference devices are p-channel junction field-effect transistors (JFETs). Changes in the output voltage and line regulation seem to largely indicate degradation in the internal bipolar op amp, but the proprietary nature of the reference precludes further investigation of the mechanisms in the core reference devices [52]. A previous attempt at an RHBD

90-nm CMOS voltage reference relied largely on the use of edgeless transistor layouts and guard rings to eliminate radiation-induced STI leakage. Lateral pnp transistors were used in this design to generate a bandgap reference, and a minimal, current-source based topology was employed to avoid the potential degradation of a complex circuit like an op amp. Radiation testing was not performed, so it is unclear how the pnp transistors would respond to radiation—particularly at low dose rate [47]. Furthermore, the basic bandgap topology is limited to low or intermediate precision, which is why the aim of this work is to employ the concept of on-chip temperature regulation that has achieved high precision in the past [51], [53], [54].

Radiation effects studies on linear voltage regulators have often identified degradation in the voltage reference as the key source of system degradation [55], [56]. In other cases it was the op amp used for the regulation that degraded, leading to output shifts or catastrophic failure [48], [55], [57]. All of these results point to the importance of using a radiation-tolerant core reference and a radiation-tolerant op amp in the feedback loop.

To date, the greatest success seen with the design of a low-voltage RHBD voltage reference is a CMOS reference designed using dynamic-threshold MOS transistors (DTMOSTs) [58]. A DTMOST is simply a transistor with the gate and body connected together, and has shown promise in low-voltage and radiation-tolerant applications [59]–[61]. This design leveraged the relative immunity of a 130-nm CMOS process to threshold shifts. By using edgeless-layout transistors and guard rings, the shift in reference voltage was limited to ± 1.5 mV (0.8%) up to a dose of 44 Mrad(Si), compared to 3% shift in a standard-layout reference [58]. While these results are impressive, the

performance of the design is fundamentally dependent on the 130-nm fabrication process. In other words the design does not advance the state of the art of RHBD analog circuits, it simply reports a good result obtained by using a particular technology node. In this work, radiation hardening techniques are presented that can be applied generally by designers to harden a variety of analog circuits in any fabrication process.

B. Single-event effects

While TID is a radiation effect of accumulation that alters circuit operation, the single-event effect (SEE) is a transient radiation effect that causes perturbations in a circuit. While in digital circuits, SEEs can cause direct data corruption—turning a ‘1’ into a ‘0’, or vice versa—in analog circuits SEEs essentially result in unwanted noise. In this section the basic SEE mechanisms are discussed along with a literature overview of SEEs in analog circuits and mitigation techniques.

SEE mechanisms

A single event (SE) occurs when an ionizing particle comes into contact with a semiconductor. Unlike TID, the effect of a single-event is transient in nature and, thus, does not alter the operation of a circuit—except for the special cases of single-event burnout, gate rupture, and latchup which are not considered in this work. The ion strike begins the charge collection process by first depositing energy in the semiconductor region, which results in electron-hole pair generation. The amount of charge deposited depends on the linear energy transfer (LET) of the ion, the ion’s path length through the material, and the struck material, which is assumed to be silicon for the remainder of this

discussion. Deposited charge can be estimated by the product of LET (represented in pC/µm by accounting for the ion LET and struck material properties) and path length (in µm). If this SE charge is deposited in a simple block of silicon, it will eventually recombine and equilibrium will be restored. However, if the charge is deposited at or near a p-n junction, then separation of charge carrier types, collection of this charge in different semiconductor regions, and propagation to the device terminals occur and a single-event effect is observed. [2], [62], [63]

The primary mechanism by which SE charge is collected is drift across reverse-biased junctions. In this way, minority carriers are collected by device drains and/or wells. Additionally, carriers diffuse away from the high-density ion track, so the drift collection process is assisted by diffusion. The basic drift collection of charge in a reverse-biased p-n junction is illustrated in Fig. 1. The ionizing particle liberates electron-hole pairs along its strike path, and the electric field in the junction's depletion region separates the mobile carriers, sweeping electrons into the n-type region and holes into the p-type region. If, for instance, the n-type region were the drain of an nFET and the p-type region were the grounded p-well, then the result of this strike would be a decrease in the

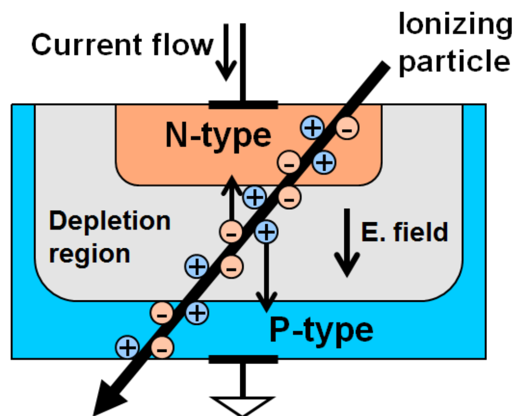


Fig. 1: Collection of charge deposited by heavy ion in a reverse-biased junction.

drain voltage. The magnitude and duration of this drain voltage dip depend on the amount of charge deposited and the circuitry to which the drain is connected. [2], [62], [63]

A single-event upset (SEU) occurs when an SE results in digital data corruption. This can occur in one of two ways: an SE directly flipping the stored bit of a storage element or an SE generating a transient signal that is latched in a storage element as incorrect data. In order to directly flip the bit of a latch, a SE simply needs to deposit sufficient charge to change the state of the latch. However, the latching of a single-event transient (SET) can be a far more complex process due to the effects of transient attenuation, logical masking and temporal masking. The duration of an SET is often used as the primary metric of severity, since the length of a transient directly relates to the probability of it being latched on clock edge [64], [65]. In many cases, an SET may not become latched, thus having zero impact on the system. The binary nature of digital circuitry allows for this relatively simple dichotomy of SET and SEU, but the continuous nature of analog circuitry can blur the line between transient and upset. [2], [62], [63]

Analog single-event transients

An analog single-event transient (ASET) is simply an SE-induced transient in an analog circuit. In analog circuitry an ASET is largely indistinguishable from a legitimate signal, since the effects—like the signals—are continuous and not discrete like in digital logic. This has led to extensive research aimed at characterizing and analyzing ASETs [66]–[71]. In order to determine a threshold for an "analog error," a context for the specifications of a system or application is typically required. While a subcircuit may be

SET-immune in one application, the same subcircuit could be the most vulnerable in a more rigorous application.

Due to the large time constants in typical analog circuits—compared to minimum-dimension digital cells—ASETs can be quite long in duration and large in magnitude. For example, depending on the closed-loop gain of a system an ASET in an op amp exhibited a duration of several microseconds up to milliseconds [72]–[74]. In a high-speed AMS system, ASETs of this duration can corrupt digitized data for many clock cycles [75]. While architecture-level hardening schemes such as error correction can be successfully implemented in digital system, analog circuits require circuit- and system-level hardening to mitigate the impact of ASETs.

SET mitigation

The conventional SET hardening techniques can be viewed as sort of brute-force approaches. One of these techniques is to increase the rate of charge dissipation in a circuit by increasing the transistor drive and bias current [2], [76]. By increasing transistor W/L, the charge deposited by a SE can be more rapidly dissipated, shortening the duration of an SET. This technique can be undesirable due to the area and power penalties of larger transistors. A similar technique is reducing resistor values to mitigate SETs [77]. Another mitigation technique is essentially adding capacitance to a node to reduce the voltage amplitude of an SET. While this technique can successfully reduce the magnitude of an SET, its main drawbacks include significant area and speed penalties. In fact, this technique has been shown to actually elongate SETs [78]. A similar technique involves the use of low-pass filters to attenuate SETs, but—as before—area and speed

penalties are associated with this technique, as well as the additional dynamic power required to quickly charge and discharge the added capacitance [2].

Redundancy can be leveraged in digital logic to discern SETs from legitimate signals. One of the most successful digital RHBD techniques uses three identical blocks that utilize a voter circuit to ensure the correct output, even if one of the blocks is struck by an SE; this technique is called triple-modular redundancy (TMR). Another form of spatial redundancy is seen in the most prominent SEU-tolerant latch design, the dual-interlocked storage cell (DICE) latch [79]. The obvious drawbacks of spatial redundancy techniques are the increase in layout area and dynamic power dissipation. Temporal redundancy can also be used in digital logic to filter out pulses that are shorter than a designed threshold [65]. These temporal filters have an area penalty associated with them and—by their nature—set a hard limit on the maximum operating speed of a circuit.

There are also several layout techniques that seek to mitigate the well/substrate potential modulation caused by SE-deposited charge. The main goal of these techniques is to increase the effectiveness of well contacts. This is mainly done by either increasing the total area of well contacts or decreasing the distance from sensitive devices to well contacts [76], [80]–[84] By mitigating these well/substrate effects, the impact of the strike on one or more transistors can be lessened, resulting in less severe SETs.

While redundancy-based mitigation schemes have seen success in digital circuits, ASET mitigation techniques have historically been limited to the brute force methods of increased drive current and/or increased nodal capacitance, in addition to the aforementioned well-contact techniques. Over the last several years, however, new ASET mitigation techniques have been devised. At the core of many of these techniques is the

multiple-node charge collection—or charge sharing—phenomenon that has become prominent in submicron CMOS processes [80], [81], [85]–[87]. At small device dimensions and spacing, it is possible for the charge deposited by a single strike to be collected by more than one transistor. With a conscientious layout, this effect can be exploited in a differential analog circuit to mitigate ASETs via the circuit's inherent common-mode rejection [88]–[90]. If two transistors on opposite sides of a differential signal path collect a similar amount of charge, then the resulting transient is mostly a common-mode signal that is mitigated by the differential topology. This technique is termed differential charge cancellation (DCC). A similar mitigation scheme has been applied to sensitive nodes in a bias circuit, where charge sharing induces a current mirroring network to provide a compensating current to the node, significantly mitigating the resulting voltage transient. This technique is termed sensitive-node active charge cancellation (SNACC) [78]. Another application of the DCC layout technique is in the gain stage of a folded-cascode op amp, in which the self-biased current-mirroring topology is used to mitigate ASETs in the same manner as the SNACC technique [91]. Similar charge sharing layout techniques have been proposed for digital designs as well [92], [93].

ASETs have been observed to be problematic in voltage references in the past [75]. Since reference voltages are often distributed to many subcircuits in a system, a temporary glitch can have a significant impact on downstream circuits. A voltage reference design may have several high-impedance nodes and fairly large time constants. SETs on these nodes would likely result in multiple-microsecond long transients. In Chapter V, system-level SET mitigation schemes are proposed for voltage reference

designs. The op amp in the reference topology also poses a potential SET vulnerability. However, ongoing work has addressed SETs at the multiple stages of a CMOS op amp [91], [94], [95].

Since AMS systems require some form of front-end sampling, it is also crucial to examine SEEs in discrete-time circuits such as switched capacitors. In the past, switched-capacitor (SC) circuits have been identified as significant SE vulnerabilities in AMS designs such as ADCs [96]. This is largely due to the high-impedance nature of SC circuits. With charge temporarily stored on a capacitor, SE charge deposition can further charge or discharge the capacitor, resulting in a sample error. With the charge stored on a high-impedance node, there is no current source or sink present to dissipate the SE charge. Thus, it is impossible to employ one of the most common RHBD techniques, increasing charge dissipation. In addition, it is also undesirable to increase the node capacitance (another popular RHBD technique) because of the large speed and area penalties associated with such a change. In order to reduce the SE sensitivity of SC circuits with minimal or negligible performance tradeoff, it is necessary to employ a more novel RHBD technique, such as multi-path hardening [97], [98]. In Chapter VI a novel quad-path hardening technique for SC circuits is introduced and validated experimentally [99].

CHAPTER III

VOLTAGE REFERENCE CIRCUITS

Voltage reference circuits are a core building block of any high-performance AMS system. For example, an analog-to-digital converter (ADC) requires a constant voltage to accurately quantize input analog signals, and a digital-to-analog converter (DAC) requires it to quantize output signals. That reference voltage must be stable with respect to temperature and supply voltage so the ADC can precisely quantize the input signal in terms of the least significant bit (LSB). The minimum value of the LSB can be directly determined by the precision of the reference voltage and the signal range. Thus, the precision of a voltage reference can be a limiting factor in a low-voltage design, so it is of the utmost importance to achieve the smallest variation possible.

One of the goals of this research is the development of techniques that would, for instance, enable the design of a radiation-hardened precision voltage reference. While the developed techniques can be applied to a wide range of analog circuits, the voltage reference is used as a case study. This chapter provides background information on conventional voltage reference design, and the concept of using on-chip heating to control the temperature of a reference is also discussed, as this idea is central to the design approach of the research. The chapter ends with an overview of the voltage references designed as part of this research in 180-nm and 40-nm technologies.

A. Basic bandgap reference theory

Voltages in an integrated circuit change with respect to temperature, exhibiting a nonzero *dV/dT*. This first-order linear dependence of voltage on temperature is called the temperature coefficient, or tempco. An ideal voltage reference has a tempco of 0 V/°C, so various tempco cancellation techniques have been developed to combine equal and opposite tempcos in order to achieve a zero-tempco (ZTC), or temperature-independent, voltage. Among the most popular of these techniques is the first-order tempco cancellation seen in the conventional bandgap reference.

The core principle behind the bandgap reference is the temperature dependence of the forward voltage (V_f) of a p-n junction. At a given forward current, V_f exhibits a negative linear dependence on temperature, called a complementary-to-absolute-temperature (CTAT) voltage. In other words the voltage drop across a forward-biased p-n junction has a negative tempco. The V_f tempco also has a dependence on current density in the p-n junction. As current density increases, V_f increases and its tempco becomes less negative. By using two forward-biased junctions at different current densities, the difference of the two CTAT voltages yields a proportional-to-absolute-temperature (PTAT) voltage that can be combined with a CTAT voltage to generate a zero-tempco voltage [100].

Figure 2 shows a basic implementation of a bandgap reference using two diode-connected npn bipolar transistors to implement forward-biased junctions [101]. R_1 and R_2 are identical and Q_2 is scaled to have *n* times the area of Q_1. The high gain of the op amp forces the inputs to be equal, and since $V_X = V_Y$ and $R_1 = R_2$, it follows that $I_1 = I_2$.

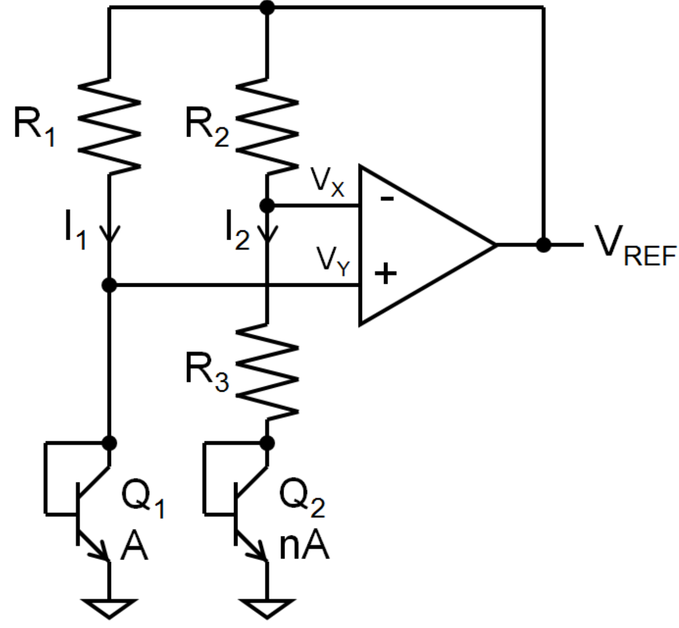


Fig. 2: Basic bandgap reference.

The current-voltage characteristics of the forward-active transistor Q_1 can be used to derive the following expression for V_{BE1} as:

$$I_1 = I_S\, e^{\frac{q\,V_{BE1}}{k\,T}} \rightarrow V_{BE1} = \frac{k\,T}{q}\, ln\left(\frac{I_1}{I_S}\right), \tag{1}$$

and V_{BE2} can be derived as:

$$I_2 = n\, I_S\, e^{\frac{q\,V_{BE2}}{k\,T}} \rightarrow V_{BE2} = \frac{k\,T}{q}\, ln\left(\frac{I_1}{n\,I_S}\right) = \frac{k\,T}{q}\left[\, ln\left(\frac{I_1}{I_S}\right) - ln(n)\right]. \tag{2}$$

Using (1), (2), and the fact that V_Y and V_{BE1} are equal, I_2 can be expressed as:

$$I_2 = \frac{V_{BE1} - V_{BE2}}{R_3} = \frac{1}{R_3}\,\frac{k\,T}{q}\left[ln\left(\frac{I_1}{I_S}\right) - ln\left(\frac{I_1}{I_S}\right) + ln(n)\right] = \frac{k\,T}{q\,R_3}\, ln(n). \tag{3}$$

Using this equation for I_2, the output voltage V_{REF} is:

$$V_{REF} = V_{BE2} + (R_3 + R_2)I_2 = V_{BE2} + \left(\frac{R_2 + R_3}{R_3}\right)\frac{k\,T}{q}\, ln(n). \tag{4}$$

To demonstrate the first-order cancellation of tempcos, the derivative of V_{REF} is taken with respect to temperature, yielding:

$$\frac{dV_{REF}}{dT} = \frac{dV_{BE2}}{dT} + \left(\frac{R_2 + R_3}{R_3}\right)\frac{k}{q}\, ln(n). \tag{5}$$

The derivative of V_{BE2} is negative with respect to temperature (typically around -2 mV/°C), so R_2, R_3, and n can be chosen such that the positive and negative tempcos cancel to yield zero temperature dependence in the reference voltage. For a V_{BE2} tempco of -2 mV/°C, the values $R_1 = R_2 = 10$ kΩ, $R_3 = 1.1$ kΩ, and $n = 10$ yield a zero tempco in V_{REF} at 27 °C. Assuming $V_{BE2} = 0.6$ V, the value of V_{REF} in this circuit is approximately 1.2 V. This is nearly the bandgap voltage of silicon, giving the reference circuit its name.

The precision of the bandgap reference is limited by second-order dependence on temperature (or the curvature) of the reference voltage. Second-order temperature dependence of V_{BE} and other terms in the bandgap voltage cause curvature in the temperature response, resulting in positive or negative tempcos at temperatures above or below the ZTC temperature. As a result typical bandgap reference temperature drift is on the order of 25-50 ppm/°C, where ppm is parts per million (1 ppm = 0.0001%) [102]. Over a temperature range of 100 °C, for example, a 50 ppm/°C tempco would yield approximately 6 mV of reference variation. Assuming ½ LSB ≥ 6 mV and a signal range of 2 V, this would make the reference suitable for a 7-bit ADC, where each LSB is worth ~16 mV. While the conventional bandgap is fairly limited in precision, various curvature-correction techniques have been developed in the past to extend the tempco cancellation across a wider temperature range, lowering the reference tempco [103], [104].

B. Integrated low-voltage CMOS reference topologies

To avoid the radiation vulnerabilities of bipolar transistors and take advantage of the radiation tolerance of modern CMOS, the reference design in this work does not use

bipolar transistors as in the bandgap reference. Integrated CMOS references, in particular, are investigated. The two references presented in this section employ the basic bandgap topology, but use CMOS devices rather than bipolar transistors to generate and cancel tempcos.

An RHBD voltage reference was fabricated in a 0.13-μm CMOS technology using the dynamic-threshold MOS transistor (DTMOST) as the reference device in place of the bipolar transistors in a bandgap topology [58]. This DTMOST reference had an output voltage of 412 mV, which exhibited an untrimmed tempco of less than 490 ppm/°C (125 ppm/°C with trim). The details of the radiation response of this reference will be discussed in Chapter V. The fundamental device of the reference, the DTMOST, is a p-type MOSFET (pFET) with the wiring shown in Fig. 3; the gate, drain, and body are grounded, while voltage is applied to the source. The DTMOST exhibits exponential current-voltage characteristics over the voltage range of weak inversion in the channel, and the voltage across the DTMOST has a negative tempco, making it a suitable replacement for the p-n junction in the bandgap reference [58]. In this regime of operation, the forward-biased source/body junction contributes negligibly to current consumption, meaning channel conduction dominates device operation. For further

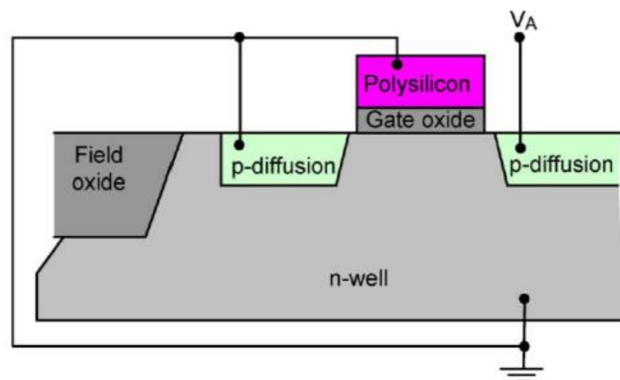


Fig. 3: Dynamic-theshold MOS transistor (DTMOST) [58].

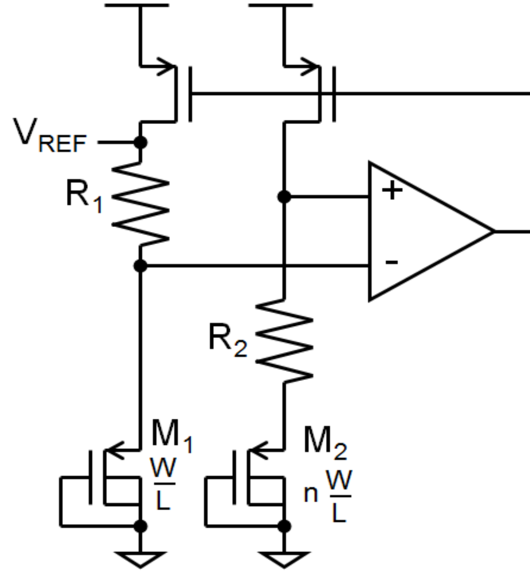


Fig. 4: DTMOST reference.

details on the operation of the DTMOST, the reader is referred to [58]–[61].

Figure 4 shows the DTMOST reference circuit using a topology very similar to the basic bandgap reference previously discussed. M_1 and M_2 are both DTMOSTs, and M_2 is scaled to be n times wider than M_1, with equal lengths. The pFET current mirror sources the same current through R_1 and R_2, and the output voltage V_{REF} can be expressed as:

$$V_{REF} = V_{S1} + \frac{R_1}{R_2}(V_{S1} - V_{S2}), \tag{6}$$

where V_{S1} is the voltage across M_1 and V_{S2} is the voltage across M_2. Taking the derivative of (6) with respect to temperature yields the temperature dependence of the reference voltage:

$$\frac{dV_{REF}}{dT} = \frac{dV_{S1}}{dT} + \frac{R_1}{R_2}\frac{d(V_{S1}-V_{S2})}{dT}. \tag{7}$$

For simplicity, the resistors are assumed to be constant across temperature.

As in the conventional bandgap, the tempco of a single DTMOST voltage is negative (around -0.8 mV/°C), and this tempco becomes more negative as current density

decreases, yielding a positive tempco in the voltage $(V_{S1} - V_{S2})$. Thus, R_1 and R_2 can be chosen such that the positive and negative tempcos cancel, resulting in a temperature-independent (to first order) reference voltage. The DTMOST reference is a suitable for a precision RHBD reference circuit due to its low-voltage operation, CMOS-compatibility, and demonstrated radiation hardness [58], [60].

Another low-voltage CMOS reference design proposes the use of n-type MOSFETs (nFETs) in weak inversion for tempco cancellation. It was observed that in this region of operation an nFET exhibits exponential I-V characteristics very similar to those of a bipolar transistor. Moreover, the gate-source voltage of a weak-inversion nFET, V_{GS}, has a negative tempco that becomes more negative as current density decreases, making it a suitable reference device to be used in a bandgap reference topology. Simulations of a 0.18-µm implementation of this reference demonstrated an output voltage of 512 mV with a temperature drift of 54 ppm/°C [105].

Figure 5 shows an nFET voltage reference circuit that resembles the conventional bandgap. Assuming the same current flows through R_1 and R_2, the reference voltage can be expressed as:

$$V_{REF} = V_{GS1} + \frac{R_1}{R_2}(V_{GS1} - V_{GS2}). \tag{8}$$

The derivate of V_{REF} with respect to temperature is:

$$\frac{dV_{REF}}{dT} = \frac{dV_{GS1}}{dT} + \frac{R_1}{R_2}\frac{d(V_{GS1} - V_{GS2})}{dT}. \tag{9}$$

The temperature dependence in (9) shows how R_1 and R_2 can be chosen to obtain a zero-tempco reference voltage, since V_{GS1} has a negative tempco (around -0.4 mV/°C) and $(V_{GS1} - V_{GS2})$ has a positive tempco.

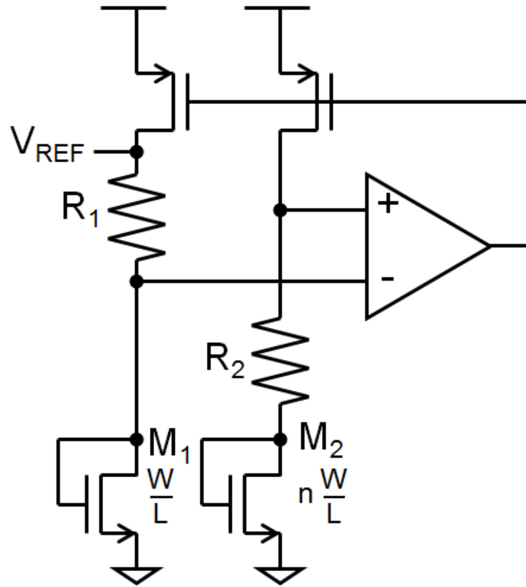


Fig. 5: NFET reference.

The nFET reference is not particularly suitable for an RHBD reference since the nFETs themselves are susceptible to edge leakage. Although using edgeless layout transistors (ELT) eliminates the effects of radiation-induced leakage the DTMOST-based reference is the main focus of this work. The nFET reference does, however, offer a good comparison with the DTMOST reference.

C. Temperature regulation of voltage references

Since both of the references discussed in the previous section still employ first-order bandgap reference architectures, their precision is similarly limited by the second-order temperature drift. In this section a method for dramatically reducing temperature drift is discussed. The method uses on-chip heating in a feedback loop to control the temperature of the reference, thereby minimizing temperature drift in the reference voltage.

Examples in industry and literature

Among the earliest applications of temperature regulation in voltage references is the buried-zener reference. Buried-zener references, as in Fig. 6, can typically achieve temperature drift on the order of 1-10 ppm/°C. Some of the original findings on thermal stabilization showed that the temperature drift of a buried-zener reference could be reduced to 0.3 ppm/°C by regulating the die temperature with an on-chip heater in a control loop [106], [107].

One of the most prominent commercial examples of a temperature-regulated buried-zener reference is Linear Technology's LTZ1000 [51]. As shown in Fig. 7, the

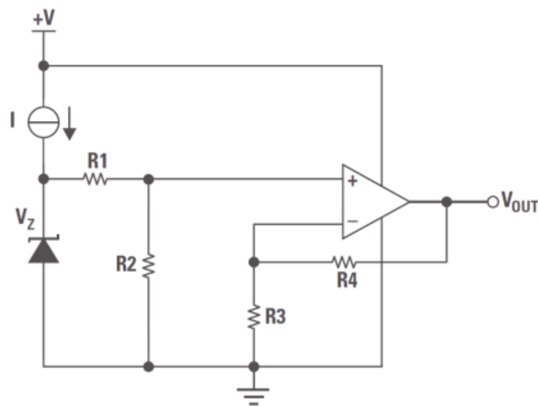


Fig. 6: Basic buried-zener voltage reference [101].

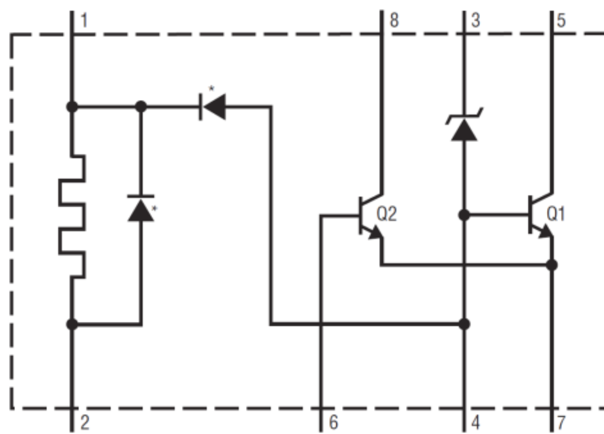


Fig. 7: LTZ1000 components [51].

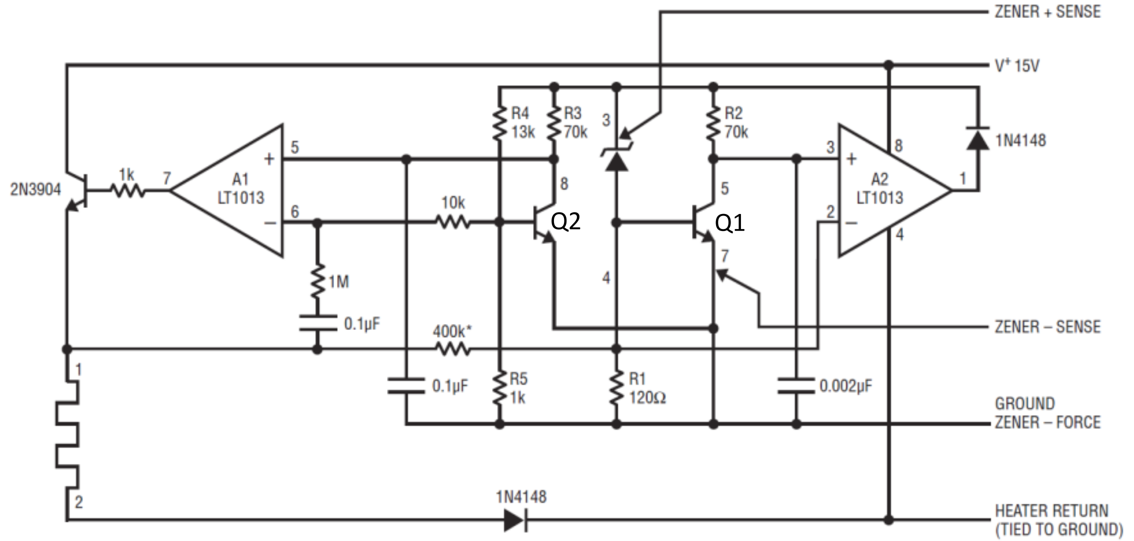


Fig. 8: Temperature-regulated 7-V reference using the LTZ1000 [51].

LTZ1000 consists of a 7-V buried-zener diode, two npn transistors, and a heater. The reference voltage is taken across pins 3 and 7. Q1 provides tempco compensation with the buried-zener diode because V_{BE} has a negative tempco (around -2 mV/°C) and the zener breakdown voltage has a positive tempco (around 2 mV/°C). Q2 can be used as a temperature sensor in the temperature control loop with the heater. Combined with the proper external components, the LTZ1000 can achieve temperature drifts as low as 0.05 ppm/°C [51].

Figure 8 shows a 7-V, temperature-regulated voltage reference using the LTZ1000. Op amp A2 on the right provides an electrical feedback loop with the zener diode and Q1 that regulates the output voltage (measured at node labeled 'ZENER + SENSE'). Op amp A1 on the left provides the thermal feedback loop, controlling the power dissipated by the heater based on the temperature sensed by Q2. The temperature of the LTZ1000 die follows:

$$T_{die} = T_{ambient} + R_{th} \, P_{heater}, \tag{10}$$

where R_{th} is the LTZ1000 thermal resistance in °C/W, and P_{heater} is the power dissipation in the heater. The thermal resistance is a measure of temperature rise generated by power dissipation and thermal isolation of the die in the package. The thermal resistance of the LTZ1000A is 400°C/W, and the heater resistance is typically 250 Ω.

The 7-V reference of Fig. 8 was simulated in Spectre with and without the thermal feedback loop to demonstrate the benefit of temperature regulation. Custom models were developed for the heater and zener diode. The heater model behaves electrically like a resistor, but it outputs a signal representing the rise in chip temperature, calculated based on power dissipation. The zener model is a basic zener model with an added "trise" terminal that indicates the temperature of the zener above ambient temperature. The npn models were also basic models with an extra "trise" terminal to indicate the temperature above ambient. By connecting the heater's output (rise in temperature) to the temperature inputs of the three LTZ1000 components, the on-chip heating was modeled. For this simple demonstration, the op amp models were ideal.

Figure 9 shows a temperature sweep of the reference voltage with and without thermal feedback. When there is no thermal feedback, the temperature drift (the slope of the line) is 1.9 mV/°C, which is essentially the tempco of the buried-zener breakdown voltage. With thermal feedback the temperature drift is reduced to 30 pV/°C, an unrealistically low value due to the ideal nature of the models. The thermal feedback curve is only flat between -90°C and 140°C, indicating the two limits on temperature control. The thermal feedback loop basically sets the die temperature to 140°C, and it maintains that temperature until the ambient temperature is either too high or too low. When the ambient temperature surpasses 140°C the temperature drift looks identical to

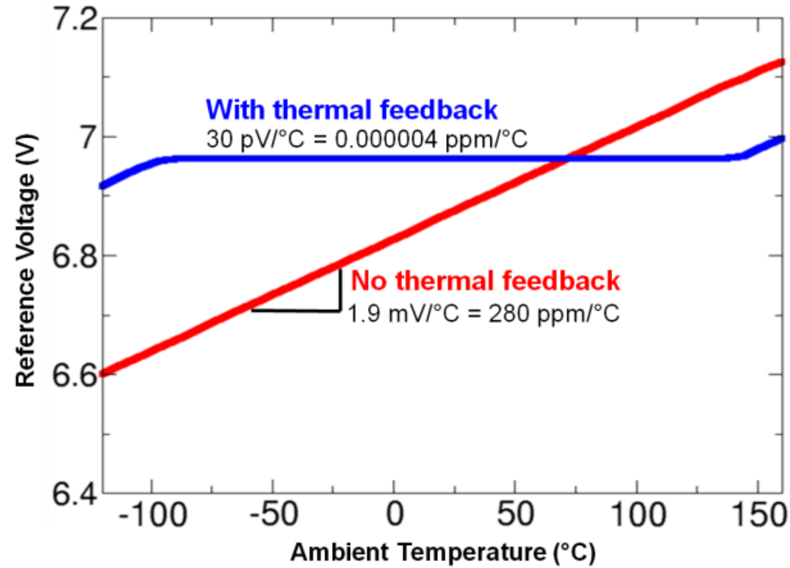


Fig. 9: Simulation of 7-V reference of Fig. 8 with and without thermal feedback.

that of the unheated reference, indicating that the heater is not affecting the temperature. This is because the heater cannot reduce the die temperature to 140°C, so it consumes no power. The more than 100-mV offset between the two voltages in this temperature range is due to the change in bias when the thermal control portion of the circuit is removed. When the ambient temperature drops below -90°C, the heater is at its maximum power dissipation. With a 15-V power supply, the maximum voltage across the heater is approximately 12 V, yielding a maximum power of 576 mW—corresponding to 230°C rise in temperature using the thermal resistance of 400°C/W. At -90°C ambient the heater can barely maintain 140°C on the die, but at lower temperatures the heater can only offset the temperature by 230°C and not negate the drift. Therefore the range of temperature regulation is ultimately set by maximum power dissipation, but the maximum temperature can be altered by changing the design of the temperature control loop.

The main drawbacks of the buried-zener reference are the unavailability of buried-zener diodes in most CMOS processes and the high supply voltages required.

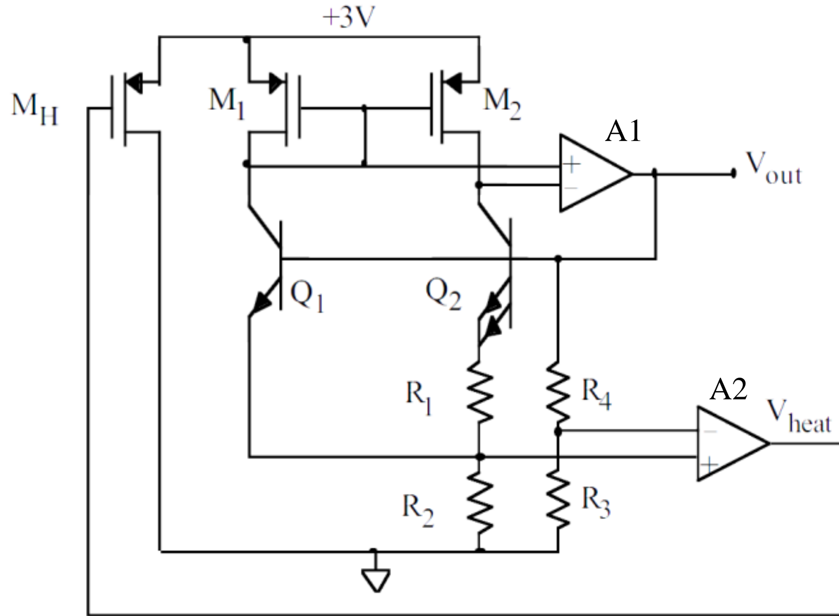


Fig. 10: Temperature-regulated bandgap reference [53].

However, the application of thermal stabilization is not limited to buried-zener references. For example, in [53] the temperature drift of a bandgap voltage reference was reduced from 400 ppm/°C to 9 ppm/°C by adding temperature regulation. Furthermore, micromachining techniques were used to physically isolate the bandgap circuit from the rest of the die, increasing the thermal resistance to 53,000°C/W, compared to a typical value of 200°C/W. This high thermal resistance allows the circuit substrate to be heated with low power dissipation in the heater (1 mW generates 53°C rise in temperature) [53].

The temperature-regulated bandgap reference is shown in Fig. 10. As in the LTZ1000 reference, there are two feedback loops present. Op amp A1 forms the fundamental feedback loop of the core bandgap reference and op amp A2 forms the temperature control loop. The positive terminal is connected to the PTAT voltage between R_1 and R_2, and the negative terminal is connected to a voltage divider of the reference voltage (a low-tempco voltage compared to the PTAT voltage). The temperature at which the PTAT voltage and low-tempco voltage are equal is the set point

for thermal regulation. The output of A2 drives the pFET MH, which is the heater. The die temperature is increased by dissipating power in MH, heating the other devices on the circuit. It is clear from this circuit that adding thermal regulation to a very simple reference drastically improves the precision [54].

Modeling techniques

When designing a temperature-regulated voltage reference it is useful to be able to model the thermal feedback. This significantly aids in both the design of the control loop and the prediction of the system outputs. Before discussing modeling techniques, it is useful to perform a generalized analysis of the temperature-regulated voltage reference. An illustration of a first-order voltage reference without thermal regulation is presented in Fig. 11(a). The input to the system is the ambient temperature, and positive- and negative-tempco voltages are summed to generate VREF with only second-order temperature dependence, as indicated by the curvature of the temperature response. This circuit is called the reference core. The positive-tempco voltage which is proportional to absolute temperature (PTAT) can be expressed as:

$$V_{PTAT} = V_{PTAT0} + \alpha\, T, \tag{11}$$

where V_{PTAT0} is the voltage at 0°C and α is the first-order tempco. The second-order tempco of the voltage is ignored because it is much smaller than α. The reference output can be expressed as:

$$V_{REF} = V_{REFztc} + \beta\, (T - T_{ztc})^2, \tag{12}$$

where V_{REFztc} and T_{ztc} are the voltage and temperature at which the tempco is zero (indicated in Fig. 11) and β is the second-order tempco (the sum of the second-order

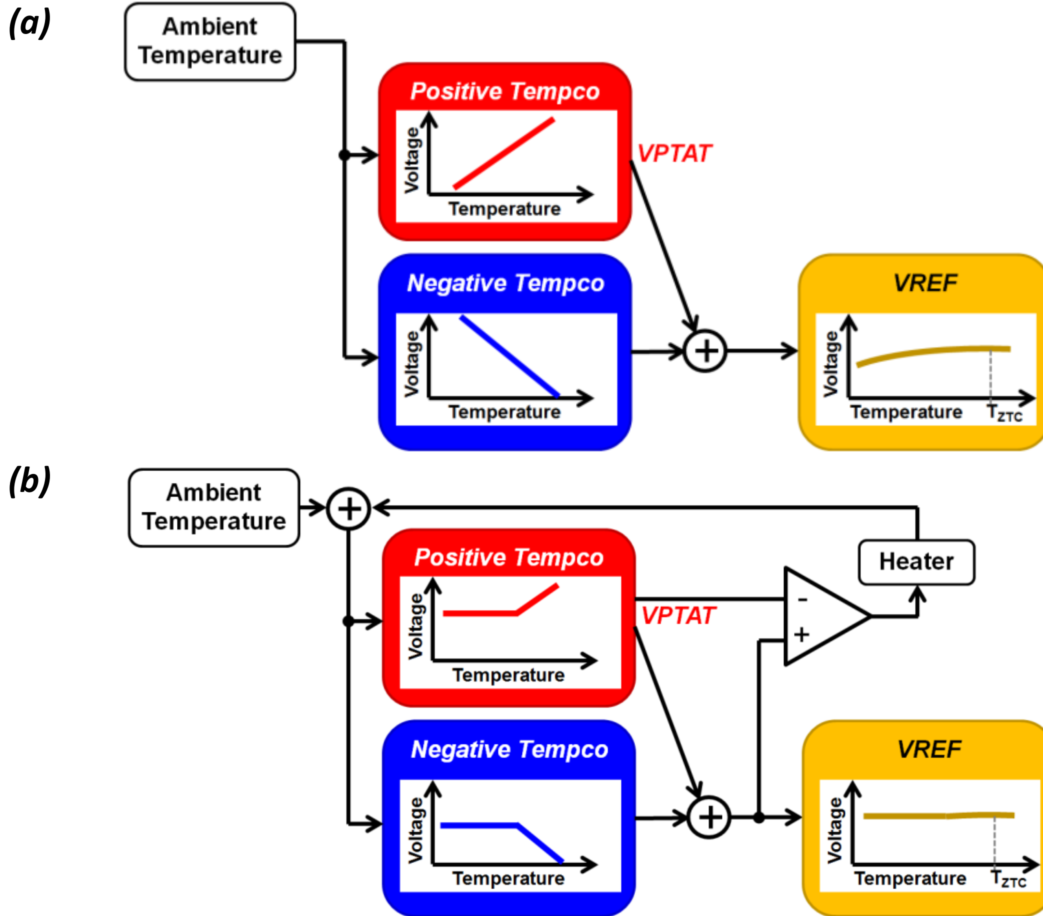


Fig. 11: Functional illustration of first-order voltage reference (a) without and (b) with thermal regulation. The label 'T_{ZTC}' indicates the temperature at which the VREF tempco is zero.

tempcos of the positive- and negative-tempco voltages). It is this second-order temperature dependence that ultimately limits the precision of the voltage. While curvature compensation techniques can eliminate this dependence, thermal regulation can theoretically eliminate all temperature dependence.

The temperature-regulated reference illustrated in Fig. 11(b) is simply the same first-order reference core with a thermal feedback loop. The VPTAT and VREF voltages are compared by an op amp that controls a heater. The die temperature, which determines the values of the positive- and negative-tempco voltages, is simply the ambient

temperature ($T_{ambient}$) plus the rise in temperature due to power dissipated in the heater (T_{rise}):

$$T_{die} = T_{amb} + T_{rise}. \tag{13}$$

Assuming the gain from the op amp input voltages to the heater output is the thermal gain A_{th} (in °C/V), the temperature increase can be expressed as:

$$T_{rise} = A_{th}(V_{REF} - V_{PTAT}). \tag{14}$$

Substituting (11) for V_{PTAT} and (12) for V_{REF} yields:

$$T_{rise} = A_{th}(V_{REFztc} - V_{PTAT0}) + A_{th}[\beta\,(T_{die} - T_{ztc})^2 - \alpha\, T_{die}]. \tag{15}$$

Because $\beta T^2 << \alpha T$, the second-order term can be ignored, and substituting (13) for T_{die} yields:

$$T_{rise} = A_{th}(V_{REFztc} - V_{PTAT0}) - \alpha A_{th}T_{amb} - \alpha A_{th}T_{rise}. \tag{16}$$

Grouping the T_{rise} terms together and assuming the loop gain $\alpha A_{th} >> 1$ the final expression for the heat generation is:

$$T_{rise} = \frac{A_{th}}{1+\alpha A_{th}}(V_{REFztc} - V_{PTAT0}) - \frac{\alpha A_{th}}{1+\alpha A_{th}}T_{amb} \approx \frac{1}{\alpha}(V_{REFztc} - V_{PTAT0}) - T_{amb}. \tag{17}$$

Since $(V_{REFztc} - V_{PTAT0})/\alpha$ is a constant, the derivative of T_{rise} with respect to T_{amb} is equal to -1, meaning the increase in temperature compensates for changes in the ambient temperature. The effect this has on the die temperature can be seen by differentiating (13):

$$\frac{\partial T_{die}}{\partial T_{amb}} = \frac{\partial T_{amb}}{\partial T_{amb}} + \frac{\partial T_{rise}}{\partial T_{amb}} = 1 - 1 = 0. \tag{18}$$

Thus the die temperature is constant despite changes in ambient temperature. The die temperature regulated by the thermal feedback is the first term in (17):

$$T_{die} = \frac{1}{\alpha}(V_{REFztc} - V_{PTAT0}). \tag{19}$$

Thus the relative values of V_{REFztc} and V_{PTAT0} as well as the tempco α can be designed to obtain a particular die temperature.

One of the limitations of thermal regulation is the maximum rise in temperature that can be generated on a chip $T_{rise,max}$, which is limited by the maximum power dissipation. If the ambient temperature is less than ($T_{die} - T_{rise,max}$) then the thermal regulation will only offset the die temperature by the maximum rise in temperature. Likewise, if the ambient temperature is above the designed die temperature, then the heater dissipates no power and the die temperature matches the ambient temperature. The final unified die temperature equation incorporating these limitations is:

$$T_{die} = \begin{cases} T_{amb} + T_{rise,max}, & \text{for } T_{amb} \leq \frac{1}{\alpha}(V_{REFztc} - V_{PTAT0}) - T_{rise,max} \\ T_{amb}, & \text{for } T_{amb} \geq \frac{1}{\alpha}(V_{REFztc} - V_{PTAT0}) \\ \frac{1}{\alpha}(V_{REFztc} - V_{PTAT0}), & \text{otherwise.} \end{cases} \quad (20)$$

The temperature-regulated reference voltage plotted in Fig. 11(b) is flat in one region and slightly curved in the other; showing the operating regions of active temperature regulation and zero power dissipation in the heater.

Now that the functionality of the thermal feedback loop has been analyzed, two behavioral modeling approaches can be discussed. The first model of the thermal feedback loop is shown in Fig. 12, with the separate electrical and thermal domains of the model indicated. In the thermal domain, temperature is represented using voltage. The control voltages V_{REF} and V_{PTAT} are both modeled with voltage sources. The reference voltage is modeled as a constant DC source equal to the zero-tempco voltage, and a voltage-controlled voltage source (VCVS) is used in series with a DC source to model V_{PTAT}. The op amp can be ideal or the actual op amp design, and the heater is

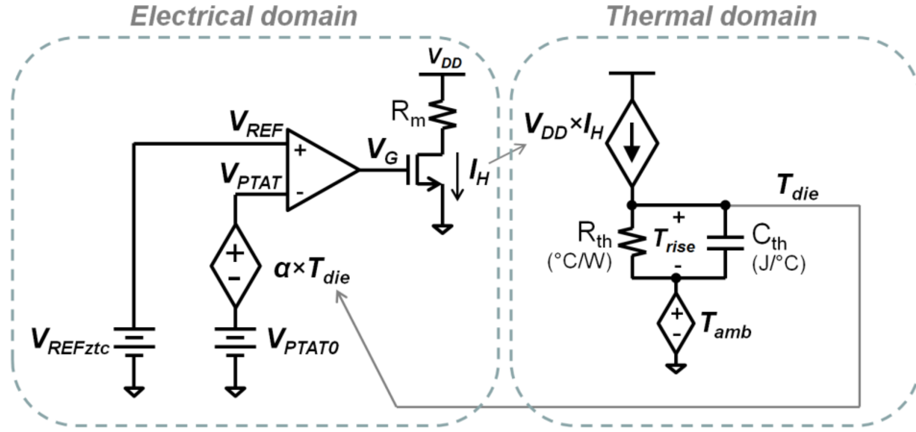


Fig. 12: Behavioral model of thermal feedback loop using voltage sources for V_{REF} and V_{PTAT}.

implemented with a large W/L nFET; R_m represents parasitic metal resistance. A standard practice in electro-thermal modeling is representing power dissipation with current and representing temperature with voltage. Thus the thermal resistance R_{th} (°C/W) and capacitance C_{th} (J/°C, for transient simulations) of the chip can be modeled with a resistor and a capacitor [54]. The voltage drop across R_{th} is equal to the power dissipated by the heater multiplied by R_{th}, and this voltage T_{rise} represents the resulting rise in temperature. A voltage source with 1-to-1 dependence on the ambient temperature supplies the thermal ground equal to T_{amb}. Thus the die temperature is the sum of ambient and the rise in temperature caused by the heater, $T_{amb} + T_{rise} = T_{die}$. This voltage representing die temperature is fed back to the V_{PTAT} VCVS to model the die temperature dependence. Thus the electro-thermal loop is closed. This entire model can be constructed using basic Spice components, and it can all be run in the same simulation.

This model was used to simulate thermal feedback of a voltage reference designed in the UMC 40-nm process. The reference voltage was 457 mV and the PTAT voltage was 361 mV at 0°C with a 1.18 mV/°C tempco. The temperature response of these voltages is plotted in Fig. 13 without thermal feedback (open-loop). The thermal gain A_{th} of the circuit can be computed from the open-loop response of the heater, but it can be

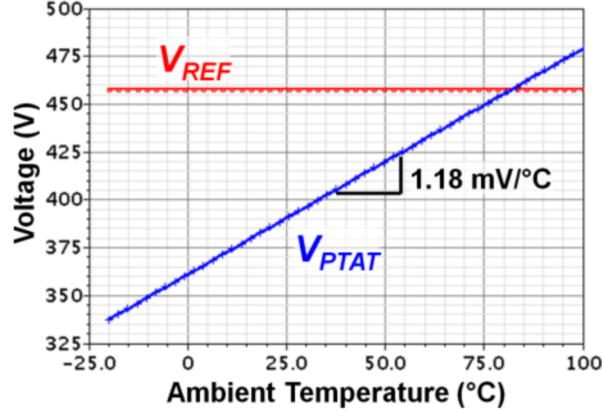


Fig. 13: Open-loop (no thermal feedback) temperature response of model of 40-nm voltage reference using behavioral model of Fig. 12.

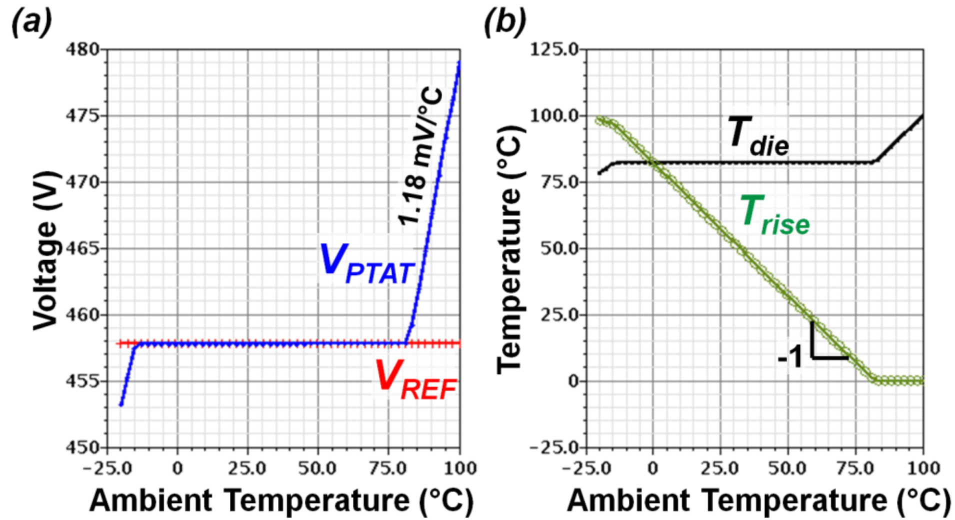


Fig. 14: Closed-loop (with thermal feedback) temperature response of model of 40-nm voltage reference using behavioral model of Fig. 12. (a) Control voltages, (b) rise in temperature and the resulting die temperature.

expressed analytically as:

$$A_{th} = V_{DD}\, R_{th}\, G_m\, A, \tag{21}$$

where G_m is the linearized large-signal transconductance of the heater nFET and A is the open-loop gain of the op amp. From the open-loop simulation, the thermal gain is 1.49×10^6 °C/V, and therefore the loop gain αA_{th} is 65 dB. When the thermal feedback loop is closed, the temperature-regulated response is plotted in Fig. 14. The values for the simulation are R_{th} = 100°C/W, R_m = 5 Ω, and V_{DD} = 3.3 V. The die temperature feedback is apparent in the close grouping of V_{PTAT} to V_{REF} between -15 and 82°C. The

thermal-domain response in Fig. 14(b) indicates that the regulated die temperature was 82°C, which agrees closely with equation (19). At ambient temperatures above 82°C, T_{die} tracks the ambient temperature and T_{rise} is 0°C; the lack of thermal feedback in this range causes V_{PTAT} to diverge from V_{REF}. The divergence of the two voltages at -15°C indicates that the increase in temperature is (82 + 15) = 97°C. The model validates the presented thermal loop analysis.

The voltage-source-based model is adequate in simulating the feedback loop, but the assumption of a constant reference voltage prevents the model from predicting the effect of thermal regulation on the primary system output V_{REF}. The solution to this problem involves the use of Verilog-A. Verilog-A is an analog hardware description language that is particularly useful for behavioral modeling of analog circuits. Specifically, the "table" function in this language is used to enhance the thermal control model. This function references a two-column text file in which the first column holds the input values and the second column holds the output values. Given an input value, the "table" function interpolates based on the values in the text file to determine the appropriate output value. By representing the temperature responses of V_{REF} and V_{PTAT} in text files—with temperature as the first column and voltage as the second—the "table" function can be used to model the temperature response of these circuits in Verilog-A. The benefit of this is that the effective temperature inside the Verilog-A module can be altered by an external input, unlike the Process Design Kit (PDK) transistor models provided by a foundry. Therefore, a "trise" input can be added to the Verilog-A module. Thus, the circuit temperature is set to (T_{amb} + T_{rise}), and then the output voltage is

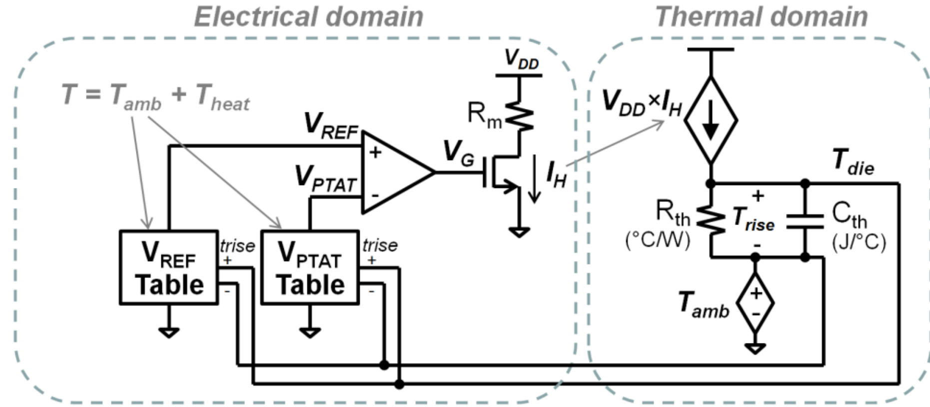


Fig. 15: Behavioral model of thermal feedback loop using Verilog-A tables for V_{REF} and V_{PTAT}.

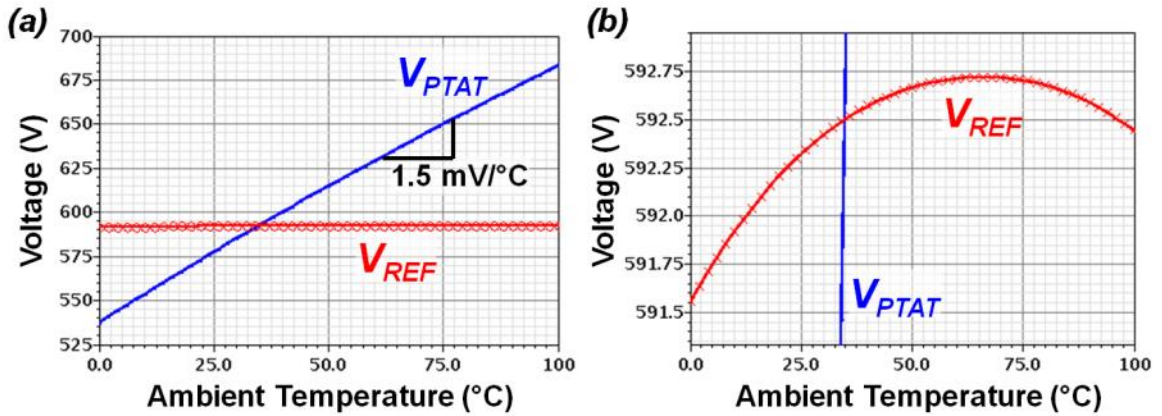


Fig. 16: Open-loop (no thermal feedback) temperature response of model of voltage reference in 180-nm process using behavioral model of Fig. 15. Plot in (b) is simply zoomed in on V_{REF} in (a).

determined from by "table" function. By parameterizing the V_{REF} and V_{PTAT} outputs to temperature, the heating of these circuits can be modeled in Verilog-A.

The thermal feedback model using Verilog-A table functions for V_{REF} and V_{PTAT} is presented in Fig. 15. The thermal domain of the model is similar to that of Fig. 12, except the T_{rise} signal is directly fed back to the Verilog-A models. Inside the Verilog-A models the heater-generated rise in temperature is added to the ambient temperature to compute the output voltages. The Verilog-A models constitute the primary difference between the two behavior electro-thermal models. The open-loop simulation results of this model for a reference designed in IBM 180-nm are plotted in Fig. 16. The plotted voltages are the outputs of the Verilog-A table functions, so they represent the actual

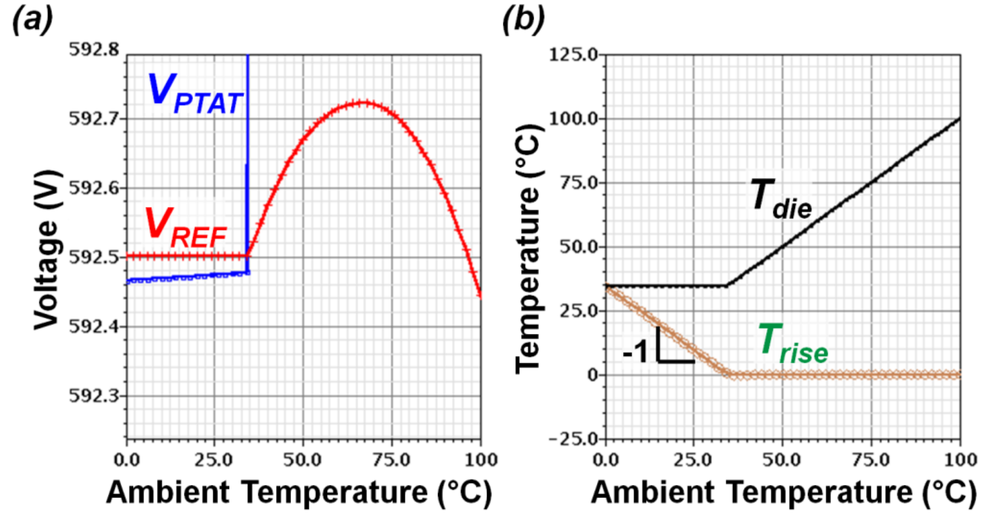


Fig. 17: Closed-loop (with thermal feedback) temperature response of model of voltage reference in 180-nm process using behavioral model of Fig. 15. (a) Control voltages, (b) rise in temperature and the resulting die temperature.

response. The y-axis is zoomed in on V_{REF} in Fig. 16(b) to show the curvature. Although the voltage only varies by 1.16 mV (0.2%), the goal of the thermal feedback is to limit the variation to 0.05%. The two control voltages intersect at 35°C, indicating the temperature for regulation. The thermal gain A_{th} of this circuit is 21×10^6 °C/V, and the loop gain αA_{th} is 90 dB. Using V_{DD} = 5 V, R_{th} = 100°C/W, and R_m = 1 Ω, the thermal feedback loop was simulated, and the results are plotted in Fig. 17. The reference voltage in Fig. 17(a) is flat from 0 to 35°C, and the original curvature is evident from 35 to 100°C because the targeted die temperature is exceeded. Even with this modest rise in die temperature, the reference voltage variation is only 275 μV (0.046%). Interestingly the offset voltage of the op amp can be seen in the difference between V_{REF} and V_{PTAT}, which is on the order of 30 μV, with a shallow slope of 320 nV/°C. Even this minimal drift is pessimistic because the op amp and the heater itself are actually outside the thermal control loop in this simulation. The temperature of PDK transistor models cannot be independently controlled during a simulation, so they simply operate at ambient temperature. The thermal-domain response in Fig. 17(b) shows the expected flat die

temperature below 35°C and tracking with ambient temperature above 35°C. These results demonstrate the effectiveness of this modeling technique in predicting the impact of thermal regulation on the circuit response itself. The temperature responses of circuits can be essentially plugged into an electro-thermal simulation with real-time thermal feedback handled inside Verilog-A. This model is still fairly simplified, assuming equal temperature across the entire die area occupied by the circuit, which is only realistic if the chip packaging has a particularly high thermal resistance. A more sophisticated and computationally intensive model would be required to account for on-chip thermal gradients.

The primary drawback of thermal regulation is the power requirement. Depending on the thermal resistance, the heater must dissipate appreciable power to generate a sufficient rise in die temperature. In [53] and [54] the heated bandgap circuits were physically isolated using micromachining techniques, achieving thermal resistance values in the 53,000°C/W range. In this design, 1 mW of power in the heater generates a 53°C rise in temperature. However, in typical IC packages the thermal resistance is less than 200°C/W, so considerably more power is required—e.g., assuming R_{th} of 200°C/W, 265 mW of power in the heater generates a 53°C rise in temperature. The power-reduction technique used in the presented temperature-regulated reference (Fig. 16 and Fig. 17) is designing the reference to require minimal heating to achieve a particular level of precision. By designing the reference voltage to minimize voltage drift to 0.05% from 35 to 100°C, the heater can simply maintain a fairly low temperature of 35°C to limit the reference drift to 0.05% at ambient temperatures below 35°C. The highest level of precision would clearly be achieved if the reference were heated at 100°C, thereby

eliminating the temperature drift of the voltage at temperatures below 100°C. This is the method used in the LTZ1000, but this is only suitable when a high thermal resistance is achieved because of the power required.

Operating an IC at an elevated temperature via thermal regulation can also significantly impact the lifetime of the part. Since the on-chip rise in temperature is generated by high levels of DC current consumption, the temperature-regulated reference is susceptible to interconnect failure caused by electro-migration. The median time to failure (in hours) due to electro-migration predicted by Black's equation is:

$$MTTF = A\,J^{-2} exp\left(\frac{Q}{kT}\right), \tag{22}$$

where A is a constant based on material and geometry, J is current density (A/cm^2), Q is activation energy (eV), k is the Boltzmann constant, and T is temperature [108]–[110]. The MTTF has an exponential dependence on the operating temperature. This dependence highlights another benefit of the design for minimal heating in Fig. 16 and Fig. 17. Assuming a constant current density and 1-eV activation energy, reducing the operating temperature of an IC from 100°C to 35°C increases the MTTF by a factor of 710. Therefore, designing the reference with minimal heating is a key factor in maximizing the lifetime.

Since the MTTF also shows a strong dependence on the current density, it is another parameter to minimize in the design of a temperature-regulated reference. The primary means for minimizing current density is the width of the heater metal lines. The electro-migration layout rules of a PDK provide guidelines for avoiding electro-migration in high-current lines. A further reduction in current density can be achieved by using I/O transistors for heating circuitry. These transistors have thicker oxides than the primary

core devices in a process, and can operate with higher voltages. Since the only requirement for heating is power dissipation, the required current decreases if the voltage increases. Assuming all other parameters constant, the decrease in current density that results from operating on 5 V (I/O voltage in 180-nm process) rather than 1.8 V (core voltage in same process) increases the MTTF by a factor of $(5/1.8)^2 = 7.7$. Therefore it is critical to minimize current density in metallization through layout and the use of thick-oxide transistors.

D. Voltage reference designs

Three voltage reference test chips were taped out in the following bulk CMOS processes: IBM CMHV7SF 180 nm, UMC 40 nm, and IBM CMRF7SF 180 nm. The individual components of the DTMOST and nFET voltage references discussed in Section B were fabricated on the first 180-nm test chip (in the CMHV7SF process). For these first-pass designs, the reference circuits were not temperature-regulated, although some heating elements were included in the test chip layout. On the 40-nm chip, eight different temperature-regulated voltage reference topologies were fabricated, with single-event mitigation as the primary objective. Finally, the second 180-nm test chip (in the CMRF7SF process) includes two RHBD voltage reference designs with thermal regulation. In this section a brief overview of each reference design is presented along with simulation and experimental results of the temperature responses.

Test structures on first-pass 180-nm chip

On the first 180-nm test chip, voltage reference components were individually laid out for characterization. By externally wiring together the components, different voltage reference topologies were achievable. Having direct access to each component was crucial in determining how to harden the voltage reference. The components on the test chip were:

- DTMOSTs and diode-connected nFETs in standard and enclosed layouts
- Two matched pairs of pFET current mirrors
- Matched pairs of p+ polysilicon (poly) resistors with resistances of 31 kΩ, 61.5 kΩ, and 123 kΩ
- Four complementary folded-cascode op amps.

These components were used to implement the DTMOST-based and nFET-based voltage reference topologies in Fig. 18. The resistors R1 and R2 in each design are both implemented using the bank of matched-pair resistors with unit cells of 15.5 kΩ, and the op amps and current mirrors are the same. The only unique components in the two designs are the DTMOST and nFET reference devices. Symmetric layouts based on unit

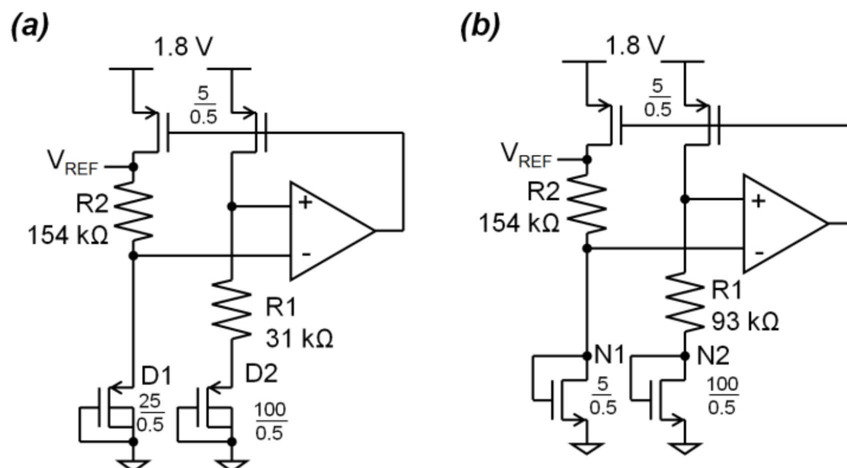


Fig. 18: (a) DTMOST and (b) nFET reference designs fabricated in IBM 180-nm process.

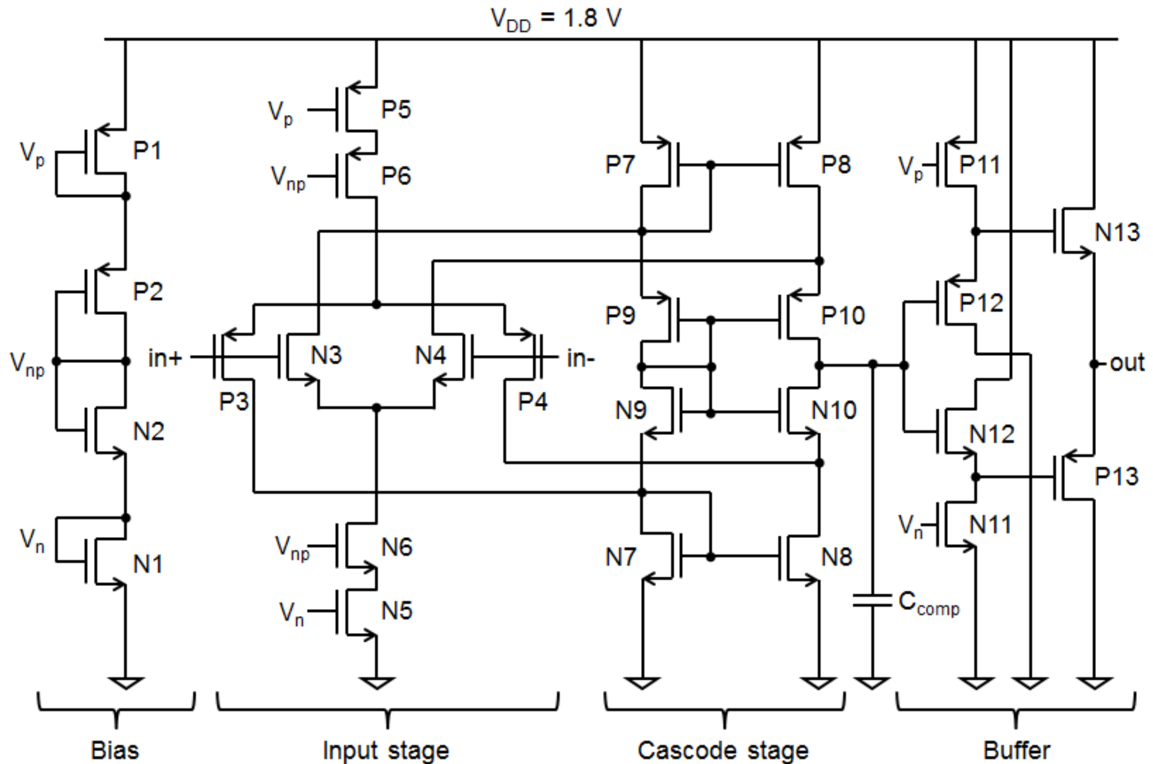


Fig. 19: Complementary folded-cascode op amp.

cells were used for all layouts of matched devices, and measurements of each device showed good matching with PDK models—including the temperature response.

Because the op amp is a crucial block in both of the voltage reference designs the amplifier is briefly discussed first. Being pinned out individually it was desirable to make the op amp function as a general-purpose amplifier with a wide common-mode input range. A complementary folded-cascode topology was selected for its rail-to-rail input range and its successful implementation in the past [111], [112]. The op amp schematic is shown in Fig. 19 with the primary stages labeled. On the test chip, versions of this design with 0.5-µm channel length and 2-µm channel length input transistors were included. The n- and p-type input transistors allow the input stage to function when the common-mode input voltage is 0 V to V_{DD}. The self-biased cascode stage provides a high-resistance load for the input stage, resulting in high voltage gain. The push-pull source-follower output

buffer isolates the high-impedance cascode stage output from the pad connected to the "out" node. Several papers have been published on the single-event performance of this 180-nm op amp design [91], [95], [113].

The DC and AC characteristics of the op amp were tested to verify functionality. Measurements indicated the open-loop gain of the op amp was greater than 73 dB, and the power-supply rejection ratios were 123 dB for both V_{DD} and V_{SS}. The input-referred offset voltage was measured between ±10 mV, and the gain-bandwidth product was approximately 5 MHz. The phase margin of the op amp was below 0° because the amplifier was not unity-gain stable. While this was a problem in performing some tests on the op amp, stability was observed when configured in the two presented voltage references.

Temperature measurements of the DTMOST reference of Fig. 18(a) are plotted in Fig. 20. Two measurements were performed on the same circuit, and the response shows some hysteresis. However, the reference voltage does exhibit the expected second-order curvature with first-order tempco cancellation. The voltage variation in the measurements is approximately 15 mV (3.4%) in the first measurement and 6 mV (1.4%) in the second, which are significantly higher than the 3 mV predicted by simulation. The main reason

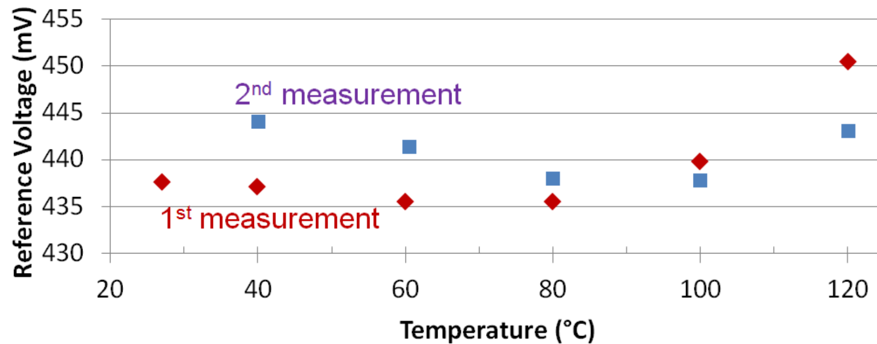


Fig. 20: Effect of temperature on voltage of DTMOST reference with *R2* = 154 kΩ and *R1* = 31 kΩ. Two temperature measurements on the same reference were performed.

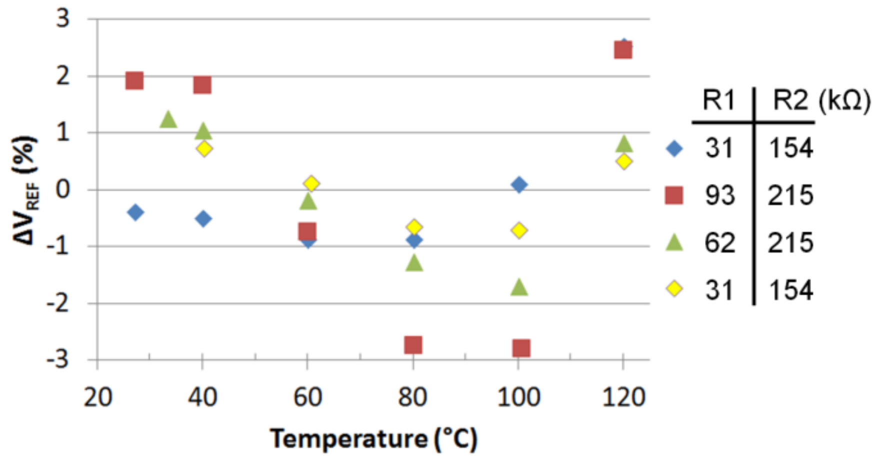


Fig. 21: Temperature variation of DTMOST reference in three R1/R2 configurations.

for this is the temperature drift of the op amp offset voltage. Since the resistor ratio R2/R1 controls the tempco cancellation of the variation, measurements were taken with these resistor values varied in Fig. 21. The voltages are plotted as percent variation from the average across the temperature range. All voltages show a sharp increase from 100°C to 120°C, reinforcing the notion that temperature drift in the offset voltage of the op amp—identical in all these circuits—is degrading the precision of the reference voltage. The measurement results show that first-order tempco cancellation is achievable using DTMOSTs and the effects of offset voltage must be mitigated.

The temperature response was also measured for the nFET reference of Fig. 18(b). Three different combinations of R2/R1 were tested, and the combination with the least temperature drift is plotted in Fig. 22. The voltage variation is approximately 10 mV (2%), which is again notably higher than the 1.3 mV predicted by simulation. This again is likely due to op amp offset drift. The temperature responses of three different R2/R1 configurations are shown in Fig. 23. It is interesting to note that the configurations with the highest gain (set by the R2/R1 ratio) have the largest increases in voltage from 80°C

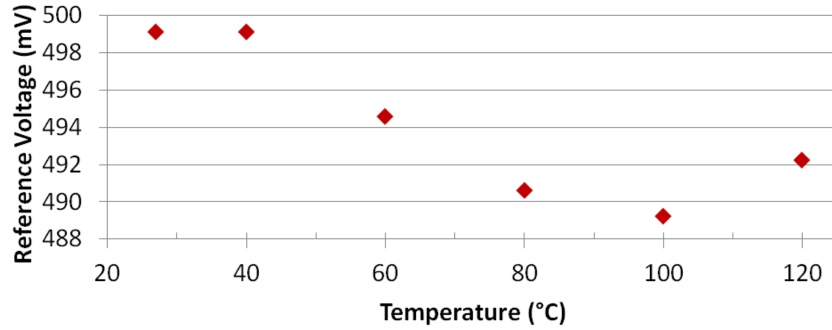


Fig. 22: Effect of temperature on voltage of nFET reference with *R2* = 154 kΩ and *R1* = 123 kΩ. Two temperature measurements on the same reference were performed.

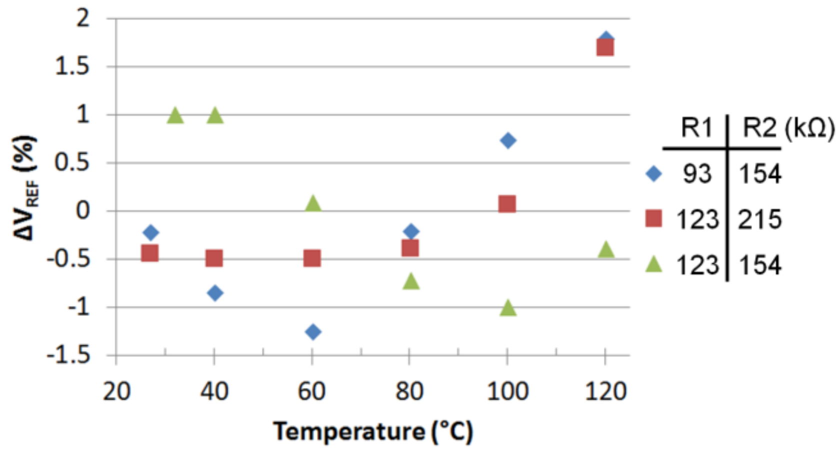


Fig. 23: Temperature variation of nFET reference in three R2/R1 configurations.

to 120°C. Since the offset voltage of the op amp is amplified by the R2/R1 ratio, this again indicates the effect of the offset voltage on precision.

The voltage reference designs on the 180-nm test chip exhibited the expected tempco cancellation, validating the CMOS-only approaches to voltage reference design. In addition the individual component measurements helped cultivate confidence in the PDK models in accurately modeling the DTMOST temperature response. However, the most elucidating measurements taken from the test chip were the radiation measurements that will be discussed in Chapter V.

Table 1: Number and description of voltage references on 40-nm test chip.

1	Voltage-summed DTMOST reference
2	Voltage-summed DTMOST reference with SE hardening
3	Voltage-summed pFET reference
4	Voltage-summed pFET reference with SE hardening
5	Current-summed DTMOST reference with 2X size scale
6	Current-summed DTMOST reference with 4X size scale
7	Current-summed nFET reference
8	Current-summed nFET reference with SE hardening

Temperature-regulated reference on 40-nm chip

Eight temperature-regulated voltage reference designs were fabricated in the UMC 40-nm process. The focus of the designs was single-event mitigation, but presented here is a proof-of-concept of the thermal regulation scheme. The eight reference designs are summarized in Table 1. A variety of reference devices including DTMOSTs and diode-connected nFETs and pFETs were used to implement the references. The voltage-summing and current-summing reference topologies are presented in Fig. 24 and Fig. 25. The voltage-summing topology is particularly well-suited to single-event hardening—as

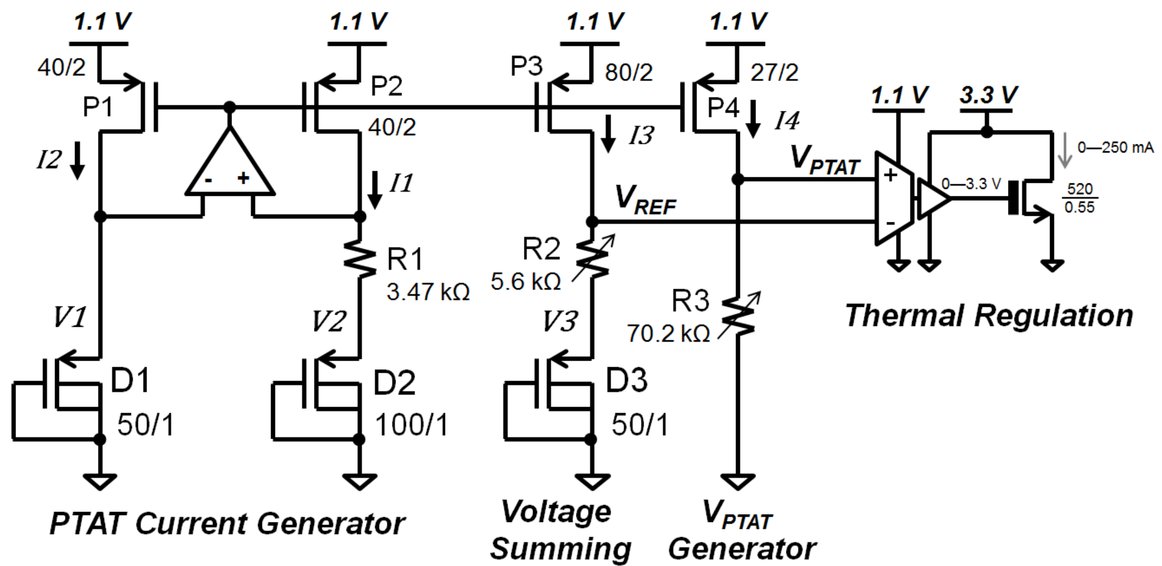


Fig. 24: Voltage-summed DTMOST reference on 40-nm test chip (#1 in Table 1).

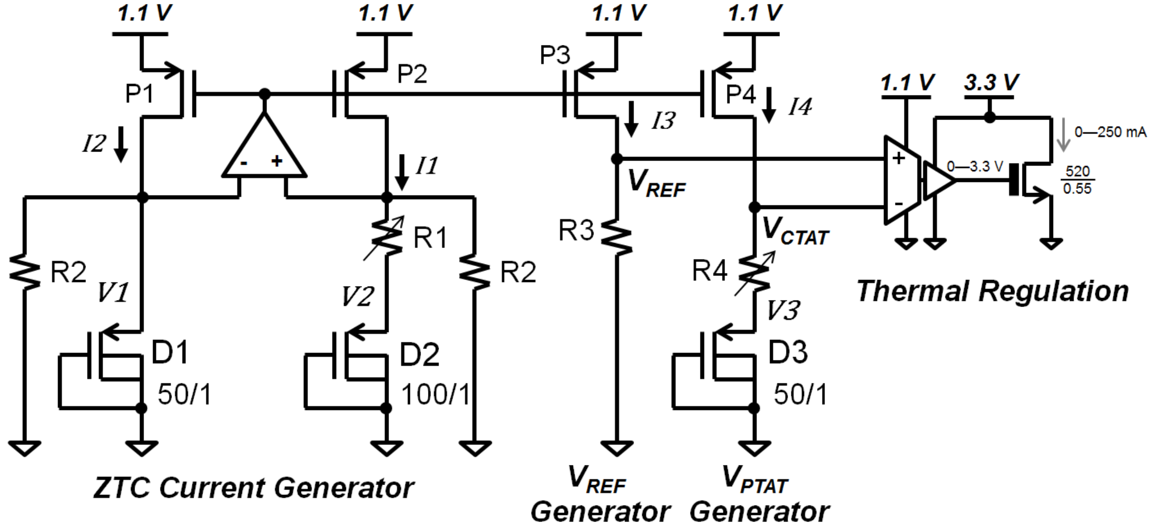


Fig. 25: Current-summed DTMOST reference on 40-nm test chip (#5 in Table 1).

will be discussed in Chapter V. It consists of four circuit blocks with the PTAT current generator being the most important. The current I1 or I2 mirrored by this circuit is:

$$I1 = I2 = I_{PTAT} = \frac{V1-V2}{R1}. \tag{23}$$

Because V1 and V2 are the voltages of DTMOSTs at different current densities, the resulting current is proportional to absolute temperature (PTAT). When this current is mirrored to P3, the voltage reference is:

$$V_{REF} = V3 + I_{PTAT}\,R2 = V3 + 2\frac{R2}{R1}(V1 - V2). \tag{24}$$

Thus, by adjusting the resistance R2, the negative tempco of V3 can be cancelled with the positive tempco of (V1 – V2). Similarly mirroring the PTAT current across the programmable resistor R3, a PTAT voltage V_{PTAT} is generated. The PTAT and zero-tempco voltages control the op amp that drives the 3.3-V heater nFET. The first stage of the op amp is powered by 1.1 V, and the output stage is powered by 3.3 V so the heater can be driven. By dissipating power, the large W/L nFET increases the temperature of the die.

The current-summed reference (based on [114]) of Fig. 25 performs the tempco cancellation in the zero-tempco (ZTC) current generator block. The current I1 or I2 mirrored from this circuit is the sum of the currents through R1 and R2 at the non-inverting op amp input:

$$I1 = I2 = I_{ZTC} = \frac{V1}{R2} + \frac{V1-V2}{R1}. \tag{25}$$

By adjusting the value of R1, the negative tempco of V1 and the positive tempco of (V1 – V2) are cancelled. Mirroring this current across the resistor R3 generates the reference voltage:

$$V_{REF} = I_{ZTC}\,R3 = \frac{R3}{R2}V1 + \frac{R3}{R1}(V1 - V2). \tag{26}$$

The primary benefit of this topology is that it is well-suited to low-voltage design; even if conventional p-n junctions were used then the output voltage can still be designed to be much lower than the typical bandgap voltage 1.2 V [114]. A temperature-dependent voltage is necessary for temperature sensing in the thermal regulation scheme, so a complementary-to-absolute-temperature (CTAT) voltage is generated with a DTMOST voltage:

$$V_{CTAT} = V3 + I_{ZTC}\,R4. \tag{27}$$

By adjusting R4 the voltage level of V_{CTAT} can be adjusted, while the negative tempco of V3 dominates the temperature response. Since V_{CTAT} decreases with temperature, the op amp connections for thermal regulation are swapped, compared to the voltage-summed reference.

The focus of this section is the voltage-summed DTMOST reference of Fig. 24, so temperature simulation and measurement results will be presented for it and not the current-summed reference. The programmable resistors R2 and R3 in the voltage-

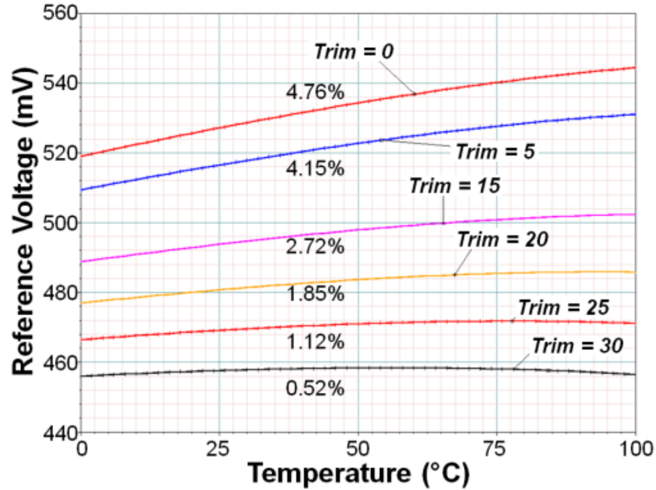


Fig. 26: Trimming of V_{REF} via R2 in voltage-summed reference of Fig. 24. Digital trim code and voltage variation are indicated for each curve.

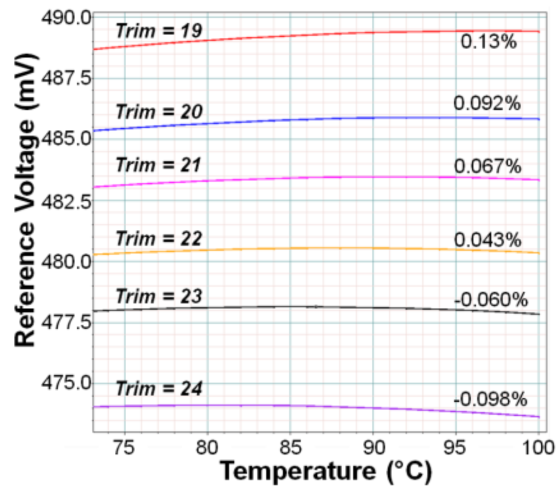


Fig. 27: Temperature response of reference voltage across the 75—100°C range at different R2 trim codes. Digital trim code and voltage variation are indicated for each curve.

summed reference are constructed with a series combination of binary-weighted resistors with nFET switches connected in parallel. A 5-bit digital word is used to control the resistance. Trimming R2 adjusts V_{REF}, and the functionality of this trim is demonstrated with simulation results in Fig. 26. The voltage and temperature drift of the reference output are adjusted by the trim code. Across the range of 0—100°C, the minimum variation achievable is 0.52%. If the chip temperature is regulated at 75°C the heating maintains a flat voltage from 0—75°C, and the overall variation is simply the variation

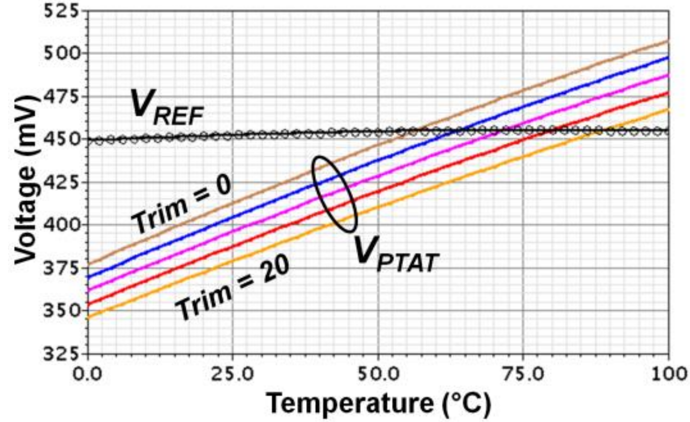


Fig. 28: Temperature response of PTAT voltage with R3 trim codes of 0, 5, 10, 15, and 20.

from 75 to 100°C shown in Fig. 27. As shown, the temperature drift in this range can be as low as 0.043%, which is less than ½ LSB for 10 bits of precision.

The trimming of V_{PTAT} via R3 (Fig. 24) is important for proper thermal regulation, since the thermal feedback will regulate to the temperature at which $V_{PTAT} = V_{REF}$. The functionality of trimming R3 is demonstrated with simulation results in Fig. 28, showing the temperature response of V_{REF} and V_{PTAT} at various R3 trim codes. The trimming of the PTAT voltage allows the intersection with the reference voltage to be controlled, which in turn controls the regulated die temperature.

Some basic temperature testing was done on the 40-nm chip to verify functionality of the thermal feedback design. Due to a bonding issue, it was not possible to apply trim codes to the PTAT voltage (R3). Therefore the maximum trim code of 31 was used to trim the reference voltage to the minimum voltage in order to ensure the intersection of V_{REF} and V_{PTAT} at a temperature below 100°C. The measured temperature responses of these two voltages without thermal feedback are plotted in Fig. 29(a). The PTAT voltage shows a linear response with tempco of approximately 0.95 mV/°C, which is reasonably within the expected process variation from the expected 1.2 mV/°C. The

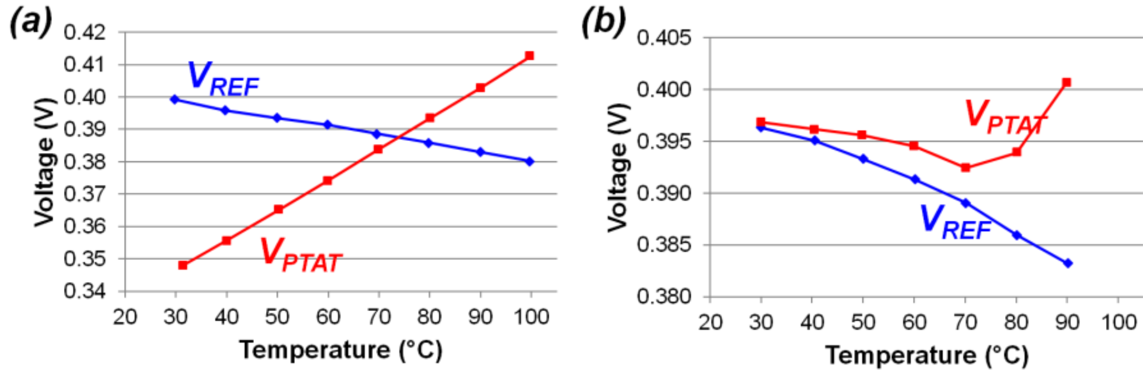


Fig. 29: Measured temperature response of reference (a) without and (b) with thermal regulation. For both measurements the trim code for V_{REF} is the maximum 31.

reference voltage shows much weaker temperature dependence, but does not exhibit the tempco cancellation. This is expected because the reference is trimmed to have the lowest voltage and the most negative tempco possible. If the reference trim code were decreased, the voltage would increase and the temperature response would flatten out. However, if this were done the two plotted voltages would not intersect in this temperature range, while this sub-optimal trim code results in intersection at 75°C.

The response of the reference with thermal feedback loop closed is plotted in Fig. 29(b). The PTAT voltage shows a dramatic change compared to the open-loop response. Up to approximately 70°C, the PTAT voltage tracks the reference voltage within at most 4 mV. At 80 and 90°C the two voltages clearly diverge, indicating the ambient temperature has exceeded the regulated temperature. The slightly increasing difference between V_{REF} and V_{PTAT} below 70°C is due to drift in the systematic offset of the heater op amp. The variation in reference voltage is only slightly improved by thermal regulation—from 19.6 mV down to 13.1 mV. Part of the reason for the minor improvement is the incorrect trim of the reference's tempco cancellation. The other factor is most likely thermal gradients introduced by the heater itself. While symmetric layouts between matched pairs were used on chip, it is difficult to ensure uniform temperature

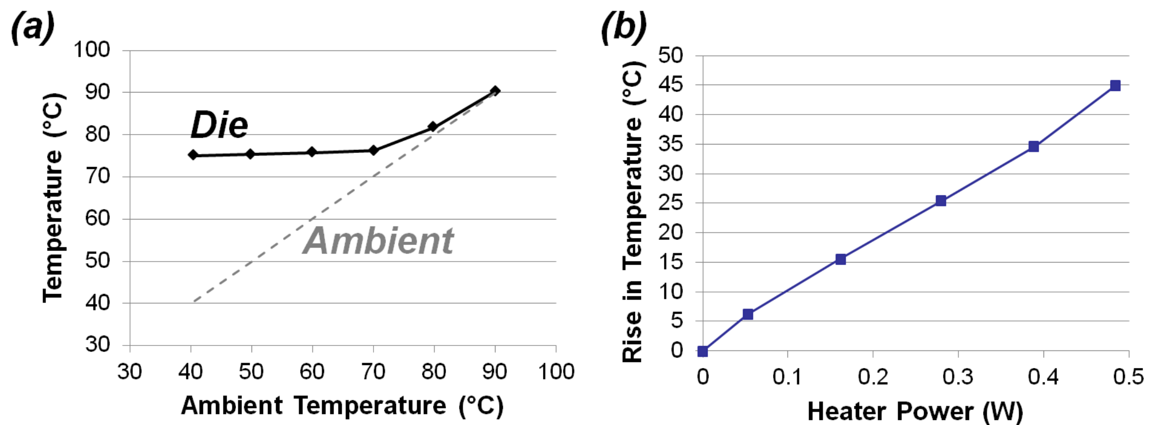


Fig. 30: (a) Die temperature measured using on-chip diode when thermal regulation is active. (b) Rise in temperature as a function of power dissipated by heater.

over the relatively large area of an analog design. While it is possible to overcome this issue by trimming the reference to compensate for these gradients, the bonding issues with the chip did not allow such experimentation. On the other hand, the PTAT voltage variation was reduced from 64.7 mV to 8.3 mV—an 87% reduction. This result is representative of the intended impact of thermal regulation.

A diode on the chip was used to measure the die temperature. A 10-kΩ off-chip resistor connected to 1.1 V was used to bias the device, and a calibration curve of voltage versus temperature was acquired. Using this calibration curve with voltage measurements from the diode, the die temperature during the thermal feedback test can be plotted in Fig. 30(a). As expected, the die temperature is fairly constant within 1.2°C of 75.1°C when the ambient temperature is below 80°C, but at 80°C and higher the die temperature closely tracks ambient. The small temperature variations of die temperature in the flat region are due to offset drift in the heater op amp. For instance, if the offset changes 0.95 mV, then the regulation temperature determined by matching V_{PTAT} to V_{REF} changes by 1°C, since the tempco of V_{PTAT} is 0.95 mV/°C. Finally, the on-chip heater is characterized in Fig. 30(b). The measured rise in temperature is simply the difference

between die temperature and ambient temperature, and it shows a linear response to heater power. The slope of the line indicates the thermal resistance of the chip to be on the order of 90°C/W. This value is most likely conservative because the lid of the package had to remain off during these tests to avoid contact with protruding bond wires. A package with higher thermal resistance would reduce the power required for heating and reduce the thermal gradients on the chip, which caused the significant variations in reference voltage.

RHBD temperature-regulated reference on 180-nm chip

The final reference design to discuss is the RHBD reference taped out on another 180-nm test chip (using the CMRF7SF process), shown schematically in Fig. 31. The temperature response of the reference will be covered, and the radiation response of the reference will be discussed in Chapter V. While the overall architecture is similar to the DTMOST reference of Fig. 18(a), there are some significant differences. The reference of

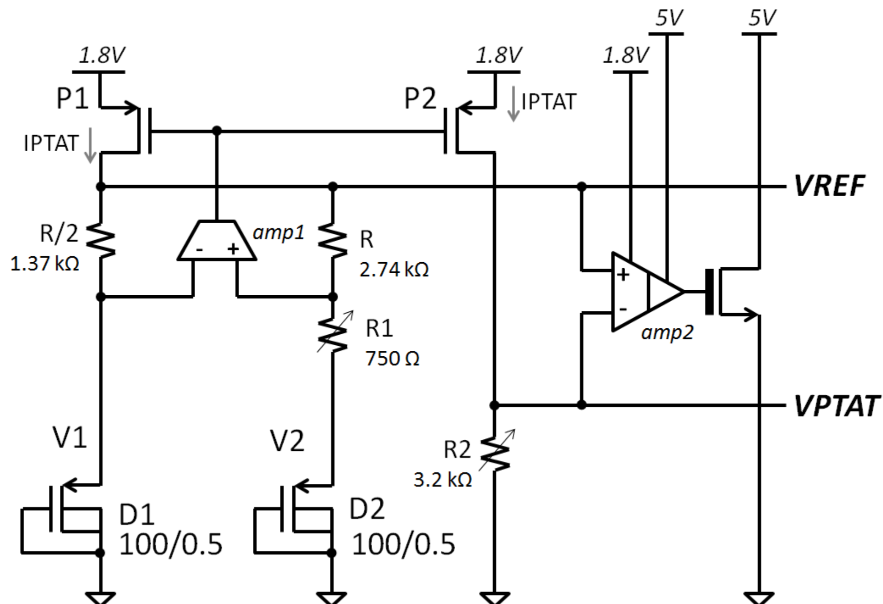


Fig. 31: RHBD temperature-regulated voltage reference designed in IBM 180-nm process.

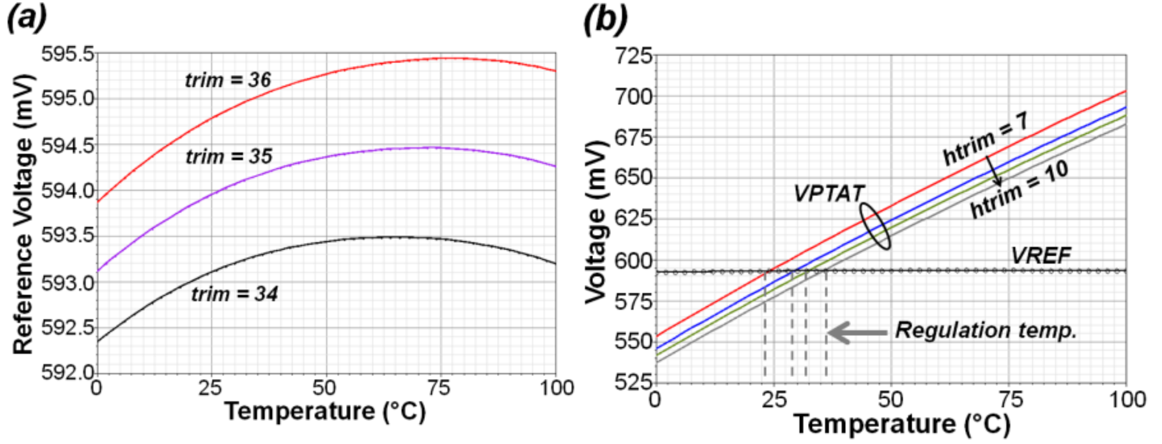


Fig. 32: Simulation results demonstrating trim functionality of (a) reference voltage and (b) PTAT voltage.

Fig. 31 uses two identical DTMOSTs with scaled bias currents to generate the negative-tempco voltages V1 and V2. Furthermore, the bias currents of D1 and D2 are scaled using resistors R and R/2 connected to the VREF output. The total bias current for the reference core is the sum of these currents:

$$IPTAT = 3\frac{(V1-V2)}{R1}. \tag{28}$$

The reference output voltage is:

$$VREF = V1 + \frac{IPTAT}{3}R = V1 + \frac{R}{R1}(V1 - V2), \tag{29}$$

with first-order tempco cancellation between the V1 and (V1 – V2) terms. By adjusting the trimmed resistor R1, the PTAT current and the R/R1 ratio are adjusted, which changes the voltage and tempco of VREF. The trimming of VREF is demonstrated in Fig. 32(a), showing the VREF temperature response when three trim codes are used for R1. As the trim code increases, the voltage increases as well as the temperature at which the tempco is zero (the ZTC point).

The reference employs the same temperature regulation scheme as the 40-nm test chip. A trimmable PTAT voltage VPTAT is compared against the reference voltage by an op amp that drives a thick-oxide (5 V) heater nFET. By mirroring the PTAT current

across a trimmed resistor the level of VPTAT can be adjusted, as shown in Fig. 32(b). The plot shows temperature sweeps of the reference voltage and the PTAT voltage at four different trim codes ("htrim"). The point at which the two voltages intersect is the regulation temperature of the heater, so adjusting VPTAT basically adjusts the die temperature during thermal regulation. The temperature-regulated operation of this circuit was simulated and presented in Fig. 17 in the previous section. The results demonstrated how the reference voltage drift can be limited to 0.05% with minimal heating at 35°C.

As will be discussed in Chapter V, this reference also incorporates a dynamic offset cancellation scheme using chopper stabilization. By cancelling the offset voltage of the op amp in the reference core, the op amp offset will be very small and relatively insensitive to temperature. Since the op amp offset severely degraded the temperature responses of the previous two reference designs, the physical temperature response of this design is expected to match much more closely to simulations.

E. Summary

In this chapter the basic theory of designing voltage references was discussed. The low supply voltages of modern CMOS processes makes it increasingly difficult to employ traditional bandgap references, so the chapter focused on the DTMOST-based reference as a low-voltage alternative. As an added benefit, DTMOST references are implemented with standard CMOS devices, so the designs are portable to any CMOS process. Like BJTs in a bandgap reference, DTMOSTs can be used to generate a reference voltage with zero first-order temperature dependence.

The concept of reducing the temperature drift and increasing the precision of voltage references using thermal regulation was also discussed in detail. The thermal control loop was analyzed, and generalized equations as well as Spice-level electro-thermal modeling techniques were presented. Design techniques for minimizing the effect of thermal regulation on chip lifetime were also presented.

Finally, voltage reference designs implemented in commercial 180-nm and 40-nm processes were presented. Experimental results from a 180-nm test chip demonstrated the expected first-order tempco cancellation in DTMOST- and nFET-based references. Thermal testing of a temperature-regulated reference fabricated on a 40-nm test chip demonstrated the functionality of the proposed thermal control scheme. Non-idealities in the circuit such as thermal gradients and offset voltages limited the precision enhancement of the temperature regulation. Bonding issues and time constraints prevented further testing of the chip, but the experiment does provide proof of the thermal regulation concept. Temperature simulations were also presented for the RHBD voltage reference detailed in Chapter V.

CHAPTER IV

SWITCHED-CAPACITOR CIRCUITS

Discrete-time circuits such as switched-capacitor (SC) circuits are commonly used in analog integrated circuits because they are generally more efficient and precisely controlled than resistors. Switched capacitors are able to achieve relatively large effective resistances in a significantly smaller area than a polysilicon or metal resistor. The dynamic power consumption of switched capacitors is often less than the DC power consumed by resistors. In addition, capacitors are less prone to process variation, and thus mismatch, in typical CMOS processes. Finally, switched capacitors are especially suited for mixed-signal applications like ADCs because of the sampling nature of their circuit operation. In this chapter, the basic concept of the switched capacitor is discussed and several 45-nm designs of a sample/hold amplifier are discussed.

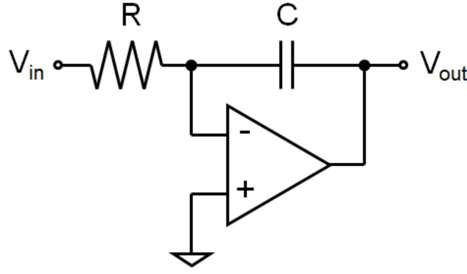
A. Basic switched-capacitor concept: the integrator

In this section the basic integrator circuit is used to demonstrate the fundamental operation of a switched capacitor. Figure 33 shows both a standard continuous-time integrator and an SC integrator. The time-domain output of the continuous-time integrator can be expressed as:

$$V_{out}(t) = -\frac{1}{RC}\int_{-\infty}^{t} V_{in}(\tau)d\tau. \qquad (30)$$

The frequency-domain output of the integrator can be expressed as:

$$V_{out}(s) = -\frac{1}{sRC}\,. \qquad (31)$$



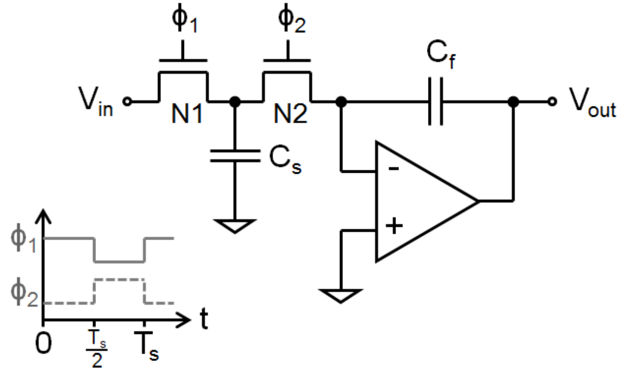


Fig. 33: (a) A basic continuous-time integrator implemented with a resistor and capacitor. (b) A switched-capacitor integrator implemented with two capacitors and two switches operated on non-overlapping control signals ϕ_1 and ϕ_2 with frequency $f_s = 1/T_s$.

The SC integrator has the same topology as the continuous-time integrated, except *R* has been replaced with a capacitor C_s and two switches *N1* and *N2*. The two switches operate on opposite-phase control signals ϕ_1 and ϕ_2 with frequency $f_s = 1/T_s$, as shown in Fig. 33(b).

The switches regulate the current flow to and from the capacitor, creating an effective resistance between V_{in} and the inverting input of the op amp. During phase 1, *N1* is on, and *N2* is off, so the charges stored on C_s and C_f at the beginning of phase 1 (time t_0) are:

$$Q_{Cs}(t_0) = C_s V_{in}(t_0) \tag{32}$$

and

$$Q_{Cf}(t_0) = -C_f V_{out}(t_0). \tag{33}$$

The sample capacitor C_s simply samples the input voltage, and the feedback capacitor C_f holds the output voltage value from the previous phase. During phase 2, *N1* is turned off, and *N2* is turned on, so the charges stored on C_s and C_f at the beginning of phase 2 (time $t_0+T_s/2$) are:

$$Q_{Cs}(t_0 + \frac{T_s}{2}) = 0 \tag{34}$$

and

$$Q_{Cf}\left(t_0 + \frac{T_s}{2}\right) = -C_f\, V_{out}(t_0) + C_s V_{in}(t_0). \tag{35}$$

The sample capacitor is discharged because *N2* connects it to virtual ground. Therefore, the charge from C_s is transferred to the feedback capacitor C_f. Now at the end of phase 2 (time t_0+T_s), the charge on C_f is the same as at the beginning of phase 2, and an expression for the discrete derivative of V_{out} can be derived starting with the charge conservation equation for the feedback capacitor:

$$Q_{Cf}(t_0 + T_s) = Q_{Cf}\left(t_0 + \frac{T_s}{2}\right). \tag{36}$$

Substituting (36) yields:

$$-C_f\, V_{out}(t_0 + T_s) = -C_f\, V_{out}(t_0) + C_s V_{in}(t_0). \tag{37}$$

Finally, manipulating (37) into a discrete derivative expression yields:

$$\frac{V_{out}(t_0+T_s) - V_{out}(t_0)}{T_s} = -\frac{C_s}{C_f}\frac{1}{T_s} V_{in}(t_0). \tag{38}$$

As T_s becomes small, the above expression becomes the derivative of V_{out}, and the equation can be integrated to obtain an expression for the output of the switched-capacitor integrator:

$$V_{out}(t) = -\frac{C_s}{C_f}\frac{1}{T_s}\int_{-\infty}^{t} V_{in}(\tau)\, d\tau. \tag{39}$$

The expression is identical to that of the continuous-time integrator; therefore the equivalent resistance of the switched capacitor can be computed as:

$$R_{eq} = \frac{T_s}{C_s} = \frac{1}{f_s\, C_s}. \tag{40}$$

The expression for equivalent resistance of the switched capacitor summarizes one of the primary benefits of SC circuits. An arbitrary resistance can be realized by providing the appropriate sampling frequency f_s and capacitance C_s. For example, in the 180-nm CMOS process discussed in the previous chapters, the p+ poly resistors have a nominal sheet resistance of 260 Ω/□, so it would require 10,000 squares to implement a 2.6-MΩ resistor. At a width of 1 μm, this amounts to 10,000 μm^2 of area. With a switched-capacitor sampled at 1 MHz, the required capacitor size is 385 fF, which can be implemented with a 705-μm^2 four-layer metal capacitor or a 188-μm^2 metal-insulator-metal (MIM) capacitor (a 98% smaller area than the resistor). The area overhead of the switches is negligible compared to the capacitor size. Furthermore, the ±10% process variation of the MIM capacitor is less than the ±15% variation of the p+ poly resistor. This analysis demonstrates the efficacy of the use of switched-capacitor circuits in AMS designs.

B. Differential sample-and-hold amplifier

Differential topologies are commonly used in analog/mixed-signal circuits because the inherent common-mode rejection significantly reduces noise, increasing accuracy and precision. This section discusses the fully-differential sample/hold amplifier (S/H amp), which is the case study of this work for single-event effects in SC circuits.

The S/H amp, shown in Fig. 34, consists of identical SC networks of opposite signal polarities centered around the operational transconductance amplifier (OTA). As was the case in the SC integrator, two non-overlapping clock signals are required to

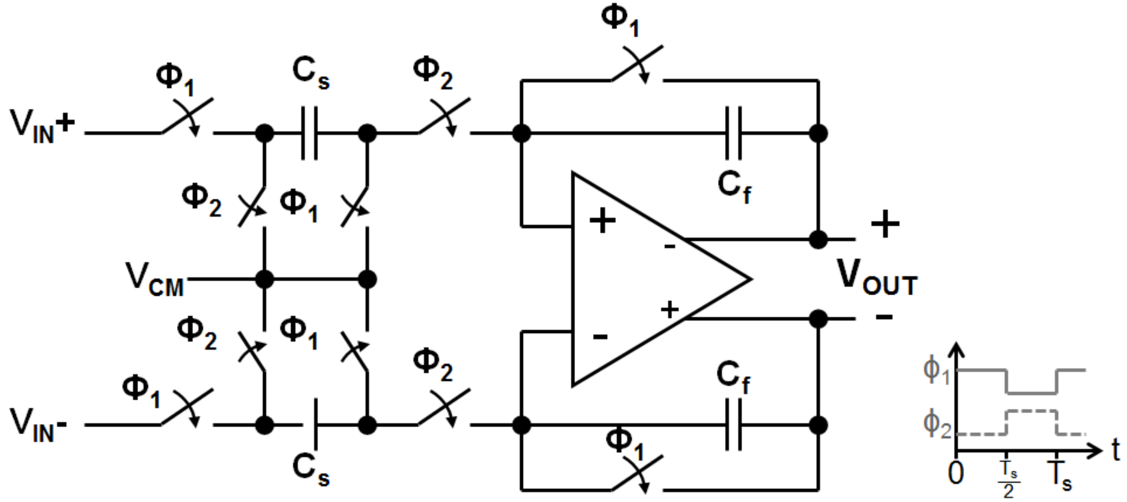


Fig. 34: Differential sample-and-hold amplifier with switches operated on non-overlapping control signals ϕ_1 and ϕ_2 with frequency $f_s = 1/T_s$.

operate the switches. When ϕ_1 is HIGH and ϕ_2 is LOW, all the switches controlled by ϕ_1 are closed, and all the switches controlled by ϕ_2 are open, putting the circuit in sample mode, as shown in Fig. 35(a). In the sample phase, the differential input is sampled across the sample capacitor C_s in the positive and negative paths of the circuit, and both sample capacitors are referenced to the common-mode voltage V_{CM}, which serves as a virtual ground. Meanwhile, the feedback capacitors are shorted out, allowing the OTA to reset its differential output. Without this step, the circuit would behave like a differential integrator. Now the differential charge stored on the sample capacitors is given by:

$$Q = V_{in}C_s. \tag{41}$$

When ϕ_1 is LOW (turning off all its switches) and ϕ_2 is HIGH (turning on all its switches), the circuit goes into evaluation mode, as shown in Fig. 35(b). In evaluation mode both sides of each sample capacitor are shorted to V_{CM}, since the op amp inputs form a virtual short. Thus, the charge stored in the sample capacitors is discharged onto the feedback capacitors. Since the input switches are open, no additional charge has entered the system. The conservation of charge dictates that:

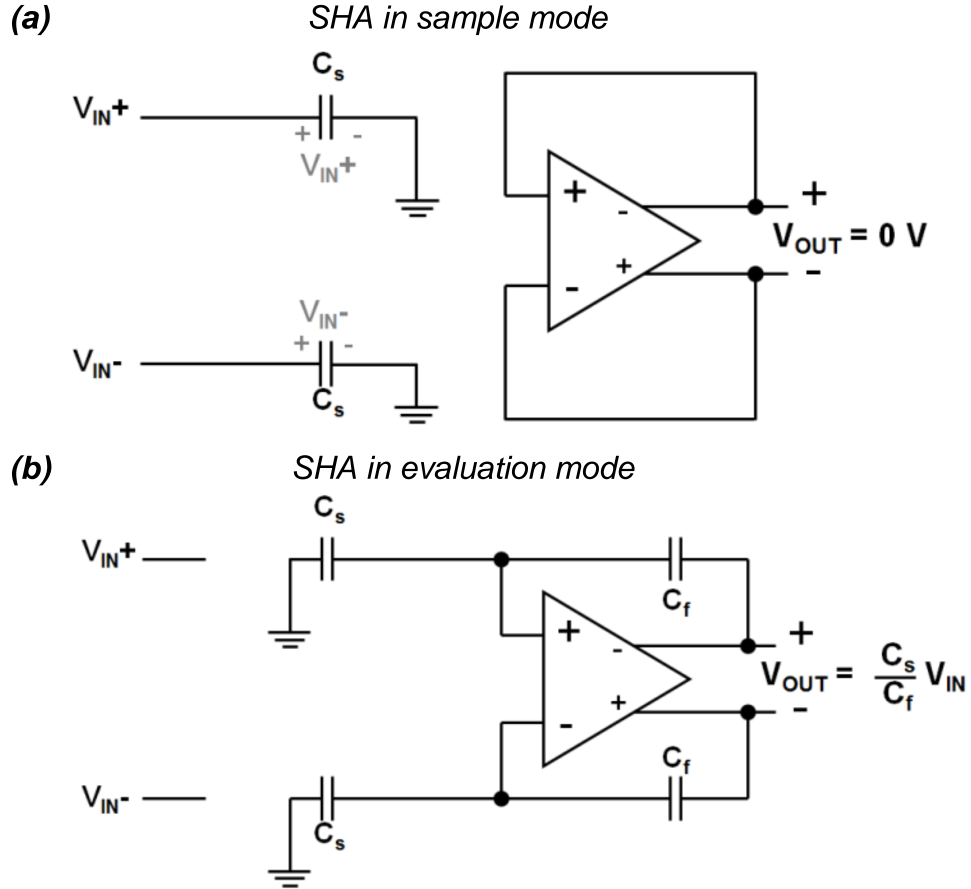


Fig. 35: Differential sample-and-hold amplifier in (a) sample mode and (b) evaluation mode.

$$Q_{total,sample} = Q_{total,evaluation}. \tag{42}$$

Substituting (41) for the sample-mode charge and $V_{out}C_f$ for the evaluation-mode charge yields:

$$V_{in}C_s = V_{out}C_f. \tag{43}$$

Finally, manipulating (43) into an input/output transfer function yields:

$$V_{out} = \frac{C_s}{C_f}V_{in}. \tag{44}$$

Thus, the input voltage is sampled and then amplified by the ratio of C_s to C_f.

C. Overview of 45-nm sample-and-hold amplifier designs

In order to validate the RHBD technique to be discussed in Chapter VI, five differential S/H amps were designed and laid out on a 45-nm Silicon-On-Insulator (SOI) test chip. The five S/H amp designs were variants of two primary topologies, an nFET-only design and a transmission-gate based design. The nFET S/H amp implements each switch with a single nFET and uses an OTA with an nFET input stage. The transmission-gate (TG) S/H amp implements each switch with a transmission gate and uses an OTA with a complementary input stage. Figure 36 shows the switches used for each of these topologies. Thick-oxide body-contacted transistors were used for each S/H amp design. These transistors have a maximum drain-source voltage of 1.8 V. Replacing each ideal switch in Fig. 34 with the switch shown in Fig. 36(a) yields the nFET S/H amp design, and replacing each ideal switch with the switch of Fig. 36(b) yields the TG S/H amp design. The switch networks of both S/H amps require control circuitry to generate the non-overlapping clock signals, shown in Fig. 37. On the test chip, multiplexing circuitry was added to the clock generation circuit of Fig. 37(a) to overwrite the generated clocks with external clock signals, if necessary.

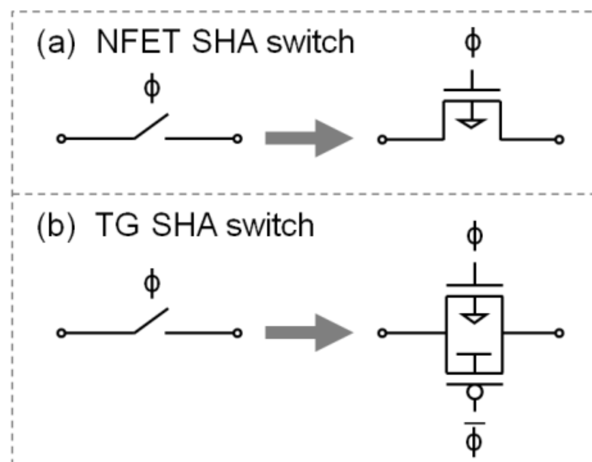
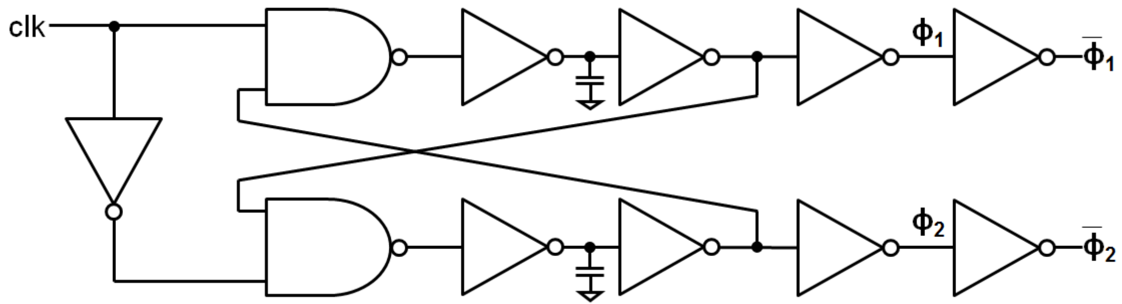


Fig. 36: Switch implementations in (a) nFET SHA and (b) transmission-gate SHA.

(a) Non-overlapping clock generation



(b) Non-overlapping clock signals

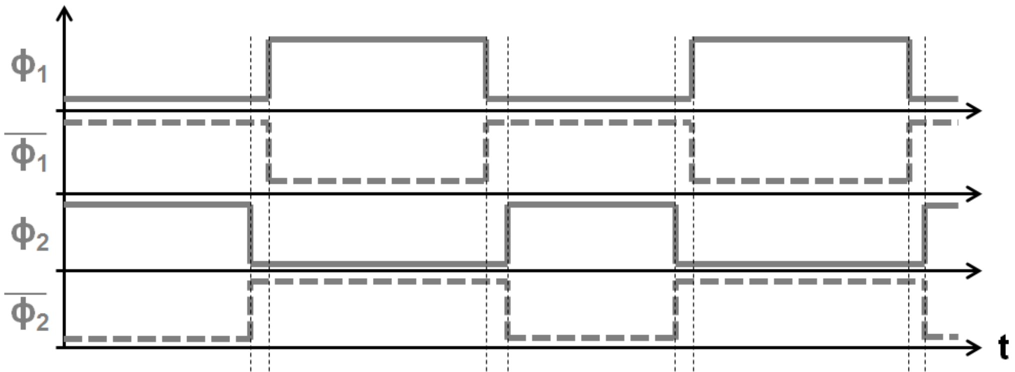


Fig. 37: (a) Non-overlapping clock generation circuit. Test chip design also includes multiplexing to overwrite the circuit-generated signals with external clocks. (b) Non-overlapping clock signals. The vertical dashed lines indicate the non-overlapping time windows of the clocks.

The central subcircuit of the nFET SHA is the OTA, shown schematically in Fig. 38. The topology of the op amp is a fully-differential folded cascode. The bias voltages are generated with a boot-strapped current source and several current mirrors, as shown in Fig. 39. The transistor sizes of the OTA and bias circuit are listed in Table 2 and Table 3, respectively. The input stage consists of an nFET differential pair source-connected to a tail current source. The output stage is a differential cascode stack with a current-source pair controlled by the common-mode feedback circuitry. The common-mode voltage *vcm* is generated at $V_{DD}/2$ with a simple voltage divider. Compensation capacitors would typically be connected from *out+* and *out-* to ground, but in the S/H topology, the feedback capacitors C_f provide compensation in the OTA. In fact, the amount of

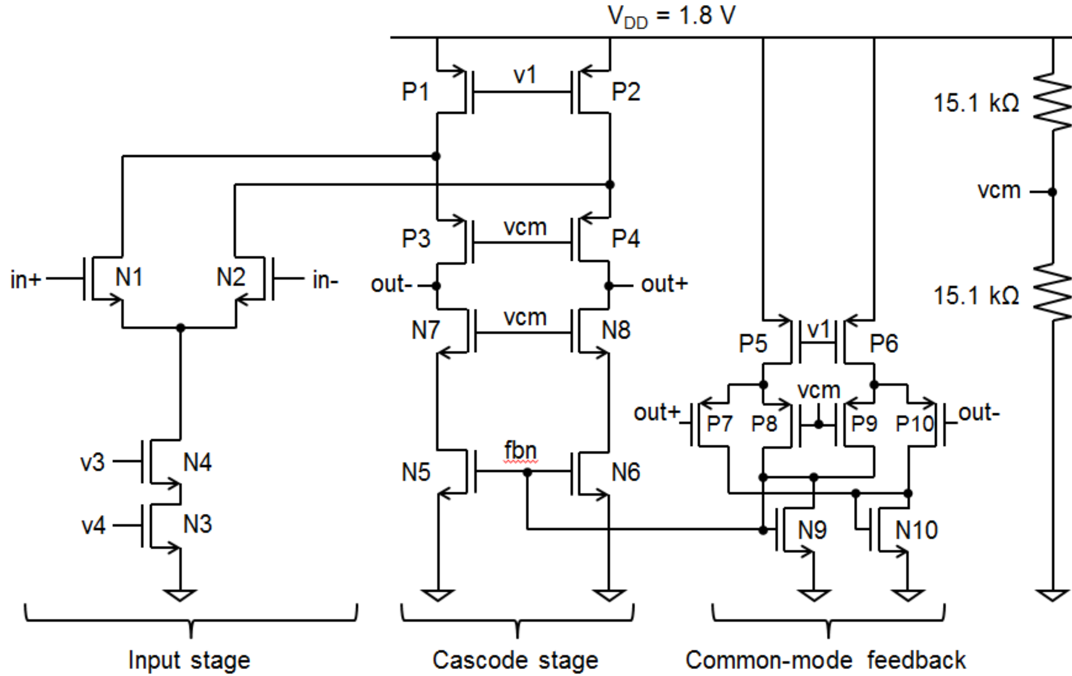


Fig. 38: Schematic of nFET-input OTA used in nFET SHA. Each transistor is body-source tied. Bias voltages *v1*, *v3*, and *v4* are generated in the bias circuit of Fig. 39. The sizes of the transistors in the OTA are listed in Table 2.

Table 2: Transistor sizes of nFET-input OTA in Fig. 38.

NFETs	W/L (μm/μm)		PFETs	W/L (μm/μm)
N1—N2	48/0.472		*P1—P2*	15/2
N3—N4	2/0.472		*P3—P4*	12/0.472
N5—N8	0.8/0.472		*P5—P6*	6/0.472
N9—N10	2/0.232		*P7—P10*	3/0.472

compensation required drives the design value of C_f. Table 4 shows the OTA parameters, simulated using typical process parameters and parasitic extraction.

Figure 40 shows the schematic of the fully-differential complementary folded-cascode OTA used in the TG SHA; transistor sizes are listed in Table 5. The bias circuit is identical to that of the nFET OTA. The input stage is comprised of both an nFET pair and a pFET pair along with the corresponding tail current sources. These input pairs feed

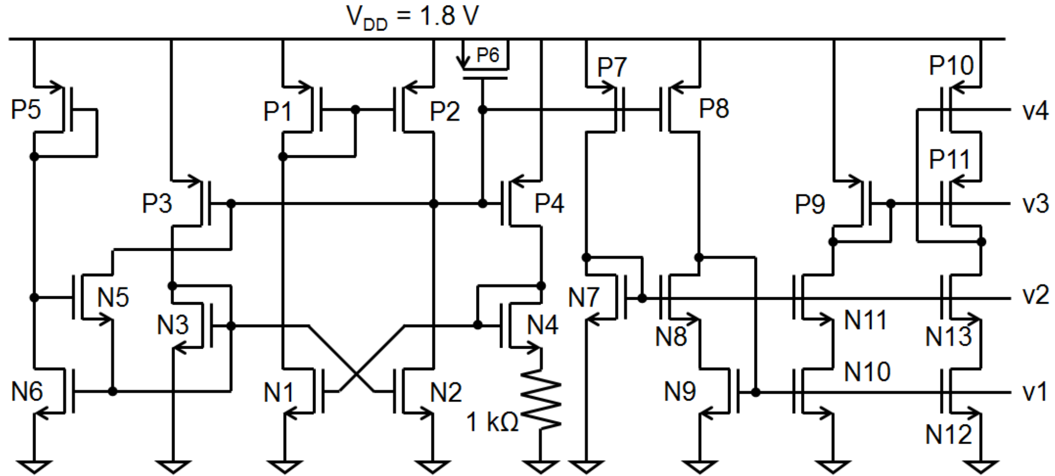


Fig. 39: Bias circuit used in both nFET-input and complementary-input OTA. The labeled nodes are referenced in the OTA schematics of Fig. 38 and 40. The size of each transistor is listed in Table 3.

Table 3: Transistor sizes in bias circuit in Fig. 39.

NFET(s)	W/L (μm/μm)		PFET(s)	W/L (μm/μm)
N1—N2	4/0.472		*P1—P2*	12/0.472
N3—N6	1/0.472		*P3—P5*	3/0.472
N7	2/2		*P6*	12/2
N8—N13	1/0.472		*P7-P8*	3/0.472
			P9	3/2
			P11—P10	3/0.472
			P12	120/0.472
			P13	300/0.472

Table 4: Performance parameters of the nFET-input OTA in Fig. 38.

Open-loop gain (A_{OL})	66 dB
Unity-gain frequency	107 MHz
Compensation capacitor	495 fF
Phase margin	72°
Common-mode range	± 1.63 V
Slew rate	37 V/μs

into the differential-output cascode stack. Because there are two types of differential input pairs, two common-mode feedback circuits are required. The nFET common-mode

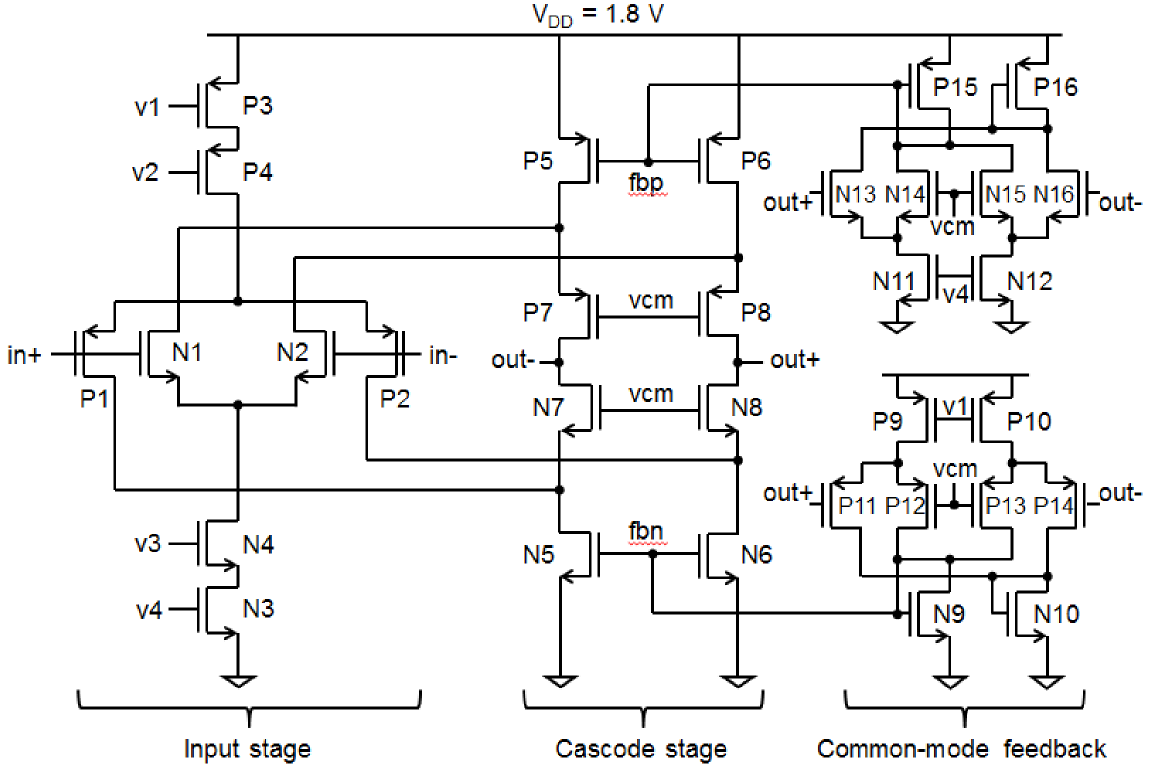


Fig. 40: Schematic of complementary-input OTA used in TG SHA. Each transistor is body-source tied. Bias voltages *v1*, *v2*, *v3*, and *v4* are generated in the bias circuit of Fig. 39. The sizes of the transistors in the OTA are listed in Table 5. The common-mode voltage *vcm* is generated with a resistor divider as in Fig. 38.

feedback controls the nFET current sources, and the pFET common-mode feedback controls the pFET current sources. As with the nFET OTA, the compensation capacitors are absent since the SHA topology provides the compensation. Table 6 summarizes the typical-process, post-layout parameters of the complementary OTA.

Table 5: Transistor sizes of complementary-input OTA in Fig. 40.

NFETs	W/L (μm/μm)		PFETs	W/L (μm/μm)
N1—N2	16/0.472		*P1—P2*	48/0.472
N3—N4	2/2		*P3—P4*	6/2
N5—N6	2.5/2		*P5—P6*	8/2
N7—N8	1/0.472		*P7—P8*	3/0.472
N9—N10	2/0.232		*P9—P10*	6/0.472
N11—N12	2/0.472		*P11—P14*	3/0.472
N13—N16	1/0.472		*P15—P16*	6/0.232

Table 6: Performance parameters of the complementary-input OTA in Fig. 40.

Open-loop gain (A_{OL})	69 dB
Unity-gain frequency	65 MHz
Compensation capacitor	495 fF
Phase margin	75°
Common-mode range	± 1.64 V
Slew rate	69 V/µs

The 45-nm differential S/H amp of Fig. 34 was designed with unity gain, i.e. $C_s = C_f$ = 495 fF. Spectre simulations were performed on the S/H amp in the nFET-only topology, i.e. nFET switches as in Fig. 36(a) and the nFET OTA of Fig. 38. The same simulations were also performed using the TG-based topology, i.e. TG switches as in Fig. 36(b) and the complementary OTA of Fig. 40. Both S/H amps were clocked at 1 MHz, and the response of each circuit to a voltage ramp input is plotted in Fig. 41. The plot shows how the TG switches of the TG S/H amp result in a nearly rail-to-rail signal range.

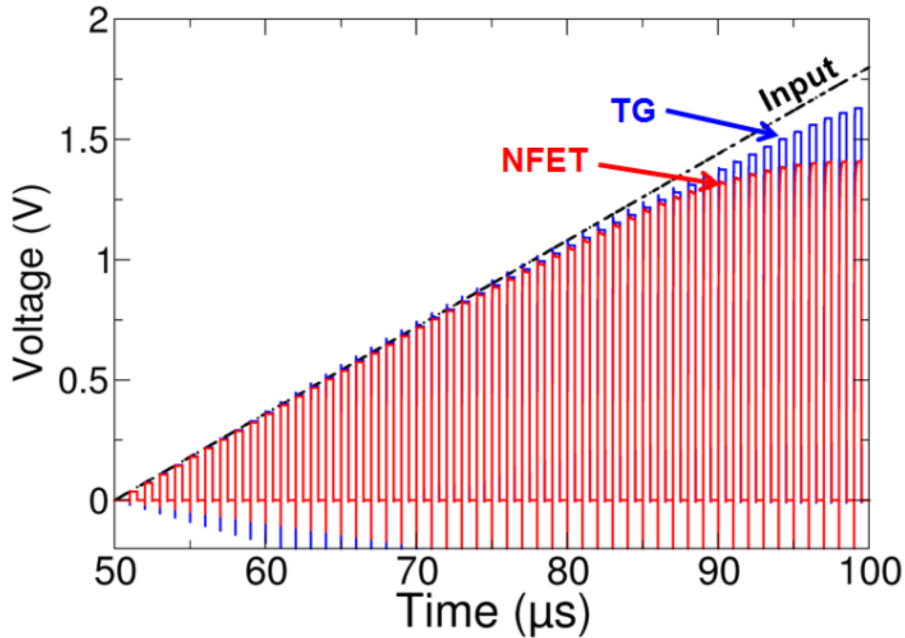


Fig. 41: Differential output of nFET and TG SHA with a voltage ramp input.

In fact, the limiting factor is the common-mode range of the complementary OTA design and not the switches. On the other hand the nFET S/H amp has an even more limited signal range. The signal over which each S/H amp can reproduce the output within 4-bits of precision is given in Table 7 along with the maximum sample rates, based on the slew rates of the OTAs. The signal range of the TG S/H amp is 50% greater than that of the nFET design, demonstrating the benefit of using a slightly more complicated switch network. In Chapter VI single-event hardening techniques on these two S/H topologies are discussed.

Table 7: Performance parameters of the nFET and TG SHAs.

	NFET	**TG**
Signal range	± 0.96 V	± 1.44
Max. sample rate	19 MS/s	24 MS/s

D. Summary

The basic theory of switched-capacitor circuits was discussed in this chapter. The example of the SC integrator was used to demonstrate the concept, and the differential sample/hold amplifier design used as a case study in this dissertation was presented. With the decreasing supply voltages of scaled CMOS processes, it is critical to maximize the voltage signal range of analog circuits. This is particularly important in the front-end stages of mixed-signal systems where the input voltage is initially sampled. Therefore, two S/H designs using nFET and transmission-gate switches were compared to demonstrate the difference in signal range; a 50% larger signal range was achieved using TG switches. In Chapter VI the quad-path technique for mitigating single events in TG-based SC circuits is presented, so signal range can be achieved without sacrificing radiation response.

CHAPTER V

RADIATION EFFECTS IN CONTINUOUS-TIME CIRCUITS

In this chapter radiation vulnerabilities and mitigation schemes in continuous-time circuits are discussed. In particular experimental measurements of the radiation response of the voltage reference components on the 180-nm test described in Chapter III are presented. An in-depth analysis of the radiation vulnerabilities of the design is used to propose radiation hardening schemes. The experimental results are used along with simulation to validate the proposed design techniques. The hardened designs include a modified version of the previously presented reference design and a novel voltage reference architecture that is well-suited to radiation-hardened design. Finally SEE mitigation schemes are presented using simulations.

A. Total dose effects and mitigation

The most difficult challenge in a precision voltage reference in radiation environment is the TID degradation. This section presents experiments, analyses, designs, and simulations with the end goal of mitigating TID degradation in continuous-time circuits, such as the voltage reference. In order to first demonstrate the measured effects of TID on CMOS voltage references, the 180-nm DTMOST and nFET voltage references described in Chapter III were exposed to X-ray radiation. The ARACOR Model 4100 10-keV x-ray source was used for irradiation. For convenience the schematics of each reference are reproduced in Fig. 42, with the actual values of R1 and

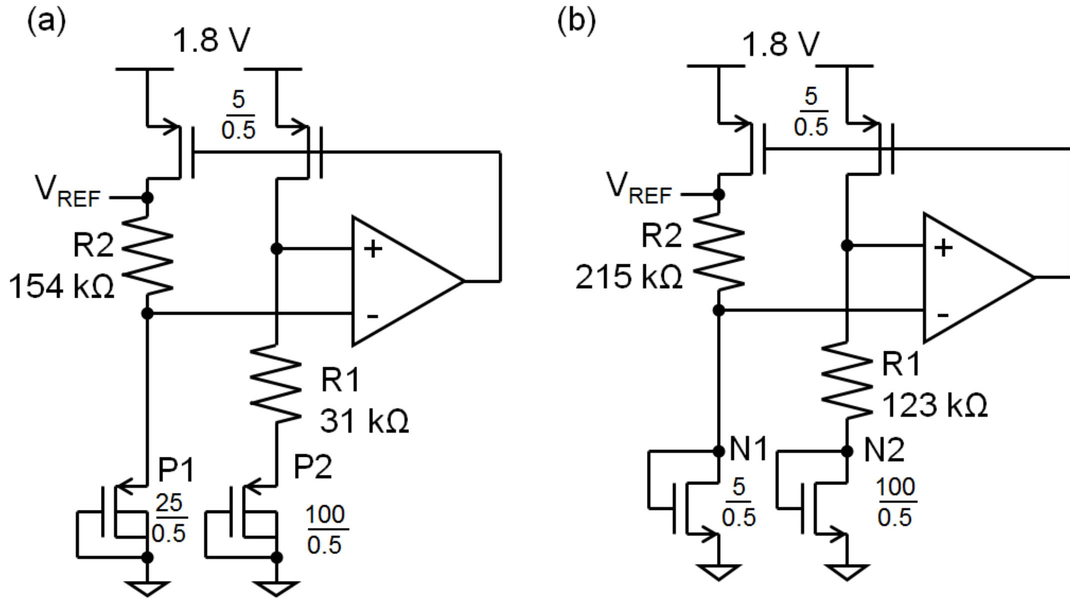


Fig. 42: (a) DTMOST reference. (b) NFET reference.

R2 indicated. Measurements were performed with the HP4156 parameter analyzer. The reference voltage was measured 1810 times and then averaged to quantify the variability of the measurement. Before irradiation, this measurement varied by up to 3 mV. Measurements were performed on the circuits using both standard-layout and edgeless-layout reference devices. At each step in the radiation exposure, the chip was powered off and placed in different reference configurations for measurement. In other words, all the references measured used the same exact op amp, current mirror, and resistor bank. The only differences between each design were the reference devices.

Figure 43 compares the percent change in the DTMOST reference voltage for standard and edgeless layouts. The pre-rad values were 488 mV for the standard layout and 503 mV for the edgeless layout. Because the DTMOSTs are constructed using pFETs, the edgeless layout makes little difference in the TID response. It is interesting that there is no clear trend in the response until a dose of 300 krad(SiO_2) is surpassed. This indicates a number of competing effects in the circuit, until perhaps one effect

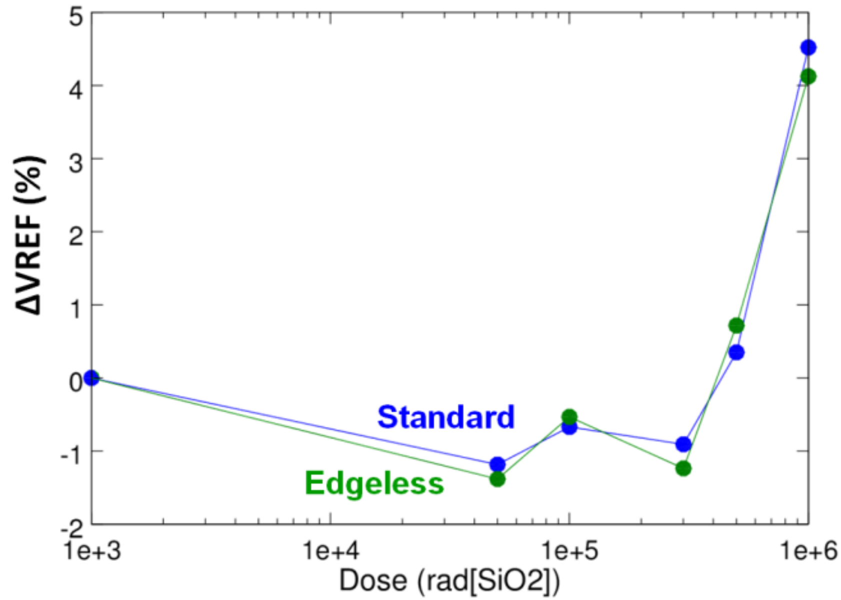


Fig. 43: Change in DTMOST reference output as a function of total dose.

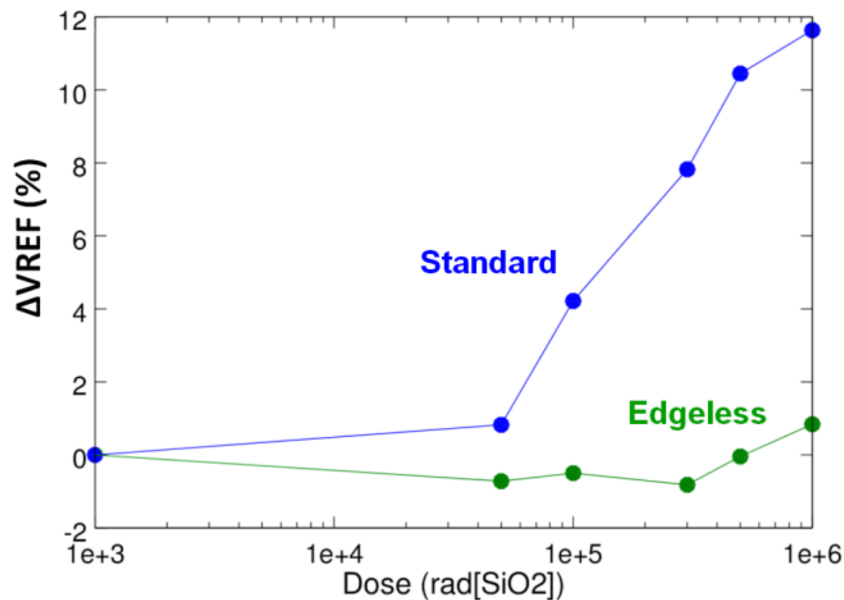


Fig. 44: Change in nFET reference output as a function of total dose.

dominates at dose levels of 500 krad and higher. The measured shifts in the voltage reference clearly indicate a need for mitigation, as shifts are greater than 4% at 1 Mrad.

Figure 44 compares the TID response of the standard and edgeless versions of the nFET-based reference. The pre-rad values were 567 mV in the standard layout and 544 mV in the edgeless layout. As expected, the edgeless transistor layout makes a marked

difference in the TID response. It is clear that the shift in output voltage of the standard-layout reference is due to STI leakage in the diode-connected nFETs in the reference, and this is confirmed by isolated measurements of the nFETs. However, the most interesting feature of the edgeless layout response is how the trend qualitatively matches that of the two DTMOST references. As will be discussed in the next section, the radiation degradation of the DTMOST and edgeless nFET references is dominated by the op amp, which is identical in the irradiated circuits. The edgeless nFET reference exhibits smaller voltage shifts simply because the gain of the circuit (R2/R1 = 1.75) is much smaller than the gain of the DTMOST circuit (R2/R1 = 4.97), so that the degradation of the op amp offset is amplified by a smaller factor. This and the other sources of radiation-induced degradation in the DTMOST reference are analyzed in detail in the next section.

Radiation vulnerabilities in CMOS voltage reference

By identifying the radiation vulnerabilities of the CMOS voltage reference—in particular the DTMOST-based reference—mitigation schemes can be devised. This was done through experimental investigation on the 180-nm test chip with isolated voltage reference components, as described in Chapter III. The test chip includes the following blocks used in the DTMOST reference design:

- DTMOSTs in standard and enclosed layouts
- Matched pairs of pFET current mirrors
- Matched pairs of p+ polysilicon resistors with resistances of 31 kΩ, 61.5 kΩ, and 123 kΩ
- Complementary folded-cascode op amps.

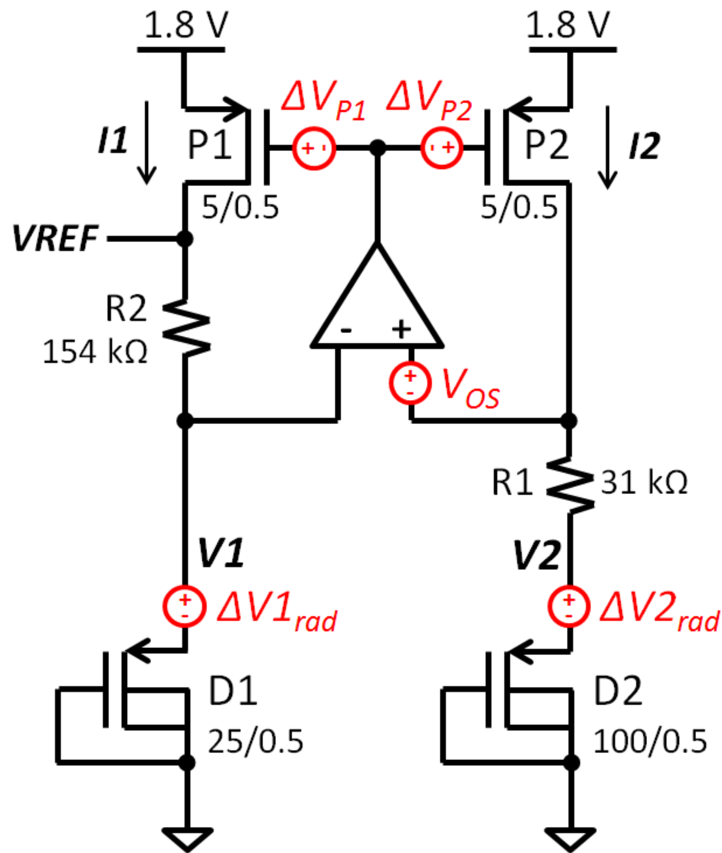


Fig. 45: DTMOST-based voltage reference. Red voltage sources indicate radiation-induced shifts.

The components on the test chip were designed to be externally connected to implement the DTMOST voltage reference of Fig. 45. The circuit consists of two DTMOSTs with W/L ratios 100/0.5 and 25/0.5 (µm/µm), two poly resistors, an op amp with input-referred offset V_{OS}, and a 1:1 pFET current mirror. The voltage sources in the schematic indicate the radiation-induced voltage shifts in the reference components; except for V_{OS}, these are ignored for the electrical analysis of the circuit. The op amp feedback in the circuit sets the non-inverting input voltage equal to $V1$, so the voltage drop across R1 is ($V1 - V2 - V_{OS}$), where $V1$, $V2$, and V_{OS} are the voltages labeled in Fig. 45. The 1:1 current mirror sets equal currents in each branch of the reference according to:

$$I = I1 = I2 = (V1 - V2 - V_{OS})/R1. \tag{45}$$

This results in an output voltage of:

$$VREF = V1 + \frac{R2}{R1}(V1 - V2 - V_{OS}). \tag{46}$$

As discussed in [58], [59], the DTMOSTs provide voltages with negative temperature coefficients (tempcos) depending on current density. Since D2 has a lower current density than D1, the tempco of *V2* is more negative than that of *V1*. Therefore, the difference *(V1 – V2)* has a positive tempco. By summing *V1* and the difference of *V1* and *V2* amplified by the resistor ratio *R2/R1*, first-order tempco cancellation is achieved in the output voltage *VREF* in (46). This cancellation is very similar to that of a first-order bandgap reference. Unfortunately, the offset voltage of the op amp is also amplified and contributes to temperature drift in the output.

Separating the components on the chip provided the ability to individually track the radiation response of each block in the reference circuit. The components on the test chip were irradiated using the ARACOR 4100 10-keV X-ray source. Biases were applied and shifts in device operation were measured using the HP4156B Semiconductor Parameter Analyzer. Since the poly resistors were the only components to show no radiation-induced degradation, the results are focused on the op amp, the reference devices (DTMOSTs), and the current mirror.

<u>Op amp offset voltage</u>

The test chip contained two identical op amps with 0.5-μm channel-length input transistors, and two identical op amps with 2-μm channel-length input transistors. The only other difference in the op amp designs was the size of the compensation capacitor.

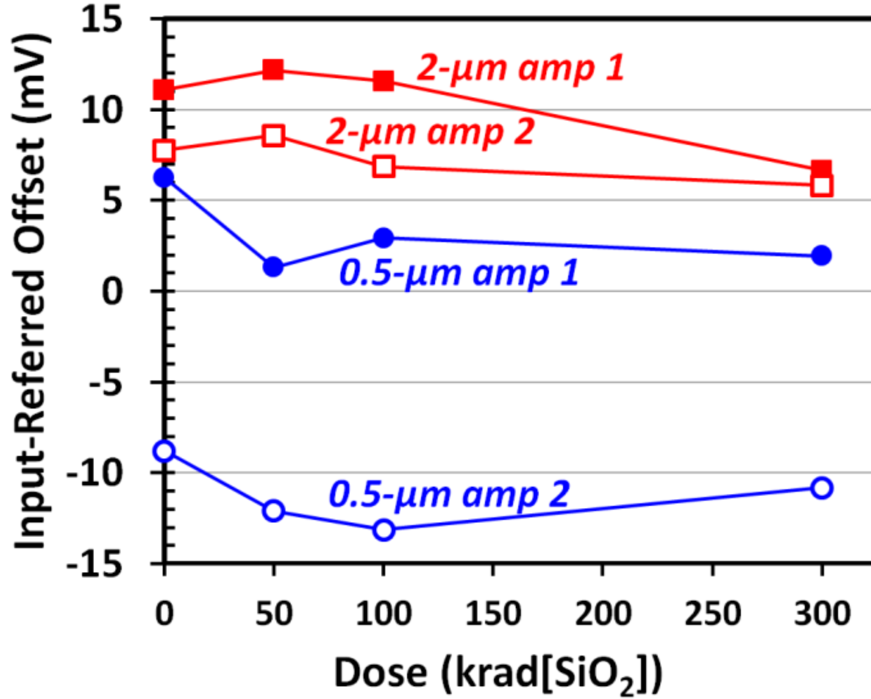


Fig. 46: Radiation-induced shifts in op amp offset voltage. The labels "0.5-µm" and "2-µm" indicate the channel length of the input transistors of the op amp.

These op amps are the same as those simulated and tested in [91], [95], [113].The input-referred offset voltages of the op amps are plotted as a function of total ionizing dose in Fig. 46. During irradiation each op amp was powered with a 1.8-V supply and configured as a voltage follower with a half-rail input voltage. The offset was measured by calculating the difference between the output voltage and the input voltage of 0.9 V. All four tested op amps showed significant shifts in offset voltage V_{OS}, ranging from 2.8 to 5.5 mV. Degradation in the open-loop gain of the op amps was negligible.

The offset voltage is amplified in the *VREF* output (46) and affects the DTMOST bias currents *I1* and *I2* (45). The changes in DTMOST voltages $\Delta V1$ and $\Delta V2$ caused by the change in bias current ΔI depend on their small-signal equivalent resistances as follows:

$$\Delta V1 = \Delta I\ r_{s1} \text{and } \Delta V2 = \Delta I\ r_{s2}, \tag{47}$$

where $\Delta I = \Delta I1 = \Delta I2$, and r_{s1} and r_{s2} are the small-signal resistances of D1 and D2, respectively. These resistance values depend on the gate transconductance, back-gate transconductance, and channel length modulation (r_0), with the forward-biased source-body junction contributing little to current conduction at the typical voltages of operation (< 0.3 V). Substituting the voltage shifts for $V1$, $V2$, and V_{OS} in (45) yields the shift in bias current:

$$\Delta I = \frac{\Delta V1 - \Delta V2}{R1} - \frac{\Delta V_{OS}}{R1}. \tag{48}$$

Substituting (47) into (48) and solving for ΔI yields the bias current shift as a function of the offset voltage shift:

$$\Delta I = -\frac{\Delta V_{OS}}{R1 - (r_1 - r_2)}. \tag{49}$$

The change in VREF output as a function of the changes in $V1$ and the bias current I is:

$$\Delta VREF = \Delta V1 + R2\,\Delta I. \tag{50}$$

Substituting (47) and (49) into (50) finally yields the shift in $VREF$ caused by a shift in V_{OS}:

$$\Delta VREF = -\frac{R2 + r_{s1}}{R1 - (r_{s1} - r_{s2})} \Delta V_{OS}. \tag{51}$$

At a bias current of 5 µA, the DTMOST small-signal resistances r_{s1} and r_{s2} have values of approximately 8 kΩ and 6.67 kΩ, respectively. Substituting these values along with the resistor values from Fig. 45 into (51) reveals that offset voltage shifts are amplified by a gain of -5.5 V/V in the $VREF$ output. The magnitude of this gain is slightly higher than the $R2/R1$ ratio in (46) because of the additional shift in bias current caused by the V_{OS} shift. Therefore, even a V_{OS} shift of 2.8 mV—as measured in Fig. 46—causes a shift of -15.4 mV in the VREF design of Fig. 45. The nominal output voltage of the circuit is approximately 460 mV, so this shift is greater than 3%.

Radiation experiments revealed the offset voltage as the most sensitive parameter of the op amp. The open-loop gain and power supply rejection—important parameters for precision—showed negligible degradation. The tested op amps have a complementary folded-cascode architecture [111], which includes both nFET and pFET input transistors, as shown in Fig. 19. The nFET input transistors, being composed of multiple cells in parallel, present significant radiation vulnerability in the leakage currents induced by radiation at the STI boundaries of the channels. In addition to the input transistors, the current source devices in the cascode stage contribute significantly to the offset voltage of the op amp. The initial offset voltage of the op amp is primarily dependent on random process variation that fundamentally results in device mismatch. This initial offset results in slightly different internal bias voltages between matched pairs in the op amp. Therefore, the radiation response of each device will vary slightly, resulting in further radiation-induced offset shift. The same mechanism contributes to temperature drift of offset voltages. The result of Fig. 46 and the analysis of (47)-(51) clearly indicate that the op amp offset voltage is a significant vulnerability in the voltage reference that must be mitigated.

DTMOST reference devices

The DTMOSTs in the reference of Fig. 45 directly generate the VREF output with first-order tempco cancellation, so the radiation response of the reference fundamentally depends on the response of these devices. The radiation response of edgeless layout 100/0.5 DTMOSTs at several bias points is plotted in Fig. 47. During X-ray irradiation, each device was biased at the indicated voltage. I-V sweeps were recorded between each

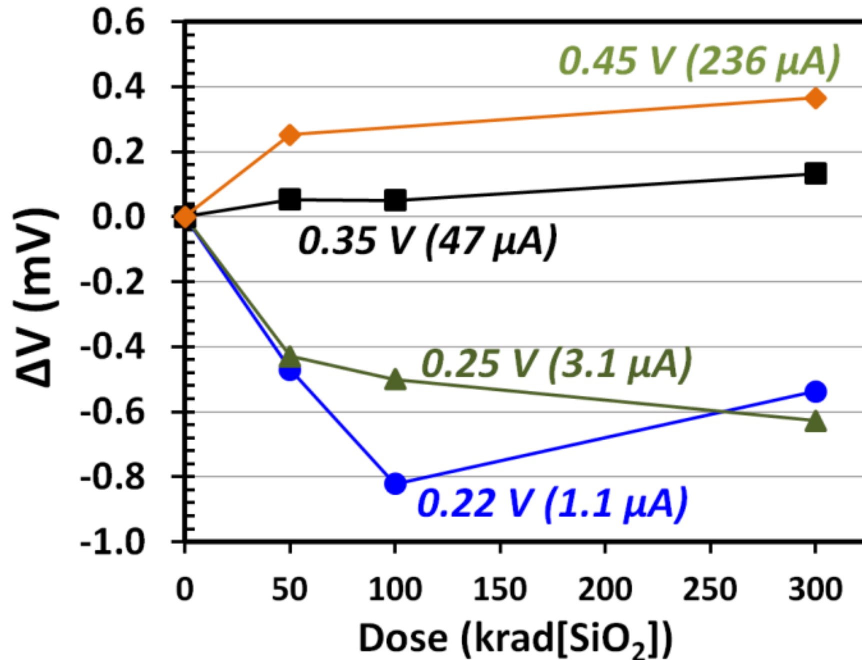


Fig. 47: Radiation-induced voltage shifts in edgeless DTMOSTs with 100 μm width and 0.5 μm length at various bias points. The voltage labels indicate the bias voltage during irradiation, and the current labels indicate the corresponding current. The voltage shift is reported as the change in voltage with the device sinking a constant current (indicated in parenthesis), which corresponds to the pre-rad bias point.

irradiation level, and the voltage required for the device to sink the current indicated in parentheses was calculated from the sweeps. This current corresponds to the pre-rad current at the specified bias voltage. The curves in Fig. 47 show the shift in operating voltage required to maintain a constant current. From a circuit perspective it is useful to consider the device degradation in this way, since it more closely reflects how device operation will change in a circuit than calculating parameters such as threshold voltage shifts. Furthermore, the on-chip connections of the DTMOSTs prevented conventional measurements of device parameters. Representing radiation degradation in this manner basically lumps all radiation effects—oxide charge, interface charge, leakage, etc.—into a single voltage shift at a particular bias point.

Overall, the DTMOSTs exhibit a resilient response to ionizing radiation with voltage shifts ranging from 800 μV to less than 200 μV with dose levels up to

300 krad[SiO_2]. The specific radiation response of these devices is mostly dependent on the process itself, but it does indicate that relatively small shifts are achievable in even a 180-nm process. In more advanced processes, it is reasonable to expect similar or better radiation response, due to the thinner oxides that are less vulnerable to the charge trapping that causes threshold voltage shifts.

The bias dependence of the voltage shifts in Fig. 47, however, is a general trend that is present in any process. The voltage reference architecture requires the two DTMOSTs to be biased at different current densities to generate different tempcos for cancellation. These different bias points result in different radiation responses in the two devices (as shown in Fig. 47), so it is important to analyze the effect of shifts in the DTMOST voltages $\Delta V2_{rad}$ and $\Delta V2_{rad}$ on the *VREF* output. If the radiation-induced shifts in *V1* and *V2* are defined as $\Delta V1_{rad}$ and $\Delta V2_{rad}$, then the overall shifts in *V1* and *V2* can be expressed as a function of the radiation-induced shifts and the resulting bias current shift:

$$\Delta V1 = \Delta V1_{rad} + \Delta I\, r_{s1}, \text{and } \Delta V2 = \Delta V2_{rad} + \Delta I\, r_{s2}, \tag{52}$$

where r_{s1} and r_{s2} are the small-signal equivalent resistances of D1 and D2, as defined in the previous section. Considering the radiation-induced shift of *V2* relative to that of *V1*, the difference between shifts can be defined as:

$$\Delta V_{diff} = \Delta V2_{rad} - \Delta V1_{rad}. \tag{53}$$

Substituting the voltage shifts of (52) into (45) and ignoring the op amp offset voltage yields the bias current shift:

$$\Delta I = \frac{\Delta I}{R1}(r_{s1} - r_{s2}) + \frac{\Delta V1_{rad} - \Delta V2_{rad}}{R1}. \tag{54}$$

Solving this for ΔI while substituting (53) yields the bias current shift:

$$\Delta I = -\frac{\Delta V_{diff}}{R1 - (r_{s1} - r_{s2})}. \tag{55}$$

The current shift shows the same dependence on ΔV_{diff} that it did on the op amp offset voltage ΔV_{OS} in (49). Substituting (52) and (55) into the general *VREF* equation (50) yields the *VREF* shift dependence on the DTMOSTs:

$$\Delta VREF = \Delta V1_{rad} - \frac{R2+r_{s1}}{R1-(r_{s1}-r_{s2})}\Delta V_{diff}. \tag{56}$$

While the radiation-induced shift in *V1* appears directly in the *ΔVREF* term, the difference between *V2* and *V1* shifts (ΔV_{diff}) is amplified by the same factor as the op amp offset in (51).

This analysis indicates that even though the DTMOSTs may exhibit small radiation-induced shifts, the difference in shifts has an amplified effect on the *VREF* output. For instance, the -5.5-V/V gain previously calculated for op amp offset will cause a 200-μV difference in shifts to change the *VREF* output by more than a millivolt. Although the shift in *V1* appears directly in the output, the limiting factor for the reference radiation response is the difference between DTMOST radiation responses. Unlike the op amp offset voltage the difference in DTMOST voltage shifts is systematic, since different bias points are required for tempco cancellation.

Current mirror mismatch

The final voltage reference vulnerability to discuss is the current mirror formed by P1 and P2 in Fig. 45. The pFETs supply current to the reference devices, so matching is critical in the current mirror. The radiation responses of three pFETs on the same 180-nm chip are plotted in Fig. 48. The plot tracks the source-gate voltage V_{SG} required to source 5 μA with a source-drain voltage V_{SD} of 1.75 V. During the irradiation V_{SG} was biased at 0.9 V with V_{SD} at similar biases—12 mV and 18 mV. By referring the radiation response

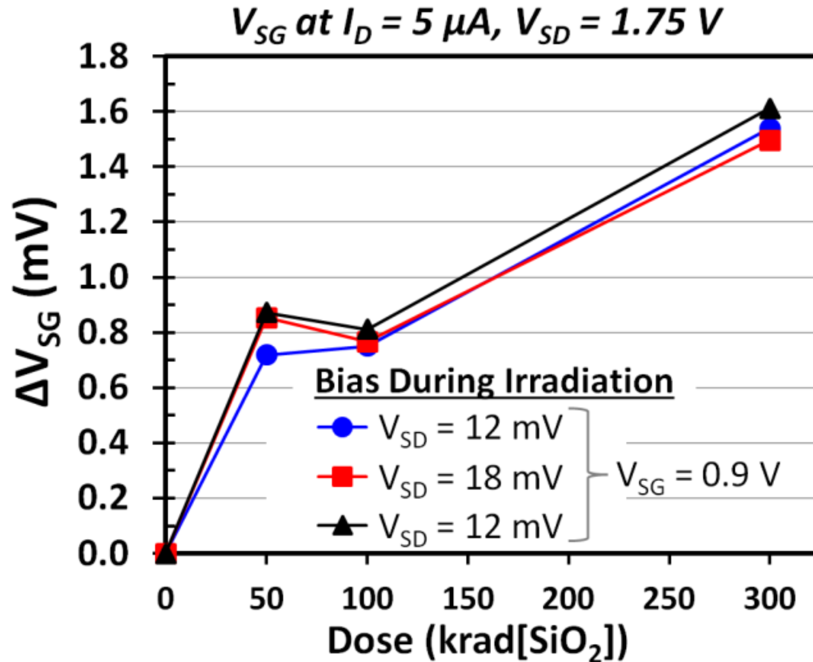


Fig. 48: Radiation response of pFETs with 5 μm width and 0.5 μm length. The shift in source-gate voltage required to source 5 μA with source-drain voltage of 1.75 V is plotted. All gates were biased at 0.9 V during X-ray irradiation.

to shifts on the gate voltage, the impact of the pFETs on the voltage reference can be analyzed, as indicated by the voltage sources ΔV_{P1} and ΔV_{P2} in Fig. 45. With similar biases during irradiation, the three pFETs show very similar gate voltage shifts. At 300 krad[SiO_2], all three gate voltages shift by approximately 1.5 mV. The largest difference between gate voltage shifts was 150 μV.

The primary impact the current mirror has on the voltage reference in Fig. 45 is the radiation-induced mismatch. For proper functionality the currents *I1* and *I2* must be equal as in (45). If the radiation-induced voltage shifts of P1 and P2 are perfectly matched, then *I1* = *I2* and the VREF output is negligibly affected. Random mismatch in the process of fabricating the circuit will result in some initial error in the current mirror. However, when this mismatch is altered by ionizing radiation—even to the small degree exhibited in Fig. 48—it can have a significant impact on the *VREF* output.

A current mirror offset voltage ΔV_{OP} is defined as the difference between the gate voltage shifts of P1 and P2:

$$\Delta V_{OP} = \Delta V_{P1} - \Delta V_{P2}. \quad (57)$$

By assuming the transconductances of P1 and P2 are equal to g_{mp}, the current error ΔI_{err} can be expressed in terms of ΔV_{OP}

$$\Delta I_{err} = \Delta I1 - \Delta I2 = -g_{mp}\Delta V_{OP}. \quad (58)$$

Combining the fact that $I2 = (V1 - V2)/R1$ with the current error in (58), the change in $I1$ can expressed as:

$$\Delta I1 = \frac{\Delta V1 - \Delta V2}{R1} - g_{mp}\Delta V_{OP}. \quad (59)$$

Using the DTMOST small-signal resistances to substitute $\Delta V1$ and $\Delta V2$ with $\Delta I1\ r_{s1}$ and $\Delta I2\ r_{s2}$, respectively, in (59) yields the following expression for $\Delta I1$:

$$\Delta I1 = -\frac{R1 + r_{s2}}{R1 - (r_{s1} - r_{s2})} g_{mp}\Delta V_{OP}. \quad (60)$$

Finally, substituting (60) into the $VREF$ shift in (50) reveals the effect of current mirror offset on the reference voltage:

$$\Delta VREF = -\frac{(R2 + r_{s1})(R1 + r_{s2})}{R1 - (r_{s1} - r_{s2})} g_{mp}\Delta V_{OP}. \quad (61)$$

This equation contains additional amplification compared to the op amp and DTMOST offset voltages, due to the transconductance of the pFETs g_{mp}. This indicates a higher level of sensitivity to the current mirror.

As before it is informative to demonstrate the circuit impact with an example. At 5 μA the pFET transconductance is equal to 63 μS. Using the DTMOST equivalent resistances from the previous sections—8 kΩ and 6.67 kΩ—it can be seen that ΔV_{OP} is amplified by -13 V/V. The magnitude of this amplification is larger than previously seen

because of the additional $(R1 + r_{s2})\, g_{mp}$ term, which increase the gain by a factor of 2.4. Therefore, even a relatively small current mirror offset shift of 150 μV will cause nearly 2 mV of reference voltage shift. The measurements on the 180-nm chip indicate that offset shifts in the current mirror can be expected to be relatively small (< 1 mV) due to the simplicity of the circuit block—two devices at identical gate voltages. This is in contrast to the op amp where several transistor pairs—including both n- and p-type transistors—independently contribute to the offset voltage, resulting in shifts of several millivolts.

Since the effects of the three discussed radiation vulnerabilities are independent of each other, the principle of superposition can be used to combine the effects into a single expression for voltage reference shifts:

$$\begin{aligned} \Delta VREF = \; & -A\Delta V_{OS} \\ & + \Delta V1_{rad} - A(\Delta V2_{rad} - \Delta V1_{rad}) \\ & - A\left(R1 + \frac{1}{g_{m2}}\right) g_{mp}(\Delta V_{P1} - \Delta V_{P2}), \end{aligned} \tag{62}$$

where A is the fundamental system gain that was identified in all three previous computations as:

$$A = \frac{(R2 + r_{s1})}{R1 - (r_{s1} - r_{s2})} \,. \tag{63}$$

Equation (62) summarizes the reference susceptible to radiation-induced degradation in the fundamental circuit blocks, showing the contributions of each block on a separate line. The delta terms of the equation correspond to the voltage sources in Fig. 45. All mismatch components in the equation are amplified by the system gain A, with an additional gain factor on the current mirror mismatch. The component with the largest output amplification is the current mirror, but the component with the largest measured

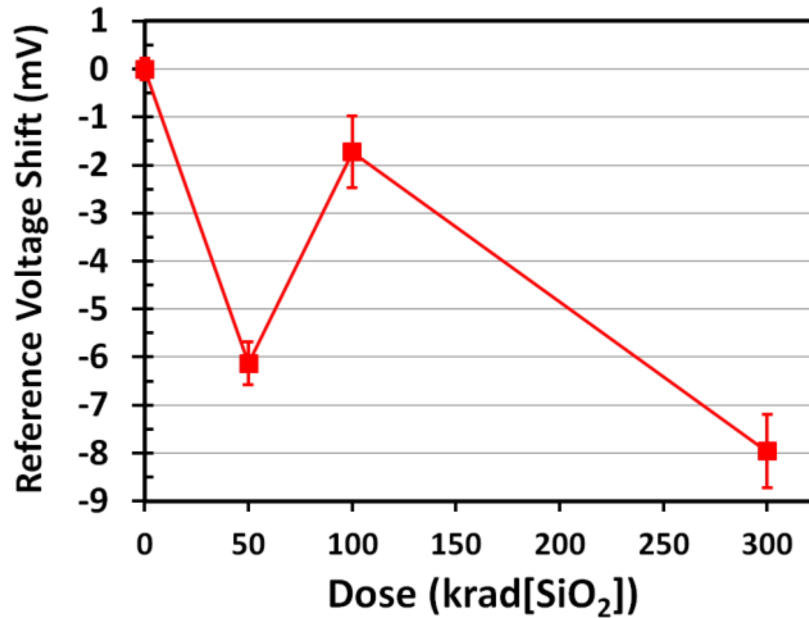


Fig. 49: Radiation-induced shift in voltage reference. The pre-rad output voltage was 484 mV. Each point is the mean of 1010 samples, with the error bars indicating the standard deviation.

shifts is the op amp by a significant margin. While it is possible for the terms in the equation to cancel each other out to some extent, such an effect is not predictable, as the radiation-induced mismatch is strongly linked to the initial mismatch resulting from random process variation.

The voltage reference of Fig. 45 was irradiated and the radiation response is plotted in Fig. 49. The reference shows nearly 8 mV degradation—1.7% of the pre-rad value of 484 mV. The maximum acceptable VREF shift in data conversion is set by the quantization error of ½ LSB. In a 4-bit analog-to-digital conversion, ½ LSB corresponds to 3.1%. If the voltage reference shifts 1.7%, then the highest precision the reference can support in a radiation environment is 4 bits.

Measurements of the DTMOSTs showed voltage shifts less than 1 mV (0.2% or 7 bits) are achievable. However, the sources of radiation-induced mismatch in the voltage reference dominate the radiation response, significantly limiting the precision. The

presented results and circuit analysis demonstrate the need to mitigate the effects of mismatch in the voltage reference. The generalized circuit analysis in particular indicates that the mismatch effects can be expected to dominate the response in any fabrication process. Furthermore, the small-signal analysis provides a general framework for analyzing radiation effects in other continuous-time circuits.

Radiation hardening of voltage reference using chopper stabilization

Dynamic offset cancellation: chopper stabilization

The fundamental vulnerabilities of the voltage reference were identified as the sources of offset that can be altered by ionizing radiation, so the radiation response of the circuit can be significantly improved by employing dynamic offset cancellation. While there are several well-established offset cancellation techniques, the technique best-suited to a DC circuit like a voltage reference is chopper stabilization, as opposed to the auto-zero and correlated double sampling methods which are well suited to sampled-data circuits [115]–[117]. More conventional methods for reducing mismatch—primarily transistor sizing—only serve to reduce the initial random mismatch of a fabrication process. A dynamic scheme is required for radiation hardening because the transistor mismatch in a circuit can be altered by ionizing radiation.

The chopper stabilization technique is summarized in Fig. 50. In Fig. 50(a) the chopper circuit is introduced along with its schematic symbol. The circuit consists of two inputs, two outputs, and four switches controlled on clocks 1 and 2. The two clocks operate in non-overlapping phases 1 and 2. In phase 1 switches labeled ‘2’ are open, and switches labeled ‘1’ are closed, connecting *IN1* to *OUT1* and *IN2* to *OUT2*. In phase 2 the

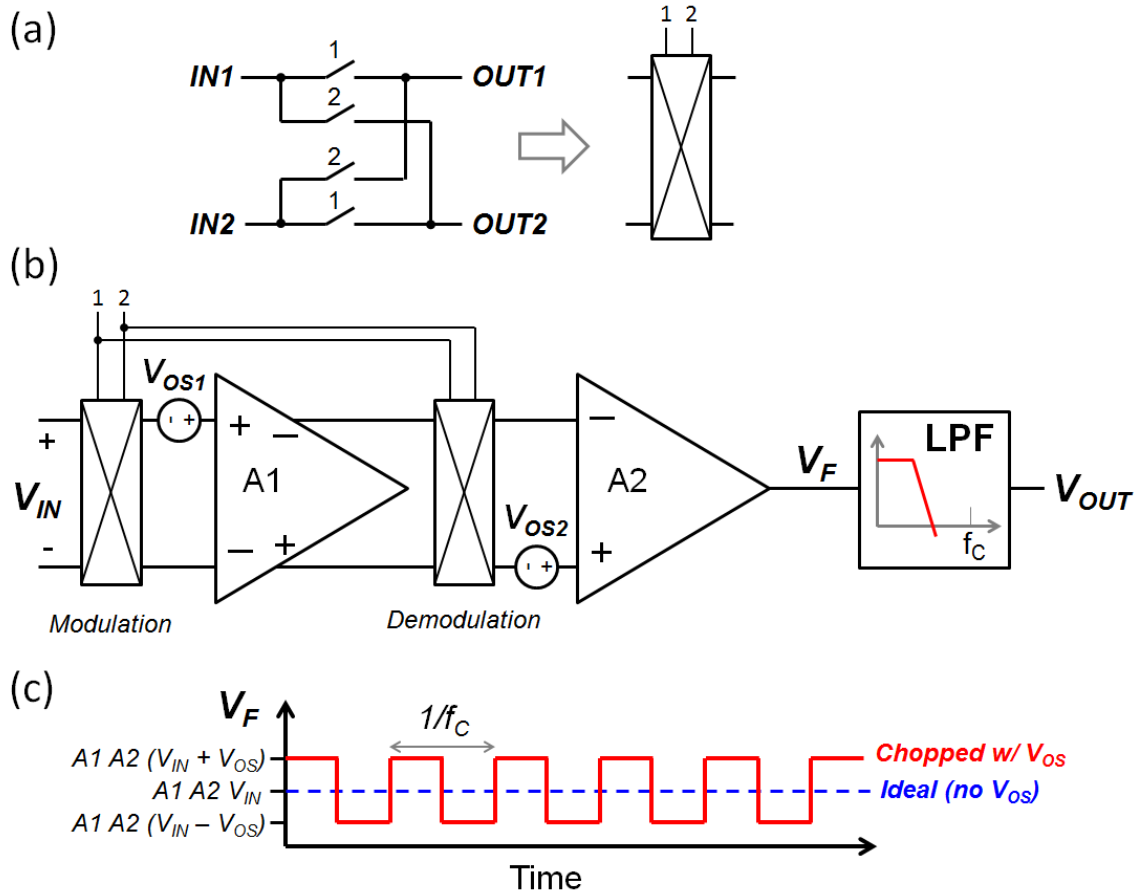


Fig. 50: (a) Chopper schematic symbol. (b) Chopper amplifier with single-ended output and low-pass filter. (c) Time-domain representation of unfiltered output V_F with and without offset voltage $V_{OS} \approx V_{OS1}$.

opposite is true and *IN1* and *IN2* are connected instead to *OUT2* and *OUT1*, respectively. Assuming a differential signal is connected across *IN1* and *IN2*, the chopper periodically reverses the polarity of the signal at the differential output, which modulates the signal to a square wave at the chopping frequency f_C. In Fig. 50(b) the implementation of a chopper amplifier—or chopper-stabilized amplifier—is illustrated. The circuit consists of a fully-differential input stage with gain *A1* and input-referred offset V_{OS1}, a single-ended output stage with gain *A2* and input-referred offset V_{OS2}, two choppers, and a low-pass filter (LPF). The chopper on the differential input modulates the input signal to the chopping frequency. The second chopper serves the dual purpose of demodulating the

signal back to DC and modulating the offset voltage (along with the low-frequency noise) of the input stage to the chopping frequency. The LPF is necessary to filter out the modulated circuit non-idealities.

Figure 50(c) shows the unfiltered output V_F in the ideal case where there is no offset and in the case where the offset is chopped. In phase 1 the voltage V_F can be expressed as:

$$V_F = A1\,A2\left(V_{IN} + V_{OS1} + \frac{V_{OS2}}{A1}\right), \tag{64}$$

where V_{IN} is the input signal and $V_{OS1}+V_{OS2}/A1$ is the overall input-referred offset voltage. Since $A1$ is large, the offset voltage can be approximated as simply $V_{OS} \approx V_{OS1}$, meaning V_{OS2} contributes negligibly. Similarly V_F in phase 2 can be expressed as:

$$V_F = A1\,A2(V_{IN} - V_{OS}), \tag{65}$$

where the polarity of the offset has been reversed, relative to (64) With sufficient filtering the amplitude of the square wave in Fig. 50(c) is reduced such that the output V_{OUT} is near the ideal value of the dashed line—equal to the average of phase 1 and phase 2 values of V_F. There are limitations to the offset cancellation achieved with the modulation and demodulation of this scheme. These are primarily related to non-idealities in the MOSFET switches, such as charge injection and clock feedthrough that result in residual offset in the circuit. For more details on chopper stabilization, the reader is referred to [116].

RHBD chopper voltage reference design

The proposed radiation-hardening scheme for the voltage reference is presented in Fig. 51. The pFET current mirror is replaced with a single pFET current source, and

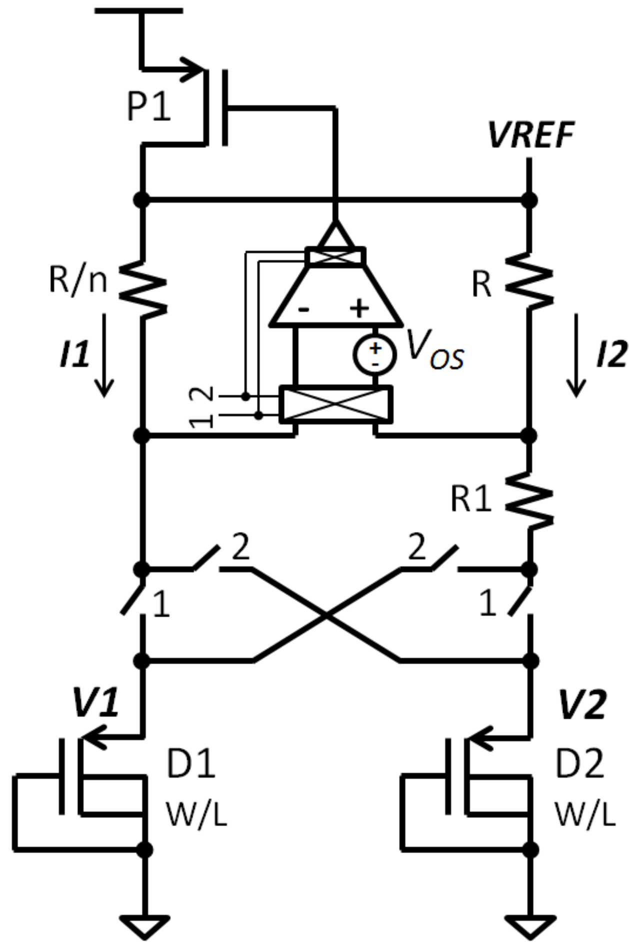


Fig. 51: Radiation-hardened voltage reference design.

resistors with values *R* and *R/n* are used to scale the bias currents of the DTMOSTs by a factor of *n*. Eliminating the current mirror eliminates one of the dominant sources of radiation-induced mismatch that is amplified in the output voltage. The op amp feedback creates a virtual short between inputs, ensuring the voltage drop across each resistor is equal. The resistor pair can easily be implemented with parallel combinations of unit-cell resistors. By scaling the bias currents—rather than sourcing identical currents—the DTMOSTs D1 and D2 can be identical. The interchangeable nature of the two reference devices allows chopping of D1 and D2 by the switches labeled '1' and '2'. In phase 1, the current *I1* flows through D1, and the current *I2* flows through D2. In phase 2, each of the

currents is redirected to the other DTMOST—*I1* to D2 and *I2* to D1. The voltages of D1 at the bias currents *I1* and *I2* can be defined as $V_{D1}(I1)$ and $V_{D1}(I2)$, respectively. The voltages of D2 are similarly defined as $V_{D2}(I1)$ and $V_{D2}(I2)$. The chopper symbols on the op amp input and output indicate the op amp is also chopper-stabilized by the same clocks 1 and 2. As discussed in the previous section, the chopper inverts the input-referred offset voltage of the op amp in each phase. During phase 1 the input-referred offset voltage is V_{OS}, and during phase 2 the offset is $-V_{OS}$. Since the reference is no longer a strictly continuous-time circuit, a dual-phase analysis is necessary to determine the output voltage *VREF*.

In phase 1 the current *I2* is:

$$I2_{phase1} = \frac{V_{D1}(I1) - V_{D2}(I2)}{R1} - \frac{V_{OS}}{R1}, \tag{66}$$

and *I1* is:

$$I1_{phase1} = n\frac{V_{D1}(I1) - V_{D2}(I2)}{R1} - nV_{OS}\left(\frac{1}{R} + \frac{1}{R1}\right). \tag{67}$$

Using (67) the circuit output during phase 1 can be expressed as the voltage drop across D1 plus the IR drop across *R/n*:

$$VREF_{phase1} = V_{D1}(I1) + \frac{R}{R1}[V_{D1}(I1) - V_{D2}(I2)] - V_{OS}\left(1 + \frac{R}{R1}\right). \tag{68}$$

In phase 2 the bias current *I2* is:

$$I2_{phase2} = \frac{V_{D2}(I1) - V_{D1}(I2)}{R1} + \frac{V_{OS}}{R1}, \tag{69}$$

and *I1* is:

$$I1_{phase2} = n\frac{V_{D2}(I1) - V_{D1}(I2)}{R1} + nV_{OS}\left(\frac{1}{R} + \frac{1}{R1}\right). \tag{70}$$

In phase 2 the V_{D1} and V_{D2} terms are swapped and the sign of the op amp offset V_{OS} is inverted. Using (70) the circuit output during phase 2 can be expressed as:

$$VREF_{phase2} = V_{D2}(I1) + \frac{R}{R1}[V_{D2}(I1) - V_{D1}(I2)] + V_{OS}\left(1 + \frac{R}{R1}\right). \quad (71)$$

As with the currents, the DTMOST voltage and op amp offset signs are reversed. When the op amp output is low-pass filtered, the bias currents and reference voltage become averages of the phase 1 and 2 values, assuming a 50% duty cycle. An efficient method for implementing this filter is using an operational transconductance amplifier (OTA) in the design. A large capacitive load can be placed on the high-impedance OTA output to create an effective low-pass filter, as in [118]. The filtered current *I1* can be expressed as the average of $I1_{phase1}$ and $I1_{phase2}$:

$$I1 = \frac{n}{2}\frac{V_{D1}(I1) - V_{D2}(I2) + V_{D2}(I1) - V_{D1}(I2)}{R1}. \quad (72)$$

Similarly, the filtered current *I2* is:

$$I2 = \frac{1}{2}\frac{V_{D1}(I1) - V_{D2}(I2) + V_{D2}(I1) - V_{D1}(I2)}{R1}. \quad (73)$$

Because the op amp chopper reverses the polarity of V_{OS} each phase, the offset term is cancelled out when the phases are averaged by the low-pass filter. The filtered *VREF* output is:

$$VREF = \frac{1}{2}[V_{D1}(I1) + V_{D2}(I1)] + \frac{1}{2}\frac{R}{R1}[V_{D1}(I1) - V_{D2}(I2) + V_{D2}(I1) - V_{D1}(I2)]. \quad (74)$$

As with the currents, the op amp offset is cancelled out.

The expressions in (72)-(74) also illustrate how DTMOST mismatch is eliminated. If $\Delta V1$ and $\Delta V2$ voltage sources are connected to the DTMOSTs D1 and D2 in Fig. 51 to represent the radiation-induced voltage shift—as done in Fig. 45—then the current *I1* after filtering can be computed as:

$$I1 = \frac{n}{2}\frac{[V_{D1}(I1)+\Delta V1]-[V_{D2}(I2)+\Delta V2]+[V_{D2}(I1)+\Delta V2]-[V_{D1}(I2)+\Delta V1]}{R1}$$

$$= \frac{n}{2}\frac{V_{D1}(I1)-V_{D2}(I2)+V_{D2}(I1)-V_{D1}(I2)}{R1}. \quad (75)$$

Because the filtered current contains both plus and minus terms of V_{D1} and V_{D2}, the voltage shifts $\Delta V1$ and $\Delta V2$ appear in both polarities, resulting in cancellation of the voltage shifts. Therefore the shift in *I1* can be expressed as:

$$\Delta I1 = n\,\Delta I2 = \frac{n}{2}\frac{\Delta V1-\Delta V1+\Delta V2-\Delta V2}{R1} = 0. \quad (76)$$

By inspection, the shift in the *VREF* output voltage can be similarly computed:

$$\Delta VREF = \frac{1}{2}[\Delta V1 + \Delta V2] + R\,\Delta I1 = \frac{1}{2}[\Delta V1 + \Delta V2]. \quad (77)$$

By chopping the reference devices D1 and D2, the difference between their voltage shifts is cancelled. This simply leaves the average of the two voltage shifts $\Delta V1$ and $\Delta V2$ as the dominant shift in reference voltage.

The primary goal of the topology of Fig. 51 was eliminating the amplified terms in the radiation-induced reference voltage shift computed in (62). The resistive biasing scheme eliminated the term with the highest amplification, the current mirror. The chopping scheme in the op amp eliminated the impact of the op amp offset, the term with the largest measured shifts in a radiation environment. Finally, the chopping scheme in the reference devices eliminated the amplified difference between voltage shifts. The final result is the reference voltage shift in (77) which depends only on the reference device shifts without any amplification. The proposed scheme eliminates the effects of mismatch in the voltage reference, allowing the output to take advantage of the radiation tolerance of the DTMOST reference devices.

Another benefit of chopper stabilization is improved low-frequency noise performance. The noise at frequencies lower than the chopping frequency is significantly reduced when it is modulated to the chopping frequency and filtered out. This increases the precision of the voltage reference by mitigating the output noise.

The primary design tradeoff in chopper stabilization is bandwidth. Since it is necessary to filter out the square wave created by the chopper modulation and demodulation, the system bandwidth is ultimately limited by this filtering. Typically in chopper-stabilized amplifiers, the filter is designed with a cutoff frequency at approximately half the chopper frequency. The ideal chopper frequency is the noise corner of a circuit at which the flicker and thermal noise components are equal, because this ensures significant reduction in flicker noise. However, the chopper frequency is limited by the bandwidth of the system [116]. Furthermore, increasing the chopper frequency exacerbates parasitic effects—such as charge injection and dynamic input bias currents—that introduce residual offset in a chopper-stabilized circuit [116]. Because of these design considerations, chopper stabilization is primarily used in circuits that require high levels of precision rather than speed. The voltage reference is such a circuit, requiring DC precision above all else. While the speed penalty of chopper stabilization can significantly slow down start-up time, the lack of high-frequency signal handling in a voltage reference makes the chopper scheme highly suitable.

In previous work dynamic offset cancellation has been used to reduce the initial error and temperature drift of bandgap references [117], [119]–[123]. This was largely done by addressing the offset voltage in the op amp via chopper stabilization or auto-zeroing [117], [121]–[123]. However, the chopper principle has also been applied to the

diode pair and current mirror of a bandgap reference, with the primary goal of eliminating output error due to random mismatch [119], [120]. A complex switching scheme was used to average out the offsets of the diode pair, pFET current mirrors, and the op amp. The switching scheme for the scaled current mirrors required extensive digital control [120], whereas the proposed voltage reference architecture offers a more simplified approach to the problem of mismatch. Since the main priority of the design is reducing radiation-induced drift, the resistive biasing scheme eliminates the need to cancel current mirror offset. The initial resistor mismatch will be static in the radiation response.

The addition of the choppers in the voltage reference of Fig. 51 introduces a new radiation vulnerability to the design. However, the effect of degradation in the switches can be made negligible with the proper design. Guidelines for designing radiation-tolerant chopper switches are presented in the next section.

Simulation results: 180-nm design

The fully integrated chopper-stabilized voltage reference of Fig. 51 was designed and taped out in the IBM CMRF7SF 180-nm bulk CMOS process, which is comparable to the CMHV7SF process. Figure 52 shows the architecture of the temperature-regulated voltage reference. The chopper-stabilized reference core is composed of the chopper OTA “amp1”, the matched DTMOST pair D1/D2 with chopper switches, the pFET current source P1, trim resistor R1, and poly resistors R and R/2. The clock subcircuit generates the non-overlapping clock signals 1 and 2 and their complements for chopper control. The thermal control circuit is composed of the op amp “amp2”, the *IPTAT* current mirror P2, trim resistor R2, and the heater nFET connected to the op amp output.

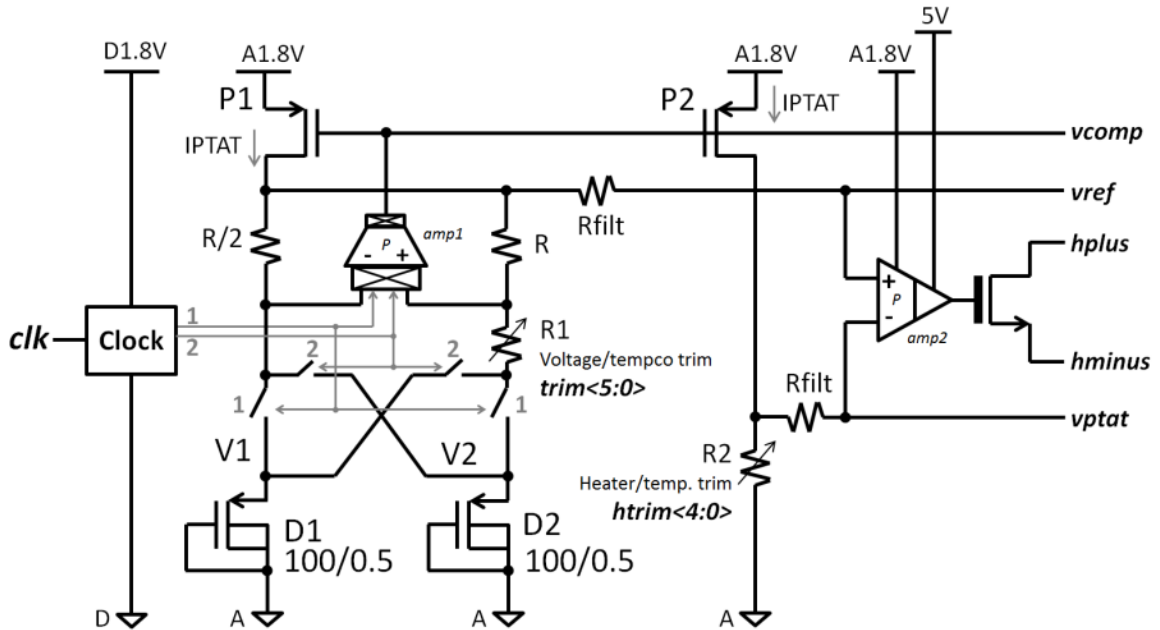


Fig. 52: RHBD temperature-regulated voltage reference designed in IBM 180-nm process. R = 2.74 kΩ, R1≈ 750 Ω, R2 ≈ 3.2 kΩ, Rfilt = 10 kΩ.

There are 1.8-V supplies (A1.8V for analog and D1.8V for digital) and a 5-V supply for the heating. The functionality of the reference core is as described in the previous section, generating a PTAT current *IPTAT* and a voltage *vref* with first-order tempco cancellation. The details of the trim resistor designs are covered in Section D of this chapter, but they consist of poly resistors and nFET switches. By adjusting R1, the current *IPTAT* is adjusted, changing the output voltage *vref* and the temperature at which the voltage exhibits zero tempco (the ZTC point). The typical value of *IPTAT* is 165 µA, biasing one DTMOST at 55 µA and the other at 110 µA. These bias points correspond closely to the smallest measured shifts in 100/0.5 DTMOSTs in Fig. 47.

The operation of the thermal control loop was detailed in Chapter III. However, the design of the mixed-voltage (1.8 V and 5 V) op amp "amp2" is important for the overall system's radiation tolerance, so it is detailed in Section D of this chapter.

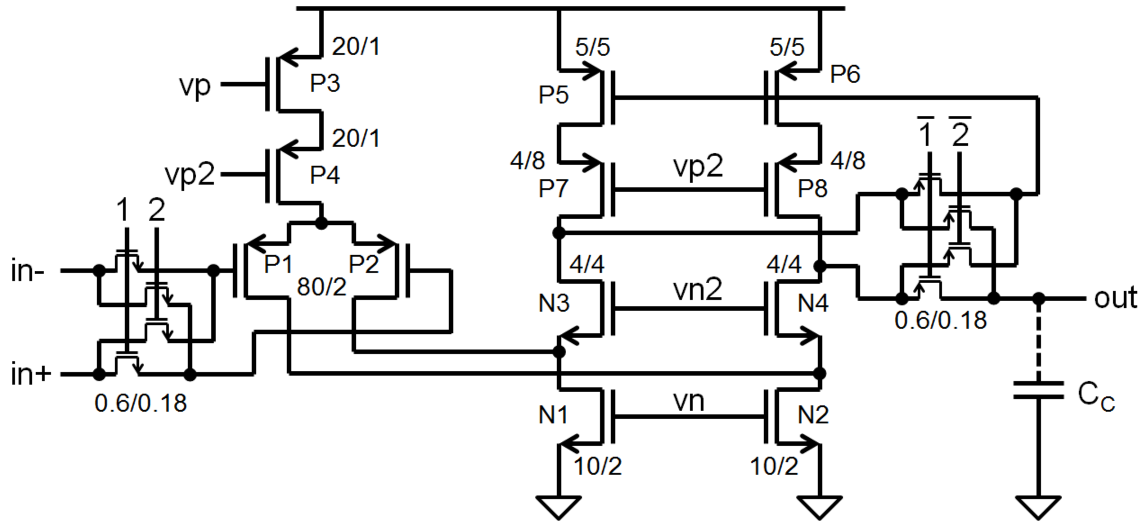


Fig. 53: Chopper OTA used in RHBD voltage reference design. Dimensions of each transistor indicated in micrometers.

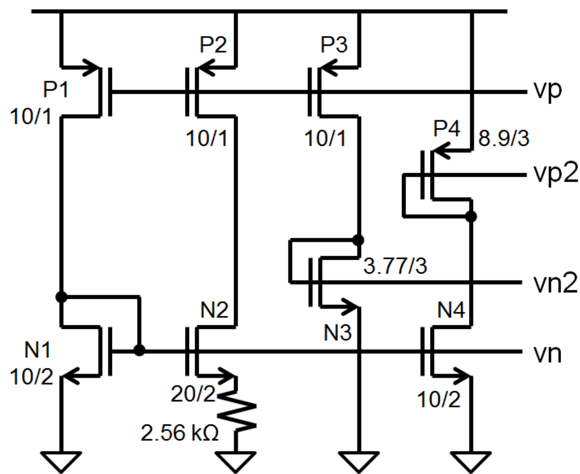


Fig. 54: Bias circuit for OTA in Fig. 53.

The p-input chopper OTA used in the reference design ("amp1") is shown schematically in Fig. 53. The circuit generating the bias voltages vp, vp2, vn2, and vn is shown in Fig. 54. The simple chopper OTA design is loosely based on the design presented in [118], in which the high-impedance output of the folded-cascode gain stage is combined with a large compensation capacitor to the form the low-pass filter required to filter the chopper ripple. The capacitor C_C in the schematic is an off-chip capacitor with capacitance greater than or equal to 10 nF. Since the common-mode range of the

OTA input stage is 0—0.8 V, nFETs can be used for the input chopper switches. Furthermore, the negligible input bias current of the OTA allows the use of minimum-size nFETs (0.6 μm/0.18 μm). Since the high-impedance output of the OTA is typically greater than 0.9 V, minimum-size pFETs can be used for the output chopper switches. The OTA functions like a fully differential design with the negative output used as a bias voltage for current sources P5 and P6.

The input chopper modulates the signal to the chopping frequency of 100 kHz, while the output signal demodulates the signal while modulating the op amp non-idealities to the chopping frequency. With this chopping scheme the noise and offset voltage of each transistor pair in the circuit are modulated. For example, with the choppers enabled the Monte Carlo three-sigma input-referred offset voltage of the op amp is 855 nV, compared to 3.63 mV without chopping. In Cadence Spectre the offset voltage in a matched pair can be modeled by placing a DC voltage source in series with the gate of one of the devices. The baseline effect of offset voltage in the OTA input pair (P1 and P2 in Fig. 53) is illustrated in Fig. 55. These plots show the reference output VREF and the bias current IPTAT when the offset voltage is -5, 0, and +5 mV with the choppers disabled. The reference voltage shifts by up to 70 mV due to a 5-mV offset shift, and the bias current shifts by up to 55 μA. The relatively high bias currents (55 μA and 110 μA) of the DTMOSTs result in fairly low small-signal resistances, which yield sizable shifts in bias current due to the offset drift. Because these current shifts are so large, the small-signal resistance of each DTMOST actually changes as well, resulting in the asymmetric voltage and current shifts shown in Fig. 55. The waveforms of VREF and IPTAT plotted in Fig. 56 show how chopping mitigates the impact of OTA offset voltage.

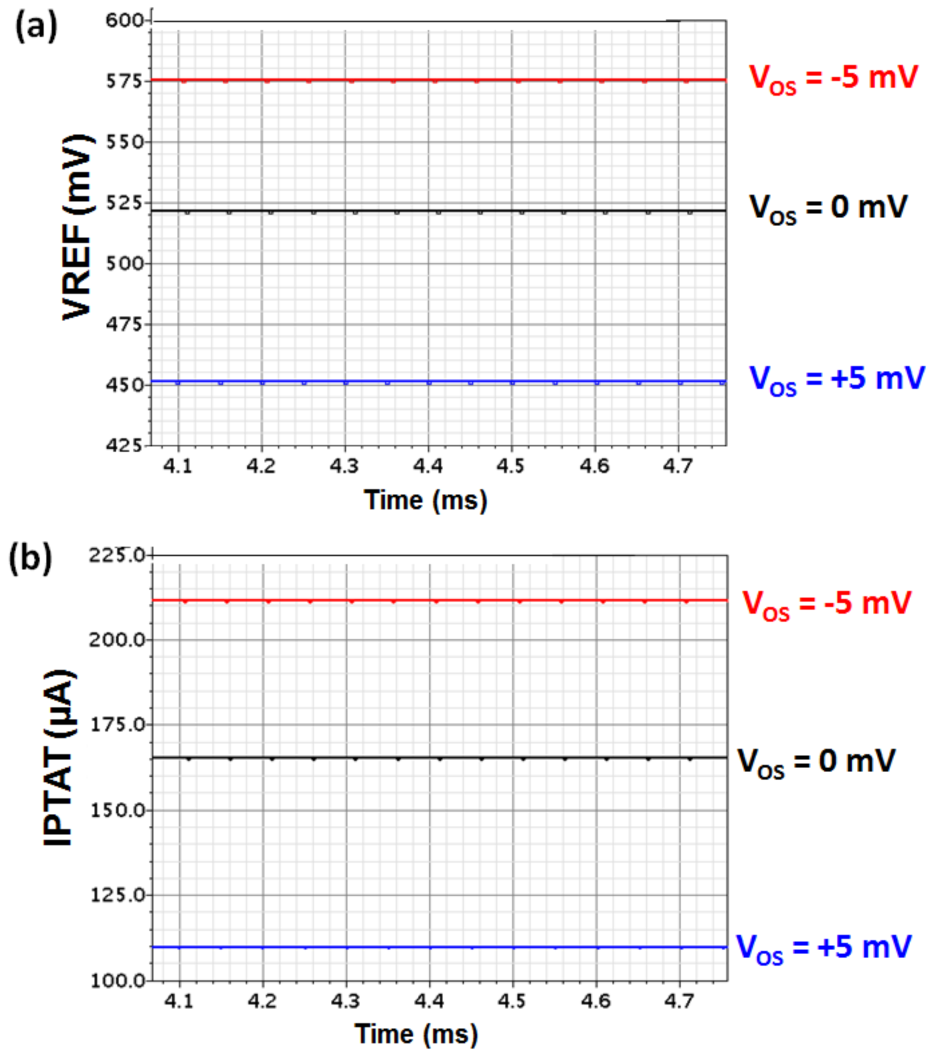


Fig. 55: Effect of offset voltage (V_{OS}) of OTA input pair on (a) VREF output and (b) IPTAT bias current in the voltage reference without chopping.

In Fig. 56(a) the 100-kHz chopper ripple in the reference voltage is evident; the value of C_C in these simulations was 1 nF, illustrating the need for larger filter capacitors to further flatten out the ripple. Nevertheless, if the periodic signals for V_{OS} = -5 mV and +5 mV are averaged, the DC component of the voltage can be computed. Doing so reveals that the voltage reference output shifts by less than 22 μV with chopping enabled. The current waveforms in Fig. 56(b) similarly show ripple, while the DC components show shifts smaller than 22 nA. Offset voltage was simulated in all the matched pairs of the

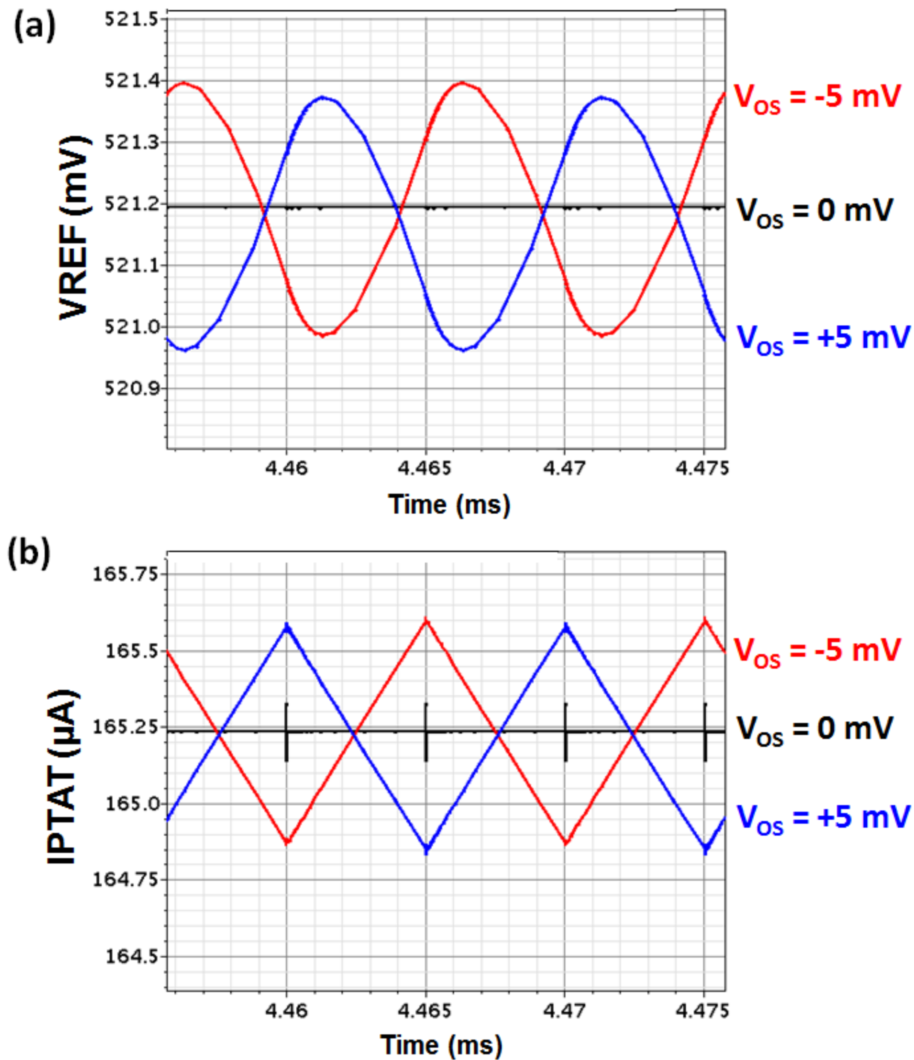


Fig. 56: Effect of offset voltage (V_{OS}) of OTA input pair on (a) VREF output and (b) IPTAT bias current in the voltage reference with chopping at 100 kHz.

OTA of Fig. 53, and the resulting impact on VREF and IPTAT is summarized in Table 8 both without (measured in mV and μA) and with (measured in μV and nA) chopping. The chopper stabilization in the OTA effectively mitigates the effect of offset voltage in all the matched pairs.

The next component to investigate is the matched DTMOST pair D1/D2. Radiation-induced shifts in the operating voltage of D1 and D2 were modeled by putting

Table 8: Effect of offset voltage in matched pairs in OTA of Fig. 53 on output (VREF) and bias current (IPTAT) of voltage reference in Fig. 52 both (a) without and (b) with chopping. Initial values are 521.195 mV for VREF and 165.236 μA for IPTAT.

(a) Without chopping.

		ΔVREF (mV)		ΔIPTAT (μA)	
Matched pair	**Description**	**-5mV**	**+5mV**	**-5mV**	**+5mV**
P1/P2	Input pair	54.1	-70	46.3	-55.5
N1/N2	N current source	-56.7	46	-45.4	39.2
N3/N4	N cascode	-0.97	0.97	-0.8	0.8
P7/P8	P cascode	0.01	-0.01	-0.009	0.009
P5/P6	P current source	2.4	-2.4	-2	2

(b) With chopping (note change in units).

		ΔVREF (μV)		ΔIPTAT (nA)	
Matched pair	**Description**	**-5mV**	**+5mV**	**-5mV**	**+5mV**
P1/P2	Input pair	2	-22	2	22
N1/N2	N current source	4	-17	-17	0
N3/N4	N cascode	-1	0	0	0
P7/P8	P cascode	0	0	0	-1
P5/P6	P current source	-26	-25	-22	-21

DC voltage sources in series with the DTMOSTs, as shown in Fig. 45. The values of these voltage sources were ΔV1 for D1 and ΔV2 for D2. For example, shifts of 0.3 mV in D1 and 0.2 mV in D2 were simulated, choosing shifts that match reasonably well with those measured at 300 krad at these bias points in Fig. 47. Using parameters R1 = 750 Ω, R2 = 2.74 kΩ, r_{s1} = 991 Ω, and r_{s2} = 622 Ω, the voltage reference shift according to (56) is approximately 1.18 mV without chopping, and with chopping the voltage shift according to (77) is 0.25 mV, which is simply the average of ΔV1 and ΔV2. The baseline and shifted VREF without chopping are plotted in Fig. 57(a). The reference voltage shift of 1.1 mV is very close to the predicted value. This illustrates how even a small difference in ΔV1 and ΔV2 of 0.1 mV is amplified, significantly impacting the output

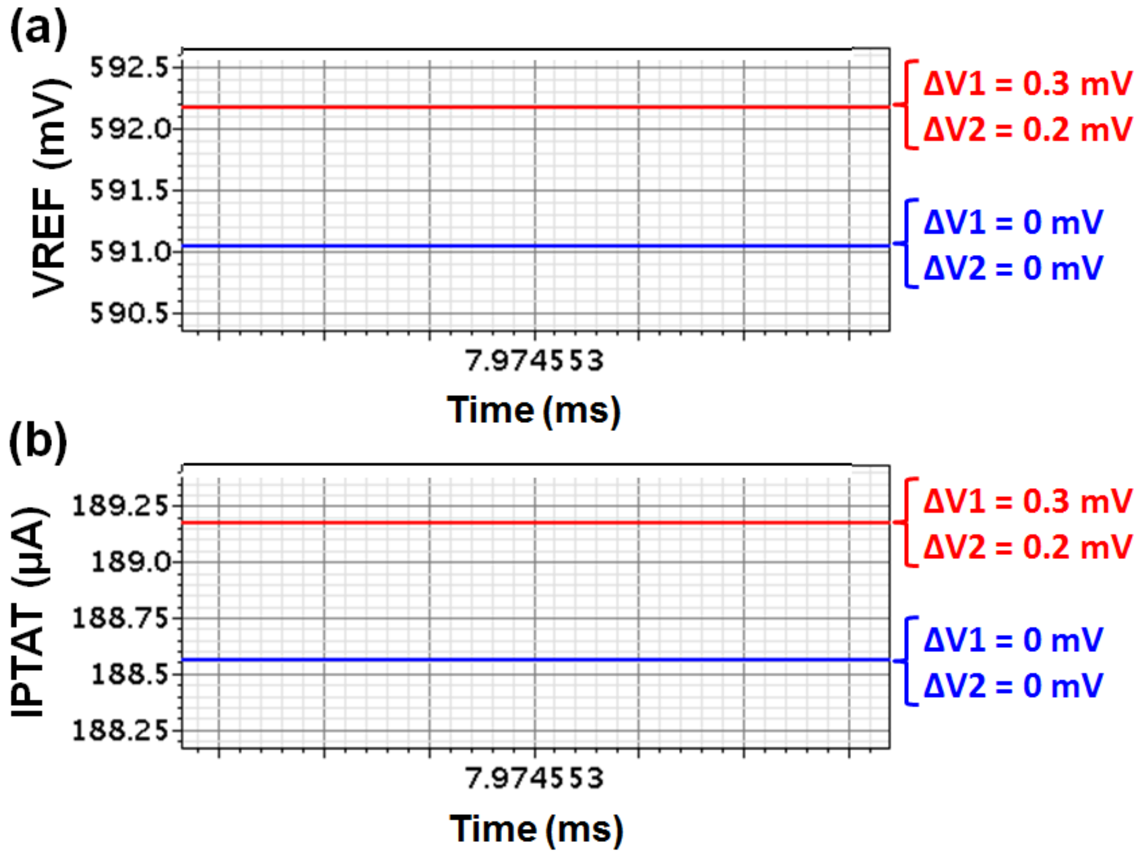


Fig. 57: Effect of shifts in DTMOSTs D1 and D2 (shown as ΔV1 and ΔV2, respectively) on voltage reference (a) output VREF and (b) bias current IPTAT *without chopping*. The blue lines show the baseline values and the red lines show the values when D1 shifts by 0.3 mV and D2 shifts by 0.2 mV.

voltage. Additionally, the shift in bias current IPTAT is plotted in Fig. 57(b), showing a shift of 610 nA.

The effect of the same DTMOST shifts ΔV1 and ΔV2 when chopping is enabled is plotted in Fig. 58. The baseline and shifted VREF are shown in Fig. 58(a), with the shifted value exhibiting 100-kHz chopper ripple. The DC component of VREF shifts by 0.25 mV, as predicted. The two IPTAT waveforms in Fig. 58(b) show the DC component of the bias current shifting by a few nA. In both cases, the radiation-induced shifts are dramatically reduced, eliminating the amplification of the 0.1-mV mismatch in DTMOST shifts.

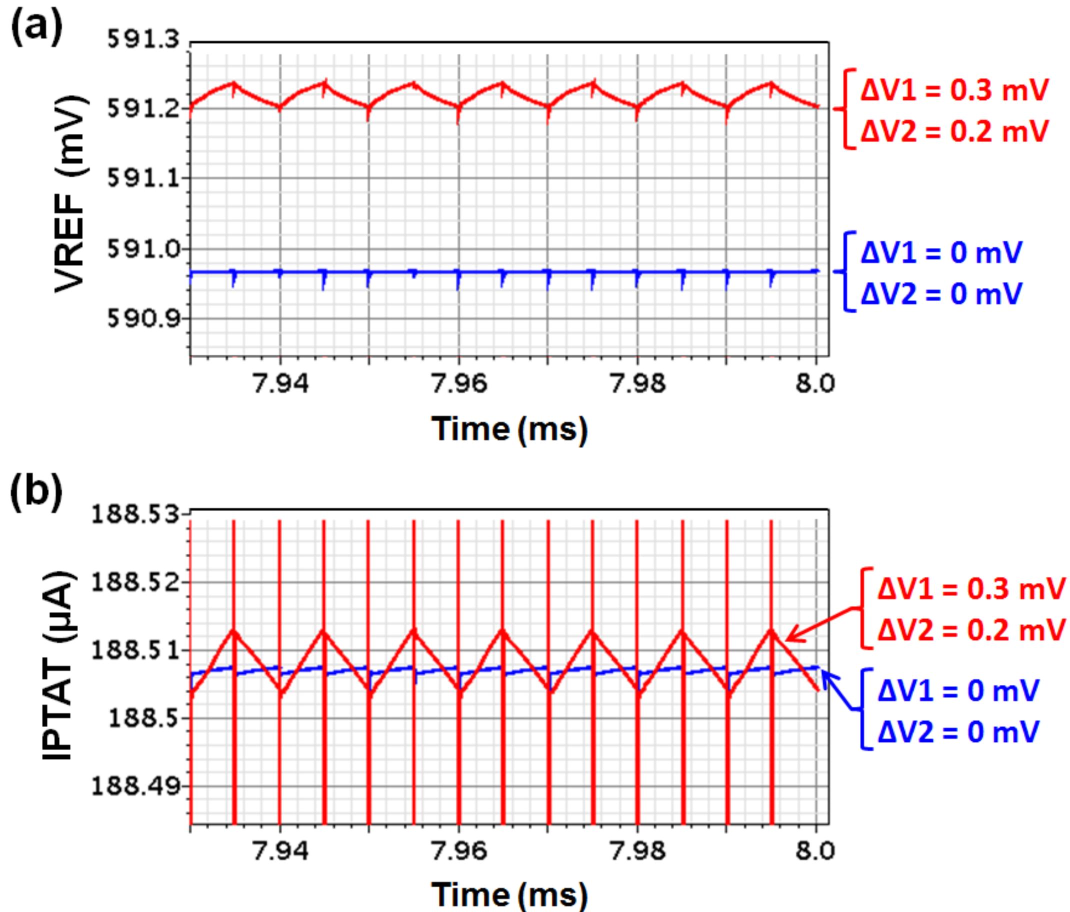


Fig. 58: Effect of shifts in DTMOSTs D1 and D2 (shown as ΔV1 and ΔV2, respectively) on voltage reference (a) output VREF and (b) bias current IPTAT *with chopping*. The blue lines show the baseline values and the red lines show the values when D1 shifts by 0.3 mV and D2 shifts by 0.2 mV.

To illustrate the fundamental difference in the radiation responses of the reference with and without chopping, a sensitivity plot for ΔV1 and ΔV2 is shown in Fig. 59. The shaded region inside each box represents the possible ΔV1 and ΔV2 combinations which cause voltage reference shifts less than or equal to 0.1% of the baseline value 520 mV. It is assumed that the maximum shift in D1 (ΔV1) is ±1 mV, and the shift in ΔV2 that generates a ±0.1% shift in VREF is calculated to generate the plot as ΔV2 vs. ΔV1. The blue box representing the design without chopping is very thin, indicating that shifts in D1 and D2 must be closely matched, since mismatched shifts are amplified by a factor of

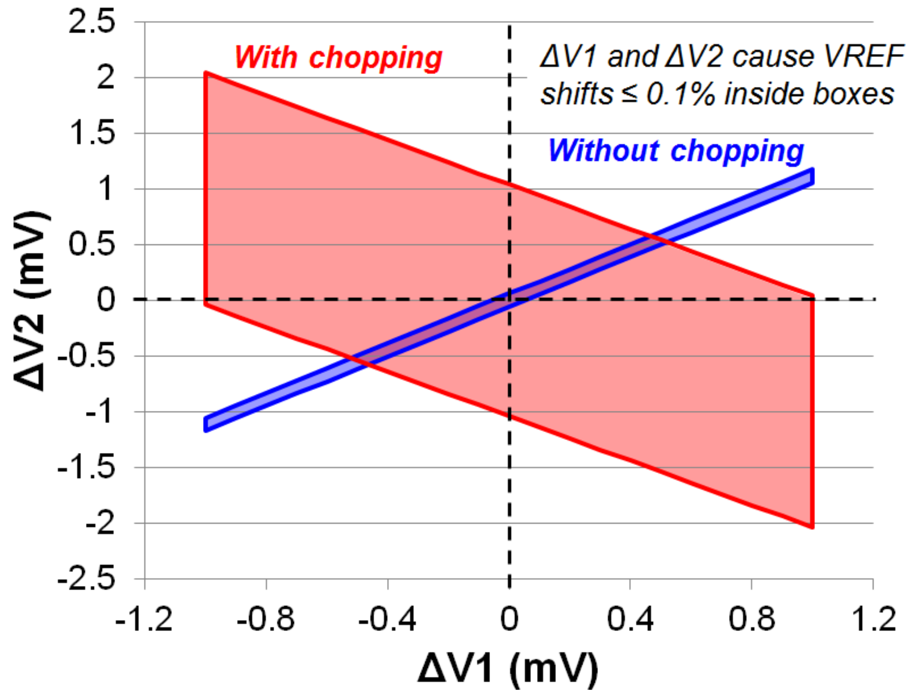


Fig. 59: Sensitivity plot of radiation-induced voltage shifts in DTMOSTs D1 (ΔV1) and D2 (ΔV2). Shaded region inside boxes indicate combinations of ΔV1 and ΔV2 that cause shifts in voltage reference less than ±0.1% of baseline value 520 mV. The maximum ΔV1 is assumed to be ±1 mV.

8.8. The red box representing the design with chopping is much wider, indicating the ability of the chopper to eliminate the amplification of mismatched voltage shifts. The chopped design is only limited by the average shift of D1 and D2. The area inside each box can be used to compare the relative sensitivity of each design to DTMOST voltage shifts. The area of the chopped reference is 17.3 times larger than that of the static reference, indicating a significantly higher resilience to TID effects in the DTMOSTs.

To demonstrate the robustness of the single pFET current source, threshold voltage shifts were modeled in P1 (Fig. 52) using a DC voltage source connected in series with the gate. The voltage reference output VREF is plotted as a function of P1 threshold voltage shift ΔV_{TP} in Fig. 60. A threshold shift of ±10 mV generates reference shifts less than ±12 μV, showing significant attenuation of the threshold shift. The resistive biasing topology eliminates the amplified current mirror mismatch in the radiation response. The

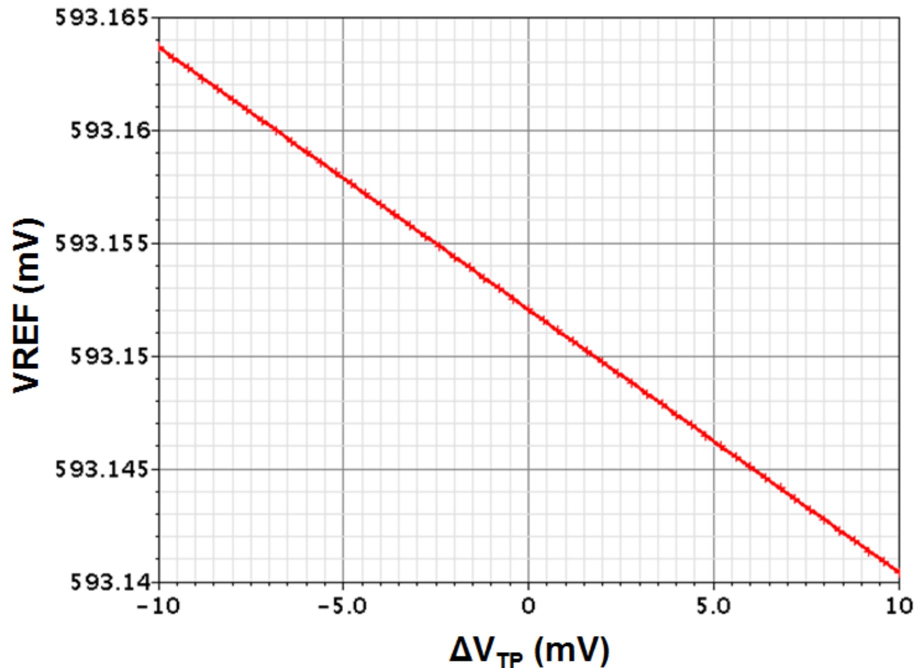


Fig. 60: Effect of threshold voltage shift in pFET current source P1 on voltage reference output.

current source P1 essentially acts as the common-source output stage of the OTA, so the negative feedback loop easily compensates for parametric shifts. The pFET measurements in Fig. 48 exhibited gate voltage shifts less than 2 mV, so these simulation results spanning a range of ±10 mV can be considered quite pessimistic for this technology.

The use of resistors to distribute current from a single current source is a novel radiation-hardened current mirroring scheme. The resistors can easily be sized to provide scaled or equal currents. Furthermore, the current mirror functionality is only dependent on the ratio of resistor values and not the absolute values. This flexibility makes the simple circuit an effective rad-hard alternative to classical MOSFET current mirrors. While mismatch between the resistors will impose an initial current mirror error, that error is not affected by total dose, due to the simple passive nature of the resistors. The simplicity of the rad-hard current mirror makes it applicable to a wide range of circuits.

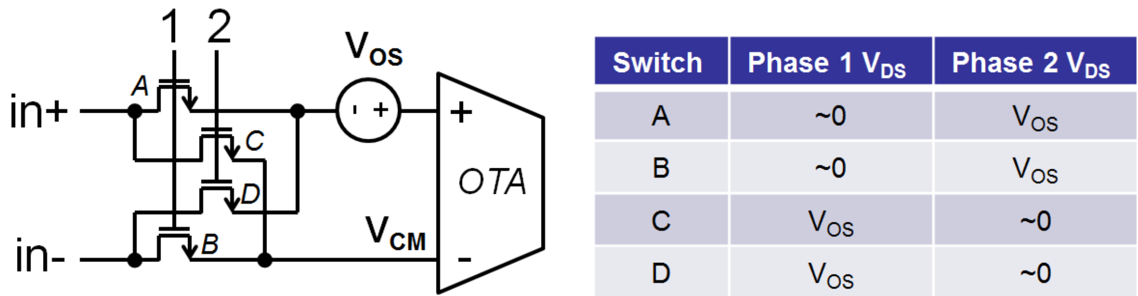
Essentially any circuit requiring current mirrors controlled by a single gate voltage can benefit from this resistive biasing scheme. In particular, designs sensitive to current mirror mismatch will benefit the most as the impact of radiation-induced mismatch is eliminated with this novel circuit. The degradation of the single current source has a "common-mode" effect on the currents being supplied by the resistive mirror, meaning all currents are affected equally. With the addition of negative feedback, the effects of total dose degradation in the current mirror are negligible, as demonstrated in the voltage reference simulations.

The remaining active components of the core reference whose radiation responses must be considered are the clock generation, the trim resistor R1, and the chopper switches. Since the chopper frequency is limited by the bandwidth of analog components, the digital circuitry generating and handling the clock signals operate well below their maximum speed—e.g., the chopper frequency for this design is 100 kHz, while the rise/fall times of minimum-size inverters are under 100 ps. Therefore, threshold shifts of a few mV and leakage currents will negligibly impact the performance of these digital circuits, which will in turn negligibly impact the voltage reference. The switches used in the trim resistor are vulnerable to TID, so design guidelines for trim resistors are given in Section D.

It is important to understand the radiation response of the chopper switches because chopper stabilization is fundamentally what makes the proposed reference radiation-hardened. The currents carried by the choppers inside the OTA are negligible because they only switch out high-impedance nodes. The primary parameter affected by threshold voltage shifts in a FET switch operated at low speed is the ON resistance. The

high-impedance nature of the OTA choppers makes the ON resistance relatively unimportant as no DC current is transmitted. Therefore, threshold shifts negligibly affect the OTA choppers; for example, threshold shifts in both OTA choppers up to ±100 mV were simulated with no change in the output voltage. This means the pFET switches on the OTA output are inherently tolerant to radiation, but the nFET switches on the input are still susceptible to radiation-induced leakage in the sidewalls.

The following analysis will demonstrate why leakage effects are also negligible in the OTA input chopper. The chopper and the OTA with input-referred offset V_{OS} are illustrated in Fig. 61. The voltage on the inverting input of the OTA is the common-mode voltage V_{CM}, and the feedback in the circuit will set the non-inverting voltage equal to V_{CM} as well. As a result, the voltages handled by the switches are limited to V_{CM} and (V_{CM} − V_{OS}). Therefore, when a chopper switch is OFF, the drain-source voltage is simply the offset voltage V_{OS}. When a chopper switch is ON there is no DC current



Switch	Phase 1 V_{DS}	Phase 2 V_{DS}
A	~0	V_{OS}
B	~0	V_{OS}
C	V_{OS}	~0
D	V_{OS}	~0

Fig. 61: Input chopper of OTA with table showing drain-source voltages of each switch during each phase.

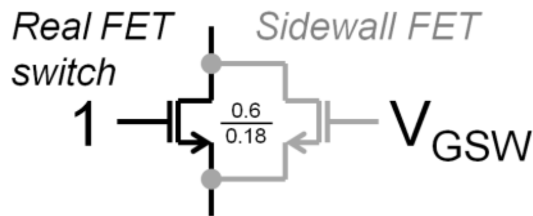


Fig. 62: Single chopper switch with sidewall leakage modeled using identical transistor with gate voltage representing trapped STI charge.

flowing through it, so the drain-source voltage is 0 V. These voltages are indicated in Fig.

61. The conclusion of this voltage analysis is that the maximum source-drain voltage of the switches is V_{OS}, which is typically much less than 10 mV.

Charge trapped in the STI region along the sidewalls of a switch can cause inversion in the p-type body region, creating a channel in parallel with the intentional device, as shown in Fig. 62. The sidewall trapped charge acts as a gate voltage V_{GSW}, increasing as the trapped charge increases. However, the current flowing in the parasitic sidewall channel still depends on the drain-source voltage of the real FET, since it is connected in a parallel. The highest drain-source voltage can be conservatively estimated as 10 mV, which does not result in significant leakage current. For example using the model in Fig. 62, an equivalent sidewall gate voltage V_{GSW} of 300 mV increases the device leakage current at V_{DS} = 10 mV from 2 pA to 3.9 nA—an increase of over three orders of magnitude. However, when this model is added to the voltage reference design, no shift results in the reference voltage. The bias voltages of the switches are simply too small for the parasitic sidewall transistor to make a significant impact. It is straightforward to employ an edgeless layout in the chopper switches to absolutely ensure TID tolerance—as was done on this design—but this analysis shows it is not totally necessary.

The chopper connected to DTMOSTs D1 and D2, however, must be properly designed for TID tolerance. Since the currents of D1 and D2 are scaled by a factor of two in this design, the maximum drain-source voltage across one of these chopper switches is the difference between V1 and V2—on the order of 50 mV. Using the same leakage model as before, a parasitic sidewall gate voltage V_{GSW} of 400 mV increases the switch leakage current at V_G = 0 V, V_S = 0.3 V, V_D = 0.35 V from 21 fA to 1 nA—a factor of

nearly 48,000. When simulated in the voltage reference, this sizable increase in leakage in the DTMOST chopper switches caused only a 1 μV shift in reference voltage. The relatively high bias currents 55 μA and 110 μA that run through the chopper switches cause the leakage current to have a negligible impact. As before an edgeless layout can be used to absolutely ensure leakage immunity, but it is not totally necessary.

The disadvantage of using high bias currents in the reference core is the requirement of low ON resistance in the chopper switches. Unlike the OTA chopper, the DTMOST chopper transmits sizable DC current, so the ON resistance is a critical parameter for the design. When an nFET operates as a switch, it operates in the ohmic region with the following current-voltage relationship:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TN}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right], \tag{78}$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate-source voltage, and V_{TN} is the threshold voltage. In the voltage reference the ON resistance of the chopper switches is critical because the drain-source voltage, which directly impacts the reference output, depends on the DC current flowing in the switch. The voltage drop across the switch can be computed from (78), yielding:

$$V_{DS} = (V_{GS} - V_{TN}) - \sqrt{(V_{GS} - V_{TN})^2 - \frac{2\, I_D}{\mu_n C_{ox}} \frac{L}{W}}. \tag{79}$$

The effect of threshold voltage shifts on the drain-source voltage can be expressed by differentiating V_{DS} with respect to the threshold voltage:

$$\frac{\partial V_{DS}}{\partial V_{TN}} = -1 + (V_{GS} - V_{TN}) \left[(V_{GS} - V_{TN})^2 - \frac{2\, I_D}{\mu_n C_{ox}} \frac{L}{W} \right]^{-1/2}. \tag{80}$$

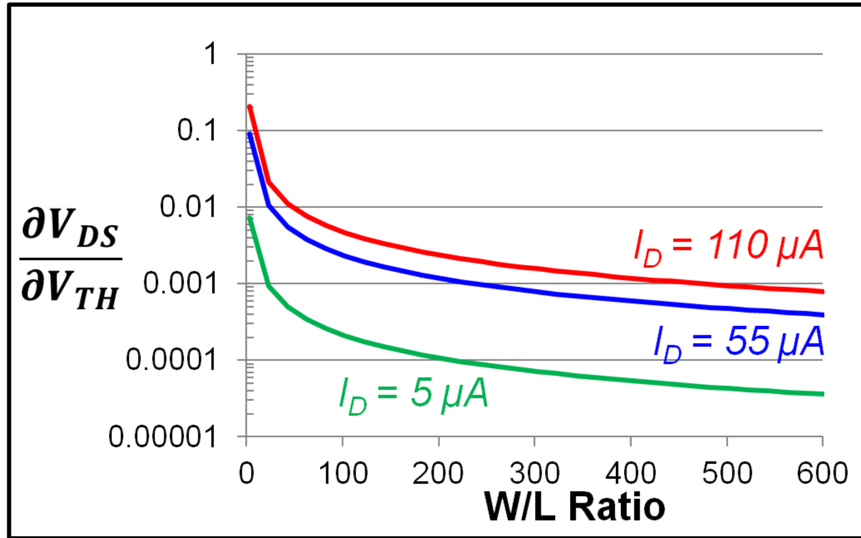


Fig. 63: Effect of threshold voltage on switch drain-source voltage as a function of the aspect ratio, using IBM 180-nm process parameters.

Since the bias current I_D is chosen for the voltage reference based on the DTMOSTs and V_{GS} is dependent on the supply voltage, the remaining design variable in (80) is the W/L ratio. The effect of threshold voltage on V_{DS} in (80) is plotted as a function of W/L ratio in Fig. 63, using currents of 5, 55, and 110 µA and the IBM 180-nm process parameters. This plot shows how increasing W/L decreases the effect of threshold voltage shifts on the drain-source voltage. It also illustrates how lowering the bias current can reduce this effect.

Therefore, the primary method for hardening the DMOST chopper switches in the voltage reference is increasing the W/L ratio such that the expected threshold shifts do not cause significant voltage reference shifts. In the presented reference design, 100-µm/0.18-µm (W/L = 556) nFETs were used for the chopper switches. Threshold voltage shifts were simulated in the DTMOST chopper, and the resulting voltage reference shift is plotted in Fig. 64. A rather pessimistic threshold shift of 10 mV in the switches generates a nearly 50-µV shift in VREF—just a 0.008% change. The slope of

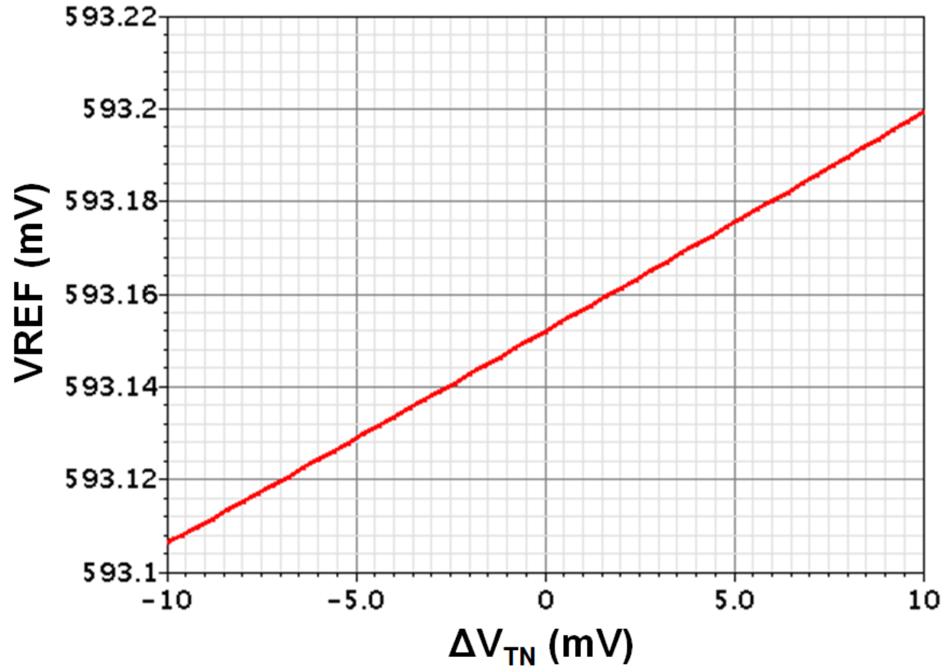


Fig. 64: Effect of threshold voltage shifts in the DTMOST chopper on the voltage reference output VREF.

the line in the plot is approximately 0.005 V/V; this value is steeper than predicted in Fig. 63 because of the systematic offset in V_{DS} shifts in the switches. As shown in Fig. 63 the ON switch carrying 110 μA exhibits a slightly larger V_{DS} shift than the ON switch carrying 55 μA, and that slight offset is amplified just like the op amp offset voltage in (51). Since this offset is systematic, the chopper does not modulate it. However, random mismatch in the chopper switches is modulated and cancelled by the chopper.

Typically the use of large switches is avoided due to charge injection, which is directly related to the gate area of the switch. However, charge injection effects are insignificant in the DTMOST chopper for several reasons. First, the fully-differential nature of the chopper promotes cancellation via common-mode rejection. Second, when one chopper switch is switched ON, there is another chopper switch on the same node that immediately switches OFF, injecting equal and opposite charge and thereby cancelling the effect. Third, the nodes being switched by the DTMOST chopper are low-

impedance nodes—with resistances less than 1 kΩ—so the injected charge is quickly dissipated by the high DC currents. This observation will hold true for all cases, since large switches are only required when the DC current levels are high, meaning the charge dissipation closely tracks the charge injection.

These simulation results have applied the measured subcircuit responses to the new RHBD design to demonstrate TID tolerance. While the chopper in the OTA is inherently radiation tolerant—due to the high impedance of the switching nodes—the chopper between DTMOSTs introduces radiation vulnerability. It was shown that the effect of threshold voltage shifts in the chopper can be mitigated by simply using large W/L ratios and/or reducing the bias currents. Since this RHBD design was recently taped out, there was not an opportunity to test the radiation response. However, in the next section experimental results are presented using previously fabricated hardware to demonstrate the proposed techniques.

Experimental setup

The radiation tolerance of the discussed chopping schemes was demonstrated using hardware. In addition to the previously discussed voltage reference chip (termed the VREF chip), a 180-nm CMRF7SF test chip (termed the AMP chip) containing several fully-differential (FD) op amp designs was used to demonstrate chopping in the op amp. Both chips were fabricated in similar IBM 180-nm bulk CMOS processes, so the radiation responses are comparable. Neither chip was designed with chopper stabilization, so external components were used to implement board-level chopper schemes. The FD op amps on the AMP chip were required because the op amps on the

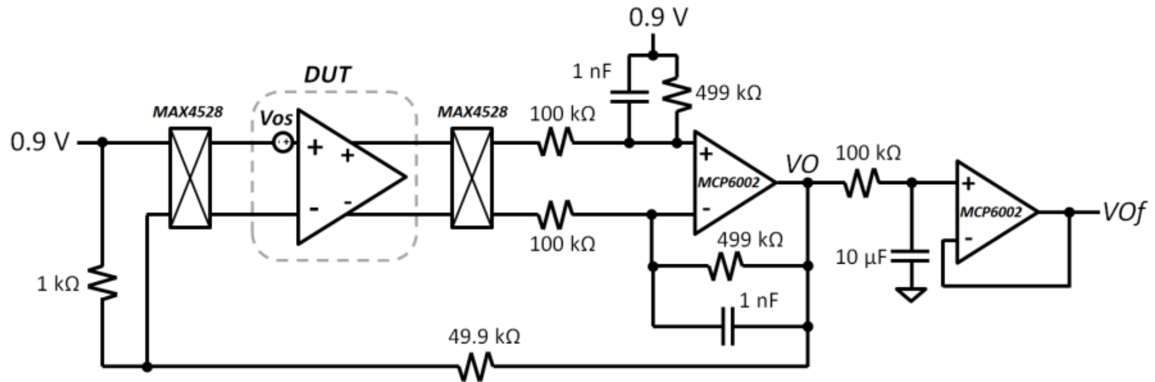


Fig. 65: Chopper-stabilized op amp test circuit implemented with 180-nm test chip (the DUT) and external components on breadboard.

VREF chip were single-ended without access to the internal nodes that would be required for chopping.

The chopper-stabilized op amp test circuit is shown in Fig. 65. The FD op amp labeled Device Under Test (DUT) is the complementary folded-cascode op amp on the AMP chip in Fig. 66. The op amp is essentially an FD version of the previously discussed design. The unity-gain output buffers are identical push-pull source followers. The matched pairs N1/N2, P1/P2, N5/N6, and P5/P6, all contribute significantly to the input-referred offset of the op amp, indicated as V_{OS} in Fig. 65. The AMP chip contains several op amp designs, but the two used in this experiment are the baseline (OA1) and sensitive-node active charge cancellation, or SNACC, (OA2) designs. The SNACC design has additional transistors—that are nominally OFF—in the bias circuit for single-event mitigation [113]. Because these additional transistors are only activated during a single event, the bias circuits of OA1 and OA2 are electrically comparable. More importantly the circuitry of Fig. 66 that results in offset voltage is identical in the two designs.

The AMP chip was packaged in a 40-pin dual-inline package (DIP), and the test circuit of Fig. 65 was built on a breadboard. A single-ended op amp was constructed with the fully-differential DUT as the input stage and a single-ended difference amplifier as

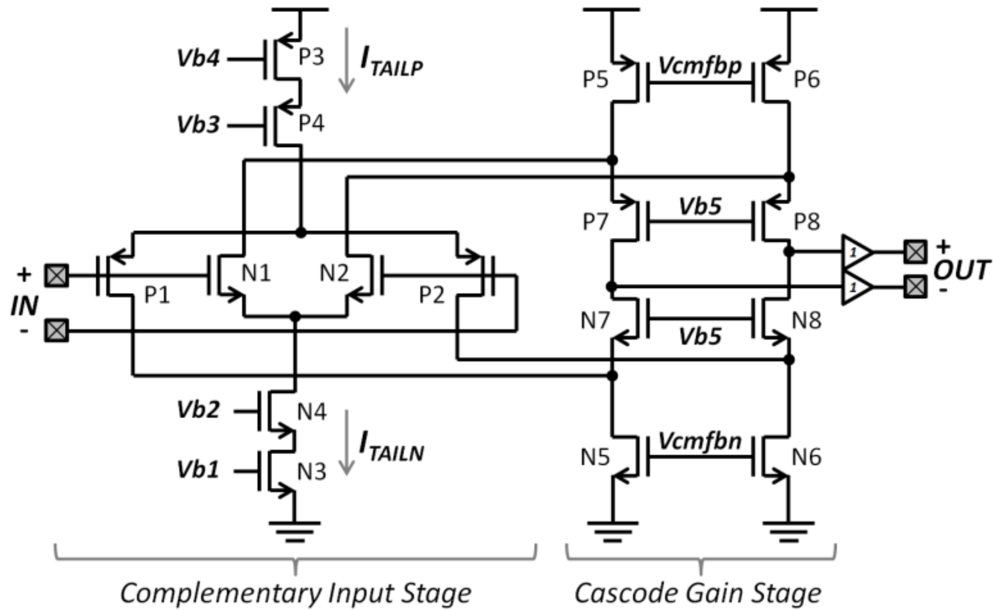


Fig. 66: Fully-differential complementary folded-cascode op amp on AMP test chip (the DUT in Fig. 65). The bias circuit that generates *Vb1, Vb2, Vb3,* and *Vb4,* the common-mode feedback circuits that generate *Vcmfbp* and *Vcmfbn*, and the compensation capacitors on the cascode stage outputs are not shown.

the output stage. The difference amplifier was implemented using the MCP6002, a general purpose dual op amp that can be powered from the same 1.8-V supply as the DUT. The gain of the difference amplifier was 4.99, as determined by the 100-kΩ and 499-kΩ resistors. The single-ended op amp formed by the DUT and the difference amplifier was placed in a non-inverting amplifier configuration with a gain of 50.9 V/V. This gain was chosen both to amplify the input-referred offset of the DUT and to ensure the stability of the DUT, which was not unity-gain stable. In fact, the instability of the op amps on the AMP chip was primary reason the op amp and voltage reference were tested separately, since the reference requires a gain around 10 V/V.

Finally the output of the 50.9-V/V non-inverting amplifier was low-pass filtered with a 100-kΩ resistor and 10-μF capacitor—cutoff frequency of 0.16 Hz— and buffered with a MCP6002 voltage follower to prevent loading by measurement equipment. Since the non-inverting amplifier input was shorted to the common-mode voltage of 0.9 V, the

output voltage is:

$$VOf = 0.9\,V + 50.9\,V_{OS}, \tag{81}$$

where V_{OS} is the input-referred offset of the DUT op amp. The offset voltage of the MCP6002 in the difference amplifier does not contribute significantly, because it is divided by the gain of the first stage of the op amp, the DUT. The gain of the DUT is greater than 1000 V/V, so the MCP6002 contributes less than 4.5 μV to the overall amplifier offset—the maximum offset on the datasheet is 4.5 mV. The MCP6002 voltage follower also contains some offset, but since the DUT is the only irradiated component, the voltage follower offset only causes a static initial error. Therefore, the offset voltages of the MCP6002 components can be neglected.

The MAX4528 discrete chopper chip was used to perform the chopper modulation and demodulation on the inputs and outputs of the DUT, with a chopping frequency of 1 kHz. For direct comparison, both a chopped and a static op amp were implemented using the OA1 and OA2 op amps on a single DUT. The chopped op amp was built as shown in Fig. 65, and the static op amp was simply built without the MAX4528 chips. In the static design, the signals were connected as they would be in phase 1 in Fig. 65. With both of these circuits constructed, a single DUT could be irradiated in the ARACOR X-ray source to compare the radiation response of the chopped and static op amps.

The chopper-stabilized voltage reference test circuit is shown in Fig. 67. The components in gray—the DTMOSTs, resistors, and pFET current source—were the components on the 180-nm DUT, while the remaining components were discrete parts. The DUT was packaged in a 40-pin DIP, and the test circuit was built on a breadboard.

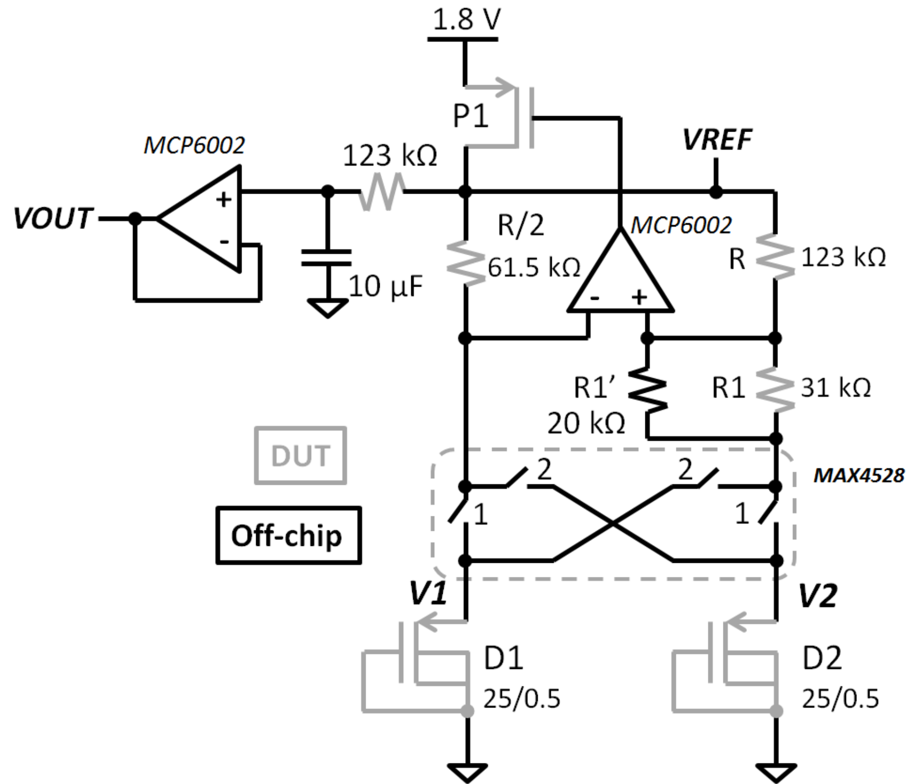


Fig. 67: Chopper-stabilized voltage reference test circuit. Components in gray were on the 180-nm DUT, and all other components were discrete parts.

The reference topology of Fig. 67 is nearly the same as the topology in Fig. 51. One difference is the use of the MCP6002 op amp instead of a chopper-stabilized op amp. Another modification is the addition of the external resistor *R1'* in parallel with *R1* to adjust the bias currents of D1 and D2. Since the chopper-stabilized op amp in the previous section would be unstable in this circuit, the MCP6002 was used as the op amp in the circuit. The on-chip 123-kΩ resistor was used with an external capacitor to low-pass filter the *VREF* voltage. This filtered signal is buffered by an MCP6002 voltage follower to generate the output *VOUT*. Only the DUT components were irradiated, so the MCP6002 offsets only contribute to initial error and are neglected from the analysis. The reference voltage in phase 1 is, therefore, computed as:

$$VREF = V1 + \frac{R}{R1||R1'}(V1 - V2), \quad (82)$$

where R = 123 kΩ, $R1$ = 31 kΩ, and $R1'$ = 20 kΩ, yielding a gain factor of 10.1 V/V on the $(V1 - V2)$ term. The currents flowing through R and $R/2$ were approximately 1.8 µA and 3.6 µA, respectively.

As before, the MAX4528 discrete chopper was used to chop the DUT reference devices D1 and D2. A chopper frequency of 1 kHz was used. There were only enough components on a single DUT to implement a single voltage reference, so separate irradiations of two DUTs were used to compare a chopped and a static voltage reference. The chopped reference was implemented as shown in Fig. 67, and the static reference was the same circuit with the clock signal held static at 5 V (the supply for the MAX4528). In this way, the effect of chopper stabilization on the radiation response of the CMOS voltage reference was demonstrated.

Experimental results

Two irradiations were performed on two AMP chips using op amps OA1 and OA2 to implement static and chopped op amps. In the irradiation of AMP chip 1 the chopped op amp was built using OA1, and the static op amp was built using OA2. In the irradiation of AMP chip 2, the chopped op amp was built using OA2, and the static op amp was built using OA1. Both times, the DUT was exposed to a dose of 300 krad[SiO_2] with the outputs measured when the dose reached 50, 100, and 300 krad. Measurements were performed using the Agilent 34401A 6½-digit multimeter. The output voltages were sampled over a period of approximately 20 seconds, tracking the average, minimum, and maximum readings. After the dose of 300 krad was reached and

measurements were taken, the DUT remained powered for several minutes of post-rad room-temperature annealing and additional measurements were made. By calculating the difference between the average output voltage and the input voltage and then dividing by 50.9, the input-referred offset voltage of the DUT was obtained, according to (81).

The results of the two irradiations are plotted in Fig. 68 and Fig. 69. Both plots track the input-referred offset of the chopped and static op amps as a function of total dose and then post-rad anneal time. In the irradiation of AMP chip 1 in Fig. 68, the static op amp offset started at a small value of -180 μV but shifted by 9.82 mV. On the other hand, the chopped op amp offset started at 10 μV and shifted by only 50 μV. It is interesting to note that with the chopper disabled the initial offset of OA1 was 2.27 mV, demonstrating the effectiveness of the chopper scheme in reducing offset voltage. The chopper stabilization of the offset voltage can be quantified in comparing the chopped and static op amps, demonstrating a reduction in offset drift of 99.5%. The results of the

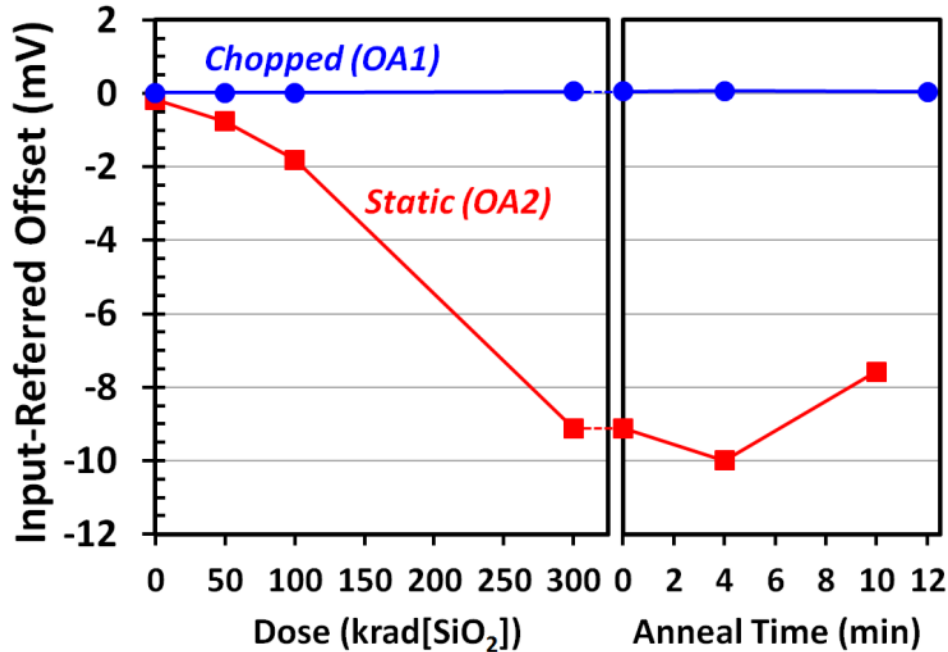


Fig. 68: Input-referred offset voltages of chopped and static op amps measured on AMP chip 1.

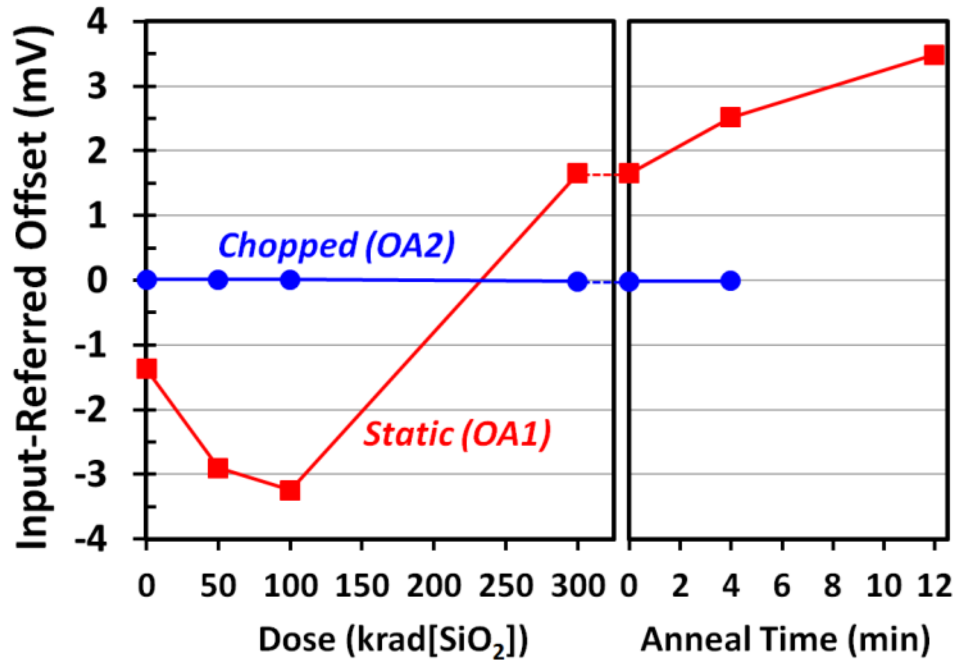


Fig. 69: Input-referred offset voltages of chopped and static op amps measured on AMP chip 1.

irradiation of AMP chip 2 are plotted in Fig. 69. On this chip the static op amp was OA1, with an initial offset of -1.37 mV. The chopped op amp was OA2, with an initial offset of 10 μV (2.68 mV with the chopper disabled). The static op amp offset showed shifts of up to 6.73 mV, while the chopped op amp offset showed shifts less than 30 μV, a 99.6% reduction. On both parts and both op amp designs, chopper stabilization dramatically improved the radiation response.

It is informative to contextualize the results in the voltage reference of Fig. 45. It was shown in (51) that a shift in amplifier offset voltage is amplified in the voltage reference output. Using the calculated gain of -5.5 V/V for example, the -9.82-mV offset shift of OA2 in a static scheme would cause a 54-mV shift in the reference voltage, a nearly 12% shift from the nominal 460-mV output. Since ½ LSB of a 2-bit ADC corresponds to 12.5%, the op amp offset degradation limits the reference precision to 2 bits. The -30-μV offset shift of OA2 in a chopped scheme would cause a 165-μV shift in

reference voltage, a 0.036% shift. The offset degradation of the chopper-stabilized op amp supports up to 10 bits of precision (½ LSB = 0.05%).

Two irradiations were also performed on two VREF chips using the same components. The only difference in the two irradiations was the chopper clock, which ran at 1 kHz for VREF chip 1 (chopped) and was at 5 VDC for VREF chip 2 (static). The measurement and irradiation procedures were identical to those used in the previous section for the op amps.

The results of the two irradiations are plotted in Fig. 70 as the shift in reference voltage. The initial voltage was 528.8 mV for the static reference and 527.7 mV for the chopped reference. The static reference exhibited a maximum voltage shift of 5.0 mV (or 0.95%), while the chopped reference exhibited a maximum voltage shift of 1.3 mV (or 0.25%). By simply chopping the reference devices, the radiation-induced degradation

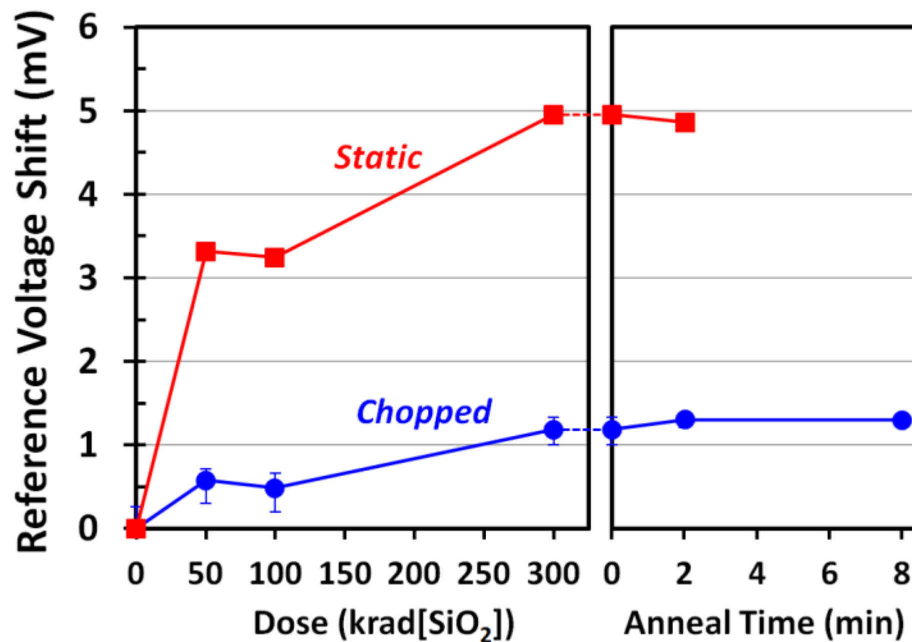


Fig. 70: Measured shifts in reference voltage for the chopped reference (VREF chip 1) and the static reference (VREF chip 2). The pre-rad voltage was 527.7 mV for the chopped reference and 528.8 mV for the static reference. Error bars indicate the minimum and maximum readings over a measurement period of 20 s.

was reduced by 74%, and the supported precision was increased from 5 bits to 7 bits.

As discussed previously, degradation in the VREF current source P1 is compensated within the op amp feedback loop. Furthermore, the discrete op amp in the circuit was not irradiated, so it contributed nothing to the measured reference voltage degradations. Therefore, the voltage shifts plotted in Fig. 70 are due solely to shifts in the reference devices D1 and D2. Radiation-induced shifts in the static reference follow (56) with the mismatch between D1 and D2 amplified, while shifts in the chopped reference follow (77) with the shifts in D1 and D2 averaged in the output.

In both the op amp and voltage reference experiments, the absolute values of the voltage shifts are largely specific to the process in which the test chips were fabricated. However the relative improvement in radiation response through the use of chopper stabilization demonstrates the effectiveness of the presented techniques in the design of radiation-hardened voltage references.

Radiation-hardened voltage reference using PTAT subtraction

PTAT subtraction topology

The previously presented RHBD voltage reference was a hardened version of a basic first-order design. In this section a novel PTAT subtraction reference topology is proposed. The fundamental concept behind the topology is illustrated in Fig. 71. If there are two proportional-to-absolute-temperature (PTAT) currents IPTATa and IPTATb that have the same positive tempco but different absolute values, then they can be subtracted to generate a current with first-order tempcos cancelled. These currents can be expressed analytically as:

$$IPTATa = I_a + \alpha\, T + \beta_a\, T^2 \qquad (83)$$

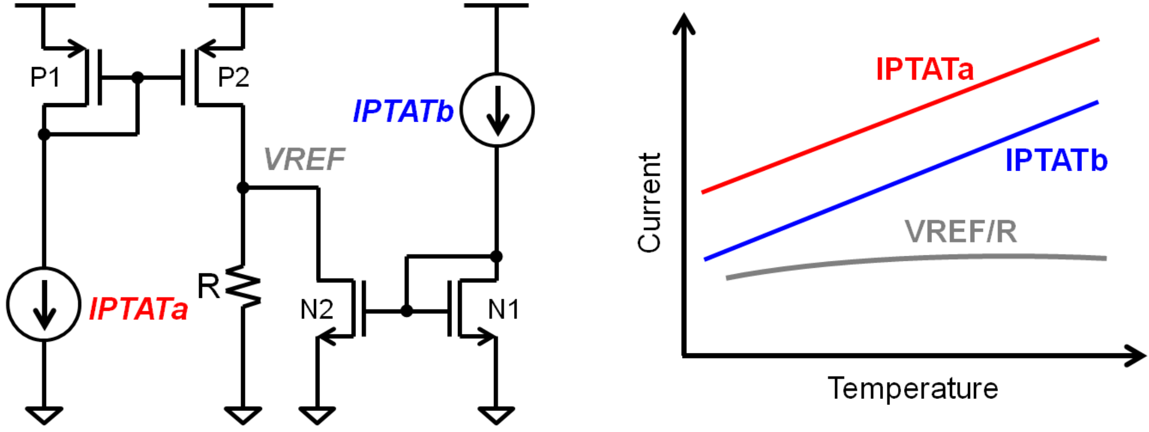


Fig. 71: Concept of PTAT subtraction voltage reference topology, schematic on left and temperature response on right.

and

$$IPTATb = I_b + \alpha\, T + \beta_b\, T^2, \tag{84}$$

where I_a and I_b are the currents at 0°C, α is the first-order tempco, and β_a and β_b are the second-order tempcos.

In the schematic IPTATa is mirrored to source current to the resistive VREF node, and IPTATb is mirrored to sink current from the same node. Using the definitions in (83) and (84), the resulting current flow through the resistor R can then be expressed as:

$$\frac{VREF}{R} = IPTATa - IPTATb = I_a - I_b + (\beta_a - \beta_b)T^2. \tag{85}$$

The first-order α terms are cancelled out, leaving second-order and higher (not shown) temperature dependence in the resulting voltage and current. This analysis shows that this topology does indeed provide first-order tempco cancellation similar to the previously discussed CMOS reference.

In the previous voltage reference, the PTAT bias current for the circuit was generated by subtracting the voltages of two DTMOSTs at different current densities. It was also shown that chopper stabilization effectively eliminated the contribution of this

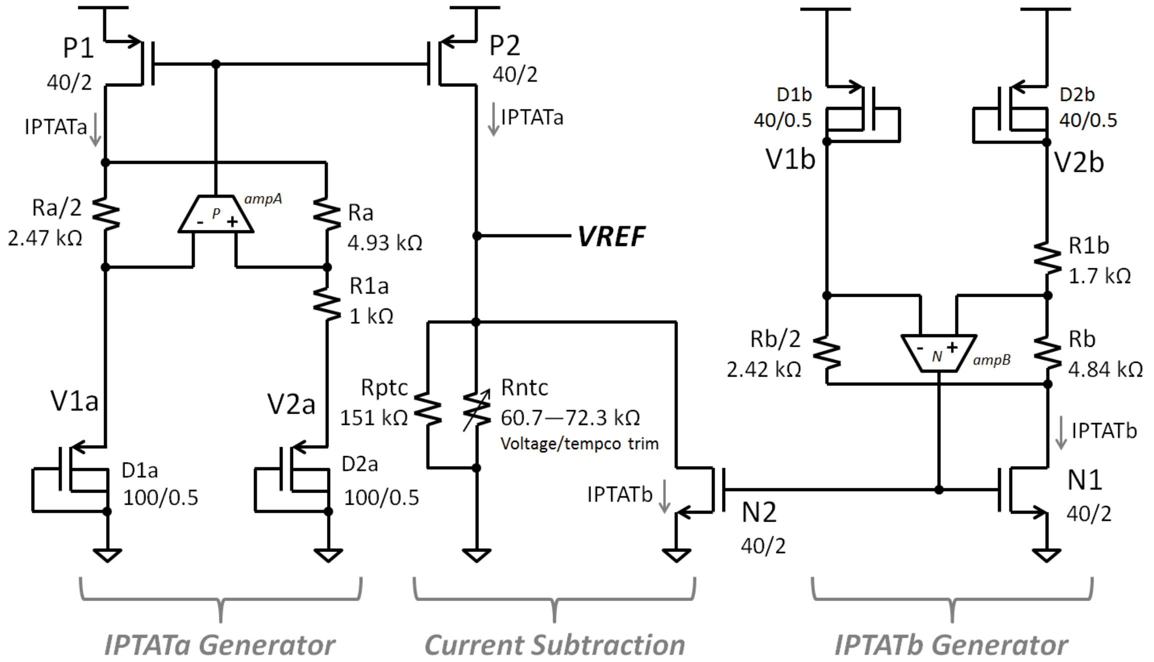


Fig. 72: Implementation of PTAT subtraction voltage reference in IBM 180-nm process.

difference term to the reference radiation response. The main goal of the PTAT subtraction topology is the generation of a reference voltage that is composed of only difference terms, so that chopper stabilization can be used to cancel out all radiation-induced voltage shifts.

The PTAT subtraction reference design implemented in the IBM CMRF7SF 180-nm process is shown schematically in Fig. 72. The circuit consists of three subcircuits: the IPTATa generator, the IPTATb generator, and the current subtraction circuit. The IPTATa generator is the same reference topology used in the previous section. The main difference is that the resistor R1a that sets the bias current is not trimmable. IPTATa can be analytically expressed as:

$$IPTATa = 3\frac{V1a - V2a}{R1a}, \tag{86}$$

and the typical current level at 75°C is 122 µA. While the IPTATa generator uses DTMOST voltages referenced to ground, the IPTATb generator uses DTMOST voltages

referenced to V_{DD}. This is a convenient topology because the current can easily be mirrored by an nFET to the VREF node for subtraction. In order to obtain a similar current tempco but a lower current level from IPTATa, the DTMOSTs in the IPTATb generator are sized smaller and biased at a lower current. The IPTATb current is:

$$IPTATb = 3\frac{(V_{DD}-V2b)-(V_{DD}-V1b)}{R1b} = 3\frac{V1b-V2b}{R1b}, \tag{87}$$

and the typical current level at 75°C is 92 μA. Even though the voltages used to generate IPTATb depend directly on V_{DD}, the differential nature of the circuit cancels out the V_{DD} dependence. Since the common-mode input voltage to the OTA in the IPTATb generator is on the order of 1.5 V, it was necessary to use a different OTA with an n-type input stage. The design is essentially a complement to the p-type design previously described.

Finally, the current subtraction circuit is where the tempco of the output voltage is trimmed. By getting the tempcos of the two PTAT currents close to each other, the tempco of the resistor can be trimmed to adjust the VREF tempco. The subtracted current flows through a parallel combination of a positive-tempco resistor—Rptc with tempco of +210 ppm/°C—and a negative-tempco resistor—Rntc with a tempco of -1360 ppm/°C. Rntc is a trim resistor that can be adjusted, and by doing so the tempco of the parallel combination is adjusted. If Rntc increases, so does the magnitude of its negative tempco, and the tempco of Rntc || Rptc becomes more negative. Using this scheme the voltage VREF could be trimmed to have first-order tempco cancellation across all process corners. The reference voltage can be expressed as:

$$VREF = 3(Rntc \mid\mid Rptc)\left(\frac{V1a-V2a}{R1a} - \frac{V1b-V2b}{R1b}\right), \tag{88}$$

The typical VREF output is 1.276 V—the voltage dropped across a 42.5-kΩ resistor when the subtracted current is 30 μA.

The circuit of Fig. 72 was simulated to demonstrate the temperature response. The temperature response of the two PTAT currents is shown in Fig. 73(a), and the reference voltage is shown in Fig. 73(b). Tempco of zero is evident in the reference voltage at 52°C. At this temperature the tempcos of IPTATa and IPTATb are 230 nA/°C and 206 nA/°C, respectively. When subtracted the resulting current tempco is 24 nA/°C, which is cancelled with the negative-tempco resistance Rntc || Rptc. Over a temperature range of 34—100°C the output voltage varies by less than 638 μV, or 0.05%. The readily available PTAT control signals make it very straightforward to integrate this reference core in to a temperature-regulated system. By heating the reference at 34°C, 10-bit precision—half LSB of 0.05%—is achievable with a relatively low amount of heat.

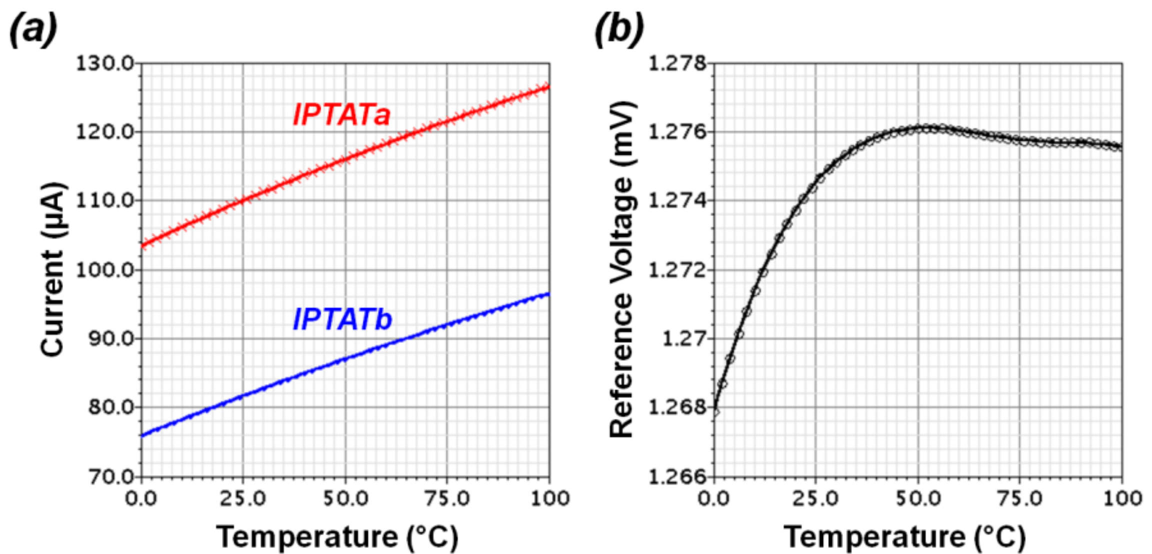


Fig. 73: Temperature responses of (a) PTAT currents and (b) reference voltage VREF.

Radiation hardening using chopper stabilization

The expression for the PTAT subtraction reference voltage in (88) is composed entirely of difference terms. It was previously shown that the radiation response of a difference term can be cancelled out using chopper stabilization. Therefore, chopper schemes in the two IPTAT generators harden the subcircuits to TID degradation. As before, choppers will need to be placed in the OTAs as well as the DTMOSTs to cancel radiation-induced offsets. With the offsets cancelled, radiation-induced voltage shifts affect the circuit as common-mode shifts, which are easily rejected by the differential nature of the topology. The P1/P2 and N1/N2 current mirrors (Fig. 72), however, can be quite sensitive to radiation-induced mismatch. Since these current mirrors are necessary for this topology, there is not a resistive alternative for hardening. Instead the current-mirror mismatch can be treated as a differential offset voltage and chopper stabilization can be used to cancel the offset.

The chopper-stabilized reference is shown schematically in Fig. 74, with the current mirror offsets V_{OP} for P1/P2 and V_{ON} for N1/N2 in red. The nodes VCOMPa,

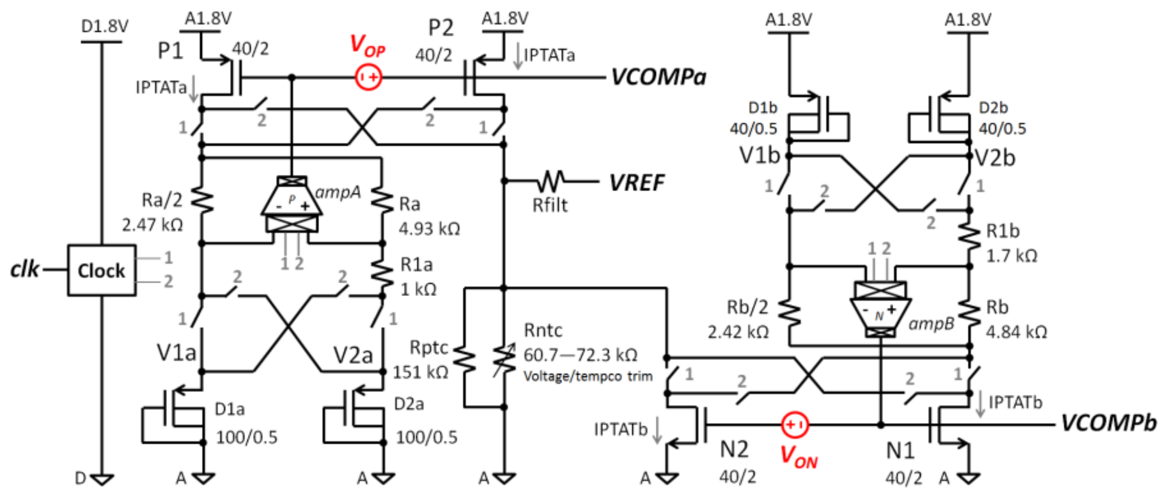


Fig. 74: RHBD PTAT subtraction voltage reference using chopper stabilization.

VCOMPb, and VREF require external capacitors on the order of 10 nF for compensation and filtering of chopper ripple. The radiation response of the IPTATa generator is considered first. Defining the D1a and D2a voltage shifts as ΔV_{D1a} and ΔV_{D2a}, and defining the shift in input-referred offset of the OTA ampA as ΔV_{OSa}, the shift in the IPTATa current sourced to the VREF node during phase 1 can be expressed as:

$$\Delta IPTATa_{phase1} = 3\frac{\Delta V_{D1a} - \Delta V_{D2a}}{R1a} - \left(\frac{3}{R1a} + \frac{2}{Ra}\right)\Delta V_{OSa} - g_{mp}V_{OP}, \qquad (89)$$

where g_{mp} is the transconductance of P1 and P2. The first term in (89) shows the effect of mismatch between D1a and D2a, the second term shows the effect of the OTA offset voltage, and the third term shows the effect of current mirror mismatch. During phase 2, all the chopper switches flip and the polarities of the offsets are reversed:

$$\Delta IPTATa_{phase2} = -3\frac{\Delta V_{D1a} - \Delta V_{D2a}}{R1a} + \left(\frac{3}{R1a} + \frac{2}{Ra}\right)\Delta V_{OSa} + g_{mp}V_{OP}. \qquad (90)$$

Defining the D1b and D2b voltage shifts as ΔV_{D1b} and ΔV_{D2b}, and defining the shift in input-referred offset of the OTA ampB as ΔV_{OSb}, the shifts in the IPTATb current sunk from the VREF node during phase 1 and phase 2 can be expressed as:

$$\Delta IPTATb_{phase1} = 3\frac{\Delta V_{D1b} - \Delta V_{D2b}}{R1b} + \left(\frac{3}{R1b} + \frac{2}{Rb}\right)\Delta V_{OSb} + g_{mn}V_{ON} \qquad (91)$$

and

$$\Delta IPTATb_{phase2} = -3\frac{\Delta V_{D1b} - \Delta V_{D2b}}{R1b} - \left(\frac{3}{R1b} + \frac{2}{Rb}\right)\Delta V_{OSb} - g_{mn}V_{ON}, \qquad (92)$$

where g_{mn} is the transconductance of N1 and N2. As with the IPTATa generator, the polarity of each offset term is reversed in each phase of operation.

When the chopped PTAT currents are filtered, the two phases are averaged together, so the shift in reference voltage can be expressed in terms of the average PTAT current shifts:

$$\Delta VREF = \frac{1}{2}(Rntc \,||\, Rptc)(\Delta IPTATa_{phase1} + \Delta IPTATa_{phase2}$$

$$-\Delta IPTATb_{phase1} - \Delta IPTATb_{phase2}). \quad (93)$$

For both IPTATa and IPTATb the phase 1 and phase 2 current shifts are equal in magnitude but opposite in the sign, so the final reference shift can be computed as:

$$\Delta VREF \approx 0. \quad (94)$$

By generating a voltage reference using only difference terms, chopper stabilization can theoretically cancel out all TID degradation. Of course, the residual offset from the chopping due to parasitics and non-idealities can still cause voltage reference shifts, but these shifts are very small, particularly when compared to the shifts without chopper stabilization.

While the implementation of the DTMOST and OTA choppers in the IPTATa generator were already discussed in a previous section, it is important to discuss the other choppers in this voltage reference. Since the P1/P2 current mirror chopper transmits currents in excess of 100 µA and the voltages being switched were on the order of 1.2 V, pFET switches with 200/0.18 aspect ratios were used. The high W/L is necessary to ensure negligible drain-source voltage shifts due to changes in threshold voltage. The IPTATb generator uses the opposite type of switches as the IPTATa generator: pFET chopper for OTA input, nFET chopper for OTA output, pFET chopper for DTMOSTs, and nFET chopper for N1/N2 current mirror. All the OTA chopper switches are sized at 0.6 µm/0.18 µm, all current-carrying nFET chopper switches are sized at 100 µm/0.18 µm, and all current-carrying pFET chopper switches are sized at 200 µm/0.18 µm.

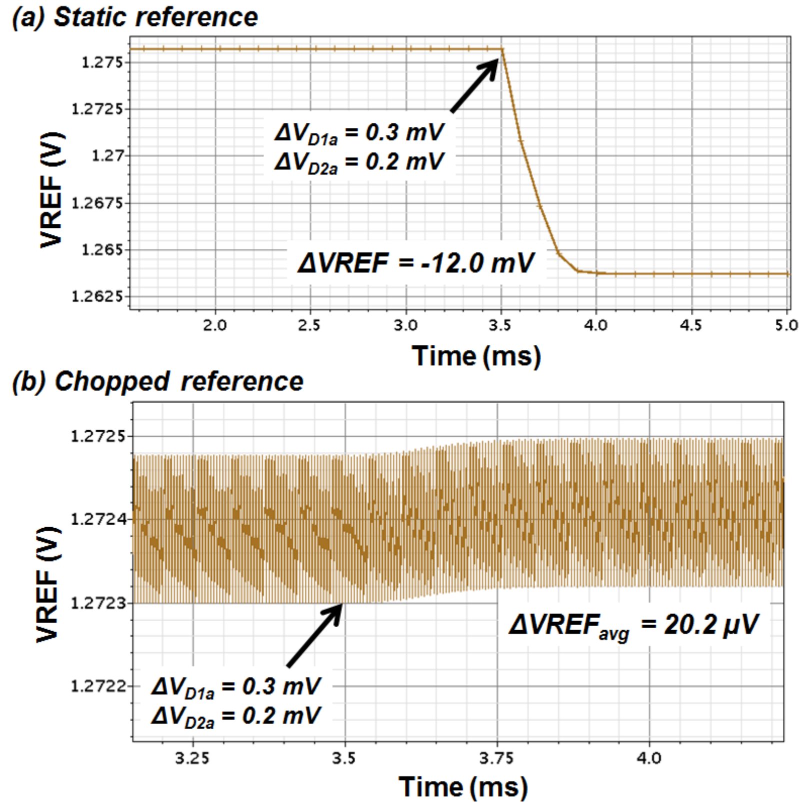


Fig. 75: Transient response of voltage reference (a) without chopping and (b) with chopping to voltage shifts of 0.3 mV and 0.2 mV in D1a and D2a, respectively. The DTMOST voltage shifts occur at 3.5 ms.

Simulation results: 180-nm design

The chopper-stabilized reference of Fig. 74 was simulated in the IBM 180-nm CMRF7SF process. To characterize the response of the circuit, voltage shifts were simulated in the subcircuits with the choppers disabled (static) and enabled (chopped). The waveforms in Fig. 75 show the circuit response to shifts in the DTMOSTs D1a and D2a. The chopped waveform in Fig. 75(b) shows the 100-kHz chopper ripple of 180 µVp-p, which can be further reduced with larger filter capacitors (1 nF used in these simulations). At 3.5 ms in both waveforms, the voltage of D1a shifts by 0.3 mV, and the voltage of D2a shifts by 0.2 mV. The small 0.1-mV offset causes a -12.0-mV shift (0.94%) in the reference, while the chopped reference only shifts by 20.2 µV (0.0016%). A similar simulation of DTMOST voltage shifts in the IPTATb generator was performed,

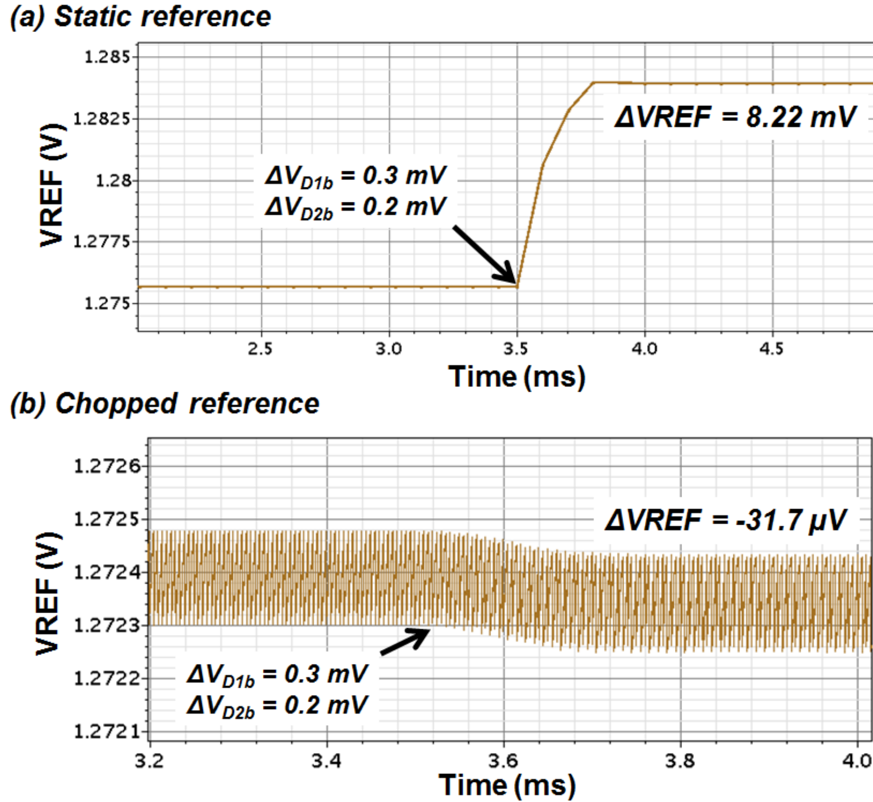


Fig. 76: Transient response of voltage reference (a) without chopping and (b) with chopping to voltage shifts of 0.3 mV and 0.2 mV in D1b and D2b, respectively. The DTMOST voltage shifts occur at 3.5 ms.

with the results plotted in Fig. 76. Again, the small offset between D1b and D2b causes a sizable 8.22-mV (0.64%) shift in the static reference, while the chopped reference exhibits a shift of only -31.7 µV (0.0025%). In the previously presented reference, the offset between DTMOSTs was cancelled, while the absolute shifts of the DTMOSTs were averaged, resulting in a 0.25 mV reference shift. The PTAT subtraction topology eliminates that direct dependence on DTMOST shifts through common-mode rejection.

The OTA offset voltage cancellation was seen in the previous voltage reference, so the other novel element in this design is the current mirror chopping. Current mirrors are not—strictly speaking—differential circuits, so the application of chopper stabilization is somewhat unusual. However, as demonstrated by the dual-phase analysis and the simulation results in Fig. 77 current mirror mismatch can be mitigated with

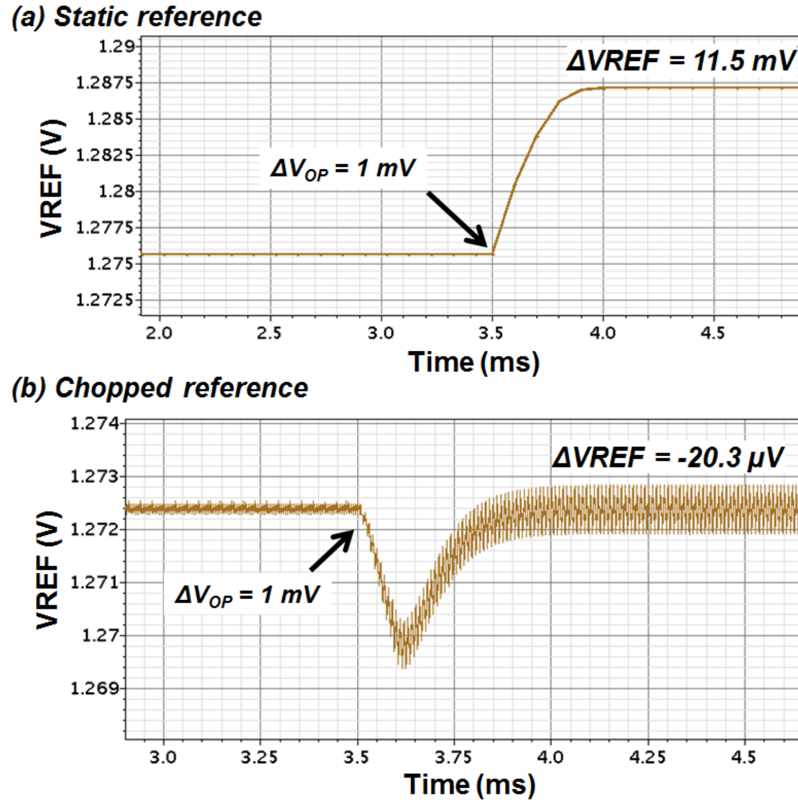


Fig. 77: Transient response of voltage reference (a) without chopping and (b) with chopping to a shift in pFET current mirror offset voltage V_{OP}. The voltage shifts occur at 3.5 ms.

chopper stabilization. The waveforms in Fig. 77 show the static and chopped reference outputs when the offset voltage between P1 and P2 increases by 1 mV. The static reference changes by 11.5 mV (0.90%), while the chopped reference only changes by -20.3 µV (0.0016%). Because the offset shift was modeled using a voltage step with a rise time of 100 µs, a transient does appear on the reference output before damping out to a small DC shift, but this is simply a result of the simulation setup. It is also interesting to note that the magnitude of the chopper ripple increases significantly to nearly 1 mVp-p. This highlights the importance of adequate filtering, as smaller than necessary capacitors were used in these simulations to decrease run time.

The effect of each of the offset voltages in the PTAT subtraction reference on the output is summarized in Table 9; gain factors from each offset to the output voltage were

Table 9: Effect of each offset voltage in the PTAT subtraction reference on the output voltage expressed as the magnitude of the gain from the offset to the output.

Offset Source	Gain at output without chopping (V/V)	Gain at output with chopping (V/V)	Reduction (%)
D1a/D2b	120	0.202	99.8
D1b/D2b	82.2	0.317	99.6
OTA ampA	73.3	0.102	99.9
OTA ampB	77.5	0.0237	99.97
P1/P2 mirror	11.5	0.0203	99.8
N1/N2 mirror	23.0	0.0103	99.96

computed from the simulations with and without chopping. Each number is essentially the absolute value of the partial derivative of the reference voltage with respect to the indicated offset voltage. The gain without chopping indicates the baseline sensitivity of the circuit, while the gain with chopping indicates the residual offset that still results. All the offset components have a significant gain factor at the reference output, but by using chopper stabilization these offset effects are attenuated rather than amplified. The percent improvement for all components is greater than 99.6%. These results demonstrate the tolerance of the design to voltage shifts in the subcircuits. The reference generates a voltage using difference amplifiers (the PTAT current generators), and the choppers cancel out any radiation-induced mismatch. In particular, the choppers on the DTMOSTs ensure that voltage shifts only affect the output as common-mode shifts, which are rejected by the differential nature of the circuit. Furthermore, the results demonstrate the efficacy of chopper stabilization applied to simple current mirrors.

RHBD considerations for analog circuits

In this section some general considerations for designing TID-tolerant analog

circuits are discussed. The designs in the previous two sections employed the techniques that will be presented, which include RHBD approaches for layout, trimming, and mixed-voltage interface design.

RHBD layouts

The most common approach to radiation hardening is through individual transistor layout. Edgeless transistor layout eliminates the radiation-induced sidewall channel leakage in nFETs [17], [34]–[44], [124]. Furthermore, the trapped charge in the field oxide bordering the channel can contribute slightly to threshold voltage shifts [125]. In this section several RHBD layouts are briefly discussed, including a novel edgeless dog bone layout.

Figure 78 shows four different RHBD layouts. The enclosed layout in Fig. 78(a) is the type of layout used on the previously discussed 180-nm (IBM CMHV7SF process) test chip; the 's' indicates the source regions, and the 'd' indicates the drain region. The

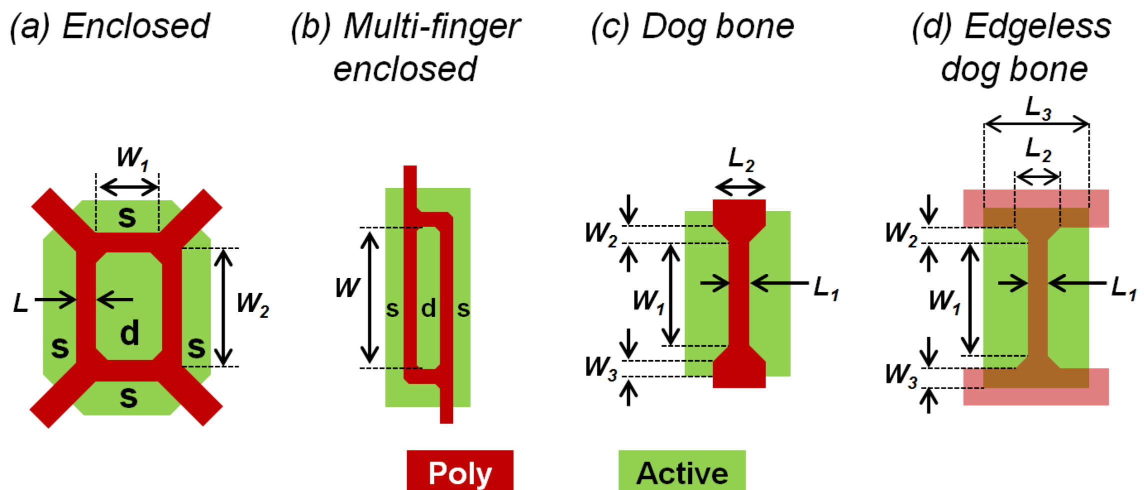


Fig. 78: RHBD transistor layouts: (a) enclosed layout used on CMHV7SF test chip, (b) multi-finger enclosed layout used in RHBD voltage reference designs, (c) dog bone layout, and (d) edgeless dog bone layout used in RHBD voltage reference designs.

layout rules of the technology only permitted 45° angles in poly over active and 90° in poly extending over active. The main purpose of the four poly extensions is limiting the current flow as much as possible to the four intended channels. The layout has two axes of symmetry with current flow in four directions and the intended W/L ratio is:

$$\left(\frac{W}{L}\right)_{eff} = 2\frac{W_1+W_2}{L}, \tag{95}$$

where W_1, W_2, and L are the dimensions indicated in Fig. 78(a). The DTMOSTs and diode-connected nFETs on the CMHV7SF test chip used both standard and enclosed layouts. Current-voltage measurements on an enclosed DTMOST with intended W/L of 50 (25/0.5) revealed an effective W/L of approximately 56.5, using the standard layout DTMOST as a reference. The 13% W/L error is most likely due to current flow in the corners of the device. The results indicate the difficulty in confidently designing the W/L ratio of an enclosed transistor, an issue well-documented in the literature [126], [127]. Although the device has two axes of geometric symmetry, the electrical operation is exceptionally asymmetric due to the drain being surrounded by four source regions [124].

For these reasons the enclosed layout in Fig. 78(a) is not suitable for analog design. It would be best suited to mitigating leakage effects in switches, but there is a significant area overhead in implementing this layout—e.g., nearly 2.2× larger area required for 25/0.5 DTMOST. Therefore, the layout in Fig. 78(b) was used in the final RHBD voltage reference designs for DC switches. The layout is achieved by starting with a standard two-finger layout and adding poly to connect the two fingers over the active. The active area must then be stretched vertically. The spacing between the two vertical poly strips is the same as in a standard two-finger device, so the (minimal) area overhead is only in the vertical dimension. The enclosed nature of the layout makes it immune to

radiation induced leakage, but it still exhibits electrical asymmetry similar to the original enclosed layout. This would cause the charge injection to be different on the source and drain nodes, which could result in transient issues in dynamic switching applications. Thus, the use of this layout is limited to DC switches, such as those used in trimmed resistors. Since one of the main requirements for a DC switch is that the ON resistance is below a specific value, the proposed layout convenient ensures that:

$$\left(\frac{W}{L}\right)_{eff} > 2\frac{W}{L}, \tag{96}$$

where W is the indicated dimension in Fig. 78(b) and L is the length of the two vertical poly gates. Additionally, multiple transistors with this geometry can be overlapped together with source regions merged to implement multi-finger enclosed transistors with very little area overhead.

The dog bone layout of Fig. 78(c) presents the classic approach to avoiding the source-drain asymmetry of enclosed layouts. By increasing the poly length at the transistor edge, the effect of the radiation-induced channel can be somewhat mitigated [19]. The main drawback of this geometry is the effect the longer section of the gate—L_2 in Fig. 78(c)—has on the effective aspect ratio of the transistor. The solution to this problem is the "edgeless" dog bone layout of Fig. 78(d). By simply extending the poly horizontally, the edge of the transistor is essentially eliminated. Furthermore, the four right triangles of poly—with height W_2 and width $(L_2 - L_1)/2$—can be drawn with minimum allowable dimensions (80 nm in IBM 180-nm processes) so that they minimally impact the designed W/L of the transistor. The transistor can be considered as having two channels: the rectangular channel and the combined 45° channels. Approximating the channel length of the 45° channels as the mid-point channel length, or

$(L_1 + L_2)/2 = L_1 + 80$ nm, the effective W/L can be approximated as:

$$\left(\frac{W}{L}\right)_{eff} = \frac{W_1}{L_1} + 2\frac{W_2}{(L_1+L_2)/2} = \frac{W_1}{L_1} + 2\frac{80\,nm}{L_1+80\,nm}, \quad (97)$$

using the dimensions labeled in Fig. 78(d). The first term is the rectangular channel, and the second term is the combined 45° channels. The small dimensions of the 45° channels result in a W/L ratio dominated by the rectangular channel. The effective length of the channel created by STI charge trapping is $2W_3 + L_3$, which can be extended with minimal impact on the functionality of the intentional device. Finally, when large W/L ratios are required—as in the current-carrying choppers—multiple edgeless dog bone transistors may be overlapped such that source/drain regions and gate regions merge, resulting in a truly edgeless multi-finger transistor. This is the layout geometry used in all the current-carrying chopper switches of the RHBD voltage references. Single-finger edgeless dog bone layouts were used for all nFETs in the OTAs and the DTMOSTs.

Digital trimming schemes

For accurate tempco cancellation in a voltage reference, it is typically necessary for some kind of trimming scheme to be implemented. The purpose of trimming is to account for process variation by adjusting one or several components. In the presented RHBD references, trimmed resistors were used to adjust the circuit to combat process variation. Laser trimming is a common but expensive way to trim resistor values, while digital trimming is much cheaper and can be done easily with resistors and FET switches. However, in an RHBD circuit it is important to properly design the trimmed resistor to withstand radiation degradation. In this section series and parallel trimming schemes are presented and their radiation responses are discussed in the context of a precision voltage

reference.

The schematic of a series trimming scheme is shown in Fig. 79(a). The TOP and BOT nodes are the two terminals of the programmable resistor, and t0—t4 are the digital inputs controlling the nFET switches. The resistors are poly resistors, and the binary-weighted resistors are made from series and parallel combinations of the unit cell resistor with resistance 4×Rlsb. When a trim bit is HIGH, the associated switch is turned ON, shorting out the binary-weighted resistor that is connected in parallel. Thus, the ideal resistance between TOP and BOT can be expressed as:

$$R_{series} = Rmin + (31 - trim)\ Rlsb, \tag{98}$$

where Rmin is the minimum resistance 2.1 kΩ, Rlsb is the least-significant-bit (LSB) resistance 44 Ω, and trim is the digital trim code in decimal 0—31. The trim functionality of the circuit is demonstrated in Fig. 79(b), showing a linear trend between resistance and

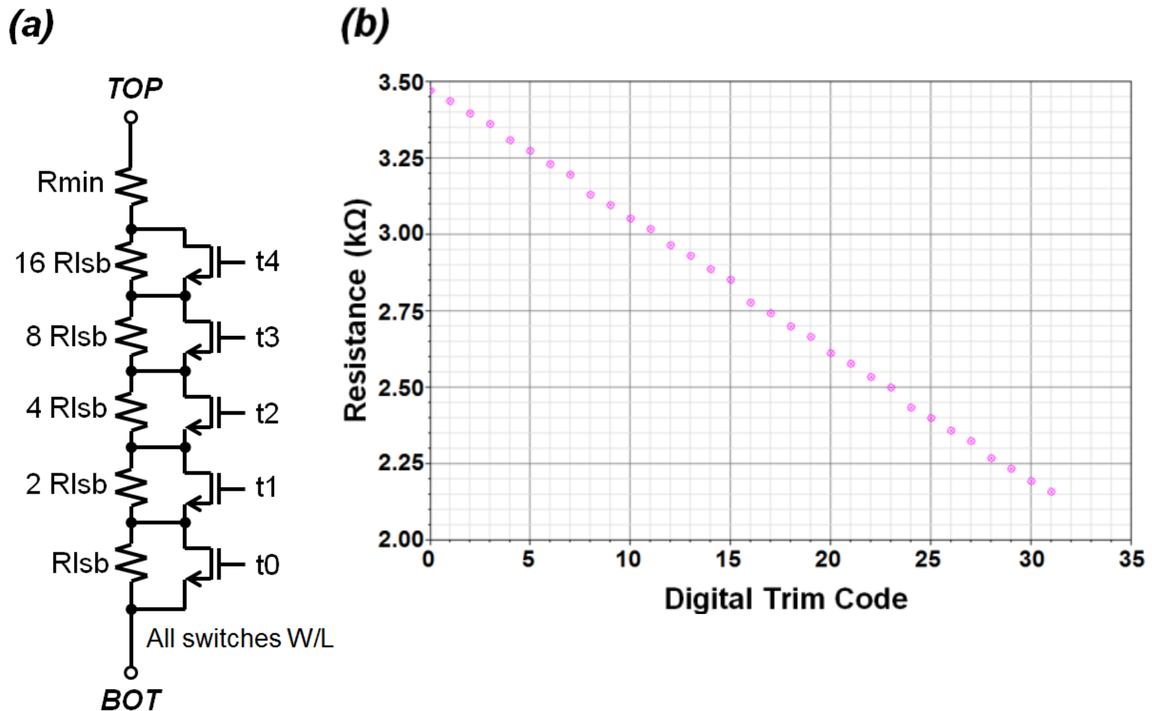


Fig. 79: (a) Schematic and (b) trim functionality of a 5-bit programmable resistor with series trimming scheme. Rlsb ≈ 44 Ω, Rmin ≈ 2.1 kΩ, W/L = 20/0.18.

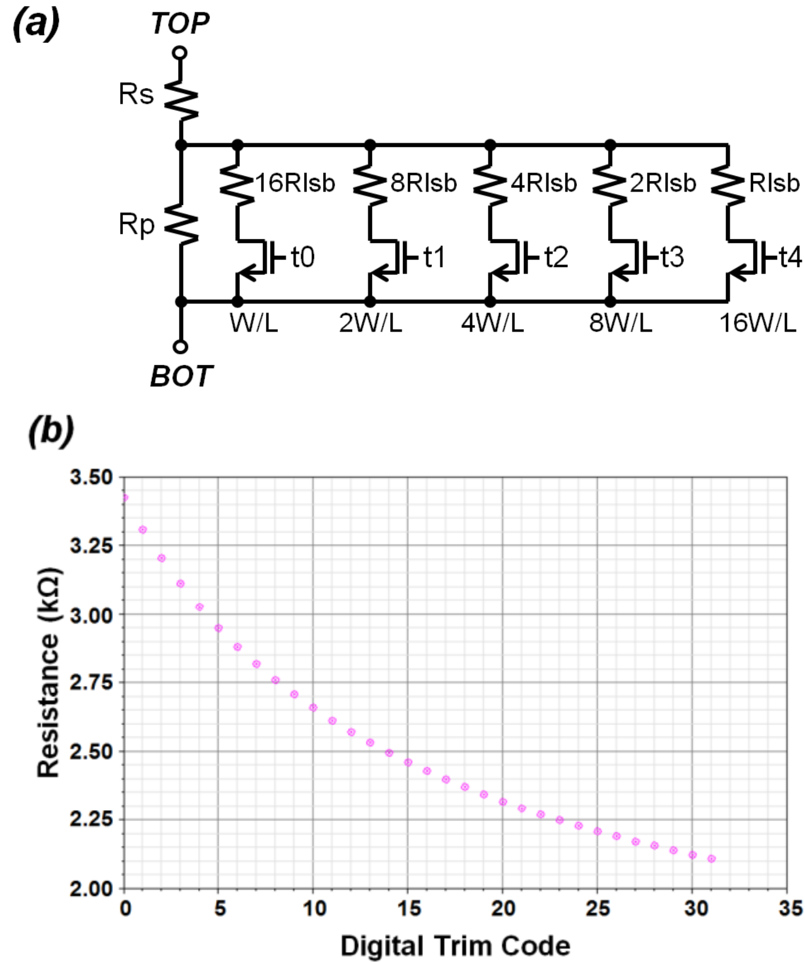


Fig. 80: (a) Schematic and (b) trim functionality of a 5-bit programmable resistor with parallel trimming scheme. Rs ≈ 1 kΩ, Rp ≈ 2.42 kΩ, Rlsb ≈ 4 kΩ, W/L = 20/0.18.

trim code. Nonlinearities are introduced by nonzero switch resistance, but since the circuit is simply a variable resistor and not functioning as a DAC, these are not of major concern. Although the switches do not require binary weighting themselves, their W/L must be quite large to minimize the ON resistance of each series connection. It will be shown that this is the main drawback to using this scheme in an RHBD circuit.

The schematic of a parallel trimming scheme is shown in Fig. 80(a). As before, the TOP and BOT nodes are the two terminals of the programmable resistor, and t0—t4 are the digital inputs controlling the nFET switches. In this topology the resistors—apart from Rs and Rp—*and* the switches are binary-weighted. Because each switch is only

immediately in series with its corresponding resistor, the ON resistance must only be sufficiently less than that particular resistor. Therefore, the switches can be binary weighted. Furthermore the ideal resistance of each binary-weighted branch can be expressed as:

$$R_{branch,n} = \frac{2^{4-n}\, Rlsb}{t_n}, \tag{99}$$

where n is the corresponding bit index (0—4), Rlsb is the LSB resistance, and t_n is the corresponding trim bit t0—t4 with a value of 0 or 1. The R_{branch} equation may not be mathematically sound because it divides a resistance by either 1 or 0, but by equating division by zero to infinite branch resistance (an open switch), the expression does accurately describing the trim function. Thus the parallel combination of all the binary-weighted resistors is:

$$R_{trim} = \frac{1}{\frac{t0}{16\, Rlsb}+\frac{t1}{8\, Rlsb}+\frac{t2}{4\, Rlsb}+\frac{t3}{2\, Rlsb}+\frac{t4}{Rlsb}} = \frac{16\, Rlsb}{t0+2\, t1+4\, t2+8\, t3+16\, t4} = \frac{16\, Rlsb}{trim}, \tag{100}$$

where t0—t4 are the trim bits and *trim* is the digital trim code in decimal 0—31. Finally the resistance between TOP and BOT can be expressed as the sum of Rs with the parallel combination of Rp and the trimmed resistance:

$$R_{parallel} = Rs + Rp \,||\, \frac{16\, Rlsb}{trim}, \tag{101}$$

where Rs is the series resistance 1 kΩ, Rp is the parallel resistance 2.42 kΩ, and Rlsb is 4 kΩ. These resistance values produce the trim resistance curve in Fig. 80(b). As expected from (101), the resistance does not decrease linearly with increasing trim code. However, since the purpose of the circuit is a programmable resistance and not a DAC, this is not an issue. The maximum resistance can be specified by the sum of Rp and Rs, and the span of the resistance can be specified by Rlsb.

The two trim schemes are fundamentally different in the way they respond to threshold voltage shifts and leakage. As discussed previously, the effect of V_{TH} shifts depends on how critical the switch ON resistance is. Since the series trim switches must short out fairly small resistances (Rlsb = 44 Ω), the ON resistance must be much lower than 44 Ω, making it a critical parameter. On the other hand, the parallel trim scheme can achieve small steps in resistance, but it is done using much larger resistors (Rlsb = 4 kΩ). The main function of the switches in the parallel scheme is creating open circuits, so the ON resistance is not nearly as critical, since the resistance of each branch is easily dominated by the poly resistor.

Simulation results of V_{TH} shifts in the two trim schemes are plotted in Fig. 81. The W/L for the unit-cell switch in both designs was 20/0.18, and each design was trimmed to the minimum resistance. This is the trim code most sensitive to V_{TH} shifts because every switch in ON. The series-trim resistance in Fig. 81(a) shows a linear response to the threshold shift with a slope of 0.18 Ω/mV. The parallel-trim resistance in Fig. 81(b) also shows a linear response, but the slope is significantly lower at 0.0037

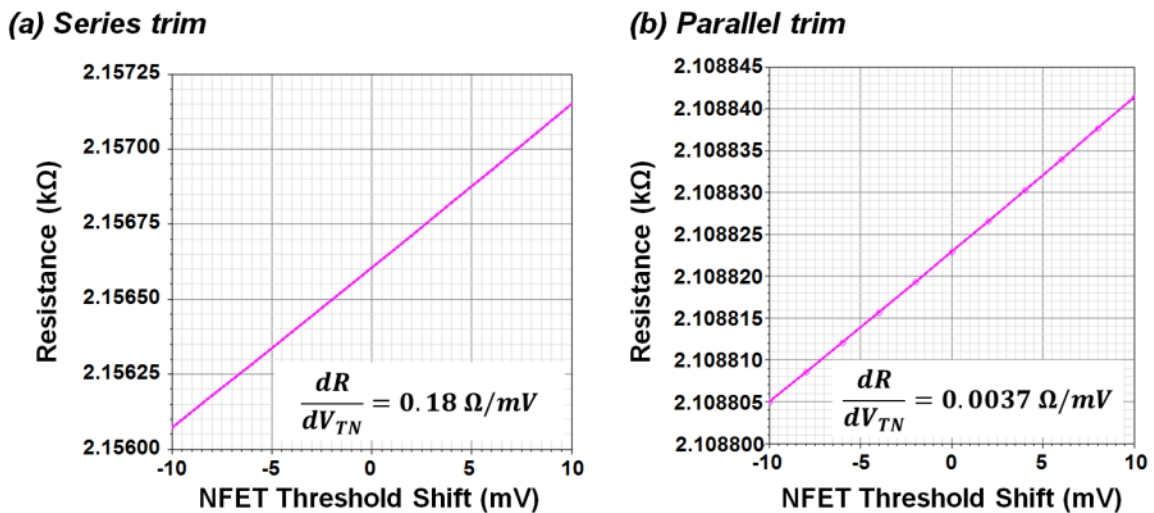


Fig. 81: Response of programmable resistor to nFET threshold voltage shifts with (a) series and (b) parallel trimming schemes.

Ω/mV. This indicates the series trimming scheme is nearly fifty times more sensitive to V_{TH} shifts. In a precision reference, the trimmed resistance may need to be stable within ±0.05% (½ LSB with 10-bit precision), corresponding roughly to 1 Ω in the two programmable resistors. The series trimming scheme can only tolerate a threshold shift of 5.56 mV before the resistance shifts by 1 Ω. However, the parallel trimming scheme can tolerate a shift of up to 270 mV. The previously discussed method for hardening switches to threshold voltage shifts is increasing the W/L ratio. The programmable resistors being compared in Fig. 81 do not utilize the same total switch area; because of the binary weighting, the parallel-trimmed resistor uses 6.2× more switch area than the series-trimmed resistor even though the same unit-cell W/L is used. When the W/L of the parallel trimming scheme is reduced to 4/0.18, it still tolerates V_{TH} shifts up to 103 mV. However, even when the W/L of the series trimming scheme is increased to 100/0.18, it only tolerates up to 19 mV of V_{TH} shift. With these modifications, the series-trimmed resistor now uses 4× more switch area. When the unit-cell W/L of the series trimming scheme is increased to 1000/0.18, it can tolerate up to 170 mV of V_{TH} shift. Five switches with unreasonably large channel widths of 1 mm are required to achieve this level of radiation tolerance in the series scheme.

One of the trimmable resistors in the RHBD voltage reference had a trim range of approximately 700—800 Ω. This would require the resistance to shift by less than 380 mΩ. Furthermore, for a 5-bit series-trim resistor, the ON resistance of a switch would have to be significantly smaller than 3.2 Ω. Since this is not feasible in a reasonable layout area, a parallel trimming scheme was used for R1 in Fig. 53. Because the parallel scheme does not require very small ON resistance, it is intrinsically more tolerant to

threshold voltage shifts, particularly when a fairly low resistance value (several kΩ or less) is required in the programmable resistor. On the other hand, the programmable resistor Rntc in Fig. 72 was implemented with a series trimming scheme, because the desired resistance was 61—72 kΩ.

The other radiation effect that affects the trimmed resistors is field-oxide leakage in the n-type switches. Because the switches in the series scheme are in parallel with low-valued resistors, the drain-source voltages of the OFF switches are quite low. With low V_{DS} the parasitic sidewall channel does not generator significant leakage current. However, the parallel trimming scheme is more sensitive to leakage effects, since the main function of the switches is preventing current flow. Although the Rp resistor in parallel with all switched resistors will keep drain-source voltages from getting too large, they can still be enough to cause resistance shifts. Leakage effects are easily mitigated with edgeless layouts or the use of pFET switches (if the voltage range allows it). If neither of these options is possible, then a V_{DS} analysis should be done to estimate the worst-case leakage currents.

In summary the proposed parallel trimming scheme is far more tolerant of threshold voltage shifts, while the series trimming scheme is more tolerant of leakage. For circuits in which a precise, low-value resistance of a few kΩ or less is required (or significant current is flowing through the resistor) the parallel trimming scheme should be used. Care must be taken to ensure leakage effects are eliminated or insignificant. For circuits in which a precise but higher-value resistance of 10 kΩ or more is required, the series trimming scheme is better suited due to its linearity, small resistors, and small switches. In general it is more straightforward to use the parallel trimming scheme

because it is easier to harden a design against leakage—using edgeless layouts—than it is to harden a design against threshold shifts—using very large W/L switches. However, in some processes edgeless transistors are forbidden by design rules, so the series trimming scheme may be a better option.

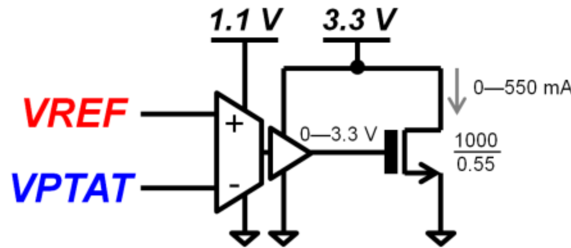


Fig. 82: Heater control in 40-nm temperature-regulated voltage reference. VREF is the reference voltage, and VPTAT is the temperature sensor voltage.

Mixed-voltage interfaces

In analog system design, it is often necessary for two blocks with different operating voltages to communicate. Although thin-oxide (core voltage) FETs in a deep submicron process are quite resistant to TID-induced degradation, thick-oxide (I/O voltage) FETs in the same process are significantly more sensitive to radiation, due to thicker gate oxides and lower doping concentrations [17], [19]. If an analog signal from a low-voltage (thin-oxide) circuit is processed by a high-voltage (thick-oxide) circuit, the radiation response of the high-voltage circuit can significantly alter how the signal is handled. However, with the proper interface design, the relative insensitivity of the low-voltage block can be leveraged to increase the robustness of the high-voltage block.

In the temperature-regulated designs implemented in the UMC 40-nm process, voltages from the reference core (thin-oxide transistors with 1.1-V supply) were used to control the heater (thick-oxide nFET with 3.3-V supply), as shown in Fig. 82. The heater was implemented with a 3.3-V nFET because large levels of power (hundreds of mW)

are required to adequately heat a temperature-regulated voltage reference. For the same power level, a 1.1-V nFET would require three times the current. The challenge with high currents is designing a layout with wide enough metal lines to pass electro-migration (EM) design rules. Using a higher voltage decreases the current requirement, which in turn decreases the required metal width.

The heater control circuit in Fig. 82 uses thermal feedback to ensure that the low-voltage signals VREF and VPTAT are equal. Since VPTAT is proportional to temperature, it is equal to the reference voltage VREF at only one temperature, which is the set point for the chip temperature. A constant temperature is maintained by controlling the current flow of the 3.3-V nFET heater. Thus a 3.3-V high-swing output stage attached to the 1.1-V OTA is required to interface the low- and high-voltage

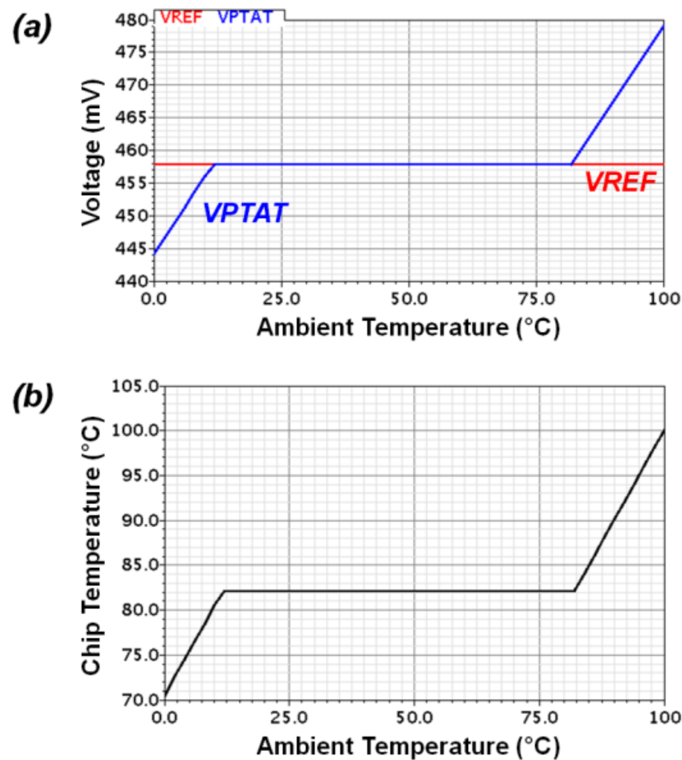
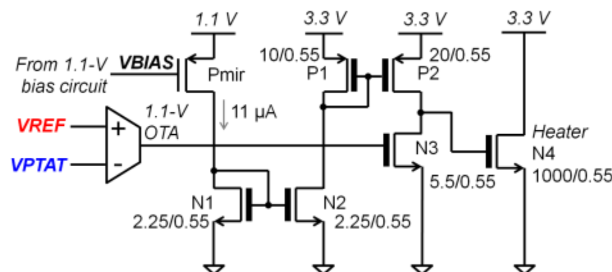


Fig. 83: (a) VREF and VPTAT control signals and (b) chip temperature (ambient temperature + rise in temperature generated by heater) as a function of ambient temperature in a closed-loop thermal feedback simulation of heater control circuit.

components of the circuit. The functionality of the heater control is demonstrated in Fig. 83. For this simulation the thermal resistance R_{TH} was 400°C/W and the electrical resistance in series with the heater was 60 Ω, so the maximum rise in temperature generated by the heater was $400 \times 3.3^2/60 = 72.6$°C. The set point for the heater was 82°C, so the temperature range during which the thermal feedback is fully functional is 9.4—82°C. In this temperature range, it is clear in Fig. 83(a) that the voltages VREF and VPTAT (modeled with voltage sources) are equal. It is also clear in Fig. 83(b) that across the ambient temperature range 9.4—82°C, the chip temperature is constant at 82°C. This indicates that the rise in temperature tracks the ambient temperature with a -1°C/°C slope, compensating for changes, as discussed in Chapter III.

The TID-sensitive blocks in this circuit are the 3.3-V output stage of the heater op amp and the heater itself in Fig. 82, since they are implemented with thick-oxide FETs. The heater design is primarily determined by the required current draw for adequate heating, so the high-voltage op amp output stage is the block to design for radiation hardness. Two implementations of the output stage are presented in Fig. 84. Both designs are simple common-source amplifiers—N3 with load P2—but they differ in how their

***(a)** Current-biased output stage*



***(b)** Voltage-biased output stage*

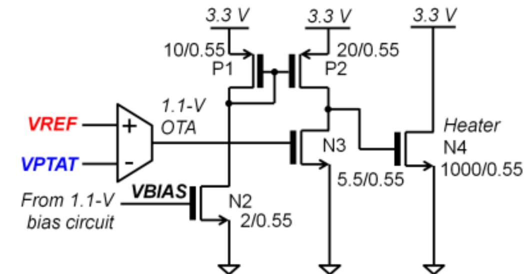


Fig. 84: (a) Current-biased and (b) voltage-biased implementations of high-voltage output stage of heater op amp. A thick gate line in the FET symbol indicates a thick-oxide (3.3-V) FET.

bias currents are generated. The current-biased circuit of Fig. 84(a) references an 11-μA current from a low-voltage current mirror (Pmir) to set the amplifier bias currents. The voltage-biased circuit of Fig. 84(b) simply references a bias voltage from the low-voltage domain to set the amplifier bias currents.

The primary radiation effect of concern in the amplifier stages is that of threshold voltage shifts, which can be sizable in thick-oxide FETs. Since thin-oxide FETs show very little threshold shift relative to thick-oxide FETs, V_{TH} shifts were only simulated in the thick-oxide FETs. Therefore, the simulations offer a one-to-one comparison of the two interface designs. Shifts in the threshold voltage ΔV_{TP} of P1 and P2 were simulated at 0, 100, 200, 300, and 400 mV, and shifts in the threshold voltage ΔV_{TN} of N1 and N2 were simulated at -300, -150, 0, 150, and 300 mV. In order to be fairly pessimistic it was assumed that threshold shifts in N3 were 1.2× larger than N2, and shifts in N4 (the

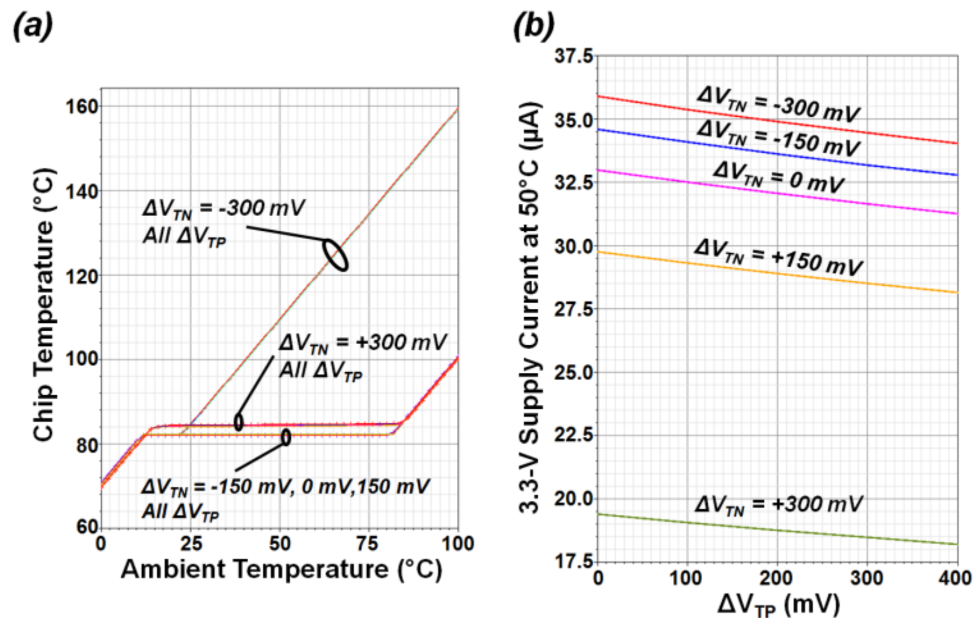


Fig. 85: (a) Thermal feedback simulations using current-biased amplifier with V_{TH} shifts. (b) 3.3-V supply current at 50°C as a function of pFET threshold voltage shift.

heater) were 4× larger than N2. All these V_{TH} shifts were applied simultaneous in the thermal feedback simulation of Fig. 83, for a total of 25 combinations.

The simulation results for the current-biased output stage are plotted in Fig. 85. Fig. 85(a) shows the thermal feedback operation of the circuit with the chip temperature as a function of ambient temperature. When the magnitude of the nFET threshold shift is less than or equal to 150 mV, the temperature is correctly regulated. However, when ΔV_{TN} is +300 mV the chip temperature increases by 2.3°C, although the thermal feedback is still functional. Given the nature of tempco cancellation in the reference voltage output, a temperature shift of 2.3°C will not cause a significant change in the output. In the other extreme, a V_{TN} shift of -300 mV causes circuit failure. The chip temperature is only regulated from 9°C to 23°C. Above 23°C the chip temperature increases with ambient, but with a 60°C higher temperature. Failure in the thermal feedback loop resulted in a much higher chip temperature than intended, pushing the device out of the recommended operating range. These results show very little dependence on threshold shifts in the pFETs. The 3.3-V supply current drawn by P1 and P2 at 50°C is plotted as a function of ΔV_{TP} in Fig. 85(b); these currents do not include the heater current. The separate lines show the effect of threshold voltage shifts. Overall, the total supply current varies by less than 16 μA, despite the large V_{TH} shifts in the circuit. As with the thermal regulation, the supply current shows very little dependence on V_{TP} and is dominated by the nFET radiation response.

The simulation results for the voltage-biased output stage are plotted in Fig. 86. The overlapping thermal feedback simulations in Fig. 86(a) show that the on-chip temperature regulation is fully functional for all 25 combinations of V_{TH} shifts. In fact,

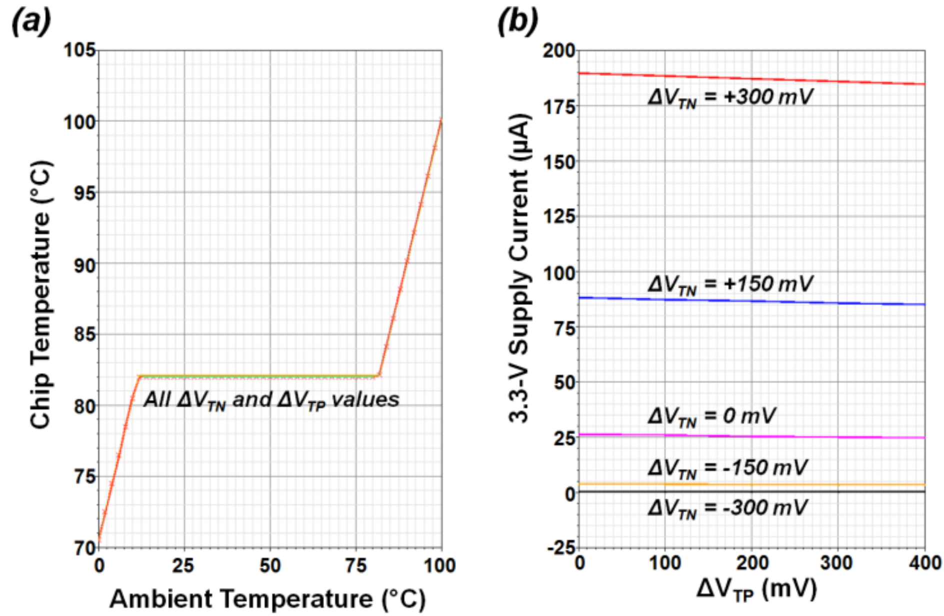


Fig. 86: (a) Thermal feedback simulations using voltage-biased amplifier with V_{TH} shifts. (b) 3.3-V supply current at 50°C as a function of pFET threshold voltage shift.

the chip temperature varies by less than 0.15°C, showing a very robust circuit response. The consequence of biasing with voltage rather than current is demonstrated by the supply current variations in Fig. 86(b). As before, the current draw of P1 and P2 is plotted and shows little dependence on ΔV_{TP}, but the current does vary by 187 µA in response to V_{TN} shifts. By using VBIAS to directly bias the thick-oxide nFET N2, any parametric shift in N2 strongly impacts all bias currents of the amplifier.

The fundamental difference in the two circuits' radiation response can be attributed to the supply current variations in Fig. 85(b) and Fig. 86(b). By referencing a specific current, the current-biased amplifier manages to minimize bias current variation, compared to the voltage-biased amplifier. However, the variation in bias current in the voltage-biased amplifier is precisely the reason for its high tolerance to V_{TN} shifts. For instance if all the nFET thresholds decrease, then the current sunk by N2 in Fig. 84(b) increases. The P1/P2 current mirror then increases the current supplied to the amplifying

transistor N3. Therefore, the bias current—optimized for transconductance—tracks the radiation-induced changes in threshold voltage, maintain the gain of the common-source amplifier stage. If on the other hand, the bias current of N3 stays relatively constant while V_{TN} decreases, then the overdrive voltage ($V_{GS} - V_{TN}$) of N3 increases without any change in current, pushing the device closer to the ohmic region of operation. This is what causes the amplifier to fail in Fig. 85(a). These results highlight the benefit of designing a circuit that is able to adapt to its own parametric shifts. The voltage-biased nFET N2 in Fig. 84(b) is basically a V_{TN} tracker that helps maintain the bias point of the amplifier N3. The same compensation mechanism is expected to mitigate the effects of leakage as well.

In conclusion, when designing an analog mixed-voltage interface, a biasing scheme that references a voltage—rather than a current—from the low-voltage domain is recommended. The relative insensitivity of the low-voltage (thin-oxide) circuit provides a somewhat stable reference point for the more sensitive thick-oxide circuitry to adjust for its own parametric shifts.

B. Single-event effects and mitigation

While the most difficult radiation effects to deal with in voltage references are the cumulative effects of TID, single-event effects (SEEs) must also be mitigated. A reference voltage is a global signal used by many blocks in a system-on-a-chip, so transient voltage perturbations can cause errors in every downstream block, from data conversion to power management. In this section, mitigation schemes for ASETs in first-order voltage references are presented using the differential charge cancellation (DCC)

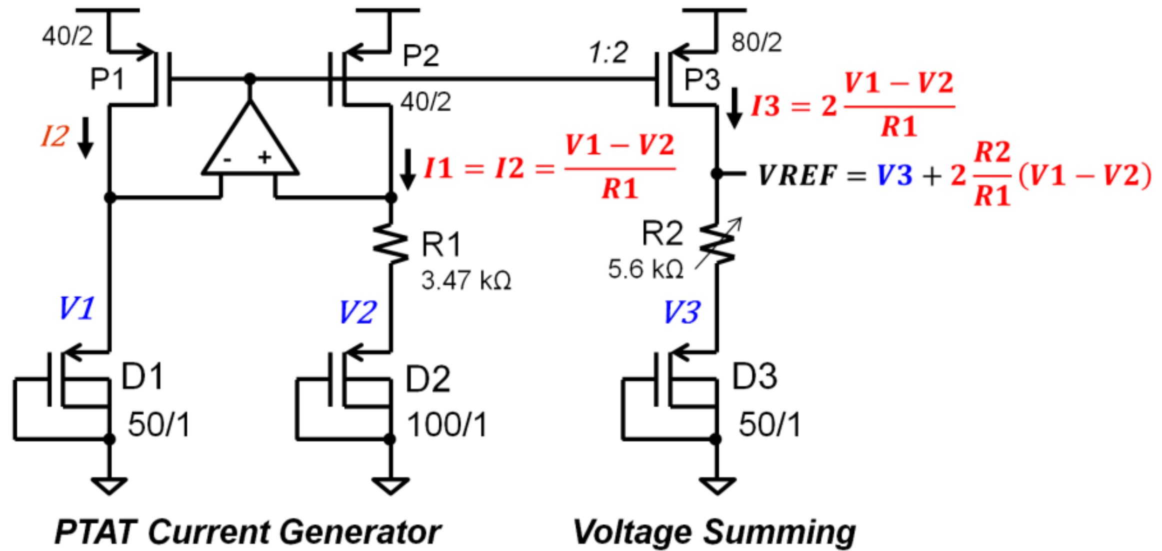


Fig. 87: Voltage-summing topology of reference designed and fabricated in UMC 40-nm process. Quantities in blue have a negative tempco, and quantities in red have a positive tempco.

and sensitive-node active charge cancellation (SNACC) techniques. Simulations of the voltage references designed in the UMC 40-nm process are used to demonstrate these techniques. In addition, the single-event hardness of the chopper-stabilized voltage reference from the previous section is discussed.

SEE mitigation in first-order voltage references

The voltage-summing reference designed in the UMC 40-nm process from Chapter III is used to demonstrate system-level applications of DCC and SNACC. For convenience the reference schematic is reproduced in Fig. 87, and the two subcircuits—the PTAT current generator and the voltage summing circuit—are labeled. The PTAT current generator is simply a difference amplifier that subtracts the DTMOST voltages V1 and V2, generating a current with a positive tempco. This PTAT current is mirrored and the sum of the PTAT voltage drop across R2 and the DTMOST voltage V3 yields a VREF voltage with first-order tempco cancellation. The heavy reliance on current mirrors

makes this topology ill-suited to precision TID-robust applications, but it is well-suited to unconventional ASET hardening techniques. In particular the differential nature of the PTAT current generator can be leveraged to mitigate ASETs using DCC, and SNACC can be applied to harden the sensitive nodes V3 and VREF.

Differential charge cancellation (DCC)

The concept of differential charge cancellation is exploiting multi-node charge collection (charge sharing) in a differential transistor pair to turn an ASET into a common-mode transient. The effect of the common-mode transient is then significantly mitigated by the common-mode rejection of the differential circuit. In the PTAT current generator of Fig. 87, promoting charge sharing between DTMOSTs D1 and D2 results in common-mode rejection in the mirrored output current I1 (equal to I2). The ideal output current transient can be expressed as:

$$i1_{SET} = \frac{v1_{SET} - v2_{SET}}{R1}, \tag{102}$$

where $v1_{SET}$ and $v2_{SET}$ are the voltage transients on nodes V1 and V2. It is evident that if the transients on D1 and D2 are equal, then the transient in the mirrored current is zero. The DCC technique uses a symmetric common-centroid layout to increase the probability of balanced charge sharing.

The two key design variables for a DTMOST in a voltage reference are the bias current and the current density. The current density is calculated as the bias current divided by the channel width, and it determines the voltage drop across the DTMOST. As current density decreases, the voltage tempco becomes more negative so it is necessary for D1 and D2 to operate at different current densities. There are two ways to scale the

current densities of D1 and D2. It can be done as in Fig. 87 by supplying equal current and scaling the channel widths, or it can be done as in Fig. 72 by supplying scaled currents and using identical channel widths. It is important to identify the most critical parameters to the SET response of D1 and D2 in order to match voltage transients as closely as possible.

In order to quantify the effects of bias current and current density, single events were simulated on a single DTMOST with 1-μm channel length using a traditional double-exponential current source with a 2-ps rise time and 200-ps fall time. The bias current of the DTMOST was varied while the current density was held constant at 0.1 μA/μm (corresponding to 100-μm channel width at 10-μA bias), which means the channel width was scaled proportionally with the bias current. This was done to separate the effect of bias current from that of current density. The resulting voltage ASETs are plotted in Fig. 88(a) for bias currents ranging from 1 to 15 μA. The constant current

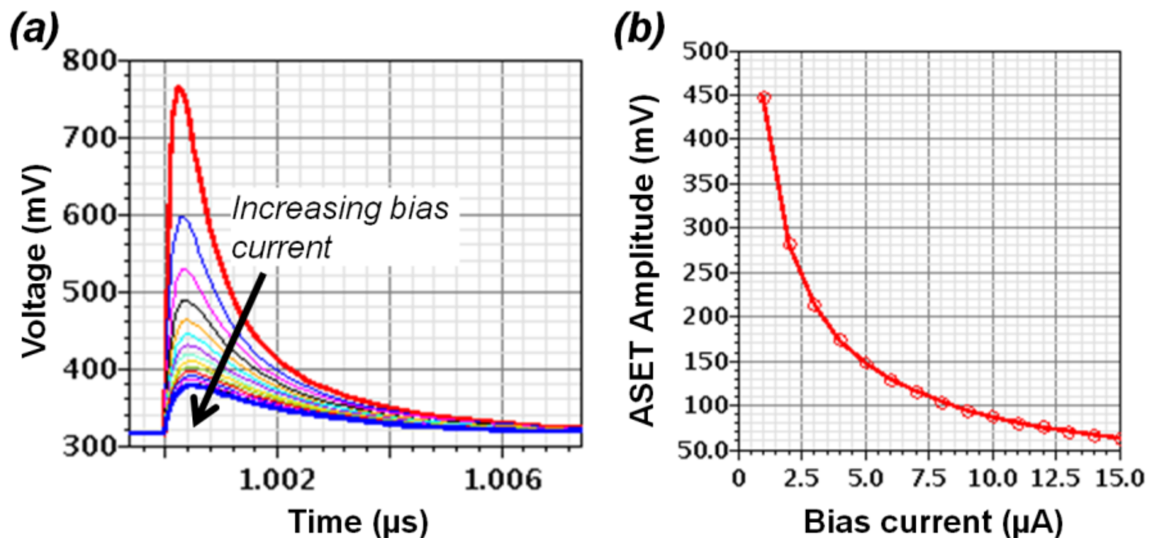


Fig. 88: Effect of bias current on ASETs generated in DTMOST. (a) ASET waveforms for bias currents ranging from 1 to 15 μA. (b) ASET amplitude plotted as a function of bias current. The width of the DTMOST is scaled such that a constant current density (current/width) of 0.1 μA/μm is maintained.

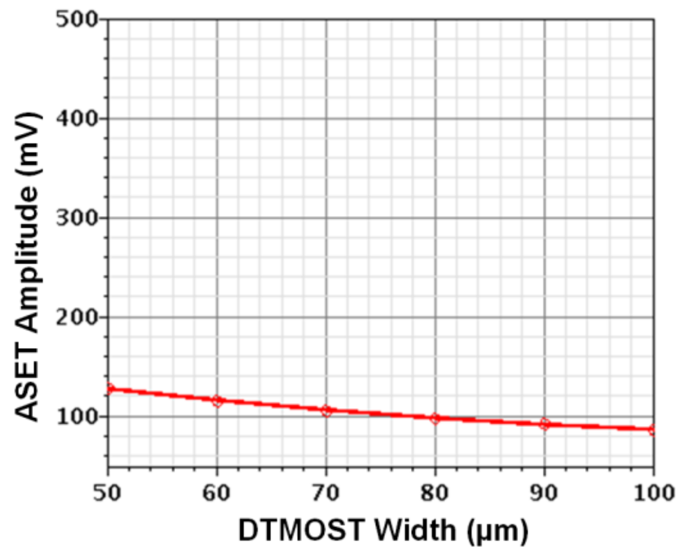


Fig. 89: Effect of DTMOST width on ASET amplitude when bias current is 10 µA.

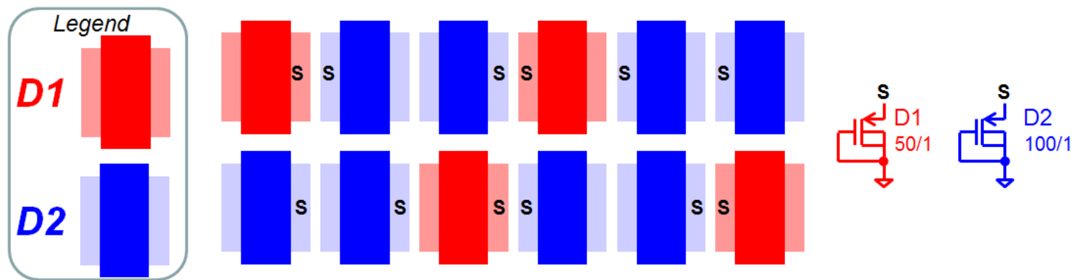
density is evident in the identical DC voltage across the DTMOST before the strike occurs. Since the bias current and the channel width of the DTMOST are both increasing, there are two effects causing the evident trend. As channel width increases the capacitance increases, reducing the ASET amplitude. Typically increased capacitance reduces the ASET amplitude while elongating the duration, but the increased bias current causes the duration to decrease as well. The amplitudes of the ASETs are plotted against the bias current in Fig. 88(b). These results show a strong dependence on bias current, so for optimal ASET matching between D1 and D2, identical bias currents should be used. A bias current of 10 µA is selected.

To quantify the effect of current density, the channel width of the DTMOST was varied at a constant bias current of 10 µA. The resulting ASET amplitudes are plotted as a function of channel width in Fig. 89. The scale for the y-axis is the same range as Fig. 88(b) in order to contrast the two effects. The current density (obtained by dividing 10 µA by the channel width) has much less of an impact on the SE response than the bias

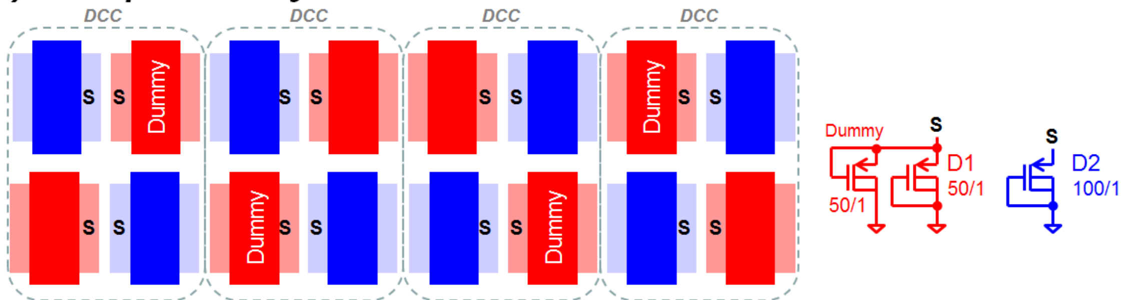
current, although there is still an effect. In the voltage reference D1 and D2 were designed with channel widths of 50 µm and 100 µm, respectively, so assuming equal charge collection their ASETs will be matched reasonably closely, as indicated in Fig. 89.

In order to increase the probability of charge sharing between D1 and D2, a DCC layout must be implemented. Typically the DCC layout is used between two identical transistors, but the reference requires D1 and D2 to have different dimensions. Using unit-cell 3.125/1 DTMOSTs the D1/D2 pair is laid out in the quadrant shown in Fig. 90(a), and the quadrant is repeated to create the common-centroid pattern in Fig. 90(c), which implements the pair in a vertically and horizontally symmetric layout. The size difference between D1 and D2 makes it difficult to promote equal charge collection in the

(a) Baseline quadrant layout of D1 and D2



(b) DCC quadrant layout of D1 and D2



(c) Common-centroid layout of quadrants

Quadrant	Quadrant
Quadrant	Quadrant

Fig. 90: (a) Baseline and (b) DCC layouts and schematics of D1/D2 DTMOST pair. Each drawn transistor has length 1 µm and width 3.125 µm. Each layout shown is only a quadrant of the complete layout; the complete layout is implemented with four quadrants as in (c).

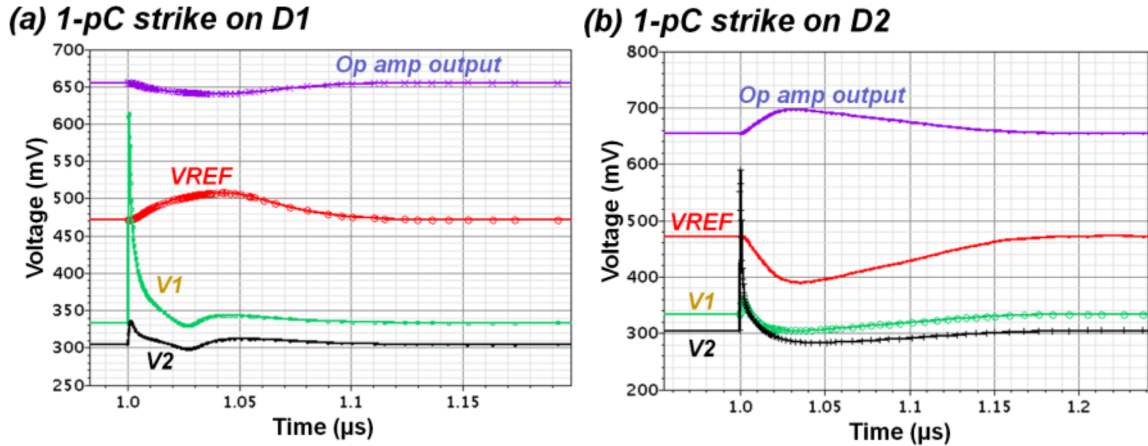


Fig. 91: Transient waveforms caused by 1-pC ion strike on (a) D1 and (b) D2.

two devices as there are twice as many D2 cells as D1 cells. Dummy transistors with the source shorted to the gate can be connected in parallel with D1 to equalize the layout areas of the two DTMOSTs, as shown in Fig. 90(b). Since the DTMOST current is dominated by channel conduction, the dummy transistors negligibly affect the current and voltage of D1. By adding the dummies, the overall layout area increases by 33%, but the layout can be implemented in DCC pairs, which have been shown to dramatically increase charge sharing benefits [91], [95].

Ion strikes depositing 1 pC of charge on either D1 or D2 were simulated, and the results are plotted in Fig. 91. These results are shown to demonstrate the opposite effect each strike has on the VREF output, as predicted, but another benefit of the voltage summing topology is highlighted. When D1 is struck in Fig. 91(a), the resulting V1 transient is 281 mV in magnitude, and based on the circuit operation the VREF transient should be approximately 3.2 times larger at 899 mV. However, the limited bandwidth of the op amp (less than 10 MHz due to phase compensation) results in significant transient attenuation at the op amp output, where the ASET amplitude is only 15 mV. Thus the VREF transient is only 36 mV, showing 96% attenuation via filtering. The same strike on

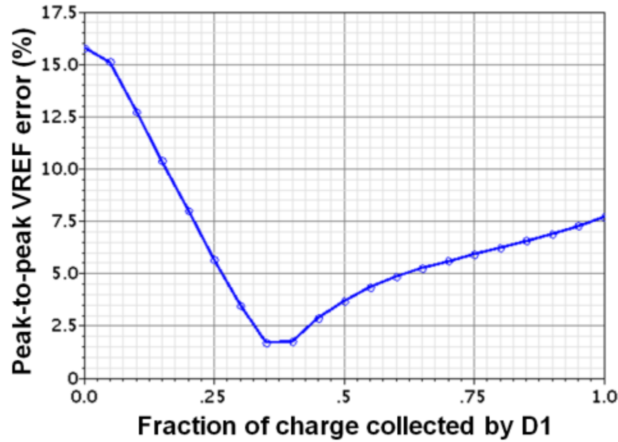


Fig. 92: Reference voltage ASET amplitude expressed as percentage of DC value 472 mV and plotted as a function of the fraction of charge collected by D1. The remainder of the 1 pC of deposited charge is collected by D2.

D2 in Fig. 91(b) results in a similar filtering effect, with a VREF ASET amplitude of 82 mV instead of 912 mV. Because the current mirror gates are driven by the op amp, the op amp low-pass filters all ASETs generated in the PTAT current generator. However this slow op amp response also elongates the ASET duration.

Charge sharing between D1 and D2 was simulated by depositing a total of 1 pC on the two devices. The resulting ASET amplitudes are plotted in Fig. 92 as the fraction of charge collected by D1 increases from 0 (all charge collected by D2) to 1 (all charge collected by D1). It is clear that charge sharing is beneficial to the SE response of the voltage reference. Interestingly, the minimum VREF perturbation of 1.7% (an 89% reduction from the worst case) is achieved when only 35% rather than 50% of the deposited charge is collected by D1. The reason for this offset is the systematic asymmetry in the design resulting from factors such as the additional gate capacitance at V1 introduced by the dummy DTMOSTs and the resistor R1 connected to V2. When D1 and D2 collect half the deposited charge, the output transient is still 76% smaller than the in the worst case of D2 collecting all the charge. Combining the filtering effect of the op amp with the charge sharing effects of Fig. 92 the SE response of a CMOS voltage

reference can be dramatically improved by separating the PTAT generation from the tempco cancellation.

Sensitive-node active charge cancellation (SNACC)

With the PTAT current generator hardened in the previous section, the remaining subcircuit to harden is the voltage summing block (Fig. 87). The output voltage is taken directly from this circuit, so it is the most sensitive to SE. Since this is simply a two-node circuit consisting of current source, programmable resistor, and DTMOST the SNACC hardening technique can be applied. SETs generated by ion strikes on a sensitive node can be mitigated by simultaneously collecting charge and providing a compensating current with a current mirroring scheme [78].

The voltage summing circuit is shown schematically in Fig. 93 with the added SNACC circuitry for SE hardening. The source of DTMOST D3 is connected to VREF through the resistance R2, so it is not as sensitive as the VREF node itself but still benefits from SNACC hardening. The SNACC circuit that mitigates ASETs on the V3 node is made up of a dummy transistor D3d and the current mirror formed by P1s and

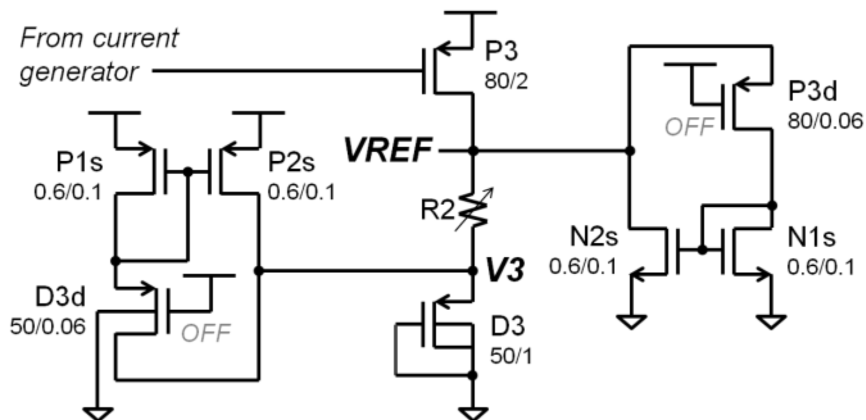


Fig. 93: Voltage summing circuit of Fig. 87 with SNACC circuitry added.

P2s. The purpose of D3d is for the source to collect charge that closely matches the charge collected by the source of D3. If both D3 and D3d collect charge, then the current flow in D3d triggers the P1s/P2s current mirror to supply an equal current to the V3 node, compensating for the SE-induced current in D3. By merging the drain region of D3d with the source region of D3 and biasing the gate of D3d OFF, the spacing between the sources of D3 and D3d is simply the dummy channel length, without the additional impediment of STI between the two nodes. Such a layout technique has been successful in reinforcing charge collection in latch designs [92], but this presents a novel application of the concept to the SNACC scheme. Using the dummy transistor as a spacer takes advantage of the small feature size of modern CMOS processes, promoting significant charge sharing while minimizing the area overhead of the SNACC circuitry. Furthermore, in any CMOS process the minimum channel length is a shorter distance than the minimum active-to-active spacing.

The 50/1 DTMOST D3 was laid out in 16 unit cells of 3.125/1 aspect ratio, and the layout (drawn to scale) of two of those unit cells along with two unit cells of D3d is shown in Fig. 94. The only area added by the two D3d cells is the sum of the two short channel areas and the source region in between. The sizes of the current mirror pFETs P1s and P2s were chosen for small size and fast response time; typically matching is critical in current mirrors, but these devices only activate during a single event so matching is much less critical. The total area overhead for the SNACC circuitry added to the V3 node is only 9.6%, compared to the layout of D3 alone.

The drain of current source P3 is connected directly to the VREF output, so it constitutes the most sensitive node in the circuit (and in the entire voltage reference). The

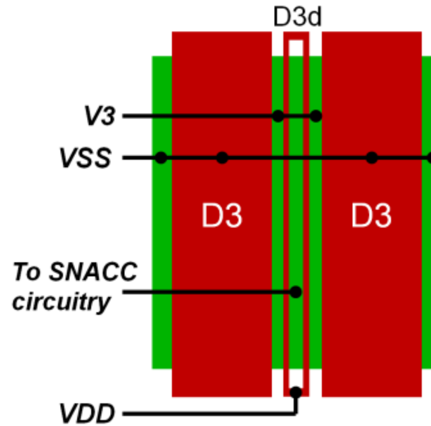


Fig. 94: Layout of two D3 unit cells with two D3d unit cell dummies. Channel width of each unit cell is 3.125 µm, channel lengths of D3 and D3d unit cells are 1 µm and 60 nm, respectively. Node names correspond to Fig. 93.

SNACC circuit that mitigates ASETs on the VREF node is made up of the dummy transistor P3d and the current mirror formed by N1s and N2s. The charge sharing nodes of P3 and P3d are laid out in the same manner as D3 and D3d. The SNACC circuitry added to the VREF node increases the layout area by less than 5.2%. The longer channel width of P3 compared to D3 results in a smaller area impact. The overall area overhead for implementing the SNACC scheme of Fig. 93 is 6.4%.

An ion strike depositing a total of 200 fC of charge on P3 and P3d was simulated, and the division of collected charge between the two transistors was varied to demonstrate the effect of charge sharing. The resulting VREF ASET waveforms are plotted in Fig. 95(a). The cases when all charge was collected by either P3 or P3d produced the largest ASETs, with amplitudes of 528 mV and -312 mV, respectively. While these ASET magnitudes are quite large, they are highly unlikely given the layout scheme used for P3 and P3d. When comparable amounts of charge are collected by P3 and P3d, both the magnitude and duration of the ASETs are significantly diminished. In order to capture information on both the amplitude and duration of ASETs, the error energy metric from [113] is used. The error energy of an ASET is defined as:

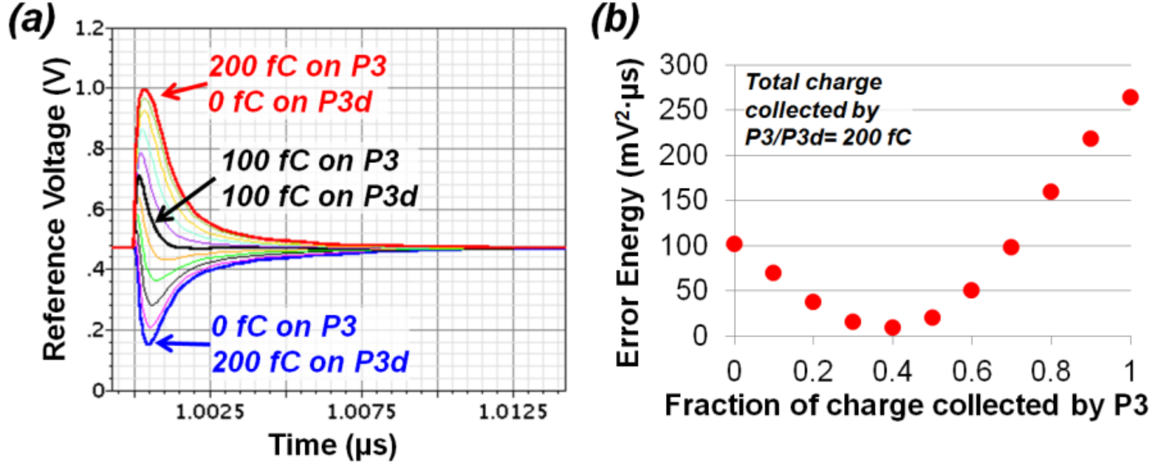


Fig. 95: (a) ASETs on VREF output due to ion strike depositing a total of 200 fC of charge on P3 and P3d in Fig. 93. The extremes cases and the case of a 50/50 split are labeled. (b) Error energies of ASETs plotted as a function of the fraction of charge collected by P3, with the remainder of the 200 fC collected by P3d.

$$\epsilon_{ASET} = \int_{t_0}^{t_0+T} [v(t) - V_{DC}]^2 dt, \tag{103}$$

where t_0 is the time of the strike, T is the duration of the computation, v(t) is the transient voltage signal, and V_{DC} is the baseline DC voltage. By integrating the square error signal a value with units of $mV^2 \cdot \mu s$ that increases with ASET amplitude and/or duration is obtained.

The error energies of the ASETs of Fig. 95(a) are plotted in Fig. 95(b) as a function of the fraction of charge collected by P3; at 0 all charge is collected by P3d, and at 1 all charge is collected by P3. The maximum error energy of 264 $mV^2 \cdot \mu s$ results when all 200 fC of deposited charge is collected by P3, and the minimum error energy of 8.62 $mV^2 \cdot \mu s$ results when 40% of the charge is collected by P3—a 97% reduction. As with the DCC scheme, there appears to be some systematic asymmetry in the SNACC scheme, as the 50/50 split of charge does not produce the smallest ASET.

The error energies of ASETs generated by 200-fC strikes on D3/D3d are plotted in the same manner in Fig. 96. It is first apparent that the severity of these ASETs is nearly 100× lower than those generated on P3. Because of the programmable resistor—

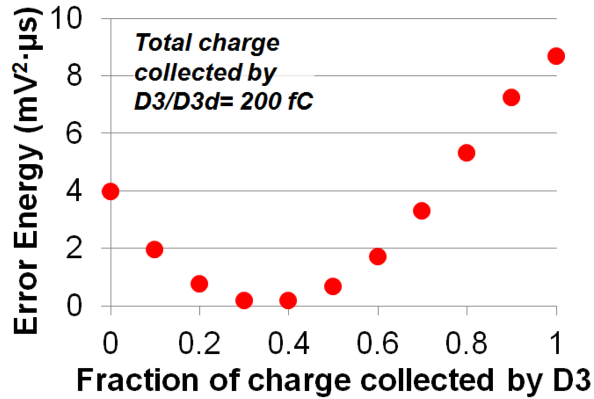


Fig. 96: Error energies of reference voltage ASETs plotted as a function of the fraction of charge collected by D3, with the remainder of the 200 fC collected by D3d

composed of poly resistors and nFET switches—between V3 and the output VREF, there is a fair amount of low-pass filtering of the ASETs at the output node. Although this makes the V3 node much less SE-sensitive than the VREF node, error energy reductions of up to 98% are still achievable with the SNACC scheme.

It is important to note that since the added SNACC circuitry is nominally OFF—only activated during a single event—it negligibly impacts the DC performance of the voltage reference. Although slight changes in tempco were observed due to sub-threshold leakage in the short-channel dummy transistors, the changes were insignificant and much less than the expected process variation. The simulation results of the two sensitive nodes in the voltage summing circuit demonstrate that ASET mitigation of up to 98% is possible with an overall area increase of only 6.4%. Furthermore the SE analysis of both the PTAT current generator and the voltage summing circuit highlight how designing the system with the two functions separated is beneficial to the SE response. Since the PTAT current is created using the difference between two voltages, ASETs can be mitigated using both DCC and the inherent low-pass filtering of an op amp. With the voltage summing occurring in a single current branch, ASETs can be mitigated with an area-

efficient SNACC scheme. If the PTAT generation and voltage summing were to occur in the same circuit as in Fig. 45, then the benefit of these techniques would be significantly diminished. The ASET mitigation presented in this section provides a general framework for implementing similar system-level schemes to general analog circuits, by altering the system topology to employ proven RHBD techniques.

SEE in RHBD chopper-stabilized voltage reference

Chopper stabilization was previously discussed as a hardening technique for TID-induced parametric shifts in a first-order voltage reference. In this section the SE hardness of the TID-hardened voltage reference is demonstrated using simulations. The SE tolerance of the design is simply a side effect of the chopper scheme, due entirely to the low-pass filtering required to filter out the chopper ripple. The schematic in Fig. 97

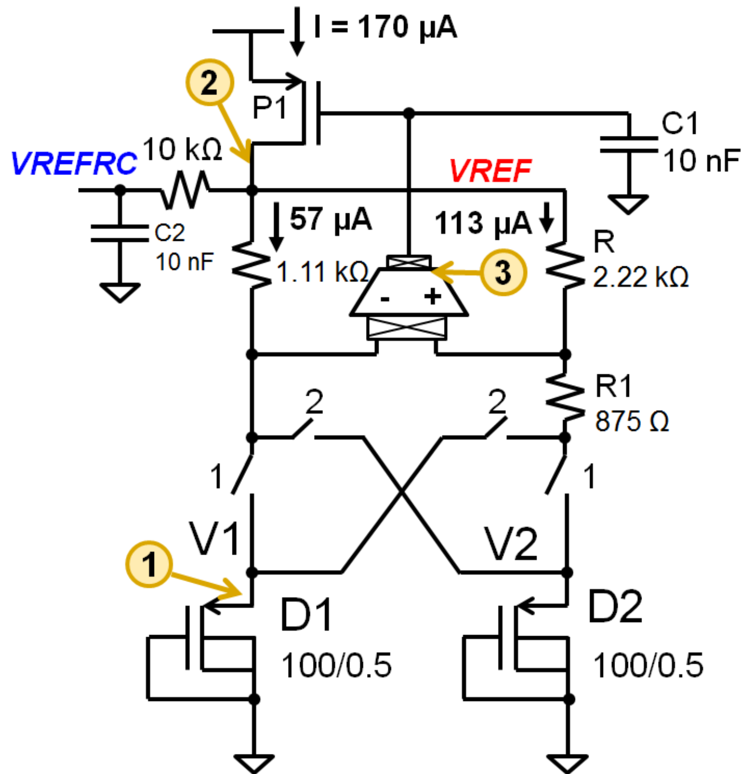


Fig. 97: Chopper-stabilized voltage reference with filter capacitors and three SE strike locations labeled.

shows the chopper-stabilized voltage reference with the filter capacitors C1 and C2. C1 serves a dual purpose of compensating the OTA and filtering the chopper ripple at the OTA output—leveraging the high impedance of the OTA output for a low cutoff frequency. C2 forms a simple RC filter with the 10-kΩ filter resistor, required for filtering the ripple introduced by the DTMOST chopper. Since the chopper frequency is 100 kHz, these filters have cutoff frequencies several orders of magnitude lower than 100 kHz, effectively filtering out all ASETs.

Using a simple double-exponential current source, ion strikes were simulated at the three strike locations indicated in Fig. 97. Location 1 is the source of DTMOST D1 during phase 1, so it is biased at 57 μA. An ion strike depositing 1 pC of charge (ion with LET of 100 MeV-cm^2/mg or 1 pC/μm in silicon with a collection depth of 1 μm) on the source of D1 was simulated, and the resulting ASETs on nodes VREF and VREFRC are plotted in Fig. 98(a). A large transient with amplitude of 130 mV is generated on the VREF node, but the 57-μA bias current dissipates the deposited charge within a few nanoseconds. With the time constants of the chopper filters orders of magnitude larger than a few nanoseconds, the ASET amplitude is reduced to a few microvolts at the filtered VREFRC node. A strike on D2 has an even smaller impact on the output because in phase 1 D2 is biased at twice the current of D1, resulting in even quicker charge dissipation.

The next node of interest is the drain of the current source P1, or the VREF node itself. The ASETs induced by an ion strike depositing 1 pC of charge are plotted in Fig. 98(b). Since it is struck directly, the VREF node exhibits an ASET with very high amplitude of over 1 V. However, the 170-μA bias current of P1 dissipates the deposited

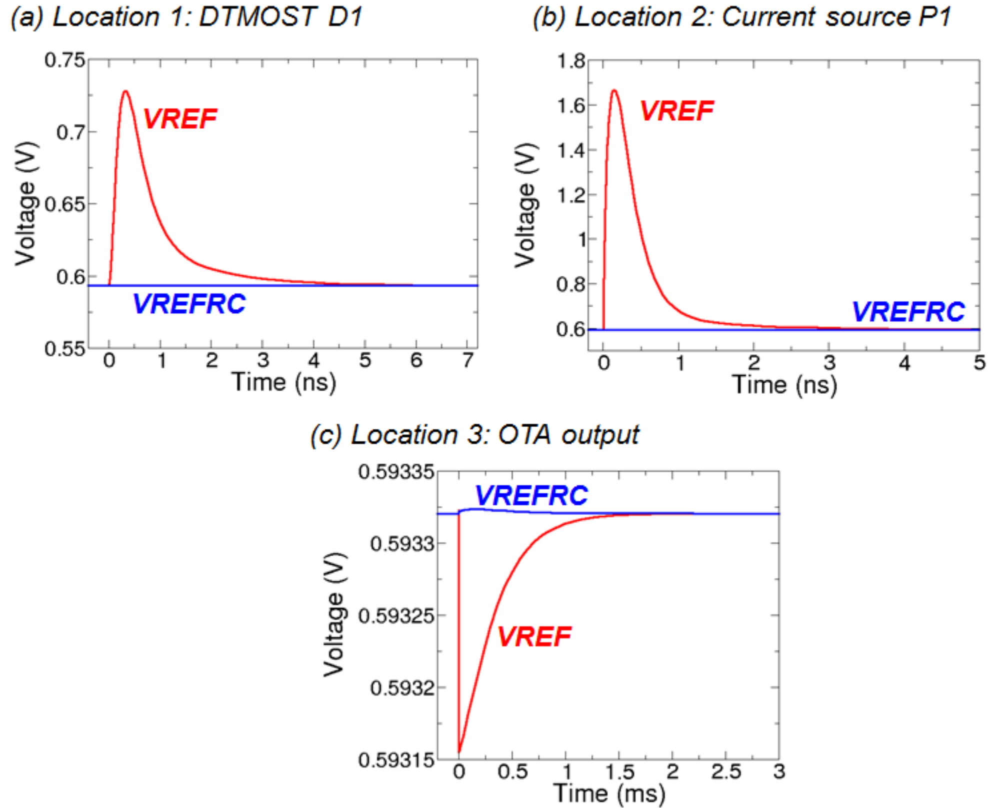


Fig. 98: SETs at VREF and VREFRC nodes when the three indicated locations in Fig. 97 are struck with ions depositing 1 pC of charge. Note: voltage and time scales are different in each plot.

charge within a few nanoseconds. As before, the quick transient is filtered down to a few microvolts at the VREFRC output. The potentially most sensitive node in the design is the OTA output. The high-impedance nature of the node would typically result in ASETs with long durations. As shown in Fig. 98(c), the resulting ASET at the VREF node is quite long, lasting more than a millisecond. The long duration is due to the large compensation capacitor C1 on the struck node. However, C1 also mitigates the magnitude of the voltage perturbation, which is only 175 µV. Once filtered, the output transient is reduced to a few microvolts. Since the other nodes in the OTA are low-impedance nodes, ASETs generated on those nodes are much shorter in duration than ASETs generated at the output node. Therefore, these transients would be even more heavily filtered, resulting in negligible output perturbations.

The final SE-sensitive circuitry to discuss is the chopper circuitry. The DTMOST chopper switches have SE responses similar to the DTMOSTs, since they are low-impedance nodes with DC currents of 57 or 113 μA. Deposited charge is quickly dissipated, and the fast transient that results is filtered out. The chopper on the OTA input is connected to DC-biased low-impedance nodes, so transients are similarly short in duration and easily filtered. The chopper on the OTA output has an SE response similar to the OTA output node itself, generating ASETs with long durations and small amplitudes that are further reduced through filtering.

Since the choppers themselves do not add SE vulnerability to the reference, the final block to consider is the digital control logic. The non-overlapping clocks are generated and buffered using simple combinational logic. Even a long digital SET with a 1-ns pulse width minimally impacts the voltage reference, because that 1-ns perturbation lasts for merely 0.01% of the clock period of the 100-kHz chopper clock. The only real sensitivity in the digital logic would be in the divide-by-2 block used to generate the clock with 50% duty cycle. Since a divide-by-2 circuit is implemented with a single D flip flop (DFF), the clock can be significantly perturbed by an upset in the DFF. Furthermore, since a positive-edge on the divide-by-2 input causes a change in the output, any buffering circuitry connected to the divide-by-2 input can similarly cause a significant disruption of the chopper clock. The simple solution to ion strikes on the divide-by-2 block is triple-modular redundancy (TMR) in the divide-by-2 DFF. Digital SETs in the combinational logic feeding the divide-by-2 circuit can easily be eliminated with a temporal filter on the divide-by-2 input, since the clock being buffered is only 200 kHz or slower. As long as the threshold pulse width of the filter is shorter than half of the

clock period, circuit operation will not be affected. By eliminating single-event upsets (SEUs) in the divide-by-2 circuit, the voltage reference is made immune to single events.

Single-event transients in the chopper-stabilized voltage reference are mitigated by the classic filtering RHBD technique. The filtering is required in the circuit to eliminate the ripple created by the choppers, so no additional modifications are required to make the analog components immune to ASETs. The only SE vulnerability in the circuit is the DFF in the divide-by-2 circuit required to generate a chopper clock with 50% duty cycle, but a simple temporal filtering and TMR scheme can be used to harden this block. Thus, the TID-hardened reference design can easily be made SE-hardened as well.

C. Conclusion

In this chapter radiation effects and mitigation schemes in continuous-time circuits were discussed. In particular, the voltage reference—being a fundamental component required in AMS systems—was used as a case study for analysis and mitigation of total-dose and single-event effects. The design techniques demonstrated in the voltage reference can be applied to a wide range of analog circuits.

The primary TID vulnerability of the voltage reference was shown to be sources of mismatch that can be altered by accumulated dose. The technique used to combat these effects was chopper stabilization, which can be generally applied to all op amp circuits, matched pairs, and current mirrors to mitigate the effect of offset voltage. By mitigating these effects the design is able to take full advantage of the radiation tolerance of modern deep submicron CMOS. A novel PTAT subtraction voltage reference scheme composed

of two difference amplifiers was presented to highlight the efficacy of the chopper stabilization technique in cancelling radiation-induced offset. The resistive current mirror was also demonstrated as a rad-hard alternative to a classical CMOS current mirror. By using resistors to distribute current from a single current source, mismatch effects are eliminated, and negative feedback can be used to compensate for current source degradation. RHBD guidelines were also presented for the layout of analog transistors, the design of programmable resistors, and the design of mixed-voltage interfaces. These techniques are not specific to voltage reference design and can thus be applied generally to AMS systems.

System-level applications of the DCC and SNACC single-event hardening techniques were also presented. While applying these techniques to basic building blocks such as bias circuits and op amps is beneficial, the proposed designs demonstrate a more generalized approach to applying the techniques to an analog system. In particular this was done by separating the functions of PTAT current generation and voltage summing (tempco cancellation) into two blocks and hardening each block with the most applicable technique—DCC for the PTAT generation and SNACC for the voltage summing. In addition it was shown that the filtering required for the TID-hardened chopper-stabilized reference also results in excellent ASET tolerance.

CHAPTER VI

RADIATION EFFECTS IN DISCRETE-TIME CIRCUITS

In Chapter IV the basic concept of switched-capacitor (SC) circuits was discussed, and designs of a differential SC sample/hold (S/H) amplifier were presented. In this chapter TID and SEE mitigation schemes for discrete-time circuits are presented. An SC voltage reference is used to present the TID tolerance of dynamic matching and auto-zeroing schemes in precision SC circuits. The previously presented S/H amp designs are used as a case study in demonstrating the single-event tolerance achieved by the novel quad-path hardening technique for SC circuits.

A. Total dose effects and mitigation

In the previous chapter, it was shown that radiation-induced mismatch was the most significant radiation vulnerability in the CMOS voltage reference. The most suitable mismatch reduction technique for continuous-time circuits is chopper stabilization, and it was shown that this technique significantly improved radiation robustness. In sampled-data circuits like SC circuits, the most suitable offset cancellation technique is auto-zeroing. Furthermore in SC circuits, it is possible to implement a voltage reference with first-order tempco cancellation using a single DTMOST, thereby eliminating the amplified DTMOST mismatch. In this section, both of these concepts are discussed as TID mitigation schemes with supporting simulations.

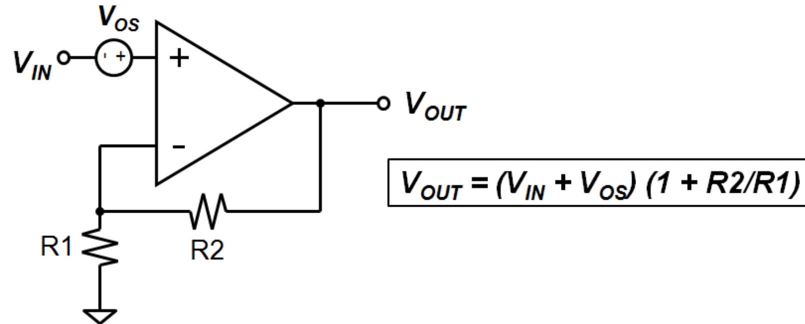


Fig. 99: Non-inverting amplifier with input-referred offset voltage V_{OS}.

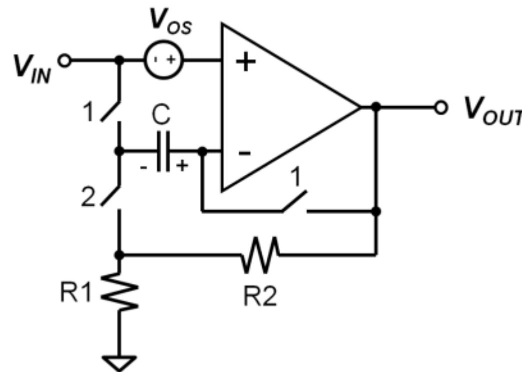


Fig. 100: Non-inverting amplifier with auto-zeroed op amp.

Dynamic offset cancellation: auto-zeroing

The concept behind auto-zero dynamic offset cancellation is much more straightforward than the previously discussed chopper technique. While chopper stabilization is a modulation technique, auto-zeroing is a simple sample-and-cancel technique [116]. The non-inverting amplifier in Fig. 99 is used to demonstrate the fundamental auto-zeroing concept. The op amp has an input-referred offset voltage V_{OS} that is amplified by the (1 + R2/R1) gain of the circuit. An auto-zero op amp in this circuit is implemented with the addition of a capacitor and three switches operated on two non-overlapping clock signals, as shown in Fig. 100. The first phase of operation is the sample phase, during which the switches labeled '1' are closed and the switch labeled '2' is open. The circuit operation during the sample phase is described in Fig. 101(a). The op

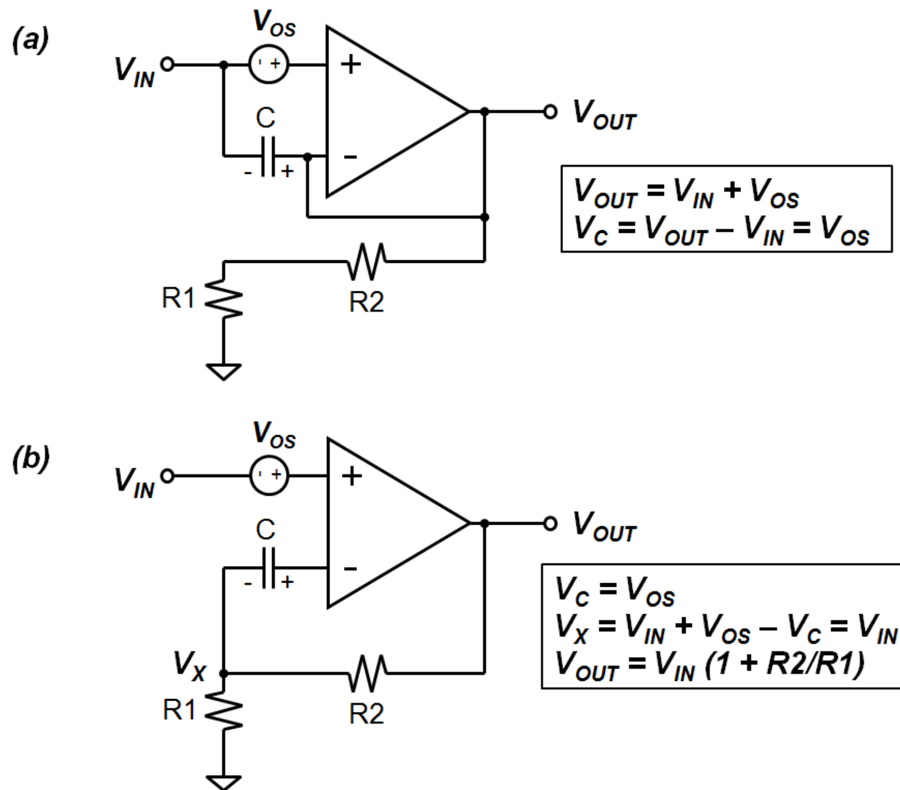


Fig. 101: Operation of auto-zeroed amplifier in (a) sample phase and (b) cancel phase.

amp is configured as a voltage follower with the sample capacitor between the inverting and non-inverting inputs. The voltage follower output is the input voltage with the input-referred offset, so the voltage sampled across the capacitor is the offset voltage. The second phase of operation is the cancel phase, during which the switch labeled ‘2’ is closed and the other switches are open. By placing the capacitor with V_{OS} stored on it in series with the inverting input, the input-referred offset voltage is cancelled at the V_X node. Therefore, the output is equal to the amplified input without the offset voltage.

The auto-zeroing scheme in the non-inverting amplifier is a simple example of an input-sampled scheme. Other schemes exist that sample/cancel the offset voltage at the output or apply a sampled offset-correction signal to an internal node [116], [128], [129]. In the scheme of Fig. 100, the circuit only has a valid output during the cancel phase, so a sample/hold stage would be required to maintain a continuous output voltage. This dual-

phase operation makes auto-zero offset cancellation particularly well-suited to discrete-time systems, which typically require several phases of operation. In general the residual offset in auto-zeroed circuits is lower than chopper circuits, since the offset if actually sampled and nulled. While the auto-zero technique significantly reduces the low-frequency noise of an amplifier, it does increase the thermal noise floor via noise folding effects [115]. This is the main drawback of the sample/cancel scheme, but it is still well-suited to RHBD AMS systems.

Switched-capacitor voltage reference with auto-zeroed op amp

A switched-capacitor DTMOST-based voltage reference is shown schematically in Fig. 102. The operation of the circuit is similar to the voltage references in [130], [131]. Although there are two DTMOSTs D1 and D2, only D1 is used to generate voltages for the reference; D2 is simply there to prevent large transients when the second bias current is switched over to D1. During phase 1, the switches labeled ‘1’ are closed

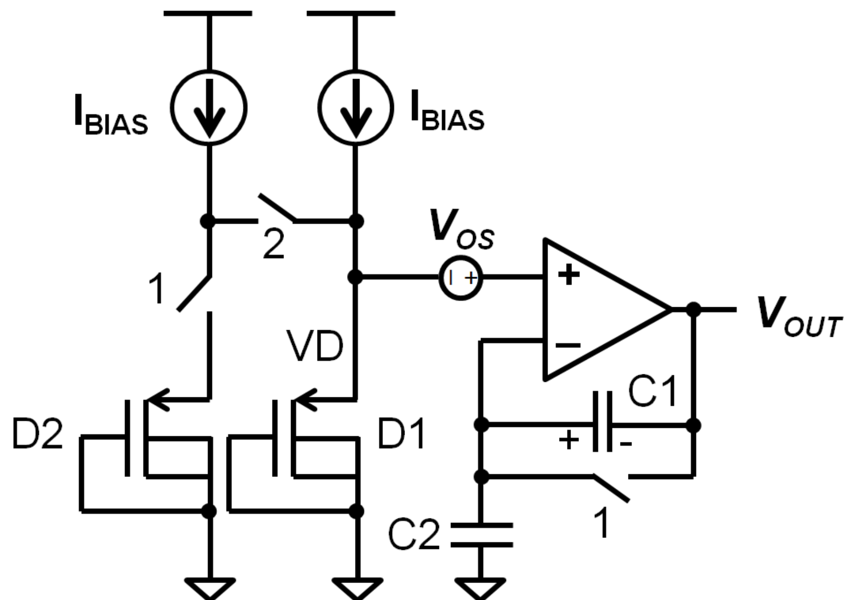


Fig. 102: Switched-capacitor DTMOST voltage reference.

and the switch labeled '2' is open. In this phase the op amp is configured as a voltage follower, and the voltage stored on C2 is equal to the output voltage:

$$V_{C2,phase1} = V_{OUT,phase1} = VD(I_{BIAS}) + V_{OS} = V1 + V_{OS}, \quad (104)$$

where V1 is the DTMOST voltage VD when the current I_{BIAS} is applied. In phase 2 the switch labeled '2' is closed and the other switches are open. Now the voltage at VD is $VD(2\times I_{BIAS})$, defined as V2. The feedback of the op amp forces the inverting input to be equal to ($V2 + V_{OS}$), and some of the charge store on C2 is transferred to C1. Following the principle of the conservation of charge, the output voltage can be expressed as:

$$V_{OUT,phase2} = V_{C2,phase2} - V_{C1,phase2} = V2 + V_{OS} + \frac{C2}{C1}(V2 - V1). \quad (105)$$

Thus, the circuit has a valid voltage reference output during the second phase only, easily supporting integration with the SC front-end stages of an ADC.

Both V1 and V2 have negative tempcos, and their difference has a positive tempco, therefore first-order cancellation can be achieved by properly designing the C2:C1 gain factor. Without any additional modifications, two things make this a viable topology for an RHBD reference: the use of a single DTMOST and the lack of offset amplification. Both V2 and V1 are generated by D1, meaning TID-induced shifts in the voltages V1 and V2 will be perfectly matched. Therefore, changes in the (V2 – V1) which would be amplified by C2/C1 are negligible, and the radiation response of the DTMOST only affects the V2 term. In addition, the offset voltage appears unamplified in the output voltage expression. This is in contrast to the continuous-time voltage references of Chapters III and V, whose radiation responses were severely limited by amplified offset voltage. However, the complexity of the op amp can result in offset voltage shifts of a few mV, which can still limit the precision of the reference.

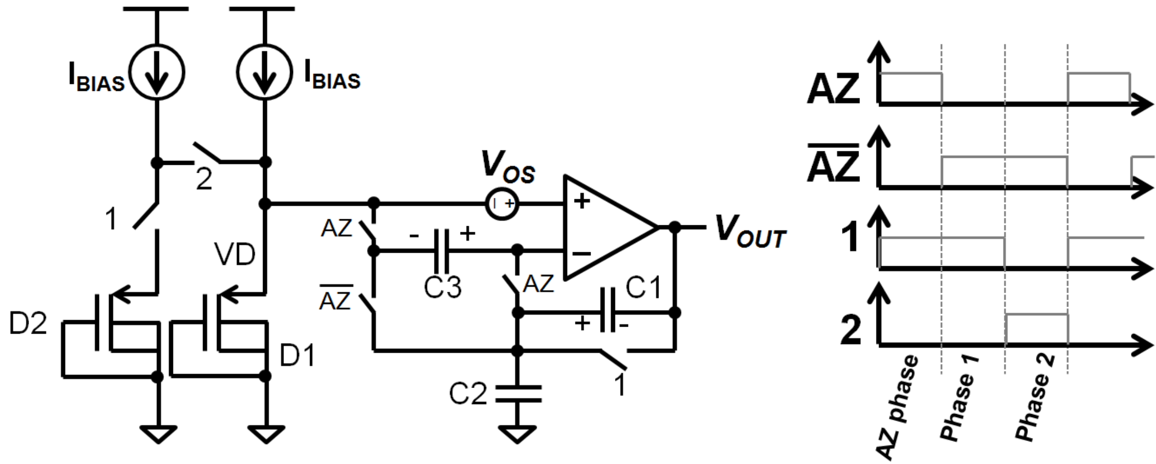


Fig. 103: SC voltage reference with auto-zeroed op amp with clock timing diagram.

With the addition of an auto-zeroing scheme, the SC voltage reference can be hardened against TID effects. The same SC voltage reference with auto-zeroing is presented in Fig. 103. The circuit has three additional switches and an additional capacitor C3, and it now operates on three phases with the clock signals plotted in Fig. 103. The additional AZ (auto-zero) phase is when the offset voltage is sampled onto C3, while phases 1 and 2 have the same operation as before.

The three phases of operation are illustrated in Fig. 104. Fig. 104(a) shows the circuit during the AZ phase, when the op amp is configured as a voltage follower with C3 between the two inputs. The voltage sampled onto C3 is:

$$V_{C3} = V_{OUT} - V1 = V_{OS}. \tag{106}$$

Then in phase 1—shown in Fig. 104(b)—C3 is placed in series with the inverting op amp input, so the voltage sampled onto C2 is:

$$V_{C2,phase1} = V_{OUT} = V1 + V_{OS} - V_{C3} = V1. \tag{107}$$

Finally in phase 2—shown in Fig. 104(c)—C3 continues to cancel the offset voltage and the output reference voltage is:

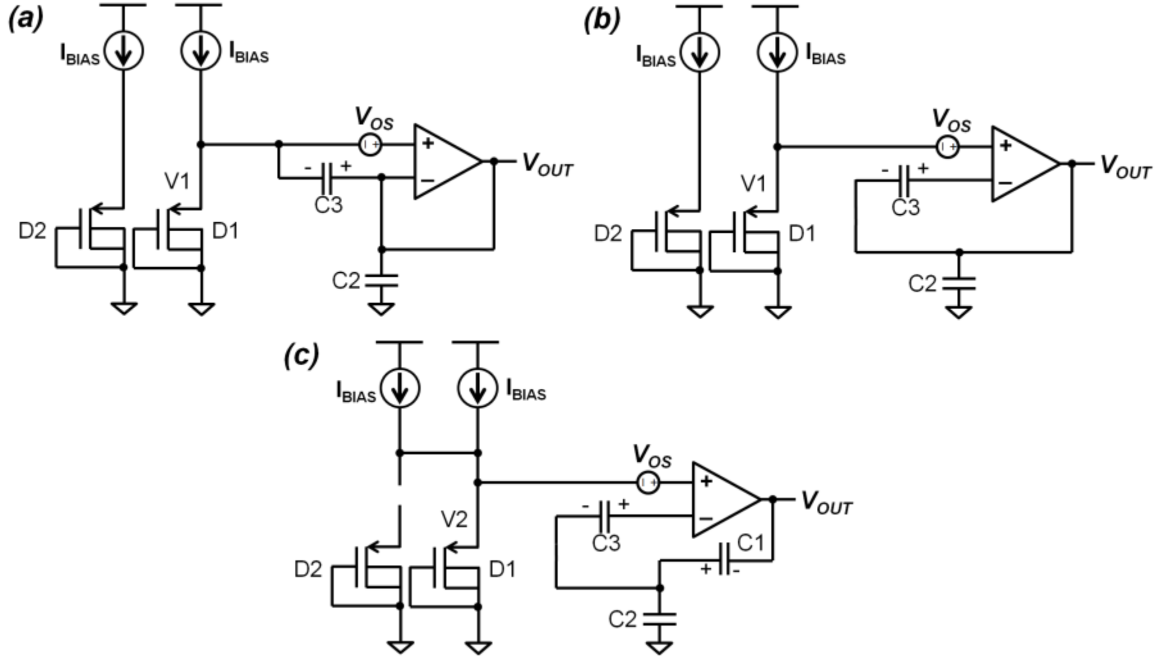


Fig. 104: (a) AZ phase, (b) phase 1 and (c) phase 2 of operation of the auto-zeroed SC voltage reference in Fig. 103.

$$V_{OUT,phase2} = V2 + V_{OS} - V_{C3} + \frac{C2}{C1}(V2 - V1) = V2 + \frac{C2}{C1}(V2 - V1). \qquad (108)$$

Thus the offset voltage is cancelled in the valid output phase of the circuit. This cancellation occurs each cycle so it tracks V_{OS} as TID degrades it.

To demonstrate the offset cancellation of the circuit, the auto-zeroed reference of Fig. 103 was simulated in an IBM 180-nm process. The complementary folded-cascode op amp design discussed in Chapter III was used. The DTMOSTs had W/L ratios of 25/0.5, the current I_{BIAS} was equal to 50 μA, and the capacitance values were C1 = 1 pF, C2 = 3 pf, and C3 = 10 pF. The clock frequency was 100 kHz, so each phase had a duration of 3.33 μs. Since the offset voltage must be stored stably on C3 for two full phases, increasing the size of C3 aids in the offset cancellation. Ideal switches were used, and a simple pFET current mirror was used to source the two I_{BIAS} currents. The temperature response of the circuit is illustrated in Fig. 105. The V_{OUT} waveforms plotted

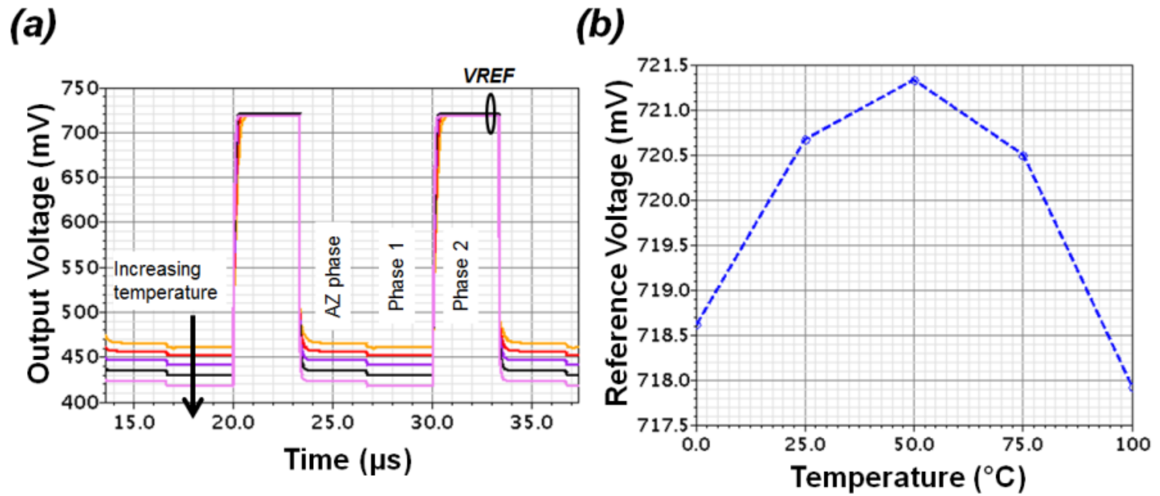


Fig. 105: (a) Time-domain waveforms of SC reference output at 0, 25, 50, 75, and 100°C. (b) Voltage reference output at the end of phase 2 as a function of temperature.

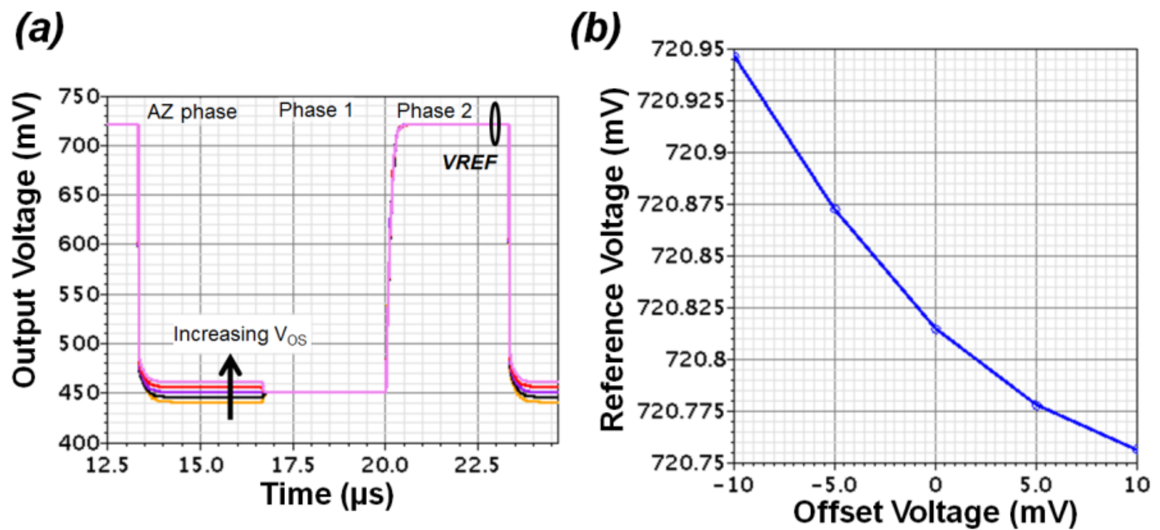


Fig. 106: (a) Time-domain waveforms of SC reference output with -10, -5, 0, +5, and +10 mV of offset voltage in the op amp. (b) Voltage reference output at the end of phase 2 as a function of offset.

in Fig. 105(a) demonstrate the functionality, showing the three phases of operation with the valid reference output at the end of phase 2. The circuit was simulated with an input-referred offset of 5 mV modeled with a DC voltage source. The 5-mV correction in the output can be seen as the circuit transitions from the AZ phase to phase 1. The phase 2 output is plotted as a function of temperature in Fig. 105(b) to demonstrate the first-order tempco cancellation in the design.

The effect of op amp offset voltage is shown in Fig. 106. The output waveforms in Fig. 106(a) show the sampled offset voltage in the AZ phase and the offset correction in phases 1 and 2. The output at the end of phase 2 is plotted as a function of offset voltage in Fig. 106(b), showing the significant attenuation of offset drift. A -10-mV shift in offset voltage generates a 130-μV shift in output voltage—a less than 0.02% change. To demonstrate the benefit of using a single DTMOST to generate a reference voltage, shifts in the DTMOST operation were simulated by placing a voltage source in series with D1. Voltage shifts from 0 to 0.4 mV were simulated—a reasonable range values based on measurements in the previous chapter—and the resulting shift in reference voltage is plotted in Fig. 107. As predicted the reference shifts shows a 1:1 correlation with the DTMOST shifts. Since there is only one DTMOST, there is no mismatch amplification causing large reference voltage shifts. A reference shift of 0.4 mV corresponds to a 0.055% shift. The radiaiton response of the SC reference is primarily limited by the DTMOST radiation response, which has been measured to be exceptionally minimal.

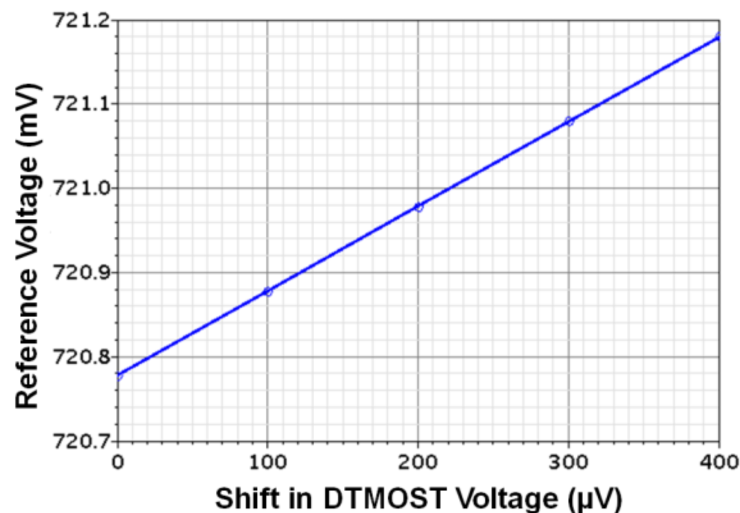


Fig. 107: The effect of shifts in the DTMOST D1 on the phase 2 output of the SC voltage reference.

The remaining possible sources of TID degradation in the circuit are the switches and the current sources. The only switch whose ON resistance is critical is the switch transmitting the I_{BIAS} current to D1 (labeled '2' in Fig. 103). Therefore, this switch should be sized appropriately to minimize any anticipated threshold voltage shifts. The larger size will not be a significant issue in terms of charge injection because the switch is connected to a low-impedance node with a DC current. Radiation-induced sidewall leakage is primarily a problem in OFF switches with sufficiently high V_{DS}, which can result in substantial leakage current in the parasitic sidewall channel. The switch with the highest OFF-state V_{DS} is the switch in parallel with C1, with a drain-source voltage equal to (V2 – V1)—generally on the order of 50 mV. While this most likely will not result in significant leakage current, using edgeless layout for n-type switches would combat the effect.

The I_{BIAS} current sources still poses a significant weakness in the radiation tolerance of the SC reference. While a simple resistive biasing scheme would be TID tolerant, the power supply rejection would suffer significantly. A pFET current mirror would be sensitive to radiation-induced mismatch effects. Furthermore, a TID-hardened current generator would be required to supply the current to the current mirror. This remains an unsolved problem with the RHBD SC reference concept, and would be an interesting avenue of further research.

The final issue with the SC design is the difficulty of integrating the core reference into a temperature-regulated system. The continuous-time references have PTAT signals readily available to serve as on-chip temperature sensors for the thermal

regulation, but it appears further circuit modifications would be required to generate such control signals in the SC reference. This problem also requires further investigation.

The implementation of the auto-zeroing scheme in a discrete-time circuit does involve area and speed penalties. The area overhead in implementing the auto-zeroing scheme depends on the area of the additional switches and capacitor. In this example, the addition of C3 constitutes a 2.5× increase in capacitor area. However, the added capacitor is still a reasonable on-chip value, unlike the 10-nF off-chip capacitors proposed in the chopper-stabilized reference. At worst the additional auto-zero phase slows down circuit operation by 33%, assuming equal phase durations. If the circuit already has a reset phase—like the S/H amplifier in the next section—then the auto-zeroing can be incorporated into that phase without a significant speed penalty.

B. Single-event effects and mitigation

The previous section demonstrated some features of SC circuits that can be beneficial to the TID response of a system. However, in previous work switched-capacitor circuits have exhibited significant single-event (SE) vulnerability in AMS designs such as analog-to-digital converters (ADCs) [96]–[98], [132]. This is largely due to the high-impedance (or floating) nodes inherent in SC circuits during part of the clock cycle, resulting in extreme sensitivity to collected charge. This sensitivity worsens as CMOS technologies scale, with node capacitances and supply voltages decreasing. In order to reduce the SE sensitivity of SC circuits with minimal performance tradeoff, it is necessary to employ a more unconventional RHBD technique, such as dual-path hardening [97], [98], [132].

The dual-path hardening technique was first presented in 2008 by Fleming et al., using simulations of a differential sample-and-hold (S/H) amplifier to demonstrate the single-event tolerance of the technique [97]. The technique was also presented by Olson et al. as a hardening technique for switched-capacitor comparators in [98], and the efficacy of this application was demonstrated experimentally in [132]. However, while the dual-path topology significantly improves SE tolerance in differential SC circuits, it also forces the designer to use single-FET switches for the SC network, and also use the same FET type in the amplifier input stage (e.g. nFET switches with nFET inputs).

Using single-FET switches—as opposed to transmission-gate (TG) switches—prevents a switched-capacitor circuit from achieving a rail-to-rail input signal range unless a charge pump circuit is used. On the other hand, the *quad-path hardening technique* described in this paper allows a designer to use TG switches while maintaining excellent SE tolerance. In this section, the quad-path hardening technique is presented and demonstrated using the differential sample/hold amplifier described in Chapter IV.

The quad-path hardening technique

The general topology of a S/H amplifier is shown in Fig. 108. The circuit consists of switches controlled by non-overlapping clocks ϕ_1 and ϕ_2, matched pairs of sample capacitors (C_S) and feedback capacitors (C_F), and a fully-differential operational transconductance amplifier (OTA). When ϕ_1 is HIGH and ϕ_2 is LOW, the circuit is in sample mode, and the differential input voltage ($V_{IN}+$ - $V_{IN}-$) is sampled onto the C_S pair while the OTA discharges the feedback capacitors C_F. In this stage, the differential output is reset to zero. When ϕ_1 is LOW and ϕ_2 is HIGH, the circuit is in evaluation mode, and

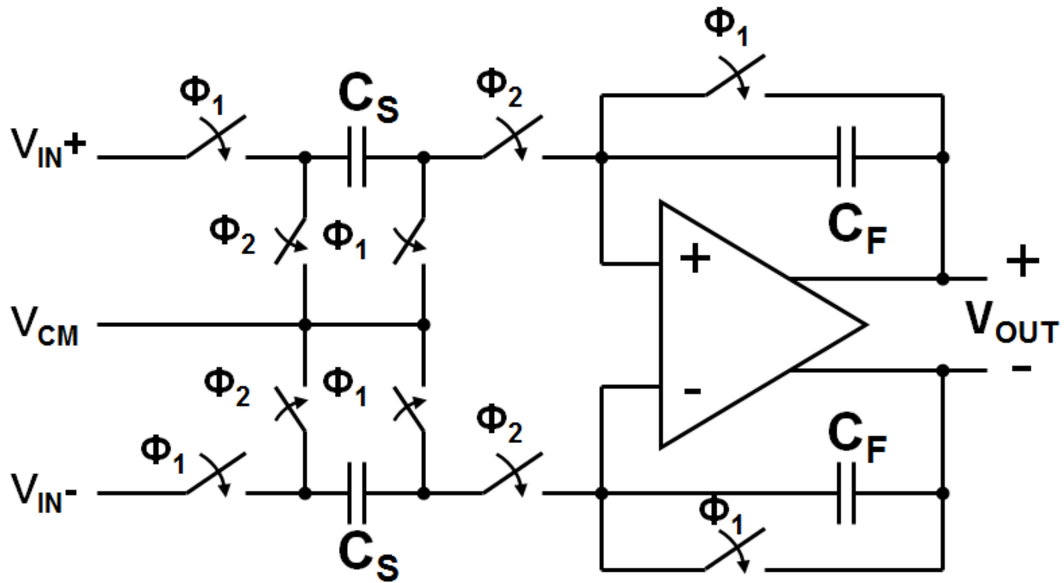


Fig. 108: Differential sample/hold amplifier.

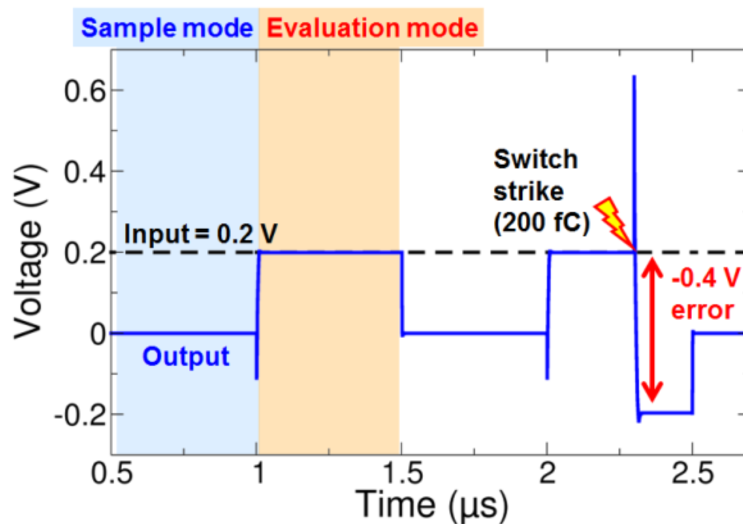


Fig. 109: Single-event transient in nFET SHA with input of 0.2 V and sample rate of 1 MS/s. Charge deposition of 200 fC resulted in -0.4 V sample error.

the virtual short between OTA inputs transfers the charge on the sample capacitors to C_F, amplifying the voltage by a factor of $-C_S/C_F$.

When in evaluation mode, the inputs to the OTA are floating nodes with nothing driving them. This is the vulnerable state of the S/H amplifier, because whatever charge is deposited on the switches connected to the OTA inputs will directly affect the output voltage. Furthermore, this incorrect output will persist until the next sample phase when

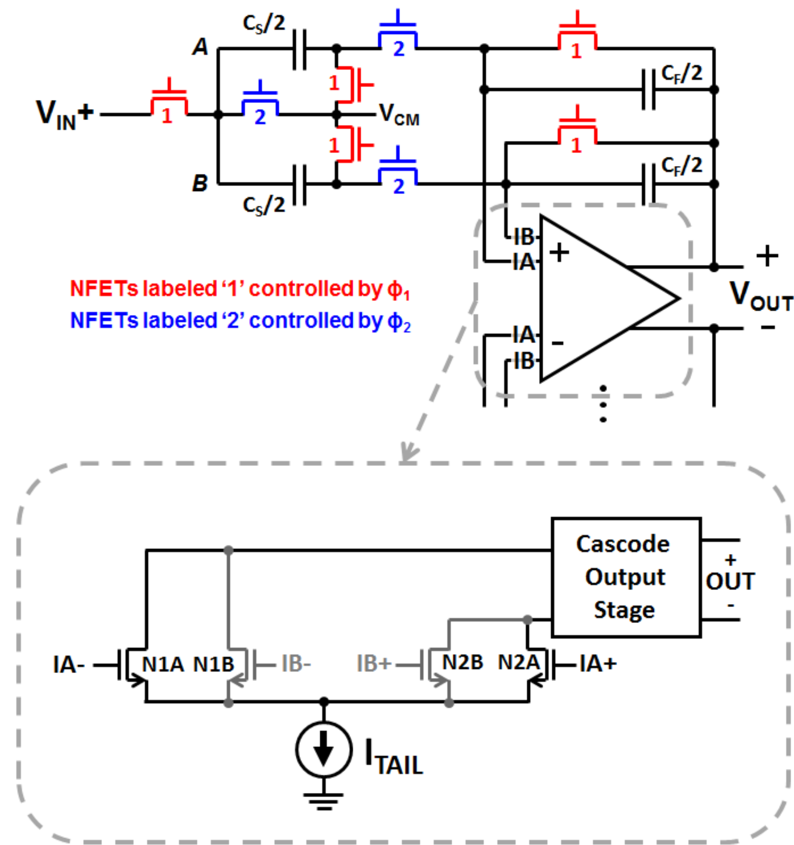


Fig. 110: Schematic showing half of the dual-path S/H amp topology (negative half is identical) and simplified schematic of modified dual-input nFET OTA.

the OTA resets the feedback capacitors. The switches connected to the OTA inputs comprise a significant SE vulnerability that can be mitigated using dual- or quad-path hardening. The simulated output of an S/H amp after being struck by an ion in the evaluation mode is shown in Fig. 109, demonstrating the magnitude and persistence of such SETs.

Before describing the quad-path technique, it is informative to discuss the dual-path scheme. The dual-path hardening technique is illustrated schematically in Fig. 110. The schematic shows half of the SC network and the OTA of an nFET-based S/H amplifier. The ideal switches in Fig. 108 have been replaced with nFETs, and dual paths

have been created—labeled ‘A’ and ‘B’. In each of the dual paths, the sample and feedback capacitors have been halved from the original values (since they effectively operate in parallel), yielding the same total capacitance as the conventional design. The simplified schematic of the OTA demonstrates how the dual-input stage is implemented to support the dual-path SC network. A typical OTA would have a single inverting input transistor and a single non-inverting input transistor, but the dual-path technique intentionally separates each of the original input transistors into A and B halves. The OTA has two inverting—N1A and N1B—and two non-inverting—N2A and N2B—input transistors, with each A/B pair connected in parallel except for the gates.

If a switch connected to an OTA input is struck by an ionizing particle during the evaluation phase, then the n-type diffusion collects electrons, and the voltage at the OTA input decreases, depending on the amount of collected charge. For example, a sufficient voltage drop at the OTA input IA+ will cause the corresponding input transistor N2A to enter the cutoff regime of operation, temporarily disabling the device. However, the feedback of the SC network will increase the voltage at IB+ and increase the current flowing through N2B to maintain the current balance of the differential OTA. Thus, the S/H amplifier’s feedback path is maintained and the output error is mitigated. The level of mitigation is ultimately limited by the offset voltage shift required for N2B to compensate for the cutoff of N2A. For a more in-depth discussion of the dual-path hardening technique, the reader is referred to [97].

As previously mentioned, this method only works if the type of transistor implementing the switch matches the type of input transistor in the OTA. This is demonstrated by considering a single-event on a different type of switch in the circuit of

Fig. 110. If the nFET switches are replaced with pFET switches and one is struck during the evaluation phase, the OTA input voltage will increase as the p-type diffusion collects holes. Since the OTA input transistors have a high transconductance (g_m), even a small increase in voltage will cause a large increase in the current flowing through the effected transistor. If the current through N2A, for instance, increases by a factor greater than two, then there is no way for the dual device N2B to sufficiently decrease current flow to compensate for the increased current. Similarly, if the voltage increase at IA+ is sufficiently large, then N2A will enter the triode regime of operation, creating a low resistance path between the cascode stage and the tail current source, temporarily disabling N2B. Therefore, an nFET-based dual-input OTA can only mitigate single-event sample errors if nFET switches are also used in the SC network. Conversely, a pFET-based dual-input OTA can only mitigate sample errors if pFET switches are used.

Since the maximum output voltage of an nFET switch is ($V_{DD} - V_{TN}$) and the minimum output voltage of a pFET switch is ($V_{SS} + |V_{TP}|$), it is often desirable to connect the two in parallel in a transmission-gate (TG) switch that can pass voltages from V_{SS} to V_{DD}. This is particularly true in advanced CMOS technologies with supply voltages at or below 1 V. However, dual-path hardening cannot be used unless a charge pump is added to the design to obtain full signal swing using only nFETs.

The quad-path hardening technique overcomes this limitation by combining TG switches with a complementary-input-stage OTA (a complementary folded-cascode OTA [111]). Conventional OTAs with a single type of input transistor have limited common-mode input range, while the complementary folded-cascode OTA uses both n-type and p-type input transistors (as shown in Fig. 111) to achieve a rail-to-rail common-mode input

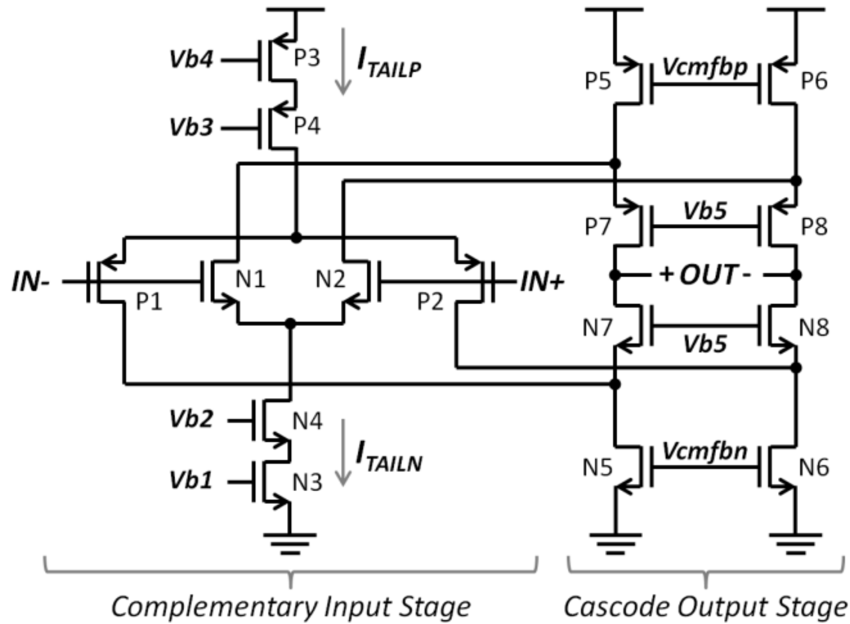


Fig. 111: Schematic of fully-differential complementary folded-cascode operational transconductance amplifier (OTA). The bias circuit that generates Vb1, Vb2, Vb3, Vb4, and Vb5, as well as the two common-mode feedback circuits that generate Vcmfbp and Vcmfbn are not shown.

range. For more details on the OTA design, the reader is referred to Chapter IV Section C. The core concept of the quad-path hardening technique is the use of complementary input paths in addition to the redundant paths of the original dual-path topology. Half of the topology of the quad-path S/H amp is shown in Fig. 112 along with the modified input stage of the quad-input OTA.

The conventional S/H amplifier in Fig. 108 can be transformed to the quad-path design in Fig. 112 in three steps. First, the switches in Fig. 108 are replaced with transmission gates. Second, the dual-path redundancy of Fig. 110 is employed, creating two positive and two negative signal paths with half the original capacitance in each path. A constant total capacitance is maintained, and the number of TG switches is doubled in creating the dual path. The third step is to separate the nFET and pFET components of the TG switches, giving each device type its own signal path; in effect, creating a quad-path topology. The quad paths are labeled 'AP', 'BP', 'AN', and 'BN'. For example,

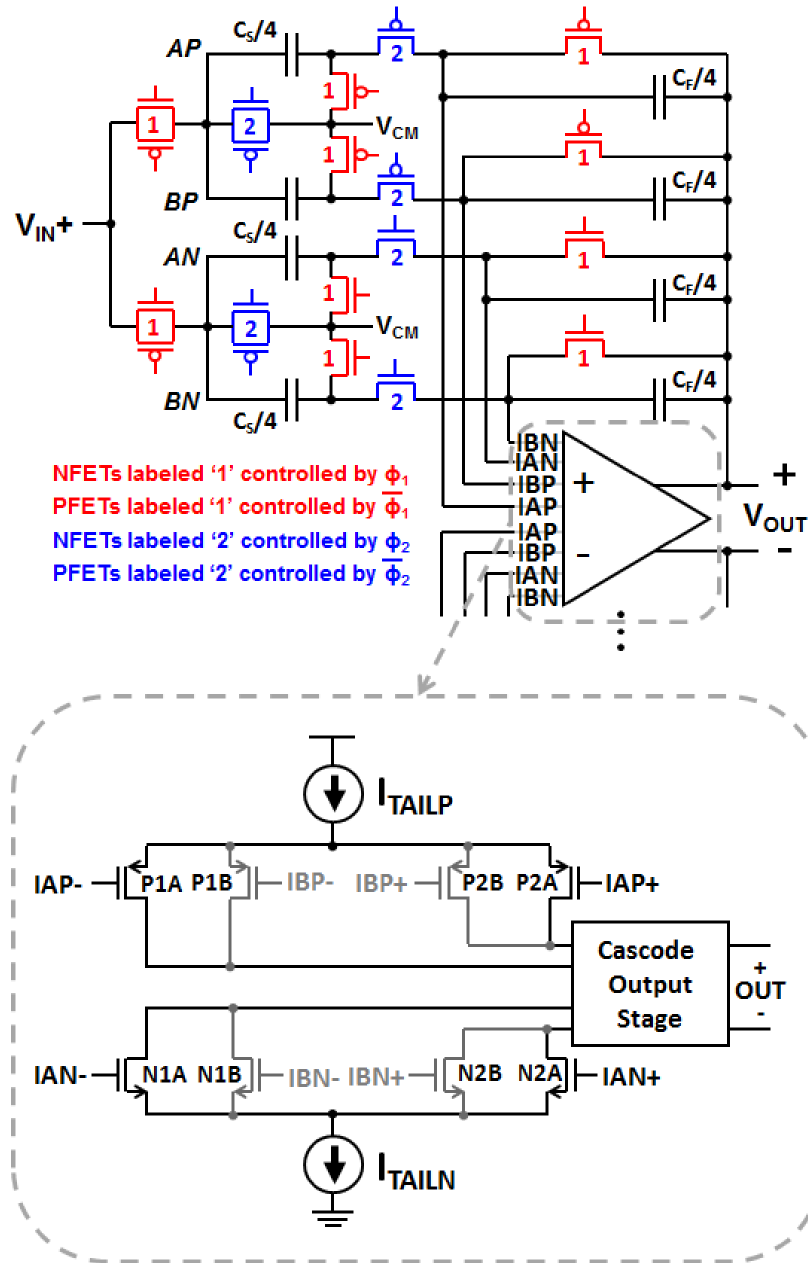


Fig. 112: Schematic showing half of the quad-path S/H amp topology (negative half is identical) and simplified schematic of modified quad-input complementary folded-cascode OTA.

'AP' represents the 'A' half of the p-type paths going to the p-type differential input of the complementary input-stage OTA. It is important to note that this separation of TG transistors is only required for the TGs to the right of the sample capacitors, since the sample switches do not create a floating node, and must remain conventional TGs to

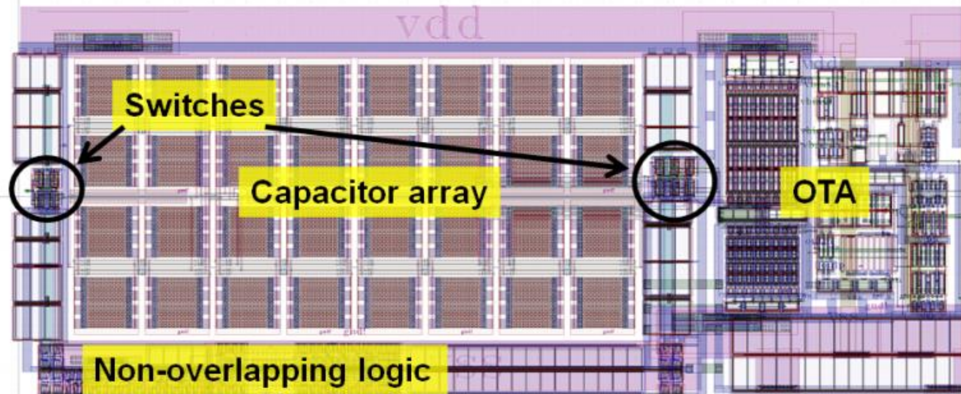
support rail-to-rail input sampling. Compared to a conventional TG S/H amplifier, the quad-path topology doubles the number of switch FETs and quadruples the number of signal paths and capacitors, but the capacitors are quartered to maintain constant total capacitance compared to the original design. Because the n- and p-type signal paths function in parallel, the voltage range of the quad-path topology is identical to that of a single-path TG S/H amplifier.

The quad-input OTA in Fig. 112 is essentially a modified complementary folded-cascode OTA. The main components of the design are the tail current sources, the n- and p-type input transistor pairs, and the cascode output stage (from Fig. 111). The input transistors N1, N2, P1, and P2 of the OTA in Fig. 111 are halved into A and B components, and the gate of each A and B transistor is separated to yield four inverting and four non-inverting inputs in Fig. 112. The quad-input OTA now supports the dual ('A' and 'B') and complementary ('N' and 'P') signal paths of the SC network. It is crucial for the p-type switch signal paths to connect to the p-type OTA inputs and the n-type switch signal paths to connect to the n-type OTA inputs. By matching switch transistor type to input transistor type, the same SE tolerance of the dual-path technique is achieved in the quad-path topology without sacrificing input signal range. As in the original dual-path implementation, if an n-type (p-type) switch is struck, the voltage at the OTA input will decrease (increase), causing the corresponding n-type (p-type) input transistor to decrease its current flow to the output stage (Fig. 112) or even go into cutoff. Due to the feedback in the S/H amp, the dual counterpart of that input transistor will then increase its current to compensate, mitigating the output error.

The quad-path OTA input stage is modified by halving the sizes of the input transistors and separating the gate connections for the quad input paths. Since the input pairs are typically laid out in a symmetric, common-centroid pattern of identical sub-cells to optimize matching, the only change to the layout in implementing the quad-path technique is a different metal routing. The number of capacitors in the SC network is quadrupled in comparing the quad-path S/H amp compared to the baseline design of Fig. 108, but each capacitance value is also quartered in the quad-path design, maintaining the same total capacitance and total capacitor area. Since these capacitors are also typically laid out in a symmetrical pattern of sub-cells for optimal matching, this change primarily affects the routing of the metal lines of capacitors. By maintaining the same total capacitance—the primary limitation on S/H speed—the speed of the S/H amplifier is not affected in any significant manner by the quad-path modifications. However, it is not always possible to divide the switch areas when creating quad paths, since the switches may already have minimum areas in the unhardened design. In comparing the quad-path and conventional designs, the number of switch FETs must be doubled to implement the quad-path scheme. Therefore the total switch area is, at most, doubled compared to the conventional design in Fig. 108. The switches are significantly smaller than the capacitors or the OTA, so the impact of this layout increase is minimal.

In Fig. 113, layout images of a conventional TG S/H amp and a quad-path S/H amp fabricated in a 45-nm process are compared to demonstrate the negligible area impact of the design technique. The total transistor and capacitor area in the conventional layout is 5149 μm^2, compared to 5235 μm^2 in the quad-path layout—a less than 2% area penalty since only the area occupied by switches is doubled. The DC currents of the OTA

(a) Conventional TG S/H amplifier layout



(b) Quad-path S/H amplifier layout

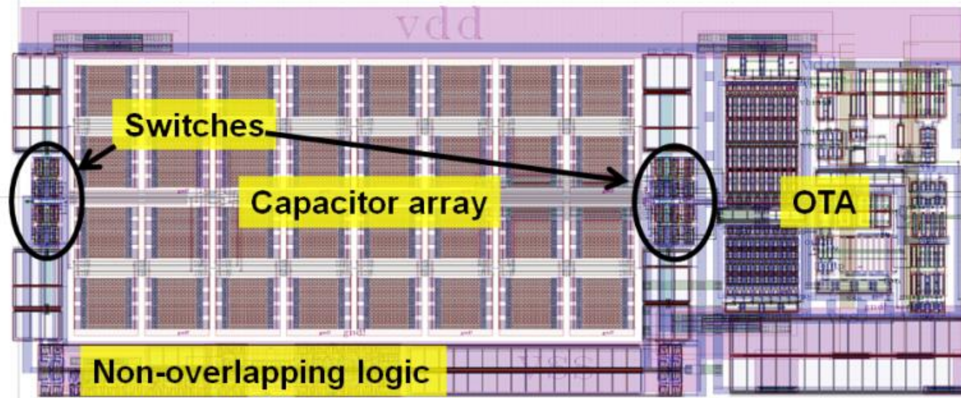


Fig. 113: Layouts of (a) conventional, or baseline, TG S/H amplifier and (b) quad-path S/H amplifier fabricated in 45-nm technology with sub-circuits labeled. Layout images are on same scale.

that dominate the S/H amp power consumption are unaffected by the quad-path modifications, so the technique has a negligible power penalty. As was shown in [97], the quad-input scheme in the OTA has no impact on the noise in the amplifier. The primary penalty of the quad-path technique is the increase in design complexity. The additional switches also increase the amount of charge injection in the S/H amplifier. The differential nature of the circuit mitigates this effect through symmetry, and additional design techniques for decreasing charge injection are well understood [133]–[136].

One of the primary benefits of the quad-path technique over the dual-path technique is the input signal range. For example, when S/H amps were designed in the IBM 45-nm SOI process using 1.8-V transistors, an nFET-based design exhibited a signal range of ±0.96 V, while a TG-based design exhibited a signal range of ±1.44 V—a 50% increase. The main limitation on the signal range of the TG-based S/H amp was the common-mode range of the complementary folded-cascode OTA. While rail-to-rail common-mode input ranges can certainly be achieved with complementary-input OTAs, that full range was not obtained in this particular design.

Table 10: Description of tested S/H circuits.

S/H Amplifier	Switch Type	OTA Input	Description
TG Baseline	Transmission gate	Complementary	Single-path TG S/H
TG dual	Transmission gate	Complementary	Dual-path TG S/H
Quad	Transmission gate	Complementary	Quad-path TG S/H
N Baseline	NFET	NFET	Single-path nFET S/H
N Dual	NFET	NFET	Dual-path nFET S/H

Experimental setup

Five different S/H amps were fabricated in the IBM 45-nm SOI process. Thick-oxide, body-contacted devices were employed in the design in order to use a 1.8-V power supply. The S/H circuits of the test chip are summarized in Table 10. The total sample capacitor and feedback capacitor values were designed to be equal to 500 fF; thus, all the designs perform unity-gain sampling.

Single-event experiments were carried out using the femtosecond pulsed laser facility at the Naval Research Laboratory (NRL). Charge was injected into precise

locations of the tested circuits using the two-photon absorption (TPA) technique. TPA emulates the charge deposition of an ion strike by generating electron-hole pairs in the active areas of circuits in silicon [137]–[140]. The differential signal inputs and the common-mode voltage input (Fig. 108) were connected to 0.9 V, with the chip powered from 1.8 V. The differential outputs of the targeted S/H amplifier were connected to a 2.5-GHz oscilloscope while the circuit was clocked at 50 kHz from a signal generator. Event sequence triggering was used on the oscilloscope to capture the output only when a strike occurred during the vulnerable evaluation phase.

Experimental results

Because the quad-path hardening technique addresses the most sensitive components in the S/H circuit—i.e., the switches—specific switches were targeted using the 3-D scanning system. The physical dimensions of each switch were approximately 2 μm by 0.5 μm, making them fairly small targets. In addition, the switches were SOI transistors, so the sensitive volume was similarly small. Therefore, in order to maximize the efficiency of the available test time, preliminary area scans were used to identify the most sensitive switch in the designs, and that strike location was then used as the main comparison point between designs. The most sensitive differential pair of switches was identified as the switches clocked on the ϕ_2 phase connected between sample capacitors and OTA inputs (Fig. 108, Fig. 110, and Fig. 112). For consistency between designs the switch connected to the inverting OTA input was the worst-case strike location in the five designs.

The point at which a TPA laser pulse deposits charge is specified not only by the location in the circuit layout (i.e., the X-Y coordinates) but by the focal point of the beam in the silicon (the Z coordinate), as well. While X, Y, and Z coordinates can be controlled, the focal point of the beam can also vary across a chip due to various imperfections such as tilt in the mounting of the die or the chip package. Furthermore, non-uniformities in the roughness of the die surface can cause slight variations in charge deposition at different locations on the chip. These factors contribute to the challenge of comparing laser results in multiple circuits.

To account for variations of charge deposition in the sensitive volumes of the SOI transistors, the laser focus (the Z coordinate) was moved into and out of the silicon to identify the point of maximum charge deposition at the worst-case strike location (X-Y coordinates). The focal point of the beam was then scanned ±2.5 μm in 0.5-μm steps from the point of maximum charge deposition, capturing 10 SETs at each location. The measured SETs did not vary significantly in this 5-μm range. By averaging the amplitudes of the 110 captured SETs, the mean error amplitude was computed for the most sensitive switch in the design. Comparing the circuits in this manner yielded results that are less dependent on finding a specific 3-D location of maximum charge deposition in each S/H circuit, which is challenging given the previously mentioned imperfections of a chip. Since each switch is composed of an nFET and a pFET in the TG circuits, these measurements were performed on both devices. In the dual- and quad-path designs, the most-sensitive switch has an identical dual counterpart, but it was confirmed that the response was the same for both switches, as expected. In order to compare the different designs, the measurement of the average response of the most sensitive switch was

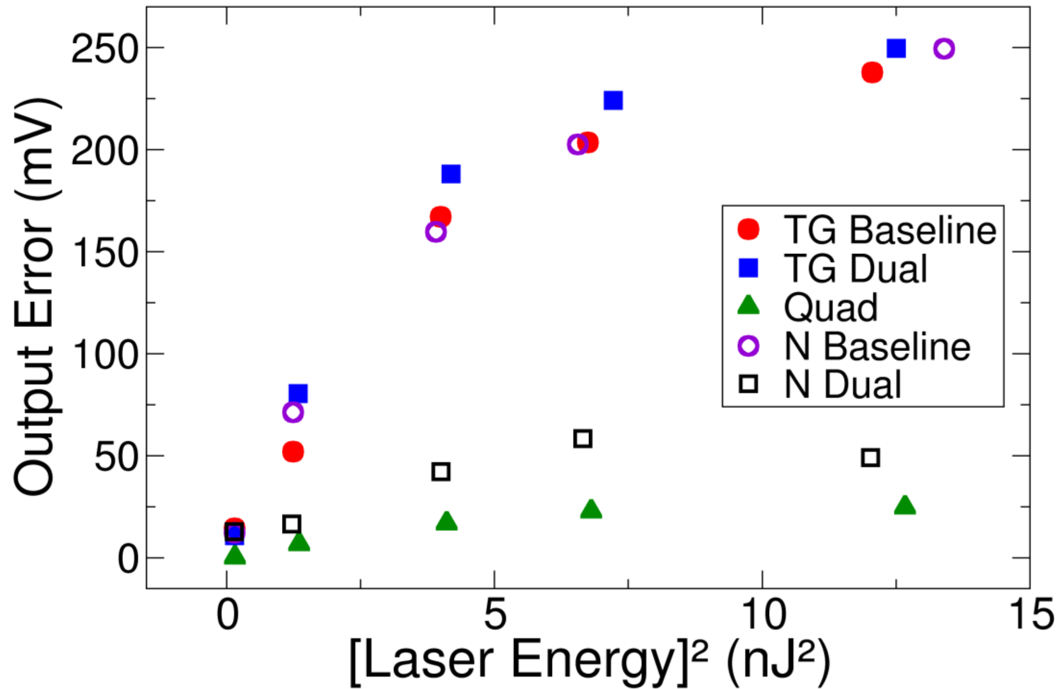


Fig. 114: Average sample error generated by strikes on most sensitive nFET switch.

performed on all five S/H amplifiers using a range of laser pulse energies from approximately 0.3 to 3.5 nJ.

The SE-induced output errors (or sample errors) generated in the most sensitive nFET switch of each design are plotted in Fig. 114 as a function of laser energy squared, which correlates linearly with charge deposition. The labels in the legend correspond to the S/H circuit names in Table 10. As expected the TG baseline, TG dual, and N baseline designs track each other fairly closely. These circuits exhibit a strong dependence on the square laser energy (or charge deposition) with average sample errors as large as 250 mV. Conversely, the sample errors in the quad-path and N dual S/H amps essentially saturate at much lower values, showing a rather weak dependence on charge deposition. The maximum error in the dual-path nFET S/H amplifier was approximately 59 mV, and the maximum error in the quad-path design was on the order of 25 mV—a 90% decrease from the TG baseline. The significant reduction in sample errors in the quad-path circuit

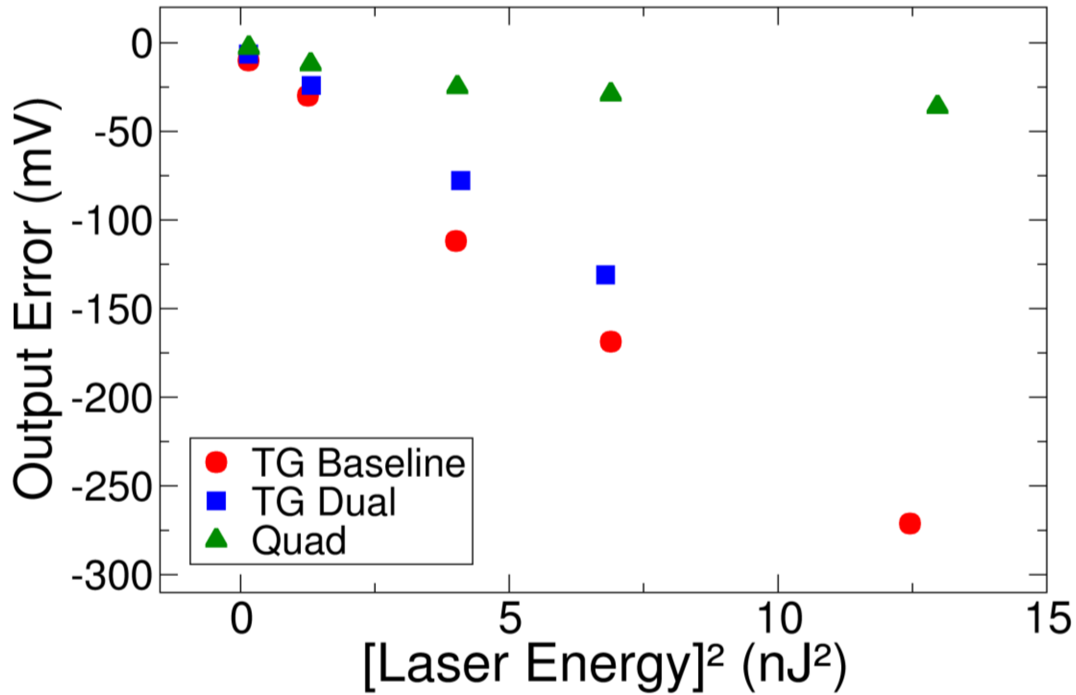


Fig. 115: Average sample error generated by strikes on most sensitive pFET switch.

compared to the TG dual-path circuit reiterates the importance of matching switch type to OTA input type. In the TG dual-path S/H amp, the n- and p-type signal paths were connected together to n- and p-type input FETs in the OTA, preventing the design from benefitting from the dual-path topology.

The sample errors observed in the quad-path design were smaller than in the dual-path nFET design because of the higher number of separate OTA input transistors. In the dual-path topology there are only A and B input transistors, so when a switch is struck one of two input transistors is disabled; only half of the input stage is functional following the strike. In the quad-path topology there are A and B as well as N and P input transistors, so when a switch is struck one of four input transistors is disabled; three quarters of the input stage remains functional following the strike. By further diluting the effect of the SET, the quad-path topology yields smaller sample errors than the dual-path

topology. This effect was discussed in [98], but it was in the context of expanding the dual-path A and B signal path into A, B, C, and D paths of the same transistor type—doing nothing to enhance the signal range as the proposed quad-path technique does.

The average output errors in the most sensitive pFET switch of each S/H amplifier are plotted in Fig. 115. By striking the pFET switch instead of the nFET switch, the polarity of the sample errors was reversed. As with the nFETs, the TG baseline and TG dual-path designs exhibited strong trends with charge deposition, while the quad-path design did not. The largest sample error in the quad-path S/H amp was 36 mV, an 87% reduction from the 271-mV sample error in the baseline.

Since the S/H circuit is a fundamental block in AMS systems, it is informative to contextualize the TPA results in the framework of a theoretical ADC design. Assuming the ADC has a full-scale range of ±1 V and 5 bits of resolution, the observed sample errors may be reported in least significant bits (LSBs), with 1 LSB = 62.5 mV. In the TG baseline S/H amp, the maximum error of 271 mV is equivalent to 4.34 LSBs, resulting in a significant conversion error. In the quad-path S/H amp, the maximum error of 36 mV is equivalent to 0.58 LSBs, which is just above the quantization error of the ADC, indicating a mild conversion error. The maximum error observed in the dual nFET S/H amp corresponds to 0.94 LSBs. This analysis demonstrates how dramatically the quad-path hardening technique can enhance the SET tolerance of an AMS system.

In conclusion, quad-path hardening can be applied to any differential switched-capacitor circuit to provide a dramatic reduction in single-event vulnerability with negligible performance penalty. Laser tests have shown that SE-induced sample errors are reduced by up to 90% in a quad-path hardened sample-and-hold amplifier, compared

to a conventional design. The quad-path RHBD technique provides more design flexibility than dual-path hardening by allowing the use of complementary switches, which support rail-to-rail signal swings. Furthermore, quad-path hardening provides excellent SE tolerance with less than 2% area penalty and negligible speed and power penalties in an analog/mixed-signal system. The design specs and results of the laser experiment are summarized in Table 11.

Table 11: Comparison of 45-nm SHA designs.

Specification	TG Baseline	TG Dual-path	Quad-path	NFET Baseline	NFET Dual-path
Signal range (V)	± 1.44	± 1.44	± 1.44	± 0.96	± 0.96
Max. sample rate (MS/s)	24	24	24	19	19
Average power @ 1 MS/s (mW)	1.2	1.2	1.2	1.0	1.1
Active + capacitor area (μm^2)	5149	5235	5235	4803	4835
Largest measured SET (mV)	354	317	54	318	70

C. Conclusion

In this chapter mitigation schemes for total-dose and single-event effects were proposed for discrete-time circuits—switched-capacitor circuits in particular. A switched-capacitor DTMOST voltage reference was presented that generated a voltage using a single DTMOST. By eliminating DTMOST mismatch, the op amp offset voltage was the most TID-sensitive circuit parameter. As chopper stabilization is suitable for offset cancellation in continuous-time circuits, auto-zeroing is suitable for offset cancellation in

discrete-time circuits. A system-level modification of the SC reference architecture that auto-zeroes the op amp offset voltage was proposed. By sampling and canceling the offset voltage, the reference was hardened to TID effects in the op amp. However, there is still future work to be done in this area regarding the biasing of the single DTMOST. The addition of a capacitor, switches, and a phase of operation to support auto-zeroing was a system-level change that can be implemented in any SC circuit that is sensitive to radiation-induced offset voltage shifts.

The high-impedance nature of switched-capacitor circuits makes them significantly more sensitive to SEE than TID. The quad-path hardening technique for SC circuits was presented in this chapter with experimental laser data. The technique is essentially a generalization of multi-path hardening in which dual redundancy and n- and p-type isolation are applied. By following the guidelines of this technique SC circuits using transmission-gate switches can be SE-hardened while maintaining a wide signal range—a critical factor in the front-end blocks of low-voltage AMS systems.

CHAPTER VII

CONCLUSIONS

In this dissertation analyses and mitigation schemes for radiation effects in both continuous- and discrete-time analog circuits have been presented. The cumulative effects of total ionizing dose and the transient effects of single events were both considered. The voltage reference was used as a case study for continuous-time circuits. For discrete-time circuits a switched-capacitor-based voltage reference was used as a case study of dose effects, and a sample/hold amplifier was used as a case study of single-event effects.

The presented system-level hardening techniques advance the state of the art of TID-hardened AMS circuits. Previously, RHBD analog design relied heavily on the radiation robustness of modern CMOS processes. Designs were simply TID-hardened by implementing edgeless-layout transistors and guard bands to mitigate leakage effects, while threshold voltage shifts were largely ignored because of the resilience of thin gate oxides. The research presented in this dissertation combines circuit analysis with measurements to demonstrate that—despite the resilience of modern CMOS—device mismatch ultimately limits the TID tolerance of analog circuits. Due to the ubiquity of matched-pair transistors in analog design, these analyses and the accompanying mitigation schemes have an exceptionally wide impact in the field of analog RHBD.

This work presents the first in-depth demonstration of the impact of chopper stabilization on the TID response of continuous-time analog circuits. Implementing a

chopper scheme in a circuit attenuates—rather than amplifies—the effects of device mismatch, which were shown to fundamentally limit the TID response. Using this design technique a novel voltage reference architecture subtracting two PTAT currents was also introduced. The circuit combines system-level chopper stabilization with the differential nature of the circuit to mitigate all TID-induced degradation as mismatch. The proposed circuit demonstrates a new approach for designing TID-hardened analog circuits without relying directly on the robustness of a particular process.

In addition to the chopper-stabilized current mirror, a new class of TID-hardened resistive current mirrors was introduced. The use of a single current source with the current distributed by resistors eliminates the effect of radiation-induced mismatch in current mirrors. Combining this scheme with negative feedback reduces the TID-induced degradation to a negligible level. The simplicity and flexibility of this design technique give it a wide range of applications in analog RHBD.

The presented work in the discrete-time domain is also novel in presenting the switched-capacitor voltage reference as a potential TID-hardened topology. The inherent mismatch mitigation of the switched-capacitor circuit can be further enhanced with auto-zeroing. The fundamental dynamic matching of the SC topology combined with auto-zeroing constitutes a novel system-level approach to hardening SC circuits to total dose effects.

The main contribution of this work in the discrete-time domain is the quad-path hardening technique. While the technique does improve upon the signal range and single-event mitigation of the original dual-path technique, the greater impact is that it fundamentally presents a generalization of multi-path hardening in SC circuits. The

sample/hold case study provides a guide map to analog designers for mitigating single events in a wide variety of SC circuits. It is demonstrated that by implementing analog redundancy along with the separation of complementary (n- and p-type) signal paths, analog designers have the flexibility of using complementary switches, which enable rail-to-rail signal range. This ultimately ensures that multi-path hardening continues to be beneficial as the voltage headroom of CMOS circuits continues to scale down.

The mitigation schemes presented in this dissertation are summarized by the following list of RHBD guidelines for AMS circuits:

- It is important to minimize the closed-loop gain of precision circuits, when possible. Total dose alters device mismatch and offset voltages, which both have an impact on the output that depends on the system gain. In voltage reference design this means selecting the bias points of the reference devices that require minimal amplification to achieve first-order tempco cancellation.
- If small-signal analysis of a circuit reveals sensitivity to mismatch in a current mirror, then the effect of the mismatch can be mitigated using a resistive current mirror. Like a typical current mirror, the resistors can be sized to provide equal or scaled currents that will all be affected identically by the common current source. The effects of radiation-induced degradation can be further reduced with negative feedback.
- Chopper stabilization can be used to attenuate the effects of offset voltages and mismatch in matched pairs. The most common application of this is a differential amplifier like an op amp, but it can also be applied to other types of matched pairs like reference devices or current mirrors. The frequency of the chopping depends on the initial bandwidth of the system. In a system like a voltage reference that requires

DC precision, the chopping frequency must be fairly low (<1 MHz) to accommodate high DC gain and low bandwidth. However, AC amplifier circuits with less stringent DC gain requirements fundamentally have larger bandwidths, so much higher chopping frequencies are possible. Ultimately the filtering required with chopper stabilization will limit the bandwidth, but that bandwidth limitation is directly related to the initial bandwidth of the system.

- The low-pass filtering required for chopper stabilization effectively attenuates ASETs generated in the analog circuitry. Due to the typical range of chopper frequencies (relative to digital SET pulse widths) temporal filtering can be combined with TMR can be used to harden the clock generation and distribution.
- The threshold and leakage effects of total dose must be analyzed in the chopper switches of a chopper-stabilized system. Typically leakage is less problematic due to the small voltage drops across chopper switches. The effect of threshold voltage shifts on the voltage drop across a current-carrying switch can be mitigated by sufficiently increasing W/L and/or decreasing the bias currents. In systems where chopping is applied to high-impedance nodes with negligible current, the effects of V_T shifts are negligible.
- In designing a small-value (<10 kΩ), programmable resistor, a parallel trimming scheme offers better mitigation of V_T shifts in the switches than a series trimming scheme. Series trimming offers better linearity but requires large W/L switches to mitigate V_T shifts. Such a scheme is most suitable for higher-value resistances. The parallel scheme is slightly more susceptible to sidewall leakage, but this can be mitigated with edgeless layout if necessary.

- In a mixed-voltage interface between thin- and thick-oxide circuits, biasing the thick-oxide circuit with a voltage from the thin-oxide circuit allows the more TID-sensitive thick-oxide circuit to maintain performance by compensating for its own parametric shifts. The fundamental concept is to leverage the lower radiation sensitivity of the thin-oxide circuit to enhance the thick-oxide circuit.
- ASETs can be mitigated in a first-order voltage reference by separating the positive tempco generation from the tempco cancellation subcircuits. The frequency-compensated op amp between the two stages effectively filters out ASETs generated in the positive tempco generator. In addition, separating these subcircuits allows for them to be more easily hardened with charge sharing techniques DCC and SNACC, improving the overall system response.
- Offset and mismatch effects can be mitigated in switched-capacitor circuits using dynamic matching and auto-zeroing. Dynamic matching in a voltage reference uses a single reference device to generate multiple voltages, thereby matching the TID-induced voltage shifts. The sampling and cancelling of offset voltage performed by auto-zeroing is easily incorporated into the multi-phase operation of discrete-time circuits.
- ASETs can be mitigated in switched-capacitor circuits through multi-path hardening. Redundant, parallel signal paths allow the circuit to compensate for a strike on one of the signal paths. The signal range of a transmission-gate switch can be achieved with this scheme by using analog redundancy along with separate n- and p-type signal paths—resulting in A and B signal paths of both n- and p-type transistors. This device type separation must be maintained in both the switching network and the input stage

of the op amp required by the circuit. It is important to lay out the redundant signal paths such that simultaneous charge collection does not occur.

The radiation hardening techniques proposed in this dissertation can be used to enhance the TID and SEE tolerance of AMS systems. Furthermore, the analyses used to demonstrate radiation vulnerabilities can be generally used to identify vulnerabilities in analog circuits, so that the appropriate mitigation scheme may be employed. Although simply hardening the voltage reference in an AMS system can greatly enhance the radiation tolerance of the overall system, the system-level nature of the presented hardening techniques promotes portability to other circuits in the system. In addition, the RHBD techniques do not rely on the responses or mechanisms of a specific process. Therefore, the design techniques and guidelines in this dissertation will continue to be effective tools in the field of analog RHBD as CMOS processes continue to scale.

REFERENCES

[1] J. R. Schwank, "Total-dose effects in MOS devices," *NSREC Short Course*, 2002.

[2] R. Lacoe, "CMOS Scaling: Design Principles and Hardening-by-Design Methodology," *NSREC Short Course*, 2003.

[3] H. J. Barnaby, "Total-dose effects in modern integrated circuits," *NSREC Short Course*, 2005.

[4] B. G. Rax, A. H. Johnston, and C. I. Lee, "Proton damage effects in linear integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, Dec. 1998.

[5] A. H. Johnston and R. E. Plaag, "Models for Total Dose Degradation of Linear Integrated Circuits," *IEEE Trans. Nucl. Sci.*, vol. 34, no. 6, 1987.

[6] A. H. Johnston, G. M. Swift, and B. G. Rax, "Total dose effects in conventional bipolar transistors and linear integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, Dec. 1994.

[7] R. L. Pease, "Total ionizing dose effects in bipolar devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, Jun. 2003.

[8] A. H. Johnston, B. G. Rax, and D. Thorbourn, "Total Dose Effects in Op-Amps With Compensated Input Stages," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, Aug. 2008.

[9] E. H. Snow, A. S. Grove, and D. J. Fitzgerald, "Effects of ionizing radiation on oxidized silicon surfaces and planar devices," *Proceedings of the IEEE*, vol. 55, no. 7, 1967.

[10] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation Effects in MOS Capacitors with Very Thin Oxides at 80degK," *IEEE Trans. Nucl. Sci.*, vol. 31, no. 6, 1984.

[11] A. H. Johnston, "Radiation effects in advanced microelectronics technologies," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, Jun. 1998.

[12] M. Manghisoni, L. Ratti, V. Re, and V. Speziali, "Radiation hardness perspectives for the design of analog detector readout circuits in the 0.18-µm CMOS generation," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, Dec. 2002.

[13] M. Manghisoni, L. Ratti, V. Re, V. Speziali, G. Traversi, and A. Candelori, "Comparison of ionizing radiation effects in 0.18 and 0.25 µm cmos technologies for analog applications," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, Dec. 2003.

[14] V. Re, M. Manghisoni, L. Ratti, V. Speziali, and G. Traversi, "Total ionizing dose effects on the analog performance of a 0.13-μm CMOS technology," presented at the Radiation Effects Data Workshop, 2005.

[15] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[16] A. H. Johnston, R. T. Swimm, G. R. Allen, and T. F. Miyahira, "Total Dose Effects in CMOS Trench Isolation Regions," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, Aug. 2009.

[17] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, Dec. 2005.

[18] B. Jun, R. M. Diestelhorst, M. Bellini, G. Espinel, A. Appaswamy, A. P. G. Prakash, J. D. Cressler, D. Chen, R. D. Schrimpf, D. M. Fleetwood, M. Turowski, and A. Raman, "Temperature-Dependence of Off-State Drain Leakage in X-Ray Irradiated 130 nm CMOS Devices," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[19] M. McLain, H. J. Barnaby, K. E. Holbert, R. D. Schrimpf, H. Shah, A. Amort, M. Baze, and J. Wert, "Enhanced TID Susceptibility in Sub-100 nm Bulk CMOS I/O Transistors and Circuits," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[20] A. H. Johnston, "The Application of Operational Amplifiers to Hardened Systems," *IEEE Trans. Nucl. Sci.*, vol. 24, no. 6, 1977.

[21] A. H. Johnston and C. A. Lancaster, "A Total Dose Homogeneity Study of the 108a Operational Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 26, no. 6, 1979.

[22] C. I. Lee and A. H. Johnston, "Comparison of total dose effects on micropower op-amps: bipolar and CMOS," presented at the Radiation Effects Data Workshop, 1998.

[23] A. H. Johnston and B. G. Rax, "Failure Modes and Hardness Assurance for Linear Integrated Circuits in Space Applications," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, Aug. 2010.

[24] H. J. Barnaby, R. D. Schrimpf, A. L. Sternberg, V. Berthe, C. R. Cirba, and R. L. Pease, "Proton radiation response mechanisms in bipolar analog circuits," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, Dec. 2001.

[25] B. G. Rax, A. H. Johnston, and T. Miyahira, "Displacement damage in bipolar linear integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, Dec. 1999.

[26] C. I. Lee, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects In 12-bit Successive-approxmation Analog-to-digital Converters," presented at the Radiation Effects Data Workshop, 1993.

[27] J. R. Srour and K. Y. Chiu, "MOS Hardening Approaches for Low-Temperature Applications," *IEEE Trans. Nucl. Sci.*, vol. 24, no. 6, 1977.

[28] J. M. McGarrity, "Considerations for Hardening MOS Devices and Circuits for Low Radiation Doses," *IEEE Trans. Nucl. Sci.*, vol. 27, no. 6, 1980.

[29] H. Hatano, "Radiation hardened high performance CMOS VLSI circuit designs," *IEEE Proceedings on Circuits, Devices, and Systems*, vol. 139, no. 3, Jun. 1992.

[30] H. Hatano and K. Doi, "Radiation-Tolerant High-Performance CMOS VLSI Circuit Design," *IEEE Trans. Nucl. Sci.*, vol. 32, no. 6, 1985.

[31] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, Dec. 1998.

[32] D. R. Williams and N. W. Van Vonno, "Two Radiation-Hardened Analog Multiplexers," *IEEE Trans. Nucl. Sci.*, vol. 30, no. 6, 1983.

[33] R. Lacoe, "Designing Radiation Hardened CMOS Microelectronic Components at Commercial Foundries: Space and Terrestrial Radiation Environments and Device and Circuit Techniques to Mitigate Radiation Effects," in *IEEE International Integrated Reliability Workshop Final Report*, 2005.

[34] D. R. Alexander, "Design Issues for Radiation Tolerant Microcircuits for Space," *NSREC Short Course*, 1996.

[35] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Floria, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, Dec. 1999.

[36] R. C. Lacoe, J. V. Osborn, R. Koga, S. Brown, and D. C. Mayer, "Application of hardness-by-design methodology to radiation-tolerant ASIC technologies," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, Dec. 2000.

[37] R. C. Lacoe, D. Mayer, and E. King, "Reliable and hardened-by-design (RHBD) components for space," presented at the Design Hardening Workshop, Albuquerque, NM, 2002.

[38] R. N. Nowlin, J. Bailey, R. Turfler, and D. R. Alexander, "A total-dose hardening-by-design approach for high-speed mixed-signal CMOS integrated circuits," *Int. J. High Speed Electronics*, vol. 14, no. 2, Jun. 2004.

[39] C. L. Champion and G. S. La Rue, "Accurate SPICE models for CMOS analog radiation-hardness-by-design," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, Dec. 2005.

[40] R. N. Nowlin, S. R. McEndree, A. L. Wilson, and D. R. Alexander, "A new total-dose-induced parasitic effect in enclosed-geometry transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, Dec. 2005.

[41] Z. Zhou, I. Horowitz, and G.S. La Rue, "Design of a radiation-hard DDFS," presented at the IEEE Workshop on Microelectronics and Electron Devices, 2005.

[42] B. Jun, A. K. Sutton, R. M. Diestelhorst, G. J. Duperon, J. D. Cressler, J. D. Black, T. Haeffner, R. A. Reed, M. L. Alles, R. D. Schrimpf, D. M. Fleetwood, and P. W. Marshall, "The Application of RHBD to n-MOSFETs Intended for Use in Cryogenic-Temperature Radiation Environments," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[43] N. D. Hindman, Z. Wang, L. T. Clark, and D. R. Allee, "Experimentally Measured Input Referred Voltage Offsets and Kickback Noise in RHBD Analog Comparator Arrays," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[44] A. R. Jones, D. O'Connor, E. Thiemann, V. A. Drake, G. Newcomb, N. White, D. D. Aalami, H. L. Clark, R. L. Ladbury, B. von Przewoski, S. Dooley, S. Finkelstein, P. Haskins, V. Wei Hsu, B. Kirby, T. Reese, and P. Soto Hoffmann, "Radiation Testing a Very Low-Noise RHBD ASIC Electrometer," presented at the Radiation Effects Data Workshop, 2010.

[45] W. J. Snoeys, T. A. P. Gutierrez, and G. Anelli, "A new NMOS layout structure for radiation tolerance," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 4, Aug. 2002.

[46] R. C. Lacoe, J. V. Osborn, D. C. Mayer, S. Brown, and J. Gambles, "Total-dose tolerance of the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-µm CMOS process," presented at the Radiation Effects Data Workshop, 2001.

[47] E. Vilella and A. Diéguez, "Design of a Bandgap Reference Circuit with Trimming for Operation at Multiple Voltages and Tolerant to Radiation in 90nm CMOS Technology," presented at the IEEE Computer Society Annual Symposium on VLSI, 2010.

[48] P. C. Adell, R. D. Schrimpf, W. T. Holman, J. L. Todd, S. Caveriviere, R. R. Cizmarik, and K. F. Galloway, "Total dose effects in a linear Voltage regulator," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, Dec. 2004.

[49] J. Y. Ahn, W. T. Holman, R. D. Schrimpf, K. F. Galloway, D. A. Bryant, P. Calvel, and M.-C. Calvet, "Design issues for a radiation-tolerant digital-to-analog converter in a commercial 2.0-µm BiCMOS process," presented at the Radiation and Its Effects on Components and Systems Conference, 1997.

[50] B. G. Rax, C. I. Lee, and A. H. Johnston, "Degradation of precision reference devices in space environments," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, Dec. 1997.

[51] "LTZ1000 data sheet." Linear Technology Corporation, Milpitas, CA.

[52] F. J. Franco, Y. Zong, J. A. Agapito, and A. H. Cachero, "Radiation effects on XFET voltage references," presented at the Radiation Effects Data Workshop, 2005.

[53] R. J. Reay, E. H. Klaassen, G. T. A. Kovacs, "A Micromachined Low-Power Temperature-Regulated Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, Dec. 1995.

[54] E. H. Klaassen, "Micromachined Instrumentation Systems," Ph. D. Dissertation, Dept. of Electrical Engineering, Stanford University, May 1996.

[55] R. M. Chavez, B. G. Rax, L. Z. Scheick, and A. H. Johnston, "Total ionizing dose effects in bipolar and BiCMOS devices," presented at the Radiation Effects Data Workshop, 2005.

[56] V. Ramachandran, B. Narasimham, D. M. Fleetwood, R. D. Schrimpf, W. T. Holman, A. F. Witulski, R. L. Pease, G. W. Dunham, J. E. Seiler, and D. G. Platteter, "Modeling Total-Dose Effects for a Low-Dropout Voltage Regulator," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[57] A. T. Kelly, P. C. Adell, A. F. Witulski, W. T. Holman, R. D. Schrimpf, and V. Pouget, "Total Dose and Single Event Transients in Linear Voltage Regulators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, Aug. 2007.

[58] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers, P. Timmer, "A Radiation Hard Bandgap Reference Circuit in a Standard 0.13 μm CMOS Technology," *IEEE Trans. Nucl. Sci*, vol. 54, no. 6, Dec. 2007.

[59] A.-J. Annema, "Low-power bandgap references featuring DTMOSTs," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, Jul. 1999.

[60] V. Ferlet-Cavrois, P. Paillet, O. Musseau, J. L. Leray, O. Faynot, C. Raynaud, and J. L. Pelloie, "Total dose behavior of partially depleted SOI dynamic threshold voltage MOS (DTMOS) for very low supply voltage applications (0.6-1 V)," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 3, Jun. 2000.

[61] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and Chenming Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. on Electron Devices*, vol. 44, no. 3, Mar. 1997.

[62] L. W. Massengill, "SEU Modeling and Prediction Techniques," *NSREC Short Course*, 1993.

[63] P. E. Dodd, "Basic Mechanisms for Single-Event Effects," *NSREC Short Course*, 1999.

[64] M. P. Baze and S. P. Buchner, “Attenuation of single event induced pulses in CMOS combinational logic,” *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, Dec. 1997.

[65] D. G. Mavis and P. H. Eaton, “Soft error rate mitigation techniques for modern microcircuits,” in *International Reliability Physics Symposium Proceedings*, 2002.

[66] T. L. Turflinger, “Single-event effects in analog and mixed-signal integrated circuits,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, Apr. 1996.

[67] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, “Analysis of single-event transients in analog circuits,” *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, Dec. 2000.

[68] Y. Boulghassoul, L. W. Massengill, T. L. Turflinger, and W. T. Holman, “Frequency domain analysis of analog single-event transients in linear circuits,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, Dec. 2002.

[69] M. W. Savage, J. L. Titus, T. L. Turflinger, R. L. Pease, and C. Poivey, “A comprehensive analog single-event transient analysis methodology,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, Dec. 2004.

[70] A. V. Kauppila, G. L. Vaughn, J. S. Kauppila, and L. W. Massengill, “Probabilistic Evaluation of Analog Single Event Transients,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[71] B. D. Olson, W. T. Holman, L. W. Massengill, and B. L. Bhuva, “Evaluation of Radiation-Hardened Design Techniques Using Frequency Domain Analysis,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, Dec. 2008.

[72] R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. LaLumondiere, S. J. Hansel, K. B. Crawford, and W. R. Crain, “Observation of single event upsets in analog microcircuits,” *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, Dec. 1993.

[73] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, Y. Boulghassoul, H. J. Barnaby, S. Buchner, R. L. Pease, and J. W. Howard, “Effect of amplifier parameters on single-event transients in an inverting operational amplifier,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 3, Jun. 2002.

[74] P. C. Adell, R. D. Schrimpf, W. T. Holman, J. Boch, J. Stacey, P. Ribero, A. Sternberg, and K. F. Galloway, “Total-dose and single-event effects in DC/DC converter control circuitry,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, Dec. 2003.

[75] L. Najafizadeh, S. D. Phillips, K. A. Moen, R. M. Diestelhorst, M. Bellini, P. K. Saha, J. D. Cressler, G. Vizkelethy, M. Turowski, A. Raman, and P. W. Marshall, “Single Event Transient Response of SiGe Voltage References and Its Impact on the Performance of Analog and Mixed-Signal Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, Dec. 2009.

[76] O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, and J. R. Ahlbin, “Design Techniques to Reduce SET Pulse Widths in Deep-Submicron Combinational Logic,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[77] Y. Boulghassoul, P. C. Adell, J. D. Rowe, L. W. Massengill, R. D. Schrimpf, and A. L. Sternberg, “System-level design hardening based on worst-case ASET Simulations,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, Oct. 2004.

[78] R. W. Blaine, S. E. Armstrong, J. S. Kauppila, N. M. Atkinson, B. D. Olson, W. T. Holman, and L. W. Massengill, “RHBD Bias Circuits Utilizing Sensitive Node Active Charge Cancellation,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, Dec. 2011.

[79] T. Calin, M. Nicolaidis, and R. Velazco, “Upset hardened memory design for submicron CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, Dec. 1996.

[80] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, “Charge Collection and Charge Sharing in a 130 nm CMOS Technology,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[81] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf, and L. W. Massengill, “Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[82] B. D. Olson, O. A. Amusan, S. Dasgupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, and D. R. Ball, “Analysis of Parasitic PNP Bipolar Transistor Mitigation Using Well Contacts in 130 nm and 90 nm CMOS Technology,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, Aug. 2007.

[83] J. R. Ahlbin, N. M. Atkinson, M. J. Gadlage, N. J. Gaspard, B. L. Bhuva, T. D. Loveless, E. X. Zhang, L. Chen, and L. W. Massengill, “Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, Dec. 2011.

[84] N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, B. L. Bhuva, T. D. Loveless, and L. W. Massengill, “Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, Dec. 2011.

[85] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, J. R. Ahlbin, R. A. Reed, and M. W. McCurdy, “Mitigation Techniques for Single-Event-Induced Charge Sharing in a 90-nm Bulk CMOS Process,” *IEEE Trans. on Device and Materials Reliability*, vol. 9, no. 2, Jun. 2009.

[86] O. A. Amusan, M. C. Casey, B. L. Bhuva, D. McMorrow, M. J. Gadlage, J. S. Melinger, and L. W. Massengill, "Laser Verification of Charge Sharing in a 90 nm Bulk CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, Dec. 2009.

[87] O. A. Amusan, L. W. Massengill, M. P. Baze, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, and J. D. Black, "Single Event Upsets in Deep-Submicrometer Technologies Due to Charge Sharing," *IEEE Trans. on Device and Materials Reliability*, vol. 8, no. 3, Sep. 2008.

[88] B. Mossawir, I. R. Linscott, U. S. Inan, J. L. Roeder, J. V. Osborn, S. C. Witczak, E. E. King, and S. D. LaLumondiere, "A TID and SEE Radiation-Hardened, Wideband, Low-Noise Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[89] A. T. Kelly, P. R. Fleming, W. T. Holman, A. F. Witulski, B. L. Bhuva, and L. W. Massengill, "Differential Analog Layout for Improved ASET Tolerance," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

[90] S. E. Armstrong, B. D. Olson, W. T. Holman, J. Warner, D. McMorrow, and L. W. Massengill, "Demonstration of a Differential Layout Solution for Improved ASET Tolerance in CMOS A/MS Circuits," *IEEE Trans. Nucl. Sci.*, Dec. 2010.

[91] N. M. Atkinson, R. W. Blaine, J. S. Kauppila, S. E. Armstrong, T. D. Loveless, N. C. Hooten, W. T. Holman, L. W. Massengill, and J. H. Warner, "RHBD Technique for Single-Event Charge Cancellation in Folded-Cascode Amplifiers," *IEEE Trans. Nucl. Sci.*, 2013.

[92] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, and A. Balasubramanian, "On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies," *International Reliability Physics Symposium Proceedings,* 2010.

[93] N. M. Atkinson, A. F. Witulski, W. T. Holman, J. R. Ahlbin, B. L. Bhuva, and L. W. Massengill, "Layout Technique for Single-Event Transient Mitigation via Pulse Quenching," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, Jun. 2011.

[94] R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, T. D. Loveless, W. T. Holman, and L. W. Massengill, "A single-event-hardened CMOS operational amplifier design," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, 2012.

[95] R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, N. C. Hooten, J. H. Warner, W. T. Holman, and L. W. Massengill, "Differential Charge Cancellation (DCC) Layout as an RHBD Technique for Bulk CMOS Differential Circuit Design," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, Dec. 2012.

[96] A. L. Sternberg, L. W. Massengill, M. Hale, and B. Blalock, "Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[97] P. R. Fleming, B. D. Olson, W. T. Holman, B. L. Bhuva, and L. W. Massengill, "Design Technique for Mitigation of Soft Errors in Differential Switched-Capacitor Circuits," *IEEE Trans. on Circuits and Systems II*, vol. 55, no. 9, Sep. 2008.

[98] B. D. Olson, W. T. Holman, L. W. Massengill, B. L. Bhuva, and P. R. Fleming, "Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, Dec. 2008.

[99] N. M. Atkinson, W. T. Holman, J. S. Kauppila, T. D. Loveless, N. C. Hooten, A. F. Witulski, B. L. Bhuva, L. W. Massengill, E. X. Zhang, and J. H. Warner, "The Quad-Path Hardening Technique for Switched-Capacitor Circuits," *IEEE Nuclear and Space Radiation Effects Conference Proceedings*, Jul. 2013.

[100] D. F. Hilbiber, "A New Semiconductor Voltage Standard," *ISSCC Dig. of Tech. Papers*, pp. 32–33, Feb. 1964.

[101] K. E. Kujik, "A Precision Reference Voltage Source," *IEEE Journal of Solid-State Cirucits*, vol. 8, Jun. 1973.

[102] P. Miller and D. Moore, "Precision Voltage References," *Texas Instruments Analog Applications Journal*, Nov. 1999.

[103] G. C. M. Meijer, P. C. Schmale, K. Van Zalinge, "A new curvature-corrected bandgap reference,"," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, Dec. 1982.

[104] M. Gunawan, G. C. M. Meijer, J. Fonderie, J. H. Huijsing, "A Curvature-Corrected Low-Voltage Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, Jun. 1993.

[105] Y. S. Park, H. R. Kim, J. H. Oh, Y. K. Choi, B. S. Kong, "Compact 0.7-V CMOS Voltage/Current Reference with 54/29-ppm/°C Temperature Coefficient," *International SoC Design Conference (ISOCC)*, pp. 496–499, Nov. 2009.

[106] R. C. Dobkin, "Monolithic Temperature Stabilized Voltage Reference with 0.5 ppm/°C Drift," *International Solid-State Circuits Conference*, pp. 108–109, 1976.

[107] D. P. Laude and J. D. Beasom, "5 V Temperature Regulated Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. SC-15, no. 6, Dec. 1980.

[108] J. R. Black, "Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons," *Reliability Physics Symposium,* 1967.

[109] J. R. Black, "Electromigration;A brief survey and some recent results," *IEEE Trans. on Electron Devices*, vol. 16, no. 4, Apr. 1969.

[110] J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proceedings of the IEEE*, vol. 57, no. 9, 1969.

[111] R. E. Vallee, E. I. El-Masry, "A Very High-Frequency CMOS Complementary Folded-Cascode Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 2, Feb. 1994.

[112] J. S. Kauppila, "The Design of a Custom Single-Event Hardened Analog-to-Digital Converter," Masters Thesis, Dept. of Electrical Engineering and Computer Science, Vanderbilt University, Aug. 2003.

[113] R. W. Blaine, N. M. Atkinson, J. S. Kauppila, T. D. Loveless, S. E. Armstrong, W. T. Holman, and L. W. Massengill, "Single-Event-Hardened CMOS Operational Amplifier Design," *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, Aug. 2012.

[114] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, May 1999.

[115] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, Jun. 1987.

[116] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, Nov. 1996.

[117] A.-G. Vasilica, G. Pristavu, C. Pasoi, and G. Brezeanu, "Offset cancellation in bandgap references with CMOS operational amplifiers," International Semiconductor Conference (CAS), 2011.

[118] X. Yang, Y. Zhang, W. Huang, and C. Ling, "Low power chopper amplifier without LPF," *IEEE Asia Pacific Conference on Circuits and Systems*, 2010.

[119] V. G. Ceekala, L. D. Lewicki, J. B. Wieser, D. Varadarajan, and J. Mohan, "A method for reducing the effects of random mismatches in CMOS bandgap references," *IEEE International Solid-State Circuits Conference*, vol. 1, 2002.

[120] A. H. Atrash and A. Aude, "A bandgap reference circuit utilizing switching to reduce offsets and a novel technique for leakage current compensation," *IEEE Northeast Workshop on Circuits and Systems*, 2004.

[121] Y. Jiang and E. K. F. Lee, "A Low Voltage Low 1/f Noise CMOS Bandgap Reference," *IEEE International Symposium on Circuits and Systems*, 2005.

[122] S. Ruzza, E. Dallago, G. Venchi, and S. Morini, "An offset compensation technique for bandgap voltage reference in CMOS technology," *IEEE International Symposium on Circuits and Systems*, 2008.

[123] G. Ge, C. Zhang, G. Hoogzaad, and K. Makinwa, “A single-trim CMOS bandgap reference with a 3σ inaccuracy of ±0.15% from -40°C to 125°C,” *IEEE International Solid-State Circuits Conference,* 2010.

[124] Li Chen and D. M. Gingrich, “Study of N-channel MOSFETs with an enclosed-gate layout in a 0.18 /spl mu/m CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 4, Aug. 2005.

[125] L. Dong-Mei, W. Zhi-Hua, H. Li-Ying, and G. Qiu-Jing, “Study of total ionizing dose radiation effects on enclosed gate transistors in a commercial CMOS technology,” *Chinese Physics*, vol. 16, no. 12, Dec. 2007.

[126] P. Grignoux and R. L. Geiger, “Modeling of MOS transistors with nonrectangular-gate geometries,” *IEEE Trans. on Electron Devices*, vol. 29, no. 8, Aug. 1982.

[127] A. Giraldo, A. Paccagnella, and A. Minzoni, “Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout,” *Solid-State Electronics*, vol. 44, no. 6, Jun. 2000.

[128] D. Dzahini and H. Ghazlane, “Auto-zero stabilized CMOS amplifiers for very low voltage or current offset,” *IEEE Nuclear Science Symposium*, 2003.

[129] I. G. Finvers, J. W. Haslett, and F. N. Trofimenkoff, “A high temperature precision amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 30, no. 2, Feb. 1995.

[130] S. Chen and B. J. Blalock, “Switched capacitor bandgap voltage reference for sub-1-V operation,” *IEICE Electronics Express*, vol. 3, no. 24, 2006.

[131] Z. Qu, M. Zhang, and J. Wu, “A switched-capacitor CMOS voltage reference for ultra low-voltage and ultra low-power operation,” *IEEE Conference on Electronics, Circuits, and Systems*, 2009.

[132] B. D. Olson, “Single-Event Effect Mitigation in Pipelined Analog-to-Digital Converters,” PhD Dissertation, Dept. of Electrical Engineering and Computer Science, Vanderbilt University, Dec. 2010.

[133] J.-H. Shieh, M. Patil, and B. J. Sheu, “Measurement and analysis of charge injection in MOS analog switches,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, Apr. 1987.

[134] G. Wegmann, E. A. Vittoz, and F. Rahali, “Charge injection in analog MOS switches,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, Dec. 1987.

[135] Ming-Jer Chen, Yen-Bin Gu, T. Wu, Po-Chin Hsu, and Tsung-Hann Liu, “Weak inversion charge injection in analog MOS switches,” *IEEE Journal of Solid-State Circuits*, vol. 30, no. 5, May 1995.

[136] C. Eichenberger and W. Guggenbuhl, "Dummy transistor compensation of analog MOS switches," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 4, Aug. 1989.

[137] D. McMorrow, S. Buchner, W. T. Lotshaw, J. S. Melinger, M. Maher, and M. W. Savage, "Demonstration of single-event effects induced by through-wafer two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, Dec. 2004.

[138] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, Y. Boulghassoul, L. W. Massengill, and R. L. Pease, "Three-dimensional mapping of single-event effects using two photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, Dec. 2003.

[139] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, Dec. 2002.

[140] T. Boggess, K. Bohnert, K. Mansour, S. Moss, I. Boyd, and A. Smirl, "Simultaneous measurement of the two-photon coefficient and free-carrier cross section above the bandgap of crystalline silicon," *IEEE Journal of Quantum Electronics*, vol. 22, no. 2, Feb. 1986.