MEASUREMENT AND ANALYSIS OF SINGLE EVENT INDUCED CROSSTALK IN NANOSCALE CMOS TECHNOLOGIES

By

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To the love of my life, the source of my existence, my husband, Karthik Subramanian

To my beloved parents, Mrs. Geetha & Dr. N. Balasubramanian

and

To our bundle of joy Vrushab

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LIST OF ABBREVIATIONS

ASET	Analog Single-Event Transient
BUJ	Bounded Uncorrelated Jitter
CME	Coronal mass ejections
CMOS	Complementary Metal Oxide Semiconductor
CR	Cosmic Rays
DD	Displacement Damage
DSET	Digital Single-Event Transient
DUT	Device Under Test
ECC	Error-Correcting Code
EDA	Electronic Design Automation
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FWHM	Full width half max
FWHR	Full width half rail
GCR	Galactic Cosmic Rays
GeV	Giga electron volts
GHz	Giga Hertz
HF	High Frequency
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors
LET	Linear Energy Transfer

LF	Low Frequency
MBU	Multiple Bit Upset
MOS	Metal Oxide Semiconductor
NASA	National Aeronautics and Space Administration
NIR	Near infra red
NSREC	Nuclear and Space Radiation Effects Conference
RFID	Radio Frequency Identification
RHBD	Radiation Hardening by Design
SAA	South Atlantic Anomaly
SE	Single Event
SEB	Single-Event Burnout
SEE	Single-Event Effects
SEGR	Single-Event Gate Rupture
SEL	SE-induced latchup
SEM	Scanning Electron Microscopy
SEP	Single-Event Phenomenon
SES	SE-induced snapback
SET	Single-Event Transient
SEU	Single-Event Upset
SoC	System-on-Chip
SOHO	Solar and Heliospheric Observatory
SOI	Silicon-on-Insulator
SPA	Single-Photon Absorption

SR	Set-Reset
SRAM	Static Random Access Memory
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
TMR	Triple-Mode Redundancy
TPA	Two-Photon Absorption
VLSI	Very Large Scale Integrated Circuits
WCN	Worst case Crosstalk Noise

CHAPTER I

INTRODUCTION

The radiation effects community has for the past few decades studied the effects of random bombardment of Integrated Circuits (ICs) developed for space applications by ionizing particles of very high energy. Complementary Metal Oxide Semiconductor (CMOS) scaling has caused Single-Event Effects (SEE) to be the prevalent radiation induced anomaly for these space borne electronics. This constant race for integration has not only decreased the minimum feature size but also the minimum amount of charge required to represent a HIGH node voltage [1]. In the radiation domain, this translates into reduced charge requirements for generating a Single-Event Transient (SET) and the resulting Single-Event Upset (SEU). Most of the hardening techniques to combat these effects focus only on the propagation of SET pulses through the logic gates, without regard to the interconnects between them.

With the design and fabrication of ICs entering the deep sub-micron era, there is an ever increasing demand for the on-chip electrical isolation of various signals. However scaling has caused devices and interconnect wires to be placed at an ever-increasing proximity, and these reductions both in the interconnect distances and in the transistor switching delays, lead to faster signal transition times. Though the minimum device sizes are shrinking to the nanometer scale and the operating speeds increasing to the Giga Hertz (GHz) range, this has not had a comparable effect on the length and thickness of metal interconnects. In these deep sub-micron technologies, the thickness of the wire is

generally greater than its width. Additionally, the spacing between adjacent metal lines is often smaller than the distance between the metal levels. All of these factors contribute to increasing the *coupling* effect between interconnecting wires, and the resulting increase in the ratio of the coupling capacitance (between the lines) to the total capacitance (includes area and fringe capacitance) at global nodes. As a result crosstalk noise has become a major source of performance degradation in ICs today to the extent that sometimes it is the limiting factor for the use of advanced technologies [2] - [5].

In today's CMOS technologies with decananometer (between 10 and 100 nm) dimensions, conventional design rules account for crosstalk from normal signal transitions, but they fail to account for the faster signal transitions due to a Single Event (SE) hit. For such technologies, in the presence of a SE on an active line, interconnect crosstalk coupling might lead to the *creation* of an SET pulse on a passive line and its consequent propagation through electronically unrelated circuit parts. This not only increases circuit susceptibility by increasing the vulnerable area but also causes unexpected errors and leads to circuit malfunction in hardened designs. The severity is exacerbated if a critical circuit node is affected by crosstalk, for example a clock line in digital circuits or a biasing line in analog or mixed-mode circuits, causing the injection of multiple unexpected faults. This may invalidate the reliability of both voting and diagnosing operations in traditional hardening schemes, such as Triple-Mode Redundancy (TMR) [6]. Thus, to obtain a required level of radiation tolerance and for the purpose of validating existing fault-tolerance schemes addressing radiation effects in keeping with high performance demands, it is imperative to model SE induced crosstalk coupling in technologies used today and in the near future.

Objective of Proposed Research

The objective of this research is threefold; primarily to identify the factors that exacerbate SE induced coupling using simulations and modeling, secondly to design, fabricate and test a sample circuit to provide the first ever experimental measurement of SE induced interconnect crosstalk coupling and finally to propose design margins and mitigation techniques to contain this effect in the technologies studied. To elaborate a bit on the specific tasks, this proposed study focuses on the following:

- Identify the significance of SE induced crosstalk coupling compared to a normal voltage transient
- Identify factors affecting SE induced crosstalk including : collected charge, coupling capacitance and scaling technologies
- Calculate the coupling capacitance for deep sub-micron technologies investigated : IBM 180 nm, IBM 130 nm, IBM 90 nm and a generic 90 and 65 nm CMOS process
- Comprehensive Cadence® Spectre and Synopsis® Technology Computer Aided Design (TCAD) simulations to quantify this effect
- Design, fabricate and test a sample structure to experimentally measure SE induced crosstalk through the MOSIS IBM 90 nm trusted foundry
- Finally, provide design margins or mitigation techniques for designers to adopt to contain this effect

Organization of the Dissertation

The work proposed in this dissertation is organized as follows:

- Chapter I highlights the motivation for this work.
- Chapter II begins with a brief introduction of the space environment and the various sources of radiation. The effects these Single Events have on electronics are discussed. Charge collection mechanisms and equivalent circuit models used are also included.
- Chapter III then introduces crosstalk in the commercial (non-radiation) domain and the various models and mitigation techniques used.
- Chapter IV focuses on SE induced crosstalk coupling. It discusses the model used for calculating the coupling capacitance and differentiates SE induced crosstalk from normal voltage transient signals. The dependence of the crosstalk pulse (on *victim* line) on the *aggressor* pulse rise and fall times is emphasized here. Simulation results obtained show SETs propagating in the *victim* (passive) line due to a hit on the *aggressor* (active) line; even when technology specific design and layout rules were observed.
- Chapter V details the factors affecting capacitive crosstalk in the SE domain through Cadence® Spectre and 3D Technology Computer Aided Design (TCAD) mixed-mode simulations. A range of deep sub-micron technologies were simulated and the crosstalk pulse quantified in each case.
- Chapter VI discusses the test circuit fabricated in the IBM 90 nm CMOS9SF process. The results from the single-photon (top-side) and two-photon (through wafer) laser irradiation tests are presented measuring a voltage flip on the output

of a Set-Reset (SR) latch on the *passive* line due to SE induced crosstalk from a hit on the *active* line.

- Chapter VII demonstrates mitigation techniques that designers can use for this technology and in general to contain this effect.
- Chapter VIII provides conclusions and insights into the impact of this work for the community, summarizing this dissertation.

CHAPTER II

SINGLE-EVENT EFFECTS: SOURCES, MECHANISMS AND MODELING

Electronics that are exposed to radiation can be damaged by primarily three mechanisms: (i) Total Ionizing Dose (TID) effects, (ii) Displacement Damage (DD) effects and the focus of this work (iii) Single-Event Effects (SEEs). Total dose effects are discussed in detail in the following references [7] – [13] and Displacement Damage (DD) effects covered in [14] – [19] for the interested reader. The rest of this chapter focuses only on SEEs.

Ironically enough, the first paper to ever deal with the issue of Single-Event Upsets (SEUs) was not of on-board space electronics but one assessing scaling trends in terrestrial microelectronics [20]. The paper published in 1962, forecasted the eventual occurrence of SEUs in microelectronics due to terrestrial cosmic rays and further stated that “already at the present time the essential part of semiconductor devices, the active region, is close to the minimum size possible” [20]. The first confirmed report of cosmic-ray-induced upsets in space appeared a decade later at the Nuclear and Space Radiation Effects Conference (NSREC) and was presented in 1975 by Binder *et al.* [21]. The authors had observed four upsets in 17 years of satellite operation in bipolar J–K flip–flops operating in a communications satellite. However it was only in 1978-79 that the importance of SEU was fully recognized and a lot of papers published at conferences.

Today it is common knowledge that any satellite or vehicle designed for a space application must be robust to the atmospheric environment it operates in and that these

on-board electronics will be exposed to natural interplanetary and atmospheric radiation backgrounds. If during that exposure, an unreliable operation or malfunction occurs, it leads to failure of the mission and staggering losses. To ensure suitable operation in space and to increase the longevity and success of the mission, it is vital to study the factors involved. This chapter begins with an introduction of Single Events with their resulting impact on electronics and concludes with how the radiation-induced photocurrents can be modeled for circuit simulations. The first section begins with a discussion of CMOS scaling and how that has made space-borne electronics more vulnerable to Single-Event Effects (SEEs). Next the sources of radiation and the characteristic particles responsible for triggering SEEs in space and aircraft electronics are listed. This follows with the basic mechanisms involved in the collection and transport of this incident charge in the semiconductor material of the electronic device. The concept of linear energy transfer (LET) and the manifestation of the charge collection/transport processes and the resulting circuit response is highlighted. The chapter concludes with details and examples of the prevalent modeling and simulation techniques used to incorporate the single event induced photocurrents in circuit design for accurate results.

CMOS Scaling

We are living in a world where technology is progressing at a pace that is meteoric. Specifically, the incredibly rapid growth in the performance and throughput of CMOS integrated circuits over the last couple of decades has led to a microelectronics revolution that has profoundly changed the world. Favorable attributes, such as reduced cost and power, along with increased speed and performance have led to the widespread

adaptation of digital microelectronics and have changed nearly every aspect of the day-to-day lives of most of the world's inhabitants.

In the radiation domain, the very existence of Single-Event Effects (SEEs) and its rapidly gaining prominence are consequences of scaling. Previously, for larger devices, SEE did not exist, because device sizes had not been scaled down enough for a single particle to have any detectable effect [22]. Scaling is synonymous with Moore's Law [23], [24] and the consistent reduction in the size of electronic devices, has been a hallmark of the semiconductor industry.

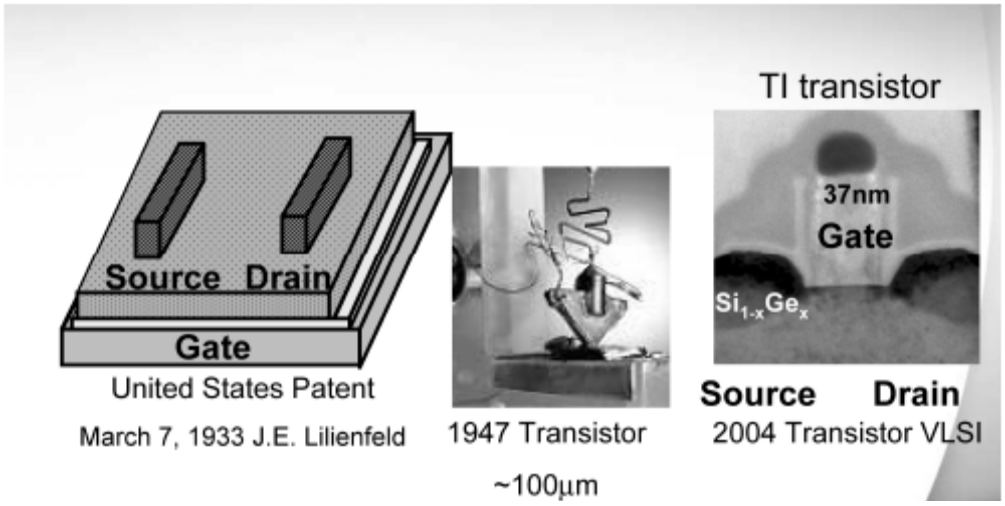


Figure 1. History of Transistors

The dominance of MOS technology in commercial applications began only in the late 1960s. The most advantageous property of CMOS digital logic is its reduced power consumption, which occurs primarily during the switching cycle when both devices are momentarily conducting. **Figure 1** shows the initial concept of the field-effect transistor in 1933, the first bipolar junction transistor that was successfully produced in 1947 by

Bardeen, Shockley and Brattain with a feature size of approximately 100 μm [25], [26], and a state-of-the art transistor with a gate length of 37 nm [27]. From the first planar integrated circuit fabricated in 1965 [28], we are now at microprocessors with over 400 million transistors, made possible through CMOS scaling.

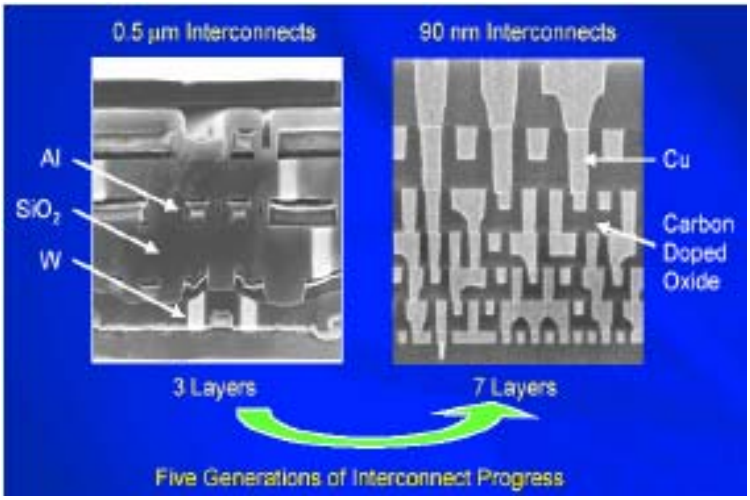


Figure 2. SEM micrographs of backend interconnect structures used in the 0.50 μm and 90 nm technology nodes [29], [30]

However as technology scales, the interconnect dimensions have not scaled comparably. There has been a trend toward an increased number of metal interconnect layers for a scaled process technology node. **Figure 2** shows Scanning Electron Microscopy (SEM) micrographs of backend interconnect structures used for the 0.50 μm and 90 nm technology nodes [29], [30] as a sample. For these deep sub-micron technologies, the thickness of the wire is generally greater than its width. Additionally, two interconnects of a same level metal are placed much closer than those belonging to two different metal levels. These factors in addition to increased coupling in the SE domain accentuate the need to model SE induced crosstalk.

Radiation Environments

For the success of a space mission, it is imperative to have reliable, radiation hardened and cost-effective designs, and to achieve that the radiation environment must be understood and accurately modeled. This helps obviate any underestimation of the radiation levels (excessive risk and may cause mission failure) or overestimation (leads to excessive shielding, reduced payloads, over-design and increased cost). Unlike terrestrial based electronics, any satellite or spacecraft once deployed into space is incapable of being reset or rectified without involving astronomical costs. Hence it is vital to have a thorough knowledge of the environmental hazards that the spacecraft must be designed for. These include low energy plasma, particle radiation, neutral gas particles, ultraviolet and x-ray radiation, micrometeoroids and orbital debris. Since we are interested in the hazards present for devices and integrated circuits operating in the space environment with ion energies ranging from keV to GeV and beyond, the discussion of sources and effects will be limited to that area. These malfunctions in on-board electronics can result from a single ionizing particle of very high energy or can occur from a finite number of particles, resulting in randomly-appearing glitches in electronic systems. These are frustrating errors which may cause anything from annoying (hopefully) system responses to catastrophic (hopefully not) system failures [31].

This section discusses the three important categories of high-energy particle radiations in space capable of affecting on-board electronics:

- Trapped radiation: consists of particles trapped by planetary magnetic fields in the Earth's magnetosphere such as the earth's Van Allen Belts

- Cosmic rays: comparatively low-level flux of energetic heavy ions extending to energies beyond TeV that originate outside of our solar system
- Solar Flares: bursts of radiation emitted by the sun, characterized by high fluxes of protons and heavy ions, referred to as solar particle events. They are a minor contributor to alpha particles, heavy ions and electrons with energies up to MeV.

Trapped Radiation Environment

The Earth has two radiation belts of different origins. The inner belt (Van Allen Belts) is a byproduct of cosmic radiation. It is populated by protons of energies in the 10-100 MeV range, capable of penetrating spacecrafts and on prolonged exposure, damaging instruments and being a hazard to astronauts, also called the "proton belt". The primary region of high particle flux lies between altitudes of 1,000 to 32,000 km and depends on latitude. **Figure 3** shows the Van Allen Belts contained in the earth's magnetosphere.

The proton belt has associated with it a very significant anomaly called the South Atlantic Anomaly (SAA), whose geologic origin is not yet known. It is located above South America; about 200 - 300 kilometers off the coast of Brazil, and extends over much of South America. It is a dip in the Earth's magnetic field allowing cosmic rays and other charged particles to reach lower into the atmosphere being a significant cause of SEs for satellites, aircrafts and space shuttles operating in the region. It occurs because of the tilt and shift in the Earth's geomagnetic and rotational axes relative to each other, resulting in the inner edge of the proton belt dipping to lower altitudes. The light blue and

green bands in **Figure 4** are due to an enhanced particle flux about the Earth's particle belts.

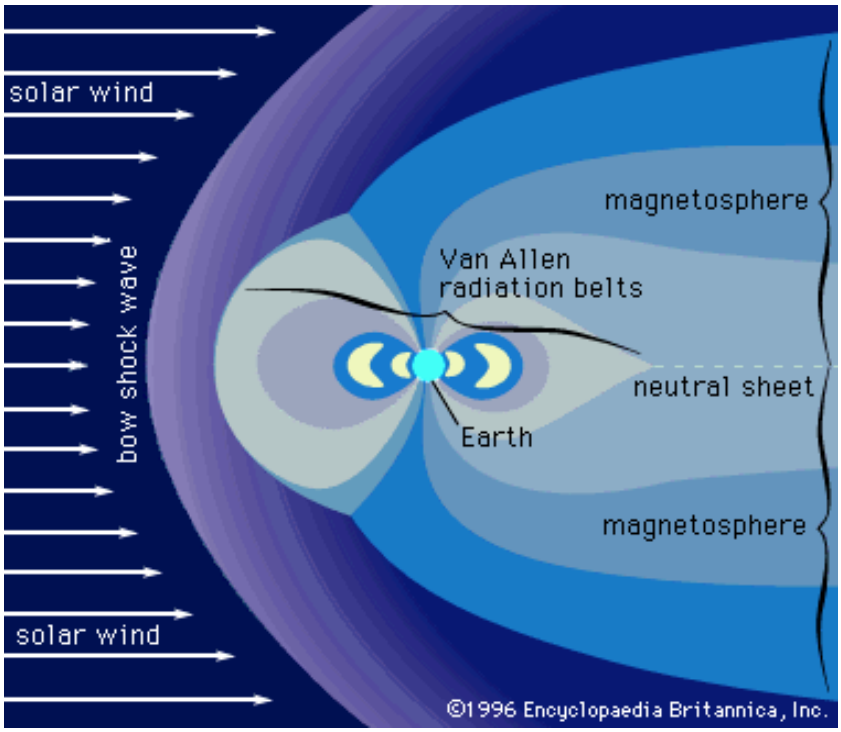


Figure 3. The Van Allen radiation belts contained within the Earth's magnetosphere [32]

The outer radiation belt is part of the plasma or ionized gas that is continually emitted by the sun called the solar wind, trapped in the magnetosphere. The name "radiation belt" is usually applied to the more energetic part of that plasma population, e.g. ions of about 1 MeV of energy. The solar wind streams off of the Sun in all directions at speeds of about 400 km/s (about 1 million miles per hour). It is the sun's hot corona, which is the source of solar wind. This solar wind is always directed away from the Sun, and its magnetic clouds interacting with the earth's magnetosphere cause it to vary in speed and composition. These high and low speed streams interact with each other and alternately

pass by the Earth with the Sun's rotation. During a period of high solar activity, the Galactic Cosmic Rays (GCR) are diverted away by the solar wind, from the magnetosphere and during low solar activity; the weak solar wind allows the higher GCR flux into the earth's magnetosphere, a source for SEs.

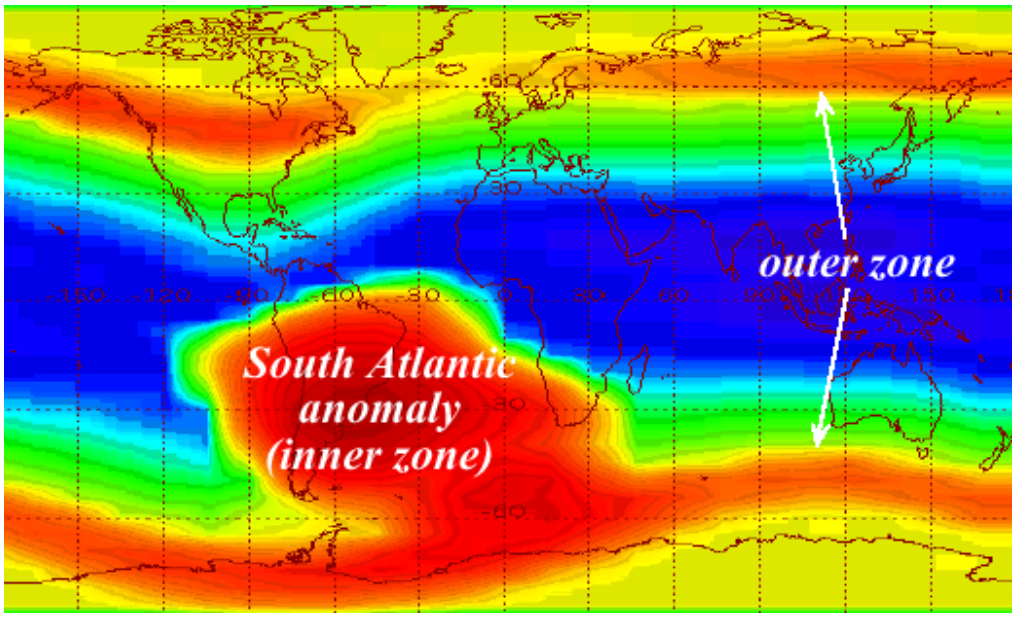


Figure 4. The illustration above shows the relative location of the SAA, with particle flux (arbitrary units) of > 0.7 MeV protons and > 0.5 MeV electrons in LEO measured on the NASA/SAMPEX satellite [33]

Cosmic Rays (CR)

There are three main sources of cosmic rays: galactic, solar and terrestrial.

Galactic Cosmic Rays

Galactic cosmic rays (GCR) are the 'primary' high-energy charged particles, assumed to be remnants from supernova explosions, originating outside the solar system but associated with the galaxy, providing a continuous, low flux component.

Recent observations from NASA and Japanese X-ray observatories have helped demonstrate that the magnetic fields in supernova remnants are stronger than previously thought, and are thus fully capable of producing cosmic rays [34]. Some general characteristics are listed in **Table 1** [35]. Composed mainly of hadrons, their relative abundance is shown in **Figure 5**.

Table 1. Characteristics of Galactic Cosmic Rays [35]

Hadron Composition	Energies	Flux	Radiation Effect	Metric
87% protons 12% alphas 1% heavier ions	Up to 10^{11} GeV	1 to 10 $cm^{-2}s^{-1}$	SEE	LET

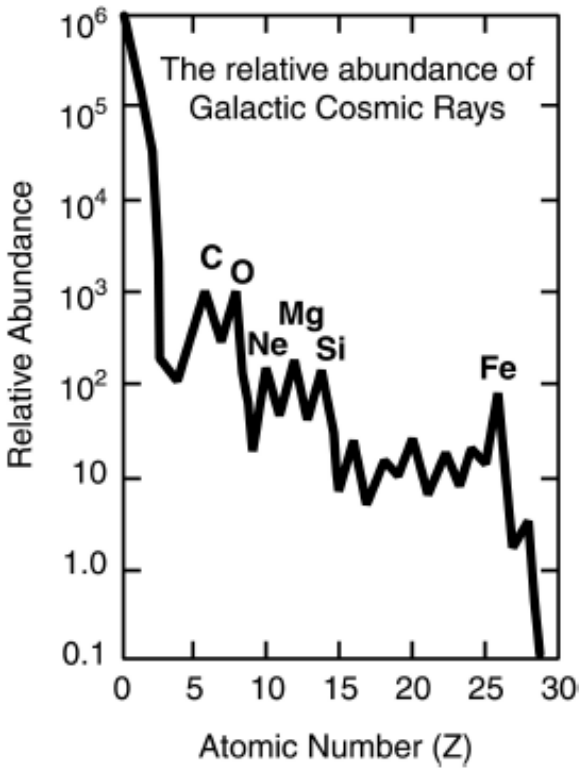


Figure 5. Abundances of Galactic Cosmic Rays up to Z = 28 [35]

Elements in the Periodic Table (up through Uranium) are present in GCR, although there is a steep drop-off for atomic numbers higher than Iron (Z=26). As a result, GCRs with particles heavier than Iron are not a major source of radiation errors because of their negligible statistical occurrence. Though heavy ions constitute only about 1% of GCRs, their high energies make them a formidable source of errors for on-board electronics. Although the source to reach such high energies is unknown, they have been recorded to be as high as 10^{11} GeV.

Solar Cosmic Rays

Originating from the sun, solar flares are tremendous explosions on its surface. They release energy as much as a billion megatons of TNT, heating up material to many millions of degrees, all within minutes. They are present usually near sunspots, along the dividing line (neutral line) between areas of oppositely directed magnetic fields. Flares release energy in many forms - electro-magnetic (Gamma rays and X-rays), energetic particles (protons and electrons), and mass flows. Apart from releasing energy, they also accelerate solar material to high velocities. Though similar to Galactic Cosmic Rays, they are not identical in composition owing to different origins [36].

Terrestrial Cosmic Rays

In spite of being softer than the radiation environments in space, the earth's atmosphere is also capable of contributing to SEs through terrestrial cosmic radiation. These are the primary cosmic rays penetrating the earth's atmosphere being rapidly

transformed by interactions with the earth's atmospheric atoms, into a cascade of secondary radiations, as shown in **Figure 6**. These cascades take place in the earth's atmosphere and they are the principal components of cosmic radiation at the earth's surface. Cosmic rays at sea level consist mostly of neutrons, protons, pions, muons, electrons, and photons. The particles, which cause significant soft fails in electronics, are those particles with strong interaction: neutrons, protons, and pions.

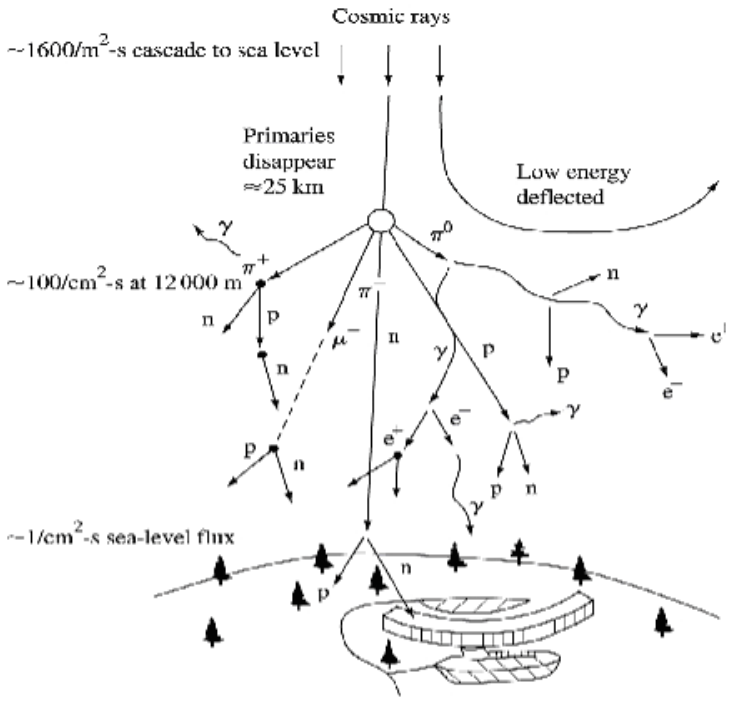


Figure 6. Schematic of how cosmic rays cascade into a shower of secondary particles interacting with the earth's atmosphere [37]

Solar Flares

Solar Flares have already been included under solar cosmic rays as the protons and electrons present can also contribute to errors. **Figure 7** below of a solar flare is the

biggest ever solar flare on record, released by the sun on April 2, 2001 [38], as observed by the Solar and Heliospheric Observatory (SOHO) satellite. The types of flares and the number of occurrences are associated with the sun's solar cycle, with an average span of 11 years (mainly seven years of high activity followed by four years of relative inactivity). It is during the active years that the maximum number of solar flares and coronal mass ejections occur.

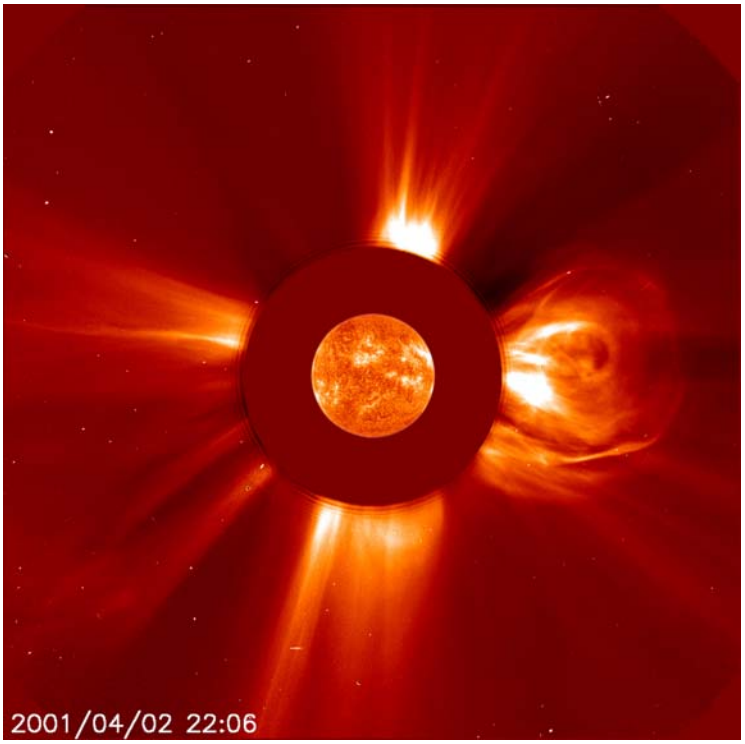


Figure 7. The biggest solar flare ever recorded unleashed by the sun as observed by the SOHO satellite, on Monday, April 2, 2001. This recent explosion from the active region near the sun's northwest limb hurled a coronal mass ejection into space at a whopping speed of roughly 7.2 million kilometers per hour, not aimed directly towards Earth [38]

Coronal mass ejections (or CMEs) are huge bubbles of gas that are ejected from the Sun over the course of several hours. They release 10^{17} grams of plasma and are rich in

protons. They have in the past been associated with Solar Flares, but can occur on their own also. The known effect they have is that they disrupt the flow of the solar wind and produce disturbances that strike the Earth causing catastrophic results sometimes.

Effect of Ionizing Radiation on Electronics

In the previous section the sources of radiation were identified, and here we discuss one of the dominating effects they can have on on-board electronics – Single-Event Effects (SEEs). The common cause for all SEEs is the passage of an energetic ion through the semiconducting or insulting materials used in the manufacture of integrated circuits. As discussed previously, neither electrons nor neutrons generate sufficient charge to produce SEEs directly, though neutrons can produce SEEs indirectly through secondaries emitted as a result of nuclear interactions. The highly energetic particles, such as heavy ions (in this context any ion with atomic number greater than or equal to two), protons and alphas are most critical for SEEs. The energetic ions as they pass through the material generate a dense track of electron-hole pairs. If the track passes near an electric field (semiconductor p/n junction or MOS transistor oxide), the free carries (electrons and holes) are separated and give rise to an electric current. It is this electric or photocurrent that is the root cause of all SEEs. Depending on the circuit response, they contribute to a range of errors.

Fundamental Single Event Mechanisms

The interaction of the energetic particles with the semiconductor material and the resulting mechanisms can be best understood by dividing the process into three stages (i) charge generation (ii) charge collection and (iii) circuit response [39] – [41]. Since

charge generation depends on the incident ion's mass and energy and on the properties of the material through which it passes – the same mechanism applies to all circuits fabricated in the same process (in this case silicon). Charge collection depends on electrical parameters such as applied bias and doping levels in the semiconductor and varies widely even from one transistor to the other in the same circuit. The last, circuit response depends on the circuit topology and determines if the SE leads to an SEU (a bit flip in a latch) or a Single-Event Transient (SET) (a voltage transient that may or may not be latched). The amplitude and duration of these SETs depend on factors such as ion LET, ion strike location and on the layout of the circuit including fan-out, transistor drive, and nodal capacitance. The three stages are discussed in greater detail below.

Charge Generation

Charge is generated when the incident ion interacts via Coulomb forces with the bound electrons of atoms constituting the semiconductor material (silicon in this work). The ionizing radiation can release energy in the semiconductor by one of these two methods (i) direct ionization by the incident particle itself or (ii) indirect ionization by secondary particles created by nuclear reactions between the incident particle and the sensitive (hit) device(s). Both mechanisms can lead to integrated circuit malfunction and are discussed below.

Direct Ionization

When a highly energetic carrier passes through the semiconductor material, electron-hole pairs are created along its path as it loses energy; and in silicon the

average energy required to produce these electron-hole pairs is 3.6 eV. The generated electrons (also known as delta rays) travel away from the points of origin, losing energy and generating additional electrons along the way. This results in a charge track of dense plasma of free electrons and holes formed along the ion path. The width of the track depends on the maximum energy of the delta rays, which, in turn, depends on the incident ion's energy.

Indirect Ionization

Though a light particle might not cause direct ionization, it is capable of producing secondary particles (through nuclear reactions) with high enough energies to cause SEUs. Protons and neutrons are examples of such particles that can produce significant upset rates due to indirect mechanisms by undergoing inelastic collisions with a target nucleus [42] - [44]. Examples of nuclear reactions that can occur include: 1) elastic collisions producing Si recoils; 2) Alpha/Gamma particle emission and the recoil of a daughter nucleus (e.g., Si emits alpha-particle and a recoiling daughter Mg nucleus); and 3) spallation reactions (target nucleus is broken into two fragments (e.g., Si breaking into C and O ions), each of which can independently recoil. Once the reaction has occurred, any of these reaction products (much heavier than original proton/ neutron) can now deposit energy along their paths by direct ionization capable of causing an SEU [45]. Normally inelastic collision products are localized, as they don't possess high energies. They may or may not traverse in the direction of the original strike, and hence affect angular SEU sensitivity [44], [46],

[47]. Once a nuclear reaction has occurred, the charge deposition by secondary charged particles is the same as from a directly ionizing heavy ion strike.

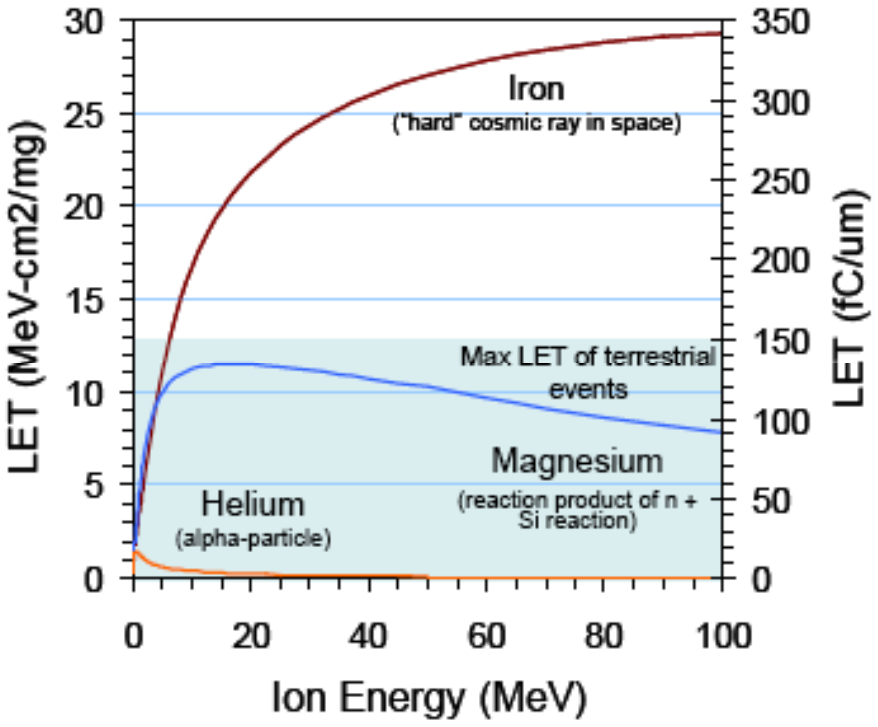


Figure 8. Linear energy transfer vs. Ion Energy for three types of ions in silicon, generated using SRIM. [51] The blue region denotes LET range for typical terrestrial events.

The LET Metric

When any energetic charged particle, passing through a semiconductor surface, transfers (loses) all of its energy, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's *range* [48]. Per unit depth into the material, the amount of energy the ion deposits is defined as its *stopping power*. The mass-stopping power is expressed by the standard metric for energy loss, the *Linear Energy Transfer (LET),* which is given by

$$\text{LET} = \frac{1}{\rho}\frac{dE}{dx}$$

where ρ is the density (mg/cm^3) of the material and *dE/dx* is the rate of energy loss in the material (MeV/cm). LET hence has the units MeV-cm^2/mg and can be quoted roughly independent of the target. An easier notation for LET is using the units (pC/μm) where it is denoted based on the charge deposited per unit length, as shown in **Figure 8** [49]. In silicon, the average energy required to produce these electron-hole pairs is 3.6 eV, and silicon has a density of 2328 mg/cm^3 [50], hence an LET of 1 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm. This conversion factor of ~100 provides an easy transition going back and forth between energy loss (LET) and charge deposition. These LET curves can be generated by computer codes derived from the work of Ziegler *et al.* (e.g., the TRIM and SRIM family of codes, [51]), and are useful in determining where the charge is likely to be generated and help analyze the location of sensitive volumes in these devices.

Charge Collection and Transport

Various methods (experimental and theoretical) have been used to study the charge collection processes. Some of the previous works include broadbeam measurements [52] - [54], ion microbeams and lasers with high-speed sampling oscilloscopes to measure charge-collection transients in Si devices [55] – [57], and to map charge collection as a function of position in ICs [58], [59] and more recently as a function of both time and position [60]. Charge collection physics have also been studied through the use of two- (2D) and three-dimensional (3D) numerical simulations [61], [62]. These are included

for reference and a brief discussion of charge collection mechanisms follows. The charge collection and conduction processes occur through depletion region drift collection, field-assisted funneling collection and diffusion collection. The final consequence of these free carrier generation and collection processes is the creation of a photocurrent at the terminals of the struck device.

Depletion region drift collection

The region in a device most sensitive to charge collection is usually the reverse-biased p-n junction [48]. These are the drain-well, drain-substrate and well-substrate junctions in CMOS transistors. The high electric field present in a reverse-biased junction depletion region efficiently collects the particle-induced charge through drift processes, leading to a transient current at the junction contact. Strikes occurring near a depletion region can also result in significant transient currents due to carriers diffusing back to the junction. This charge collection by the p-n junction leads to a circuit response to the initial single event penetration. The time period of this transient is extremely short as the drift is limited by the saturation velocity of carries, which for electrons in Si is $1x10^7$ cm/sec.

Field assisted funneling collection

The existence of a transient disturbance in the junction electrostatic potential called the “field funnel” was discovered by IBM researches [61], [63]. The high density of free carries localized along the strike, makes the semiconductor material more conductive, resulting in a collapse of the junction electric field along the ion

track, bending the equipotential boundaries, extending the junction deep into the surface. This in turn causes charges that were not initially exposed (outside the depletion junction) to the electric field assisted drift to be pushed to the junction contacts due to the “funneling” action. Thus the overall charge collected by drift is increased by this phenomenon, helping the initial flip of the node voltage.

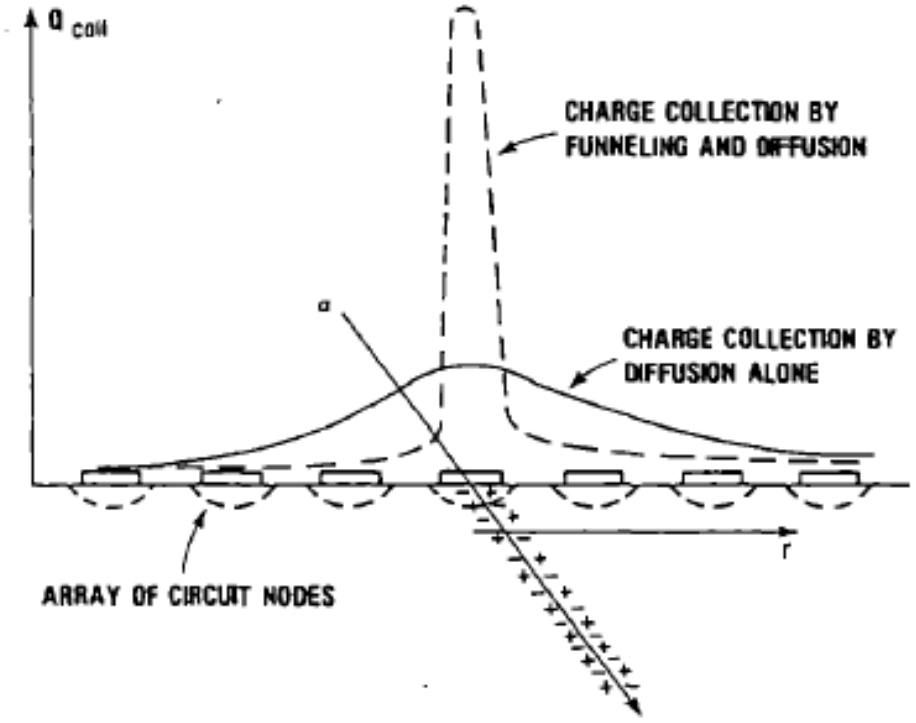


Figure 9. Charge collection as a function of the various charge transport mechanisms involved. Funneling causes enhanced collection at the struck node, and most likely leads to a single-event effect [33], [65]

Diffusion Collection

Finally, diffusion collection completes the charge collection process. The charges generated outside of the funnel, but within a diffusion junction length, diffuse to the junction and can be swept across the depletion region, leading to another current

mechanism [64]. This collecting junction could be the hit junction or an innocent neighboring region within that distance, as shown in **Figure 9**. This is a much slower process and this current component is delayed with respect to the field-assisted collection current. **Figure 9** depicts the charge collected as a function of the various mechanisms involved.

In the nanoscale CMOS technologies used today it has become a rarity to have single isolated nodes, instead a sea of nodes occur in close proximity, thus in all probability charge sharing among nodes will occur and parasitic mechanisms such as unintentional bipolar action and current shunts can also be major features of collection in real devices.

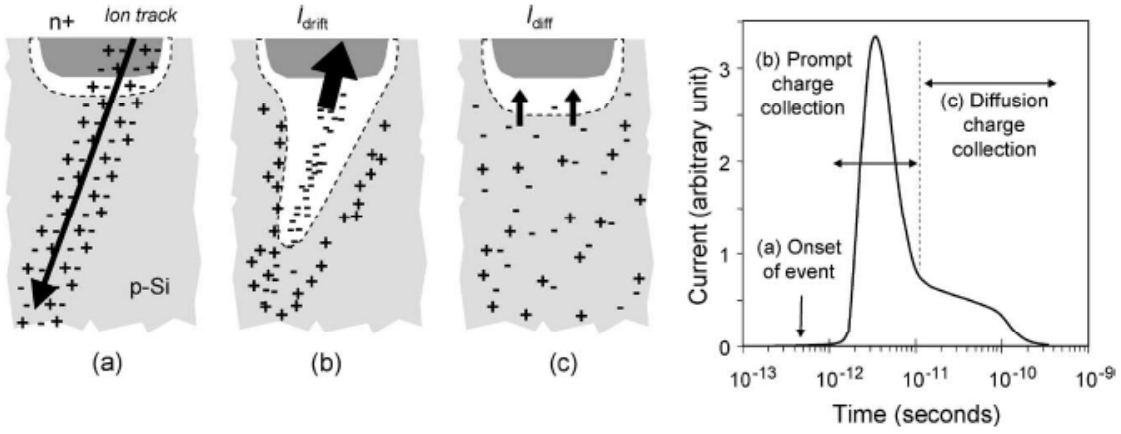


Figure 10. The charge generation and collection phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion [66]

Radiation Induced Photocurrent

The end consequence of the whole charge generation and collection phase is the generation of the radiation induced photocurrent as shown in **Figure 10** at the

terminals of the struck device. The shape of the current pulse can be related to the dynamics of charge collection. We can express current as

$$I = \frac{dQ}{dt}$$

where I is the current, Q is the charge and t is time. As soon as the strike occurs, the charge collection occurs by a fast drift of carries and the radiation induced photocurrent should be characterized by a sharp rising edge. As the charge collection progresses into a slow diffusion process, the charges move away from the device terminals and the change is mirrored in the current pulse by a decrease in the form of an asymptotic tail until all the excess charge is drained out from the struck device and normal operating conditions are restored (assuming no permanent SEEs occurred).

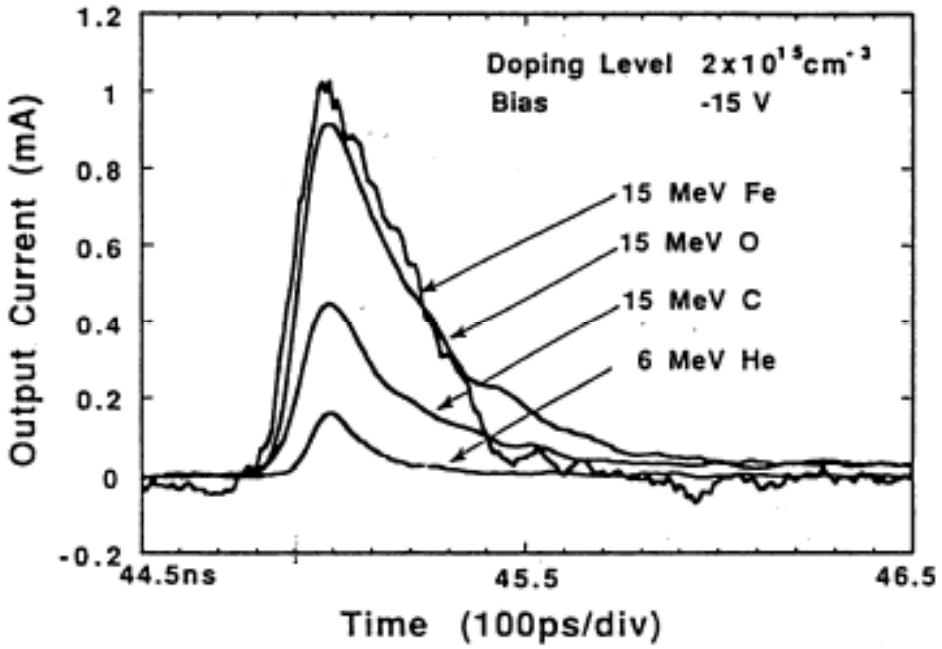


Figure 11. Current transients as a function of time for a series of ions with different energies [67]

Figure 10 shows a schematic of the expected photocurrent, and **Figure 11** illustrates several examples of radiation induced photocurrents measured at the outputs of irradiated diodes. Here, it is observed that the photocurrent shapes concur with the expected configuration. This photocurrent is the connecting thread between the microscopic world of nuclear reactions, molecular interaction of coulombic forces and the macroscopic commercial world of solid state devices and integrated circuits. When the radiation induced photocurrent is included in the circuit during integration and analysis through accurate models, it mimics the effect a SE has on the circuit operation, and the circuit response to these single-event effects can be predicted.

Circuit Response

The previous two sections discussed the deposition and consequent collection of charge. Here the potential circuit's response to these single events is explored. The circuit response is largely dependent on the topology of the circuit. The response of the circuit can either be destructive (permanent or hard errors) or harmless (soft errors).

The most basic term is the Single Event (SE) or the Single-Event Phenomena (SEP), which is nothing but the localized interaction of the single ionizing particle with a semiconductor device not dependent on flux or total exposure. All of the circuit responses fall under the broad definition of Single-Event Effects (SEEs).

Permanent Errors

The very name permanent or hard error signifies their destructive, non-correctable origins. This occurs when the single event causes physical damage to the circuit,

leading to a noncorrectable fault. Single-Event (SE) -induced burnout (SEB), gate rupture (SEGR) (where the gate ruptures due to the electric field exceeding the maximum limit) in power transistors and latchup (SEL) are examples of hard errors. These errors are most often analyzed and modeled at the individual device level.

SEB generally occurs either in power bipolar or MOS transistors. It is dependent on the currents generated by the ion strike. The generated current activates either the parasitic or active bipolar device, triggering a regenerative feedback mechanism, second breakdown or snap-back [68]. In the event, the high current is not curtailed and a permanent short exists between the source and drain, it will eventually lead to burning out the device or metallization [69].

SEGR is a failure in the insulation between the gate and channel region due to the electric field across exceeding a threshold value, and can occur in concurrence with SEB [48]. When an ion strikes the gate oxide, and charge is trapped and transported near the Si/SiO_2 interface, SEGR can occur. Accumulation of charge beneath the gate region (dependent on gate bias) will result in an increase in the electric field of the insulator, resulting in a localized dielectric failure.

SEL occurs in CMOS devices due to the presence of the back-to-back n-p-n-p junction. The parasitic latchup structure that is present in a CMOS process is illustrated in **Figure 12** [70]. This process is initiated by the current flow in the well/substrate junction, induced by the ionizing radiation strike, thereby causing a voltage drop in the well. The voltage drop forward biases the vertical device, consequently leading to an increased current into the substrate. This increase in substrate current causes a voltage drop in the substrate, turning on the lateral device.

The net resulting effect is an increase in current flow in the base of the vertical device, initiating the positive feedback loop. When latchup is triggered, the sustained high current can destroy the device due to the thermal runaway or metallization failure [70]. Reducing or disconnecting power from the device when in the latched state can enable it to return to normal operation, preventing a permanent failure.

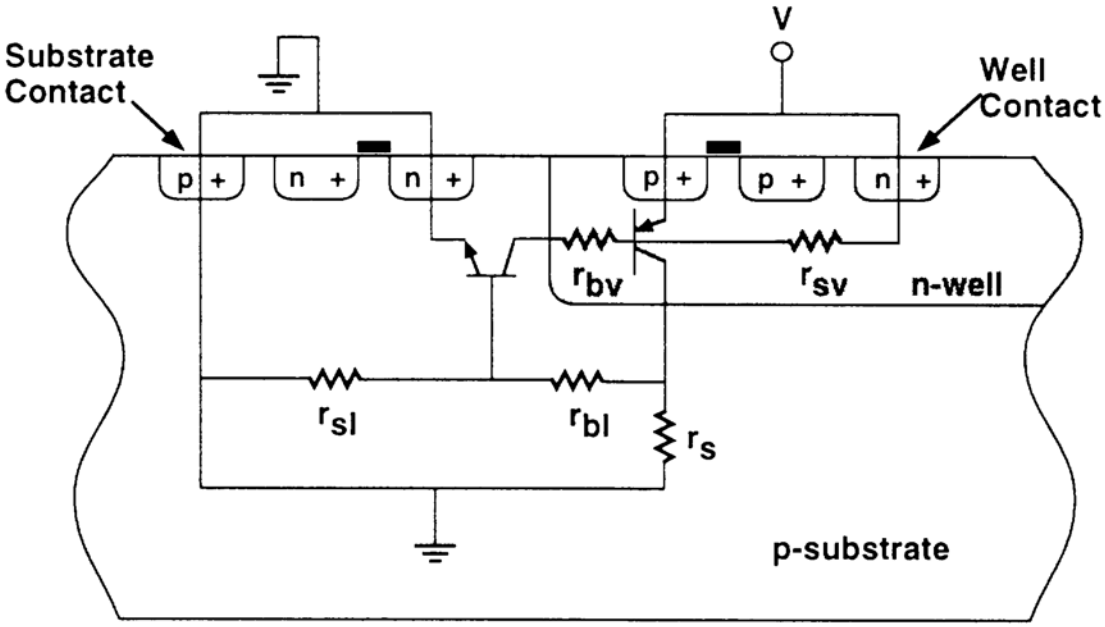


Figure 12. Parasitic latchup structure inherent to bulk CMOS technologies [70]

Transient Errors

These errors are false or spurious signals that propagate through the circuit paths during one clock cycle. These asynchronous signals can propagate to a latch and become static within that clock cycle, or be overwhelmed by the legitimate synchronous signals of the circuit. The timing of these single-event transients relative to the legitimate clock or synchronous signals decides if they lead to an error or not.

They are most important in combinational logic (non-sequential) circuitry and analog subsystems.

Single-Event Transient (SET) is the physical signal glitch (voltage) caused by a SE that may or may not get latched. It can either be an ASET (analog single-event transient) or a DSET (digital single-event transient) though there is no fundamental difference between the forms. ASET is typically used when working with analog circuits and DSET when using combinational logic apart from memory cells.

Single-Event Upset (SEU) is a bit flip or the corruption of information to an unrecognizable, unreadable, or unstable state, usually applied to memory cells. It can lead to a *circuit error* if the corrupted state alters legitimate information stored in or propagating through the circuit. That is, the upset can become an error, when it gets latched or if it is misinterpreted as valid data by other circuitry. Hence, from a hardening by design perspective, we are concerned only with upsets that cause errors, and an error is the finalized effect of that state. It can also be the potential end result of the DSET, if the memory circuit latches the incorrect value. Multiple Bit Upsets (MBUs) affects multiple circuits at once, not from multiple ion hits but from one event spreading to multiple sensitive nodes spaced close together.

Finally, as discussed above some of these circuit responses can fall either under permanent or transient errors based on the intensity of the response. SE-induced snapback (SES) in n-channel MOS output devices and SE-induced latchup (SEL) in CMOS structures are regenerative current conditions which can be reset if the current levels are benign. In cases where the regenerative current energy exceeds the thermal dissipation of

the affected region, these effects can cause melting and permanent physical damage to the circuit and become permanent errors. Though all known responses are introduced in this section, the focus of this work is on one of the non-destructive responses: Single-Event Transients in combinational logic. This leads to the next section of this chapter- the effective modeling and simulation of SEEs in processes to be able to precisely predict the SE response.

Single-Event Effects: Modeling and Simulation

The role of modeling is to provide designers with a set of tools that can be used to (i) better understand the SE mechanisms, (ii) analyze and predict the results of SE testing, and (iii) develop appropriate hardening strategies based on findings. Among the models used, some are commercially available software tools developed for generic applications while others are 'custom' tools and methods developed by researchers for specific SEEs. Frequently used commercial tools include (i) Mixed-mode Device/Circuit simulators (Standford's PISCES, Silvaco's Atlas and Athena, GENESIS, PADRE, DaVinci, MEDICI, Synopsis's DEVISE and DESSIS), (ii) Circuit simulators (Berkeley's SPICE, Silvaco's SmartSpice, Mentor's AccuSim, Cadence Virtuoso Spectre), and finally (iii) Logic level tools (Model*Sim*, QuickSim, and SpeedSim) to name a few.

From the previous section, it was identified that the result of a SE in a p-n junction is a radiation induced photocurrent. Depending on the tool used the photocurrent is modeled. If a device simulator is used, the hit transistor(s) is constructed in 3D, all the physics included and the photocurrent accurately calculated in the presence of a SE. Device simulators use doping profile information to determine the interaction of the

device with the ion strike. They provide a cost effective methodology for analyzing the effects of ionizing radiation on devices, and by integrating the generated currents in circuit simulators the results can be analyzed. On the other hand, circuit simulators are used for simulating complex circuit designs from a macro-model device view. Since device model information is provided by process designers, circuit simulations tend to represent realistic circuit performance, providing cost effective solutions. While it is accepted that circuit simulators sacrifice accuracy in device modeling, they compensate for it in vastly increased computational throughput. The optimal technique for modeling the photocurrent at the circuit level will depend on the complexity and functionality of the circuit in question. The photocurrent is incorporated into circuits through the insertion of an ideal time dependent current source across the terminals of the struck device. The use of either a simple double exponential current pulse profile (reasonably accurate) or a three dimensional (3D) mixed-mode calibrated current pulse (more accurate) will depend on the circuit complexity and electrical response. In some cases, only the time integral of the transient current source (total amount of injected charge) is relevant.

Current Pulse Profile for Circuit level simulations

For circuits with a few dozen to a few hundred transistors, the standard double-exponential current source injection with Spice® or Spectre®- level simulations is used. Though carrier flow across a junction is a complex three-dimensional microscopic process, affected by various factors including junction material parameters, geometry and location of the hit, time profile of thermalization, ambipolar diffusion of free carriers and the creation/collapse of a field funnel, the double-exponential model can be used

effectively as a simple approximation of the SET pulse generation for a macroscopic circuit simulation [31]. The advantage to this approach is that it is equally suited for digital, analog and mixed-signal circuits and has been reasonably accurate in correlating experimental SET measurements with the simulated SET pulse widths and durations for a majority of the cases. Typical parameters of this pulse are a rise time on the order of tens of picoseconds and a fall time on the order of 200 to 300 picoseconds.

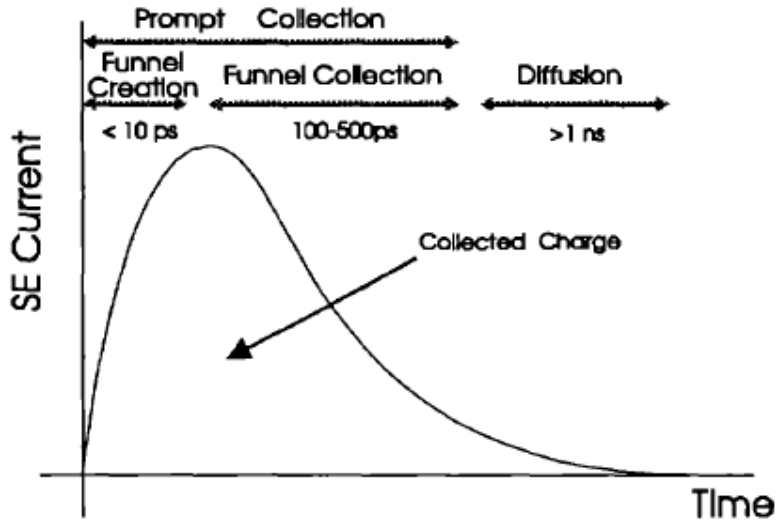
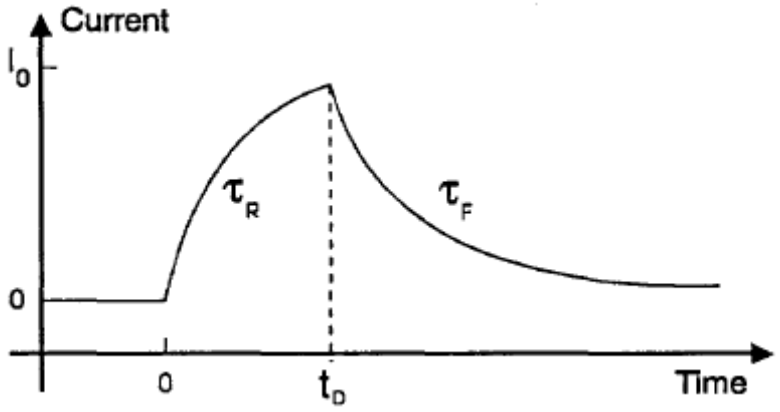


Figure 13. Typical shape of a SE charge collection current at the junction. The total injected/deposited charge Q is the area under the pulse curve [31]

Figure 13 shows the typical shape of the SET photocurrent pulse with the mechanisms attributing it. By comparing with the experimentally recorded current transients in **Figure 11**, a close co-relation is observed. This can be modeled in a circuit using a piece-wise double exponential function (**Figure 14**), by adjusting the rise, fall and transition times to fit experimental measurements, thus tailoring the final curve to achieve a precise total collected charge (Q).



$$I(t) = \begin{cases} I_o\left(1 - e^{-t/\tau_R}\right) & ; \quad t < t_D \\ I_o\left(1 - e^{-t_D/\tau_R}\right)e^{-(t-t_D)/\tau_F} & ; \quad t > t_D \end{cases}$$

$$Q = I_o\left[t_D + \tau_F - \tau_R - (\tau_F - \tau_R)e^{-t_D/\tau_R}\right]$$

Figure 14. The double exponential pulse used for circuit simulations and the equations defining it. The total charge (Q) delivered by the current pulse is obtained by the integral over time of I(t) [31]

However as we scale into deep sub-micron technologies, the double exponential current pulse will not suffice. The double exponential current pulse is described by charge collection models involving drift and diffusion across the drain body junction [45], [52], [65], [67], [68], and mostly assumes a constant built-in potential for the junction during the entire duration of the single-event voltage transient. These models hold good for technologies where the minimum dimensions are on the order of microns and prove sufficiently accurate for investigating SEEs on CMOS devices and circuits using compact models and circuit-level simulators (such as SPICE) in micron scale

technologies. However, as we scale into deep sub-micron (130 nm, 90 nm and beyond), the redistribution of electric fields resulting from an ion strike, affect multiple nodes and contacts. This in turn causes a distinct change in the shape of the current pulse. Characterizing SEs and SETs through Technology Computer Aided Design (TCAD) simulations results in a transient waveform significantly different from the familiar double exponential shape [62], [72] – [75]. Due to these findings, simulations were performed using 3D mixed-mode calibrated current pulses in the IBM 90 nm CMOS9SF process for accuracy, discussed in Chapters IV and V.

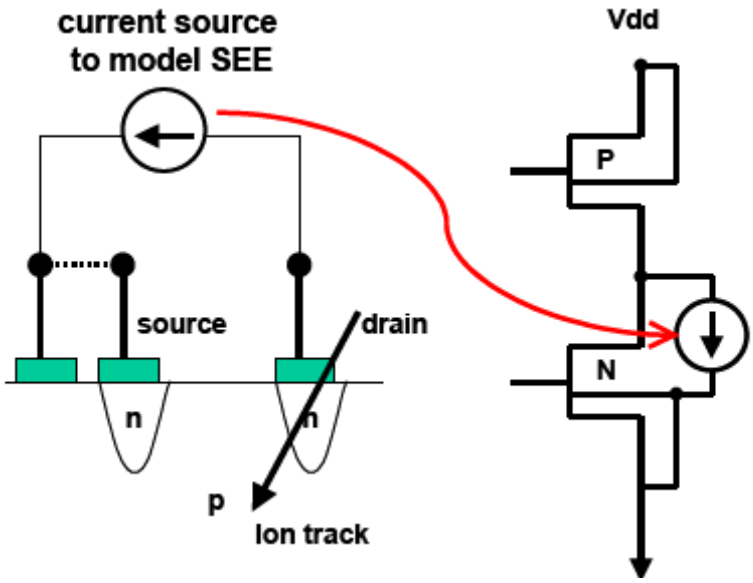


Figure 15. An ion strike on the NMOS transistor drain and an equivalent current source across its terminals modeling the hit [76]

The impact of the current source (modeling the radiation induced photocurrent) across the terminals of the struck device is its ability to turn ON a transistor that was OFF, or delay a transistor turning OFF, until the deposited charge is removed from the node. **Figure 15** shows such a sample case for a metal-oxide-semiconductor (MOS)

transistor, by placing the current source across the targeted junction. The total deposited charge is decided by the integral of the current pulse and the desired time decided by the rise and fall time values for the current pulse used.

Though using a circuit level simulation to model SEE is convenient even with complicated circuits, there are a couple of pitfalls associated with it. Primarily it is the generation of an accurate SE current pulse especially with scaling technologies as discussed earlier. Once that signal is generated within the circuit, these tools are a lot more accurate in propagating the SE current pulse. This is where device simulators (2-D and 3-D tools) come in, and they can much more accurately represent the SE current pulse generation. Their limitation is however, the size of the circuit to be modeled. The second problem with a circuit simulator is its inability to account for effects related to physical layout of devices such as charge sharing at multiple nodes for example, and also the focus of this dissertation "*SE induced crosstalk*". Typical transistor-level SEE modeling applies the ion strike to only one node. Though multiple current sources can be used to observe multiple node hits, these don't tie to the spatial relationship of the circuit nodes. These are only a couple of reasons why mixed-mode SEE modeling and simulation have become more widely used.

Mixed-Mode Simulations

In this chapter, the term *"mixed-mode"* refers to a simulator that combines a device-level model with standard circuit-level SPICE models to create a unified simulation environment in which the effects of single-event strikes on a particular device (modeled at the device level) can be studied at the circuit level. Today many commercial TCAD

simulators support mixed-level simulations for single-event effects. They allow selected components in a circuit to be modeled at the device level while the rest of the circuit is modeled at the circuit level. **Figure 16** shows a mixed-mode modeling representation for a four transistor latch circuit with a single transistor modeled at device level and the rest of the circuit modeled at the circuit level. These tools are frequently used in modeling the charge collection, transient pulse generation and early circuit responses to single-event transients. The limitation with these is that the size of the circuit that can be modeled is generally just a few (<25) circuit elements [41]. Both circuit level and detailed mixed-mode simulations have been used in this work.

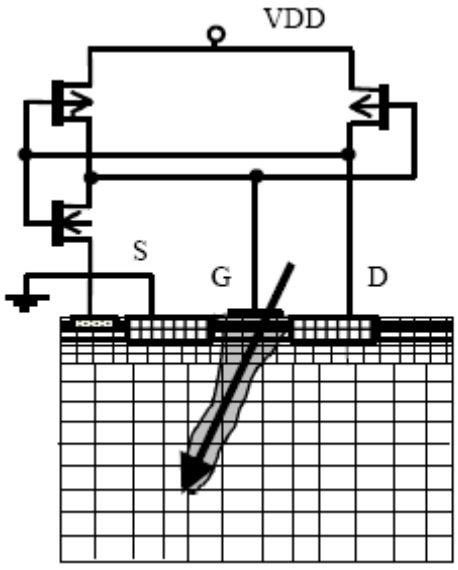


Figure 16. Mixed-mode simulation of a 4 transistor latch

CHAPTER III

CROSSTALK IN A NON-RADIATIVE ENVIRONMENT

The tremendous advances in lithography over the recent years have made GHz clock speeds available today. The key improvements that have enabled this achievement include the reduction of the device channel length and the multiplication of the interconnect layers, as shown in **Figure 17**. The increasing number of metal interconnects provide more layers for routing and enable efficient use of the silicon surface [77]. **Figure 18** shows how MOS devices are placed closer to each other due to the availability of many routing layers. However, the shrinking geometries and growing density of integration and speed of ICs have created concern for scrutiny of crosstalk faults [78] - [80].

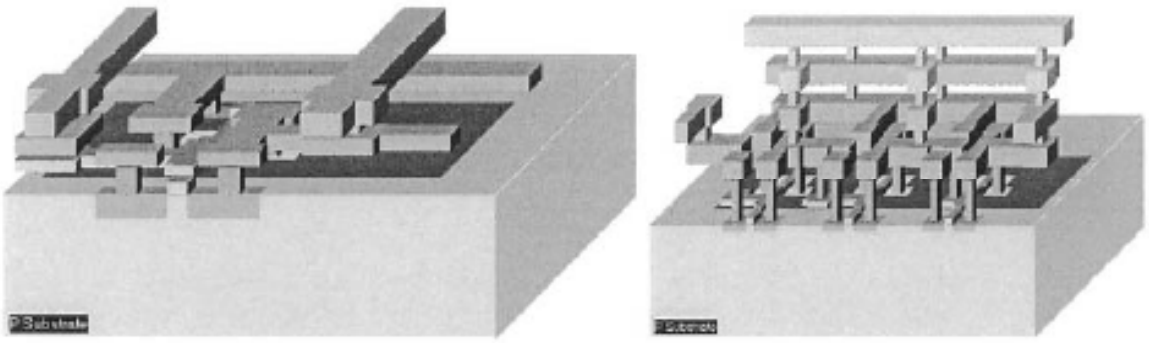


Figure 17. Evolution of the integrated circuit technology from 0.8 μm 2-metal layer CMOS process down to the 90 nm 8-metal layer CMOS process [77]

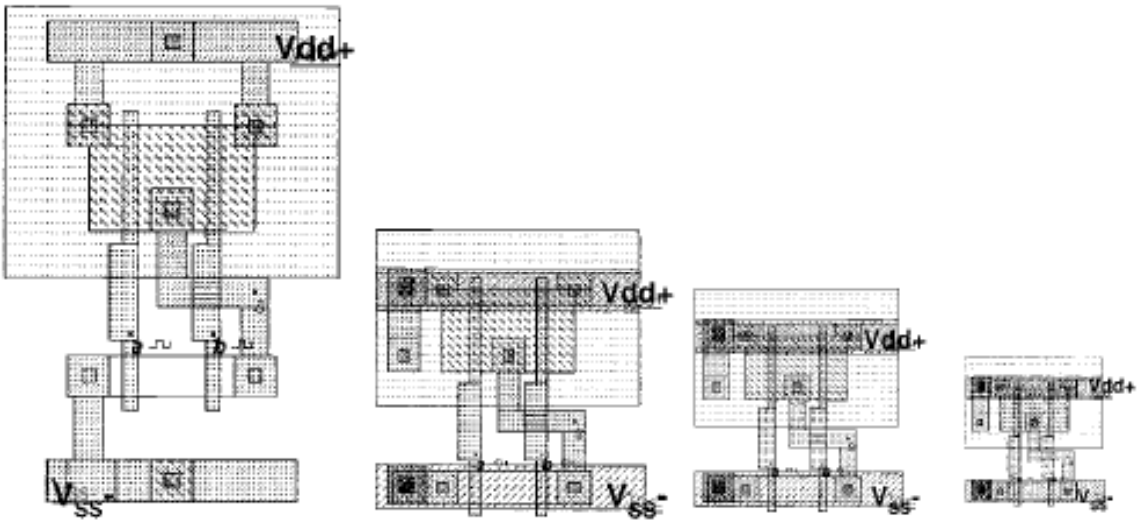


Figure 18. The evolution of silicon area used to implement a basic logic gate [77]

Scaling has greatly increased the role of interconnects in IC performance. The industry faces quite a few challenges as a result, further necessitating solutions through design for interconnects [81]. One of the issues with continued scaling is additional strain on the performance of multilevel interconnects. An issue arising from this is grain boundary scattering, increasing the resistivity of copper lines as they get narrower. The 2006 International Technology Roadmap for Semiconductors (ITRS) attributes about 25% of the switching voltage to crosstalk for a mere 100 μm long interconnect line in current processes [82] providing an insight into the impact of scaling on crosstalk coupling, as listed in **Table 2**. One of the solutions include the use of materials with lower dielectric constant between the interconnect layers to reduce crosstalk and power dissipation. Ultra high operating frequencies, lead to increased parasitic coupling due to increased switching speeds. This results in noise or timing modifications at the involved signals in the circuit. Specifically, signals transmitted over long wires are exposed to this

problem also due to the resistivity related to such interconnects. Prevalent signal integrity losses due to overshoot, undershoot, hazards and glitches, ringing/ oscillation and long settling time etc., caused due to interconnect parasitics are further aggravated in the presence of crosstalk coupling. Crosstalk in a normal operating environment has been the focus of many researchers for the past many decades, as it is an inevitable byproduct of the quest for smaller devices and increased packing densities. In this chapter, crosstalk is defined, and some of its detrimental effects in the digital and mixed-mode domain highlighted, in a normal operating environment.

Table 2. Interconnect Technology requirements: Near- Term Years [82]

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Line length (μm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk	136	118	107	96	90	84	79	73	61

Capacitance and Charge

Charge accumulates between two conductors separated by a dielectric in the presence of a voltage differential between them, as shown in **Figure 19**. The magnitude of charge is directly proportional to the differential voltage. Capacitance (C, units of farads) is the proportionality constant relating the charge accumulated (Q, in Coulombs) to the voltage difference between the plates (V, in volts) as given below:

$$Q = CV$$

Keeping capacitance constant, and differentiating above equation w.r.t time,

$$\frac{dQ}{dt} = C\frac{dV}{dt}$$

The rate at which charge changes with time defines current, which yields the familiar equation relating voltage, current and time to capacitance

$$CdV = idt$$

When the capacitance at the node is a constant, the other factor that influences the charge/coupling at the node is the dV/dt of the node voltage. In the presence of sufficient coupling between two interconnects, the node voltage on the *passive* (victim) line changes based on the dV/dt of the *active* (aggressor) line attributing to *crosstalk*, as discussed in the following section.

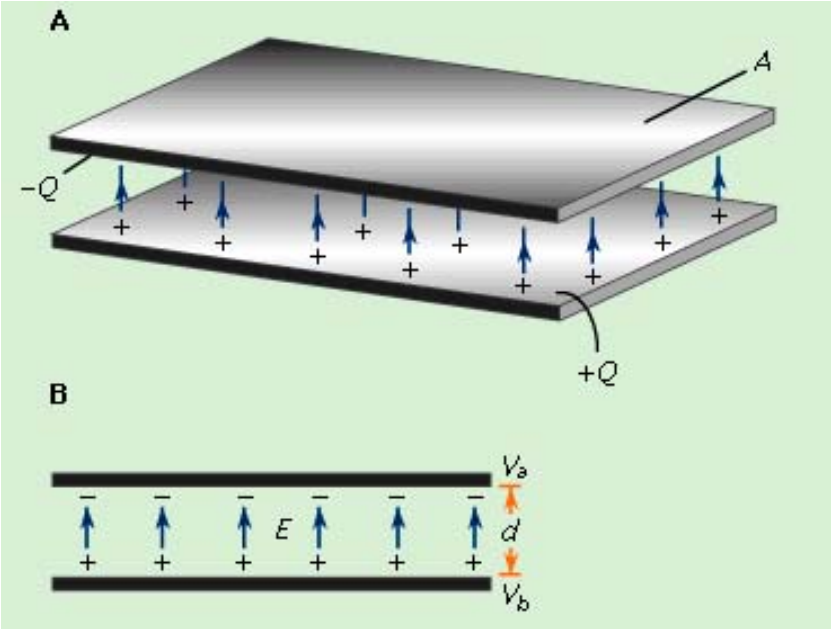


Figure 19. Schematic of a large parallel plate capacitor [83]

Crosstalk

Crosstalk can be defined simply as the unwanted transfer (leakage) of information (signal) from one conductor to another. The crosstalk coupling effect can be induced primarily through three coupling mechanisms: radiative, inductive and capacitive [84] which are briefly described below.

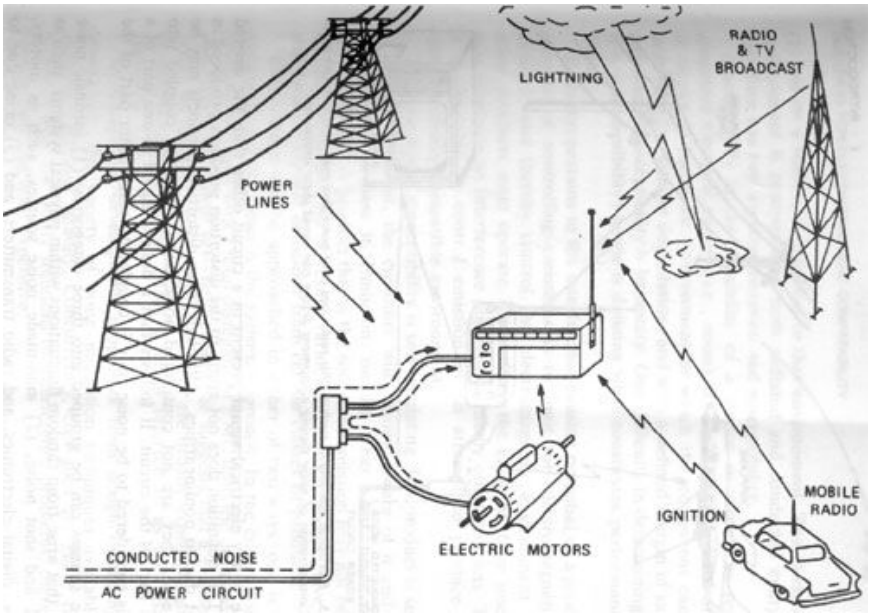


Figure 20. Radiative Coupling

Radiative Coupling

When electromagnetic fields travel through space with the velocity of light, they may influence electrical installations in the vicinity (near or far) of the source. Some examples of sources of electromagnetic fields are radio or TV transmitters, cell phones or any kind of wireless applications as shown in **Figure 20**. The high frequency parts of fast signals or of fast transients (ESD, surge, burst lightning) may also lead to the radiation of electromagnetic fields by cables or any other conductive parts of the electrical installation

and may cause disturbances even in distant electrical systems. Radiative coupling is essentially any such self induced EMI disturbance and is treated with an EMI/ EMC (electromagnetic interference/ electromagnetic compatibility) design framework [85]. An electromagnetic compatibility (EMC) design framework describes the ability of the electrical or electronic system, machine or appliance to operate without malfunction in the presence of a disturbing electromagnetic environment while itself not disturbing the operation of any other components of the system.

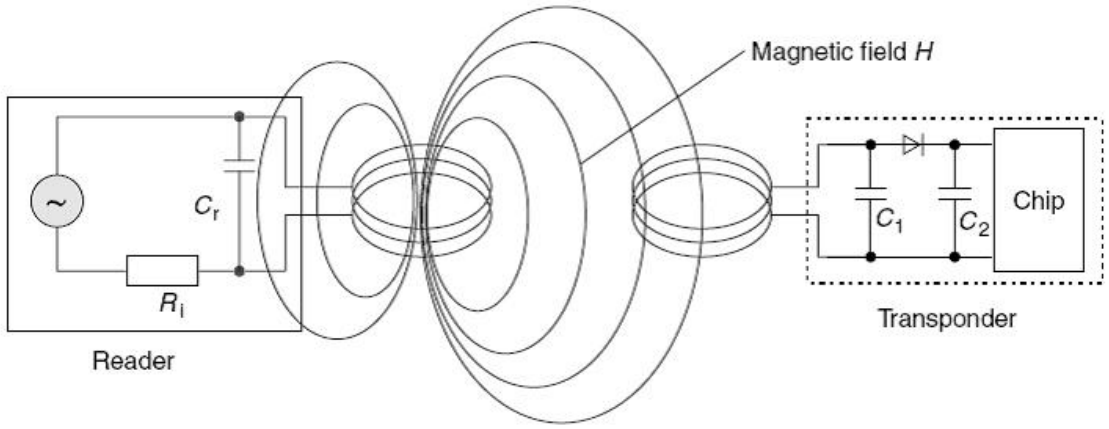


Figure 21. Inductive Coupling

Inductive Coupling

Inductive coupling can be defined as the transfer of energy from one circuit to another through a shared magnetic field or mutual inductance [86], as shown by an example in **Figure 21**. An electrical current passing through the coil of a primary conductor creates a magnetic field that induces an electrical current in the coil of a secondary conductor exposed to the magnetic field. One example is when Low Frequency (LF) and High

Frequency (HF) passive Radio Frequency Identification (RFID) devices use inductive coupling to transfer energy [87]. Inductive coupling may be deliberate and desired (as in the case of an antenna coupler) or may be undesired (as in the case of a power line inductive coupling into telephone lines). Generally, capacitive coupling favors transfer of higher frequency components, whereas inductive coupling favors transfer of lower frequency components.

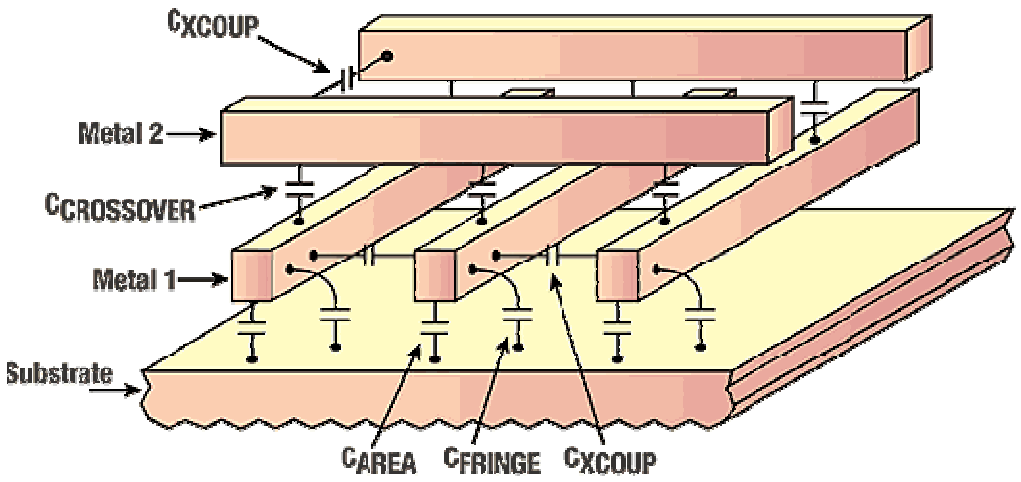


Figure 22. Capacitive Coupling

Capacitive Coupling

In this work, crosstalk is attributed primarily to capacitive coupling as in state of the art CMOS technologies this accounts for approximately 70% - 95% of the total node capacitances [88], due to increasing number of interconnect levels as shown in **Figure 22**. This manifests itself between two adjacent interconnect wires when their cross-coupling capacitance is large enough to influence each other's electrical characteristics. All conductors exhibit some interwire capacitances in their midst. In the nanoscale

regime of operation they are placed at sufficient proximity, that the capacitance becomes sizable enough to couple significant energy from one conductor, called an *aggressor* or *active* line, to another conductor, called a *victim* or *passive* line. When the coupling is large enough the logic value held by the victim is compromised [89].

Conventional methods of quantifying Capacitance Crosstalk

Previously capacitive crosstalk has been effectively modeled using a coupling capacitance between two metal interconnect lines. The total interconnect capacitance consists of three components (i) *area capacitance* (capacitance between the top or bottom side of an interconnect and its upper or lower layer or ground plane) (ii) *fringe capacitance* (capacitance between the vertical side of an interconnect and its upper or lower layer or ground plane) and (iii) *lateral capacitance* (capacitance between the vertical side of an interconnect and its neighboring interconnects on the same layer); a portion of which is the coupling capacitance as shown in **Figure 23** [90].

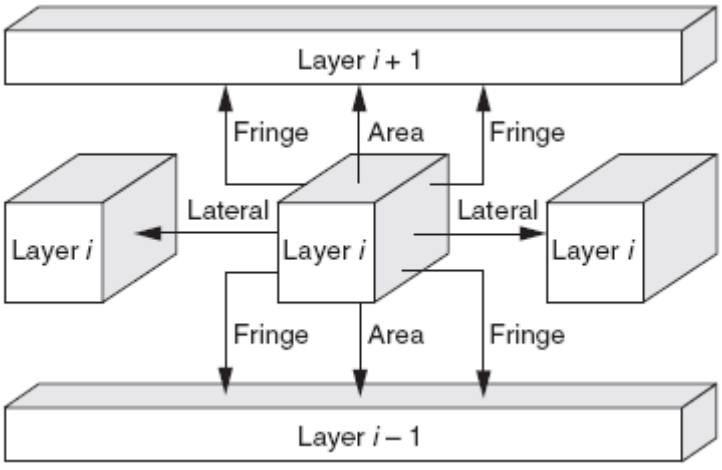


Figure 23. Components constituting the interconnect capacitance: area, fringe and lateral capacitance [90]

Capacitive coupling is limited between adjacent interconnects, however the effects of inductive coupling can extend beyond two adjacent lines as the inductive impedance of thick wires is now comparable to that of wire resistances at operating frequencies used in present day applications. At the interconnect dimensions used in current CMOS processes, the simple parallel plate approximation underestimates the coupling capacitance, and extensive research has been performed to identify an accurate model and to quantify the coupling capacitance at a node.

Some of the prevalent techniques used to model crosstalk include formulae derived by Sakurai and Tamaru [91], models for layout primitives by Choudhury *et al.* [92], general capacitance formula given by Chern *et al.* [93], equations for distributed RC lines by Sakurai [94] and closed form formulas by Wong *et al*. [95]. Some of the more recent techniques include closed form expressions for the peak amplitude, pulse width and time domain waveform of crosstalk noise in high speed very large scale integrated circuits (VLSI) by Heydari and Pedram [88], a lumped configuration model including the distributed properties of interconnect capacitance and resistance by Yungseon *et al*. [96] , worst case crosstalk noise (WCN) (maximum crosstalk noise peak generated by the aggressor) analysis using dual-exponential noise metrics by Sun and co-authors [97] and WCN generation for a quiet or a noisy victim by determining switching patterns and times of multiple aggressors using a RLC model by Chen *et al.* [98]. Kobrinsky *et al*. validate a simulation tool for calculating on-chip interconnects using S-Parameters [99].

Crosstalk in the Digital Domain

The increased coupling can cause two catastrophic events in the *digital domain*; increase in the signal delays (changing signal propagation time causing setup or hold time failures) and compromised signal integrity by introducing glitches (causing voltage spikes on wires, resulting in false logic behavior). The signal delays which get latched or logic errors caused due to signal integrity losses may jeopardize the circuit functionality and reliability. The pulse on the passive node induced by capacitive crosstalk depends on the following factors in a non-radiation domain:

(i) coupling capacitance itself – higher the capacitance at the node, greater the coupling,

(ii) the relative strength of the drivers which causes different slew rates for the signals than a case of matched drive strengths – a large device connected at a node take a long time to charge/discharge unlike a smaller device which is quicker,

(iii) presence and direction of a transition on the adjacent wire and the relative slew time between transitions on the aggressor and victim lines – if transitions on both the lines have the same direction, the transition times are reduced (crosstalk delay-speedup), and if they are in opposite directions, the effective delay is increased (crosstalk delay-slowdown).

Past researchers have studied crosstalk in the digital domain and also proposed multiple techniques to rectify its effects on signal delay [100] - [106], and integrity [107] - [109]. Wu and Lee use a Built in testing scheme to test for crosstalk faults using a

periodic square wave test signal [100]. Rossi *et al.* studied the usefulness of error-correcting code redundancy (ECC) in reducing these signal delays showing that dual rail codes perform better than Hamming codes at this task [101]. Takahashi *et al*. propose a technique for identifying the target crosstalk faults using topological and timing information, hence reducing the number of nodes to be tested in synchronous sequential circuits [102]. Xiao and Sadowska discuss gate [103] and transistor sizing [107] to reduce crosstalk. Kuo and co-authors study how crosstalk bounded uncorrelated jitter (BUJ) affects the signal integrity of the victim line [108].

Crosstalk in the Mixed-Signal Domain

As better functioning, cheaper and more efficient design solutions are sought; the combination of analog and digital domains for mixed-signal designs becomes attractive. The analog part of the chip should function in a noisy environment, and unlike its digital counterpart is very sensitive to voltage variations of the power supplies as well as the substrate ground. Thus, crosstalk is also a major concern for *mixed-signal designs* where digital circuits degrade dynamic range and sensitivity of analog circuits, such as switched capacitor filters, A/D and D/A converters.

These effects are minimized through shielding and isolation of the different circuit blocks to avoid transmission of digital noise to the analog domain through the common substrate (substrate crosstalk) [110] - [118]. Various techniques have been proposed to suppress substrate crosstalk including use of a decoupling operational amplifier in mixed-signal system-on-chip (SoC) devices [110], use of guard rings [111] and guard bands [112] - [113], use of a low resistivity substrate compared to a high or medium resistivity

substrate to lower substrate crosstalk [114], placing a thin, grounded highly conductive area in between active device layers in three-dimensional integrated circuits [115], reduction in substrate crosstalk due to use of various Silicon-on-Insulator (SOI) technologies compared to a bulk CMOS process [116] and use of metal faraday cages in a SOI technology [117].

All of the models, effects and solutions described in this chapter have been provided to emphasize the significance of crosstalk due to normal signal transitions in a non-radiative environment. However, little, if any research has been focused on *SE induced crosstalk*. The ensuing chapters of this dissertation describe the proposed approach to investigate this phenomenon and the factors influencing it through simulations and experimental verification.

CHAPTER IV

CAPACITIVE CROSSTALK IN THE SINGLE-EVENT DOMAIN

Crosstalk in electronics developed for space is a significant issue as the effects are much more pronounced than individual effects in the digital and mixed-signal domains as discussed in the previous chapter. Since parts built for space based electronics are also fabricated in commercial foundries, they are exposed to all the issues that come with scaling and also with closely packed, multi-level interconnects in current CMOS technologies as discussed in Chapter III. This chapter discusses the 2D TCAD model used for calculating the coupling capacitances, the factors causing a SE induced crosstalk pulse to dominate through 3D TCAD mixed-mode simulations in the various technologies and also the impact this has for space based electronics.

Aggressor Pulse Characteristics

When capacitive coupling between two interconnect lines is the source for crosstalk as in this study, the voltage pulse generated on the *victim* or *passive* node greatly depends on the characteristics of the *aggressor* pulse, especially the rise and fall times. The factors that decide the *aggressor* pulse characteristics are the rise and fall time and the duration of the pulse. For a simple CMOS gate, the switching speed is limited by the time taken to charge or discharge the load capacitance C_L connected at its output [119]. The sizes of the devices connected to the node and the size of the load capacitance contribute to the switching current at the node and decide the rise and fall times of the current pulse. For a

sample case as shown in **Figure 24**, the saturation current in a non-radiation, normal transient switching scenario is in the order of µAs for the IBM 90 nm CMOS process [120]. For the same circuit, if a SE strike were to occur at the node $V_{out,}$ the saturation current in a radiation domain would be in the order of mAs [75] assuming similar loading conditions. From the equation relating current, capacitance and voltage,

$$i = C * \frac{dV}{dt}$$

an expression for *dt* or the change in time can be obtained:

$$dt = C * \frac{dV}{i_{sat}}$$

When the current is approximated to be the saturation current as is done conventionally, there is an order of magnitude difference in the *dt* resulting from the difference in saturation currents for a normal, non-radiative domain and for a radiation environment.

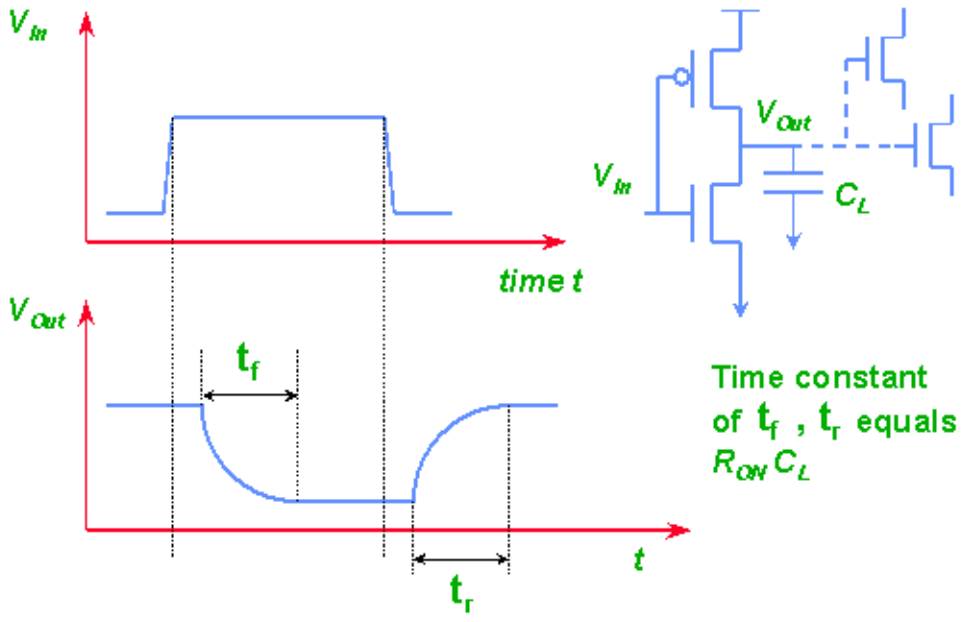


Figure 24. Rise and Fall times for a CMOS gate [121]

As a result, the rate at which a SE-induced voltage transient rises is much quicker than a normal voltage transient because of the characteristics of the SE current pulse (reaches a peak value in about 5-10 ps) [75], as discussed here and as shown in Chapter V. The duration of the pulse depends on the amount of charge deposited, and is longer for more deposited charge. These factors cause the voltage pulse generated from SE induced crosstalk coupling on the *victim* node to be more pronounced (reach a peak value much quicker than a normal voltage transient), and attain a magnitude at least two times greater than a normal transient crosstalk voltage pulse (shown through simulations in this chapter). This effect worsens with scaling as shown through simulations in Chapter V.

Dependence on dV/dt of Aggressor Pulse

In a radiation domain, the *aggressor* pulse that causes SE induced crosstalk on the *victim* line is a SET caused due to a radiation event. In sub-100 nm CMOS technologies, parasitic elements in the CMOS structure lead to significantly distinct PMOS and NMOS device charge collection characteristics, especially the temporal nature of the currents related to charge collection, leading to distinctly different pulse shapes [74], [75]. The SET pulse width can be measured by the amount of charge collected at the hit node, the rate at which the charge accumulates at the node, and the rate at which charge is removed from the node. This *dV/dt* of the *aggressor* pulse defines its characteristics at the various stages.

From Chapter III, the familiar equation relating voltage, current and time to capacitance was obtained

$$CdV = idt$$

In both a non-radiation and a single-event domain, crosstalk coupling between the *aggressor* and *victim* interconnect lines decide when coupling occurs. Once sufficient coupling is present, the other factor that the crosstalk pulse depends on is the *aggressor* pulse characteristics, specifically *dV/dt* of the node voltage (as discussed above and in Chapter III). The duration of the voltage transient on the *aggressor* node decides the width of the *victim* voltage pulse, and when the transient switches (non-radiation domain) or when the charge deposited at the node is removed (radiation domain), the corresponding voltage pulses on *aggressor* and *victim* nodes die out.

$$\text{Crosstalk Effect} \propto \text{Rate of rise/fall time of Aggressor pulse}$$

However,

$$\left(\frac{dV}{dt}\right)_{SET} > \left(\frac{dV}{dt}\right)_{NormalVoltageTransient}$$

which causes SE induced crosstalk to dominate. The fast rise times (few ps), higher saturation currents and quickly peaking current pulses associated with SEs in deep sub-micron technologies enhance the coupling between the interconnect line (*aggressor*) connected to the hit device and the interconnect line (*victim)* connected to passive devices, demonstrated through simulations in the ensuing chapters.

2D Capacitive Crosstalk Model

For all the simulations performed, the capacitance values between the two interconnects were calculated by using a 2D Technology Computer Aided Design (TCAD) simulation. Two metal lines in oxide were generated using Synopsis® DESSIS.

The net capacitance between them was calculated by including the parameters (l, w, h and d) specific to the technology simulated. The capacitance was calculated as a function of frequency using an AC sweep. More information is provided in Appendix A which includes information about the structure defined, and the files used to run the simulations. This provides a more accurate estimate than the simple parallel plate approximation, as the latter fails to be a precise approximation at interconnect dimensions used today. **Figure 25** is a schematic of the structure modeled using DESSIS, identifying the parameters given as inputs to the simulator. **Table 3** provides a few sample values for the parasitic capacitances estimated between two metal lines ($C_{m\text{-}m}$) for a range of technologies for a µm long interconnect line. The specific parameters (l, w, h and d) for each technology were estimated from the following sources [122] - [124].

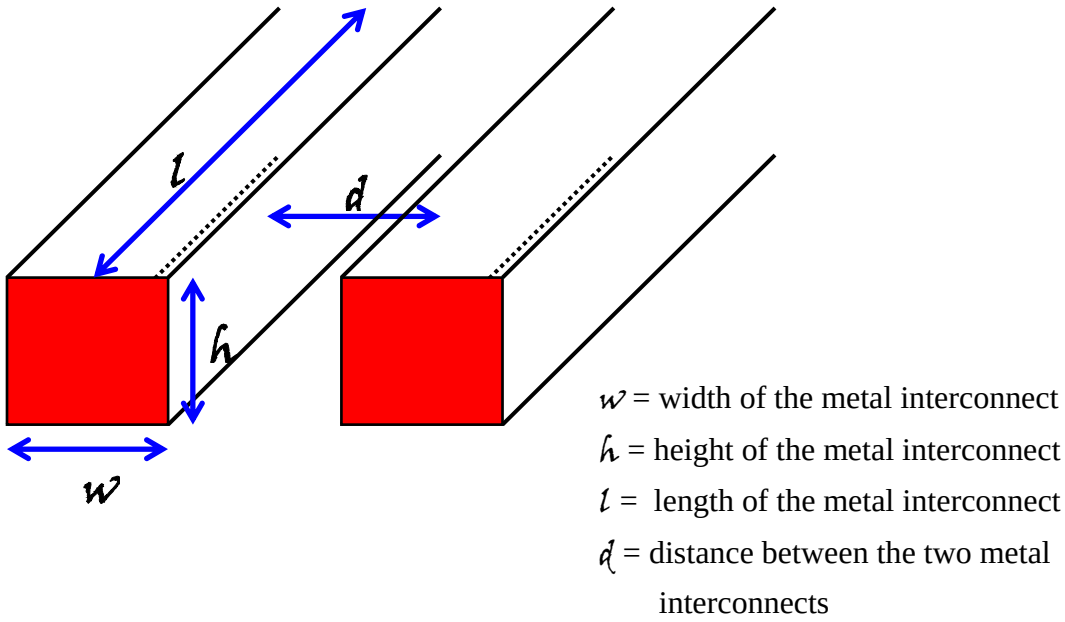


Figure 25. Schematic of the two metal lines modeled using a 2D TCAD simulation

Table 3. Parasitic Capacitances estimated from the 2D TCAD simulation

Process	Width (µm)	Height (µm)	Distance (µm)	C_{m-m} (fF/µm)
IBM 180 nm	0.27	0.36	0.27	0.106
IBM 130 nm	0.16	0.29	0.065	0.1104
IBM 90 nm	0.12	0.15 – 0.25	0. 12	0.107 – 0.14
Generic 90 nm	0.135	0.29	0.135	0.136
Generic 65 nm	0.0975	0.24 - 0.29	0.0975	0.148 – 0.166

Normal vs. Single-Event induced Crosstalk

Two chains of inverters were used to compare the voltage pulse from a normal voltage transient and that generated from a SE. A voltage transient pulse or a SE was simulated on one chain (*aggressor*) and the effect of coupling observed on the second chain (*victim).* **Figure 26** is a schematic of the circuit used and **Figures 27** and **28** illustrate the results obtained in the IBM 90 nm CMOS9SF process as a sample. The SE generated transient is for a p-hit case (strike on the PMOS transistor) with the SE strike simulated using Synopsys® 3D Technology Computer Aided Design (TCAD) mixed-mode simulations for an LET value of 40 MeV-cm^2/mg. In both cases the hit and corresponding passive transistor were modeled in 3D TCAD and the rest of the circuit in compact models. More detail about these kinds of simulations are discussed in Chapter V. The result shows that the transient arising from SE induced crosstalk for a 500 µm long line is more than 4 times greater in magnitude than that of a normal transient pulse. Similar results were obtained for other simulated cases as shown in **Figure 28**. If this pulse on the *victim* line surpasses the threshold voltage of the transistors in this process,

it may lead to an SEU. The next chapter describes in detail the simulation methodology and the circuit model used to investigate the factors affecting the amplitude and width of this pulse.

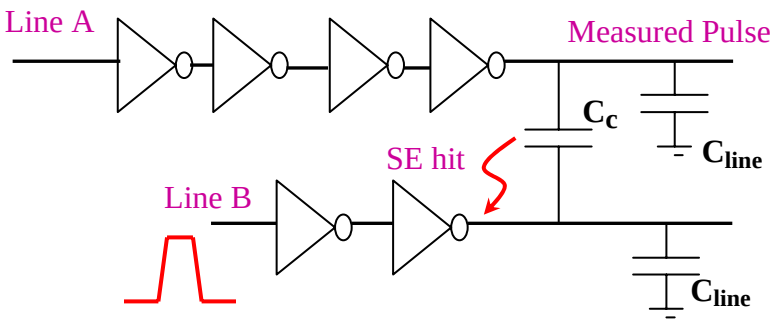


Figure 26. Schematic of the circuit used to compare crosstalk pulse profiles

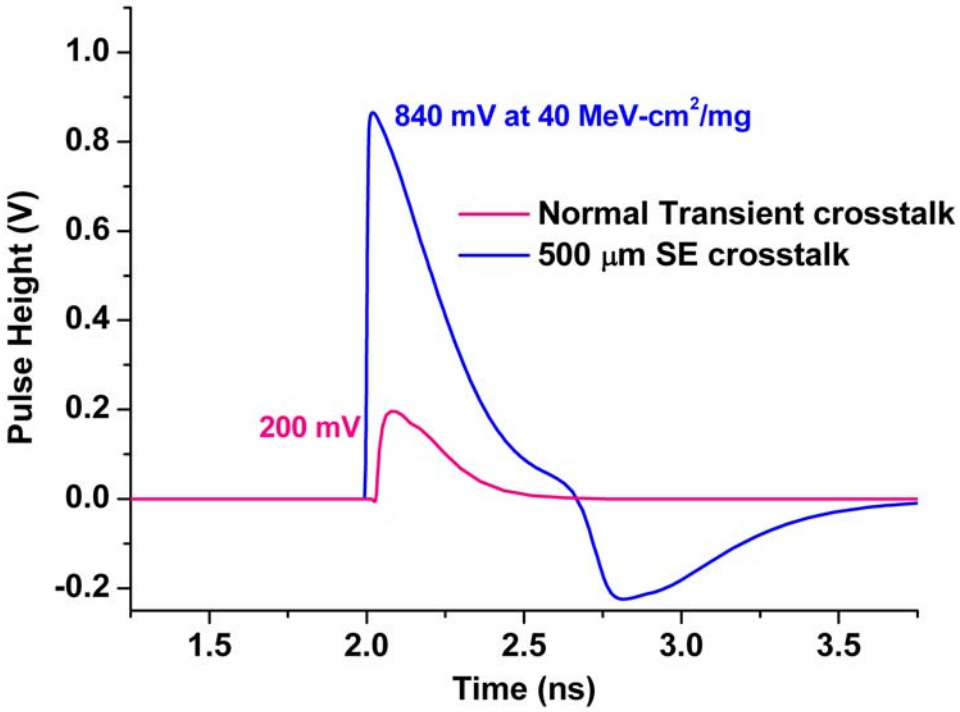


Figure 27. Simulation results showing normal vs. SE induced crosstalk at an LET of 40 MeV-cm^2/mg for a 500 µm long interconnect line (p-hit)

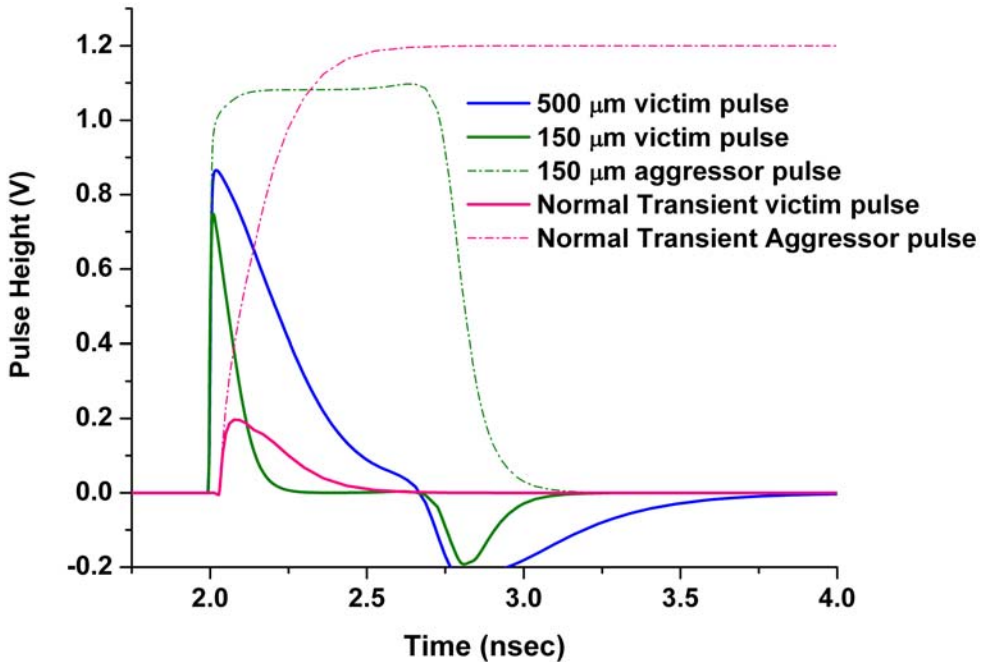


Figure 28. Simulation results showing normal vs. SE induced crosstalk at an LET of 40 MeV-cm^2/mg for a 150 μm and 500 μm long interconnect line (p-hit); both on the aggressor and victim lines

Impact for Space based Electronics

Though there has been a lot of emphasis on crosstalk in a normal operating environment, this has been quite low on the radar when investigating factors affecting the SE performance of combinational or sequential logic circuits. Research has been extremely minimal if any in this area. Scaling and interconnect dimensions used currently have exacerbated this effect. When conventional layout and spacing rules are observed in current CMOS technologies with nanoscale dimensions, crosstalk from normal signal transitions might be inconsequential, but the faster signal transitions due to a Single Event (SE) hit may still dominate. The simulation and experimental results obtained from laser experiments in the following chapters demonstrate this effect. If the charge

collected from a SE on an active line is substantial, a SET pulse can be *created* on a neighboring passive line and consequently propagate through electronically unrelated circuit parts as depicted in **Figure 29**.

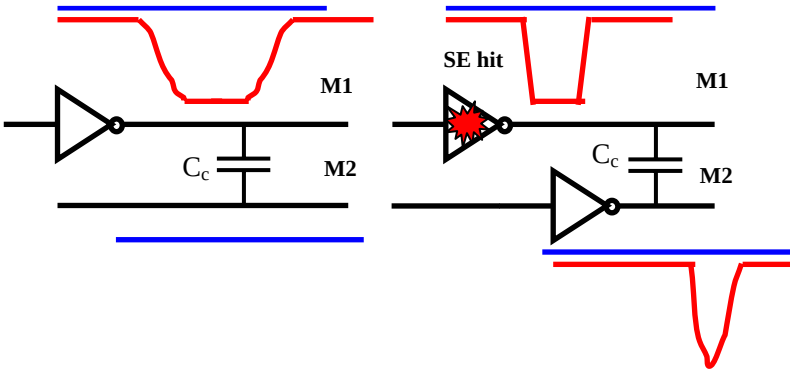


Figure 29. A SET is created on the passive line in the presence of increased crosstalk coupling due to SEs (right) whereas a normal transient does not affect the passive line due to reduced crosstalk coupling in the absence of SEs (left)

The consequence is the generation of an unexpected SET, which can get latched and impair circuit functionality in hardened designs based on circuit operation and favorable conditions. The severity is exacerbated if a critical circuit node is affected by crosstalk, for example a clock line in digital circuits or a biasing line in analog or mixed-signal circuits, causing the injection of multiple unexpected faults. Voting and diagnosing based hardening schemes like TMR, temporal or delay based hardening schemes [125] –[128] depend on the presence of a SET pulse only on one of the inputs. Unexpected transient pulses resulting from SE induced crosstalk may invalidate the reliability of these voting and diagnosing operations [6] as shown in **Figures 30** and **31**. The input to the voters in TMR systems are more vulnerable because the interconnects between the functional units

and voters are likely to be long, and thus sensitive to crosstalk [129]. In the absence of any protection or diagnostic scheme to combat faults in the voters or its interconnects, an incorrect signal maybe latched and the diagnosing operation affected.

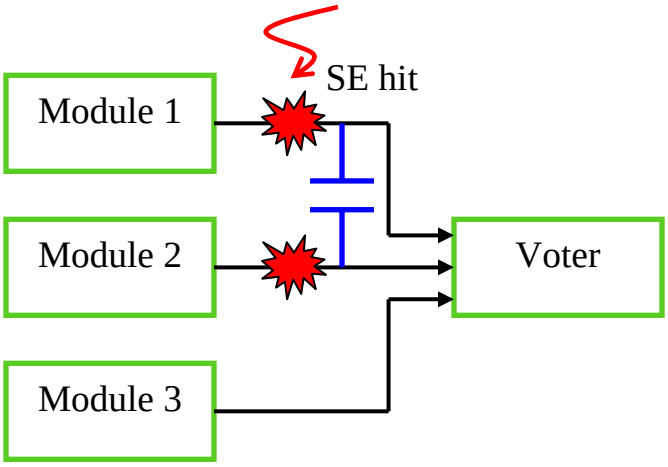


Figure 30. Sample schematic of how SE induced crosstalk coupling can cause an unexpected voltage transient at a voter input jeopardizing its reliability

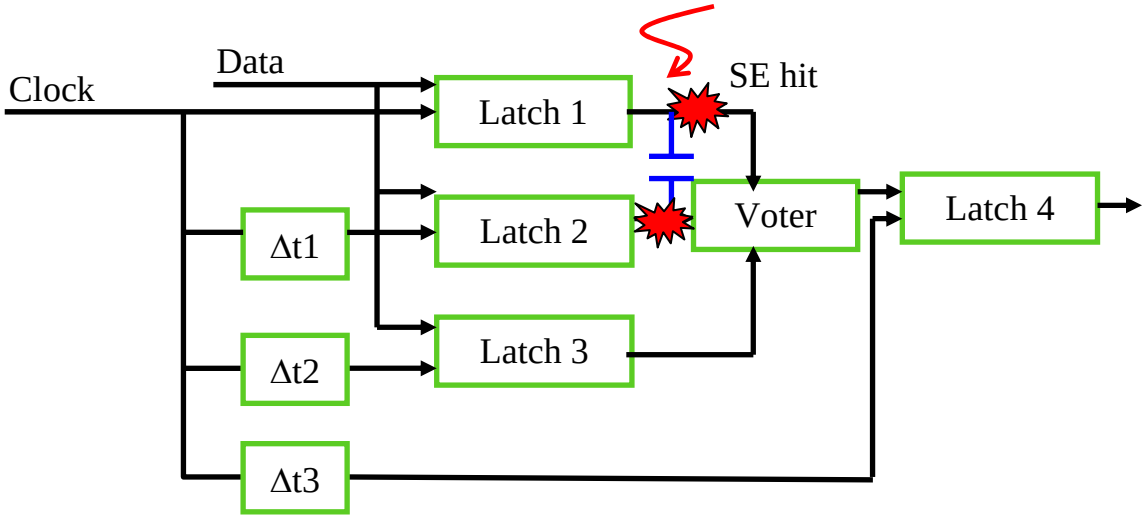


Figure 31. Sample schematic of how SE induced crosstalk coupling can occur in a temporal sampling circuitry affecting voting and diagnosing operations

CHAPTER V

FACTORS AFFECTING CAPACITIVE CROSSTALK IN THE SINGLE-EVENT DOMAIN

This chapter is split into two sections - the first part investigates the various factors that impact SE induced crosstalk through simulations using the Cadence® Electronic Design Automation (EDA) toolset for a range of technologies including the IBM 180 nm, IBM 130 nm and generic 90 and 65 nm processes, and the second part focuses on the IBM 90 nm CMOS9SF process using calibrated models and 3D mixed-mode simulations with the Synopsis® toolset. In the first part of this chapter, for the simulations performed the focus is in trying to identify the various trends that exist by using circuit level simulators. However, once that has been achieved a combination of circuit and device level simulations is used to accurately estimate the aggressor pulse characteristics described in the latter part of this chapter.

The circuit model used is identical to the one described earlier in **Figure 26**, except for the inverters connected at the end of the metal interconnects on both the lines as shown in **Figure 32** (repeated here for clarity and throughout this chapter with the parameter being varied highlighted). A SE hit was simulated at the output of the second inverter on *line B* using a calibrated double exponential current pulse and the resulting SE induced crosstalk pulse observed at the output of the fourth inverter on *line A.* A double exponential current pulse is used here for reducing simulation complexity; as trends across various parameters and across various technologies are examined. Unless specified

differently approximately 200 fC of charge was deposited to simulate the hit. A strike on the PMOS transistor is referred to as a p-hit and a strike on the NMOS transistor referred to as an n-hit. The values of C_c (capacitance between two metal layers in the same level) and C_{line} (capacitance between the metal line and ground) were calculated using the 2D TCAD model described in the preceding chapter. The input capacitance of the inverter was added to line capacitances within the circuit simulator. The circuit was simulated using the Cadence® EDA toolset for the IBM 180 nm (supply voltage = 1.8 V), IBM 130 nm (supply voltage = 1.2 V), generic 90 nm (supply voltage = 1.2 V) and 65 nm (supply voltage = 1.2 V) technologies. Simulations were carried out to study the effect of different parameters; such as interconnect lengths, deposited charge, and scaling technologies. The Cadence® Spectre simulation results are organized as follows. The same parameters are varied for the different technologies used and the results presented together in each case.

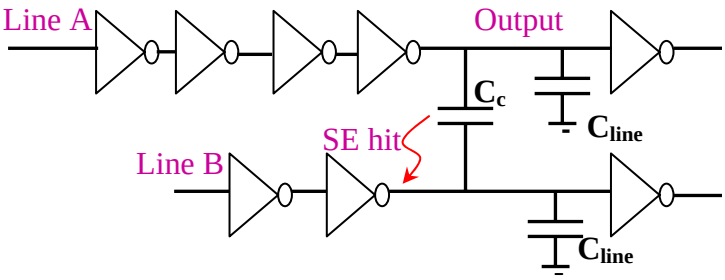


Figure 32. Circuit used to quantify the effect of various parameters on SE induced crosstalk

Varying Interconnect Lengths

One of the major problems with advanced technologies is interconnect spacing and routing. Though scaling has caused reduced nodal capacitances and device sizes, the trend has not been comparable for metal interconnects. In the deep sub-micron technologies, the metal thickness is now greater than its width. Moreover, the separation between adjacent metals on a same level is much smaller than those between different levels. These factors contribute to increasing the coupling between metal interconnects in state-of-the-art CMOS technologies. The following set of simulations was performed to determine the effects of varying interconnect lengths on the crosstalk pulse characteristics.

The set up was maintained as in **Figure 32** and the interconnect lengths varied from 100 to 5000 µm (reflected as varying capacitances) as highlighted in **Figure 33**. **Figure 34** displays the results for the 130 nm and 90 nm processes, a similar trend was observed in the other two technologies simulated. The average interconnect line length used for routing purposes range from 100 to 1500 µm but depending on circuit functionality and routing difficulty long lines do exist in some designs exceeding these values even in highly scaled processes. The pulse due to crosstalk noise peaks at 500 µm (445 mV) in 180 nm, at 1500 µm (732 mV) in 130 nm, at 2000 µm (805 mV) in 90 nm and at 3000 µm (847 mV) in 65 nm, based on the *dV/dt* characteristics of the aggressor pulse. The width of the crosstalk pulse however keeps increasing with increasing line length and reaches a maximum value of approximately 1.2 ns at 5000 µm in all four technologies as shown in **Table 4**.

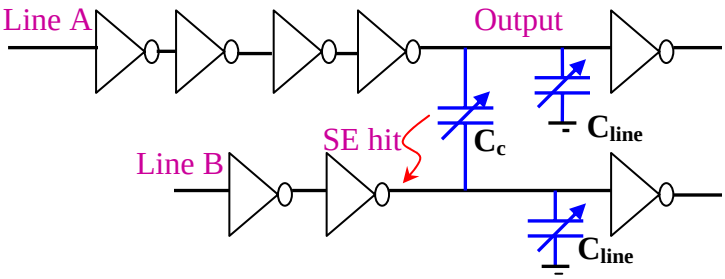


Figure 33. Circuit used to quantify the effect of SE induced crosstalk as a function of varying interconnect lengths (Varying C_c and C_{line})

Table 4. Maximum Crosstalk Pulse Height and Width as a function of varying interconnect lengths over a range of technologies

Technology	Maximum Crosstalk Pulse Height (mV)	Length at which Maximum Crosstalk Pulse Height Occurs (µm)	Maximum Crosstalk Pulse Width (ns) at 5000 µm length
180 nm	606	1000	~ 1.2
130 nm	605	2000	~ 1.2
90 nm	762	2500	~ 1.2
65 nm	869	2500	~ 1.2

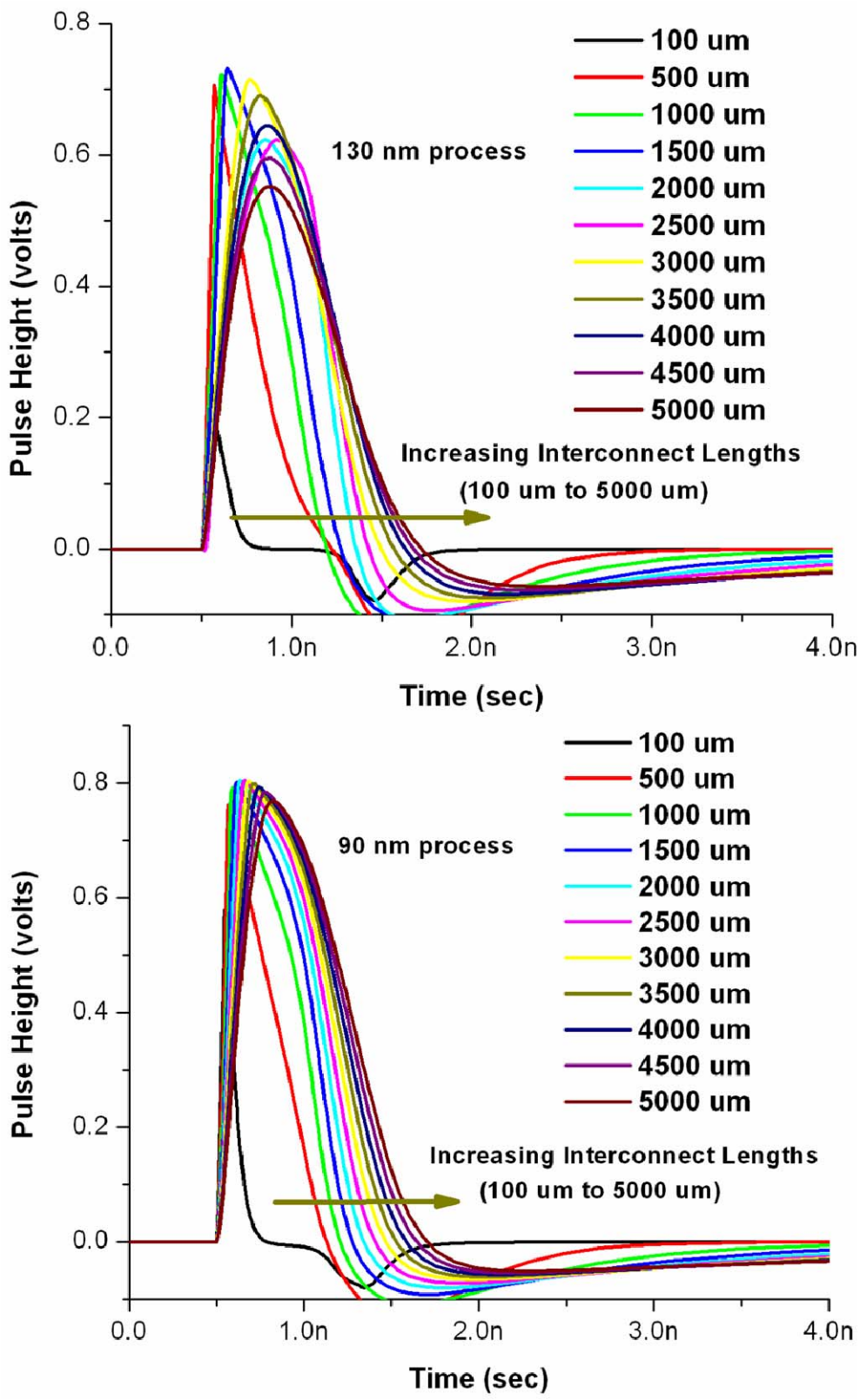


Figure 34. Crosstalk pulse measured on *Line A* for varying interconnects (100 μm to 5000 μm) for a p-hit on *Line B* for the 130 nm process (top) and the 90 nm process (bottom)

The crosstalk pulse on the passive node is a direct result of the change in the hit node voltage. As *dV/dt* of the hit node increases, the resulting crosstalk pulse height on the victim node increases. As long as *dV/dt* on the aggressor node is non-zero, a crosstalk pulse will be induced on the victim node. **Figure 35** shows the *dV/dt* curves for the rise and fall times in the IBM 130 nm technology for various interconnect line lengths and **Figure 36** shows the corresponding crosstalk pulses on the victim lines (a subset of **Figure 34**). The initial change in node voltage is similar for all line lengths up to those when the charge stored on the hit node (C * ΔV) is comparable to prompt charge collection. This is because prompt charge is collected within the first hundred picoseconds (96 ps for simulations performed) of the hit and the resulting change in node voltage will be fast and results in similar *dV/dt* curves for most interconnects. Consequently, the rising slope of the crosstalk pulse is similar for all cases except for large capacitances. The falling slope of the crosstalk pulse depends to a larger extent on the interconnect length and differs in each case. Three scenarios exist here: (i) small line lengths (smaller nodal capacitances), (ii) medium line lengths (medium nodal capacitances) and (iii) long line lengths (large nodal capacitances). For smaller nodal capacitances, the devices connected to the hit node are able to quickly revert the hit node voltage to its original value. For these line lengths, the pulse width is small as the hit node recovers quickly resulting in a crosstalk pulse that peaks and also recovers quickly as seen from **Figures 35** and **36**. For larger capacitances, the hit node voltage does not change all the way from rail to rail, due to the large capacitances associated with the node. As a result, the recovery time (or *dV/dt* for recovery voltage) slows (as the hit inverter dimensions are kept identical for the various interconnect lengths). This results in

drawn out crosstalk pulses at longer line lengths with diminished pulse amplitude as seen in **Figure 35** and **36**. The peak value in the crosstalk pulse height indicates a peak value in *dV/dt*. For medium line lengths, the speed of restoring operation is slow and the amount of charge is large resulting in the worst-case scenario as shown in **Figure 35**. Thus the medium line lengths result in relatively drawn out pulses with peak values exceeding the threshold voltages of transistors in this technology as seen in **Figure 36**.

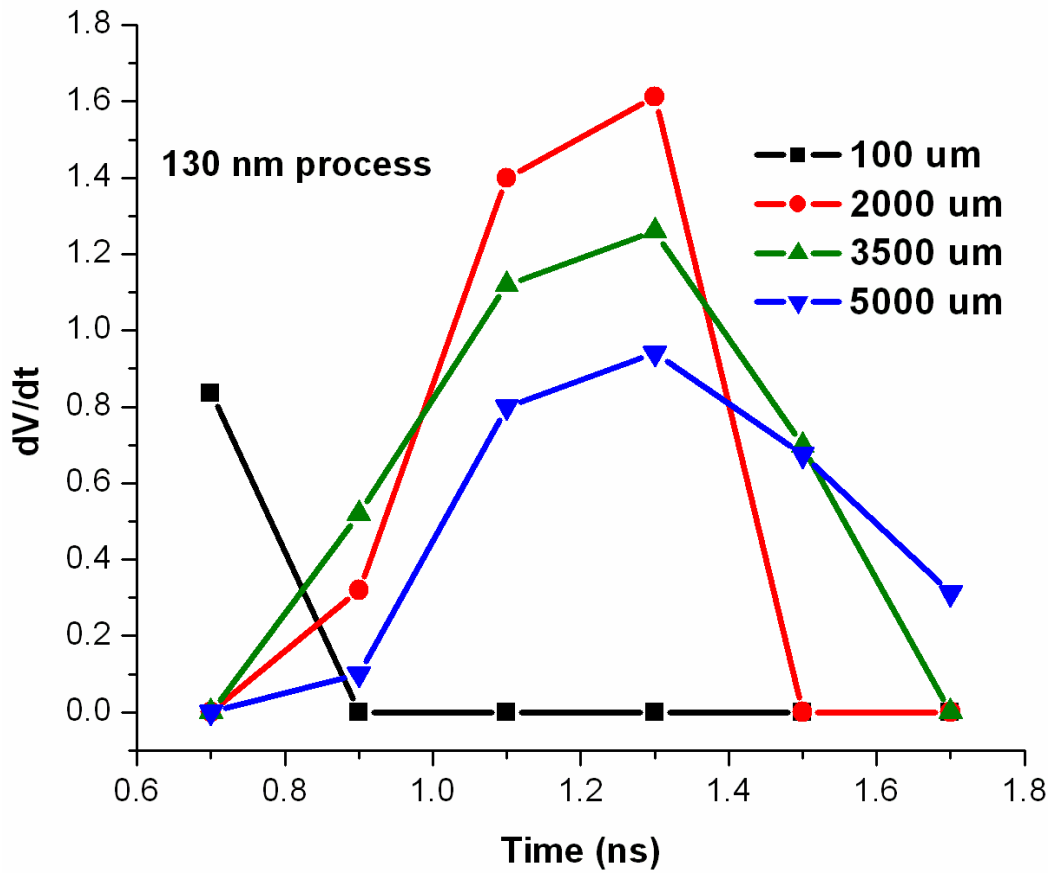


Figure 35. Crosstalk pulse dependence on *dV/dt*

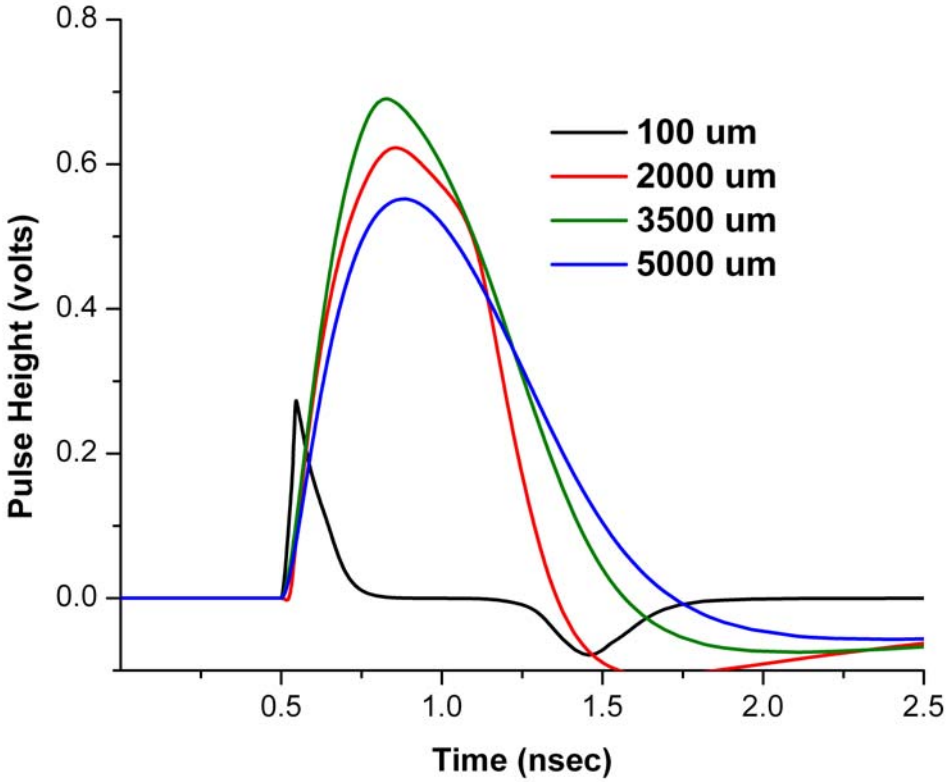


Figure 36. Crosstalk pulse measured on *Line A* for varying interconnects corresponding to Figure 35 for a p-hit on *Line B* for the IBM 130 nm process

Varying Collected Charge

As discussed previously, the decreasing transistor sizes in deep sub-micron technologies reduce the amount of charge required to represent a node voltage (in fCs). This in turn reduces the charge required to cause an SET, and this parameter was studied by simulating the circuit in **Figure 37** with varying deposited charge. **Figures 38a** and **38b** show the height and width of the crosstalk noise pulse on the victim node with incremental charge deposition from 50 fC to 1 pC in 90 nm and 65 nm technologies as a sample of the trends observed in all four processes. The height and width of the pulse increase with incremental charge deposited from 50 fC to 1 pC reaching a maximum of 904 mV in magnitude and 1.26 ns in width in 65 nm, 877 mV in magnitude and 1.25 ns

in width in 90 nm, 830 mV in magnitude and 1.26 ns in width in 130 nm, 665 mV in magnitude and 1.08 ns in width in 180 nm as detailed in **Table 5**.

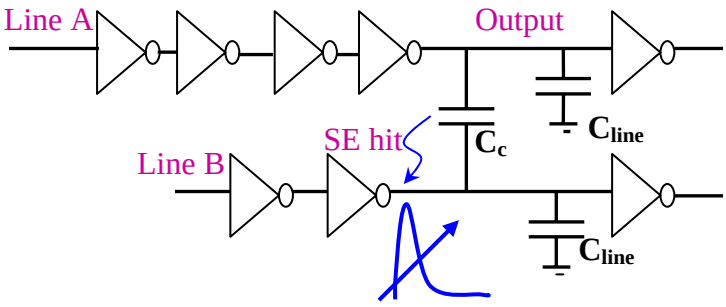


Figure 37. Circuit used to quantify the effect of SE induced crosstalk as a function of varying deposited charge (Varying current pulse)

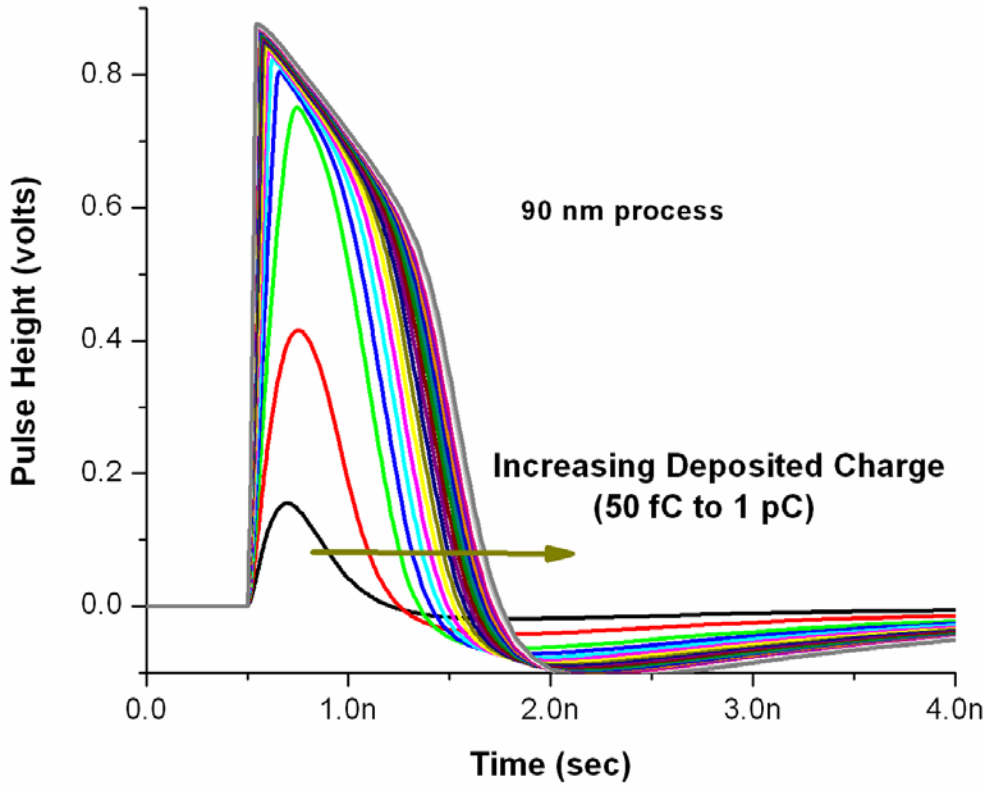


Figure 38a. Crosstalk pulse characteristics with increasing deposited charge for the 90 nm process

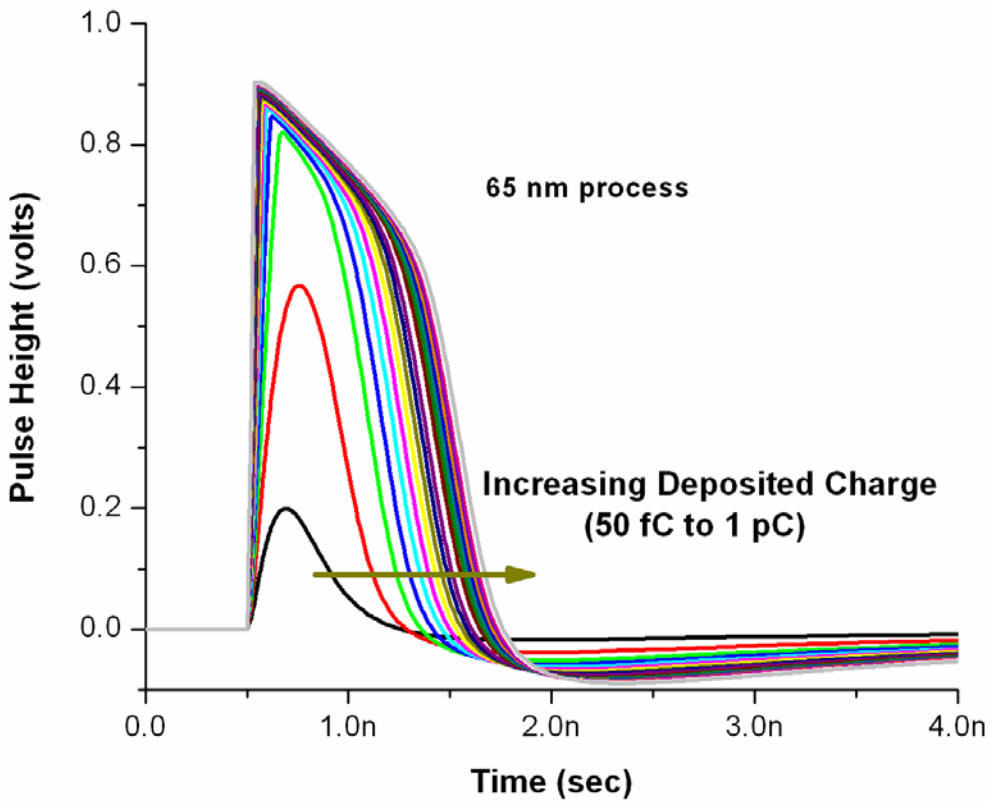


Figure 38b. Crosstalk pulse characteristics with increasing deposited charge for the 65 nm process

Table 5. Maximum Crosstalk Pulse Height for each technology as deposited charge was varied (50 fC to 1 pC)

Technology	Height (mV)	Width (ns)
180 nm	665	1.08
130 nm	830	1.26
90 nm	877	1.25
65 nm	904	1.26

Scaling

The next set of simulations emphasizes the importance of studying the effects of crosstalk in scaling technologies. The increased SE crosstalk coupling as technologies scale, cause a bigger glitch, which can be captured by the circuitry in the next stage

leading to an incorrect logic signal. **Figure 39** plots the crosstalk pulse height as a function of deposited charge for different technologies. In smaller technologies, the crosstalk pulse reaches it maximum height at small amounts of deposited charge (approximately 50 -100 fC). The *dV/dt* curves for these technologies also show a similar trend. As observed in **Figure 39**, in the 65 nm technology, the charge required to reach the saturated crosstalk pulse peak (identical *dV/dt* transition) (~ 120 fC) is much lesser than the charge required in the IBM 130 nm (~ 200 fC) due to lower capacitances and lower device currents.

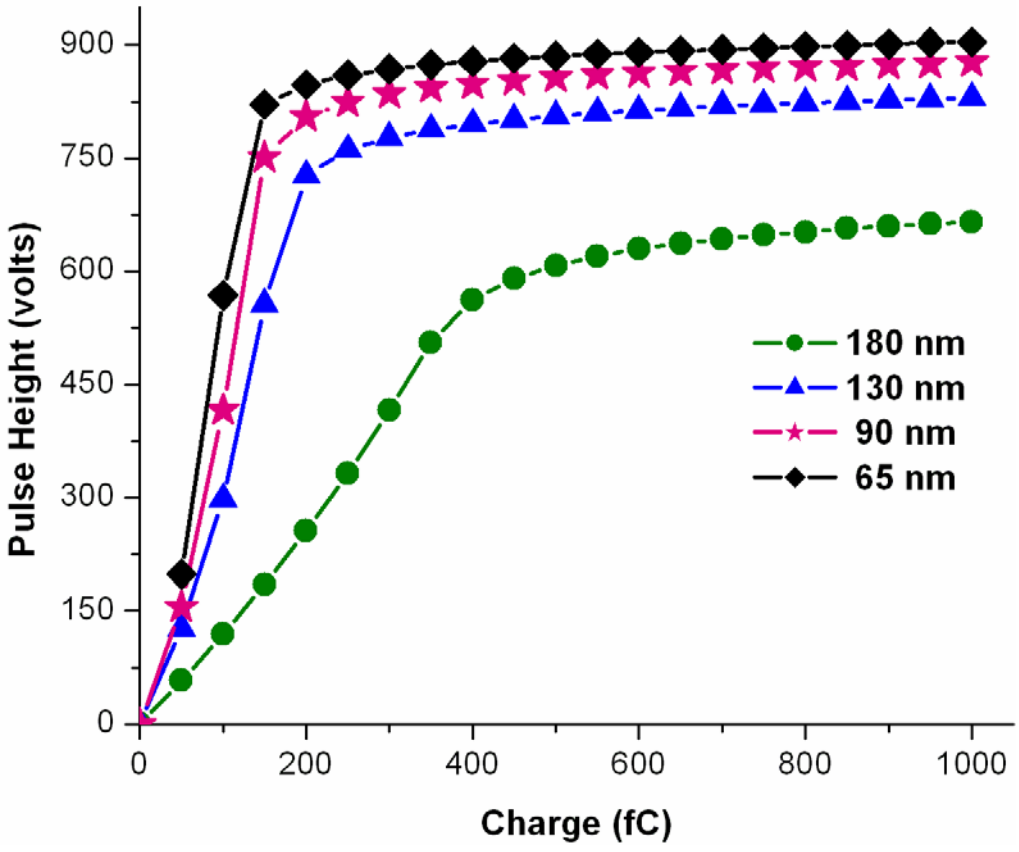


Figure 39. Reduced collected charge required for crosstalk effects with scaling

The simulations performed in this section help determine the parameters that affect the characteristics of the SE crosstalk pulse which are - the *dV/dt* of the aggressor pulse voltage, interconnect length, deposited charge and scaling technologies. However all the simulations in this section were at a circuit level and did not encompass any mixed-mode simulations at the device level. Certain issues exist with just using this approach which are discussed in more detail in following section.

Issues with Spectre level simulations

One of the major issues with this approach is the use of only the double exponential current pulse to model the SE hit. Though the double exponential current pulse is widely used and accurate in predicting circuit performance and trends for the most part, it fails to suffice as we scale into 90 nm and beyond [74], [75]. As discussed in Chapter II, the double exponential current pulse is described by charge collection models involving drift and diffusion across the drain body junction [45], [52], [65], [67], [68], and mostly assumes a constant built-in potential for the junction during the entire duration of the single-event voltage transient. These models hold good for technologies with micron scale dimensions and prove sufficiently accurate for investigating SEEs on CMOS devices and circuits using compact models and circuit-level simulators (such as SPICE). However, as we scale into deep sub-micron (130 nm, 90 nm and beyond), the redistribution of electric fields resulting from an ion strike, affect multiple nodes and contacts. This in turn causes a distinct change in the shape of the current pulse. Characterizing SEs and SETs through Technology Computer-Aided Design (TCAD) simulations result in a transient waveform significantly different from the familiar double

exponential shape [62], [72] – [75]. Moreover, circuit level simulations fail to account for device level effects such as parasitic bipolar turn on, charge sharing between multiple nodes [74], [75] and the focus of this work *"SE induced crosstalk"*. In addition to these reasons, since the *dV/dt* of the *aggressor* pulse influences the response of the *victim* crosstalk pulse to a great extent, it is vital to model that precisely. Having identified the trends using circuit level simulations, the second part of this chapter focuses on investigating these effects through 3D mixed-mode simulations using 3D mixed-mode calibrated current pulses in the IBM 90 nm CMOS9SF process.

3D Mixed-Mode Simulations: IBM 90 nm CMOS9SF process

Comprehensive simulations were performed in the IBM 90 nm CMOS9SF process using the Cadence® EDA toolset and 3D Technology Computer Aided Design (TCAD) structures developed with Synopsis® DEVISE and DESSIS simulator using scaled structural information available from multiple sources [123], [124], to further characterize the parameters affecting SE crosstalk. All simulations were conducted using the ACCRE computing cluster [130]. The NMOS and PMOS devices (for the inverters highlighted in RED and BLUE in **Figure 40**) were calibrated to match electrical characteristics (I_d - V_d and I_d - V_g curves) obtained from the standard compact models for this technology. The IBM 90 nm CMOS9SF process has dual operating voltages of 1.2 V and 1 V, and simulations were performed at both these supply voltages. Single Event simulations were performed to determine charge collection on the "hit" device on the *active* line and its effects on the "victim" device on the *passive* line due to interconnect crosstalk coupling. All single events were performed with the "heavy-ion" command in

DESSIS. A SE hit was simulated in all cases on the drain of the second inverter on line B (RED inverter in **Figure 40**) and the output observed at the *S Input* to the latch. All parasitic capacitance values like C_c (the parasitic capacitance between two metal layers) and C_{line} (the parasitic capacitance between metal to substrate) were estimated using the 2D Synopsys® TCAD simulation as described earlier.

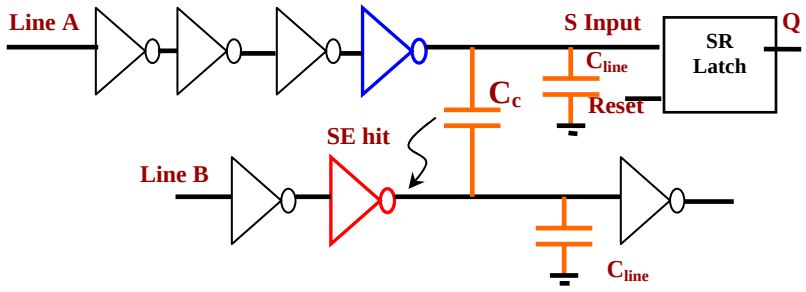


Figure 40. Circuit used to quantify the effects of crosstalk (SE hit simulated in each case at the drain of the 2nd inverter and crosstalk pulse observed at node S Input for simulations). Inverters highlighted in red and blue modeled in 3D TCAD.

Figure 41 shows the 3D TCAD devices (2 PMOS/NMOS transistors of the highlighted inverters in **Figure 40**) for the case of a p-hit/n-hit. A SE strike on the PMOS transistor is termed a p-hit and a SE strike on the NMOS transistor is termed an n-hit. All the simulations were conducted for strikes normal to the surface of the structure. **Figures 42a** and **42b** show the SE hit current pulses for a p-hit and an n-hit respectively, for a few sample LETs obtained from a matched-current-drive inverter chain. Similar current pulses were generated with the "heavy-ion" command in DESSIS, at the hit node.

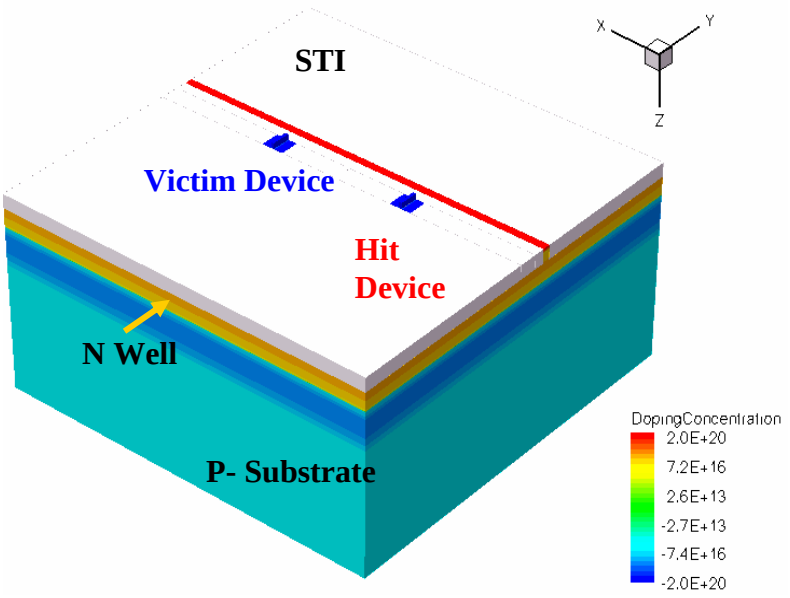


Figure 41. 3D TCAD devices showing the *Hit* device on Line B and the *Victim* device on Line A

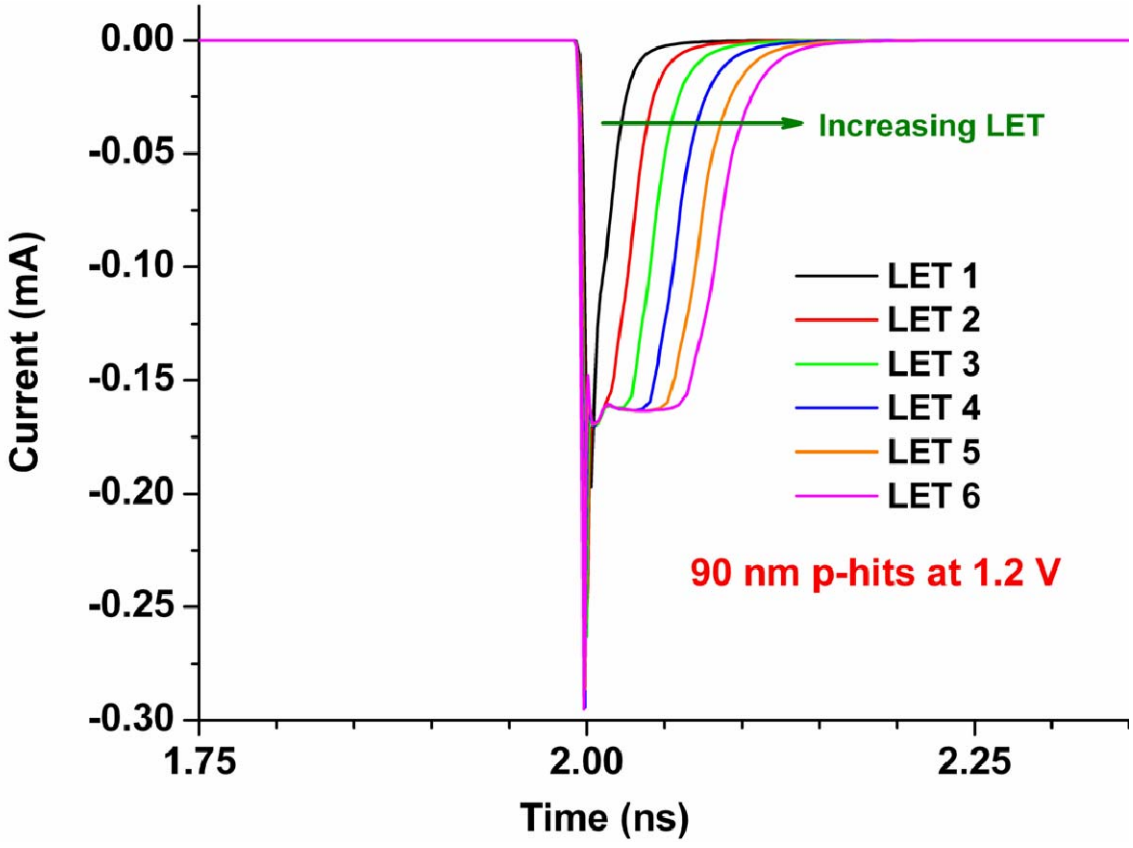


Figure 42a. Current pulses measured at the drain of the PMOS device modeled in 3D TCAD in a chain of 4 matched-current-drive inverters

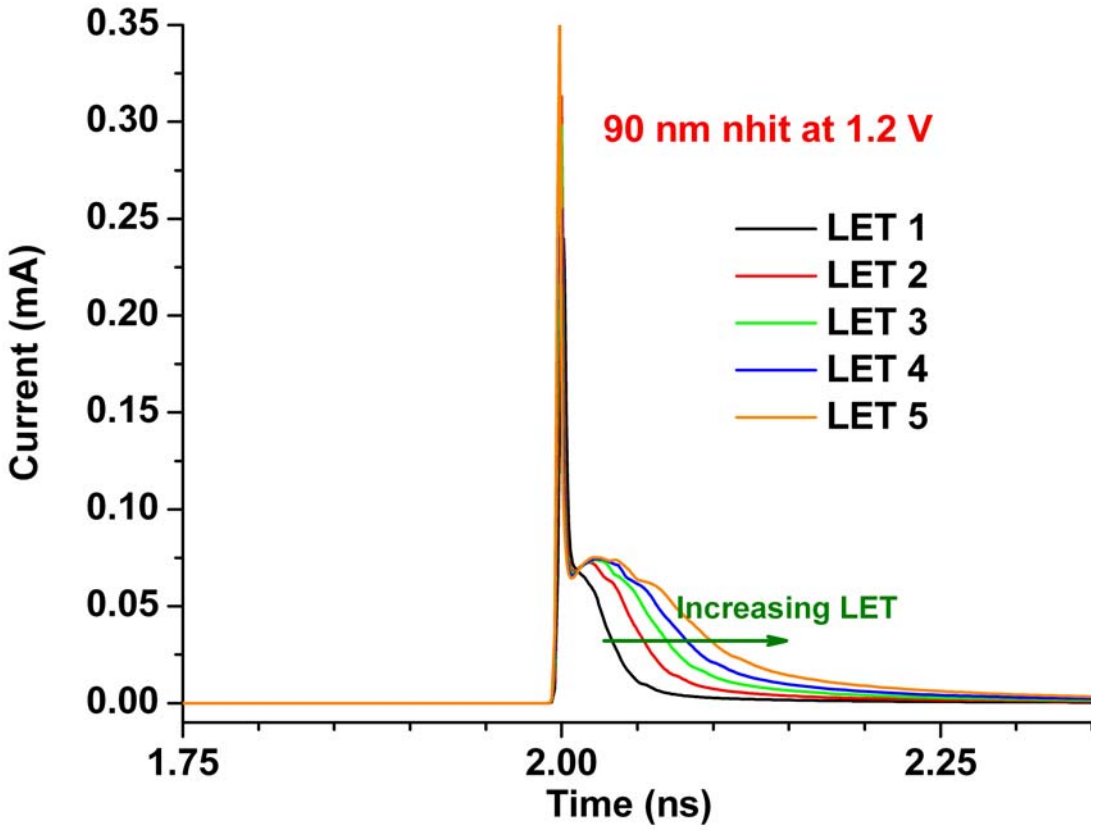


Figure **42b**. Current pulses measured at the drain of the NMOS device modeled in 3D TCAD in a chain of 4 matched-current-drive inverters

Aggressor Current and Voltage Pulses: IBM 90 nm CMOS9SF process

Since the characteristics of the SE hit current pulse determine the *aggressor* pulse characteristics, it is important to understand the factors that influence it. As we scale into sub-100 nm CMOS technologies, parasitic elements in the CMOS structure lead to significantly different PMOS and NMOS device charge collection characteristics, which in turn lead to distinct current pulses. The amount of charge collected at a struck node (i.e., Linear Energy Transfer - LET) is composed of the sum of drift, diffusion, and parasitic bipolar amplification of the SE related currents [31], and can vary between the NMOS and PMOS devices for a given technology. Amusan *et al.* and Dasgupta *et al.* have studied the charge collection mechanisms in 130 and 90 nm processes and have

shown PMOS charge collection to result in longer pulse widths over the matched-current-drive NMOS devices [131] – [133]. The longer pulse widths in the PMOS devices have been identified due to parasitic bipolar amplification [131], [134] – [138]. **Figure 43** shows a 2D cross-section view of a CMOS device identifying the parasitic elements [131], which helps explain this effect. As identified previously, the primary reason for this enhanced amplification is the collection of electrons in the n-well from deposited charge, reducing the n-well potential. This drop in n-well potential combined with the additional carriers in the substrate due to the ion strike; activate the parasitic PNP bipolar transistor, resulting in higher charge collection and longer SET pulse widths. However the concentration of minority carriers (for the hit device) is not very high for the p-well (NMOS) due to the absence of any regions for charge confinement making drift and diffusion currents in the p-well the dominant charge collection mechanism for the NMOS device [131].

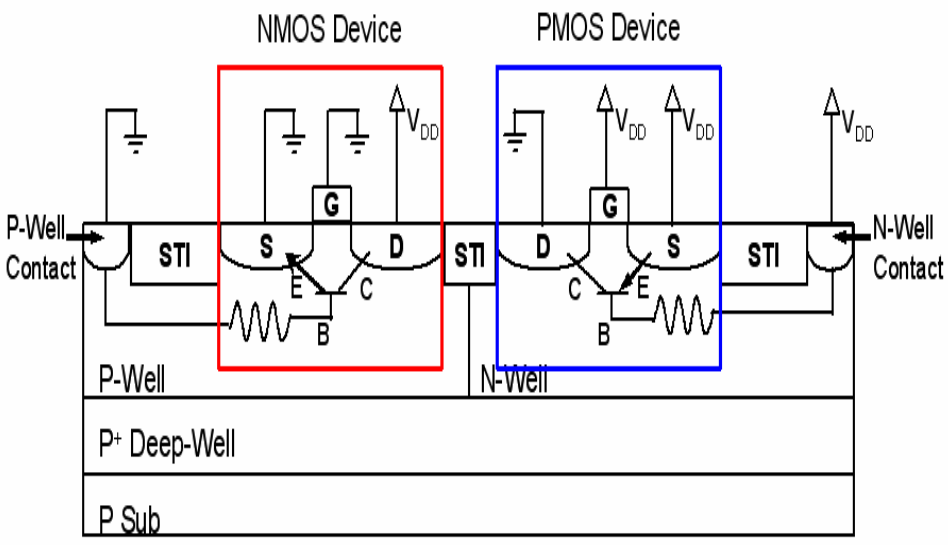


Figure 43. CMOS cross section showing parasitic elements. The NMOS device has a lateral parasitic npn bipolar transistor and the PMOS device has a lateral parasitic pnp bipolar transistor [131]

To illustrate the difference in the *aggressor* and *victim* pulses for this technology, simulation results for both a p- and an n-hit are presented for a 1000 µm long interconnect line with an LET of 40 MeV-cm^2/mg at a 1.2 V supply voltage. The devices calibrated and shown in **Figure 41** were used. **Figure 44a** shows the *aggressor* current and voltage pulse at the hit device and the voltage pulse at the victim device on the *passive* line for a 1000 µm long line for an LET of 40 MeV-cm^2/mg for two PMOS devices for a p-hit. **Figure 44b** presents the analogous results for two NMOS devices for an n-hit. The results obtained show that the voltage pulses behave according to the characteristics of the current pulse which are different for both cases as identified. The rate of change of current *dI/dt*, causes a corresponding *dV/dt* in the *aggressor* voltage pulse that is coupled to the *passive* voltage pulse as visible in these figures.

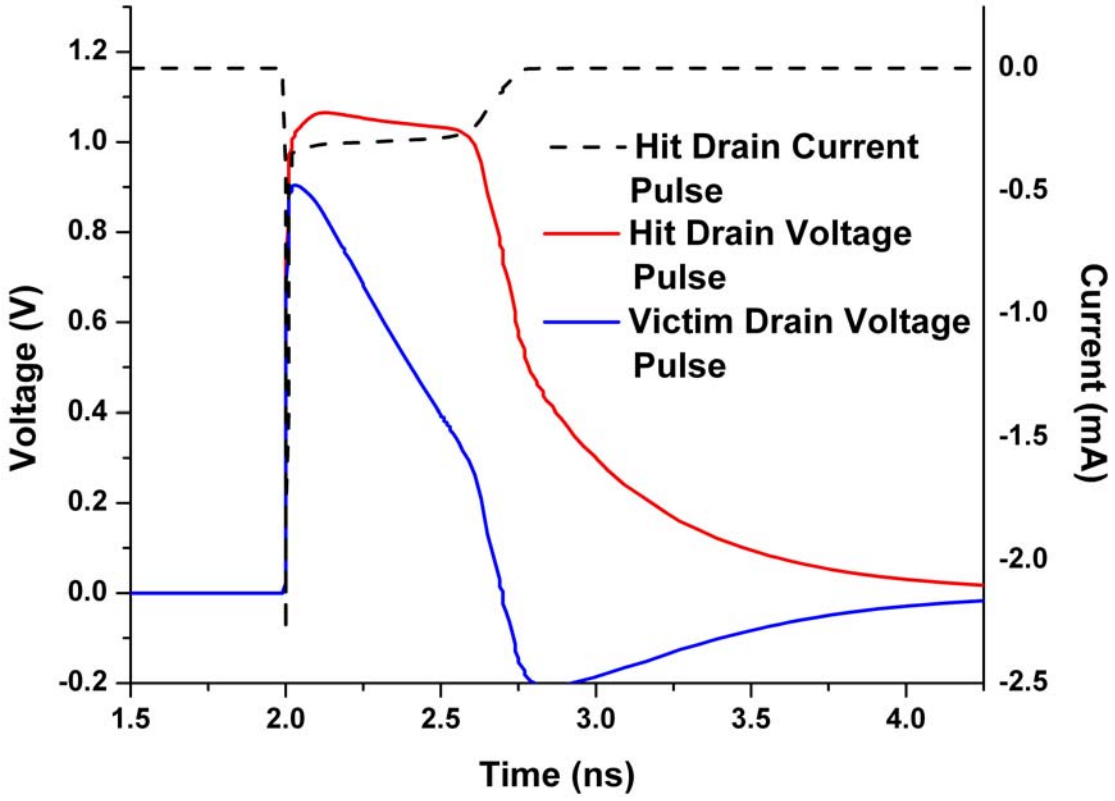


Figure 44a. Voltage (Hit and Victim node) and Current Pulse (Hit node) for two PMOS devices for a 1000 µm long line for an LET of 40 MeV-cm^2/mg at a 1.2 V supply voltage

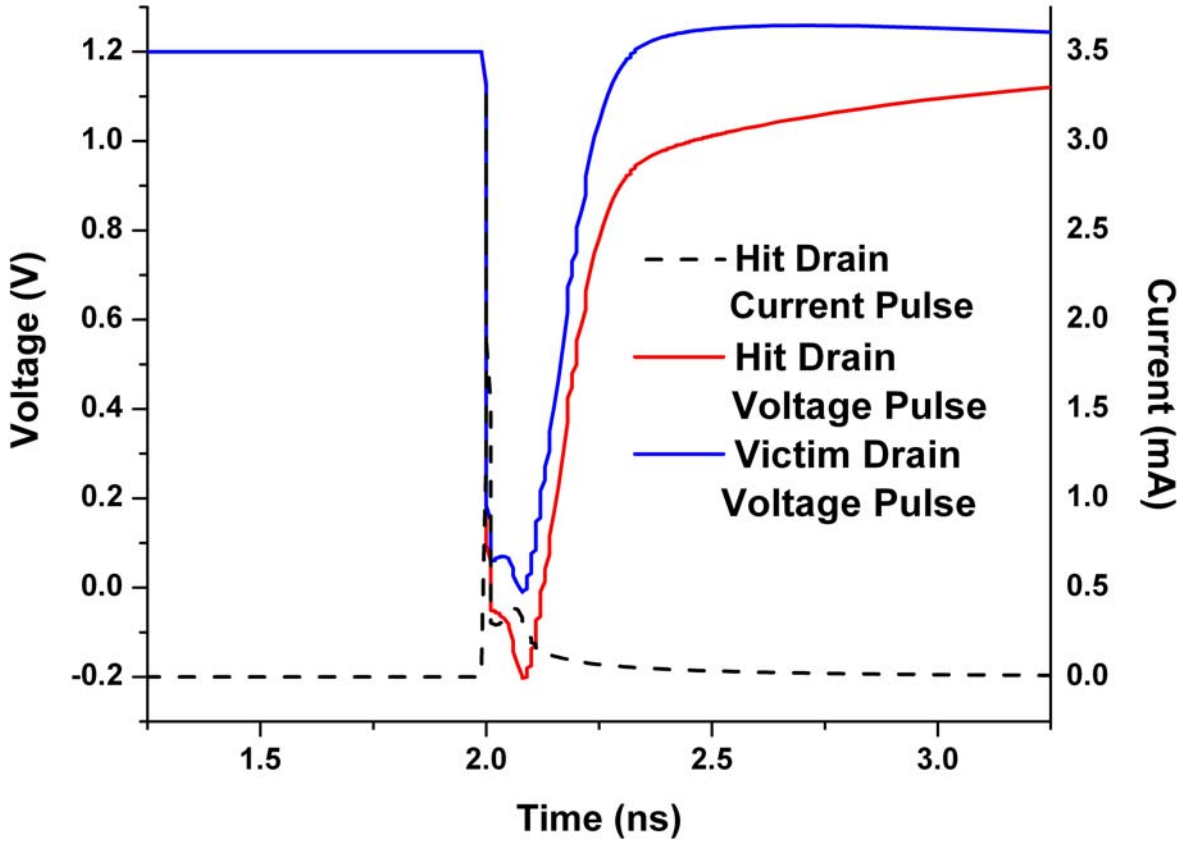


Figure 44b. Voltage (Hit and Victim node) and Current Pulse (Hit node) for two NMOS devices for a 1000 µm long line for an LET of 40 MeV-cm^2/mg at a 1.2 V supply voltage

Isolating SE induced crosstalk effects

To isolate the effects observed as those only due to SE induced crosstalk, the devices were spaced far apart (2 µm) to avoid any charge sharing mechanisms [131]. **Figure 45** presents the current pulses at the hit or *active* drain and on the victim or *passive* drain for a p-hit (strike on the PMOS transistor) for an LET of 40 MeV-cm^2/mg. **Figure 46** shows the voltage transient pulses on the *active* and the *passive* nodes in the absence of any crosstalk coupling or charge sharing (2 µm spacing) when a SE p- hit (LET of 40 MeV-cm^2/mg) was simulated on the PMOS transistor on *Line B.* This serves as a reference and isolates all the effects observed henceforth as those only due to SE induced crosstalk alone; as the same device spacing was maintained in all cases. Simulations were carried

out for the different parameters identified previously, such as interconnect lengths and deposited charge both for a p- and an n-hit case using calibrated 3D mixed-mode current pulses. The results are presented for a supply voltage of 1.2 V and 1 V for four different interconnect lengths (150 µm, 500 µm, 1000 µm and 2000 µm) at LETs of 10, 20, 30 and 40 MeV-cm^2/mg. Results obtained at 1 V show that the effect is exacerbated at lower operating voltages.

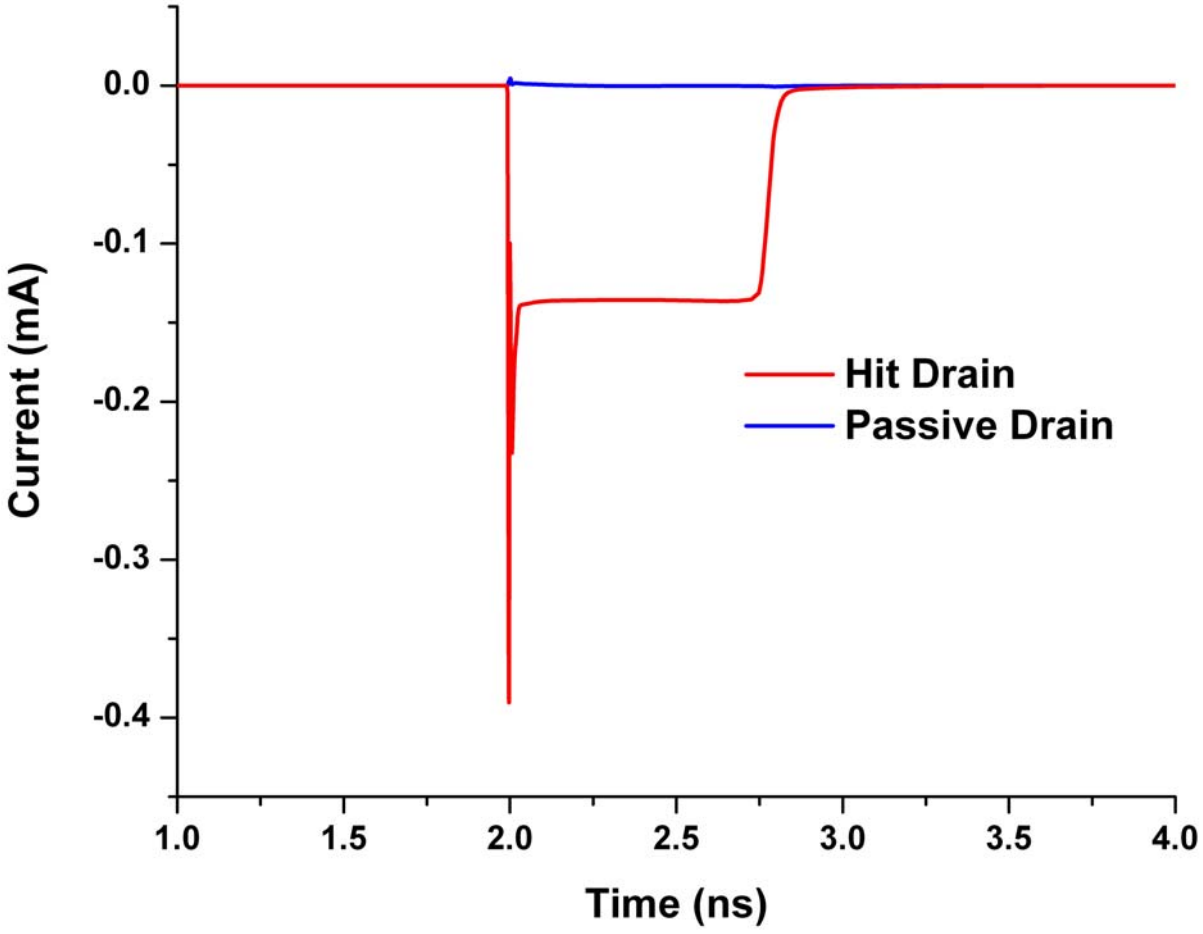


Figure 45. Current pulses at the struck node (hit drain) and at the victim node (passive drain) in the absence of any crosstalk coupling (spaced 2 µm apart) for an LET of 40 MeV-cm^2/mg

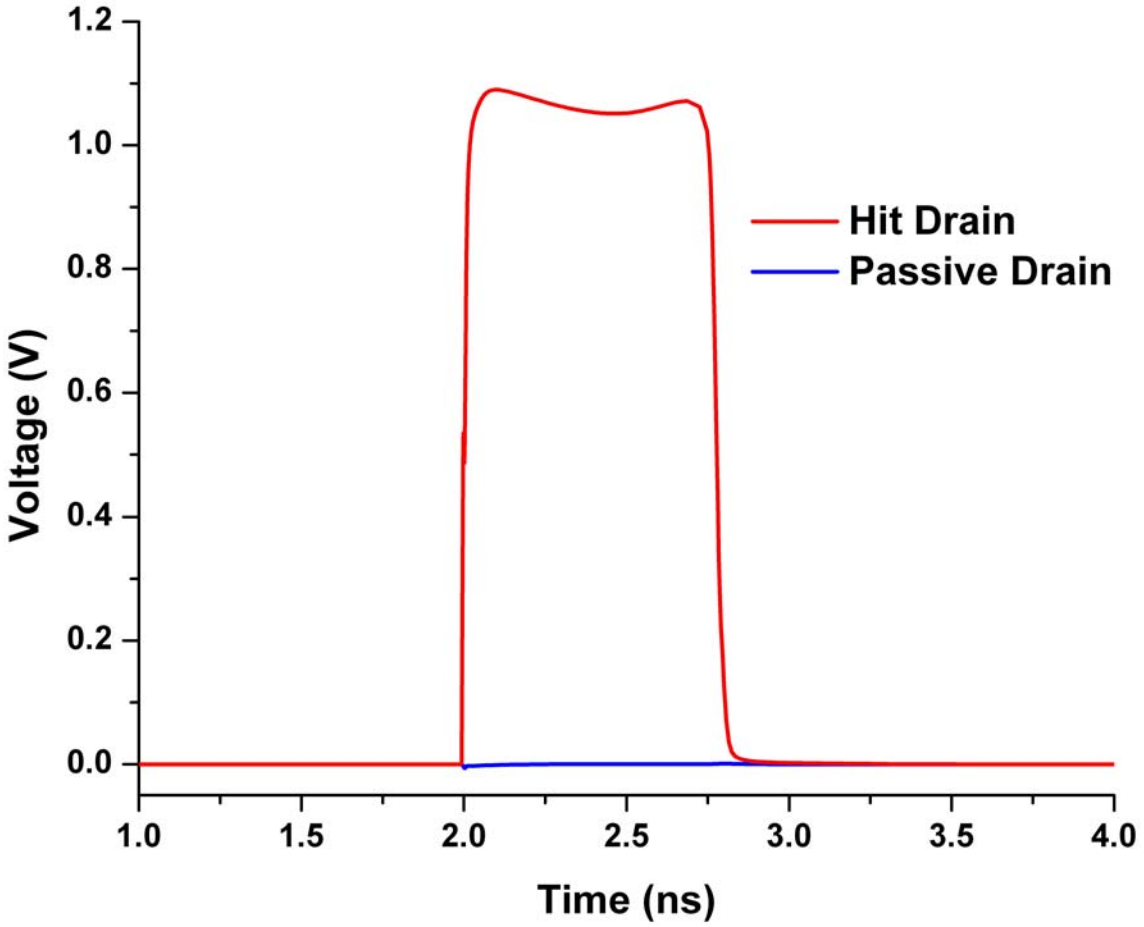


Figure 46. Voltage pulses at the struck node (hit drain) and at the victim node (passive drain) in the absence of any crosstalk coupling (spaced 2 µm apart) for an LET of 40 MeV-cm^2/mg

Interconnect Lengths

Figures 47 and **48** present the simulated crosstalk coupling transient pulse at a 1.2 V supply voltage and an LET of 40 MeV-cm^2/mg for an n-hit and a p-hit respectively. **Figure 49** presents the results for an n-hit at a 1 V and 1.2 V supply voltage at the same LET for two sample interconnect lengths. The crosstalk pulse widens with increasing interconnect lengths as seen in the previous section with simulations using the double exponential pulses in **Figures 34** and **36**. At lower operating voltages the crosstalk pulse

reaches the supply rail and is well above the threshold for upset for transistors in this technology leading to an SET on the passive line.

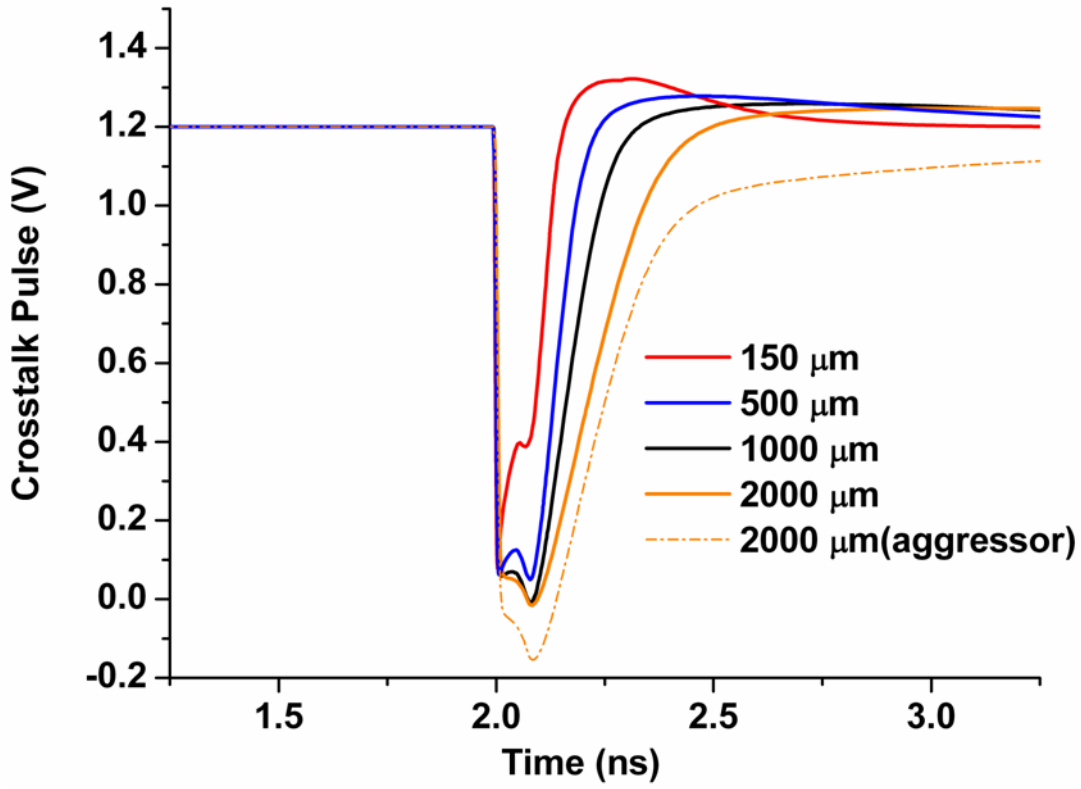


Figure 47. Simulation results showing the crosstalk pulse on the passive node as the interconnect length increases at V_{dd} =1.2 V for an n-hit at an LET of 40 MeV-cm^2/mg; and the aggressor pulse for a sample case

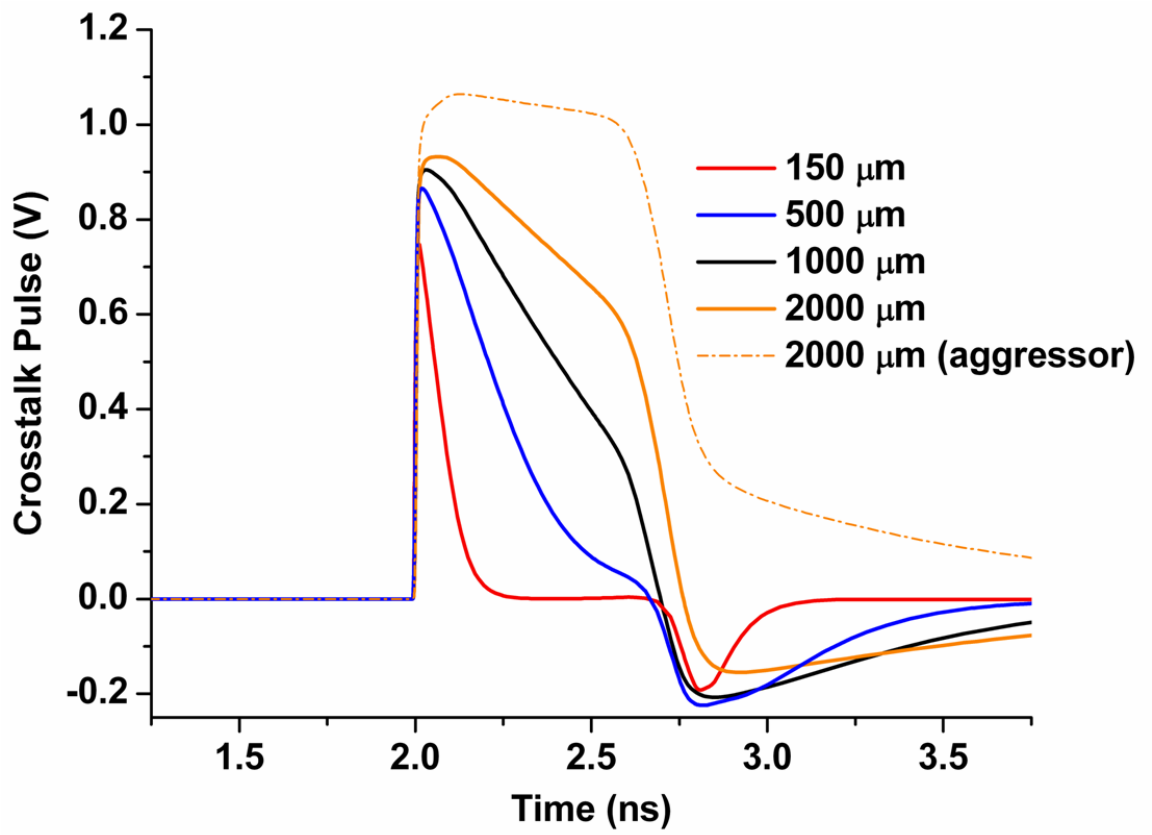


Figure 48. Simulation results showing the crosstalk pulse on the passive node as the interconnect length increases at V_{dd} =1.2 V for a p-hit at an LET of 40 MeV-cm^2/mg; and the aggressor pulse for a sample case

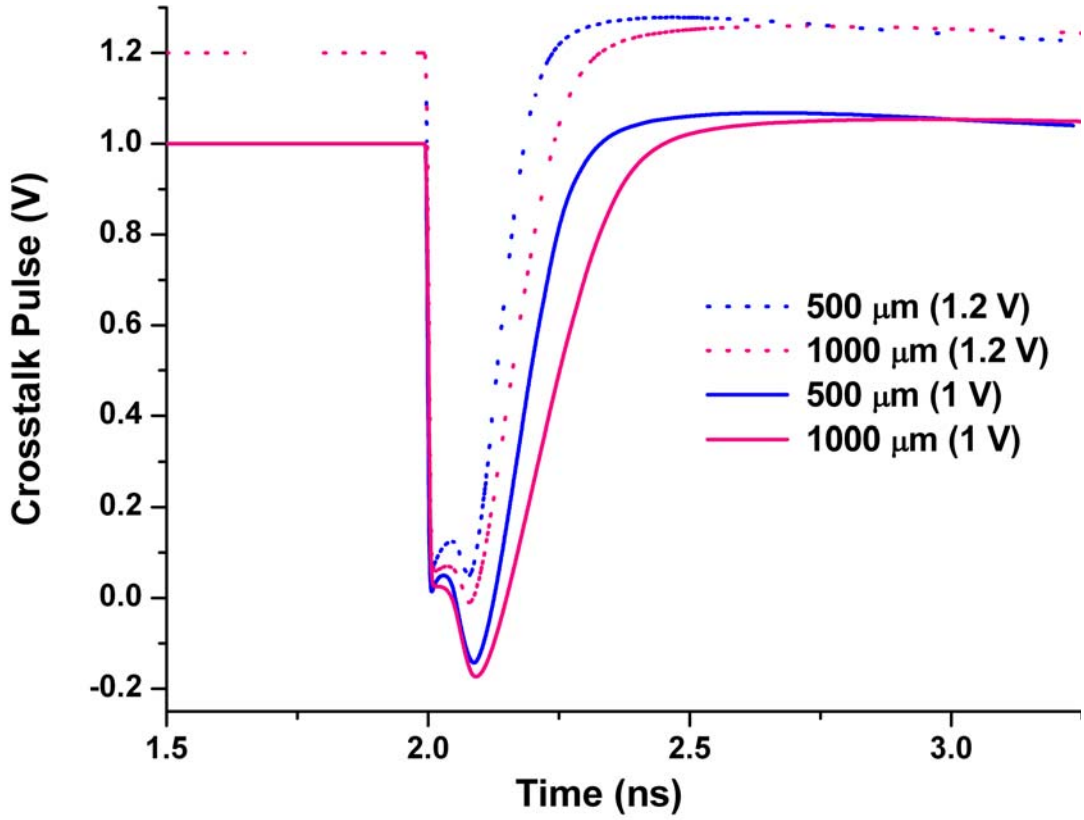


Figure 49. Simulation results showing the crosstalk pulse on the passive node as the interconnect length increases for both the supply voltages for an n-hit at an LET of 40 MeV-cm^2/mg

Supply Voltages

Figure 50 presents the crosstalk pulse for a p-hit case at a 1.2 V supply voltage for a line length of 1000 μm and **Figure 51** shows the crosstalk transient pulse for an n-hit at both operating voltages for a line length of 1000 μm, both over a range of deposited charge. **Figure 52** presents the crosstalk pulse width at Full Width Half Rail (FWHR) on the passive line at both these operating voltages for a 500 μm and 1000 μm long interconnect line for an n-hit case. Similar results were obtained for the p-hit case. With increasing deposited charge the crosstalk pulse width at the full width half rail continues to increase slightly for both p- and n- hits. However strikes on PMOS devices result in

longer pulse widths as identified previously [131]. Reduction in the supply voltage from 1.2 V to 1 V leads to an average increase of about 40 % in the crosstalk pulse width.

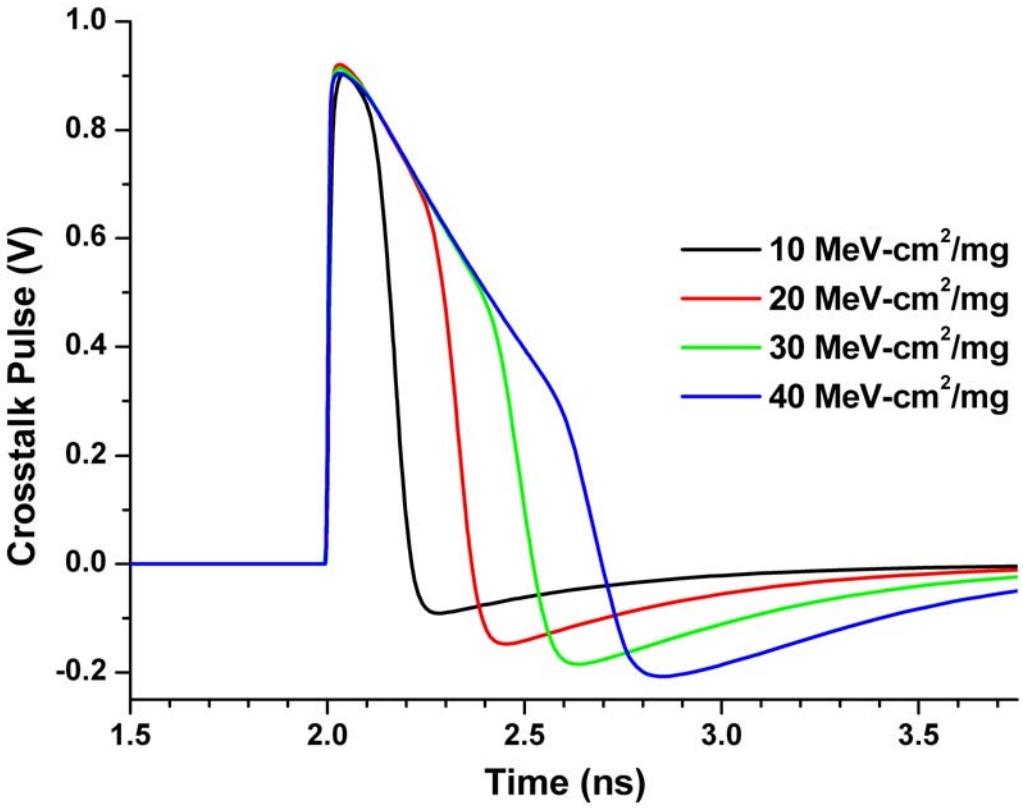


Figure 50. Simulation results showing the crosstalk pulse on the passive node as the deposited charge increases at V_{dd} =1.2 V for a p-hit for a 1000 µm long interconnect line

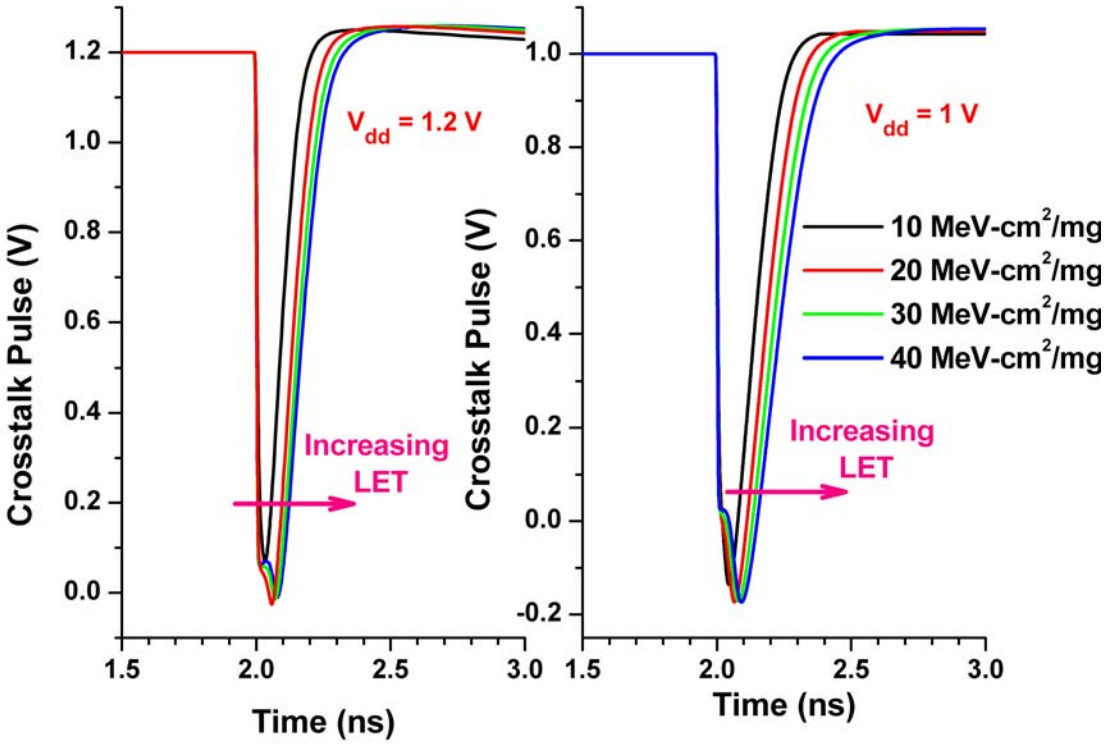


Figure 51. Simulation results showing the crosstalk pulse on the passive node as the deposited charge increases at both the supply voltages for an n-hit for a 1000 µm long interconnect line

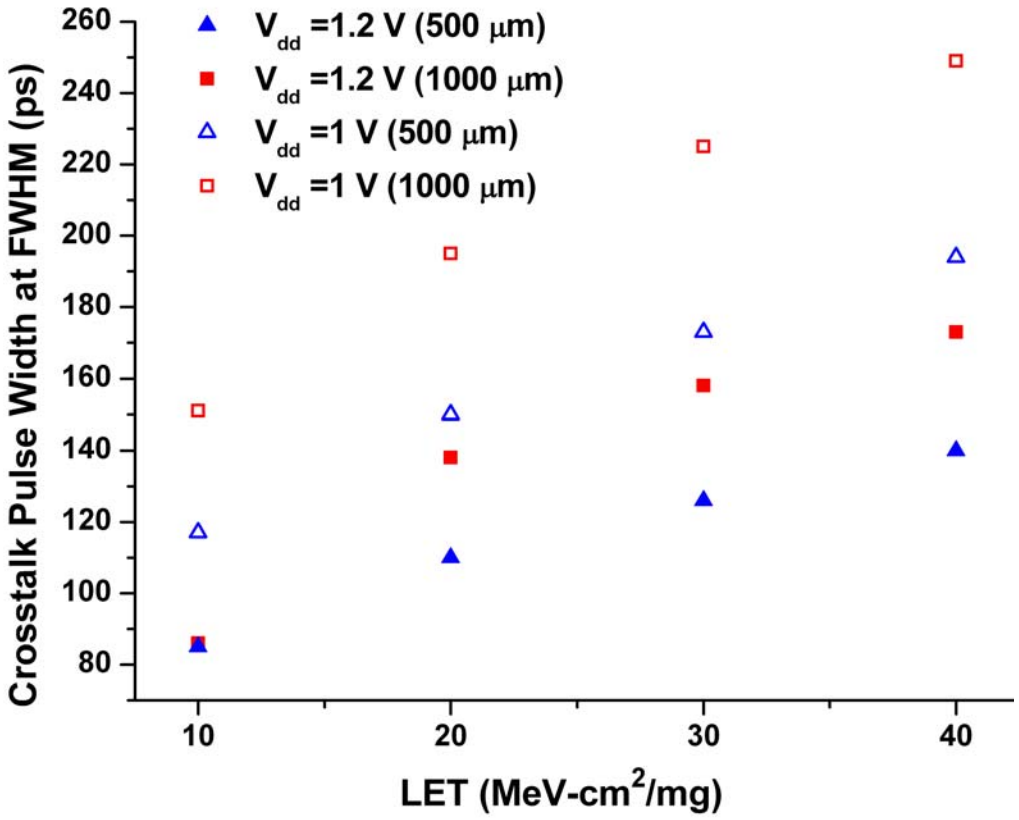


Figure 52. Increasing crosstalk pulse width at full width half rail at two supply voltages for 500 μm and 1000 μm long interconnect lines (n – hit)

When compared to the results in the first section of this chapter, it can be determined that the shape of the crosstalk voltage transient pulse is different in both the cases. This occurs due to the different shape of the current pulse (double exponential vs. 3D mixed-mode) causing the SE in each case. However the trends identified remain consistent for the various parameters studied. Thus, as seen from the results, in this technology and with scaling, the current pulse is no longer effectively modeled by a double exponential and is different for a p- and an n-hit [131] - [133]. It has already been demonstrated by DasGupta that the voltage transient at the hit node depends on the rise/fall times of the current pulse [75] and is distinctly different for a strike on the PMOS and on the NMOS

transistor in this technology. Since SE interconnect crosstalk primarily depends on the *dV/dt* of the aggressor pulse voltage, the rise/fall time of the current pulse (different for p- and n- hits) strongly affects the behavior with increasing charge deposition and scaling technologies as demonstrated in this chapter. Chapter VI presents the experimental results from both single- and two- photon laser absorption measurements performed to evaluate SE induced interconnect crosstalk.

CHAPTER VI

EXPERIMENTAL VERIFICATION OF SINGLE-EVENT INDUCED CROSSTALK

Though heavy-ion broadbeam testing may mimic the space radiation environment more accurately, a major disadvantage with this method of testing is its inability to isolate sensitive nodes for investigating new single-event (SE) phenomena. As an alternative, pulsed laser single-event upset tests are used to identify and characterize sensitive circuit nodes and provide information vital to the development and optimization of radiation-hardened designs. The pulsed laser is a powerful tool for the interrogation of SE phenomena in a range of complex integrated circuits including memories, logic circuits, microprocessors, and neural networks [139] - [143]. The primary advantage of this technique is its ability to locate and characterize sensitive nodes with sub-micron precision, without the concomitant damage associated with accelerator techniques [144] – [146]. When integrated into the design process, in particular, critical circuit evaluation with a laser often leads to not only the identification of the specific single-event effect (SEE) but also the most direct and cost effective solutions to the potential SEE.

The most common implementation of the pulsed laser technique is based on the excitation of carriers in a semiconductor material using tightly focused, above-bandgap optical excitation [139] – [153]. As carrier generation is governed primarily by Beer's law of absorption and, for a given material, the optical penetration depth is determined by the wavelength of the laser pulse. Recently, the pulsed laser has been used successfully in a range of investigations of SEE phenomena, including interrogation of the spatial and

temporal aspects of single-event upset (SEU) and single-event latch up (SEL) in a variety of digital circuits [140], [141], [144], investigation of the basic charge-collection mechanisms of individual transistors [147], as an essential tool for unraveling the complex SEE response of bipolar linear circuits [148] – [152], and most recently for evaluating the SE response of flip-chip mounted static random access memory (SRAM) using through-wafer (backside) irradiation [153].

Test Circuit Details

To measure SE induced crosstalk, specificity and exposure of only the sensitive area to radiation is vital for purposes of isolating the effect. For this purpose, pulsed laser experiments were performed at the Naval Research Laboratories, Washington. To provide an experimental verification of the SE induced crosstalk effect seen through mixed-mode simulations in Chapter V, the sample test circuit illustrated in **Figure 40** was fabricated in the MOSIS IBM 90 nm CMOS9SF process. As detailed earlier the fabricated circuit consists of a series of inverters on *line A* leading to the input of the SR latch, which represents the *passive* line. The inverters on *line B* represent the *active* line as shown in **Figure 53** (repeated here for clarity without the parasitic capacitances). Matched-current-drive inverters were used and a NAND based SR latch was implemented. Minimum device dimensions, interconnect line length and thickness allowed for this technology without violating any process design rules were used to simulate a worst-case condition. The crosstalk and line-to-ground capacitances are not shown separately but exist based on the length and proximity of the interconnect lines, and are the parasitic capacitances resulting from the layout. Three test structures with

interconnect length of 1500 µm, 2500 µm and 3500 µm were designed and tested. **Figure 54** shows the layout of a single setup and **Figure 55** displays the three setups designed. The drain of the second inverter in *Line B* was hit using a laser pulse and the output Q of the SR latch monitored for a voltage flip (upset) in every case. **Figure 56** shows the die photo of the circuit fabricated with the markers for the hit locations identified.

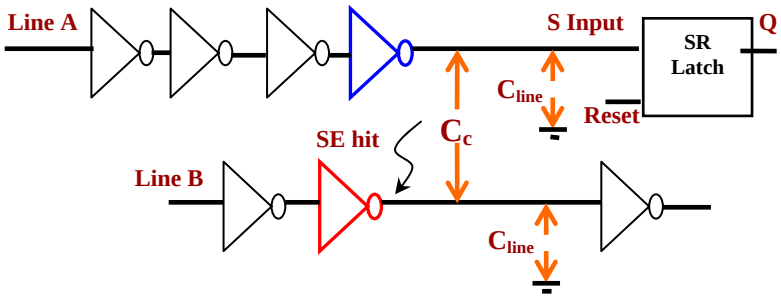


Figure 53. Circuit used to quantify the effects of crosstalk (SE hit simulated in each case at the drain of the 2nd inverter with a pulsed laser and output Q of the SR latch monitored for a voltage flip (upset) in every case. Parasitic capacitances C_c (between two metal lines) and C_{line} (between metal and substrate) result from the layout

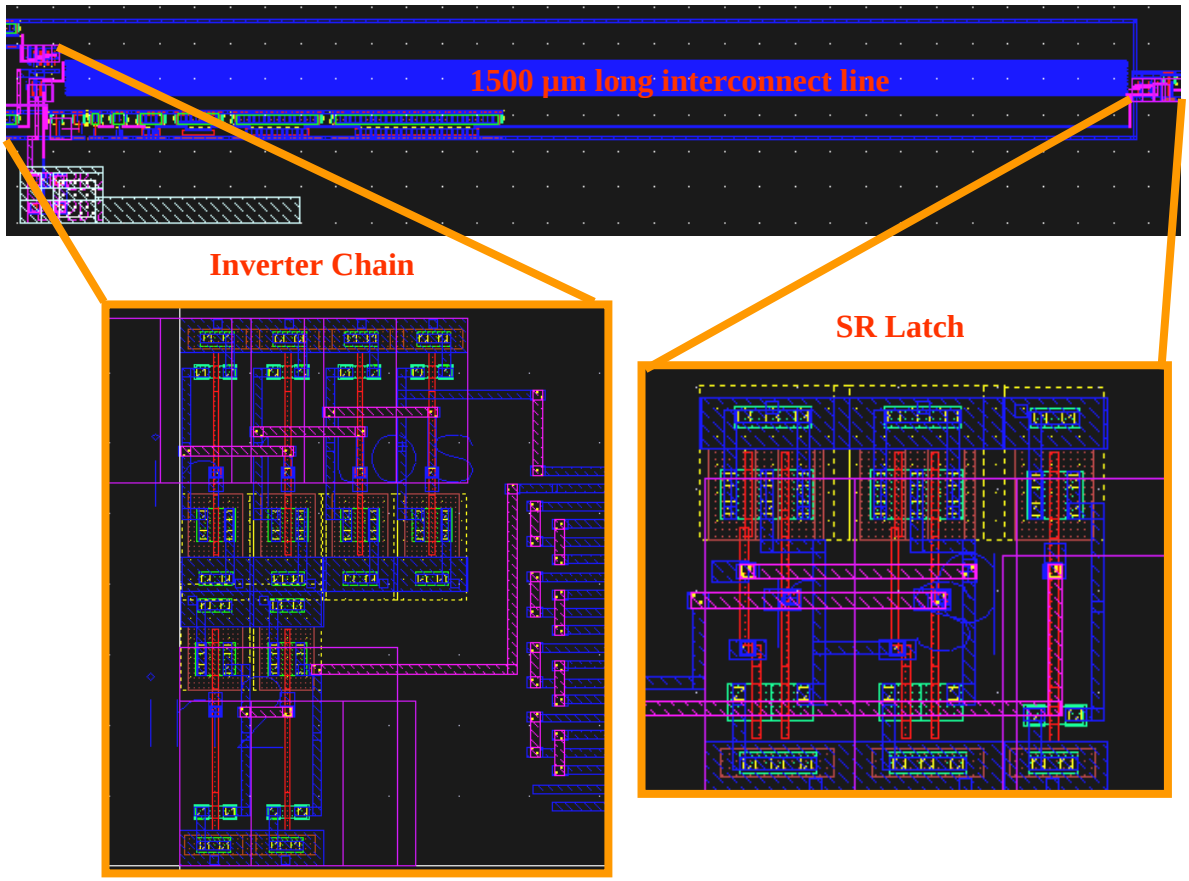


Figure 54. Layout of one of the three setups; with interconnect length of 1500 µm, and layouts of the inverter chain and the SR latch

Figure 55. Layout of the three crosstalk setups designed in the IBM 90 nm CMOS9SF process

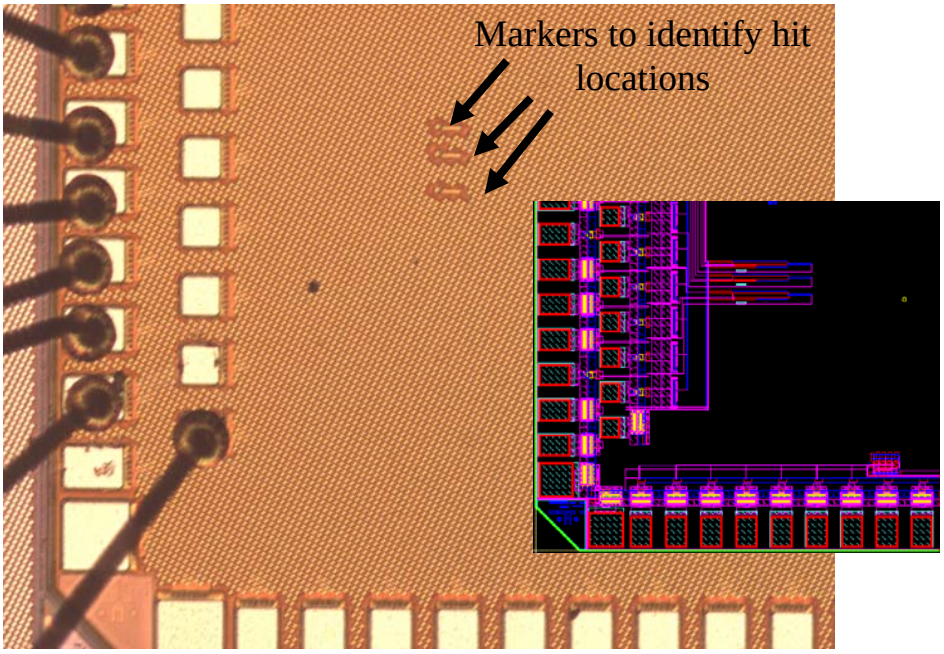


Figure 56. Die photo of the circuit fabricated with the markers for the hit locations identified (for top-side irradiation)

Single- and Two-Photon Laser Absorption Measurements

Carriers were injected into the sensitive nodes using both the top-side, single-photon absorption (SPA) and through-wafer, two-photon absorption (TPA) approaches at the Naval Research Laboratory [144] – [146]. For the SPA technique, the laser-induced single-event transient measurements are performed with nominally 1 ps duration optical pulses centered at 590 nm (2.1 eV) at a laser pulse repetition rate of 1 kHz. The optical pulses are focused onto the device under test (DUT) with a 100x microscope objective, resulting in a Gaussian spot size of 1.2 μm at the surface of the DUT. The DUT is mounted on a motorized xyz stage with 0.1 μm resolution with the laser spot positioned at the most sensitive location for each node investigated. The incident laser pulse energy is monitored with a calibrated large-area photodiode, with the values reported corrected for reflection losses [144]. **Figure 57** displays the single-photon absorption setup.

Through-wafer carrier injection is achieved using sub-bandgap, 1.26 μm, 120 fs optical pulses generated with a tunable optical parametric amplifier pumped by a titanium sapphire regenerative amplifier (Clark-MXR CPA 2110). The strong IR beam is attenuated with a waveplate-polarizer combination to precisely control the pulse energy incident on the device under test (DUT), which is monitored with a calibrated large area InGaAs photodiode. This laser system generates pulses with a near-Gaussian beam profile with a full width at half maximum (fwhm) diameter of 1.6 μm at focus [140]. Because the carrier deposition varies as the pulse irradiance squared, the resulting Gaussian carrier density distribution exhibits a fwhm diameter of 1.1 μm. The DUT is imaged through the wafer using near-infrared (NIR) imaging optics in conjunction with an InGaAs focal plane array (Indigo Alpha NIR). Other aspects of the experimental setup

are similar to those of the SPA experiment. **Figure 58** shows the setup for the two-photon absorption technique. An advantage of the TPA SEE technique is its ability to interrogate SEE phenomena through the wafer using back-side irradiation, eliminating any interference from the metallization layer stacks that exist in these technologies. All experiments were performed at room temperature.

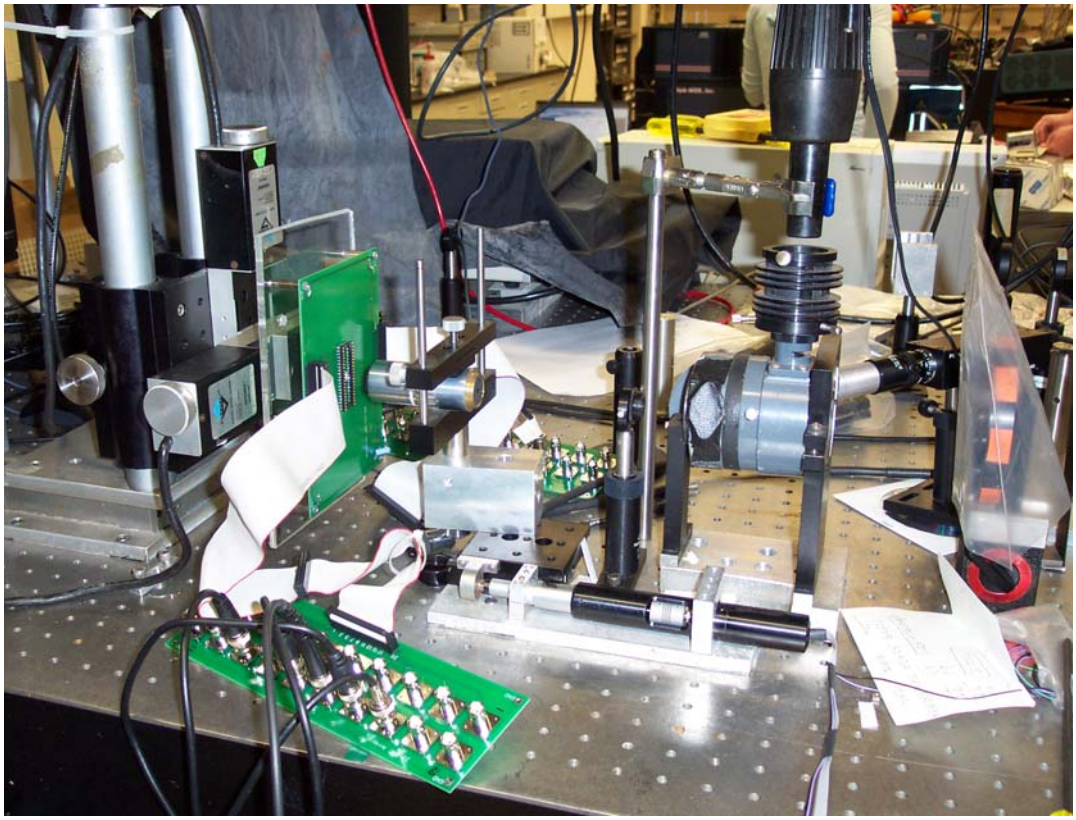


Figure 57. Single-photon laser absorption experimental setup with the laser pulse irradiating the sample from the top-side

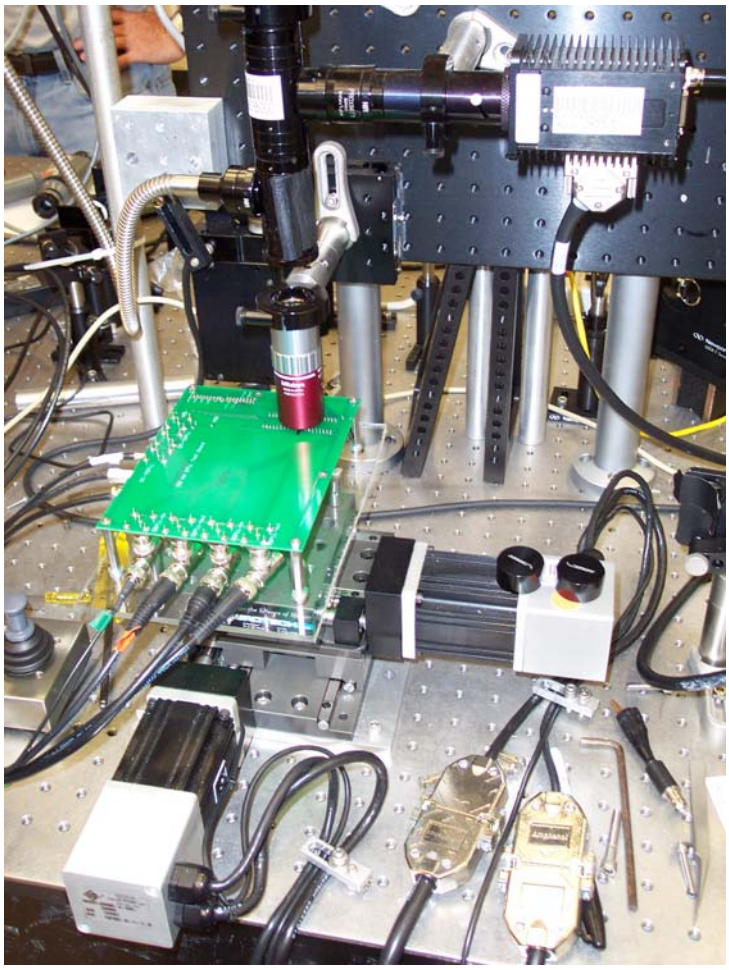


Figure 58. Two-photon laser absorption experimental setup with the laser pulse irradiating the sample from the back-side

Figure 59 shows the experimental results for the SPA experiment and **Figure 60** shows the analogous results for the TPA technique. The drain of the NMOS transistor (second inverter in *Line B*) was used as a laser target, with the upset detected on the output of the SR latch of *Line A*. Each data point in these figures corresponds to an incident laser pulse energy that the test circuit was exposed to. For the data points shown in the shaded grey areas, SE interconnect crosstalk coupling was sufficient to flip the output of the SR latch, even though technology specified design rules were followed. In the design fabricated, the hit or target drain was placed 15 μm away from the rest of the

circuit to avoid any charge sharing effects [131].

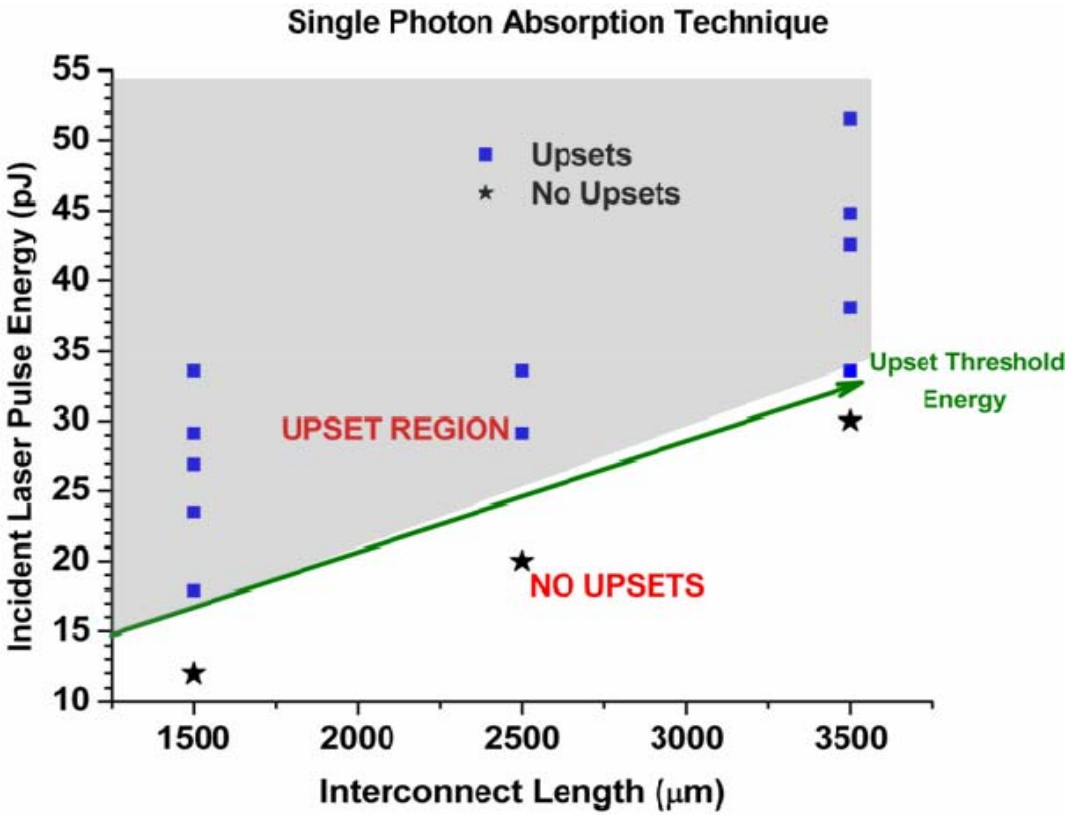


Figure 59. Upsets recorded for increasing laser energies (grey area) at three different interconnect lengths for an n-hit using SPA technique

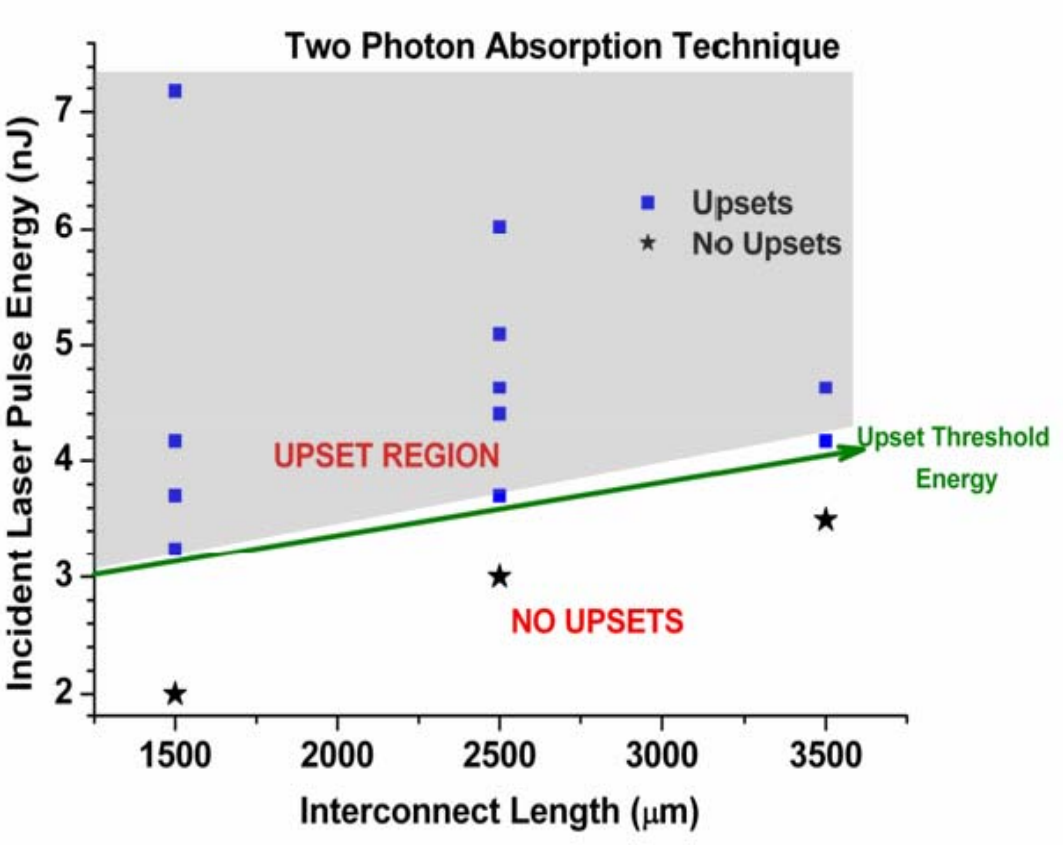


Figure 60. Upsets recorded for increasing laser energies (grey area) at three different interconnect lengths for an n-hit using TPA technique

To record each data point, the sensitive area is identified and located; sufficient laser pulse energy is applied to result in an SEU; in an iterative fashion the xyz position is optimized and the laser pulse energy is lowered to identify the upset threshold at the most sensitive position. The data of **Figures 59** and **60** illustrate this process both for the Single-Photon and the Two-Photon Laser Absorption Techniques. All laser energies the circuit was exposed to are plotted here. No upsets were observed for laser pulse energies lower than those indicated in the grey area, thus the lowest data points in the shaded area for each interconnect length represent the SEU threshold for that circuit. The points plotted in the "NO UPSETS" region (unshaded region) were energies the circuit was

exposed to where no upsets were recorded. In both the single- and two-photon laser absorption case, the data show an increase in upset threshold as the interconnect length increases; as the collected/deposited charge (Q) is directly proportional to C*(dV/dt). As capacitance increases, it takes longer for the node to charge or discharge, resulting in the need for more laser energy for the upset. This corresponds with the analysis in Chapter V where the longest interconnect line length simulated (**Figures 34** and **36**) took the longest time to charge or discharge compared to other cases. The experimental results obtained provide the first ever measurement of the existence of SE induced crosstalk and its ability to increase circuit susceptibility by causing SETs in nearby interconnect lines. However, to identify the circumstances when the impact is detrimental, individual technologies and circuits have to be examined based on analyses performed and trends identified in this dissertation.

CHAPTER VII

MITIGATION TECHNIQUES

Through the past few chapters, a novel radiation induced anomaly "*SE induced crosstalk*" has been identified (Chapter IV), the factors affecting it investigated (Chapter V) and experimental verification provided (Chapter VI). This chapter discusses possible mitigation techniques that can be implemented to contain this effect.

Past research has provided very effective mitigation techniques for normal transient crosstalk including gate and transistor sizing [103], [107], use of guard rings [111], guard bands [112] – [113], use of a low resistivity substrate [114] and placing a thin, grounded highly conductive area in between active device layers [115]. The techniques proposed in this chapter are for SE induced crosstalk in addition to these for the specific technology - IBM 90 nm CMOS9SF.

In combinational logic, one measure of the intensity of a SE is the pulse width of the resulting Single-Event Transient (SET) either at the struck node or any of the subsequent or related nodes where the effect is felt [154]. Many prevalent SE hardening schemes use this pulse width as a threshold for upset eliminating SETs below this pre-determined value [125] – [128], [155]. As a result, it is vital to understand the factors contributing to this SET pulse width (in this case, resulting from SE induced crosstalk) and ways to mitigate it. To reduce the SE vulnerability at a struck node or the resulting SET pulse width, one of the following two things can be done, (i) the amount/rate of charge collected at the node reduced and/or (ii) the rate at which the deposited/collected charge

is removed increased. The approach taken will lead to design tradeoffs in optimizing area, power, speed and required SE tolerance. This chapter addresses a few mitigation strategies that can be used to reduce the impact of the SE induced crosstalk transient pulse.

Device Dimensions

One technique to increase the rate of removal of charge collected at the node is by increasing the drive strength of the restoring device. Also, the rate at which charge changes with time defines current, which yields the familiar equation relating voltage, current and time to capacitance

$$i = C * \frac{dV}{dt}$$

For any given design or circuit, the value of C and *dV/dt* are fixed because of technology and routing line length requirements. The variable "i" can be controlled by varying the device dimensions; hence varying the current drive at the node. Since the duration of the SET generated at a node depends on how quickly the deposited charge from a SE is removed, a larger current drive results in a shorter transient.

To look at the effect of varying the device dimensions for a range of technologies, the circuit in **Figure 61** was simulated using the Cadence® EDA toolset by varying the device sizes (highlighted in blue) from the minimum matched-current-drive inverter dimensions to 7X the initial dimensions using 1500 µm long parallel interconnects and 300 fC of deposited charge. In all four cases, 180 nm through 65 nm technologies, the minimum device sizes are most susceptible to the effect of crosstalk and the disturbance

dies out as the device sizes increase. However, in more advanced technologies the effects are pronounced even at 5 times minimum transistor dimensions. As a result, there is an associated area penalty when increasing the device sizes to values much larger than matched minimum current drive. **Figures 62a** and **62b** show the output of *line A* varying from its original "low" state due to the effect of crosstalk for the 180 nm and 65 nm technologies simulated for various device sizes.

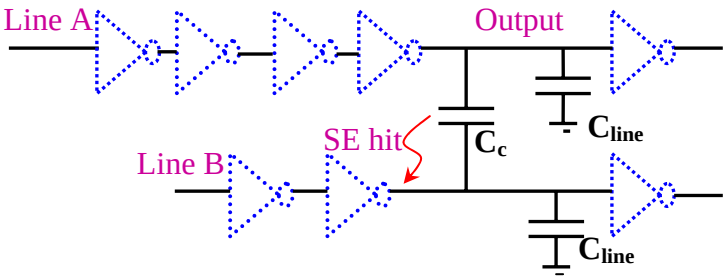


Figure 61. Circuit used to quantify the effect of SE induced crosstalk as a function of varying device sizes (1X – 7X)

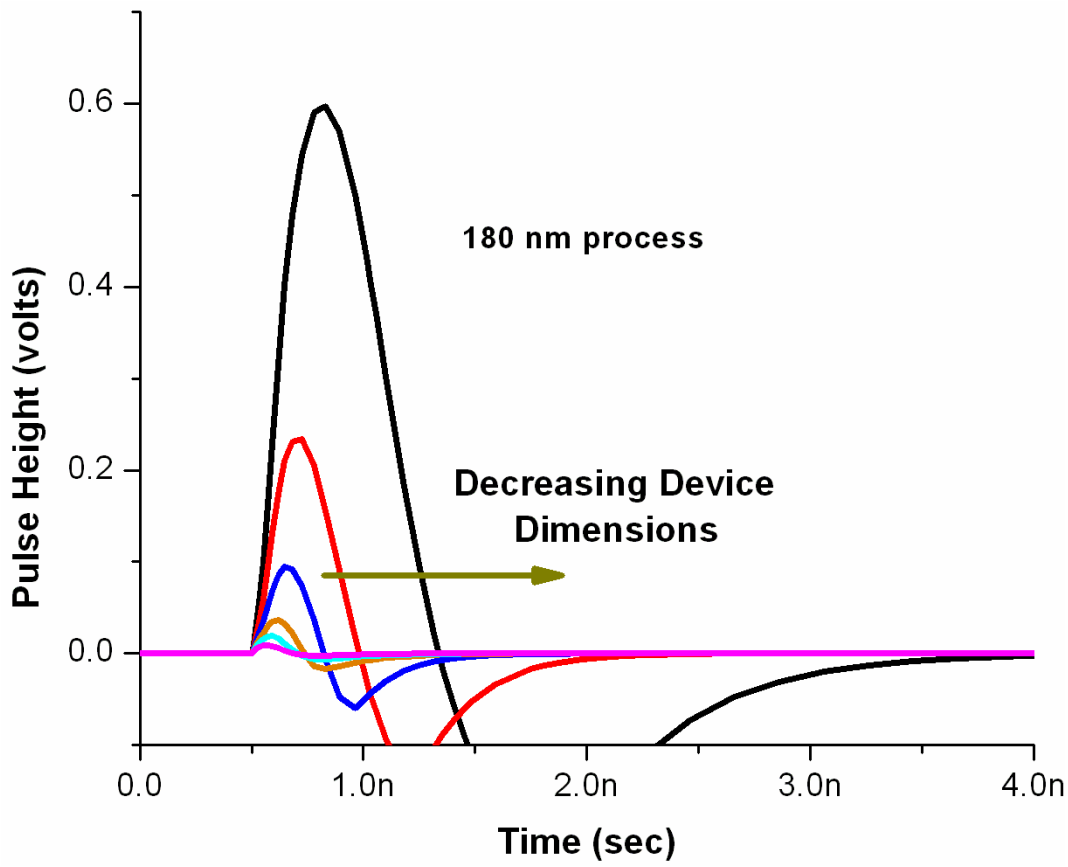


Figure 62a. Crosstalk pulse characteristics with increasing device sizes for the 180 nm process (effect dies out at the 2X device dimension)

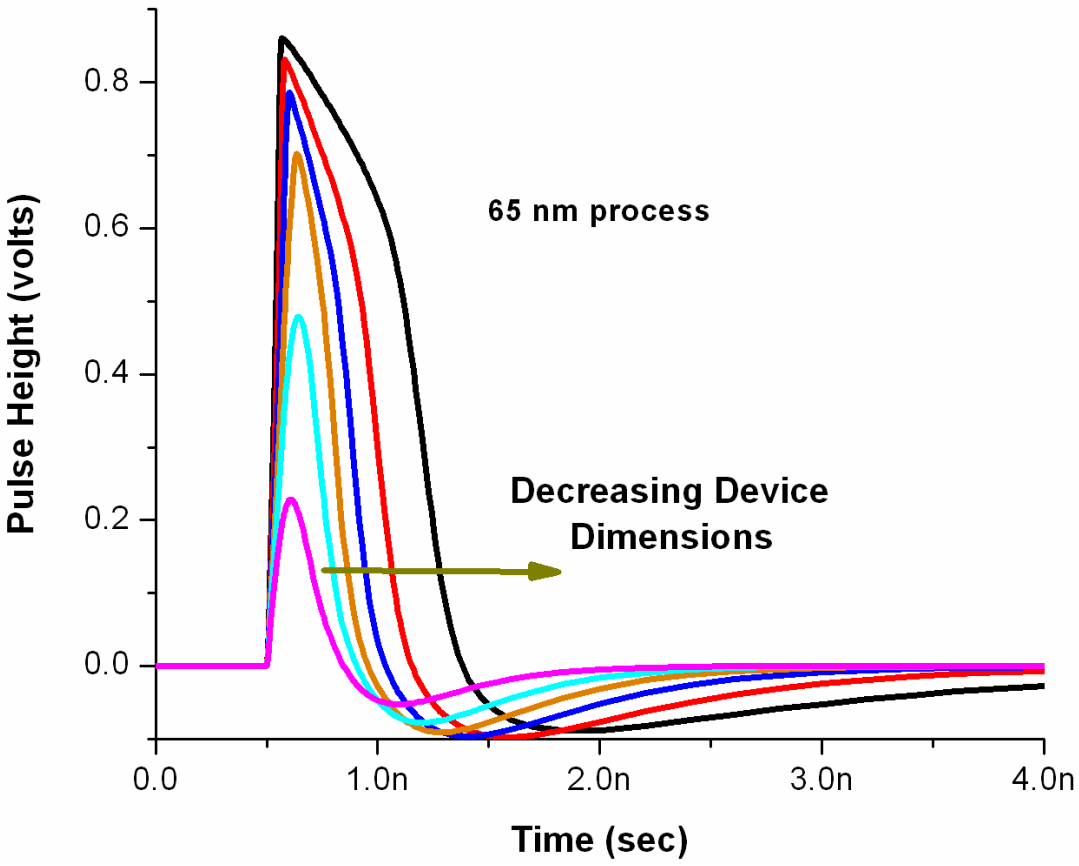


Figure 62b. Crosstalk pulse characteristics with increasing device sizes for the 65 nm process (effect exists even at 5X device dimension)

3D mixed-mode TCAD simulations were performed in the IBM 90 nm CMOS9SF process using the Cadence® EDA toolset and 3D Technology Computer Aided Design (TCAD) structures. The details for these simulations are identical to those discussed in Chapter V. However the device dimensions of the transistors modeled in TCAD were increased to 3 times the minimum matched-current-drive inverter size for the entire chain as shown in **Figure 63**. Simulations were performed with a supply voltage of 1.2 V. All parasitic capacitance values like C_c (the parasitic capacitance between two metal layers) and C_{line} (the parasitic capacitance between metal to substrate) were estimated using the 2D Synopsys® TCAD simulation as described earlier.

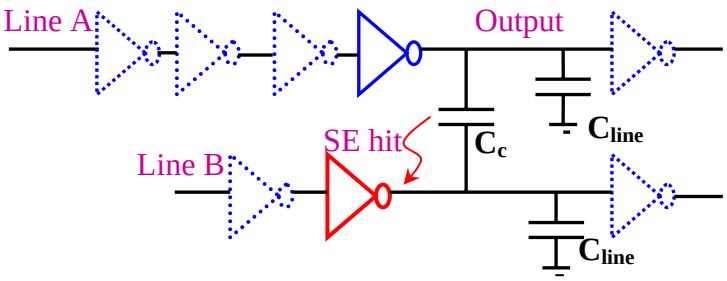


Figure 63. Circuit used to quantify the effect of SE induced crosstalk as a function of device sizes (3X device dimensions). Inverters highlighted in red and blue solid lines modeled in 3D TCAD.

Figures 64a and **64b** show the 3D TCAD devices (2 PMOS/NMOS transistors of the highlighted inverters in **Figure 63**) for the case of a p-hit/n-hit at 3X minimum matched-current-drive inverter sizes. A SE strike on the PMOS transistor is termed a p-hit and a SE strike on the NMOS transistor is termed an n-hit as before. All the simulations were conducted for strikes normal to the surface of the structure. These devices were spaced 3 µm apart to avoid any charge sharing effects and isolate SE induced crosstalk coupling. Current pulses similar to those shown in **Figures 42a** and **42b** were generated with the "heavy-ion" command in DESSIS, at the hit node to simulate the strike.

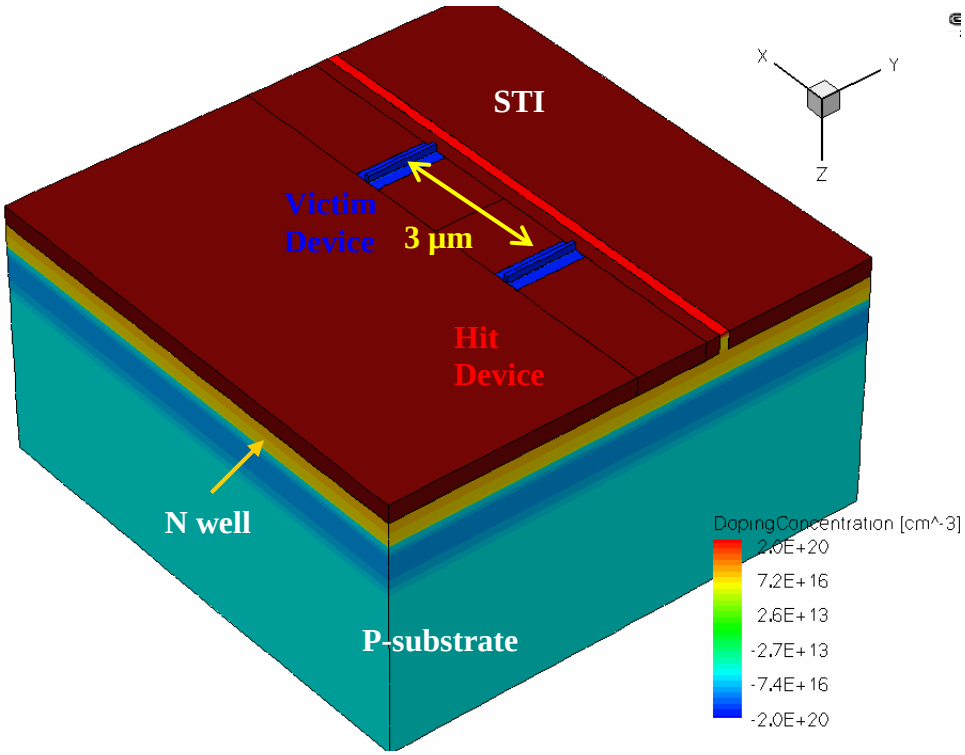


Figure 64a. 3D TCAD PMOS devices showing the *Hit* device on Line B and the *Victim* device on Line A

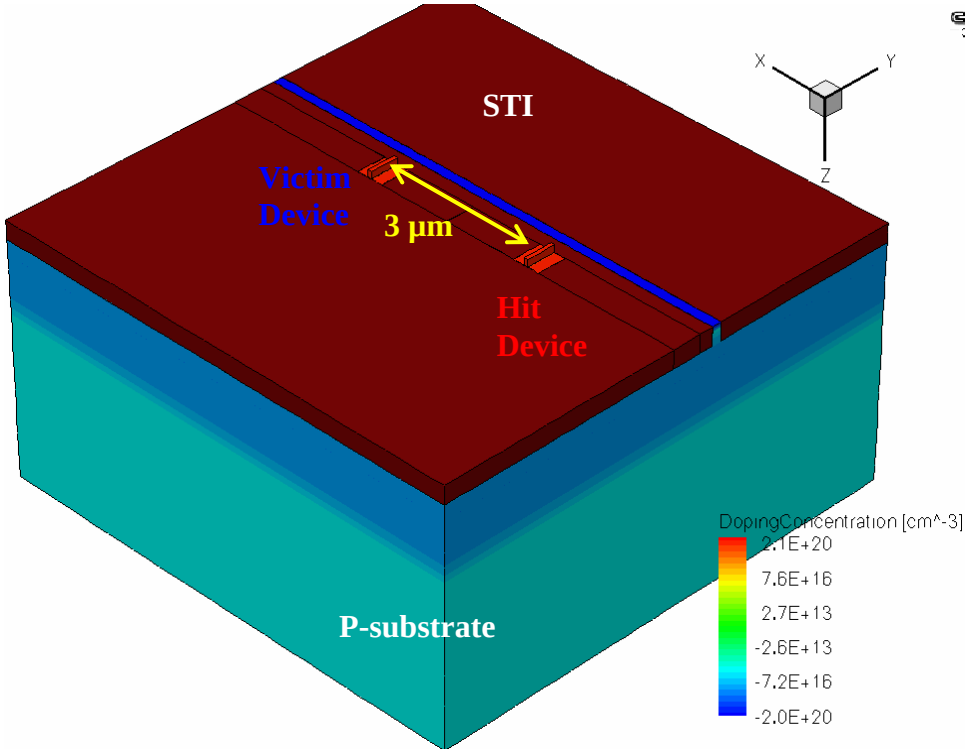


Figure 64b. 3D TCAD NMOS devices showing the *Hit* device on Line B and the *Victim* device on Line A

Figure 65 shows the SE induced crosstalk pulse on the *victim* node for a 1X and 3X matched-current-drive inverter chain for the case of a p-hit. **Figure 66** presents the analogous results for the case of an n-hit. These results are for an LET of 40 MeV-cm^2/mg and for a 1000 μm long interconnect line. From the results it is visible that when the device sizes are increased to 3X the minimum dimensions; the pulse on the *victim* node falls below the threshold voltages of transistors for this technology. For the p-hit case there is a 3X reduction in peak magnitude and for the case of the n-hit there is greater than 10X reduction in peak magnitude. As a result, this will most likely not propagate to the next stage and will be eliminated. The penalty for this technique is definitely the increased area; limiting it to critical nodes helps keep the increase in area minimal.

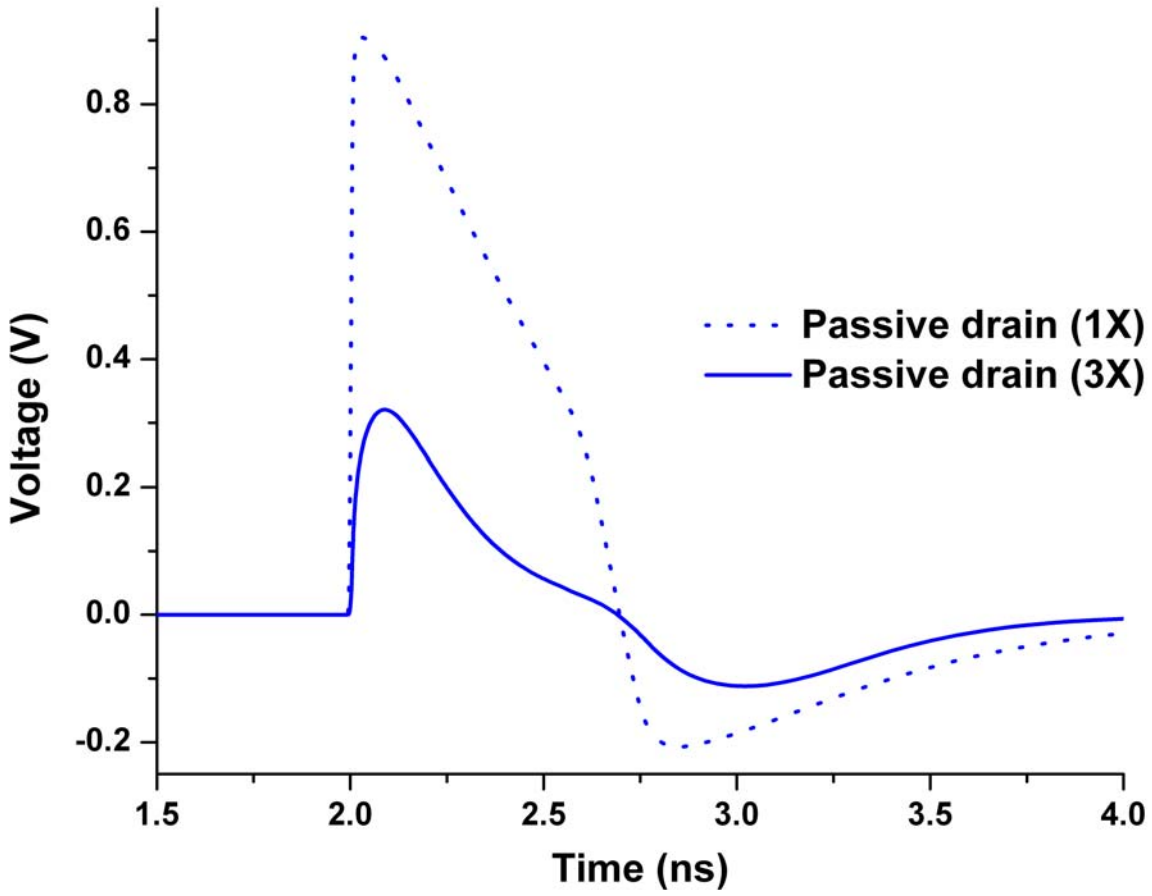


Figure 65. Voltage pulse on the passive drain (*victim* node) for a 1X and 3X matched-current-drive inverter chain for the case of a p-hit at an LET of 40 MeV-cm^2/mg for a 1000 μm long interconnect line

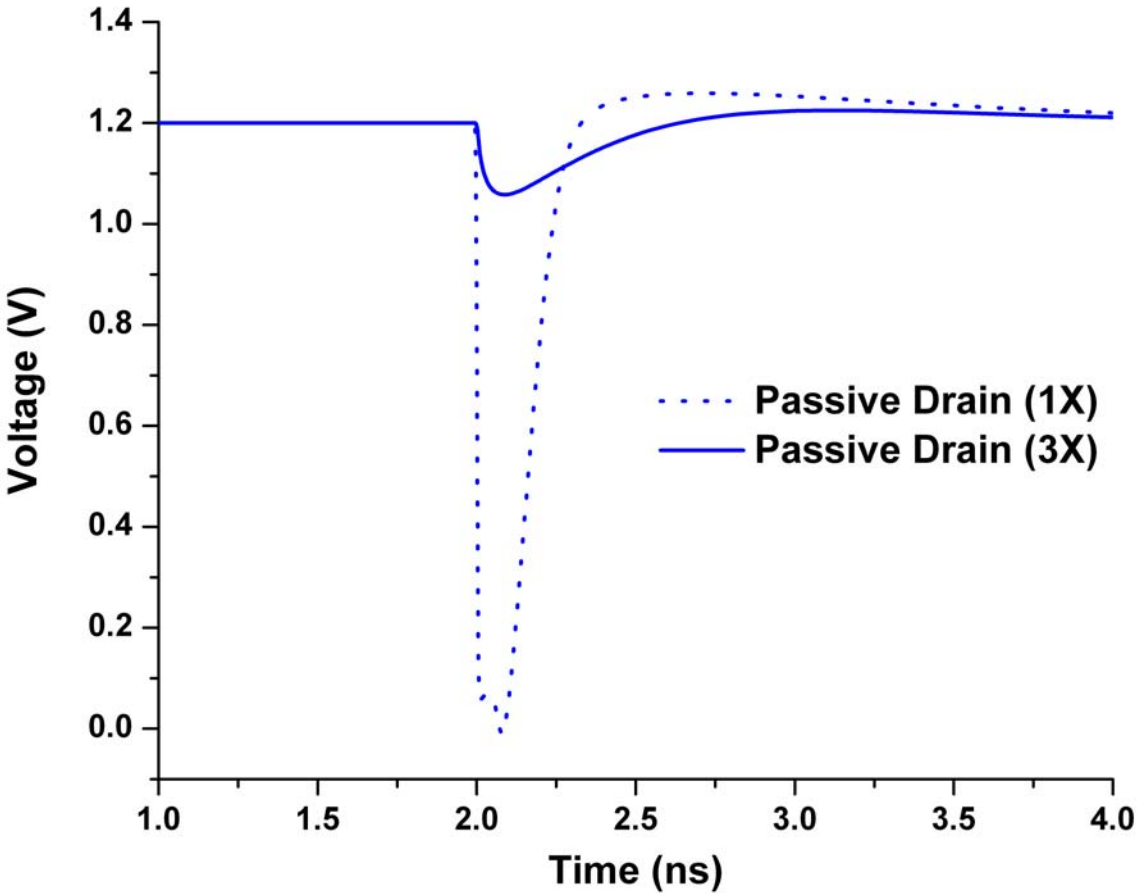


Figure 66. Voltage pulse on the passive drain (*victim* node) for a 1X and 3X matched-current-drive inverter chain for the case of a n-hit at an LET of 40 MeV-cm^2/mg for a 1000 µm long interconnect line

Coupling Capacitance

The main parameters that contribute to the capacitive coupling between two metal interconnects are the length, width, thickness and spacing between them. The minimum for each of these is process defined. Parameters the designer can vary include the length, width and spacing. Using the minimum metal width is preferable to avoid added resistance, and routing between devices will decide the interconnect line length; resulting in the spacing between metal interconnects being available as the variable parameter. The further apart the metal interconnects are placed from each other, the lesser the coupling

is. However, this comes with additional area requirements as designers usually tend to space interconnects following manufacturer provided design rules.

For this work, the coupling capacitance was calculated using a 2D TCAD simulation, details of which are covered in Chapter IV and in Appendix A. The same tool was used for calculating the capacitances for the IBM 90 nm CMOS9SF process when the metal interconnect spacing was increased by 50%. **Table 6** lists the decrease in coupling capacitance (approximately 26%) when the spacing between the interconnects is increased by 50% for a 1 µm long interconnect line.

Table 6. Coupling capacitances between two metal interconnects for the IBM 90 nm CMOS9SF process

IBM 90 nm CMOS9SF process	Coupling Capacitance (C_C) [fF/µm]
Minimum Metal-Metal Spacing	0.12
Minimum + 50% spacing	0.09514

Figures 67 and **68** present the results for a p- and an n-hit in the IBM 90 nm CMOS9SF process. The figures show the voltage pulses on the *victim* nodes for both minimum metal spacing and increased spacing (50%) for an LET of 40 MeV-cm^2/mg for 150 µm and 1000 long µm interconnect lines. The simulations were performed at a supply voltage of 1.2 V. From the results it is visible that the increased metal spacing does not do much to mitigate this effect. There is minimal difference especially for the case of an n-hit as seen in **Figure 68**. Larger metal spacing may be required to reduce the capacitance further in order to considerably mitigate this effect. However, with the

associated penalty of increased area this may not be an effective mitigation technique to use.

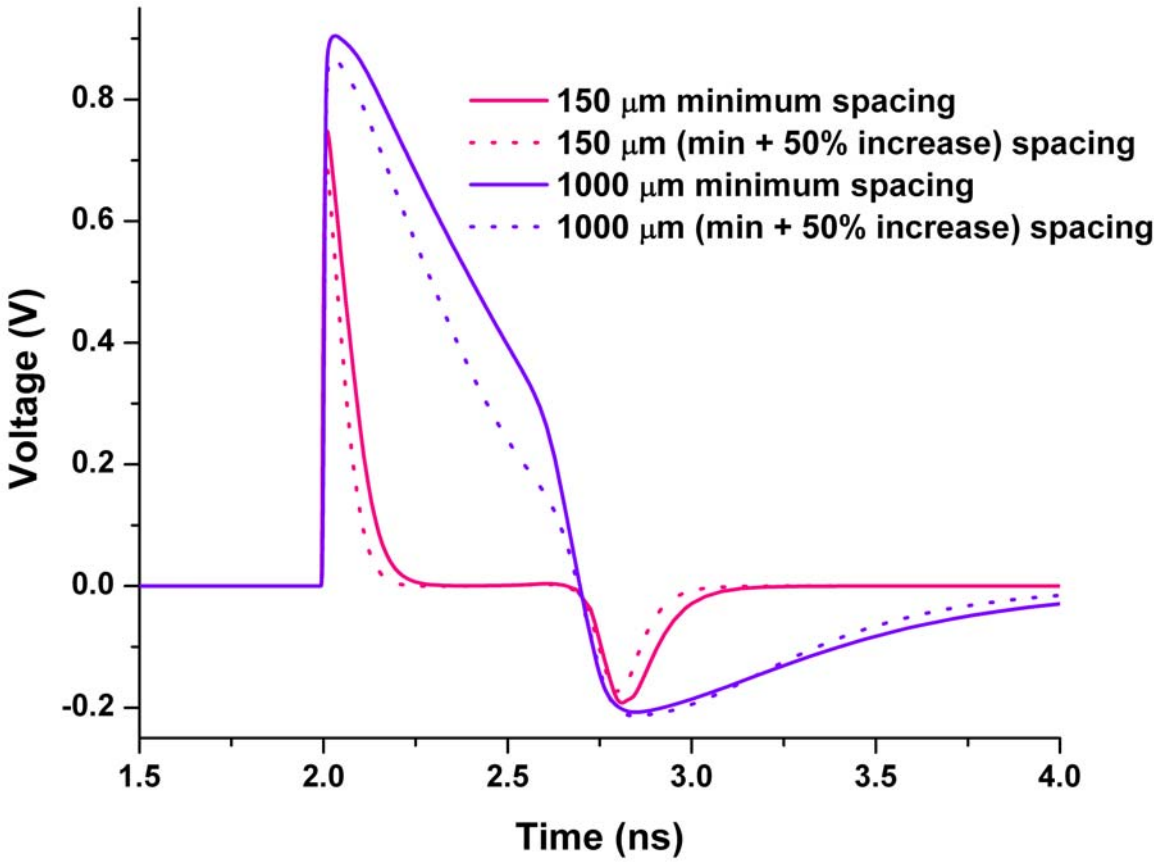


Figure 67. Voltage pulse on the passive drain (*victim* node) for minimum metal to metal spacing and 50% increased spacing for the case of a p-hit at an LET of 40 MeV-cm^2/mg for 150 μm and 1000 μm long interconnect lines

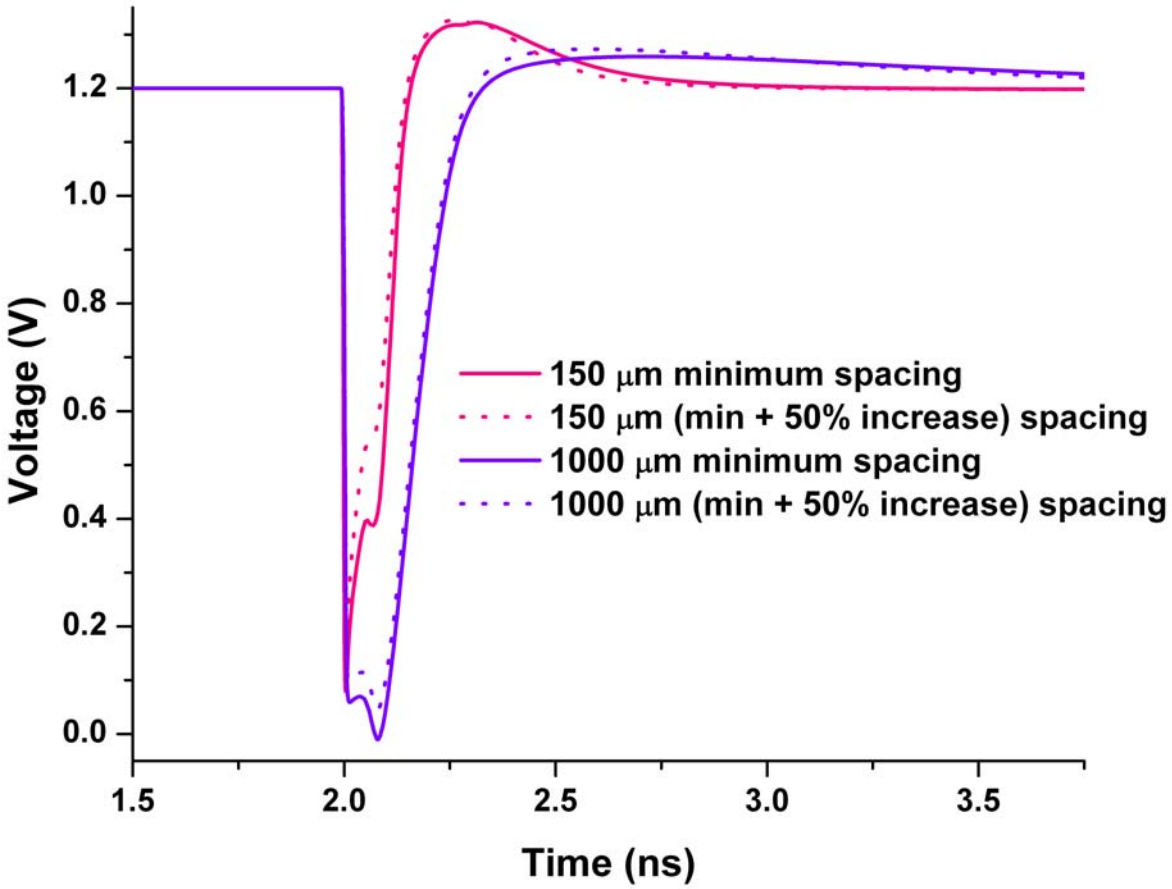


Figure 68. Voltage pulse on the passive drain (*victim* node) for minimum metal to metal spacing and 50% increased spacing for the case of an n-hit at an LET of 40 MeV-cm^2/mg for 150 μm and 1000 μm long interconnect lines

Design Rules

Manufacturer specified design rules are provided for each technology based on the feasibility of fabricating the circuit the designer designs without any fabrication or process related errors. While they may be sufficient to account for crosstalk from normal signal transitions, these design rules might not account for SE induced crosstalk. As a result even a circuit fabricated with manufacturer specified design rules might be susceptible to these effects.

Since the amount of charge that a designed circuit is exposed to cannot be pre-

determined, it is important to harden it by identifying other parameters that can be controlled. Performing simulations to identify the minimum line length at which crosstalk coupling occurs for SE induced events for the technology of interest, identifying the associated device dimensions without losing out on area help minimize these effects. This may result in a new set of design rules for the technology of interest with respect to interconnect length and spacing. However this needs to be applied only to sensitive nodes or parts of the circuit with extensive routing.

3D mixed-mode TCAD simulations were performed in the IBM 90 nm CMOS9SF process in an attempt to provide design margins that can help designers estimate how much SE induced crosstalk coupling to expect for the various cases considered. The SE induced crosstalk voltage pulse width at Full Width Half Rail (FWHR) was used as the measure for all the cases considered as it is a commonly used standard, and this magnitude surpasses the threshold voltages of transistors for this technology. The following parameters were considered with strikes simulated on both the PMOS and NMOS transistors;

- range of interconnect lengths -150 µm, 500 µm and 1000 µm
- range of LETs- 10, 20, 30 and 40 MeV-cm^2/mg
- couple of device dimensions- 1X and 3X minimum matched-current-drive transistors and
- minimum metal to metal spacing and a 50% increase in metal to metal spacing to vary the coupling capacitance

Because of the simulation time and complexity associated with these kinds of 3D mixed-mode simulations; in some cases the best and worst cases were simulated to give

an estimate instead of considering the whole spectrum. Results are presented in a tabular format with the pulse width measured at FWHR in each case listed. Depending on the designer's requirements these guidelines can be utilized to eliminate or mitigate crosstalk in the circuit of interest.

Tables 7 and **8** cover the range of LETs and line lengths for minimum size matched-current-drive devices. **Table 9** shows the analogous results for a 1V supply for strikes on the NMOS transistor. From the values observed it can be seen that p-hits are longer than n-hits and lower supply voltages provide a worst-case condition.

Table 7. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the PMOS transistor at a supply voltage of 1.2 V for 1X device dimensions

Line Length (μm)/ LETs (MeV-cm^2/mg)	10	20	30	40	1X
150	44 ps	41 ps	41 ps	37 ps	
500	123 ps	160 ps	163 ps	158 ps	
1000	140 ps	266 ps	306 ps	314 ps	

Table 8. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the NMOS transistor at a supply voltage of 1.2 V for 1X device dimensions

Line Length (μm)/ LETs (MeV-cm^2/mg)	10	20	30	40	1X
150	61 ps	79 ps	92 ps	102 ps	
500	82 ps	110 ps	126 ps	141 ps	
1000	90 ps	137 ps	158 ps	172 ps	

Table 9. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the NMOS transistor at a supply voltage of 1 V for 1X device dimensions

Line Length (μm)/ LETs (MeV-cm^2/mg)	10	20	30	40	1X
500	131 ps	164 ps	192 ps	213 ps	
1000	169 ps	214 ps	246 ps	273 ps	

Tables 10 and **11** provide the best and worst case interconnect length and LET from the matrix considered for 3X minimum size matched-current-drive devices compared with the 1X minimum size matched-current-drive devices . From the values observed it can be seen that the pulse does not exist at FWHR (for 3X devices) and hence increasing the device dimensions helps mitigate this SE induced voltage pulse completely for this technology for the cases considered.

Table 10. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the PMOS transistor at a supply voltage of 1.2 V for 1X and 3X device dimensions

	1X		3X	
Line Length (μm)/ LETs (MeV-cm^2/mg)	10	40	10	40
150	44 ps	37 ps	0	0
1000	140 ps	314 ps	0	0

Table 11. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the NMOS transistor at a supply voltage of 1.2 V for 1X and 3X device dimensions

	1X		3X	
Line Length (μm)/ LETs (MeV-cm^2/mg)	10	40	10	40
150	61 ps	102 ps	0	0
1000	90 ps	172 ps	0	0

Finally, **Tables 12** and **13** provide the best and worst case interconnect length and LET from the matrix considered for 1X minimum size matched-current-drive devices with a 50% increased metal to metal spacing compared to the minimum metal to metal spacing. This reduces the coupling capacitance between the *hit* and the *victim* devices. However, from the pulse widths obtained and comparing with the values for minimum metal to metal spacing it is visible that even a 50% increase in the minimum spacing does little to mitigate this effect and the pulse is still considerably wide at FWHR. Hence, either the metal lines may have to spaced further apart or an alternate mitigation strategy used.

Table 12. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the PMOS transistor at a supply voltage of 1.2 V for 1X device dimensions with a 50% increase in minimum metal to metal spacing compared to the minimum metal to metal spacing

	Minimum Metal to Metal Spacing		Minimum + 50% increase in Metal to Metal spacing	
Line Length (μm)/ LETs (MeV-cm^2/mg)	10	40	10	40
150	44 ps	37 ps	26 ps	20 ps
1000	140 ps	314 ps	134 ps	223 ps

Table 13. Voltage pulse at full width half rail (FWHR) on the *victim* node for a strike on the NMOS transistor at a supply voltage of 1.2 V for 1X device dimensions with a 50% increase in minimum metal to metal spacing compared to the minimum metal to metal spacing

	Minimum Metal to Metal Spacing		Minimum + 50% increase in Metal to Metal spacing	
Line Length (μm)/ LETs (MeV-cm^2/mg)	10	40	10	40
150	61 ps	102 ps	56 ps	84 ps
1000	90 ps	172 ps	95 ps	166 ps

This chapter provides certain mitigation techniques (increased device dimensions, reduced capacitive coupling and design rules) that can be used to contain this effect for the various cases simulated. These are specific to the IBM 90 nm CMOS9SF process but can be extended to other technologies using the analyses performed in this dissertation. In addition to the techniques provided in this chapter, conventional mitigation schemes as identified earlier (e.g. use of ground lines between signal lines, guard bands etc.) used for normal transient crosstalk (discussed in Chapter III) can also be applied whenever appropriate.

CHAPTER VIII

SUMMARY AND CONCLUSIONS

A new phenomenon – "*SE induced crosstalk"*, capable of *creating* unexpected SETs in the radiation domain has been identified and investigated in this dissertation. In the presence of crosstalk coupling due to SEs, the vulnerable area of a circuit increases and the reliability is affected, as shown through comprehensive Cadence Spectre® and 3D TCAD mixed-mode simulations in Chapters IV and V. The threefold objective of this research was achieved: (i) identification of the factors that exacerbate SE induced coupling using simulations and modeling (Chapter V) (ii) design, fabrication and test of a sample circuit to provide the first ever experimental measurement of SE induced interconnect crosstalk coupling (Chapter VI) and finally (iii) propose design margins to mitigate this effect in the technologies studied (Chapter VII).

The milestones achieved in this dissertation include primarily the identification of a new anomaly in the radiation domain: *SE induced crosstalk* (Chapter IV). This was differentiated from normal transient crosstalk and the impact it has for the radiation domain highlighted. The significance of SE induced crosstalk coupling compared to a normal voltage transient was quantified through detailed 3D mixed-mode simulations in Chapter IV and the detrimental effect it can have on traditional radiation hardening by design (RHBD) techniques like Triple modular redundancy (TMR) or Temporal sampling outlined. Transients occurring on voter inputs in TMR or Temporal sampling can render these schemes ineffective as described in Chapter IV.

In nanoscale CMOS technologies, the parallel plate approximation no longer provides an accurate estimate of the coupling capacitance and hence a 2D TCAD model was developed for calculating the coupling capacitance for deep sub-micron technologies investigated: IBM 180 nm, IBM 130 nm, IBM 90 nm and a generic 90 and 65 nm CMOS process (Chapter IV). This methodology was used to calculate the parasitic capacitances used for simulations. Next, a detailed investigation of the various factors affecting SE induced crosstalk including collected charge, coupling capacitance and scaling technologies (Chapter V) was performed. This was achieved using comprehensive simulations with Cadence® Spectre (circuit simulations) and Synopsis® Technology Computer Aided Design (TCAD) (device simulations) in Chapters IV and V. Results obtained showed that the effect worsened with increased amount of collected charge and scaling technologies.

In the final phase of this study, a measurement circuit to observe SE induced crosstalk effects was designed in the IBM 90 nm CMOS9SF process and fabricated through the MOSIS trusted foundry, to efficiently complement the simulations performed. Single- and Two- Photon laser experiments were performed at the Naval Research Laboratories, Washington and provide verification and measurement of this phenomenon (Chapter VI). The experimental results obtained provide the first ever measurement of the existence of SE induced crosstalk and its ability to increase circuit susceptibility by causing SETs in nearby interconnect lines.

To conclude, design methodologies and rules were also provided for circuit and layout engineers to follow, which will contain/mitigate this effect (Chapter VII). By increasing the device dimensions of the transistors connected to sensitive nodes,

decreasing the coupling capacitance between the *hit* and *victim* nodes, careful consideration of design rules - the transient pulse generated due to SE induced crosstalk can be eliminated effectively. However, designers face the associated area penalty and a design tradeoff may be essential for hardening sensitive nodes or extensively routed parts of the design.

This work has presented to the radiation effects community a new phenomenon that is gaining significance with scaling technologies, and with the use of commercial foundries to fabricate parts for space. As the semiconductor industry keeps up with the scaling trend with increasing chip density and interconnect routing complexity, SE induced crosstalk effects are inevitable. Judicious design and layout planning using analyses performed in this dissertation can help mitigate or contain this effect.

APPENDIX A

2D TCAD SIMULATION FOR CAPACITANCE ESTIMATION

This appendix contains all the files used to calculate the coupling capacitances between the two metal lines for the various technologies simulated.

Structure Definition

```
(define t 0.15)   ; thickness of metal lines
(define d 0.12)   ; spacing between metal lines
(define w 0.12)   ; width of metal lines - assume both are same

(define x1 (* -0.5 d))
(define x2 (- x1 w))
(define x3 (* 0.5 d))
(define x4 (+ x3 w))
(define y1 (* 0.5 t))
(define y2 (* -0.5 t))

(define hw (* (+ w d) 4)) ; half width of structure
(define hh (* t 200)) ; half-height

; new replaces old
(isegeo:set-default-boolean "ABA")

; create a silicon block for the simulator
;(isegeo:create-rectangle (position (* -1.1 hw) (* -1.1 hh) 0) (position (* 1.1 hw) (* 1.1
hh) 0) "Silicon" "R.Silicon")
;(isedr:define-constant-profile "P.SubstrateDoping" "BoronActiveConcentration" 1e15)
;(isedr:define-constant-profile-region  "PlaceCD.Psub" "P.SubstrateDoping" "R.Silicon" )

; create the oxide block
(isegeo:create-rectangle (position (* -1.0 hw) (* -1.0 hh) 0) (position hw hh 0) "Oxide"
"R.Oxide")

; create the left conductor
(isegeo:create-rectangle (position x1 y1 0) (position x2 y2 0) "PolySilicon" "R.Lmetal")
(isedr:define-constant-profile "P.MetalDoping" "BoronActiveConcentration" 1e22)
```

```
(isedr:define-constant-profile-region  "PlaceCD.Psub" "P.MetalDoping" "R.Lmetal" )

; create the right conductor
(isegeo:create-rectangle (position x3 y1 0) (position x4 y2 0) "PolySilicon" "R.Rmetal")
(isedr:define-constant-profile-region  "PlaceCD.Psub2" "P.MetalDoping" "R.Rmetal" )

; contacts
(isegeo:define-contact-set "Left"    4.0(color:rgb 1 0 0) "##")
(isegeo:insert-vertex (position x2 0 0))
(isegeo:define-2d-contact (find-edge-id (position x2 0 0))  "Left")

(isegeo:define-contact-set "Right"    4.0(color:rgb 1 0 0) "##")
(isegeo:insert-vertex (position x4 0 0))
(isegeo:define-2d-contact (find-edge-id (position x4 0 0))  "Right")

;(isegeo:define-contact-set "Substrate"    4.0(color:rgb 1 0 0) "##")
;(isegeo:insert-vertex (position 0 (* -1.1 hw) 0))
;(isegeo:define-2d-contact (find-edge-id (position 0 (* -1.1 hh) 0))  "Substrate")

; whole mesh
;(define r1 (/ hw 20))
;(define r2 (/ hh 20))
;(define r3 (/ d 10))
;(define r4 (/ t 20))
(define r1 (/ hw 50))
(define r2 (/ hh 50))
(define r3 (/ d 50))
(define r4 (/ t 4))

(isedr:define-refinement-size "Ref.NBL" r1 r2 r1 r2 )
(isedr:define-refinement-region "RefPlace.Nminus" "Ref.NBL" "R.Oxide" )

; refine between source/contact regions // surface
(isedr:define-refinement-size "Ref.6" (/ r3 2) (/ r4 2) (/ r3 2 ) (/ r4 2) )
(isedr:define-refinement-function "Ref.6" "DopingConcentration" "MaxTransDiff" 0.5)
(isedr:define-refinement-window "Ref.6" "Rectangle" (position (* x2 2) (* 2.0 y1) 0)
(position (* x4 2) (* 2.0 y2) 0))
(isedr:define-refinement-placement "Ref.6" "Ref.6" "Ref.6" )

; refine between source/contact regions // surface
(isedr:define-refinement-size "Ref.7" (* r3 5) (* r4 8) (* r3 5 ) (* r4 8) )
(isedr:define-refinement-function "Ref.7" "DopingConcentration" "MaxTransDiff" 0.5)
(isedr:define-refinement-window "Ref.7" "Rectangle" (position (* x2 2.5) (* 50.0 y1) 0)
(position (* x4 2.5) (* 50.0 y2) 0))
(isedr:define-refinement-placement "Ref.7" "Ref.7" "Ref.7" )
(ise:save-model "structure")
```

Mixed-Mode Dessis file for running simulations

```
Device NMOS {
File {
#         PMIPath = "."
        grid    = "structure_msh.grd"
        doping  = "structure_msh.dat"
           Plot    = "plot"
           Current = "current"
#       Output = "output"
}

  Electrode {
    { name="Left"    Voltage=0.0}
    { name="Right"    Voltage=0.0}
#    { name="Substrate" Voltage=0.0}
  }

  Physics {
    Fermi
    Recombination(SRH)
    Mobility( DopingDep HighFieldSaturation Enormal )
    EffectiveIntrinsicDensity( oldSlotboom )
  }
}

File {
           PMIPath = "."
           Plot    = "plot"
           Current = "current"
       Output = "output"
           ACExtract = "acplot"
}

Plot {
    eDensity hDensity Current
    eCurrent hCurrent
    ElectricField eEnormal hEnormal
    eQuasiFermi hQuasiFermi
    Potential Doping SpaceCharge
    DonorConcentration AcceptorConcentration
    HeavyIonChargeDensity PMIRecombination
}

Math {
    wallclock
```

```
  Extrapolate
  Transient=BE
  Derivatives
  RelErrControl
  Digits=6
  Notdamped=50
  Iterations=12
  -NewDiscretization
  NoCheckTransientError
#  method=slip
}

System{
  Vsource_pset Vin (Vin 0) { dc = 0.0 }
  Vsource_pset V2  (V2 0)  { dc = 0.0 }
#  NMOS nmos1 ( "Left"=V2  "Right"=Vin "Substrate"=0 )
  NMOS nmos1 ( "Left"=V2  "Right"=Vin  )
  Plot "system.out.plt" (time() v(Vin) i(nmos1,Vin)  i(nmos1,V2) )
}

Solve {
  #-build up initial solution
  Coupled(iterations=100)  { Poisson }
  Coupled(iterations=100)  { Poisson Electron}
  Coupled(iterations=100)  { Poisson Hole Electron}

  Plot (FilePrefix = "Biased")
  NewCurrentFile="AC"
    ACCoupled(StartFrequency=1e2 EndFrequency=1e12 NumberOfPoints=10 Decade
Node(Vin V2)){Poisson Electron Hole}
}
```

APPENDIX B

SPICE NETLISTS

This appendix displays the netlist for the various simulations (a sample is provided here) performed using CADENCE and the SPECTRE environment in the IBM 180 nm, 130 nm and generic 90 nm and 65 nm technologies for identifying the various parameters affecting crosstalk.

IBM 130 nm – Various Charge Deposited

```
// Generated for: spectre
// Generated on: Jul  6 09:36:48 2006
// Design library name: NSREC06_crosstalk
// Design cell name: JULY06_Inv1x_Variouschargedeposited_130nm_anu
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters vdd=1.2
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmrf8sf/V1.3.0.2LM/Spectre/models/allModels.scs
"

// Library name: NSREC06_crosstalk
// Cell name: JULY06_Inv1x_Variouschargedeposited_130nm_anu
// View name: schematic
V1 (net0963 0) vsource type=pulse val0=0.0 val1=vdd period=10n delay=500p \
        rise=200p fall=200p width=2n

//////////Diodes to limit the current pulse going one voltage drop above and below the rail//////////
D79 (net1003 vdd!) diodenwx dtemp=0.0
D78 (net1003 0) diodenwx dtemp=0.0
D77 (net1047 0) diodenwx dtemp=0.0
D76 (net1047 vdd!) diodenwx dtemp=0.0
D75 (net1067 vdd!) diodenwx dtemp=0.0
D74 (net1067 0) diodenwx dtemp=0.0
D73 (net1111 0) diodenwx dtemp=0.0
```

D72 (net1111 vdd!) diodenwx dtemp=0.0
D71 (net1131 vdd!) diodenwx dtemp=0.0
D70 (net1131 0) diodenwx dtemp=0.0
D69 (net1175 0) diodenwx dtemp=0.0
D68 (net1175 vdd!) diodenwx dtemp=0.0
D67 (net1195 vdd!) diodenwx dtemp=0.0
D66 (net1195 0) diodenwx dtemp=0.0
D65 (net1239 0) diodenwx dtemp=0.0
D64 (net1239 vdd!) diodenwx dtemp=0.0
D63 (net1259 vdd!) diodenwx dtemp=0.0
D62 (net1259 0) diodenwx dtemp=0.0
D61 (net1303 0) diodenwx dtemp=0.0
D60 (net1303 vdd!) diodenwx dtemp=0.0
D59 (net1323 vdd!) diodenwx dtemp=0.0
D58 (net1323 0) diodenwx dtemp=0.0
D57 (net1367 0) diodenwx dtemp=0.0
D56 (net1367 vdd!) diodenwx dtemp=0.0
D55 (net1387 vdd!) diodenwx dtemp=0.0
D54 (net1387 0) diodenwx dtemp=0.0
D53 (net1431 0) diodenwx dtemp=0.0
D52 (net1431 vdd!) diodenwx dtemp=0.0
D51 (net1451 vdd!) diodenwx dtemp=0.0
D50 (net1451 0) diodenwx dtemp=0.0
D49 (net1495 0) diodenwx dtemp=0.0
D48 (net1495 vdd!) diodenwx dtemp=0.0
D47 (net1515 vdd!) diodenwx dtemp=0.0
D46 (net1515 0) diodenwx dtemp=0.0
D44 (net1559 vdd!) diodenwx dtemp=0.0
D45 (net1559 0) diodenwx dtemp=0.0
D42 (net1579 0) diodenwx dtemp=0.0
D40 (Bhit1x vdd!) diodenwx dtemp=0.0
D43 (net1579 vdd!) diodenwx dtemp=0.0
D41 (Bhit1x 0) diodenwx dtemp=0.0

////////**Double exponential current pulses to define the SE strike**//////////
I58 (vdd! net1559) isource type=exp val0=0.0 val1=750u td1=500p tau1=50p \
td2=505p tau2=250p
I49 (vdd! Bhit1x) isource type=exp val0=0.0 val1=250u td1=500p tau1=50p \
td2=505p tau2=250p
I68 (vdd! net1003) isource type=exp val0=0.0 val1=2.75m td1=500p tau1=50p \
td2=505p tau2=250p
I67 (vdd! net1047) isource type=exp val0=0.0 val1=3m td1=500p tau1=50p \
td2=505p tau2=250p
I66 (vdd! net1067) isource type=exp val0=0.0 val1=3.25m td1=500p tau1=50p \
td2=505p tau2=250p
I65 (vdd! net1111) isource type=exp val0=0.0 val1=3.5m td1=500p tau1=50p \

td2=505p tau2=250p
I64 (vdd! net1131) isource type=exp val0=0.0 val1=3.75m td1=500p tau1=50p \
td2=505p tau2=250p
I63 (vdd! net1175) isource type=exp val0=0.0 val1=4m td1=500p tau1=50p \
td2=505p tau2=250p
I62 (vdd! net1195) isource type=exp val0=0.0 val1=4.25m td1=500p tau1=50p \
td2=505p tau2=250p
I61 (vdd! net1239) isource type=exp val0=0.0 val1=4.5m td1=500p tau1=50p \
td2=505p tau2=250p
I60 (vdd! net1259) isource type=exp val0=0.0 val1=4.75m td1=500p tau1=50p \
td2=505p tau2=250p
I59 (vdd! net1303) isource type=exp val0=0.0 val1=5m td1=500p tau1=50p \
td2=505p tau2=250p
I50 (vdd! net1579) isource type=exp val0=0.0 val1=500u td1=500p tau1=50p \
td2=505p tau2=250p
I51 (vdd! net1515) isource type=exp val0=0.0 val1=1m td1=500p tau1=50p \
td2=505p tau2=250p
I52 (vdd! net1495) isource type=exp val0=0.0 val1=1.25m td1=500p tau1=50p \
td2=505p tau2=250p
I53 (vdd! net1451) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
td2=505p tau2=250p
I54 (vdd! net1431) isource type=exp val0=0.0 val1=1.75m td1=500p tau1=50p \
td2=505p tau2=250p
I55 (vdd! net1387) isource type=exp val0=0.0 val1=2m td1=500p tau1=50p \
td2=505p tau2=250p
I56 (vdd! net1367) isource type=exp val0=0.0 val1=2.25m td1=500p tau1=50p \
td2=505p tau2=250p
I57 (vdd! net1323) isource type=exp val0=0.0 val1=2.5m td1=500p tau1=50p \
td2=505p tau2=250p

////////**Coupling capacitances and line to ground capacitances**//////////
C326 (Ainv11 net1003) capacitor c=165.6f
C325 (net1003 0) capacitor c=20.1825f
C324 (Ainv11 0) capacitor c=20.1825f
C323 (Ainv12 0) capacitor c=20.1825f
C322 (net1047 0) capacitor c=20.1825f
C321 (Ainv12 net1047) capacitor c=165.6f
C320 (Ainv13 net1067) capacitor c=165.6f
C319 (net1067 0) capacitor c=20.1825f
C318 (Ainv13 0) capacitor c=20.1825f
C317 (Ainv14 0) capacitor c=20.1825f
C316 (net1111 0) capacitor c=20.1825f
C315 (Ainv14 net1111) capacitor c=165.6f
C314 (Ainv15 net1131) capacitor c=165.6f
C313 (net1131 0) capacitor c=20.1825f
C312 (Ainv15 0) capacitor c=20.1825f

C311 (Ainv16 0) capacitor c=20.1825f
C310 (net1175 0) capacitor c=20.1825f
C309 (Ainv16 net1175) capacitor c=165.6f
C308 (Ainv17 net1195) capacitor c=165.6f
C307 (net1195 0) capacitor c=20.1825f
C306 (Ainv17 0) capacitor c=20.1825f
C305 (Ainv18 0) capacitor c=20.1825f
C304 (net1239 0) capacitor c=20.1825f
C303 (Ainv18 net1239) capacitor c=165.6f
C302 (Ainv19 net1259) capacitor c=165.6f
C301 (net1259 0) capacitor c=20.1825f
C300 (Ainv19 0) capacitor c=20.1825f
C299 (Ainv20 0) capacitor c=20.1825f
C298 (net1303 0) capacitor c=20.1825f
C297 (Ainv20 net1303) capacitor c=165.6f
C296 (Ainv10 net1323) capacitor c=165.6f
C295 (net1323 0) capacitor c=20.1825f
C294 (Ainv10 0) capacitor c=20.1825f
C293 (Ainv9 0) capacitor c=20.1825f
C292 (net1367 0) capacitor c=20.1825f
C291 (Ainv9 net1367) capacitor c=165.6f
C290 (Ainv8 net1387) capacitor c=165.6f
C289 (net1387 0) capacitor c=20.1825f
C288 (Ainv8 0) capacitor c=20.1825f
C287 (Ainv7 0) capacitor c=20.1825f
C286 (net1431 0) capacitor c=20.1825f
C285 (Ainv7 net1431) capacitor c=165.6f
C284 (Ainv6 net1451) capacitor c=165.6f
C283 (net1451 0) capacitor c=20.1825f
C282 (Ainv6 0) capacitor c=20.1825f
C281 (Ainv5 0) capacitor c=20.1825f
C280 (net1495 0) capacitor c=20.1825f
C279 (Ainv5 net1495) capacitor c=165.6f
C278 (Ainv4 net1515) capacitor c=165.6f
C277 (net1515 0) capacitor c=20.1825f
C276 (Ainv4 0) capacitor c=20.1825f
C275 (Ainv3 0) capacitor c=20.1825f
C273 (Ainv3 net1559) capacitor c=165.6f
C272 (Ainv2 net1579) capacitor c=165.6f
C271 (net1579 0) capacitor c=20.1825f
C270 (Ainv2 0) capacitor c=20.1825f
C274 (net1559 0) capacitor c=20.1825f
C32 (A_4 net01318) capacitor c=165.6f
C57 (net01318 0) capacitor c=20.175f
C268 (Ainv1 Bhit1x) capacitor c=165.6f
C269 (Ainv1 0) capacitor c=20.1825f

C33 (A_4 0) capacitor c=20.175f
C66 (Bhit1x 0) capacitor c=20.1825f

//////////**Input voltage sources definition**//////////
V125 (net910 0) vsource dc=0 type=dc
V124 (net912 0) vsource dc=0 type=dc
V123 (net914 0) vsource dc=0 type=dc
V122 (net916 0) vsource dc=0 type=dc
V121 (net918 0) vsource dc=0 type=dc
V120 (net920 0) vsource dc=0 type=dc
V119 (net922 0) vsource dc=0 type=dc
V118 (net924 0) vsource dc=0 type=dc
V117 (net926 0) vsource dc=0 type=dc
V116 (net928 0) vsource dc=0 type=dc
V115 (net930 0) vsource dc=0 type=dc
V114 (net932 0) vsource dc=0 type=dc
V113 (net934 0) vsource dc=0 type=dc
V112 (net936 0) vsource dc=0 type=dc
V111 (net938 0) vsource dc=0 type=dc
V110 (net940 0) vsource dc=0 type=dc
V109 (net942 0) vsource dc=0 type=dc
V108 (net944 0) vsource dc=0 type=dc
V107 (net946 0) vsource dc=0 type=dc
V106 (net948 0) vsource dc=0 type=dc
V105 (net950 0) vsource dc=0 type=dc
V104 (net952 0) vsource dc=0 type=dc
V103 (net954 0) vsource dc=0 type=dc
V102 (net956 0) vsource dc=0 type=dc
V101 (net958 0) vsource dc=0 type=dc
V100 (net960 0) vsource dc=0 type=dc
V99 (net962 0) vsource dc=0 type=dc
V98 (net964 0) vsource dc=0 type=dc
V97 (net966 0) vsource dc=0 type=dc
V96 (net968 0) vsource dc=0 type=dc
V95 (net970 0) vsource dc=0 type=dc
V94 (net972 0) vsource dc=0 type=dc
V93 (net974 0) vsource dc=0 type=dc
V92 (net976 0) vsource dc=0 type=dc
V91 (net978 0) vsource dc=0 type=dc
V90 (net980 0) vsource dc=0 type=dc
V89 (net982 0) vsource dc=0 type=dc
V88 (net984 0) vsource dc=0 type=dc
V12 (net01211 0) vsource dc=0 type=dc
V86 (A1 0) vsource dc=0 type=dc
V87 (net986 0) vsource dc=0 type=dc
V0 (vdd! 0) vsource dc=vdd type=dc

/////////Transistor Parameter Definitions//////////

```
T1289 (A_4 net01310 0 0) nfet l=130.0n w=520.0n nf=1 m=1 par=1 ngcon=1 \
      ad=2.86e-13 as=2.86e-13 pd=2.14u ps=2.14u nrd=0.3846 nrs=0.3846 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T1288 (net01302 net0963 0 0) nfet l=130.0n w=520.0n nf=1 m=1 par=1 ngcon=1 \
      ad=2.86e-13 as=2.86e-13 pd=2.14u ps=2.14u nrd=0.3846 nrs=0.3846 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T1286 (net01318 net01302 0 0) nfet l=130.0n w=520.0n nf=1 m=1 par=1 \
      ngcon=1 ad=2.86e-13 as=2.86e-13 pd=2.14u ps=2.14u nrd=0.3846 \
      nrs=0.3846 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1283 (net01306 net01318 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 \
      ngcon=1 ad=1.43e-13 as=1.43e-13 pd=1.62u ps=1.62u nrd=0.7692 \
      nrs=0.7692 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1281 (Afinal_normal A_4 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 \
      ngcon=1 ad=1.43e-13 as=1.43e-13 pd=1.62u ps=1.62u nrd=0.7692 \
      nrs=0.7692 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1244 (net995 net910 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
      ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T1243 (net999 Ainv11 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
      ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T1242 (net1003 net1007 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
      ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

```
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1241 (net1007 net912 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1240 (net1011 net1003 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1239 (net1015 net1019 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1238 (net1019 net995 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1237 (Ainv11 net1015 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1164 (Ainv12 net1035 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1163 (net1031 net1055 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1162 (net1035 net1031 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
```

ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1161 (net1039 net1047 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1160 (net1043 net914 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1159 (net1047 net1043 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1158 (net1051 Ainv12 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1157 (net1055 net916 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1156 (net1059 net918 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1155 (net1063 Ainv13 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1154 (net1067 net1071 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1153 (net1071 net920 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1152 (net1075 net1067 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1151 (net1079 net1083 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1150 (net1083 net1059 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1149 (Ainv13 net1079 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1148 (Ainv14 net1099 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1147 (net1095 net1119 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1146 (net1099 net1095 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T1145 (net1103 net1111 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T840 (net1107 net922 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T839 (net1111 net1107 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T838 (net1115 Ainv14 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T837 (net1119 net924 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T836 (net1123 net926 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T835 (net1127 Ainv15 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \

```
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T834 (net1131 net1135 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T833 (net1135 net928 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T832 (net1139 net1131 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T831 (net1143 net1147 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T830 (net1147 net1123 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T829 (Ainv15 net1143 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T828 (Ainv16 net1163 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
```

```
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T827 (net1159 net1183 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T826 (net1163 net1159 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T825 (net1167 net1175 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T824 (net1171 net930 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T823 (net1175 net1171 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T822 (net1179 Ainv16 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T821 (net1183 net932 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T820 (net1187 net934 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

```
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T819 (net1191 Ainv17 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T818 (net1195 net1199 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T817 (net1199 net936 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T816 (net1203 net1195 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T815 (net1207 net1211 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T814 (net1211 net1187 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T813 (Ainv17 net1207 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T812 (Ainv18 net1227 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
```

ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T811 (net1223 net1247 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T810 (net1227 net1223 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T809 (net1231 net1239 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T808 (net1235 net938 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T807 (net1239 net1235 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T806 (net1243 Ainv18 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T805 (net1247 net940 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T804 (net1251 net942 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T803 (net1255 Ainv19 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T802 (net1259 net1263 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T801 (net1263 net944 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T800 (net1267 net1259 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T799 (net1271 net1275 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T798 (net1275 net1251 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T797 (Ainv19 net1271 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T796 (Ainv20 net1291 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T795 (net1287 net1311 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T794 (net1291 net1287 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T793 (net1295 net1303 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T792 (net1299 net946 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T791 (net1303 net1299 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T790 (net1307 Ainv20 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T789 (net1311 net948 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \

ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T788 (net1315 net950 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T787 (net1319 Ainv10 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T786 (net1323 net1327 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T785 (net1327 net952 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T784 (net1331 net1323 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T783 (net1335 net1339 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T782 (net1339 net1315 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T781 (Ainv10 net1335 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T764 (Ainv9 net1355 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T763 (net1351 net1375 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T762 (net1355 net1351 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T761 (net1359 net1367 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T760 (net1363 net954 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T759 (net1367 net1363 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T758 (net1371 Ainv9 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
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rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T757 (net1375 net956 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T756 (net1379 net958 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T755 (net1383 Ainv8 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T754 (net1387 net1391 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T753 (net1391 net960 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T752 (net1395 net1387 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T751 (net1399 net1403 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T750 (net1403 net1379 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \

ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T749 (Ainv8 net1399 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T732 (Ainv7 net1419 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T731 (net1415 net1439 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T730 (net1419 net1415 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T729 (net1423 net1431 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T728 (net1427 net962 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T727 (net1431 net1427 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

```
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T726 (net1435 Ainv7 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T725 (net1439 net964 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T724 (net1443 net966 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T723 (net1447 Ainv6 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T722 (net1451 net1455 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T721 (net1455 net968 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T720 (net1459 net1451 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T719 (net1463 net1467 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

```
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T718 (net1467 net1443 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T717 (Ainv6 net1463 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T700 (Ainv5 net1483 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T699 (net1479 net1503 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T698 (net1483 net1479 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T697 (net1487 net1495 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T696 (net1491 net970 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T695 (net1495 net1491 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
```

ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T694 (net1499 Ainv5 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T693 (net1503 net972 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T692 (net1507 net974 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T691 (net1511 Ainv4 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T690 (net1515 net1519 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T689 (net1519 net976 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T688 (net1523 net1515 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T687 (net1527 net1531 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T686 (net1531 net1507 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T685 (Ainv4 net1527 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T668 (Ainv3 net1547 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T667 (net1543 net1567 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T666 (net1547 net1543 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T665 (net1551 net1559 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T664 (net1555 net978 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T663 (net1559 net1555 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T662 (net1563 Ainv3 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T661 (net1567 net980 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T652 (net1571 net982 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T651 (net1575 Ainv2 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T650 (net1579 net1583 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T649 (net1583 net984 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T648 (net1587 net1579 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \

```
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T647 (net1591 net1595 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T646 (net1595 net1571 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T645 (Ainv2 net1591 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T170 (net01310 net01322 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.43e-13 as=1.43e-13 pd=1.62u ps=1.62u nrd=0.7692 nrs=0.7692 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1 (net01298 net01211 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.43e-13 as=1.43e-13 pd=1.62u ps=1.62u nrd=0.7692 nrs=0.7692 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T169 (net01322 net01298 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.43e-13 as=1.43e-13 pd=1.62u ps=1.62u nrd=0.7692 nrs=0.7692 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T643 (net1631 A1 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
```

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T160 (Bhit1x net1619 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T161 (net1619 net986 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T162 (net1615 Bhit1x 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T243 (net1611 net1607 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T242 (net1607 net1631 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T244 (Ainv1 net1611 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T644 (net1627 Ainv1 0 0) nfet l=130.0n w=260.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.13e-13 as=1.13e-13 pd=1.485u ps=1.485u nrd=1.2093 nrs=1.2093 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T1290 (A_4 net01310 vdd! vdd!) pfet l=130.0n w=1.44u nf=1 m=1 par=1 \
    ngcon=1 ad=7.92e-13 as=7.92e-13 pd=3.98u ps=3.98u nrd=0.1389 \
    nrs=0.1389 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1287 (net01302 net0963 vdd! vdd!) pfet l=130.0n w=1.44u nf=1 m=1 par=1 \
    ngcon=1 ad=7.92e-13 as=7.92e-13 pd=3.98u ps=3.98u nrd=0.1389 \
    nrs=0.1389 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1285 (net01318 net01302 vdd! vdd!) pfet l=130.0n w=1.44u nf=1 m=1 par=1 \
    ngcon=1 ad=7.92e-13 as=7.92e-13 pd=3.98u ps=3.98u nrd=0.1389 \
    nrs=0.1389 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1284 (net01306 net01318 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.2778 \
    nrs=0.2778 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1282 (Afinal_normal A_4 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.2778 \
    nrs=0.2778 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1252 (Ainv11 net1015 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1251 (net1011 net1003 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1250 (net1003 net1007 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1249 (net1007 net912 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
```

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1248 (net995 net910 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1247 (net999 Ainv11 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1246 (net1019 net995 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1245 (net1015 net1019 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1236 (net1035 net1031 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1235 (net1031 net1055 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1234 (net1051 Ainv12 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

```
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1233 (net1055 net916 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1232 (net1043 net914 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1231 (net1047 net1043 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1230 (net1039 net1047 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1229 (Ainv12 net1035 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1228 (Ainv13 net1079 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1227 (net1075 net1067 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1226 (net1067 net1071 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1225 (net1071 net920 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1224 (net1059 net918 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1223 (net1063 Ainv13 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1222 (net1083 net1059 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1221 (net1079 net1083 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1220 (net1099 net1095 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1219 (net1095 net1119 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1218 (net1115 Ainv14 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
```

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1217 (net1119 net924 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1216 (net1107 net922 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1215 (net1111 net1107 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1214 (net1103 net1111 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1213 (Ainv14 net1099 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1212 (Ainv15 net1143 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1211 (net1139 net1131 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

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    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1210 (net1131 net1135 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1209 (net1135 net928 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1208 (net1123 net926 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1207 (net1127 Ainv15 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1206 (net1147 net1123 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1205 (net1143 net1147 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1204 (net1163 net1159 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1203 (net1159 net1183 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
```

lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1202 (net1179 Ainv16 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1201 (net1183 net932 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1200 (net1171 net930 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1199 (net1175 net1171 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1198 (net1167 net1175 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1197 (Ainv16 net1163 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1196 (Ainv17 net1207 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1195 (net1203 net1195 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1194 (net1195 net1199 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1193 (net1199 net936 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1192 (net1187 net934 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1191 (net1191 Ainv17 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1190 (net1211 net1187 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1189 (net1207 net1211 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1188 (net1227 net1223 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

```
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1187 (net1223 net1247 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1186 (net1243 Ainv18 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1185 (net1247 net940 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1184 (net1235 net938 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1183 (net1239 net1235 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1182 (net1231 net1239 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1181 (Ainv18 net1227 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1180 (Ainv19 net1271 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1179 (net1267 net1259 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1178 (net1259 net1263 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1177 (net1263 net944 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1176 (net1251 net942 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1175 (net1255 Ainv19 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1174 (net1275 net1251 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1173 (net1271 net1275 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1172 (net1291 net1287 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1171 (net1287 net1311 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1170 (net1307 Ainv20 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1169 (net1311 net948 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1168 (net1299 net946 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1167 (net1303 net1299 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1166 (net1295 net1303 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1165 (Ainv20 net1291 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

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    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T780 (Ainv10 net1335 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T779 (net1331 net1323 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T778 (net1323 net1327 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T777 (net1327 net952 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T776 (net1315 net950 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T775 (net1319 Ainv10 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T774 (net1339 net1315 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T773 (net1335 net1339 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T772 (net1355 net1351 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T771 (net1351 net1375 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T770 (net1371 Ainv9 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T769 (net1375 net956 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T768 (net1363 net954 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T767 (net1367 net1363 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T766 (net1359 net1367 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T765 (Ainv9 net1355 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
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ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T748 (Ainv8 net1399 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T747 (net1395 net1387 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T746 (net1387 net1391 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T745 (net1391 net960 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T744 (net1379 net958 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T743 (net1383 Ainv8 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T742 (net1403 net1379 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

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    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T741 (net1399 net1403 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T740 (net1419 net1415 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T739 (net1415 net1439 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T738 (net1435 Ainv7 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T737 (net1439 net964 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T736 (net1427 net962 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T735 (net1431 net1427 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T734 (net1423 net1431 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T733 (Ainv7 net1419 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T716 (Ainv6 net1463 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T715 (net1459 net1451 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T714 (net1451 net1455 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T713 (net1455 net968 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T712 (net1443 net966 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T711 (net1447 Ainv6 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T710 (net1467 net1443 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
```

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T709 (net1463 net1467 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T708 (net1483 net1479 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T707 (net1479 net1503 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T706 (net1499 Ainv5 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T705 (net1503 net972 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T704 (net1491 net970 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T703 (net1495 net1491 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

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    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T702 (net1487 net1495 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T701 (Ainv5 net1483 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T684 (Ainv4 net1527 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T683 (net1523 net1515 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T682 (net1515 net1519 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T681 (net1519 net976 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T680 (net1507 net974 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T679 (net1511 Ainv4 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
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    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T678 (net1531 net1507 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T677 (net1527 net1531 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T676 (net1547 net1543 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T675 (net1543 net1567 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T674 (net1563 Ainv3 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T673 (net1567 net980 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T672 (net1555 net978 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T671 (net1559 net1555 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
```

ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T670 (net1551 net1559 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T669 (Ainv3 net1547 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T660 (Ainv2 net1591 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T659 (net1587 net1579 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T658 (net1579 net1583 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T657 (net1583 net984 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T656 (net1571 net982 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

```
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T655 (net1575 Ainv2 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T654 (net1595 net1571 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T653 (net1591 net1595 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T0 (net01298 net01211 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.2778 \
    nrs=0.2778 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T168 (net01322 net01298 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.2778 \
    nrs=0.2778 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T171 (net01310 net01322 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.2778 \
    nrs=0.2778 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T163 (net1615 Bhit1x vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T164 (Bhit1x net1619 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
```

```
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T165 (net1619 net986 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T166 (net1631 A1 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
    ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T167 (net1627 Ainv1 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T245 (net1607 net1631 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T246 (net1611 net1607 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T247 (Ainv1 net1611 vdd! vdd!) pfet l=130.0n w=720.0n nf=1 m=1 par=1 \
    ngcon=1 ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 \
    nrs=0.3852 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0

//////////Simulation performed and output file definitions//////////
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
   tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
   digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
   sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=10n write="spectre.ic" writefinal="spectre.fc" \
```

```
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
```

IBM 180 nm – Various Device Dimensions

```
// Generated for: spectre
// Generated on: Jun 29 13:44:09 2006
// Design library name: NSREC06_crosstalk
// Design cell name: JULY06_VaryingInvSizes_180nm_1500um_anu
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters vdd=1.8
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmrf7sf/V1.1.0.0ML/Spectre/models/allModels.scs
"

// Library name: NSREC06_crosstalk
// Cell name: JULY06_VaryingInvSizes_180nm_1500um_anu
// View name: schematic
```

/////////Diodes to limit the current pulse going one voltage drop above and below the rail//////////

```
D14 (Bhit4x 0) diodenwx dtemp=0.0
D15 (Bhit4x vdd!) diodenwx dtemp=0.0
D16 (Bhit5x vdd!) diodenwx dtemp=0.0
D17 (Bhit5x 0) diodenwx dtemp=0.0
D19 (Bhit7x vdd!) diodenwx dtemp=0.0
D18 (Bhit7x 0) diodenwx dtemp=0.0
D2 (Bafter2inv1 vdd!) diodenwx dtemp=0.0
D3 (Bafter2inv1 0) diodenwx dtemp=0.0
D12 (Bhit3x vdd!) diodenwx dtemp=0.0
D0 (Bhit2x 0) diodenwx dtemp=0.0
D1 (Bhit2x vdd!) diodenwx dtemp=0.0
D13 (Bhit3x 0) diodenwx dtemp=0.0
```

/////////Double exponential current pulses to define the SE strike//////////

```
I23 (vdd! Bhit3x) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
      td2=505p tau2=250p
```

I22 (vdd! Bhit4x) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
td2=505p tau2=250p
I20 (vdd! Bhit7x) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
td2=505p tau2=250p
I21 (vdd! Bhit5x) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
td2=505p tau2=250p
I25 (vdd! Bafter2inv1) isource type=exp val0=0.0 val1=1.5m td1=500p \
tau1=50p td2=505p tau2=250p
I24 (vdd! Bhit2x) isource type=exp val0=0.0 val1=1.5m td1=500p tau1=50p \
td2=505p tau2=250p

//////////**Coupling capacitances and line to ground capacitances**//////////
C73 (Bhit5x 0) capacitor c=55.5f
C74 (Ainv5x Bhit5x) capacitor c=159f
C75 (Ainv5x 0) capacitor c=55.5f
C70 (Ainv4x 0) capacitor c=55.5f
C71 (Ainv4x Bhit4x) capacitor c=159f
C72 (Bhit4x 0) capacitor c=55.5f
C78 (Bhit7x 0) capacitor c=55.5f
C77 (Ainv7x Bhit7x) capacitor c=159f
C76 (Ainv7x 0) capacitor c=55.5f
C51 (Bafter2inv1 0) capacitor c=55.5f
C16 (Ainv1x Bafter2inv1) capacitor c=159f
C17 (Ainv1x 0) capacitor c=55.5f
C53 (Ainv2x Bhit2x) capacitor c=159f
C68 (Ainv3x Bhit3x) capacitor c=159f
C67 (Bhit3x 0) capacitor c=55.5f
C54 (Bhit2x 0) capacitor c=55.5f
C69 (Ainv3x 0) capacitor c=55.5f
C52 (Ainv2x 0) capacitor c=55.5f

//////////**Input voltage sources definition**//////////
V32 (net278 0) vsource dc=0 type=dc
V33 (net276 0) vsource dc=0 type=dc
V30 (net282 0) vsource dc=0 type=dc
V31 (net280 0) vsource dc=0 type=dc
V36 (net272 0) vsource dc=0 type=dc
V35 (net274 0) vsource dc=0 type=dc
V18 (net290 0) vsource dc=0 type=dc
V19 (net288 0) vsource dc=0 type=dc
V34 (A1 0) vsource dc=0 type=dc
V6 (B1 0) vsource dc=0 type=dc
V29 (net284 0) vsource dc=0 type=dc
V28 (net286 0) vsource dc=0 type=dc
V0 (vdd! 0) vsource dc=vdd type=dc

//////////**Transistor Parameter Definitions**//////////

```
T219 (net451 net455 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T218 (net455 net288 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T225 (net427 Bhit2x 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T220 (net447 net451 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T221 (Ainv2x net447 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T222 (net439 Ainv2x 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T223 (net435 net290 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
     rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
     panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
     sb=5.5e-07 sd=3.6e-07 dtemp=0
T224 (Bhit2x net435 0 0) nfet l=180.0n w=720.0n nf=1 m=1 par=1 ngcon=1 \
     ad=3.56e-13 as=3.56e-13 pd=2.405u ps=2.405u nrd=0.3852 nrs=0.3852 \
     rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T258 (net487 net475 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T260 (net483 net487 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T254 (Bhit4x net391 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T262 (Ainv1x net483 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T158 (net475 A1 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T157 (Afinal3 Ainv1x 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T154 (Bfinal1 Bafter2inv1 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 \
ngcon=1 ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 \
nrs=0.8254 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T151 (Bhit1 B1 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \

ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T152 (Bafter2inv1 Bhit1 0 0) nfet l=180.0n w=360.0n nf=1 m=1 par=1 ngcon=1 \
ad=1.66e-13 as=1.66e-13 pd=1.685u ps=1.685u nrd=0.8254 nrs=0.8254 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T292 (net319 Bhit7x 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T273 (net359 net276 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T274 (Bhit5x net359 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T277 (net351 Bhit5x 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T279 (net347 Ainv5x 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T281 (Ainv5x net339 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

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    sb=5.5e-07 sd=3.6e-07 dtemp=0
T282 (net339 net335 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
    ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T285 (net335 net331 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
    ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T286 (net331 net278 0 0) nfet l=180.0n w=1.8u nf=1 m=1 par=1 ngcon=1 \
    ad=9.26e-13 as=9.26e-13 pd=4.565u ps=4.565u nrd=0.1481 nrs=0.1481 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T257 (net383 Bhit4x 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T264 (Ainv4x net371 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T267 (net371 net367 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T268 (net367 net363 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T251 (net379 Ainv4x 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
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rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T253 (net391 net282 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T301 (net303 net299 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T302 (net299 net272 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T294 (net315 Ainv7x 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T297 (Ainv7x net307 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T298 (net307 net303 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T290 (net327 net274 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \
ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T291 (Bhit7x net327 0 0) nfet l=180.0n w=2.52u nf=1 m=1 par=1 ngcon=1 \

ad=1.306e-12 as=1.306e-12 pd=6.005u ps=6.005u nrd=0.1051 \
nrs=0.1051 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T235 (net423 net286 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T236 (net419 net423 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T239 (net415 net419 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T240 (Ainv3x net415 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T243 (net407 Ainv3x 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T244 (net403 net284 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T247 (Bhit3x net403 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \

```
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T248 (net395 Bhit3x 0 0) nfet l=180.0n w=1.08u nf=1 m=1 par=1 ngcon=1 \
    ad=5.46e-13 as=5.46e-13 pd=3.125u ps=3.125u nrd=0.2512 nrs=0.2512 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T271 (net363 net280 0 0) nfet l=180.0n w=1.44u nf=1 m=1 par=1 ngcon=1 \
    ad=7.36e-13 as=7.36e-13 pd=3.845u ps=3.845u nrd=0.1864 nrs=0.1864 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T226 (net455 net288 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T233 (net427 Bhit2x vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T227 (net451 net455 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T228 (net447 net451 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T229 (Ainv2x net447 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T230 (net439 Ainv2x vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
    ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T231 (net435 net290 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T232 (Bhit2x net435 vdd! vdd!) pfet l=180.0n w=2u nf=1 m=1 par=1 ngcon=1 \
ad=1.031e-12 as=1.031e-12 pd=4.965u ps=4.965u nrd=0.133 nrs=0.133 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T238 (net415 net419 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T259 (net487 net475 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \
ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T261 (net483 net487 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \
ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T263 (Ainv1x net483 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \
ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T276 (net351 Bhit5x vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T150 (Bhit1 B1 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \

```
    ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T153 (Bafter2inv1 Bhit1 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 \
    ngcon=1 ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 \
    nrs=0.2723 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T156 (Afinal3 Ainv1x vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \
    ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T155 (Bfinal1 Bafter2inv1 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 \
    ngcon=1 ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 \
    nrs=0.2723 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T159 (net475 A1 vdd! vdd!) pfet l=180.0n w=1u nf=1 m=1 par=1 ngcon=1 \
    ad=5.04e-13 as=5.04e-13 pd=2.965u ps=2.965u nrd=0.2723 nrs=0.2723 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T234 (net423 net286 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
    ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
T275 (Bhit5x net359 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T278 (net347 Ainv5x vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
```

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    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T280 (Ainv5x net339 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T283 (net339 net335 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T284 (net335 net331 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T287 (net331 net278 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T255 (Bhit4x net391 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T256 (net383 Bhit4x vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T265 (Ainv4x net371 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T266 (net371 net367 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
```

```
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T269 (net367 net363 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T270 (net363 net280 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T272 (net359 net276 vdd! vdd!) pfet l=180.0n w=5u nf=1 m=1 par=1 ngcon=1 \
    ad=2.614e-12 as=2.614e-12 pd=10.965u ps=10.965u nrd=0.0525 \
    nrs=0.0525 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T252 (net391 net282 vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
    ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
    nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T299 (net307 net303 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
    ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
    nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T300 (net303 net299 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
    ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
    nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T303 (net299 net272 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
    ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
    nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T295 (net315 Ainv7x vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
```

ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T296 (Ainv7x net307 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T293 (net319 Bhit7x vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T289 (net327 net274 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T237 (net419 net423 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T241 (Ainv3x net415 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T242 (net407 Ainv3x vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
sb=5.5e-07 sd=3.6e-07 dtemp=0
T288 (Bhit7x net327 vdd! vdd!) pfet l=180.0n w=7u nf=1 m=1 par=1 ngcon=1 \
ad=3.669e-12 as=3.669e-12 pd=14.965u ps=14.965u nrd=0.0374 \
nrs=0.0374 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \

```
      sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T245 (net403 net284 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
      ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T246 (Bhit3x net403 vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
      ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T249 (net395 Bhit3x vdd! vdd!) pfet l=180.0n w=3u nf=1 m=1 par=1 ngcon=1 \
      ad=1.559e-12 as=1.559e-12 pd=6.965u ps=6.965u nrd=0.088 nrs=0.088 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=3.6e-07 dtemp=0
T250 (net379 Ainv4x vdd! vdd!) pfet l=180.0n w=4u nf=1 m=1 par=1 ngcon=1 \
      ad=2.086e-12 as=2.086e-12 pd=8.965u ps=8.965u nrd=0.0657 \
      nrs=0.0657 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0

//////////Simulation performed and output file definitions//////////
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
   tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
   digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
   sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=10n write="spectre.ic" writefinal="spectre.fc" \
   annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
save I20:sink
saveOptions options save=allpub
```

Generic 90 nm – Various Interconnect Lengths

```
// Generated for: spectre
// Generated on: Jul  7 10:24:08 2006
// Design library name: NSREC06_crosstalk
// Design cell name: JULY06_Inv1x_variouslinelengths_90nm_anu
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters vdd=1.2
include "/gpfs0/home/balasua/TImodellib/pmos90nm.mod"
include "/gpfs0/home/balasua/TImodellib/nmos90nm.mod"
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmrf8sf/V1.3.0.2LM/Spectre/models/allModels.scs
"

// Library name: NSREC06_crosstalk
// Cell name: JULY06_Inv1x_variouslinelengths_90nm_anu
// View name: schematic
```

////////Diodes to limit the current pulse going one voltage drop above and below the rail//////////

```
D21 (net01213 vdd!) diodenwx dtemp=0.0
D20 (net01213 0) diodenwx dtemp=0.0
D3 (net0476 0) diodenwx dtemp=0.0
D18 (net037 0) diodenwx dtemp=0.0
D19 (net037 vdd!) diodenwx dtemp=0.0
D9 (net0424 vdd!) diodenwx dtemp=0.0
D10 (net0396 vdd!) diodenwx dtemp=0.0
D5 (net0464 vdd!) diodenwx dtemp=0.0
D4 (net0464 0) diodenwx dtemp=0.0
D15 (net0356 0) diodenwx dtemp=0.0
D1 (net0504 vdd!) diodenwx dtemp=0.0
D0 (net0504 0) diodenwx dtemp=0.0
D2 (net0476 vdd!) diodenwx dtemp=0.0
D6 (net0436 vdd!) diodenwx dtemp=0.0
D7 (net0436 0) diodenwx dtemp=0.0
D14 (net0356 vdd!) diodenwx dtemp=0.0
D12 (net0384 0) diodenwx dtemp=0.0
D13 (net0384 vdd!) diodenwx dtemp=0.0
D16 (net0344 0) diodenwx dtemp=0.0
D17 (net0344 vdd!) diodenwx dtemp=0.0
D11 (net0396 0) diodenwx dtemp=0.0
D8 (net0424 0) diodenwx dtemp=0.0
```

//////////**Double exponential current pulses to define the SE strike**//////////

```
I34 (vdd! net01213) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I33 (vdd! net0344) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I30 (vdd! net0396) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I26 (vdd! net0476) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I28 (vdd! net0436) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I31 (vdd! net0384) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I27 (vdd! net0464) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I29 (vdd! net0424) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I32 (vdd! net0356) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I17 (vdd! net0504) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
I0 (vdd! net037) isource type=exp val0=0.0 val1=1mA td1=500p tau1=50p \
      td2=505p tau2=250p
```

//////////**Coupling capacitances and line to ground capacitances**//////////

```
C85 (net01213 0) capacitor c=931.5a
C84 (A_100 0) capacitor c=931.5a
C83 (A_100 net01213) capacitor c=13.6f
C68 (A_inv9 0) capacitor c=41.9175f
C69 (A_inv9 net0356) capacitor c=612f
C70 (A_inv10 net0344) capacitor c=680f
C71 (A_inv10 0) capacitor c=46.575f
C55 (A_inv2 0) capacitor c=9.315f
C54 (A_inv2 net0504) capacitor c=136f
C72 (net037 0) capacitor c=4.6575f
C73 (net0504 0) capacitor c=9.315f
C74 (net0476 0) capacitor c=13.9725f
C75 (net0464 0) capacitor c=18.63f
C76 (net0436 0) capacitor c=23.2875f
C77 (net0424 0) capacitor c=27.945f
C78 (net0396 0) capacitor c=32.6025f
C79 (net0384 0) capacitor c=37.26f
C80 (net0356 0) capacitor c=41.9175f
C81 (net0344 0) capacitor c=46.575f
C0 (A_inv net037) capacitor c=68f
C60 (A_inv5 0) capacitor c=23.2875f
```

C61 (A_inv5 net0436) capacitor c=340f
C62 (A_inv6 net0424) capacitor c=408f
C63 (A_inv6 0) capacitor c=27.945f
C56 (A_inv3 0) capacitor c=13.9725f
C57 (A_inv3 net0476) capacitor c=204f
C58 (A_inv4 net0464) capacitor c=272f
C59 (A_inv4 0) capacitor c=18.63f
C64 (A_inv7 0) capacitor c=32.6025f
C65 (A_inv7 net0396) capacitor c=476f
C66 (A_inv8 net0384) capacitor c=544f
C67 (A_inv8 0) capacitor c=37.26f
C2 (A_inv 0) capacitor c=4.6575f

////////**Transistor Parameter Definitions**//////////
M365 (net01217 net01551 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M364 (net01205 net01217 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M363 (net01209 net01213 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M362 (net01201 A_100 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
ad=.208p ps=1.94u pd=1.94u
M361 (net01213 net01197 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M360 (net01197 net01549 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M359 (A_100 net01225 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
ad=.208p ps=1.94u pd=1.94u
M358 (net01225 net01205 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M353 (net01534 net01546 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M349 (net01550 net01856 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M350 (net01546 net01854 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M347 (net01558 net01562 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M348 (A_inv9 net01558 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
ad=.208p ps=1.94u pd=1.94u
M352 (net01538 net01534 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u
M351 (A_inv10 net01538 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
ad=.208p ps=1.94u pd=1.94u
M346 (net01562 net01550 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
as=.208p ad=.208p ps=1.94u pd=1.94u

```
M285 (net0821 net0825 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M286 (A_inv net0821 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M331 (net01590 net01594 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M333 (net01582 net01860 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M337 (net01566 net01578 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M336 (net01570 net01566 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M335 (A_inv8 net01570 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M332 (A_inv7 net01590 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M268 (net0364 A_inv9 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M269 (net0360 net0538 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M270 (net0356 net0360 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M271 (net0352 net0356 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M194 (net0500 net0564 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M272 (net0348 net0344 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M273 (net0344 net0340 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M274 (net0340 net0532 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M275 (net0336 A_inv10 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M195 (net0496 A_inv2 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M193 (net0504 net0500 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M334 (net01578 net01858 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M330 (net01594 net01582 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M188 (net0508 net0504 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M304 (net01634 net01630 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
```

```
M305 (net01630 net01642 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M289 (net0805 net0801 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M228 (net0444 A_inv5 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M296 (A_inv3 net01654 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M295 (net01654 net01658 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M229 (net0440 net0554 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M230 (net0436 net0440 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M231 (net0432 net0436 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M232 (net0428 net0424 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M294 (net01658 net01646 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M208 (net0484 A_inv3 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M209 (net0480 net0562 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M210 (net0476 net0480 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M211 (net0472 net0476 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M297 (net01646 net01868 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M248 (net0404 A_inv7 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M212 (net0468 net0464 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M249 (net0400 net0546 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M185 (net0989 net043 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M186 (net037 net0989 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M184 (net025 A_inv vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M187 (net033 net037 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M288 (A_inv2 net0805 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
```

```
M233 (net0424 net0420 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M213 (net0464 net0460 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M250 (net0396 net0400 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M290 (net0801 net0813 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M251 (net0392 net0396 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M214 (net0460 net0556 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M215 (net0456 A_inv4 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M302 (net01642 net01866 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M313 (net01614 net01864 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M234 (net0420 net0548 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M282 (net0825 net0829 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M1 (net0829 net201 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M235 (net0416 A_inv6 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M318 (net01610 net01862 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M252 (net0388 net0384 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M253 (net0384 net0380 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M254 (net0380 net0540 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M255 (net0376 A_inv8 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M319 (A_inv6 net01602 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M320 (net01602 net01598 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M321 (net01598 net01610 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
      as=.208p ad=.208p ps=1.94u pd=1.94u
M303 (A_inv4 net01634 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
M312 (A_inv5 net01622 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
      ad=.208p ps=1.94u pd=1.94u
```

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M311 (net01622 net01626 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M196 (net0813 net0566 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n as=.208p \
     ad=.208p ps=1.94u pd=1.94u
M310 (net01626 net01614 vdd! vdd!) pch_1p2v_1233c027 w=650n l=120n \
     as=.208p ad=.208p ps=1.94u pd=1.94u
M373 (net01197 net01549 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M372 (net01201 A_100 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M371 (net01205 net01217 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M370 (net01209 net01213 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M369 (net01213 net01197 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M368 (net01217 net01551 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M367 (A_100 net01225 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M366 (net01225 net01205 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M345 (net01550 net01856 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M357 (net01534 net01546 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M342 (net01562 net01550 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M356 (net01538 net01534 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M355 (A_inv10 net01538 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M344 (A_inv9 net01558 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M354 (net01546 net01854 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M328 (A_inv7 net01590 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M338 (net01578 net01858 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M284 (net0821 net0825 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M287 (A_inv net0821 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
M292 (net0805 net0801 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
     ad=.0832p ps=1.16u pd=1.16u
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M293 (net0801 net0813 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M341 (net01566 net01578 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M327 (net01590 net01594 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M326 (net01594 net01582 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M307 (A_inv4 net01634 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M314 (net01626 net01614 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M277 (net0348 net0344 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M278 (net0344 net0340 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M279 (net0340 net0532 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M280 (net0336 A_inv10 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M291 (A_inv2 net0805 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M199 (net0500 net0564 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M200 (net0496 A_inv2 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M198 (net0504 net0500 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M201 (net0813 net0566 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M197 (net0508 net0504 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M324 (net01602 net01598 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M329 (net01582 net01860 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M339 (A_inv8 net01570 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M340 (net01570 net01566 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M263 (net0364 A_inv9 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M264 (net0360 net0538 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M265 (net0356 net0360 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
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```
M298 (net01658 net01646 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M306 (net01642 net01866 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M308 (net01634 net01630 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M243 (net0404 A_inv7 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M244 (net0400 net0546 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M245 (net0396 net0400 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M246 (net0392 net0396 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M203 (net0484 A_inv3 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M0 (net0829 net201 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M204 (net0480 net0562 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M205 (net0476 net0480 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M206 (net0472 net0476 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M299 (net01654 net01658 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M191 (net037 net0989 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M192 (net033 net037 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M283 (net0825 net0829 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M300 (A_inv3 net01654 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M343 (net01558 net01562 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M217 (net0468 net0464 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M218 (net0464 net0460 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M219 (net0460 net0556 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M237 (net0428 net0424 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M238 (net0424 net0420 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
```

```
M239 (net0420 net0548 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M240 (net0416 A_inv6 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M315 (net01622 net01626 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M316 (A_inv5 net01622 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M257 (net0388 net0384 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M309 (net01630 net01642 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M258 (net0384 net0380 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M259 (net0380 net0540 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M260 (net0376 A_inv8 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M189 (net025 A_inv 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M190 (net0989 net043 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M220 (net0456 A_inv4 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M322 (net01610 net01862 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M317 (net01614 net01864 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M323 (A_inv6 net01602 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M325 (net01598 net01610 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M301 (net01646 net01868 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M266 (net0352 net0356 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M223 (net0444 A_inv5 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M224 (net0440 net0554 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M225 (net0436 net0440 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
M226 (net0432 net0436 0 0) nch_1p2v_1233c027 w=260n l=120n as=.0832p \
      ad=.0832p ps=1.16u pd=1.16u
```

//////////**Input voltage sources definition**//////////
V61 (net01549 0) vsource dc=0 type=dc
V60 (net01551 0) vsource dc=0 type=dc
V58 (net01856 0) vsource dc=0 type=dc
V50 (net201 0) vsource dc=0 type=dc
V57 (net01858 0) vsource dc=0 type=dc
V56 (net01860 0) vsource dc=0 type=dc
V51 (net0566 0) vsource dc=0 type=dc
V49 (net0532 0) vsource dc=0 type=dc
V33 (net0564 0) vsource dc=0 type=dc
V59 (net01854 0) vsource dc=0 type=dc
V0 (vdd! 0) vsource dc=vdd type=dc
V42 (net0546 0) vsource dc=0 type=dc
V34 (net0562 0) vsource dc=0 type=dc
V46 (net0538 0) vsource dc=0 type=dc
V41 (net0548 0) vsource dc=0 type=dc
V45 (net0540 0) vsource dc=0 type=dc
V53 (net01866 0) vsource dc=0 type=dc
V38 (net0554 0) vsource dc=0 type=dc
V54 (net01864 0) vsource dc=0 type=dc
V55 (net01862 0) vsource dc=0 type=dc
V52 (net01868 0) vsource dc=0 type=dc
V1 (net043 0) vsource dc=0 type=dc
V37 (net0556 0) vsource dc=0 type=dc

//////////**Simulation performed and output file definitions**//////////
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=10n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save I26:sink
saveOptions options save=allpub

APPENDIX C

3D TCAD MIXED-MODE SIMULATION FILES

This appendix lists all the files used for defining the 3D structures (NMOS and PMOS) and for setting up the mixed-mode simulations.

3D TCAD structure: Devise File for the NMOS device

This file contains the structural dimensions, the doping profiles and the meshing for the calibrated IBM 90 nm CMOS9SF NMOS device.

```
(isegeo:set-default-boolean "ABA")

; Bulk silicon
(isegeo:create-cuboid (position -5 85 5)        (position 5 75 0)       "Silicon" "R.Bulk")


; Gate oxides and gate polysilicon
(isegeo:create-cuboid (position -1.82 80 0)             (position -1.74 80.2 -0.0014)
"SiO2"    "R.GateOxidePC")
(isegeo:create-cuboid (position -1.82 80 -0.0014)     (position -1.74 80.2 -0.1414)
"PolySi"  "R.PolyGatePC")

(isegeo:create-cuboid (position 1.82 80 0)              (position 1.74 80.2 -0.0014)  "SiO2"
"R.GateOxidePD")
(isegeo:create-cuboid (position 1.82 80 -0.0014)      (position 1.74 80.2 -0.1414)
"PolySi"  "R.PolyGatePD")


; Field oxide extensions
;(isegeo:create-cuboid (position -1.82 80 -0.0)                (position -1.74 79.82 -0.014)
"SiO2" "R.FieldOxideP1C")
;(isegeo:create-cuboid (position -1.82 80.2 -0.0)      (position -1.74 80.38 -0.014) "SiO2"
"R.FieldOxideP2C")
```

```
;(isegeo:create-cuboid (position 1.82 80 -0.0)                (position 1.74 79.82 -0.014)
"SiO2" "R.FieldOxideP1D")
;(isegeo:create-cuboid (position 1.82 80.2 -0.0)       (position 1.74 80.38 -0.014) "SiO2"
"R.FieldOxideP2D")


;Gate poly extensions
;(isegeo:create-cuboid (position -1.82 80 -0.014)      (position -1.74 79.82 -0.1414)
"PolySi" "R.PolyGateP1C")
;(isegeo:create-cuboid (position -1.82 80.2 -0.014)   (position -1.74 80.38 -0.1414)
"PolySi" "R.PolyGateP2C")

;(isegeo:create-cuboid (position 1.82 80 -0.014)       (position 1.74 79.82 -0.1414)
"PolySi" "R.PolyGateP1D")
;(isegeo:create-cuboid (position 1.82 80.2 -0.014)    (position 1.74 80.38 -0.1414)
"PolySi" "R.PolyGateP2D")


;STI
(isegeo:create-cuboid (position -5 80 0)        (position -2.06 80.2 0.36) "SiO2"
"R.STI1A")
(isegeo:create-cuboid (position -1.5 80 0)      (position 0.0 80.2 0.36)   "SiO2"
"R.STI2A")
(isegeo:create-cuboid (position 5 80 0)         (position 2.06 80.2 0.36)  "SiO2"
"R.STI3A")
(isegeo:create-cuboid (position 1.5 80 0)       (position 0.0 80.2 0.36)   "SiO2"
"R.STI4A")

(isegeo:create-cuboid (position -5 85 0)        (position 5 80.68 0.36)   "SiO2" "R.STI5")
(isegeo:create-cuboid (position -5 80.48 0)     (position 5 80.2 0.36)   "SiO2" "R.STI6")
(isegeo:create-cuboid (position -5 80 0)        (position 5 75 0.36)     "SiO2" "R.STI7")


;contacts
(isegeo:define-contact-set "DrainC"    4.0  (color:rgb 1.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "GateC"     4.0  (color:rgb 1.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "SourceC"   4.0  (color:rgb 1.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "DrainD"    4.0  (color:rgb 1.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "GateD"     4.0  (color:rgb 1.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "SourceD"   4.0  (color:rgb 1.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "PwellB"    4.0  (color:rgb 0.0 1.0 1.0 ) "##")


(isegeo:create-cuboid (position -1.82 80  -0.1414)    (position -1.74 80.2 -2) "Metal"
"GatemetalC")
(isegeo:define-3d-contact (find-face-id (position -1.78 80.1 -0.1414)) "GateC")
```

```
(isegeo:delete-region (find-body-id (position -1.78 80.1 -1)))

(isegeo:create-cuboid (position 1.82 80 -0.1414)      (position 1.74 80.2 -2) "Metal"
"GatemetalD")
(isegeo:define-3d-contact (find-face-id (position 1.78 80.1 -0.1414)) "GateD")
(isegeo:delete-region (find-body-id (position 1.78 80.1 -1)))

(isegeo:create-cuboid (position -4.9 80.51 0)          (position 4.9 80.65 -2) "Metal"
"PwellmetalB")
(isegeo:define-3d-contact (find-face-id (position 0 80.58 0)) "PwellB")
(isegeo:delete-region (find-body-id (position 0 80.58 -1)))

;(isegeo:define-3d-contact (find-face-id (position 0 0 5))    "Substrate")


(isegeo:create-cuboid (position -1.86 80.04 0)          (position -1.98 80.16 -2) "Metal"
"SourcePmetalC")
(isegeo:define-3d-contact (find-face-id (position -1.94 80.1 0)) "SourceC")
(isegeo:delete-region (find-body-id (position -1.94 80.1 -1)))


(isegeo:create-cuboid (position 1.86 80.04 0)          (position 1.98 80.16 -2) "Metal"
"SourcePmetalD")
(isegeo:define-3d-contact (find-face-id (position 1.94 80.1 0)) "SourceD")
(isegeo:delete-region (find-body-id (position 1.94 80.1 -1)))


;Commented out drains for device with no interconnect

(isegeo:create-cuboid (position -1.7 80.04 0)          (position -1.58 80.16 -2) "Metal"
"DrainPmetalC")
(isegeo:define-3d-contact (find-face-id (position -1.62 80.1 0)) "DrainC")
(isegeo:delete-region (find-body-id (position -1.62 80.1 -1)))

(isegeo:create-cuboid (position 1.7 80.04 0)  (position 1.58 80.16 -2) "Metal"
"DrainPmetalD")
(isegeo:define-3d-contact (find-face-id (position 1.62 80.1 0)) "DrainD")
(isegeo:delete-region (find-body-id (position 1.62 80.1 -1)))


; ------------- Adding some dopings for the device ------------------------------------------------
; ----- First, all the constant doping profiles-------------------------------------------------------

; Constant Doping in the poly
; Constant Doping in the poly
```

```
(isedr:define-constant-profile "Profile.Polyconst.Phos" "ArsenicActiveConcentration"
1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1" "Profile.Polyconst.Phos"
"PolySi")


; -- Constant Doping in the silicon substrate region
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid" (position -5 85 0)
(position 5 75 5))
(isedr:define-constant-profile "Profile.Silconst.Bor" "BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor" "Profile.Silconst.Bor"
"Window.Silconst.Bor")


; -- Boron doping in the silicon
; --   Assumes deep pwell implant goes through whole die
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle" (position -5
85 1.25) (position 5 75 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1"
"Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace" "Eval")


; PWELL doping
(isedr:define-refinement-window "Window.PWell.Bor.2" "Rectangle" (position -5 85
0.65) (position 5 75 0.65))
(isedr:define-gaussian-profile "Profile.PWell.Bor.2" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.35 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.2" "Profile.PWell.Bor.2"
"Window.PWell.Bor.2" "Symm" "NoReplace" "Eval")


; pwell contact doping
(isedr:define-refinement-window "Window.PWellCon.Bor.3B" "Rectangle" (position  -5
80.48 0) (position 5 80.68 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3B" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3B"
"Profile.PWellCon.Bor.3B" "Window.PWellCon.Bor.3B" "Symm" "NoReplace" "Eval")
```

```
; STI Implant - Front & Back Extensions NMOS
(isedr:define-refinement-window "Window.FrontPC" "Cuboid" (position -1.82 80 0)
(position -1.74 79.985 0.36))
(isedr:define-refinement-window "Window.BackPC" "Cuboid" (position -1.82 80.2 0)
(position -1.74 80.215 0.36))
(isedr:define-constant-profile "Profile.ImplantC" "BoronActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontPC" "Profile.ImplantC"
"Window.FrontPC")
(isedr:define-constant-profile-placement "Place.Implant.BackPC" "Profile.ImplantC"
"Window.BackPC")

(isedr:define-refinement-window "Window.FrontPD" "Cuboid" (position 1.82  80 0)
(position 1.74 79.985 0.36))
(isedr:define-refinement-window "Window.BackPD" "Cuboid" (position 1.82 80.2 0)
(position 1.74 80.215 0.36))
(isedr:define-constant-profile "Profile.ImplantD" "BoronActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontPD" "Profile.ImplantD"
"Window.FrontPD")
(isedr:define-constant-profile-placement "Place.Implant.BackPD" "Profile.ImplantD"
"Window.BackPD")


; -- Arsenic/boron doping of the drain/source in the silicon
; DRAIN C SIDE NMOS
(isedr:define-refinement-window "drain.Profile.RegionC" "Rectangle" (position -1.712
80 0) (position -1.5 80.2 0))
(isedr:define-gaussian-profile "drain.ProfileC" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceC" "drain.ProfileC"
"drain.Profile.RegionC" "Symm" "NoReplace" "Eval")


; SOURCE C SIDE NMOS
(isedr:define-refinement-window "source.Profile.RegionC" "Rectangle" (position -1.848
80 0) (position -2.06 80.2 0))
(isedr:define-gaussian-profile "source.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceC" "source.ProfileC"
"source.Profile.RegionC" "Symm" "NoReplace" "Eval")


; DRAIN D SIDE NMOS
(isedr:define-refinement-window "drain.Profile.RegionD" "Rectangle" (position 1.712 80
0) (position 1.5 80.2 0))
(isedr:define-gaussian-profile "drain.ProfileD" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
```

```
(isedr:define-analytical-profile-placement "drain.Profile.PlaceD" "drain.ProfileD"
"drain.Profile.RegionD" "Symm" "NoReplace" "Eval")


; SOURCE D SIDE NMOS
(isedr:define-refinement-window "source.Profile.RegionD" "Rectangle" (position 1.848
80 0) (position 2.06 80.2 0))
(isedr:define-gaussian-profile "source.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceD" "source.ProfileD"
"source.Profile.RegionD" "Symm" "NoReplace" "Eval")


; Lightly doped drain/source
; LDD - DRAIN C SIDE NMOS
(isedr:define-refinement-window "drainldd.Profile.RegionC" "Rectangle" (position -
1.755 80 0) (position -1.708 80.2 0))
(isedr:define-gaussian-profile "drainldd.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2.2e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceC" "drainldd.ProfileC"
"drainldd.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LDD - SOURCE C SIDE NMOS
(isedr:define-refinement-window "sourceldd.Profile.RegionC" "Rectangle" (position -
1.805 80 0) (position -1.852 80.2 0))
(isedr:define-gaussian-profile "sourceldd.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2.2e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceC"
"sourceldd.ProfileC" "sourceldd.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LDD - DRAIN D SIDE NMOS
(isedr:define-refinement-window "drainldd.Profile.RegionD" "Rectangle" (position 1.755
80 0) (position 1.708 80.2 0))
(isedr:define-gaussian-profile "drainldd.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2.2e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceD" "drainldd.ProfileD"
"drainldd.Profile.RegionD" "Symm" "NoReplace" "Eval")


; LDD - SOURCE D SIDE NMOS
(isedr:define-refinement-window "sourceldd.Profile.RegionD" "Rectangle" (position
1.805 80 0) (position 1.852 80.2 0))
(isedr:define-gaussian-profile "sourceldd.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2.2e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
```

```
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceD"
"sourceldd.ProfileD" "sourceldd.Profile.RegionD" "Symm" "NoReplace" "Eval")


; halo structure
; HALO - DRAIN C SIDE
(isedr:define-refinement-window "drainhalo.Profile.RegionC" "Rectangle" (position -
1.76 80 0.03) (position -1.755 80.2 0.03))
(isedr:define-gaussian-profile "drainhalo.ProfileC" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainhalo.Profile.PlaceC"
"drainhalo.ProfileC" "drainhalo.Profile.RegionC" "Symm" "NoReplace" "Eval")


; HALO - SOURCE C SIDE
(isedr:define-refinement-window "sourcehalo.Profile.RegionC" "Rectangle" (position -
1.8 80 0.03) (position -1.805 80.2 0.03))
(isedr:define-gaussian-profile "sourcehalo.ProfileC" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcehalo.Profile.PlaceC"
"sourcehalo.ProfileC" "sourcehalo.Profile.RegionC" "Symm" "NoReplace" "Eval")


; HALO - DRAIN D SIDE
(isedr:define-refinement-window "drainhalo.Profile.RegionD" "Rectangle" (position 1.76
80 0.03) (position 1.755 80.2 0.03))
(isedr:define-gaussian-profile "drainhalo.ProfileD" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainhalo.Profile.PlaceD"
"drainhalo.ProfileD" "drainhalo.Profile.RegionD" "Symm" "NoReplace" "Eval")


; HALO - SOURCE D SIDE
(isedr:define-refinement-window "sourcehalo.Profile.RegionD" "Rectangle" (position 1.8
80 0.03) (position 1.805 80.2 0.03))
(isedr:define-gaussian-profile "sourcehalo.ProfileD" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcehalo.Profile.PlaceD"
"sourcehalo.ProfileD" "sourcehalo.Profile.RegionD" "Symm" "NoReplace" "Eval")


; threshold voltage implant
; Vt IMPLANT C NMOS
(isedr:define-refinement-window "implant.Profile.RegionC" "Rectangle" (position -1.81
80 0.01) (position -1.75 80.2 0.01))
```

```
(isedr:define-gaussian-profile "implant.ProfileC" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 1.1e19 "ValueAtDepth" 6e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceC" "implant.ProfileC"
"implant.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LEAKAGE IMPLANT C (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.RegionC" "Rectangle" (position -1.81
80 0.03) (position -1.75 80.2 0.03))
(isedr:define-gaussian-profile "limplant.ProfileC" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 7e18 "ValueAtDepth" 2e17 "Depth" 0.005 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceC" "limplant.ProfileC"
"limplant.Profile.RegionC" "Symm" "NoReplace" "Eval")


; Vt IMPLANT D NMOS
(isedr:define-refinement-window "implant.Profile.RegionD" "Rectangle" (position 1.81
80 0.01) (position 1.75 80.2 0.01))
(isedr:define-gaussian-profile "implant.ProfileD" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 1.1e19 "ValueAtDepth" 6e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceD" "implant.ProfileD"
"implant.Profile.RegionD" "Symm" "NoReplace" "Eval")


; LEAKAGE IMPLANT D (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.RegionD" "Rectangle" (position 1.81
80 0.03) (position 1.75 80.2 0.03))
(isedr:define-gaussian-profile "limplant.ProfileD" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 7e18 "ValueAtDepth" 2e17 "Depth" 0.005 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceD" "limplant.ProfileD"
"limplant.Profile.RegionD" "Symm" "NoReplace" "Eval")


;bulk meshing
; Meshing Strategy:
(isedr:define-refinement-size "size.wholea" 0.25 0.25 0.25 0.25 0.25 0.1)
(isedr:define-refinement-window "window.wholea" "Cuboid" (position -5 85 0) (position
5 75 1.5))
(isedr:define-refinement-placement "placement.wholea" "size.wholea" "window.wholea"
)

(isedr:define-refinement-size "size.whole2a" 0.5 0.5 0.5 0.5 0.5 0.25)
(isedr:define-refinement-window "window.whole2a" "Cuboid" (position -5 85 1.5)
(position 5 75 5))
```

```
(isedr:define-refinement-placement "placement.whole2a" "size.whole2a"
"window.whole2a" )


;p-well contact meshing
(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.05 0.05 0.05 0.025)
(isedr:define-refinement-function "size.dopingmesha" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position -5 80.48 0)
(position 5 80.68 0.1))
(isedr:define-refinement-placement "placement.dopingmesha" "size.dopingmesha"
"window.dopingmesha" )


; SOURCE/DRAIN C MESH
(isedr:define-refinement-size "size.dopingmesh1c" 0.025 0.1 0.025 0.025 0.025 0.01)
(isedr:define-refinement-function "size.dopingmesh1c" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh1c" "Cuboid" (position -2.06 80
0) (position -1.5 80.2 0.36))
(isedr:define-refinement-placement "placement.dopingmesh1c" "size.dopingmesh1c"
"window.dopingmesh1c" )


; VT & LEAKAGE C IMPLANT MESH
(isedr:define-refinement-size "size.dopingmesh2c" 0.01 0.05 0.01 0.005 0.01 0.005)
(isedr:define-refinement-function "size.dopingmesh2c" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh2c" "Cuboid" (position -1.84 80
0) (position -1.72 80.2 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2c" "size.dopingmesh2c"
"window.dopingmesh2c" )


; SOURCE/DRAIN D MESH
(isedr:define-refinement-size "size.dopingmesh1d" 0.025 0.1 0.025 0.025 0.025 0.01)
(isedr:define-refinement-function "size.dopingmesh1d" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh1d" "Cuboid" (position 2.06 80 0)
(position 1.5 80.2 0.36))
(isedr:define-refinement-placement "placement.dopingmesh1d" "size.dopingmesh1d"
"window.dopingmesh1d" )


; VT & LEAKAGE D IMPLANT MESH
(isedr:define-refinement-size "size.dopingmesh2d" 0.01 0.05 0.01 0.005 0.01 0.005)
```

```
(isedr:define-refinement-function "size.dopingmesh2d" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh2d" "Cuboid" (position 1.84 80 0)
(position 1.72 80.2 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2d" "size.dopingmesh2d"
"window.dopingmesh2d" )

(ise:save-model "NMOS")
; (ise:build-mesh "mesh""-R" "CMOS")
```

3D TCAD structure: Devise File for the PMOS device

This file contains the structural dimensions, the doping profiles and the meshing for the calibrated IBM 90 nm CMOS9SF PMOS device.

```
(isegeo:set-default-boolean "ABA")

; Bulk silicon
(isegeo:create-cuboid (position -5 85 5)        (position 5 75 0)       "Silicon" "R.Bulk")

; Gate oxides and gate polysilicon
(isegeo:create-cuboid (position -1.82 80 0)             (position -1.74 80.48 -0.0014)
"SiO2"    "R.GateOxidePC")
(isegeo:create-cuboid (position -1.82 80 -0.0014)     (position -1.74 80.48 -0.1414)
"PolySi"  "R.PolyGatePC")

(isegeo:create-cuboid (position 1.82 80 0)              (position 1.74 80.48 -0.0014)
"SiO2"    "R.GateOxidePD")
(isegeo:create-cuboid (position 1.82 80 -0.0014)      (position 1.74 80.48 -0.1414)
"PolySi"  "R.PolyGatePD")

; Field oxide extensions
;(isegeo:create-cuboid (position -1.82 80 -0.0)                (position -1.74 79.82 -0.014)
"SiO2" "R.FieldOxideP1C")
;(isegeo:create-cuboid (position -1.82 80.48 -0.0)    (position -1.74 80.66 -0.014) "SiO2"
"R.FieldOxideP2C")

;(isegeo:create-cuboid (position 1.82 80 -0.0)                 (position 1.74 79.82 -0.014)
"SiO2" "R.FieldOxideP1D")
```

```
;(isegeo:create-cuboid (position 1.82 80.48 -0.0)       (position 1.74 80.66 -0.014) "SiO2"
"R.FieldOxideP2D")


; Gate poly extensions
;(isegeo:create-cuboid (position -1.82 80 -0.014)       (position -1.74 79.82 -0.1414)
"PolySi" "R.PolyGateP1C")
;(isegeo:create-cuboid (position -1.82 80.48 -0.014) (position -1.74 80.66 -0.1414)
"PolySi" "R.PolyGateP2C")

;(isegeo:create-cuboid (position 1.82 80 -0.014)        (position 1.74 79.82 -0.1414)
"PolySi" "R.PolyGateP1D")
;(isegeo:create-cuboid (position 1.82 80.48 -0.014)   (position 1.74 80.66 -0.1414)
"PolySi" "R.PolyGateP2D")


; STI
(isegeo:create-cuboid (position -5 80 0)         (position -2.06 80.48 0.36) "SiO2"
"R.STI1A")
(isegeo:create-cuboid (position -1.5 80 0)       (position 0.0 80.48 0.36)   "SiO2"
"R.STI2A")
(isegeo:create-cuboid (position 5 80 0)          (position 2.06 80.48 0.36)  "SiO2"
"R.STI3A")
(isegeo:create-cuboid (position 1.5 80 0)        (position 0.0 80.48 0.36)   "SiO2"
"R.STI4A")


(isegeo:create-cuboid (position -5 85 0)         (position 5 80.96 0.36)   "SiO2" "R.STI5")
(isegeo:create-cuboid (position -5 80.76 0)   (position 5 80.48 0.36)   "SiO2" "R.STI6")
(isegeo:create-cuboid (position -5 80 0)         (position 5 75 0.36)     "SiO2" "R.STI7")


; contacts
(isegeo:define-contact-set "DrainC"    4.0  (color:rgb 1.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "GateC"     4.0  (color:rgb 1.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "SourceC"   4.0  (color:rgb 1.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "DrainD"    4.0  (color:rgb 1.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "GateD"     4.0  (color:rgb 1.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "SourceD"   4.0  (color:rgb 1.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "NwellB"    4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "Substrate"     4.0  (color:rgb 0.0 1.0 1.0 ) "##")


(isegeo:create-cuboid (position -1.82 80  -0.1414)    (position -1.74 80.48 -2) "Metal"
"GatemetalC")
(isegeo:define-3d-contact (find-face-id (position -1.78 80.24 -0.1414)) "GateC")
```

```
(isegeo:delete-region (find-body-id (position -1.78 80.24 -1)))


(isegeo:create-cuboid (position 1.82 80 -0.1414)       (position 1.74 80.48 -2) "Metal"
"GatemetalD")
(isegeo:define-3d-contact (find-face-id (position 1.78 80.24 -0.1414)) "GateD")
(isegeo:delete-region (find-body-id (position 1.78 80.24 -1)))


(isegeo:create-cuboid (position -4.9 80.79 0)          (position 4.9 80.93 -2) "Metal"
"NwellmetalB")
(isegeo:define-3d-contact (find-face-id (position 0 80.86 0)) "NwellB")
(isegeo:delete-region (find-body-id (position 0 80.86 -1)))

(isegeo:define-3d-contact (find-face-id (position 0 80 5))    "Substrate")


(isegeo:create-cuboid (position -1.86 80.18 0)         (position -1.98 80.3 -2) "Metal"
"SourcePmetalC")
(isegeo:define-3d-contact (find-face-id (position -1.94 80.24 0)) "SourceC")
(isegeo:delete-region (find-body-id (position -1.94 80.24 -1)))


(isegeo:create-cuboid (position 1.86 80.18 0)          (position 1.98 80.3 -2) "Metal"
"SourcePmetalD")
(isegeo:define-3d-contact (find-face-id (position 1.94 80.24 0)) "SourceD")
(isegeo:delete-region (find-body-id (position 1.94 80.24 -1)))


; Commented out drains for device with no interconnect
(isegeo:create-cuboid (position -1.7 80.18 0)          (position -1.58 80.3 -2) "Metal"
"DrainPmetalC")
(isegeo:define-3d-contact (find-face-id (position -1.62 80.24 0)) "DrainC")
(isegeo:delete-region (find-body-id (position -1.62 80.24 -1)))

(isegeo:create-cuboid (position 1.7 80.18 0)  (position 1.58 80.3 -2) "Metal"
"DrainPmetalD")
(isegeo:define-3d-contact (find-face-id (position 1.62 80.24 0)) "DrainD")
(isegeo:delete-region (find-body-id (position 1.62 80.24 -1)))


; ------------- Adding some dopings for the device ----------------------------------------------
; ----- First, all the constant doping profiles-----------------------------------------------

; Constant Doping in the poly
; Constant Doping in the poly
```

```
(isedr:define-constant-profile "Profile.Polyconst.Phos" "BoronActiveConcentration"
1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1" "Profile.Polyconst.Phos"
"PolySi")


; -- Constant Doping in the silicon substrate region
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid" (position -5 85 0)
(position 5 75 5))
(isedr:define-constant-profile "Profile.Silconst.Bor" "BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor" "Profile.Silconst.Bor"
"Window.Silconst.Bor")


; -- Boron doping in the silicon
; --   Assumes deep pwell implant goes through whole die
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle" (position -5
85 1.25) (position 5 75 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1"
"Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace" "Eval")


; N-well doping
(isedr:define-refinement-window "Window.NWell.Bor.2" "Rectangle" (position -5 85
0.45) (position 5 75 0.45))
(isedr:define-gaussian-profile "Profile.NWell.Bor.2" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 1e17 "ValueAtDepth" 1e16 "Depth" 0.45 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.NWell.Bor.2" "Profile.NWell.Bor.2"
"Window.NWell.Bor.2" "Symm" "NoReplace" "Eval")


; nwell contact doping
(isedr:define-refinement-window "Window.NWellCon.Bor.3B" "Rectangle" (position  -5
80.76 0) (position 5 80.96 0))
(isedr:define-gaussian-profile "Profile.NWellCon.Bor.3B" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "Place.NWellCon.Bor.3B"
"Profile.NWellCon.Bor.3B" "Window.NWellCon.Bor.3B" "Symm" "NoReplace" "Eval")
```

```
; STI Implant - Front & Back Extensions PMOS
 (isedr:define-refinement-window "Window.FrontPC" "Cuboid" (position -1.82 80 0)
(position -1.74 79.985 0.36))
(isedr:define-refinement-window "Window.BackPC" "Cuboid" (position -1.82 80.48 0)
(position -1.74 80.495 0.36))
(isedr:define-constant-profile "Profile.ImplantC" "ArsenicActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontPC" "Profile.ImplantC"
"Window.FrontPC")
(isedr:define-constant-profile-placement "Place.Implant.BackPC" "Profile.ImplantC"
"Window.BackPC")


(isedr:define-refinement-window "Window.FrontPD" "Cuboid" (position 1.82  80 0)
(position 1.74 79.985 0.36))
(isedr:define-refinement-window "Window.BackPD" "Cuboid" (position 1.82 80.48 0)
(position 1.74 80.495 0.36))
(isedr:define-constant-profile "Profile.ImplantD" "ArsenicActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontPD" "Profile.ImplantD"
"Window.FrontPD")
(isedr:define-constant-profile-placement "Place.Implant.BackPD" "Profile.ImplantD"
"Window.BackPD")


; -- Arsenic/boron doping of the drain/source in the silicon
; DRAIN C SIDE PMOS
(isedr:define-refinement-window "drain.Profile.RegionC" "Rectangle" (position -1.712
80 0) (position -1.5 80.48 0))
(isedr:define-gaussian-profile "drain.ProfileC" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceC" "drain.ProfileC"
"drain.Profile.RegionC" "Symm" "NoReplace" "Eval")


; SOURCE C SIDE PMOS
(isedr:define-refinement-window "source.Profile.RegionC" "Rectangle" (position -1.848
80 0) (position -2.06 80.48 0))
(isedr:define-gaussian-profile "source.ProfileC" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceC" "source.ProfileC"
"source.Profile.RegionC" "Symm" "NoReplace" "Eval")


; DRAIN D SIDE PMOS
(isedr:define-refinement-window "drain.Profile.RegionD" "Rectangle" (position 1.712 80
0) (position 1.5 80.48 0))
```

```
(isedr:define-gaussian-profile "drain.ProfileD" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceD" "drain.ProfileD"
"drain.Profile.RegionD" "Symm" "NoReplace" "Eval")


; SOURCE D SIDE PMOS
(isedr:define-refinement-window "source.Profile.RegionD" "Rectangle" (position 1.848
80 0) (position 2.06 80.48 0))
(isedr:define-gaussian-profile "source.ProfileD" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceD" "source.ProfileD"
"source.Profile.RegionD" "Symm" "NoReplace" "Eval")


; lightly doped drain/source
; LDD - DRAIN C SIDE PMOS
(isedr:define-refinement-window "drainldd.Profile.RegionC" "Rectangle" (position -
1.755 80 0) (position -1.708 80.48 0))
(isedr:define-gaussian-profile "drainldd.ProfileC" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceC" "drainldd.ProfileC"
"drainldd.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LDD - SOURCE C SIDE PMOS
(isedr:define-refinement-window "sourceldd.Profile.RegionC" "Rectangle" (position -
1.805 80 0) (position -1.852 80.48 0))
(isedr:define-gaussian-profile "sourceldd.ProfileC" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceC"
"sourceldd.ProfileC" "sourceldd.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LDD - DRAIN D SIDE PMOS
(isedr:define-refinement-window "drainldd.Profile.RegionD" "Rectangle" (position 1.755
80 0) (position 1.708 80.48 0))
(isedr:define-gaussian-profile "drainldd.ProfileD" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceD" "drainldd.ProfileD"
"drainldd.Profile.RegionD" "Symm" "NoReplace" "Eval")


; LDD - SOURCE D SIDE PMOS
(isedr:define-refinement-window "sourceldd.Profile.RegionD" "Rectangle" (position
1.805 80 0) (position 1.852 80.48 0))
```

```
(isedr:define-gaussian-profile "sourceldd.ProfileD" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceD"
"sourceldd.ProfileD" "sourceldd.Profile.RegionD" "Symm" "NoReplace" "Eval")


; halo structure
; HALO - DRAIN C SIDE
(isedr:define-refinement-window "drainhalo.Profile.RegionC" "Rectangle" (position -
1.76 80 0.04) (position -1.755 80.48 0.04))
(isedr:define-gaussian-profile "drainhalo.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 5e18 "ValueAtDepth" 4e17 "Depth" 0.035 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainhalo.Profile.PlaceC"
"drainhalo.ProfileC" "drainhalo.Profile.RegionC" "Symm" "NoReplace" "Eval")


; HALO - SOURCE C SIDE
(isedr:define-refinement-window "sourcehalo.Profile.RegionC" "Rectangle" (position -
1.8 80 0.04) (position -1.805 80.48 0.04))
(isedr:define-gaussian-profile "sourcehalo.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 5e18 "ValueAtDepth" 4e17 "Depth" 0.035 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcehalo.Profile.PlaceC"
"sourcehalo.ProfileC" "sourcehalo.Profile.RegionC" "Symm" "NoReplace" "Eval")


; HALO - DRAIN D SIDE
(isedr:define-refinement-window "drainhalo.Profile.RegionD" "Rectangle" (position 1.76
80 0.04) (position 1.755 80.48 0.04))
(isedr:define-gaussian-profile "drainhalo.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 5e18 "ValueAtDepth" 4e17 "Depth" 0.035 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainhalo.Profile.PlaceD"
"drainhalo.ProfileD" "drainhalo.Profile.RegionD" "Symm" "NoReplace" "Eval")


; HALO - SOURCE D SIDE
(isedr:define-refinement-window "sourcehalo.Profile.RegionD" "Rectangle" (position 1.8
80 0.04) (position 1.805 80.48 0.04))
(isedr:define-gaussian-profile "sourcehalo.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 5e18 "ValueAtDepth" 4e17 "Depth" 0.035 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcehalo.Profile.PlaceD"
"sourcehalo.ProfileD" "sourcehalo.Profile.RegionD" "Symm" "NoReplace" "Eval")
```

```
; threshold voltage implant
; Vt IMPLANT C PMOS
(isedr:define-refinement-window "implant.Profile.RegionC" "Rectangle" (position -1.81
80 0.01) (position -1.75 80.48 0.01))
(isedr:define-gaussian-profile "implant.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 8e18 "ValueAtDepth" 6e17 "Depth" 0.01 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceC" "implant.ProfileC"
"implant.Profile.RegionC" "Symm" "NoReplace" "Eval")


; LEAKAGE IMPLANT C (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.RegionC" "Rectangle" (position -1.81
80 0.035) (position -1.75 80.48 0.035))
(isedr:define-gaussian-profile "limplant.ProfileC" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 8e18 "ValueAtDepth" 5e17 "Depth" 0.01 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceC" "limplant.ProfileC"
"limplant.Profile.RegionC" "Symm" "NoReplace" "Eval")


; Vt IMPLANT D PMOS
(isedr:define-refinement-window "implant.Profile.RegionD" "Rectangle" (position 1.81
80 0.01) (position 1.75 80.48 0.01))
(isedr:define-gaussian-profile "implant.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 8e18 "ValueAtDepth" 6e17 "Depth" 0.01 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceD" "implant.ProfileD"
"implant.Profile.RegionD" "Symm" "NoReplace" "Eval")


; LEAKAGE IMPLANT D (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.RegionD" "Rectangle" (position 1.81
80 0.035) (position 1.75 80.48 0.035))
(isedr:define-gaussian-profile "limplant.ProfileD" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 8e18 "ValueAtDepth" 5e17 "Depth" 0.01 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceD" "limplant.ProfileD"
"limplant.Profile.RegionD" "Symm" "NoReplace" "Eval")


; bulk meshing
; Meshing Strategy:
(isedr:define-refinement-size "size.wholea" 0.25 0.25 0.25 0.25 0.25 0.1)
(isedr:define-refinement-window "window.wholea" "Cuboid" (position -5 85 0) (position
5 75 1.5))
```

```
(isedr:define-refinement-placement "placement.wholea" "size.wholea" "window.wholea"
)

(isedr:define-refinement-size "size.whole2a" 0.5 0.5 0.5 0.5 0.5 0.25)
(isedr:define-refinement-window "window.whole2a" "Cuboid" (position -5 85 1.5)
(position 5 75 5))
(isedr:define-refinement-placement "placement.whole2a" "size.whole2a"
"window.whole2a" )


; n-well contact meshing
(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.05 0.05 0.05 0.025)
(isedr:define-refinement-function "size.dopingmesha" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position -5 80.76 0)
(position 5 80.96 0.1))
(isedr:define-refinement-placement "placement.dopingmesha" "size.dopingmesha"
"window.dopingmesha" )


; SOURCE/DRAIN C MESH
(isedr:define-refinement-size "size.dopingmesh1c" 0.025 0.1 0.025 0.025 0.025 0.01)
(isedr:define-refinement-function "size.dopingmesh1c" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh1c" "Cuboid" (position -2.06 80
0) (position -1.5 80.48 0.36))
(isedr:define-refinement-placement "placement.dopingmesh1c" "size.dopingmesh1c"
"window.dopingmesh1c" )


; VT & LEAKAGE C IMPLANT MESH
(isedr:define-refinement-size "size.dopingmesh2c" 0.01 0.05 0.01 0.005 0.01 0.005)
(isedr:define-refinement-function "size.dopingmesh2c" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh2c" "Cuboid" (position -1.84 80
0) (position -1.72 80.48 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2c" "size.dopingmesh2c"
"window.dopingmesh2c" )


; SOURCE/DRAIN D MESH
(isedr:define-refinement-size "size.dopingmesh1d" 0.025 0.1 0.025 0.025 0.025 0.01)
(isedr:define-refinement-function "size.dopingmesh1d" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh1d" "Cuboid" (position 2.06 80 0)
(position 1.5 80.48 0.36))
```

```
(isedr:define-refinement-placement "placement.dopingmesh1d" "size.dopingmesh1d"
"window.dopingmesh1d" )


; VT & LEAKAGE D IMPLANT MESH
(isedr:define-refinement-size "size.dopingmesh2d" 0.01 0.05 0.01 0.005 0.01 0.005)
(isedr:define-refinement-function "size.dopingmesh2d" "DopingConcentration"
"MaxTransDiff" 0.1)
(isedr:define-refinement-window "window.dopingmesh2d" "Cuboid" (position 1.84 80 0)
(position 1.72 80.48 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2d" "size.dopingmesh2d"
"window.dopingmesh2d" )

(ise:save-model "PMOS")
; (ise:build-mesh "mesh""-R" "CMOS")
```

3D Mixed-mode: Dessis File for the NMOS device simulations

This file contains the setup for the mixed-mode single event simulations for an N-hit (strike on the NMOS drain) using two NMOS devices calibrated in 3D TCAD, including the netlist for the SE induced crosstalk measurement structure.

```
#########################################################################

DEVICE CFET1{
File     {
      Grid    = "NMOS_msh.grd"
      Doping  = "NMOS_msh.dat"
      Param   = "dessis.par"

         }


Electrode {

         { Name="DrainC"      Voltage=0  }
         { Name="GateC"       Voltage=0   }
         { Name="SourceC"    Voltage=0   }
         { Name="DrainD"      Voltage=0   }
         { Name="GateD"       Voltage=0   }
```

```
        { Name="SourceD"    Voltage=0  }
        { Name="PwellB"     Voltage=0   }
        }


Physics {
      Recombination(SRH Auger) #TPA_gen
      Mobility( Phumob HighFieldsat Enormal)
      EffectiveIntrinsicDensity( OldSlotboom )
        Fermi
        HeavyIon(
        time=2e-9
        length=5
        wt_hi=0.05
        location=(1.64,80.1,0)
        direction=(0,0,1)
        LET_f=0.1
        Gaussian
        Picocoulomb )

        }


Plot    {
      Potential Electricfield
      eDensity hDensity
      eCurrent/Vector hCurrent/Vector
      TotalCurrent/Vector
      SRH Auger Avalanche
      eMobility hMobility
      eQuasiFermi hQuasiFermi
      eGradQuasiFermi hGradQuasiFermi
      eEparallel hEparallel
      eMobility hMobility
      eVelocity hVelocity
      DonorConcentration Acceptorconcentration
      Doping SpaceCharge
      ConductionBand ValenceBand
      BandGap Affinity
      xMoleFraction
      eTemperature hTemperature
      HeavyIonChargeDensity
        }
}
```

```
Math    {
        WallClock
        Extrapolate
        Derivatives
        RelErrControl
        Iterations=15
        notdamped=100
        Newdiscretization
        Method=slip
        RecBoxIntegr
        number_of_threads=2
        }


File    {
        Output = "xtalk150umlog"
        SPICEPath = "." ###path where your spice models are ###
        Plot    = "xtalk150um.dat"
        Current = "xtalk150um.plt"
        Load = "Biased_Device_Xtalk_des.sav"
      }


System{

        Vsource_pset  VDD   (HIGH 0){dc = 1.2}  ###voltage source  (HIGH 0) are
node names###

        Vsource_pset  GND   (GD 0){dc = 0}   ###voltage source (GND 0) are node
names###

        Vsource_pset  DATAA         (A1 0)  {dc = 1.2}   ###voltage source (A1 0) are
node names###

        Vsource_pset  DATAB         (B1 0)  {dc = 1.2}   ###voltage source (B1 0) are
node names###

        Capacitor_pset CP       (B3 A150)      {capacitance = 18.6e-15}       ###btw B3
and A150, coupling capacitance between the metal interconnects###

        Capacitor_pset CP1      (A150 0)       {capacitance = 1.295e-15}      ###btw A150
and GD, interconnect line to ground capacitance###

        Capacitor_pset CP2      (B3 0)         {capacitance = 1.295e-15}      ###btw B3
and GD, interconnect line to ground capacitance ###
```

######## mosfet (drain gate source bulk) ####################
###This is the TCAD device that is referenced above and connecting the electrodes to spice nodes here below##

```
CFET1device1                (

                        "DrainC"=A150
                        "GateC"=A4
                        "SourceC"=GD
                        "DrainD"=B3
                        "GateD"=B2
                        "SourceD"=GD
                        "PwellB"=GD   )
```

###These are spice transistors, PMOS_480 & NMOS_480 are the names from the spice model file, MP1-MP8 and MN1-MN8 are the names given here (drain gate source bulk) ###

```
PMOS_480    MP1    (A2 A1 HIGH HIGH)
            {w = 0.48e-6   l = 0.08e-6
            pd = 1.44e-6    ps = 1.44e-6
            ad = 1.15e-13  as = 1.15e-13}

NMOS_200    MN1    (A2 A1 GD GD)
            {w = 0.2e-6     l = 0.08e-6
            pd = 880e-9     ps = 880e-9
            ad = 0.48e-13  as = 0.48e-13}

PMOS_480    MP2    (A3 A2 HIGH HIGH)
            {w = 0.48e-6   l = 0.08e-6
            pd = 1.44e-6    ps = 1.44e-6
            ad = 1.15e-13  as = 1.15e-13}

NMOS_200    MN2    (A3 A2 GD GD)
            {w = 0.2e-6     l = 0.08e-6
            pd = 880e-9     ps = 880e-9
            ad = 0.48e-13  as = 0.48e-13}

PMOS_480    MP3    (A4 A3 HIGH HIGH)
            {w = 0.48e-6   l = 0.08e-6
            pd = 1.44e-6    ps = 1.44e-6
            ad = 1.15e-13  as = 1.15e-13}

NMOS_200    MN3    (A4 A3 GD GD)
            {w = 0.2e-6     l = 0.08e-6
```

```
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13  as = 0.48e-13}

        PMOS_480    MP4    (A150 A4 HIGH HIGH)
                    {w = 0.48e-6   l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
                    ad = 1.15e-13  as = 1.15e-13}

#       NMOS_200    MN4    (A150 A4 GD GD)
#                   {w = 0.2e-6     l = 0.08e-6
#                   pd = 880e-9     ps = 880e-9
#                   ad = 0.48e-13  as = 0.48e-13}

        PMOS_480    MP5    (A5 A150 HIGH HIGH)
                    {w = 0.48e-6   l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
                    ad = 1.15e-13  as = 1.15e-13}

        NMOS_200    MN5    (A5 A150 GD GD)
                    {w = 0.2e-6     l = 0.08e-6
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13  as = 0.48e-13}

        PMOS_480    MP6    (B2 B1 HIGH HIGH)
                    {w = 0.48e-6   l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
                    ad = 1.15e-13  as = 1.15e-13}

        NMOS_200    MN6    (B2 B1 GD GD)
                    {w = 0.2e-6     l = 0.08e-6
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13  as = 0.48e-13}

        PMOS_480    MP7    (B3 B2 HIGH HIGH)
                    {w = 0.48e-6   l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
                    ad = 1.15e-13  as = 1.15e-13}

#       NMOS_200    MN7    (B3 B2 GD GD)
#                   {w = 0.2e-6     l = 0.08e-6
#                   pd = 880e-9     ps = 880e-9
#                   ad = 0.48e-13  as = 0.48e-13}

        PMOS_480    MP8    (B4 B3 HIGH HIGH)
                    {w = 0.48e-6   l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
```

```
                    ad = 1.15e-13  as = 1.15e-13}

        NMOS_200    MN8    (B4 B3 GD GD)
                    {w = 0.2e-6     l = 0.08e-6
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13  as = 0.48e-13}


####This initializes the node outright to 0 volts, look at the manual for more
information###

#Initialize (A4 = 1.2)
#Initialize (A5 = 0)
#Initialize (A100 = 1.2)
#Initialize (B2 = 0)
#Initialize (B3 = 1.2)
#Initialize (B4 = 0)


### This is for the spice .plt file###
        Plot "xtalk3_spectre" (time()  v(A1) v(A2) v(A3) v(A4) v(A5) v(A150) v(B1)
v(B2) v(B3) v(B4) i(B3 0))

   }

Solve{
   Coupled (iterations=100) {Circuit}
   Coupled (iterations=100) {Poisson}
   Coupled (iterations=100) {Poisson Circuit}
   Coupled (iterations=100) {Poisson Circuit Contact}
   Coupled (iterations=100) {Poisson Hole Contact Circuit}
   Coupled (iterations=100) {Poisson Electron Hole Contact Circuit}

NewCurrentFile="xtalk_transient"

Transient (
        InitialTime=0
        FinalTime=1.98e-9
        InitialStep=1e-12
        MaxStep=1.5e-10 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="before" Time=(1.5e-9) NoOverwrite)
    }
```

```
Transient (
        InitialTime=1.98e-9
        FinalTime=2.5e-9
        InitialStep=1e-12
        MaxStep=1e-11 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="during" Time=(2e-9;2.05e-9;2.1e-9;2.25e-9;2.5e-9)
NoOverwrite)
    }


Transient (
        InitialTime=2.5e-9
        FinalTime=5e-9
        InitialStep=1e-12
        MaxStep=1.5e-10 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="after" Time=(3e-9;5e-9;10e-9) NoOverwrite)
    }


}
```

3D Mixed-mode: Dessis File for the PMOS device simulations

This file contains the setup for the mixed-mode single event simulations for a P-hit (strike on the PMOS drain) using two PMOS devices calibrated in 3D TCAD, including the netlist for the SE induced crosstalk measurement structure.

```
#########################################################################

DEVICE CFET1{
File    {
      Grid    = "PMOS_msh.grd"
      Doping  = "PMOS_msh.dat"
      Param   = "dessis.par"
```

```
        }

Electrode {
        { Name="DrainC"      Voltage=1.2  }
        { Name="GateC"       Voltage=1.2   }
        { Name="SourceC"    Voltage=1.2   }
        { Name="DrainD"      Voltage=1.2   }
        { Name="GateD"       Voltage=1.2   }
        { Name="SourceD"    Voltage=1.2  }
        { Name="NwellB"      Voltage=1.2   }
        { Name="Substrate"    Voltage=1.2   }
        }


Physics {
      Recombination(SRH Auger) #TPA_gen
      Mobility( Phumob HighFieldsat Enormal)
      EffectiveIntrinsicDensity( OldSlotboom )
         Fermi
         HeavyIon(
         time=2e-9
         length=5
         wt_hi=0.05
         location=(1.64,80.24,0)
         direction=(0,0,1)
         LET_f=0.1
         Gaussian
         Picocoulomb )

         }


Plot     {
      Potential Electricfield
      eDensity hDensity
      eCurrent/Vector hCurrent/Vector
      TotalCurrent/Vector
      SRH Auger Avalanche
      eMobility hMobility
      eQuasiFermi hQuasiFermi
      eGradQuasiFermi hGradQuasiFermi
      eEparallel hEparallel
      eMobility hMobility
      eVelocity hVelocity
      DonorConcentration Acceptorconcentration
      Doping SpaceCharge
```

```
      ConductionBand ValenceBand
      BandGap Affinity
      xMoleFraction
      eTemperature hTemperature
      HeavyIonChargeDensity
         }
}


Math   {
         WallClock
         Extrapolate
         Derivatives
         RelErrControl
         Iterations=15
         notdamped=100
         Newdiscretization
         Method=Slip
         RecBoxIntegr
         number_of_threads=2
         }


File     {
         Output = "xtalk150umlog"
         SPICEPath = "." ###path where your spice models are ###
         Plot    = "xtalk150um.dat"
         Current = "xtalk150um.plt"
         Load = "Biased_Device_Xtalk_des.sav"
      }

System{

         Vsource_pset  VDD   (HIGH 0){dc = 1.2}  ###voltage source  (HIGH 0) are
node names###

         Vsource_pset  GND   (GD 0){dc = 0}   ###voltage source (GND 0) are node
names###

         Vsource_pset  DATAA         (A1 0)  {dc = 0.0}   ###voltage source (A1 0) are
node names###

         Vsource_pset  DATAB         (B1 0)  {dc = 0.0}   ###voltage source (B1 0) are
node names###
```

Capacitor_pset CP (B3 A150) {capacitance = 18.6e-15} ###btw B3 and A150, coupling capacitance between the metal interconnects ###

Capacitor_pset CP1 (A150 0) {capacitance = 1.2956e-15} ###btw A150 and GD, interconnect line to ground capacitance ###

Capacitor_pset CP2 (B3 0) {capacitance = 1.295e-15} ###btw B3 and GD, interconnect line to ground capacitance ###

######## mosfet (drain gate source bulk) ####################
###This is the TCAD device that is referenced above and connecting the electrodes to spice nodes here below##

```
CFET1device1            (
                        "DrainC"=A150
                        "GateC"=A4
                        "SourceC"=HIGH
                        "DrainD"=B3
                        "GateD"=B2
                        "SourceD"=HIGH
                        "NwellB"=HIGH
                        "Substrate"=GD  )
```

###These are spice transistors, PMOS_480 and NMOS_480 are the names from the spice model file, MP1-MP8 and MN1-MN8 are the names given here (drain gate source bulk) ###

```
PMOS_480    MP1    (A2 A1 HIGH HIGH)
                   {w = 0.48e-6   l = 0.08e-6
                   pd = 1.44e-6    ps = 1.44e-6
                   ad = 1.15e-13  as = 1.15e-13}

NMOS_200    MN1    (A2 A1 GD GD)
                   {w = 0.2e-6     l = 0.08e-6
                   pd = 880e-9     ps = 880e-9
                   ad = 0.48e-13  as = 0.48e-13}

PMOS_480    MP2    (A3 A2 HIGH HIGH)
                   {w = 0.48e-6   l = 0.08e-6
                   pd = 1.44e-6    ps = 1.44e-6
                   ad = 1.15e-13  as = 1.15e-13}

NMOS_200    MN2    (A3 A2 GD GD)
```

```
                {w = 0.2e-6     l = 0.08e-6
                pd = 880e-9     ps = 880e-9
                ad = 0.48e-13   as = 0.48e-13}

        PMOS_480    MP3    (A4 A3 HIGH HIGH)
                {w = 0.48e-6    l = 0.08e-6
                pd = 1.44e-6    ps = 1.44e-6
                ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN3    (A4 A3 GD GD)
                {w = 0.2e-6     l = 0.08e-6
                pd = 880e-9     ps = 880e-9
                ad = 0.48e-13   as = 0.48e-13}

#       PMOS_480    MP4    (A150 A4 HIGH HIGH)
#               {w = 0.48e-6    l = 0.08e-6
#               pd = 1.44e-6    ps = 1.44e-6
#               ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN4    (A150 A4 GD GD)
                {w = 0.2e-6     l = 0.08e-6
                pd = 880e-9     ps = 880e-9
                ad = 0.48e-13   as = 0.48e-13}

        PMOS_480    MP5    (A5 A150 HIGH HIGH)
                {w = 0.48e-6    l = 0.08e-6
                pd = 1.44e-6    ps = 1.44e-6
                ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN5    (A5 A150 GD GD)
                {w = 0.2e-6     l = 0.08e-6
                pd = 880e-9     ps = 880e-9
                ad = 0.48e-13   as = 0.48e-13}

        PMOS_480    MP6    (B2 B1 HIGH HIGH)
                {w = 0.48e-6    l = 0.08e-6
                pd = 1.44e-6    ps = 1.44e-6
                ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN6    (B2 B1 GD GD)
                {w = 0.2e-6     l = 0.08e-6
                pd = 880e-9     ps = 880e-9
                ad = 0.48e-13   as = 0.48e-13}

#       PMOS_480    MP7    (B3 B2 HIGH HIGH)
#               {w = 0.48e-6    l = 0.08e-6
```

```
#                       pd = 1.44e-6    ps = 1.44e-6
#                       ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN7    (B3 B2 GD GD)
                    {w = 0.2e-6     l = 0.08e-6
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13   as = 0.48e-13}

        PMOS_480    MP8    (B4 B3 HIGH HIGH)
                    {w = 0.48e-6    l = 0.08e-6
                    pd = 1.44e-6    ps = 1.44e-6
                    ad = 1.15e-13   as = 1.15e-13}

        NMOS_200    MN8    (B4 B3 GD GD)
                    {w = 0.2e-6     l = 0.08e-6
                    pd = 880e-9     ps = 880e-9
                    ad = 0.48e-13   as = 0.48e-13}


####  This initializes the node outright to 0 volts, look at the manual for more
information###
#Initialize (A4 = 1.2)
#Initialize (A5 = 0)
#Initialize (A100 = 1.2)
#Initialize (B2 = 0)
#Initialize (B3 = 1.2)
#Initialize (B4 = 0)


### This is for the spice .plt file###
        Plot "xtalk3_spectre" (time()  v(A1) v(A2) v(A3) v(A4) v(A5) v(A150) v(B1)
v(B2) v(B3) v(B4) i(B3 0))

   }

Solve{
   Coupled (iterations=100) {Circuit}
   Coupled (iterations=100) {Poisson}
   Coupled (iterations=100) {Poisson Circuit}
   Coupled (iterations=100) {Poisson Circuit Contact}
   Coupled (iterations=100) {Poisson Hole Contact Circuit}
   Coupled (iterations=100) {Poisson Electron Hole Contact Circuit}

NewCurrentFile="xtalk_transient"
```

```
Transient (
        InitialTime=0
        FinalTime=1.98e-9
        InitialStep=1e-12
        MaxStep=1.5e-10 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="before" Time=(1.5e-9) NoOverwrite)
    }


Transient (
        InitialTime=1.98e-9
        FinalTime=2.5e-9
        InitialStep=1e-12
        MaxStep=1e-11 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="during" Time=(2e-9;2.05e-9;2.1e-9;2.25e-9;2.5e-9)
NoOverwrite)
    }


Transient (
        InitialTime=2.5e-9
        FinalTime=5e-9
        InitialStep=1e-12
        MaxStep=1.5e-10 Increment=1.2)
    {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
                Plot ( FilePrefix="after" Time=(3e-9;5e-9) NoOverwrite)
    }


}
```

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