GEOMETRIC DEPENDENCE OF THE TOTAL IONIZING DOSE RESPONSE OF FINFETS

By

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To

Sourendra Nath Banerjee, *my grandfather*

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

The advances in the development of microelectronic materials and device architectures in the past few years have ushered in a new era of devices and circuits. While some of these new technologies are still in the developmental stages, many of them are on the way to become mainstream workhorses for the coming few years. With the push to deploying state-of-the-art technologies for military and space applications, the radiation hardness of the emerging technologies is a concern. The properties of the material determine the carrier lifetime, transport and defect dynamics in the ICs and the device geometry and doping strongly affect the radiation-induced trapped charge, lifetime degradation, and leakage components in the devices. There are numerous challenges ahead for the semiconductor industry in its effort to track Moore's Law beyond the 28 nm node. The main challenges in this regime are twofold: (a) minimization of leakage current (subthreshold gate leakage), and (b) reduction in the device-to-device variability to increase yield. FinFETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling. Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing.

While many of the classical threats posed by radiation environments have been diminished by aggressive semiconductor scaling, unknown and potentially worst threats lurk in the deep sub-micron regime. For deployment of these devices in harsh environments, it is important to understand the radiation response of these emerging technologies. The goal of this work is to understand how these devices, such as FinFETs, respond to ionizing radiation and the various factors that affect the radiation response of these devices.

Chapter II of this work discusses the inherent problems associated with technology scaling and short channel effects as a limiting factor to scaling. It talks briefly on Silicon-on-Insulator (SOI) as an alternative technology and goes on to introduce the concepts and evolution of multigate transistors as a workhorse for the 22 nm technology node and beyond.

Chapter III gives a brief overview of the various radiation environments, a semiconductor device is exposed to, in space and nuclear reactors. The chapter then focuses on a review of the basic mechanisms of the primary radiation effects in CMOS devices.

Chapter IV reviews the previous work on the effects of ionizing dose in SOI and multigate transistors.

Chapter V details the transistors used in the experiments in this work and the various experimental setup and conditions.

Chapter VI details the charge trapping mechanisms in bulk FinFETs and contrast them with SOI FinFETs.

Chapter VII and VII details the bias dependence and the geometry dependence of bulk and SOI FinFETs. TCAD simulations to understand the difference in the radiation response of these two technologies are elaborated in this section.

Chapter IX proposes a hardening measure to make bulk FinFETs tolerant to dose radiation effects through simulations and Chapter X lists the salient points of the study.

CHAPTER II

THE EVOLUTION OF FINFETS

The reliability of microelectronic devices and circuits is a major factor that determines both their manufacturability and application lifetime. Design for reliability should be implemented during technology, device and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. In this work, the reliability of FinFETs in extreme environments have been studied in detail.

2.1 CMOS Technology Scaling

In 1965, Gordon Moore published his famous paper describing the evolution of the transistor density in integrated circuits. He predicted that the number of transistors per chip would quadruple every three years [Moor-65]. This prediction became known as Moore's law and has been remarkably followed by the semiconductor industry for the last fifty years (Figure 2.1). Since the early 1990s, semiconductor companies and academia have teamed up to predict more precisely the future of the industry. This initiative gave birth to the International Technology Roadmap for Semiconductors (ITRS) organization [ITRS-98]. Every year, the ITRS issues a report that serves as a benchmark for the semiconductor industry. These reports describe the type of technology, design tools, equipment and metrology tools that have to be developed in order to keep pace with the exponential progress of semiconductor devices predicted by Moore's law. Figure 2.1 shows the evolution of the number of transistors per chip predicted by the ITRS 2005 for DRAMs and high-performance microprocessors.

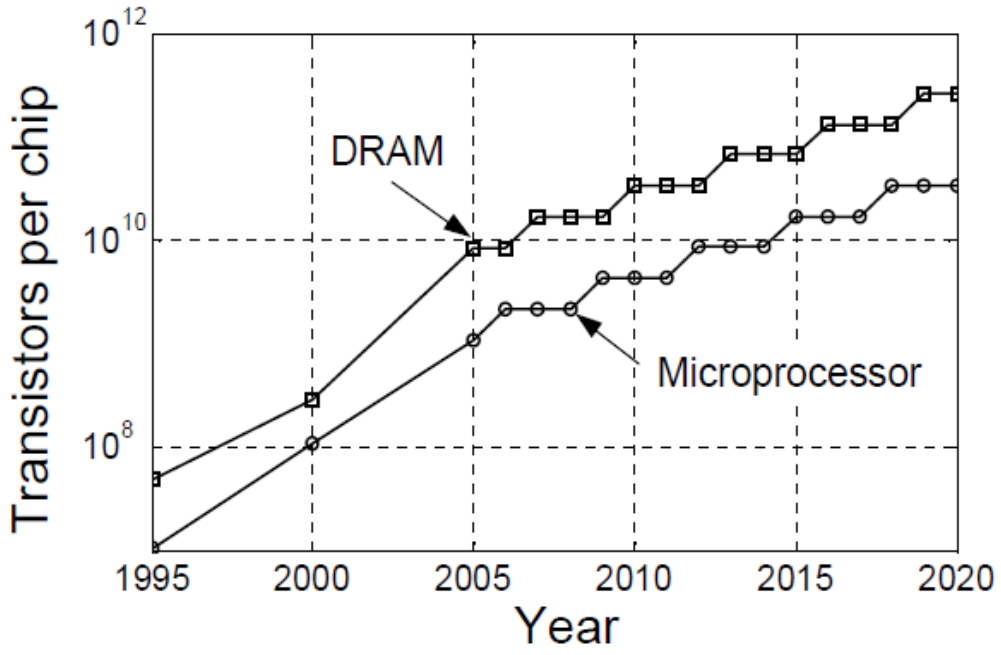


Figure 2.1. Evolution of the number of transistors per chip (Moore's law) predicted by the ITRS 2005 for DRAMs and high-performance microprocessors. (After [Moor-65].)

The semiconductor industry's workhorse technology is silicon CMOS, and the building block of CMOS is the MOS transistor, or MOSFET (MOS field-effect transistor). In order to keep up with the Moore's law, the linear dimensions of transistors have decreased by half every three years. The sub-micron dimension barrier was overcome in the early 1980s, and as of 2014, semiconductor manufacturers are producing transistors with a 22 nm gate length on a regular basis. However, a critical problem that have plagued advanced technology nodes is Short Channel Effects (SCE). A brief review of SCE is presented in the following section.

2.2 Short Channel Effects in CMOS

A MOSFET device is considered to be short when the channel length is of the same order of magnitude as the depletion-layer widths of the source and drain junction [Tsuc-98]. As the channel length is reduced to increase both the operation speed and the number of components per

chip, the so-called short-channel effects arise. The short-channel effects are attributed to two physical phenomena:

1) The limitation imposed on electron drift characteristics in the channel.
2) The modification of the threshold voltage due to the shortening channel length.

Source/drain Charge Sharing: In short channel MOSFETs, parts of the drain and source space charge regions contribute to the substrate depletion region (underneath the gate insulator). Figure 2.2 illustrates the depletion required at the threshold voltage (V_T) and the depletion charge provided by drain/source regions in a planar MOSFET transistor [Mull-03]. The contributions of the source/drain depletion regions to the channel depletion result in reducing the required gate voltage to deplete this region, thereby decreasing the threshold voltage of the transistor.

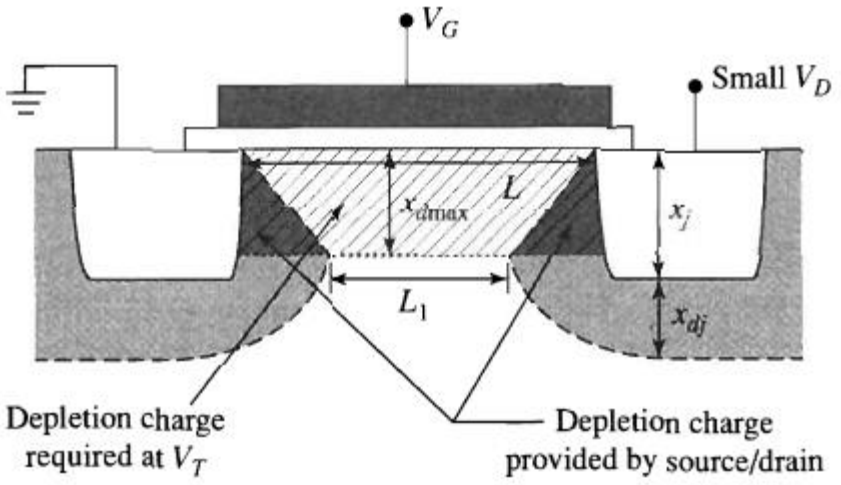


Figure 2.2: Depletion required at the threshold voltage (V_T) in the channel region and the depletion charge provided by drain/source regions in a planar MOSFET. (After [Mull-03].)

Drain-Induced Barrier Lowering (DIBL): Increasing the drain voltage in a short channel MOSFET can significantly modulate the surface potential in the channel region of the transistor.

Indeed, the surface potential increase in the channel lowers the source barrier to electron injection into the channel. DIBL reduces the threshold voltage at high drain biases.

Punch-through: As in the DIBL case, high drain bias lowers the source-substrate barrier in a short channel transistor. However, the punch-through conduction takes place in the silicon bulk. The drain depletion region expands deep in the substrate, where the doping is low, and reaches the source depletion region, creating a parasitic conductive path from the source to the drain.

2.3 Alternate Gate Dielectrics:

The gate insulator thickness is another challenging limit to MOSFET scaling [Fran-01]. Transistors with silicon dioxide (SiO_2) gate insulator of thicknesses lower than 2 nm are being manufactured. It has been reported that devices with gate insulators 2 nm thick exhibit leakage current of ~0.1 A/cm^2 at 1.2 V [Fran-01]. At this thickness, SiO_2 or nitrided SiO_2 gate insulators are only a few monolayers thick [Taur-95], [Buch-99]. According to Dennard's constant field scaling method, the operating voltages should be scaled in conjunction with the device dimensions [Denn-74], [Denn-84]. However, in practice, device operating voltages have scaled less aggressively than the device dimensions. Hence, devices with ultra-thin gate insulators operate at rather large electric fields [Bacc-84]. This raises concerns about the long-term reliability of devices with highly scaled gate insulators. Furthermore, devices with oxides thinner than ~4–5 nm also exhibit large off-state leakage currents (i.e., 1–10 A/cm^2) since carriers are able to tunnel directly between the substrate and gate electrode [Wilk-00], [Wilk-01], [Fran-02]. This a significant concern for space systems and mobile electronics where power conservation is essential. To reconcile the need for reduced off-state leakage currents in highly scaled devices, several high dielectric constant (high-K) alternative gate dielectrics to SiO_2 have been incorporated into ICs [Ribe-05]. Some of the high-K materials that have been integrated into IC

technologies are Al_2O_3, HfO_2, ZrO_2, Y_2O_3, TiO_2, and Ta_2O_5 and/or the silicates and aluminates of some of these materials [Ribe-05]. Each of these materials has its advantages and disadvantages, but none of them are currently at the material quality level of SiO_2. Still, all of these alternative gate dielectrics have a larger dielectric constant than SiO_2. Therefore it is possible to manufacture a gate stack that is physically thicker, yet electrostatically show a capacitance which is similar to an ultra-thin SiO_2 layer. The increased physical thickness significantly reduces the probability of tunneling across the insulator, and therefore reduces the amount of off-state leakage current [Ribe-05], [Guse-01]. However, the use of high-K dielectric alone cannot extend Moore's law beyond 32 nm. However, one approach that takes care of most of these constraining factors is modifying the physical structure of MOSFET transistors from planar to 3D technology.

2.4 SOI as an Alternative

The first integrated circuit transistors were fabricated on "bulk" silicon wafers. At the end of the 1990s, however, it became apparent that significant performance improvement could be gained by switching to a new type of substrate, called Silicon-On-Insulator (SOI) in which transistors are made in a thin silicon layer fabricated on top of a silicon dioxide layer. For SOI technology, a thick buried oxide layer (called BOX), usually SiO_2, is inserted below the active region to prevent parasitic effects experienced in bulk devices, in particular latchup, by isolating the active area from the substrate. Latchup is ruled out because there is no current path to the substrate. The parasitic capacitors between the source and the drain and the substrate are potentially reduced, due to the buried oxide layer, making the device faster [Skot-00, Xion-02]. SOI devices offer the advantage of reduced parasitic capacitances and enhanced current drive [King-05, Bern-03]. In an SOI MOSFET, the thickness of the silicon film determines the physics of the device operation. When the silicon film thickness is less than the maximum depletion

width, the film is completely depleted and the device is considered to be fully depleted (FD). In this case, there is an interaction between the front interface and the back interface, i.e., a coupling effect. In other words, applying a back gate voltage can affect the top-gate electrical characteristics, in particular the front threshold voltage. In the absence of a body contact, i.e., a silicon film contact, SOI devices exhibit floating body effects. These effects can be seen in partially depleted (PD) as well as in FD SOI devices. A major concern is the open-base *n-p-n* bipolar transistor between the drain and source in an *n*-channel SOI device. Among several unwanted parasitic effects, these body effects can be related to the insufficient control of the gate over the body in an SOI device. In this direction, new SOI device architectures such as Ultra-thin BOX (UTB) etc. were brought to light, focusing on increased control of the body region. SOI technology brings about improvements in both circuit speed and power consumption. In the early 2000s major semiconductor companies, including IBM, AMD and ST Microelectronics, began manufacturing microprocessors using SOI substrates on an industrial scale.

The use of SOI as an alternative to bulk, however, remained confined only to specific sectors and applications. The majority of the commercial market use bulk process, championed by companies including Intel, TSMC, UMC and GlobalFoundries. The main challenges scaling the bulk technologies ahead are twofold: (a) minimization of leakage current (subthreshold gate leakage), and (b) reduction in the device-to-device variability to increase yield [Xion-02]. In 2005, ITRS published a document the minimum gate length that can be used with the different technologies (Figure 2.3) [Coli-08]. It showed that the limitations of bulk transistors beyond a gate length of 15-20 nm. FD SOI can be used until 10 nm, but smaller gate lengths can be only achieved by the use of multiple-gate structures.

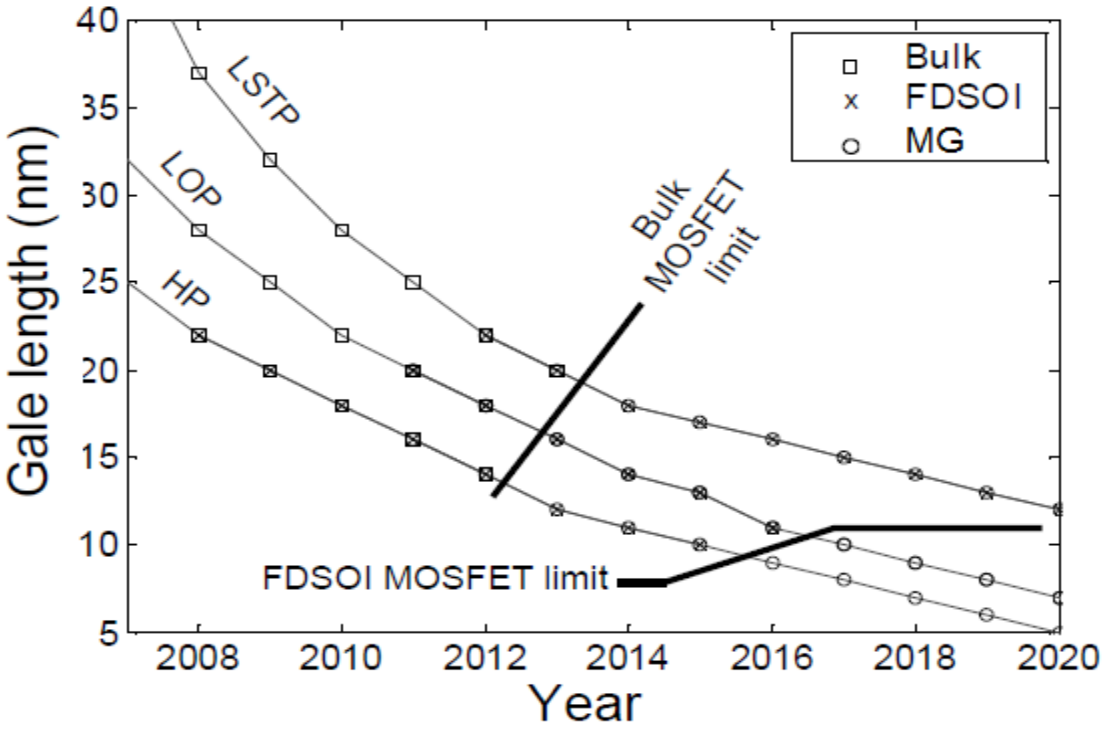
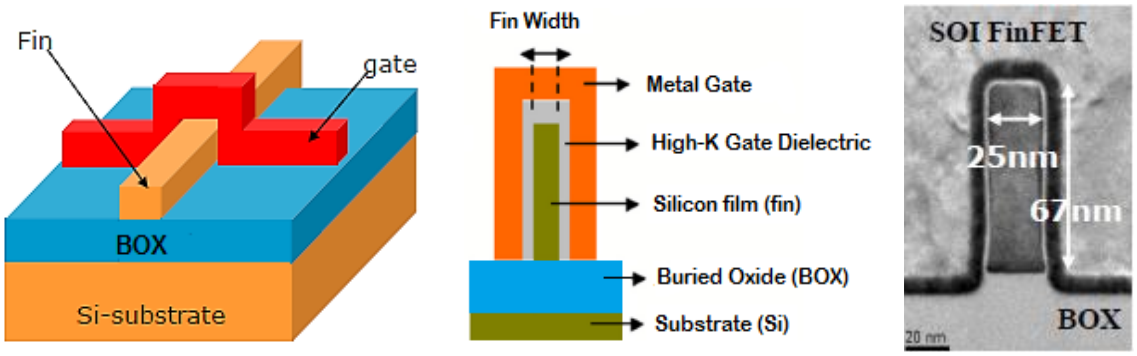


Figure 2.3 Evolution of gate length predicted by the 2005 ITRS for high performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits. (After [Coli-08].)

2.5 Evolution of FinFETs

Historically speaking, double gate transistors date back from the late eighties [Bale-87], [Hisa-91]. Besides the advantage of doubling the drive current by the presence of two inversion layers, additional interest existed in the possibility of volume inversion for thin-film devices, whereby the channel is concentrated in the middle of the silicon film, away from the interfaces, modulated by the front and back gate voltage, as in the case of a four-gate SOI transistor [Coli-90]. While the concept of the double-gate SOI transistor appeared very promising, it was quite challenging to fabricate such devices, considering the difficulties in aligning the top and bottom gates. Early success was achieved by the Gate-All-Around (GAA) transistors [Simo-95]. But the main breakthrough of the double- (or multiple-) gate transistors came in the beginning of the

millennium, with the concept of the FinFET, whereby the planar arrangement was abandoned for a vertical one and the top channel is replaced by two sidewall channels, wrapped around a silicon fin (Figure 2.4) [Hisa-99], [Kedz-01], [Choi-02]. As shown in the figure, a FinFET has its gate stack wrapped around a fin with height H_{fin} and may have two or three active channels, depending on the thickness of the gate dielectric on the top gate. Based on the width of the fins, W_{fin}, the device can be considered as a FinFET, dominated by conduction in the two sidewall channels (narrow fins) or as a planar transistor (wide fins). In the case of narrow-fin transistors, the proximity of the front-gate allows a tight control of the electrostatics in the fin and a reduction of the short channel effects. The influence of the back electrode on the front-gate parameters by coupling can be largely suppressed.

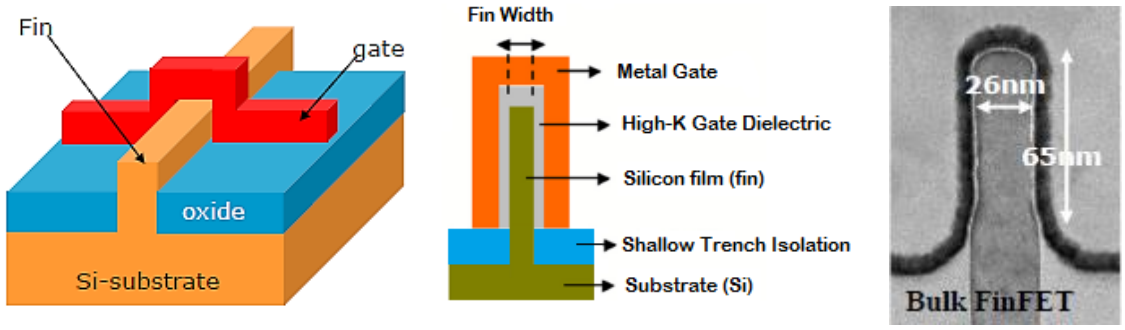


(a) (b) (c)

Figure 2.4: (a) 3D schematic illustration of an SOI FinFET. (b) Schematic cross-section of an SOI FinFET (c) Scanning Electron Microscope (SEM) image of a SOI FinFET. (After [Parv-09].)

More recently, the FinFET concept has been translated to standard bulk Si substrates [Park-03], whereby the fins are now defined by Shallow Trench Isolation (STI) regions, as shown in Figure 2.5. Bulk FinFETs allow fabrication on standard Si substrates without major overhaul of fabrication technologies and the scaling advantages of the FinFET architecture can be combined, resulting in the first adoption of these devices by Intel at the 22 nm CMOS technology node [Jan-12]. Foundries such as TSMC followed suit for the 16 nm technology node [TSMC-13] and

other majors such as Samsung and GlobalFoundries collaborated to produce their 14 nm FinFETs [Sams-14].



(a) (b) (c)

Figure 2.5: (a) 3D schematic illustration of a bulk FinFET. (b) Schematic cross-section of a bulk FinFET (c) Scanning Electron Microscope (SEM) image of a bulk FinFET. (After [Parv-09].)

2.6 Comparison between Bulk & SOI FinFETs

In this section, the primary differences between bulk and SOI FinFETs that affect the transistor response, are evaluated [Hook-13].

2.6.1 Fin Shape

The most important difference in the devices formed in these two manifestations lie in the shape of the fin, the processes that determine the effective fin height, and the presence of doping in the fin, which consequently affects the device in many adverse ways such as the variability and the reliability (mobility degradation and random dopant fluctuation). In a bulk-based process, as the spaces between the lower, electrically inactive portions of the fins must be filled with an insulator, some angling of the fin is required to prevent the formation of voids. Bulk and SOI fin profiles are pictured in Figure 2.6. As tapering the fin compromises the subthreshold slope and degrades the effective drive current as well as the output conductance, minimization of the taper is important to the electrical integrity of the device.

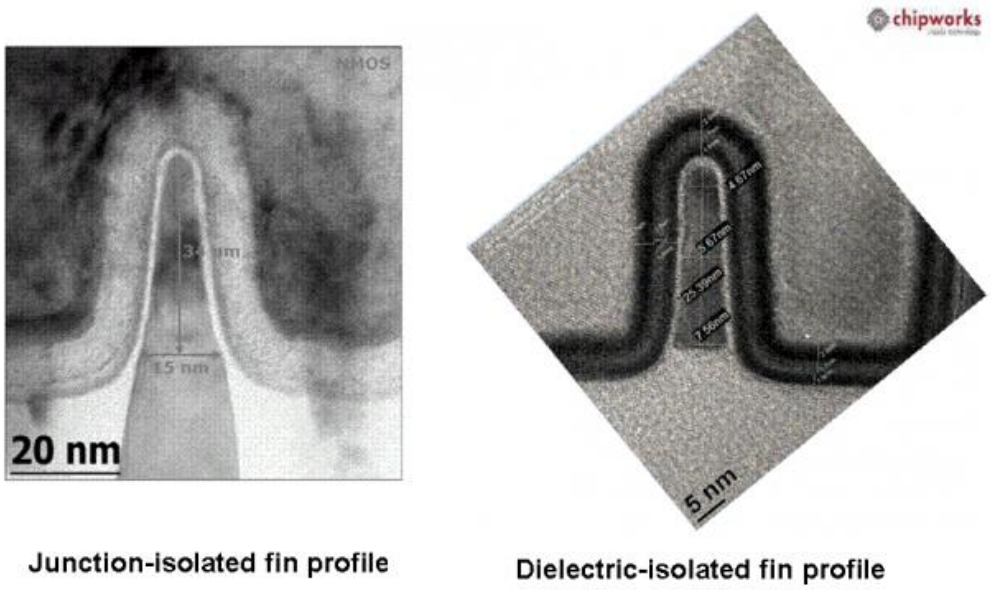


Figure 2.6: Typical bulk junction and dielectric-isolated FinFET fin profiles. (After [Hook-13].)

2.6.2 Doping in the Fin

In an SOI design the transistor-transistor and sub-surface source-drain current paths are inherently disrupted by the dielectric layer, but in a bulk-based process, adequate doping for electrical isolation and latchup immunity needs to be established. This requires additional processing steps and connections for electrical bias. Suppression of punch-through current requires some level of doping at least in the bottom portion of the fin. The adverse effects of doping on mobility and random-dopant-fluctuation have been reported [Kawa-09], [Chia-07]; non-uniform doping is particularly egregious as it increases capacitance without a concomitant increase in drive current [Hook-13]. Another adverse effect of doping in the fin is the implication for the gate work function. For junction-isolated FinFETs, the gate metal work function is established so as to provide the desired threshold voltage in the presence of doping; for undoped dielectric-isolated FinFETs the appropriate work function is closer to midgap, which reduces gate leakage and improves reliability.

2.6.3 Fin Height

Fin height variation has a much more serious impact than the planar analog of transistor width variation. Whereas in the SOI-based version the electrical fin height is determined by the starting silicon thickness, in the bulk-based FinFET process the fin height is determined by several processes, and the distinction between “active” and “inactive” fin is blurred by the conjunction of the gate alignment with the source junction.

The advantages of SOI FinFETs is determined by the choice of isolation. Increased range of operating voltage, process simplification, reduced variation, lower soft error rate, and higher circuit density are all features of a dielectric-isolated architecture. However, commercial foundries have adopted bulk FinFETs over SOI FinFETs because of reduced process costs, better yield and process compatibility with existing bulk planar process.

2.7 FinFETs for Military and Space Applications

As of 2014, radiation-hardened integrated circuits in spacecraft, unmanned vehicles, and wearable devices are being fabricated on 45-nanometer processes, with the promise for even smaller chip geometries in the future for high-reliability electronics [Wils-13]. Space, however, is not the only environment where the military and many civil operations are looking to radiation-harden critical electronics. From precision-guided weapons and the increasingly networked battlespace to electric power grids, financial computers, and GPS position, navigation, and timing (PNT), radiation reliability is a concern. As a result, the demand for rad-hardened electronics has grown from space applications to include any critical system operating in the other three environmental regimes-air, land, and sea. The devices to be protected now include those smartphones and tablets to vehicles (military, commercial, and civil), bank ATMs, the internet, personal and business computers, and hospital equipment.

With the push to deploying state-of-the art technologies for space systems and avionics, it is important to understand the long-term radiation tolerance of these technologies in extreme environments. The following chapter provides a basic understanding of the harsh environment surrounding the earth and effects of radiation on semiconductor devices and circuits.

CHAPTER III

RADIATION EFFECTS IN MICROELECTRONIC DEVICES

There are numerous system environments that can lead to significant radiation-induced degradation of electronic components, including space environments and the environment associated with high-energy particle accelerators. Radiation effects in semiconductor materials and oxides can be categorized into three main classes: total ionizing dose (TID) effects, displacement damage (DD) and single event effects (SEE). The first two, TID and DD, are cumulative effects; they are related to long term effects and more or less uniform throughout the target material. SEE is a transient effect with a short time response and it depends on the position of the ion strike. This work focuses on the total ionizing dose effects in advanced technology nodes. The following section discusses the various radiation environments and the basic mechanisms of radiation effects in electronic devices.

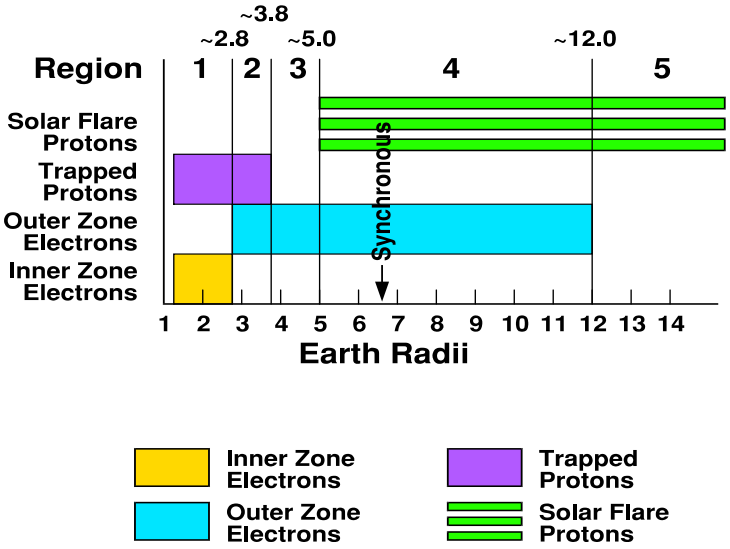
3.1 Radiation Environments

3.1.1 Space Environment

The space radiation environment consists of variety of energetic particles with energies varying from keV to GeV and beyond. There are three main categories of these particles.

1. Trapped particles: This consists of a broad spectrum of energetic particles that are trapped by the earth's magnetic field, called the Van Allen Belts. It is divided into two belts: an inner belt extending to 2.5 times earth radii and comprising of energetic protons up to 600 MeV together with electrons up to several MeV, and an outer belt comprising of mainly electrons extending to 10 times earth radii.

2. Galactic cosmic rays: This consists of low fluxes of energetic charge particle that originate outside of our solar system. These cosmic rays comprise of 85% protons (hydrogen nuclei), 14% alpha particles (helium nuclei) and 1% heavy ions with energies extending up to 1 GeV.



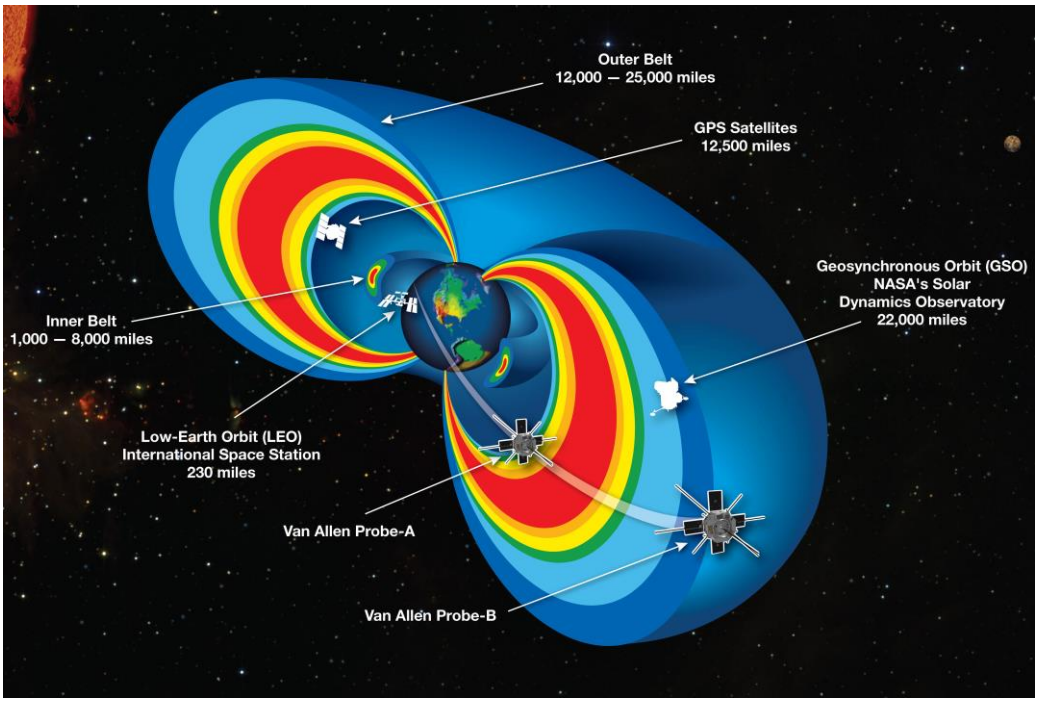


Figure 3.1: The earth's radiation belts. 1 Earth Radius = 6380 km. Geosynchronous orbit at 35,800 km, Outer zone electrons have higher fluxes (~10 times) and energies than inner zone electrons. Maximum energy of trapped electrons is ~ 7 MeV. (After [Stass-88].)

3. Solar particle events: This consists of sporadic bursts of radiation emitted by the sun, mainly protons and heavy ions. Energies typically range up to several hundred MeV to GeV.

The low energy particles are stopped by the layer of shielding material that is used to protect the IC. For a typical shielding depth of 1 to 5 mm, photons with energy above 20 keV, electrons above 1 MeV and protons above 10 MeV can penetrate into the semiconductor.

3.1.2 Nuclear Facilities

In the nuclear facilities, the radiation-tolerant electronics are mainly used for diagnostics or remote handling. The diagnostic systems consist of a combination of measurements that are needed to control, evaluate and optimize the involved processes. In several nuclear environments, the presence of people in certain locations can be tolerated only for a very short time. In many cases, remote operation of machines is a possible solution. This remote handling and also the diagnostic system are already used in most existing nuclear facilities, and they will be even more important in future nuclear installations.

The typical radiation environment of a pressurized water reactor is shown in Table 1 [Holm-93]. The most important environment for equipment and components is 'in containment'. While the gamma and neutron dose rates are moderate, the accumulated dose for an operating lifetime of 40 years is significant. The equipment must also be able to operate during and after a radioactive accident.

3.2 Interaction of Ionizing Radiation with Semiconductor Material

Ionizing radiation possesses enough energy to break atomic bonds and create electron/hole pairs in the materials of interest, which in the case of MOS devices are primarily silicon dioxide and silicon [Curt-74]. The radiation may be in the form of photons with energies greater than the

TABLE 3.1

RADIATION ENVIRONMENT OF A PRESSURIZED WATER REACTOR

In core		In containment	
Neutrons [n· cm^{-2}· s^{-1}]	Gamma [Gy·s^{-1}]	Normal [kGy]	Accident [kGy]
$10^{12} - 10^{14}$(thermal) $10^{10} - 10^{14}$(fast)	$10^{3} - 10^{9}$	500 (40 years)	1500

bandgap of the material of concern (1.1 eV in case of silicon; 9 eV for silicon dioxide), or in the form of particles, such as electrons, protons, or atomic ions. As long as energies of the generated electrons and holes are greater than the minimal energy required for an electron-hole pair generation, they can in turn generate supplementary pairs. As a result, one sufficiently energetic single incident particle can create thousands or millions of electron-hole pairs [Boes-76], [Amus-75]. The total amount of energy deposited by a particle that results in electron-hole pair production is commonly referred to as total ionizing dose (TID). The typical unit of TID that is used is rad(Si) or rad(SiO_2), which denotes the energy absorbed per unit mass of the material. 1 rad(SiO_2) denotes 100 ergs absorbed per gram of SiO_2. The basic degradation mechanisms of ionizing radiation on MOS devices are presented below.

3.3 Single Event Effects in MOS Devices

Single Event Effects (SEE) in microelectronics are caused when highly energetic particles present in the natural space environment (e.g., protons, neutrons, alpha particles, or other heavy ions) strike *sensitive* regions of a microelectronic circuit. Depending on several factors, the particle strike may cause no observable effect, a transient disruption of circuit operation, a change of logic state, or even permanent damage to the device or integrated circuit (IC) [Dodd-03]. The first type introduces no physical damage, only a loss of information, and may be correctable. An example of such a soft error is the single event upset (SEU), i.e. the corruption of

a single bit in a memory array. Hard errors cause permanent damage. For example, when a high-energy particle deposits its energy in a small region of the dielectric, it can lead to single event gate rupture (SEGR), resulting in a catastrophic gate insulator breakdown [Sext-97]. Ion strike may trigger a high-current condition that could result in a permanent failure, depending on the intervention of protection systems. An example from this category is single event latchup (SEL). This is the activation of the parasitic bipolar structure in a CMOS transistor that can trigger high-current conditions [Brug-96]. Heavy ions with high LET can also create microdose effects, similar to total ionizing dose effects [Swif-94].

3.4 Displacement Damage

Displacement damage arises when irradiation causes a displacement of atoms in the lattice of the target material. It is generated by energetic particles like neutrons, protons, electrons and heavy ions [Dale-91]. Photons can indirectly give rise to displacement damage due to their secondary electrons. The probability of such displacements increases with the increase in the mass and energy of the impinging particle [Hopk-96]. When a particle knocks an atom from its lattice position, it leaves an empty position (vacancy). The displaced atom can stop in a non-lattice position (interstitial). These two point defects can either disappear by recombination or give rise to more stable secondary defects by getting trapped by impurity atoms [Hopk-96], [Mars-90]. These radiation-induced defects in the semiconductor lattice can give rise to energy levels in the forbidden gap which gives rise to various degradation in the devices. When the energy level of the radiation-induced defects is close to midgap, generation or recombination of electron-hole pairs (EHP) is dominant. Generation of EHPs can result in an increase of leakage current, while recombination can lead to the decrease of the carrier lifetime [Srou-88]. When the energy level of the defect is shallower, they will give rise to the temporary trapping of carriers. And finally,

radiation-induced defects can lead to the compensation of donors or acceptors or the defect-assisted tunneling of carriers [Srou-88].

3.5 Total Dose Effects on MOS Devices

3.5.1 The Physics behind Total Ionizing Dose in MOS devices

A MOS device exposed to ionizing radiation typically suffers degradation in one or more of its performance parameters. MOS transistors experience a shift in threshold voltage, a decrease in mobility of charge carriers, and higher junction leakage. The damage responsible for these total dose effects occurs in the insulator layers of the circuit structures. The radiation damage in the oxide layers consists of two components (Figure 3.2):

1) The build-up of trapped charge in the oxide.
2) An increase in the number of interface traps.

Electron and holes are created within the silicon dioxide by the ionizing radiation or may be injected into the SiO_2 by internal photoemission from the contacts. These carriers can recombine within the oxide or transport through the oxide. The fraction of holes and electron which escape the initial recombination is defined as *charge yield* [Ma-89]. The charge yield is a function of applied electric field for irradiated MOS devices with SiO_2 gate dielectrics as shown in Figure 3.3. Electrons are very mobile in SiO_2 and quickly move to the contacts; in contrast, the holes have a very low effective mobility and transport via a complicated stochastic trap-hopping process. “Stochastic” transport involves hole motion via polaron hopping between localized sites randomly distributed in the SiO_2. When the holes arrive at the SiO_2/Si interface a certain percentage are trapped. This percentage strongly depends on processing. In commercial oxides, it

can be greater than 50 percent, while for oxides that receive special processing to decrease their sensitivity to radiation it can be a few percent or lower.

Most holes are trapped within 7.5 nm of the SiO_2/Si interface and generally anneal with time. The most widely used model for predicting hole anneal is the first-order tunnelling model of

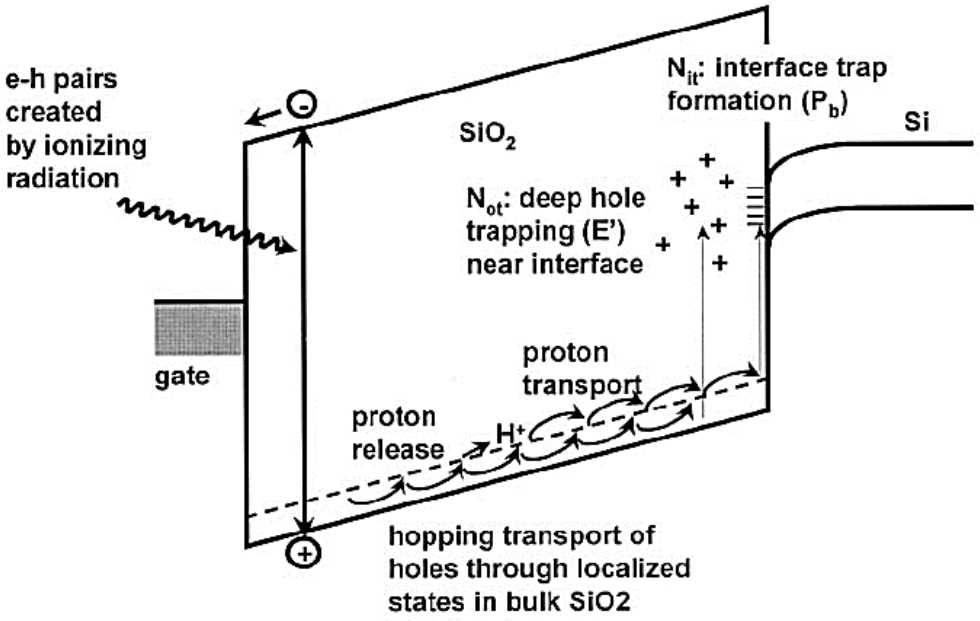


Figure 3.2. Band diagram illustrating the physical processes governing the response of MOS devices to total-dose ionizing radiation. (After [McLe-87].)

McLean [McLe-76]. This model assumes that the dominant charge loss mechanism for irradiated MOS devices is recombination between trapped holes and electrons that tunnel from the silicon substrate. Holes trapped within the first 3 nm recombine in the first minute with electrons that tunnel from the Si [Boes-76]. The model accounts for many features of experimentally observed hole anneal, including electric field effects. In 1990, McWhorter *et al*. [McWh-90] developed a new model for predicting hole anneal that, in addition to tunneling, includes a thermal emission charge loss mechanism. The thermal emission model assumes the anneal of radiation trapped holes results from the thermal emission of holes from traps in the oxide to the valence band of the oxide. This combined tunneling/thermal emission model is consistent with a wide range of

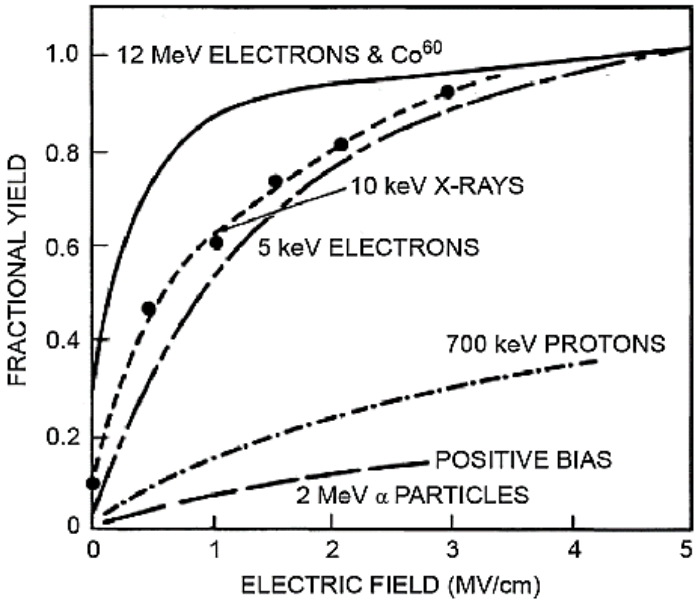


Figure 3.3. Charge yield as a function of applied electric field for irradiated MOS devices with SiO_2 gate dielectrics. (After [Oldham-83].)

experimental data in the literature which examines the effect of temperature, as well as electric field, on hole anneal [Schw-84], [Leli-89], [SimoM-71], [SimoM-72], [Derb-77]. Both tunneling and thermal emission models are also consistent with a wide body of experimental data that suggests the anneal of holes proceeds as a logarithmic function of the anneal time [Buck-80], [Wino-81], [Habi-73], [Bruc-81]. The thickness dependence of radiation-induced charge trapping was investigated by Saks with Co-60 gamma rays [Saks-84] and by Benedetto *et al*. with 12-MeV electrons [Bene-85]. In each case, a strong decrease in radiation-induced hole trapping is observed at 80 K as the gate insulator thickness decreases. For thicknesses below ~10 nm, the decrease in hole trapping is much more rapid than expected from the established $\sim t_{ox}^2$ dependence for thicker oxides [Boes-76]. This is attributed to the removal of trapped holes located within 3 nm of either the gate SiO_2 or Si-SiO_2 interface via tunneling. Because tunneling processes vary quite slowly with temperature, these results show that ultra-thin MOS gate

insulators are nearly immune to failure as a result of radiation-induced hole trapping at any temperature.

Along with the electron-hole generation process, chemical bonds in the SiO_2 structure may be broken. Some of these bonds may reform when the electrons and holes recombine, whereas others may remain broken and give rise to electrically active defects. These defects can serve as trap sites for carriers or as interface traps. Bonds associated with hydrogen or hydroxyl groups when broken can release a proton (H^+) which are then mobile within the silicon dioxide. These protons may then migrate to the SiO_2/Si interface, where they undergo a reaction which results in an interface trap. The defects created by the radiation may themselves migrate in the strained region near the SiO_2/Si interface and also result in the formation of an interface trap [Wino-89], [Oldh-89], [Lai-83], [Shan-90].

Typically, the net charge trapped in the oxide layer after irradiation is positive. Radiation-generated interface traps can have either a positive or negative charge depending on whether they are donor or acceptor states, and their charge occupancy depends on the applied bias or band bending at the SiO_2/Si interface. Specifically, a donor trap level is in a neutral charge state when it is below the Fermi level, and becomes positive by donating (giving up) an electron when it moves above the Fermi level. An acceptor trap level is in a neutral charge state when it is above the Fermi level, and becomes negative by accepting an electron when it moves below the Fermi level. When a voltage is applied to the gate of a MOS device, the interface trap levels move up or down (along with the valence and conduction bands) relative to the Fermi level. The charge state of the interface trap changes when it crosses the Fermi level. Under all conditions, the interface trap is in its more positive charge state when it is above the Fermi level [McLe-80], [Gris-85].

The interface traps can exchange charge freely with the silicon substrate, and thus their charge state depends upon the bias applied to the device – more negative for a positive bias applied to the gate electrode than for a negative bias applied to the gate electrode. As the total dose to the device increases, the amount of oxide-trapped charge and number of interface traps monotonically increase. The radiation hardness of a device is determined by the rate at which these two damage measures build up as the cumulative dose increases. Interface traps are present at the oxide-semiconductor interface and can communicate with the semiconductor. They can trap both electrons and holes. Interface traps have been associated with P_b centers, which are trivalent Si defects at the Si/SiO_2 interface [Lena-84]. Interface traps build up slowly following radiation. Radiation-induced oxide-trapped charge has been associated with E' centers, which are trivalent Si defects in SiO_2 [Lena-84]. Border traps are near-interfacial oxide traps that communicate with the Si [Flee-92]. Only studies of defect microstructure, e.g., via electron-spin-resonance, in combination with measurements of the electrical response, allow clear discrimination between interface traps and border traps. MOS capacitors provide a good way to determine the effective border trap density from hysteresis between forward and reverse sweep of MOS *C-V* characteristics [Flee-96].

3.5.2 Effect of Total Dose Radiation on MOS Devices and Circuits

3.5.2.1 MOS Capacitors

In MOS capacitors, the oxide-trapped charge shifts the *C-V* curve in the negative direction. The interface traps tend to "stretch out" the *C-V* curve, so that a greater change in applied bias voltage is required to cause the same change in capacitance as before the irradiation (Figure 3.4). [Wino-84], [Boes-78].

3.5.2.2 MOS Transistors

Similar effects occur in MOS transistors. The basic radiation problem in a MOS transistor is illustrated in Figure 3.5, where Figure 3.5(a) shows the normal operation of a MOSFET. The application of an appropriate gate voltage causes a conducting channel to form between the

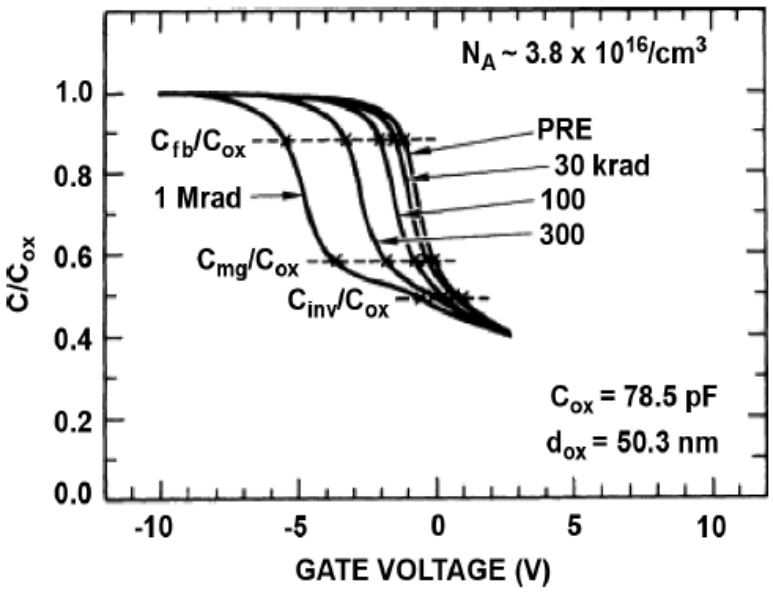


Figure 3.4: Normalized high-frequency capacitance-voltage curves for a *p*-substrate MOS capacitor with a polycrystalline Si gate irradiated to 1.0 Mrad(SiO_2) with Co-60 gamma rays at a dose rate of 240 rad(SiO_2)/s and an oxide electric field of 2 MV/cm. (After [Wino-84].)

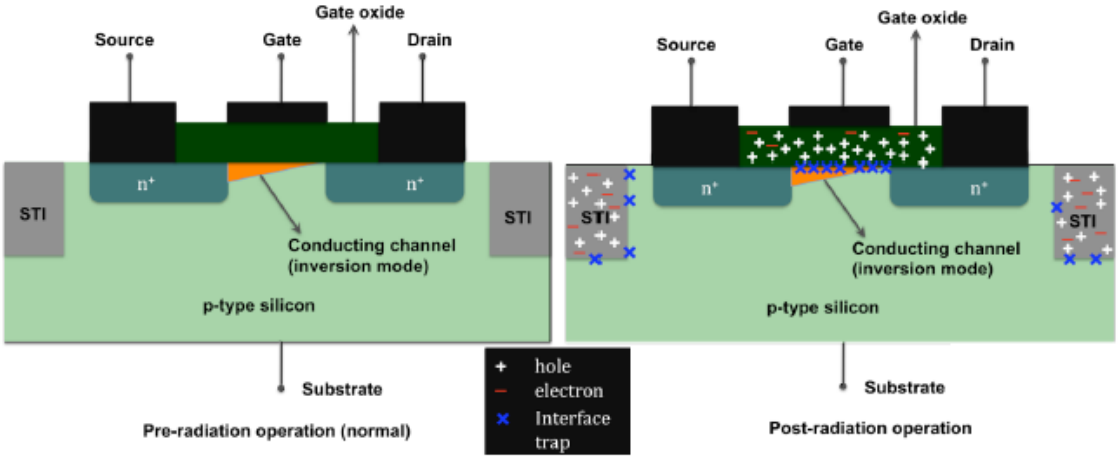


Figure 3.5. Schematic diagrams of *n*-channel MOSFETs illustrating radiation-induced charging of the gate oxide: a) normal operation and b) post-irradiation operation.

source and the drain so that current flows when the device is turned on. In Figure 3.5(b), the effect of ionizing radiation is illustrated. Radiation-induced trapped charge has built up in the gate insulator, which causes a shift in the threshold voltage. If this shift is large enough, the device cannot be turned off, even at zero volts applied, and the device is said to have failed by going into depletion mode. As discussed in the previous section, the generation of electron-hole pairs in the SiO_2 layer is the primary effect of ionizing radiation on MOS structures. The generated electron-hole pairs can either recombine or transport through the oxide. The electrons being very mobile, move quickly towards the gate contact and exit out of the oxide while a fraction of the less mobile holes eventually become trapped within the oxide region. The electrons and holes that escape the initial recombination process can produce photocurrents and space charge effects in MOS devices and circuits. Ionizing radiation will create both fixed oxide trapped charge and interface traps. The fixed oxide-trapped charge (OT) is net positive and induces a negative shift ΔV_{ot} in the drain current (I_D) versus gate voltage (V_G) characteristic. This is illustrated in Figure 3.6. For *p*MOS devices the threshold voltage (V_T) goes to more negative values while off-state and drive currents are reduced. *n*MOS devices suffer from a decrease in V_T and an increase in off-state and drive currents. In Figure 3.7, the effect of interface traps (IT) on the I_D-V_G characteristics of *p*MOS as well as *n*MOS devices is shown. One of the principal effects of interface charge build-up is the increase of the subthreshold swing (ΔS). The mechanism for this effect is the V_G dependent trapping or de-trapping of charge at the interface [Flee-13]. The change in subthreshold swing ΔS can be used to calculate the density of radiation-induced interface traps ΔN_{it} [Wino-89]:

$$\Delta Nit = \frac{C_{ox}}{k \cdot T \cdot ln(10)} \cdot \Delta S \qquad \text{..... (1)}$$

In this equation C_{ox} is the gate dielectric capacity density, k is the Boltzmann constant and T is the temperature. The interface trap density also results in a decrease of the transconductance and surface mobility [Dent-06].

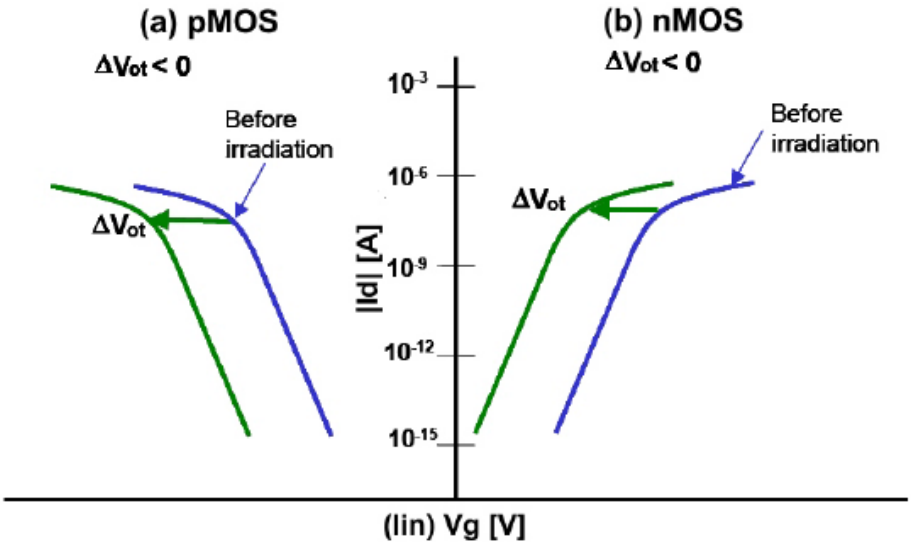


Figure 3.6: Effect of fixed oxide-trapped charge (OT) on the I_D-V_G characteristics of (a) *p*MOS and (b) *n*MOS devices. (After [Barn-05].)

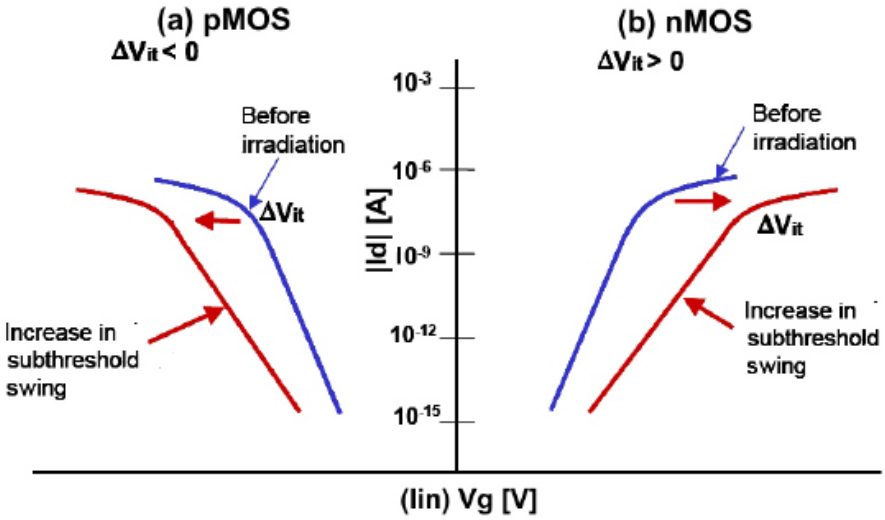


Figure 3.7: Effect of interface traps (IT) on the I_D-V_G characteristics of (a) *p*MOS and (b) *n*MOS devices. (After [Barn-05].)

Effect of Threshold Voltage Shifts on MOS Transistors: The threshold voltage of a MOS capacitor and transistor as a function of total-dose is illustrated in Figure 3.8. The voltage shift is due to trapping of holes in the oxide and the build-up of interface traps [Schw-08]. In general, the effect of radiation-generated charge, $\Delta\rho$, on the threshold voltage shift, $\Delta V_{OT/IT}$, of a transistor is given by:

$$\Delta V_{ot,it} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x dx \qquad \text{..... (2)}$$

where: t_{ox}: thickness of the oxide

C_{ox}: capacitance of the oxide,

x: Distance is measured from the gate of MOS.

Trapped positive charge (holes) in the oxide will cause will cause a negative shift in the threshold voltage of a device and negative charge will cause a positive shift in the threshold voltage. Generally, the initial response of a MOS transistor to radiation is a negative shift in the threshold voltage due to the build-up of trapped holes. The *n*MOS device may turn 'ON" at zero gate bias (no voltage applied to the gate) if a sufficient amount of holes is trapped in the oxide. In this case, the device is said to have gone into "depletion mode" and the device is permanently in the "ON" state. After sometime, the acceptor-like (negatively charged) interface traps can shift the threshold voltage in the positive direction. This is termed as turn-around and can be attributed to negatively charged interface traps building up at a higher rate than trapped oxide charge. If sufficient negative charge is built-up in the interface traps then it is possible for the threshold voltage of *n*MOS device to increase to values more than the pre-irradiation value. This condition is termed as "rebound" [Schw-84] or "super-recovery" [John-84] where most of the trapped holes are annealed leaving primarily the negative charge contribution of the interface traps.

Hence we can say that the threshold voltage shift is time dependant, causing the shift at long times to be opposite to that observed at short times after irradiation. For the case of *p*MOS transistor, both the oxide trapped charge and interface trap charge (donor-like states) are positively charged. Hence the threshold voltage shift is negative and continues to increase in magnitude. The *p*MOS transistor can become permanently turned "OFF" if the magnitude of the threshold voltage increases more than the power supply voltage.

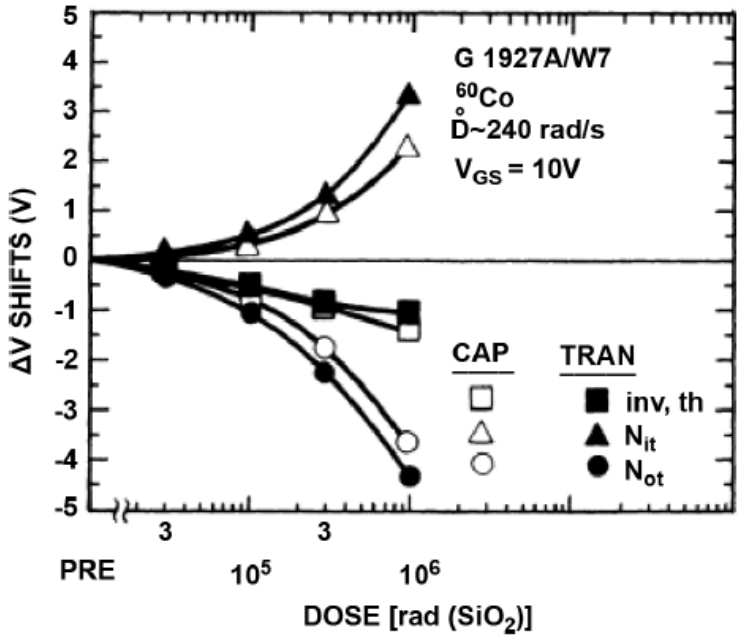


Figure 3.8. Threshold voltage shifts due to interface- and oxide-trap charge for MOS capacitors and transistors. These estimates assume that interface traps are approximately charge neutral at midgap surface potential. (After [Wino-84].)

Effects of Threshold Voltage Shifts on ICs: From the above section we can see that the threshold voltage shifts in *n*MOS and *p*MOS transistors can lead to functional failure of the IC when the threshold voltage of the *n*MOS transistor becomes lesser than 0 V and/or the magnitude of threshold voltage of *p*MOS transistor becomes greater than supply voltage. During "rebound" of *n*MOS transistors, the increase of threshold voltage more than the pre-irradiation value causes

the reduction of the drain current or the current drive of the transistor thereby slowing down the IC. “Rebound” has been observed to cause IC failure [Schw-84]. The threshold voltage shifts in PMOS transistors also reduce the current drive and lead to a degradation in speed or loss of TTL comparability. Finally, increased off-state transistor leakage will be reflected by an increase in standby power consumption for an IC.

Induced Parasitic Leakage Currents: Transistors are electrically isolated from each other by the use of a field dielectric. Up to the 0.25 μm node, the lateral isolation is based on LOCOS (local oxidation of silicon). Because this isolation structure is no longer scalable and penalizes the control of the transistor width, the field oxide in more recent CMOS technology is replaced by the shallow trench isolation (STI). The fabrication process of the STI is as follows: first a trench is etched in the silicon, then a dielectric is deposited in these trenches with CVD (chemical vapor deposition) and finally the excess dielectric is removed using CMP (chemical-mechanical planarization). As the field isolation is much thicker and of a poorer quality than the gate insulator, it is likely to be more efficient in charge trapping during radiation. There exist two possible leakage paths created by radiation effects in the STI. Inter-device leakage between two adjacent devices is shown in Figure 3.9. It will result in a lack of device isolation. Edge leakage along the sidewalls of a single device is illustrated in Figure 3.10. Edge leakage can lead to an increase of the drain current in the off-state as is illustrated in Figure 3.11. This happens when the parasitic edge transistor suffers from a threshold voltage shift large enough that it becomes conductive in the off state. In *p*MOS devices edge leakage is no problem as the effect of the oxide-trapped charge as well as the interface traps is to shift an already negative threshold voltage further away in the negative direction [Facc-05], [Laco-03].

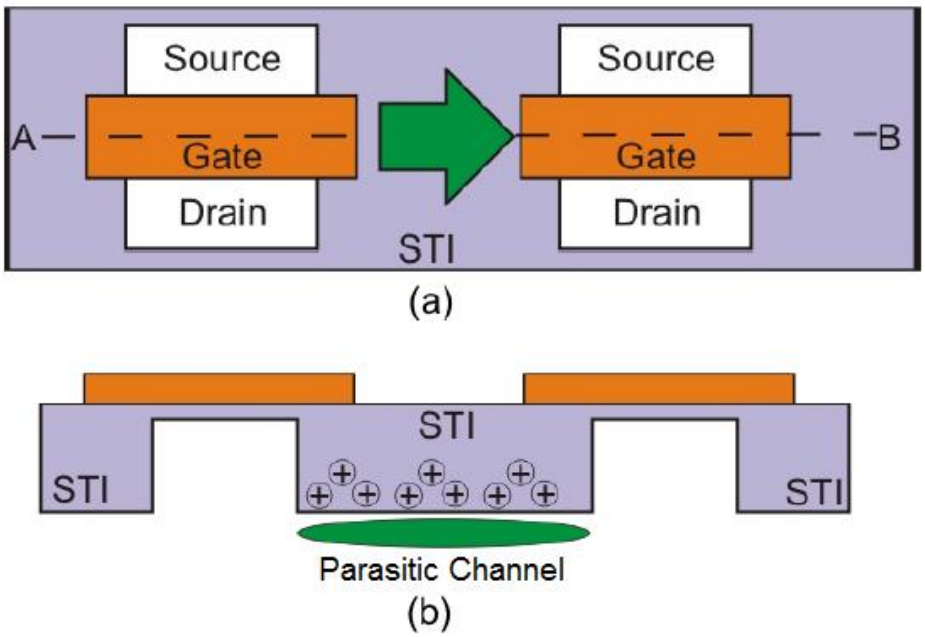


Figure 3.9: Inter-device leakage illustrated in the top view of (a) two transistors and (b) the same transistors viewed along the A-B cutline. (After [Barn-05].)

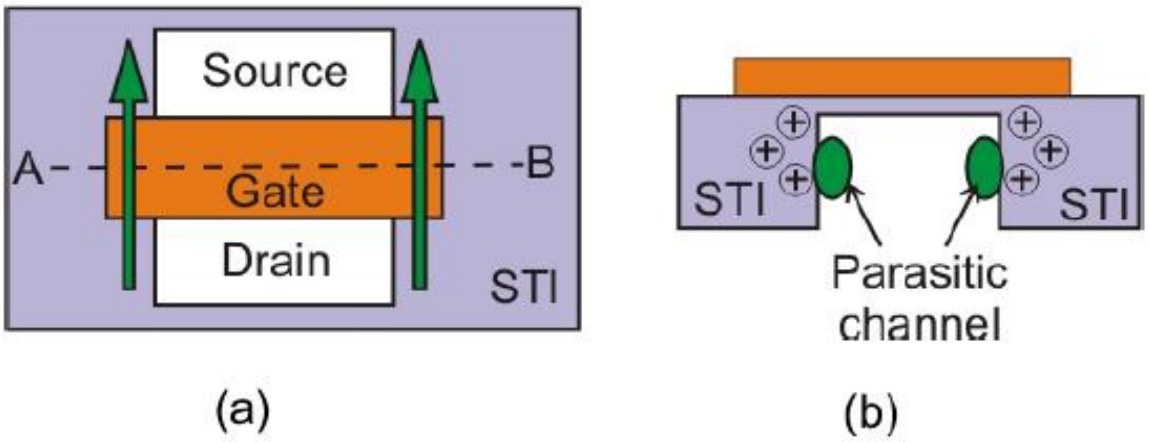


Figure 3.10: (a) Edge leakage illustrated in the top view of a transistor and (b) the same transistor viewed through the A-B cross-section. (After [Barn-05].)

Mobility Degradation: A very important effect of the build-up of interface traps is mobility degradation. Initial work [Stan-67], [Gaw-74] suggested that reductions in mobility were due to increased lattice and Coulomb scattering by charged interface traps, and that the average surface

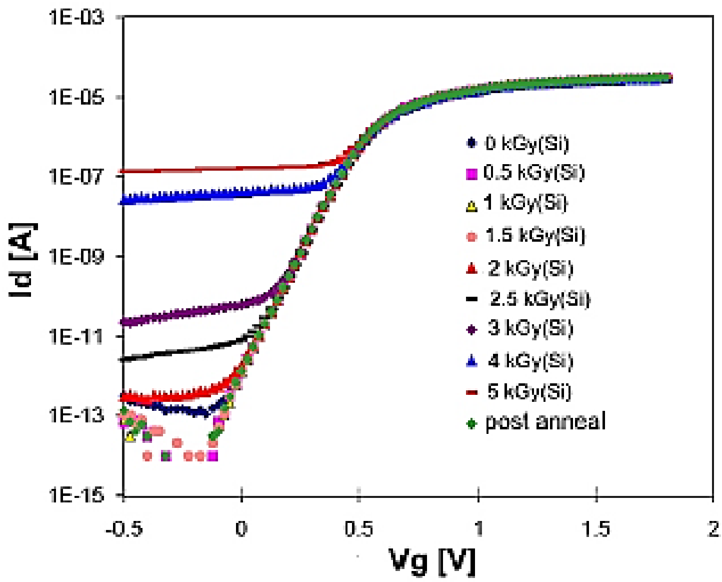


Figure 3.11: Drain current I_D versus gate voltage V_G as a function of total dose, showing an increase in off-state current due to radiation-induced edge leakage. (After [Laco-03].)

mobility was proportional to $1/N_{it}$, where N_{it} (cm^{-2}) is the areal density of interface traps. Following the earlier work of Sun *et al.* [Sun-80] and Galloway *et al.* [Gall-84], [Gall-85], Sexton *et al.* [Sext-85] showed that mobility degradation can be fitted (over a wide range of experimental conditions) by the empirical relationship:

$$\mu = \mu_o/(1 + \alpha(\Delta N_{it})) \quad \text{……………………………………..} \ (3)$$

where μ_o is the pre-irradiation value of mobility and $\alpha = (8 \pm 2) \times 10^{-13}$ cm^2. The data of Sexton *et al.* [Sext-85], showing mobility degradation following irradiations of *n*- and *p*-channel transistors under all bias conditions, is plotted in Figure 3.12. Galloway *et al.* [Gall-84], [Gall-85] have used this relationship between mobility and interface traps as a basis for a simple model to separate the effects of oxide-trapped and interface-trap charge on MOSFET *I-V* characteristics. From first principles, radiation-induced decreases in mobility lead to reductions in subthreshold slope, g_m, transistor drive, circuit speed, etc.

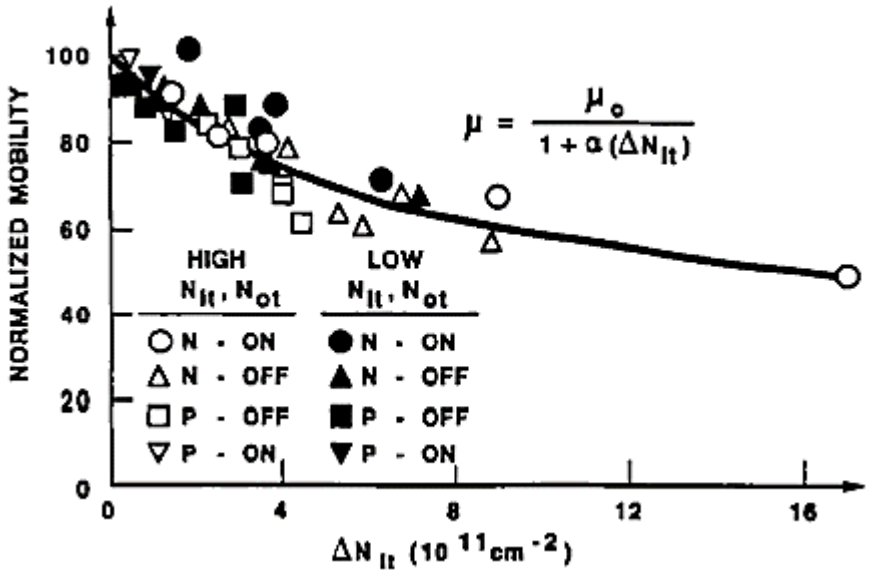


Figure 3.12. Normalized effective channel mobility plotted as a function of interface-trap density. (After [Sext-85].)

3.6 Summary

This chapter provided a summary of the key concepts on the effects of total-ionizing dose effects in semiconductor materials. It also gives an overview of the degradation of conventional CMOS technologies due to ionizing radiation. The mechanisms described in this chapter will also be applicable in the radiation response of the more state-of-the-art devices described in the following chapters.

CHAPTER IV

RADIATION EFFECTS IN ADVANCED SOI AND MULTIPLE GATE TRANSISTORS

The introduction of new materials into highly scaled CMOS technologies presents challenges from a TID perspective that once were thought solved by the scaling down of MOS gate insulator thickness. The ever-shrinking dimensions of MOS transistors makes each interaction of a high-energy particle with a device or IC less of a collection of nominally equivalent phenomena that can be characterized completely via simple accounting for the numbers of electron–hole pairs, and more of a "single event" that must be understood in greater detail [Flee-13]. The aim of this chapter is to describe in a comprehensive manner the current understanding of the radiation response of SOI and FinFET technologies.

4.1 Overview of TID Effects in SOI Architectures

TID effects in Fully Depleted (FD) SOI architectures have been studied since the 1990s by several workers [Ferl-97], [Ferl-00], [Jenk-94], [Schw-00]. They all highlight the particular case of fully depleted SOI devices for which electrostatic coupling effects between the gate insulator, silicon and the silicon-BOX interfaces play an important role in their ionizing radiation response. Any modification of the electrostatic potential occurring at the silicon-BOX interface will influence the potential at the front gate interface [Lima-83]. Radiation-induced charges trapped in the BOX can thus efficiently modify the electrostatic potential at the silicon-BOX interface and then at the silicon-gate insulator interface due to coupling effects. Degradation in threshold voltage and the subthreshold slope of the transistor are observed [Ferl-97], [Jenk-94], [Maye-90]. Furthermore, more complex mechanisms may also be triggered, such as total dose latch

phenomena, due to floating body effects inherent to the SOI architecture [Brad-92], [Brad-96], [Ferl-98], [Pail-05]. Radiation effects in FD SOI devices are thus strongly dependent on the BOX type and thickness. Several studies have been conducted to investigate the trapping properties of such dielectrics [Pail-95] in order to estimate the hardness potential of each type of material. More recently, it was demonstrated that thinning the BOX after removing the substrate yielded enhanced tolerance to TID [Gouk-03]. However, thinning the BOX down to a few nanometers may not improve the TID tolerance of FD SOI devices at each time [Gail-13]. This is pointed out in nanometer scaled technologies where the balance between the amount of radiation- induced trapped charges into the BOX and their relative weight determined by coupling effects should be taken into account to understand their TID sensitivity [Gail-13].

4.2 Overview of TID Effects in Multigate Architectures

The first papers related to total ionizing dose experiments on multi-gate devices were the works of Lawrence *et al*. in 1991 [Lawr-91], Colinge *et al.* in 1993 [Coli-93], Francis *et al.* in 1994.[Franc-94] and E. Simoen *et al*. in 1995 [Simo-95]. Their seminal work highlighted the promising potential of multiple-gate devices to withstand high TID. In early 2000s, several studies were conducted on FinFETs processed on SOI substrates. This section will provide a brief overview of total ionizing dose effects in multigate transistors.

Charge trapping in the BOX of planar FD SOI devices can affect the main transistor through direct coupling effects between the front and back interface [Schw-03], [Jenk-94], [Lim-83], [Ferl-98], [Gail-13], [Song-13]. However, coupling effects differ in multiple-gate devices such as FinFETs. A horizontal coupling induced by lateral gates appears in addition to the standard vertical coupling of single-gate FD SOI transistors. The geometry of the active silicon finger influences the coupling behavior [Daug-04], [Ritz-06]; horizontal coupling effects vary

substantially with the lateral gate spacing. i.e., the fin width. Figure 4.1 shows the location of the trapped charge and the back-gate transistor in SOI FinFETs and Figure 4.2 shows the I_D-V_G characteristics of a wide and a narrow multiple-gate transistor are displayed both before and after a 500 krad(SiO_2) exposure.

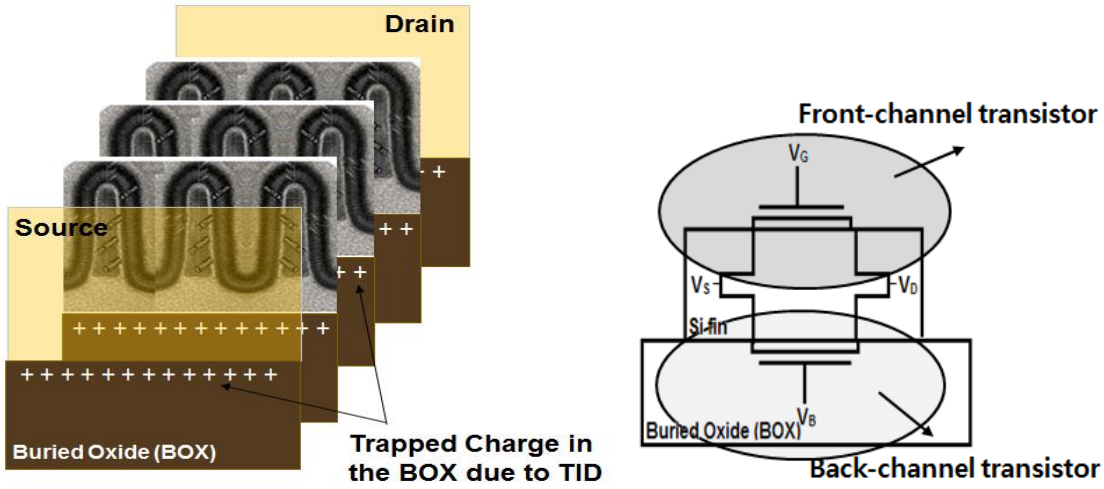


Figure 4.1. Schematic diagram showing the trapped charges in the isolation oxide in a multi-fin SOI FET. (After [Chat-14] and [Chip-12].)

The wide multiple-gate transistor behaves as a conventional FD SOI single-gate transistor since the lateral gates have little impact on the electrostatic potential in the active silicon layer contrary to the one of the top gate. Positive trapped charges in the BOX then act as a back-gate bias as already observed in planar FD SOI transistors [Schw-00], [Ferl-98], [Gouk-03] leading to a significant degradation of the electrical characteristics. On the contrary, the narrow fin transistor shows no measurable voltage deviation with TID [Gail-06], [Gail-06(2)], [Mamo-10], [Coli-06]. The threshold voltage shift after a cumulative dose of 500 krad(SiO_2) stays within measurement uncertainties. It is worth noting that this behavior is almost the same irrespective of the gate length under consideration [Gail-06]. The proximity of the lateral gates in narrow fin transistors screens the vertical coupling effect between the front and the back interfaces.

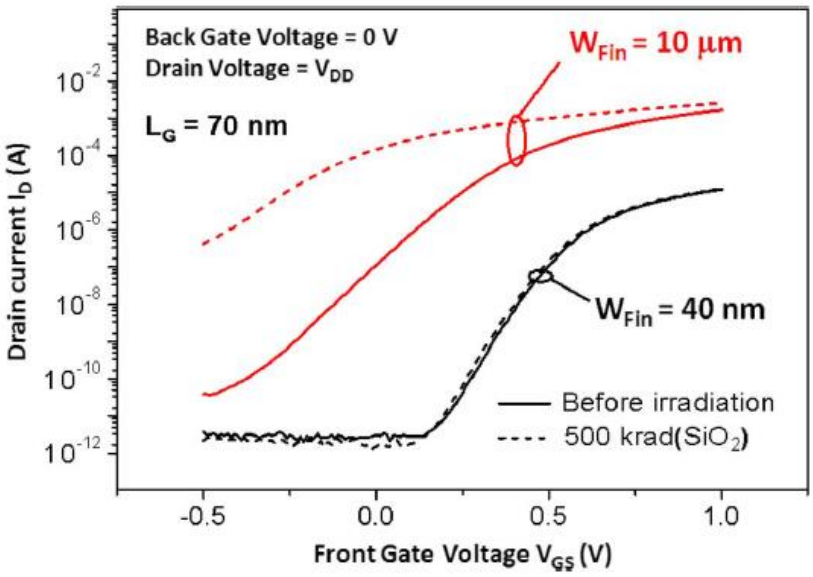


Figure 4.2. Drain current vs gate voltage curve of multiple-gate FETs processed with an Ω-shaped gate with various fin widths: W_{fin} = 40 nm and 10 µm and both before irradiation and after 500 krad(SiO_2). The drawn gate length is 70 nm. The bias condition during irradiation was the OFF state. (After [Gail-06].)

Figure 4.3 highlights the progressive control taken by the lateral gates over the electrostatic potential in the silicon fin with decreasing fin width. Multiple-gate devices with a wide fin (W_{fin} = 10 µm) show threshold voltage shifts which are close to those extracted on a planar single-gate FD SOI transistor with the same geometry and OFF-state irradiation bias.

4.3 Summary

The total dose degradation of the SOI FinFET technologies studied is primarily due charge trapped in the buried oxide. In this way, the back inversion channel is affected. This, in turn, influences the transconductance of the devices at intermediate gate voltage. The TID tolerance of SOI multiple-gate transistors with an optimized geometry is very promising. SOI FinFETs designed with narrow silicon fingers show intrinsic immunity to TID effects This geometry allows lateral gates to naturally mitigate potential parasitic effects induced by TID: the impact of

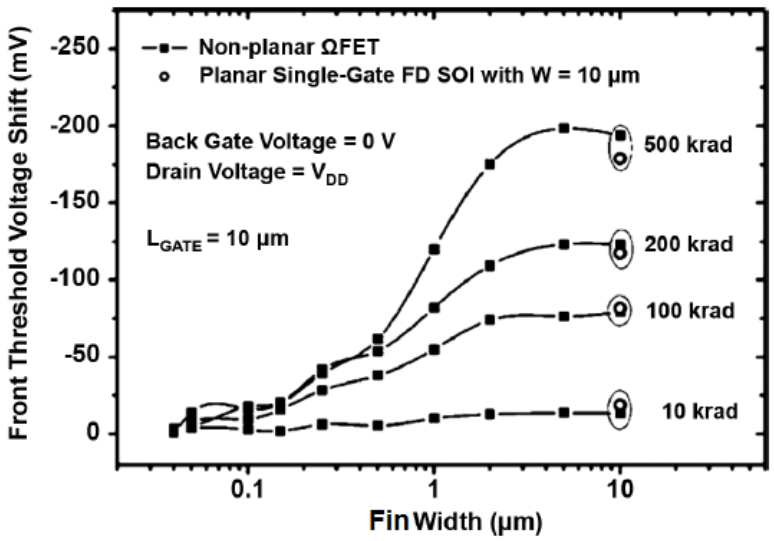


Figure 4.3: Top-gate threshold voltage shift as a function of fin width and dose for the devices of Figure 65, irradiated to 500 krad(SiO_2) with 10-keV X-rays at a dose rate of 100 rad(SiO_2)/s. These devices were irradiated with a drain bias of 0.7 V, with all other pins grounded. (After [Gail-06].)

trapped charges is mostly screened, effects of bias configuration during irradiation are reduced These properties make SOI FinFET a strong candidate for embedded memory applications for nanometer scaled technologies [Zhang-10].

By contrast, only a few studies have been conducted on the TID response of bulk FinFETs. There have been only a couple of work that details on the total ionizing dose response of bulk FinFETs [Put-10], [Put-10(2)]. This work, for the first time, investigates the bias dependence and geometry dependence of total ionizing dose response of bulk FinFETs. The various mechanisms at play are studied using 3D TCAD simulations and finally some process changes are investigated that would enhance the TID tolerance of bulk FinFETs.

CHAPTER V

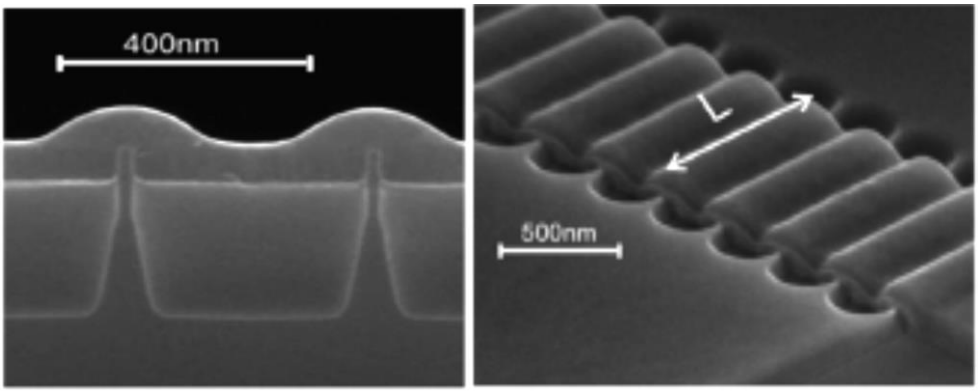
DEVICE AND EXPERIMENTAL DETAILS

Bulk FinFETs have advantages in terms of cost and defect density of the Si substrate, heat transfer and compatibility with conventional planar bulk CMOS devices and have emerged as the technology of choice from 22 nm node onwards [Jan-12], [TSMC-13], [Sams-14]. The radiation hardness of the SOI FinFETs have been discussed in the previous chapter: in general these devices are quite hard in terms of radiation response. However, most of the radiation degradation can be related to effects in the back-channel characteristics, due to radiation-induced charges in the buried oxide. At the same time, it was anticipated that bulk FinFETs could be even harder with respect to total ionizing dose degradation, due to the absence of the buried oxide [Put-10]. In this chapter we present the details of the testing facilities and the measurement techniques, along with the details about the FinFETs used in this work.

5.1 Transistor and Technology Parameters

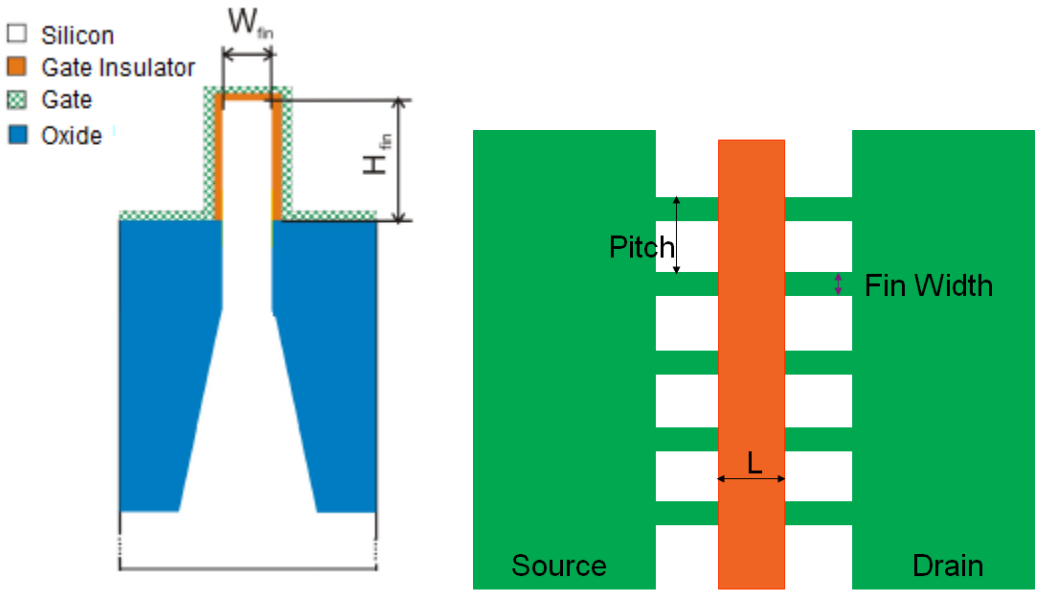
5.1.1 Bulk FinFETs:

The bulk FinFETs under study have been processed on 300 mm Czochralski silicon wafers. A cross-sectional and top view image of a bulk FinFET are shown in Figure 5.1 and a schematic cross-section in Figure 5.2. The gate insulator consists of a 2.6 nm HfSiON-layer, with 40% Hf on a 1 nm interfacial SiO_2 and 100 nm of poly-crystalline silicon on top of a 5 nm TiN metal gate. The equivalent oxide thickness EOT=1.5 nm. The source/drain access region is formed by selective epitaxial growth of Si on the source and drain areas, followed by NiPt silicidation [Put-10(2)]. The *n*MOS transistors used in this study have a nominal V_{DD} of 1.0 V. A selective



(a) Cross-sectional SEM (b) Top-view SEM

Fig. 5.1: Cross-sectional (a) and top-view (b) SEM image of a bulk *n*-channel FinFET (After [Put-10(2)].)



(a) Cross-section (b) Top-view

Fig. 5.2: Schematic cross-section (not to scale) of a bulk *n*-channel FinFET. Definition of fin height, fin-width, channel length and pitch in the FinFETs. (After [Put-10(2)].)

epitaxial growth (SEG) of the source/drain regions is used to reduce the series resistance. The processing is performed on (100) bulk Si wafers, with the channel directed along the crystallographic direction. This yields the maximum low-field electron mobility, μ_n [YSun-07]. The sidewalls of a FinFET, on the other hand, are formed by (110) planes for the standard wafer

orientation, as shown in Figure 5.3(a), resulting in a lower μ_n, while the hole mobility (μ_p) is maximum in this plane. In order to achieve sidewall conduction along (100) surfaces, the fin was rotated over 45º, as shown in Figure 5.3(b).

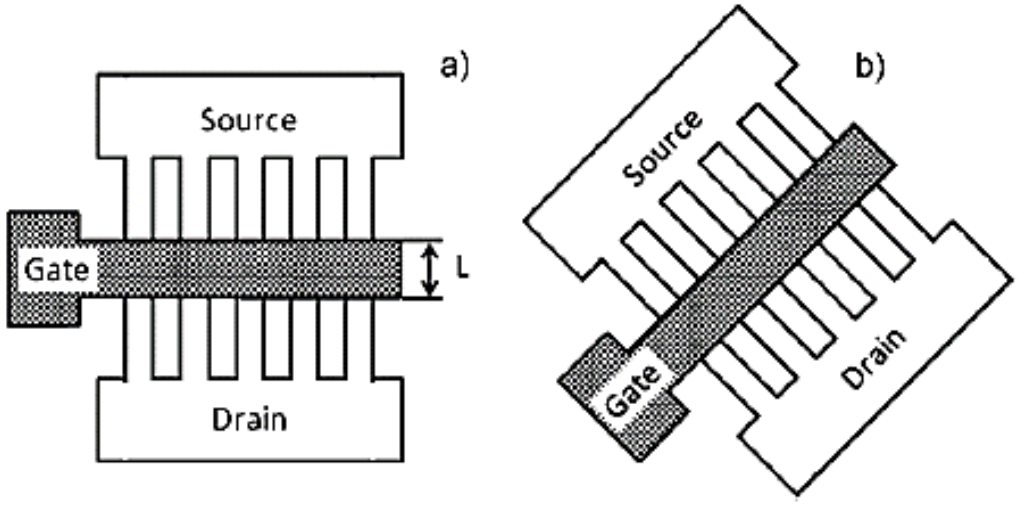


Fig. 5.3: Top view of a standard (a) and a 45º rotated (b) configuration of a multiple gate FinFET. (After [Put-10(2)].)

5.1.2 SOI FinFETs

SOI FinFETs were processed on (100) SOI substrates of thickness 150 nm. In the devices with fins according to standard orientation, the sidewalls have a (110) crystal orientation, resulting in a better hole mobility. When the fins are rotated over 45º the sidewall orientation is (100) and the electron mobility increases. The gate insulator consists of a 2.6 nm HfSiON-layer, with 45% Hf on a 1 nm interfacial SiO_2 and 100-nm of poly-crystalline silicon on top of a 5 nm TiN metal gate. The equivalent oxide thickness EOT=1.5 nm [Put-10(2)]. A top view SEM is shown in Figure 5.4 and the schematic cross-section is shown in Figure 5.5.

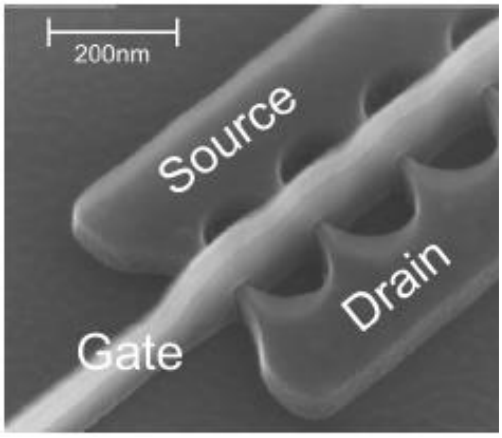
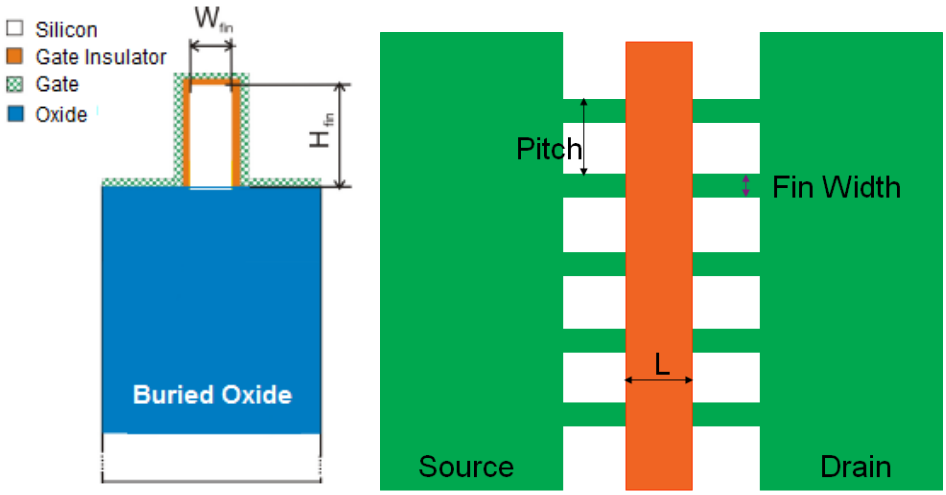


Figure 5.4: Top-view SEM image of a SOI n-channel FinFET. (After [Put-10(2)].)



(a) Cross-section (b) Top-view

Figure 5.5: Schematic cross-section (not to scale) of a SOI n-channel FinFET. Definition of fin height, fin-width, channel length and pitch in the FinFETs. (After [Put-10(2)].)

5.2 Experimental Details: Device-under-test

5.2.1 Bias Dependence Experiments

The transistors used in the experiments have a drawn channel length of 70 nm with 5 fins in parallel. The fin width is 5 nm and the fin height is 35 nm, so the effective device width is given by: $W = N \times (W_{fin} + 2H_{fin}) = 375$ nm. For each of the test conditions, 5-7 devices were tested.

5.2.2 Geometry Dependence Experiments

Transistors of varying geometries were used for these experiments. For understanding the effects of TID with varying fin widths, four different fin-widths were exposed to irradiation. The channel length was 70 nm and the fin-to-fin pitch was 1 µm. For the channel length variation experiments, three channel lengths 50 nm, 70 nm and 130 nm were exposed to ionizing radiation. The fin width for the channel length studies was 40 nm and the fin-to-fin pitch was 1 µm. For fin-to-fin pitch studies, two different flavors were tested, one with fin-pitch of 200 nm and the other 1 µm. For each of the test conditions, 5-7 devices were tested. The details are summarized in Table 5.1.

TABLE 5.1

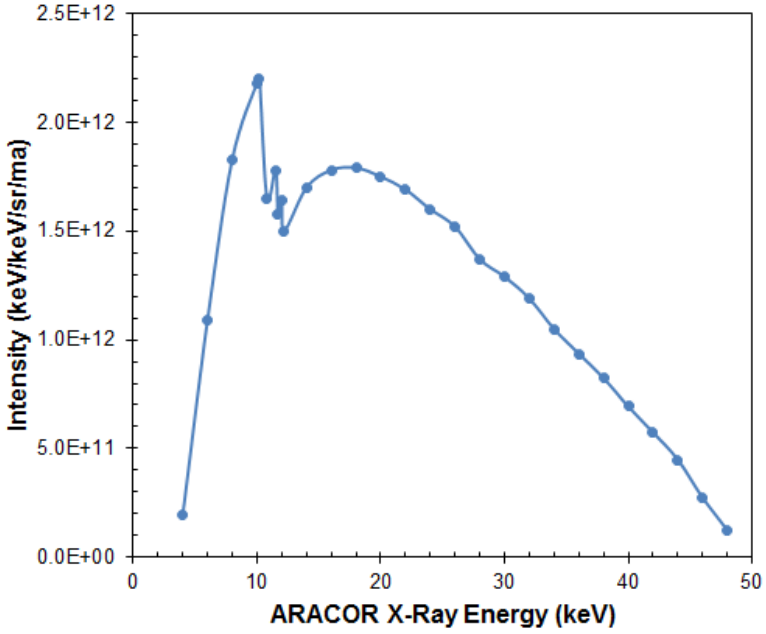
GEOMETRY VARIATIONS IN BULK FINFETS

Test Conditions	Varying Parameters (in nm)	Fixed parameters
Fin Width (FW) Variation	FW: 5/20/40/130	CL: 70 nm, P: 1000 nm, No. of fins: 5
Channel Length (CL) Variation	CL: 50/70/130	FW: 40 nm, P: 1000 nm, No. of fins: 5
Pitch (P) Variation	P: 200/1000	FW: 20 nm, CL: 70 nm, No. of fins: 5

5.3 Experimental Details: Irradiation and Measurements

Transistors were irradiated at room temperature with 10-keV X-rays using an (Advanced Research and Applications CORporation (ARACOR) Model 4100 Irradiator at a dose rate of 31.5 krad(SiO_2)/min to a cumulative dose of 500 krad(SiO_2). The irradiator generates soft X-rays with the peak at 10 keV. The beam is produced by a 60 kV, 3 kW x-ray tube [Arac-78]. A collimator and shutter system provides a uniform 3-cm-diameter beam. The system has a radiation-tight and interlocked enclosure that provides safety to the operator during the exposure

(a) ARACOR Model 4100 10-keV X-ray source at Vanderbilt University



(b) ARACOR 4100 X-ray source spectrum

Figure 5.6: (a) ARACOR X-ray system (model 4100) used in this work (b) Typical X-ray spectrum in an ARACOR operated at 35 kV. (After [Dozi-83].)

of the samples. A calibrated Si *p-i-n* diode is mounted at the sample platform level to measure the dose rate at the front surface. The dose rate can be controlled by changing the voltage and/or current setting in the XRG 3100 X-ray generator from Philips [Arac-78]. The voltage can be

changed in the range of 20 kV to 45 kV and the current can be changed in the range of 0.5 mA to 40 mA. In normal operation, the X-ray beam passes through 150 μm of Al filtering before exposing the sample to shield the low energy portion of the x-ray spectrum. An image of the system is shown in Figure 5.6(a) and a typical spectrum of the ARACOR x-ray beam is shown in Figure 5.6(b) [Dozi-83].

5.3.1 Transistor Characterization

Current-voltage (I_D-V_G) characteristics were measured with an Agilent 4156 semiconductor parameter analyzer on unpackaged wafers. During measurements, both the source and the substrate were grounded, and a 50 mV bias was applied to the drain. The gate voltage was varied from -0.2 V to 1.0 V.

5.3.2 Bias Dependence Experiments

The bias conditions during irradiation correspond to (1) on-state (ON) and (2) off-state (OFF) for inverter and (3) transmission gate (TG) operation. Other bias conditions were also tested, with the source, drain, and gate either at 0 V (ALL-0), as shown in Table 5.2.

TABLE 5.2

BIAS CONDITIONS FOR IRRADIATION OF BULK FINFETS

	Gate	Source	Drain
ON	1.0 V	0	0
OFF	0	0	1.0 V
ALL-0	0	0	0
TG	0	1.0 V	1.0 V

5.3.3 Geometry Dependence Experiments

For understanding the effects of geometry on the total-dose response of FinFETs, transistors were irradiated at three bias conditions, ON state, OFF state and ALL-0 states. All three bias conditions showed qualitatively similar results. In this dissertation, results from the worst case state are reported. Thus the responses recorded in this section are the worst case behaviour of the FinFETs when exposed to ionizing dose.

In the following chapter, the experimental and simulation studies of the bias dependence of total ionizing dose response of bulk FinFETs are reported.

CHAPTER VI

CHARGE TRAPPING MECHANISMS IN BULK FINFETS

Total-ionizing-dose irradiation induces net positive trapped charge in oxides and interface traps at silicon/oxide interfaces. The extremely small increase in post-irradiation gate leakage observed in these transistors suggests that there were no leakage paths created in the gate insulator stack (Figure 6.1). The gate stack is very thin, so the trapped charge in the gate insulator is quite small. However, the radiation-induced charge trapping in the STI oxide still leads to macroscopic effects, such as the drain-to-source leakage current, and ultimately limits the radiation tolerance of CMOS circuits [Shan-98]. Thus, the post-irradiation response of these

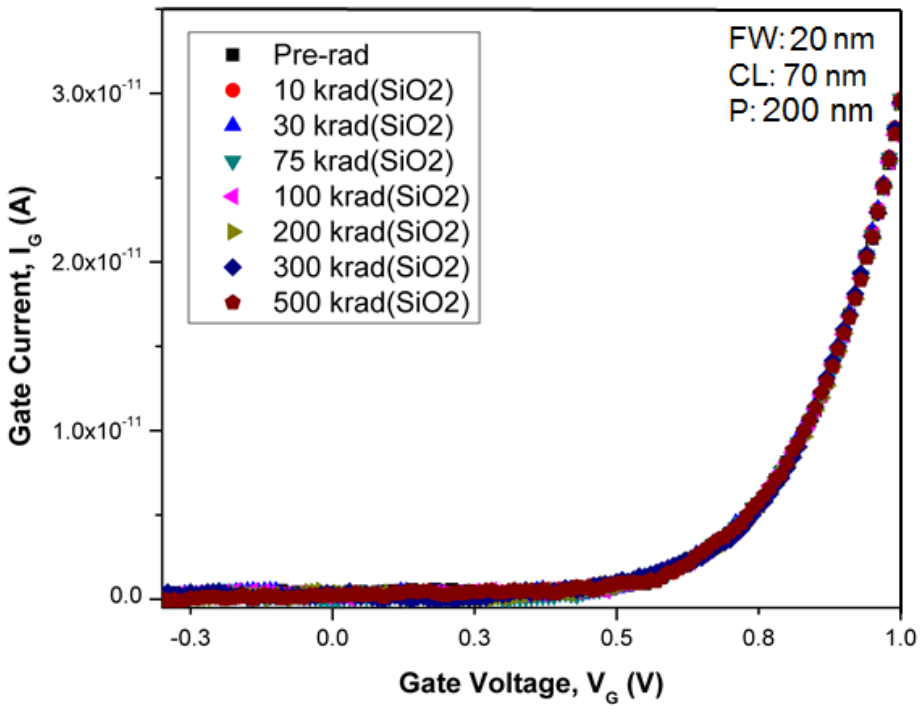


Figure 6.1: I_G-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min. TID Conditions: OFF State. (After [Chat-13].)

bulk FinFETs is dominated by buildup of charge in the isolation oxides (the shallow trench isolation) around the transistors. The change in drain current post irradiation, when plotted

against the FinFET gate voltage takes the shape of a nMOS transistor with a threshold voltage that is lower than that of the original channel. Thus the parasitic transistor turns on earlier than the true transistor and contributes to the off-state leakage current of the system. Figure 6.2 shows the pre-irradiation and post-irradiation characteristics of a sample *n*MOS FinFET and the leakage curent at various doses. The leakage current is a strong function of the gate voltage in the subthreshold region and then saturates with increasing gate voltage when it is swamped by the on-state current of the main transistor.

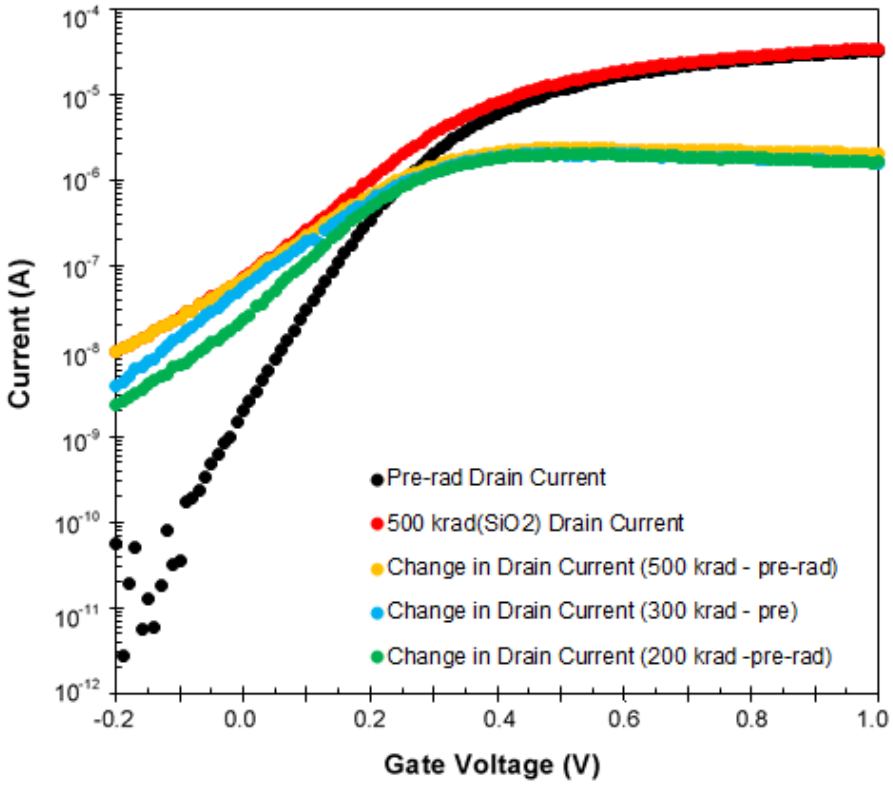


Figure 6.2: I_D-V_{GS} characteristics and change in drain current as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min. TID Conditions: OFF State.

If an electric field exists across an insulator during total dose irradiations, electrons and holes in the insulator will immediately begin to transport in opposite directions. Electrons are extremely mobile in the silicon oxides and are normally swept out of it in picoseconds [Hugh-

73], [Hugh-73(2)]. Holes generated in the silicon oxides transport much slower than electrons and a substantial fraction may be trapped. As a result, hole trapping usually determines the transistor response after irradiation. As the electric field increases, the probability that a hole will recombine with an electron decreases and the fraction of un-recombined holes increases [Flee-13]. The electric field extends into the trench region and plays a pivotal role in both the initial separation of electron–hole (e–h) pairs and the charge migration. Figure 6.3 shows an illustration of the trapped charges in the isolation oxides. There are a large number of oxygen vacancies in the STI close to the silicon/oxide interface due to the out diffusion of oxygen near the oxide and the lattice mismatch at the interface [Flee-13]. These oxygen vacancies can act as trapping centers. The fraction that is trapped is strongly related to the electric field in the oxide during irradiation [Shan-98], [Flee-13]. The overall response of bulk FinFETs is therefore similar to planar bulk MOSFETs.

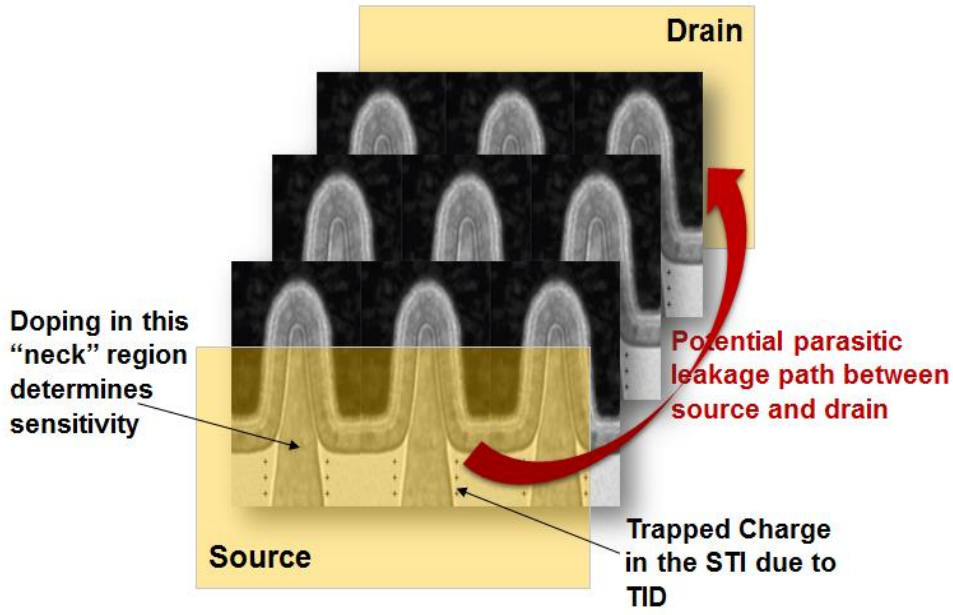


Figure 6.3: Schematic diagram showing the trapped charges in the isolation oxide in a multi-fin FET (representative figure only, not to scale) (After [Chat-14] and [Chip-12].)

CHAPTER VII

BIAS DEPENDENCE OF TOTAL IONIZING DOSE EFFECTS IN FINFETS

This chapter focuses on the bias dependence of total ionizing dose effects in bulk FinFETs. The experimental results would be contrasted to those of SOI FinFETs. 3D TCAD simulations were deployed to understand the experimental results and the differences in the charge trapping mechanism in bulk and SOI FinFETs.

7.1 Bulk FinFETs:

The bias applied to the transistor terminals during exposure to radiation is a critical parameter influencing charge trapping. Figure 7.1 shows the pre- and post-irradiation *I-V* characteristics for the four bias conditions under consideration. The highest increase in off-state leakage is observed for the OFF-state bias condition, for all doses considered. The pre-irradiation off-state leakage is ~3 nA and increases to ~500 nA after a cumulative dose of 500 krad(SiO_2). The smallest shift is observed in the case of the ALL-0 bias condition. The off-state leakage for this bias condition increased from ~2 nA (pre-irradiation) to ~30 nA (500 krad(SiO_2)). Figure 7.2 shows I_{OFF} vs. cumulative dose for the bias conditions under consideration. At low dose, the high electric fields in the corners of the shallow trench isolation are partly responsible for the increased transistor leakage current [Shan-98], [Flam-03]. The simulations detailed later in this chapter show that the electric field at the trench corners is highest for the OFF state bias. At a high dose, the leakage current becomes relatively independent of gate voltage, which means that the parasitic transistors play an important role for the leakage current. As the fin width is less than 15 nm, the electrostatic potential is predominantly controlled by the lateral gates, fully depleting the silicon fin in the ON state. The longitudinal penetration of the fringing electric field

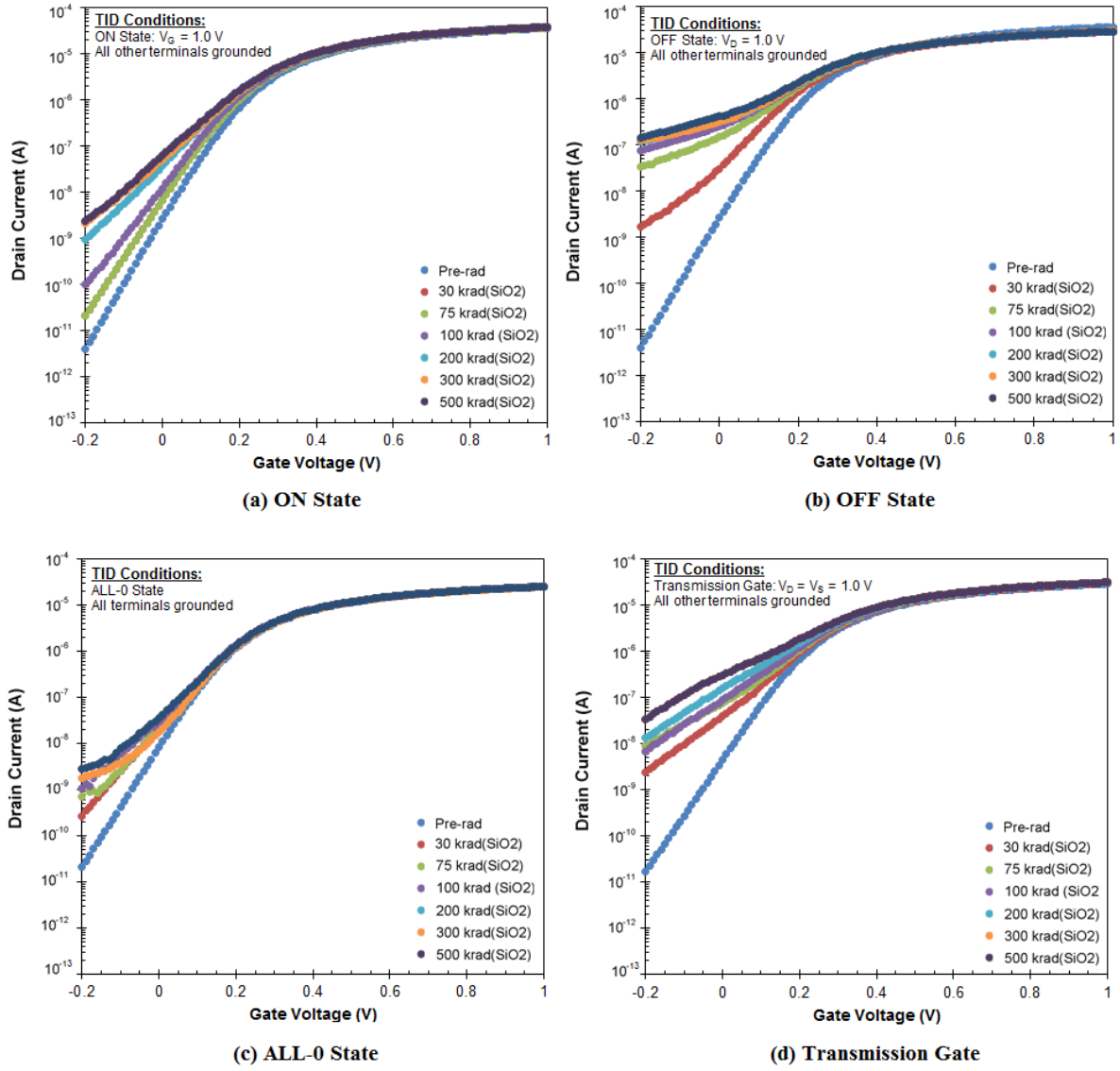


Figure 7.1: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for the various bias conditions under consideration. The DUT is 5-fin 70 nm FinFET. (After [Chat-13].)

from the source and drain to the channel, e.g., the drain-induced virtual substrate biasing (DIVSB) effect [Gail-06], is prevented. Figure 7.3 shows the subthreshold swing (SS = dV_G/d(log I_D)) of the 70-nm-gatelength FinFET as a function of dose for the worst case and best case bias condition. Irradiation of the samples to a dose of 500 krad(SiO_2) produced significant changes in the subthreshold slope. The subthreshold slope increases by ~75 mV/decade for the

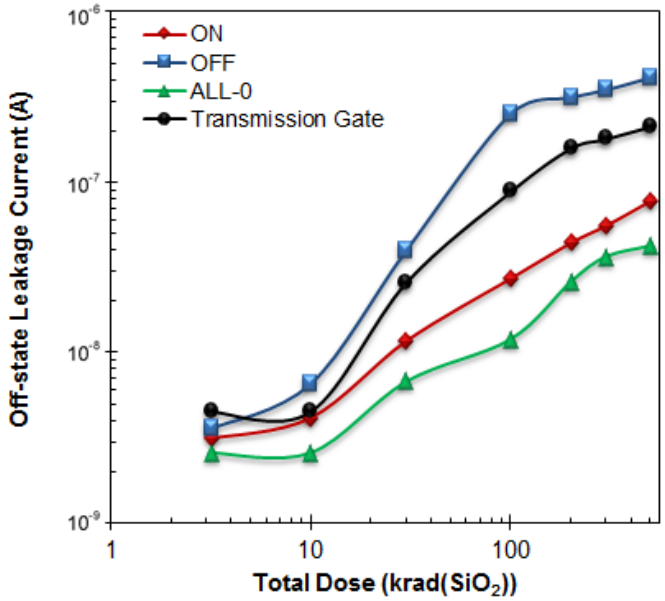


Figure 7.2: Off-state leakage current (I_{OFF}) as a function of total dose for a 70 nm 5-fin width bulk FinFET. The continuous line joining the discrete data points is to be used as an aid to the eye. (After [Chat-13].)

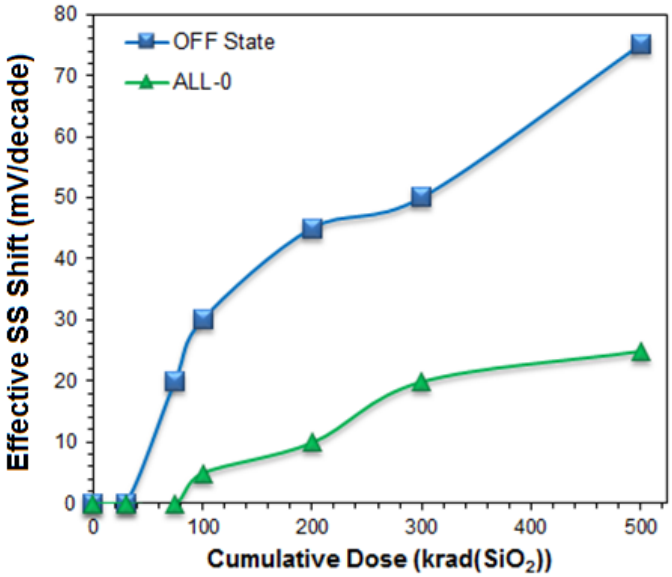


Figure 7.3: SS shift as a function of dose for a 70 nm 5-fin width bulk FinFET for the worst-case and best-case bias condition. The measurement is done at V_D = 50 mV (After [Chat-13].)

worst-case bias condition and ~25 mV/decade for the best-case condition. It is important to note here that the subthreshold slope degradation observed here is not because of formation of interface traps in the gate insulator stack of the main transistor, but rather because of the turning

of the parasitic channel before the main transistor. As mentioned in Chapter VI, the parasitic channel is controlled by the gate voltage in the subthreshold region and thus gives the impression of a subthreshold slope degradation of the main transistor.

7.2 SOI FinFETs

Bias configuration during irradiation should impact the TID response of multiple-gate devices as it governs the electric field shape in the BOX and thus the resulting oxide-trapped charge distribution. Figure 7.4 shows the pre-irradiation and post-irradiation characteristics of SOI FinFETs for different TID bias conditions. The highest shift in the off-state leakage current (~20 nA to ~100 nA) is seen for the ON state bias condition and the least in ALL-0 state (~10 nA to ~25 nA). This is in accordance with what has been observed previously. The threshold voltage shift of the front-channel and back-channel combination is negligible for these devices and insignificant subthreshold slope degradation was observed. This shows that the effect of irradiation on the thin front-gate insulator is negligible and the charge trapped in the buried oxide dominates the radiation response of the SOI FinFETs. For the ON-state bias configuration, radiation-induced electron-hole pairs are separated by the electric field and the holes are driven towards the fin/BOX interface. The radiation-induced carriers follow the fringing field lines from the gate to the fin/BOX and are trapped near the fin/BOX interface. Holes trapped near the back interface have an electrical influence on the silicon film. As net positive charge builds up, it increases the off-state leakage of the SOI FinFETs [Song-11]. However, compared to bulk FinFETs of similar dimensions, the increase in off-state leakage current in SOI FinFETs is much less. Thus these devices are relatively strong candidates for next generation of electronics operating in harsh environments.

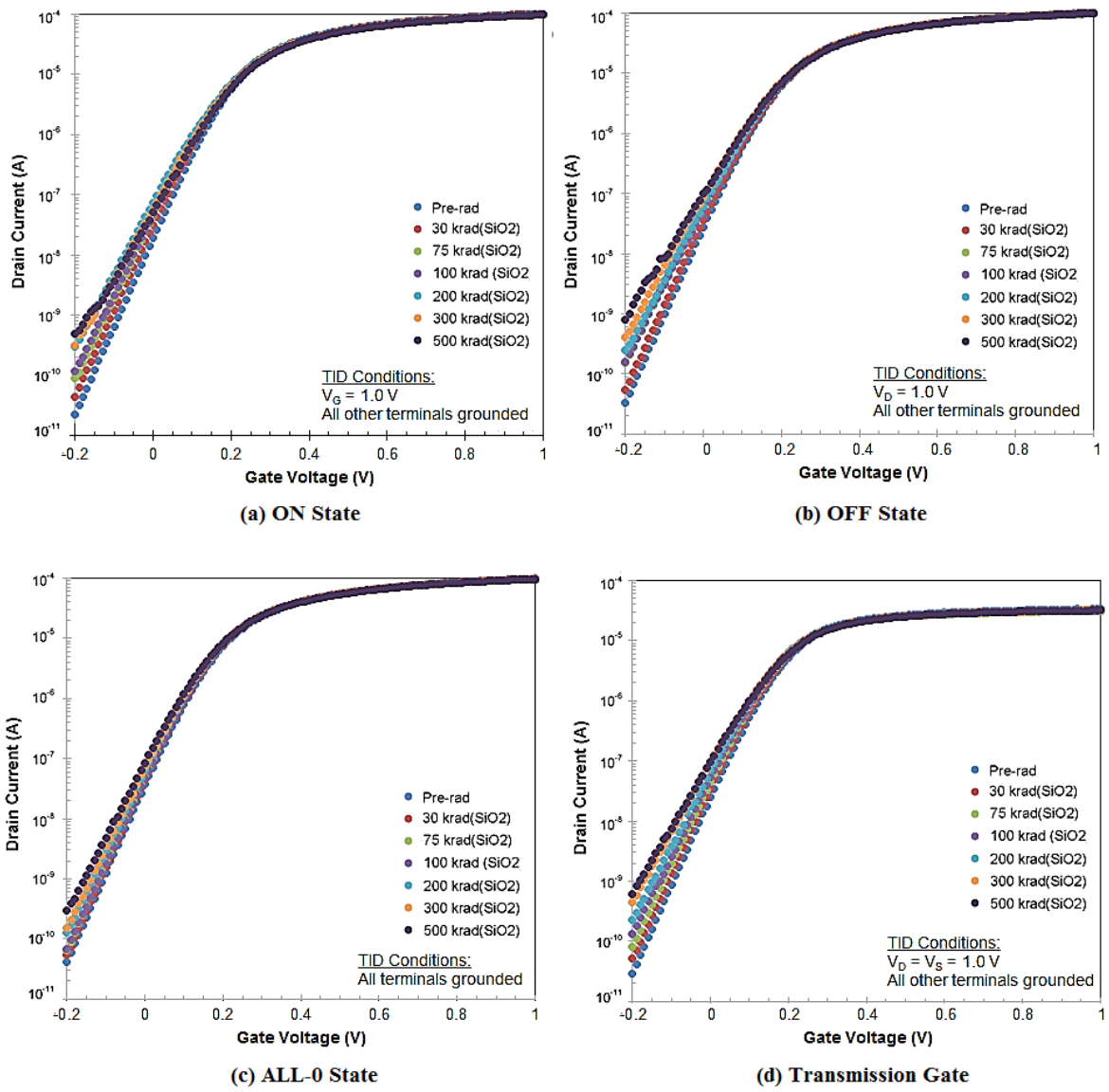
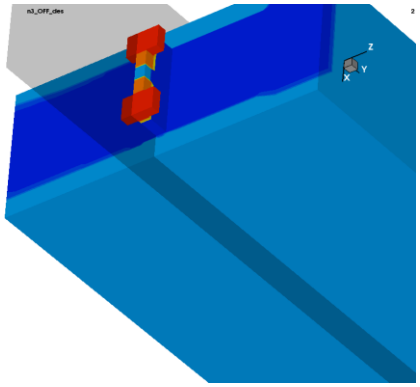


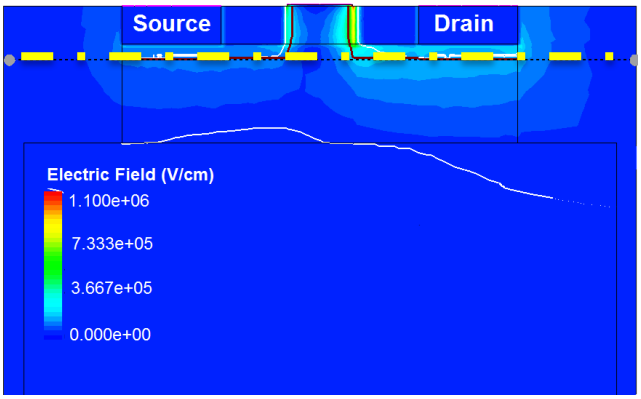
Figure 7.4: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for the various bias conditions under consideration. The DUT is 5-fin 70 nm SOI FinFET.

7.3 TCAD Simulations

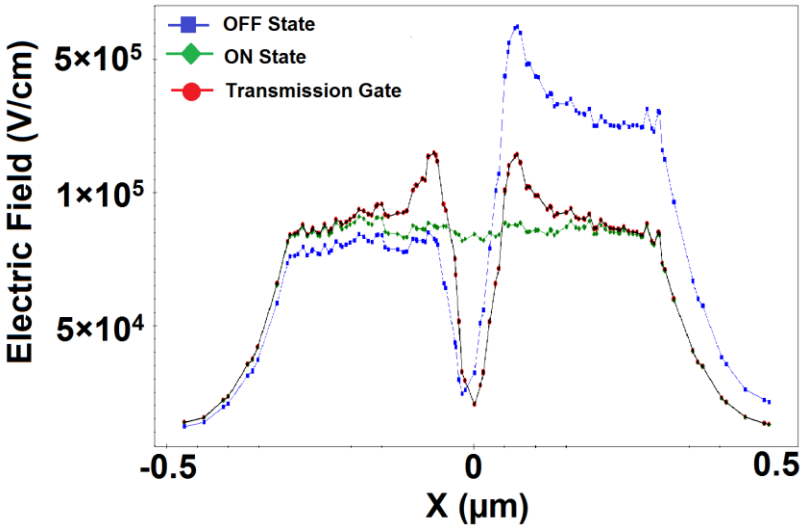
To gain an understanding of the experimental results in the previous sections, 3-D TCAD simulations were carried out. A 1-fin FinFET was developed in the Synopsys® TCAD suite. The block of silicon used for the simulations is 10 µm × 10 µm × 10 µm. The gate length is 70 nm



(a) Plane showing the location of the Z-cut



(b) Dashed line showing the location of the Y-cut



(c) Electric field along the cutline shown in (b) for OFF, ON, and Transmission Gate

Figure 7.5: (a) & (b) Illustration of the FinFET showing the cuts in the device. (c) Electric fields along the Y-cut for ON, OFF and transmission gate bias conditions. The electric field is highest near the fin/STI interface in the case of the transistor biased in the OFF-state configuration. (After [Chat-13].)

and the fin width is 20 nm. The fin height is 35 nm. The STI oxide is 250 nm thick. The area of the source and drain is ~0.5 μm^2. Since the radiation-induced charge in the thin gate insulator is much smaller than that in the shallow trench isolation (STI), charge at the gate insulator/substrate interface was not included in the simulations. The field in the STI is shown in Figure 7.5 for three different bias conditions: OFF, ON, and transmission gate bias conditions. The electric field extending into the trench region is important for the separation of electron–hole pairs and the charge migration. Three processes are involved i.e., (1) charge yield, (2) charge transport by drift and diffusion, and (3) hole trapping at the interface between the STI and the substrate silicon. Figure 7.6 shows that the electric field in the STI corner along the bottom of the channel where the isolation oxide touches the channel is largest for the OFF-bias condition, compared to the other bias conditions. The charge yield is the greatest at the highest fields [Shan-91], so the trapped charge and the off-state leakage are the largest for the OFF-state irradiation (Figure 7.2(b)). The leakage current depends on the doping along those parasitic paths [Razz-11]. Further simulations were carried out to study the Radiation-Induced Narrow Channel Effect (RINCE) [Gail-11]. A sheet of positive trapped charge ($10^{12}/cm^2$) was incorporated along the STI boundary to study the effects of the trapped charge on the threshold voltage. No observable effect was seen in the simulations, indicating the strong electrostatic control of the lateral gates on the narrow-channel FinFETs. In SOI FinFETs, for ON state bias, a number of electric field lines points directly to the silicon finger area, as depicted in Figure 7.6 by black arrows. A significant buildup of trapped-charge occurs in this region, modifying efficiently the potential in the silicon finger and then the device's electrical characteristics.

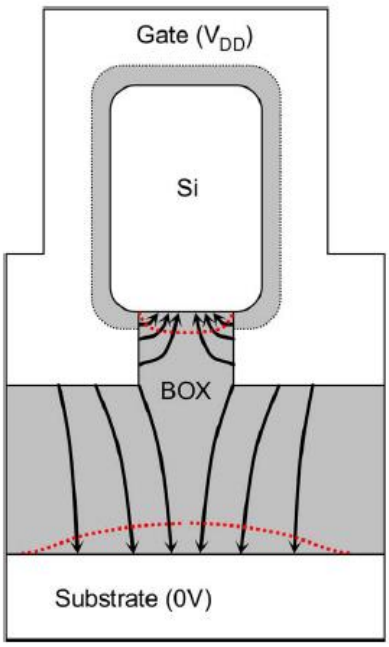


Figure 7.6: Schematic description of the shape of the electric field lines into the BOX of a SOI FinFET biased in the transmission gate. Red dashed lines correspond to the resulting trapped charge distribution after irradiation (located either at the bottom of the BOX or next to the silicon finger). (After [Gail-06].)

7.4 Summary

Bulk FinFETs have a similar total ionizing dose response as planar bulk MOSFETs, i.e., the build-up of oxide-trapped charge in the STI triggers a parasitic lateral transistor which modifies the electrical characteristics (higher I_{OFF}). The worst-case total-dose radiation response of bulk FinFETs occurs under the OFF bias condition where the drain is at a higher potential and the rest of the transistor terminals are at 0 V. The degradation is found to be least under ALL-0 and negative gate bias conditions up to 500 krad(SiO_2). The total ionizing dose effects on these bulk FinFETs are attributed to the relatively higher electric field at the STI corner and the resulting threshold-voltage shift of the parasitic STI transistors. The trapped charge in the STI oxide induces a parasitic leakage current path that dominates the radiation response of bulk FinFETs. This is in contrast to the radiation response of SOI FinFETs, where the worst-case bias condition

was determined to be the On state bias configuration (drain and source at V_{DD}, other contacts grounded) because of charge trapping in the buried oxide. 3D TCAD simulations were performed to understand the mechanisms behind the bias dependence of total dose radiation response of these transistors. Degradation due to the ionizing radiation leads to increased leakage current and subsequent increase in power consumption.

CHAPTER VIII

GEOMETRY DEPENDENCE OF TOTAL IONIZING DOSE EFFECTS IN FINFETS

In non-planar multiple-gate devices, the coupling behavior between various fields in the transistor is different and complex, especially as fin widths and gate lengths are of comparable dimensions. A lateral coupling effect induced by the lateral gates appears in addition to the vertical coupling effect of single-gate devices [Doyl-03], [Kava-06]. These complex electrostatic coupling effects are strongly geometry dependent. Thus, it is important to understand the effect of these parameters on the TID response of FinFETs. In this section, the dependence of TID induced degradation on various geometry variations, namely, fin-width, channel length and fin-pitch are investigated for bulk and SOI FinFETs.

8.1 Fin Width Variation

For better subthreshold slope (SS) and drain induced barrier lowing (DIBL) of FinFETs, the fin width is a more important parameter than the physical gate length. Thus, scaling FinFETs requires reducing the fin-width as narrow fins enhance electrical performance by reducing short channel effects.

8.1.1 Bulk FinFET

Figure 8.1 shows the pre- and post-irradiation I_D-V_G characteristics for four different fin-widths (5 nm, 20 nm, 40 nm, and 130 nm). With increasing fin-width, the TID-induced degradation decreases. Examination of the shapes of the transistor characteristics shows that it is the parasitic transistor that turns on and produces the high leakage current. The least change in off-state leakage current (V_G = 0 V) is observed in the 130 nm fin-width transistor (almost no

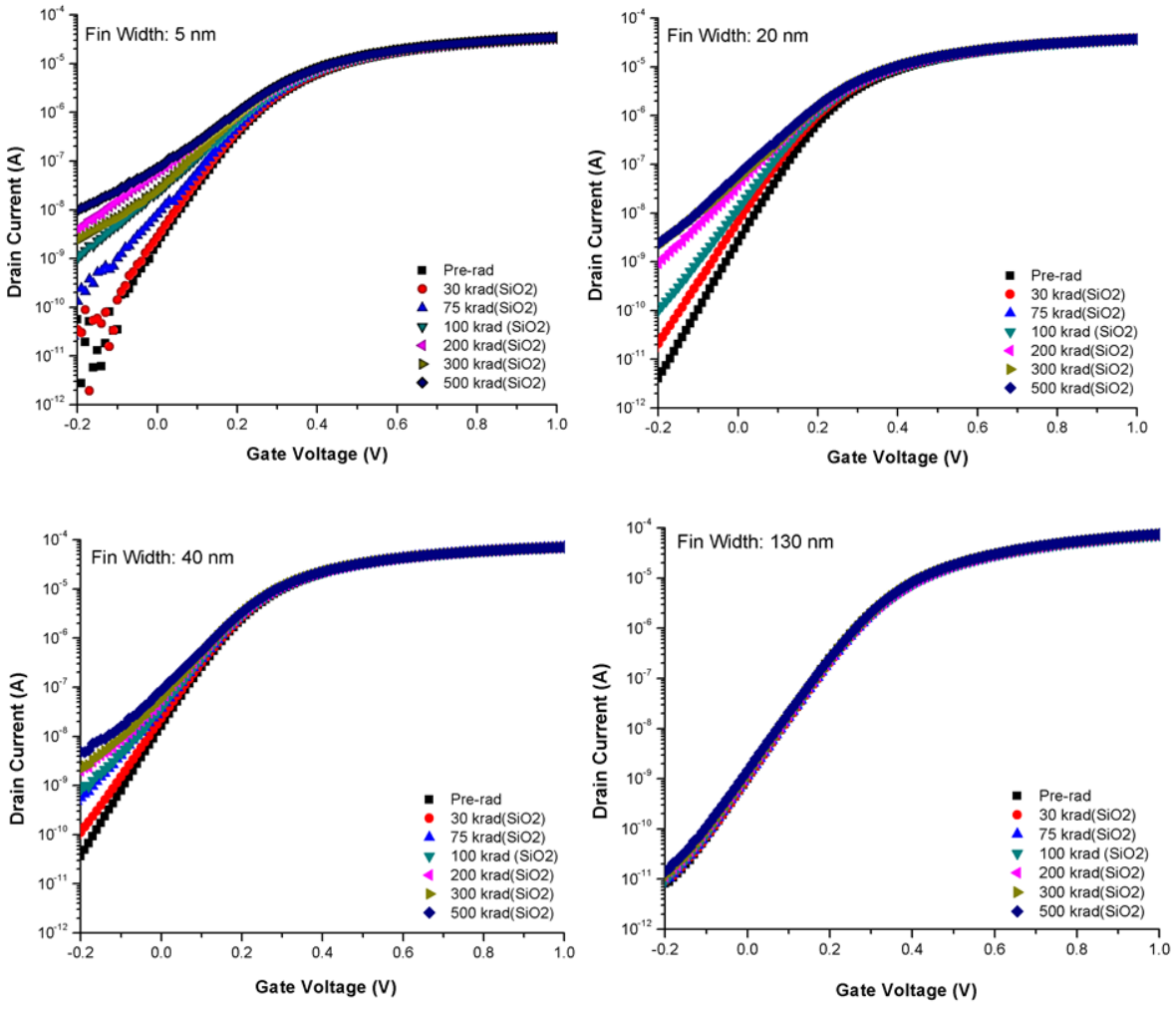


Figure 8.1: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for a 70 nm 5-fin width bulk FinFET for the four different fin widths under consideration. (After [Chat-14].)

change). The largest change is observed in the 5 nm fin-width transistor (~3 nA to ~100 nA) (Figure 8.2). Figure 8.3 shows the effective subthreshold swing (SS = dV_G/d(*log* I_D)) of the 70-nm-gatelength FinFET as a function of dose for the different fin-widths under consideration. The result shows that the trapped charge in the STI reduces the I_{ON}/I_{OFF} ratio, or in other words, subthreshold slope degradation is observed.

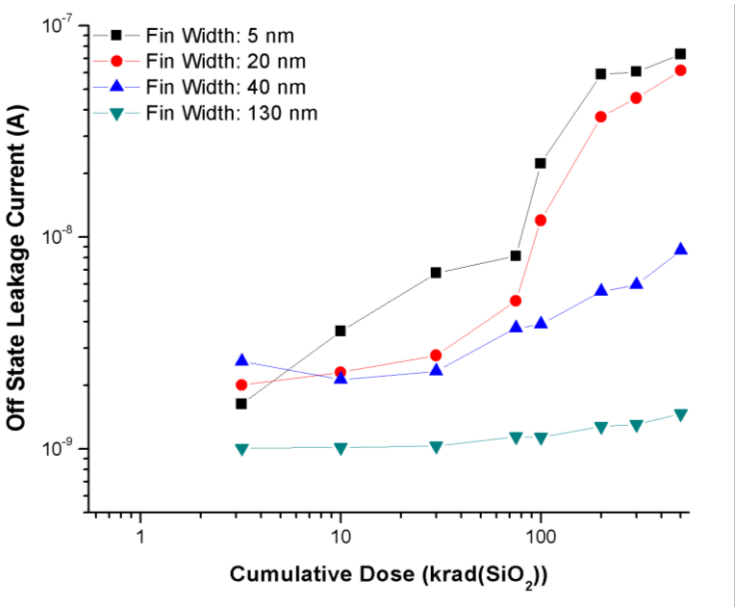


Figure 8.2: Off-state leakage current as a function of dose for a 70 nm 5-fin width bulk FinFET for the four different fin widths under consideration. The measurement is done at V_D = 50 mV. (After [Chat-14].)

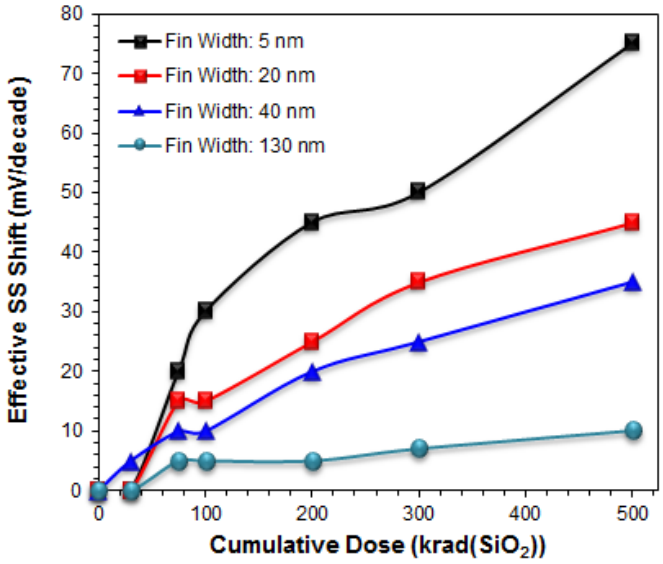


Figure 8.3: Effective SS shift as a function of dose for a 70 nm 5-fin width bulk FinFET for the four different fin widths under consideration. The measurement is done at V_D = 50 mV.

8.1.2 SOI FinFET

The trend observed is completely different from that observed in SOI FinFETs where the

radiation-induced degradation increases when the fin width increases. Figure 8.4 shows the pre- and post-irradiation I_D-V_G characteristics for four different fin-widths (5 nm, 20 nm, 40 nm, and 130 nm). The results are consistent with experimental evidences obtained earlier [Mamo-10], [Put-10(3)], [Esqu-11], [Koba-11], [Simo-13].

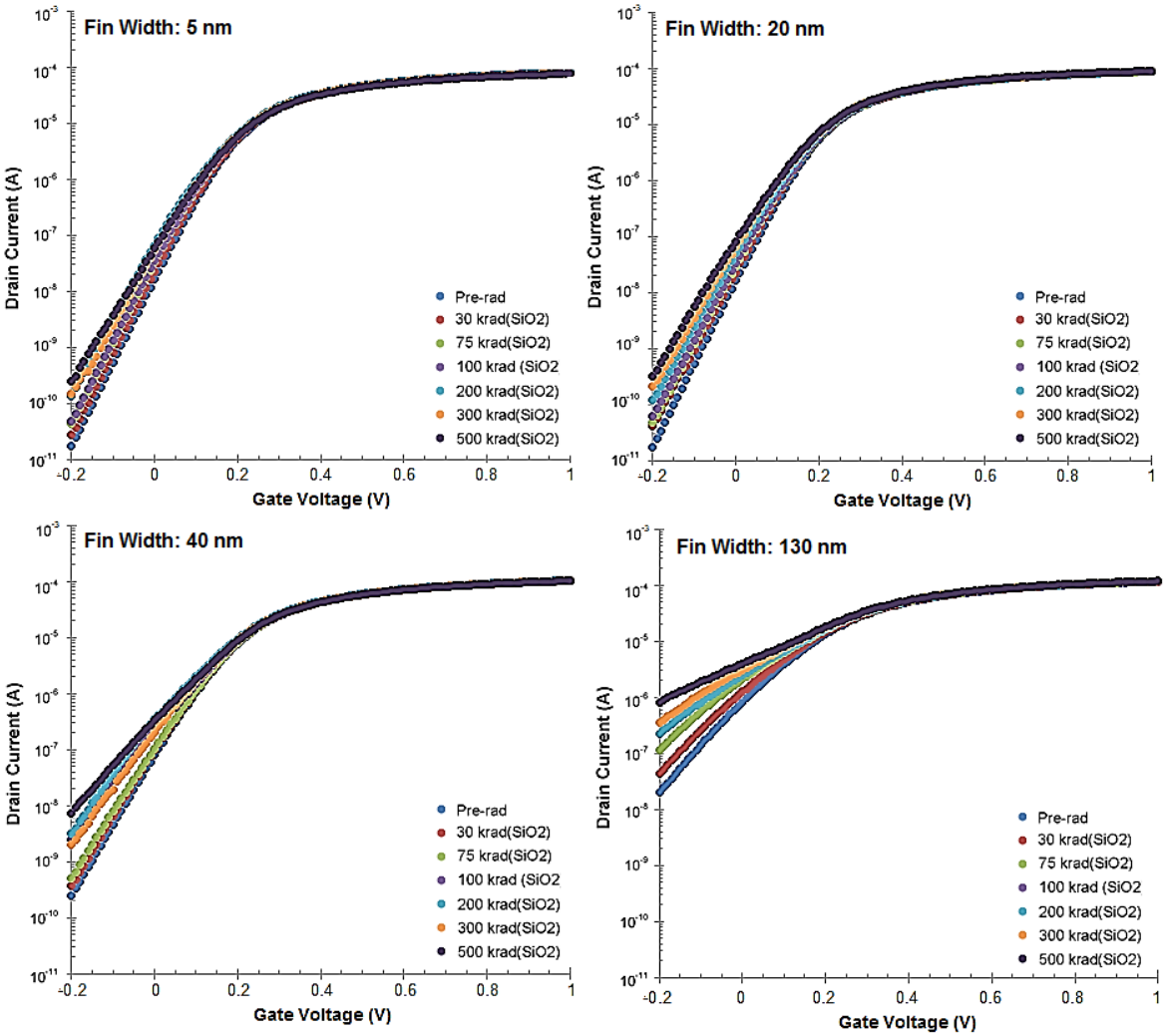


Figure 8.4: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for a 70 nm 5-fin width bulk FinFET for the four different fin widths under consideration.

8.1.3 TCAD Simulations:

To gain an understanding of the experimental results, 3-D TCAD simulations were carried

out. A 1-fin FinFET was developed in the Synopsys® TCAD suite. The block of silicon used for the simulations was 10 μm × 10 μm × 10 μm. The STI oxide was 250 nm thick. The areas of the source and drain were each ~0.5 μm^2. Because the concentration of radiation-induced charge in the thin gate insulator stack is much smaller than that in the shallow trench isolation (STI), charge at the gate insulator/substrate interface was not included in the simulations. As discussed earlier, charge trapped in the STI is the key degrading mechanism in bulk FinFETs, compared to SOI FinFETs, where charge trapped in the BOX plays the key role in transistor parameter degradation.

For fin-width variation studies, two fin-widths, 5 nm, and 40 nm were simulated. The channel length was 70 nm and the fin height was 35 nm. The post-irradiation simulations were performed by placing a sheet charge with a non-uniform distribution at the trench sidewall interfaces. An areal density of 10^{12} cm^{-2} positive charges was introduced in the STI. The leakage current depends on the doping along those parasitic paths [Razz-11]. Figure 8.5 shows the electron density and Figure 8.6 shows the electron current density from the source to the drain along the channel. This is the parasitic transistor induced because of the trapped charge in the STI and constitutes the off-state leakage current in the transistor. When the fin width is reduced, the radiation-induced charge in the STI is closer to the middle of the channel and affects the potential in a stronger way. Therefore, the same amount of charge has a stronger influence on the behavior of bulk finFETs when the fin width decreases (Figure 8.7). The current density from source to drain is higher in the 5 nm fin-width transistor compared to that of the 40 nm fin-width transistor. An interesting point to note here is the shape of the current density path between the source and the drain. A greater portion of the charge follows a curved path from the source to the drain instead of a straight path. This is because of the strong

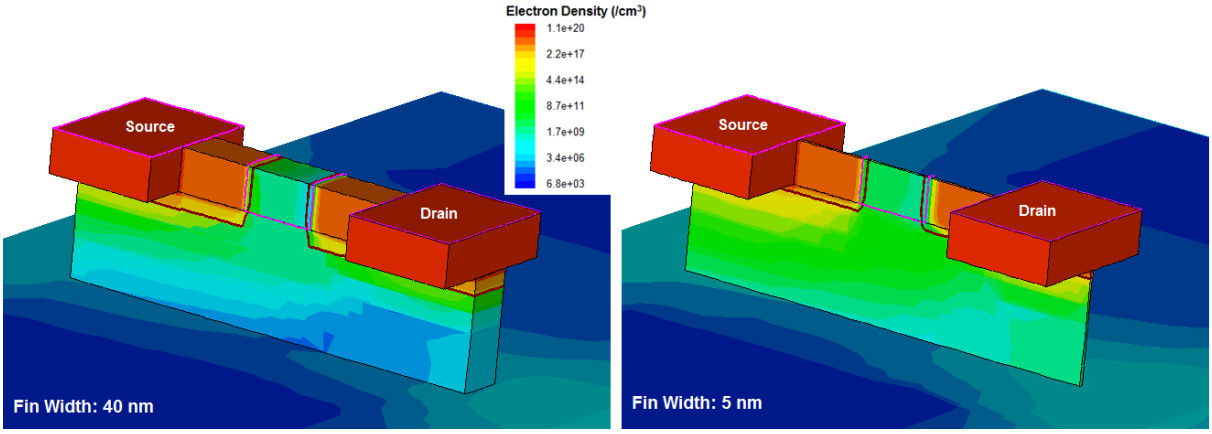


Figure 8.5: Illustration of the FinFET TCAD model showing the electron density (parasitic transistor) from the source to the drain along the channel. The density is higher in the FinFET with 5 nm fin-width.

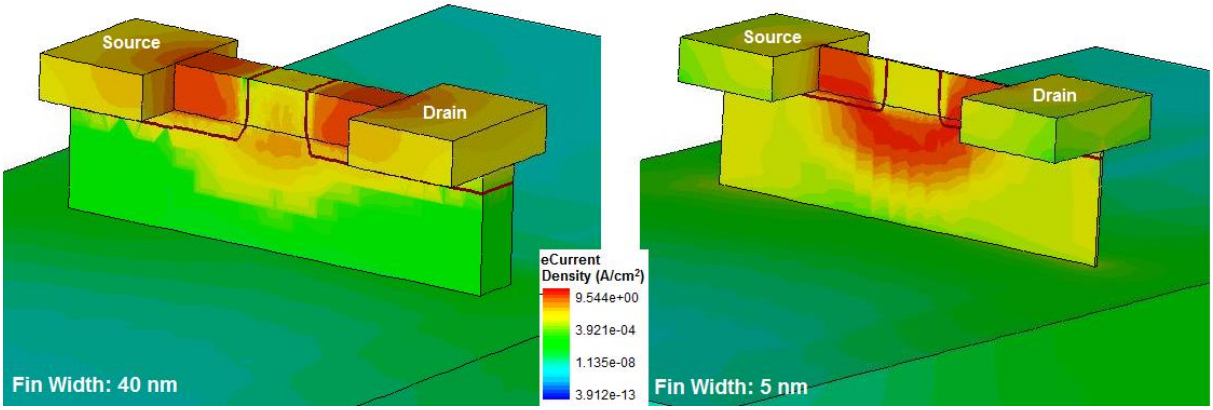


Figure 8.6: Illustration of the FinFET TCAD model showing the electron current density (subsurface leakage) from the source to the drain along the channel. The current density is higher in the FinFET with 5 nm fin-width. (After [Chat-14].)

electrostatic control of the lateral gates which does not allow the leakage current to take a straight path. Instead, it bends right outside the lateral control of the gate. Also, the presence of halo doping at the bottom of the source-drain region hinders the formation of the direct parasitic path. The curved path is the path of least resistance between the source and the drain.

The different behavior for SOI and bulk FinFETs is related to the location of the radiation-induced traps. For SOI FinFET devices, positive trapped charge in the BOX is a greater concern. In FD SOI devices, charge trapping in the BOX can affect the device degradation

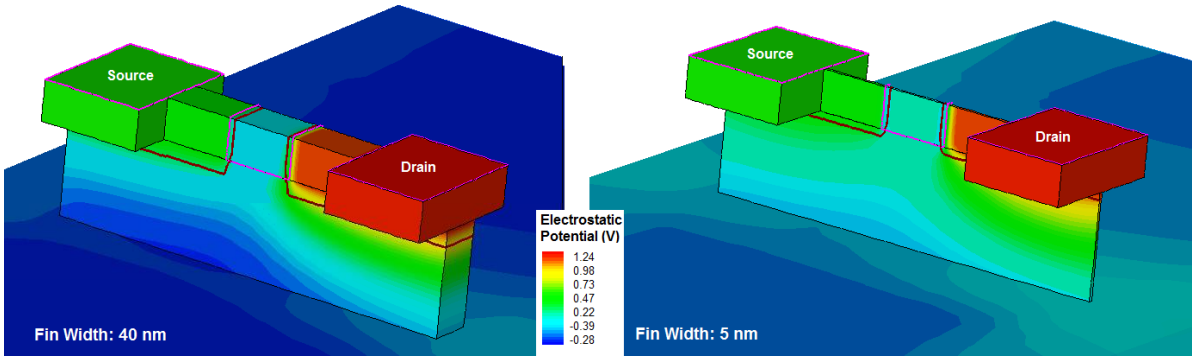


Figure 8.7 Illustration of the FinFET TCAD model showing the electrostatic potential across the fin. The influence of trapped charge on the potential is higher in the FinFET with 5 nm fin-width.

through a direct coupling effect between the front and back interfaces. The width of the back-channel transistor increases in wide-fin SOI devices [Simo-13]. Thus, the radiation-induced degradation in off-state leakage current is greater in wide-fin SOI FinFETs compared to narrow-fin devices. A wide-fin FinFET is similar to a "pseudo" single-gate FD SOI transistor. Its electrostatic behavior is dominated by the front and back gates. The electrostatic control of the lateral gates over the potential in the active silicon film and in the BOX under the silicon-film/BOX interface is weak [Gail-06]. Ionizing radiation exposure induces a positive charge buildup in the BOX of SOI devices, which increases the back-gate surface potential [Gail-06], [Mamo-09]. In single-gate FD SOI devices, the charge trapped in the BOX acts as a positive back-gate bias. Because of the strong vertical electrostatic coupling effects, the front surface potential increases and induces a negative front-gate threshold voltage shift. For narrow fin devices, on the other hand, the primary effect is the screening of the trapped charges into the BOX due to the strong electrostatic control of the lateral gates when they are close to each other. The electrostatic potential in the silicon body and in the BOX under the Si fin/BOX interface is dominated by the lateral gates, thereby limiting the amount of radiation-induced hole charge trapped in the middle of the channel [Song-11]. These effects are shown in Figures 8.8 and 8.9.

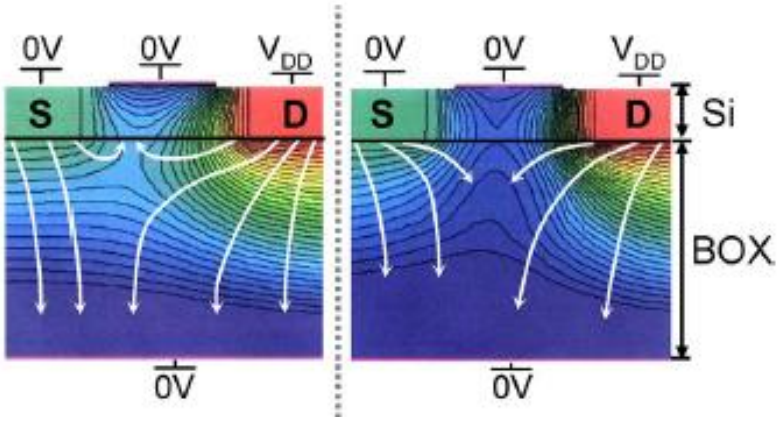


Figure 8.8: TCAD simulations of the electrostatic potential of a wide fin FinFET (a) and a narrow fin FinFET (b) biased under the OFF-state bias (drain voltage at , other terminals grounded) in a cut in the middle of the fin along the source-drain direction. Electric field lines are depicted as white arrows. (After [Gail-06].)

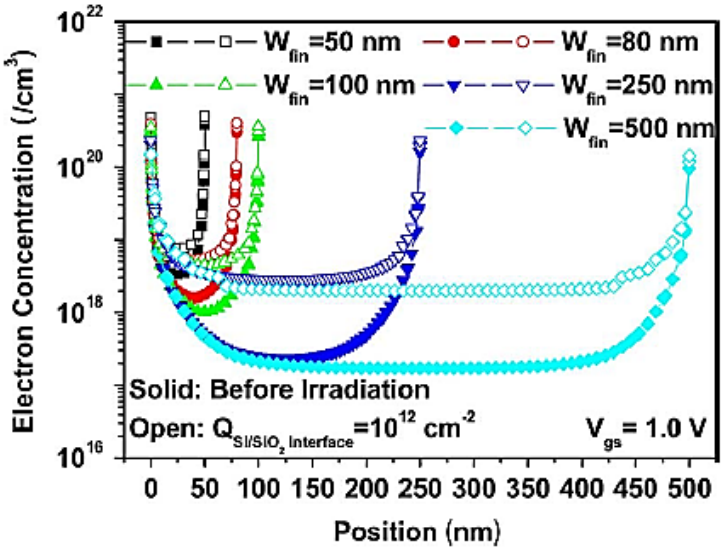


Figure 8.9: Simulated distribution of the electron concentration in the silicon, at fin/BOX interface along the fin width. The gate bias is 1.0 V. (After [Song-11].)

8.2 Channel Length Variation

With technology scaling, channel length has decreased, resulting in faster, more efficient, but more complex transistors. It is important to understand the effects of channel length scaling on the TID response of FinFETs.

8.2.1 Bulk FinFET

Figure 8.10 shows the pre-irradiation and post-irradiation I_D-V_G characteristics of FinFETs with channel lengths of 50 nm, 70 nm and 130 nm up to a cumulative dose of 500 krad(SiO_2).

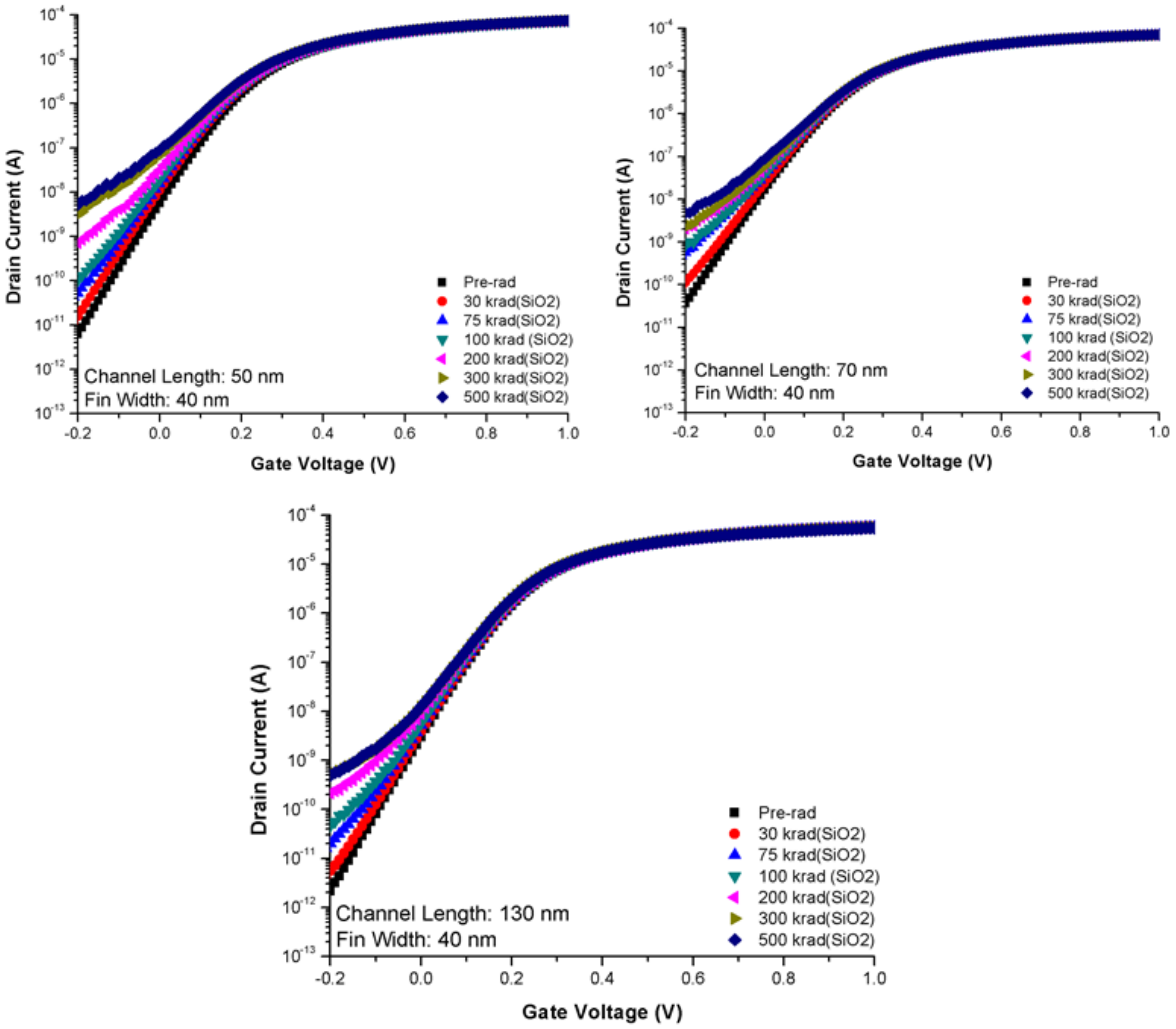


Figure 8.10: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 50 nm, 70 nm and 130 nm channel length transistors. The number of fins 5 and the fin-width is 40 nm. (After [Chat-14].)

Figure 8.11 shows the I_{OFF} vs. cumulative dose. The highest degradation is observed in the transistor with 50 nm channel length and the least in the 130 nm transistor. Effective subthreshold slope degradation was highest in the transistor with minimum channel length (~55 mV/decade) (Figure 8.12).

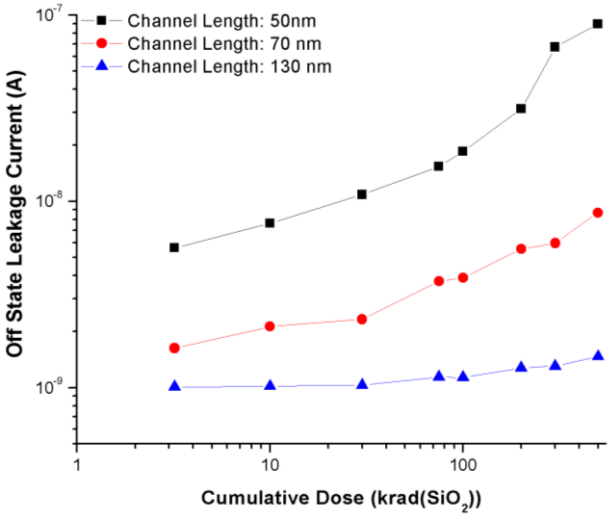


Figure 8.11: Off-state leakage current as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 50 nm, 70 nm and 130 nm channel length transistors. The number of fins 5 and the fin-width is 40 nm. The measurement is done at V_D = 50 mV. (After [Chat-14].)

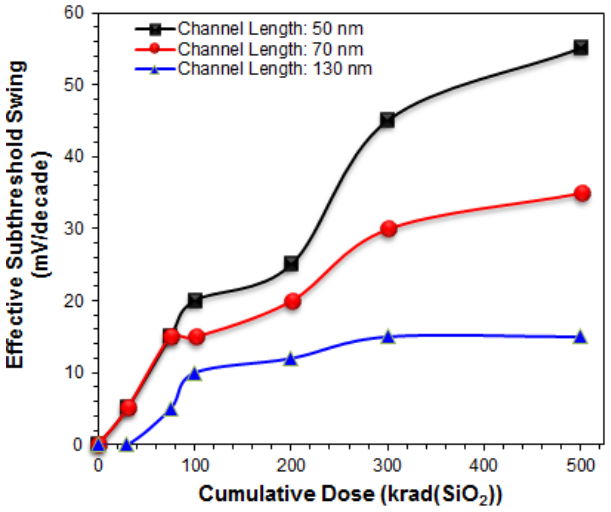


Figure 8.12: Effective subthreshold swing as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 50 nm, 70 nm and 130 nm channel length transistors. The number of fins 5 and the fin-width is 40 nm. The measurement is done at V_D = 50 mV.

8.2.2 SOI FinFET

Similar trends were observed in SOI FinFETs where degradation decreases with increasing channel length. The pre-irradiation and post rad I_D-V_G characteristics of three FinFETs with

channel lengths 50 nm, 70 nm and 130 nm are shown in Figure 8.13. As seen in bulk FinFETs, the highest increase in off-state leakage current is seen in the transistor with minimum channel length. This is because of the weakening of the back channel transistor with increasing channel length in SOI FinFETs.

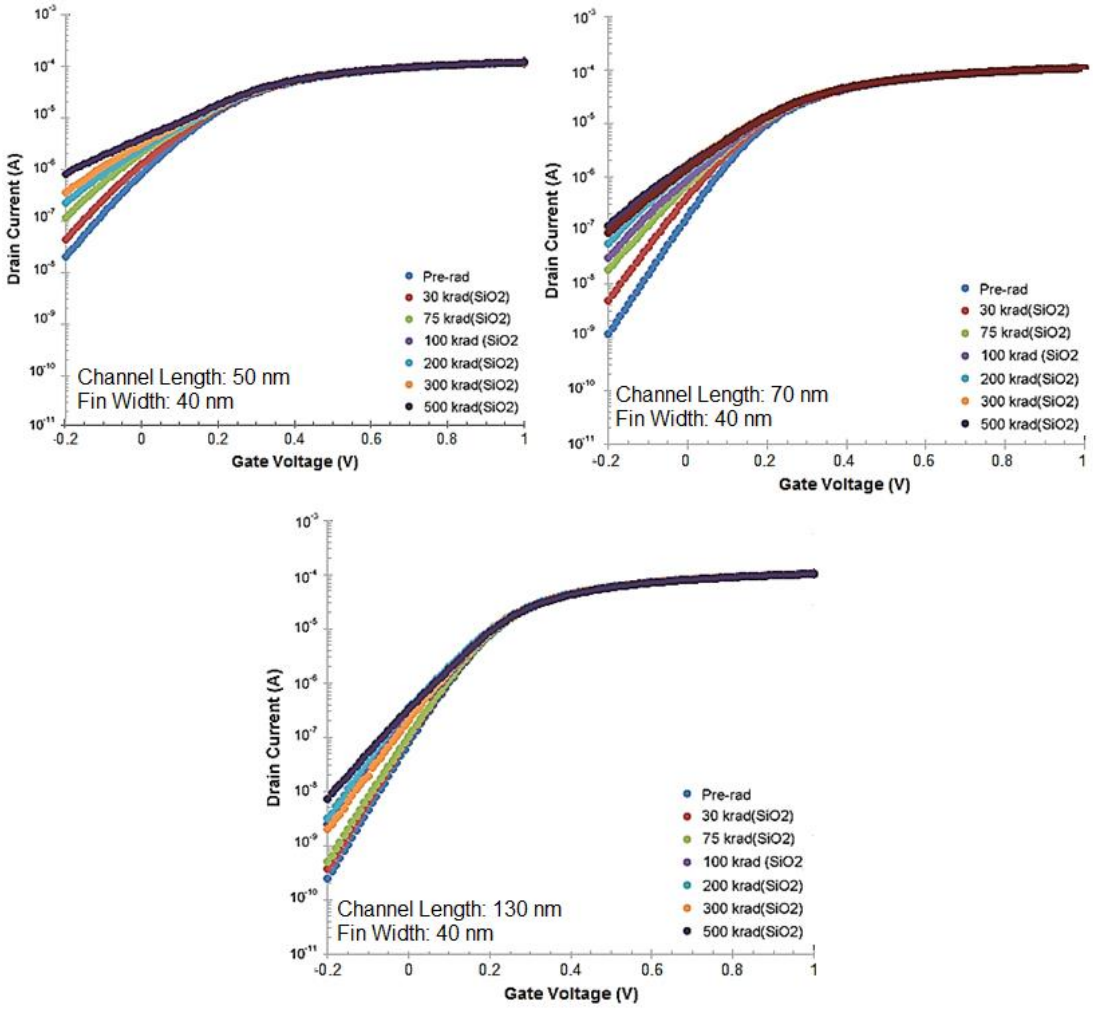


Figure 8.13: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 50 nm, 70 nm and 130 nm channel length transistors. The number of fins 5 and the fin-width is 40 nm.

8.2.3 TCAD Simulations

For channel length variation studies, 30 nm, 70 nm and 250 nm transistors were simulated. The fin width was 40 nm and the fin height was 35 nm. Figure 8.14 shows the electron density

(parasitic leakage) from the source to the drain for the three transistors. In bulk FinFETs, the parasitic channel induced by the trapped charge in the STI dominates the TID response. The current in this channel is inversely proportional to the channel length of the parasitic transistor. The trapped charge in the STI is independent of the channel length. Thus, the charge yield is the same for all three transistors under consideration. So, for the same amount of trapped charge in the isolation oxide, the parasitic transistor has a weaker drive in the long channel FinFET

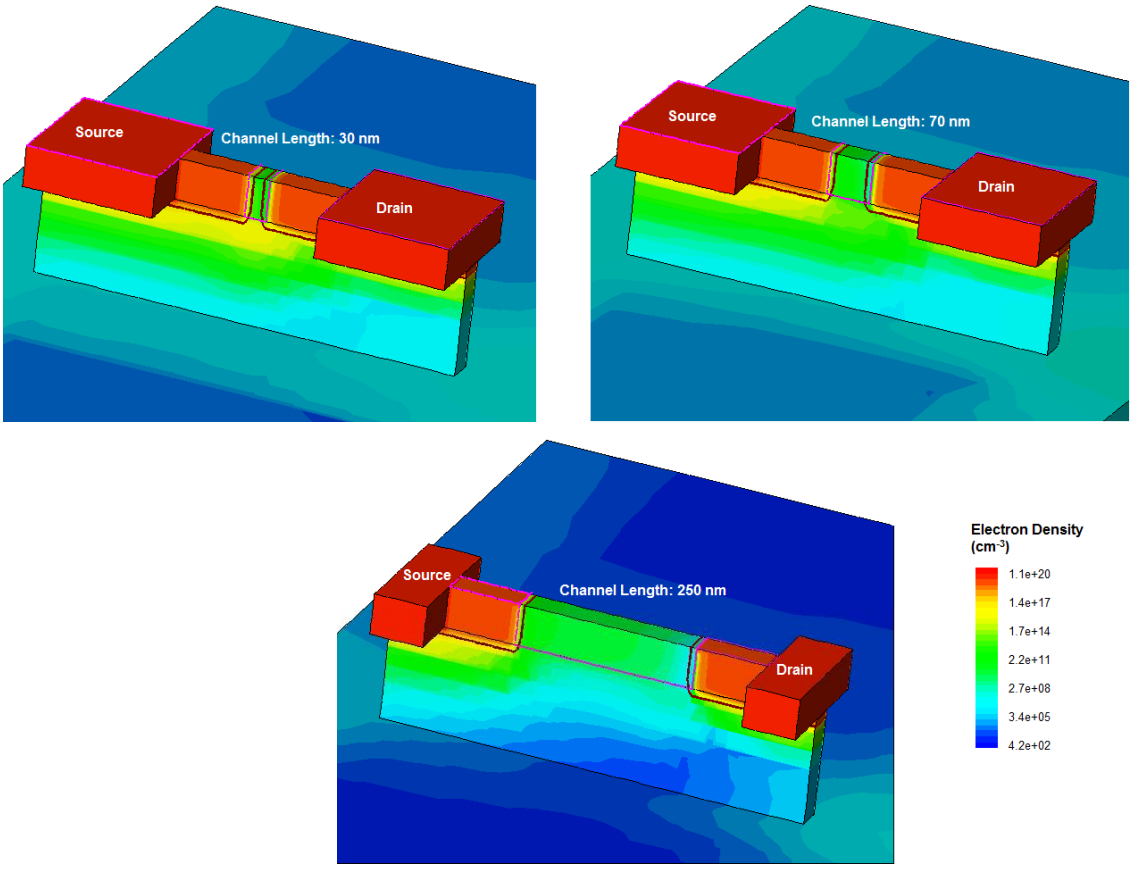


Figure 8.14: Illustration of the FinFET TCAD model showing the electron density (parasitic leakage path) from the source to the drain. The electron density is highest in the FinFET with 30 nm channel length. (After [Chat-14].)

compared to that in the short channel transistor. The off-state leakage current is highest in the 30 nm channel length transistor and the lowest in the 250 nm channel length device. Similarly for SOI FinFETs, the length of the back-channel does not influence the charge trapped in the buried

oxide. Thus for the same amount of trapped charge, the drive of the back-gate transistor is inversely proportional to the length of the back-channel transistor.

8.3 Pitch Variation

The fin-pitch is the minimum spatial period of multiple fins allowed by lithography at a particular technology node. Using spacer lithography, the pitch can be made as small as half of the lithography pitch. FinFET devices come in many flavors. In shorted-gate (SG) FinFETs, the two gates are connected together, leading to a three-terminal device. This can serve as a direct replacement for conventional bulk-CMOS devices. In independent-gate (IG) FinFETs, the top part of the gate is etched out, resulting in two independent gates. Because the two independent gates can be controlled separately, IG-mode FinFETs offer more design options. In IG-mode FinFETs, the front and back gates have a separate contact and, thus, the fin pitch needs to be increased to accommodate the back-gate contact. Consequently, the fin pitch in IG-mode FinFETs is greater than the fin pitch in SG-mode FinFETs [Alio-10]. Thus, it is important to study the effects of fin pitch on the TID response of bulk FinFETs.

8.3.1 Bulk FinFETs

Figure 8.15 shows the pre- and post-irradiation I_D-V_G characteristics of transistors with two different fin-pitches (200 nm and 1 μm) and Figure 8.15 shows the off-state leakage current vs. cumulative dose for the two types of devices. Figure 8.16 show the effective subthreshold swing. The TID-induced degradation decreases with decreasing pitch. Thus, with all other geometry and process parameters remaining constant, IG-mode FinFETs are likely to degrade more than SG-mode transistors. Similar experiments on SOI FinFETs show no dependence on fin-pitch.

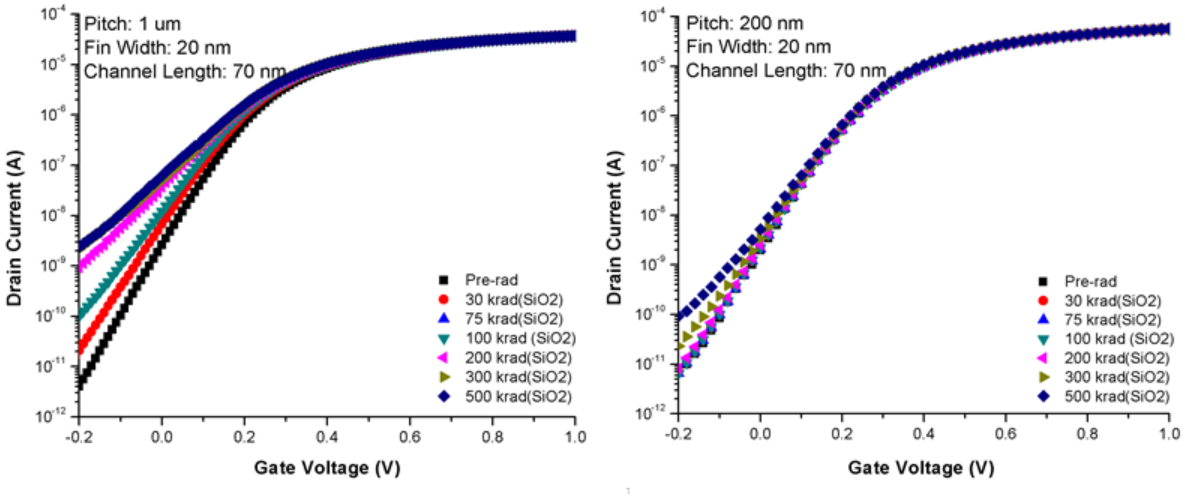


Figure 8.15: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 5-fin 70 nm channel length transistors with 200 nm and 1 µm pitch. (After [Chat-14].)

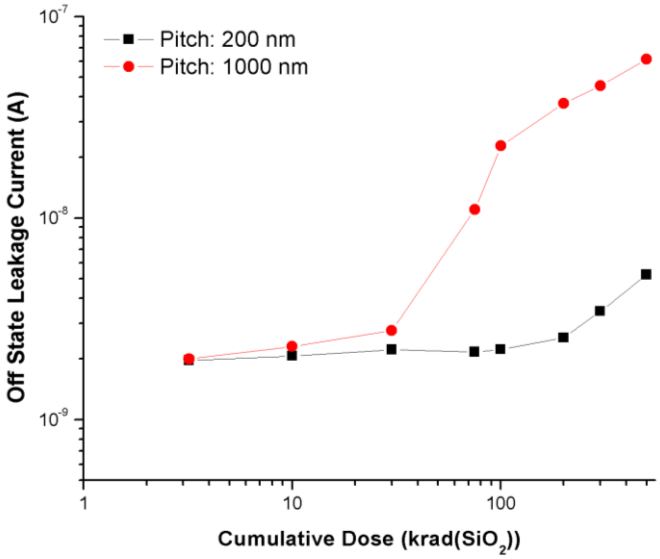


Figure 8.16: Off-state leakage current as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for a 5-fin 70 nm channel length transistors with 200 nm and 1 µm pitch. (After [Chat-14].)

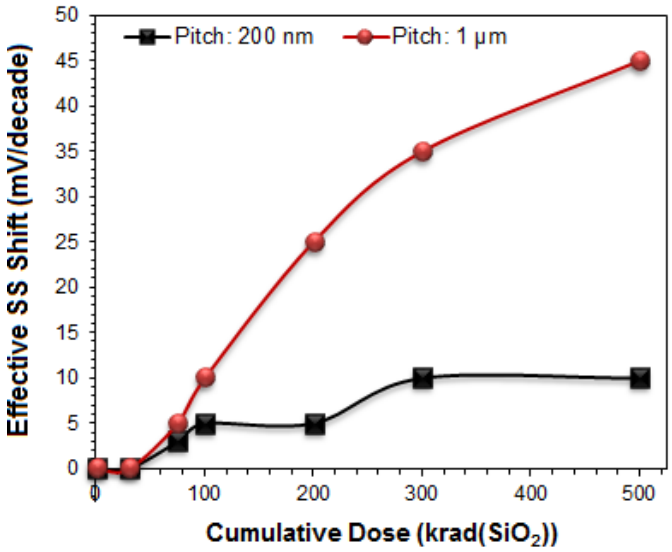


Figure 8.17: Effective subthreshold swing as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for a 5-fin 70 nm channel length transistors with 200 nm and 1 µm pitch.

8.3.2 SOI FinFETs

Pitch dependence is not observed in SOI FinFETs. This is expected as in SOI FinFETs, charge trapping in the BOX is the key issue and it is present in the entire wafer. Thus pitch in SOI FinFETs only changes the distance between two fins and has no impact on the BOX. Thus, the radiation-induced degradation in SOI FinFETs is independent of any change in the fin pitch. Figure 8.17 shows the I_D-V_G characteristics as a function of dose for SOI FinFETs.

8.3.3 TCAD Simulations:

For fin-pitch variation studies, two FinFETs with fin-pitches of 200 nm and 1µm were simulated. Figure 8.18 shows the electric field distribution in the isolation oxide between the fins. The cut is taken across the fin, as shown in the figure. The wider pitch leads to a greater effective thickness of the isolation oxide, which increases the amount of trapped charge in the STI [Shan-98], [Flee-13]. The electric field in the STI between the fins sweeps the charge towards the interface where it induces the parasitic channel as shown in Figure 6.3. The excess

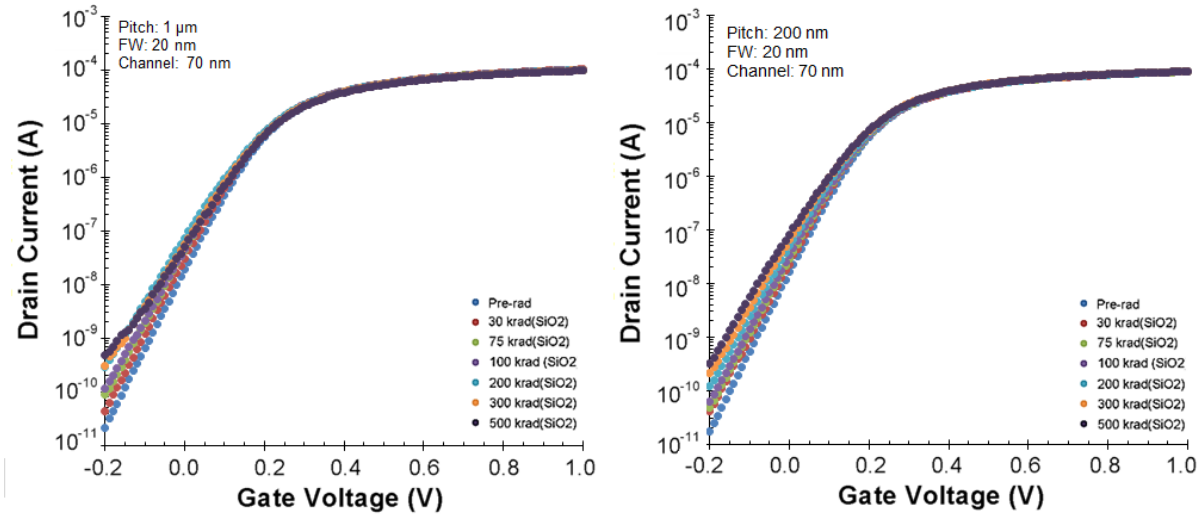


Figure 8.18: I_D-V_{GS} characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for 5-fin 70 nm channel length transistors with 200 nm and 1 µm pitch.

charge in the transistor with wider pitch results in a stronger parasitic transistor effect compared to the one with a 200 nm pitch. Thus the transistor characteristics are more affected in the FinFET with wider pitch.

8.4 Summary

Bulk FinFETs have a similar total ionizing dose response as planar bulk MOSFETs, i.e., the buildup of oxide-trapped charge in the STI triggers a parasitic lateral transistor that modifies the electrical characteristics (higher I_{OFF}). In this section, the geometry dependence of total ionizing dose effects on bulk FinFETs is presented. Three geometry variations are taken into consideration: fin-width, channel length and fin-pitch. The TID-induced degradation increases with decreasing fin-width. For thin-fin transistors, the radiation-induced charged traps in the STI are much closer to the middle of the channel and affect the channel electrical field more significantly than in the narrow-fin transistor. Channel length also plays a role in the TID-induced degradation, as transistors with longer channel length show less degradation because of the weakening of the current drive of the parasitic transistor induced by the charge trapped in the

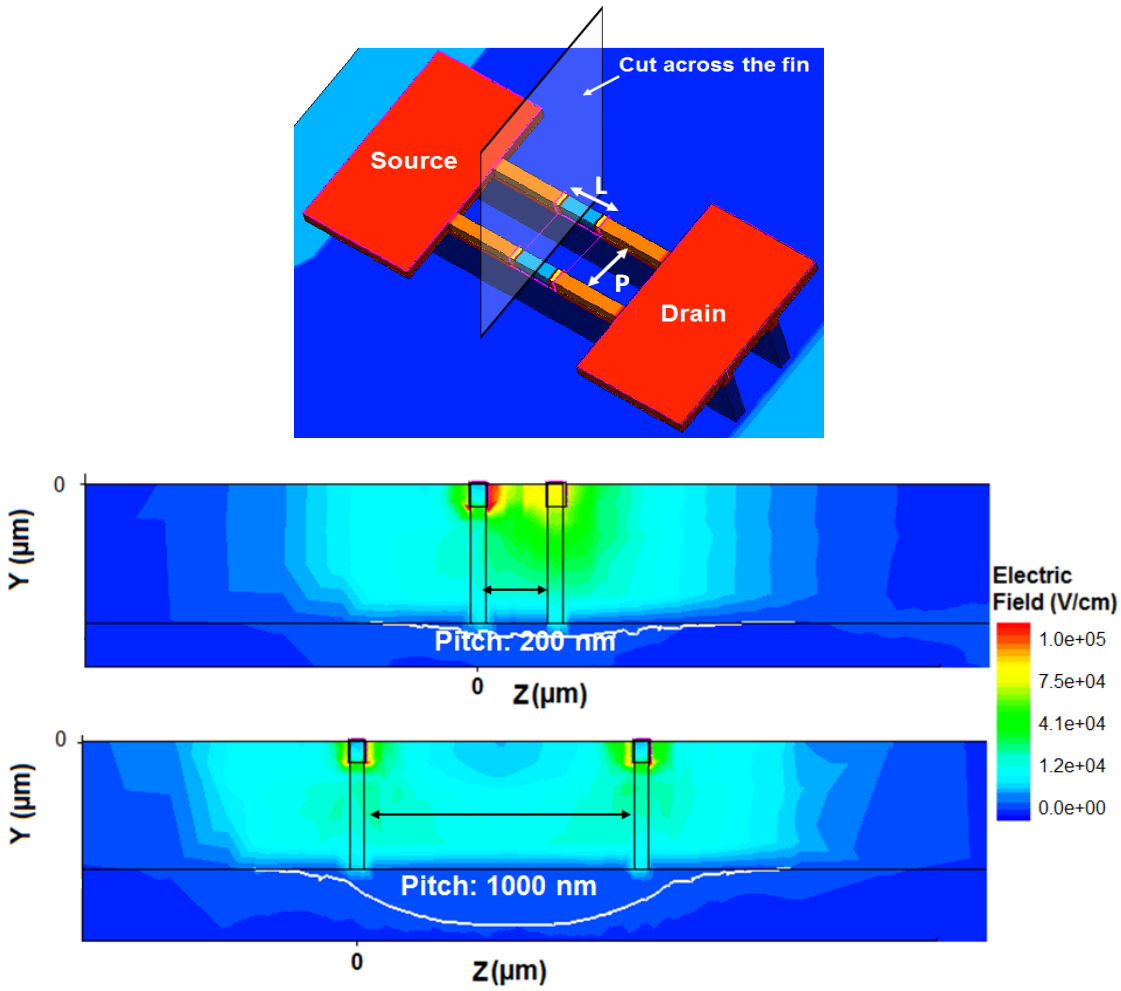


Figure 8.19: Illustration of the FinFET TCAD model showing the electric field in the STI between two consecutive fins (cut taken as in (a)). The field in the STI sweeps trapped charges close to the STI-fin boundary where it induces the parasitic channel. (After [Chat-14].)

isolation oxide. The larger the pitch, the more trapped charge in the STI contributes to degradation of the transistor characteristics. The trapped charge in the STI oxide induces a parasitic leakage current path that dominates the radiation response of bulk FinFETs. This is in contrast to the radiation response of SOI FinFETs, where the primary degradation typically occurs because of charge trapping in the buried oxide. 3D TCAD simulations were performed to understand the mechanisms behind the geometry dependence of total dose radiation response of these transistors. Degradation due to the ionizing radiation leads to increased leakage current and subsequent increase in power consumption.

CHAPTER IX

A TOTAL IONIZING DOSE HARDENING APPROACH IN BULK FINFETS

TID tolerance of SOI multiple-gate transistors with an optimized geometry is very promising. SOI FinFETs designed with narrow silicon fingers—the real optimized FinFET design— show intrinsic immunity to TID effects This geometry allows lateral gates to naturally mitigate potential parasitic effects induced by TID; the impact of trapped charges is mostly screened, and the effects of bias configuration during irradiation are reduced. These properties make SOI FinFET a strong candidate for embedded memory applications for nanometer scaled technologies [Zhan-10]. In contrast, bulk devices show an increased TID sensitivity for narrow devices. The TID response of bulk FinFETs is dominated by charge trapping in the STI. This leads to triggering a parasitic "lateral" transistor with increasing TID as observed in planar bulk MOSFETs. So, narrow bulk FinFETs are more sensitive to TID than wide bulk FinFETs. This may be an issue for bulk FinFETs since the narrow design is the most efficient architecture to enhance electrical performances by reducing short channel effects for advanced CMOS technology nodes.

An efficient method to make bulk FinFETs robust to total ionizing dose is to increase the doping at the bottom of the fin. In FinFETs, the channel region or the fin (both active fin and the inactive part) is undoped and any control over the threshold voltage relies purely on device geometry. It is in the inactive part of the fin, where the STI sidewall touches the fin and induces the parasitic leakage current path. Thus, by increasing the well doping, the parasitic channel formation can be hindered. At the same time, such an implant would help to reduce off-state leakage beneath the channel in a FinFET and this implant would not affect the threshold voltage

of the FinFET. However, the active part of the fin should be undoped as any implant in that region would lead to mobility degradation and random dopant fluctuations.

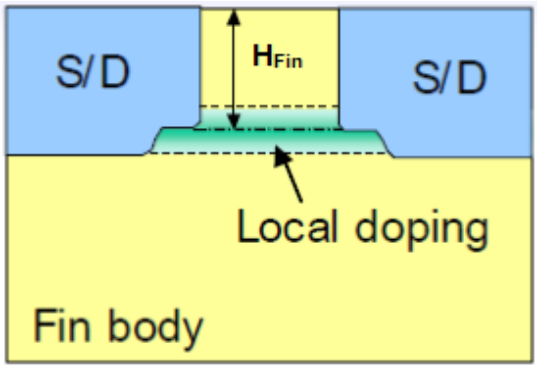


Figure 9.1: Conceptual schematic diagram of doping at the bottom of the fin, called local doping. (After [Lee-12].)

A 1-fin FinFET is evaluated for multiple well doping and the effect of the doping on the TID induced trapped charges. The fin width is 5 nm, the channel length is 50 nm and the fin-height is 35 nm. Figure 9.2 shows the off-state leakage current with respect to well-doping before and after incorporating a sheet of charge of concentration $10^{12}/cm^2$. It shows that the increase in off-state leakage current is significantly lower in case of the highest well-doping. Also, the increase in off-state leakage current with the incorporation of the trapped charges is also the lowest in the device with highest well doping. However, simulations show that the increased well-doping leads to a decrease in the drive current of the transistor by almost 16% between well doping of $10^{15}/cm^2$ to $10^{18}/cm^2$. Also, the simulations do not take into account the effects of mobility degradation and random dopant fluctuations. Thus, increasing the well doping reduces the as-processed off-state leakage and the radiation-induced leakage current but with the penalty of reduced current drive. The offset in drive current can be compensated by increasing the fin height which increases the current but does not affect the total-dose response of the devices.

Thus, a combination of the two can be an effective solution to maintaining the drive of the device and improving its radiation tolerance and decreasing static power consumption.

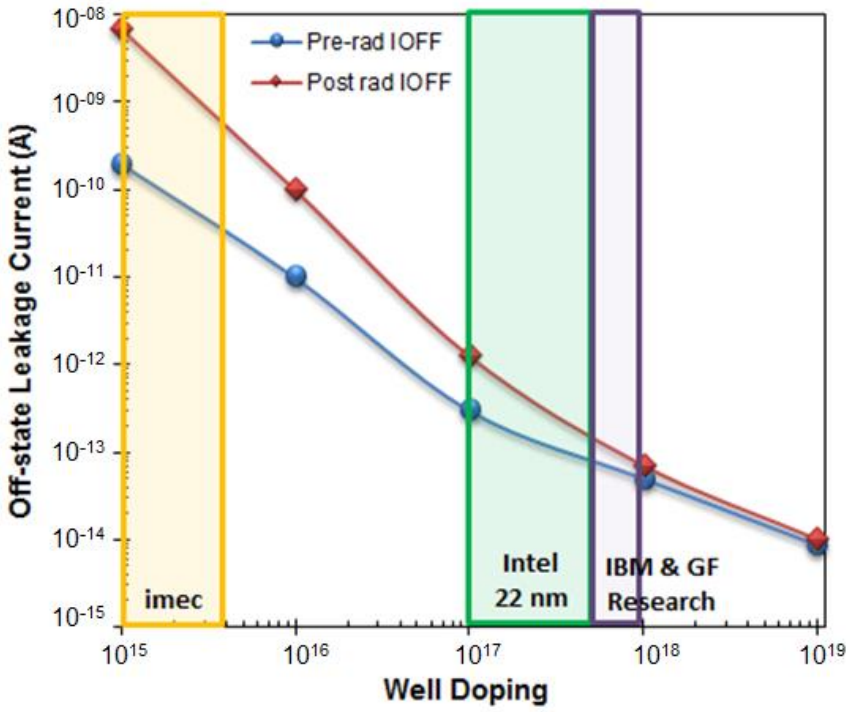


Figure 9.2: Off-state leakage current (pre-irradiation and post-irradiation) with respect to well doping in a 1-fin FinFET. (Doping information: After [Put-10], [Jan-12], and [Tech-12])

CHAPTER X

CONCLUSIONS

Electronic systems that are utilized in harsh environments such as in space or in terrestrial nuclear applications are designed to be tolerant to total dose damage and single-event upsets. In order to design such a system, a certain methodology has to be followed. First of all, the transistor technology used in the design of the integrated circuit has to be assessed. This implies that the radiation effects on this technology are studied qualitatively in test facilities which best simulates the radiation environment. The goal of this study is threefold: to identify the weak points of the technology in terms of radiation hardness, to determine the most radiation sensitive parameters of the technology and, finally, to find the physical mechanism behind the radiation-induced degradation, wherever this is possible. The next step in the design methodology is to utilize the knowledge obtained from transistor-level studies and combine them with circuit level effects. Further, if a radiation sensitive parameter of the technology is also important in the circuit design, an extensive statistical radiation study has to be carried out for this parameter. The goal of this study is to find the quantitative amount of degradation. The implementation of the statistical radiation behavioral model in a circuit simulation determines if the electronic circuit will operate inside the specification when subjected to the radiation field.

FinFETs are placed to be the workhorse of the industry for the coming few generations and thus in a few years, military and space technologies would adopt the use of these devices for the most advanced circuits and systems. This work provides an understanding of the various factors affecting the total ionizing dose response of bulk and SOI FinFETs. The main total dose degradation mechanism of the SOI FinFETs is the creation of positively charged holes trapped in

the buried oxide. These radiation-induced traps influence a parasitic transistor, located at the BOX of the SOI devices. It was found that the radiation behavior is more determined by the quality of the buried oxide (i.e. the a priori defect distribution in the oxide), than by the Si film thickness, especially for wide fin transistors, where degradation of the buried oxide can have a detrimental influence. For the SOI FinFET studies, only damage related to radiation-induced charges at the buried oxide was found, affecting the back inversion channel. This, in turn, influences the off-state leakage current of the devices. For narrow fin devices, radiation-induced damage is negligible and thus are prospective candidates for the next generation of radiation-hardened devices.

In contrast, for bulk FinFETs, the charge trapped in the shallow trench isolation offers a parasitic sub-surface leakage path below the active fin. This affects the dependence of the radiation hardness on the fin width: radiation tolerance decreases with decreasing fin width. Both SOI and bulk FinFETs degrade more with decreasing channel length. An effective way to reduce the radiation-induced degradation in bulk FinFETs is by increasing the doping of the well. This method can be used to reduce the as-processed leakage of the transistor as well as hinder the formation of the parasitic transistor by the radiation-induced trapped charge in the isolation oxide. This leads to reduced static power dissipation and enhanced TID tolerance of bulk FinFETs.

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