A Fully Embedded Silicon On Insulator Total Ionizing Dose Monitor

By

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1. Introduction

1.1 Total Ionizing Dose effect

For space applications, microelectronics has to face the harsh space radiation environment [1-2]. It includes trapped electrons, trapped protons, solar events and galactic cosmic rays (GCR). When exposed to these types of radiations, various radiation effects can occur in devices and circuits, which could degrade performance and even cause failures. One of the most important radiation effects, Total Ionizing Dose (TID) is related to charge build up in oxides, which is a big concern for microelectronic long-term reliability.

1.1.1 Basic Mechanisms

High-energy charged particles are able to ionize atoms, generating electron-hole pairs. The average electron hole pair generation energies in Si and SiO_2 are $3.6eV$ and $17eV$ respectively. When a MOS transistor is exposed to high-energy radiation, electron-hole pairs will be created in the oxide. **Figure 1** shows a MOS band diagram for a p-substrate capacitor with a positive gate bias [4].

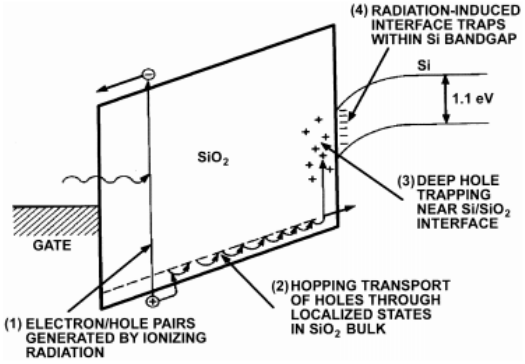


Figure 1 Main process of the ionization-induced charge generation in p-substrate MOS capacitor[4]

Under the ionizing irradiation, many processes happen in the oxide. First electron-hole pairs are created in the SiO_2. However, because of the higher mobility, electrons move out of SiO_2 faster than holes. But in the first picosecond, some fraction of generated electrons and holes recombine [4]. This fraction is highly dependent on the applied electric field and the incident particle types. The surviving holes determine the initial response after a short pulse of irradiation. Second, holes that escape the recombination will transport to the Si/SiO_2 interface by the continuous-time-random-walk (CTRW) hopping transport mechanism [5]. This process determines the short-term recovery of MOS devices.

Thirdly, as the holes moves near the Si/SiO_2 interface, some of them will fall into the deep traps [6]. The fraction could be as low as 1% in radiation-hardened oxides and as high as 50% in unhardened commercial oxides. The few holes that are trapped produce a remnant threshold voltage shift, which is some fraction of the initial shift. Then these trapped holes undergo a long term annealing process, which has roughly $\ln(t)$ dependence.

The fourth process is the build up of radiation-induced interface traps. These traps are localized states with energy levels in the Si band gap. Their occupancy is determined by the Fermi level, which gives rise to the voltage-dependent threshold voltage shift. **Figure 2** shows the threshold voltage shift corresponding to each process presented above.

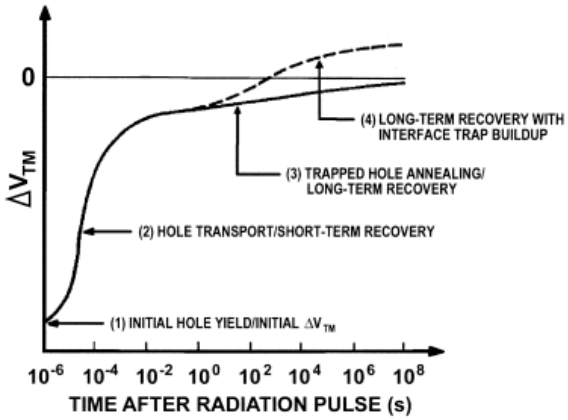


Figure 2 Schematic time-dependent post irradiation threshold voltage recovery of n-channel MOSFET, relating major features of the response to underlying physical processes [4]

1.1.2 Traps

There are oxide traps and interface traps in SiO_2. Their charge states will be different in different conditions. In SiO_2, there are oxygen vacancies due to the out-diffusion of oxygen in the oxide [4, 7]. The oxygen vacancy leaves a weak Si-Si bond, where each Si atom is back-bonded to three oxygen atoms as shown in **Figure 3**. These oxygen

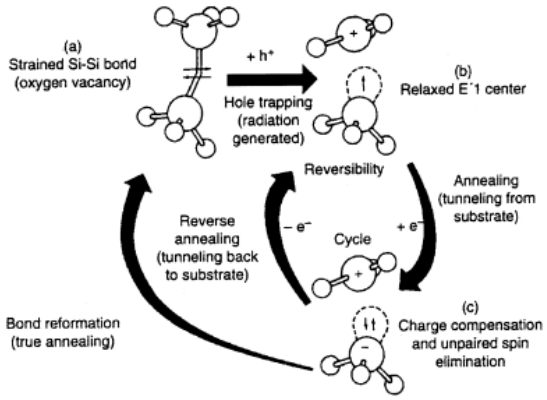


Figure 3 Model of hole trapping, permanent annealing, and compensation process [4]

vacancies act like trapping centers, and they are called E' center. When holes approach the centers, they may be trapped. The number of trapped holes is determined by the capture cross section of the trapping center.

Trapped holes are relatively stable, but they undergo a long-term annealing process by two mechanisms: tunneling and thermal excitation, as shown in **Figure 4**[8]. The electrons

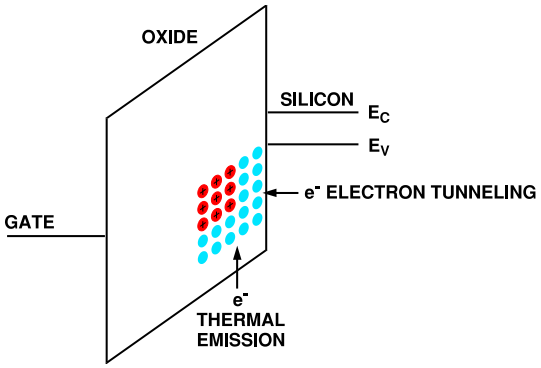


Figure 4 Band diagram of MOS transistor showing two mechanisms for the neutralization of oxide traps [8]

from the Si substrate tunnel through the barrier and get neutralized at or near room temperature. This neutralization depends on the trap spatial distribution. In this condition, thermal excitation remains negligible compared with the tunneling. However, if the temperature increases enough, the thermal process will eventually dominate. The electrons from the oxide valence band may be excited into the oxide traps and this process relies on the spatial and energy distribution of the traps.

The buildup of interface traps is a different process. Many models are proposed for the mechanism, but the most robust and convincing model is two-stage hydrogen model [4]. First, radiation-induced holes transport through the oxide and free hydrogen, in the form of protons. In the second stage, the protons undergo hopping transport. When they reach

the interface, they react with SiH bonds there, forming H_2 and dangling bonds as shown below [9].

$$H^+ + SiH \rightarrow H_2 + D^+$$

where SiH bonds represent a Si atom bonded to a hydrogen atom and back bonded to three Si atoms, while D^+ denotes the Pb center (the interface trap), which is a Si atom with a dangling bond back bonded to three Si atoms. Figure 5 below shows the above reaction processes.

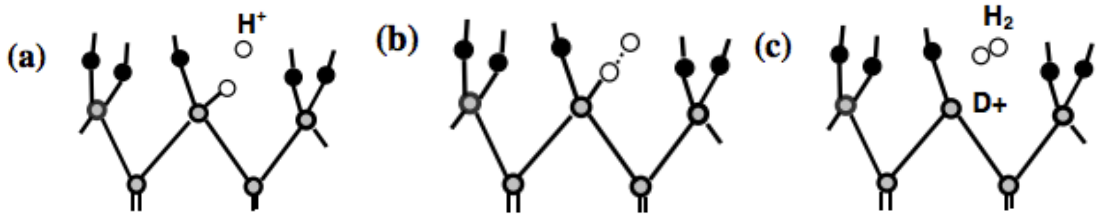


Figure 5 Reaction between H+ and SiH bond: (a) a proton approaches the SiH bond; (b) a H+ and -H-Si "bridge" is created; (c) an H2 molecule and D+ trap are formed [9]

Unlike the oxide traps, which are always positive, the interface trap charge states are not fixed [3]. The charge state can be determined by the following reasoning. When the Fermi level is at the midgap level, the interface trap charge is approximately neutral. Traps in the lower portion of the bandgap are donor-like, while those in the upper portion are acceptor-like. Donor-like traps, are neutral when occupied by an electron, and positive when empty. Similarly, acceptor-like traps, are neutral when empty and negative when an electron is trapped. So when the Fermi level is below the midgap level, the donor-like traps would "donate" an electron and become positive. Therefore for p-channel transistors, the interface traps are predominantly positive when the device is biased at threshold. Conversely, when the Fermi level is above the midgap level, the

acceptor-like trap receive an electron, resulting in the negatively charged state. Therefore, for n-channel transistors, the interface traps are predominantly negative at threshold.

1.1.3 Issues with TID effect

TID effects degrade device performance. Here two main effects are discussed: threshold voltage shift and radiation-induced leakage current.

1.1.3.1 Threshold Voltage Shift

There are four types of charges existing in the oxide, as shown in Fig. 6 [10]. They are mobile ionic charge Q_m, fixed oxide charge Q_f, oxide trapped charge Q_{ox}, and interface trapped charge Q_{it}. For the radiation situation considered here, only Q_{ox} and Q_{it} are considered.

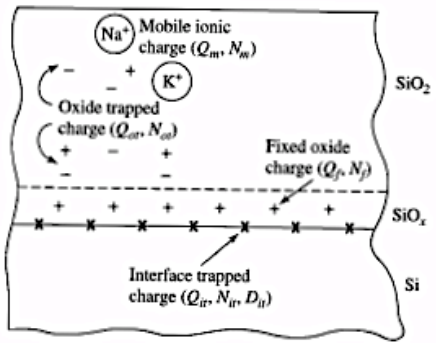


Figure 6 Oxide charges in SiO2 and Si system [10]

The threshold voltage shifts due to the oxide charges and interface charge buildup [10].

$$\Delta V_{th} = -\frac{Q_{it}}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} x \rho_{ox}(x) dx \quad \textbf{(1)}$$

where C_{ox} is the oxide capacitance, ε_{ox} is the oxide dielectric constant, $\rho_{ox}(x)$ is the oxide traps charge density. It shows that the oxide traps cause negative threshold voltage shift,

while the behavior of the interface traps has to be determined according to their charge states.

Table 1 summarizes these results for NMOS and PMOS transistors. For PMOS transistors, the charge in the oxide traps and interface traps add together, giving rise to more negative threshold voltage shift. However, for NMOS transistors, the oxide traps and interfaces traps have opposite polarities, so the threshold voltage shifts tend to cancel each other, rendering an undetermined result.

	Q_{ox}	Q_{it}	ΔV_{ox}	ΔV_{it}	$\Delta V_{th} = \Delta V_{ox} + \Delta V_{it}$
NMOS	+	-	-	+	?
PMOS	+	+	-	-	-

Table 1 traps charge states and corresponding effect in the threshold voltage shift, "+" represents positive voltage shift, "-" denotes negative voltage shift, and "?" represents undetermined.

There is another noteworthy point about the difference between oxide and interface traps. Because interface traps lie in the bandgap of Si, the occupancy of interface traps is voltage dependent. However the oxide traps do not have this dependence. This difference enables us to separate the contributions of oxide and interface traps to the threshold voltage shift [11].

It's also very important to know the relationship between the oxide thickness and threshold voltage shift. It's generally believed to have a square law dependence [12].

$$\Delta V_{th} = \frac{Q_{ot}}{C} \propto t_{ox}^2 \qquad \textbf{(2)}$$

Because trapped hole density Q_{ot} is approximately proportional to the oxide thickness, while the gate capacitance is inversely proportional to the oxide thickness. So the threshold voltage shift shows the square law dependence. As technology scales, the gate oxide thickness is getting thinner and thinner, so the net hole trapping becomes very small. As a result, the scaling is the best hardening technique in terms of the TID effect.

1.1.3.2 Leakage Current

Another important issue with TID effects is the radiation-induced leakage current (RILC) [3]. With the ultra-thin gate oxide, the electrons from the Si substrate could tunnel through the barrier into the gate oxide. Defects created by radiation-induced damage could contribute to the gate current.

The Field Oxide (FOX) plays an important role in increasing the leakage current under TID irradiation [3]. Though the gate oxide makes a negligible contribution due to its ultra-thin thickness, the FOX remains relatively thick. As a result, a lot of charge buildup in the FOX, gives rise to undesirable results.

Two common FOX isolation methods are local oxidation of silicon (LOCOS) and shallow trench isolation (STI). And LOCOS has been replaced by STI in the submicron

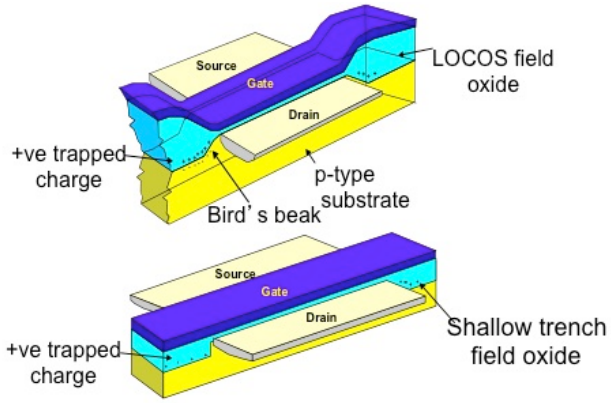


Figure 7 Transistor cross section with LOCOS and STI isolation [3]

technology. **Figure 7** shows the cross section of LOCOS and STI isolation, and it illustrates the charge buildup in the LOCOS bird's beak regions and in STI. For p type substrate, the charge buildup in the FOX could invert the surface and create an n-channel underneath the FOX, thus forming a parasitic field-oxide transistor in parallel with the gate-oxide transistor. The parasitic field-oxide transistor contributes the edge leakage.

Figure 8 shows the leakage paths for a 2 input NAND gate. As shown in the figure, there are three main leakage paths. The first is the leakage path under the FOX between N-channel source and N-well. The second is the edge leakage where the thin gate oxide is in transition to FOX. The third is the leakage between the drain output of one NAND to the source of the adjacent NAND gate.

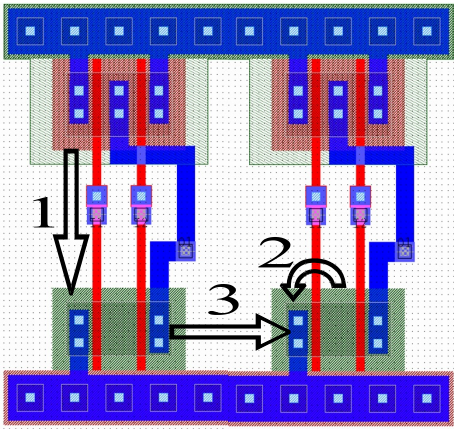


Figure 8 2 input NAND gates showing the leakage current paths

Because of the predominantly positive charge buildup in the oxide, the FOX leakage is the most serious in NMOS transistors. To sum up the radiation-induced leakage, **Figure 9** shows the gate oxide transistor leakage current caused by the field-oxide transistor. Because of the large thickness of the FOX, the pre-irradiation threshold voltage of the parasitic field oxide transistor is relatively large, and it has a large threshold voltage shift due to the large charge build up in the FOX. Even though the contribution from the gate oxide transistor is small, the total leakage current is significant.

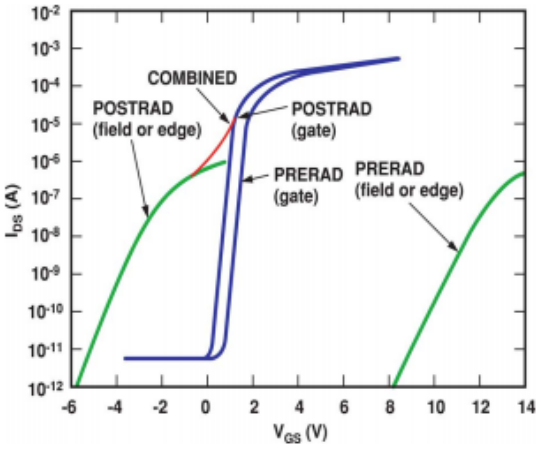


Figure 9 I-V curve for a gate oxide transistor and a parasitic field-oxide transistor showing the increase in leakage current of the gate oxide transistor caused by the parasitic field-oxide transistor [3]

1.2 Silicon On Insulator (SOI) Technology

The use of SOI has been motivated by the full dielectric isolation of individual transistors. Only the very top region of the silicon wafer is used for carrier transport in bulk CMOS, while more than 99.9% of the wafer is used as a mechanical support of the active device [13]. However, the inactive volume causes undesirable effects such as the substrate coupling. SOI technology comes from the idea of separating the active volume from the silicon substrate by a thick insulator.

SOI technology is receiving more and more attention because of its advantages over conventional bulk CMOS technology. First, it is immune to latchup due to the isolation between active volume and substrate. Second it increases performance by raising the integration density and decreasing the source and drain junction capacitance. Finally, it provides radiation hardness for space and military applications [14].

1.2.1 SOI Transistor Structure

There are planar and non-planar SOI transistors [14]. For illustration purpose, only the planar SOI transistors are considered. Two types of planar SOI transistors are commonly used: the fully depleted (FD) and partially depleted (PD) transistors [13] as shown in **Figure 10**. For the FD SOI transistor, the silicon body is fully depleted, while the silicon body is only partially depleted, leaving a neutral body for the PD SOI transistor.

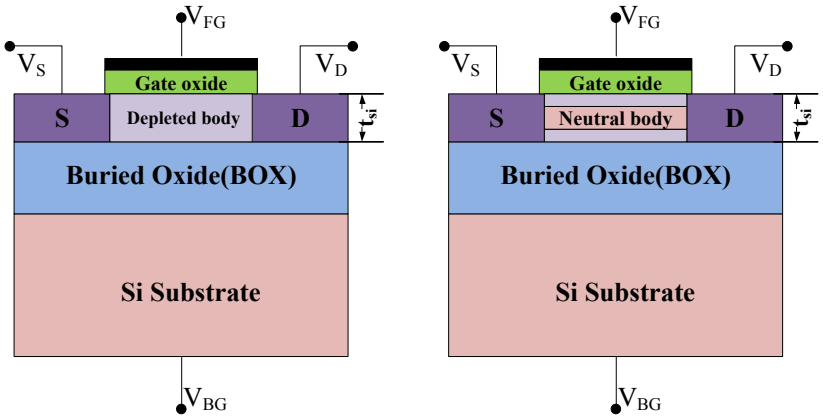


Figure 10 Two types of SOI transistors: (a) FD SOI transistor; (b) PD SOI transistor

For a SOI transistor, except for the thin gate oxide transistor, called the front gate transistor, there is a parasitic transistor formed by the thick buried oxide (BOX) and the silicon substrate, which is called back gate transistor. BOX is unique for SOI technology, which is used to isolate the active volume and the silicon substrate. And it plays an important role in the TID response of SOI technology.

Both the front gate transistor and the back gate transistor will deplete the silicon body, so if the body is thin enough such that

$$t_d(FG)+t_d(BG)\geq t_{si} \tag{3}$$

where $t_d(FG)$ is the depletion layer thickness of the front gate transistor, $t_d(BG)$ is the back gate transistor depletion layer thickness, and t_{si} is the silicon island thickness as shown in **Figure 10**. Then the SOI transistor is a FD SOI transistor, otherwise it is a PD SOI transistor. Here the difference of FD SOI and PD SOI transistors is emphasized because of their different behavior. For a FD SOI transistor, there is a strong coupling between the front gate and back gate transistors due to the fully depleted body region.

As mentioned above, there is a parasitic back gate transistor in every SOI front gate transistor. However, in addition, there is also a parasitic bipolar transistor in a PD SOI transistor [13]. The neutral body acts as the base, while the source and drain act as emitter or collector. This parasitic bipolar structure could be triggered by proper bias or radiation. **Figure 11** shows the equivalent electrical structure of a PD SOI transistor.

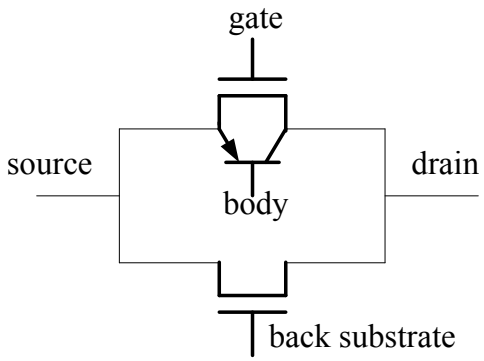


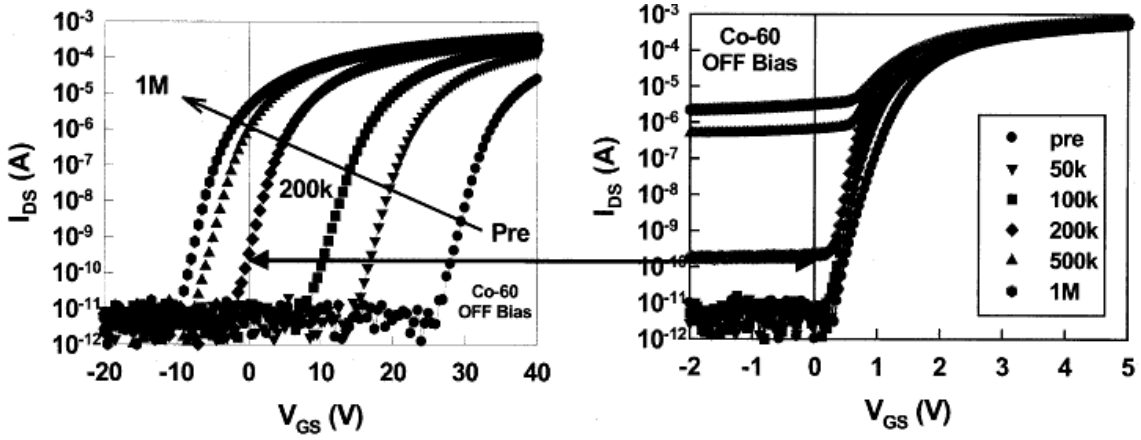
Figure 11 Equivalent electrical structure of a PD SOI transistor [13]

1.2.2 TID Effect in SOI Transistors

Compared with their bulk counterparts, what is unique in SOI technology is the BOX, which is a big concern for TID effects. The charge traps in the BOX include the E' and P_b center as in the bulk transistor; however the BOX also has other types of traps, for example, the delocalized spin center, where the unpaired electron does not belong to any particular atom. [13]. The traps are highly fabrication process dependent [15-16].

The oxide charge buildup will cause the threshold voltage shift and leakage current increase. However, PD SOI and FD SOI transistors have some different responses for TID effects. The difference is examined below.

The primary effect of radiation-induced charge buildup in the BOX of PD SOI transistors is to increase the leakage current of the front gate transistor and threshold voltage shift in the back gate transistor. This is illustrated in Figure 12 [13]. From the Figure 12(a), the positive charge buildup in the BOX causes large negative threshold voltage shift in the back gate transistor. As the charge buildup is large enough to cause an increase in the leakage current at zero back-gate bias, the front gate leakage current will begin to increase, as shown in Figure 12(b).



(a) (b)

Figure 12 I-V characteristics for: (a) a back-gate transistor irradiated to 1Mrad (SiO2) and its effect on (b) the front gate transistor leakage current. The transistors were irradiated in the OFF ($V_{GS} = V_S = 0; V_{DS} = 5V$) bias condition [13]

Due to coupling effects, the FD SOI transistor TID response is more complicated. The front gate transistor is electrically coupled with the back gate transistor and charge trapping in the BOX will directly affect the front gate transistor characteristics [13]. Basically, the charge buildup in BOX will cause the increase of leakage current and threshold voltage shift both in the front gate transistor and back gate transistor [13,17-18].

Figure 13 shows the comparison between fully and partially depleted devices in terms of the threshold voltage shift under irradiation [13]. The partially depleted device shows negligible front gate threshold voltage shift while the fully depleted device shows nearly linear coupling between the front gate and back gate.

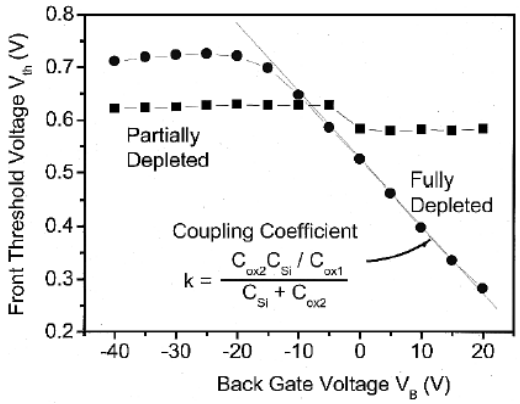


Figure 13 Front gate transistor threshold voltage versus back gate bias for floating body fully and partially depleted 0.25um NMOS depended on C_S the fully depleted silicon film capacitance, C_{ox1} the front gate oxide capacitance, C_{ox2} the back gate oxide capacitance [18].

The TID effect of SOI transistors due to the BOX charge buildup is summarized in **Table 2** below.

	$\Delta V_{th,FG}$	$\Delta V_{th,BG}$	$I_{leakage,FG}$	$I_{leakage,BG}$
PD SOI transistor	×	√	√	√
FD SOI transistor	√	√	√	√

Table 2 PD and FD SOI transistors TID response: $\Delta V_{th,FG}$ the front gate transistor threshold voltage shift, the $\Delta V_{th,BG}$ back gate transistor threshold voltage shift, $I_{leakage,FG}$ the leakage current increase in front gate transistor, $I_{leakage,BG}$ the leakage current increase in back gate transistor

2. TID Effect Monitor

There are many kinds of radiation detectors, such as quartz fiber dosimeter, film badge dosimeters, and thermoluminescent dosimeters [19-20]. But in this chapter, only different kinds of solid-state TID monitors are examined [21-28]. Their working principles, advantages and disadvantages will be compared. Finally a design of an embedded SOI TID monitor is presented.

Almost all the literature about radiation dose detectors falls into one category: utilizing the radiation induced threshold voltage shift. The mechanism of this threshold voltage shift has been introduced in Chapter 1. However, from Chapter 1, except for the threshold voltage shift, there is another important aspect of TID effects, the increase of leakage current. Next, these two different aspects are illustrated.

2.1 Threshold Voltage Shift Approach

Threshold voltage shift is the most straightforward method quantifying radiation-induced changes in a MOS device. Based on this idea, different methods have been put forward. Here two main methods are illustrated: discrete PMOS radiation sensitive field effect transistor (RADFET) [21-25] and an on-chip CMOS circuit [26-28].

2.1.1 Discrete PMOS RADFET

The use of a PMOS RADFET to measure the total dose irradiation level was first suggested in the 1970s by Holmes-Siedle [28]. The principle of this monitor is illustrated as below. As

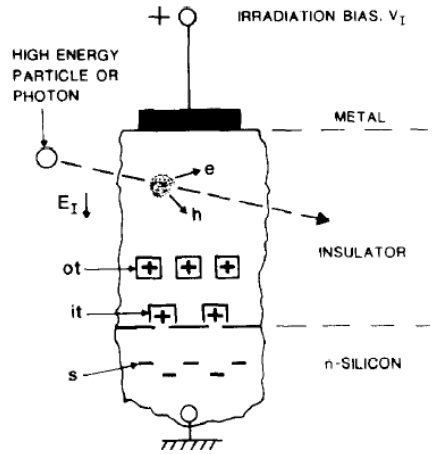


Figure 14 Cross section of a MOS capacitor under irradiation, "ot" represents the oxide traps, "it" represents interface traps, and "s" represents semiconductor image charge [22]

shown in **Figure 14**, the radiation will introduce positive charge buildup in the oxide and at the interface for a PMOS transistor. The effect of the oxide traps and interface traps will add together, which is the reason of the selection of a PMOSFET, instead of a NMOSFET as the RADFET. It's already known that the charge buildup will cause negative threshold voltage shift in PMOS. Thus, by measuring the threshold voltage shift; and from the relationship between the total dose irradiation level and threshold voltage shift, we can monitor the irradiation level.

The circuit that measures the threshold voltage shift is shown in **Figure 15** [22]. During irradiation all terminals are grounded; however during the sensing measurement, the gate and drain are connected together, and the source and body are connected to a constant current source. Because drain to source current is fixed, the source to drain voltage change is equal to the threshold voltage shift

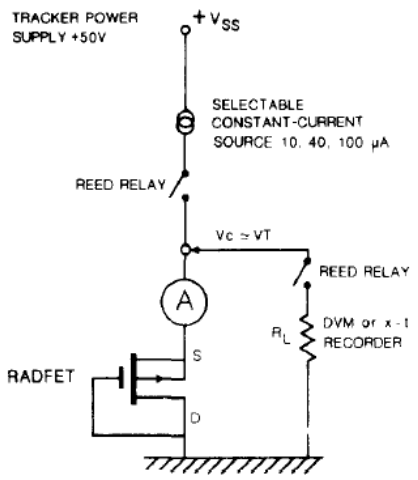


Figure 15 A type of read circuit for PMOS RADFET [22]

It is shown in section 1.3.1.1 that the threshold voltage shift is proportional to the square of the oxide thickness. Now define the sensitivity as

$$S = \frac{\partial \Delta V_{th}}{\partial D} \tag{4}$$

here ΔV_{th} is the threshold voltage shift, and D is the total dose. Then it can be concluded

$$S \propto t_{ox}^2 \tag{5}$$

So to obtain high sensitivity, the oxide thickness should be made large. This requirement makes it impossible to integrate the PMOS RADFET in present-day commercial technology.

The monitor above works well. However, to reduce the effect of annealing and fading of trapped holes in the oxide, a dual-dielectric PMOS RADFET is suggested [24-25]. Illustrated in **Figure 16** is the cross section of the proposed RADFET. The dielectric layers contain one layer of SiO_2, and on top of it is one layer of Si_3N_4.

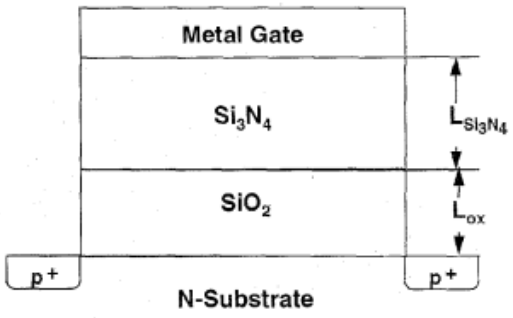


Figure 16 Cross section of dual-dielectric PMOS RADFET [24]

For a single dielectric, to get substantial threshold voltage shift, positive gate bias is applied during irradiation so that holes move to the Si/SiO_2 interface instead of to the gate/SiO_2 interface. However this would also increase the chance of trapped holes neutralization. The PMOS RADFET shown in **Figure 16** resolves this issue. During irradiation, negative gate bias is applied so that generated holes move to the Si_3N_4/SiO_2 interface. As a result, little or no interface trap buildup and hole neutralization by electron tunneling occurs [24].

In order to improve the linearity of sensitivity as a function of total accumulated dose and minimize the temperature dependence, a differential type of RADFET is proposed [29]. The schematic is shown in **Figure 17**. By measuring the threshold voltage shift of each transistor in the sensor pair and calculating the difference of the two threshold voltage shifts, the performance could be improved considerably.

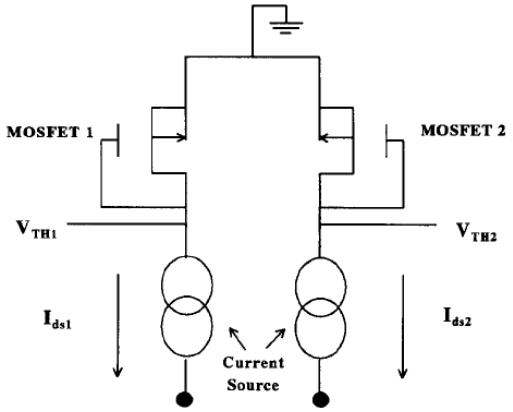


Figure 17 Read out circuit for the threshold voltages V_{TH1}, V_{TH2} of each MOSFET in the sensor pair[29]

In the end, the advantages and disadvantages of the discrete PMOS RADFET detector are summarized. First, it is easy to build and very straightforward. In addition, it could receive a large range of dose. However, the main drawback is that it could only be integrated with relatively thick oxide technologies. As technology scaling continues, it is impossible to integrate into present-day ultra-thin gate oxide technologies.

2.1.2 On-Chip CMOS Circuit

Several types of solid-state circuits could be used to monitor the total dose level. Some of them only provide a dose threshold, which only gives very limited information about the total dose [26]. Some of the circuits can measure the threshold voltage shift in situ [27-28]. These circuits are introduced below briefly.

The total dose switch is a type of circuit that only provides a dose threshold [26]. When the total dose reaches this threshold, the circuit switches its state. **Figure 18** shows the schematic of the circuit. In the circuit, only Q_1 is sensitized to radiation and the other transistors are radiation hardened. When the total dose is below the threshold, Q_1 remains

"ON", and the output is low. However, once the total dose reaches the threshold, Q_1 turns off, then the output goes high. So by observing the output state, the total dose information could be gathered. However this is a kind of "binary" information, and it is quite limited.

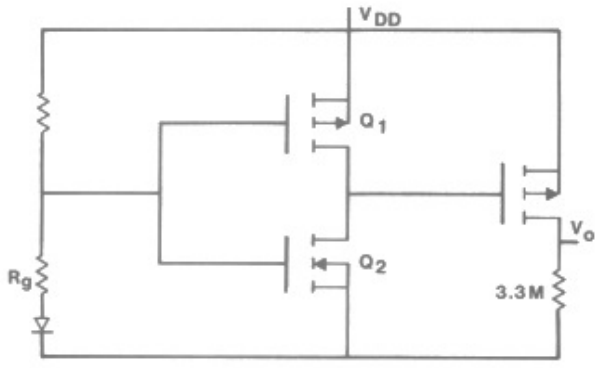


Figure 18 Circuit for use as a total dose switch [26]

Another type of solid-state circuit TID monitor could be borrowed from the negative bias temperature instability (NBTI) monitor. NBTI is characterized by a positive shift in the absolute value of the PMOS threshold voltage, which occurs when a device is biased in strong inversion [27]. This threshold voltage shift is due to the breaking of Si-H bonds at the oxide interface. The dangling bonds are Pb centers (Section 1.1.2) and they are positive for PMOS transistors. Because TID effect and NBTI have the same result, the positive absolute threshold voltage shift, NBTI monitors could be "borrowed" to build a TID monitor. Here one such design is presented.

This NBTI monitor is based on a delay locked loop (DLL). **Figure 19** is the block diagram of the NBTI monitor [27]. The voltage controlled delay line (VCDL) shown in the diagram is composed of stressed stages and unstressed stages. The stressed stages are biased by V_{const} which is constant, while the unstressed stages are biased by $V_{control}$, which

is the output of a loop filter. The basic idea of this circuit is to translate the stressed stage threshold voltage shift into $V_{control}$. Then by measuring the change of $V_{control}$, the threshold voltage shift can be calculated by the relationship between $V_{control}$ and $|\Delta V_{th}|$.

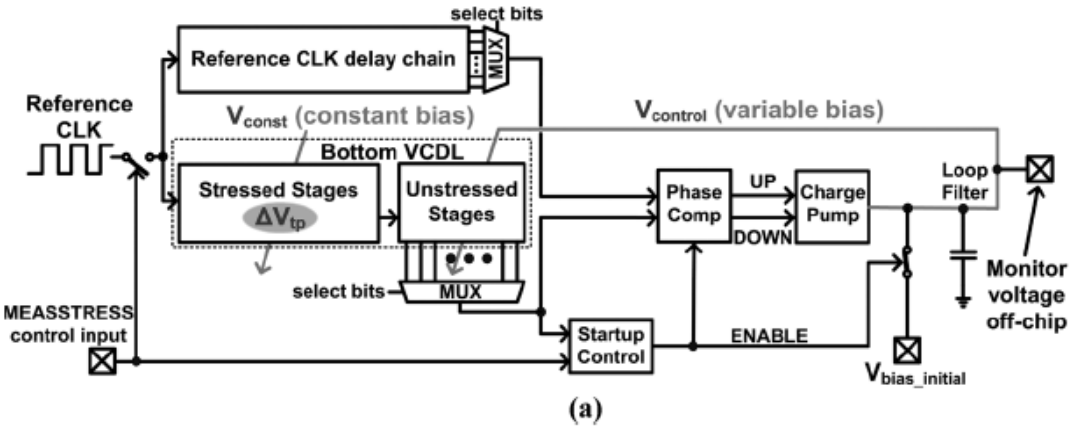


Figure 19 Block diagram of NBTI monitor [27]

This type of NBTI monitor could be used in a TID monitor design. It could give the in-situ result of the threshold voltage shift, which could be translated into the total dose level. However, the circuit is complicated and requires fitting between the relevant parameters. This could result in considerable errors.

2.2 Leakage Current Approach

A TID monitor based on leakage current was first implemented in [30]. This paper shows the feasibility and the advantage of this kind of TID monitors over the threshold voltage shift based monitors. However, to be able to fully integrate with the standard CMOS technology, SOI technology is used here. Due to its thick buried oxide, it is a reasonably good candidate for this application.

Standard methods used to fabricate SOI wafers require high temperature anneals ($>1100^{o}C$) [30]. These high temperature anneals will result in the oxygen out-diffusion from the buried oxide, thus creating lots of traps. So the buried oxide could trap close to 100% of the radiation-induced holes at deep trap sites in the bulk of the buried oxide. In addition, the trapped holes do not readily anneal even if the oxides are exposed to temperatures as high as $350^{o}C$. Though electrons would be trapped in the buried oxide, they will be thermally detrapped within less than 1s after being trapped. All these characteristics make the SOI technology a good candidate for TID monitors.

Figure 20 shows the leakage current versus irradiation and anneal time [30]. It shows

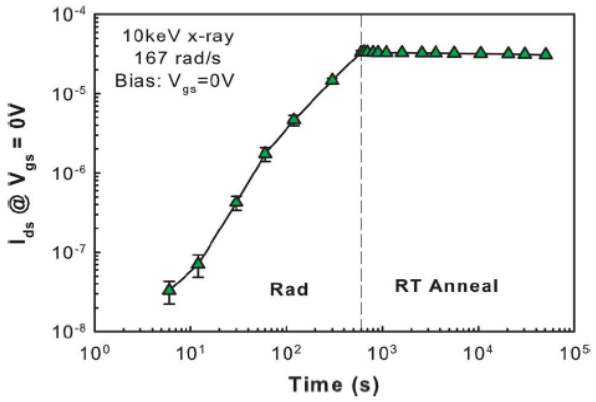


Figure 20 "Off" state leakage current versus irradiation and anneal time for BOX RADFET irradiated at dose rates of 167 rad (SiO_2)/s with all pins shorted. The transistor was annealed at room temperature with all pins shorted [30]

that the leakage current has a nearly power law dependence on the total dose. And the fade is around 10% for $5\times10^{4}s$ anneal, which is small enough to be a good TID monitor.

The basic idea behind the leakage current based TID monitor is measuring the leakage current. There are a lot of ways to realize this. **Figure 21** presents an elegant method. By translating the leakage current into a periodic wave output through a current controlled oscillator (CCO), the leakage current could be easily identified. The periodic wave

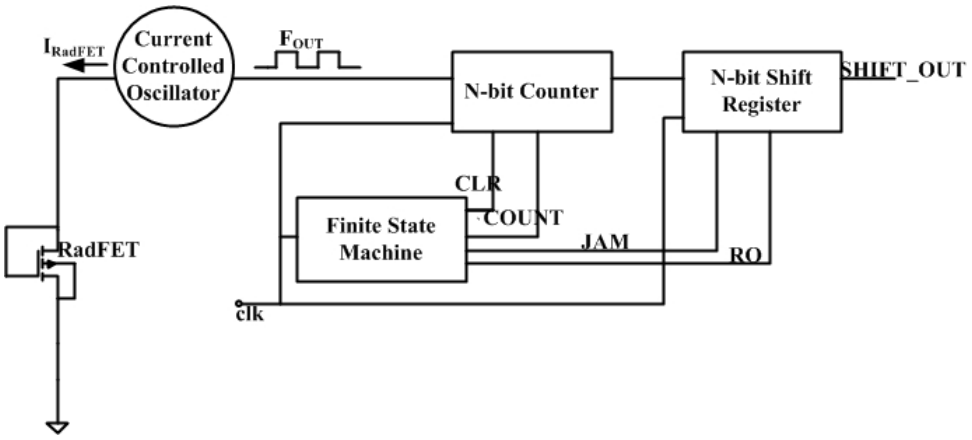


Figure 21 Block diagram for the leakage current measuring circuit [30]

frequency could be measured through a counter with a known clock frequency. Assume that the counter output is a digital word N_C, then the periodic wave frequency is

$$N_C = \frac{F_{out}}{F_{clk}} \tag{6}$$

where F_{out} represents the CCO output periodic wave frequency, and F_{clk} represents the counter clock frequency. To read out the digital word N_C, a shift register is used as shown in the block diagram. A finite state machine (FSM) is used to control the digital circuits.

The idea is straightforward and easy to implement. And these are great advantages over threshold voltage shift-based TID monitors. **Figure 22** shows the output waveforms of the whole circuit. From the output waveforms, the FSM first sends a "*CLR*" signals to clear

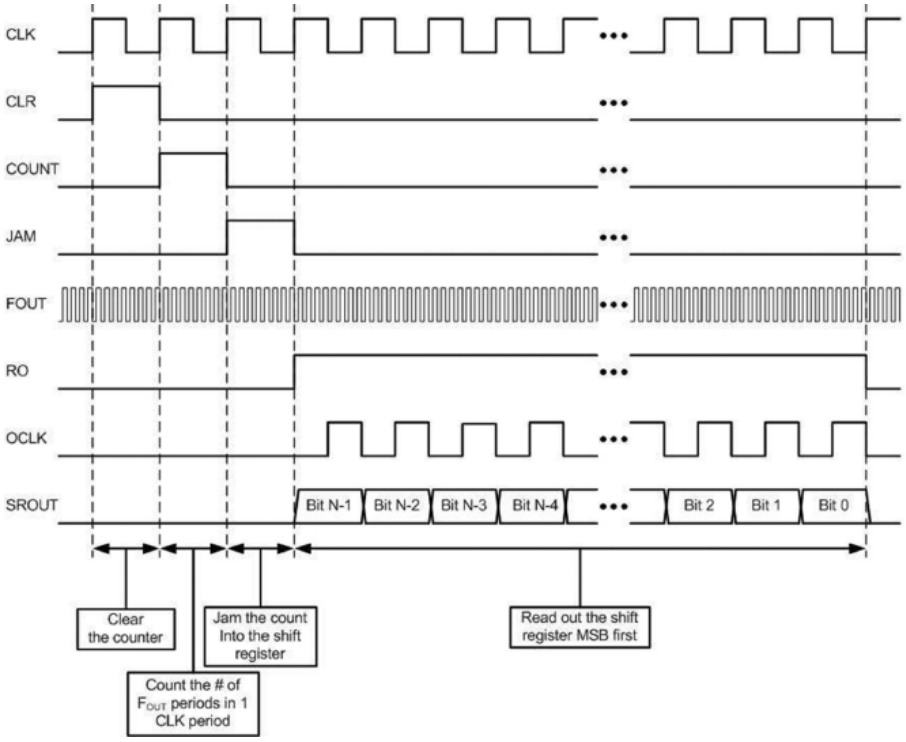


Figure 22 Leakage current based TID monitor read out circuit waveforms [30]

the counter, then a "*COUNT*" signal to enable the counter. After that, the counter starts to count the CCO output periodic wave frequency. Then FSM sends a "*JAM*" signal to the shift register to latch the counter output. Finally FSM sends a "*RO*" signal to the shift register to shift the digital word N_C bit by bit.

One important step in characterizing the monitor is the relationship between the leakage current and the output digital word. **Figure 23** illustrates the relationship of these two parameters. As can be seen, the digital word is quasi-linear with the input leakage current. The dependence can be characterized by a power law. This is important and very advantageous over the threshold voltage shift-based TID monitor. After measuring the digital word, the input current can be readily identified.

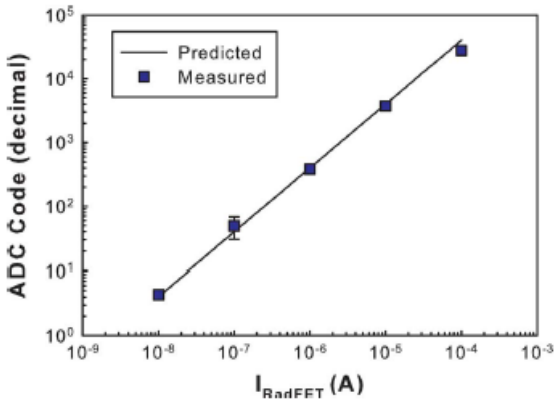


Figure 23 digital words versus leakage current [30]

The leakage current based TID monitor presents an insightful and easy approach to work with. And the monitor shows good performance. Another inherent advantage is that the output is a digital word. So there is no need of an ADC to perform the analog to digital conversion.

2.3 Conclusion

In this chapter, two categories of TID monitors are presented. Although there are other options, such as the organic semiconductor monitor described in [31], which is based on the resistivity change after irradiation, the threshold voltage shift based TID monitors and the leakage current based TID monitors are the most common and most promising to integrate with the standard CMOS technology.

Leakage current based TID monitor shows a great advantage over its threshold voltage shift based counterpart. It's much easier to build, easy to characterize, and has good performance. **Table 3** summarizes several aspects of the threshold voltage shift-based TID monitors, discrete PMOS RADFET and On-chip CMOS circuit, and the leakage current-

based TID monitors. From the table, it is very clear that the leakage current-based TID monitor is a promising approach. The rest of the thesis is based on this method.

	Embeddable	**Accurate**	**Sensitivity**	**Easiness**
Discrete PMOS RADFET	Very poor	Good	Good	Very good
On-chip CMOS circuit	Very good	Fair	Poor	Very poor
Leakage current circuit	Good	Very good	Very good	Good

Table 3 Comparison between the threshold voltage shift based TID monitors and leakage current based TID monitors

3. Embedded Leakage Current Based TID Monitor

In this chapter, the leakage current-based TID monitor is designed. The technology used in this thesis is an IBM 32nm SOI technology. To implement this technology, there are a few difficulties that need to be overcome. Next, different components of the system are examined individually. Different design strategies are evaluated and proper choices are made.

3.1 Current Controlled Oscillator (CCO)

The design requirement for the CCO in this work should be

- Input current range: 10nA~100uA
- High linearity between oscillation frequency and input current, i.e., K_{ICO} should be independent of input current
- Maximum output oscillation frequency should not exceed several gigahertz. In this work 1GHz is chosen.

There are a lot of CCO designs in the literature [31-36]. Loosely speaking, they can be classified in three categories: grounded capacitor relaxation oscillator [31-33], set-reset oscillator [34-35], and inductive current tuning oscillator [36]. These oscillators will be examined below briefly and the proper oscillator will be chosen.

3.1.1 Grounded Capacitor Relaxation Oscillator

A relaxation oscillator is an oscillator based upon the behavior of a physical system's return to equilibrium after being disturbed [37]. Taking a capacitor as an example, the capacitor can be charged toward a positive power supply until it reaches a threshold voltage sufficiently close to the supply. At that moment, the capacitor turns to discharge

toward the negative power supply. Similarly, when it reaches another threshold, it changes to charge again. Alternatively, when the capacitor reaches each threshold, the charging source can be switched from the positive power supply to the negative power supply or vice versa. This repeatedly charging and discharging behavior forms the oscillation. However there are usually two different strategies of realizing the oscillator: single capacitor CCO and double capacitor CCO.

3.1.1.1 Single Capacitor CCO

Conventionally only one grounded capacitor is used. **Figure 24** shows one such structure. The input current is mirrored into transistor $M3, M5$, which are the discharging and charging current correspondingly. Note that in this structure, the output parasitic capacitance is parallel to the external capacitance, so they could be just added together, which is a big advantage over the floating capacitor structure shown in [32]. The control

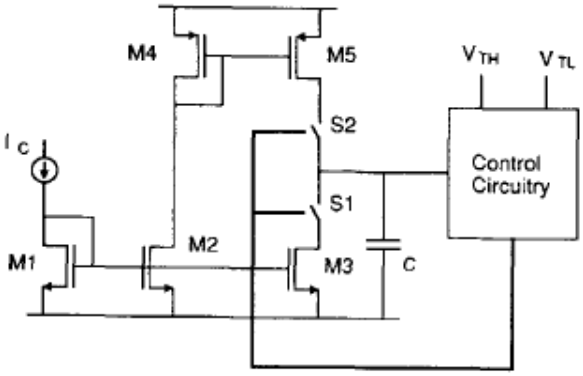


Figure 24 Single capacitor CCO schematic [31]

circuit outputs the control signal for the switches S1 and S2, such that when the capacitor voltage reaches the V_{TH}, S1 turns on and S2 turns off. When the capacitor voltage reaches the V_{TL}, S1 turns off and S2 turns on. The control circuit can be realized as a Schmidt Trigger as shown in [33] or the comparator based circuit in [31].

Figure 25 shows the single capacitor CCO capacitor voltage waveform. It can be shown

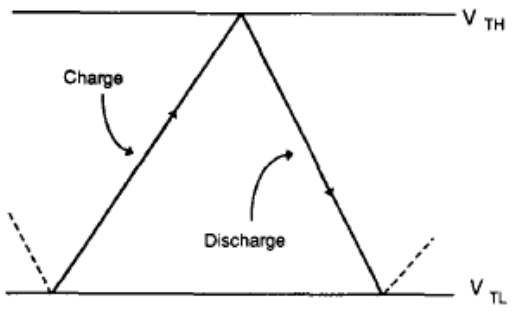


Figure 25 Capacitor voltage waveform of single capacitor CCO [31]

that the oscillation period is equal to the sum of the charging and discharging time.

$$f = \frac{1}{T} = \frac{1}{\frac{2(V_{TH} - V_{TL})C}{I_C}} = \frac{I_C}{2(V_{TH} - V_{TL})C} \tag{7}$$

The single capacitor CCO suffers from several disadvantages [31]. It's hard the match the NMOS and PMOS current, so the charging and discharging current will not be the same. In addition, switching at different voltages means that 50% duty cycle is difficult to achieve. However, the double capacitor CCO avoids the above issues.

3.1.1.2 Double Capacitor CCO

The double capacitor CCO design is shown in **Figure 26**. Here two grounded capacitors C1 and C2 are used. Current mirrors MP1, MP2 and MP3 are used to match the charging current. A comparator based control circuit is designed here to switch the charging signals.

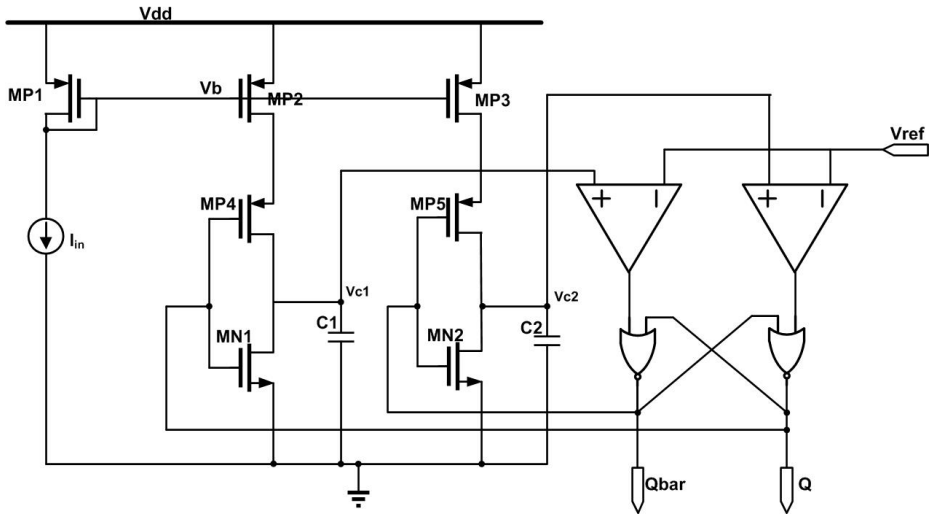


Figure 26 Double capacitor CCO schematic [31]

Next, the operation of the whole circuit is explained. Suppose initially the voltage on C1 is high and the voltage on C2 is low compared with V_{ref} ; then the SR latch will set. The feedback from the SR latch will turn MN1 and MP5 on; while at the same time turn MP4 and MN2 off. So C1 starts to discharge and C2 starts to charge. Again, until the voltage on C2 reaches V_{ref} , the SR latch will reset. The feedback will turn MN1 and MP5 off; at the same time MP4 and MN2 will be turned on. This will charge C1 and discharge C2. So the oscillation is formed by repeated cycles of charging and discharging. The C1 and C2 voltage waveform is shown in **Figure 27**.

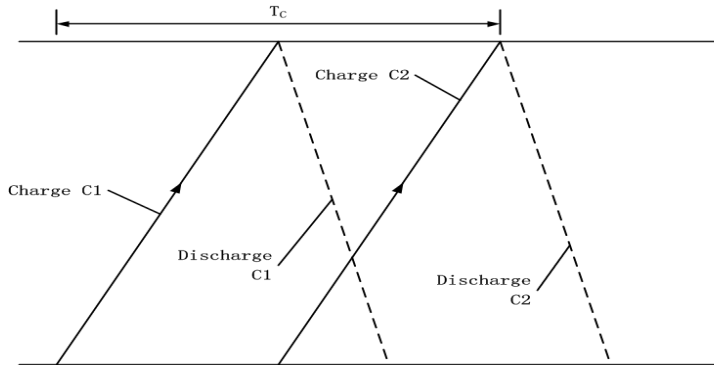


Figure 27 Voltage waveform of C1 and C2 of double capacitors CCO [31]

Compared with the single capacitor CCO, the oscillation period is the sum of the two capacitors' charging time, instead of the sum of the charging and discharging time of a single capacitor.

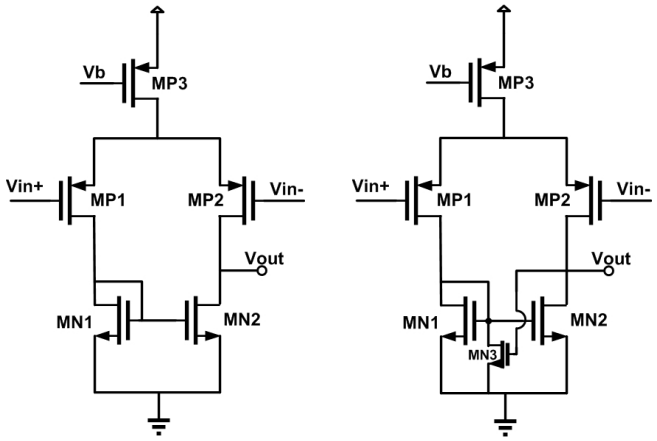
$$f = \frac{1}{T} = \frac{1}{\frac{V_{ref}C_1}{I_C} + \frac{V_{ref}C_2}{I_C}} = \frac{I_C}{V_{ref}} \frac{1}{C_1 + C_2} \tag{8}$$

If the two capacitances are equal, then

$$f = \frac{1}{T} = \frac{I_C}{2V_{ref}C} \tag{9}$$

This is a big advantage. Because as long as the discharging is faster than charging, the oscillation period has nothing to do with the discharging time. This means that there is no need to match the charging and discharging current, which is very difficult in reality. Another advantage of this structure is that there is only one reference voltage used. So it is much easier to achieve the 50% duty cycle oscillation.

One of the key components in this structure is the comparator. There are several options, such as the single stage open-loop amplifier, the cascade open-loop amplifier, and the latched comparator. Here due to the regular and predictable voltage waveform on the two capacitors, the single stage open-loop amplifier with active current mirror load is used.



(a) (b)

Figure 28 (a) Single stage open-loop amplifier schematic, (b) modified version

Figure 28(a) shows the structure of the comparator. The input is a differential transconductance stage, and the output stage is an active current mirror load. If faster response is needed once V_{in}+ exceeds V_{in}-, the modified version shown in **Figure 28**(b) can be used. Here the additional small size transistor MN3 provides a positive feedback so that the steady state is settled much faster. If V_{out} is high, then MN3 is ON, pulling down the gate voltage of MN2 and MN1, thus favoring the charging of the output capacitance. However MN3 size has to be small, or the cross-coupled pair MN2 and MN3 will keep the output voltage going low, so the discharging time of the output node will be quite long when V_{in}+ falls below V_{in}-.

3.1.2 Set-Reset Oscillator

This type of oscillator uses a cross-coupled inverter pair, like SRAM cells. If somehow, the cross-coupled inverter pair could be set and reset periodically, then the oscillation is formed. **Figure 29** shows such a structure. If V_d is high and V_c is low, then PMOS P1 is ON to pull up the node voltage V_a. NMOS N3 is gradually turning ON, which will discharge the node capacitance, so V_d is pulled low. The same process goes for P2 and N4.

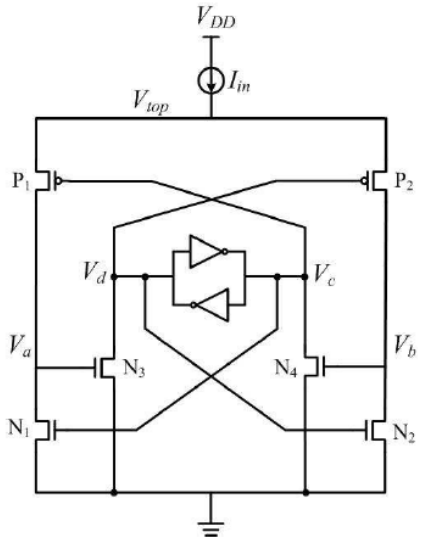


Figure 29 Set-reset oscillator [34]

This oscillator is very simple and straightforward. However, there are several issues associated with it. First, due to the meta-stability of cross-coupled inverter pair, the circuit may enter the third stable point that P1 and P2 divide the input current equally, and the oscillation is no longer sustained. Second, there is no simple relationship between the input current and the oscillation frequency. This adds difficulty in designing the circuit to fulfill specific requirements.

3.1.3 Inductive Current Tuning Oscillator

This type of oscillator is the analog of the varactor-based voltage controlled oscillator (VCO), where a control voltage is used to vary the capacitance, thus varying the center oscillation frequency. Here inductive component that is controlled by current is used to tune the inductance [36].

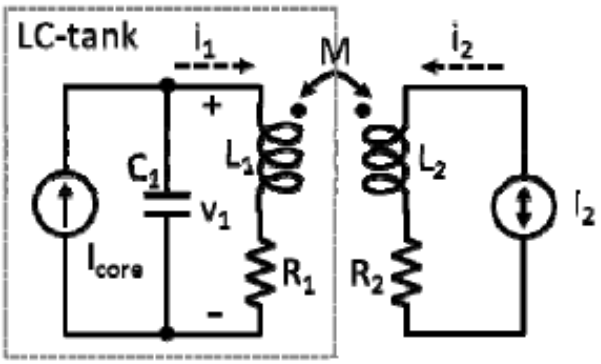


Figure 30 Principle of the inductive current tuning [36]

Inductive current tuning is shown in **Figure 30**. The principle of this circuit is that

$$V_1 = sL_1 i_1 + sMi_2 + R_1 i_1 \tag{10}$$

If $I_2 = \alpha I_1$, then

$$V_1 = s\left(L_1 + \alpha M\right) i_1 + R_1 i_1 \tag{11}$$

so

$$L_{eff} = L_1 + \alpha M \tag{12}$$

By changing the secondary inductor current, the primary inductor inductance can be tuned. If this inductor is applied in the LC oscillator, the output frequency can be tuned.

3.1.4 Conclusion

In this section, three different types of CCO are discussed. They show associated advantages and disadvantages. In this work, large input current range and high linearity are required. As a result, the double capacitor CCO structure is applied in this work.

3.2 On-Chip Clock

This is the second oscillator needed in this design. This clock is fed into the digital read out block. It's a relatively easy design because we do not need a phase locked loop here. So, a simple ring oscillator is designed. The design requirements are

- Oscillation frequency should be smaller than the minimum CCO output frequency
- Ring stages should be as small as possible
- Sustained oscillation

3.2.1 Circuit Diagram

The schematic of a ring oscillator is shown in **Figure 31**. It contains N stages, where N is an odd number. The NAND2 gate is used with an extra input EN, which is used to start up the oscillation.

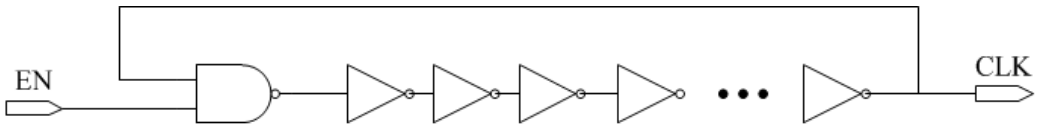


Figure 31 Ring oscillator block diagram

The oscillation frequency is

$$f = \frac{1}{T} = \frac{1}{N\left(t_{pHL} + t_{pLH}\right)} \tag{13}$$

where t_{pHL} is the high to low single stage propagation delay, and t_{pLH} is the low to high single stage propagation delay.

In IBM 32nm SOI technology, the single stage inverter delay would be around 1ps, which is extremely small. So for a 1MHz CCO minimum oscillation frequency, it would need a huge number of stages to achieve the delay. So the single stage could not be just a simple inverter, instead it should be modified.

The first option would be a current starved single stage. By controlling the charging and discharging current, the single stage inverter propagation delay could be modified. **Figure 32** shows the structure of the single stage. Here "ContP" and "ContN" are used to control

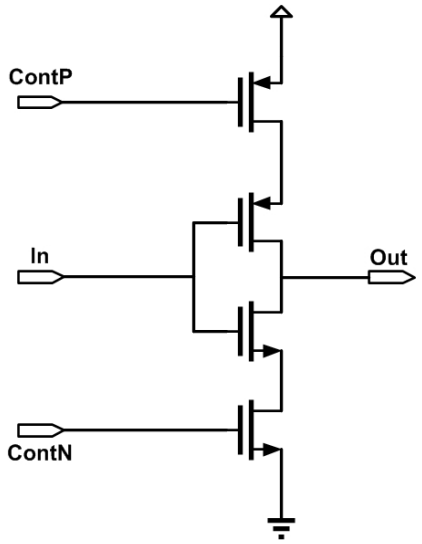


Figure 32 Current starved single stage inverter

the charging and discharging current. These two currents could be tuned to be smaller than the simple inverter, so output node capacitor charging and discharging time could be made much longer.

Another option could be adding a series transmission gate between the input and the inverter, which increases the propagation delay. The transmission gate could be

controlled by a control voltage. **Figure 33** shows the circuit diagram. The transmission gate

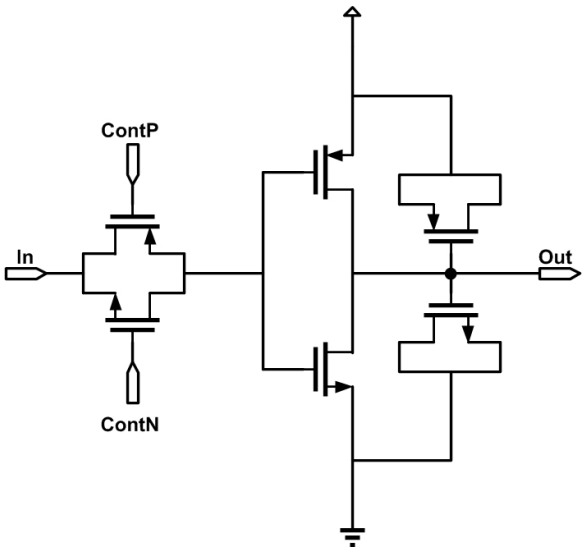


Figure 33 Series transmission gate single stage inverter

inserted between the input and the inverter is used to control the propagation delay of the signal from the input to the inverter gate. Furthermore, to increase the delay, drain and source connected NMOS and PMOS are connected to the output node.

This structure is much better than the previous one. Because in the previous one, the charging and discharging current is tuned, there is a great possibility that the oscillation will damp out if the stage number is large. To get a reasonable stage number, the bias transistors in the previous design operate around the subthreshold region. This small charging and discharging current will make things worse.

The above issues are resolved in the latter structure. Because the inverter connects directly to the power supply, the charging and discharging current do not degrade. This property helps sustain the oscillation.

3.3 Digital Read-Out Circuit

A digital read out circuit is used to measure the CCO output frequency. It is composed of simple blocks: counter, FSM, and shift register. **Figure 34** presents the circuit diagram.

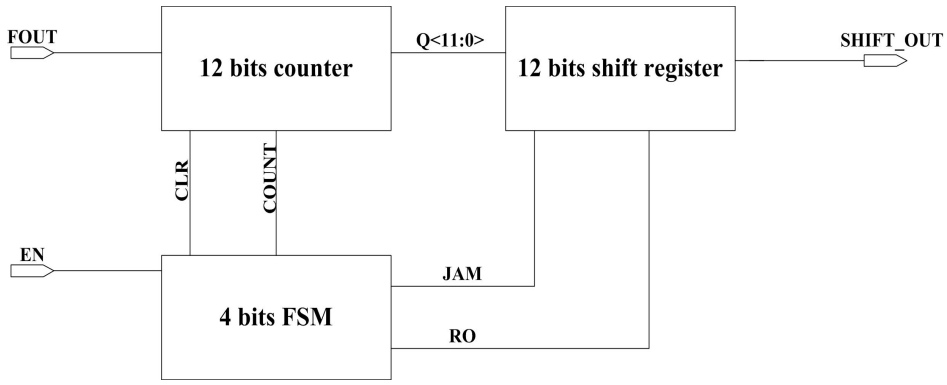


Figure 34 Digital read-out circuit diagram [30]

"FOUT" is the output of CCO, and 12 bits counter measure the FOUT frequency, and stores the output in Q<11:0>. Shift register receives the Q<11:0>, and shifts out the digital word bit by bit. The 4bit FSM is used to coordinate the counter and shift register. Because counter and shift register are the standard digital circuits, their circuit diagram is simple and not reproduced here. **Figure 35** is the circuit diagram of the 4bit FSM.

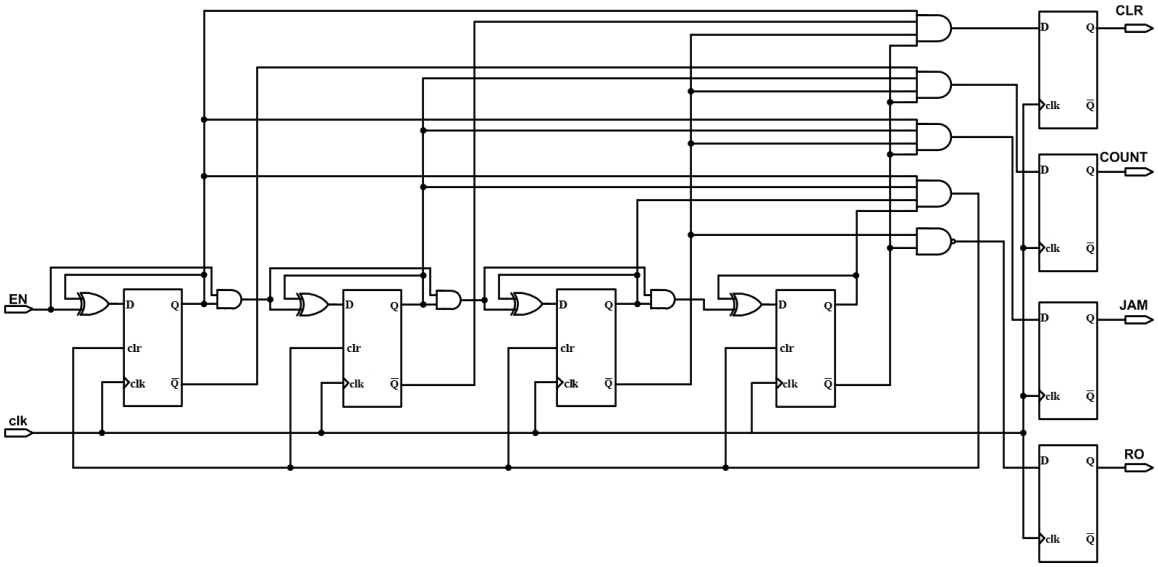


Figure 35 4bits FSM circuit diagram

4. Simulation and Verification

In the last chapter, different circuit components are examined and different design alternatives are presented. For each component, the design choice is made. In this chapter, these circuits are designed and simulated in IBM 32nm SOI technology.

4.1 CCO Simulation and Verification

In this section, the comparator and the whole CCO are designed and simulated. The CCO output frequency versus input current relationship is characterized.

The key component in the double capacitor circuit is the comparator as shown in **Figure 28**. First, the design of the comparator is discussed, and then the results are presented. In this thesis, it's designed in an IBM 32nm SOI technology, and all the transistors have the same minimum gate length $L = 40nm$. **Figure 36** shows the bias and sizes of the transistors. Because only a single stage is used here, the gain is not sufficient. From the

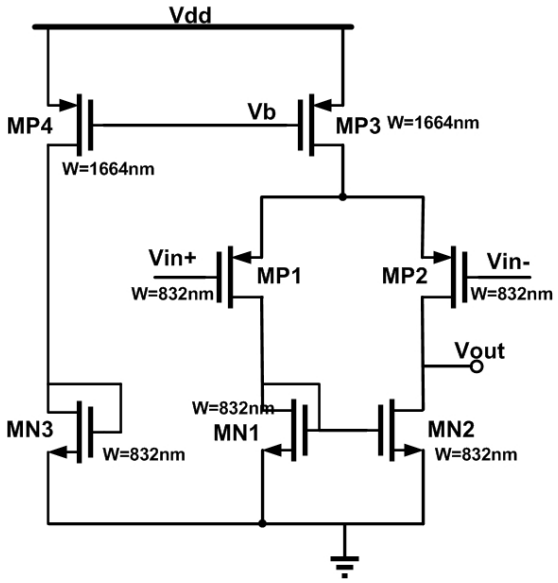


Figure 36 Single stage open loop comparator biasing and transistor sizes

simulation results, the low frequency gain is less than 10. **Figure 37** shows the comparator output waveform. And it verifies that the gain is not so large that the output does not saturate at the power supplies. In the IBM 32nm SOI technology considered here, the positive power supply voltage is equal to 0.9V. The input triangular voltage pulse frequency is 2GHz, which is larger than the maximum CCO oscillation frequency, 1GHz. In this situation, the propagation delay is approximately 35ps, which is relatively small, less than 10% of the input wave period. So for this project, the comparator is good enough. However, in order to improve the low gain, a buffer is connected to the output. The delay introduced by the buffer is around several picoseconds and is negligible.

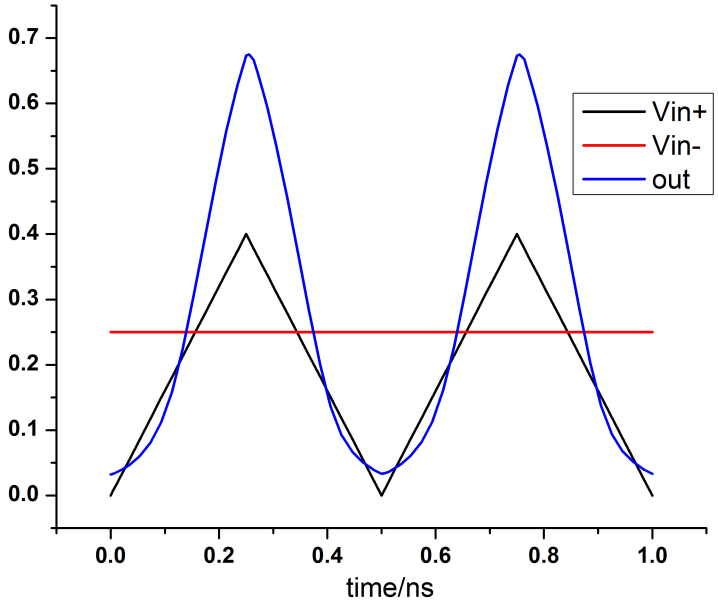


Figure 37 comparator output waveform when Vin- is equal to 0.25V, and Vin+ is a 2GHz triangular pulse and peak-to-peak value of 0.4V, which is similar to the situation in the double capacitor CCO.

Figure 38 shows the final design and output waveform of the comparator. The output buffer is implemented with minimum size transistors. With the same input condition as Figure 37, the output before the buffer is the same as Figure 37. But the output after the

buffer has rail-to-rail voltage swing. The propagation delay now is approximately equal to 60ps, which is approximately equal to 10% of the input signal period. Since the maximum output frequency of the CCO is 1GHz, the comparator is good enough.

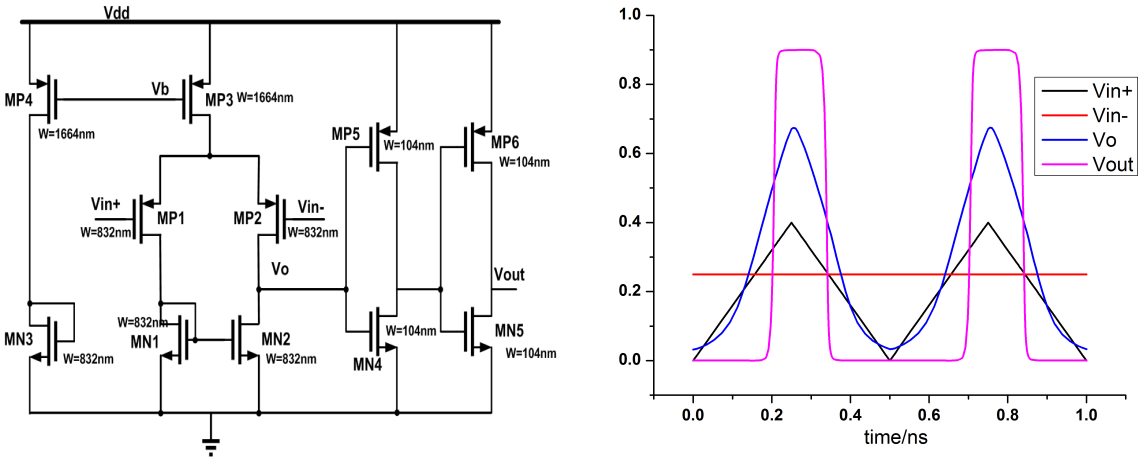


Figure 38 (a) final design of single stage open loop comparator with output buffer; (b) the output waveform of (a) with the same input waveform as Figure 37

Next the double capacitor CCO is simulated. **Figure 39** shows the biasing and sizing of each transistor in the CCO. C1 and C2 both have the size of $8.96\mu m \times 8.96\mu m$. The RS latch is realized by two cross-coupled NOR2 gates. The reference voltage is set to 0.30V to achieve about 1GHz oscillation when the input current is 100uA.

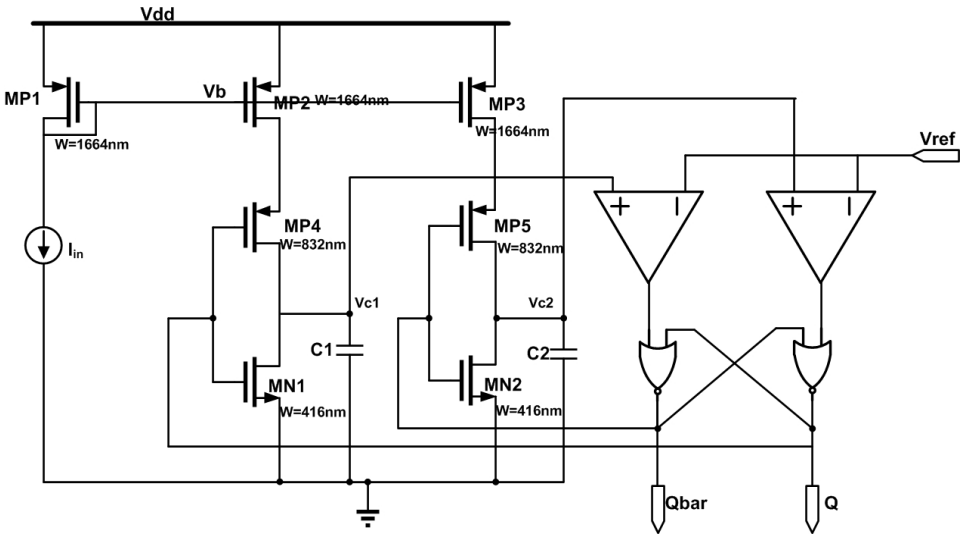


Figure 39 Biasing and sizing of each transistor in double capacitor CCO

At 100uA input current, the output waveform is shown in **Figure 40**. It's shown that the output waveforms are exactly complementary. The oscillation period is 0.9ns, so the frequency is 1.1GHz.

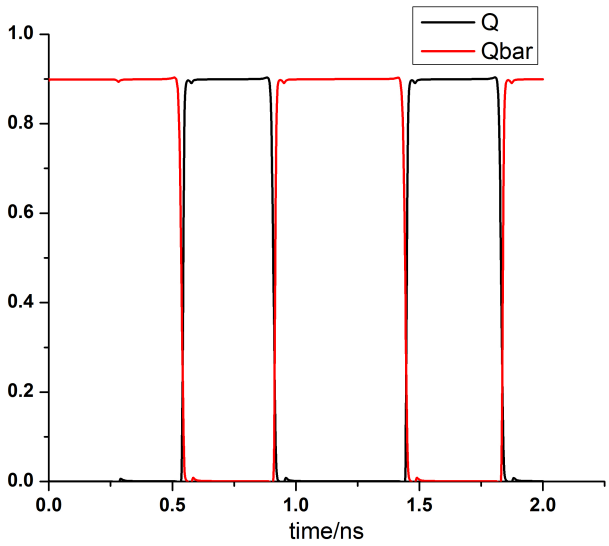


Figure 40 Output waveform of double capacitor CCO schematic simulation when input current is 100uA

Furthermore, the layout of the CCO is designed. Because of the differential amplifier in the comparator and the current mirrors in this CCO, the common centroid layout is used here for better matching. **Figure 41** shows the layout of the circuit. The following

paragraphs present the post layout simulation and comparison between schematic and layout results.

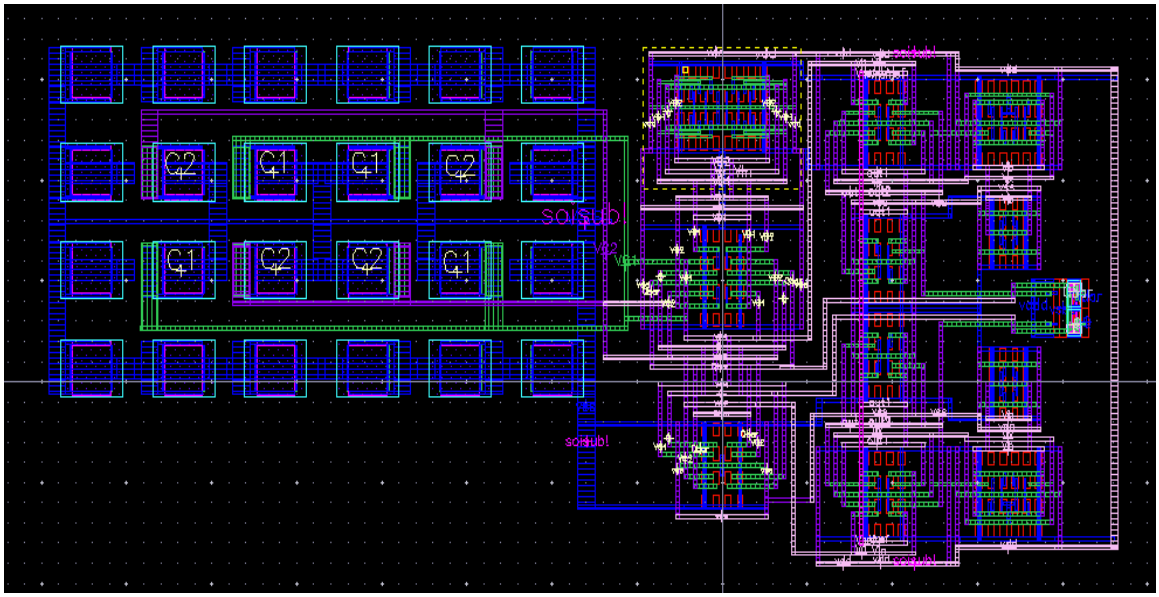


Figure 41 double capacitor CCO layout

For the layout, an important design aspect is the metal width. If it is too small, then the interconnect resistance is very high so that the voltage drop on the metal lines is large. On the other hand, if it is too wide, the parasitic capacitance is a big problem. In the initial layout used in this design, the metal line width was set to be large so that in the low current range, the circuit did not oscillate. This issue was resolved when the metal lines were resized.

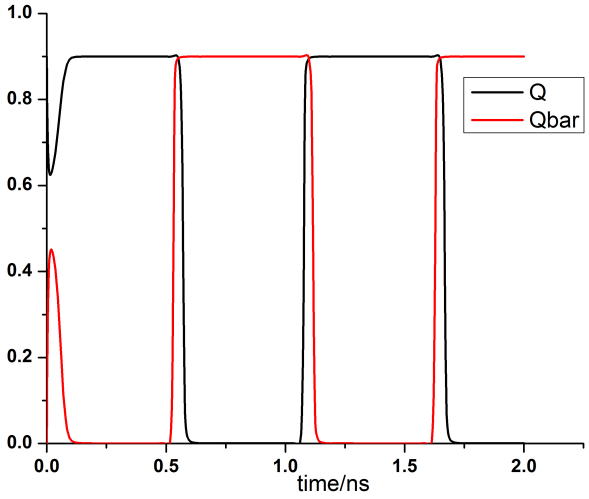
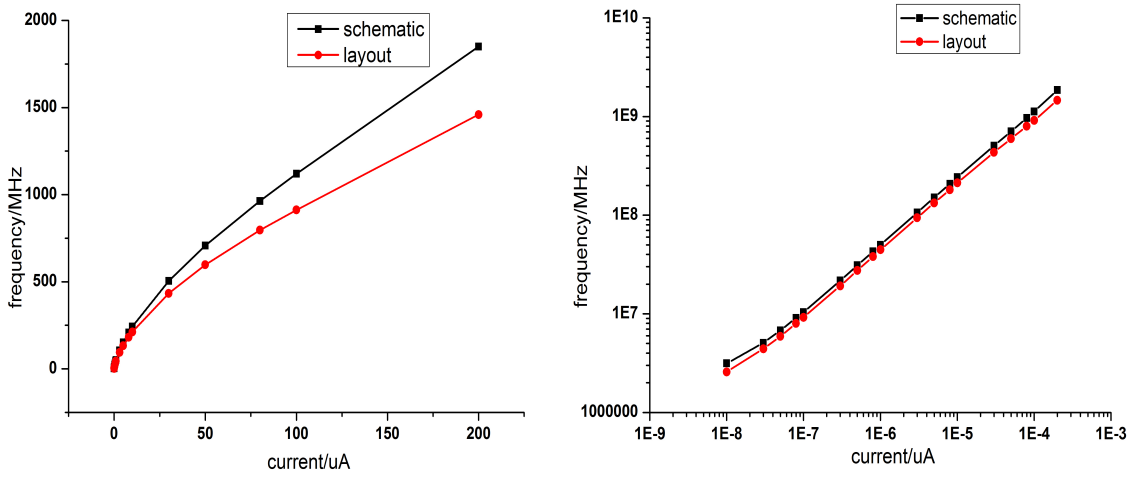


Figure 42 Output waveform of double capacitor CCO layout simulation when input current is 100uA

Figure 42 is the post layout simulation. The oscillation period is 1.097ns, so the frequency is 0.91GHz. That the period is longer than predicted is fairly reasonable because of the larger parasitic capacitance and resistance in the layout. Next it's important to examine the relationship between the input current and oscillation frequency relationship.

Figure 43(a) shows the oscillation frequency versus input current on the linear-linear scale and **Figure 43**(b) is the same relationship on the log-log scale. **Figure 43**(a) shows that this relationship deviates from linear to power law. And **Figure 43**(b) confirms this point. Moreover, the schematic and layout follows the power law with almost the same power index. By curve fitting, we can get the following relationship

$$f_{schematic} = 10^{11.752} \times I^{0.675}$$
$$f_{layout} = 10^{11.638} \times I^{0.666} \quad \textbf{(14)}$$



(a) (b)

Figure 43 CCO frequency versus input current (a) linear-linear scale; (b) log-log scale

That the frequency versus current gradually saturates is due to the delay of the comparator and RS latch. So the ideal linear relationship saturates with increasing input current. The actual relationship could be represented by

$$f_{actual} = \frac{1}{\frac{1}{f_{ideal}} + T_d} \tag{15}$$

where T_d is the total delay of the comparator and RS latch.

In this section, the CCO design and simulation results are presented. The key component in CCO, the comparator, is simulated. The total delay of the comparator is approximately 60ps, which poses little issue when the input current is low. Simulation of the CCO suggests that the input current range could be 10nA~100uA, and the corresponding oscillation frequency is 2.5MHz~1GHz. The post layout simulation is also conducted. The results are reasonable due to the increase of parasitic resistance and capacitance. The frequency versus input current relationship is characterized, which shows a power law dependence. The power index is approximately 0.67, which, since it is less than 1, suggests the saturation behavior mentioned above. For this project, to be able to infer the

input current from the measured frequency, the relationship between frequency and input current has to be characterized.

4.2 On-chip Clock Simulation and Verification

In this section, the on chip clock is designed and simulated. Though the on chip clock is realized using a simple ring oscillator, there are a lot of issues that need to be resolved. The biggest problem is that in IBM 32nm SOI technology, the single stage inverter propagation delay is extremely small. In order to get oscillation frequency as low as 2MHz, the stage numbers would be formidably large. Next, several types of single stage designs are presented and simulated.

The first stage is a simple inverter with the minimum sizes. The transient simulation is shown in **Figure 44**. It shows that the single stage propagation delay is

$$t_d = \frac{t_{pHL} + t_{pLH}}{2} = \frac{1.73 + 0.98}{2} ps = 1.35 ps \quad \textbf{(16)}$$

So to get a 2MHz clock, the number of stages needed would be

$$N = \frac{5 \times 10^5}{2.7} = 185185 \quad \textbf{(17)}$$

which is extremely high and impractical to design for a ring oscillator.

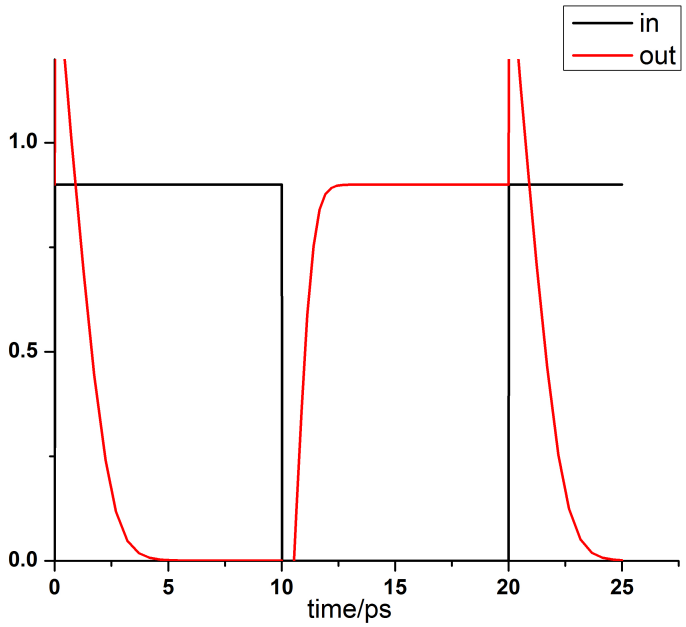


Figure 44 single stage of simple minimum sized inverter transient simulation

The next stage is the current starved single stage mentioned in section 3.2.1. The bias and sizes of transistors are shown in **Figure 45**. To achieve considerable propagation delay, the charging and discharging current should be highly restricted. Here "ContP" is chosen

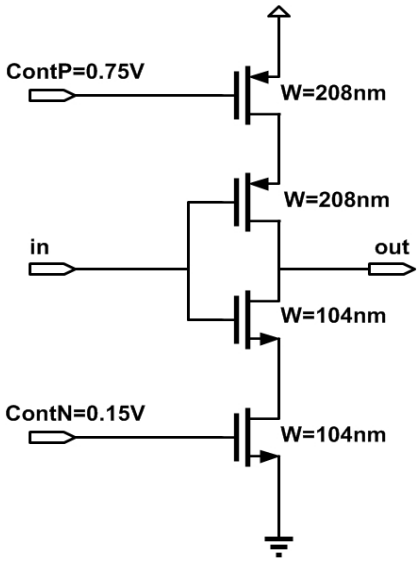


Figure 45 biasing and sizing of transistors in current starved inverter

to be 0.75V and "ContN" is chosen to be 0.15V. the transient behavior of such circuit is shown in **Figure 46**. It shows that the single stage propagation delay is

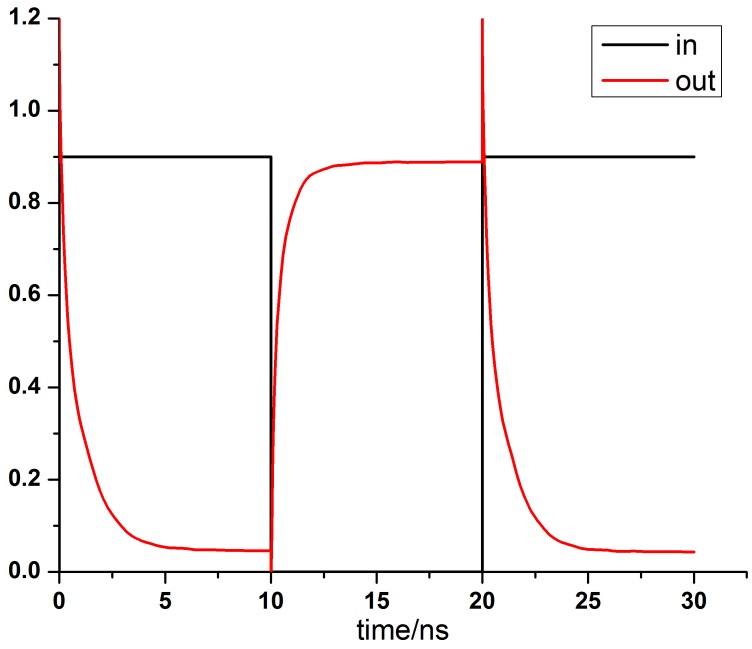


Figure 46 transient behavior of single stage current starved inverter biased at "ContP" equals 0.75V, while "ContN" equals 0.15V

$$t_d = \frac{t_{pHL} + t_{pLH}}{2} = \frac{576 + 201}{2} ps = 388.5 ps \quad \textbf{(18)}$$

which is much bigger than the single stage inverter. So the number of stages needed to achieve 2MHz oscillation would be

$$N = \frac{5 \times 10^5}{2 \times 388.5} = 643 \quad \textbf{(19)}$$

which is a fairly reasonable number. However, this is not the end. In order to achieve a large single stage propagation delay, the bias is being pushed almost to the extreme. As a result, the output waveform is highly deformed. If more stages are included, the waveform would fade out. So in reality, the oscillation would be damped out and could not sustain itself. This is verified in the 10 stages current starved inverter transient

behavior as shown in **Figure 47**. The transient could not propagate far enough before it is damped out.

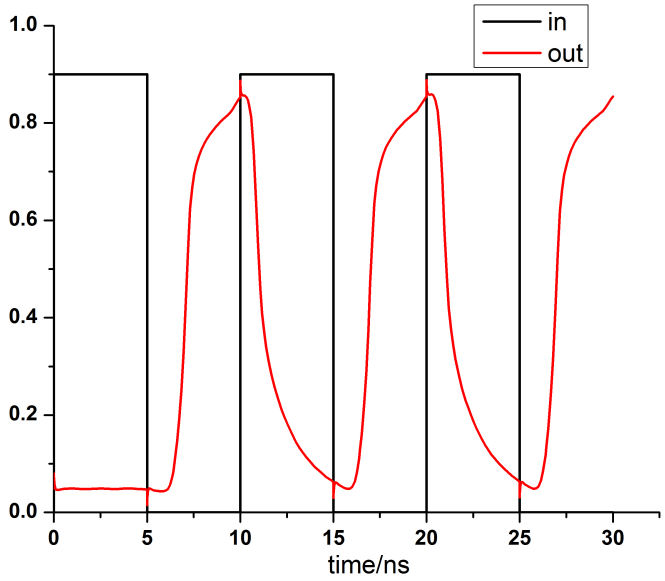


Figure 47 transient behavior of 10 stages of current starved inverter biased at "ContP" equals 0.75V, while "ContN" equals 0.15V

The third design is presented in section 3.2.1, which is a transmission gate based inverter stage. The biasing and sizing of each transistor are shown in **Figure 48**. The biasing "ContP" and "ContN" of the transmission gate are 0.75V and 0.15V, respectively.

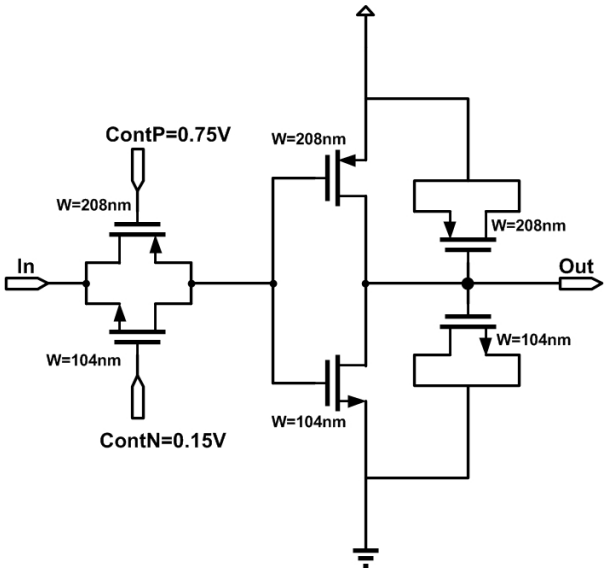


Figure 48 biasing and sizing of each transistors in transmission gate based inverter stage

As explained in section 3.2.1, this type of stage shows much more robust performance. **Figure 49** presents the transient behavior of this stage. Compared with the current starved inverter stage, the transient of the transmission gate based inverter stage is much better. The output waveform does not fade out and the propagation delay is

$$T_d = \frac{t_{pHL} + t_{pLH}}{2} = \frac{356 + 198}{2} ps = 277 ps \quad \textbf{(20)}$$

So to get 2MHz oscillation, the number of stages needed would be

$$N = \frac{5 \times 10^5}{554} = 903 \quad \textbf{(21)}$$

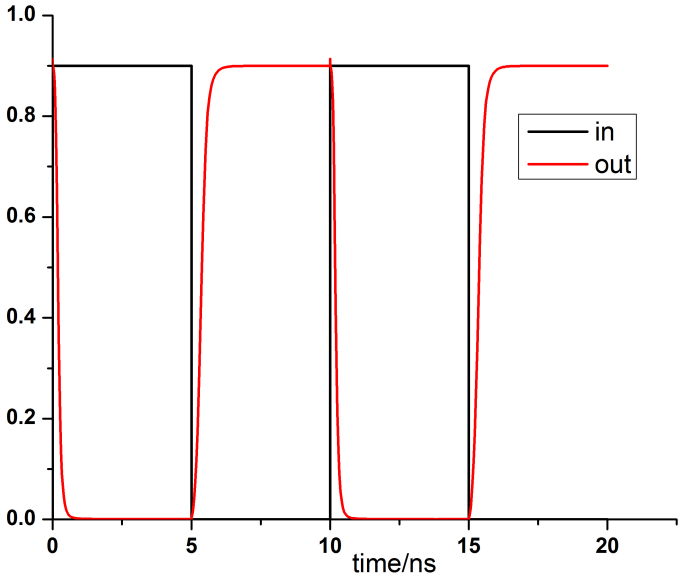


Figure 49 transient behavior of transmission gate based inverter stage

The result is also applicable. Further simulation suggests that the propagation of the transient along the stages is pretty good. And the number of stages is actually 401 to get a 2MHz oscillation. Next a ring oscillator composed of 401 stages of the transmission gate based inverter is simulated. **Figure 50** shows the schematic as well as the layout output waveform of the ring oscillator when "ContP" equals 0.75V, while "ContN" equals

0.15V. The schematic simulation shows that the oscillation frequency is 2MHz, while the layout simulation shows that the oscillation frequency is 1.3MHz. The results are reasonable considering the additional parasitic resistance and capacitance introduced in the layout.

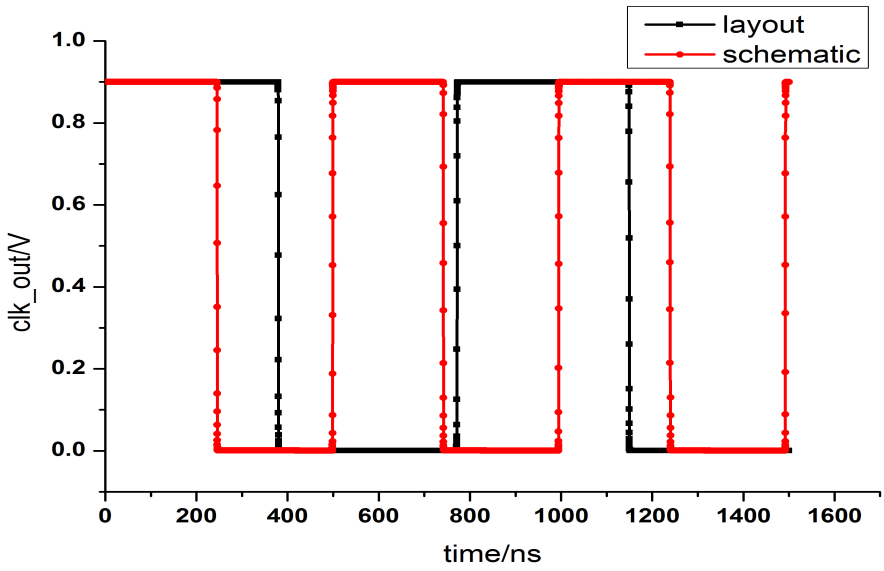


Figure 50 output waveform of ring oscillator composed of 401 transmission gate based inverter stages when "ContP" equals 0.75V, while "ContN" equals 0.15V

In addition, **Figure 51** shows the layout of the ring oscillator. It consumes a tolerable space and is pretty regular.

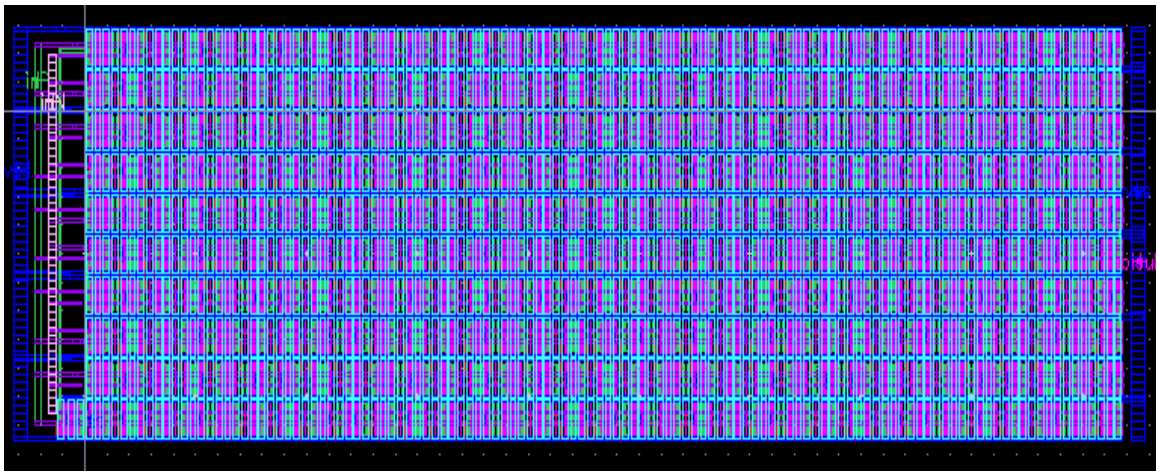


Figure 51 layout of the ring oscillator

In this section, the on-chip clock is designed and simulated. By comparing different single stage inverters, the transmission gate based single stage inverter is chosen. Because it has a similar propagation delay as the current starved inverter stage, and it has similar output waveform as the simple inverter stage. So it has the advantages of the other two types, and at the same time, avoids the disadvantages of the other two. Final simulation shows that a ring oscillator composed of 401 transmission gate based inverter stages has an oscillation frequency of 2MHz in schematic, and 1.3MHz in layout. This meets the requirement that the oscillation frequency should be less than the minimum CCO output frequency, 2.5MHz.

4.3 Digital Read-out Circuit Simulation and Verification

In this section, the digital read-out circuit is designed and simulated. **Figure 35** gives the schematic of the 4 bit FSM. The schematic simulation result is shown in **Figure 52**.

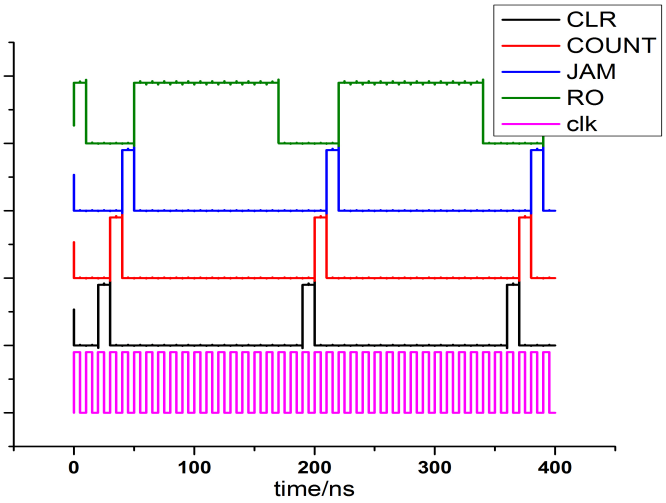


Figure 52 Schematic simulation waveform of the 4bits FSM when input clock frequency is 100MHz

The FSM first outputs the “CLR” signal to clear the counter, then “COUNT” signal to enable the counter. Then it outputs “JAM” signal to the shift register to latch the output

of the counter. Finally, the “RO” signal is used to enable the shift register to shift out the stored word bit by bit. From the waveform, the design requirement is fulfilled.

Figure 53 shows the layout of the 4bits FSM. It is designed in a very compact form.

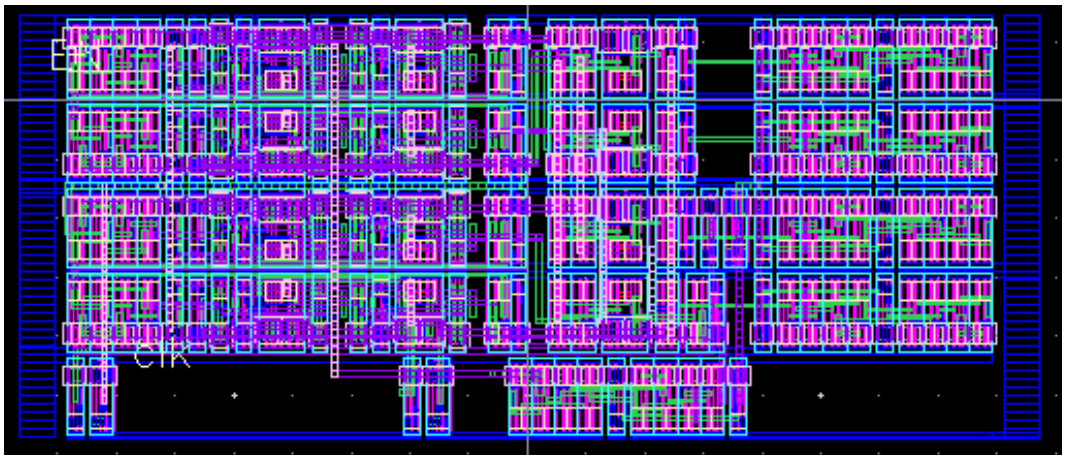


Figure 53 The layout of the 4bits FSM

The post-layout simulation is shown in **Figure 54**. In comparison with **Figure 52**, we find that the output waveforms of the schematic and layout are almost the same, except for some little spurs in the layout simulation waveform. This is due to the fact that

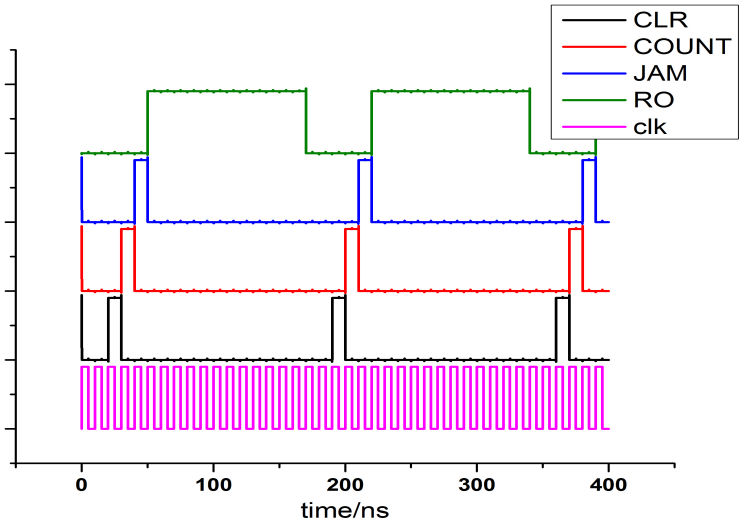


Figure 54 Post-layout simulation waveform of 4bits FSM when input clock frequency is 100MHz

the additional parasitics introduced in the layout do not have a significant effect on the output when the input clock frequency is as low as 100MHz. Since the designed clock frequency is 2MHz, the circuit works adequately. **Figure 55** shows the layout of a digital read out circuit that integrates the 4bit FSM, 12bit counter, and 12bit shift register. The whole digital read out circuit verification is put together with the whole system introduced in section 4.4.

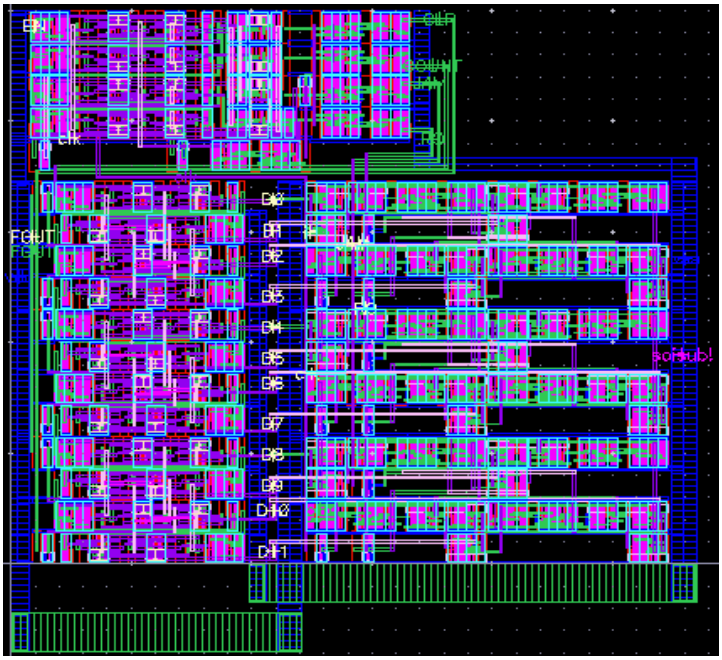


Figure 55 layout of the digital read out circuit

4.4 Whole System Simulation and Verification

Up to this point, all the circuit components are simulated and verified except for the whole digital read out circuit. In this section, all the components are integrated into the whole system. Then the whole system is simulated and verified. Next two different cases are tested. The first case is when the input current equals 1uA. The schematic simulation result is shown in **Figure 56**. For 1uA input current, the CCO oscillation frequency is 43.4MHz, and the clock frequency is 2MHz. In this case the counter digital word would

be 22, which is 0000 0001 0110 in binary format. And the simulation output is exactly 0000 0001 0110.

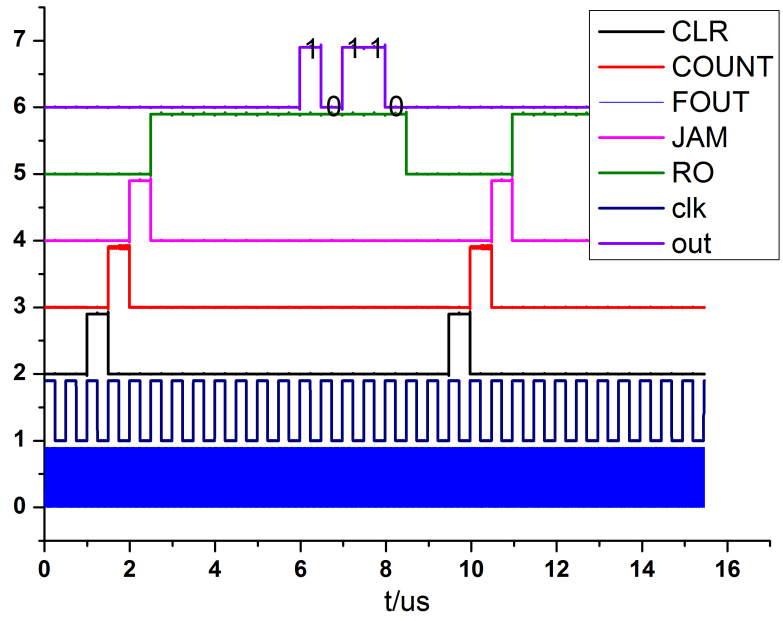


Figure 56 schematic simulation waveform of the whole system when input current is 1uA.

Another input example is when the input current is 100nA. The output waveform is shown in **Figure 57**. When input current is 100nA, the CCO output oscillation frequency is 9.5MHz. The clock frequency is still 2MHz. Because the counter stores the floor of the number, so the digital word would be 4, which is 0000 0000 0100 in binary format. And the output of the shift register is exactly 0000 0000 0100.

These two cases verify the system function. It shows that the digital word shifted out by the shift register correctly measures the input current, which gives the information about the total dose.

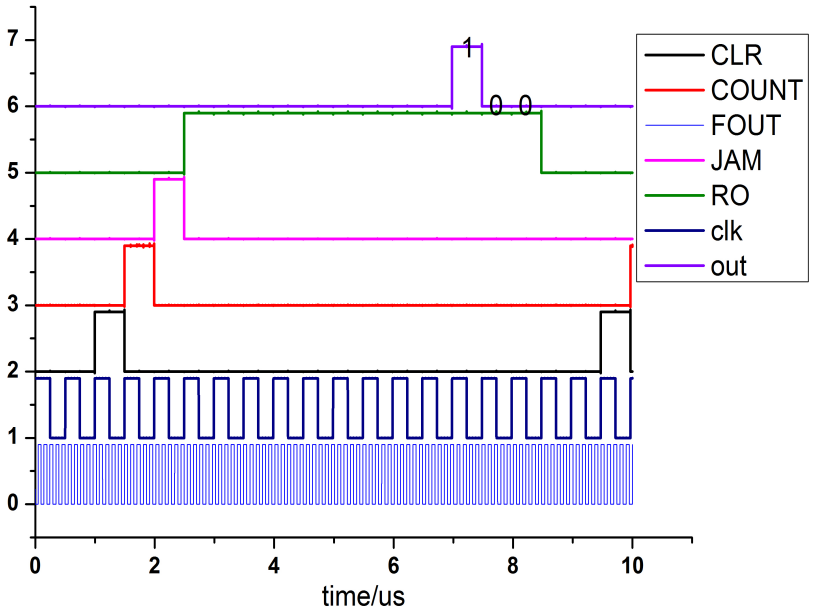


Figure 57 schematic simulation waveform of the whole system when input current is 100nA

4.5 Conclusion

In this chapter, all the components in the circuit are designed and simulated, and further the layouts are shown. In terms of the comparator, the open loop differential amplifier is chosen. If the gain is not big enough, a second stage could also be added. A double capacitor CCO structure is used here for better control and linearity. In terms of the on-chip clock, the series transmission gate inverter is used and verified. The simulation results show that all the components work very well and the system could function as a whole.

5. Validation of the On-chip TID Monitor

5.1 Introduction

All the simulation and verification work shown in Chapter 4 is done under the assumption that only the input device leakage current increases, while the other on-chip devices' leakage currents do not change. However, this is usually not a good assumption. Though the simulation results are promising in the case without leakage current, they do not guarantee that it will work if all the transistors have the increasing leakage current. In this chapter, we examine the effects of the leakage current in all the transistors and verify that the circuit will still function well.

Apart from the leakage current, we should characterize the effect of threshold voltage shift. For 32nm SOI technology, the transistor gate thickness is around 2nm, which is extremely small, such that the threshold voltage shift is negligible. Especially in this monitor circuit, most of the components are just functional components, like the comparator and the digital read out block, which do not depend on the exact parameter values. The analog part may be susceptible to the gain degradation after TID effect. However, in this circuit the only analog part is the current mirror, which is used to mirror the input current. Since the gain degradation has little effect on its performance, it can be concluded that the threshold voltage shift has negligible effect in this circuit.

If only the leakage current is included, the different circuit components need to be scrutinized separately. First for the digital part, which includes the digital read-out circuit

and on-chip clock, the leakage current effect could be neglected. The reason is that for typical digital circuit, for example an inverter, the leakage current always exists, but it does not affect the function of the digital circuit. In addition, the transistors used in the digital circuit are the smallest size transistors, which indicates that the leakage current would be much smaller than the input leakage current. We can conclude that the digital circuit would still function well under the increasing leakage current. But the speed of the digital circuit may decrease. However speed is not a very important parameter in this circuit, especially considering the already designed low speed of the digital circuit. So this analysis focuses on the effects of leakage current on the current controlled oscillator.

Before we simulate the effect of the leakage current on the CCO, we need to make several valid assumptions about the leakage current based on its behavior.

1. The leakage current is negligible for ON state transistors while substantial only for OFF state transistors.
2. At any instant, the leakage current is assumed to be constant and only perturbs the bias current. This is because the dose rate is limited [30], and to reach a given total dose level, it needs a long time. Compared with the maximum oscillation period of the CCO, which is 0.4us, the leakage current increases at an extremely slow rate. So at any instant of the operation of CCO, the leakage current could be considered to be constant, and perturb the bias current only.
3. The leakage current behaves quite differently for PMOS and NMOS transistors. Because the radiation-induced charges are positive, they will never create the back conducting channel for a PMOS FET. However the channel could be created

in a NMOS FET. So the PMOS leakage current would be simply be neglected, and the OFF state NMOS leakage current is the principal component that we care about.

4. As a first order approximation, the leakage current density is assumed to be constant across all the transistors, which simply means that the leakage current scales with the transistor area. The effect of edge leakage will invalidate this assumption, because the edge leakage does not scale with the area, instead it scales with the perimeter.

Suppose the edge leakage current is I_{lE} and the back channel leakage current is I_{lB}, then together with the leakage current not caused by radiation I_{l0}, the total leakage current could be approximately rewritten in terms of the transistor width and length as

$$I_l = I_{l0} + I_{lE} + \frac{W}{L} I_{lB} \tag{22}$$

If we simply scale the width $W' = NW$, the leakage current would not scale as expected, i.e., $I_l' \neq NI_l$. Since

$$I_l' = I_{l0}' + N\frac{W}{L} I_{lB} + N' I_{lE} \tag{23}$$

From simulation, it shows that $I_{l0}' \approx NI_{l0}$. So the first two terms in equation (23) approximately scale with the width. But the third term, the edge leakage, does not. It is related with the number of transistor fingers. The more the fingers, the larger is the edge leakage. As a result, if the first two terms dominate (the usual case), the leakage current would scale as the width, but if the third term dominates, the leakage current would scale as the number of fingers. So

$$N'I_{l0} \le I'_{l0} \le NI_{l0} \quad \textbf{(24)}$$

By proper choice of the width and the number of fingers of the sensing device, the leakage current would be scaled.

Two leakage current models are presented. The first one is a voltage independent current source model, and the other one is a voltage dependent parasitic transistor model. The first one is crude because it only accounts for the back channel leakage current, which is approximately constant at each instant, but it provides precious intuition into its behavior. The second one is more accurate as it considers the voltage dependent leakage current, such as the edge leakage.

5.2 Constant leakage current source model

After making these assumptions, we could now examine the leakage current effect on the CCO. First, let's look at the comparator with the first model. **Figure 58** shows the added

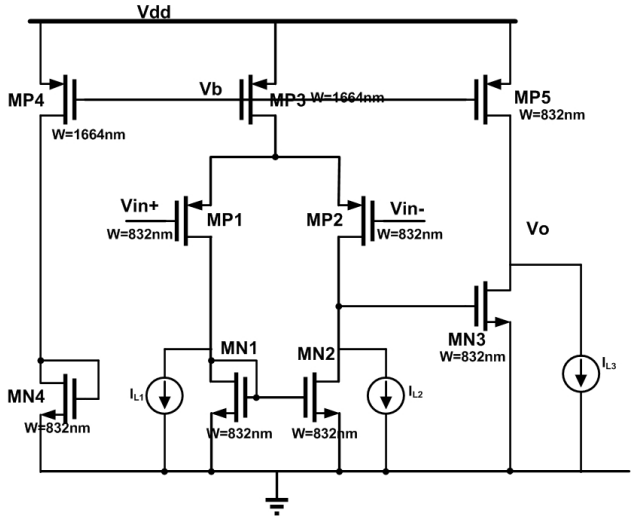


Figure 58 comparator with leakage current source connected in parallel with the three NMOS transistors

leakage current sources I_{l1}, I_{l2}, I_{l3} connected in parallel with the NMOS transistors MN1, MN2, and MN3. In the CCO, the Vin- is set to be the reference voltage, which is 0.3V, and Vin+ is the capacitor voltage, which is expected to increase linearly from 0 to V_{ref}. In this input range, the MP1 and MP2 transistors are always ON, and so are the bias transistors MN3, MP3, MP4, and MP5. So we neglect the PMOS transistor leakage current and the bias transistors. And only the NMOS transistors leakage currents are considered.

Applying the KCL at the critical nodes, we have

$$\begin{aligned} I_{P3} &= I_{P1} + I_{P2} \\ I_{P1} &= I_{N1} + I_{l1} \end{aligned} \tag{25}$$

And because MN1 and MN2 are matched, the leakage current in them could be considered to be equal. Then

$$I_{N2} + I_{l2} = I_{N1} + I_{l1} \tag{26}$$

Then the charging and discharging current would be

$$\begin{aligned} I_{C/D} &= I_{P2} - \left(I_{N2} + I_{l2}\right) \\ &= I_{P2} - \left(I_{N1} + I_{l1}\right) \\ &= I_{P2} - I_{P1} \end{aligned} \tag{27}$$

So in a certain range, the leakage current has little effect on the first stage of the comparator. This range is set by the condition that the leakage current should be less than the input transistor current, namely

$$I_{P1} \geq I_{l1} \tag{28}$$

Or MN1 current has to be reversed to satisfy the KCL rule, which is unphysical. And the limit of the leakage current is hard to reach, because the input current is much larger than the NMOS leakage current. Here the input current is at the range of 10nA~100uA, so the

leakage current in the NMOS FET will be less than 10uA, which is safely below the input transistor current. The simulation results verify this point.

Next, let analyze the effect of second stage leakage current I_{l3}. Because I_{l3} directly attaches to the output node, it only slightly affects the charging and discharging time of the output capacitor. As long as $I_{P5} \geq I_{l3}$, the circuit function will not change. As I_{P5} is approximately equal to I_{P1}, and I_{l3} is close to I_{l1}, so this condition is the same condition as $I_{P1} \geq I_{l1}$. **Figure 59** shows the simulation results

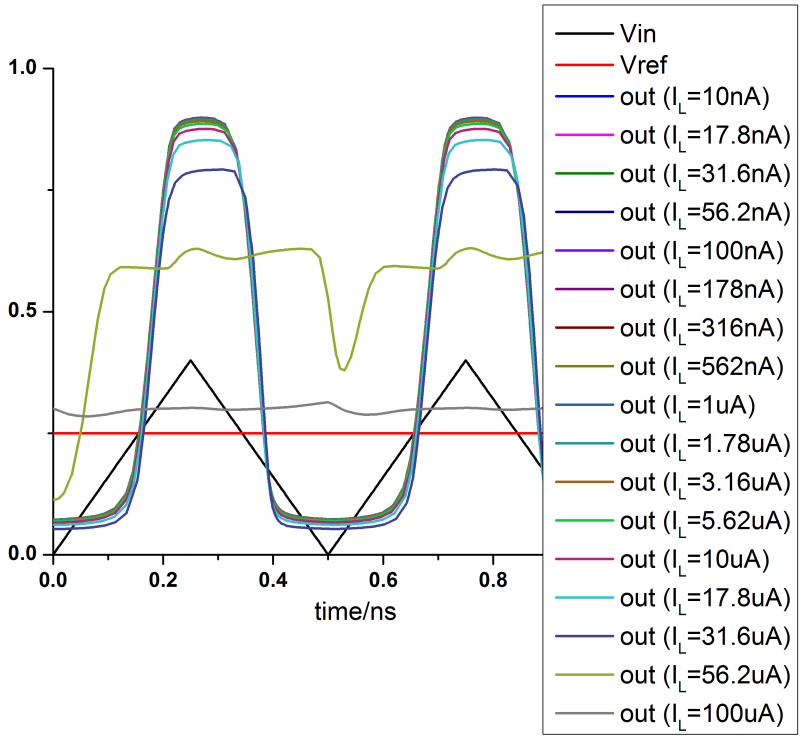


Figure 59 results of comparator with parallel leakage current source with NMOS under different current levels

of the comparator under different leakage current levels. It can be seen that up to 31.6uA, the circuit function does not change, although with a little degradation of the gain, which is a less important parameter here. At more than 56.2uA, the circuit fails to work, which is just that the leakage current is more than the bias current, and the circuit won't work in

this situation. If we can size the transistors size such that the input current is more than 10 times the leakage current of the NMOS in the comparator, for the input current detection range 10nA~100uA, the NMOS leakage current will never exceed 31.6uA. Moreover, the comparator transistor could be resized such that the bias current could be doubled or tripled, and the input current detection range could be further enhanced. All in all, we can conclude that for a certain input current range, the comparator would still work fine with little degradation. Next the whole CCO is examined and simulated.

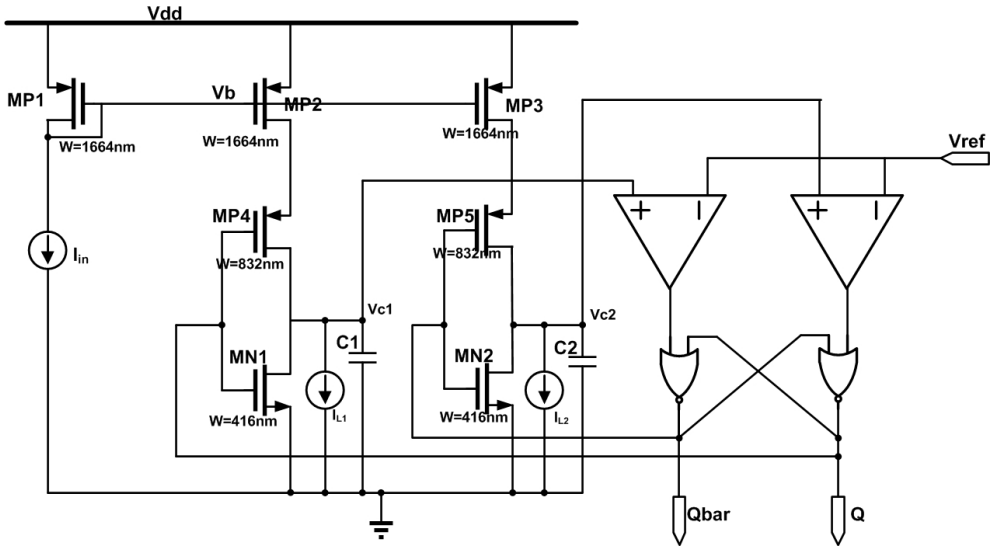


Figure 60 double capacitor CCO with leakage current source in parallel with NMOS transistors

Figure 60 shows the added leakage current sources in parallel with NMOS transistors. Examining these two sources, we conclude that as long as the leakage current level does not exceed the bias current, the circuit will still oscillate, but with a longer period. The oscillation period is known to be (10) in section 3.1.1.2, but with the leakage current, it changes to

$$T = \frac{2CV_{ref}}{I_C - I_{leakage}} \tag{29}$$

For simulation, we assume that the NMOS leakage current $I_{l1} = I_{l2} = \frac{1}{20} I_{in}$, which is just the sizing effect. Besides, the NMOS FET in the comparator has the leakage current of $\frac{1}{10} I_{in}$. The simulation results are shown in Figure 61.

From the results, it is clear that the period is longer, but it is not that significant. The behavior of the CCO does not change. So we can conclude that the leakage current would have limited effect on the CCO function, and the CCO would still function well in the presence of the leakage current.

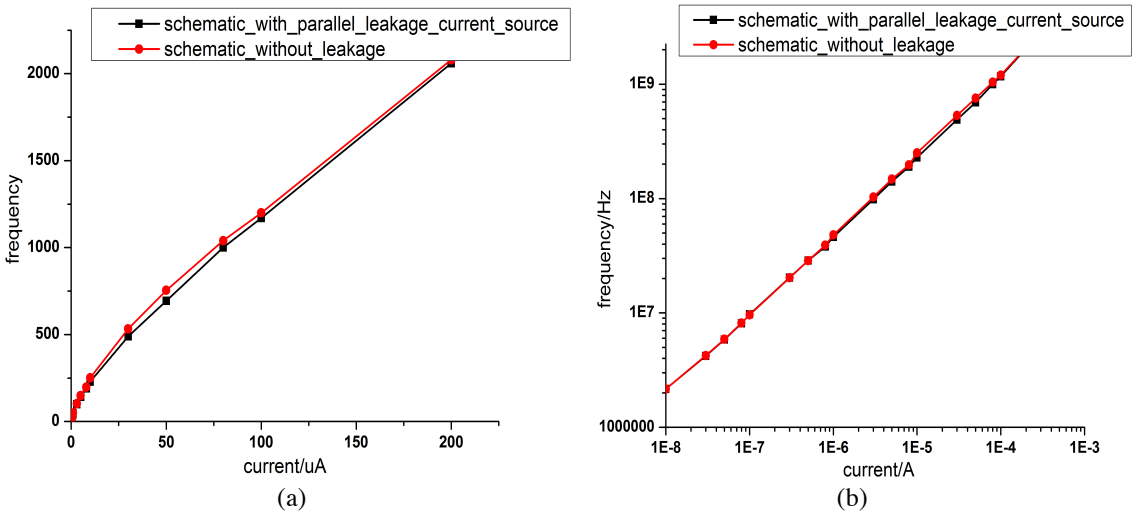


Figure 61 comparison of CCO frequency versus input current relationship between the condition of no leakage current and the condition of parallel leakage current source with NMOS (a) frequency vs. input current on linear-linear scale; (b) frequency vs. input current on log-log scale

5.3 Voltage Dependent Current Source

Next the voltage dependent current source model is included. We attach a parasitic NMOS transistor to each NMOS transistor in the CCO, and add a series voltage source

with each parasitic transistor gate to model the voltage dependent behavior. Now, let's look at its behavior in the comparator. As shown in **Figure 62**, three parasitic

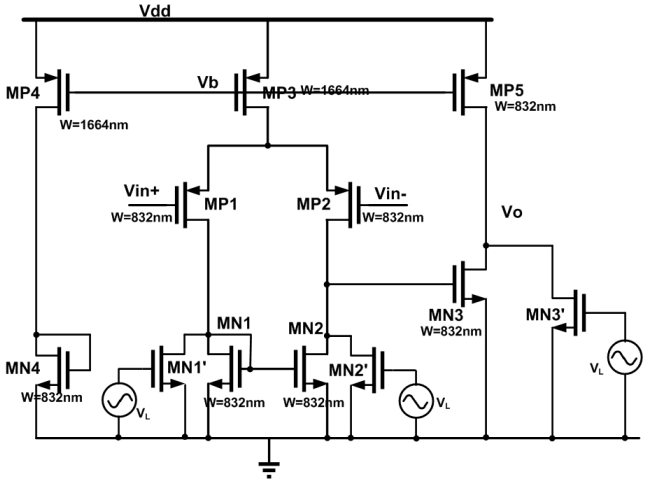


Figure 62 comparator with parallel parasitic transistor for each NMOS, and a constant voltage source is connected to gates of each parasitic NMOS

NMOS transistors, MN1', MN2', and MN3' are added in parallel to original NMOS transistors. If the original NMOS transistors are working, it means that the drain node is pulling down; the effect of the parasitic transistor effect would be diminishing, which is expected for an ON NMOS transistor. And when the original transistors are cut off, the drain node would be pulled high by the pull up branch, so the parasitic transistor effect would be more evident, which is also expected. Next we simulate this circuit for the minimum size parasitic transistors (W/L=104/40).

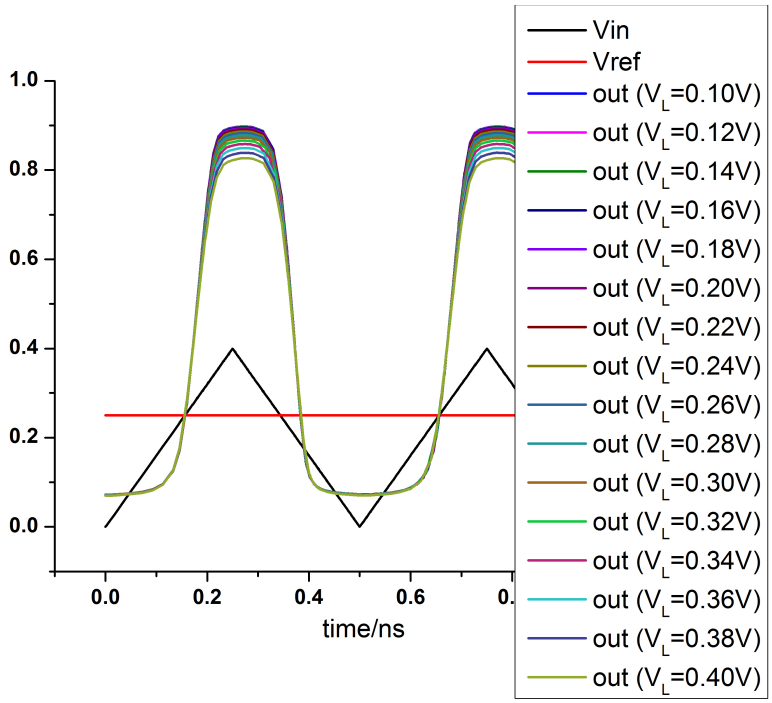


Figure 63 results of comparator with parasitic transistor biased by V_L, which sweeps from 0.10V to 0.40V

Figure 63 shows the comparator behavior under different bias conditions for the parasitic transistors. It shows little degradation to the transient performance, but there is some gain degradation of the comparator. So the comparator is reliable in this bias range. In this range, the maximum parasitic transistor current is 14uA, which is fairly reasonable compared with the maximum detection level of input current. Next, we need to examine the effect in the whole CCO structure. **Figure 64** presents the structure which includes the parasitic transistor and the series voltage source connected with the parasitic transistor gate.

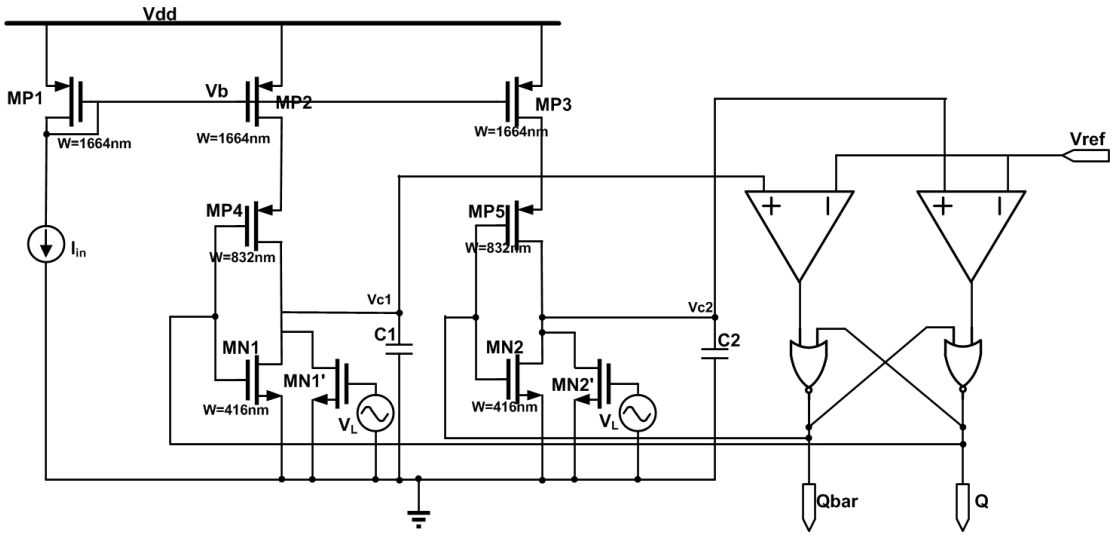


Figure 64 double capacitor CCO with parasitic transistor in parallel with NMOS transistors

When MN1, MN2 are ON, the drain node is pulled down, so that the parasitic transistor MN1' and MN2' effects are small, as they are in the deep triode region, and hence its current is very small. When MN1 and MN2 are OFF, the drain node is pulled up, so that the parasitic transistor MN1' and MN2' current is more evident. For simulation, we choose the smallest size for the parasitic transistors (W/L=104/40), and the bias such that the parasitic transistor current is approximately 1/20 of the input current.

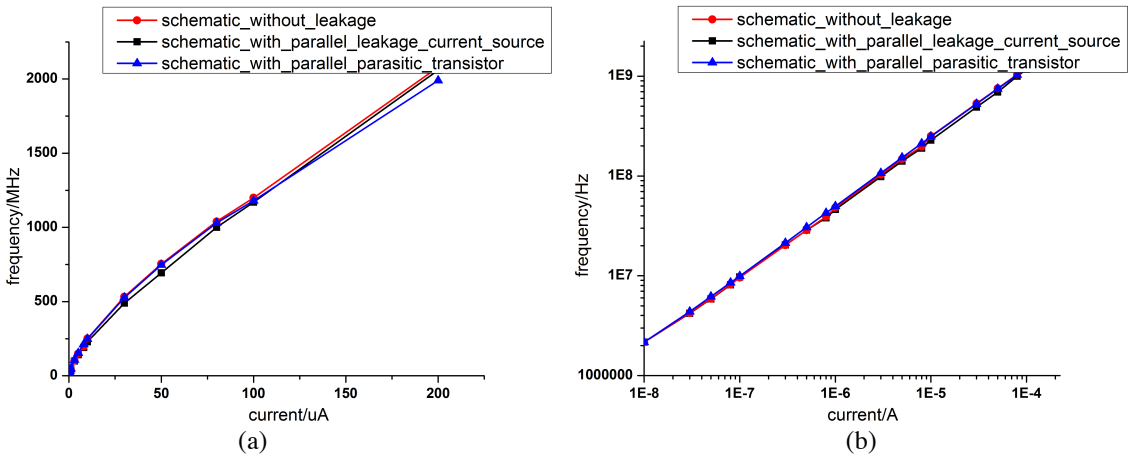


Figure 65 results of double capacitor with parasitic transistor in parallel with NMOS transistors (a) linear-linear scale; (b) log-log scale

Figure 65 compares the CCO frequency versus input current relationship in three different conditions, condition without leakage current, condition with parallel constant current source leakage current, and condition with parallel parasitic transistor. It shows that there is little change to the relationship in the detection current range as long as the leakage current follows the scaling strictly. Although it may be different in reality, we could still rely on the results in a certain range.

5.4 Conclusion

In this chapter, it is verified that when all the transistors in the circuit are exposed to the TID effect, the circuit still functions well in certain range. This range is set by the circuit bias current, which could be chosen high enough so that the circuit would function well in the input current range 10nA~100uA. Both leakage current models verify the effect, and they show similar results.

6. Conclusions and Future Work

In this thesis, a fully embedded TID monitor is designed in SOI technology. Unlike the traditional methods of designing TID monitors, which usually utilizes the radiation induced threshold voltage shift, the radiation induced leakage current method is used here. This method is simple and straightforward compared with the threshold voltage shift method; in addition, it is accurate and fully embedded.

To apply the leakage current based method, a current controlled oscillator is designed, which is used to convert the leakage current into a periodic wave for measurement. The periodic wave output could be directly measured, or its frequency could be measured through a counter and the digital word output by a shift register. The latter way of measurement is adopted here, as it provides an easy way to measure and observe. The simulation results of all the circuit components and whole system show good performance and function.

Furthermore, the key question that is needed to answer is whether the circuit will work if TID effects in all the transistors are considered. Neglecting the small threshold voltage shift induced, we verify that the circuit will still work for a certain range of increase in the leakage current. Simulation demonstrates that the leakage current tends to decrease the CCO output frequency, but not too much. But the effect is not big and the circuit works in the input current range of 10nA~100uA.

The next step is to fabricate the circuit and test it. By comparing the experiment and the simulation, the circuit function could further be verified.

Reference

[1] E.G.Stassinopoulos and James P. Raymond, "The Space Radiation Environment for Electronics", proceedings of the *IEEE*, Vol. 76, No. 11, p. 1423-1442, Nov. 1988

[2] J.L.Barth, C.S.Dyer, and E.G. Stassinopoulos, "Space, Atmospheric, and Terrestrial Radiation Environments", *IEEE, Trans. Nuc. Sci.* Vol. 50, No. 3, p. 466-482, Jun. 2003

[3] James R. Schwank, Marty R. Shaneyfelt, et al., "Radiation Effects in MOS Oxides", *IEEE, Trans. Nuc. Sci.* Vol. 55, No. 4, p. 522-538, Aug. 2008

[4] T.R.Oldham and F.B.McLean, "Total Ionizing Dose Effects in MOS Oxides and Devices", *IEEE, Trans. Nuc. Sci.* Vol. 50, No. 3, p. 483-499, Jun. 2003

[5] H.E.Boesch, Jr., F.B.McLean, J.M.McGarrity, and G.A.Ausman, "Hole transport and charge relaxation in irradiated SiO_2 MOS capacitors", *IEEE, Trans. Nuc. Sci.* Vol. NS-22, No. 6, p. 2163-2167, Dec. 1975

[6] T.R.Oldham, F.B.McLean, H.E.Boesch Jr., and J.M.McGarrity, "An overview of radiation induced interface traps in MOS structures", *Semicond. Sci. Technol.* 4, p.986-999, 1989

[7] W.L.Warren, M.R.Shaneyfelt, D.M.Fleetwood, J.R.Schwank, P.S.Winokur, and R.A.B. Devine, "Microscopic nature of border traps in MOS devices", *IEEE Trans. Nucl. Sci.*, Vol. 41, No. 6, p. 1817-1827, Dec. 1994

[8] P.J.McWhorter, S.L.Miller, and W.M.Miller, "Modeling the anneal of radiation-induced trapped holes in a varying thermal", *IEEE Trans. Nucl. Sci.*, Vol. 37, No. 6, p. 1682-1689, Dec. 1990

[9] S.N.Rashkeev, D.M.Fleetwood, R.D.Schrimpf, and S.T.Pantelides, "Defect Generation by Hydrogen at the Si-SiO2 Interface", *Phys. Rev. Lett.* Vol. 87, No. 16, p. 165506-1, Oct. 2001

[10] R.S.Muller, T.I.Kamins, and M.Chan, "Device Electronics for Integrated Circuits", p.405, third edition

[11] P.J.McWhorter and P.S.Winokur, "Simple technique for separating the effects of interface traps and trapped oxide charge in metal-oxide-semiconductor transistors", *Appl. Phys. Lett.* 48, p. 133-135, Jan. 1986

[12] N.S.Saks, M.G.Ancona, and J.A.Modolo, "Radiation effects in MOS capacitors with very thin oxides at 80K", *IEEE Trans. Nucl. Sci.*, Vol. NS-31, No. 6, p.1249-1255, Dec. 1984

[13] J.R.Schwank, V.Ferlet-Cavrois, M.R.Shaneyfelt, P.Paillet, and P.E.Dodd, "Radiation Effects in SOI Technologies", *IEEE Trans. Nucl. Sci.*, Vol. 50, No. 3, p. 522-538, Jun. 2003

[14] G.K.Celler and Sorin Cristoloveanu, "Frontiers of silicon-on-insulator", *J.Appl. Phys.*, Vol. 93, No.9, pp. 4955-4978, May 2003.

[15]W.L.Warren, M.R.Shaneyfelt, J.R.Schwank, D.M.Fleetwood, and P.S.Winokur, "Paramagnetic defect centers in BESOI and SIMOX buried oxides", *IEEE. Trans. Nucl. Sci.* Vol. 40, No. 6, pp.1755-1764 , Dec. 1993

[16]W.L.Warren, D.M.Fleetwood, J.R.Schwank, M.R.Shaneyfelt, P.S.Winokur et al. "Shallow oxygen related donors in bonded and etchback silicon on insulator structures", *Appl. Phys. Lett.* 64, 508 1994.

[17] Farah E. Mamouni et al. “Gate Length and Drain Bias Dependence of Band to Band Tunneling-Induced Drain Leakage in Irradiated Fully Depleted SOI Devices”, *IEEE, Trans. Nucl. Sci.* Vol. 55, No. 6, pp. 3259-3264, Dec. 2008

[18] V. Ferlet-Cavrois, G.Gasiot, C.Marcandella, C.D’hose, O.Flament, O.Faynot, J.d.P.d. Pontcharra, and C.Raynaud, “Insights on the transient response of full and partially depleted SOI technologies under heavy ion and dose rate irradiations”, *IEEE Trans. Nucl. Sci*., Vol. 49, p. 2948-2956, Dec. 2002

[19] http://en.wikipedia.org/wiki/Dosimeter

[20] W.Beezhold, D.E.Beutler, J.C.Garth, and P.J.Griffin, “A Review of the 40-Year History of the NSREC’s Dosimetry and Facilities Session (1963–2003)”, *IEEE Trans. Nucl. Sci*., Vol. 50, No.3, p. 635-652, Jun. 2003

[21] A.H.Siedle, “The Space-Charge Dosimeter: General Principles of a New Method of Radiation Detection”, Nuclear Instruments and Methods 121, p.169-179, 1974

[22] A.H.Siedle, and L.Adams, “RADFET: a review of the use of MOS devices as integrating dosimeters”, *Radiat. Phys. Chem*. Vol.28, No.2, p. 235-244, 1986

[23] L. Adams and A. H. Siedle, “The development of an MOS dosimetry unit for use in space”, *IEEE, Trans. Nucl. Sci*. Vol. NS-25, No. 6, p.1607-1612, Dec. 1978

[24] J. R. Schwank, S. B. Roeske, D. E. Beutler, D. J. Moreno, and M.R.Shaneyfelt, “A dose rate independent pMOS dosimeter for space applications”, *IEEE Trans. Nucl. Sci*., Vol. 43, No. 6, p.2671-2678, Dec. 1996

[25] R.C.Hughes, W.R.Dawes, W.J.Meyer, and S.W.Yoon, “Dual dielectric silicon metal oxide semiconductor field effect transistors as radiation sensors”, *J. Appl. Phys*., 65, p. 1972-1976, Mar. 1989

[26] W.R.Dawes, and J.R.Schwank, "An IC compatible ionizing radiation detector", *IEEE Trans. Nucl. Sci.,* Vol. NS-28, No. 6, p.4152-4155, Dec. 1981

[27] John Keane, Tae-Hyoung Kim, and Chris H. Kim, "An On-Chip NBTI Sensor for Measuring pMOS Threshold Voltage Degradation", *IEEE Trans. VLSI*, Vol. 18, No. 6, p.947-956, Jun. 2010

[28] Amlan Ghosh, Rahul M.Rao, Richard B. Brown and Ching-Te Chuang, "A Precise Negative Bias Temperature Instability Sensor using Slew-Rate Monitor Circuitry", *IEEE International Symposium on Circuits and Systems*, Issue 24-27, p. 381-384 May 2009

[29] M.Soubra, J.Cygler, and G.Mackay, "Evaluation of a dual bias dual metal-oxide-silicon semiconductor field effect transistor detector as radiation dosimeter", *Med. Phys.* Vol. 21, No. 4, p. 567-572, Apr. 1994

[30] Marty R. Shaneyfelt, Tom A. Hill, Thomas M. Gurrieri, James R. Schwank, Richard S. Flores, Paul E. Dodd, Scott M. Dalton, and Alex Robinson, "An Embeddable SOI radiation sensor", *IEEE. Tran. Nucl. Sci.*, Vol. 56, No. 6, p. 3372-3380, Dec. 2009

[31] Michael P. Flynn, and Sverre U. Lidholm, "A 1.2um CMOS current controlled oscillator", *IEEE J. Solid-State Circuits*, Vol. 27, No. 7, p.982-987, Jul. 1992

[32] Joseph F. Kukielka, and Robert G. Meyer, "A high frequency temperature stable monolithic VCO", IEEE J. Solid-State Circuits, Vol. SC-16, No. 6, p. 639-647, Dec. 1981

[33] M.A.Abou EL-Atta, M.A.Abou EL-Ela, and M.K.EL Said, "Current-controlled oscillator with practical implementation in phase-locked loop", *Radio Science Conference*, p.494-501, 2002

[34] Junhong Zhao, Chunyan Wang, "CMOS current-controlled oscillators ", *International Symposium on Circuits And Systems*, p.929-932, 2007

[35] Chunyan Wang, M. Omair Ahmad, and M.N.S. Swamy, " A CMOS current controlled oscillator and its applications", *International Symposium on Circuits And Systems, p. I-793~I-796, 2003*

[36] Yiwu Tang, Jianyun Hu, Jongmin Park, Jaehyouk Choi1, Lincoln Leung, Chiewcharn Narathong, and Kamal Sahota, "A 65nm CMOS current controlled oscillator with high tuning linearity for wideband polar modulation", *IEEE, Custom Integrated Circuits Conference*, Sep. 2012

[37] http://en.wikipedia.org/wiki/Relaxation_oscillator