MODELS FOR CHARACTERIZING SINGLE-EVENT EFFECTS

IN ADVANCED TECHNOLOGY CIRCUITS

By

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DEDICATION

For my daughter, Emma. I hope that you too will finish what you start in life even when

the journey is difficult and the path is unclear.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

xii

CHAPTER I

INTRODUCTION

When transistors operate in a radiation environment, ionizing particles from the environment can deposit energy and create electron-hole pairs in device junctions. In the presence of an electric field, these radiation-induced electron-hole pairs result in current flow that can cause a variety of undesirable effects. A radiation effect caused by a single ionizing particle interaction, or single-event (SE), may result in a hard error, which is destructive and requires a reset, or a soft error, which results in corruption of data. This work focuses on two main types of single-event effects (SEEs) that cause soft errors - single-event upsets (SEUs) and single-event transients (SETs).

At each emerging technology node, characterization of single-event transients and upsets is crucial to accurately predict soft error rates (SER) for circuits operating in radiation environments. The single-event sensitivity of circuit elements is experimentally characterized by fabricating a test characterization vehicle (TCV) and observing the response of the TCV to irradiation with ionizing particles. Chains of logic gates are fabricated to measure the radiation-induced node voltage transients (SETs) that can propagate through logic gates and be captured by latches. Similarly, a single-event upset is captured in storage elements on a TCV as a change in the memory's state. Data sets gathered by such testing lend insight into the relationship between technology-dependent fundamental charge collection mechanisms and design-dependent manifestations. Characterization of SEEs also provides circuit designers with data to guide radiation-hardening-by-design (RHBD) efforts to reduce or eliminate the effects of radiation.

Experimental single-event characterization is crucial for gaining knowledge about the radiation response for circuits in any given technology node. However, designing, fabricating, and testing TCVs is expensive and time consuming. Furthermore, experimental characterization ultimately captures only a subset of the information needed to gain a comprehensive knowledge of single-event effects for a technology node. Therefore, models are often developed to predict single-event behavior of circuits in the absence of data and to explore parametric sensitivity. Utilizing experimental single-event data to develop reliable, accessible models is an important step in radiation effect circuit design. As circuits scale to lower voltages and faster logic gate switching times, experimental characterization methods and existing single-event models are challenged.

First, circuit speeds increase for advanced technologies and logic gate switching times are now on the order of single-event charge collection. As these times converge, the shape of the single-event current pulse more significantly affects the circuit response than in previous, slower technologies. Static approximations for dynamic changes in circuit state during a single-event may no longer provide an accurate estimation of circuit response. Furthermore, fast single-event transients are more likely to be captured in a storage element and cause an upset as frequency of operation increases. While TCVs provide designers with a distribution of SET pulse widths and cross-sections, transient measurement circuits have fundamental measurement limitations. While fast transients are capable of causing circuit or system-level errors, every fast transient is not acquired, propagated, and measured in single-event experiments.

Second, transistors now operate at lower biases than in previous technologies. This reduction in circuit bias is beneficial for power savings; however, the effect of low-bias operation is also an increase in sensitivity to ionizing particles. The transistor structure of

FinFET devices where the gate wraps around three sides of the channel has further enhanced operation such that transistors operate in reduced, near-threshold biases. Modeling to assess the impact of circuit bias on single-event effects allows circuit designers to weigh the benefit of decreasing power consumption and cost of increasing radiation sensitivity.

Increasing logic gate switching speed, reduced circuit bias, and limitations for experimental characterization of single-event effects all necessitate development of single-event modeling for advanced technologies. In this work, the following models are given for characterizing single-event upsets and transients given that circuits operate at lower biases and faster speeds than in previous technologies:

- **Analytical Single-Event Upset Model:** An analytical model has been developed for predicting the charge to upset memory circuits where charge collection and circuit response happen concurrently.

- **Experimental SEU Logic Cross-Section Estimation:** Single-event transient data is used to predict single-event upset logic cross-sections for technologies where transient pulse widths are on the order of clock periods.

- **Empirical SEU Model for Bias Variation:** A model for evaluating bias effects on transistor sensitive area has been developed for the 14/16nm technology generation.

- **Extracting Fast Single-Event Transients:** Single-event upset data is used to extract SETs that are not experimentally captured in SE characterization measurement circuits.

- **Evaluating Drive Current Effects on SETs for Bias Variation:** A method has been

developed for evaluating bias effects on single-event transient cross-sections and pulse widths using drive current analysis.

In Chapter II, background information about single event characterization and technology advancement are presented. Chapter III details three models developed to characterize single-event upsets for advanced technologies. First, a state space model developed to analytically characterize single-event upsets in memory elements is presented. The model takes into consideration the single-event waveform shape in order to predict whether or not an upset will occur in static random access memory (SRAM). Second, a model for estimating logic SEU cross-section given experimental SET data is derived for circuits where transient widths are on the order of logic gate switching times. Third, data from irradiation of a 14/16nm flip-flop are used to develop an empirical model for predicting SEU cross-section for variation in circuit bias that incorporates an analysis of transistor sensitive area. In Chapter IV, two models for characterizing single-event transients are given. The issue of increased circuit switching speed is addressed through a model that extracts fast single-event transients from single-event upset data. Analyses of the impact of these fast transients on single-event upset cross-sections is also presented. Finally, an evaluation of the effect of bias variation on SETs in FinFET transistors allows circuit designers to gain insight into SET distributions from transistor drive currents. Chapter V concludes the dissertation by discussing the impact of key points and findings from this work. Information about the 14/16nm bulk FinFET and 32nm SOI test chips and SEU data referred to frequently in this dissertation are given in Appendix A. Appendix B contains the comprehensive derivations for two of the presented models presented. Appendix C contains scripts in Matlab code that were used to implement the analytical model of Chapter III.

CHAPTER II

BACKGROUND

Single-Event Effects

When ionizing particles traverse silicon, losing energy, electron hole pairs are created which deposit charge in the device. The amount of energy lost is the particle's linear energy transfer (LET) and depends on the particle type and energy. This deposition of charge on a circuit node can result in a variety of SEEs depending on the LET and the location and angle of incidence of the strike. The likelihood of a single particle causing an error is directly related to the particle's linear energy transfer. Higher LET particles are generally more likely to cause errors in circuits than low LET particles. In fact, trends often vary from low LET to high LET particle irradiation for varying circuit design and operation factors [16].

While the first cosmic-ray-induced single-event upsets in space were first confirmed in 1975, it was still years later before SEUs became a popular and important topic for discussion not only for space applications, but for terrestrial applications as well. In 1980, the term single-event upset was coined by Guenzer et al. to describe any ionization event which caused an error in circuit memory [17]. Single-event upsets can occur in storage elements in two ways: when a single-event transient is captured or when an internal node is struck by a single-event particle and the state of the cell is changed. In the 1980s, as single-event transients were just being discovered, most single-event research focused on internal upsets in latches, registers, and memories. Several experiments were performed on SRAMs, as they accounted for a large portion of circuit memories. The schematic for a mixed-mode simulation of an SRAM consisting of a pair of back to back inverters is shown in Fig. 1.

Through experimental characterization, it was discovered that a particle LET threshold existed above which an upset will occur and below which it will not in the SRAM. This threshold was found to be dependent on which of two events occurred faster- the feedback of a voltage transient through the feedback inverter or the recovery of the struck node. Fig. 2 shows the results of simulated particle strikes to an SRAM by Dodd et al. [1]. The LET threshold is identified by the dashed line before which no upset would occur and after which an upset would occur. The figure shows both total collected charge and the significant charge to upset defined by the time it takes for a single-event to switch the feedback inverter to the opposite state.
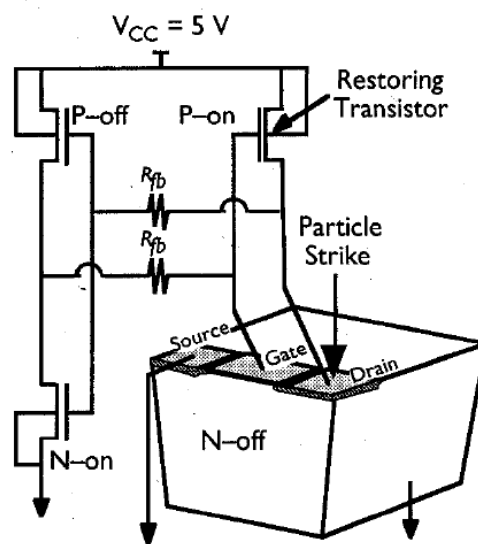
Figure 1: Mixed-mode simulation of an SRAM with an NMOS single-event particle strike [1].

Since the SRAM single-event upset threshold was first discovered, the concept of critical charge has been widely used to approximate the charge delivered by a single-event that will cause an upset to a memory element. The critical charge is the static approximation of the total charge deposited by a single-event that will completely alter the state of a memory
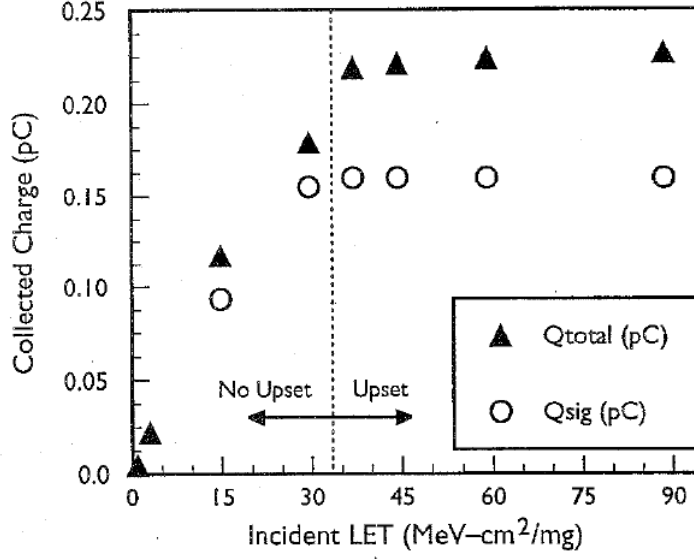
Figure 2: Identified LET threshold for an SRAM in 1.25 micron technology from simulated collected charge simulations for different LET particles. [1].

circuit node (Q_{crit}=C×V_{DD}). This critical charge value can be related to a single-event particle LET, from which designers can determine an error rate for a circuit or system for a given radiation environment. Particle LET and deposited single-event charge are related by the following equation [5]:

$$Q_{Dep}[pC] = 1.035 \times 10^{-2} \times LET \times L_{col}[\mu m]. \tag{1}$$

Although single-event transients were discovered in the early 1980s, their presence was initially more of a research interest than any type of major concern for space applications [18]. The acronym SET wasn't coined until 1990 in a work by Newberry et al. that experimentally measured transients [19]. Single-event transients occur in logic cells and (as their name implies) are transient, lasting only a period of time. An SET will only cause an error if it propagates through a circuit from the place of its origin and is captured in a storage element as a single-event upset.

Soon after the discovery of the SET, both simulation and experimental research confirmed

7

a "window of vulnerability" in which a sequential element was susceptible to capturing SETs. However, in the 1980s, relatively low clock speeds made the timing necessary to capture an SET unlikely. An experiment performed in 1987 by Koga and Kolasinski revealed significant sensitivity to SETs. While the authors considered this response to be atypical, they said the presence of SETs could be a warning of what may come [20]. Soon the potential of SETs to disrupt entire systems became evident as transients were measured to be growing in width for high LET irradiation. In just a decade, SETs became well-known sources of error that seemed only to be getting worse with technology scaling.

Characterization of Single-Event Effects

Experimental techniques for characterizing single-event effects are employed at each new technology node in order to identify mechanisms, create error mitigation schemes, and predict single-event response. First, identifying the mechanisms that cause single-event errors is particularly important as technology scales and device structure changes can impact SE charge collection mechanisms [21, 22]. Single-event upset and transient characterization is also imperative for developing radiation-hardening-by-design techniques to mitigate single-event effects. For example, circuit designers rely on accurate single-event transient distributions for knowledge about the width of transients an RHBD circuit should mitigate in order to effectively harden the circuit [23, 24]. Single-event transient data provides circuit designers with critical information to build these mitigation schemes with confidence. Finally, single-event characterization is important for predicting single-event response. Models are developed based on characterization data that designers can use to predict single-event effects for a variety of circuit types [25, 26].

In order to experimentally characterize single-event effects, chains of logic or memory

elements (or both) are irradiated with ionizing particles of various linear energy transfer. Single-event upsets and transients are captured in real time and the data provides information about the radiation hardness of a given transistor type, process, or circuit design. The data is most often given in terms of single-event transient or upset cross-section for a specific particle LET, where the cross-section is calculated as follows

$$\sigma_{SET} = \frac{\# \, SETs \, / fluence}{logic \, elements \, per \, chain}$$

(2)

$$\sigma_{SEU} = \frac{\# \, SEUs \, / fluence}{storage \, elements \, per \, chain.}$$

The single-event cross-section can be interpreted as the sensitive area of the irradiated circuit element. Measuring single-event transients and upsets continues to be an important step towards quantifying radiation effects in any given technology, as well as understanding the mechanisms involved in transient generation, propagation, and capture. Only by identifying how SEs affect circuits and systems can designers work to design better systems for radiation environments. The following subsections provide more background and information about state-of-the-art single-event upset and transient experimental characterization. The section concludes with the experimental limitations that serve as the inspiration for the models developed in this work.

SEU Characterization

In the 2000s, at-speed testing to capture the single-event upset response of memory cells became increasingly difficult due to the need for high-speed testing equipment and complicated test setups. So, in 2005, Marshall et al. created the circuit for radiation effects self test (CREST) design which allowed for built-in self testing. Fig. 3 shows the block diagram for CREST [2].

9
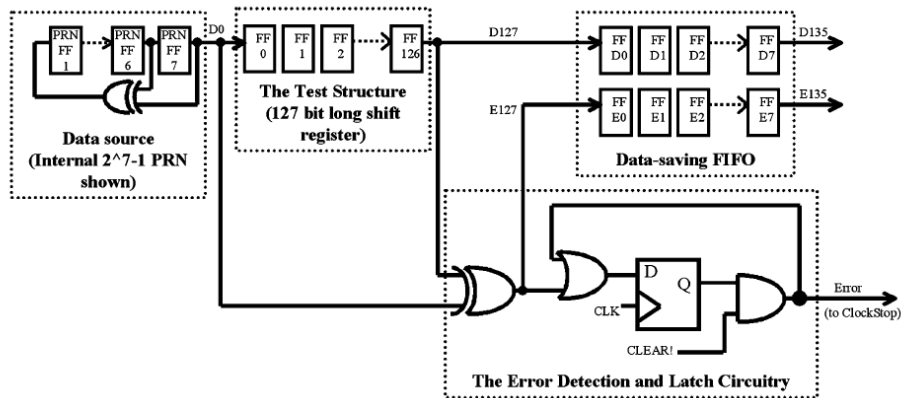
Figure 3: The CREST built-in self test architecture for single-event upset capture [2].

CREST uses a shift register of flip-flops as a radiation target and measures the number of upsets that occur in the chain of cells when exposed to radiation. The single-event upset cross-section per flip-flop can then be found by dividing the number of SEUs by the number of flip-flops. This cross-section can be correlated with the sensitive area of a single cell. The CREST design has been widely used since its debut for characterizing single-event upsets in a variety of flip-flop and other memory cell designs. Since the first SEU capture circuits were built, several modifications and improvements to the basic concept of SEU characterization circuits have been implemented in subsequent technologies [27, 28, 15]. Improvements include on-chip error counting, a checkerboard pattern generator, and at-speed testing with an on-chip clock.

SET Characterization

In the 1990s, curiosity and concern over the increase in circuit errors resulting from SETs motivated several researchers to develop experimental test setups in order to measure transients in standard circuit elements. In 1997, Buchner et al. implemented a test setup

10

using a pulsed laser to characterize the SET response of strings of inverters [29]. In the same year, Baze et al. developed a test structure for performing heavy-ion testing on logic gates. The test structure consisted of long chains of identical logic gates followed by a sequential element for capturing SETs generated at any location in the chain. Under irradiation or a laser pulse, an SET could be generated in any of the logic gates and would then propagate to the output of the chain where it would be recorded along with the transient's width.

After several years of measuring SETs from long chains of logic gates, it was discovered that transients can be significantly distorted by passing through subsequent gates and the problem grew in proportion to the length of the chain. The realization of pulse attenuation and broadening through long chains of inverters invalidated data sets and drew attention to the phenomenon termed propagation-induced pulse broadening (PIPB) [30, 31]. As a result of this discovery, more recent SET characterization circuits have been designed with short chains of logic that converge to a single output as shown in Fig. 4. The challenge of combining short SET test chains is only rivaled by the challenge of measuring transient width. Ultimately, the effects of modulation due to SET propagation and resolution limitations imposed by measurement circuits cannot be fully overcome. Therefore, the measurement limitations of any given experimental design must be carefully considered when interpreting single-event transient data.

For SET measurement, various implementations of logic gate and measurement circuitry have been designed, fabricated, and tested. In analyzing the impact of single-event transients on logic circuits, the total number of transients generated along with the distribution of pulse widths contributes valuable information for understanding and mitigating SET effects. Influenced by the CREST design in [2], Ahlbin et al. created a test chip design approach called Combinational Circuit for Radiation Effects Self-Test (C-CREST) that

11
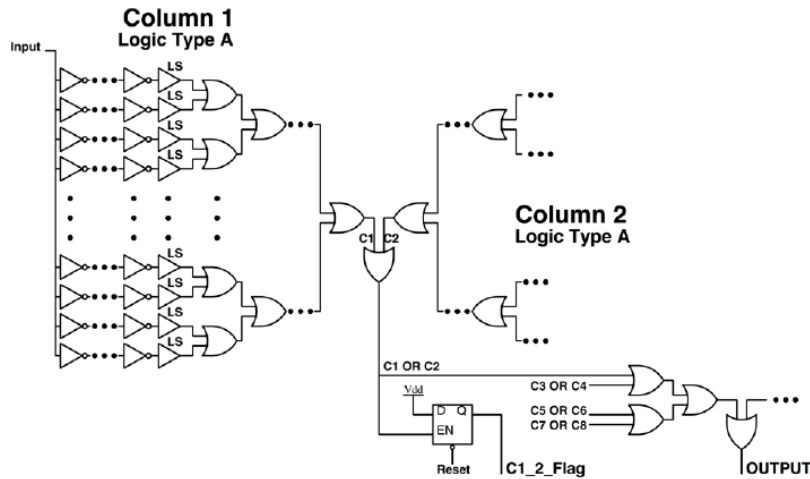
Figure 4: Short chains of logic connected to a common output by OR gates in order to reduce pulse attenuation or broadening as transients propagate through the test chains [3].

allows SETs in combinational logic to be distinguished from SEUs in latches. Like the original CREST design, C-CREST has been implemented and improved upon for many technology generations. In 2006, Narasimham et al. developed an autonomous on-chip single-event transient pulse width measurement circuit with a similar design [32]. This design was modified to quantify pulse attenuation and broadening through logic chains by Loveless et al. in 2012 for 45nm silicon-on-insulator (SOI) technology SET characterization as shown in Fig. 5 [4]. A similar design was also implemented in 32nm SOI technology [12]. SET measurement circuits have continued to improve with the use of a Vernier delay line topology, first implemented in 2010 by Harada, et al. [33]. In 2017, a study was performed to evaluate the quality of several SET measurement circuit typologies by Glorieux et al. that detailed the results from three different measurement circuits all fabricated on the same 65nm test chip [34]. Most recently a 14/16nm bulk FinFET SET test chip was designed with both well established and novel features including a Vernier Delay Line topology measurement circuit and a heterogeneous target design which greatly reduced testing time [3].
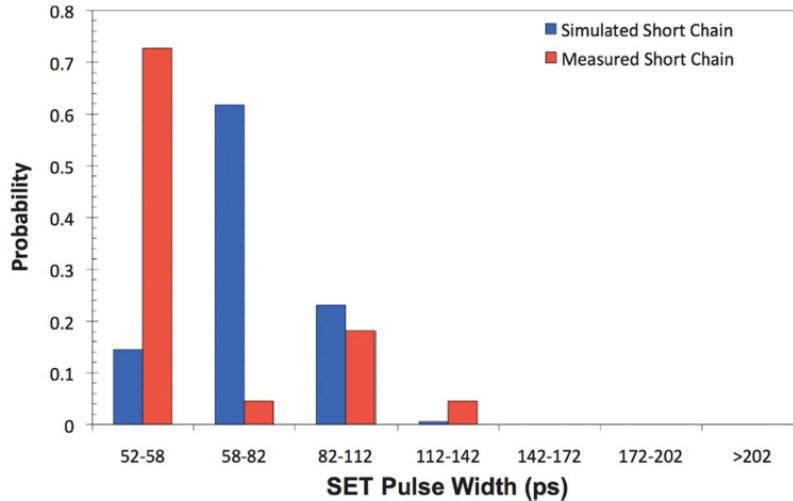
Figure 5: SET pulse width distribution measured experimentally compared with simulated pulse widths for 45nm SOI technology [4].

Experimental Limitations

Experimental characterization of single-event upsets and transients is invaluable, however, performing tests to extract this information becomes increasingly complex and expensive as technology advances. Chains of thousands of flip-flops or other memory elements must be fabricated in order to gather sufficient data to draw conclusions about technology, circuit design, or circuit operation. For SETs, a variety of measurement techniques have been implemented, however these designs have a fundamental limitation in the ability to measure fast SET pulses [3, 35, 34, 4]. Reasonably high numbers of devices must be included in a target to gather SET data in a manageable amount of test time. This limitation results in using long chains of devices where fast pulses may not propagate and be captured, compared to typical logic paths in circuits where fast SETs can propagate and cause errors. While methods of combining shorter chains of inverters have been implemented to mitigate this problem, some attenuation still occurs for fast transients. Another measurement limitation is that even the most advanced SET measurement circuits such as the Vernier

13

Delay Line topology require a minimum pulse width threshold in order for the transient to be captured in a flip-flop to trigger the measurement circuitry. Fundamental transient measurement limitations along with the increasing importance of knowledge about fast SETs with frequency scaling indicate that modeling efforts to extend knowledge in this area are increasingly important.

In conjunction with experimental results, modeling efforts that provide insight into radiation response over a variety of parameters are useful for circuit designers to predict circuit response and develop radiation hardened designs. Several types of models exist for analyzing single-event effects at different levels of the design process. A SE model is often developed at either the device, circuit, or system level. Circuit-level models provide an often desired balance between accuracy and speed of computation. While a device-level model will give the most accurate result, the computation time can be a drawback to using these models and can even make these models unavailable because of the necessary computing time and resources. Furthermore, modeling every test case using device-level modeling is rarely justified as a good use of limited time and resources for single-event modeling. Therefore, device-level models are primarily useful for specific unknown test cases and when searching for particular mechanistic anomalies. A system-level model, on the other hand will provide results quickly for a large number of test cases. However, the accuracy of the results is often sacrificed due to a lesser degree of detail implemented for each element of the system. System-level modeling can be particularly useful for quick estimates and general knowledge about single-event errors. These models also cannot give insight into how circuit or device level parameters influence the results. For these reasons, circuit-level modeling is an excellent choice when designers desire single-event effect knowledge based on circuit parameters in a timely manner.

Technology Advancement

In 1965, Gordon Moore first predicted that the number of transistors on an integrated circuit would double every two years. Since then, technology has continued to scale as predicted. This technology scaling results in smaller devices, lower circuit operating voltages, and faster gate switching times. While these advancements provide excellent power, area, and speed metrics for advanced technologies, they can conversely contribute to increased radiation sensitivity [36, 37, 8, 38]. These factors associated with technology scaling affect how single-event effects manifest at each new technology node.

Beyond changes in transistor size, technology advancements including the silicon-on-insulator process and FinFET transistor structure result in different single-event charge collection mechanisms [21, 22]. Silicon-on-insulator technology was first introduced for its reduced sensitivity to latchup due to the isolation of individual transistors [5]. Fig. 6 shows the charge generation and collection in a SOI device. SOI technology offers the potential for an increase in radiation hardness over bulk technology because the buried oxide limits the amount of charge that can be collected from a single-event strike. Despite the limited charge collection, SOI devices do not always provide a more robust design. Gain from the parasitic bipolar in SOI technology can increase the effect of single-event current, resulting in comparable radiation sensitivity to bulk technologies [5, 39]. More recently, FinFET devices have emerged as an alternative to planar transistor structure that allows technology to follow Moore's law scaling. Fig. 7 shows the FinFET transistor structure that provides better gate control and lower bias operation compared to planar technologies.

As transistors evolve and change in size and structure, models for single-event effect characterization must continually be evaluated. This dissertation will focus on two major outcomes from advances in technology and their impact on single-event effects: increased
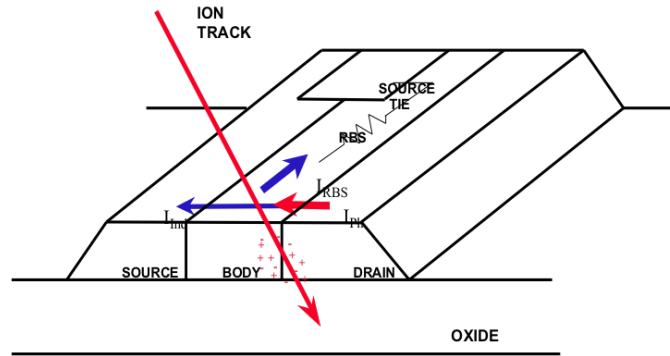
Figure 6: Illustration of charge generation and collection in a silicon-on-insulator transistor [5].
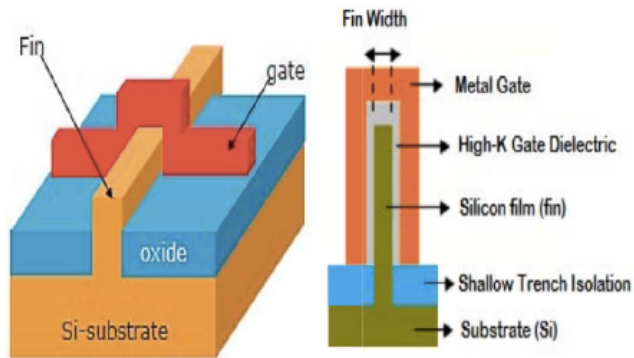
Figure 7: FinFET transistor structure where the gate wraps around three sides for increased gate control compared with planar transistor structure.[6].

circuit speed and reduced circuit voltage.

Increased Circuit Speed

As technology scales, the switching speed for logic gates increases and circuits can operate at higher frequencies. For combinational logic this increase in frequency of operation corresponds to an increased likelihood that a single-event transient will be captured in a memory element [40, 29, 7, 41, 42]. A study on 40nm bulk technology illustrates the increase in cross section of transients latched in combinational logic with increasing frequency, where the logic upsets overtake flip-flop upsets around 1 GHz as shown in Fig. 8 [7]. Due to this increase in contribution to SER, SEUs resulting from transients generated in combinational logic are important to model with accuracy. These upsets are modeled based on single-event transient data; therefore, reliable single-event transient characterization is imperative [43, 44].
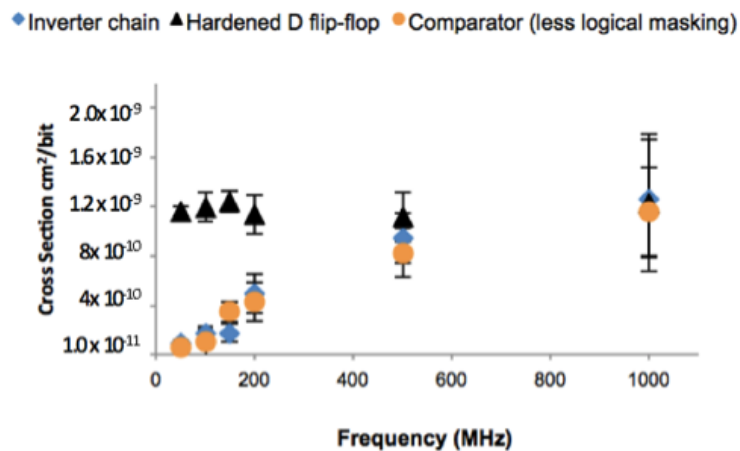
Figure 8: SER vs. Frequency (40nm bulk) shows combinational logic cross section contributes significantly to SER as frequency increases [7].

For memory elements, the threshold for upset along with saturated SEU cross-section

are the most important parameters for circuit design and radiation environment error rate calculations. The majority of ionizing particles in any radiation environment are particles with low LET. When calculating a soft error rate for a circuit, an increase or decrease in the LET threshold for a circuit can equate to including or excluding error contributions from an entire species of ionizing particles. For many years the metric for defining a single-event upset LET threshold has been the amount of collected charge at a node that is needed to change the cell state, or critical charge (Q_{crit}).

Previously, charge collection from a single-event strike occurred on a much smaller time scale than circuit switching and the amount of deposited charge could be integrated over the transient event time and summarized by a total deposited charge value. Now that the circuit response time is on the same order as single-event charge collection, the time profile of charge collection in relation to circuit switching is of growing importance [45].

The following quotation from Dodd and Massengill in [45] summarizes the issue at hand as technology scales and circuit switching speed increases:

> "If the response of the circuit at the [single-event charge] collecting node is much slower than the characteristic time constant of the SE pulse, then the pulse is effectively integrated by the nodal capacitance and only the total charge delivered by the pulse is important to the circuit response. If, however, the time constant at the node is much sorter than the time constant of the SE pulse, then the circuit responds to the delivered charge faster than the pulse can deliver it, so the pulse shape is critically important to the circuit response. These concepts are essential to the accurate modeling of SEUs at the circuit level, since they define the boundary between valid modeling using only the collected charge and modeling requiring a more accurate description of the time profile of the charge

collection"

Reduced Circuit Voltage

Reducing circuit supply voltage is a commonly used technique for reducing power consumption because of the quadratic relationship between supply voltage and power [47, 48, 8]. One of the advantages of technology scaling is the ability for circuits to operate at lower supply voltages. Advances in technology structure further promote reduced bias operation. For example, because of the 3D structure where gate encompasses channel region on three sides, FinFET-based circuits operate at supply voltages as low as near-threshold-voltage [49].

Reduced voltage improvements in power consumption are generally realized at the expense of an increase in single-event cross-section [23, 8, 36, 50]. Single-event transients have been shown to increase in both duration and number with decreasing bias, making circuit errors due to transients more difficult to mitigate [51, 36, 23]. A reduction in bias has also been found to increase propagation-induced pulse broadening [52]. Therefore, the effect of pulse propagation at low biases must be quantified through controlled bench tests in order to accurately interpret SET data [23, 3]. Results from a 14/16nm SET characterization test chip are shown in Figs. 9 and 10 illustrating the increase in SET cross-section and duration from nominal 0.8 V bias to 0.45 V bias.

Single-event effect experiments on flip-flops have shown an increase in SEU cross-section, particularly for low LET particle irradiation, over bias [8]. Recent publications have analyzed supply voltage scaling for particles with low LET values for advanced FinFET nodes [50, 8] and these works attribute increased SEU cross-section with decreasing supply voltage to classical critical charge arguments [53, 44]. For a single-event upset to occur, the collected
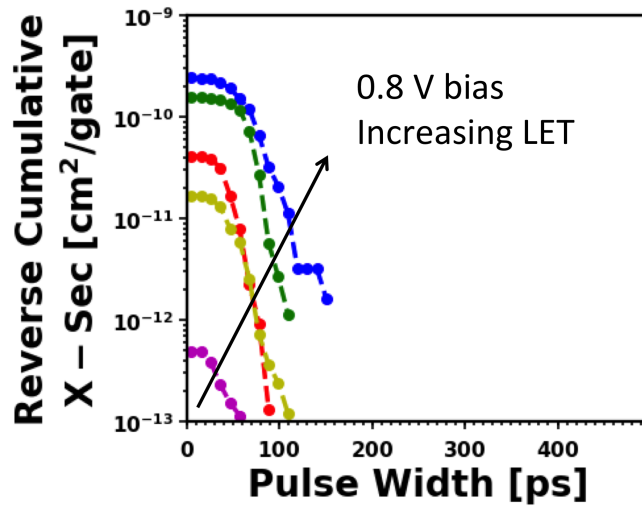
Figure 9: Single-event transient reverse cumulative cross-sections at nominal 0.8 V bias with increasing particle LET.
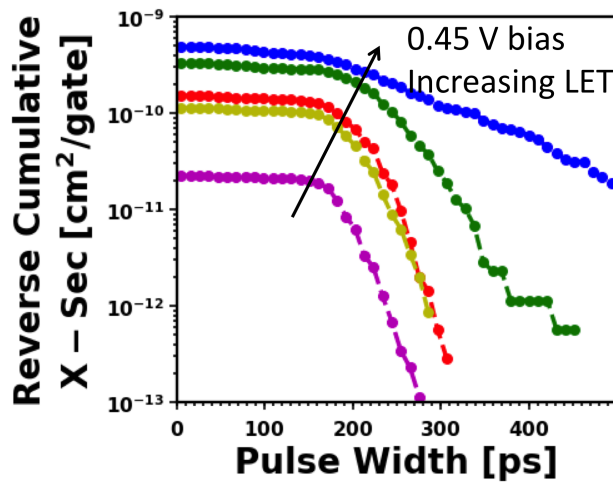
Figure 10: Single-event transient reverse cumulative cross-sections at low 0.45 V bias with increasing particle LET. Note that the transients are longer and cross-sections are higher at low bias vs. nominal bias in Fig. 9

charge on a node (Q_{coll}) must exceed the node's critical charge (Q_{crit}). Voltage scaling fundamentally changes the critical charge of a circuit node by changing the nodal voltage. Increased single-event upset cross-section has been observed with voltage scaling because the charge necessary to change the state of a storage element decreases with decreasing supply voltage.
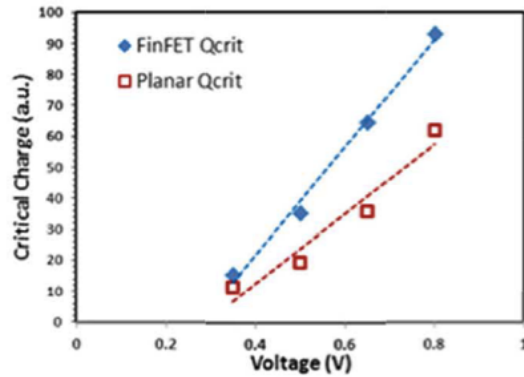
Figure 11: Supply voltage vs. critical charge for a 20nm bulk planar technology and 16nm bulk FinFET technology, found using SPICE simulations. Both technologies show a sharp decrease in critical charge with decreasing supply voltage [8].

Fig. 11 shows a SPICE simulation of critical charge for two different technology nodes [8]. The FinFET and bulk planar technologies both reveal a strong decrease in critical charge with reduction in supply voltage, which leads to an exponential increase in SE cross-section.

CHAPTER III

MODELS FOR CHARACTERIZING SINGLE-EVENT UPSETS

Several models have been developed over the years for predicting single-event upsets in memory elements. In this chapter, assumptions driving the outcome of these models are reevaluated and analyzed in light of technology advancement to low bias and high frequency operation. The following analytical, experimental, and empirical models offer different model approaches to advancing radiation-effect-aware circuit designer perspectives on two of the most important and impactful technological advancements: increased circuit speed and reduced circuit bias.

Two models are presented that address the effect of increased circuit speed for internal latch and external logic SEUs. Increased circuit speed is synonymous with decreased clock period. With clock periods decreasing to the time scale of single-event transients, assumptions regarding logic SET capture must be reevaluated. Furthermore, analyses must consider concurrent circuit operation and single-event current. The first two subsections in this chapter highlight the impact of increased circuit speed on single-event upset analysis and provide alternative models with valid assumptions for advanced, high frequency operation technologies. A third model is presented to give an accurate description of the change in SEU cross-section in 14/16nm bulk FinFET technology with decreased bias operation.

Analytical Single-Event Upset Model

Analytical models can be used relatively quickly (compared with experimental or simulation approaches) and with a high degree of accuracy. This type of model also gives

circuit designers insight into the the effects of changing node capacitance, device threshold voltage, etc. on single-event response that is not gained from experimental or simulation analyses. Furthermore, the insight provided by analytical models can be used in developing radiation-hardened-by-design circuits. A designer can determine how variation in circuit parameters influences radiation hardness and weigh the options for increasing hardness compared to circuit performance.

As circuit speeds increase for advanced technologies, single-event charge collection and circuit operation now occur on the same time scale and the shape of the current pulse more significantly affects the circuit response than in previous technologies. Single-event induced current in a transistor has long been modeled by a double exponential waveform. However, detailed device studies on FinFETs in technology computer-aided design (TCAD) at the physical level have prompted the development of an error function current model [10]. The single-event induced current described by the error function model more accurately describes the temporal single-event response of advanced technology, fast-switching devices compared to the traditional double exponential current source [46, 23].

In this work, a state space analytical model has been derived by the method of [54] to find the charge to upset an SRAM given a single-event current error function waveform within 10% of simulated data-validated results. Beyond the experimental response of test structures to irradiation, predicted response using circuit simulators, and simple static approximations, the model will provide a comprehensive look at variable factors affecting SE response. The model will give insight into the mechanisms involved in producing a particular circuit response. The developed model describes single-event transient capture in an SRAM as a means for providing insight into the single-event response of any bistable memory circuit. The model has furthermore been used to identify how circuit design and operation parameters

23

affect single-event capture in advanced technologies where fast transients occur on the same time scale as circuit operation.

State Space Modeling Overview

State space modeling, a particular type of analytical modeling has been developed to evaluate the response of an SRAM to transient noise. Dynamic state space analysis was first performed for transient noise effects on SRAMs by Zhang et al.in 2006 [9]. The developed analytical model has been utilized specifically for modeling single-event upset noise in subsequent works [54, 55]. Each of the models gives an analytical solution to the state space model in order to solve for the critical charge necessary to change the state of the SRAM and cause an SEU.

A state space model is a set of first order differential equations that describe how a physical system changes in time by relating input, output, and state variables. Equation (3) is the general form of a continuous time-invariant state space model

$$\mathbf{x}(t) = A\mathbf{x}(t) + B\mathbf{u}(t)$$
$$\mathbf{y}(t) = C\mathbf{x}(t) + D\mathbf{u}(t)$$

$$(3)$$

where $\mathbf{x}$ is the state vector, $\mathbf{y}$ is the output vector, and $\mathbf{u}$ is the input vector. The matricies A, B, C, and D are the state, input, output, and feedforward matricies respectively.

The state vector $\mathbf{x}(t)$ contains the smallest subset of system variables that can represent the entire system at any given time. How the state vector changes over time depends on the current state of the system and inputs to the system $\mathbf{u}(t)$. Any outputs of the system are defined in the vector $\mathbf{y}(t)$, which can also be related to the state and input vectors.

A state space model of a system is useful for determining what will happen in the system over a very long period of time (as time approaches infinity). An attractor is a set of

numerical values toward which a system tends to evolve over time without external influence. The attractor(s) for a state space model can be found by considering the eigenvalues of the state matrix A in (3) which define the stability of the system. Each attractor of the system has a defined region of attraction which is the state space associated with that attractor. Any state in the region of attraction will eventually converge to the attractor in the absence of external influence (i.e. **u(t)**=0).
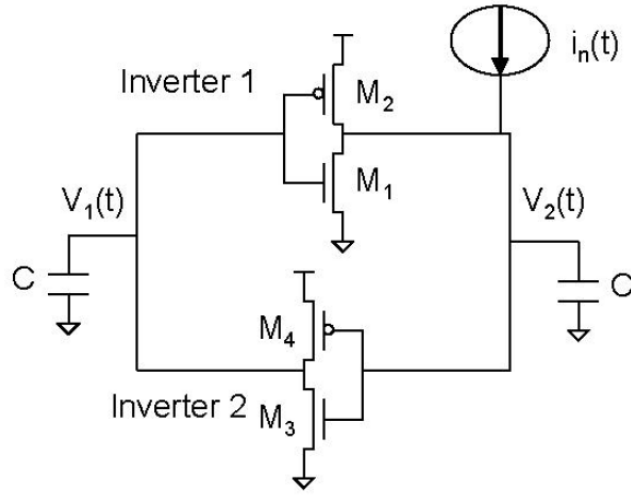
Figure 12: 6T SRAM cell with transient noise injected at node $V_2(t)$ (access transistors not shown) [9].

Dynamic state space analysis was first developed for a 6T SRAM cell by Zhang et al. for a symmetrical SRAM, as shown in Fig. 12. The transient noise current injected at node V_2 was first modeled as a rectangular pulse of amplitude I_n and pulse width T_{crit}. In subsequent works, this transient noise current has been modeled as a double exponential pulse to simulate a single-event particle strike [54, 55]. The double exponential current is described by

$$I_\mathrm{n}(t) = \frac{Q}{\tau_\mathrm{f} - \tau_\mathrm{r}}(e^{\frac{t}{\tau_\mathrm{f}}} - e^{\frac{t}{\tau_\mathrm{r}}})[56] \tag{4}$$

25

where Q is the total charge delivered by the single-event, I_n is the maximum current in the waveform, τ_r is the rise time constant of the waveform, and τ_f is the falling time constant of the waveform. The state vector $V=(V_1,V_2)$ describes the state of the cell and the set of V of all possible values forms the state space.

Dynamic equations based on the charging and discharging of the capacitors in Fig. 12 describe the system behavior of the SRAM due to the inverter currents, which are a nonlinear function of the inverter input and output voltages. In [9], the inverter currents are approximated as linear functions to reduce the complexity of the system so that an analytical solution can be found. A linear gate model developed by Horowitz is used to approximate and linearize inverter currents the state space model [57]. The gate model for an inverter with the NMOS transistor conducting is:

$$I_{inv}(V_{in}, V_{out}) = \begin{cases} 0 & \text{cutoff} \\ g_{mn}(V_{in} - V_{tn}) & \text{saturation} \\ V_{out}/R_n & \text{linear} \end{cases} \tag{5}$$

where g_{mn} is the transconductance, V_{tn} is the threshold voltage, and R_n is the linear-region resistance. In the linear gate model, the drive curves for an inverter are approximated by regions of zero slope (low gain) and infinite slope (high gain). The linear gate model assumes that the inverter output current is a function of either the input voltage or the output voltage, but not both. The saturation region is referred to as the high gain region while the linear region is referred to as the low gain region.

An SRAM has the following attractor states:

1. $(V_1,V_2)=(V_{DD},0)$

2. $(V_1,V_2)=(0,V_{DD})$

3. $V_1 = V_2$

After the transient noise in Fig. 12 disappears, the state vector will be driven to one of these three attractors over time based on the location of the state vector at the time the transient noise ceases. For the SRAM cell, the boundary for the regions of attraction is $V_1 = V_2$. Put simply, the state vector must be moved beyond the attraction region boundary by a transient noise source in order for a change in state to occur in the SRAM. Otherwise the SRAM will return to its original, unperturbed state.

The SRAM's transient noise response is divided into two regions: weak coupling mode and strong feedback mode. For the initial response only the struck node voltage varies significantly from its original value. In the strong feedback mode both node voltages vary over time. For example, in Fig. 12, assuming $V_1 = V_{DD}$ and $V_2 = 0$ V, when a single-event strikes the circuit causing current I_n, transistors M_1 and M_4 are on in linear mode and M_2 and M_3 are off. Until V_2 rises to change the state of the feedback inverter, node voltage V_1 is essentially unaffected by the SE induced change at V_2. Once V_2 reaches the threshold voltage of M_1, the SRAM enters strong feedback mode where both node voltages are changing as a result of the single-event strike. In strong feedback mode, both NMOS transistors are on in saturation mode and both PMOS transistors are off.

The point of upset is defined as $V_1 = V_2$ and used as the final condition for strong feedback mode. With the initial and final conditions defined for the each mode, sets of differential equations can be solved to determine the critical charge (Q_{crit}) needed to upset the cell. This framework first proposed in [9] and followed by [54] for a single-event double exponential current source is the foundation of the developed analytical model in this work.

Analytical Model Development

An analytical model has been derived by the method of Garg et al. to calculate the single-event current waveform needed to upset an SRAM for advanced technologies [54]. This section describes the analytical model and includes key equations. Full derivations for equations in this section can be found in Appendix B.
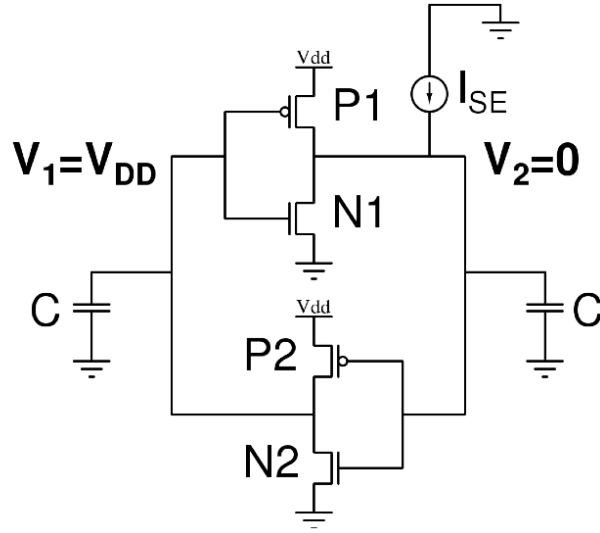
Figure 13: Schematic of the SRAM used in the proposed analytical model of this work.

Fig. 13 shows the schematic of the symmetric SRAM used to develop the analytical model. The SRAM is chosen because it is a common implementation of a memory element. However, the theory of the developed model can be applied for any bistable feedback circuit. Dynamic equations based on the charging and discharging of the capacitors in Fig. 13 describe the system behavior of the SRAM, which is nonlinear in nature due to the nonlinear currents which are a function of the inverter input and output voltages. As in the nonlinear system theory developed in [54], the inverter currents in Fig. 13 are approximated using the linear gate model of (5) in order to analytically solve the SRAM state space equations. The capacitance C in the analytical model includes the nodal capacitance due to any capacitive

28

load as well as the gate capacitance of the PMOS and NMOS in the connecting inverter.

While previously a double exponential current source has been used to characterize a single-event, recent works have shown that an error function current source more accurately captures the fast rise time and tail of the single-event waveform [10, 23]. Therefore, the single-event current used in this work is a modified version of the error function current presented in [10], simplified to reduce the complexity of the equations in order to gain an analytical solution.

$$I_{SE} = \frac{Q}{t_D + 0.5(\tau_F - \tau_R)}[erf\sqrt{(t/\tau_R)} - erf\sqrt{(t/\tau_F)}] \tag{6}$$

The simplification excludes the current at time t<t_D where t_D is the delay time between the start of the SE current to the peak. Utilizing this portion of the error function adds complexity to the solution and does not significantly affect the model results because the delay time is very small compared to the total response time of the SRAM. Including the time before t_D in the single-event current waveform was found to improve the model error from less than 10% error to less than 5% error. However, including this portion of the waveform also requires solving a differential equation for every time step which increases the model run time by 10× and requires software capable of solving differential equations. The analytical model is therefore developed in this work excluding the time before t_D in the single-event current waveform.

Fig. 14 shows how the error function (compact model) current and TCAD model current align well for a normal incidence strike to an NMOS in 14/16nm bulk FinFET technology [10]. Note that the falling time constant for the error function current equation varies over the duration of the strike in order to more accurately model the bias dependence of the single-event current. The analytical model of this work does not take into account the changing
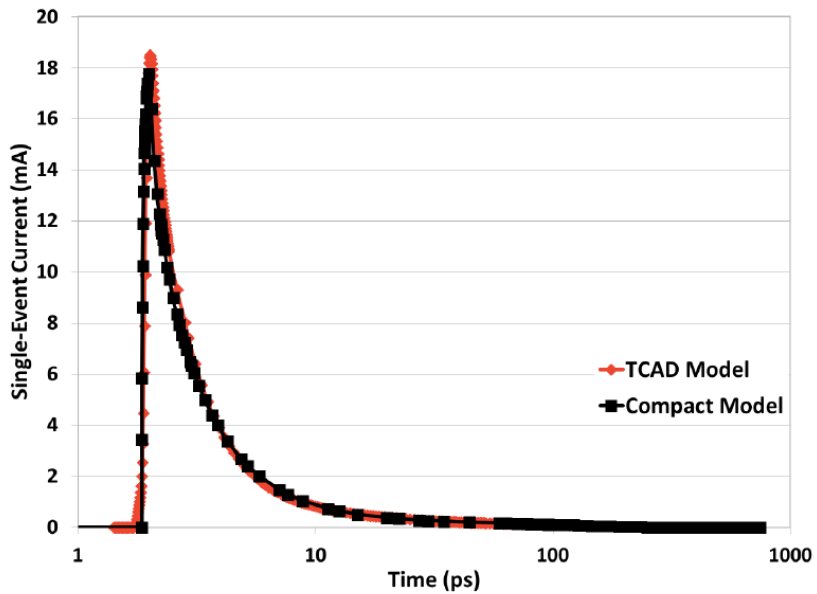
Figure 14: TCAD and SPICE simulated hard-biased NMOS response to a normal incidence single-event strike using TCAD and the bias dependent model. The bias dependent model single-event current source is given by the difference of two error functions, which shows better agreement with experimental data than the traditional double exponential current source in advanced technologies [10].

falling time constant, but rather uses a single time constant calculated from the average of the falling time constant so that the model can be solved analytically without requiring time-stepping as in a simulator.

The SRAM can operate in two modes as the circuit responds to the single-event: weak coupling mode and strong feedback mode. To demonstrate the modes as they relate to a single-event particle strike that causes and upset, nodal voltages V_1 and V_2 in response to a single-event strike to P_1 using the bias dependent error function model of [10] is shown in Fig. 15, where the single-event occurs at time t=0. The figure shows the circuit response to an error function single-event current with the lowest peak current that will cause an upset. When the single-event first strikes P_1, the node voltage V_2 begins to rise. Until V_2 increases to the threshold voltage of N_2 and turns N_2 on, the voltage on V_1 remains at approximately V_{DD}. During this time the SRAM is in weak coupling mode. Once the feedback inverter changes state where P_2 is off and N_2 is saturated, strong feedback mode is established. The SRAM remains in strong feedback mode until the node voltages V_1 and V_2 are equal. At this point, the information stored in the SRAM is lost and according to state space analysis, if the voltages move any further from their original values, the SRAM will change state.

The developed model can be used to find the minimum charge to upset when the single-event current appears in the form of (6). Let us consider the single-event current waveform which results in a total charge of Q_{test} on node V_2. The following method is developed to determine if the SRAM will upset. First, if the single-event current sufficiently alters the state of the transistors in the feedback inverter to affect V_1, then the SRAM will move from weak coupling into strong feedback mode. If the SRAM does enter strong feedback mode, whether or not the single-event current waveform will alter the SRAM voltages to the point of error (V_1=V_2) is evaluated. If the current waveform described by Q_{test} does not cause an
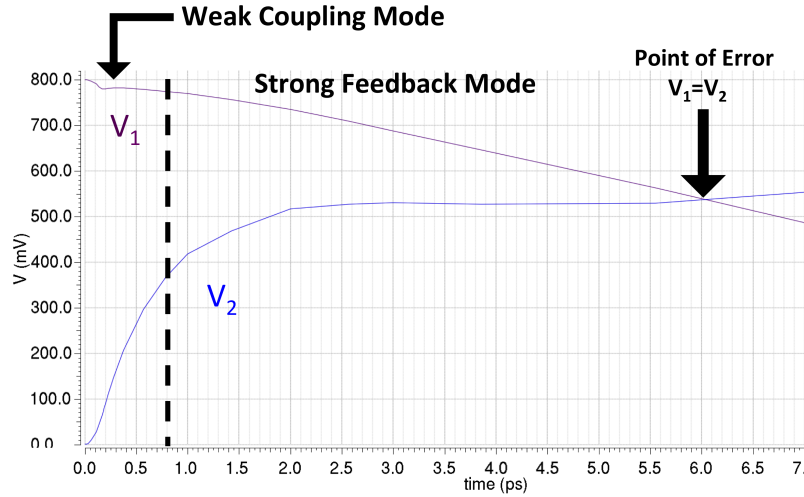
Figure 15: SPICE generated plot of the SRAM node voltages changing over time after a single-event strike to P_1 at time t=0 in Fig. 13. The weak coupling and strong feedback modes are annotated as well as the point of error when the node voltages V_1 and V_2 cross.

upset, another value for charge may be tested until a value for Q (and corresponding current waveform) is found that will upset the SRAM. The next two subsections explain the method and equations used to develop the analytical model for weak coupling and strong feedback mode.

Weak Coupling Mode

For the initial weak coupling response, only the struck node voltage varies significantly from its original value. When a single-event strikes the circuit causing current I_{SE}, transistors N_1 and P_2 are on in linear mode and P_1 and N_2 are off. Until V_2 rises to the threshold voltage of N_2, node voltage V_1 remains approximately at V_{DD}. Therefore, node voltage V_1 is considered to be unaffected by the SE induced change at V_2 in this mode.

In order to determine if the single-event current waveform will upset the SRAM, it must

<center>32</center>

first be established whether or not the corresponding charge will change the transistors in the feedback inverter to the opposite states- P_2 off and N_2 on in saturation. If these conditions are met, the SRAM moves into strong feedback mode and the cell may change state. Otherwise, a change in state will certainly not occur. The following equations describe the SRAM state in weak coupling mode:

$$V_1 = V_{DD}$$

$$\frac{dV_2}{dt} = -\frac{V_2(t)}{R_nC} + \frac{I_{SE}}{C}$$

(7)

The equation that describes V_2 uses Kirchoff's current law (KCL). The boundary condition between weak coupling mode and strong feedback mode is defined as $V_2 = V_{thn}$, the threshold voltage of N_2. In order to determine if this condition is met, the maximum value of V_2 in weak coupling mode is found from (7). If V_{2max} is less than V_{thn}, the analysis is complete. The single-event will not cause the SRAM to enter strong feedback mode and therefore cannot cause an upset. To determine V_{2max}, first the differential equation in (7) for V_2 is solved using the initial conditions t=0 and $V_2(0)=0$. To simplify the expression, consider the rise time τ_b approaching zero in the single-event current equation (6). This simplification does not substantially affect the analysis as the rise time is significantly smaller than the fall time. Therefore, the majority of the single-event current is defined by the fall time.

$$V_2 = [\frac{Q}{t_D + 0.5(\tau_a - \tau_b)}]R_n[1 - e^{-t/R_nC} - erf(\sqrt{\frac{t}{\tau_a}}) + \frac{Y}{X}e^{-t/R_nC}erf(\frac{X}{Y}\sqrt{t/\tau_a})]$$

$$where X = \sqrt{CR_n - \tau_a}, \ Y = \sqrt{C}\sqrt{R_n}$$

(8)

Next the maximum value of V_2 is found by first determining the time at which V_2 reaches its maximum point. Recall that the maximum value of a function can be found by setting the derivative of the function equal to zero. Therefore, (8) is differentiated and set this equation equal to zero to solve for t_{v2m}, the time V_2 reaches its maximum value.

Now, returning to (8) and substituting $t=t_{v2m}$ and $V_2=V_{thn}$, Q_{wc} can be solved for as the single-event charge that will cause the SRAM to move from weak coupling to strong feedback mode. If the charge Q_{test} describing the single-event current exceeds Q_{wc}, strong feedback mode is entered and analysis can continue with strong feedback mode in the next section.

Besides the knowledge that the single-event will enter strong feedback mode, the time at which the SRAM entered strong feedback mode must be known to use as an initial condition for strong feedback mode analysis. This time is not equivalent to t_{v2m} because the maximum value of V_2 in weak coupling mode may exceed V_{thn}, the condition that defines the boundary between the two modes.

For this portion of the model, return to the equation governing V_2 in weak coupling mode in (7). Now V_2 is solved for by differentiation given the same initial boundary conditions of $t=0$ and $V_2(0)=0$, which results in:

$$V_2 = [\frac{Q}{t_D + 0.5(\tau_a - \tau_b)}]R_n[W + \frac{Y}{X}e^{-t/R_nC}erf(\frac{X}{Y}\sqrt{\frac{t}{\tau_a}}) - \frac{Y}{Z}e^{-t/R_nC}erf(\frac{Z}{Y}\sqrt{\frac{t}{\tau_b}})]$$
$$where Z = \sqrt{CR_n - \tau_b}, \ W = erf(\sqrt{\frac{t}{\tau_b}}) - erf(\sqrt{\frac{t}{\tau_a}})$$

(9)

The time at which the SRAM enters strong feedback mode cannot be solved for analytically in (9) because time appears inside error functions. Therefore, the time of the transition between the modes will be found using a linear expansion around an approximation. The approximation used in [54] and in this work is from the first dynamic state space model paper by Zhang et al.[9]. In the paper, a square pulse was used as the transient input noise. Utilizing the method of Zhang et al., the boundary time between weak

coupling and strong feedback is found to be:

$$T_{wc}^{ini} = -R_n C ln(1 - \frac{V_{th}}{I_{max}R_n}) \tag{10}$$

This approximation is used as the starting point for linear expansion of (9) in time. The solution for the linear expansion in time of around T_{wc}^{ini} is then solved for T_{wc} with the final boundary conditions of $V_2 = V_{thn}$ and $t = T_{wc}$. T_{wc} is the time that the SRAM enters strong feedback mode.

Strong Feedback Mode

Once V_2 reaches the threshold voltage of N_2, the SRAM enters strong feedback mode, where both node voltages are changing as a result of the single-event strike. Using the linear gate model for strong feedback mode both NMOS transistors are considered to be on in saturation mode and both PMOS transistors to be off. When N_2 turns on, V_1 begins to drop significantly from V_{DD}. In strong feedback mode, both V_1 and V_2 are changing simultaneously based on the opposite voltage. Writing the KCL equations for strong feedback mode, this mode of operation creates a set of cross-coupled equations:

$$\frac{dV_1}{dt} = -\frac{g_{mn}V_2(t)}{C} + \frac{g_m V_{thn}}{C} \tag{11}$$

$$\frac{dV_2}{dt} = -\frac{g_{mn}V_1(t)}{C} + \frac{g_m V_{thn}}{C} + \frac{Q}{C(\tau_a - \tau_b)}(e^{-t/\tau_a} - e^{-t/\tau_b})) \tag{12}$$

Recall that an upset is defined by the point of error when nodes V_1 and V_2 are equivalent. To solve for this condition, a transformation is implemented to combine equations (11) and (12)

$$\frac{du}{dt} = -\frac{g_{mn}u(t)}{C} - \frac{Q}{C(\tau_a - \tau_b)}(e^{-t/\tau_a} - e^{-t/\tau_b})) \tag{13}$$

where $u(t)=V_1(t)-V_2(t)$. Next, (13) is integrated from $t=T_{wc}$ to $t=$infinity by applying the initial conditions of $t=T_{wc}$ and $u(T_{wc})=V_{DD}-V_{thn}$. Setting $u(t)$ equal to zero, and solving for Q, the amount of charge necessary for the SRAM to upset (Q_{upset}) is determined. Solving the equation in this manner implies that the voltages V_1 and V_2 become equal at time equals infinity. The charge Q_{upset} can now be compared with the charge Q_{test} which describes the single-event. If Q_{test} is greater than or equal to Q_{upset}, the SRAM will upset given the single-event current waveform. If Q_{test} is less than Q_{upset}, Q_{test} can be increased and the equations solved again until Q_{test} results in an upset.

The model described here can also be used like a simulator where the equations are solved iteratively in time and exact values describing how the voltages change in time are found. While using the model in this fashion is time consuming, it may be useful to visualize how the SRAM node voltages change with a given single-event input current. The iterative version of the model can be found in Appendix C.

Model Validation, Application, and Impact

The analytical model developed in this work has been applied for a 14/16nm bulk FinFET technology. Using the 14/16nm process design kit (PDK), NMOS on resistance (R_n), transconductance (g_{mn}), and threshold voltage (V_{thn}) were found for four different bias conditions ($V_{DD}=$ 0.8 V, 0.7 V, 0.6 V, and 0.5 V). The NMOS on resistance is found using the average current through the transistor in linear mode when the gate input is equal to V_{DD}. The inverter gate capacitance was found using the following equation:

$$C_{gate} = C_{ox} \times W \times L \tag{14}$$

where C_{ox} is the oxide capacitance, W is the transistor width and L is the transistor length. For the FinFET technology, the transistor width is calculated as the sum of the three side widths that wrap around the gate. Rising and falling time constants of 55 fs and 5 ps respectively were used to define the single-event current pulse. The single-event and technology parameters used in the analytical model are given in Table 1. The ranges given for the NMOS on resistance and transconductance are based on the variation in those parameters with supply voltage with the first number corresponding to 0.8 V supply voltage and the second to 0.5 V supply voltage.

Table 1: Single-Event and Technology Parameters used in the 14/16nm Analytical Model

Single-Event Parameters		Technology Parameters	
Rise Time (τ_b)	55 fs	Inverter gate capacitance (C)	0.2 fF
Fall Time (τ_a)	5 ps	Supply voltage (V_{DD})	0.8-0.5 V
Delay time (τ_D)	165 fs	NMOS on resistance (R_n)	16-67 kΩ
Q_{test}	Start with 0.01 fC and increment by 0.01 fC	NMOS threshold voltage (V_{thn})	0.384 V
		NMOS transconducance (g_{mn})	186-374 µS

Simulations using the bias dependent error function model were performed to find the critical charge by increasing the total charge gradually until an upset was observed [26, 10]. Similarly, the charge to upset for the analytical model was found by increasing the total charge (Q_{test}) in 0.01 fC increments until the model resulted in $Q_{test} \geq Q_{upset}$. In this section, the results of the analytical model for 14/16nm bulk FinFET technology are compared with traditional critical charge and double exponential single-event current models. The bias dependent error function model is considered to be most accurate compared with reality because the model has been calibrated to TCAD device simulations and validated by

37

experimental data in the 14/16nm technology for single-event effects [10], [23]. Application of the model over a variety of circuit parameters is shown and portability to other technology nodes is also demonstrated.

Comparison with Traditional Models

Critical charge has long been used to approximate the amount of charge a single-event current pulse must deliver to a memory circuit node in order to cause an upset. The critical charge describes the amount of charge that must be added to or taken from the circuit node to change the node voltage from 0 V to V_{DD} or V_{DD} to 0 V ($Q_{crit}=C \times V_{DD}$). This approximation is static in nature and does not take into account the transistors in the SRAM changing state over time based on the input and output voltages. However, as circuits increase in speed, the charge collection at a node from a single-event strike happens on the order of the circuit switching. Therefore, a memory element struck by a single-event particle will begin changing state before all of the charge from the single-event is deposited. The timing between the single-event strike and the inverter switching speeds, therefore, impact one another and an analysis of the upset in time can provide critical information about the single-event's effect.

The charge to upset a 14/16nm SRAM from the analytical model of this work is shown in Fig. 16 compared with the traditional $Q_{crit}=C \times V_{DD}$ approximation and the bias dependent error function current pulse model [10]. Fig. 16 shows that the static, critical charge approximation under-predicts the charge to upset because the model does not account for the changing inverter states and combined restoring current and single-event current that affect the node voltages. However, the analytical model shows good agreement with the bias dependent model, where less than 10% error is seen in the calculated and simulated charge to upset.
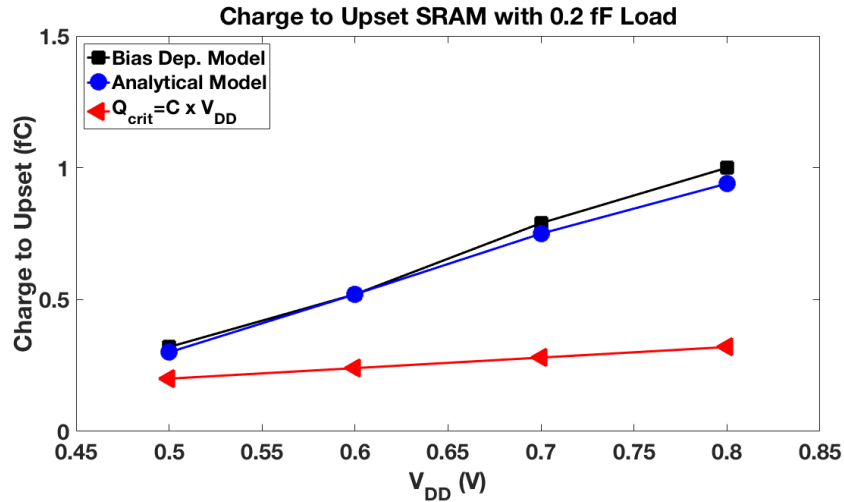
Figure 16: The charge to upset over a range of biases for the data-validated bias dependent model, traditional $Q_{crit}=C\times V_{DD}$ approximation, and analytical model of this work.

The developed model can also be used iteratively to plot the SRAM node voltages over time. Fig. 17 is an example of this model feature. The plot shows the node voltages V_1 and V_2 changing in time in response to an error function single-event current with the lowest charge to upset the SRAM. The equations used to develop Fig. 17 are given in Appendix C.

Traditionally, a double exponential current source has been used to describe single-event current in a circuit and has been used for modeling single-events [58]. Fig. 18 gives a comparison between applying the analytical model using a double exponential current model vs. an error function current model. While the double exponential model is shown to closely follow the bias dependent data-validated simulations for low bias, the approximation deviates from both the simulations and error function model approximation for higher bias values. The inset figure is a comparison of the single-event current waveforms over time. In both the error function and double exponential models, the TCAD generated current profile was used to find the rise and fall times that would match the model current waveform with the TCAD
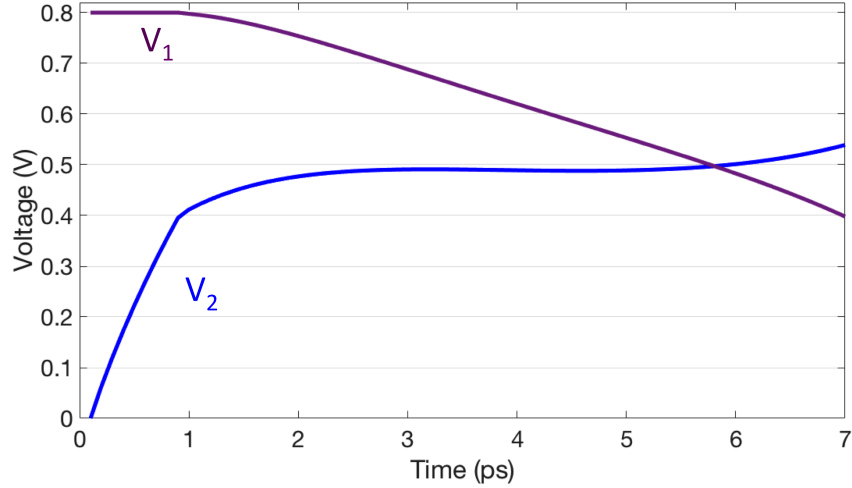
Figure 17: Iterative solution for the analytical model of this work, showing how the SRAM node voltages change in time in response to a single-event current pulse.

waveform most closely. By evaluating the analytical state space model with an error function single-event current model rather than a double exponential single-event current model, the accuracy of the analytical model's critical charge output is significantly improved towards the data-validated simulated results. This is because the FinFET SRAM responds more quickly to the single-event charge than SRAM in previous technologies; therefore, the shape of the charge collection curve has become increasingly important to model with accuracy.

Application over Circuit Parameters

Analytical circuit models are particularly useful for circuit designers because they allow a designer to approximate the impact of circuit design parameters on the single-event response without relying on experimental results or simulations. In this section the analytical model of this work is demonstrated for variation in common designer-chosen circuit parameters: circuit bias, nodal capacitance, and transistor threshold voltage. The analytical model follows bias dependent simulation results with variation in each parameter with less than
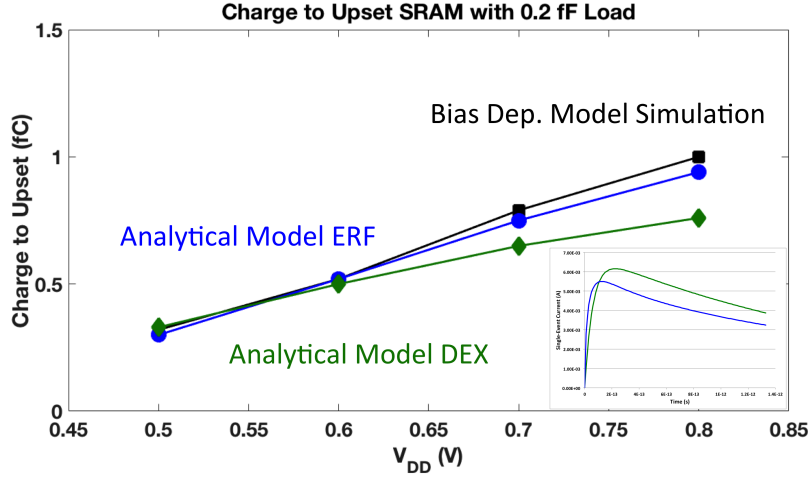
Figure 18: A comparison of the double exponential and error function single-event current models with respect to the data-validated bias dependent simulation.

10% error. Therefore, the model is proven as an additional tool beyond experiments and circuit simulation designers can use to gain understanding about the single-event response of an SRAM for variation in key circuit parameters.

Circuit Supply Voltage

Designing circuits for operation at low circuit supply voltages has become a practical and useful design tool for reducing circuit power consumption. However, the trade-off between decreased power consumption and increased radiation sensitivity must be carefully considered. Fig. 16 shows the calculated charge to upset for an SRAM with output loading equal to the gate capacitance of one inverter using the Q_{crit} model, bias dependent simulation, and analytical model. The results show that the analytical model follows the bias dependent simulation and a significant decrease in charge to upset as supply voltage decreases. This analysis holds true as the output load is increased to 2× the gate capacitance of an inverter

in Fig. 19.
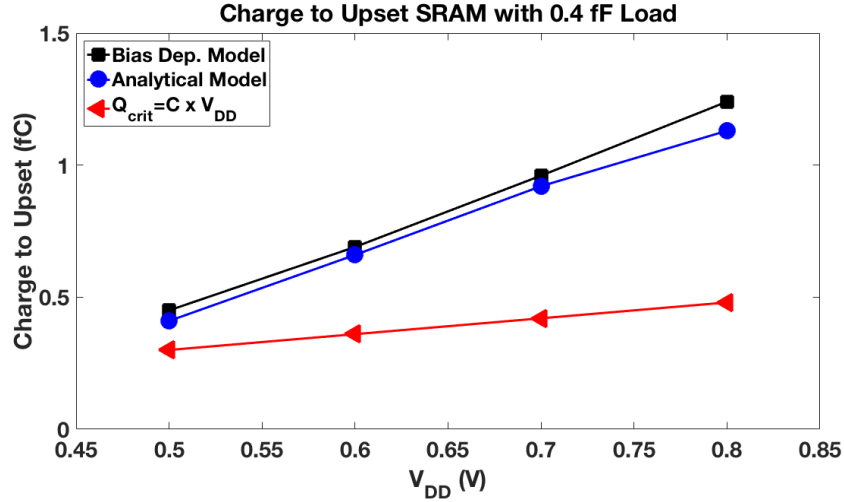
Figure 19: A comparison of the bias dependent simulated, analytical model, and Q_{crit}=C×V_{DD} charge to upset are given over bias for SRAM an SRAM capacitive load of 0.4 fF (the gate capacitance of two inverters).

Nodal Capacitance

Adding nodal capacitance is a straightforward design technique to increase single-event hardness of a circuit node. A higher nodal capacitance will store more charge on a node that must be displaced to upset the SRAM. Figs. 20 and 21 demonstrate the change in the charge to upset the SRAM with variation in nodal capacitance at nominal 0.8 V and low 0.5 V bias. Again, the analytical model tracks closely with the bias dependent simulation over variation in nodal capacitance. As nodal capacitance increases, the analytical model error increases as well. This increase in error is attributed to the changing falling time constant in the simulation that is not included in the analytical model. As nodal capacitance increases, the SRAM speed decreases and the shape of the tail of the single-event current waveform becomes increasingly important. Even so, from this analysis the analytical model provides an estimate to within 10% of the simulated charge to upset for an SRAM with less than 3× the gate capacitance of an inverter as an output load.

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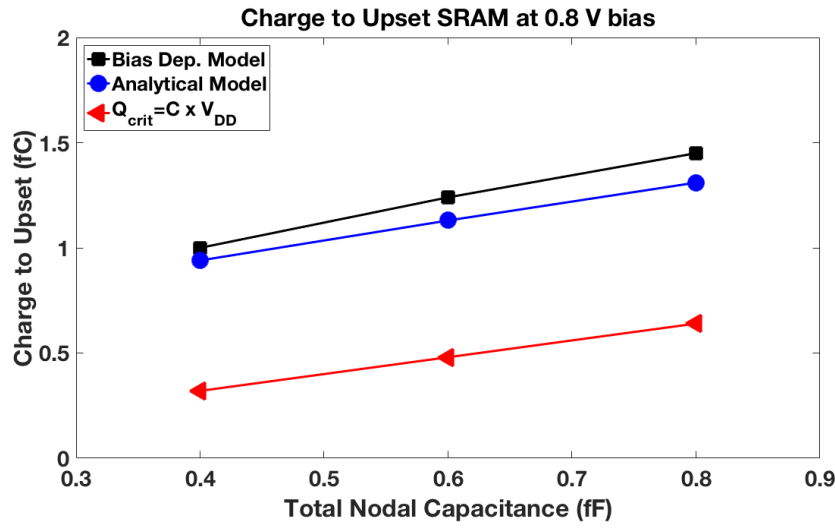
Figure 20: A comparison of the bias dependent simulated, analytical model, and $Q_{crit}=C{\times}V_{DD}$ charge to upset are given for an SRAM operating at nominal 0.8 V bias for total nodal capacitances ranging from 0.4 fF to 0.8 fF (the gate capacitance of two to four inverters).
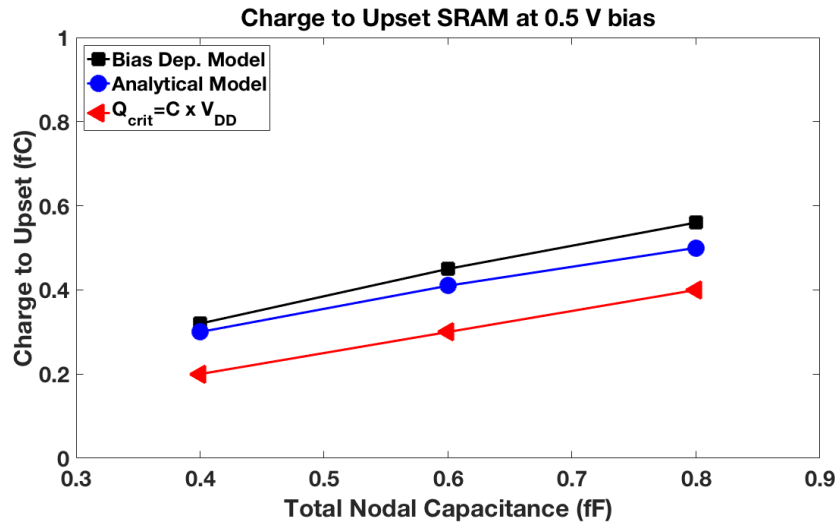
Figure 21: A comparison of the bias dependent simulated, analytical model, and $Q_{crit}=C{\times}V_{DD}$ charge to upset are given for an SRAM operating at reduced 0.5 V bias for total nodal capacitances ranging from 0.4 fF to 0.8 fF (the gate capacitance of two to four inverters).

Transistor Threshold Voltage

A third circuit design parameter that influences single-event response is transistor threshold voltage. Technology process design kits include transistors with threshold voltages that can vary by tens of millivolts. In the analytical model analysis, a change in threshold voltage will alter the boundary condition between weak coupling and strong feedback modes. A comparison for three different transistor threshold voltages is given in Fig. 22. While the traditional critical charge approximation does not account for changes in transistor threshold voltage, the analytical model reveals the upward trend in charge to upset with decreasing threshold voltage.
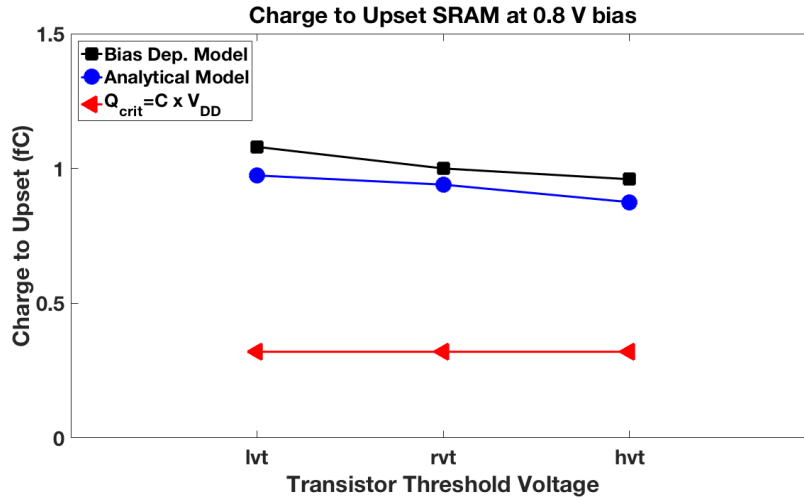
Figure 22: A comparison of the bias dependent simulated, analytical model, and $Q_{crit}=C \times V_{DD}$ charge to upset are given for an SRAM operating at nominal 0.8 V bias for low, regular, and high transistor threshold voltages.

Portability to Other Technology Nodes

The analytical model in this work has also been applied for a 180nm technology SRAM in order to demonstrate its portability to other technology nodes. The 180nm predictive technology models (PTM) [60] were used to compare simulated charge to upset with the

analytical model. A bias dependent double exponential current source is considered to be the standard to which the model is compared [26]. The bias dependent model was calibrated to TCAD simulations of single-event particle strikes to transistors. The bias dependent current source has a rise time of 1.5 ps and a fall time of 70 ps based on this calibration. Recall that the analytical model requires NMOS linear-region on resistance, transconductance, gate capacitance, and transistor threshold voltage, which have been found using the same method as described for the 14/16nm technology. These single-event and technology parameters are given in Table 2.

Table 2: Single-Event and Technology Parameters used in the 180nm Analytical Model

Single-Event Parameters		Technology Parameters	
Rise Time (τ_b)	1.5 ps	Inverter gate capacitance (C)	3 fF
Fall Time (τ_a)	55 ps	Supply voltage (V_{DD})	1.8-1.5 V
Delay time (τ_D)	6 ps	NMOS on resistance (R_n)	20 kΩ
Q_{test}	Start with 0.1 fC and increment by 0.1 fC	NMOS threshold voltage (V_{thn})	0.35 V
		NMOS transconducance (g_{mn})	116 μS

Results of the comparison between the simulated charge to upset given for double exponential single-event current simulation and the analytical model are shown in Fig. 23 over bias. Also plotted in the figure is the static $Q_{crit}=C \times V_{DD}$ approximation for charge to upset. The accuracy of the model in both 180nm bulk planar technology and 14/16nm bulk FinFET technology theoretically validates its application for a wide range of transistor sizes and structures.
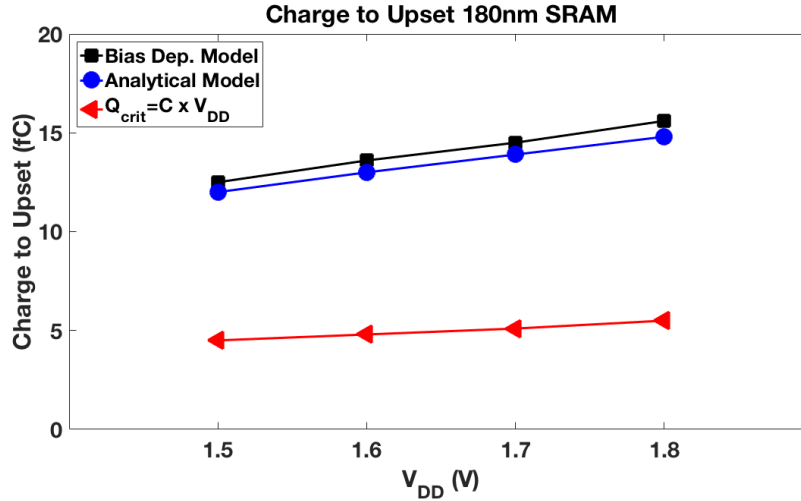
Figure 23: A comparison of the bias dependent simulated, analytical model, and $Q_{crit}=C \times V_{DD}$ charge to upset are given for 180nm technology over circuit bias. Results show the analytical model aligns well with simulated single-event charge to upset based on a double exponential single-event current.

Experimental Logic SEU Cross-Section Estimation

This section is adapted from a paper published in TNS in August, 2017 titled "Estimating Single-Event Logic Cross Sections in Advanced Technologies."

Single-event transients have been shown to decrease in pulse width as technology scales [42, 12, 36, 61, 11]. As circuit clock speeds increase, SE transients and circuit clock periods are reduced to comparable times. The goal of this section is to evaluate existing transient latching probability models for the effect of decreasing SET pulse widths on logic SEU cross section estimation, particularly as circuit speeds increase.

The trend of decreasing SET pulse width is demonstrated in Figs. 24 and 25 by SET data from bulk and SOI technologies respectively. Fig. 24 shows average SET pulse widths decrease with technology scaling for inverter chains in 130 nm, 90 nm, and 65 nm bulk

46

technologies [11]. Fig. 25 presents 45nm and 32nm partially-depleted (PD) SOI SET pulse-width cross sections. The 45nm data shows saturated cumulative SET cross section with decreasing pulse width. However, 32nm data shows a continuing increase in cross section as pulse widths decrease to the minimum measurable pulse width for the utilized on-chip measurement system [12].
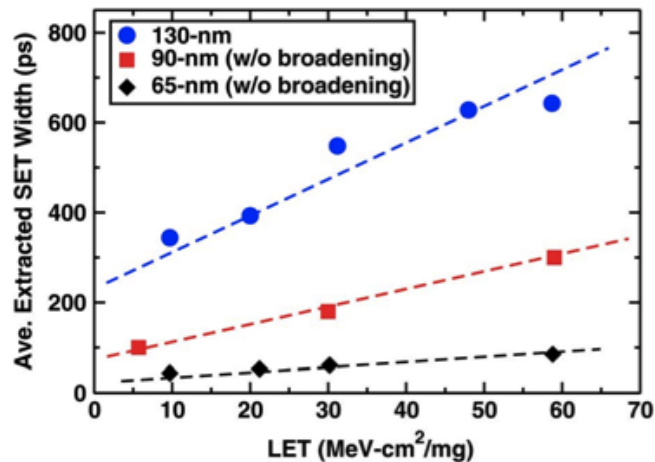
Figure 24: Average extracted inverter SET pulse width vs. LET curves at 3 different bulk technology nodes show decreasing average pulse width with scaling [11].

A probability model for latching single-event transients, which addresses previous assumptions regarding clock frequency, pulse width, and transient/clock-edge coincidence, has been developed [13]. The transient latching probability model and measured SET pulse width distributions are used to demonstrate a method for estimating the single-event upset cross section for combinational logic. Comparing results to previous transient latching probability models reveals the importance of including transients of width less than the setup-and-hold time. Single-event transient and single-event upset data from two different 32nm PDSOI test chips support the presented model.
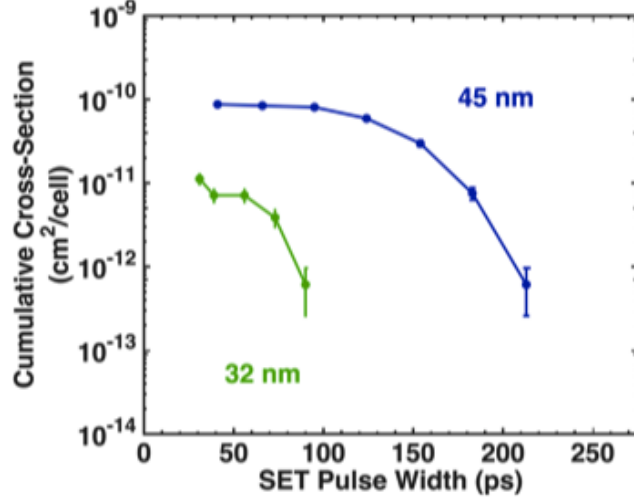
Figure 25: Inverter SET cross section vs. pulse width shows decrease in pulse width as technology scales for SOI [12].

Transient Latching Probability

The SEU cross-section of a logic circuit can be estimated by

$$\sum_{\#\,logic\,gates} Sensitive\ Area \times LM \times EM \times TM \tag{15}$$

where LM, EM, and TM are the logical, electrical, and temporal masking factors, respectively [62]. The sensitive area refers to the area of an individual logic gate that, if hit by a highly energized, ionizing particle, will create a transient voltage pulse. The sensitive area will vary based on the logical inputs and LET of the single event particles interacting with the circuit. Logical masking occurs if a transient does not propagate to the input of a sequential logic element, e.g. a flip-flop, because the circuit topology and input conditions do not provide a valid propagation path. Electrical masking occurs when a transient does not have sufficient amplitude or duration to propagate through a valid path within the combinational logic prior to arriving at the input of a sequential logic element. Temporal masking refers to the window of time in which an SET must occur in order to be latched in a sequential logic element and depends heavily on transient pulse width.

48

Temporal masking is most often discussed in relation to the window of vulnerability. An SET must arrive during the window of vulnerability in order to propagate to the next sequential element for capture. This window has been defined in [63], and is a function of the clock period (T), setup time (t_S), SET propagation time, clock rise and fall times, and clock jitter. The temporal masking factor also depends on a fundamental principle for circuit operation- the adherence to the setup and hold time for the flip-flop. The setup-and-hold time is the time before and after a clock edge that data must be stable to avoid metastability and a potential error in latching the data. A transient pulse that arrives during the setup-and-hold time violates the setup-and-hold time rule of a flip-flop and can cause an error [64, 65]. In this work the temporal masking factor is estimated as the probability of latching a transient (P_{error}) that appears at the input of a flip-flop based on the setup-and-hold time rule.

Several models have been proposed to define the transient latching probability (P_{error}) [43, 44, 66]. These models use different underlying assumptions about transient pulse width as it relates to setup-and-hold time and clock frequency. Holland et al. defined the probability of latching a SET as

$$P_{\text{error}} = \frac{t_{\text{pw}} + t_{\text{SH}}}{T} \tag{16}$$

where t_{pw} is the transient pulse width, t_{SH} is the flip-flop setup-and-hold time, and T is the clock period. This model assumes any perturbation that occurs during the setup-and-hold time causes an error because it creates an indeterminate state in the flip-flop[43]. The model also assumes that the pulse width is much smaller than the period (T). Shivakumar et al.

proposed another model in 2002, which defines the probability of latching a SET as

$$P_{\text{error}} = \begin{cases} 0 & t_{\text{pw}} < t_{\text{SH}} \\[2ex] \frac{t_{\text{pw}} - t_{\text{SH}}}{T} & t_{\text{SH}} \leq t_{\text{pw}} \leq T + t_{\text{SH}} \\[2ex] 1 & t_{\text{pw}} > T + t_{\text{SH}} \end{cases} \tag{17}$$

with the same variable definitions as utilized in (16). This model assumes that only transient pulses that overlap the entire setup-and-hold window cause an error [44].

Based on the key circuit response and performance parameters utilized in (16) and (17), it is important to understand how pulse width relates to setup-and-hold time and clock period as technology scales. Because transient pulse width has been shown to decrease with scaling, SET pulse width distributions now have a significant component that are on the order of setup-and-hold times for RHBD flip-flops [42, 12, 61]. Therefore, the relationship between SET pulse width and setup-and-hold time must be reconsidered as it relates to the transient latching probability. As technology scales, clock frequency also increases (clock period decreases), and transient pulse widths are no longer significantly smaller than the clock period, the assumption utilized in [43].

In this work, the probability of an error occurring due to an SET is defined as the probability that an SET perturbs the input voltage of a sequential logic element during the setup-and-hold time, which is a violation of the setup-and-hold rule. This model does not make the assumption that the SET pulse width is significantly shorter than the clock period. The probability of an error occurring can be expressed mathematically by the probability that a transient pulse of width t_{pw} will intersect the setup-and-hold window (t_{SH}) during a clock period (T) [13]. Fig. 26 shows the two windows intersecting at a single point. A full

mathematical derivation of the probability of the intersection of the SET pulse and setup-and-hold time, the fundamental assumption of this work, is provided in Appendix B. The probability of latching the transient is defined as

$$P_{\text{error}} = \frac{t_{\text{pw}} + t_{\text{SH}}}{T + t_{\text{pw}}} \tag{18}$$

where the variable definitions match those utilized in (16) and (17). This model is very similar to that in [43], assuming any SET can cause an error if it causes a voltage perturbation violating the setup-and-hold time. However, this model also accounts for the possibility that transient pulses are on the order of a clock period, as seen in advanced technologies [12]. Accounting for transients on the order of a clock period will become increasingly important with technology scaling and increasing clock frequency.
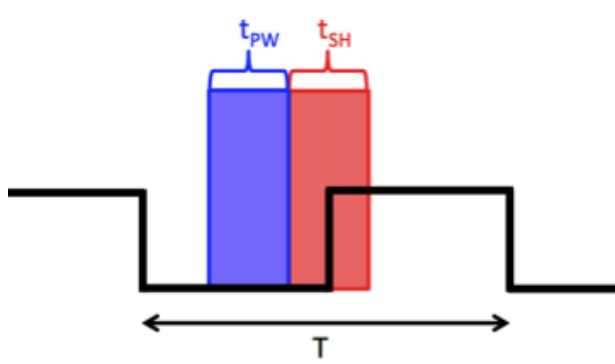
Figure 26: Illustration of an error in this work, which is considered any perturbation in input voltage due to a transient pulse during the setup-and-hold time. See the full derivation of P_{error} as the intersection of t_{pw} and t_{SH} in an Appendix.

Additionally, this work considers the potentially wide distribution of SET pulse widths in the calculation of the transient latching probability. The pulse widths generated in a circuit depend on several factors such as the operating voltage, ion energy, strike location, and temperature [61, 67]. As transient widths vary based on these factors, the transient latching

probability is consequently affected. Therefore, the transient pulse width (t_{pw}) variable in (16) -(18) is considered as a distribution of SET pulse widths. Though not included in this work, the setup-and-hold time (t_{SH}) may also have a distribution of values due to process variation, operating voltage, and temperature, as well as different mean values depending on the design of the sequential logic element. The setup-and-hold time may therefore also be treated as a distribution.

Model Application for 32nm SOI Technology

Single-event transient measurements obtained from heavy-ion irradiation of 32nm PDSOI inverter chains have been utilized to compare the probability models (16)-(18) [59]. Fig. 27 shows single event transient pulse width distributions from irradiation of a standard inverter chain with 10 MeV/amu silicon, copper, and silver at Lawrence Berkeley National Laboratory (LBNL), which have LETs of approximately 6, 21, and 48 MeV-cm^2/mg respectively. The measured SET distributions show that the majority of transients captured in the chain have the smallest measureable pulse width, 23-33 ps. These pulses are on the order of setup-and-hold times for RHBD flip-flops in this technology, approximately 26 ps. Using this approximate value for the setup-and-hold time of an RHBD flip-flop in 32nm PDSOI technology (26 ps) and the average SET pulse width (40 ps) from Cu irradiation of inverters in Fig. 27, P_{error} is plotted for each of the presented models (16)-(18) over frequency, as shown in Fig. 28. The effect of excluding pulse widths shorter than the setup-and-hold time in the Shivakumar model is seen in Fig. 28 where the transient latching probability does not increase with frequency as expected from the increase in logic SEU cross-section seen in previous work [40, 29, 42, 7, 41]. The discrepancy between this probability model and the other two models plotted is the assumption that pulse widths must be longer than the
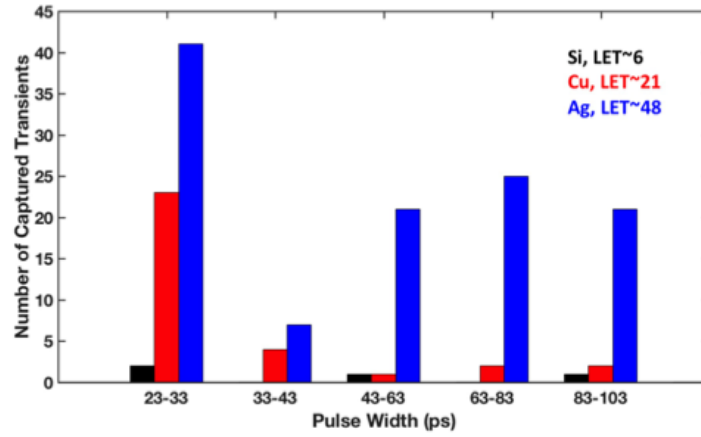
Figure 27: SET pulse width distribution data for a standard inverter chain in 32nm PDSOI technology [12]. Irradiation for a wide range of particle LET (6-48 MeV-cm^2/mg) shows the majority of transients were captured in the lowest measureable pulse width bin (23-33 ps).
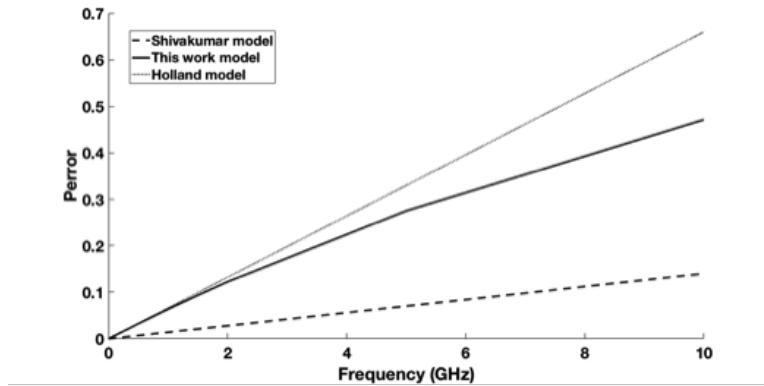
Figure 28: The transient latching probability (P_{error}) is compared for equations (16) -(18) using the average pulse width from Cu irradiation of 32nm PDSOI inverter chains (t_{pw}=40 ps) and the setup-and-hold time of an RHBD flip-flop in the same technology (t_{SH}= 26 ps) [13]

setup-and-hold time in order to cause an error [13]. While the Holland et al. model is similar to the model presented in this work, the difference in these two models can be clearly seen over the wide frequency spectrum of Fig. 28. As the Holland model continues to increase linearly over increasing frequency, the model in this work shows an inflection point in the transient latching probability as the clock period and transient pulse width values converge.

Logic SEU Cross-Section Estimation

A method for predicting logic SEU cross-section using the transient latching probability and SET data has been developed as follows. Recall from (19) the factors in calculating logic SEU cross-section: sensitive area, logical masking, electrical masking, and temporal masking. To predict logic SEU cross-section, these factors are estimated as follows:

1. Sensitive area: Measured SET cross-section from logic gate chains is used to estimate sensitive area for the gates in combinational logic. SET cross-section of a logic gate is calculated as

$$Logic\,gate\,SET = \frac{Total \; \# \; SETs}{Fluence \times \# \; gates\,per\,chain} \tag{19}$$

2. Logical masking: The logical masking factor for combinational logic can be obtained through simulation and will depend on the type of logic gates used in the circuit [66]. This factor as well as the number of gates is dependent on the logic circuit design.

3. Electrical masking: When using the SET cross-section to predict combinational logic SEU cross-section, the electrical masking factor is already accounted for, since transients that would not propagate through combinational logic also do not propagate through the SET measurement circuit.

4. Temporal masking: The temporal masking factor, or transient latching probability (P_{error}) is calculated as presented in (18).

Therefore, given SET data for a specific technology node and LET, the SEU cross-section can be predicted for any combinational logic circuit as

$$\sum_{\#\,logic\,gates} Logic\,gate\,SET\,\sigma \times LM \times P_{\text{error}} \tag{20}$$

where the SET cross-section for logic gates is determined using results from SET measurements on logic gate chains in the technology. Logical masking can be found through simulation of the logic circuit and P_{error} is calculated using the transient pulse width distribution.

The proposed method for predicting logic SEU cross-section has been implemented for an XOR combinational logic circuit fabricated on an SEU test circuit in 32nm PDSOI technology. The 32nm SEU test circuit was fabricated on a different test chip than the SET test circuit presented above. The test circuit included Circuit for Radiation Effects Self-Test (CREST)-style shift registers with chains of combinational logic between SEU hardened flip-flops [68]. More information about the 32nm SOI test chip is included in Appendix A. Fig. 29 illustrates the structure of the combinational logic test chains. The XOR gate combinational logic chain consisted of 14 XOR gates. Radiation-hardened-by-design flip-flops were implemented between the combinational blocks so that upsets could be attributed to the combinational logic. The RHBD flip-flops used on the test chip were LEAP DICE flip-flops, which use redundancy and error aware transistor layout positioning to improve the radiation response [69].

Additionally, CREST style shift registers without combinational logic between the LEAP DICE flip-flops were also tested to determine the contribution of SEUs from the flip-flops over frequency with heavy-ion irradiation. The LEAP DICE flip-flop had no recorded upsets over frequency up to 2.3 GHz with an ion fluence of $1\text{x}10^8$ ions/cm^2 for irradiation with
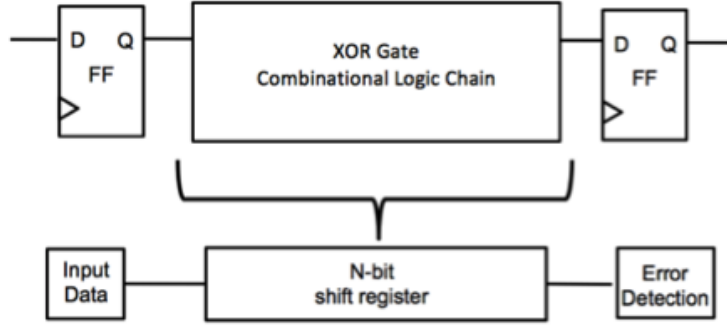
Figure 29: Schematic representation of the XOR combinational logic chain fabricated on a 32nm PDSOI test chip. The flip-flops used were LEAP DICE radiation-hardened-by-design and showed no upsets in a separate structure tested simultaneously.

LET= 39.25 MeV-cm^2/mg.

The assumption that upsets recorded in the combinational logic circuit can be attributed to transients generated in the combinational logic is validated by the fact that no errors were recorded over frequency for the LEAP DICE flip-flop. The logic inputs and outputs between the flip-flops were designed to provide transparent inputs to the flip-flops. A constant input/output pattern is observed unless a bit is changed, where that upset pattern would then propagate through the shift register to the output. For this work, the equation for predicting the XOR combinational logic SEU cross-section (20) has been adapted to fit the available inverter SET data for the 32nm technology. The logic gate SET cross-section is estimated as inverter SET cross-section for inverters of similar drive strength to the XOR combinational logic gate chains. Additionally, because no logical masking occurs for inverters, a logical masking factor of one is used. The prediction for logic SEU cross-section then becomes

$$\sum_{\#\,logic\,gates} Logic\,gate\,SET\,\sigma \times P_{error} \qquad (21)$$

where the SET pulse width distributions from Fig. 27 are used to calculate P_{error} and the inverter SET cross-section using (19). The transient latching probability distribution is

56

calculated using 1000 random pulse-width samples from the SET distributions represented in Fig. 27 and a 26 ps RHBD flip-flop setup-and-hold time. Heavy-ion experiments were performed on the XOR chain test chip at LBNL using the 4.5 and 10 MeV/amu cocktail. An on-chip multi-GHz voltage controlled oscillator (VCO) set the clock frequency to approximately 30 kHz, 1 GHz, 1.5 GHz, and 2.5 GHz. Fig. 30, 31, and 32 show the measured logic SEU cross-section compared to the predicted SEU cross-section using the Shivakumar model and the model presented in this work.
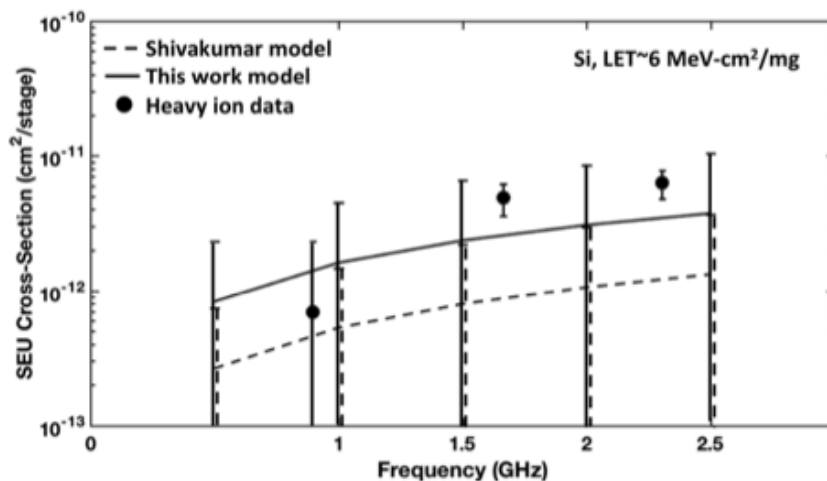
Figure 30: Comparison of measured XOR combinational logic SEU cross-section to SEU cross-section predictions using (21) and the transient latching probability models (17) and (18) for Si (LET=6 MeV-cm^2/mg).

The error bars for the model and measured data in the plots are calculated using the Poisson single-sided upper limit for an 84% confidence level as an upper bound for upset/transient counts of less than 10 [70]. For counts greater than or equal to 10, the Gaussian standard error of measurement converges within 10% for the upper limit and 1% for the lower limit of the Poisson counting statistics 84% confidence level. Therefore, the Gaussian standard error of measurement was used for experimental data with 10 or more
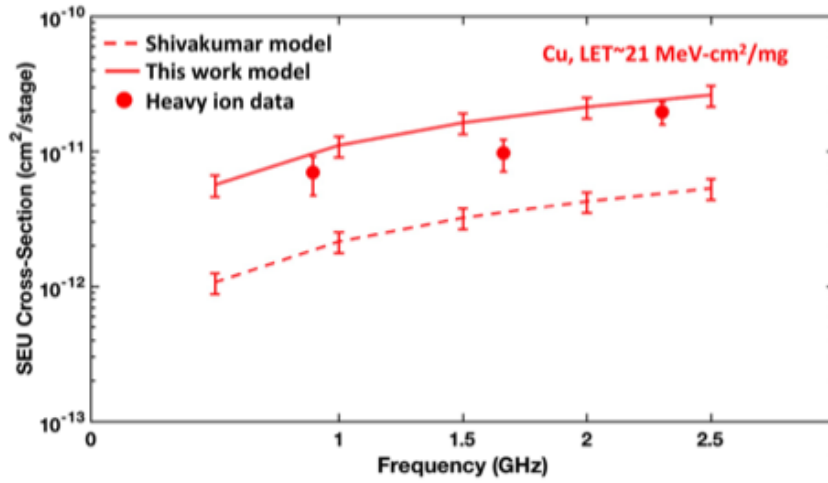
Figure 31: Comparison of measured XOR combinational logic SEU cross-section to SEU cross-section predictions using (21) and the transient latching probability models (17) and (18) for Cu (LET=21 MeV-cm^2/mg).
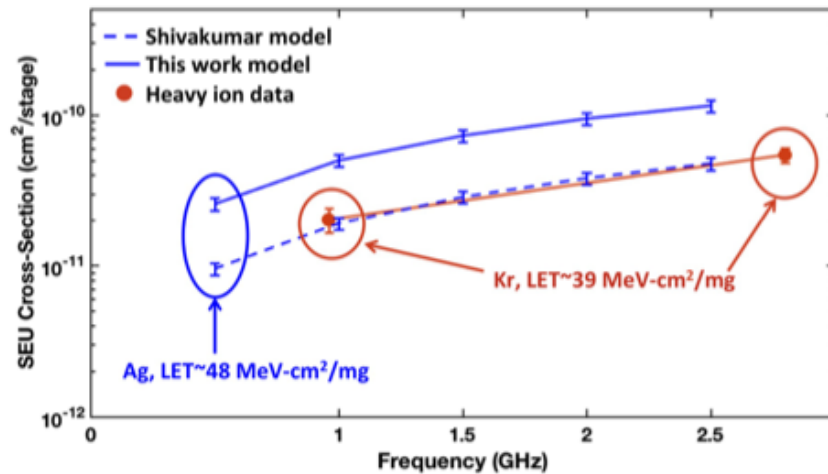
Figure 32: Comparison of measured XOR combinational logic SEU cross-section for Kr (LET=39 MeV-cm^2/mg) to SEU cross-section predictions using (21) and the transient latching probability models (17) and (18) for Ag (LET=48 MeV-cm^2/mg).

counted errors. The Gaussian standard error of measurement is calculated as

$$StdErr = \frac{\sqrt{Total\ \#\ of\ errors}}{Fluence \times \#\ of\ stages\ per\ chain} \tag{22}$$

where errors refers to SETs or SEUs for calculating either the SET or SEU cross-section and stages refers to the circuit being tested (inverters for SET cross-section and flip-flops for SEU cross-section).

Fig. 30 and 31 show the direct comparison of predicted SEU cross-section and measured heavy ion data for Si (LET=6 MeV-cm^2/mg) and Cu (LET=21 MeV-cm^2/mg). Both figures show that the Shivakumar model under predicts the logic SEU cross-section. This is due to the exclusion of transients less than the flip-flop setup-and-hold time in the P$_{error}$ term of (21). By including fast transients in the transient latching probability, the model used in this work accurately predicts the logic SEU cross-section within the error bars for Si and Cu irradiation. Fig. 32 compares the predictive capabilities of the transient latching probability models to experimental data at high LET particle irradiation. Though no data were taken at the same two LET values for the SET and SEU test chips, an understanding of the two models' accuracy can still be determined. The transient distribution used in the two models of Fig. 32 is for Ag (LET=48 MeV-cm^2/mg), while the experimental data shown is for Kr (LET=39 MeV-cm^2/mg). Because the experimental data was taken for a lower LET particle than the simulated SEU cross-section, the simulated SEU cross-section should be higher than the presented experimental SEU cross-section. This is true for the model of this work, while the Shivakumar model overlays the data, suggesting that it will under predict the SEU cross-section for LET values higher than 39 MeV-cm^2/mg. Figs. 30-32 show the importance of including transients on the order of the setup-and-hold time when using transient distributions to predict logic SEU cross-section in advanced technologies.

Empirical SEU Model for Bias Variation

This section is adapted from a paper that was submitted to TNS from RADECS 2018 and is currently under review titled "Empirical Modeling of FinFET SEU Cross-Sections Across Supply Voltage."

Gaining a comprehensive understanding of single-event response of a flip-flop design over supply voltage and the entire LET spectrum requires extensive resources and manpower. Since the modeling of SE response at advanced technologies is difficult due to unavailability of fabrication process parameters, experimental methods are usually employed to measure SE response of storage cells. Designers would like to have such characterizations at all possible supply voltages to estimate overall IC-level SE response. However, the cost of beamtime allows engineers to test for just one or two values of supply voltage. Designers are forced to use time-consuming TCAD simulations to estimate various SE-related parameters at other supply voltages to model SEU cross-sections. These TCAD models are calibrated against PDK and experimental SE results to improve accuracy.

In this section, an empirical model for predicting SEU cross-section as a function of supply voltage is developed and verified through experimental results and TCAD simulations at the 14/16nm FinFET technology generation. Results of this work provide a tool for estimating the expected increase in low- and high-LET SEU cross-section for a storage cell operating at reduced supply voltage without extensive testing and simulation. The expected SEU cross-section increase due to a decrease in supply voltage is based on changes in sensitive area and critical charge. For low-LET particles, decreasing critical charge dominates the increase in SEU cross-section. For high-LET particles, increasing sensitive area, corresponding to a reduced critical charge within the ion region of influence, dominates the increase in SEU

cross-section. The developed empirical model for supply voltage variation gives insight into SEU voltage scaling trends for FinFET devices that provide an understanding of SEU cross-section trade-offs with supply voltage and power reduction across the entire particle LET spectrum.

Proposed Data-Based SEU Model

In order to evaluate a flip-flop's response to radiation across the entire LET spectrum, engineers must account for three variable factors: critical charge, collected charge, and sensitive area of individual transistors. The following model has been used extensively to understand changes in SEU cross-section based on these factors [53]:

$$SEU\ Cross-Section = A \times K \times e^{\frac{-Q_{\text{crit}}}{Q_{\text{coll}}}} \tag{23}$$

where A is the sensitive area, K is a voltage independent constant, Q_{crit} is the critical charge, and Q_{coll} is the collected charge. Evaluation of these factors is required for each technology node where changes in device structure may affect the charge collection process. In particular, FinFET device structure connects the active device to the substrate through a narrow neck region resulting in a charge collection process very different than that of a planar transistor [71, 72]. Likewise variation in circuit operation parameters such as supply voltage influence critical charge, collected charge, and sensitive area impact on SEU cross-section.

While the effect on SEU cross-section of low-LET particle irradiation is well understood for bulk FinFET technology, high-LET particle SE trends lack a similar understanding. With high-LET particle irradiation, in addition to critical charge, the sensitive area of a transistor becomes an important factor determining SE vulnerability. In this work, sensitive area is defined as the area in and around the transistor for which the region of influence is

61

sufficiently large to result in charge collection at the device equal to or exceeding the critical charge. A high-LET particle can strike a cell at some distance away from the drain area with sufficient charge deposition across a broad region, the ion region of influence, to cause an upset. After an ionizing particle strikes, a transistor may collect charge over time. If the collected charge exceeds critical charge within a short time (determined by circuit-level parameters such as feedback loop delay of the storage cell, nodal capacitances, transistor currents, etc.), an upset will occur. The sensitive area of a transistor is therefore related to the amount of collected charge, which will vary based on particle LET, distance of the particle strike from the drain, and supply voltage. However, the supply voltage dependence of this region has not been fully studied for advanced technologies and generally requires 3D TCAD simulations in an effort to achieve insight into these mechanisms.

Equation (23) is used in the proposed model to assess supply voltage variation in both low and high-LET single-event cross-section for flip-flop designs. While limitations do exist for the extent to which (23) can be used for advanced technologies where charge collection and circuit response occur on the time scale, the equation continues to provide a useful general understanding of SEU cross-section factors and is used as the basis of the empirical model developed here. In this section the proposed model is presented and in the following sections experimental results and TCAD simulations are used to validate the model. While the results here are given for the 14/16nm technology node, the proposed model concepts are more broadly applicable. Most particle SEU cross-section measurements are carried out at nominal supply voltage (V_{nom}). However, with technology scaling and increased efforts to decrease power consumption, a storage cell may be required to operate at some reduced supply voltage (V_{op}). Assume that a circuit designer has collected SEU cross-section data for a storage cell at two supply voltages- V_{nom} and V_{op}. A ratio of SEU cross-sections at

62

these two supply voltages using (23) yields:

$$\frac{SEU\ Cross-Section_{\text{op}}}{SEU\ Cross-Section_{\text{nom}}} = \frac{A_{\text{op}}}{A_{\text{nom}}} \times \frac{K_{\text{op}}}{K_{\text{nom}}} \times e^{\frac{Q_{\text{critnom}}-Q_{\text{critop}}}{Q_{\text{coll}}}} \qquad (24)$$

The K constant is independent of supply voltage and therefore equivalent for all supply voltages [53]. Furthermore, the sensitive area is the drain region for low-LET particle strikes regardless of supply voltage because the strike must occur in the drain region in order for enough charge to be collected to cause an upset. Therefore, for low-LET particle irradiation, the ratio of single-event cross-sections can be written as:

$$\frac{SEU\ Cross-Section_{\text{op}}}{SEU\ Cross-Section_{\text{nom}}} = e^{\frac{Q_{\text{critnom}}-Q_{\text{critop}}}{Q_{\text{coll}}}} \qquad (25)$$

where Q_{critnom} is the critical charge at nominal voltage and Q_{critop} is the critical charge at operational (reduced) voltage. Since designers can estimate differences in critical charge for a flip-flop, (25) allows designers to accurately estimate SEU cross-section for any supply voltage based on experimental data from just two supply voltages. For a given LET particle, two data points at nominal and operational supply voltage can be used to solve for the collected charge. Estimations of the SEU cross-section at other reduced supply voltages may be determined using the calculated collected charge value and estimated critical charge values for the reduced supply voltage. The exponential relationship for the cross-section ratio is true for all supply voltage values for low-LET particles. It must be kept in mind that this relationship is valid only when changes in sensitive area are not significant for different supply voltages as in the case of low-LET particles where sensitive area is approximately the drawn drain area. On the other hand, particles with high-LET values can deposit charge outside of the transistor drain area that will reach a sensitive node through the diffusion process and may cause an upset. The sensitive area term in (23) is therefore variable with supply voltage for high-LET particle irradiation. Q_{crit} will also vary with supply voltage for

high-LET particles, though for advanced technologies, the critical charge value has dropped below 1 fC. For such a low value of critical charge, collected charge for a high-LET particle strike is significantly higher than Q_{crit}. Because the collected charge will well exceed the critical charge, and the exponential term in (24) approaches unity. In this case, taking a ratio of SEU cross-section at different supply voltages yields:

$$\frac{SEU\ Cross-Section_{op}}{SEU\ Cross-Section_{nom}} = \frac{A_{op}}{A_{nom}} \tag{26}$$

where A_{op} and A_{nom} designate sensitive areas at the respective supply voltages. For a given supply voltage, as particle LET increases, the amount of deposited charge, and subsequently collected charge, increases (while the critical charge remains constant). According to this model, the SEU cross-section will increase linearly with sensitive area. The empirical model of this work is particularly useful for circuit designers who may know a circuit's SEU cross-section at any two supply voltages and desire to know how the cross-section will change with decreasing supply voltage for power-saving purposes. Because collected charge and sensitive area are highly technology dependent factors, the empirical model can be used as an estimation tool for supply voltage variations in SEU cross-section for any flip-flop design. Determination of critical charge as a function of supply voltage is a simple process, usually carried out using circuit-level simulations. While critical charge arguments related to supply voltage scaling have been well established for FinFET technology [8], sensitive area analysis requires the use of modeling tools such as TCAD, which are not readily available to designers and involve long run times. The analysis in this work focuses on the supply voltage dependent change in sensitive area for heavy-ion irradiations by utilizing experimental results and TCAD simulations for a 14/16nm FinFET technology node to validate the empirical model presented.

Model Application for Predicting SEU Cross-Section

The model described above has been applied using single-event upset data from a 14/16nm bulk FinFET D flip-flop. The test chip and experimental conditions are described in detail in Appendix A. Fig. 33 shows the DFF SEU cross-section across particle LET as a function of supply voltage for the 14/16nm bulk FinFET node. The results are similar to previous bulk planar behavior for heavy-ion irradiations over decreasing supply voltage [8, 73]. The SEU cross-section, representative of the sum of all sensitive areas within a DFF, shows an increasing trend with decreasing supply voltage and a stronger SEU cross-section supply voltage dependence for low-LET ions than high-LET ions.
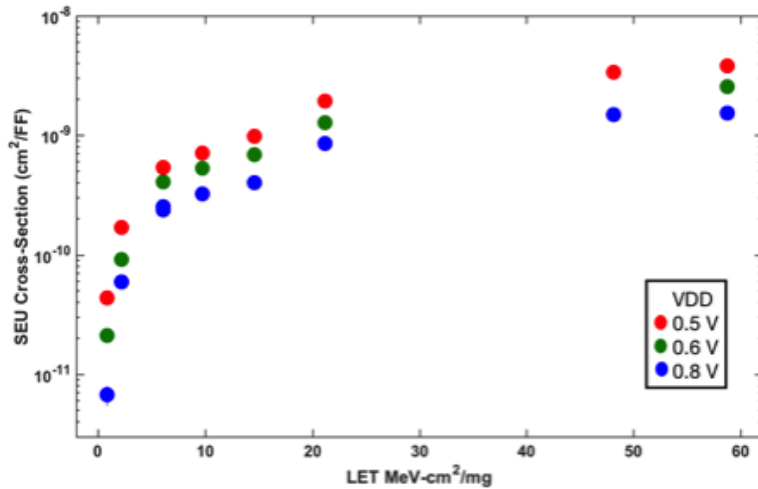
Figure 33: Experimental heavy ion SEU cross-section data in this work for a D flip-flop over LET at three different supply voltages.

In order to gain a clear understanding of the change in SEU cross-section over supply voltage, the 14/16nm FinFET irradiation data is also plotted in Fig. 34 as the SEU cross-section ratio with respect to nominal voltage for each of the voltages tested. Fig. 34 shows an increase in DFF cross-section from nominal voltage (0.8 V) to 0.5 V of 12× and 4× for Boron
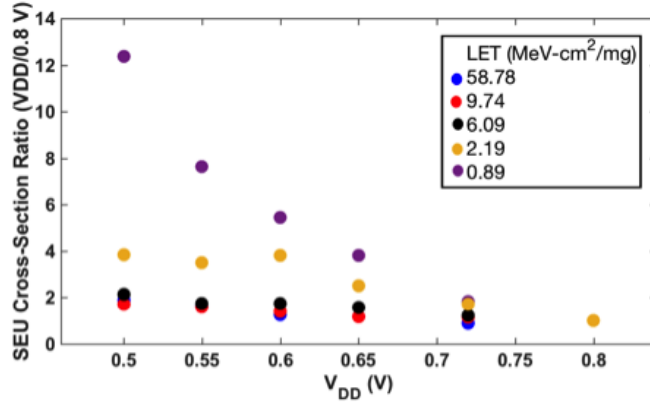
Figure 34: Heavy-ion SEU cross-section data for 14/16nm bulk FinFET DFF plotted as the cross-section ratio at a given supply voltage (0.5 V -0.8 V) compared to nominal voltage (0.8 V). Results show a large increase in SEU cross-section with decreasing supply voltage for low-LET particle irradiation and a constant increase in SEU cross-section for high-LET particle irradiation.

(LET = 0.9 MeV-cm^2/mg) and Oxygen (LET = 2.2 MeV-cm^2/mg) irradiation respectively. This result is expected for low-LET particle irradiation where the collected charge is on the order of the critical charge of the cell and critical charge is a strong function of supply voltage. Above the knee of the SEU cross-section curve, Fig. 34 shows a constant increase in cross-section at each supply voltages compared to nominal supply voltage for all high-LET particle irradiations. As the collected charge in these cases is much higher than the critical charge, the exponential term in (23) shows a weak relationship with SEU cross-section. High-LET irradiation data confirms that the increase in sensitive area with decreasing supply voltage is constant irrespective of particle LET value. The constant increase in SEU cross-section for any supply voltage over the high LET spectrum is attributed to the increase in sensitive area as seen in the proposed model. To further elucidate the effects of changing critical charge, collected charge, and sensitive area in FinFET devices, extensive TCAD analysis was performed for variations in supply voltage, particle LET, and hit location.

TCAD Analysis and Model Support

In order to investigate how changes in supply voltage affect sensitive area for FinFET devices, mixed-mode 3D-TCAD simulations were performed using a latch of minimum sized inverters. The TCAD devices were electrically calibrated to DC and AC I-V data from the 14/16nm PDK and have been previously discussed in [22]. Simulations were carried out with an ion strike at the edge of an OFF NMOS drain and for 25 nm increments beyond the drain edge as shown in Fig. 35 (each intermediate location in Fig. 35 was also simulated). It should be noted that in the figure 0 nm corresponds to the center of the OFF transistor. Simulations were run at 0.8 V, 0.6 V, and 0.5 V in order to determine the maximum distance from the OFF transistor a particle strike could occur and still cause an upset in the latch.
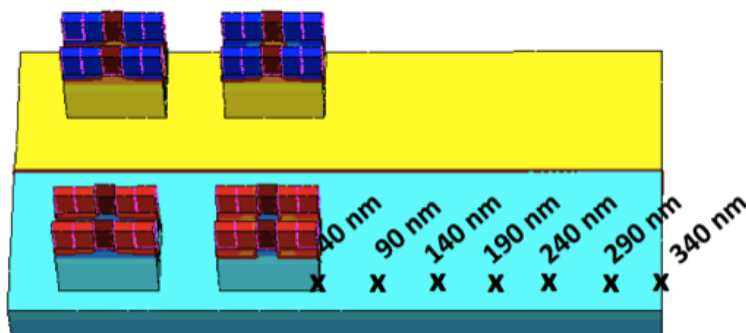
Figure 35: Single event upset simulations were performed on the shown 14/16nm FinFET latch in TCAD. Strikes of differing particle LET and strike location were simulated for three different supply voltage conditions (0.8 V, 0.6 V, and 0.5 V). Strikes at each location shown and every intermediate location were taken for each supply voltage and LET.

Table 3 summarizes the results for each simulated particle LET. For each supply voltage and LET value, the maximum distance from the center of the NMOS transistor (termed as d_{max} in Table 3), which still causes an upset in the latch, is given. For example, a 20 MeV-cm^2/mg ion strike up to 190 nm from the center of the transistor will cause an upset

67

if the circuit is operating at nominal 0.8 V supply voltage. The same LET particle strike can occur up to a distance of 290 nm and cause an upset when the latch is operating at a 0.5 V supply voltage. For simplicity of comparison, it is assumed that the sensitive area for a transistor is a circle (π x d_{max}^2) around the center of the device with radius equal to d_{max}. Based on this assumption, a hit in any direction up to d_{max} distance away from the center of the drain will cause an upset. The ratio of the squared distances for 0.5 V and 0.8 V supply voltage yields the increase in simulated sensitive area for each ion LET value. The TCAD results summarized in Table 3 show the simulated sensitive area is an average 2.28× larger at 0.5 V than at nominal supply voltage for high-LET particle irradiations. The empirical model developed in this work correlates this increase in sensitive area with a comparable increase in SEU cross-section. Table 4 gives the comparison of average increase in SEU cross-section of the experimental data points for several LET values at 0.5 V and 0.6 V supply voltages. Note that data was not taken for irradiation with particle LET 48 MeV-cm^2/mg and 0.6 V supply voltage. The average experimental cross-section ratio for 0.5 V supply voltage is 2.09× compared to the 2.28× ratio found in TCAD simulations for sensitive area. The same analysis was applied to find the simulated sensitive area ratio from 0.6 V to 0.8 V supply voltage. The results yield an average simulated sensitive area 1.48× larger at 0.6 V than at nominal supply voltage, compared to 1.53× average increase in high-LET particle experimental SEU cross-section. The TCAD simulations, which align well with experimental data, provide confirmation that the empirical model presented accurately describes the changes in critical charge, collected charge, and sensitive area that all influence SEU cross-section variation with reduced supply voltage.

For low-LET particle irradiations, the SEU cross-section ratio for variations in supply voltage is dominated by the difference in critical charge. The sensitive area ratio from 0.5 V

68

Table 3: TCAD simulated heavy ion strikes to an OFF NMOS in a 14/16nm latch show the maximum distance from the drain edge to induce an upset for ions of a given LET and supply voltage. The table also shows the ratio between the sensitive area for variation in bias when approximated as a circle around the transistor.

Simulated LET (MeV-cm^2/mg)	Maximum distance (d_{max}) from center of OFF NMOS to cause an upset (nm) V_{DD}			Simulated Sensitive Area Ratio d_{max}^2(0.5 V)/ d_{max}^2(0.8 V)	Simulated Sensitive Area Ratio d_{max}^2(0.6 V)/ d_{max}^2(0.8 V)
	0.8 V	0.6 V	0.5 V		
1	40	40	40	1	1
10	140	165	215	2.4	1.4
20	190	240	290	2.3	1.6
35	265	315	415	2.5	1.4
60	340	415	465	1.9	1.5

Table 4: Experimental SEU Cross-Section Ratios for 0.5 V and 0.6 V Supply Voltages for High LET Irradiation.

Experimental LET (MeV-cm^2/mg)	Experimental SEU Cross-Section Ratio (0.5 V)/(0.8 V)	Experimental SEU Cross-Section Ratio (0.6 V)/(0.8 V)
10	1.91	1.48
15	2.16	1.60
21	2.14	1.45
48	2.28	-
60	1.94	1.59

to 0.8 V from (24) is equal to unity because for low-LET particle irradiation the particle must strike an OFF transistor drain region in order to deposit enough charge to cause an upset. This is consistent with the TCAD simulation results for the sensitive area ratio in Table 3 as well. With the sensitive area and K constant ratios in (24) equal to unity, the change in critical charge due to variation in supply voltage will dominate the low-LET particle SEU cross-section. This conclusion results in a strong exponential increase in SEU cross-section with decreasing supply voltage, as seen in previous works and in Fig. 34. For high-LET particles, experimental results as well as TCAD simulations support the linear relationship of SEU cross-section and supply voltage. The SEU cross-section ratio is dominated by the sensitive area ratio for high-LET particle irradiations as determined in (26). This concept has been illustrated by the TCAD simulation and experimental results in Tables 3 and 4, which show that for high-LET ion irradiation, the SEU cross-section ratio is approximately equal to the sensitive area ratio. The experimental sensitive area ratio has been calculated from nominal voltage to each of the supply voltage values tested. The average SEU cross-section ratio for high-LET particle irradiation is shown in Table 5 for each of the supply voltage values tested with respect to the nominal 0.8 V supply voltage. High-LET particles are defined as those with LET above the knee of the cross-section curve.

Table 5: Average Experimental SEU Cross-Section Ratios for High LET Heavy-ion Irradiation in 14/16nm Bulk FinFET Technology.

Supply Voltage (V)	Average Experimental SEU Cross-Section Ratio (Supply Voltage)/(0.8 V)
0.72	1.20
0.65	1.31
0.6	1.53
0.55	1.83
0.5	2.09

To further illustrate the effect of changing sensitive area with supply voltage variation, TCAD simulations were also performed for two adjacent latches. Different LET particle strikes were simulated between the two latches, equidistant from both with varying node spacing. The SEU LET threshold for an upset was found for different node spacing and supply voltage. The results are shown in Fig. 36 as SEU LET threshold vs. node spacing for three different supply voltages. The data points on the figure correspond to the minimum LET particle strike that will cause an upset. Therefore, each supply voltage curve separates the figure into two sides- one where an upset will occur in both latches and another where no upset will occur in either latch. At nominal 0.8 V supply voltage, Fig. 36 shows that the further apart the latches are placed, the higher LET a particle strike must have in order to upset the latches. Furthermore, with decreasing supply voltage, the SEU LET threshold also decreases due to the decrease in critical charge. For example, latches placed 450 nm apart require a particle strike of LET= 60 MeV-cm^2/mg to upset at nominal voltage and only LET= 20 MeV-cm^2/mg to upset at 0.4 V supply voltage. These results are consistent with the TCAD analysis performed on a single latch and the empirical model developed. Fig. 36 can also be used in developing radiation-hardening techniques that rely on nodal spacing and charge sharing for single-event upset mitigation.

Summary

An analytical model has been developed for an estimation of the charge to upset memory circuits in advanced technologies with fast-switching circuits. The results from the model for an SRAM in 14/16nm bulk FinFET technology are compared with the static Q_{crit}=C×V_{DD} approximation as well as a bias dependent model that has been calibrated to 14/16nm bulk
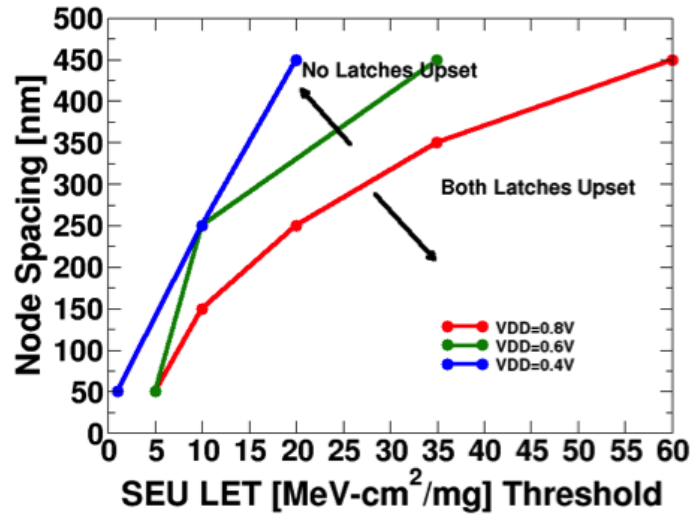
Figure 36: TCAD simulation results of the SEU LET threshold for two adjacent latches spaced at various distances apart over supply voltage. The arrows separating the two sides of the curve where no latches upset or both latches upset is shown for the 0.8 V supply voltage case.

FinFET data. Using the critical charge approximation under predicted the charge necessary to upset a cell while the analytical model followed closely with the data-validated model. Furthermore, using a single-event current pulse expressed by an error function rather than a double exponential function results in more accurate charge estimations when compared to bias dependent model simulations. The developed analytical model has been used to compare the minimum charge to upset an SRAM with variation in circuit bias, nodal capacitance, and transistor threshold voltage. The model consistently provides less than 10% error in charge to upset when compared with the bias dependent model. Furthermore, the model has been applied to a 180nm SRAM and shows good agreement with a TCAD calibrated bias dependent model as well.

An experimental model for predicting logic SEU cross section using SET data is also presented. The model for transient latching probability has readdressed the assumptions made in previous work as a result of factors driven by technology scaling, which are the

72

decrease in SET pulse width and increased operational clock frequency. Previous transient latching probability models have assumed that transients shorter than the setup and hold time do not cause an error and/or that transients are much shorter than the clock period. This model is distinct from previous models in that it accounts for the probability that fast transients can cause upsets by interrupting the setup-and-hold time of a flip-flop. Furthermore, as clock frequency increases, this model responds to decreasing clock period on the order of transient pulse widths. Heavy-ion single-event transient and single-event upset data from circuits fabricated in a commercially available 32nm PDSOI technology have been used to support the transient latching probability and logic SEU cross section prediction model developed. Predictions from the model agree well with experimental data. The model is compared to a previous transient latching probability model, which under predicts the SEU cross section based on transient distribution experimental data. As technology scales and logic SEU cross section becomes a dominant factor in SER, this model has demonstrated a capability, based on measured SET data, to calculate the transient latching probabilities that account for decreasing transient pulse width.

Irradiation data for a 14/16nm bulk FinFET DFF over a wide range of particle LET and supply voltage have been used to develop an empirical model that describes the change in single-event cross-section of any storage cell with variation in supply voltage. High-LET particle irradiation data along with simulation have confirmed a uniform increase in SEU cross-section as supply voltage is reduced, corresponding to an increase in transistor sensitive area. Through TCAD simulations the sensitive area ratio factor was found to correlate with the increase in sensitive area with decreasing supply voltage for FinFET devices. The results of this work indicate that for FinFET devices, change in sensitive area can result in a significant difference in SEU cross-section over supply voltage for high-LET particle

irradiation. This difference is directly correlated with the increase in transistor sensitive area and the increase has been defined for the 14/16nm bulk FinFET technology node. This work allows a minimal amount of experimental data to be used to predict the cell single-event behavior with decreasing supply voltage for both low and high-LET particles for a storage cell design in this technology node.

In this work, three models for evaluating single-event upsets in advanced technologies with increased speed of operation and decreased circuit supply voltage have been developed and implemented. Each of the models developed in this chapter addresses assumptions from previous SEU models based on lower clock frequency and higher supply voltage. This work provides circuit designers with new methods for evaluating SEU LET threshold, logic cross-section, and reduced bias cross-section for advanced technologies.

CHAPTER IV

MODELS FOR CHARACTERIZING SINGLE-EVENT TRANSIENTS

While measurements of single-event upsets are straightforward (a bit changes or it does not), quantifying the generation, propagation, and capture that must occur to observe an error due to a single-event transient presents a unique challenge. Experimental setups for measuring single-event transients are far more complex than those for single-event upsets. In this chapter, two experimental models are presented to enhance understanding of single-event transient cross-sections and distributions for a wide range of particle LET and circuit bias using limited SET data. A model for extracting fast SETs provides circuit designers with extended transient distributions for accurate logic SEU cross-section under high frequency circuit operation. Furthermore, a subset of experimental transient data is analyzed using transistor drive current to provide a method for analyzing SET response of FinFET devices for inverter variants.

Extracting Fast Single-Event Transients

This section is adapted from a paper that was submitted to TNS from NSREC 2018 and is currently under review titled "Exploiting SEU Data Analysis to Extract Fast SET Pulses."

In SET measurement circuits, designers must use multiple short chains of devices combined through an OR-gate network. Compared to typical logic paths in circuits where fast SETs can propagate and cause errors, these pulses may attenuate as they propagate through the chains and OR-gate network and not be captured. Furthermore, an SET must

be wide enough to trigger the measurement circuit and signal it to capture the transient and its width. These timing constraints have led to a fundamental limitation in the minimum measurable pulse width for SET characterization circuits.

Chapter III has shown that accounting for fast transients in radiation effect analysis becomes increasingly important as technologies scale and clock speeds increase. At the same time, Fig. 25 shows that SETs are decreasing in width below the experimental measurement circuit threshold. Although SET characterization circuits do not capture fast transients due to experimental limitations, these transients are increasingly abundant and are capable of causing single-event upsets as circuit speeds increase and accurate SET characterization is crucial for predicting soft error rates.

This section explores an innovative use of single-event upset data that will help radiation effects researchers overcome the inevitable minimum-pulse-width limitations of traditional SET measurements. A data analysis method has been developed by incorporating feedback-assisted capture of fast transients in minimum-sized latch circuits to extend the measured pulse width acuity window for companion logic chain SET data. Applying this method allows predictions to be made for combinational logic SEU response over a wider range of particle LET and temporal profiles than previously attainable.

SE Transient and Upset Measurement Discrepancy

Chains of logic gates and flip-flops were designed and fabricated in the 14/16nm bulk FinFET technology generation and irradiated with heavy-ions at Lawrence Berkley National Laboratory (LBNL) in order to characterize single-event transients and upsets. Here an explanation is given of the SET and SEU characterization circuitry as it pertains to this work, and a thorough explanation of the characterization chains and measurement circuit

design can be found in [3] and in Appendix A.

As discussed in [3], the SET capture circuitry including the OR-gate network and SET measurement circuit imposes limitations on the minimum measurable pulse width. This minimum pulse width was found by running fully parasitic extracted simulations in the 14/16nm PDK. The fastest transient at the output of the logic chains that could still be captured by the SET measurement circuit after propagation through the OR-gate network was found to be 15 ps for a simulation run at nominal voltage (0.8 V) and room temperature. A transient of width less than 15 ps cannot propagate to and trigger the measurement circuit; therefore, transients less than 15 ps wide are not captured experimentally by the SET characterization circuit [3].

The test chip was also designed with chains of flip-flops to experimentally determine single-event upset cross-sections. Thousands of flip-flops were chained together and single-event upsets were recorded by reading the output of the final flip-flop and comparing the output to the chain input. All of the SET and SEU experiments were run simultaneously. An inverter chain and D flip-flop (DFF) of the same transistor size and threshold voltage were implemented on the test chip. The schematic of the DFF included on the test chip is shown in Fig. 51. Heavy ion experiments over a wide range of LET were performed at LBNL in vacuum and at room temperature on the inverter and DFF chains. The circuits were run at nominal, 0.8 V bias and a 200 kHz clock speed. Each experimental test was run to a particle fluence between 2×10^7 and 2×10^8 ions/cm^2 with a maximum total fluence of 1.8 $\times 10^{10}$ ions/cm^2 per test chip. Fig. 38 shows the per sensitive transistor SET cross-section for the inverter chain and SEU cross-section for the D flip-flop chain. Error bars in the figure are calculated using the standard error. In most cases, the error bars cannot be seen in the figure, as they appear smaller than the data marker.

77
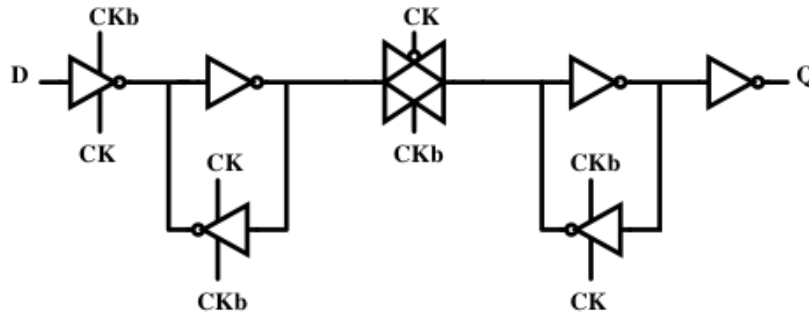
Figure 37: Schematic representation of the 14/16nm bulk FinFET conventional D flip-flop fabricated and irradiated alongside chains of inverters for single-event capture. The DFF uses minimum sized, regular threshold voltage inverters.
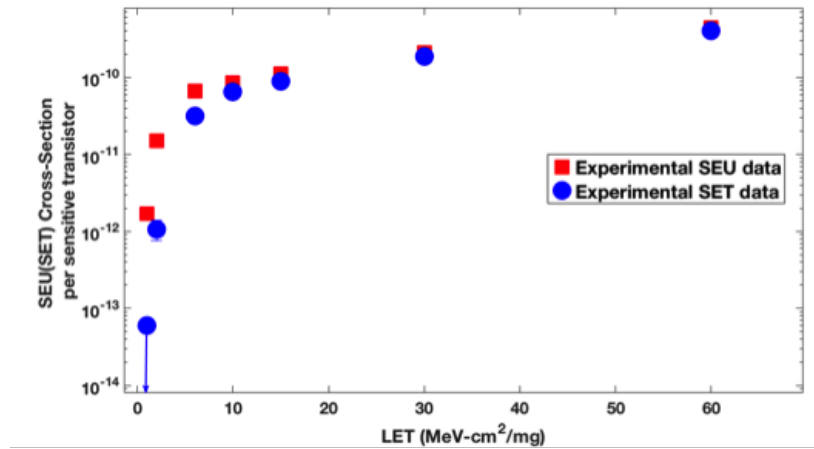
Figure 38: Experimental 14/16nm heavy-ion SET and SEU cross-section data over LET for nominal 0.8 V bias. Error bars are given for the standard error of measurement. Results are shown normalized per sensitive transistor so that the SET and SEU data can be directly compared.

The SET and SEU per transistor cross-sections are calculated as

$$\sigma_{SET} = \frac{\#\ SETs\ /fluence}{\#\ sensitive\ transistors\ per\ chain\ \times\ \#\ chains}$$

(27)

$$\sigma_{SEU} = \frac{\#\ SEUs\ /fluence}{\#\ FFs\ per\ chain\ \times\ sensitive\ transistors\ per\ FF}$$

For the inverter chain, the number of sensitive transistors is equal to the number of inverters since one transistor in each inverter is OFF (and sensitive) while the other is ON (and insensitive). For the DFF, consider an input of D = 0 and CLK= 0 in Fig. 51. With these input conditions, the master latch is storing its value, while the slave latch is loading. Therefore, an assumption is made that the slave latch is insensitive in this state. This assumption is based on the flip-flop operating at a low frequency and does not apply for high frequencies of operation where transients in the latch that is loading a value can also be captured. Therefore, three transistors are sensitive in the master latch: the PMOS in the inverter, the data-driven NMOS in the clocked inverter, and the clock-driven NMOS in the clocked inverter. A single-event strike to any of these transistors can change the DFF's state.

Considering the cross-sections per sensitive transistor rather than cross-section per inverter or flip-flop allows for a direct comparison between the measured SET and SEU data. Because the chains were made of identical transistors, one would expect the same single-event transients to be generated in both chains and therefore the single-event cross-section per sensitive transistor to also be equivalent. However, Fig. 38 reveals that the experimental SEU cross-section is consistently higher than the SET cross-section. Two factors contribute to this discrepancy in cross-section. First, the SET measurement circuit

79

has inherent limitations of measuring fast transients as discussed. The minimum measurable pulse width imposed by the SET measurement circuit does not allow all of the transients capable of causing errors to be captured. Second, the DFF has an enhanced ability to capture fast transients due to the positive feedback in its latches. Based on this observed difference in measured SET and SEU cross-section, a method has been developed to determine the number of SETs generated in transistors for this technology generation that are not captured by the SET measurement circuit, but may propagate through logic chains and cause errors.

<center>Transient Extraction Methodology</center>

By examining the data in Fig. 38, it is shown that for high LET particle irradiation, although the SEU cross-section per sensitive transistor exceeds the SET cross-section, the difference is relatively small. However, at low LET particle irradiation, the cross-sections diverge. For example, for a particle LET of 1 MeV-cm^2/mg, over 60 SEUs were captured and no SETs were captured. In this section, the observed difference between SET and SEU cross-section is explored as an effect of the different minimum measurable pulse widths imposed by measuring single-event particle strikes in inverter chains and flip-flops. In the inverter chain, the minimum measureable pulse width of the SET measurement circuit (pw$_{\text{SET,min}}$) is 15 ps. For the minimum measurable pulse width of a DFF (pw$_{\text{SEU,min}}$), I adopt the theory of a minimum full-width half-maximum (FWHM) internal voltage transient necessary to trigger a flip-flop bit corruption. Full parasitic extracted simulations were performed in SPICE to determine the minimum pulse width generated from an ionized particle strike that would cause an upset. A square pulse with 1 fs rise and fall times was applied at the output of the 14/16nm inverter and clocked inverter in the master latch of Fig. 51 in order to simulate a transient generated in the inverters. The minimum pulse width that caused the transient

to be captured in the master latch and therefore upset the flip-flop for a regular threshold voltage inverter operating at nominal voltage (0.8 V) and room temperature was found to be 6 ps. The minimum pulse to upset the DFF from a strike to the transistors in the clocked inverters was found to be 8.5 ps. Although the clocked inverters do show a larger minimum pulse to upset, I assume the absolute minimum pulse of 6 ps as the minimum measurable pulse width of the DFF in our analysis.

Consider an SET measurement circuit capable of capturing transients equal to the flip-flop minimum measurable pulse width (i.e., $pw_{SET,min} = pw_{SEU,min}$). If an SET measurement circuit were able to capture transients as fast as those captured in feedback-assisted latches, the number of measured transients per sensitive transistor would be approximately equal for an inverter chain and DFF of identical inverters. In this case, the measured cross-sections in Fig. 38 would also appear approximately equal because the experimental data was taken for a DFF and inverter chain using identical inverters. However, the results in Fig. 38, particularly for low LET particle irradiation, reveal up to over an order of magnitude difference in the measured SET and SEU cross-sections. Consequently, it is deduced that the difference between experimental SET and SEU cross-sections per transistor corresponds to the cross-section of generated transients of width greater than $pw_{SEU,min}$ (6 ps) and less than $pw_{SET,min}$ (15 ps). Based on this insight, for each experiment the number of SETs of pulse width pw (any width between $pw_{SEU,min}$ and $pw_{SET,min}$) can be found as

$$
\begin{aligned}
\# \ SETs \ (pw_{SEU,min} < pw < pw_{SET,min}) = (\sigma_{SEU} - \sigma_{SET}) \ \times \\
\# \ sensitive \ transistors \ per \ chain \ \times \ fluence
\end{aligned}
\tag{28}
$$

The transients extracted in (28) are the SETs captured in the DFF (pw > 6 ps) but not

captured in the inverter chain by the SET measurement circuit (pw < 15 ps). Figs. 39 and 40 present the SET pulse width distributions for irradiation of the inverter chain with Silicon (LET=6 MeV-cm^2/mg) and Xenon (LET=60 MeV-cm^2/mg) respectively. The blue SET pulse width distributions are the measured transient data from the inverter chain under heavy-ion irradiation. The red SET pulse width bins in Figs. 39 and 40 denote the number of pulses outside the SET measurement circuit acuity that have been extracted using (28). The high LET data in Fig. 40 show that only 13 SETs capable of upsetting a DFF were unaccounted for by the SET measurement circuit. Considering that a total 163 transients were measured through the combined SET and SEU analysis, the previously undetected SETs make up only 8% of the total captured transients. However, for LET= 6 MeV-cm^2/mg irradiation, over 50% of transients causing SEUs were not measured by the SET capture circuitry.
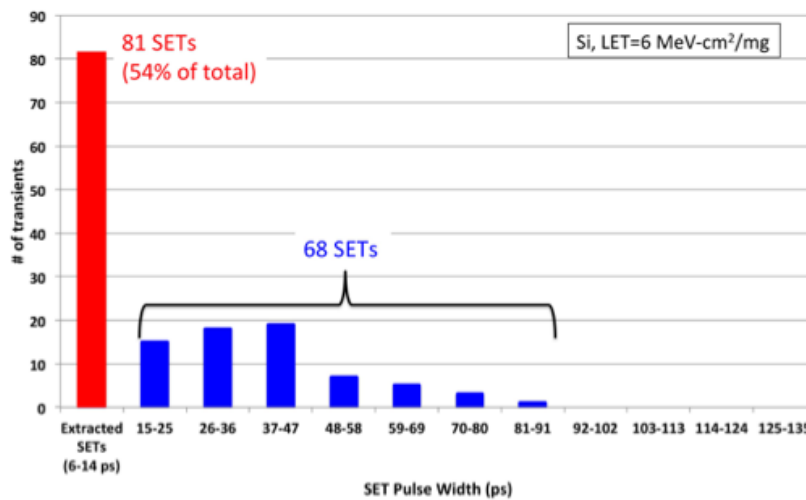
Figure 39: Single-event transient pulse width distributions for an inverter in the 14/16nm technology generation under low LET irradiation. Data shown in blue are the measured SET data from an inverter chain. The data shown in red are calculated from 28 which uses a combination of SET and SEU data to reveal the number of SETs generated that are capable of causing errors in logic, but not captured by the SET measurement circuit.
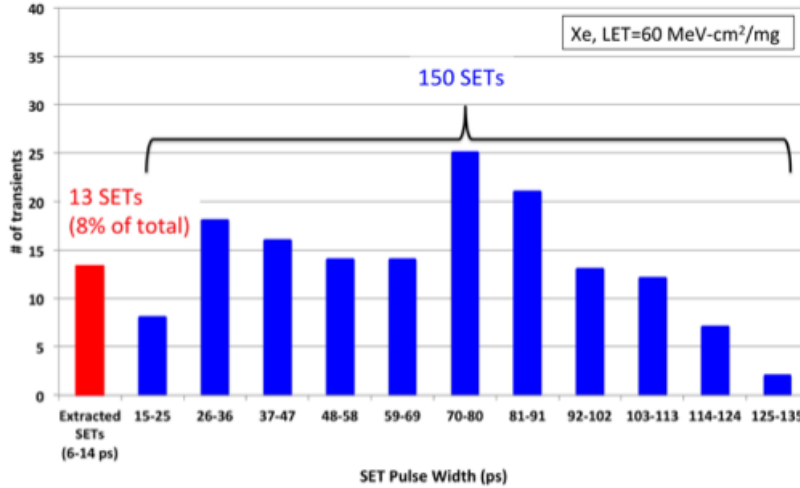
Figure 40: Single-event transient pulse width distributions for an inverter in the 14/16nm technology generation under high LET irradiation. Data shown in blue are the measured SET data from an inverter chain. The data shown in red are calculated from 28 which uses a combination of SET and SEU data to reveal the number of SETs generated that are capable of causing errors in logic, but not captured by the SET measurement circuit.

Table 6 shows the percentage of transients 6-14 ps wide across the experimental matrix of our broadbeam test found by implementing the method described. For irradiation with particle LET= 2 MeV-cm^2/mg, the previously undetected transients account for 93% of the total measured number. With particle LET= 1 MeV-cm^2/mg, only transients between 6 and 15 ps were measured by the SEU test circuit and no transients greater than 15 ps were measured by the SET characterization circuit. These results demonstrate that the method for extracting SETs below the minimum measurable pulse width presented in this section leads to greater understanding of SET distributions and total generated transients, particularly for low LET particle irradiation.

Impact of Fast SETs on SEU Cross-Sections

The results from applying the method developed in this work show a significant increase in the number of SETs measured on an inverter chain in 14/16nm FinFET technology by

Table 6: Percentage of SETs not captured by the SET measurement circuit that have been extracted by the analysis of this work.

Heavy Ion	Approx. LET (MeV-cm^2/mg)	Percentage of SETs 6-14 ps
Xenon	60	8%
Krypton	30	11%
Vanadium	15	20%
Argon	10	24%
Silicon	6	54%
Oxygen	2	93%
Boron	1	100%

extracting fast transients between 6 and 15 ps in width. In order to explore the impact of fast SETs on circuit-level single-event response, full parasitic-extracted simulations were performed in the 14/16nm technology generation PDK using the Institute for Space and Defense Electronics (ISDE) bias dependent model, which was calibrated to experimental data [26, 10], [10]. I found that a single-event strike to either OFF transistor in an inverter with an LET of 1 MeV-cm^2/mg produced a pulse on the output node that will not propagate through more than two subsequent inverters. Considering Fig. 38, it can be deduced that the SEUs experimentally captured at an LET of 1 MeV-cm^2/mg would not propagate through a typical logic chain. However, simulations reveal that a particle strike with an LET of 2 MeV-cm^2/mg or greater will propagate through a minimum of 5 inverters. Although the transients below the minimum measureable pulse width in the SET distributions are fast (6-14 ps), these transients are capable of propagating through a typical logic gate chain and being latched in a storage element.

SET distributions for logic gates in a given technology can be used to gain knowledge about combinational logic single-event upset cross-sections. In the previous section, it was shown in 32nm SOI technology that fast transients must be considered when using SET data

for logic gate error rate predictions. In 32nm SOI technology, excluding SETs on the order of the flip-flop setup-and-hold time resulted in an under estimation of the logic cross-section for logic gates. Harada et al. also discussed the importance of designing an SET measurement circuit that can capture transients with a minimum measurable pulse width of an inverter delay or the minimum pulse that can be latched in a flip-flop [33]. Furthermore, single-event transients on the order of flip-flop setup-and-hold times have been shown to contribute significantly to inverter single-event cross-sections, especially for low LET particle irradiation [74].

In order to examine the effect of accounting for (or not accounting for) the fast pulses extracted in this work, the logic SEU cross-section prediction method described in the previous section has been applied to a 5 stage inverter logic gate chain in the 14/16nm bulk FinFET technology. Recall that the method considers that any perturbation of a signal during the flip-flop setup-and-hold time can cause an error because it violates the setup-and-hold rule [65]. Theoretically, this assumption will provide an upper bound for the SEU cross-section and in 32 nm SOI technology the assumption resulted in predictions that agree well with experimental data. First, 1,000 random samples from an SET distribution are taken and the probability that each would cause an upset for a given frequency of operation using (18) and the setup-and-hold time of a standard dual interlocked storage cell (DICE) flip-flop is determined. A commercial NAND DICE was designed in 14/16nm technology and parasitic extracted simulations of the setup-and-hold time at room temperature and nominal 0.8 V bias revealed a setup-and-hold time of 25 ps. The average error probability for all of the transients is then used to predict the logic SEU cross-section from the measured inverter SET cross-section using (21).

The described method has been applied for a 5 stage inverter chain in 14/16nm technology

85

using the SET pulse width distributions in Figs. 39 and 40. The predicted logic SEU cross-section results are shown in Fig. 41 for three different particle LET irradiation data sets and over clock frequency. Single-event upset logic cross-section is predicted with and without the fast transients extracted in this work. The blue data sets indicate predicted SEU cross-section using measured SET data only. The prediction from this work, which includes extracted, fast transients, is shown in red.

Predicted SEU cross-sections in Fig. 41 for high LET particle irradiation (LET=60 MeV-cm^2/mg) reveal indistinguishable differences between the directly measured SET distribution data and the modified distribution to account for fast pulses. This result is due to only 8% of the transients being unaccounted for in the original SET data. However, the data for particle LET=6 MeV-cm^2/mg shows a 2× difference in the predicted SEU cross-sections. Furthermore, the prediction of logic SEUs based solely on measured SET data for irradiation with a particle LET=2 MeV-cm^2/mg, is an order of magnitude lower than the prediction based on the full SET pulse width distribution revealed by this work. Therefore, the inclusion of fast transients based on the method developed and employed in this work can improve the accuracy of single-event upset logic cross-sections by up to an order of magnitude.
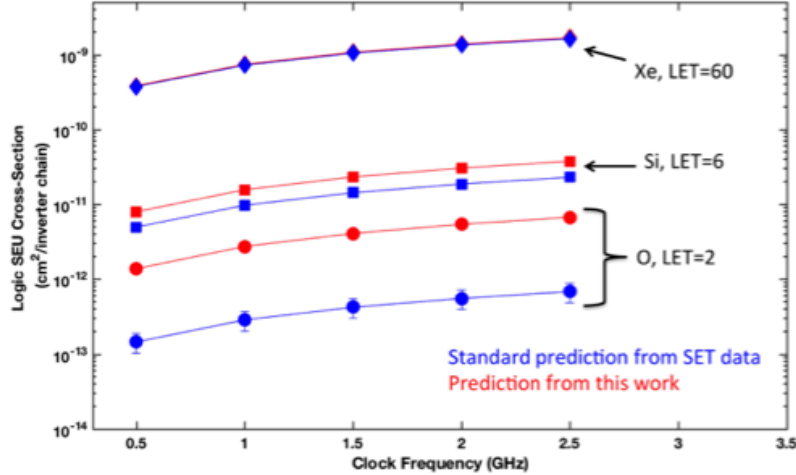
Figure 41: Predicted logic SEU cross-sections vs. clock frequency for a 5-gate inverter chain in the 14/16nm technology generation using the SET and SEU data from Fig. 38. Results are based on the method presented in [14] and are shown for three different particle LETs. The blue points show the standard prediction using only SET data and the red points show predictions based on applying the method of this work. The information about fast transients gained from this work increases the predicted cross-sections for logic gates based on improved accuracy of accounting for all generated SETs that can cause upsets.

Evaluating Drive Current Effects on SETs for Bias Variation

This section is adapted from a paper published in TNS in August, 2018 titled "Effect of Transistor Variants on Single-Event Transients at the 14/16nm Bulk FinFET Technology Generation."

The pulse widths and cross-sections of single-event transients vary based on technology parameters, transistor variants, and circuit operation parameters. Factors such as logic gate type, threshold voltage, transistor size, output capacitive load, and well/body contact placement have all been shown to impact the number and duration of SETs generated in combinational logic [36, 75, 34, 76, 77, 78, 47]. An understanding of how these factors impact SET sensitivity can greatly enhance radiation hardening by design techniques in each emerging technology node. The technology scaling from bulk planar to SOI planar (and

now to FinFET transistors) has further complicated the understanding of SET sensitivity. Understanding how transistor variants affect SET response at the latest technology node is especially important because FinFETs have a transistor structure unlike previous bulk and SOI technologies. While technology scaling leads to a decrease in transistor sensitive area, supply voltage also continues to scale down. These and other competing factors that contribute to SET formation in logic gates call for experimental results that will elucidate the contributions of each factor.

In this section, I explore the effects of transistor variants on SET pulse widths and cross-sections for FinFET logic gates. Results from heavy-ion irradiation of integrated circuits (ICs) designed at the 14/16nm bulk FinFET technology generation are presented across a range of linear energy transfer and supply voltage. Observed differences in SET pulse widths and cross-sections are evaluated as a function of transistor drive current through simulation. The results indicate that transistor drive current is a key factor governing SET pulse widths and cross-sections. For high LET particle irradiation, drive current is a dominant factor in determining SET pulse widths and cross-sections, while low LET particle irradiation data reveal that secondary factors contribute more to SET sensitivity.

A technology characterization vehicle was designed and fabricated at the 14/16nm bulk FinFET technology generation to characterize SETs over LET and supply voltage for variations in logic gate type, threshold voltage, and the number of fins in the gate. Appendix A provides a list of all the logic targets that were included in this work. While a brief description of the test chip circuitry is provided in this section, a detailed description of the SET capture circuit and test chip design can be found in [3]. The test chip was designed in a similar fashion to previous SET capture circuits using short logic gate chains that are combined using an OR tree [4]. Level shifters on the outputs of the logic chains provided

88

the capability to operate the logic chains at a variable supply voltage, while maintaining a nominal supply voltage for the propagation and SET measurement circuitry. The minimum pulse width that can be detected by the measurement circuit is 15 ps with a 10 ps per bin resolution.

A major concern when measuring SETs in chains of logic is the pulse broadening and attenuation that can occur as the transient propagates down the chain before it reaches the measurement circuit. Circuit effects such as hysteresis and asymmetric loading and current drive have been shown to affect pulse propagation through logic chains both experimentally and through analytical circuit theorems [36, 79]. Quantifying these effects is important to make an accurate interpretation of measured SET data from chains of logic. Short logic chains of less than 23 gates per chain were used on the test chip to minimize any propagation-induced skew. Furthermore, an on-chip pulse generator was used to verify the TCV's functionality and to quantify pulse attenuation and broadening through the chains and level shifters. Only the skew in the chains and level shifters needed to be quantified because the measurement circuit always operates at nominal voltage. Two pulses of different widths (100 ps and 270 ps) were injected into the logic chains and measured at the output. The pulse widths were obtained based on measuring the frequency of an on-chip ring oscillator. The skew through the level shifter increases when the circuit is operated at lower than nominal biases; however, less than 2 bins of resolution skew between the injected and measured pulse widths was observed with a circuit bias as low as 0.5 V [3]. The pulse width distributions and cross-sections presented in this paper have been corrected for pulse broadening according to the measured skew from the injected pulse tests. For example, down to a 0.65 V bias, no broadening was observed through the level shifters during the on-chip pulse generator test. Therefore, the 0.65 V pulse width distributions are presented as directly measured from

89

the measurement circuit. However, 2 bins of broadening were observed in the same pulse propagation test for a 0.5 V circuit bias. Therefore, the 0.5 V pulse width distribution data is presented as the measured data shifted by 2 bins to account for the broadening induced by the level shifters at the low bias condition.

SET Sensitivity of Transistor Variants

Several transistor-level design factors (e.g. device size and threshold voltage) can change the single-event sensitivity of combinational logic. Furthermore, these effects on a circuit's radiation response can change with decreasing technology feature size and process type. An SET study performed on 32nm SOI transistor variants determined body contacting to be an effective SET mitigation technique [75]. A recent study performed in 65nm bulk planar technology compared the SET sensitivity of several transistor variants. The results of this study revealed that the technique of adding output capacitance is more effective for hardening against SETs than increasing gate size [34]. Elucidating the effects of design factors on the SET sensitivity of the 14/16nm FinFET node is especially important due to the change in technology size and transistor structure from previous works.

Understanding how circuit design factors affect SET pulse widths and cross-sections is not only important for predicting radiation sensitivity of combinational logic, but can also be vital for developing radiation-hardened-by-design circuits. Radiation hardening techniques for combinational logic such as temporal sampling and the use of guard gates require knowledge about single-event transient width for effective single-event mitigation [24, 80]. Data driven knowledge about the factors influencing the SET response of FinFET logic gates will provide greater fidelity in RHBD implementation for emerging technology nodes.

90

When a particle strikes and forces a node to the opposite logic state, the drive current of the ON transistor becomes the restoring current that restores the logic gate back to its original state. Therefore, increasing the drive current of transistors in a circuit results in fewer or shorter single-event transients or both. Increased drive current can be achieved by using a lower V_t, by increasing the number of fins, or through effective fins via multiple fingers in the logic gate. Inverter chains with these transistor variants were included on the TCV to understand how the variants change a logic gate's SET response to irradiation. Two inverters of the same size and layout that have differing threshold voltages were included on the TCV. A 3-fin inverter and a 3-fin, 2-finger (6-fin effective) inverter that have the same threshold voltage were also included.

Heavy ion experiments were performed on the test chip over a wide range of LET, as well as over six different bias conditions between nominal (0.8 V) and 0.5 V bias. An SET pulse width distribution comparison between the three inverter types is shown in Fig. 42. The distributions show the number of captured pulses in each pulse width bin for irradiation with Cu (LET= 21 MeV-cm^2/mg) at a 0.65 V bias. Fig. 43 shows the reverse cumulative cross-section verses pulse width for each inverter chain tested. Figs. 42 and 43 reveal variation in both the pulse width distributions and the cross-sections, which are induced by the differences in threshold voltage and the number of fins. An increase in threshold voltage from a low to regular V_t 3-fin inverter shows an increase in SET cross-section, as well as SET pulse width. Conversely, the increase in the fin number from a 3-fin inverter to 6-fin inverter having the same threshold voltage results in fewer and shorter captured transients.

Since the two inverters differ only in threshold voltage, the increase in both the number and the width of SETs from the low to the regular V_t inverter seen in Figs. 42 and 43 is attributed to a difference in drive current. The restoring current from the ON transistor
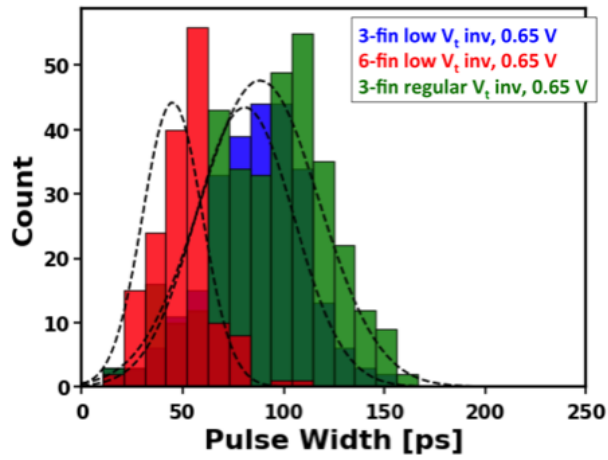
Figure 42: Heavy-ion SET pulse width distribution plot for copper (LET= 21 MeV-cm^2/mg) irradiation at 0.65 V bias. Three different transistor variants show variation in pulse width that corresponds to the changes in drive current.

Figure 43: Heavy-ion reverse cumulative SET cross-section vs. pulse width plot for copper (LET= 21 MeV-cm^2/mg) irradiation at 0.65 V bias. Transistor variants are compared; the comparison shows variation in pulse width and cross-section that is attributed to the differences in drive current.

depends on the voltage difference between the transistor's gate-source voltage and the threshold voltage. Therefore, an increase in threshold voltage from low to regular V_t results in a lower transistor drive current. By considering two inverters of the same threshold voltage and different fin count, the 6-fin inverter has a higher drive current and nodal capacitance than the 3-fin inverter. Both of these factors contribute to decreasing number and width of SETs. However, the 6-fin transistors also add additional sensitive area, which contributes to an increased number of generated SETs. The cumulative effect of increased fin count results in the 6-fin inverter producing the shortest and fewest captured transients (as seen in Figs. 42 and 43).

The extensive set of experimental data with bias variation collected on the SET test chip allows for an isolated investigation of drive current as one of the factors that determines SET pulse widths and cross-sections. Understanding the key factor(s) driving the observed differences in SET response across these transistor variants could allow circuit designers to predict the SET response of other FinFET transistor variants without extensive radiation testing for characterization of each individual transistor variant. Transistor drive current is evaluated through simulation in the next section for different FinFET variants and explored as a key factor controlling SET pulse width and cross-section.

The difference in SET pulse width distributions and cross-sections observed across transistor variants in Figs. 42 and 43 could be due to a variety of changing factors such as drive current, output capacitance, and sensitive area. Heavy-ion data collected across a wide range of supply voltage for the SET test chip provides an opportunity to isolate the effect of transistor drive current on the SET response. In order to evaluate the effect of drive current on inverter SET sensitivity, simulations were implemented at the circuit-level using the appropriate PDK for different transistor variants and biases. An Id-Vg sweep

was performed for an NMOS and PMOS transistor of each inverter variant discussed in the previous section. In Fig. 44 the drive current is plotted for each inverter variant across bias. Only the NMOS Id-Vg sweeps are shown for clarity, though the PMOS sweeps show similar results since the NMOS and PMOS transistors were current matched. The drive currents in Fig. 44 are shown normalized to the current of the 3-fin low V_t inverter at nominal bias (0.8 V). As the supply voltage decreases, the drive current also decreases. However, the rate of decrease in drive current over bias differs based on transistor variant.
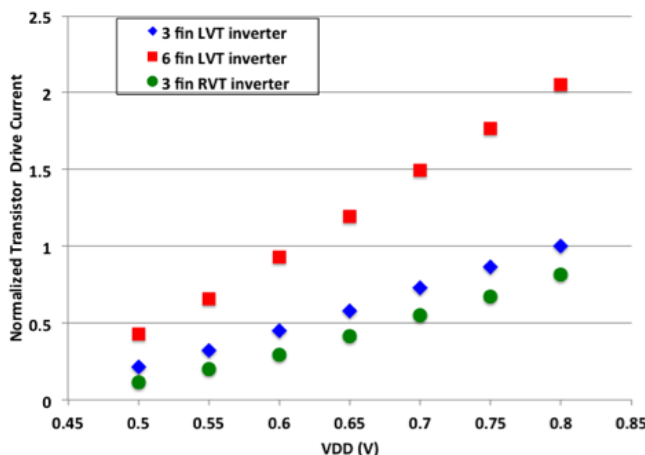
Figure 44: A comparison of simulated transistor drive current vs. supply voltage for three transistor variants fabricated and experimentally tested in bulk FinFET technology. Drive currents for NMOS and PMOS transistors were matched. Currents are normalized to the 3-fin low V_t inverter current at a nominal bias (0.8 V).

By observing the respective currents at 0.65 V bias for each inverter variant, a correlation can be drawn between the drive current and the SET data of Figs. 42 and 43. The results can be explained qualitatively by the changes in drive current simulated for each transistor variant. In order to explore drive current as a key factor in determining SET response, though, data for variations in supply voltage are used to compare SET data for transistor

variants operating with comparable drive currents. This analysis was performed in order to isolate drive current and establish whether or not it is a dominant factor that determines SET pulse widths and cross-sections. Data taken at different supply voltages resulting in similar drive current are compared for transistor variants in Figs. 45 and 46. For example, Fig. 44 reveals the drive current of the regular V_t transistor at 0.65 V to be approximately equal to the drive current for the low V_t transistor at 0.6 V. Likewise, the drive currents of the low V_t 3-fin transistor at 0.6 V and the regular V_t 3-fin transistor at 0.65 V are approximately equal to the drive current for the low V_t 6-fin transistor at 0.5 V. SET data for each transistor variant at the supply voltage resulting in a comparable drive current is shown in Figs. 45 and 46. When the drive currents for different transistor variants are matched, SET data overlay and reveal similar SET pulse width distributions and cross-sections.
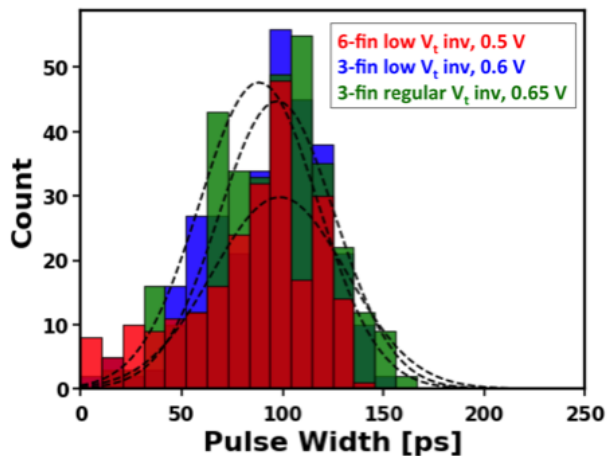
Figure 45: Heavy-ion SET pulse width distribution plot for copper (LET= 21 MeV-cm^2/mg) irradiation. Data is plotted for irradiation at different supply voltage values such that the drive current is matched for each transistor variant.

The analysis performed here highlights the significance of drive current as a dominant factor contributing to the SET sensitivity of FinFET logic gates for high LET particle
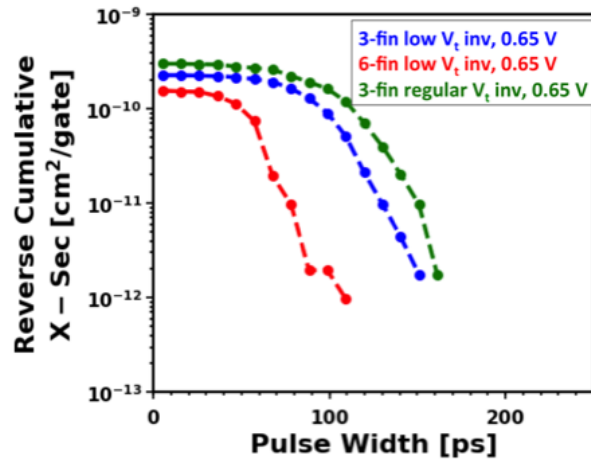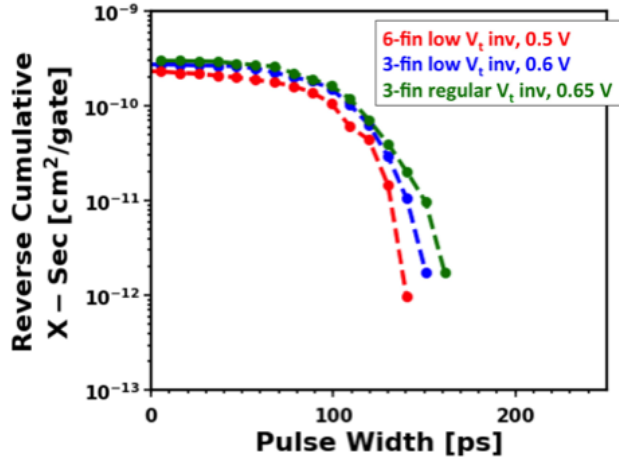
Figure 46: Heavy-ion reverse cumulative SET cross-section vs. pulse width plot for copper (LET= 21 MeV-cm^2/mg) irradiation. Based on the transistor drive currents in Fig. 44, data is plotted for each transistor variant at the supply voltage that results in matched transistor current drive. Results show similar SET cross-section when current drive is matched.

irradiation. Furthermore, it shows that the SET response for a single logic gate design over voltage can be used to extrapolate SET response of transistor variants in the same technology node by comparing simulated drive currents. Conversely, SET data at a single supply voltage over multiple transistor variants can be used to evaluate response over bias through simulated drive current. It should be noted that while the data analysis and simulation results of this work support drive current as a key factor in determining SET pulse width and cross-section for high LET particle irradiation, the results do not exclude the possibility that other factors such as output capacitive load and circuit layout may also contribute significantly to SET response. The SET response likewise depends not only on the transistor and circuit design factors, but it also varies with radiation environment. The next section discusses the difference in particle LET variation on SET sensitivity for the three transistor variants in the previous section.

SET Characterization for LET Variation

The correlation between SET distributions and drive current was also explored for lower LET particle irradiation data. Fig. 47 shows SET data for the three transistor variants at a 0.65 V bias for irradiation with oxygen (LET= 2 MeV-cm^2/mg). Data for the transistor variants with similar drive current are plotted in Fig. 48. By comparing Figs. 47 and 48, an increase in pulse width and cross-section toward the SET distribution of the 3-fin regular V$_t$ inverter chain can be seen for the 3-fin and 6-fin low V$_t$ inverter chains. Because the SET pulse widths produced by low LET particle irradiation are comparable to the minimum measurable pulse width from the measurement circuit, it is likely that the discrepancy in SET cross-section observed in Fig. 48 is due, in part, to this limitation. This discrepancy also suggests that secondary factors such as output capacitance contribute more to the SET sensitivity of the inverters for low LET particle irradiation than for high LET. Circuit designers must consider that in terrestrial environments with primarily low LET particle interactions drive current alone may not be as good of an indicator of the SET response as it can be for high LET irradiation.

In order to further investigate the effect of particle LET on SETs generated in inverters of different transistor variants, Kauppila et al.'s bias-dependent model was used to simulate worst-case particle strikes on inverters in circuit-level SPICE simulations [26]. The bias-dependent, single-event compact model has been calibrated to the 14/16nm bulk FinFET PDK [10]. An SET was simulated in a single chain of less than 23 inverters for each of the transistor variants with all extracted parasitic elements. The first inverter in the chain was struck and the voltage transient was measured at the inverter chain output before the level shifter. Two sets of simulations were performed: one at 0.65 V bias and the other at varying biases so that each of the three transistor variants had similar drive current (i.e.,
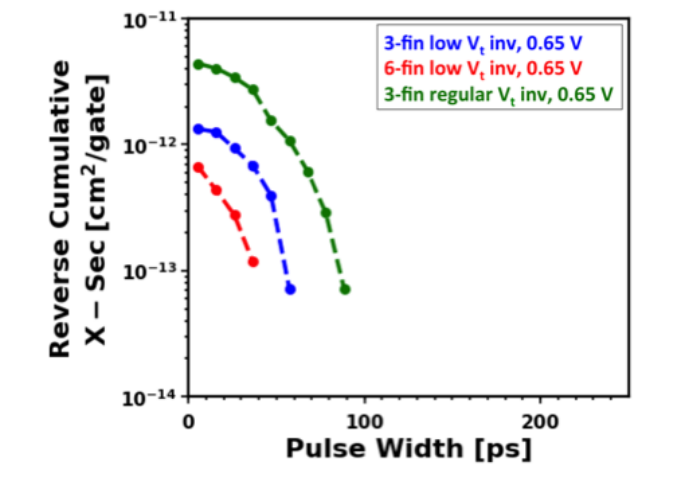
Figure 47: Heavy-ion SET reverse cumulative cross-section plot for oxygen (LET= 2 MeV-cm^2/mg) irradiation at 0.65 V bias. The variation in pulse width and cross-section for the transistor variants is attributed to changes in drive current.
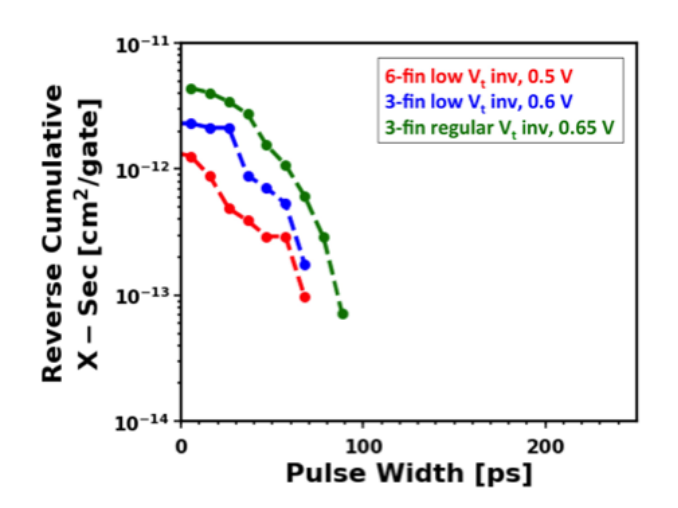
Figure 48: Heavy-ion SET reverse cumulative cross-section plot for oxygen (LET= 2 MeV-cm^2/mg) irradiation for different supply voltage values such that the drive current is matched for each transistor variant.

Table 7: SPICE Simulated Logic Gate SETs for Transistor Variants

LET (MeV-cm^2/mg)	Inverter Type	SET Pulse Width (ps)	
		0.65 V bias	Varying bias for matched drive current
3	3 fin low V_t	19.2	30.3
	6 fin low V_t	no SET	no SET
	3 fin regular V_t	36.2	36.2
20	3 fin low V_t	57.1	74.5
	6 fin low V_t	25.5	77.1
	3 fin regular V_t	86.8	86.8

0.65 V bias for 3 fin regular V_t, 0.6 V for 3 fin low V_t, and 0.5 V for 6 fin low V_t as shown in Fig. 44). In order to match simulated data with presented heavy-ion data in this work, particle strikes of LET= 3 and 20 MeV-cm^2/mg were performed. Results of the simulated particle strikes are given in Table 7. (Note that simulated transients resulting from particle strikes of LET= 2 MeV-cm^2/mg were attenuated and did not propagate to the end of any of the inverter chains. Therefore, the low LET simulation data in Table 7 is given for particle LET= 3 MeV-cm^2/mg.)

In fact, the transient generated by a particle strike of LET= 3 MeV-cm^2/mg attenuates in the highest drive current, 6-fin low V_t inverter chain and does not propagate to the output of the chain. The high-LET results at varying biases and matched drive currents show approximately one measureable bin (10 ps) difference between the transient pulse widths. Again, a particle strike of LET=3 MeV-cm^2/mg on the 6-fin low V_t inverter chain does not propagate an SET to the output. However, the 3-fin inverter chains also show less than one measureable bin of difference in pulse width for low LET particle strikes. Furthermore, the low LET transients generated are very close to the minimum measureable pulse width of the circuit, contributing to the reduction in experimental cross-section as drive current

increases. Both experimental and simulated SET data for transistor variants agree that for high LET particle irradiation, drive current is a good metric for comparing SET sensitivity of combinational logic. However, simulation results for low LET particle irradiation show that the effect of nodal capacitance contributes to attenuation of small pulses. This effect makes a significant contribution to the measured SET pulse widths and cross-sections of logic gates for low LET particle irradiation.

Design Tradeoffs for Low Bias Operation

Advancements in technology continuously present challenges for evaluating trade-offs between power, speed, area, and radiation hardness of combinational logic designs for space applications. Results from this work, which highlight the significance of drive current in determining SET pulse width and cross-section, provide insight for RHBD design in advanced FinFET technology particularly for high LET particle irradiation. Reducing transistor threshold voltage has become a common practice, since power consumption is a major area for concern in advanced technologies [76, 47, 8]. Our data have revealed decreasing SET pulse width and cross-section for lower V_t inverters at the 14/16nm FinFET technology generation. Data with regard to changing supply voltage show that drive current matched transistors produce a similar SET response. These data suggest that an analysis of the change in drive current for different threshold voltage inverters can be used to understand how different threshold voltage inverters will behave under different bias conditions. For example, a circuit designer may be faced with the option of increasing threshold voltage from low to regular V_t in order to save power, knowing that the increased threshold voltage would result in increased SET pulse width. From Fig. 44, this choice results in an increase in SET pulse width and cross-section comparable to the change in a low V_t inverter's SET response

seen by decreasing supply voltage by 0.05 V. Similar comparisons can be made for inverters of varying threshold voltage in order to evaluate the trade-off between radiation hardness and power consumption. Another common strategy for increasing the robustness of a logic gate to withstand radiation effects at previous technology nodes has been increasing transistor size. However, the benefit of increasing drive current via transistor size can be negated, and even overtaken, by the negative effect of added sensitive area and increased nodal capacitances. Our data reveal that an increased drive current due to increasing transistor size results in a decrease of SET pulse widths cross-sections. A trade-off analysis for these parameters has been evaluated for previous technology nodes [36, 75, 34], but this trade-off must likewise be evaluated and analyzed in FinFET technology. Fig. 49 presents SET cross-section data for the FinFET 3-fin and 6-fin inverters across particle LET for nominal bias. Although the increase in fin number correlates to an increase in sensitive area, SET cross-section is repeatedly lower for 6-fin transistors compared to 3-fin transistors as ion LET increases. I speculate that the observed decrease in cross-section for increased transistor size is due to the decrease in SET pulse width below a certain capture threshold. That is, as SET pulse width decreases below a certain threshold, the probability of capture decreases. With regard to the SET measurement circuit, the threshold is due to the minimum measurable pulse width (i.e., 15 ps). However, the same phenomenon may occur in any digital system. For example, flip-flops have a capture threshold equal to the loop delay of their latching circuit. Combinational circuits will have a capture threshold on the order of their propagation delay. As drive current increases due to increased transistor size, SET duration gradually decreases below the capture threshold leading to an effective decrease in cross-section.
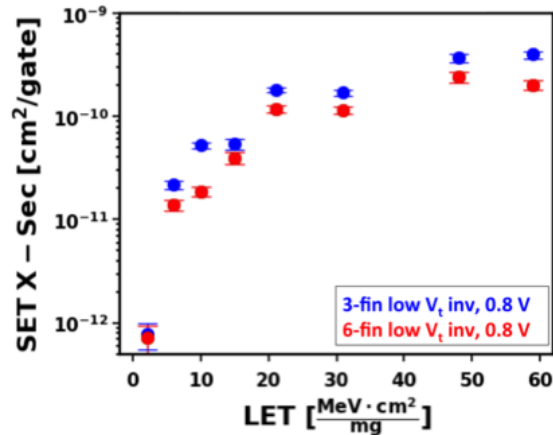
Figure 49: SET cross-section vs. LET plot for 3-fin and 6-fin low V_t inverters at a nominal 0.8 V bias. Increasing the size of FinFET transistors results in lower SET cross-section even for high LET particle irradiation due to the 6-fin transistor producing many pulses smaller than the measureable pulse width of the measurement circuit.

Summary

A model has been developed that provides insight into understanding single-event transient distributions and overcoming the inherent time-resolution limitations of SET measurement circuits. The presented method extends the transient pulse width threshold by exploiting the difference between the minimum measurable pulse widths for SET and SEU test circuits. The analysis results in transient distribution data from previously undetected, fast transients. Employing the method described at the 14/16nm technology generation provides an accurate data-based prediction of all of the generated transients that can propagate in logic and cause errors. Although the addition of fast single-event transients may be negligible for high LET particles, the insight gained from this method is invaluable for low LET particle contributions where the vast majority of transients capable of causing upsets are below the minimum measureable SET pulse width. Prior to the proposed method of this work, transients below the minimum measureable SET pulse width were not captured, and

therefore unaccounted for when using SET data for predicting error rates in combinational logic.

By analyzing single-event transient data across bias for 14/16nm bulk FinFET inverter chains with variation in transistor parameters, a method for evaluating SET response over bias has also been developed. Understanding and predicting the impact of bias on single-event response is crucial for advanced technologies because reduced bias operation has become a common and viable practice for power savings. This chapter discusses the impact of drive current on SET pulse width and cross section. A method is provided for utilizing a subset of experimental data for one logic gate over bias or multiple logic gates at a single bias in conjunction with drive current to elucidate the SET response of a variety of transistor variants over a wide range of circuit bias.

The two models presented in this chapter are given to inform single-event transient estimation in advanced technologies. Experimental limitations are overcome by extracting fast SETs below the measurement circuit resolution and by correlating transistor drive current and SET characterization for FinFET devices.These insights beyond experimental results expands knowledge of single-event transients generated in advanced, fast technologies and low bias operation.

CHAPTER V

IMPACT AND CONCLUSIONS

As circuits scale, increasing speed and decreasing bias pose new challenges for experimental characterization and modeling of single-event effects. In this work, several models have been developed for characterizing single-event effects in advanced technologies. The presented models introduce address outdated assumptions in previously developed models and contribute novel methods for characterizing single-event transients and upsets while taking into account scaling effects on circuit speed and bias.

An analytical model has been developed to determine the minimum charge to upset an SRAM as circuit associated with an error function single-event current waveform as switching speed and single-event current approach the same time scale. The model closely follows the results from data-calibrated simulations with an increased charge to upset from the traditional critical charge estimation. Utilizing the presented model will prevent designers from over designing circuits based on the critical charge time-independent $Q_{crit}=C \times V_{DD}$ approximation.

As technology decreases in feature size, transient pulse widths also decrease. The impact of these fast transients on single-event upset logic cross-section is discussed for 32nm SOI and 14/16nm bulk FinFET circuits. Results for 32nm SOI SEU logic cross-section estimations reveal the importance of including transients on the order of flip-flop setup and hold times in data-based calculations. Therefore, a method has been developed for extracting fast single-event transients from single-event upset data that are not experimentally captured on SET test circuits. Extracting fast SETs from single-event data can be implemented for any

technology node by including an inverter chain and flip-flop of the same inverter type on a test characterization vehicle. Fabricating these companion circuits on future TCVs will extend the knowledge of transient distributions beyond previously attainable single-event data.

Two models have been implemented for 14/16nm FinFET circuits to elucidate the effects of bias on single-event upset and transient cross-section. The result of the SEU analysis is an empirical model for estimating high LET bias dependence of SEU cross-section. For SETs, determining drive current as a key factor that influences SET capture in FinFET logic gates has given circuit designers a simple means of comparing the radiation response of different inverter designs without extensive radiation testing of individual designs. Both of these models provide circuit designers with data-based methods for evaluating the trade-off space between power savings and increased radiation sensitivity for low bias operation of advanced technology circuits.

The models developed in this work consider circuit speed and low bias circuit operation to advance the state-of-the-art for single-event characterization at advanced technology nodes. The analytical memory circuit SEU model and method for extracting fast SETs can be utilized to gain insight into the time-dependent response of circuits to single-events on comparable time scales to switching speed for any technology node. These models will become increasingly important as circuits continue to scale and logic gate switching speed and single-event charge collection times converge. In addition to advances in circuit speed, changes in transistor structure to FinFET devices allow advanced technology circuits to operate at near-threshold biases. Models elucidating bias effects on single-event transients and upsets in 14/16nm FinFET technology are presented. The models presented in this

disseration have been used to overcome experimental limitations for characterizing single-event effects in advanced technologies. As circuits continue to increase in speed and decrease in bias, the insights gained from this work will serve circuit designers with data-supported models to account for the effects of these changes on single-event response.

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Appendix A

32NM AND 14/16NM SINGLE-EVENT CHARACTERIZATION

This appendix includes descriptions of the test chips used to evaluate single-event effects in 32nm planar SOI and 14/16nm bulk FinFET technologies in this work. Experimental conditions and data for the single-event upset characterization structures beyond the analyses in this dissertation are given. Note that the data presented in this appendix focuses on single-event upsets because extensive single-event transient data for these test chips can be found in Maharrey's dissertation [59] .

14/16nm Bulk FinFET Technology

Extensive single-event data sets have been obtained through experiments performed on test structures in 14/16nm bulk FinFET technology. These data have been used to elucidate the effects of scaling and advances in technology on single-event effects which prompted the research objectives of this work.

Test Chip Design

Parts of this section are adapted from IEEE TNS 2018 paper "Exploiting Parallelism and Heterogeneity in Radiation Effects Test Vehicle for Efficient Single-Event Characterization of Nanoscale Circuits."

The TCV, designed and fabricated for this work, was developed with an emphasis on testing multiple combinational logic cells and flip-flop shift registers over bias, angle of incidence, and heavy-ion linear energy transfer values. The TCV was designed to be bonded

on two sides in order to perform high-angle testing without interference from bond wires.

The test chip included three flip-flop designs to characterize heavy-ion SEU cross-section over a range of particle LET values and supply voltages. A shift register design of 4K stages was used for SEU characterization and an on-chip pulse generator was used to verify the functionality of the shift registers before irradiation experiments were performed. The direct outputs from the shift registers were monitored during irradiation to count errors.

Previous SET target and measurement circuit implementations have included a single target for each of the combinational logic cells to be characterized and a method to propagate the SET to the target output, either using a single long chain of logic or multiple short chains and an OR-gate network. Each target is tested one at a time, where the target output is directly connected, or multiple target outputs may be multiplexed and connected, to one or more SET measurement circuits [4, 12].

Similar to previous SET characterization circuit designs, the test chip includes parallel short chains of logic gates, an OR-gate propagation network, and SET measurement circuit [35, 4]. A key and novel feature of this test chip design is the implementation of heterogeneous SET logic gate targets in a unique flagging system, which allows for simultaneously testing multiple target variations. Additionally, the SET targets were developed to operate with a variable supply voltage for the combinational logic and a constant supply voltage for the SET propagation network and measurement circuit, which provides the capability of multiple bias characterization of SETs in the combinational logic while maintaining a single calibration point for the SET propagation and measurement circuits. The short combinational logic chains utilized in the SET target are connected to a variable supply voltage and include a voltage level shifter between the short chain output and the OR-gate propagation network, which is enabled by breaking the V_{DD} supply rail and N-well between the combinational

116

logic chain and level shifter.

From the output of each short logic gate chain, an SET propagates through the OR-gate network to the measurement circuit [3, 35]. The measurement circuit outputs a string of zeros and ones, which indicate the width of the transient pulse. If a single-event upset occurs in the measurement circuit, the upset would appear in the output string as a bubble, unless it occurred at the 0 to 1 transition. Therefore, an SEU is most often be detected and the maximum error incurred by an SEU is a captured pulse width reduction by one bin.

Table 8 provides a list of the flip-flops and combinational logic variants, design parameters, and cell counts included on the characterization test chip.

Table 8: Listing of the Flip-Flops and Combinational Logic Cells, with Design Parameters, included on the Bulk FinFET TCV Design

Cell	# Fins	Threshold Voltage	Spacing	# Cells	Supply Voltage
DFF	2	VT_A	Min.	8,000	0.45 to 0.8 V
DICE-based FF	2	VT_A	Min.	8,000	0.45 to 0.8 V
STQQb FF	2	VT_A	Min.	12,800	0.45 to 0.8 V
Inverter	3	VT_A	Min.	17,408	0.45 to 0.8 V
Inverter	3	VT_A	4X	11,264	0.45 to 0.8 V
Inverter	3	VT_B	4X	11,264	0.45 to 0.8 V
Inverter	6 (effective)	VT_A	Min.	13,312	0.45 to 0.8 V
NAND	3	VT_A	Min.	13,312	0.45 to 0.8 V
NAND/NOR	3	VT_A	Min.	13,312	0.45 to 0.8 V
NOR/NAND	3	VT_A	Min.	13,312	0.45 to 0.8 V
Level Shifter	N/A	VT_B	Min.	1,536	0.45 to 0.8 V
Inverter	3	VT_B	Min.	17,408	0.45 to 0.8 V
NAND	3	VT_B	Min.	13,312	0.45 to 0.8 V
CVSL Cell	N/A	VT_B	Min.	8,704	0.8 V
RHBD Cell	N/A	VT_B	Min.	4,352	0.8 V

The layouts for each of the three flip-flops are shown in Fig. 50. The Schmitt-trigger/Q-Qb (STQQb) flip-flop was developed as an RHBD option for circuit designers that will provide increased radiation hardness beyond a standard commercial DFF but without the performance penalties of a DICE flip-flop.
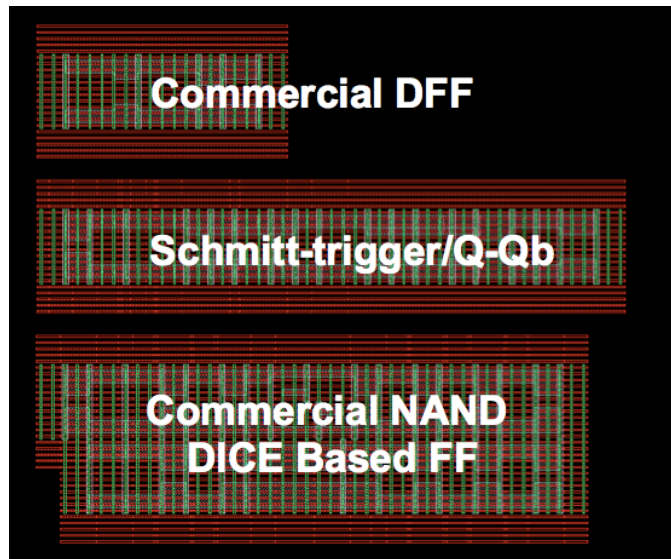

Figure 50: Layout view of the three flip-flops designed and fabricated on the 14/16nm test chip. The commercial DFF is unhardened and the STQQb and NAND DICE are radiation hardened designs.

The conventional DFF design consists of inverters, clocked inverters, and pass transistors in each latch as shown in Fig. 51. The DFF uses minimum sized inverters with 2-fin devices. The two hardened flip-flop designs are a Schmitt-trigger/Q-Qb flip-flop and a commercial NAND DICE based flip-flop. The schematics for the NAND DICE and STQQB are given in Figs. 52 and 53 respectively. The commercial NAND DICE design uses redundant nodes as the hardening technique. The latches, therefore, require a dual node strike for an upset to occur inside the latch. However, the NAND gates outside of the latches are vulnerable to a single strike as a generated transient may propagate from any of the gates and be captured in one of the latches. Fig. 53 explains the features of the STQQB flip-flop. The design is

a variation of the clocked inverter DFF design, where one of the inverters in each latch is replaced with a Schmitt-trigger inverter that is designed to filter fast transients. The STQQB design also uses the hardening technique of redundancy with a redundant connection between master and slave as well as a redundant connection between flip-flops from D to Q and Dbar to Qbar.
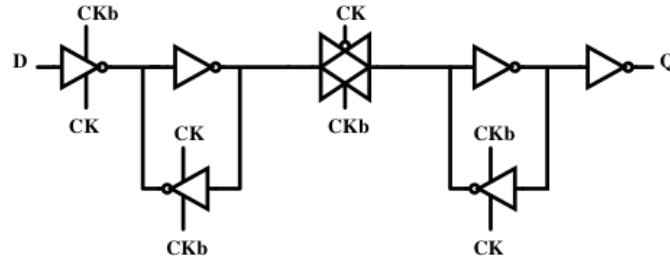

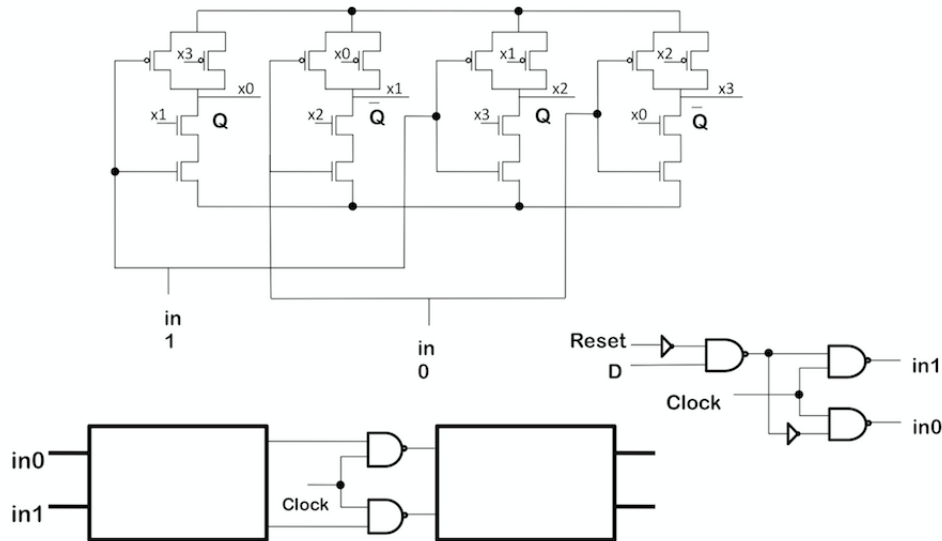Figure 51: Schematic representation of the DFF on the 14/16nm test chip.

Figure 52: Schematic representation of the commercial NAND DICE FF on the 14/16nm test chip. The master and slave latches are shown at the top of the figure with two outputs labeled Q and two labeled Qbar. The bottom left portion of the figure has two boxes representing the master and slave latches and reveals how the latches are connected. The bottom right portion of the figure gives the logic implemented on the front end of the DICE FF.
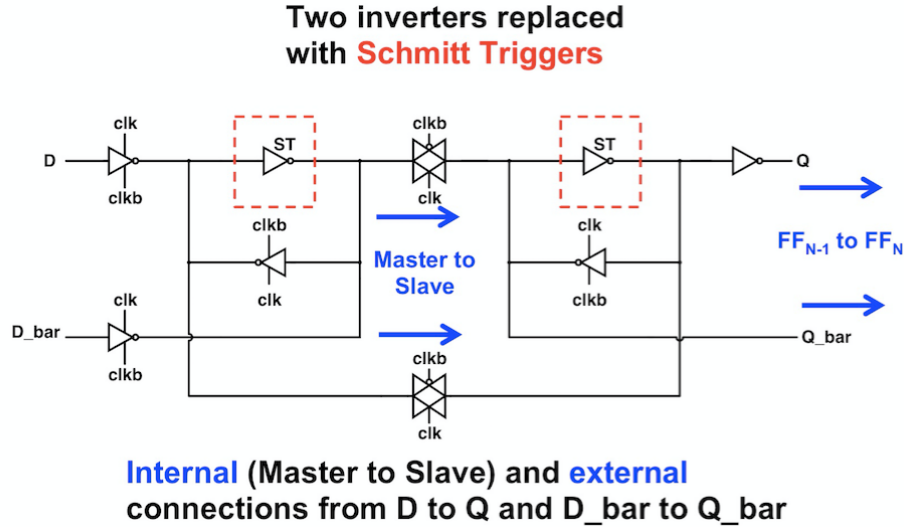
119

Figure 53: Schematic representation of the Schmitt-Trigger/Q-Qb flip-flop on the 14/16nm test chip.

Experimental Conditions and Results

Heavy-ion experiments were conducted on the 14/16nm single-event test chip at Lawrence Berkley National Laboratory (LBNL) using the 10 MeV/amu cocktail. All experiments were performed at normal incidence, at room temperature, and in vacuum. The test chip was irradiated using heavy ions ranging from LET= 0.9 to 59 MeV-cm2/mg. Tests for each of these ions were conducted at supply voltages including the nominal supply voltage of 0.8 V, 0.72 V, 0.65 V, 0.6 V, 0.55 V, 0.5 V and 0.45 V. Tests were performed using an 'All-0'or 'All-1'data pattern and at a 200 kHz clock frequency. The heavy ion test matrix of LET, bias, and angle of incidence is shown in Table 9.

LET and bias variation on the heavy-ion single-event response of the DFF are shown in Fig. 54. The response to LET variation is expected compared to previous technology data. However, the response to changing bias prompted further investigation into the relationship between critical charge and sensitive area which both vary with changes in bias which is presented in Chapter III.

Table 9: Experimental Parameters included in Testing of 14/16nm SET and SEU circuits.

Parameter	# of Variants	Values
LET (MeV-cm^2/mg)	12	0.89, 1.19, 2.19, 3.49, 4.56, 6.09, 9.74, 14.59, 21.17, 30.86, 48.15, 58.78
V$_{DD}$ (V)	7	0.8, 0.72, 0.65, 0.6, 0.55, 0.5, 0.45
Tilt Angle (°)	10	0(normal), 10, 20, 30, 40, 50, 60, 70, 80, 85
Roll Angle (°)	3	0, 90, 45
Test Chip #	6	0(normal), A14, B14, C14, D14, F14, G14
Data Pattern	2	'all 0' , 'all 1'
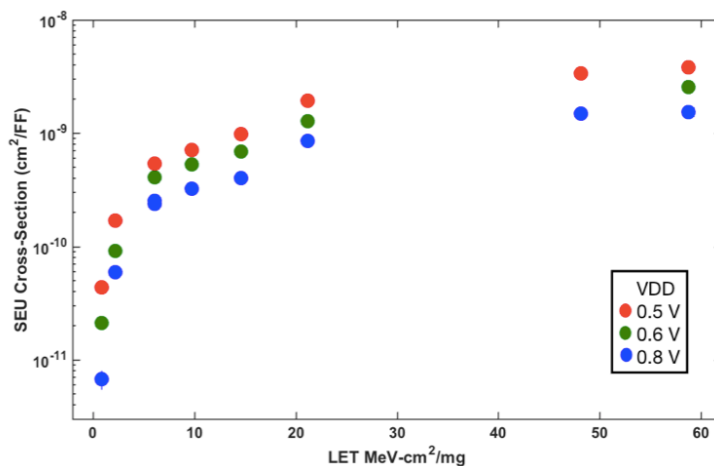
Figure 54: Experimental heavy-ion data for a DFF in 14/16nm bulk FinFET technology. Results shown are SEU cross-section vs. LET for three different circuit biases.

One of the most valuable features of the 14/16nm test chip is the ability to test for single-event transients and upsets at reduced bias operation. Fig. 55 shows the single-event upset cross-section for each of the three flip-flop designs at each of the biases tested from nominal 0.8 V down to 0.45 V.

The three flip-flops were tested with solid input patterns of 0 and 1. The SEU cross-section results are compared in Fig. 56, which shows similar results for cross-section for both data patterns.

Several different die were used to gather all of the 14/16nm heavy-ion data presented. To ensure the precision in the data set, SEU cross-section was plotted for 5 different LETs and 4 different test chips in order to evaluate any die-to-die variation. Fig. 57 shows the results of this comparison, which gives credibility to the data set because the measured cross-sections are consistent across the die tested.

Fig. 58 shows the response of all three flip-flop chains to isotropic Am-241 button source alpha particles over bias with an 'All-0'data pattern. The increase in SEU cross-section with reduced bias is apparent particularly for the hardened designs, which show no upsets with alpha particles until the 0.5 V bias irradiation. Note that the STQQb flip-flop was not functional at 0.45 V bias.

Alpha particle experiments were also conducted at Vanderbilt using the Americium-241 button source and the Pelletron, which both emit alpha particles of approximately 0.5 MeV-cm^2/mg LET. For the button source, irradiation is isotropic and the data was taken by placing the button source on top of the test chip. In the Pelletron, data was taken at several angles of incidence and biases to elucidate the angular effects of radiation on the single-event test structures. Fig. 59 shows the DFF SEU cross-section over tilt angle for nominal voltage down to 0.4 V bias. The change in cross-section with tilt angle is the discussion
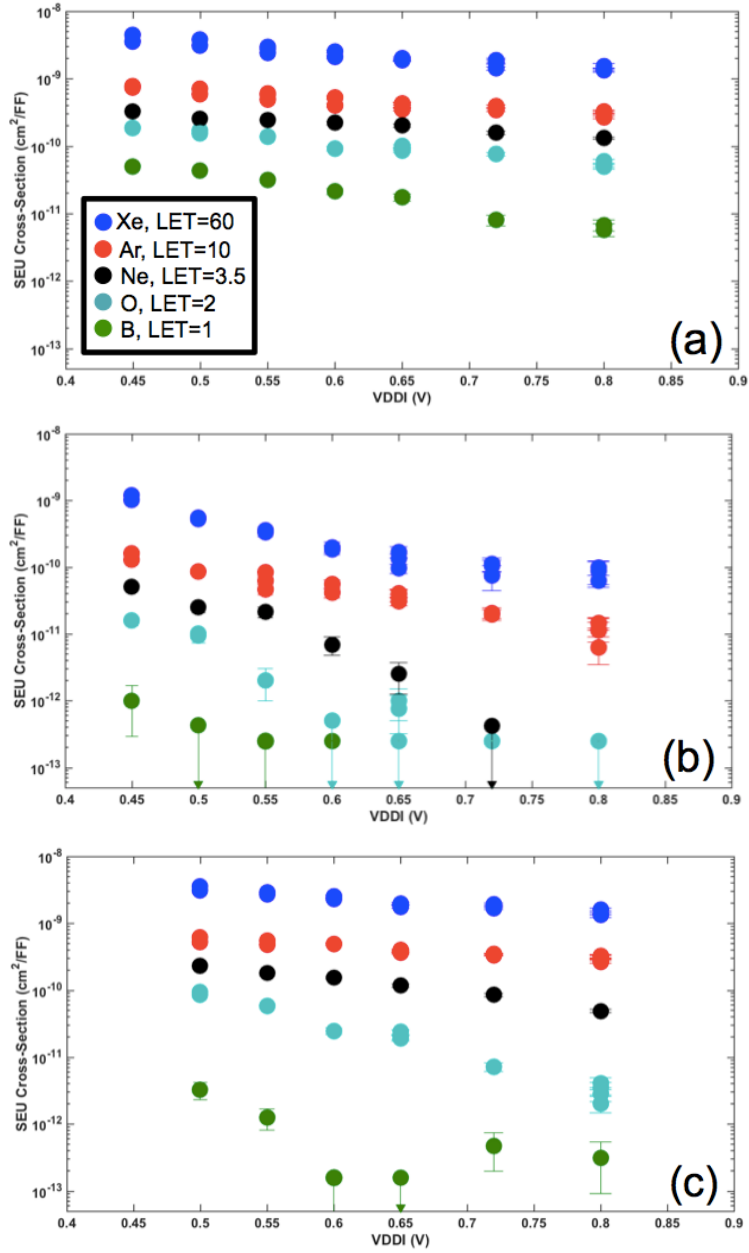
Figure 55: Experimental heavy-ion data for (a) DFF (b) NAND DICE and (c) STQQB flip-flops in 14/16nm bulk FinFET technology. Results shown are SEU cross-section vs. bias.
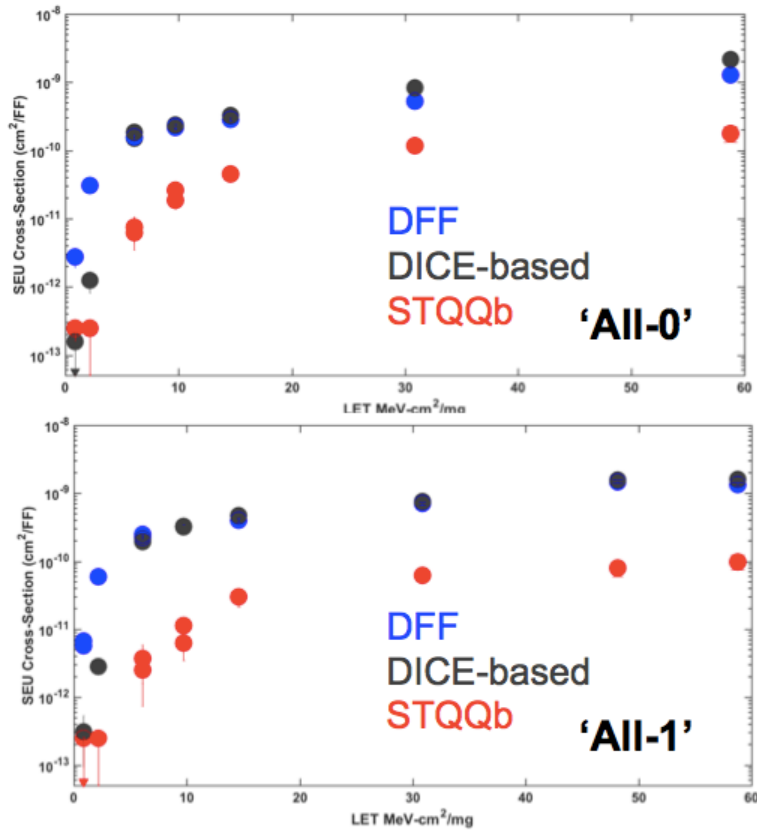
Figure 56: Experimental SEU cross-section for the three flip-flops included on the 14/16nm bulk FinFET test chip over LET for input data patterns of 'All-0'and 'All-1'.Results shown are for nominal 0.8 V bias.
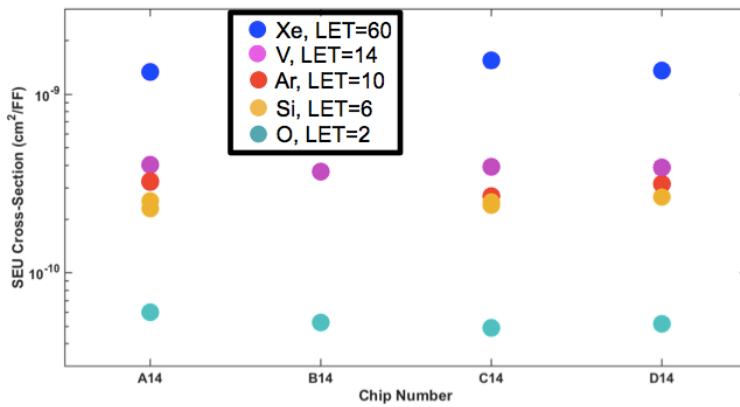

Figure 57: 14/16nm DFF SEU cross-section for four different die using the 'All-1' data pattern and 0.65 V bias.
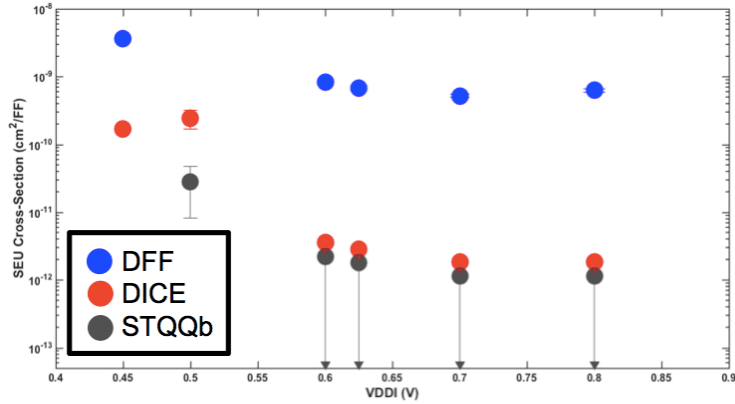
124

Figure 58: Isotropic alpha particle irradiation SEU cross-section over bias for the 3 flip-flop chains on the 14/16nm bulk FinFET test chip.

of Nsengiyumva's dissertation and is dependent on the FinFET device structure [81]. The Pelletron alpha particle data is compared with heavy ion irradiation data in Fig. 60. Figs. 61 and 62 show SEU Pelletron alpha irradiation data for the NAND DICE and STQQb hardened designs respectively.
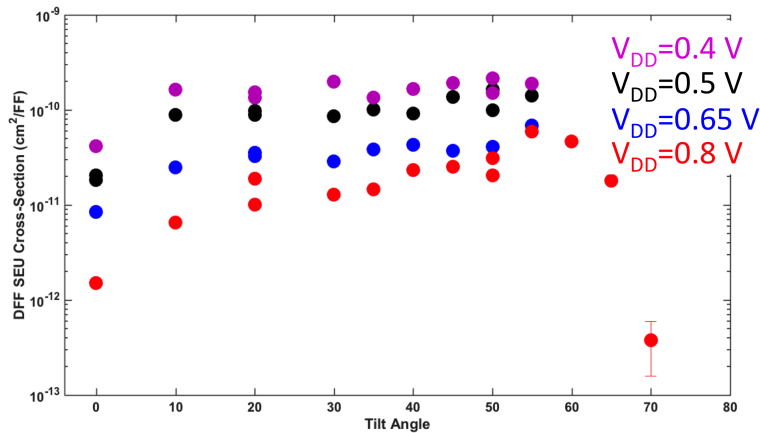

Figure 59: Pelletron alpha particle irradiation SEU cross-section over tilt angle and variation in bias for the DFF 14/16nm bulk FinFET test chip. The decreasing SEU cross-section above 55°at nominal bias is seen due to the alpha particle range.

Data for the 14/16nm DFF over angle was the topic of Nsengiyumva's PhD work. The data as well as an explanation of the data in relation to FinFET structure can be found in his dissertation [81].
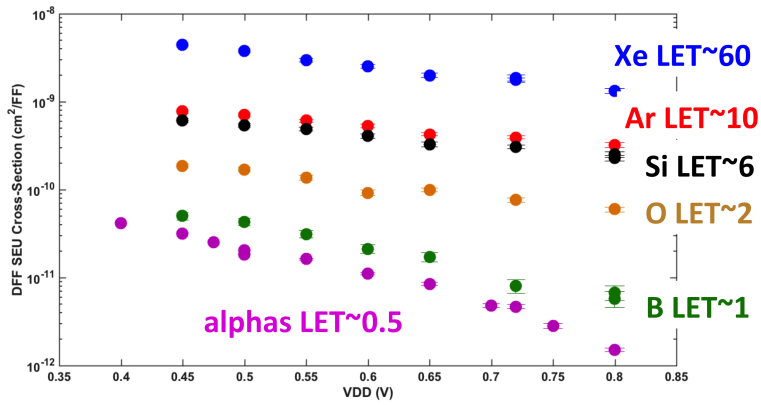
Figure 60: Pelletron alpha particle irradiation SEU cross-section compared with heavy-ion particle irradiation at nominal 0.8 V bias for the DFF 14/16nm bulk FinFET test chip.
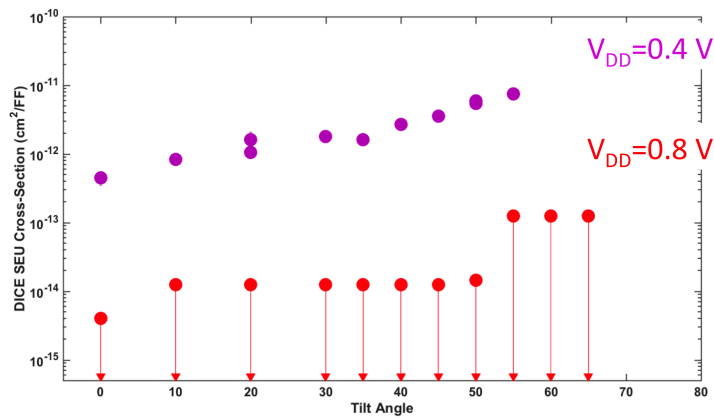

Figure 61: Pelletron alpha particle irradiation SEU cross-section over tilt angle and variation in bias for the NAND DICE FF 14/16nm bulk FinFET test chip.
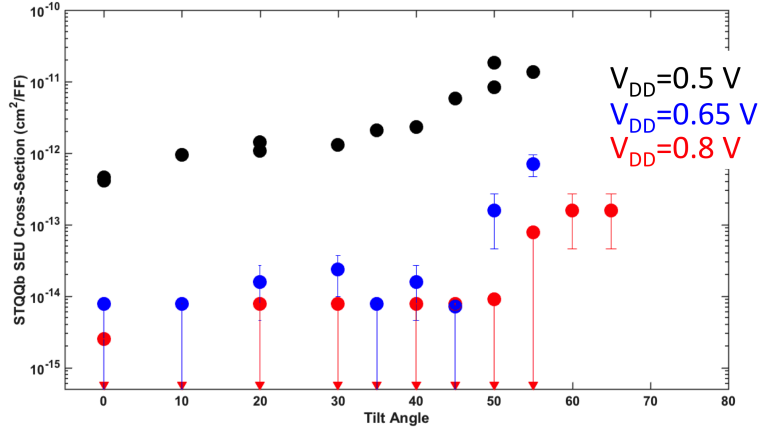
Figure 62: Pelletron alpha particle irradiation SEU cross-section over tilt angle and variation in bias for the STQQb hardened flip-flop design on the 14/16nm bulk FinFET test chip.

While the majority of the single-event transient data for the 14/16nm test chip can be found in [59], the following data give an overview of the SET data collected and utilized throughout this work. Shown in Fig. 63 is SET cross-section for a 3-fin regular threshold voltage inverter over LET compared with TCAD simulations.
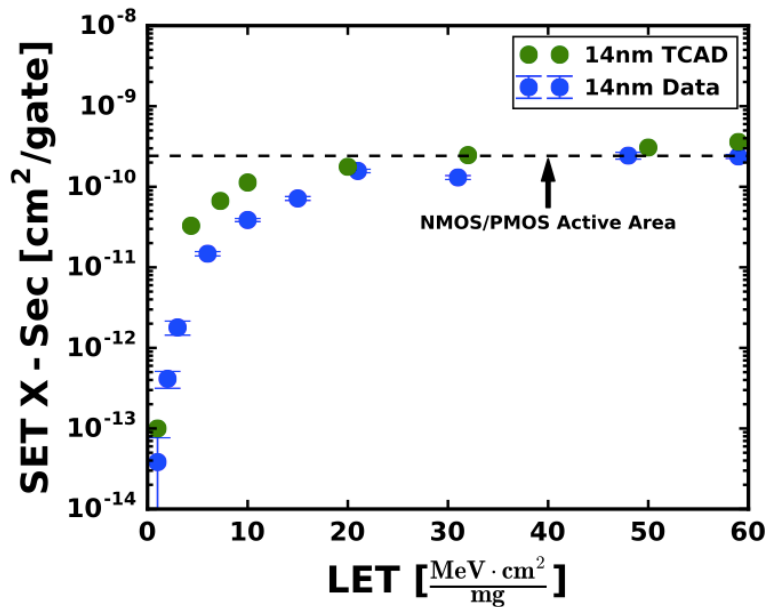

Figure 63: 14/16nm bulk FinFET 3-fin RVT inverter chain SET cross-section vs. LET at nominal voltage compared with TCAD simulations.

A broad perspective of SET variation with changing bias is given in Fig. 64 where the

captured transients for all logic circuits are shown for four different biases at an LET of 21 MeV-cm^2/mg. The plot reveals the general trend of increased transient pulse width with decreasing circuit bias. Fig. 65 shows the bias variation effect on one 3-fin RVT inverter
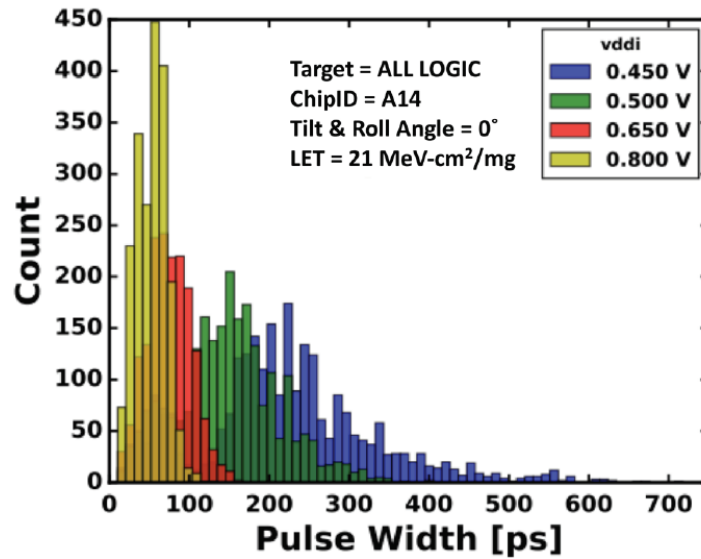

Figure 64: The distribution of SET pulse widths over all logic types across multiple bias levels at normal incidence irradiation with an LET of 21 MeV-cm^2/mg. Distributions have not been normalized to fluence.

chain. A significant increase in both transient pulse width and cross-section is seen with reduced bias.

32nm Planar SOI Single-Event Data

Test Chip Design

The 32nm SOI test chip was designed to extract single-event upset data from chains of flip-flops and logic cells. The output of each flip-flop chain was connected to a novel error detection circuit. The error detection circuitry was designed to compare the last four stored
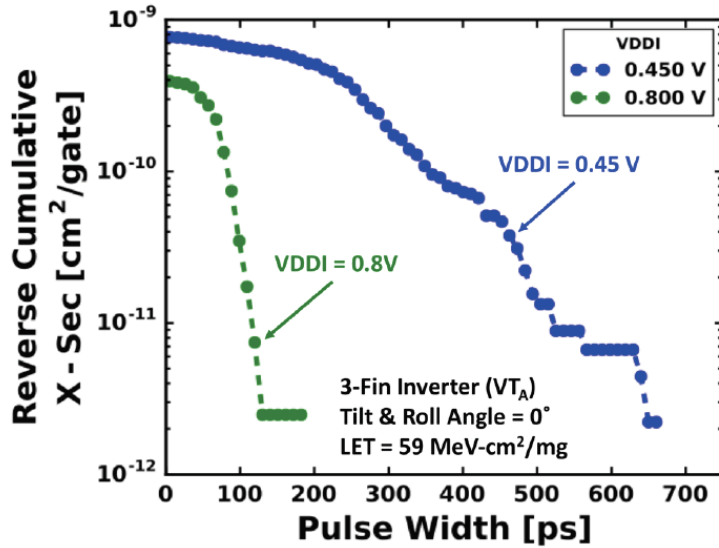
Figure 65: A reverse cumulative cross-section plot for SET pulse widths generated by the 3-Fin inverter target using the RVT threshold voltage transistors for normal incidence irradiation with an LET of 59 MeVcm^2/mg at two different variable V_{DD} levels.

flip-flop bits in the chains to determine whether or not an error occurred. Fig. 66 shows the error detection circuitry schematic [15].
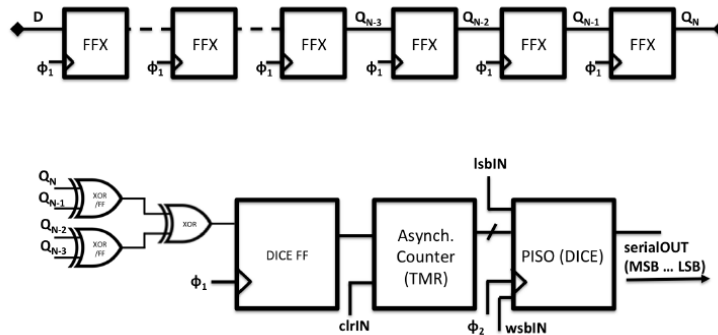
Figure 66: The novel error detection circuitry for the 32nm test chip. A detailed explanation of how the circuitry works is given in [15].

The logic chains were designed with combinational logic between hardened flip-flops. A separate chain of only the hardened flip-flops was tested and showed no upsets. Therefore, all of the upsets captured in the combinational logic are determined to be from the combinational logic itself, and not from the flip-flops. An on-chip voltage controlled oscillator allowed for

single-event testing of the structures at high frequencies of operation.

The 32nm test chip included several hardened and unhardened flip-flop and combinational logic designs. The flip-flops included a standard unhardened transmission gate D flip-flop, traditional DICE FF, stacked transmission gate DFF, and five variations of the LEAP RHBD FF [82]. The combinational logic chains on the test chip included an adder, XOR gates, decoders, and a voter.

Experimental Conditions and Results

Some of the experimental results shown here were included in the radiation effects data workshop (REDW) paper "Heavy-Ion SEU Test Data for 32nm Flip-Flops" [83].

Heavy ion experiments were performed at LBNL using the 4.5, 10, and 16 MeV/amu cocktails for particles of LET between 2.5 and 40 MeV-cm^2/mg. The test chips were irradiated over roll and tilt angles, including very high tilt angle irradiation between 80 and 88 degrees. The on-chip VCO allowed the test chips to operate up to 2.5 GHz and data were also taken at 1.5 GHz, 1 GHz, and 30 kHz.

Fig. 67 shows the good agreement between all of the different energy beam tunes by comparing all of the data taken at normal incidence and 30 kHz frequency for the standard DFF. Experimental SEU cross-section vs. LET results for DFF TG, DICE hardened, and stacked hardened flip-flops on the 32nm test chip are shown in Fig. 68. Experiments were performed at normal incidence and an 'all-0' input data pattern. The SEU cross-section for RHBD designs increases with increasing frequency. Fig. 69 shows the experimental SEU cross-section vs. tilt angle results for hardened and unhardened flip-flops on the 32nm test chip. Experiments were performed for 'all- 0' input data pattern over a variety of tilt angles. The plots show that the hardened designs have sensitivity to radiation only at very high

130

tilt angles. In alignment with previous work, the combinational logic chains on the test chip showed an increase in SE cross-section with increasing frequency. Data for three of the combinational logic blocks is given in Fig. 70, showing this trend.
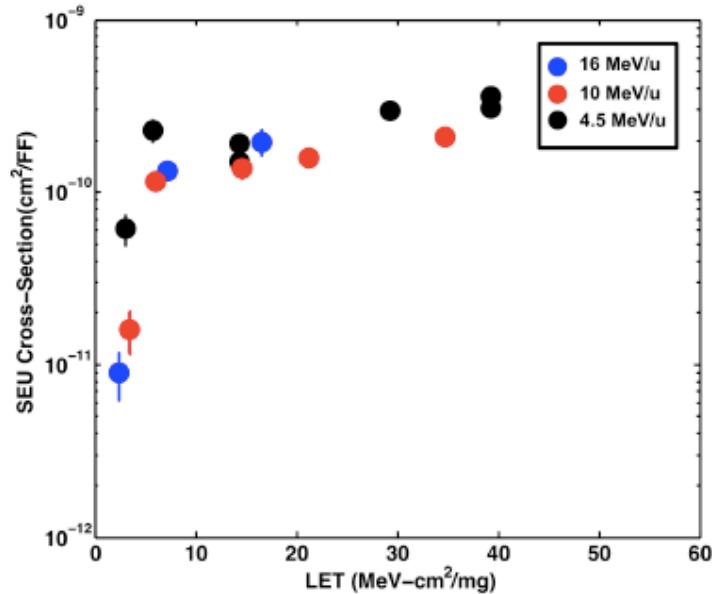

Figure 67: SEU cross-section curve for 32nm DFF for 3 different beam tunes at LBNL.

Conclusions

Extensive data sets for single-event transients and upsets have been taken for 32nm planar SOI and 14/16nm bulk FinFET technologies. Hardened and unhardened flip-flops on the 14/16nm test chip were irradiated with alpha particles and heavy-ions. Experiments were performed over a wide range of circuit bias, particle LET, and angle of incidence. Single-event upsets were measured from flip-flops and combinational logic chains on the 32nm SOI test chip over bias, frequency, and angle of incidence. Results from the irradiation experiments are the subject of this dissertation and several other dissertations and published journal papers as mentioned.
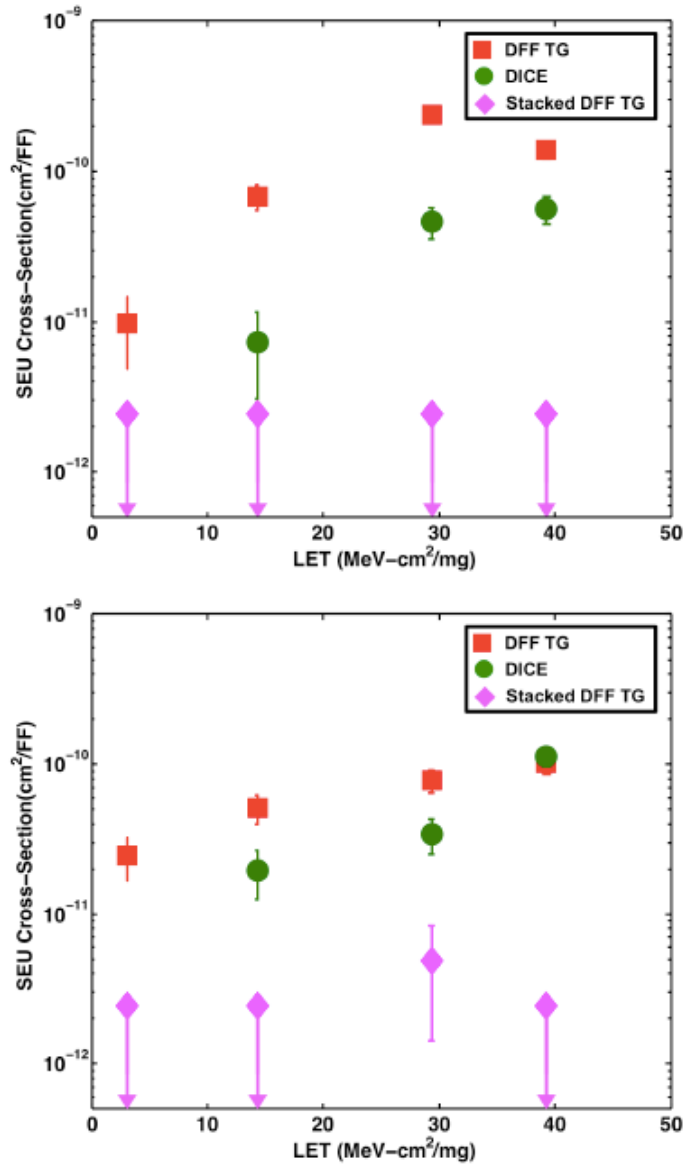
Figure 68: SEU cross-section plots that represent different clock frequency experiments (top-1.5 GHz,bottom- 2.5 GHz) performed for three different flip-flops on the 32nm test chip.
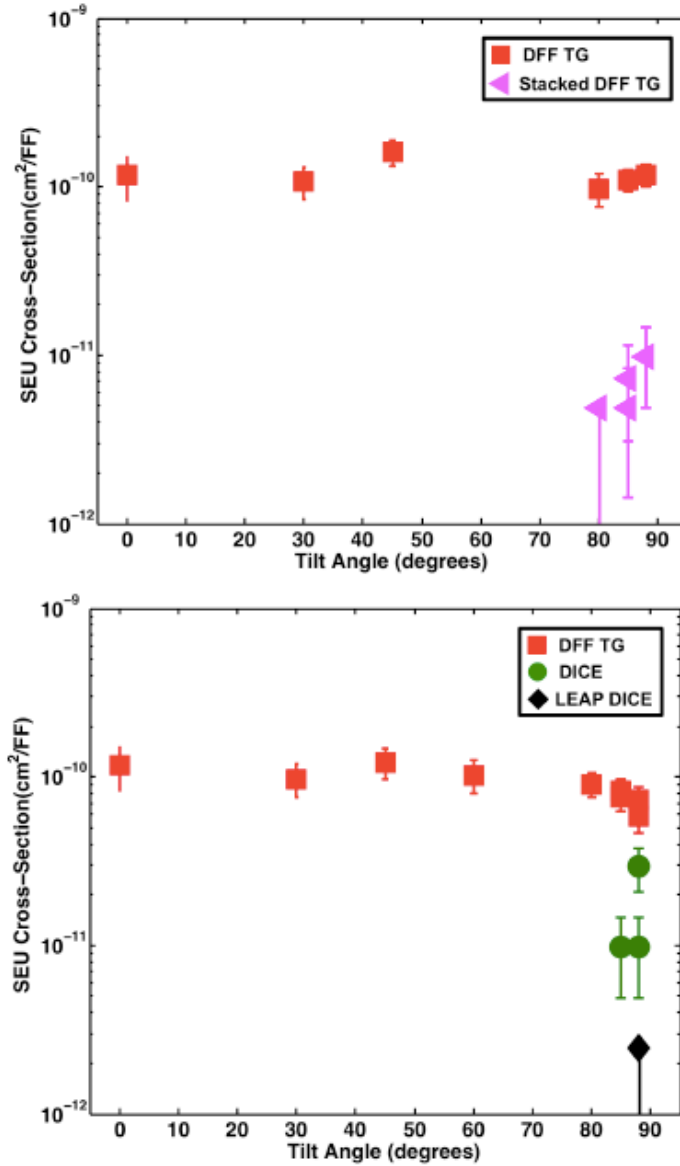
Figure 69: SEU cross-section vs. tilt angle for 32nm FFs. The top plot shows data for a 0°roll angle where upsets were seen on the stacked DFF TG flip-flop at >80°tilt angles. Similarly, the bottom plot shows data for a 90°roll angle where upsets are seen on the DICE and LEAP DICE hardened flip-flops at >80°tilt angles.
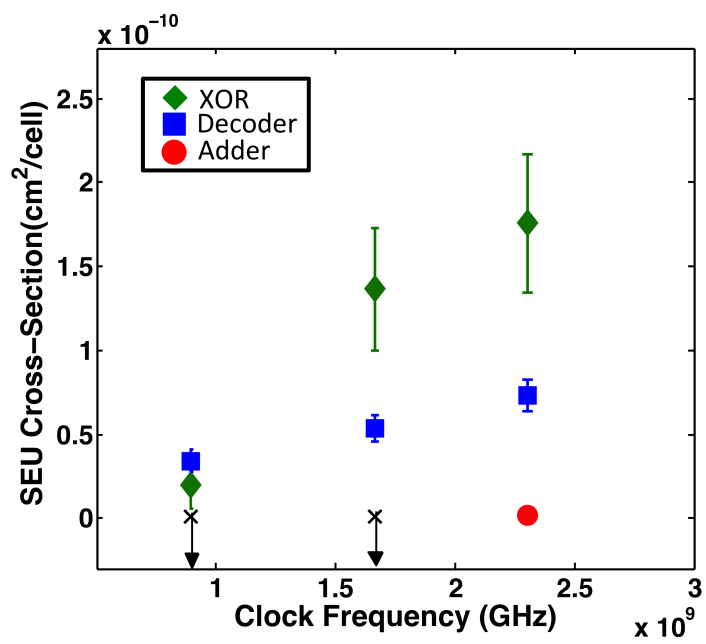
Figure 70: Normal incidence SEU cross-section vs. frequency for combinational logic chains with particle LET=6 MeV-cm^2/mg.

Appendix B

MODEL DERIVATIONS

Transient Latching Probability Equation Derivation

The following derivation is an expansion of the work in Chapter III. The transient latching

probability equation has been developed as the probability that a transient pulse of width t_{pw}

and setup-and-hold time window (t_{SH}) will intersect in a clock period (T). Fig. 71 illustrates

the transient pulse width, setup-and-hold time window, and clock period. This analysis

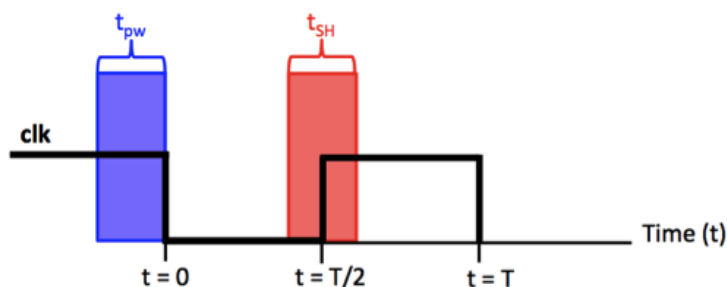assumes that the setup-and-hold time window is centered on the rising edge of the clock.

Figure 71: An illustration of the transient pulse width and setup-and-hold time window used
to calculate the probability that the two windows will intersect in the clock period (T).

Consider a transient pulse of a specific width (t_{pw}) and height as it moves in the period

with relation to the setup-and-hold window. First, consider the probability that the two

windows will not touch in the period (T). This is called the probability of a 'miss' (P_{miss})

and it will be broken down into two parts: (1) the transient pulse will not intersect the setup-

and-hold window on its left side (2) the transient pulse will not intersect the setup-and-hold

window on its right side. The limits of the analysis are considered from the moment the

leading edge of the transient pulse enters the period to the moment the trailing edge leaves

135

the period. The probability of a 'miss' is described by

$$P_{\text{miss}} = \frac{\int_{Fraction\ of\ a\ period\ to\ miss} transient\ pulse\ width\ pdf}{\int_{total\ period} transient\ pulse\ width\ pdf} \tag{29}$$

where the transient pulse width has a uniform probability distribution function (pdf). Each transient will have a different height (or in this case voltage) value associated with its pdf. Considering a single transient, its height is independent of time and will cancel in the numerator and denominator of 29 since it is a constant value over the given clock period.

Fig. 72 shows a miss on the left side (a) and right side (b) of the setup-and-hold time window. The total period for (29) is the clock period (T) + t_{pw}, since the trailing edge of the transient pulse is still touching the clock period when the leading edge is t_{pw} from the clock edge. Using (29) and the integration limits shown in Fig. 72,

$$P_{\text{miss,left}} = \frac{Fraction\ of\ period\ to\ miss\ left}{Total\ period} = \frac{\int_{0}^{\frac{T}{2} - \frac{t_{\text{SH}}}{2}} dt}{T + t_{\text{pw}}} \tag{30}$$

$$P_{\text{miss,right}} = \frac{Fraction\ of\ period\ to\ miss\ right}{Total\ period} = \frac{\int_{\frac{T}{2} + \frac{t_{\text{SH}}}{2} + t_{\text{pw}}}^{T + t_{\text{pw}}} dt}{T + t_{\text{pw}}} \tag{31}$$

The probability that the transient pulse and setup-and-hold window touch will be called an ' error ' (P_{error}). Therefore, $P_{\text{miss}} + P_{\text{error}} = 1$. The resulting probability equation,

$$P_{\text{error}} = 1 - (P_{\text{miss,left}} + P_{\text{miss,right}}) = \frac{t_{\text{pw}} + t_{\text{SH}}}{T + t_{\text{pw}}} \tag{32}$$

is a function of pulse width (t_{pw}), setup-and-hold time (t_{SH}) and clock period (T). This model accounts for the probability that a pulse width of any size can cause an error and does not assume that a transient pulse is much shorter than the clock period.
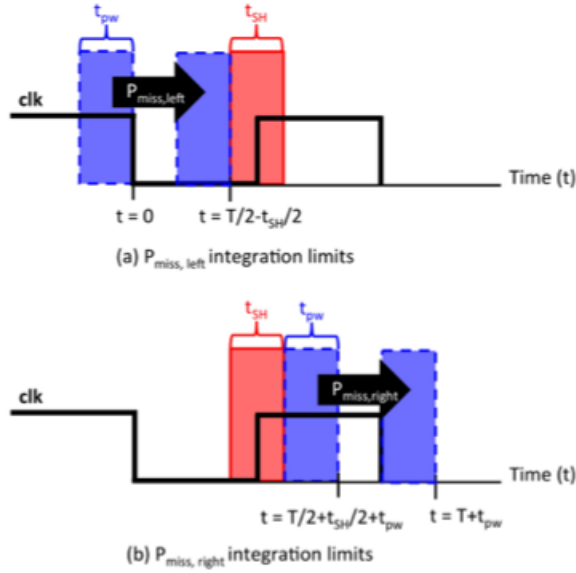
Figure 72: Shows the limits of integration for calculating the probability that the transient pulse will not intersect the setup-and-hold time window from (a) the left side and (b) the right side.

Analytical SEU Model Derivation

The full mathematical derivation of the analytical SEU model in Chapter III is presented here. The single-event current is a variation of the error function current presented in [10], simplified so that the equations containing the current pulse representation can be solved analytically.

$$I_{SE} = I_n(erf(\sqrt{(t/\tau_b)}) - erf(\sqrt{(t/\tau_a)}))$$

$$I_n = \frac{Q}{t_D + 0.5(\tau_a - \tau_b)}$$

(33)

A single-event current waveform with charge Q_{test} is assumed. In order to find the minimum charge of the SE waveform that will cause an upset, begin with a small value for Q_{test} and iteratively increase the charge until the equations derived in this section reveal that an upset has occurred.

137

Weak Coupling

Fig. 73 shows the SRAM in the weak coupling state, immediately following the single-event particle strike.
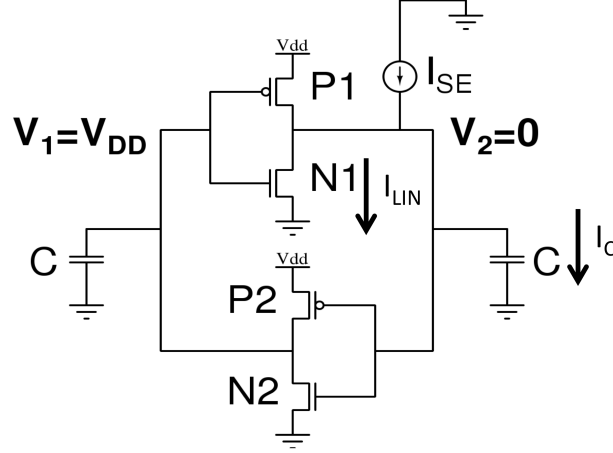

Figure 73: SRAM in weak coupling mode with the currents labeled that are used to derive an equation for the changing node voltage V_2.

First, to determine whether or not the node voltage V_2 will reach V_{thn}, Kirchhoff's current law (KCL) equations are written at node V_2 in 73. V_1 remains at V_{DD} while the SRAM is in weak coupling mode. Equation 34 is solved for V_2 with the initial conditions t=0 and $V_2(0)$=0. In this solution, τ_b is assumed to be much smaller than τ_a, therefore the error function term with τ_b approaches unity.

$$I_C + I_{LIN} = I_{SE}C\frac{dV_2}{dt} + \frac{V_2}{R_n} = I_{SE}\frac{dV_2}{dt} = -\frac{V_2}{CR_n} + \frac{I_{SE}}{C} \tag{34}$$

$$V_2 = \frac{QR_n}{t_D + 0.5(\tau_a - \tau_b))}(1 - e^{-t/R_nC} - erf(\sqrt{t/\tau_a} + \frac{Y}{X}e^{-t/R_nC}erf(\frac{X}{Y}\sqrt{t/\tau_a})))$$
$$where \ \ X = \sqrt{CR_n - \tau_a} \quad Y = \sqrt{C}\sqrt{R_n} \tag{35}$$

138

Equation (35) can then be differentiated and set equal to zero in order to calculate t_{v2m}, the time that V_2 reaches its maximum value due to the single-event current input.

$$t_{v2m} = \frac{CR_n\tau_a erfinv(\frac{X}{Y})^2}{CR_n - \tau_a} \tag{36}$$

Now, having found the time that V_2 reaches its maximum value, $t=t_{v2m}$ and $V_2=V_{thn}$ can be substituted in (35). These boundary conditions represent the case where the single-event deposits just enough charge to cause V_2 to increase to V_{thn}, the boundary for weak coupling and strong feedback modes, before decreasing back to its original value of zero. This equation can be solved for Q, where Q is the minimum amount of charge deposited that sends the SRAM into strong feedback mode- Q_{wc}.

$$Q_{wc} = \frac{V_{thn}(t_D + 0.5(\tau_a - \tau_b))}{R_n(1 - e^{-t_{v2m}/R_nC} - erf(\sqrt{t_{v2m}/\tau_a} + \frac{Y}{X}e^{-t_{v2m}/R_nC}erf(\frac{X}{Y}\sqrt{t_{v2m}/\tau_a})))} \tag{37}$$

If the single-event total deposited charge Q_{test} is greater than or equal to Q_{wc}, the analysis continues to strong feedback mode.

Strong Feedback

Once it is determined that the SRAM will enter strong feedback mode, the time at which the SRAM transitions between weak coupling and strong feedback mode must be found. For this portion of the analysis, (34) is solved again for V_2 and the initial conditions $t=0$ and $V_2(0)=0$. This time the solution will not assume τ_b approaches zero.

$$V_2 = \frac{QR_n}{t_D + 0.5(\tau_a - \tau_b)}(W + \frac{Y}{X}e^{-t/CR_n}erf(\frac{X}{Y}\sqrt{t/\tau_a} - \frac{Y}{Z}e^{-t/CR_n}erf(\frac{Z}{Y}$$
$$\sqrt{t/\tau_b})))\text{where } Z = \sqrt{CR_n - \tau_b} \quad W = erf(\sqrt{t/\tau_b}) - erf(\sqrt{t/\tau_a}) \tag{38}$$

Next, the time at which V_2 in (38) reaches V_{thn}, the boundary between the modes of operation, is found. However, time cannot be explicitly solved for in (38) because it is a transcendental equation. Therefore, a linear expansion is performed around an estimate of the time when the SRAM switches modes of operation. The estimate for the time is given by a square pulse single-event current approximation $T_{wc}{}^{ini}$ in [9].

$$T_{wc}^{ini} = -R_n C ln(1 - V_{thn}/(I_n R_n)) \tag{39}$$

Equation (10) is used to perform a linear expansion of (38). The boundary condition is then applied as $V_2 = V_{thn}$ and the equation is solved for T_{wc}, the time that represents the boundary between weak coupling and strong feedback mode.

$$T_{wc} = XZ\sqrt{C}e^{T_{wc}^{ini}}(V_{thn}(0.5(\tau_b - \tau_a) - t_D) - QR_n(erf(\sqrt{T_{wc}^{ini}/\tau_a}) + erf(\sqrt{T_{wc}^{ini}/\tau_a})))$$
$$+ Q\sqrt{R_n}(CR_n + T_{wc}^{ini})(Zerf(\frac{X}{Y}\sqrt{T_{wc}^{ini}/\tau_a}) - Xerf(\frac{Z}{Y}\sqrt{T_{wc}^{ini}/\tau_b})) \tag{40}$$

Moving into strong feedback mode, the transistors in the SRAM have changed state. Fig. 74 shows the transistor currents in strong feedback mode. As in weak coupling mode, KCL equations at each of the nodes can be written to describe the change in node voltage over time based on the transistor states and single-event current input.

$$I_{C1} - I_{SAT2} = 0$$
$$C_1 \frac{dV_1}{dt} - g_{mn}(V_2 - V_{thn}) = 0 \tag{41}$$
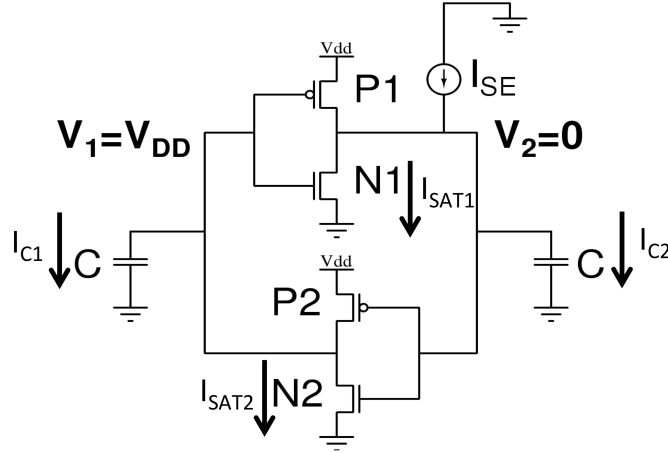$$\frac{dV_1}{dt} = -\frac{g_{mn}V_2}{C} + \frac{g_{mn}V_{thn}}{C}$$

Figure 74: SRAM in strong feedback mode with the currents labeled that are used to derive an equation for the changing node voltages V_1 and V_2. The KCL equations for these nodes result in cross-coupled equations, where V_1 is a function of V_2 and V_2 is a function of V_1.

$$I_{C2} + I_{SAT1} = I_{SE}$$

$$C_2 \frac{dV_2}{dt} + g_{mn}(V_1 - V_{thn}) = I_{SE} \tag{42}$$

$$\frac{dV_2}{dt} = -\frac{g_{mn}V_1}{C} + \frac{g_{mn}V_{thn}}{C} + \frac{I_{SE}}{C}$$

In order to determine whether or not the single-event current will cause an upset, return to the definition of an upset, which is when V_1 is equal to V_2. A single-event current of the form (33) with charge greater than or equal to Q_{upset} will cause V_1 and V_2 to be equal at some point in time. Next, solve for Q_{upset}, the minimum charge associated with the waveform (33) that will cause an upset.

Subtract the differential equation dV_2/dt from dV_1/dt in (41) and (42) respectively and apply the transformation $u(t)=V_1-V_2$.

$$\frac{du}{dt} = \frac{g_{mn}u}{C} - \frac{I_{SE}}{C} \tag{43}$$

141

Next, (43) can be integrated from time t=T_{wc} to t=infinity. Setting this equation equal to zero and solving for Q gives Q_{upset}.

$$Q_{upset} = Ce^{-g_{mn}T_{wc}/C}(V_{DD} - V_{thn})(t_D + 0.5(\tau_a - \tau_b))/(1/g_{mn}C(-e^{-((g_{mn}T_{wc})/C)}$$

$$erf(\sqrt{T_{wc}/\tau_a}) + e^{-((g_{mn}T_{wc})/C)}erf(\sqrt{T_{wc}/\tau_b}) + (-1 + erf(\sqrt{(T_{wc}(g_{mn} + C/\tau_a))/C})) \quad (44)$$

$$\sqrt{C/(C + g_{mn}\tau_a)} - (-1 + erf(\sqrt{(T_{wc}(g_{mn} + C/\tau_b))/C}))\sqrt{C/(C + g_{mn}\tau_b)))$$

If Q_{test} is greater than or equal to Q_{upset}, an upset will occur in the SRAM with the single-event current waveform of the form (33).

Appendix C

ANALYTICAL MODEL CODE

The following Matlab scripts were developed to implement the analytical SEU model described in Chapter III. The first script was developed to find the single-event current waveform that will cause an upset in an SRAM by iteratively increasing the amount of charge in the waveform until the SRAM shows an upset. The process by which it is determined whether or not an upset has occurred is explained in Chapter III. The second script may be used after the first in order to plot the node voltages V_1 and V_2 with the single-event current waveform that will cause an upset.

Matlab Script to Find Q_{upset}

%Single-event current pulse parameters from the ISDE bias dependent model [10]

```
taua=5e-12; %seconds

taub=55e-15; %seconds

td=3*taub; %seconds
```

%Technology parameters (found running simulations in the PDK using SPICE)

```
Rn=[44000 52428 72192 130901]; %Ohms

C=0.6e-15; %Farads

Vthn=0.381; %Volts

VDD=[0.8 0.7 0.6 0.5]; %Volts

gmn=[374e-6 363e-6 302e-6 186e-6]; %Siemens
```

%Initial Charge to begin iterations to find Q_{upset}

Q(1)=0.01e-15;

%Define constants used in the model equations

X=sqrt(C*Rn(i)-taua);

Y=sqrt(C)*sqrt(Rn(i));

Z=sqrt(C*Rn(i)-taub);

%This loop determines the minimum charge Qupset for a single-event with an error

function current waveform as described in [10]

for i=1:4

for j=1:100000

In=Q(j)/(td+0.5*(taua-taub));

tv2m=(C*Rn(i)*taua*erfinv(X/Y)^2)/(C*Rn(i)-taua)

Qwc=(Vthn*(td+0.5*(taua-taub))/Rn(i))*

(1/(1-exp(-tv2m/(Rn(i)*C))-erf(sqrt(tv2m/taua))

+(Y/X)*exp(-tv2m/(Rn(i)*C))*erf((X/Y)*sqrt(tv2m/taua))));

if Q(j)>Qwc

Twini(i)=-Rn(i).*C*log(1-Vthn./(In*Rn(i)));

Twc(i)=(-sqrt(C)*exp(Twini(i)/(Rn(i)*C))*Q(j)*Rn(i)*X*Z*

erf(sqrt(Twini(i)/taua))+Q(j)*sqrt(Rn(i))*Z*(C*Rn(i)+Twini(i))

*erf((X/Y)*sqrt(Twini(i)/taua))+X*(sqrt(C)*exp(Twini(i)/(Rn(i)*C))

Z(0.5*(taub-taua)-td)*Vthn+sqrt(C)*exp(Twini(i)/(Rn(i)*C))*Q(j)

*Rn(i)*Z*erf(sqrt(Twini(i)/taub))-Q(j)*sqrt(Rn(i))*(C*Rn(i)+Twini(i))

*erf((Z/Y)*sqrt(Twini(i)/taub))))/(Q(j)*sqrt(Rn(i))*(Z*erf((X/Y)

*sqrt(Twini(i)/taua))-X*erf((Z/Y)*sqrt(Twini(i)/taub))));

Qupset(i)=C*exp(-gmn(i)*Twc(i)/C)*(VDD(i)-Vthn)

144

```
*(td+0.5*(taua-taub))/(1/gmn(i) *C *(-exp(-((gmn(i)* Twc(i))/C))

* erf(sqrt(Twc(i)/taua))+exp(-((gmn(i)* Twc(i))/C))

* erf(sqrt(Twc(i)/taub))+(-1+erf(sqrt((Twc(i)* (gmn(i)+C/taua))/C)))

* sqrt(C/(C+gmn(i)* taua))-(-1+erf(sqrt((Twc(i)

* (gmn(i)+C/taub))/C))) *sqrt(C/(C+gmn(i)* taub)))));
        if Q(j)≥Qupset(i) && isreal(Qupset(i))==1 && Qupset(i)>0
            fprintf('Q=%2.3f fC for VDD=%2.2f',Q(j)/1e-15,VDD(i))
            fprintf('Twc=%2.3f ps',Tw/1e-12)
            break
        else
            Q(j+1)=Q(j)+0.0001e-15;
        end
    else
        Q(j+1)=Q(j)+0.0001e-15;
    end
end
```

<u>Matlab Script to Plot V_1 and V_2 Over Time</u>

Once the previous script is used to find Q_{upset}, the following script can be used to visualize the voltages V_1 and V_2 as they change over time in response to the single-event current that will upset the SRAM.

```
%Single-event current pulse parameters from the ISDE bias dependent model [10]
        taua=5e-12; %seconds
```

taub=55e-15; %seconds

td=3*taub; %seconds

%Technology parameters (found running simulations in the PDK using SPICE)

Rn=44000; %Ohms

C=0.6e-15; %Farads

Vthn=0.381; %Volts

VDD=0.8; %Volts

gmn=374e-6; %Siemens

%Parameters T_{wc} and Q_{upset} from the previous script

Q=1.122e-15;

Twc=7.66e-13;

%Define constants used in the model equations

X=sqrt(C*Rn(i)-taua);

Y=sqrt(C)*sqrt(Rn(i));

Z=sqrt(C*Rn(i)-taub);

%Set the initial conditions for V_1 and V_2 and an initial time to begin calculating the node voltages

V2(1)=0;

V1(1)=VDD;

t(1)=1e-13;

%Define the maximum single-event current In=Q/(td+0.5*(taua-taub));

%Run the loop to calculate V_1 and V_2 for each time step

for i=2:100 %Number of time steps to plot

146

```
    t(i)=t(i-1)+1e-13;

        if V2(i-1)≤Vth%Weak coupling mode

            V2(i)=(Q*Rn/(td+k*(taua-taub)))*(1-exp(-t(i-1)/(Rn*Cn))

            -erf(sqrt(t(i-1)/taua))+(Y/X)*exp(-t(i-1)/(Rn*Cn))*erf((X/Y)

            *sqrt(t(i-1)/taua)));

            V1(i)=VDD;

        else%Strong feedback mode

            syms v1(x) v2(x)

            inoise=In*(erf(sqrt(x/taub))-erf(sqrt(x/taua)));

            ode1=diff(v1)==(-gmn/Cn)*v2+(gmn/Cn)*Vth;

            ode2=diff(v2)==(-gmn/Cn)*v1+(gmn/Cn)*Vth+inoise/Cn;

            cond1=v1(Twc)==VDD;

            cond2=v2(Twc)==Vth;

            odes=[ode1;ode2];

            conds=[cond1;cond2];

            [v1(x),v2(x)]=dsolve(odes,conds);

            V1(i)=subs(v1(x),x,t(i));

            V2(i)=subs(v2(x),x,t(i));

        end

end

plot(V2)

hold on

plot(V1)
```