Single-Event Hardened Analog / Mixed-Signal Circuit Layouts Utilizing Node Splitting with Directional Temporal Filtering

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Chapter 1

Introduction

As device sizes scale and yet faster IC processes are developed, there is a tendency for a digital-centric mindset to emerge among engineers. The purported death of analog is no doubt a comforting thought to many circuit designers frustrated by advanced analog design concepts. Digital design is, after all, cleaner than analog design, at least at a cursory glance. However, a closer inspection reveals that the digital realm is simply a discrete framing of an inherently continuous system. Moreover, any practical application will require interaction with the physical world, which is also analog. Thus, to escape analog entirely one must remain in the realm of theory, and any talk of analog being a bygone technology is wishful thinking. Given the inescapable nature of analog components, they continue to be relevant for even the most cutting edge of processes. Their inclusion and the inherent shrinking for advancing technologies (reduction in nodal capacitance, quiescent current, etc.), leads to an increasing vulnerability (as is also the case with digital circuits) to the effects of ionizing radiation.

Since the onset of the first ASET induced malfunction, concern for the effects of ionizing radiation on electrical circuits has only continued to grow [17]. It was once assumed that as devices scaled down, radiation effects would become less of a concern. And indeed, the effects of total ionizing dose have improved dramatically as device sizes have decreased. However, shrinking device sizes saw an improvement in TID performance but a greatly increased sensitivity to single event effects (SEEs). SEEs usually manifest in digital circuits as a bit flip (Single Event Upset) or a single event fault interrupt (SEFI) which can lead to a prohibitively large number of bit errors. Because a digital error can be readily identified, hardening of soft errors in digital circuits is far easier than in the case of analog. Appropriate error-correction code is often enough to harden a circuit if the error rate

is sufficiently low. For analog signals, however, there is no way of discerning between a transient produced by a single event strike and the actual signal.

The most efficient (in terms of cost) methods of hardening analog circuits against the effects of ionizing radiation usually fall under the category of radiation-hardened by design (RHBD) techniques. This work takes one such technique, node splitting, and shows some additional configurations for it that can be applied to analog and mixed-signal (A/MS) designs. The original conception for this work was an idea called Smart Peeling, an application of the concept of node splitting for RHBD circuits. Smart Peeling was conceived as an RHBD technique that would leverage normal NMOS/PMOS behavior with respect to a changing voltage at the devices source/drain in order to achieve cutoff along the path of an erroneous transient signal, thus mitigating its magnitude at the output. In conjunction with this blocking mechanism, the critical signal path is split into two paths, so that if one path is struck the other path is able to maintain the correct signal at the output. In the course of the research, it was found that combining node splitting with an additional new technique called Directional Temporal Filtering (DTF), produced the most effective single-event transient mitigation.

Freedom from reliance on external circuits to help with the hardening is one of the chief advantages of node splitting combined with DTF. Introducing additional peripheral circuitry also introduces additional potential targets for SEE strikes, and care has to be taken that the hardening introduced by the peripheral circuitry outweighs the increased sensitive area. Node splitting combined with DTF achieves significantly improved transient mitigation along internal paths compared to unhardened layouts, but at very minimal design cost. This internal transient mitigation translates to lower current shoot-through along the power rails of the circuit, since the transient is mitigated at internal nodes rather than the output. Node splitting with DTF has thus far been verified only in simulation. Test circuits for a few key analog building blocks were designed in 180nm, 32nm SOI, and 45nm SOI. The circuits radiation responses were simulated using a bias dependent SET model calibrated

for 90nm.

1.1 Thesis Organization

This work presents the background information necessary to understand and implement the Smart Peeling RHBD technique in a selection of fundamental A/MS circuits.

Chapter II covers background information on single event effects, primarily single event transients, as well as motivation for this research.

Chapter III covers the general idea behind Radiation Hardening by Design (RHBD) techniques and background material related to the modeling and simulation of SEEs in circuits. Additionally, previous hardening techniques that proceeded this research are discussed.

Chapter IV introduces the node splitting with DTF concept. The operation of the examined circuits is discussed, and simulation results are shown for the new RHBD layouts on these circuits. Circuits examined are: Fully Differential Op Amp, Differential Input, Simple Bootstrap Current Reference, Simple Bias Voltage Reference, Cascode Current Sink, Regulated Cascode Current Mirror, and Single Ended Op-Amp. Chapter V is a summary of the results of this dissertation.

Chapter 2

Radiation Effects

The effects of ionizing radiation continue to be a cause for concern within the field of analog and mixed signal circuit design, especially for devices operating in high altitude or space environments. In order to properly harden a circuit or system against radiation, it is necessary for a designer to have a firm grasp of the principle mechanisms behind radiation induced errors. This chapter will give a short overview of general radiation effects, followed by a more in depth look at single event effects. The mechanisms behind charge generation and deposition will be examined for SEEs. Of particular relevance is Analog Single Event Transients (ASETs). Although the mechanisms behind ASET generation do not differ from SET mechanisms in digital circuits, ASET hardening techniques are significantly different from digital hardening techniques given that analog signals are continuous, and it is thus impossible to disentangle an erroneous signal from a correct signal.

2.1 Single Event Mechanisms

As mentioned before, a single event effect occurs when a single particle strikes a device, depositing some charge. The particles that most typically result in upsets are heavy ions (Z $\geq$ 2), alpha particles, and protons [26]. As the particle begins to travel through the silicon it will deposit some of its energy along the way. The particle does not deposit its energy uniformly as it traverses the material and in fact it deposits the majority of its energy right before stopping. This peaking of energy deposition is known as the Bragg Peak, pictured in Figure II-1.

The depth that a particle is able to penetrate is known as its range. A common unit for characterizing striking particles is Linear Energy Transfer (LET), in units of $MeV - cm^2/mg$. LET is defined as the energy loss per unit path length, normalized by the density

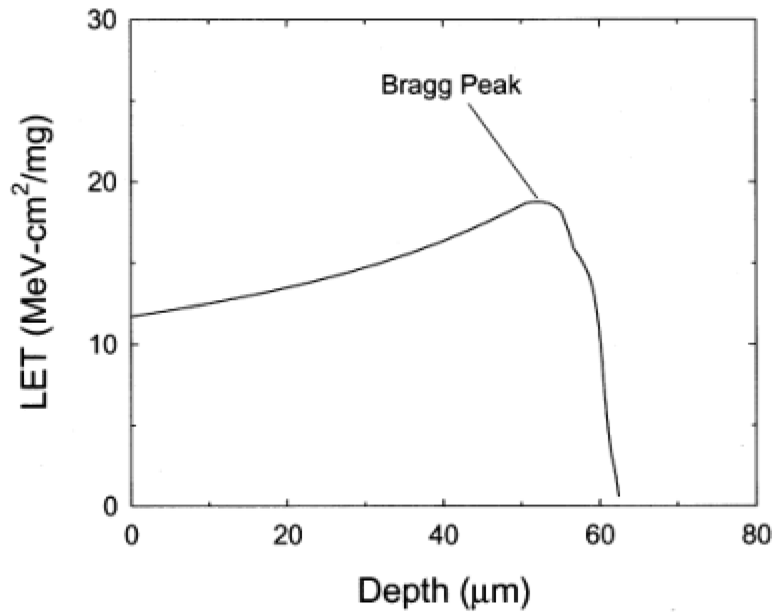


Figure 2.1: Illustration of Bragg Peak [4]

of the target material. Silicon requires a deposition of 3.6 eV to generate an electron-hole pair and has a density of 2328 mg/cm^3, so an LET of 97 deposits 1pC/um of charge. A ratio of 100:1 is often used to approximate this. Another useful rule of thumb is that the maximum LET of an ion is roughly equal to its atomic number Z. This deposited energy will result in a local departure from equilibrium and a resultant generation of electron hole pairs in the wake of the energetic particle [4,19].

There are two main ionization mechanisms for incident particles. The first, indirect ionization, occurs when a typically lower mass particle, such as a proton or neutron, strikes a particle within the devices material and causes a nuclear reaction with that particle. There are many types of nuclear reactions that can occur between particles. Inelastic collisions typically produce the aforementioned secondary particles. Elastic collusions can produce instead a recoil within the Silicon crystal, or alpha/gamma particle emission. Elastic collisions are more typical of lighter particles. The resultant particles from this reaction are typically much heavier than the original striking particle and are much more likely to cause

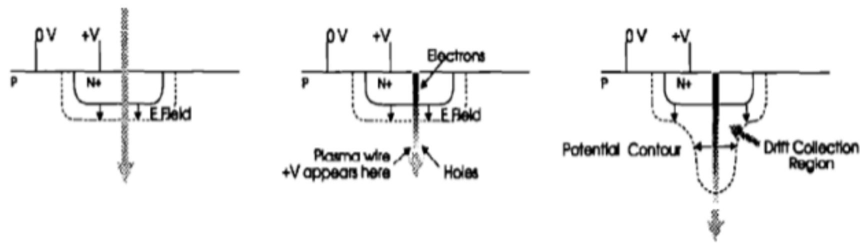


Figure 2.2: Depiction of funneling effect following an SE strike [4]

direct ionization within a circuit [2,18].

Direct Ionization usually causes relevant effects only with heavier particles (Z¿=2), however as device sizes get smaller, there has been some indication that direct ionization from high energy protons can result in upsets. The process occurs when a particle passes through a material (e.g. Silicon) and deposits energy along its path. The deposited energy results in an abundance of electron-hole pairs being generated along the path of the strike. After the strike has occurred, there are two main mechanisms by which the deposited charge can be collected and manifest as a current.

The first, drift current, occurs if the cloud of electron-hole pairs is within the vicinity of an electric field. For example, if the strike occurs at a PN junction, the inherent electric field at the junction will cause the electrons to get swept towards the n-region and the holes to get swept towards the p-region, resulting in a current spike at these nodes. Typically the portion of the transient due to drift current is relatively short, often on the order of pico-seconds. There is an additional effect that occurs along the particle track known as funneling that ends up exacerbating the severity of the drift current [4]. Funneling occurs when a particle strikes the depletion region of a device. The charge along the particle track causes the electric field present in the depletion region to extend further down along the track as pictured in Figure II-2. The result is that more carriers are able to be swept to the junction as a result of drift current.

The other mechanism for charge collection is diffusion. Diffusion current is a much

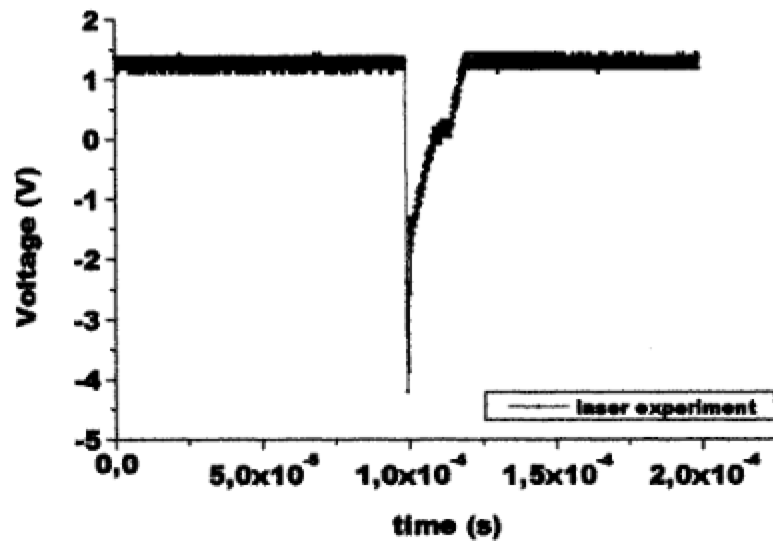


Figure 2.3: Example waveform resulting from SE strike [24]

slower process than drift current and so a substantial number of the electron-hole pairs are able to recombine before being collected at a node. As a result, the diffusion current tends to be much lower in magnitude than drift current, but longer in duration. The combination of the two mechanisms results in a typical transient shape such as the one pictured in Figure II-3.

2.2 Additional Effects

There is a common effect inherent to bulk silicon and exacerbated by SE strikes that we will consider known as the parasitic bipolar effect. A parasitic bipolar transistor naturally exists within a silicon MOS transistor, as depicted in Figure II-4. Normally the parasitic BJT is biased such that it is in cutoff, and its presence is not a huge concern. However, if the charge from an SE strike is able to raise the potential of the substrate, the source-base junction can become forward biased, and the parasitic BJT can leave cutoff and begin to induce a parasitic current across the devices source and drain. As a result, the amount of total charge collected following a strike can be greatly increased. This effect is most

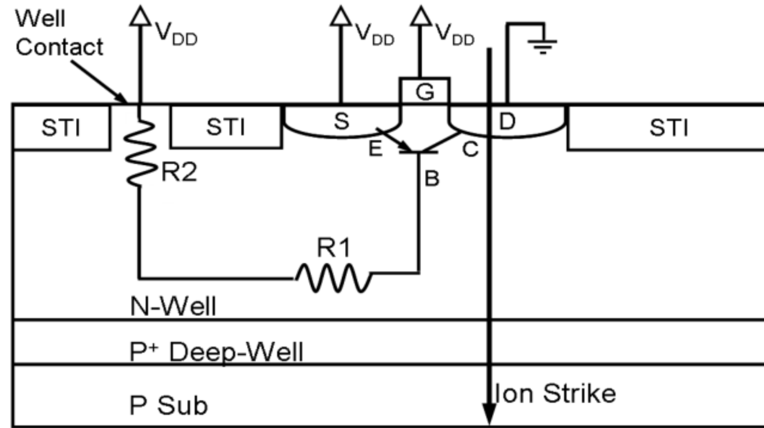


Figure 2.4: Illustration of parasitic BJT effect in bulk CMOS. [15]

common in PMOS devices due to their isolated n-well.

Lastly, we will consider an effect known as charge sharing. Technology advances and devices grow still smaller, but radiation does not feel obliged to follow this trend, and the size of striking particle tracks remains more or less the same. As a result, where once a strike might have concerned a single terminal of a device, in sub-micron technologies, a single strike can now potentially affect multiple devices adjacent to the struck device [15]. This phenomenon is pictured in Figure II-5. Charge sharing introduces multiple additional difficulties in SEE hardening, and absolutely cannot be ignored below 90nm processes. There are techniques for dealing with charge sharing that will be discussed a bit more later in this work, however an in-depth discussion of these techniques and their operation is beyond the scope of this paper. The interested reader can find a much more detailed discussion in ([3][7]).

2.3 SOI Considerations

Silicon on Insulator (SOI) devices have many advantages with regards to their radiation performance. SOI circuits consist of single-device silicon islands, that are dielectrically isolated from each other and from the underlying substrate. Figure II-6 provides an example illustration of a typical SOI device. The vertical isolation prevents the latch-up mechanism

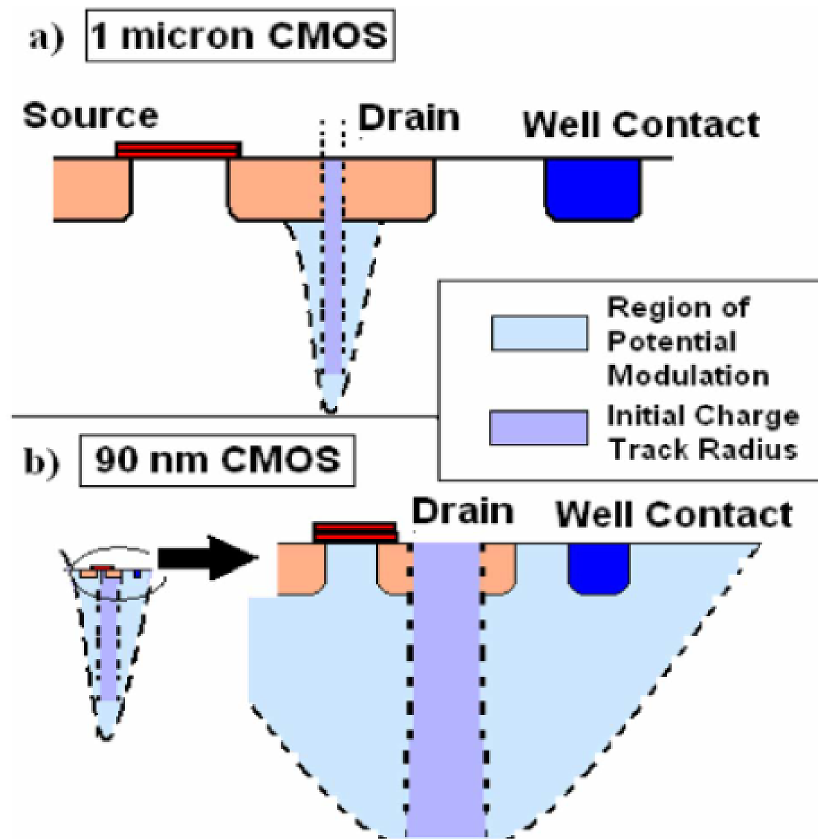


Figure 2.5: Illustration of charge-sharing phenomena as processes scale down in size. [15]

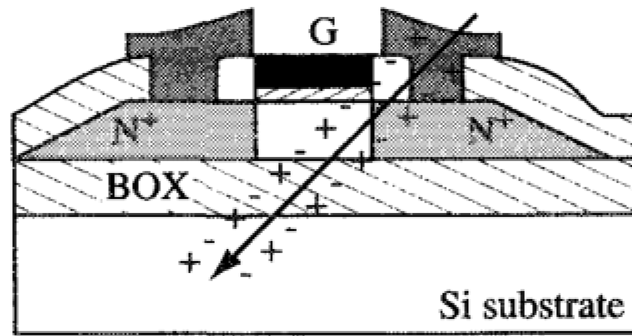


Figure 2.6: Typical SOI device configuration [14]

that exists in and can be a hindrance to bulk-Silicon. The source and drain regions extend down to the buried oxide (BOX) in order to minimize the junction surface [14].

SOI has numerous technological advantages stemming from its design, and in general tend to perform about 20-30% faster than bulk technology of the same generation. One might then be tempted to ask, Why not use SOI for everything?. And indeed, SOI does tend to see better performance with regards to transient radiation effects. However, SOIs radiation tolerance is limited by its vulnerabilities to total dose effects, which are beyond the scope of this paper. Additionally, the isolated well can lead to a build-up of charge in the well as a result of a strike that can potentially (heh) forward bias the source/base junction and lead to a parasitic bipolar effect. In some cases, snapback can occur, in which the device is not able to immediately return to its normal functioning state, and often must be power cycled. Snapback can result in damage to the device if the current from the parasitic effect is large enough. As a result, cross sections for SOI circuits are generally not orders of magnitude better than bulk processes [14, 13].

As mentioned before, charge sharing can be a large issue as processes scale below micron sizes. A few techniques actually take advantage of charge sharing in order to mitigate transients. However, because these techniques hinge on charge sharing effects being significantly large, they are not effective in a process such as SOI, which is largely immune to the

effects of charge sharing due to its isolated silicon island. We consider SOI in this section to give an example of a process where the peeling techniques presented herein might be advantageous, since they do not depend on charge sharing at all to function properly.

2.4 Single Event Effects

An SE strike can manifest itself in a circuit in a variety of ways. Errors that are permanent and destructive to the device are known as hard errors. Some examples include Single-event Burnout (SEB) and single event gate rupture (SEGR). Single Event Latch-up is sometimes considered a hard error, however it is not inherently a hard error. Latch-up can lead to destructively high currents through a device, but the latchup process itself is not necessarily destructive. Hardening against hard errors is beyond the scope of this paper.

Soft errors, on the other hand, are non-destructive errors that occur in a circuit usually in the form of corrupt data. A bit flip as the result of deposited charge is a common example known as a Single-Bit Upset (SBU). If multiple erroneous bits occur due to a single strike (for example as a result of charge sharing), this is known as a Multiple-Bit Upset (MBU). More problematic are Single Event Functional Interrupts (SEFIs), which can result in large amounts of bit errors as a result of, for example, a strike to the control circuitry of a memory that effects entire word lines. Often a system reset is necessary to recover from a SEFI. Soft errors in digital circuits can usually be dealt with by error correction code (ECC) if the error rate is low enough.

The situation is slightly different for analog circuits. Transients in a/ms circuits dont look any different than they do in digital circuits. The difficulty arises in how they are interpreted. Whereas digital circuits manifest errors as bit flips (that are detectable), there is no way for a circuit or code to examine an analog signal and discern erroneous transients from the original signal. In fact, analog signals are most often spotted downstream of the analog circuits in the digital portion of the circuit where they appear as a bit error. However, ASETs do not always create SEUs, and can often go undetected. A systems vulnerability to

ASETs is entirely dependent on the requisite functionality of the system. Because of this, and because of the lack of a universal hardening technique for ASETs, a circuit designer is encouraged to employ hardening techniques specific to the application of the circuit.

Chapter 3

RHBD Overview For A/MS Circuits

The demand for rad-hard electronics has shifted almost entirely to the military sector, and as such makes up a small percentage of the IC market. As a result, IC manufacturers have largely abandoned rad-hard processes in favor of the more lucrative commercial processes [13]. Given the cost associated with fabrication, someone looking to produce a rad-hard circuit is left with two options. Either use older (and significantly slower) rad hard processes or look towards employing radiation hardened by design (RHBD) techniques. RHBD techniques seek to use appropriate design choices and methodologies at the circuit level in order to make a circuit or system inherently tolerant to radiation, regardless of the process. Given that there are many ways in which a circuit might be vulnerable to single event effects, there is no universal optimal design methodology for RHBD. A designer should employ RHBD techniques on a case-by-case basis, and indeed methods that harden against one effect might in fact make the circuit more vulnerable to some other effect. For this reason, a thorough understanding of the application and the circuits sensitivity are required on the part of the designer. RHBD designs always involve some trade off in performance be it area, power, or bandwidth. In addition, a designer is far more limited in terms of the components available. For example, pinched resistors, diffusion resistors, MOS capacitors, surface Zener diodes, and lateral PNP transistors. The reason for this is that these devices are inherently vulnerable to radiation effects [13].

Current commercial processes consist almost entirely of Bulk CMOS or Silicon on Insulator (SOI). BiCMOS is still used though not as often. SOI provides some inherent hardness to single event effects, especially issues related to charge sharing in the smaller processes. However, functionally one only tends to see a 2-10x improvement in SER with SOI due to other vulnerabilities introduced. In general, when looking to harden electronics

against SEEs, one can employ either process modifications or schematic level techniques to inherently harden a mixed-signal circuit or system. Process modifications might include additional steps (masking and implant), which can be prohibitively expensive.

In general, RHBD techniques for SEEs rely on either filtering or dissipating the collected charge from a strike or providing a redundancy such that a single strike is not enough to produce an upset. The effects of charge sharing have made it more difficult to provide effective hardening through redundancy techniques, but have also given rise to new RHBD techniques that utilize charge sharing effects to mitigate transients. Operating frequency also plays a part in the sensitivity of mixed signal circuits to SEEs. As frequencies increase to the point where theyre on the same order as the time required to dissipate charge from an affected node, strikes can become far more disruptive.

Temporal filtering can be an effective method of hardening whereby a resistance and/or capacitance is added to a critical circuit node effectively creating a low-pass filter effect to fast single-event voltage pulses (Figure III-2). This has drawbacks at higher frequencies and introduces a speed penalty, and usually confers an upper limit of 2.5GHz on the maximum operating frequency of any individual signal path or data latch. Floating capacitor circuits are especially vulnerable as the entirety of a strikes charge can collect in the node and propagate through the rest of the circuit. Some circuit topologies are also inherently rad hard. For example, a sigma-delta Analog to Digital converter is resistant to SEEs in the analog front end due to the nature of data oversampling, which results in an SET getting converted into out-of-band noise. Global signals, such as clocks, bias voltages, and reference voltages, can create errors throughout the entire system and are especially critical. The majority of the circuits examined in this work will consist of global signal circuits.

For analog circuits, techniques are far more limited, primarily due to the lack of an analog voting circuit, such as the scheme presented in Figure III-1. Additionally, supposing there were an analog voting circuit, it would constitute a large additional of sensitive area. With RHBD techniques, when a designer is considering adding additional active area,

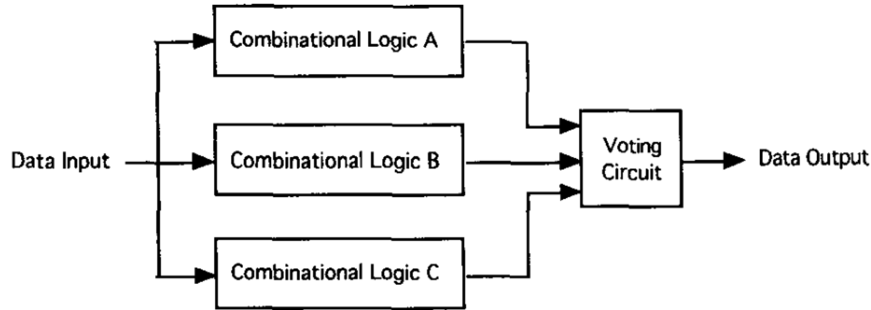


Figure 3.1: Typical Voting Circuit hardening scheme [13]

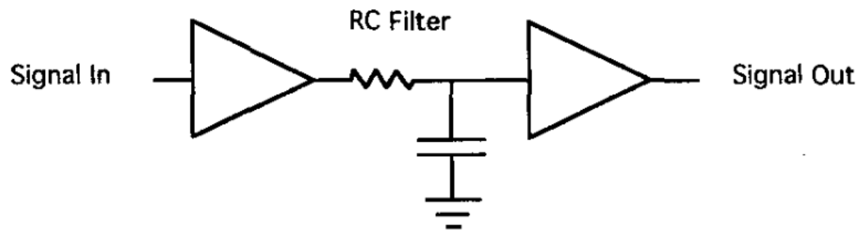


Figure 3.2: Temporal Filtering hardening scheme [13]

they must consider the vulnerability of each new node added and weigh its cost against the benefits of the hardening provided. For this reason, it is desirable especially for analog that RHBD techniques add as few additional devices as possible when hardening a circuit. A designer must carefully analyze a circuit and determine which nodes or signal paths are most vulnerable and selectively harden them, so as to minimize area, power, or speed penalties. Identifying a critical signal path often involves knowledge of what exists downstream of the signal. Input stages, for example, are very vulnerable, as any transient occurring at the input will be amplified alongside the regular signal at every other following stage.

Another limiting factor for analog hardening is short-channel effects, that dictate that most analog MOS transistors cannot take advantage of deep submicron gate lengths. Traditionally, a designer seeking to harden a purely analog circuit against SEEs was left with either charge dissipation or temporal filtering as practical options. However, a paper published in 2014 outlined two novel techniques. Hardening via node splitting and hardening

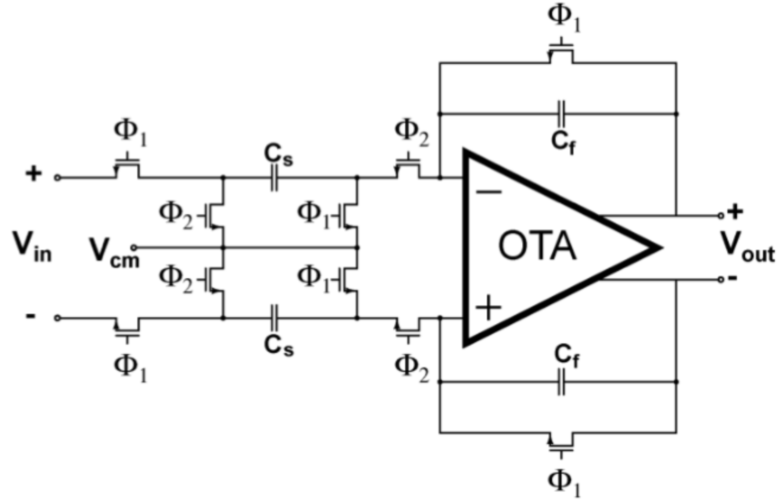


Figure 3.3: Original Switched Capacitor S/H Amplifier [8]

via charge sharing. This work concerns itself with additional node-splitting techniques, and as such hardening via charge sharing will not be discussed in any great detail. The interested reader can find out more in the cited papers over Direct Charge Cancellation and SNACC [22, 23].

3.1 Hardening Via Node Splitting

We will now examine a family of techniques known as Hardening Via Node Splitting, in which a designer creates multiple redundant signal paths within a circuit, such that if one is struck, the other paths will maintain signal integrity. Intuitively, for this to be most effective, the struck signal path needs to shut off so as to contain the erroneous transient. However, this cutoff behavior is not always achievable, especially within analog systems due to analog signals being continuous.

The first implementation of hardening via node splitting was a technique known as Dual Path Hardening. In this work, the author sought to harden a differential switched capacitor sample and hold amplifier against soft errors due to SETs. Given the nature of the floating nodes at the input, all of the erroneous charge deposited by an SEE will appear for an entire

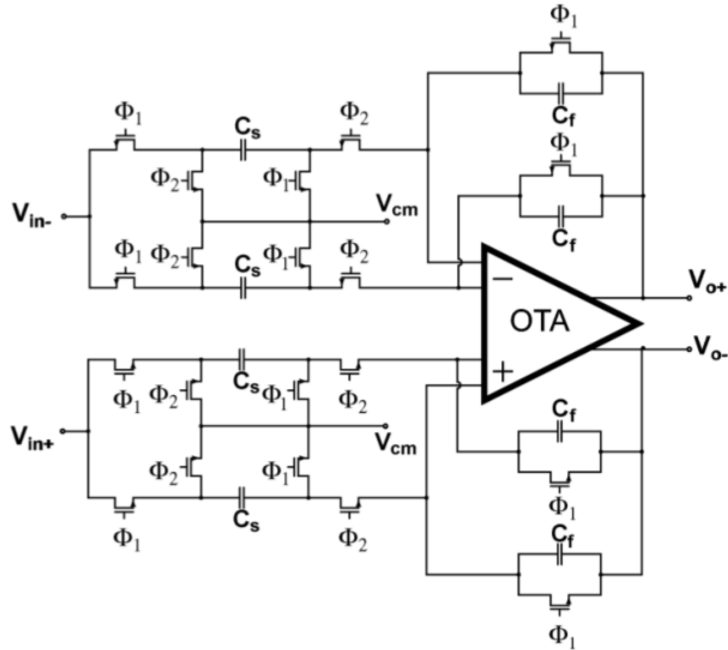


Figure 3.4: Switched Capacitor S/H Amplifier using node splitting [8]

clock cycle. Additionally, the floating nodes are upstream of the differential data path and so the erroneous charge gets amplified, as it is indistinguishable from a legitimate signal. Because of these factors, the floating nodes are very vulnerable parts of the circuit and were targeted for hardening. The capacitor and switching transistor paths were duplicated at half their original size so that the active area did not actually increase. This duplication provided two paths for the legitimate signal to travel along, the result being that, if one was struck, it would ideally shut off, and the other path would maintain the signals integrity. Charge sharing needs to be avoided for this technique to be effective.

The goal of this work is to examine the feasibility of peeling at a sub-circuit level. A more general hardening via node splitting technique was looked at in an earlier work that saw the entire analog circuit duplicated rather than a single sensitive node. This more blanketed brute-force approach to peeling is easier to implement but a circuit may not always be able to accommodate peeling, depending on device size limitations, and Gm penalties. If a designer wished for whatever reason to minimize the required peeling, the ability to

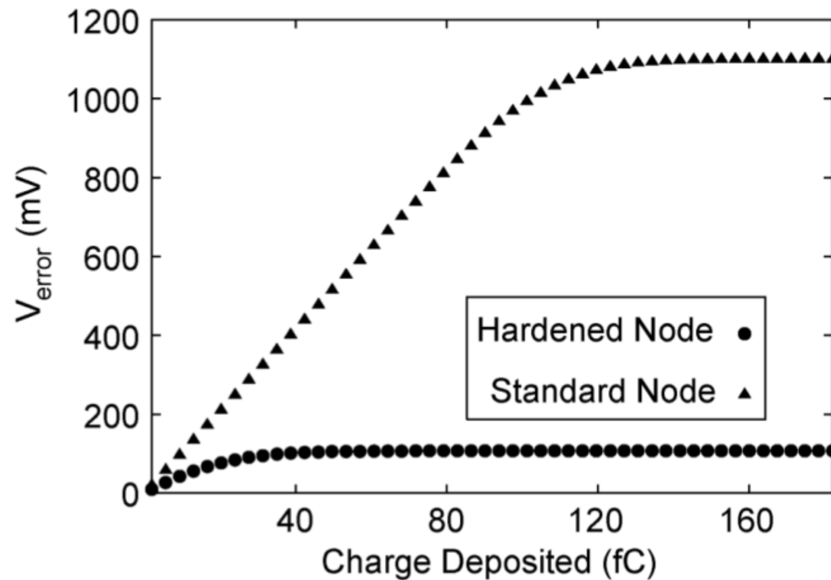


Figure 3.5: Simulation based results for dual-feedback hardening used in the Switch Capacitor Sample/Hold amplifier of Figure III-4 [8]

peel only sub-sections of a circuit while still achieving effective transient mitigation would be desirable. Input stages of a circuit, and bias circuits, are examples of especially critical sub-circuits that might be targeted for more selective peeling.

An important distinction must be made between peeling and other redundancy techniques. Peeling does not incur any additional active area. The paths are duplicated, but each duplicated path sees the active area halved. The result is the circuit providing the same performance at the summed output node, but with each peeled path carrying a smaller individual contribution to the whole output than the original unpeeled path. This can be thought of as essentially spreading out risk, analogous to diversifying ones stock portfolio. This concept was verified in 2014 when it was implemented on two different test chips designed for testing.

A 32nm SOI folded cascode op-amp described in Figure III-8 (c) was chosen as the main circuit to test this method. SOI was chosen due to its resistance to charge sharing effects. The peeled circuit showed a significant improvement on the order of 50% reduction

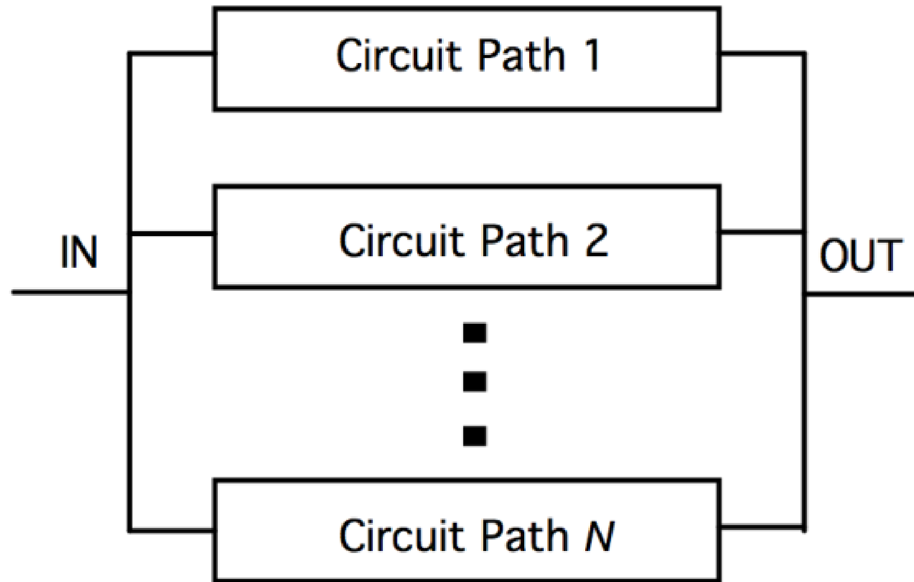


Figure 3.6: Illustration of the general concept of hardening via node splitting [16]

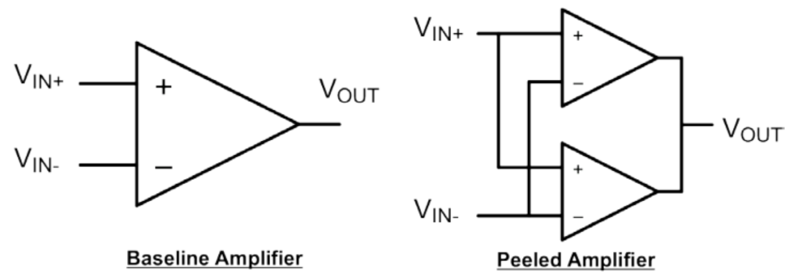
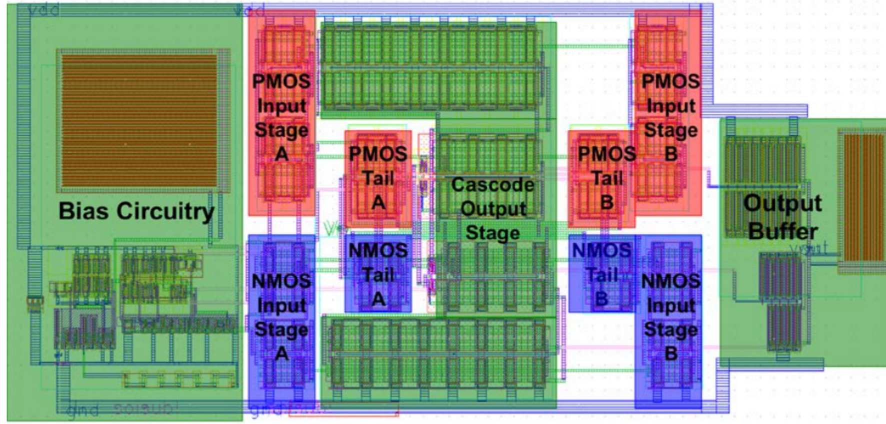
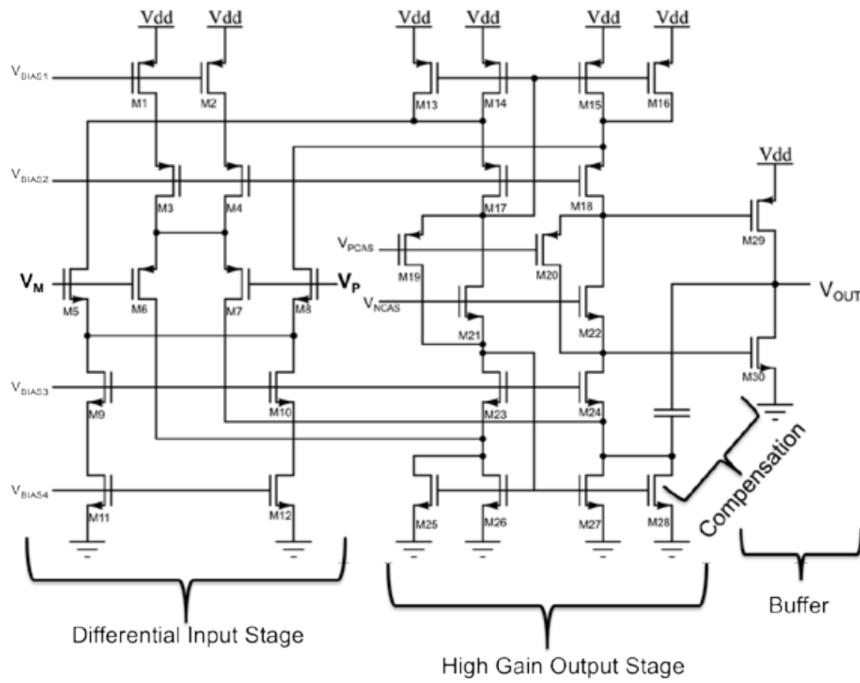


Figure 3.7: Example of what a peeled layout might look like for an op-amp. The input voltage feeds to both amplifiers, and their outputs are summed [16]

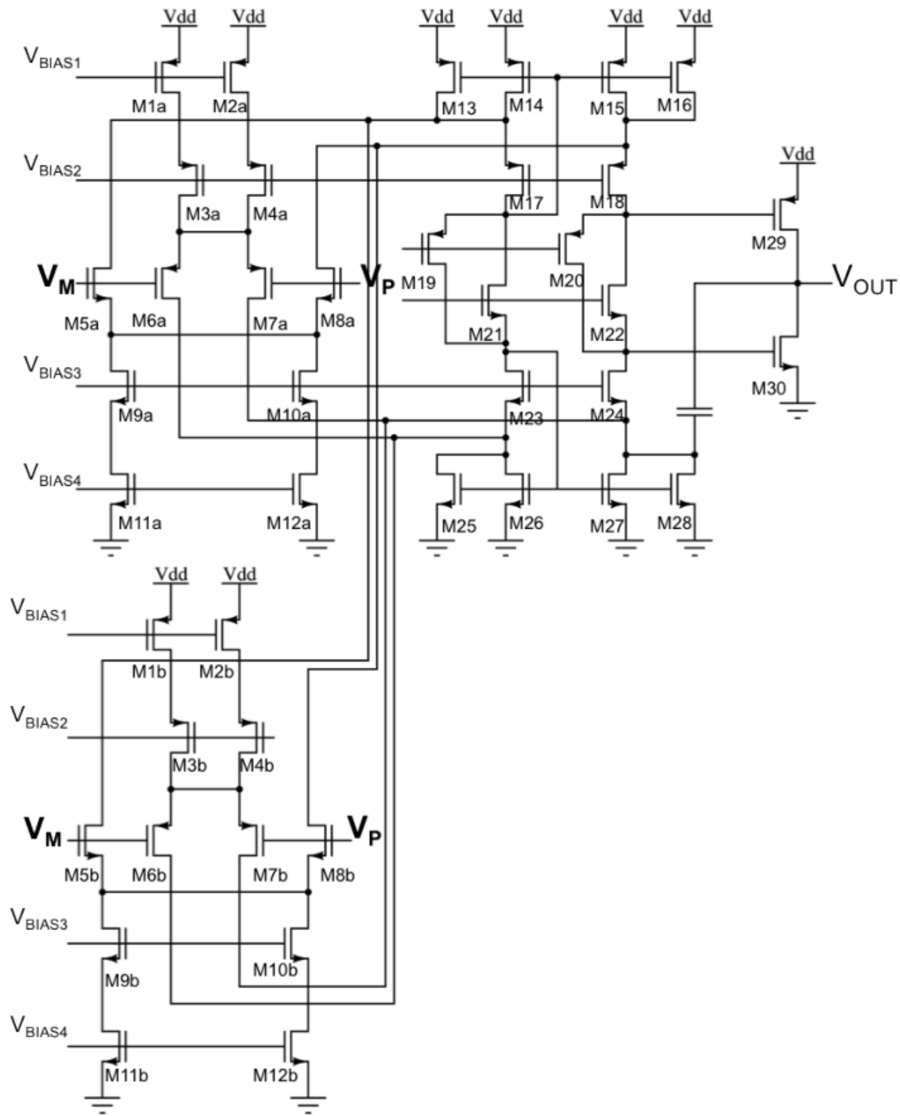


(a)



(b)

Figure 3.8: Peeling implementation in 32nm SOI. The blue portion of (a) is the peeled portion in the actual layout. The original circuit (b), and the peeled input version (c) [17]



(c)

Figure 3.8: Peeling implementation in 32nm SOI. The blue portion of (a) is the peeled portion in the actual layout. The original circuit (b), and the peeled input version (c) [17]

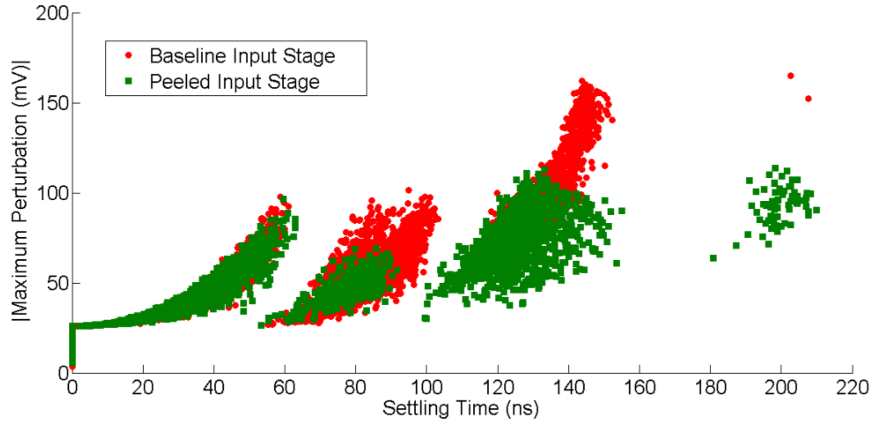


Figure 3.9: Results for 32nm SOI peeled input versus baseline circuit. Results show a decrease in maximum perturbation for peeled circuits and slight increase in settling time at higher LETs [17]

in maximum perturbation at higher settling times compared to the baseline circuit (Fig III-8 (b)). Additionally, the peeled circuit showed markedly improved sensitive area compared to the baseline circuit. However, internal to the circuit, the transient is never actually stopped, and as a result, significant transients can appear along the power rails of the circuit, which can be potentially problematic for other parts of the circuit.

3.2 Modeling and Simulation Process

Accurate modeling of SEEs is paramount to effective design and simulation of circuits. This is even more the case as technology scales and circuit operating frequency increases. As the circuit response times become comparable with the characteristic times for single-event charge deposition and collection, the charge collection process dynamically interacts with the circuit response. As a result, it is now necessary for the model to more accurately represent the pulses time width. Traditionally, a double exponential current source was used to model SEEs in a circuit. The main problem with using a double exponential current source, even if one is able to fit a TCAD result to it, is the ideal nature of the source. Idealized sources in any simulation can force unrealistic voltages or currents at a node and

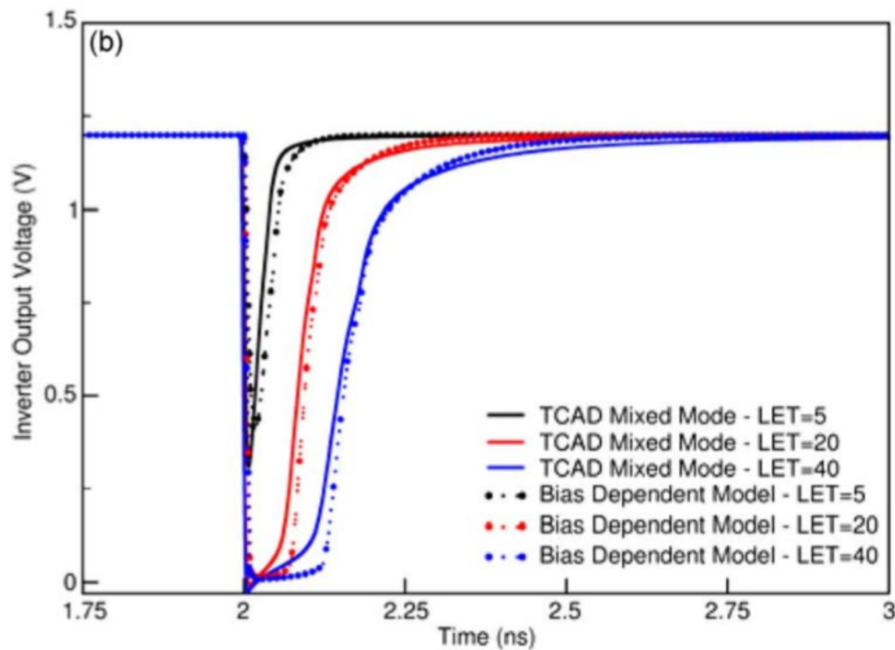


Figure 3.10: Comparison between TCAD Mixed Mode transient simulations and Bias Dependent Model [5]

provide suspect results. TCAD simulations have shown that the load on the struck device can shape the response of the current waveform within the device, resulting in an elongated plateau effect [5].

Figure III-10 shows a comparison between a traditional double exponential model and a more accurate TCAD model. Since this work is limited to simulations, an accurate transient model, and one that interacts with the circuit in a non-idealized manner, was crucial. The bias dependent SE model used in this work is one developed at Vanderbilt university that provides said functionality. Figure III-11 contains a schematic of said model implemented in Verilog.

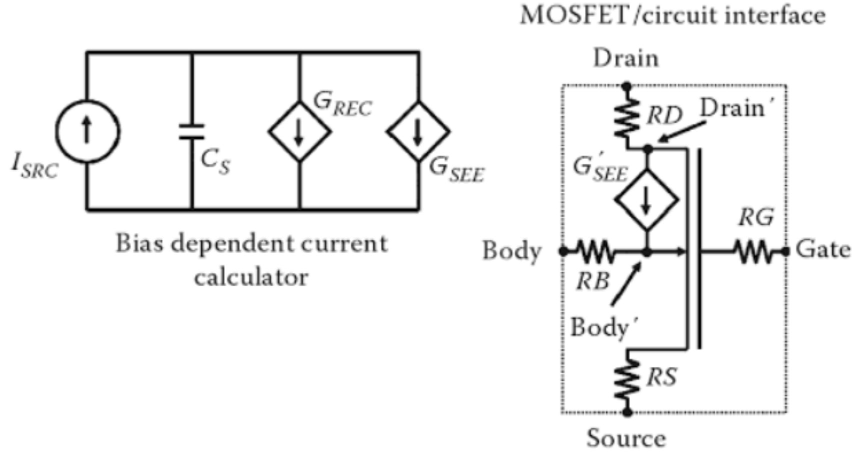


Figure 3.11: Schematic of the bias-dependent SET model used through this work [5]

$$I_{SRC}(t) + \frac{C_S dV(C_S)}{dt} = G_{REC}(t) + G_{SEE}(t) \qquad \textbf{III-1}$$

$$G_{REC}(t) = f(V(C_S), C_S, \text{RecombParameter}) \qquad \textbf{III-2}$$

$$G_{SEE}(t) = f(V(C_S), C_S, f(V(\text{drain}', \text{body}'))) \qquad \textbf{III-3}$$

$$G'_{SEE}(t) = G_{SEE}(t) \times \text{Gain} \qquad \textbf{III-4}$$

The corresponding equations are listed in III-1 through III-4. ISRC, represents the basic time-current profile for depositing the desired amount of charge into the device. The double exponential waveform will typically suffice for this. The capacitor, CS, is used to ensure charge conservation. The voltage across the capacitor is proportional to the charge that has not been dissipated by the two dependent current source branches. The GREC source accounts for recombination currents in the device. GSEE is the source, and is multiplied by some gain, usually 1, unless it is necessary to account for parasitic bipolar effects [5].

Chapter 4

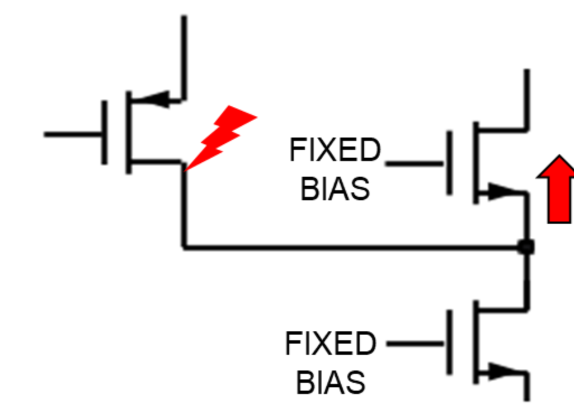
Sub-circuit Peeling and Directional Temporal Filtering

In the previous chapter, the idea of hardening via node splitting was introduced and the effectiveness of circuit peeling was examined. This chapter seeks to present additional node-splitting techniques for hardening analog circuits that work in concert with circuit peeling. The techniques presented herein can be headed more generally under hardening via node-splitting. Previous work done with peeling looked primarily at input-to-output peels for an entire circuit system.

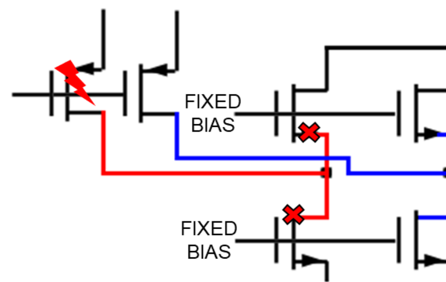
The main focus of this work is on extending peeling to smaller analog sub-circuits. Initial attempts at doing so had mixed results, largely owing to limited signal path isolation as the device count got smaller. Especially troublesome were gate-drain diode connections, a very common circuit configuration. Transistors that are connected in this diode configuration present inherently vulnerable nodes within a circuit, as a transient voltage appearing at such a location can then appear across the gate of multiple transistors, many of which often dictate bias currents for the entire circuit. Additionally, they significantly limit the applicability range of peeling at a sub-circuit level where device count is low. In order to remedy this gate-drain connection issue, it was proposed that a transistor biased in the ohmic region be placed in the diode connection path.

4.1 Peeling at a Sub-circuit Level

The effectiveness of redundant paths in hardening was shown in chapter 3 with regular circuit peeling, for which it was concluded that it was advantageous to peel virtually any analog circuit, given the small physical area penalty, relatively small sensitive area penalty, the lack of any active area penalty, the ease of implementation, and the significant mitigation provided. However, a designer may not always want to peel the entire circuit.



(a)



(b)

Figure 4.1: Self mitigating path conception (a), and peeled version of such a signal path (b)

Depending on the circuits size/design, it may not even be practical to do more than a 2x or 4x peel. If a designer wishes to minimize the amount of peeling for a circuit, it is indeed possible to achieve similar levels of mitigation by peeling only critical sub circuits. Sub-circuits for which peeling is especially effective are ones that demonstrate self-mitigating properties. An example would be any circuit that sees a signal from a PFET device flow into NFET devices, or vice versa. Such configurations naturally lend themselves to better transient mitigation.

Peeling at a sub-circuit level can be more challenging, however. Previous work done with node-splitting indicated that peeling does not improve the SET response for strikes to devices directly connected to the output nodes. For example, very minimal improvement was seen in the active load inverting amplifier with peeling. As a circuit gets down to 3-4 devices, the effectiveness and applicability of peeling becomes limited. To combat this, a

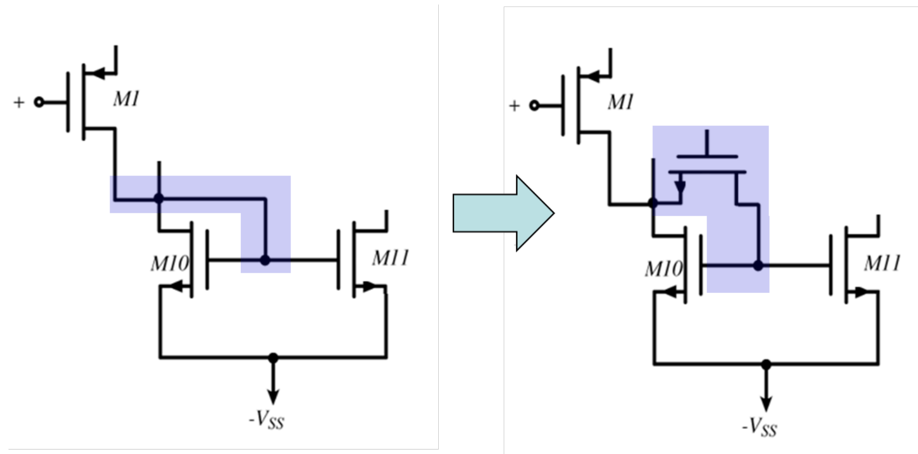


Figure 4.2: Differential Temporal Hardening implementation with an NFET

technique known as Directional Temporal Filtering was proposed.

4.2 Directional Temporal Filtering

Diode connected nodes in analog circuits are a very common circuit configuration and are often very vulnerable to single event transients. Voltage transients appearing at these nodes can potentially propagate directly to many other portions of the circuit. While attempting to achieve proper signal isolation for sub-circuit peeling, these types of connections presented an obstacle. Whereas a transient traveling into only the drains and sources of opposite-channel devices was effectively stopped, as shown in Figure IV-2, a transient that traveled into a diode connected node was not stopped and was able to essentially bypass the desired cutoff thanks to the transistor connected opposite via the gate. The solution to this was to place a transistor inside the path of the diode connection, as pictured in Figure IV-2. These devices operate in triode, effectively acting as large resistors for normal operation. This is desirable, since only a voltage signal needs to make it across to the gates of the transistors on the other side, and any significant voltage drop from a device in saturation would disturb the original bias conditions of the circuit at that node.

When a transient voltage appears at the transistor in the diode path, the desired mitigation is achieved in part through temporal filtering (i.e. resistive and capacitive elements)

and in part through an active response. When a voltage at the node rapidly goes high or low on one side of the transistor due to a transient, the capacitive effects present at the node due to the transistor prevent the voltage from immediately transitioning to the other side of the diode-path transistor. The result is a potential drop across the transistor, and current flow which acts against the incoming transient. This mechanism for behavior is supported by attempts at modeling the transient response as the result only of temporal filtering, i.e. an effective capacitor/resistor, which were not able to completely capture the behavior of the triode transistor for both positive and negative voltage transients. Through modifying capacitance and resistance values, it was possible to model some of the effects of a triode device at that node, but only for a single polarity (+/-) of transient. The opposite polarity usually showed significantly longer recovery times. PFET devices provide better mitigation response to incoming negative transients, while NFET devices provide better response to positive transients. Both NFET and PFET devices can be placed in series, which can provide mitigation of transients in both directions. In this work, the choice of device configuration is referred to as N, P, NP, or PN-DTF. PFET devices are always tied to VSS at the gate, and NFET devices are always tied to VDD. Regardless of the device used, they provide at least some mitigation for transients of both magnitudes due to the temporal filtering effects. This technique generally requires less area penalty (minimum device sizes can be used) than simply using a resistor and capacitor for temporal filtering, and the active area added is inherently hard against strikes due to the nature of its location within the circuit. Additionally, from a design and layout perspective, this technique is much simpler than choosing capacitor and resistor values for temporal filtering.

Knowledge of the local bias conditions as well as the expected magnitudes of transients is required for this technique to be effectively implemented. In addition to proper bias knowledge, it is important to note that for diode connections at PFET/NFET junctions, such as the one examined in the bootstrap current reference later in this chapter, both device types in series along the diode path are necessary to account for the potential of two different

transient polarities (i.e. negative from the NFET or positive from the PFET).

Directional Temporal Filtering (DTF) was first conceived to work in concert with peeling, but for some bias circuits, it is able to provide sufficient hardening by itself in cases where a circuit cannot be peeled. In some cases , using it alongside peeling does provide a slight improvement in the maximum transient magnitude (compared to just peeling), but this small improvement must be weighed against the addition of another device (in the newly added peeled path), and by extension more active area. In other cases, using it alongside peeling provides significant improvement in transient magnitude reduction.

The choice of either NFET or PFET devices for DTF is informed by the surrounding device types and knowledge of the typical transient magnitude direction expected at a given node. For example, in the peeled signal path of the PFET input device to the NFET differential pair and current mirror, one would expect a strike from the PFET device to pull that signal high. As such, one would opt for an NFET device for DTF. For a similar NFET input to PFET current mirror, one would opt instead for a PFET device, as they would expect to see a negative transient along that signal path from the NFET device. The methodology and logic behind device placement will be discussed further with specific examples in the later sections of this chapter.

We will now look at some common analog structures and where peeling and DTF hardening are most effectively implemented. These structures were chosen because they are fundamental analog circuits, some variation of which can almost always be found in more practical advanced analog circuits. Each example is meant to inform some aspect of the design methodology for peeling with DTF hardening. Verification of these techniques was limited to simulation for this work, the majority of which was performed in a 180nm PDK. When performing circuit simulations, the designer should have a good idea of what they expect to see from the simulations. Unpredicted or unexpected behavior is very often a fault with the simulation and not a new discovery. Ideal simulation components are often the cause for misleading results, as they can force unrealistic responses. For this reason,

care was taken to avoid using ideal current sources.

4.3 Bandgap VOltage Reference

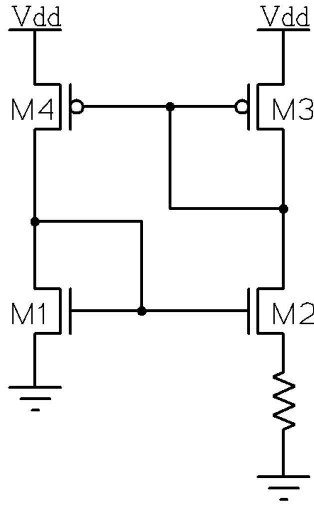
In an analog circuit it is paramount that the system has access to an invariant current or voltage source. When designing a circuit, this is usually approximated as an ideal current source from which a current mirror can draw a reference. The practical realization of this usually takes the form of a bandgap voltage reference, and not unexpectedly, represents an extremely critical component in an analog circuit. If the reference is compromised, the circuit essentially becomes lost, as it no longer has a valid frame of reference. As such, protection of voltage references, and other auxiliary bias circuitry that can affect an entire system, is paramount when hardening a system against radiation effects.

The bandgap voltage reference pictured in Figure IV-3 is the first of a few biasing circuits that will be considered. In the case of this circuit, as is readily apparent, DTF hardening is necessary for both of the diode connections present in the circuit. The full circuit was peeled and summed at the node above Rs. The best choice of DTF configuration here is the PN configuration, due to the potential for transients of either polarity to appear at the node, either due to strikes to the PFET or to the NFET.

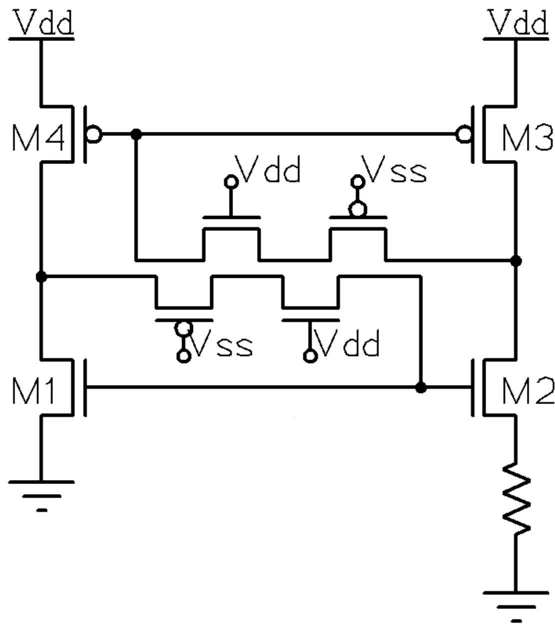
Figure IV-5 shows the results of strikes to M1 and M2 at an LET of 10 for the original circuit, the circuit with just DTF, and the peeled circuit with DTF (PN configuration). A significant decrease in transient is observed compared to the original circuit. The combination of peeling and DTF provides the largest reduction in transient magnitude. Interestingly, a circuit with just peeling did not show any improvement in transient response.

4.4 Differential Amplifier

The differential amplifier is one of the most ubiquitous circuit components, appearing as the input stage to virtually any amplifier. It is critical that transients be mitigated as much as possible at the input of a circuit, for any transient appearing at the output of the



(a)



(b)

Figure 4.3: Simple Circuit to Establish Supply Independent Currents (a), and Implementation with DTF (b)

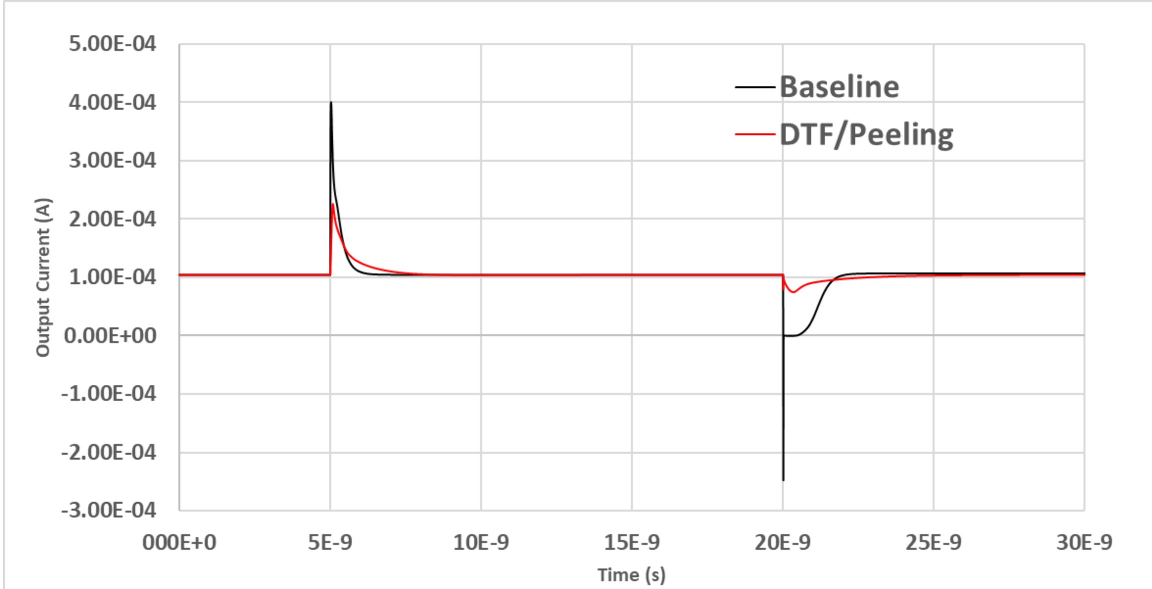


Figure 4.4: Strikes to M4 and M1 for Baseline and DTF/Peeled circuit at LET of 10

input stage will proceed to propagate, and be modified by, any circuitry downstream. If, for example, the input stage immediately feeds into a high gain stage, then an unmitigated transient will also be amplified by the same gain.

It is necessary to create a parallel peeled path in this circuit from the source of M5 to the output, as shown in Figure IV-6. Since the diode connection is connected to both P-type and N-type devices, it would stand to reason that a PN-DTF configuration would be desirable, as was the case with the bandgap reference. However, since the transient has a signal path via the connection at the top of transistors M1 and M3, there is not much that can be done to harden against strikes to M1. For this reason, a P-DTF configuration is sufficient.

Figure IV-7 shows the results of strikes to M1 and M2 at an LET of 10 for the original circuit, the peeled circuit, and the peeled circuit with DTF (P configuration). There is a slight improvement in transient magnitude between regular peeling and Peeling + DTF.

Given that the addition of the DTF devices will reduce the gain bandwidth product somewhat (.2dB at 5GHz), it is up to the designer to decide if the additional power rail protection and slight improvement in output transient mitigation is worth the loss in small

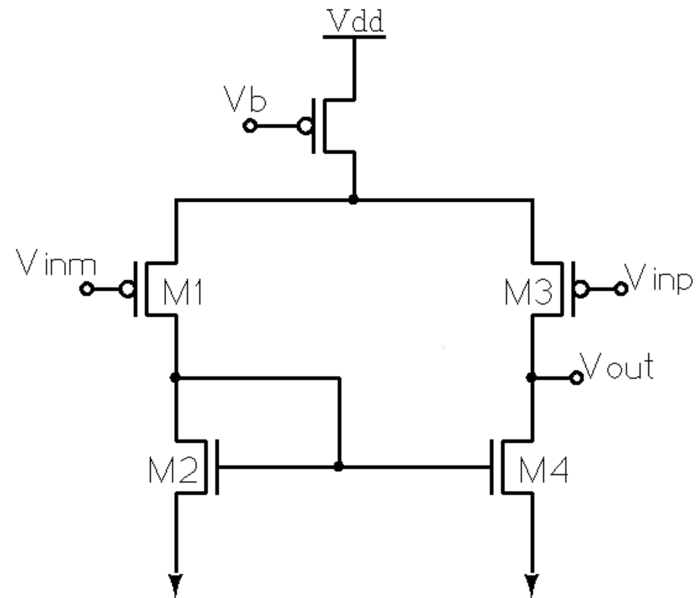


Figure 4.5: The Differential Input circuit considered for analysis in this section

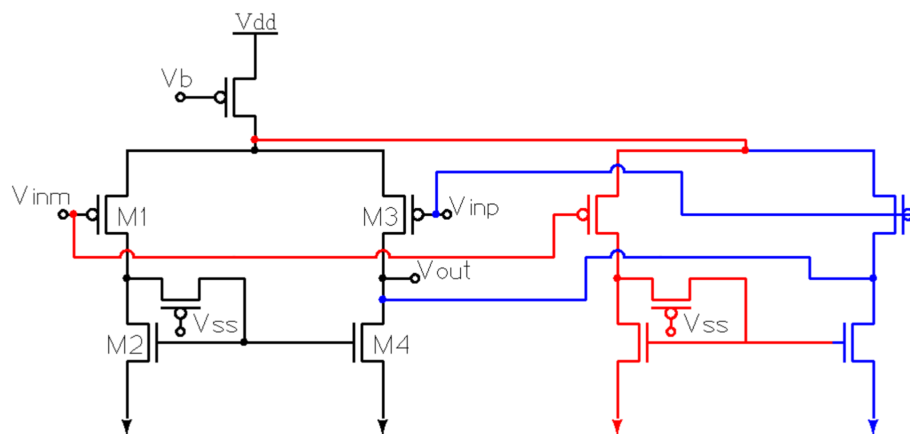


Figure 4.6: Peeled version of the differential amplifier with DTF at the diode connections

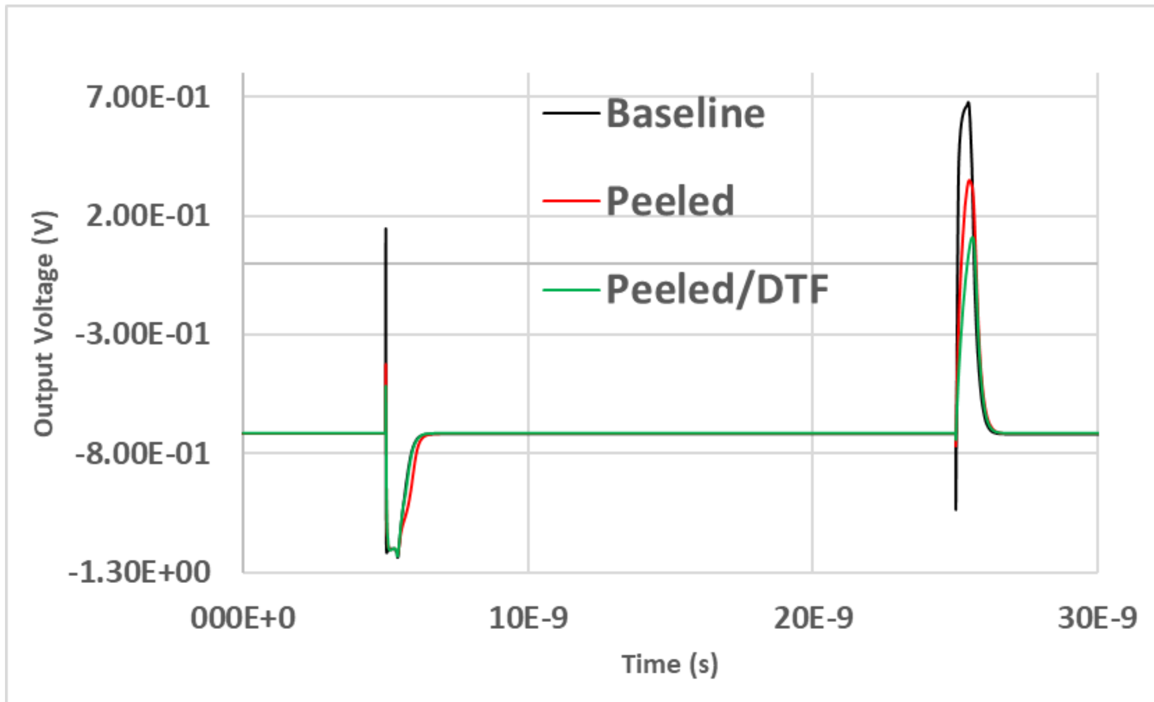


Figure 4.7: Result at output of differential amplifier due to strikes to M2 and M1 at an LET of 47

signal gain. Additionally, this example illustrates how peeling and DTF are less effective when signal path isolation is not completely achievable.

4.5 Voltage Reference Circuit

The circuit in Figure IV-8 is a simple voltage bias circuit, and happens to be the one used for the op-amps previously used to examine peeling and charge sharing techniques. For this circuit peeling was not performed, as there was no way to isolate strike paths, since every node acts as a voltage reference point. DTF hardening was used for the top and bottom diode connections, both of which used PFET devices. A complementary scheme was used for the DTF hardening whereby a PFET was placed amidst NFETs and vice versa, so as to self-assure the best possible mitigation for the N and P nodes. It is worth noting that, by using different configurations of PFET and NFET devices for DTF hardening, one can decrease the mitigation seen at the N and P nodes and increase the mitigation at the NP

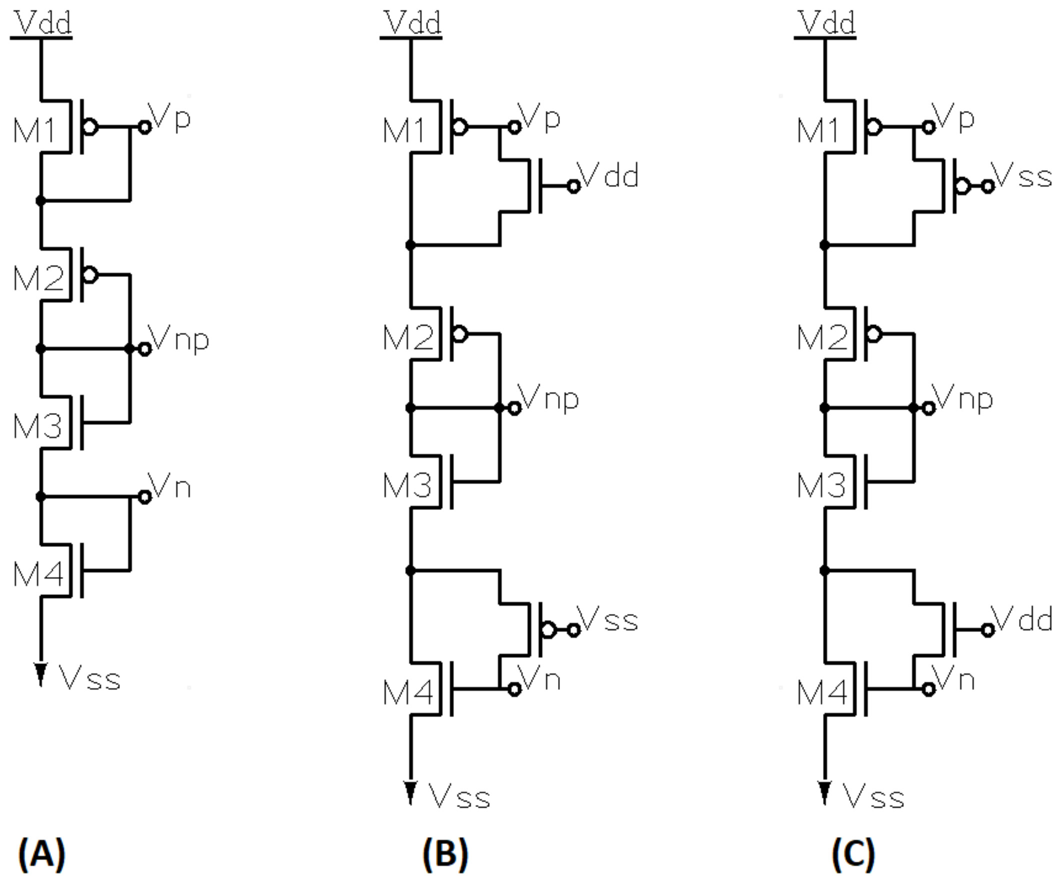


Figure 4.8: Bias Circuit found in the op-amp originally used to test the peeling concept (a), with complimentary DTF configuration (b), and matched DTF configuration (c)

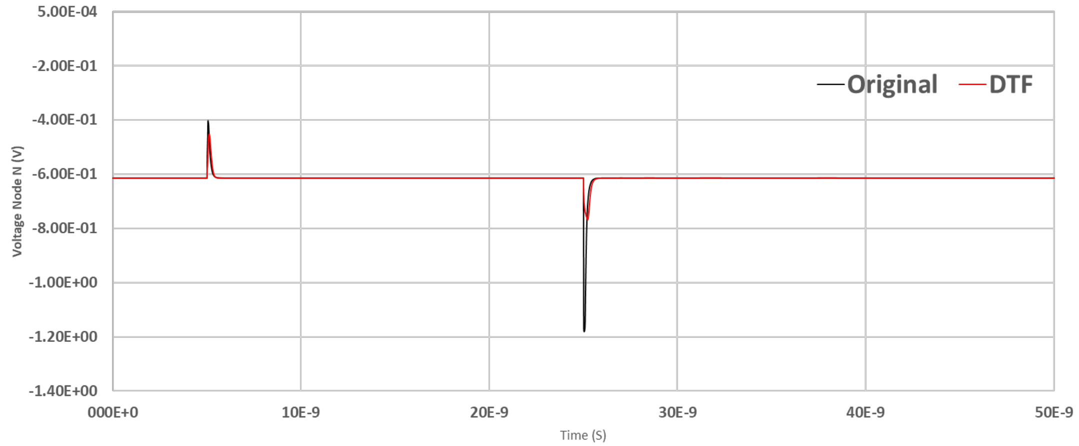


Figure 4.9: Voltage at Node Vn due to strikes to M30 (first transient) and M27 (second transient), using complimentary DTF (PFET placed with NFETS and vice versa)

node. As such there is no best way to implement DTF for this circuit.

Figure IV-9 shows strikes at M1 and M4 of LET 10. It can be seen that the N and P nodes receive significant transient mitigation, while the NP nodes response is virtually identical. A matched DTF configuration is shown in Figure IV-8 (c), and the results of strikes under the same conditions is shown in Figure IV-11 and IV-12. Here nodes N and P do not undergo as much mitigation, but the NP node sees mitigation for positive strikes. This circuit well-illustrates the mitigation options presented to a designer using DTF hardening, and how circuit configuration informs the choice of device type.

4.6 Wilson Current Mirror

The Wilson Current Mirror is a common circuit component. As a current mirror, it can function as a current source for biasing other circuits. It uses three transistors to mirror the current going in to IIN at IOUT, as shown in figure IV-13. Hardening M2 and M3 can be accomplished by peeling the circuit from VDD to IOUT. This particular peeled configuration is shown in Figure IV-X.

Since all of the devices in the Wilson current mirror are NFET devices, it is optimal to use a PFET for the DTF configuration, as strikes from the NMOS will produce negative

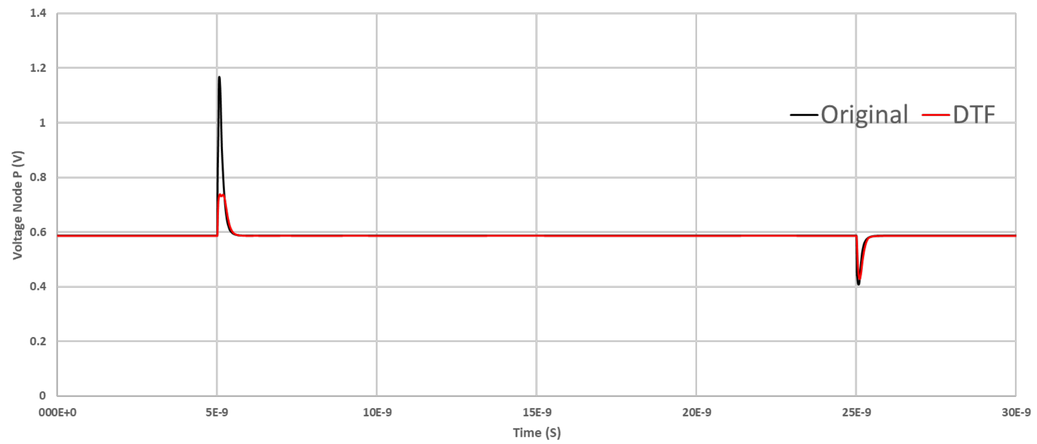


Figure 4.10: Voltage at Node Vp due to strikes to M30 (first transient) and M27 (second transient), using complimentary DTF (PFET placed with NFETS and vice versa)

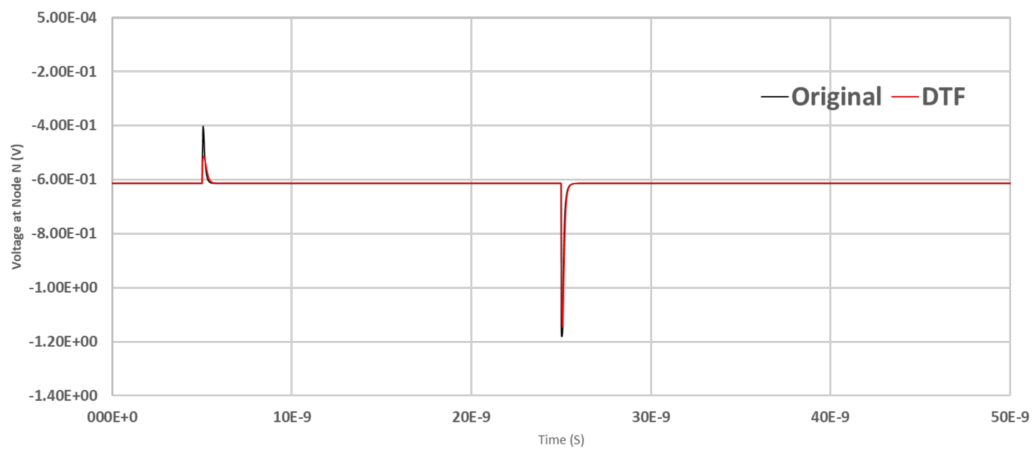


Figure 4.11: Voltage at Node Vn due to strikes to M30 (first transient) and M27 (second transient), using matched DTF (PFET placed with PFETS and vice versa)

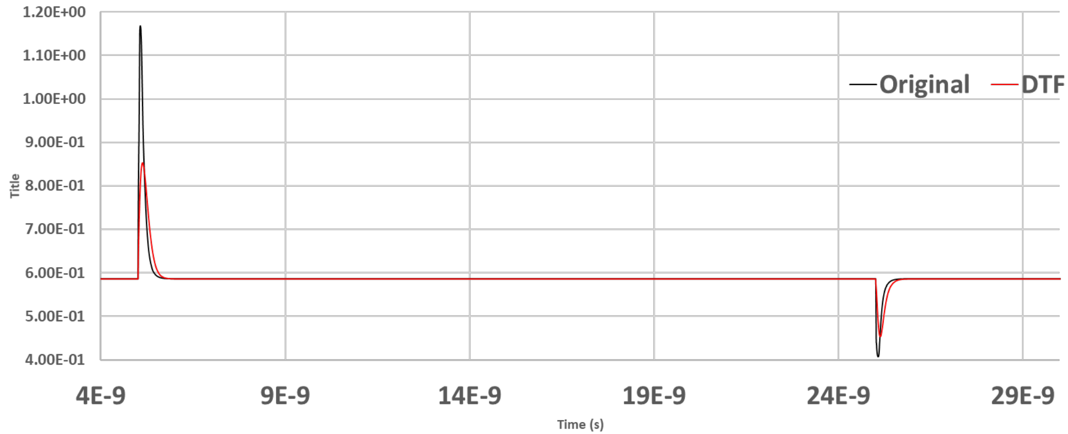


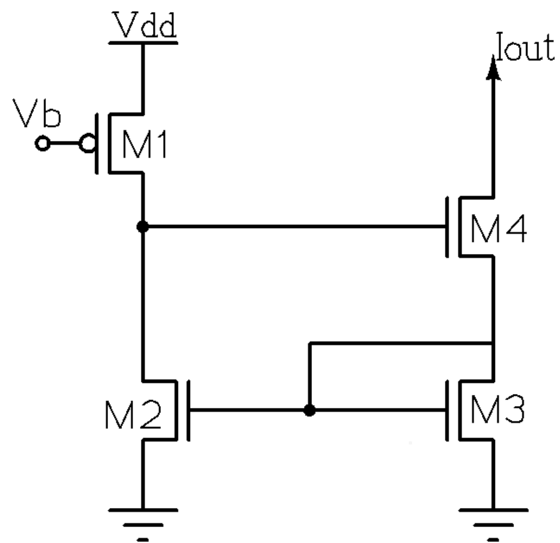
Figure 4.12: Voltage at Node Vp due to strikes to M30 (first transient) and M27 (second transient), using complimentary DTF (PFET placed with NFETS and vice versa)

transients. Additionally, by adding a PFET DTF Device to the M1 Drain ¡-¿ M3 gate connection, you can achieve slight improvement in the response. The biggest factor in hardening the WCM actually came down to being able to peel the current source feeling into it. By doing so, you are able to achieve far superior signal path isolation compared to having a single current source path where a strike to the NFET will produce a transient at a node that serves as a common input to both peeled paths.

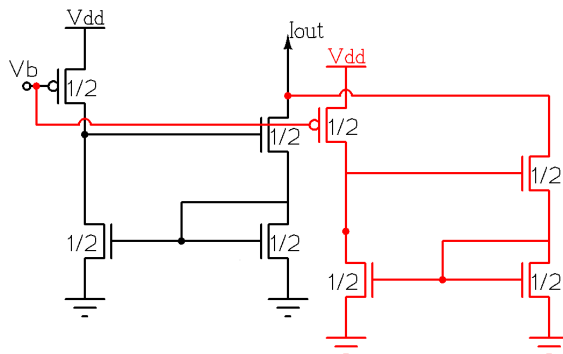
4.7 Cascode Current Sink

The Cascode Current Sink pictured in Figure Figure IV-X is a good example of the vulnerabilities presented by multiple-gate connected nodes in bias circuitry. A strike to any of the left-most transistors directly affects 2 additional transistors. The diode connection of course makes it a good candidate for DTF hardening. Indeed, this circuit was chosen to further illustrate a certain aspect of DTF, specifically the phenomena whereby a blocked signal will actually be much larger on one side of the node than in the baseline circuit.

It is loosely analogous to a wave crashing against a wall and splashing up higher than if it had simply hit the beach. This is fine, as far as the node is concerned since the other side of the wall sees a reduced transient, but its important that the circuit not provide another



(a)



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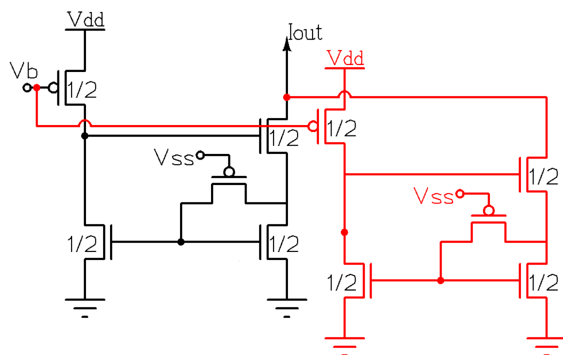


(c)

Figure 4.13: Wilson Current Mirror (a), with peeling (b), and peeling/DTF (c)

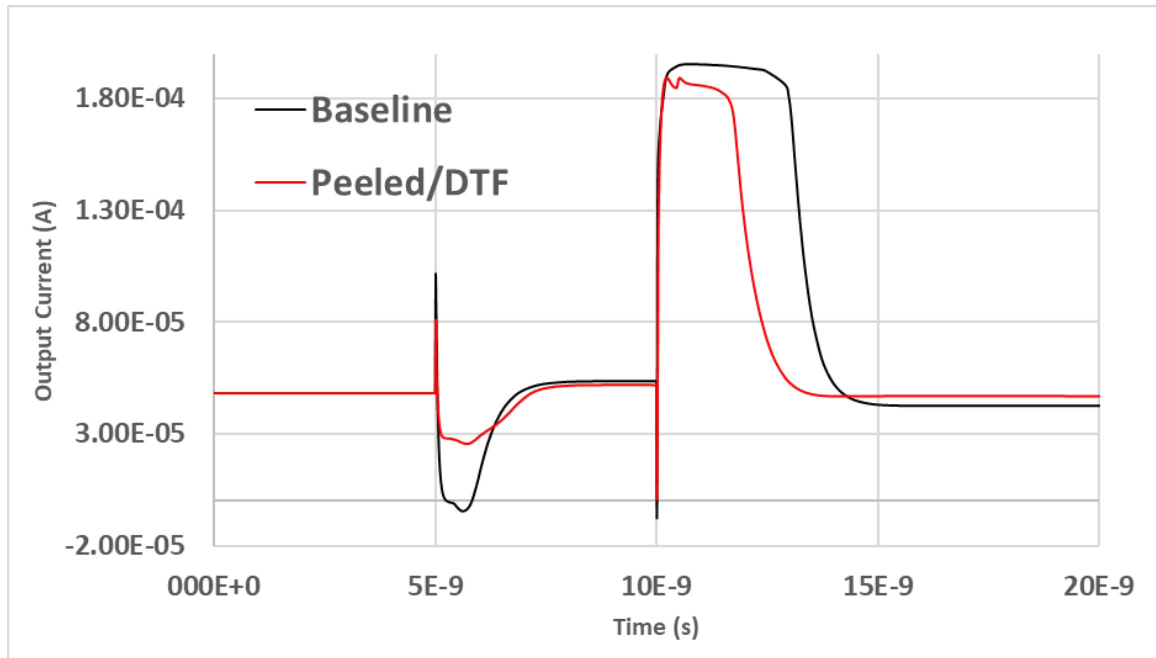
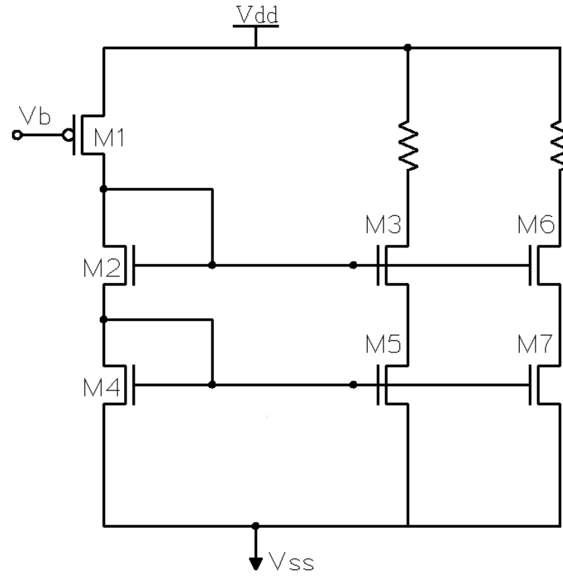


Figure 4.14: Strikes to M1 (First transient) and the NFET used for a current source (Second transient)

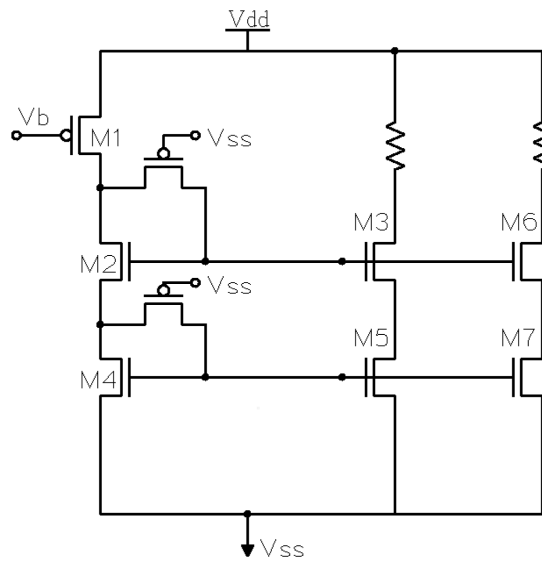
signal path for this increased voltage transient to escape to. In the case of the Cascode Current Sink, there is no such path. Strikes to M2 and M4 are effectively contained to their VDD-GND line with the addition of DTF. Peeling enhances the mitigation even further, as seen in figure IV-17. M2 and M4s peak transients were significantly reduced, and M1 saw slight reduction in pulse height.

4.8 Regulated Cascode Current Mirror

The regulated cascode current mirror pictured in Figure IV-18 does not have a diode connection, but peeling and DTF can aid it none-the-less. With peeling (2x & including the NFET current source) an improvement of about 50% was observed for peak transient magnitude. If the NFET current source was not also peeled, no improvement was observed for strikes to M2, which is expected, since the NFET creates a separate peeling path for the M1 Drain M2 Gate node. If the nodes are summed at the NFET source, M1 and M2 share a common node for both peeled paths and a strike to either path will create a transient on



(a)



(b)

Figure 4.15: Cascode Current Sink (a), with DTF (b)

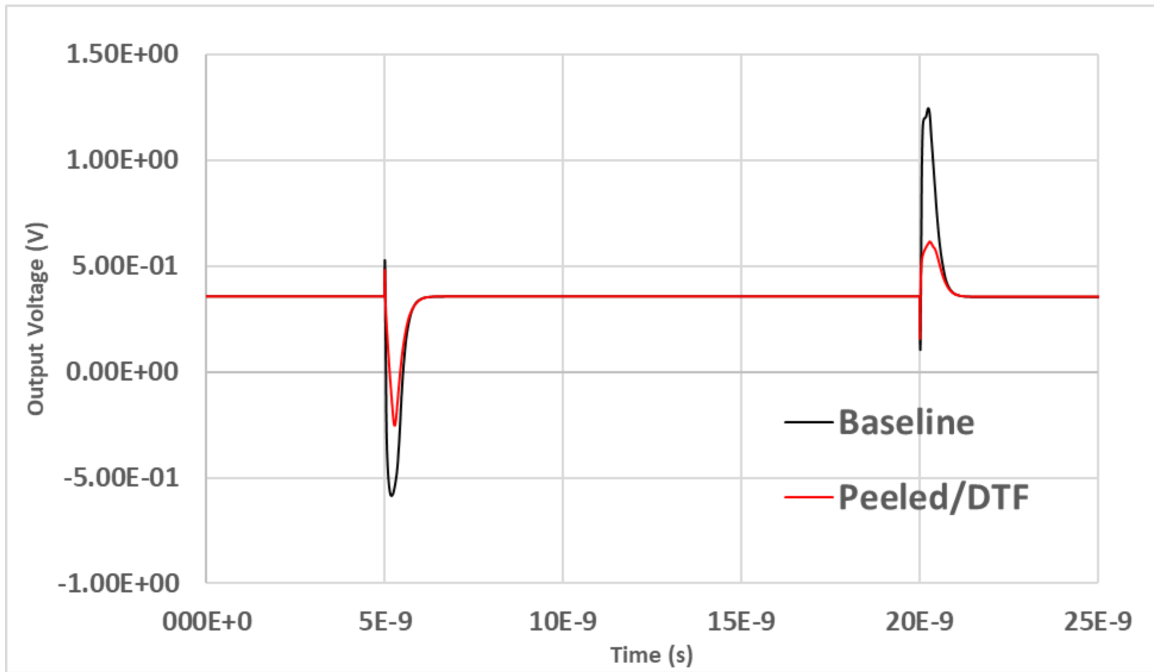


Figure 4.16: Output voltage due to strikes to M1 & M2 at an LET of 10. The first transient is the strike to M1 and the second transient is the strike to M2

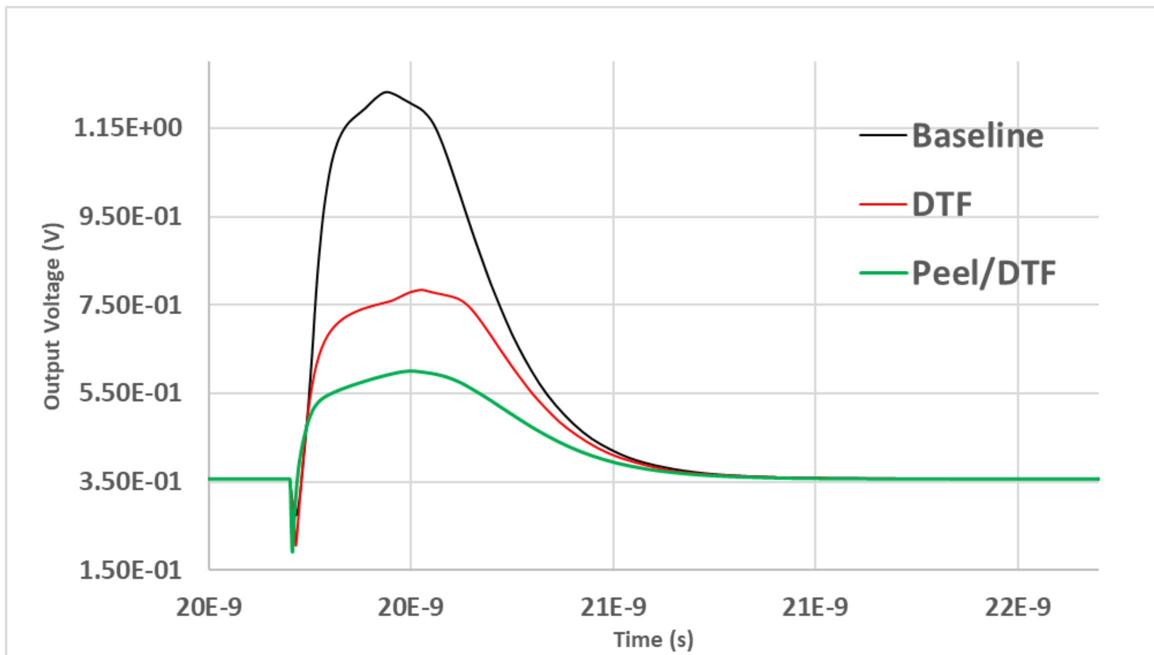


Figure 4.17: Output Voltage due to strikes to M3 at an LET of 10

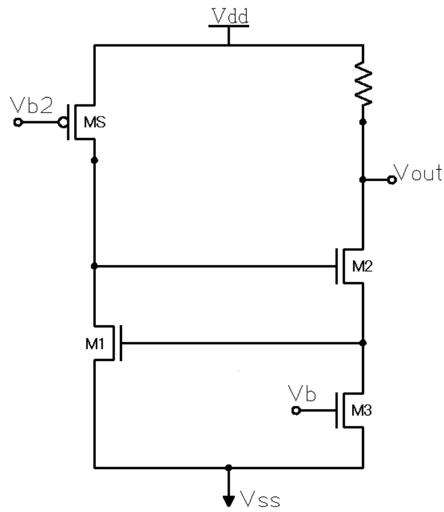


Figure 4.18: Regulated Cascode Current Mirror

both.

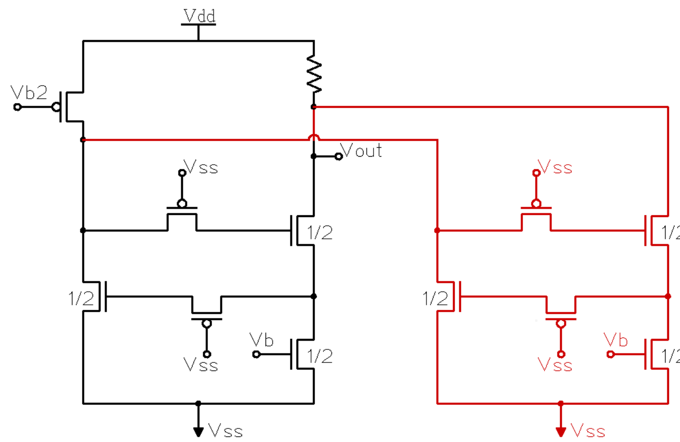


Figure 4.19: Regulated Cascode Current Mirror with peeling/DTF

However, with DTF, one can in fact harden M2 without needing to peel the NFET current source. A DTF device placed along the M1 and M2 Gate connections provides substantial mitigation at Vout against strikes to M2 compared to normal peeling.

4.9 Folded Cascode Amplifier (180nm)

Lastly, we will look at a more involved circuit, a single-ended folded cascode amplifier. One of the main motivations behind using this circuit is that the peeling concept had already

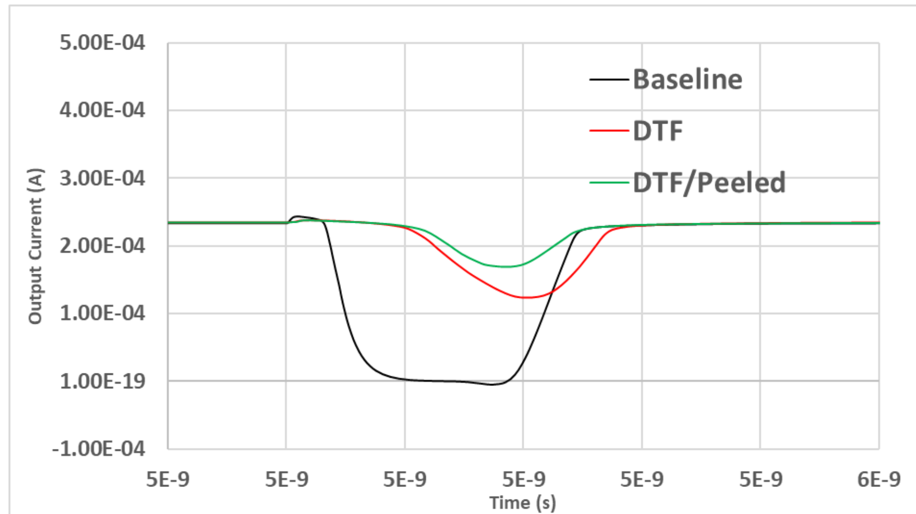


Figure 4.20: Transient at output current due to strike to M2 for regulated cascode current mirror

been experimentally verified to match simulation results for this circuit, which lends a little more validity to the simulations. The full circuit is pictured in figure IV-21. We will examine this circuit and go about identifying potential areas where peeling with DTF could be effective, to demonstrate the application of the techniques in this work to a practical circuit.

The reader will recognize the bias circuit as the same one discussed previously in this chapter. The diode connections at M19 and M13 present a good opportunity for hardening with peeling and DTF. Implementing DTF at the M15/M16 diode connection is an option, but it is not as effective given the nature of PFET/NFET nodes. Results shown are for strikes to the PFET input, M3.

4.10 Conclusion

This chapter has hopefully provided some insight into the working principles behind peeling with Directional Temporal Filtering (DTF). A collection of analog circuits was examined, each chosen to reflect some aspect of design implementation for peeling and DTF. The analysis done for this work suggests that DTF hardening in concert with peeling

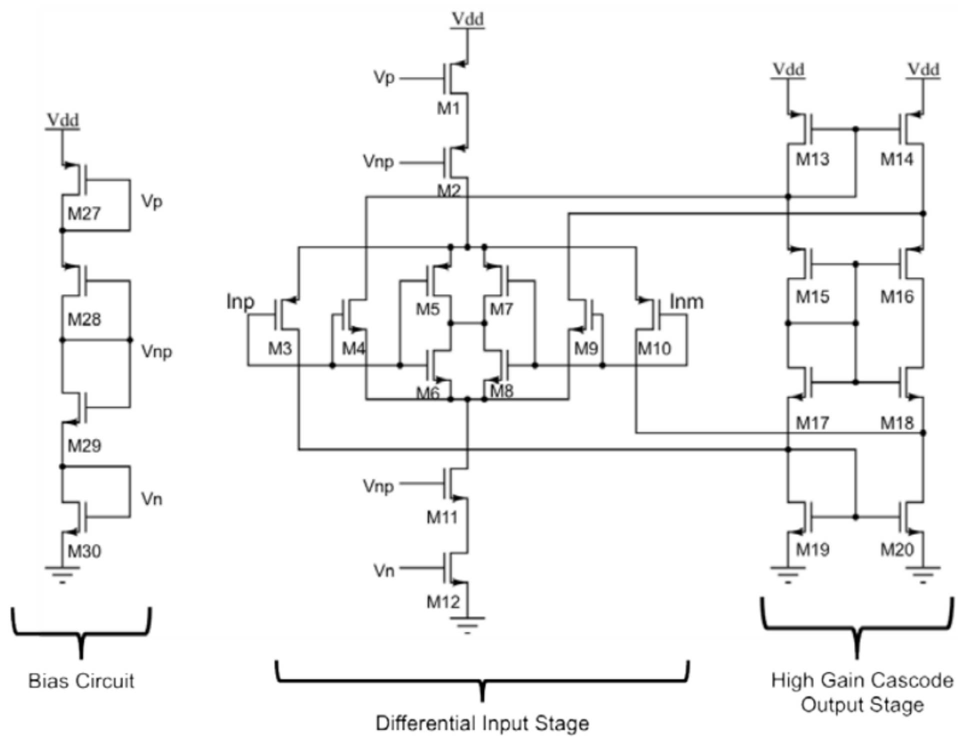


Figure 4.21: Input and Gain Stage for Single-Ended Output Folded Cascode Op-Amp

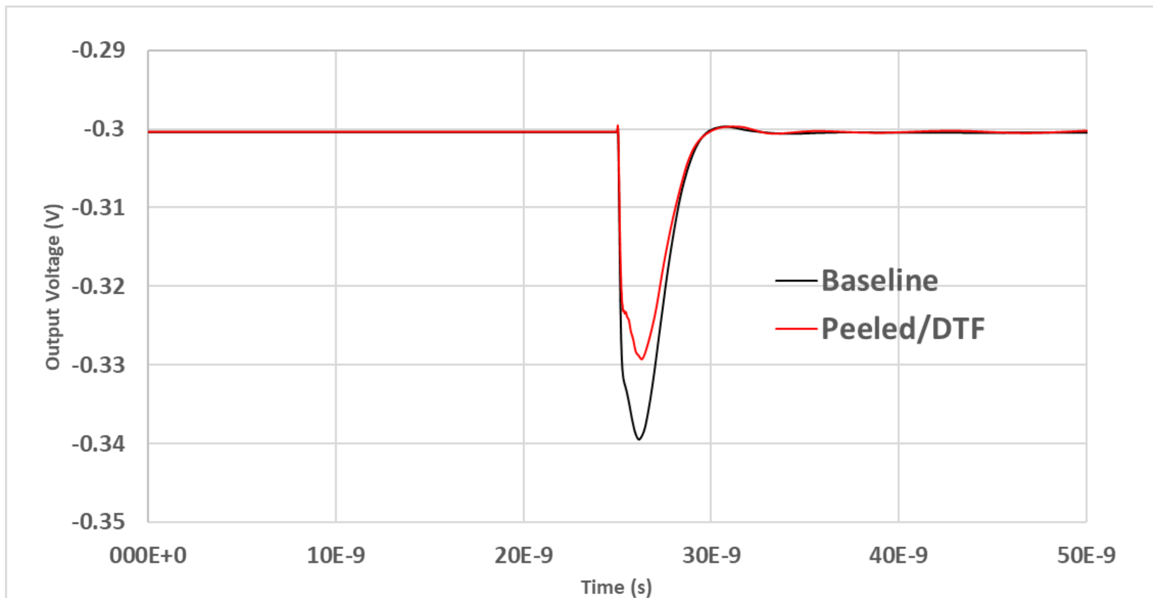


Figure 4.22: Result of strike to PFET Input Transistor at the output of the circuit in Fig IV-21, Peeled/DTF vs Baseline, configured for gain of 10 V/V

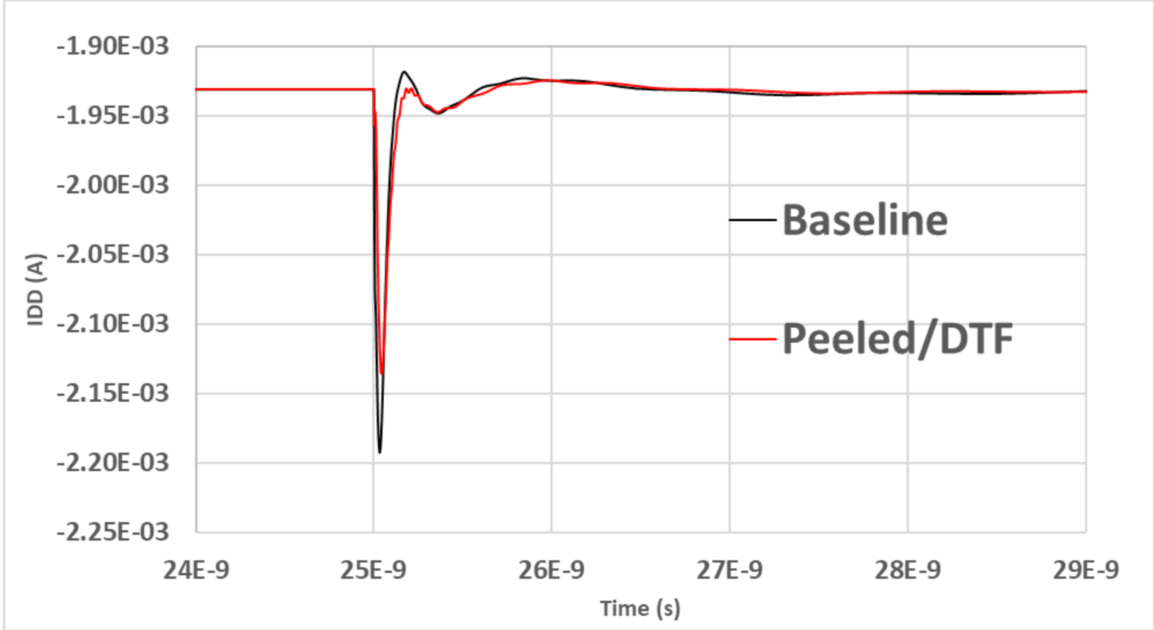


Figure 4.23: Current transient at VDD, Baseline and Peeled/DTF

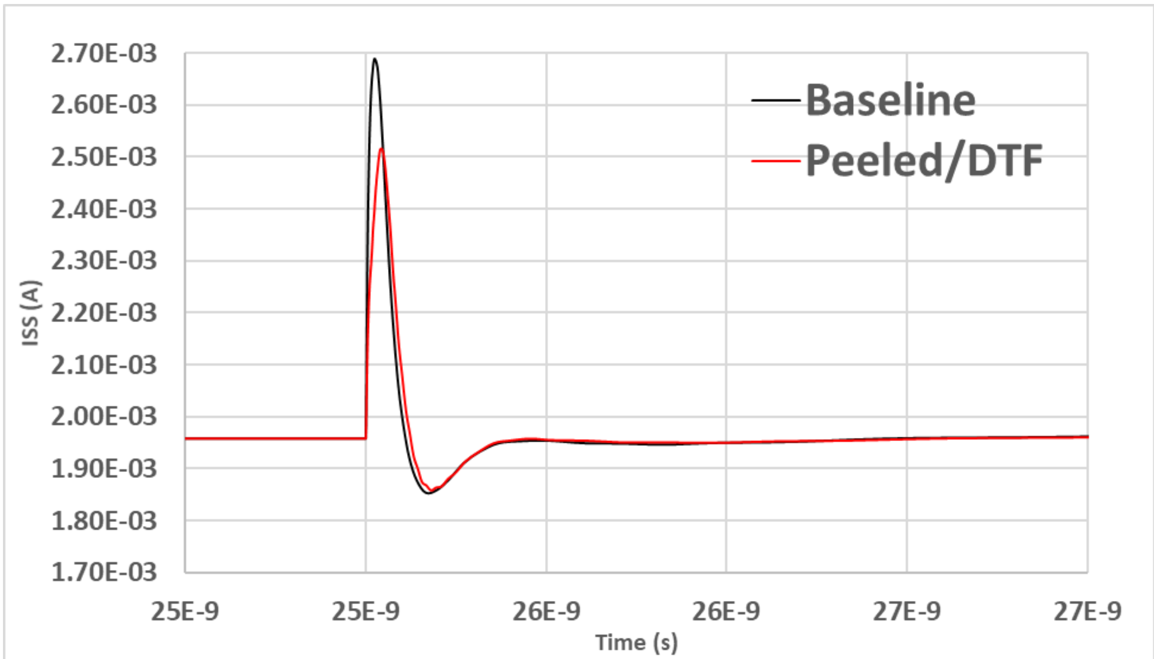


Figure 4.24: Current transient at VSS, Baseline and Peeled/DTF

can improve SE response for a wide variety of bias circuits with no electrical penalty and a very small area penalty. For small signal circuits, DTF can provide mitigation similar to temporal filtering, but in a manner more easily implemented and less costly in terms of physical and sensitive area. DTF will usually result in a small gain bandwidth penalty, as is typically the case with any kind of temporal filtering.

Chapter 5

Conclusions

This work presented additional peeling configurations that make use of a new hardening technique known as Directional Temporal Filtering. DTF was employed to harden gate-drain diode connected nodes which proved to be serious obstacles for peeling at a sub-circuit level. Using DTF devices, a designer has more options with which signal paths can be effectively peeled.

The majority of the simulations were performed in 180nm bulk, with a few preliminary simulations done in 32nm and 45nm SOI, confirming that the new peeling techniques function at a circuit level and are technology agnostic. One of the main motivations for pursuing this research was to provide an effective hardening method that did not rely on charge sharing phenomena to function, as SOI processes and some larger processes are less affected by charge sharing.

The search for a way to harden diode connected transistors gave rise to the second technique presented in this work, Directional Temporal Filtering (DTF), so-named because it provides a small amount of temporal filtering along with naturally activated cutoff from the transistor. DTF provides significant hardening for gate-drain connected nodes with very small Gain-BW and area penalties, and due to the nature of its placement within the circuit, does not introduce a potentially sensitive new device. This technique is most effective with bias circuitry. The main drawback with this technique is that it is slightly more involved from a design perspective. There are multiple configurations of PFET/NFET that a designer can choose and there is not necessarily a best configuration for every circuit, depending on which nodes are considered critical. It should also be noted that the effectiveness of any of the techniques in this work are largely dependent on the bias conditions for the circuit in question.

Combined, peeling and DTF present effective hardening techniques for analog circuits that take advantage of naturally mitigating signal paths and the principle operating mechanics of peeling. The addition of DTF hardening provides a designer with greater opportunity to create isolated signal paths, which in turn works with peeling to improve transient mitigation, and do not come with very steep penalties.

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