IMPACT OF PROCESS VARIATIONS ON SOFT ERROR SENSITIVITY OF 32-NM VLSI CIRCUITS IN NEAR-THRESHOLD REGION

By

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CHAPTER I

Introduction

As technology scales, power consumption has become a major concern in circuit design [HAP+05]. In the early history of CMOS, the scaling of the supply voltage was in accordance with the scaling of the transistors in order to maintain constant electric fields in the device. In recent years, as fabrication uses sub-100 nm feature sizes, the scaling of supply voltage slowed down to control leakage power and to maintain device performance [MBR06]. The slowing of voltage scaling causes the power density to increase dramatically [CFM+10].

There are several approaches for reducing power consumption [VF05]; one effective way is to lower the supply voltage to a value slightly higher than the transistor's threshold voltage. This region in which the circuit operates is called the near-threshold region [MWA+10]. Compared to the conventional super-threshold region (i.e., supply voltage is nominal value), circuits working in the near-threshold region are more sensitive to process variation, which is the variations introduced in the fabrication process [DWB+10]. The problem of how the process variations impact the reliability and performance of circuits in the near-threshold region needs to be addressed.

The major reliability issue of concern is the soft error sensitivity of the circuit. If the charge deposited on a circuit node by a particle strike is more than the critical charge (Q_{crit}), then the node will be flipped, which will result in a soft error. The process variations make it harder to predict the response of the circuit to a particle strike. So the impact of process variations on the single event circuit response is significant [DLX05].

The impact of process variations on a circuit operating at nominal supply voltage has gained the attention of many researchers. The soft error sensitivity, performance, and power consumption of the circuits influenced by process variations have been studied in the lit-

erature [KBK+11][KBB+12][DLX05]. As near-threshold operation becomes common, the circuit response to process variations should also be explored [SGT+08][KKKT12][KKT13]. When the supply voltage is reduced to the near-threshold region, the impact of process variations on circuit responses can be much different from the circuit at nominal supply voltage.

In this thesis, a 6T SRAM circuit as well as two flip-flops are used to investigate the effects of process variations when operating at the nominal supply voltage and the near threshold region. The test circuits are designed using a 32-nm technology. A Monte Carlo approach is used to model the process variations according to the process corners. The distributions of critical charge, leakage power, and write delay time are found to be closely related to the process variations and show differences under different supply voltages. The results show that threshold voltage variability is a more significant parameter affecting the critical charge distribution of the 6T SRAM under near-threshold voltage as well as the nominal supply voltage. Also the leakage power in standby mode and the write delay time of the SRAM circuit under near-threshold voltage shows some differences from the nominal supply voltage. For the two flip-flops, the impacts of threshold voltage and effective gate length variations on critical charge distribution are almost the same for near-threshold supply voltage and nominal supply voltage. The key findings are listed in Table 1.

The rest of the thesis is organized as follows. Chapter II introduces the background and related work of radiation effects in microelectronics, near-threshold voltage operation, and process variations. Chapter III presents the impact of the process variations on soft error sensitivity of the 6-transistor SRAM cell. Chapter IV analyzes the influence of the process variations on soft error sensitivity of the flip-flops. Chapter V summarizes the thesis.

Table 1. Key findings for circuits operating at the near-threshold region when compared to the nominal voltage for 32-nm Synopsys library [hC]

	6T SRAM	Transmission Gate Flip-flop	C^2MOS (Clocked CMOS) Flip-flop
Critical Charge (Q_{crit})	• Reduction of 77% for Q_{crit} for both NMOS and PMOS hits. • 1.5 times larger variation for Q_{crit} of the NMOS hit; 2.7 times larger variation for Q_{crit} of the PMOS hit.	• Reduction of 76% for Q_{crit} of the NMOS hit; Reduction of 75% for Q_{crit} of the PMOS hit. • Almost same Q_{crit} variation for both NMOS and PMOS hits.	• Reduction of 69% for Q_{crit} of the NMOS hit; Reduction of 73% for Q_{crit} of the PMOS hit. • Almost same Q_{crit} variation for both NMOS and PMOS hits.
Leakage power	• Reduction of 92% for leakage power • Almost same leakage power variation.	• Reduction of 97% for leakage power • 13% reduction for leakage power variation.	• Reduction of 94% for leakage power • 49% reduction for leakage power variation.
Performance	• 5.0 times larger Write 0 delay; 13.7 times larger write 1 delay. • 15.2 times larger variation for write 0 delay; 9.0 times larger variation for write 1 delay.	• 58.8 times larger clock-to-output delay. • 4.6 times larger clock-to-output delay variation.	• 69.6 times larger clock-to-output delay. • 5.2 times larger clock-to-output delay variation.

CHAPTER II

Background

Reliability is one of the most important factors in circuit design. For modern CMOS technology, the circuit reliability is influenced by the shrinking of technology, the reduced supply voltage, higher clock frequency, and higher circuit density. These factors affect the circuit's probability of soft errors (also called single event upset). In addition, the process variation introduced in the fabrication process is also a big challenge for circuit designers because it makes the same circuit show different characteristics. Moreover, to reduce power consumption of the circuit, the method of reducing supply voltage to the near threshold region is used, which is anticipated to have more effects on the reliability of the circuit. So the relationship between single event effect and process variation under near-threshold supply voltage should be analyzed and discussed.

The backgrounds information related to the main concepts in this thesis are presented in the remaining part of this chapter.

A. Single event effects

A single event effect is a circuit or system response to charge deposition from a single ionizing particle [DM03][Bau05]. Single event effects can induce destructive and nondestructive damage to the circuit. In this thesis, only the nondestructive single event effect is taken into account.

The basic mechanism for the single event effect in microelectronics includes the charge deposition and the charge collection. In the charge deposition process, there are two ways to release charge in semiconductor devices: (1) direct ionization is caused by the incident particles, and (2) indirect ionization is caused by the nuclear reaction between the incident particle and the device. Usually the deposition mechanism for heavy ions like alpha particles is mainly direct ionization, and light particles like protons and neutrons can result in

single event upset by indirect ionization [DM03].

For direct ionization, when a particle hits the silicon substrate, a track of electron-hole pairs (EHPs) is generated as the particle travels through the material and loses energy along its path. For indirect ionization, as the light particles enter the semiconductor device, nuclear reactions will occur: (1) elastic collision; (2) the emission of alpha or gamma particles and the recoil of a daughter nucleus; (3) spallation reactions. The products of these reactions can deposit energy along their path by direct ionization [DM03].

In the collection process, the most sensitive region in the transistor is the p-n junction. Because of the high electric field in the p-n junction depletion region of MOS transistor, the process of drift happens shortly after the particle strike, which leads to a transient current [Bau05]. After the drift process, as electron-hole pairs go outside of the depletion region, the charge is collected by diffusion. The diffusion is a slow process, which is related to the concentration of the carriers. Then the track of electron-hole pairs, also called the charge track, changes the electric field in the transistor, resulting in the charge collection outside the depletion region through the drift process and causing the increase of the total amount of charge collected via the drift process. These charges are deposited to circuit nodes, causing a transient current pulse. For combinational logic circuits, the transient can cause incorrect outputs if they arrive during the sampling of a latch; for memory cell, these particle strikes can cause the bit flips, which are called single event upsets (SEUs). The minimum deposited charge that can cause a bit flip is called the critical charge (Q_{crit}).

Fig. 1 shows the whole deposition and collection process and the current pulse induced by the particle strike: in Fig. 1(a), a track of electron-hole pairs are generated in the path of the particle. When the ionization track goes close to the depletion region, a large current transient is created at the node; in Fig. 1(b), the particle strike extends the depletion region further into the substrate, which facilitates the drift collection; in Fig. 1(c), the diffusion collection becomes dominant in the collection process [Bau05].

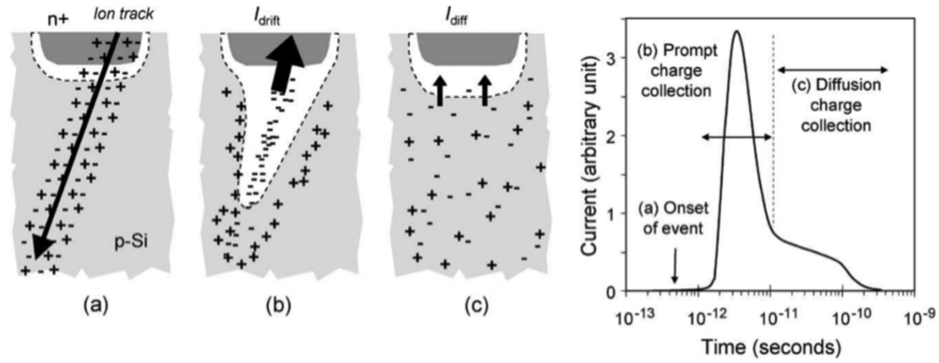

Figure 1. Charge generation and collection in a reverse-biased junction and the resultant current pulse [Bau05]

B. Process variations

Process variations are variations introduced in the manufacturing process of integrated circuits (ICs). The process variations can be classified into die-to-die variations and within-die variations. Die-to-die variations determine the distribution of frequency of dies, while within-die variations determine the maximum frequency of the die [Nar05]. For example, the performance corner of the die will be changed due to the die-to-die variations. For a die of slow corner (high threshold voltage), the transistors will have high threshold voltage.

Die-to-die variations are usually due to the processing temperature and equipment properties, while within-die variations are caused by the factors like channel length variations across a die. Within-die variations can be further divided into random and systematic variations. Systematic variations are due to lithographic aberrations, while dopant fluctuations and line edge roughness cause random variations [UTB+06].

Process variations come from many sources, such as polishing, lithography, resist, etching and doping. For example, chemical mechanical polishing is related to the nonuniform layout density, and the denser part of a chip has a slower polishing process. So the dielectric in the denser section is more highly polished, which leads to variations in dielectric thickness across the die. Furthermore, the variations resulting from lithography are becoming important as technology scales. The stepper is a significant factor causing the variations.

To be specific, the variations are mainly caused by the stepper lens heating, uneven lens focusing, and related aberrations. In addition, in the exposure and resist process, the surface tension causes the thickness variations. In the etching process, the unevenness in the etching power and density results in depth variations. After etching, the doping process causes the dopant concentration to be an important variation source [UTB+06].

As technology goes beyond 90 nm, parameter variations including process variations change the design problem from deterministic to probabilistic [BCSS08]. Process variations impact one or more design parameters of the devices, such as channel length, device width, and threshold voltage. The channel length variations are related to wafer non-uniformity, lens focus and aberration, and line edge roughness. The device width variations are induced by polishing and lithography process. Threshold voltage results from the oxide thickness and dopant fluctuations [UTB+06].

The variability of these parameters causes the variability of the circuit responses. For example, the variations in channel length and threshold voltage have a great influence on the leakage current of the circuit and therefore cause variations in leakage power and operating frequency at the chip level. Fig. 2 shows the 20x variation in chip leakage and 30% variation in chip frequency caused by process variations. The wide spread of the standby current is caused by the variations in channel length and threshold voltage. In addition, from Fig. 2, the higher frequency chips have a wider distribution of leakage [BKN+03].

C. Near threshold operation

In modern CMOS circuits, a major source of energy consumption is the switching energy caused by nodal capacitances, so reducing the supply voltage can increase the energy efficiency significantly.

Sub-threshold operation was first introduced to achieve ultralow power consumption [CC04]. However, the application of sub-threshold operation in circuits is limited by its performance degradation.

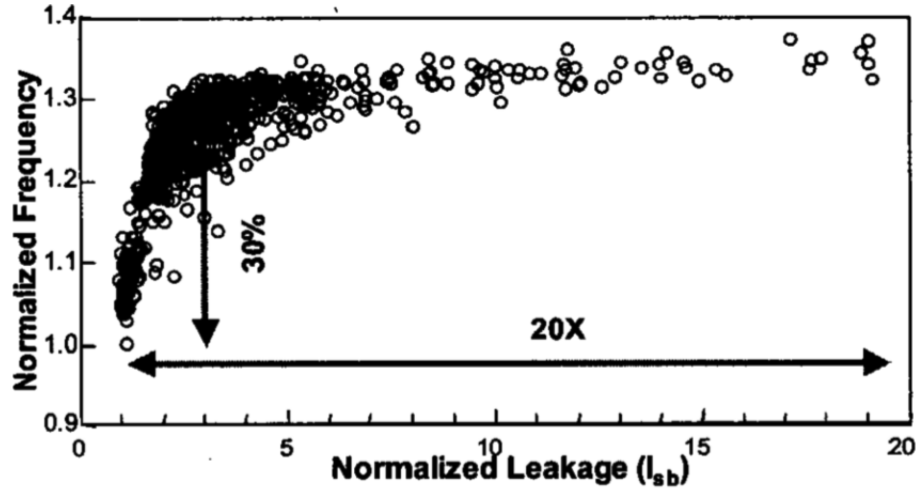

Figure 2. Leakage and frequency variations [BKN+03]

As shown in Fig. 3, the energy consumption per operation is quadratically related to the supply voltage in the super-threshold region and about 10 times larger than in the near-threshold region. In the sub-threshold region, leakage energy dominates the energy consumption, so there is only a small decrease in energy. Moreover, the delay time in the sub-threshold region increases by 50-100 times over the near-threshold region. Hence, the near-threshold region is where the supply voltage is set to the optimal value to make balanced trade-offs between energy consumption and time delay.

Near threshold computing has recently gained attention of researchers [DWB+10] [KAH+12]. Some recent work shows that near threshold operation provides higher energy efficiency [KAH+12]. However, the near threshold operation leads to some challenges, which includes performance degradation, variability, and circuit robustness. First, the reduced overdrive in gate voltage results in the performance degradation. For example, the 45-nm fan-out-of-four inverter operating with a near threshold voltage of 400 mV is ten times slower than the same inverter using a nominal supply voltage of 1.1 V [SCH+11]. Second, the variability issue becomes more pronounced in the near threshold region. In the near-threshold region, the circuit performance and reliability are more susceptible to process variation, as process variations have more impact on the drive current of the transistors.

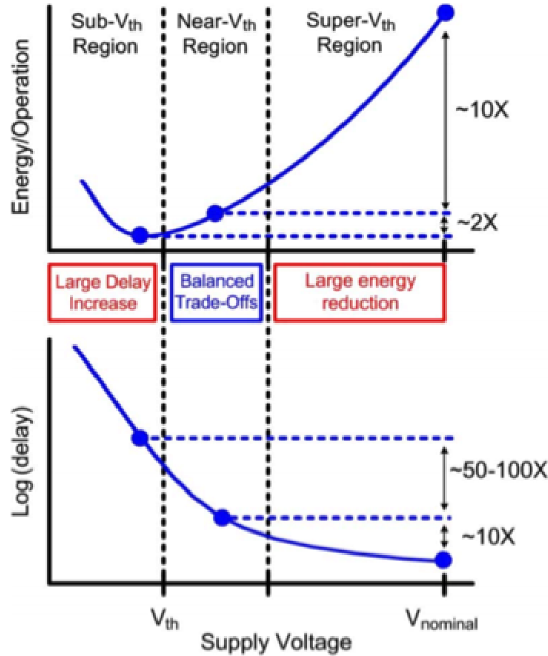

Figure 3. Energy and delay in different supply voltage operating regions [DWB+10]

For example, Fig. 4 displays the Monte Carlo simulations showing the spread of frequency at nominal voltage and near threshold voltage. The variations of frequency across fast and slow dies are two times larger at near threshold voltage.

Furthermore, the soft error reliability for near threshold operation is studied in [PCC+14]. A portable soft error reference design is implemented targeting low-voltage operation. The experiment shows that for a 6T SRAM as supply voltage scales, there is 6x increase in FIT/bit for neutron tests and 2.5x increase in FIT/bit for alpha tests [PCC+14].

D. Reliability and performance issues induced by process variations

Some recent work by other researchers shows the impact of process variations on the sensitivity of the circuit to soft errors. Kauppila et al. used a Monte Carlo method to quantify the influence of process variations on SRAM upset probability [KBK+11]. In [DLX05] by Ding et al., critical charge, one important parameter reflecting the circuits vulnerability to soft errors, is analyzed using four kinds of circuits at different technology nodes. The

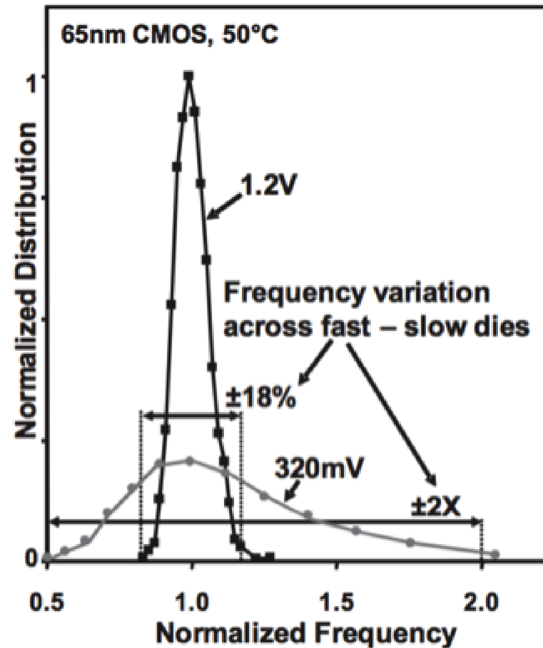

Figure 4. Frequency variations across fast and slow dies for nominal voltage and near threshold voltage [KAH+12]

simulation results show that the gate length variability is the most significant parameter, and threshold voltage must also be considered. Gate length and threshold voltage are the two parameters directly affecting the transistor drive current that most impact the critical charge [DLX05]. In [JSS09] by Jahinuzzaman et al., a compact critical charge model is introduced; this model can calculate the critical charge variability of SRAM and has good agreement with SPICE simulations [JSS09].

In [DLW+06], the 70-nm SRAM is used as benchmark circuit to study the dependence of critical charge variation on gate length variation, threshold variation, and correlation between gate lengths. Also a simple model is presented to estimate critical charge variation without Monte Carlo simulation [DLW+06].

In previous studies, most of the analyzed circuits operate at the nominal supply voltage. Some research also takes the supply voltage into account. In [MAE11] by Mostafa et al., one analytical model is developed to explain the impact of supply voltage on critical charge and its variability for a 65-nm 6T SRAM cell. The coupling capacitor is found to mitigate

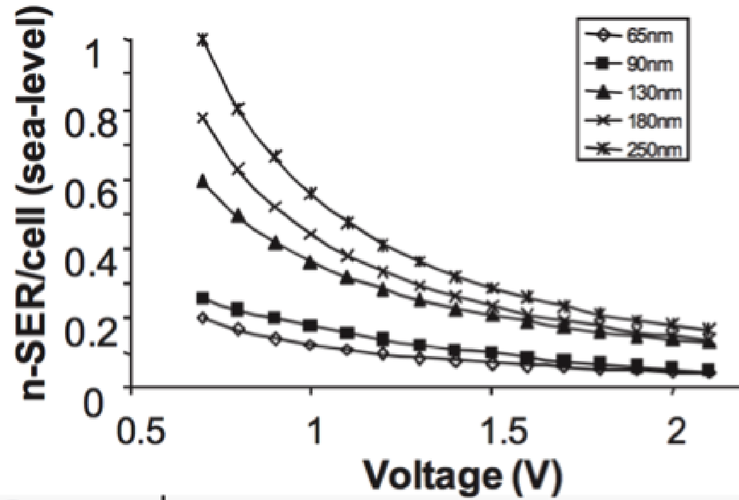

Figure 5. Soft errors increasing with reduced supply voltage [KAH+12]

the impact of process variations on critical charge variability [MAE11].

In the near-threshold region, results in Fig. 5 show that circuits are more vulnerable to soft errors. As supply voltage decreases, the soft error rate increases.

CHAPTER III

Impact of process variations on 6T SRAM in near-threshold region

In this chapter, one storage circuit is studied, which is the 6T SRAM. The critical charge, leakage power, and write delay variations caused by process variations are studied and compared for supply voltage of 1.05 V and 0.5 V.

A. Methodology

The 6T SRAM circuit is shown in Fig. 6. In order to study the response of single event effects, the particle strike on the circuit is modeled as a current source connected to the node of interest. The current source uses the Messenger's fault injection model (Double exponential current model) [Mes82]. Both a NMOS hit and an PMOS hit will be simulated for the SRAM cell.

$$I(t) = I_0(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}) \qquad \text{(III.1)}$$

In Equation III.1, I_0 is the amplitude of the current. τ_1 represents the collection time-constant of the junction, and τ_2 is the ion-track establishment time constant. This current model is used in the SPECTRE simulations in this research. The transistor simulation models used for this work are from the technology kit of the Synopsys 32-nm library [hC]. The 32-nm transistor models are implemented in Cadence SPECTRE.

In the SPECTRE circuit simulator, the Monte Carlo analysis option can be used to model the process variations like effective gate length and threshold voltage. The Monte Carlo model file defines the distribution of manufacturing parameters, which represents the real-world process variations seen in fabrication. Such a model file is usually provided by the foundry. Since there is no model file provided for 32-nm model, this model file was

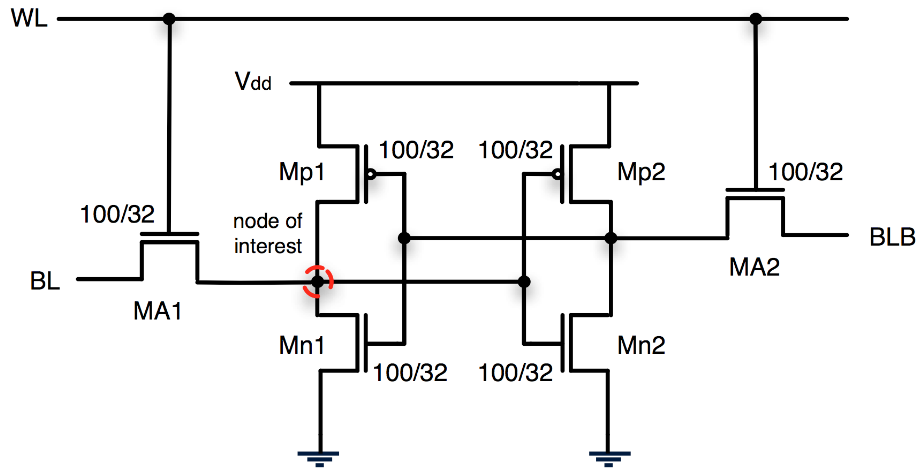

Figure 6. 6T SRAM circuit (node of interest is lableled)

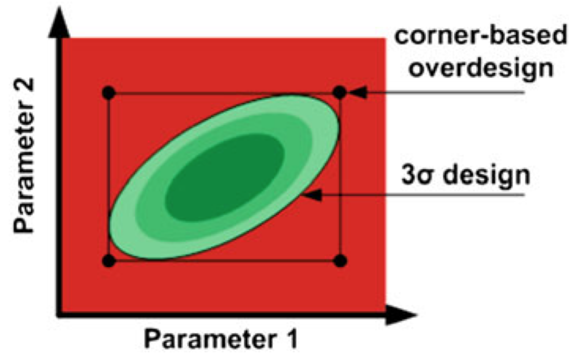

Figure 7. Process corner- based vs. 3σ design approaches [OSM]

built according to the process corners. The statistical distribution is the generalization of the process corners model. So the nominal values of process parameters are treated as the mean value of Gaussian distribution in the model file.

The worst-case process corner model leads to pessimistic designs [OSM]. As shown in Fig. 7, the x-axis and y-axis stand for the range that process parameters can vary. The area inside the ellipse is the combined range. In this area, the 3σ limits are met. The area can be modeled with statistical Monte Carlo simulations, which is more accurate than the rectangular area modeled by process corners.

The standard deviation of process parameters can be calculated using the 3-sigma rule. The 3-sigma values of the variations are shown in Table 2. The values are all based on the

Table 2. Threshold voltage and effective gate length variations for the 32-nm Synopsys library

	Threshold Voltage	Effective Gate Length
3σ	21 mV	1.2 nm

process corners in 32-nm Synopsys library.

B. Results and discussion

In the following simulations, the 32-nm technology is implemented. The number of Monte Carlo runs to determine the critical charge distribution is 1,000 for each deposited charge value. The number of Monte Carlo runs for leakage power and time delay is 10,000. The nominal supply voltage is 1.05 V.

1. Critical charge

The soft error sensitivity of an SRAM cell is determined by the following factors: (1) the critical charge, (2) the diffusion area of the sensitive drain, and (3) the charge collection efficiency [HK05]. In this section, the distribution of critical charge is analyzed. The other two factors are layout-dependent and not included in this circuit-level analysis. Both a PMOS hit and an NMOS hit are simulated.

The upset probability can be determined under process variation for different supply voltages (Fig. 8). The results in Fig. 8 (NMOS hit) are derived when all the process variations are employed in the simulations. The results of PMOS hit are shown in Fig. 9. For the curves in Fig. 8 and Fig. 9, the non-linear least square fitting can be used to calculate the mean value Q_{mean} and standard deviation σ of the critical charge distribution. Equation III.2 is used for the fitting,

$$P_{upset} = \frac{1}{2}[erf(\frac{Q_{deposit} - Q_{mean}}{\sqrt{2}\sigma}) + erf(\frac{Q_{mean}}{\sqrt{2}\sigma})] \quad \text{(III.2)}$$

where erf() is the error function.

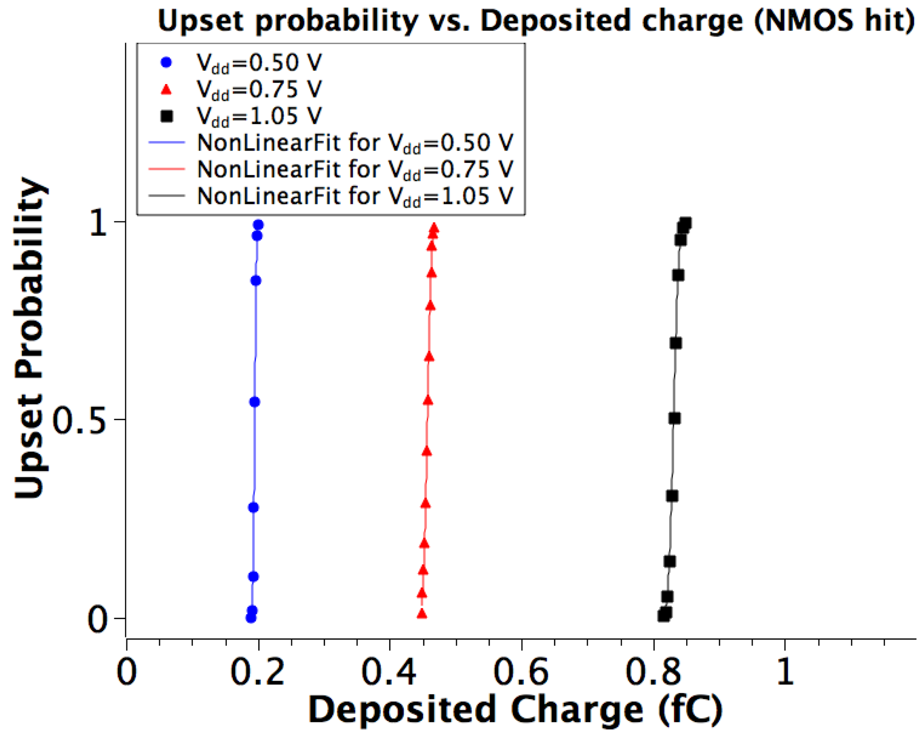

Figure 8. Impact of deposited charge on upset probability of the SRAM at different supply voltages (NMOS hit)

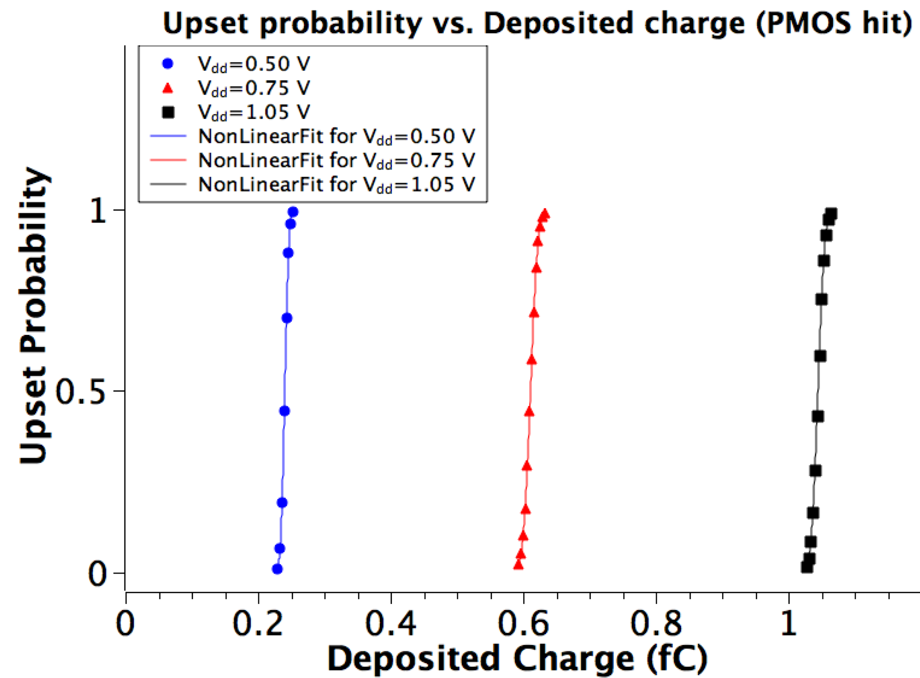

Figure 9. Impact of deposited charge on upset probability of the SRAM at different supply voltages (PMOS hit)

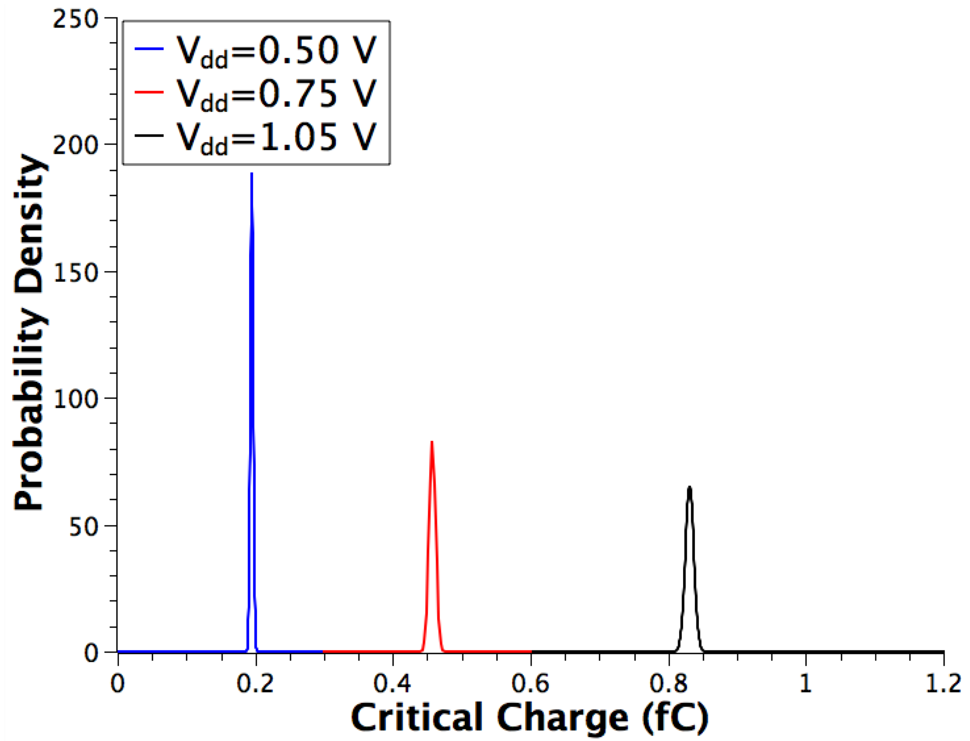

Figure 10. Critical charge distributions of different supply voltages (NMOS hit)

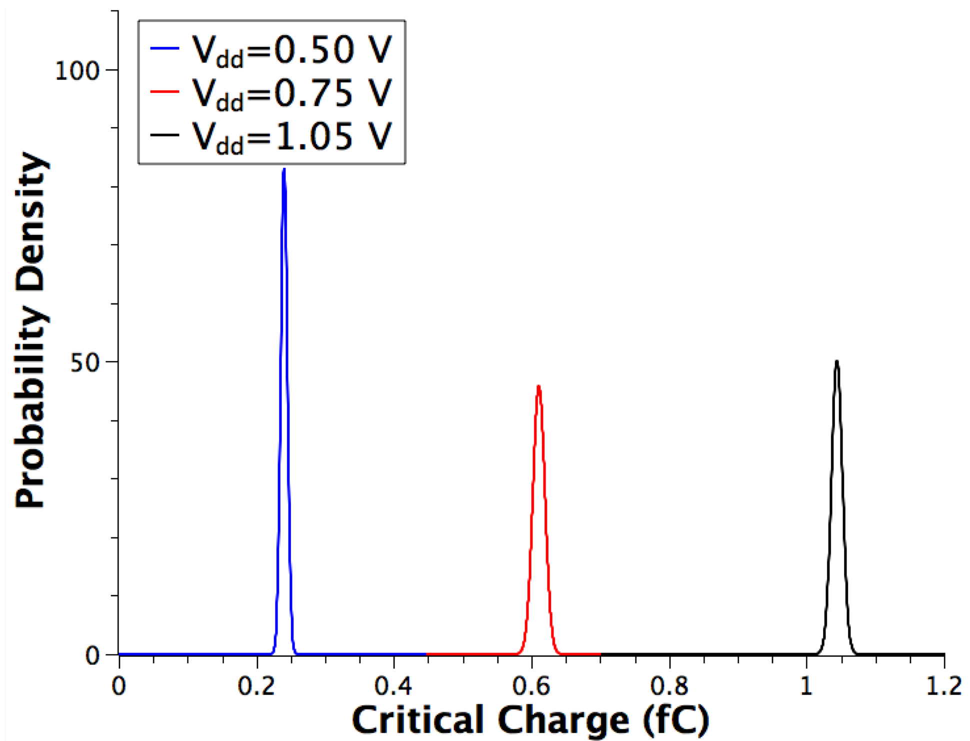

Figure 11. Critical charge distributions of different supply voltages (PMOS hit)

Table 3. Mean and relative standard deviation of critical charge of SRAM under different supply voltages (NMOS hit)

Critical Charge	Supply Voltage		
	0.5V	0.75V	1.05V
μ	0.20 fC	0.46 fC	0.83 fC
σ	0.0021 fC	0.0048 fC	0.0061 fC
σ/μ	1.08%	1.05%	0.74%

Table 4. Mean and relative standard deviation of critical charge of SRAM under different supply voltages (PMOS hit)

Critical Charge	Supply Voltage		
	0.5V	0.75V	1.05V
μ	0.24 fC	0.61 fC	1.04 fC
σ	0.0048 fC	0.0087 fC	0.0080 fC
σ/μ	2.00%	1.42%	0.76%

Fig. 10 and Fig. 11 shows the derived critical charge distribution with the fitting for both the PMOS hit and the NMOS hit. The mean value of critical charge decreases as the supply voltage decreases. Table 3 and Table 4 show that the mean critical charge decreases linearly as supply voltage decreases. Moreover, the value of σ/μ, which reflects the influence of variations (i.e., the relative standard deviation), increases as the supply voltage decreases, indicating that process variations have more impact on critical charge distribution at near-threshold voltage.

Two kinds of process variations (i.e., threshold voltage and effective gate length) are investigated separately. The same method is utilized to derive the critical charge distributions. The results are shown in Table 5-8. For the nominal supply voltage (1.05 V), threshold voltage variations induce a larger spread of critical charge when compared to effective gate length; for the near-threshold region (0.50 V), the threshold voltage variations still have more influence on the critical charge variation.

Table 5. Impact of different process variations of mean and relative standard deviation of critical charge of SRAM in near-threshold region (NMOS hit)

Critical Charge	Near-threshold Region (V_{dd}=0.50 V)	
	V_{th}	L_{eff}
μ	0.20 fC	0.20 fC
σ	0.0021 fC	0.0007 fC
σ/μ	1.05%	0.35%

Table 6. Impact of different process variations of mean and relative standard deviation of critical charge of SRAM in near-threshold region (PMOS hit)

Critical Charge	Near-threshold Region (V_{dd}=0.50 V)	
	V_{th}	L_{eff}
μ	0.24 fC	0.24 fC
σ	0.0040 fC	0.0026 fC
σ/μ	1.67%	1.08%

Table 7. Impact of different process variations of mean and relative standard deviation of critical charge of SRAM in super-threshold region (NMOS hit)

Critical Charge	Super-threshold Region (V_{dd}=1.05 V)	
	V_{th}	L_{eff}
μ	0.83 fC	0.83 fC
σ	0.0052 fC	0.0032 fC
σ/μ	0.63%	0.39%

Table 8. Impact of different process variations of mean and relative standard deviation of critical charge of SRAM in super-threshold region (PMOS hit)

Critical Charge	Super-threshold Region (V_{dd}=1.05 V)	
	V_{th}	L_{eff}
μ	1.04 fC	1.04 fC
σ	0.0062 fC	0.0060 fC
σ/μ	0.60%	0.58%

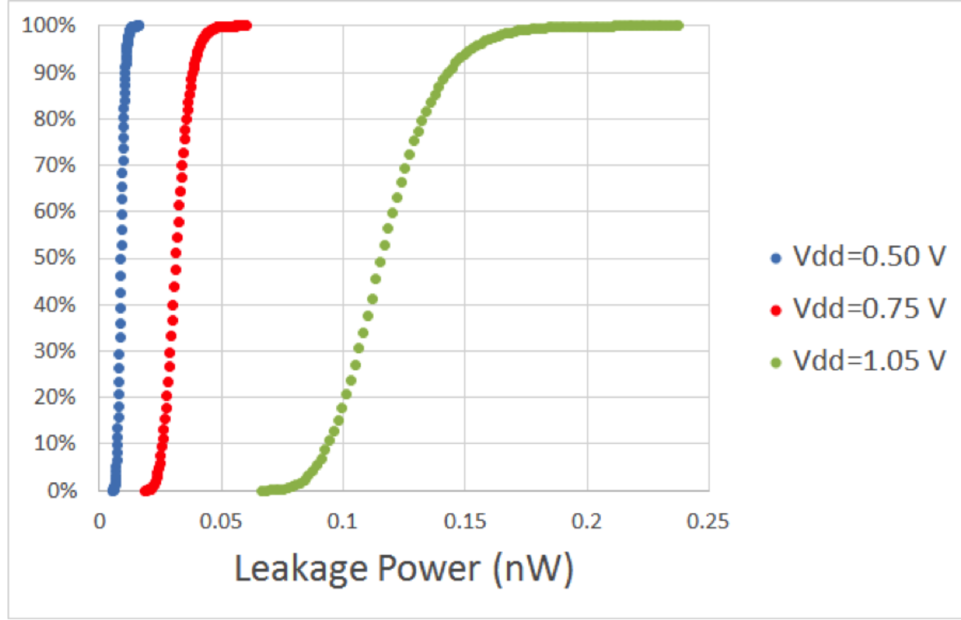

Figure 12. Impact of process variations on leakage power when V_{dd}=1.05 V, 0.75 V and 0.5 V

Table 9. Mean and relative standard deviation of leakage power of SRAM under different supply voltages

	Supply Voltage		
Leakage power	0.50V	0.75V	1.05V
μ	0.009 nW	0.032 nW	0.117 nW
σ	0.013 nW	0.0049 nW	0.0196 nW
σ/μ	14.6%	15.6%	16.7%

2. Leakage power

The leakage power of the SRAM in standby mode was calculated using OCEAN commands in SPECTRE. After 10,000 leakage power data values are obtained, the cumulative distribution function of leakage power is derived. The results are shown in Fig. 12.

From Table 9, the mean value of leakage power decreases as the supply voltage decreases. The relative standard deviation also decreases as supply voltage decreases.

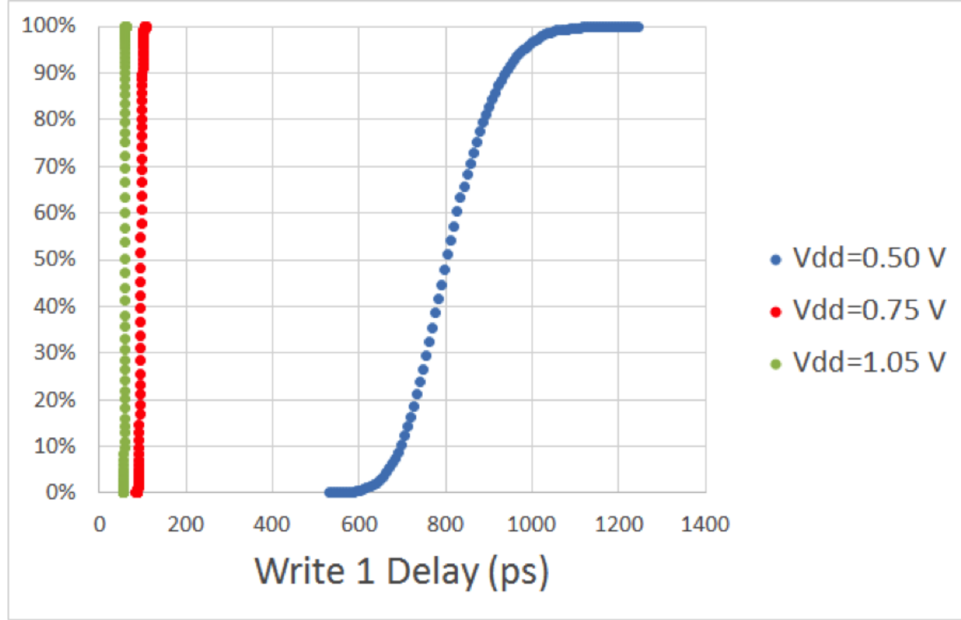

Figure 13. Impact of process variations on write 1 delay for different supply voltage

Table 10. Mean and relative standard deviation of write 1 delay time of SRAM under different supply voltages

	Supply Voltage		
Write 1 delay	0.50V	0.75V	1.05V
μ	811.05 ps	96.45 ps	58.87 ps
σ	95.14 ps	3.01 ps	0.76 ps
σ/μ	11.7%	3.1%	1.3%

3. Write delay

The write delay was examined while associated with operating within the near-threshold region. As shown in Fig. 13 and Fig. 14, different supply voltages cause different cumulative distribution functions of write 1 delay time and write 0 delay time.

From Table 10 and Table 11, it can be concluded that near threshold operation has a greater impact on the write time delay. In the near-threshold region (Vdd=0.50 V), the write delays (i.e., write 1 delay and write 0 delay) are significantly increased. In addition, the values of σ/μ due to process variations are much larger in the near-threshold region. At this supply voltage, the SRAM would incur a significant timing penalty, which might

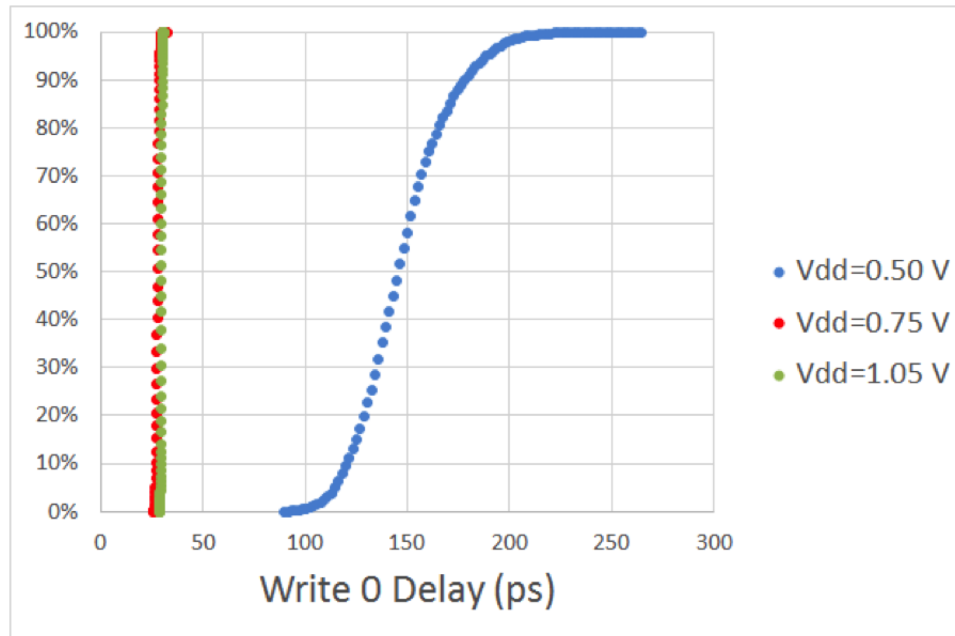

Figure 14. Impact of process variations on write 0 delay for different supply voltage

Table 11. Mean and relative standard deviation of write 0 delay time of SRAM under different supply voltages

	Supply Voltage		
Write 0 delay	0.50V	0.75V	1.05V
μ	147.59 ps	27.89 ps	29.62 ps
σ	22.45 ps	0.70 ps	0.28 ps
σ/μ	15.2%	2.5%	1.0%

make it difficult to use within a typical cache structure. On the other hand, the mean delays as well as σ/μ for Vdd=0.75 V and Vdd=1.05 V are very close.

C. Proposed solutions for solving the reliability issues

In this thesis, the derived critical charge distribution results can be used to quantitively evaluate the soft error sensitivity and impact of process variations of the circuits, especially in the near-threshold region. Therefore the results will be helpful in the redesign of the SRAM cell to achieve a better performance/cost ratio as well as reliability in the near-threshold region. It is possible that other topologies of SRAM can mitigate the influence of process variations. In [CMN+08], an 8T SRAM cell is proposed that can provide high variability tolerance compared to the 6T SRAM cell without much area penalty [CMN+08]. In [JRS09], a quad-node ten-transistor SRAM cell is proposed. The new SRAM cell significantly reduces soft error rate and achieves high SNM at a lower supply voltage [JRS09].

In previous research, the critical charge has been shown to be directly affected by parameters like gate length, gate width, and threshold voltage, because these parameters have an influence on transistor drive current [DM03]. To be specific, the increase of gate length reduces the parasitic bipolar gain and thus increases the critical charge. Also, the struck device in the SRAM has more impact on the critical charge than other devices in SRAM [CKK+08]. So, another solution to mitigate the reliability issue is to update the internal design ratios within the SRAM cell. The optimization of the ratios will result in higher critical charge and make the SRAM cell more reliable.

D. Summary and future work

In this chapter, the impact of process variations on 6T SRAM operating in near threshold region is investigated. The soft error sensitivity, leakage power, and write time delay of the circuit are studied. The SRAM circuit is simulated in SPECTRE using 32-nm model.

The simulation results show that the threshold voltage variations have more impact on the spread of the critical charge in the near-threshold region and nominal supply voltage

than effective gate length variations. The leakage power is greatly reduced in the near-threshold region as expected. However, the values of σ/μ for leakage power do not have much difference for the near-threshold region and the super-threshold region. So the impact of process variations on leakage power does not change much in the near-threshold region. Finally, the write time delays are explored. The results show that in the near-threshold region, both the mean value and σ/μ of the time delay are greatly increased compared to super threshold region. The related results are listed in Table 12.

In the future, a more accurate single-event current model can be used for particle strikes. In addition, layout-based analysis of the impact of process variation on the SRAM soft error vulnerability will be made.

Table 12. Results for 6T SRAM cell operating at the near-threshold region compared to the nominal supply voltage for 32-nm Synopsys library [hC]

	6T SRAM
Critical Charge (Q_{crit})	• Reduction of 77% for Q_{crit} for both NMOS and PMOS hits. • 1.5 times larger variation for Q_{crit} of the NMOS hit; 2.7 times larger variation for Q_{crit} of the PMOS hit.
Leakage power	• Reduction of 92% for leakage power • Almost same leakage power variation.
Performance	• 5.0 times larger Write 0 delay; 13.7 times larger write 1 delay. • 15.2 times larger variation for write 0 delay; 9.0 times larger variation for write 1 delay.

CHAPTER IV

Impact of process variations on critical charge of flip-flops in near-threshold region

In this chapter, two kinds of flip-flops are analyzed: the transmission gate flip-flop and the C^2MOS (clocked CMOS) flip-flop [MNB01]. The schematics of the two flip-flops are shown in Fig. 15 and Fig. 16. The circuits are implemented and simulated in SPECTRE with the 32-nm model.

In the following sections, the critical charge of the circuits is the major parameter of focus, which is related to the soft error sensitivity of the circuits. The nodes of interest are marked on the schematics in Fig. 15 and Fig. 16. The same method used in Chapter III will be implemented for the flip-flops. The particle strike is modeled in the SPECTRE as a double exponential current source, which is connected to the node of interest. The function of the current is shown in Equation III.1.

A. Transmission gate flip-flop

1. Critical charge

For the transmission gate flip-flop, the node connected to the input of the last inverter is investigated. Fig. 17 and Fig. 18 indicate the relationship between deposited charge and upset probability at different supply voltages for both the NMOS hit and PMOS hit.

With the same fitting used in the previous chapter, the distribution of the critical charge is derived. In Fig. 19 and Fig. 20, the critical charge distributions at both the near-threshold and the super-threshold regions are compared for both the NMOS hit and the PMOS hit. Table 13 and Table 14 show that the σ/μ value is almost the same in both near-threshold region and super-threshold region, which indicates that the process variations have almost the same influence on the critical charge variations at different supply voltages.

Also, the influences of threshold voltage and effective gate length variations are inves-

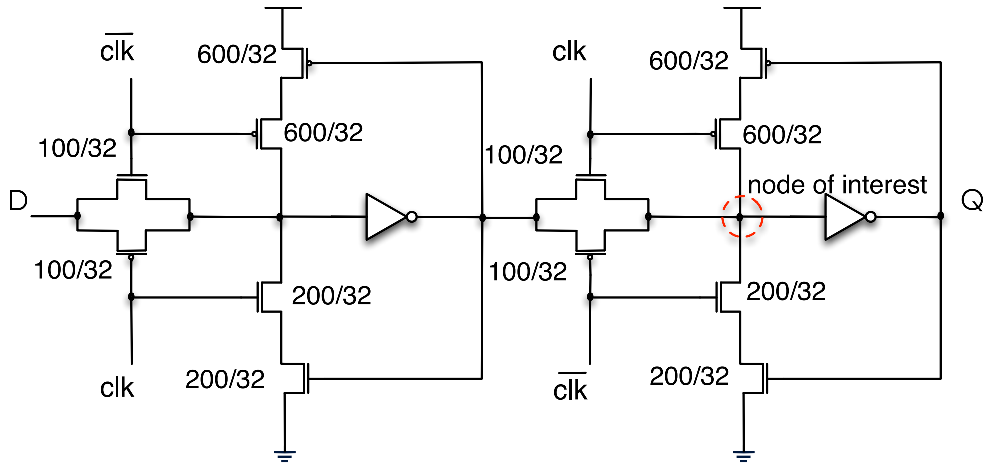

Figure 15. Transmission gate flip-flop schematic

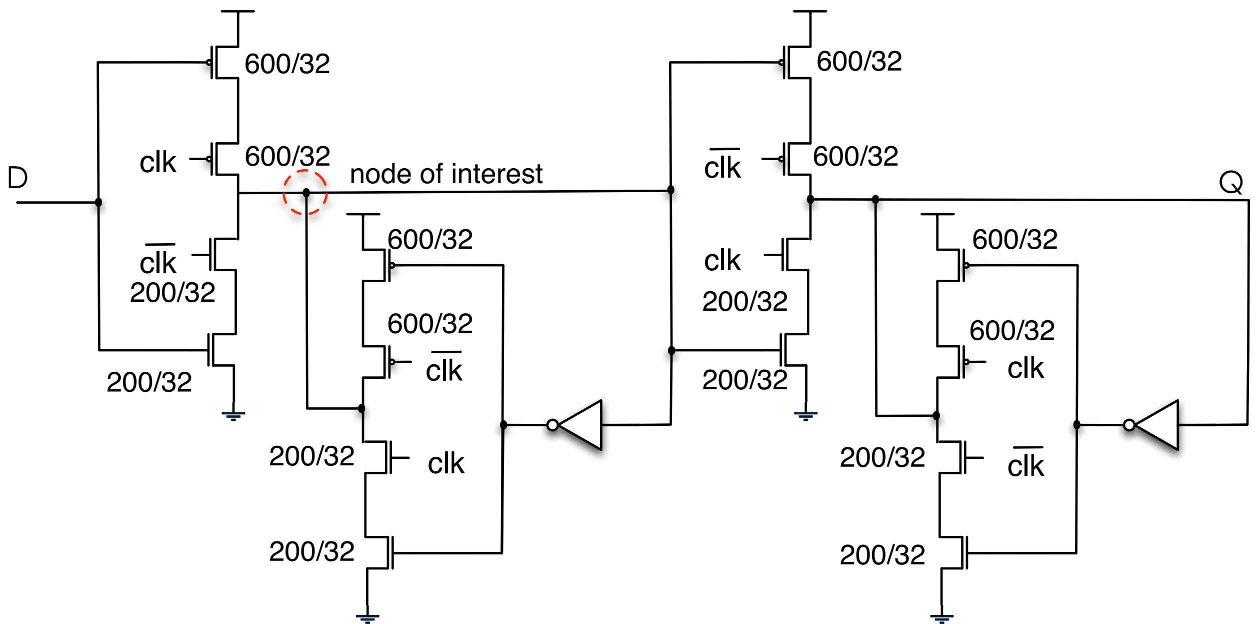

Figure 16. C^2MOS flip-flop schematic

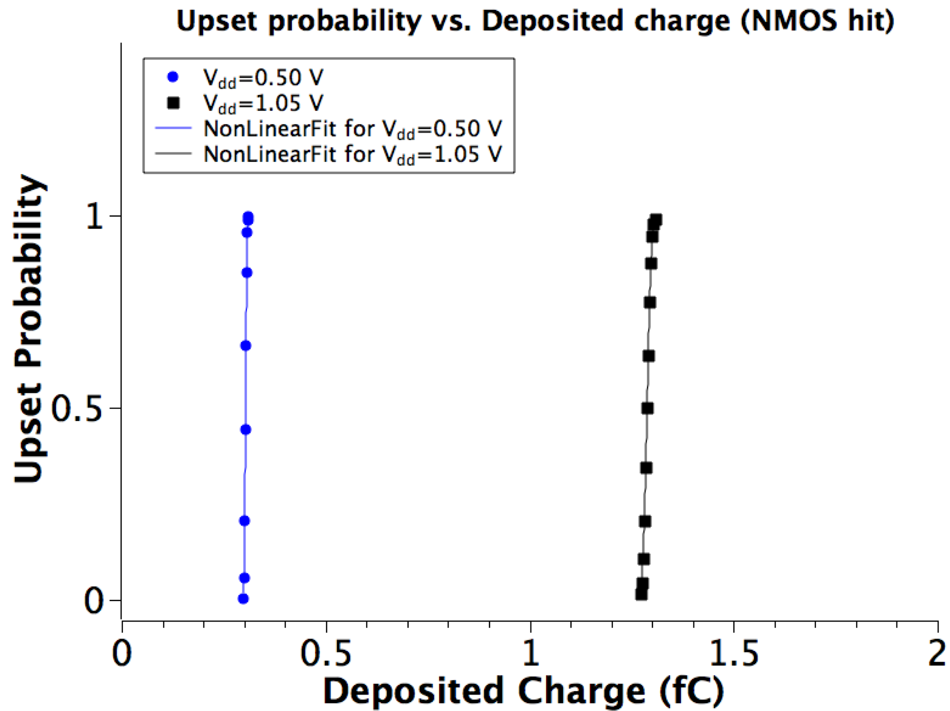

Figure 17. Impact of deposited charge on upset probability of the transmission gate flip-flop at different supply voltages (NMOS hit)

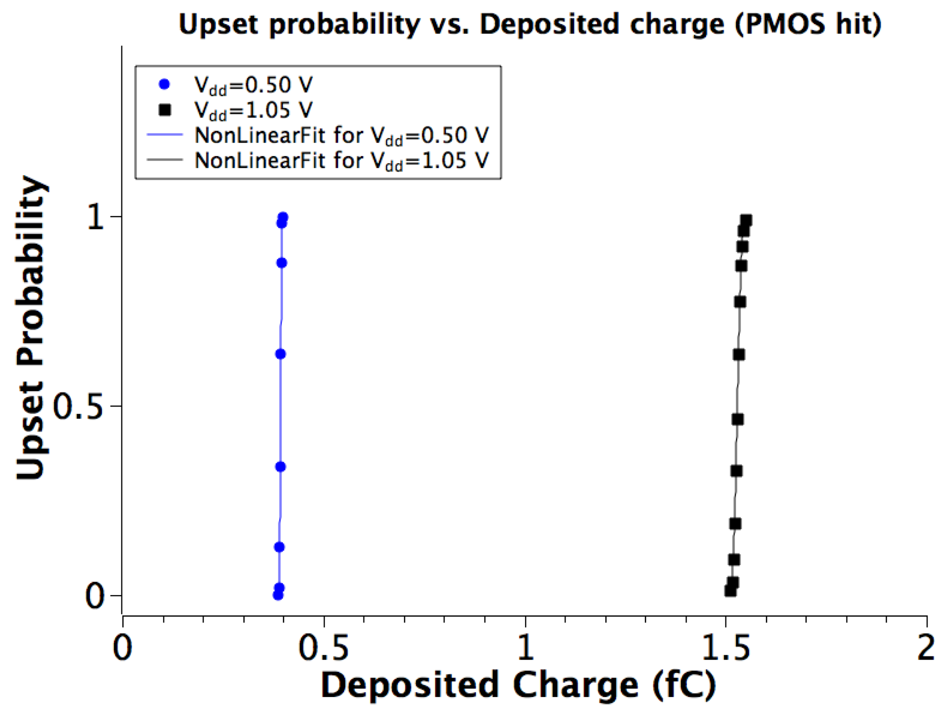

Figure 18. Impact of deposited charge on upset probability of the transmission gate flip-flop at different supply voltages (PMOS hit)

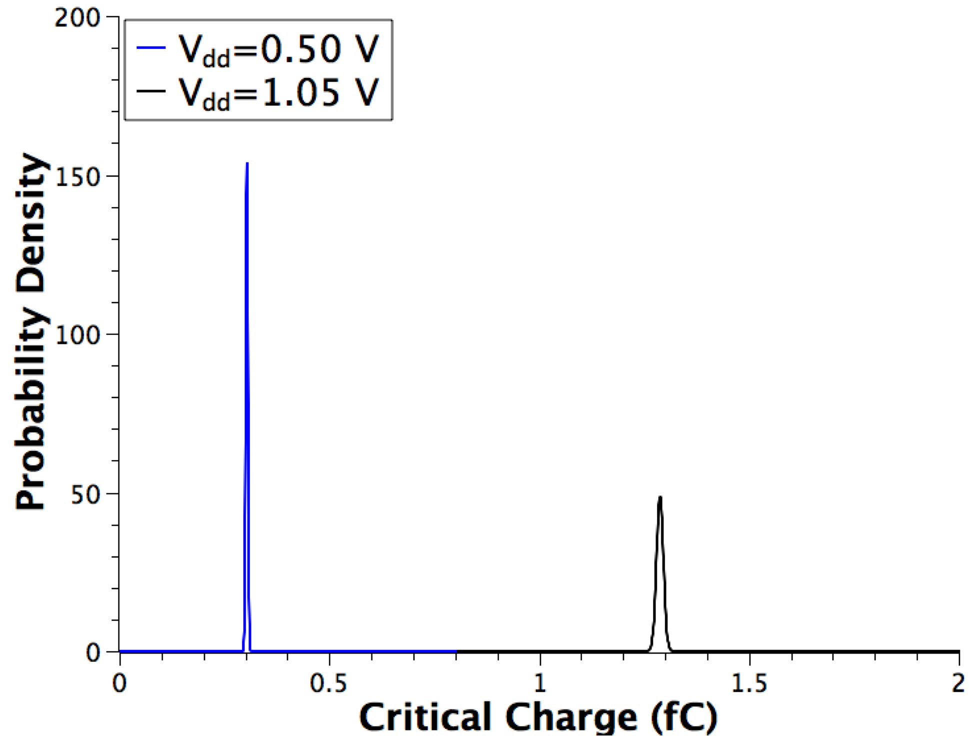

Figure 19. Critical charge distributions of different supply voltages for the transmission gate flip-flop (NMOS hit)

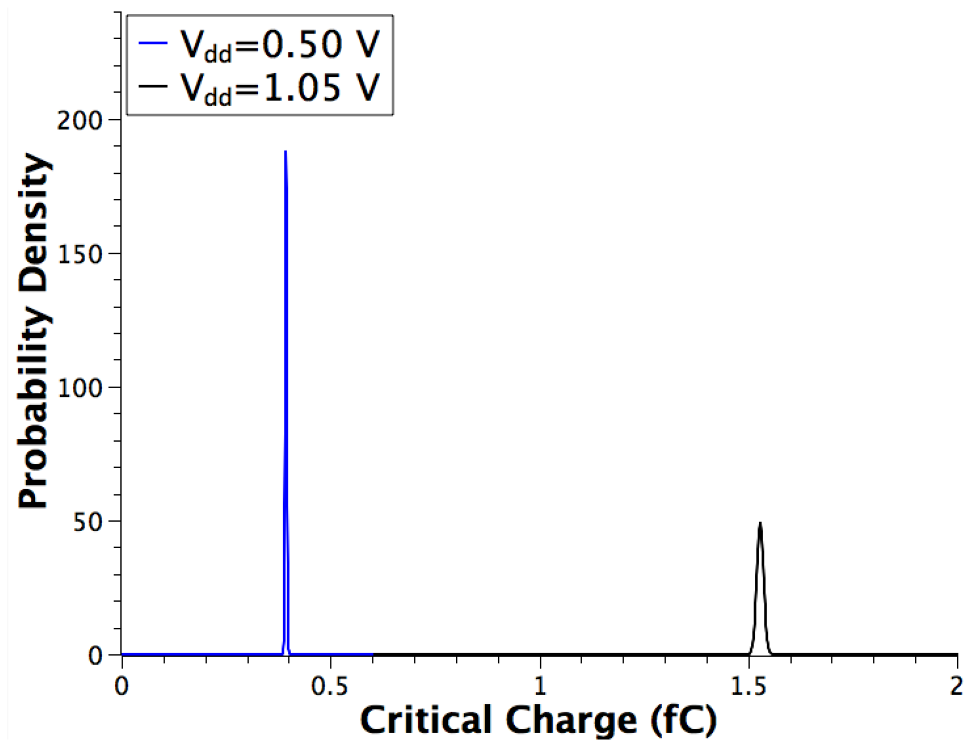

Figure 20. Critical charge distributions of different supply voltages for the transmission gate flip-flop (PMOS hit)

Table 13. Mean and relative standard deviation of critical charge of transmission gate flip-flop under different supply voltages (NMOS hit)

	Supply Voltage	
Critical Charge	0.50V	1.05V
μ	0.30 fC	1.29 fC
σ	0.0026 fC	0.0082 fC
σ/μ	0.85%	0.63%

Table 14. Mean and relative standard deviation of critical charge of transmission gate flip-flop under different supply voltages (PMOS hit)

	Supply Voltage	
Critical Charge	0.50V	1.05V
μ	0.40 fC	1.53 fC
σ	0.0021 fC	0.0081 fC
σ/μ	0.53%	0.53%

tigated separately. The μ and σ of the critical charge distribution for the NMOS hit is shown in Table 15 and Table 17. The μ and σ of the critical charge distribution for the PMOS hit is shown in Table 16 and Table 18. For the transmission gate flip-flop, the effective gate length variations have greater influence on the critical charge variations at both near-threshold voltage and super-threshold voltage.

Table 15. Impact of different process variations on mean and relative standard deviation of critical charge of transmission gate flip-flop in super-threshold region (NMOS hit)

	Super-threshold Region (V_{dd}=1.05 V)	
Critical Charge	V_{th}	L_{eff}
μ	1.29 fC	1.29 fC
σ	0.0083 fC	0.0016 fC
σ/μ	0.64%	0.12%

Table 16. Impact of different process variations on mean and relative standard deviation of critical charge of transmission gate flip-flop in super-threshold region (PMOS hit)

Critical Charge	Super-threshold Region (V_{dd}=1.05 V)	
	V_{th}	L_{eff}
μ	1.53 fC	1.53 fC
σ	0.0067 fC	0.0049 fC
σ/μ	0.44%	0.32%

Table 17. Impact of different process variations on mean and relative standard deviation of critical charge of transmission gate flip-flop in near-threshold region (NMOS hit)

Critical Charge	Near-threshold Region (V_{dd}=0.50 V)	
	V_{th}	L_{eff}
μ	0.30 fC	0.30 fC
σ	0.0026 fC	0.0004 fC
σ/μ	0.87%	0.13%

Table 18. Impact of different process variations on mean and relative standard deviation of critical charge of transmission gate flip-flop in near-threshold region (PMOS hit)

Critical Charge	Near-threshold Region (V_{dd}=0.50 V)	
	V_{th}	L_{eff}
μ	0.39 fC	0.39 fC
σ	0.0019 fC	0.0008 fC
σ/μ	0.49%	0.21%

Table 19. Mean and relative standard deviation of leakage power of transmission gate flip-flop under different supply voltages

	Supply Voltage	
Leakage power	0.50V	1.05V
μ	0.061 nW	2.343 nW
σ	0.012 nW	0.539 nW
σ/μ	19.7%	23.0%

2. Leakage power

Leakage power of the transmission gate flip-flop is measured in SPECTRE. As the leakage power of flip-flop is state dependent, the following simulations are performed under the state (D=1, clk=1, and Q=0).

The results are shown in Table 19. The leakage power of the near-threshold region is greatly reduced compared to the nominal supply voltage. The relative standard variation of leakage power decreases as the supply voltage decreases.

3. Clock-to-output delay

The clock-to-output delay was measured in SPECTRE for both the near-threshold supply voltage and the nominal supply voltage (Q is from low to high). The results are displayed in Table 20.

It is concluded that the delay time increases dramatically as the flip-flop operates in the near-threshold region. Moreover, the delay variation is greatly increased for the near-threshold operation, which means the flip-flop is much more sensitive to the process variations in near-threshold region.

B. C^2MOS flip-flop

1. Critical charge

The C^2MOS flip-flop is studied in this section. The node of interest is shown in Fig. 16. Fig. 21 and Fig. 22 show the upset probability versus deposited charge curves at different

Table 20. Mean and relative standard deviation of clock-to-output delay of transmission gate flip-flop under different supply voltages

Clock-to-output delay	Supply Voltage	
	0.50V	1.05V
μ	3351.09 ps	57.06 ps
σ	403.77 ps	1.50 ps
σ/μ	12.0%	2.6%

Table 21. Mean and relative standard deviation of critical charge of C^2MOS flip-flop under different supply voltages (NMOS hit)

Critical Charge	Supply Voltage	
	0.50V	1.05V
μ	0.55 fC	1.73 fC
σ	0.0038 fC	0.0070 fC
σ/μ	0.68%	0.40%

supply voltage for both the NMOS hit and the PMOS hit. After fitting, the σ and μ of the critical charge distribution are derived, and the probability density functions of the critical charge distribution are plotted in Fig. 23 and Fig. 24. The parameters of the critical charge distributions are shown in Table 21 and Table 22, from which it can be seen that the process variations under near-threshold voltage and the super-threshold voltage have almost the same influence on the relative standard deviation value of critical charge.

In addition, the influence of different parameter variations is explored, and the results shown in Table 23 and Table 25 are for NMOS hit while the results in Table 24 and Table 26 are for the PMOS hit. It can be concluded that in the super-threshold region, the threshold voltage variation is the dominant factor affecting the critical charge variation. In the near-threshold region, threshold voltage variation is also a much more important factor than the effective gate length variation.

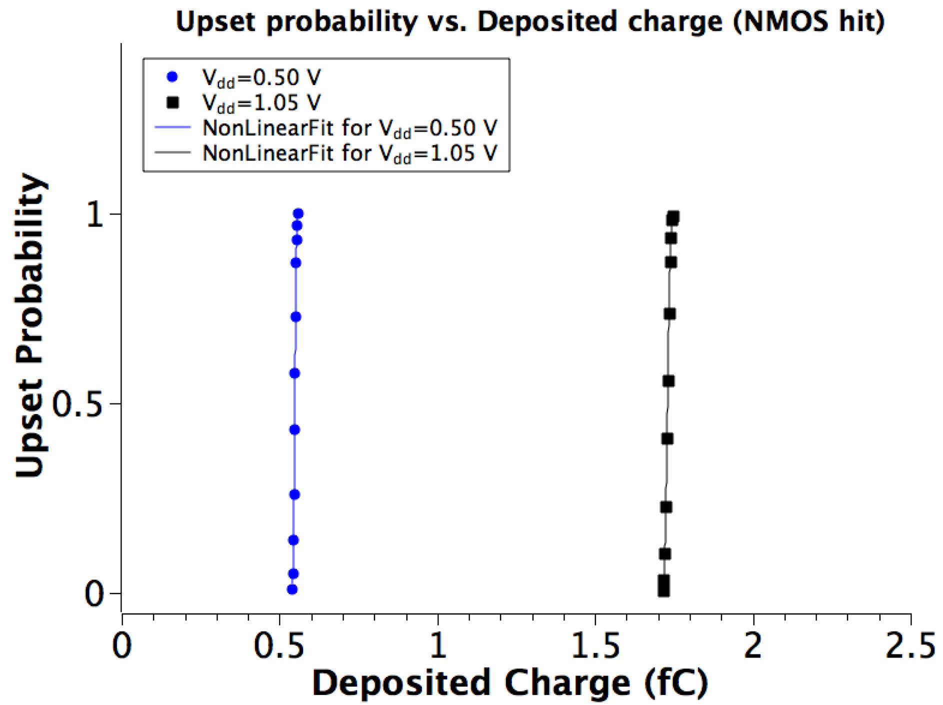

Figure 21. Impact of deposited charge on upset probability of the C^2MOS flip-flop at different supply voltages (NMOS hit)

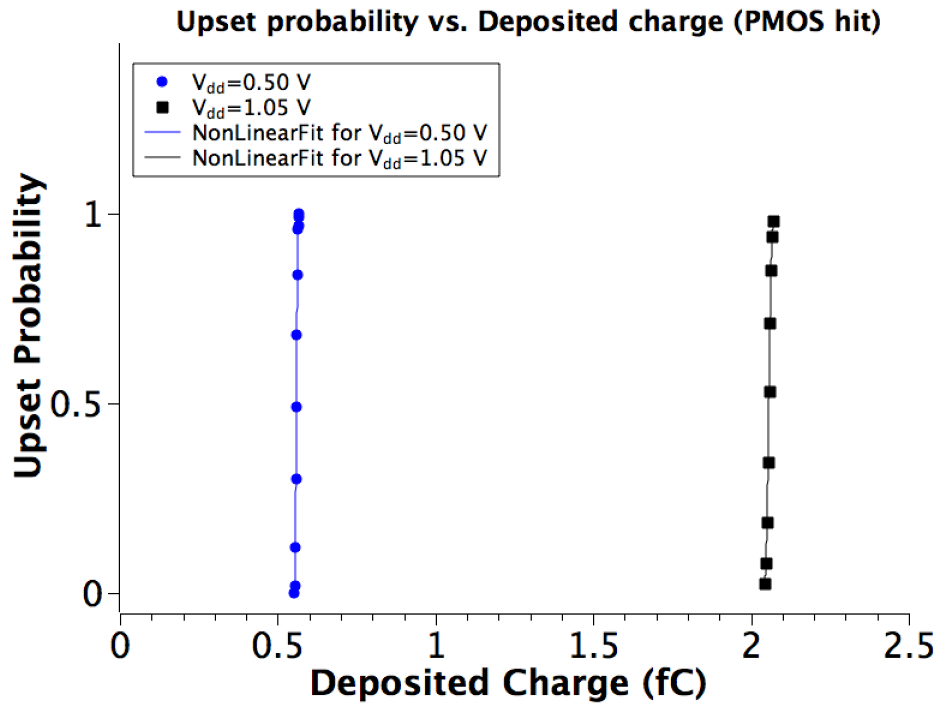

Figure 22. Impact of deposited charge on upset probability of the C^2MOS flip-flop at different supply voltages (PMOS hit)

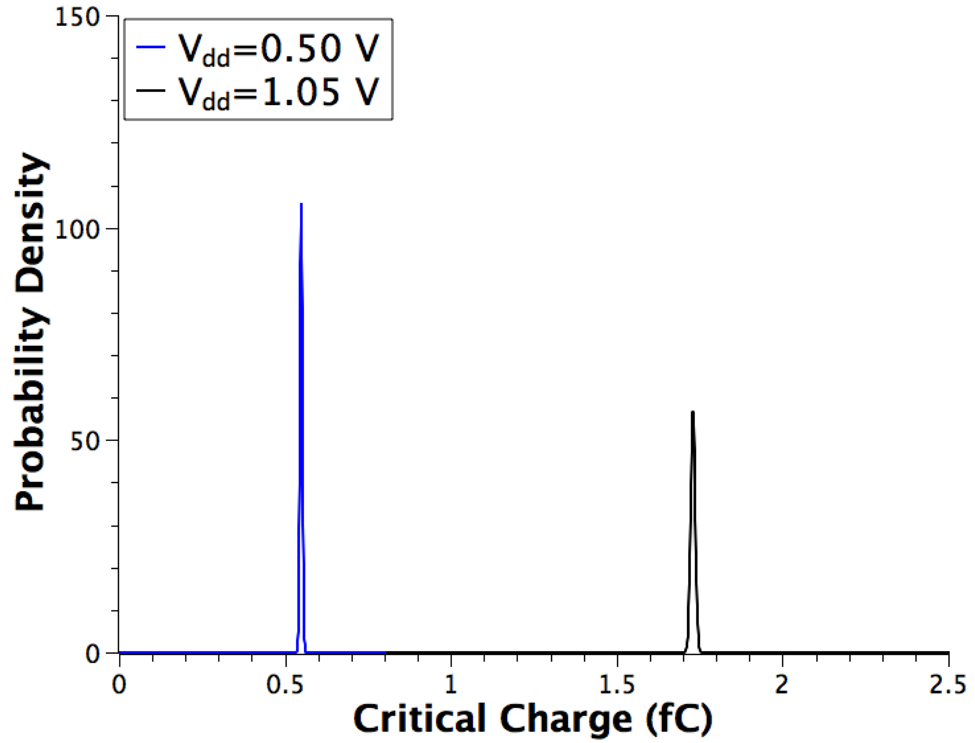

Figure 23. Critical charge distributions of different supply voltages for the C^2MOS flip-flop (NMOS hit)

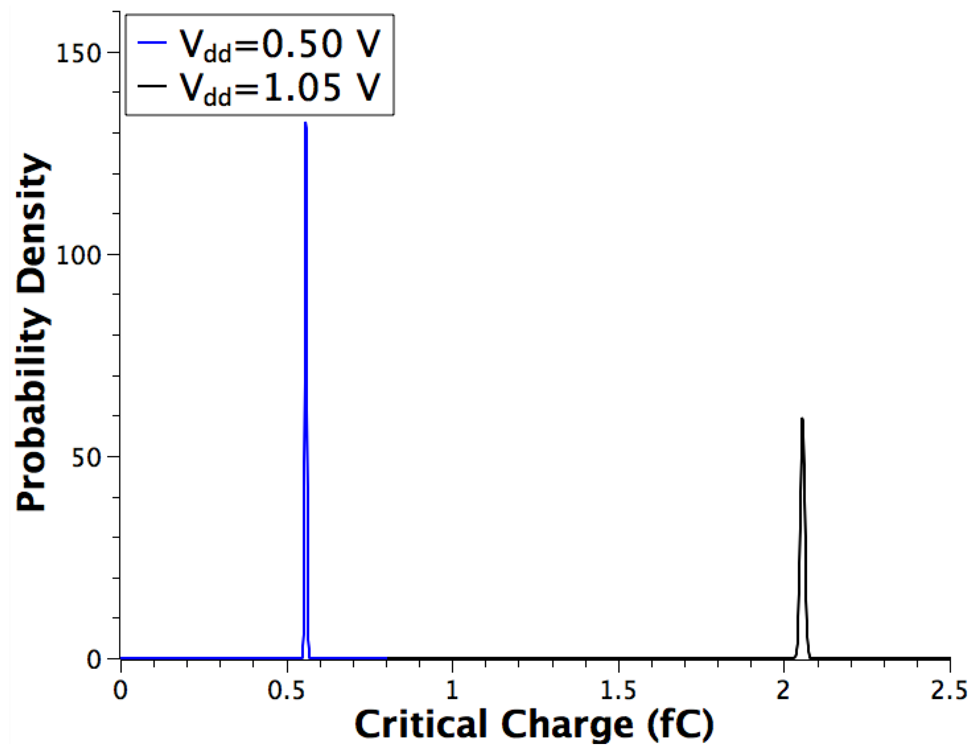

Figure 24. Critical charge distributions of different supply voltages for the C^2MOS flip-flop (PMOS hit)

Table 22. Mean and relative standard deviation of critical charge of C^2MOS flip-flop under different supply voltages (PMOS hit)

	Supply Voltage	
Critical Charge	0.50V	1.05V
μ	0.56 fC	2.06 fC
σ	0.0030 fC	0.0067 fC
σ/μ	0.54%	0.33%

Table 23. Impact of different process variations on mean and relative standard deviation of critical charge of C^2MOS flip-flop in super-threshold region (NMOS hit)

	Super-threshold Region (V_{dd}=1.05 V)	
Critical Charge	V_{th}	L_{eff}
μ	1.73 fC	1.73 fC
σ	0.0066 fC	0.0032 fC
σ/μ	0.38%	0.18%

Table 24. Impact of different process variations on mean and relative standard deviation of critical charge of C^2MOS flip-flop in super-threshold region (PMOS hit)

	Super-threshold Region (V_{dd}=1.05 V)	
Critical Charge	V_{th}	L_{eff}
μ	2.06 fC	2.06 fC
σ	0.0067 fC	0.0019 fC
σ/μ	0.33%	0.09%

Table 25. Impact of different process variations on mean and relative standard deviation of critical charge of C^2MOS flip-flop in near-threshold region (NMOS hit)

	Near-threshold Region (V_{dd}=0.50 V)	
Critical Charge	V_{th}	L_{eff}
μ	0.55 fC	0.55 fC
σ	0.0031 fC	0.0020 fC
σ/μ	0.56%	0.36%

Table 26. Impact of different process variations on mean and relative standard deviation of critical charge of C^2MOS flip-flop in near-threshold region (PMOS hit)

	Near-threshold Region (V_{dd}=0.50 V)	
Critical Charge	V_{th}	L_{eff}
μ	0.56 fC	0.56 fC
σ	0.0022 fC	0.0015 fC
σ/μ	0.39%	0.27%

Table 27. Mean and relative standard deviation of leakage power of C^2MOS flip-flop under different supply voltages

	Supply Voltage	
Leakage power	0.50V	1.05V
μ	0.081 nW	1.416 nW
σ	0.014 nW	0.484 nW
σ/μ	17.6%	34.2%

2. Leakage power

Leakage power of the C^2MOS flip-flop is measured in SPECTRE. As the leakage power of the flip-flop is state dependent, the following simulations are performed under the state (D=1, clk=1, and Q=0).

The results are shown in Table 27. The leakage power of the near-threshold region is greatly reduced compared to the nominal supply voltage. The relative standard variation of leakage power decreases as the supply voltage decreases.

3. Clock-to-output delay

The clock-to-output delay was measured in SPECTRE for both the near-threshold supply voltage and the nominal supply voltage (Q is from low to high). The results are displayed in Table 28.

It is concluded that the delay time increases dramatically as the flip-flop operates in near-threshold region. Moreover, the delay variation is greatly increased for the near-threshold operation, which means the flip-flop is much more sensitive to the process varia-

Table 28. Mean and relative standard deviation of clock-to-output delay of C^2MOS flip-flop under different supply voltages

	Supply Voltage	
Clock-to-output delay	0.50V	1.05V
μ	612.12 ps	11.25 ps
σ	92.65 ps	0.25 ps
σ/μ	15.1%	2.9%

tions in near-threshold region.

C. Summary

In this chapter, the transmission gate flip-flop and the C^2MOS flip-flop are studied. The impact of process variations on the critical charge distributions in near-threshold region is investigated. The different effects of threshold voltage variations and effective gate length variations are examined. Compared to the nominal supply voltage, near threshold voltage operation has a lower critical charge value and almost the same σ/μ value.

From the simulation results, for transmission gate flip-flop, the threshold voltage variations have more influence on critical charge variations at both near-threshold voltage and super-threshold voltage than the effective gate length variations. Furthermore, for the C^2MOS flip-flop, the threshold voltage variations also have more impact on critical charge variations when the supply voltage is 1.05 V and 0.50 V. In conclusion, the reduced supply voltage reduces the critical charge value, but does not have much effect on the σ/μ value.

The leakage power for both flip-flops decreases dramatically as the supply voltage decreases. In addition, the leakage power variations decrease when the supply voltage decreases.

The clock-to-output delay for both flip-flops increases significantly as the supply voltage decreases. Furthermore, the delay variations are also much larger while operating in near-threshold region.

The related results are listed in Table 29.

Table 29. Results for flip-flops operating at the near-threshold region compared to the nominal supply voltage for 32-nm Synopsys library [hC]

	Transmission Gate Flip-flop	C^2MOS (Clocked CMOS) Flip-flop
Critical Charge (Q_{crit})	• Reduction of 76% for Q_{crit} of the NMOS hit; Reduction of 75% for Q_{crit} of the PMOS hit. • Almost same Q_{crit} variation for both NMOS and PMOS hits.	• Reduction of 69% for Q_{crit} of the NMOS hit; Reduction of 73% for Q_{crit} of the PMOS hit. • Almost same Q_{crit} variation for both NMOS and PMOS hits.
Leakage power	• Reduction of 97% for leakage power • 13% reduction for leakage power variation.	• Reduction of 94% for leakage power • 49% reduction for leakage power variation.
Performance	• 58.8 times larger clock-to-output delay. • 4.6 times larger clock-to-output delay variation.	• 69.6 times larger clock-to-output delay. • 5.2 times larger clock-to-output delay variation.

CHAPTER V

Conclusion

In this thesis, several storage element circuits are investigated, including the 6T SRAM and two kinds of flip-flops. The double exponential current model is used to simulate the particle strike on the node of interest. The Monte Carlo method is used to model the process variations introduced in the devices. As technology scales, the importance of the process variations increases. So the impact of the process variations on single event upset response of the circuits has gained much attention of the researchers. On the other hand, in order to reduce power consumption of circuits, near threshold computing is introduced to provide higher energy efficiency while causing performance degradation.

This work explores the influence of the process variations on circuits at near threshold supply voltage. Two most important parameters are included in the chapters: threshold voltage and effective gate length.

In the thesis, the critical charge distributions are derived with σ and μ, which are from the nonlinear fitting of the upset probability versus the deposited charge curve. The σ/μ value reflects the significance of the variations.

As expected, the reduced supply voltage causes the critical charge of the circuits to reduce linearly. For each deposited charge level, 1,000 Monte Carlo runs are implemented. The results indicate that the critical charge variations of the 6T SRAM induced by process variations are more significant at near-threshold supply voltage than nominal supply voltage. In addition, as the supply voltage changes from 1.05 V to 0.50 V, 92% of the leakage power for the SRAM is saved. The write delay time of the SRAM increases dramatically as the supply voltage decreases. The write delay variations also increases a lot (Write 0 delay variation increases by a factor of 15.2 while write 1 delay variation increases by a factor of 9) when operating in near-threshold region. For the two flip-flops, the reduced

supply voltage has little impact on the critical charge variation induced by process variations. However, the clock-to-output delay is much more sensitive to the process variations as the supply voltage decreases.

To be specific, the effects of different process variations are different: the threshold voltage variations have more impact on the critical charge variations of 6T SRAM at near-threshold region as well as super-threshold voltage; as for the transmission gate flip-flop, the threshold voltage variations are also the dominant factor to critical charge variations for both near-threshold and super-threshold supply voltage; the critical charge variations of C^2MOS flip-flop are affected more by threshold voltage variations at different supply voltages.

REFERENCES

[Bau05] R.C. Baumann. Radiation-induced soft errors in advanced semiconductor technologies. *IEEE Transactions on Device and Materials Reliability*, 5(3):305–316, 2005.

[BCSS08] D. Blaauw, K. Chopra, A. Srivastava, and L. Scheffer. Statistical timing analysis: From basic principles to state of the art. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(4):589–607, April 2008.

[BKN+03] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De. Parameter variations and impact on circuits and microarchitecture. In *Proceedings of Design Automation Conference, 2003*, pages 338–342, 2003.

[CC04] B.H. Calhoun and A. Chandrakasan. Characterizing and modeling minimum energy operation for subthreshold circuits. In *Proceedings of the 2004 International Symposium on Low Power Electronics and Design*, pages 90–95, 2004.

[CFM+10] L. Chang, D.J. Frank, R.K. Montoye, S.J. Koester, B.L. Ji, P.W. Coteus, R.H. Dennard, and W. Haensch. Practical strategies for power-efficient computing technologies. *Proceedings of the IEEE*, 98(2):215–236, 2010.

[CKK+08] E.H. Cannon, A. KleinOsowski, R. Kanj, D.D. Reinhardt, and R.V. Joshi. The impact of aging effects and manufacturing variation on SRAM soft-error rate. *IEEE Transactions on Device and Materials Reliability*, 8(1):145–152, March 2008.

[CMN+08] L. Chang, R.K. Montoye, Y. Nakamura, K.A. Batson, R.J. Eickemeyer, R.H. Dennard, W. Haensch, and D. Jamsek. An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches. *IEEE Journal of Solid-State Circuits*, 43(4):956–963, April 2008.

[DLW+06] Qian Ding, Rong Luo, Hui Wang, Huazhong Yang, and Yuan Xie. Modeling the impact of process variation on critical charge distribution. In *IEEE International SOC Conference, 2006*, pages 243–246, 2006.

[DLX05] Qian Ding, Rong Luo, and Yuan Xie. Impact of process variation on soft error vulnerability for nanometer VLSI circuits. In *ASICON 2005*, volume 2, pages 1117–1121, 2005.

[DM03] P.E. Dodd and L.W. Massengill. Basic mechanisms and modeling of single-event upset in digital microelectronics. *IEEE Transactions on Nuclear Science*, 50(3):583–602, 2003.

[DWB+10] R.G. Dreslinski, M. Wieckowski, D Blaauw, D Sylvester, and T. Mudge. Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits. *Proceedings of the IEEE*, 98(2):253–266, 2010.

[HAP+05] M. Horowitz, E. Alon, D. Patil, S. Naffziger, Rajesh Kumar, and K. Bernstein. Scaling, power, and the future of CMOS. In *IEEE International Electron Devices Meeting, 2005.*, pages 7 pp.–15, 2005.

[hC] Synopsys University Program. Available: http://www.synopsys.com/ Community/UniversityProgram/Pages/default.aspx.

[HK05] T. Heijmen and B. Kruseman. Alpha-particle-induced SER of embedded SRAMs affected by variations in process parameters and by the use of process options . *Solid-State Electronics*, 49(11):1783 – 1790, 2005.

[JRS09] S.M. Jahinuzzaman, D.J. Rennie, and M. Sachdev. A soft error tolerant 10T SRAM bit-cell with differential read capability. *IEEE Transactions on Nuclear Science*, 56(6):3768–3773, Dec 2009.

[JSS09] S.M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev. An analytical model for soft error critical charge of nanometric SRAMs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 17(9):1187–1195, 2009.

[KAH+12] H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar. Near-threshold voltage (NTV) design: Opportunities and challenges. In *49th ACM/EDAC/IEEE Design Automation Conference (DAC), 2012*, pages 1149–1154, 2012.

[KBB+12] A.V. Kauppila, D.R. Ball, B.L. Bhuva, L.W. Massengill, and W.T. Holman. Impact of process variations on upset reversal in a 65 nm flip-flop. *IEEE Transactions on Nuclear Science*, 59(4):886–892, 2012.

[KBK+11] A.V. Kauppila, B.L. Bhuva, J.S. Kauppila, L.W. Massengill, and W.T. Holman. Impact of process variations on SRAM single event upsets. *IEEE Transactions on Nuclear Science*, 58(3):834–839, 2011.

[KKKT12] U.R. Karpuzcu, K.B. Kolluru, Nam Sung Kim, and J. Torrellas. VARIUS-NTV: A microarchitectural model to capture the increased sensitivity of manycores to process variations at near-threshold voltages. In *42nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, pages 1–11, June 2012.

[KKT13] U.R. Karpuzcu, Nam Sung Kim, and J. Torrellas. Coping with parametric variation at near-threshold voltages. *IEEE Micro*, 33(4):6–14, July 2013.

[MAE11] H. Mostafa, M. Anis, and M. Elmasry. A bias-dependent model for the impact of process variations on the SRAM soft error immunity. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 19(11):2130–2134, 2011.

[MBR06] S. Mukhopadhyay, S. Bhunia, and K. Roy. Modeling and analysis of loading effect on leakage of nanoscaled bulk-CMOS logic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25(8):1486–1495, 2006.

[Mes82] G.C. Messenger. Collection of charge on junction nodes from ion tracks. *IEEE Transactions on Nuclear Science*, 29(6):2024–2031, 1982.

[MNB01] D. Markovic, B. Nikolic, and R. Brodersen. Analysis and design of low-energy flip-flops. In *Proceedings of the 2001 International Symposium on Low Power Electronics and Design*, ISLPED '01, pages 52–55, New York, NY, USA, 2001. ACM.

[MWA+10] D. Markovic, C.C. Wang, L.P. Alarcon, Tsung-Te Liu, and J.M. Rabaey. Ultralow-power design in near-threshold region. *Proceedings of the IEEE*, 98(2):237–252, 2010.

[Nar05] Siva G. Narendra. Challenges and design choices in nanoscale CMOS. *J. Emerg. Technol. Comput. Syst.*, 1(1):7–49, March 2005.

[OSM] M. Onabajo and J. Silva-Martinez. Analog circuit design for process variation-resilient systems-on-a-chip. *Springer Science+Business Media New York 2012*.

[PCC+14] R. Pawlowski, J. Crop, M. Cho, J. Tschanz, V. De, B. Borkar, T. Fairbanks, H. Quinn, and H. Chiang. A reference design for effective characterization of soft error vulnerability of low voltage logic and memory circuits. *IEEE Workshop on Silicon Errors in Logic-System Effects (SELSE 2014)*, 2014.

[SCH+11] M. Seok, G. Chen, S. Hanson, M. Wieckowski, D Blaauw, and D Sylvester. CAS-FEST 2010: Mitigating variability in near-threshold computing. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 1(1):42–49, 2011.

[SGT+08] S.R. Sarangi, B. Greskamp, R. Teodorescu, J. Nakano, A. Tiwari, and J. Torrellas. VARIUS: A Model of process variation and resulting timing Errors for microarchitects. *IEEE Transactions on Semiconductor Manufacturing*, 21(1):3–13, Feb 2008.

[UTB+06] O.S. Unsal, J.W. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalez, and O. Ergin. Impact of parameter variations on circuits and microarchitecture. *IEEE Micro*, 26(6):30–39, 2006.

[VF05] Vasanth Venkatachalam and Michael Franz. Power reduction techniques for microprocessor systems. *ACM Comput. Surv.*, 37(3):195–237, September 2005.