# IMPACT OF DESIGNER-CONTROLLED PARAMETERS ON SINGLE-EVENT RESPONSES FOR FLIP-FLOP DESIGNS IN ADVANCED TECHNOLOGIES

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# Chapter 1

## Introduction

The semiconductor industry has maintained technology scaling at the pace of Moore's Law for the past 50 years [1, 2]. The feature size of transistors scales by a factor of 0.7 every three years, enabling increasing number of transistors per integrated circuit (IC) associated with improved speed and system performance.

A traditional planar transistor establishes an electrical field and forms conducting channel from the source to the drain when the gate electrode is energized [3]. As the length of the gate is reduced, the control of the gate over the channel region is also reduced and short channel effects arises [4]. The threshold voltage, subthreshold slope and leakage current become sensitive to the gate length and are significantly degraded. New controlling methods or transistor structures were in prompt need to suppress short channel effects. One effective device structure named "FinFET" has been proposed to enhance the gate control over the channel region by rapping the gate electrode around the channel [5, 6, 7]. Methods to fabricated devices in FinFET processes have been developed and simplified [5, 8]. The FinFET devices have shown promising performance and scalability.

Along with scaling down of CMOS technology and improved system performance, single-event effects (SEEs) have become a serious reliability concern for advanced technology nodes due to decreased transistor current and nodal capacitance [9, 10]. An SEE is a circuit or system response to a single-event (SE), which refers to a single ionizing particle interacting with a semiconductor device. For space radiation, the common sources of single events (SEs) include heavy-ions and cosmic rays. For terrestrial environment, the radiation components include alpha particles, high-energy neutrons and protons, thermal neutrons, muons and electrons. SEEs include radiation-induced soft errors and hard errors in microelectronic circuits caused by ionizing particles striking the sensitive region of semicon-

ductor devices. When an energetic particle strikes a semiconductor device, electron-hole pairs will be generated along the striking track and charge can be collected through drift and diffusion processes. The collected charge modifies the potential of struck nodes and produces transient voltage spikes called single-event transients (SETs) in circuits. When a SE strike occurs and deposits enough charge in a storage cell, such as SRAM cells or flip-flops (FFs), a data state change will occur. This bit flip is called a single-event upset (SEU). SETs generated in combinational logic parts may also be latched into receiving FFs to cause soft errors in integrated circuits (ICs).

Efforts have been put into evaluating and mitigating soft errors in ICs for advanced technology nodes. Nowadays, commercial fabrication houses have successfully transitioned to FinFET structure for their advanced semiconductor processes. For FinFET technologies, since the physical structure changes significantly compared to planar technologies, the charge collection mechanism at a circuit node will be affected by the thin fin region (narrow active Silicon region) and the narrow connection to the substrate. The differences in physical transistor structure for planar technologies and FinFET technologies are significant enough that most SEEs will need to be reevaluated for FinFET technologies. Previous experimental and simulation results have reported the sensitive cross-section area for individual transistors fabricated on a range of FinFET processes to be reduced, resulting in less charge collection and better SEU performance for each bit in memory cells compared to that for planar processes, especially for nominal supply voltage operations [11, 12, 13, 14].

## 1.1 Key Research Contributions

Modern ICs need to be designed to meet requirements of power, speed and SEU performance, etc. under different environment and operating conditions. Flip-flops are basic storage elements in sequential logic circuits and fundamental building blocks in digital electronic systems. Proper designer-controllable factors can be chosen to meet performance requirements for flip-flop (FF) designs in different applications. This work char-

acterizes the SEU performance for FF designs in a commercial 14/16-nm bulk FinFET technology from a designer's perspective. For the first time, effects of designer-controlled parameters related to fabrication processes, such as threshold voltage, dual- and triple-well structures, on SEU performance and power consumption have been investigated in FinFET technologies. Theoretic analysis, simulation and experimental results are used to understand the effects of threshold voltage and well structure on SEU responses. Effects of these designer-controlled parameters on SEU performance against temperature and incident angle of radiation particles are also evaluated for stability of SEU responses. By comparing with former planar technologies, this work will provide designers with better understanding of how SE mechanism evolves from planar to FinFET technologies, better idea of SEU performance for FF designs with different designer-controlled parameters and environment conditions, and provide design guidelines for choosing proper designer-controlled parameters for specific applications in the 14/16-nm bulk FinFET technology.

1. Threshold voltage ($V_T$): Increased integration density and operating frequency with technology scaling have led to significant increase in power density on ICs, increasing the need for power efficient design techniques. Fabrication houses have proposed to design low-power circuits by using different threshold voltages for individual transistors or employ multi-$V_T$ design techniques for different sub-circuits [15, 16, 17, 18]. Since it has become a standard practice to improve power requirements for a circuit by adjusting $V_T$ values, evaluating SEU vulnerability of circuits designed with different $V_T$ options is necessary. In this work, $V_T$ dependence of alpha-particle and heavy-ion-induced SEU cross-section at different supply voltages for a conventional D-flip-flop (DFF) design in a 14/16-nm bulk FinFET technology will be characterized. The SEU cross-sections for the 20-nm bulk planar DFF with different $V_T$ options will also be provided for comparison. Theory analysis and simulations will be carried out to understand the underlying mechanism for $V_T$ dependence of SEU cross-section for both the 20-nm bulk planar and the 14/16-nm bulk

FinFET technology. Design guidelines will be derived from case study to improve power, speed and SEU performance of specific circuits. Additionally, $V_T$ effects on SEU responses against temperature variations and angular strikes will also be studied to ensure the selected $V_T$ options remain efficient in real applications that face different operation conditions.

2. Dual- and triple-well structures: Triple-well technology has been widely used to provide better isolation of transistors from the substrate, which reduces substrate noise coupling as well as enable easier body bias and threshold voltage control [19, 20, 21]. With presence of the deep n-well, SEU response of circuits will be affected since the deep nSEU vulnerability-well alters the charge-collection mechanism. In order to take advantage of the triple-well technique at advanced FinFET technology nodes, evaluation of the SEU performance of dual- and triple-well structures in FinFET technologies are required. In this work, the dual-well and triple-well based 14/16-nm bulk FinFET FF designs will be irradiated with alpha particles and heavy-ions over a wide range of supply voltage to show the effect of the deep n-well on SEU performance. 3D TCAD (Technology Computer-Aided Design) simulations of transient currents, charge collection and SET pulse generation will be carried out for both planar and FinFET processes to explain the difference of underlying SE mechanism and how this alters the SEU performance. Similarly, SEU responses of dual- and triple-well FF designs will also be studied across wide ranges of temperature and particle incident angle to ensure proper choice of well-structure for system applications.

## 1.2 Dissertation Organization

The dissertation is organized as follows:

1. Chapter 1 first gave the general introduction to technology scaling, advantages of FinFET technologies, SEE, SEU and SE mechanism. After that, the objective and

planned investigation of this proposed work was presented. Finally, the organization of the area paper is listed.

2. Chapter 2 includes background information of SE mechanism, effects of the variations to be investigated (i.e. threshold voltage, dual- and triple-well structure) on SEU performance for previous technologies, theory analysis of how these parameters affect SEU vulnerability, and whether the variations affect SEU performance differently in the new FinFET structure.

3. Chapter 3 presents experimental and simulation results for $V_T$ effects on SET pulse width, feedback loop delay and overall SEU responses for the 20-nm bulk planar and the 14/16-nm bulk FinFET DFF designs, which shows how $V_T$ effects alters for different technologies. Frequency dependence of the 14/16-nm DFF with different $V_T$ options is also provided, followed by power, speed and SEU performance analysis and design guidelines.

4. Chapter 4 provides experimental and simulation results for effects of well structure on charge collection, SET pulse and overall SEU responses for the 14/16-nm bulk FinFET dual- and triple-well FF designs. Additional simulations have been carried out for designs with different well options in 40-nm and 28-nm CMOS technologies to show how SE mechanism evolves from planar to FinFET technologies.

5. Chapter 5 shows temperature and incident-angle dependence of SEU response for the 14/16-nm DFF and investigates the underlying mechanisms. Temperature and angular test results for FF designs with different $V_T$ and well options have also been provides to show $V_T$ and well-structure effects on SEU responses for the 14/16-nm FF designs across a wide range of temperature and incident angle.

6. Chapter 6 summarizes the major finding and research contributions of this work.

# Chapter 2

# Background

Microelectronic circuits are operated in systems for both space and terrestrial applications. For space applications, ICs are exposed to radiation particles from trapped "belts" as well as from galactic cosmic rays and solar events, resulting in significant SEEs in circuit systems [22]. Early evidence of SEEs occurred in 1975 and heavy-ion-induced upsets in space was observed in satellite operation [23]. Shortly after the first observation of SEU in space, soft errors in terrestrial operations were reported that alpha-particle contaminants in package materials led to significant alpha-particle-induced error rates in DRAMs [24]. Researchers also reported soft errors due to proton and neutron indirect ionization effects [25, 26], which revealed the large abundance of SE radiation sources. As technologies have scaled, the problem of soft errors has been exacerbated for both space and terrestrial applications. More recently, experimental results have shown that particles like muons and electrons can also be the cause of soft errors [27, 28].

## 2.1 Single-Event Mechanism

When a single radiation particle strikes a semiconductor device on an IC, it may cause an SE soft error in the circuit node, mainly through three processes: charge deposition, charge collection and circuit response [9].

### 2.1.1 Charge Deposition

An energetic particle can induce charge in a semiconductor device either through direct ionization or indirect ionization [29]. When an ionizing particle, like a heavy ion or an alpha particle, passes through a semiconductor material, direct ionization happens, as shown in Figure 2.1. Atoms in material can be ionized by the coulombic forces between

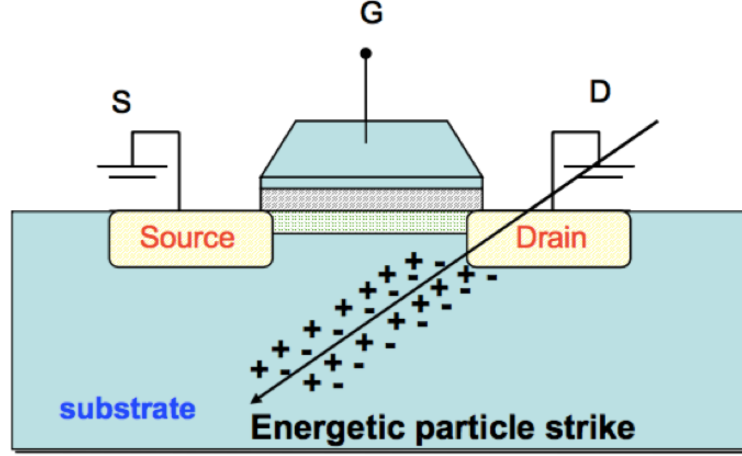



Figure 2.1: Generation of electron-hole pairs due to an energetic particle strike [30].

the moving charged particle and the electrons of the nearby atoms, leading to energy transfer from the particle to bound electrons. This ionization of the material generates a dense track of electron-hole pairs (EHPs) along the striking track. The rate of energy loss is often expressed in terms of stopping power (STP) or linear energy transfer (LET) [31]. STP is the incremental rate of energy loss along the ion's path with a unit of energy per unit length (e.g. $MeV/cm$). LET normalizes out the material density from STP and usually has a unit of $MeV \cdot cm^2/mg$. The distance traveled by the incident particle inside the semiconductor is defined as the particle's range in this particular material. Along the striking track, the charge created by the strike can be calculated by [31]:

$$\begin{aligned} dQ[pC] &= L(x)[pC/\mu m] \cdot dX[\mu m] \\ &= \frac{LET(x)[MeV \cdot cm^2/g] \cdot \rho[g/cm^3] \cdot 1.6 \times 10^{19}[C]}{G[eV]} \cdot dX[\mu m] \end{aligned} \tag{2.1}$$

For particles like protons or neutrons, production of the secondary charged particles is necessary before significant generation of EHPs occurs. These particles are considered to deposit charge through indirect ionization. The secondary particles deposit charge through the same mechanism as described above.

### 2.1.2 Charge Collection

After charge deposition, charge within specific region can be collected through drift and diffusion processes [31]. Figure 2.2 shows the drift and diffusion processes for charge collection in a reverse-biased junction and the resultant current pulse caused by the high-energy ion strike [10]. For electrons and holes passes the depletion region, presence of

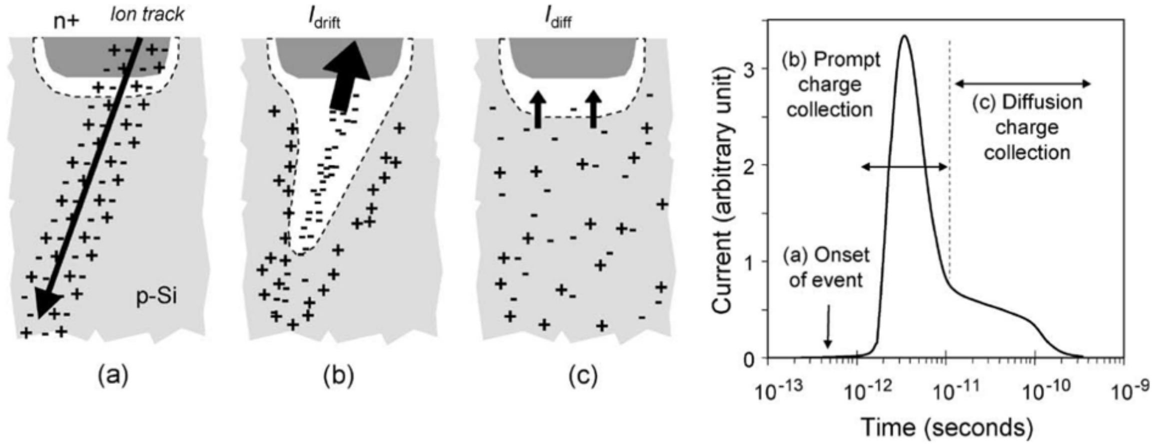



Figure 2.2: Charge generation and collection phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion [10].

electrical field helps effectively collect charge through drift process. In addition, the generated charge track can perturb the depletion region and distort the potential gradients along the track length significantly, leading to enhanced drift charge collection, which is called field funneling. Charge generated outside the funnel region but within a diffusion length of a junction may diffuse to the depletion region, leading to increased charge collection. Charge collection through diffusion is delayed since carriers need to move to the depletion region to be collected. In advanced CMOS technologies, charge collection may also be enhanced by bipolar transistor effect caused by the charge confinement within a well or body region [9]. Confined charge can modify the well potential, leading to additional injection of electrons into the channel [9, 32].

### 2.1.3 Circuit Response

The charge collected modifies the voltage of struck nodes and the restoring transistor current helps restore the struck node to its initial state, leading to a transient voltage spike or an SET pulse. Figure 2.3 shows an example of SET pulse generation when a particle strikes a 130-nm SOI NMOS transistor. The SET pulse width greatly depends on the amount of charge collection and the strength of restoring current drive.

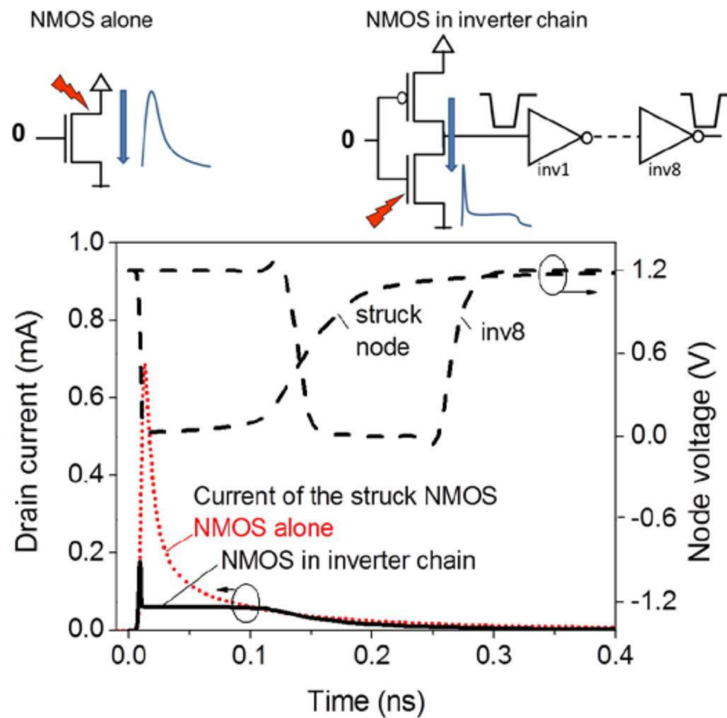



Figure 2.3: Simulation of a 5 $MeV \cdot cm^2/mg$ ion strike for a 130-nm SOI off-state NMOS transistor, either device alone or integrated in a CMOS inverter chain with mixed-mode simulation. The left axis shows the current drive and the right axis shows the output inverter voltages of the struck node [33, 34].

If the SET happens at the sensitive node of a flip-flop design or an SRAM design and is wide enough to transmit through the feedback circuit, an SEU will occur. SE upsets (SEUs) are non-destructive soft errors caused by ionizing particle strikes and normally appear as bit flips in SRAMs or FFs. Figure 2.4 shows the schematic design of a conventional D-latch, with an SET pulse generated by a particle hit. The D-latch consists of a transmission gate

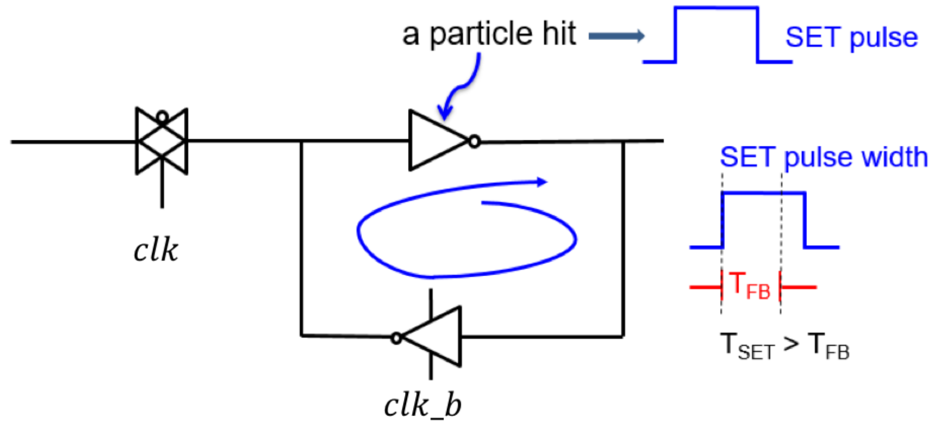



Figure 2.4: Schematic design of a conventional D-latch, with an SET pulse caused by a particle hit and defined feedback loop delay.

(outside the loop), an inverter (hit by a particle in the figure) and a clocked inverter (an inverter with clock control). Feedback loop delay is defined as the time needed for a signal to transmit through the whole loop. For example, the feedback loop delay for the D-latch in Figure 2.4 is the sum of one inverter delay and one clocked-inverter delay. If the SET pulse width is longer than the feedback loop delay of the D-latch, the state change will be latched and transmitted to the next stage, thus an SEU will be recorded.

## 2.2 Threshold Voltage

With scaling down of CMOS technology, increased integration density and operating frequency have led to significant increase in power density on ICs, increasing the need for power efficient design techniques. The preferred technique for reducing power consumption is to use reduced supply voltages since dynamic power is directly proportional to the square of supply voltage and standby power is proportional to supply voltage. However, reduction in supply voltage leads to lower operating frequency and increased vulnerability to single-event upsets [35, 36]. A alternate option provided by fabrication houses to design low-power circuits is to use different threshold voltages for individual transistors or employ multi-$V_T$ design techniques for different sub-circuits [15, 16, 17, 18]. There are

several $V_T$ options available in commercial process design kits (PDK) for power-saving purposes for each advanced technology node. While dynamic power is approximately independent of threshold voltage, standby power can be decreased by increasing threshold voltage [37, 38, 39]. Since the use of different $V_T$ options has become a standard practice to improve power requirements for a circuit, it is important to evaluate SEU vulnerability of circuits designed with different $V_T$ options.

### 2.2.1 Previous Results

Much previous work has been done to evaluate different effects of $V_T$ variations on critical charge, SEU probability or SEU cross-section in previous technologies [40, 41, 42, 43, 44]. Simulation results using 70-nm Berkeley predictive technology have been presented to show that increasing $V_T$ reduces soft error rates (SER) of transmission-gate-based FFs but increases SER for combinational logic circuits [39]. The spread in critical charge due to $V_T$ fluctuations of PMOS and NMOS transistors for 130-nm, 90-nm and 65-nm CMOS technologies have also been reported [40, 41]. The impact of $V_T$ variations on the SEU vulnerability for specific SRAM and FF designs in 90-nm and 65-nm CMOS processes has been evaluated [42, 43]. Figure 2.5 shows the SEU probability changes caused by $V_T$ variations for the 65-nm FF designs, which indicates that an increase in $V_T$ significantly increases the SEU probability. However, a different dependence of SER on $V_T$ for DFF designed in a 28-nm bulk planar process has been reported, as shown in Figure 2.6 [44]. For the 28-nm bulk planar technology, the SER of DFF with different $V_T$ options have been shown to be very similar. As a result, the power consumption of DFF designs at this technology node can be easily reduced by increasing $V_T$ without affecting the SEU vulnerability. These contradicting results have necessitated the need for reevaluating effects of $V_T$ variations on SEU cross-section for each new advanced technology node to find out the tradeoff between power consumption and SEU vulnerability.

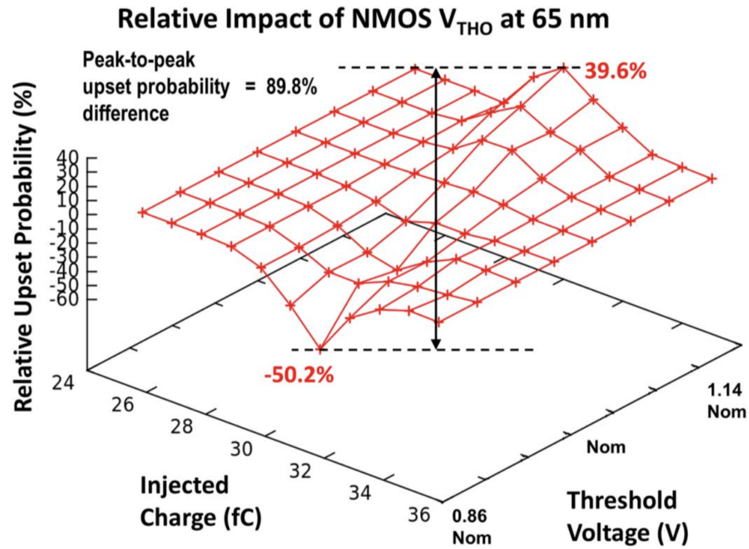



Figure 2.5: Impact of threshold voltage variations on the relative upset probability for a FF design in a 65-nm bulk CMOS technology [43].

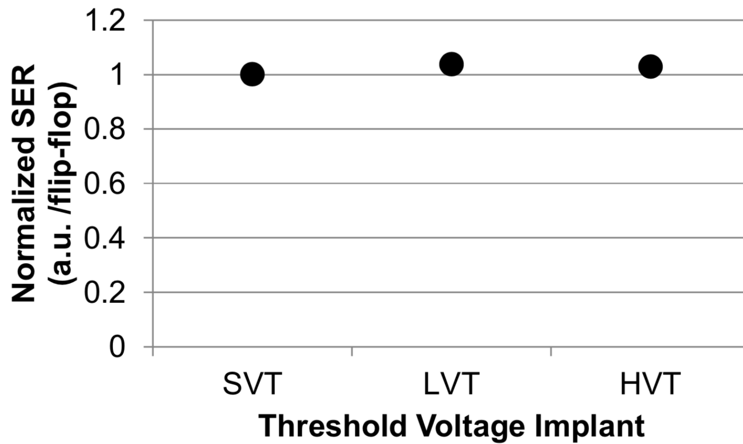



Figure 2.6: Impact of threshold voltage variations on DFF SER in a 28-nm bulk CMOS technology [44].

### 2.2.2 Theoretical Analysis

Transistor current is an important factor that affects SET pulse width and feedback loop delay. As mentioned earlier, transistor current drive is largely responsible for dissipating the deposited charge by the ion hit and leading to voltage recovery at the struck node. As transistor current decreases, SET pulse width will increase since it takes longer for a node

to restore to its original state with smaller currents. The gate delay is the length of time which starts when the input of a logic gate becomes stable and valid to change, to when the output of the logic gate is stable and valid to change. The length of time is equal to the time for charging or discharging the output node with capacitance $C_{out}$ to a desired state with current drive $I_D$ at a supply voltage of $V_{DD}$, $T_d = (C_{out} * V_{DD})/I_D$ [45]. So the gate delay is inversely proportional to transistor current and the feedback loop delay is simply the sum of several gate delays. A decrease in transistor current results in an increase in feedback loop delay. The two competing factors (SET pulse width and feedback loop delay) determine the overall SER for a given FF design. General equations for NMOS and PMOS transistor currents in linear region are shown as follows:

$$\begin{aligned} NMOS: I_{DS} &= \mu_n C_{ox}\frac{W}{L}[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2], C_{ox}=\frac{\varepsilon_0\varepsilon_{ox}}{t_{ox}} \\ PMOS: I_{SD} &= \mu_p C_{ox}\frac{W}{L}[(V_{SG}-|V_T|)V_{SD}-\frac{1}{2}V_{SD}^2], C_{ox}=\frac{\varepsilon_0\varepsilon_{ox}}{t_{ox}} \end{aligned} \quad (2.2)$$

From the equation set, the transistor current will be affected by carrier mobility, nodal capacitance, transistor length, transistor width and threshold voltage. As $V_T$ increases, transistor current decreases. Reduced transistor current leads to an increase in SET pulse width and feedback loop delay. If the SET pulse width augment outweighs that of the feedback loop delay, then the SEU probability will increase; if the feedback loop delay increases faster than the SET pulse width, a decrease in SEU probability is expected. As $V_T$ decreases, transistor current will increase. An increase in transistor current leads to a decrease in SET pulse width and feedback loop delay. If the pulse width reduction outweighs that of the feedback loop delay, a decrease in SEU probability is expected; if the feedback loop delay decreases more, the SEU probability increases.

Since SET pulse width is also closely related to the charge collection speed and amount, which is different for different technologies, varying currents caused by adjusting $V_T$ will lead to different percentage changes in SET pulse width relative to gate delay for each technology. For FinFET structure, the charge collection efficiency (from substrate) and the

charge available for collection are both reduced by the new structure [11]. Effects of $V_T$ on SEU performance for FinFET FF designs still wait to be investigated.

## 2.3 Dual-Well and Triple-Well Structures

Triple-well technology has been widely used for better isolation of transistors from the substrate to reduce substrate noise coupling [19, 20, 21]. With the deep n-well design, each NMOS transistor built in the p-well is separated from the substrate. In addition to noise isolation, triple-well structures also enable easier $V_T$ adjustment than dual-well structures through p-well bias for optimum performance and/or for controlling the power consumption without reducing supply voltage. In the presence of the deep n-well, SEU responses of circuits will be affected since the deep n-well alters the charge-collection mechanism and increases charge sharing between NMOS transistors [46].

### 2.3.1 Previous Results

Dual-well and triple-well designs for older technologies showed inconsistent SEU performance. Triple-well SRAMs fabricated in the 0.5-$\mu$m BiCMOS technology showed lower alpha-particle-induced SER compared to dual-well designs [47]. Triple-well SRAMs in a single-poly 0.15-$\mu$m process was also investigated and a significant degradation in the alpha particle-induced FIT rates was observed [48]. For triple-well SRAMs fabricated in a 130-nm technology node and a 90-nm technology node, the alpha-particle-induced SER were shown to decrease by $\sim$25% and $\sim$41% compared to the dual-well designs [49]. For the BISER and BCDMR FF designs in a 65-nm CMOS technology, triple-well design showed superior or inferior SEU performance than the dual-well design depending on operating frequency [50].

For recent planar technology generations, different behaviors of heavy-ion-induced upset cross-sections for triple-well and dual-well SRAMs designed in 65-nm, 40-nm and 28-nm technologies have been reported [51]. Results, presented in Figure 2.7, show over-

all SEU cross-section data (single-bit upsets as well as multi-cell upsets) for the 65-nm, 40-nm, and 28-nm SRAM designs. All three technology nodes show inferior performance for the triple-well designs for particle irradiation with low LET values. The 65-nm and

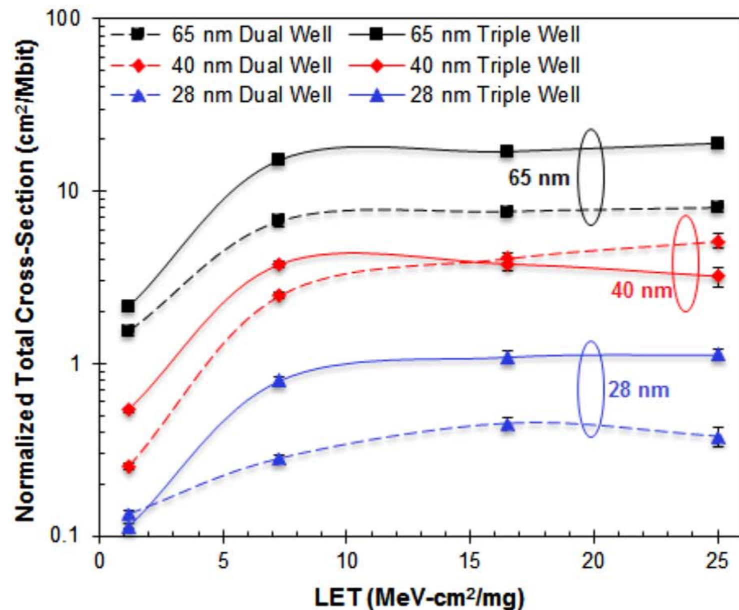



Figure 2.7: Normalized cross-section versus LET for dual-well and triple-well SRAMs for normal incidence irradiation with a checkerboard pattern in 65-nm, 40-nm, 28-nm bulk CMOS technologies [51].

28-nm nodes kept showing inferior SEU performance for triple-well designs compared to dual-well designs for all particle LET values. However, the 40-nm technology node showed better SEU performance for the triple-well design compared to the dual-well design for particles with high LET values due to single-event upset-reversal (SEUR) mechanism [51, 52].

Triple-well SRAMs were also found to have improved multi-cell upset (MCU) cross-sections at reduced supply voltages due to the dominance of SEUR at low voltage operations [53]. The results of alpha-particle exposure for the 28-nm planar dual-well and triple-well SRAM designs as a function of supply voltage are shown in Figure 2.8. For the nominal supply voltage $V_{DD}$ = 850 mV, the dual-well design shows superior performance. At reduced supply voltages, the triple-well design shows lower SEU cross-section compared to the dual-well design. These different trends are the result of competition be-

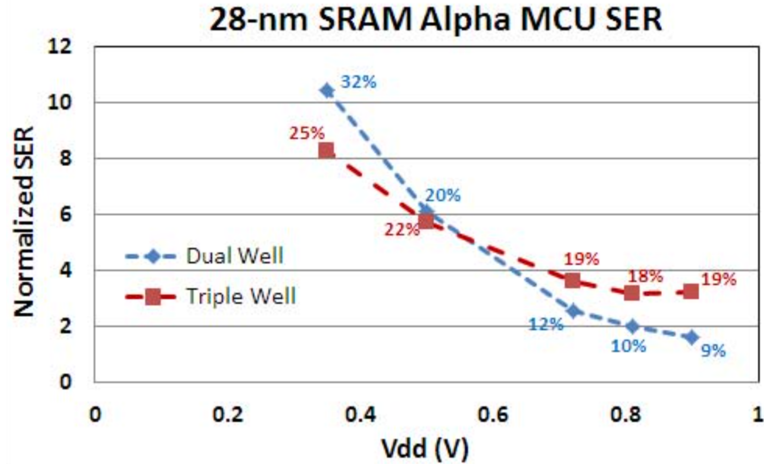
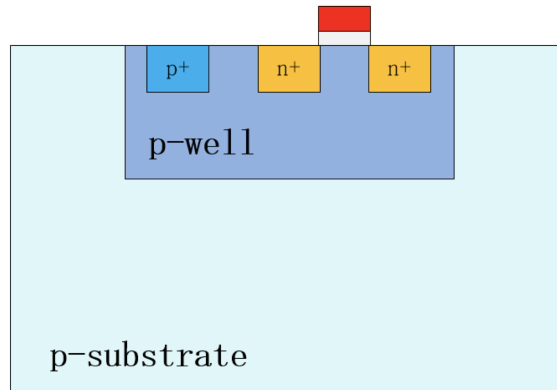



Figure 2.8: Normalized alpha-particle-induced MCU SER as a function of voltage for dual- and triple-well SRAMs in a 28-nm bulk CMOS technology [53].

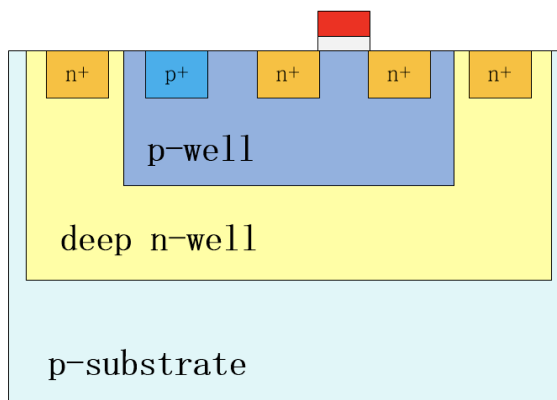
tween the charge-confinement mechanism and minimum spacing between sensitive regions at each technology node [51]. From these previous investigation, influence of well structure on SEU vulnerability highly depends on technology, which is difficult to predict for new technologies (especially for FinFET technologies when the physical structure have altered significantly).

### 2.3.2 Charge-Collection Mechanism with Different Well Structures

Figure 2.9 shows the two-dimension view of structures of dual- and triple-well planar NMOS transistors. Compared to the dual-well design, the triple-well NMOS comprises a buried deep-n-well that isolates the p-well from the p-substrate. Charge collection mechanism is altered in the triple-well structure by the third-well and has been discussed in [48]. Assume a simple application condition that source, p-well and p-substrate are connected to ground potential while drain, gate and deep-n-well are connected to high potential. For the dual-well design, generated electrons caused by ion hit in the p-well are collected by the drain region. Since the holes generated by ion hit spreads over the p-well and the p-substrate, the majority of holes inside p-well can be effectively removed by p-well contact and the potential perturbation to the p-well caused by trapped holes is not siSEU vulnerabil-




(a) Dual-Well




(b) Triple-Well

Figure 2.9: Structures of dual- and triple-well planar NMOS transistors.

itygnificant. Only small voltage perturbations exist in the p-well and the additional charge collection induced by bipolar transistor effect will not be significant. For the triple-well design, when a particle strikes, generated electrons in the p-well can be collected by the drain area and the deep-n-well. With presence of the deep-n-well, the majority of holes generated by ion hit are trapped in the p-well by the electric field between p-well and deep-n-well, leading to large voltage perturbation in p-well. Increasing p-well potential results in forward bias of the p-well to the source, leading to the source injecting additional electrons into the p-well, which may increase charge collection (bipolar transistor effect). However, the additional path for electrons from the p-well to the deep-n-well reduces charge collection (additional charge sink). If the bipolar transistor effect outweighs the effect of the

additional charge sink, enhanced charge collection will be found in the triple-well structure, leading to higher SEU vulnerability for the triple-well design than the dual-well design. If the p-well contact removes holes with such an efficiency (depending on the size and location of the p-well contact) that the bipolar transistor effect is not significant in the triple-well design, or the deep-n-well collects charge in a higher speed than the drain area, charge collection will be less for the drain region, leading to reduced SEU vulnerability compared to the dual-well design. Therefore, the SEU performance of triple-well designs compared to that of dual-well designs will depend both on hole removal efficiency of the p-well contact and charge collection efficiency of the drain and the deep-n-well.

The phenomenon of SEUR was also reported in previous work, which is similar to "pulse quenching" or "reinforcing charge collection" mechanism observed in combinational logics [51, 53, 54]. Charge confinement in the triple-well design may lead to higher numbers of multi-cell upsets within the same p-well [55]. The potential change in the second cell can form a feedback path to enhance the restoring current drive strength and restore the directly stricken cell to the original state, causing SEUR in the design and reducing overall SER.

The physical transistor structure for the FinFET transistors changes significantly compared to planar transistors. With the narrow connection between the well/substrate and the drain region, the charge collection efficiency of drain area may be further reduced, leading to the deep-n-well collecting more charge than the drain region. Besides, reduced charge-sharing effect at a FinFET node has been seen in SRAM cells where MCU size was used to show the extent of charge sharing between adjacent cells [56], which reduces charge collection and the possibility of SEUR. These differences further necessitate the need to reevaluate the SEU performance of dual- and triple-well designs in FinFET technologies in order to take advantage of the triple-well technique at advanced FinFET technology nodes.

## 2.4 Summary

In this chapter, the fundamental SE mechanism have been presented to show how soft errors can be caused by radiation particles in microelectronic systems. Threshold voltage and well structure are important designer-controllable variations that can be used for power-saving techniques or better isolation devices. Modifications on these parameters affect charge deposition, charge collection and circuit response processes, thus affecting the SEU vulnerability of advanced circuits. Previous investigations on the effects of $V_T$ and well structure on SEU responses have shown inconsistent behaviors for different technology nodes. Qualitative analysis has been presented in this chapter, which shows that impact of these factors is technology dependent. Along with significant changes in physical structure of FinFET technologies, the effects will be more unpredictable, necessitating reevaluation of $V_T$ and well-structure effects on SEU vulnerability for advanced FinFET circuits in order to take advantage of these benefits.

# Chapter 3

# Effects of Threshold Voltage Variations on Single-Event Upset Responses for Advanced Technologies

With increased use of $V_T$ options for power-saving techniques, investigation of $V_T$ effects on SEU responses for advanced circuits has come into the picture of product performance evaluation. It is crucial to understand the underlying mechanisms of $V_T$ effects on SEU performance for advanced technology nodes and the tradeoffs between power, speed and SEU performance when $V_T$ changes. This chapter mainly characterizes and compares the SEU responses of sequential circuits with different $V_T$ options in a 20-nm bulk planar technology and a 14/16-nm bulk FinFET technology. With circuit-level simulations and theoretical analysis, this work provides better understanding of how $V_T$ effects vary with technology and case study for design guidelines to achieve better overall performance to meet power, speed and SEU performance requirements for new technologies.

## 3.1 Test Circuits and Data Analysis

### 3.1.1 Test Circuits and Setup

Test chips were fabricated in both 20-nm bulk planar and 14/16-nm bulk FinFET technology at a commercial foundry. FF chains with different FF designs were implemented in Circuit for Radiation Effects Self-Test (CREST) configuration [57]. The test structure consists of 8K shift-register stages for each FF chain, with supplemental clock generation, error detection and latch circuits, as shown in Figure 3.1. All sub-circuits other than shift registers were designed with Triple Modular Redundancy (TMR) to eliminate all errors from support circuits.

The conventional master-slave DFF design with inverter and clocked inverter was used. For the 20-nm node, DFF with high (HVT), low (LVT) and ultra-low (ULVT) $V_T$ options

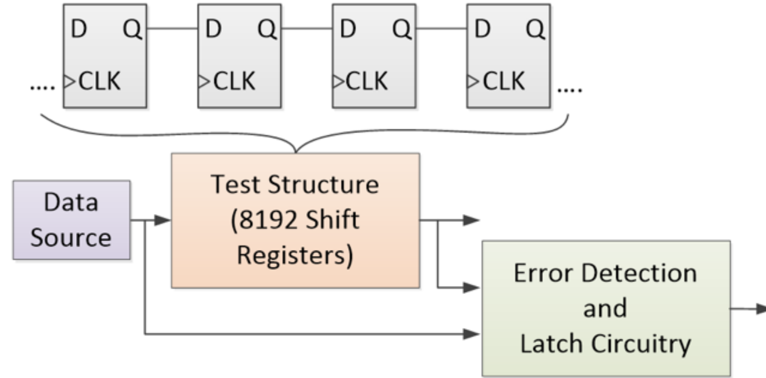



Figure 3.1: CREST block level design used for evaluating SEU response of FF cells, after [58].

($V_T$ : $HVT > LVT > ULVT$) were designed in three different CREST blocks. For the 14/16-nm technology, all four available $V_T$ implants, which are standard (SVT), low (LVT), intermediate-low (iLVT) and ultra-low (ULVT) $V_T$ options ($V_T$ : $SVT > LVT > iLVT > ULVT$), were used to design four different CREST blocks.

For further evaluating $V_T$ effects on SEU responses for advanced circuits, the 14/16-nm bulk FinFET DFF designs are operated at high frequencies to measure the logic SEU cross-sections. These DFF designs consist of master and slave stages, with one being on-hold stage and another being transparent stage. The transparent stage acts like logic circuits and SET-induced errors become an important portion as frequency increases. Additionally, identical logic circuits were designed with different $V_T$ options (SVT, LVT and iLVT) for the 14/16-nm combinational logic circuits. These logic SE measurement circuits were implemented in Combinational Circuit for Radiation Effects Self-Test (C-CREST) configuration [59] with 2K stages per block, as shown in Figure 3.2. Each stage consists of logic elements interleaved with flip-flops, which captures upsets from FFs and logic circuits. Similar to CREST blocks, C-CREST blocks also employed TMR for support circuits to eliminate all errors except those from the FFs and logic circuits.

To further reduce the number of errors from FF cells (and to increase the visibility of logic errors), Dual-Interlocked Storage Cell (DICE) FFs [61, 62] were used in the C-

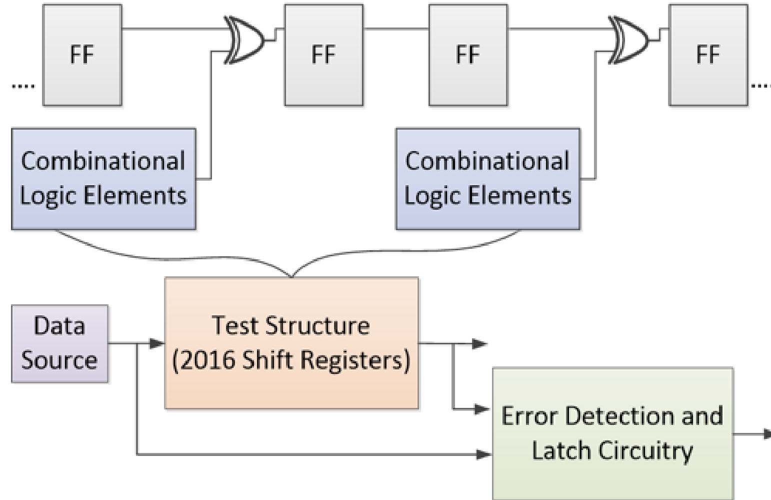
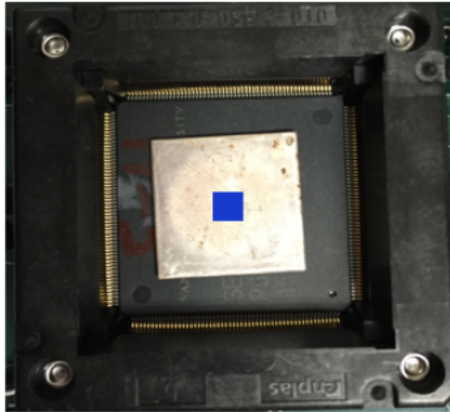


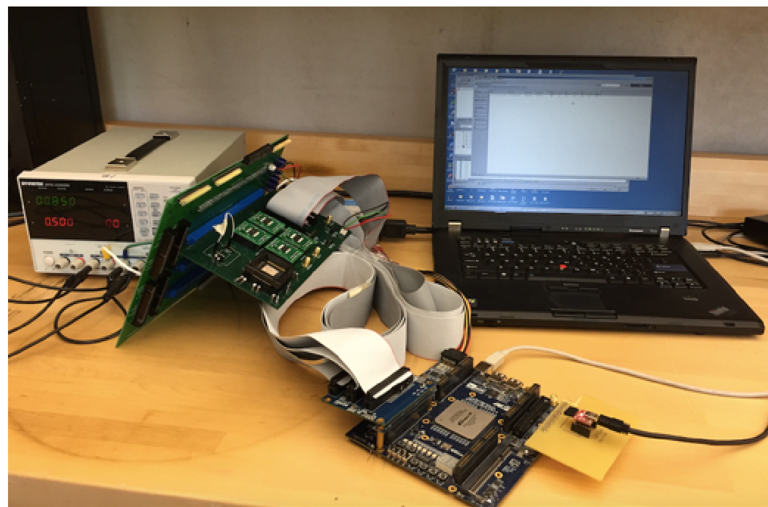

Figure 3.2: C-CREST block level design used for evaluating SEU response of FF and logic circuits [60].

CREST blocks. A separate CREST block for the same DICE FF was used to estimate the SEU cross-section of the DICE FF design. The logic structure inserted between each DICE FF was a 4-bit comparator circuit. Three different C-CREST blocks were designed, each using a different $V_T$ option (SVT, LVT, ULVT) for all transistors in the logic block.

The size of test ICs is $2\ mm \times 2\ mm$ and the packaged die is of $2\ cm \times 2\ cm$, which can fit into properly designed IC socket, as shown in Figure 3.3(a). Figure 3.3(b) shows the test setup, including equipment for testing, test boards, and the connections for the setup. Altera DE2-115 or DE3 [63] are used to control the signal and data transmission through ribbon cables for test ICs. Printed Circuit Boards (PCBs) were designed and fabricated for convenient connection and control of signal and data transmission from FPGA (Field Programmable Gate Array) boards to test ICs. Either the shift-register outputs or the error detection results can be read. When tested with radiation sources and SEUs are generated inside FF designs, errors will be counted on IC. Data will transmit out through the PCB and be stored in FPGA, and finally be shown on the control terminal of the laptop. Data analysis can be done with stored file for SEU performance.



(a) A socket holds the packaged die with alpha source sitting above. Blue block shows the position of IC under alpha source



(b) Test equipments, parts and connections.

Figure 3.3: SEU characterization test setup.

### 3.1.2 SEU Cross-Section and Failure in Time Analysis

SEU cross-section for FF designs were measured with CREST circuits (Figure 3.1). The equation used to calculate FF SEU cross-section is:

$$Cross-Section/FF[cm^2] = \frac{\#\,of\ Errors}{(\#\,of\ FFs) \times Total\ Fluence} \tag{3.1}$$

When number of errors is no less than 100, standard errors are used for error bars:

$$ErrorBarFF = \frac{\sqrt{\#\ of\ Errors}}{(\#\ of\ FFs) \times Total\ Fluence} \tag{3.2}$$

When number of errors is less than 100, error bars were calculated with a confidence level of 95%, as expressed in [64]. Failure in time (FIT) is the number of failures that can be expected in one billion ($10^9$) device-hours of operation. FIT rates and error bars are calculated for mega FFs as follows:

$$\begin{aligned} FIT/MFF &= Cross-Section/FF[cm^2] \times 10^9[hours] \times 10^6[/MFF] \times (\#\ of\ particles)[/cm^2/hour] \\ ErrorBarFIT &= ErrorBarFF \times 10^9[hours] \times 10^6[/MFF] \times (\#\ of\ particles)[/cm^2/hour] \end{aligned} \tag{3.3}$$

SEU cross-section for logic circuits were measured with C-CREST circuits (Figure 3.2). Similarly, the equations used to calculate logic SEU cross-section and error bars (or based on reference [64]) are:

$$\begin{aligned} Cross-Section/stage[cm^2] &= \frac{(Total\ \#\ of\ Errors) - (\#\ of\ Errors\ from\ FFs)}{(\#\ of\ stages) \times Total\ Fluence} \\ ErrorBarLogic &= \frac{\sqrt{(Total\ \#\ of\ Errors) - (\#\ of\ Errors\ from\ FFs)}}{(\#\ of\ stages) \times Total\ Fluence} \end{aligned} \tag{3.4}$$

### 3.1.3 Simulation Uncertainty

Compared to results from real circuit tests, there will be uncertainties in simulation results for transistor current, charge collection, SET pulse width and gate delay. In this section, the sources for simulation uncertainty will be discussed.

Circuit-level simulations were carried out in Cadence tool suite with commercial 20-nm and 16-nm PDKs or 16-nm Arizona State University Predictive Technology Models (ASU PTM) [65, 66]. The uncertainty for transistor current and gate delay mainly comes from the accuracy of PDK/PTM. For example, PDK provides transistor models for different $V_T$

options with nominal $V_T$ values. However, process variations in real circuits may shift the real $V_T$ values and induce differences in simulation results and experimental results. Other process variations, such as variations in transistor length, width, oxide thickness, doping density, may also induce differences. Besides, accuracy of temperature models in PDK and PTM affects simulation results for transistor current and gate delay as temperature changes.

The above variations also contribute to the uncertainty for SET pulse width simulation in Cadence. Other sources for uncertainty includes the current model used for particle strikes, particle LET values and hit locations. The bias-dependent single-event compact model developed in [67] was used to strike sensitive nodes in circuits. The model is capable of capturing the bias-dependent effects, recombination and parasitic bipolar effects and shows good agreement with 3D mixed-mode TCAD simulations. The model parameters were developed and calibrated with high-LET particles, and then for low-LET particles, which may induce additional uncertainty in SET pulse width. The LET value used for particle strikes in simulations and experiments may also differ, resulting in differences between simulation and experimental results. Lastly, particles may hit a specific node in circuits but the exact hit location may not be precisely known (i.e. how far from the center of the drain area) during experiments. All these factors can induce uncertainty for the SET pulse width values.

For 3D TCAD simulations, the uncertainty of charge collection and SET pulse width mainly comes from model calibration. Electrical characteristics of transistor, inverter and latch models are calibrated to 20-nm PDK or 28-nm PDK or 40-nm PDK or 16-nm PTM, so the variations in PDK and PTM will also be reflected in TCAD simulations. Besides, some of the detailed information, such as structure, doping density, carrier mobility, lifetime, recombination, gate stack, metal stack, layout, is not precisely known. With electrical characteristic calibration and sensitivity study, the accuracy of the TCAD models can be increased, but these parameters still induce uncertainties. The characteristics of striking particle, such as model of heavy-ion tracks, characteristic radius and deposition time, also

affect charge collection and SET pulse width values. These factors may induce additional uncertainty for TCAD simulations of charge collection and SET pulse width.

Quantitative error-bar analysis for simulation results can be done with additional information for fabrication processes, transistors, layouts, PDK and PTM variations and simulation models.

## 3.2 Heavy-ion Irradiation

### 3.2.1 Experimental Details

Heavy-ion tests were carried out at Lawrence Berkeley National Laboratory (LBNL) with 10 $MeV/nucleon$ cocktail for the 20-nm test ICs and 16 $MeV/nucleon$ cocktail for the 14/16-nm test ICs [68]. The LET values of heavy-ions were between $0 \sim 60\ MeV \cdot cm^2/mg$, as listed in Table 3.1 and Table 3.2. All heavy-ion tests were conducted in vacuum, at room temperature and at normal incidence, with total fluence running up to $5 \times 10^7\ /cm^2$. For the 20-nm DFF designs, static tests (clock set at "0") were carried out at 900 mV. For the 14/16-nm DFF designs, tests were carried out at 800 mV with a low operating frequency at 2.5 MHz.

Table 3.1: 10 MeV/nucleon Cocktail Components

| Ion | Energy ($MeV$) | LET ($MeV \cdot cm^2/mg$) | Range ($\mu m$) |
|---|---|---|---|
| $^{11}B^{+3}$ | 108.01 | 0.89 | 305.7 |
| $^{18}O^{+5}$ | 183.47 | 2.19 | 226.4 |
| $^{22}Ne^{+6}$ | 216.28 | 3.49 | 174.6 |
| $^{40}Ar^{+11}$ | 400.00 | 9.74 | 130.1 |
| $^{51}V^{+14}$ | 508.27 | 14.59 | 113.4 |
| $^{65}Cu^{+18}$ | 659.19 | 21.17 | 108.0 |
| $^{84}Kr^{+24}$ | 885.59 | 30.86 | 109.9 |
| $^{124}Xe^{+34}$ | 1232.55 | 58.78 | 90.0 |

Table 3.2: 16 MeV/nucleon Cocktail Components

| Ion | Energy ($MeV$) | LET ($MeV \cdot cm^2/mg$) | Range ($\mu m$) |
|---|---|---|---|
| $^{20}Ne^{+7}$ | 321.00 | 2.39 | 347.9 |
| $^{40}Ar^{+14}$ | 642.36 | 7.27 | 255.6 |
| $^{63}Cu^{+22}$ | 1007.34 | 16.53 | 190.3 |
| $^{78}Kr^{+27}$ | 1225.54 | 24.98 | 165.4 |
| $^{124}Xe^{+43}$ | 1954.71 | 49.29 | 147.9 |

### 3.2.2 Experimental Results

Heavy-ion test results for two technology nodes are shown in Figure 3.4 and Figure 3.5. For the 20-nm node, the influence of threshold voltage on SEU cross-section is not significant for high-LET heavy-ion irradiations. For low-LET particles, the ULVT DFF design shows slightly higher SEU cross-sections than those with HVT and LVT options. However, the differences are not significant. With very low critical charge values for these FF designs, differences in cross-sections are magnified near the LET threshold. For incident particles with LET significantly higher than the LET threshold, all these designs will show similar cross-sections because the underlying circuit design and layout are identical and the collected charge is large enough to cause upsets.

Similar to the DFF designs in the 20-nm technology node, high-LET heavy-ion irradiation results do not show significant differences among different $V_T$ options for the 14/16-nm FinFET node, as is shown in Figure 3.5. For heavy-ion particles with low-LET values, some differences among the SEU cross-sections of these DFF designs can be observed (not significant and within error bars). For this node, the ULVT design shows the lowest SEU cross-section and the SVT design shows the highest SEU cross-section, which is completely opposite to what was observed for the 20-nm technology node. The different trends in SEU cross-section compared to that of 20-nm DFF relate to the different changing rate of SET pulse width and feedback loop delay as $V_T$ changes for two technologies.

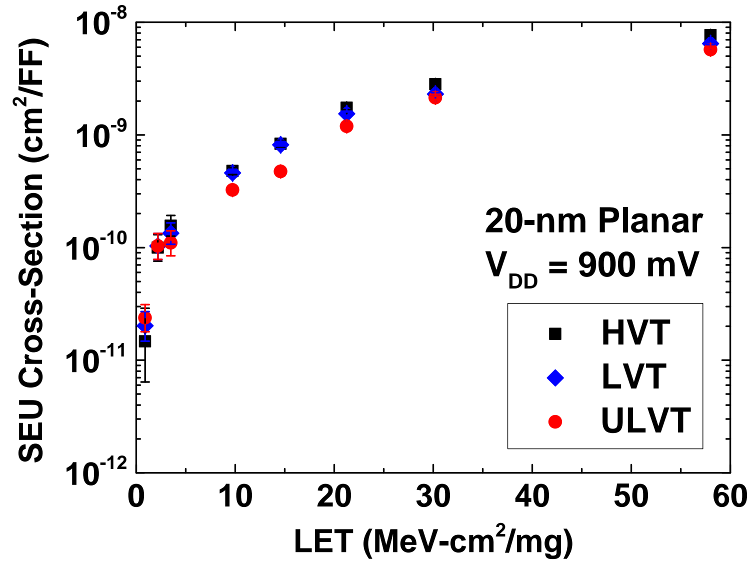



Figure 3.4: Heavy-ion-induced SEU cross-section as a function of particle LET for 20-nm DFF with different $V_T$ values.

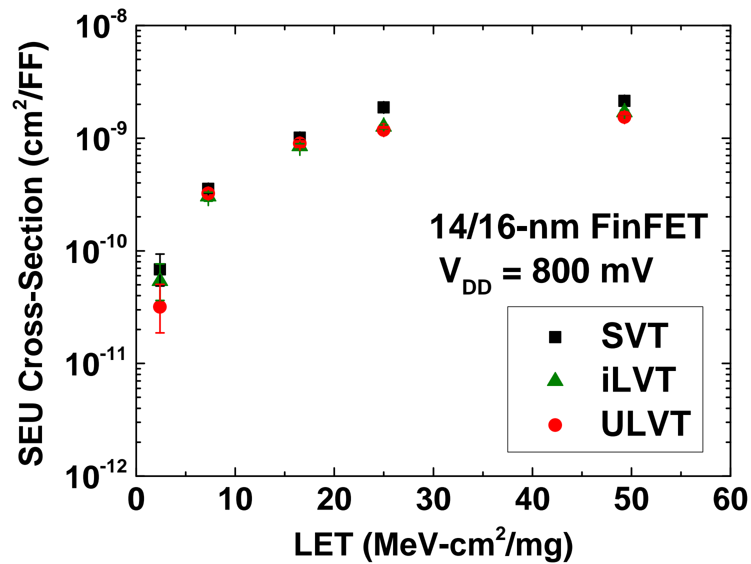



Figure 3.5: Heavy-ion-induced SEU cross-section as a function of particle LET for 14/16-nm DFF with different $V_T$ values.

## 3.3 Alpha Particle Irradiation

### 3.3.1 Experimental Details

Alpha tests were carried out at Vanderbilt University at room temperature, with a 1 $cm \times$ 1 $cm$ size 5.4 $MeV$ 10 $\mu Ci$ $^{241}Am$ foil button source to test FF SEU cross-section. Figure 3.6 shows the spectrum of the alpha source. The air gap between the Americium source and

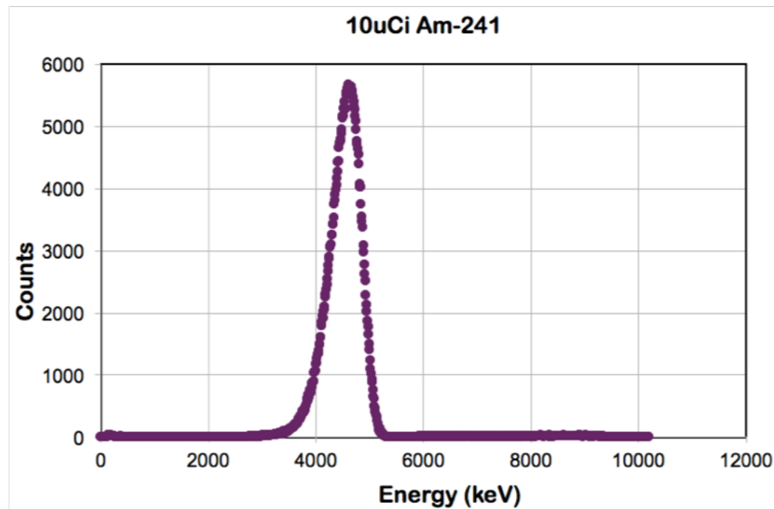



Figure 3.6: Flux-Energy Spectrum of 5.4 $MeV$ 10 $\mu Ci$ $^{241}Am$ source.

the die was less than 1 mm, leading to the particle LET less than 1 $MeV \cdot cm^2/mg$ when it reaches the active Silicon region. The alpha particle flux from the source was ~1000 $alpha/mm^2/s$. Supply voltage was varied from 750 mV to 950 mV (nominal $V_{DD}$ is 850 mV) for the 20-nm DFF designs and 550 mV to 850 mV (nominal $V_{DD}$ is 800 mV) for the 14/16-nm DFF designs. During testing, the shift registers were clocked at a low frequency of 2.5 MHz with logic input "0".

### 3.3.2 Experimental Results

Experimental results are shown in this section. All curves contain error bars (some of them are too small to see). Figure 3.7 shows the experimental results of the SEU cross-sections for DFF designs with different $V_T$ options for the 20-nm planar technology. The

ULVT design shows ∼5x higher SEU cross-section than HVT design at 950 mV. This difference increases further to ∼6x and ∼7x when supply voltage is reduced to 850 mV and 750 mV. As $V_T$ increases from ULVT to LVT to HVT, the transistor saturation current decreases, reducing the restoring current drive at a circuit node. This reduction in restoring

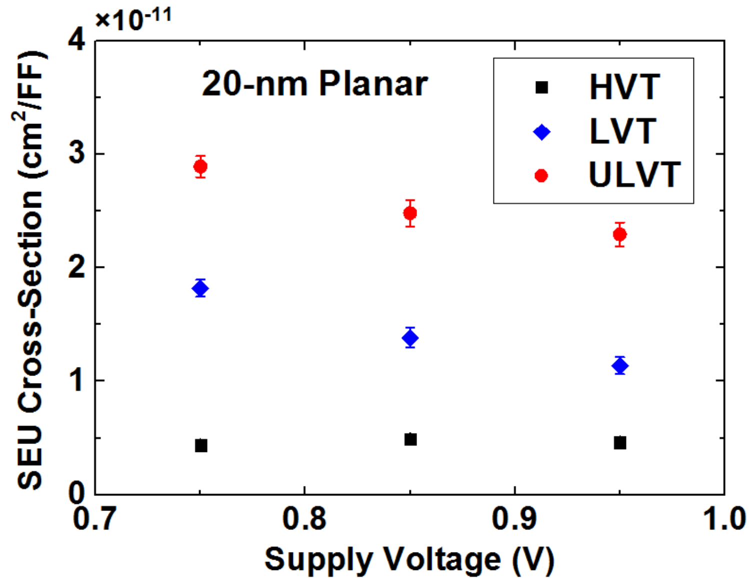



Figure 3.7: Alpha-particle-induced SEU cross-section as a function of supply voltage for 20-nm DFF with different $V_T$ values.

current drive leads to lengthening of SET pulse generated at the circuit node. Additionally, the reduction in transistor currents also leads to an increase in feedback loop delay of an FF. A larger SET pulse width increases the upset probability while a longer feedback loop delay decreases it. These two competing factors determine the overall response of DFF.

Alpha test results for the 14/16-nm DFF designs with varying threshold voltages are shown in Figure 3.8. As supply voltage decreases from 850 mV to 550 mV, the SEU cross-section increases by ∼7x to ∼10x for these DFF designs at this technology node. For this technology node, SEU vulnerability increases as $V_T$ increases within a supply voltage range of 550 mV to 850 mV. As $V_T$ increases from ULVT to SVT, the alpha-particle-induced SEU cross-section increases by ∼2x. For the 14/16-nm DFF designs, decrease in transistor current caused by increasing $V_T$ also results in an increase in SET pulse width

and feedback loop delay for the DFF designs. The different trends in SEU cross-section compared to that of the 20-nm DFF are similar to what has been observed for heavy-ion low-LET particle irradiations, which is mainly due to different changing rate of SET pulse width and feedback loop delay. Detailed simulations and analysis will be done in the next section.

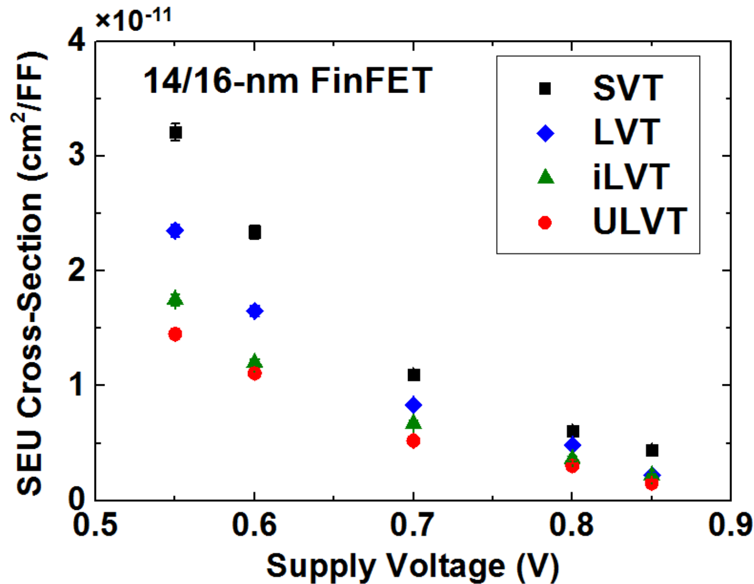



Figure 3.8: Alpha-particle-induced SEU cross-section as a function of supply voltage for 14/16-nm DFF with different $V_T$ values.

## 3.4 Simulations and Discussion

Simulations were carried out in Cadence tool suite, with a bias-dependent model striking an OFF-state NMOS in the DFF designs [67, 65]. For the 20-nm bulk planar technology, simulated SET pulse width (PW) and feedback loop delay (FD) were obtained using a commercial 20-nm process design kit (PDK) (shown in Table 3.3) to show the percentage increase in SET pulse width and feedback loop delay as $V_T$ increases at nominal supply voltage ($V_{DD}$ = 850 mV). A low-LET particle (with the LET value close to that of alpha particles, about 1 $MeV \cdot cm^2/mg$ ) was used to strike inverters with OFF-state NMOS to generate SET pulses for these simulations. The percentage changes were calculated with

respect to the SET pulse width and feedback loop delay of the ULVT design. For the 20-nm

Table 3.3: Percentage Change in SET PW and FD relative to ULVT Design for 20-nm Node

| | HVT | LVT | ULVT |
|---|---|---|---|
| SET PW | 39.7% | 15.3% | 0 |
| FD | 51.8% | 18.2% | 0 |

technology node, the increase in feedback loop delay is higher than that for the SET pulse width as $V_T$ increases from ULVT to HVT, resulting in lower upset probability for HVT and LVT designs. This will lead to lower SEU cross-sections for higher $V_T$ designs with low-LET particle irradiations. Therefore, for this 20-nm DFF design under low-LET particle irradiations, increasing $V_T$ can effectively reduce static power consumption without any penalty in SEU vulnerability. According to Figure 3.7, this conventional DFF design with HVT option operating at a reduced supply voltage provides better performance for alpha-particle-induced SEU cross-section and power consumption than lower $V_T$ options. It must be kept in mind that this may vary with different FF designs. These results are a strong function of SET pulse width and feedback loop delay. Depending on the FF design (individual transistor sizes and circuit topology), the changes in SET pulse width and feedback loop delay for different $V_T$ options may be different, resulting in a different SEU response, as was observed for the 14/16-nm DFF designs. For high-LET particle irradiations, the SEU cross-section for designs with three $V_T$ options are not significantly different since the SET pulse width becomes significantly larger than the feedback loop delay, which also leads to HVT option as the best choice for tradeoff between power and SEU responses.

For the 14/16-nm bulk FinFET node, a commercial 14/16-nm PDK was used to simulate the SET pulse width (strikes with a low-LET particle with the LET value close to that of alpha particles, about 1 $MeV \cdot cm^2/mg$) and feedback loop delay for the DFF design at nominal supply voltage ($V_{DD}$= 800 mV). Similarly, the percentage changes were calculated with respect to the SET pulse width and feedback loop delay of the ULVT design. Table 3.4 shows simulation results of the percentage change in SET pulse width and feedback

loop delay when $V_T$ increases from ULVT to SVT for the 14/16-nm bulk FinFET technology. For this technology node, SET pulse width increases faster than feedback loop delay,

Table 3.4: Percentage Change in SET PW and FD relative to ULVT Design for 14/16-nm Node

| | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|
| SET PW | 116.5% | 61.6% | 37.0% | 0 |
| FD | 78.9% | 36.0% | 15.6% | 0 |

leading to higher SEU probability for high $V_T$ options for low-LET particle irradiations, as shown in Figure 3.8. Similar increasing rates of SET pulse width and gate delay have been observed for inverters in a 14/16-nm bulk FinFET technology node as supply voltage decreases or $V_T$ changes [69]. Changing supply voltage is different from changing threshold voltage although both of them influences the transistor current. In the transistor current equation (in linear region), supply voltage and $V_T$ contribute differently to the transistor current. Besides, $V_T$ can be mainly adjusted by changing channel doping or work function, which affects differently for the depletion region and charge collection than supply voltage variations. As $V_T$ increases from LVT to RVT, the SET pulse width values and gate delays increase at similar rates [69], which is different from simulation results in this work. There are several possible reasons. The two 14/16-nm bulk FinFET technology nodes are from two different commercial foundries, which may result in process parameter differences in two commercial PDKs. Besides, the data in [69] were collected with an LET of 21 $MeV \cdot cm^2/mg$ and some short pulses were filtered out, which reduces the rate of increase for average SET pulse width. This leads to similar increasing rates for SET pulse width and feedback loop delay in [69] while a faster increasing rate is observed for SET pulse width compared to feedback loop delay in this work.

The different SEU cross-section dependences on threshold voltage between the 20-nm DFF and the 14/16-nm DFF designs are mainly due to the difference in the physical structure, doping level, transistor size and transistor spacing, which lead to different rates of change for SET pulse width and feedback loop delay. For high-LET particle irradiations,

the SEU cross-section is not affected significantly by $V_T$ options, which is similar to the 20-nm node and makes higher $V_T$ options better choices than lower-$V_T$ options for tradeoffs between power and SEU cross-sections.

## 3.5 Proton, High-Energy Neutron and Thermal Neutron Irradiation

### 3.5.1 Experimental Details

For the 14/16-nm bulk FinFET node, experiments with protons, high-energy neutrons and thermal neutrons were also performed to show $V_T$ effects on SEU vulnerability to these radiation particles. Proton experiments were performed at Tri-University Meson Facility (TRIUMF) with 105 MeV proton beam at the University of British Columbia, Vancouver. During testing, the shift registers were clocked at a low frequency of 2.5 MHz with logic input "0". All tests were performed at nominal supply voltage and at room temperature.

High-energy-neutron irradiations were carried out at the Los Alamos Neutron Science Center (LANSCE). The test setup contained 34 test boards (as shown in Figure 3.9), allowing for good statistics. All 34 test boards were placed inline in the beam. The neutron spectrum for testing is shown in Figure 3.10. The total fluence of high-energy neutrons for testing was about $1.3 \times 10^{12}$ $neutrons/cm^2$ for each test IC. During testing, the shift registers were in static mode (clock = "0") with logic input "0". All tests were performed at nominal supply voltage and at room temperature.

Thermal-neutron tests were carried out at University of Missouri Research Reactor (MURR) Center. Figure 3.11 shows the neutron spectrum at MURR thermal-neutron facility with and without a boral plate to filter thermal neutrons. In the unfiltered beam, the thermal neutron flux is $8.4 \times 10^8$ $neutron/cm^2/s$ and the flux of neutrons with energy greater than 0.1 MeV is $2.8 \times 10^7$ $neutron/cm^2/s$ [70]. Tests included two sections: (1) tests with full beam; (2) tests with thermal neutrons blocked ($\sim$99.9% of neutrons with energy less than 0.645 eV were blocked using a boral filter). The overall thermal-neutron-

Figure 3.9: High-Energy-Neutron Test Setup in LANSCE.

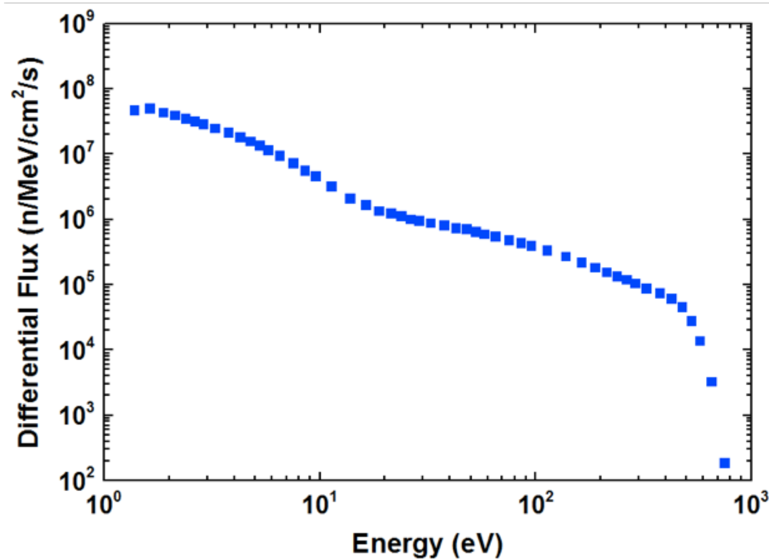



Figure 3.10: High-Energy-Neutron Beam Spectrum in LANSCE.

induced SER was calculated by subtracting SER caused by high-energy neutrons from that caused by the whole spectrum of neutrons. The test setup consisted of 4 test ICs each on a separate PCB. All four PCB were placed inline in the neutron beam. Since the presence of any material in the beam perturbs the thermal-neutron flux, the thermal-neutron flux for each IC was individually characterized by measuring $^{198}Au$ activity at the location of each test IC using a copper gold alloy flux wire. Table 3.5 shows the thermal-neutron flux and

total fluence each test IC received. Actual fluence for each board was used to calculate FIT rates.

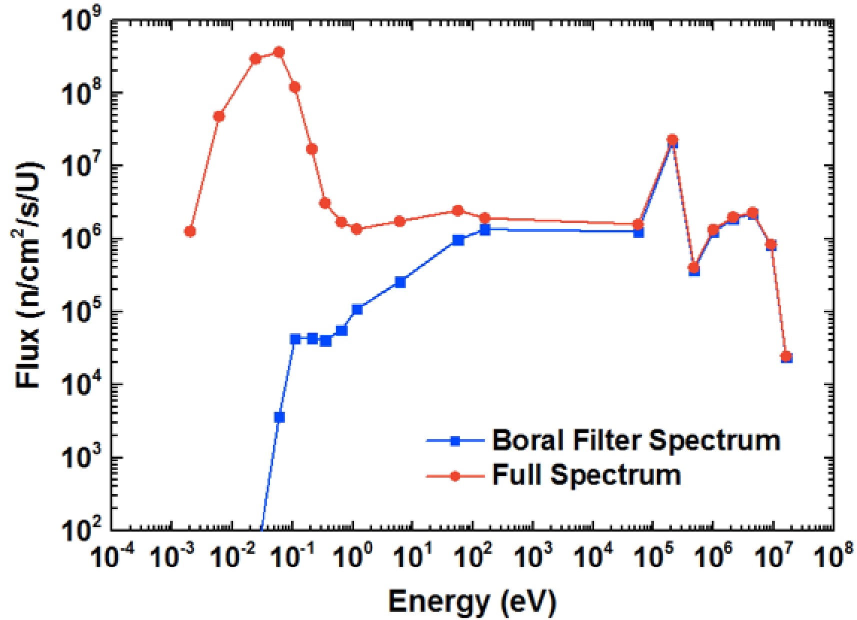



Figure 3.11: Thermal-Neutron Beam Spectrum in MURR.

Table 3.5: Thermal Neutron Flux and Fluence in Tests

| Board # | Thermal Flux ($neutrons/cm^2/s$) | Time Duration (s) | Total Fluence ($neutrons/cm^2$) |
|---|---|---|---|
| 1 | $1.03 \times 10^9$ | 66900 | $6.89 \times 10^{13}$ |
| 2 | $4.13 \times 10^8$ | 66900 | $2.76 \times 10^{13}$ |
| 3 | $1.60 \times 10^8$ | 66900 | $1.07 \times 10^{13}$ |
| 4 | $6.15 \times 10^7$ | 66900 | $4.11 \times 10^{13}$ |

### 3.5.2 Experimental Results

Table 3.6 shows the normalized NYC, sea-level, RT, FIT/MFF numbers for proton and high-energy-neutron and thermal-neutron tests. Data was normalized to FIT of the ULVT design for each particle irradiation respectively to clearly show $V_T$ effects on SEU vulnerability.

Table 3.6: Normalized FIT for DFF with Different $V_T$ Options with Exposure to Protons, High-Energy Neutrons and Thermal Neutrons

| Particles | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|
| Protons | 1.23 | — | — | 1 |
| High-Energy Neutrons | 1.16 | — | — | 1 |
| Thermal Neutrons | 2.51 | 1.71 | 1.20 | 1 |

For thermal-neutron irradiation, thermal neutrons were captured by $^{10}B$ presented in ICs. When a thermal neutron is captured by $^{10}B$, the $^{10}B$ nucleus breaks apart, emitting an excited $^{7}Li$ recoil nucleus (mostly 0.84 MeV), a gamma photon (0.48 MeV) and an alpha particle (1.47 MeV) [71]. The generated lithium recoil and alpha are capable to cause bit-flips to adjacent sensitive nodes in FF designs. As reported in [71], the range of these particles is less than 3 $\mu m$, and in most cases particles beyond $\sim 0.5$ $\mu m$ (from sensitive region) have insufficient energy to induce soft errors. Thus $^{10}B$ containment within $\sim$ 0.5 $\mu m$ from the sensitive region contributes to the overall thermal-neutron-induced SER. For the same DFF design with different $V_T$ option, $^{10}B$ concentration is the same. With low-LET particles generated to cause SEUs, $V_T$ effects on SEU responses should be similar to alpha-particle irradiations, as shown in Table 3.6.

For protons and high-energy neutrons, high-LET particles are also generated through elastic and inelastic reactions to induce soft errors. SEU vulnerability to high-LET particles is not as sensitive to $V_T$ as that to low-LET particles (as shown in Figure 3.5 and in [72]). Therefore, the overall $V_T$ effects on SEU response is reduced, depending on the probability of generation of different LET particles.

## 3.6 Frequency Dependence

With the ICs designed at advanced technology nodes expected to operate in the GHz range of frequencies, it is important to evaluate the frequency response of FF designs and

other sequential circuits for predictive models. Previous work has shown different dependences of SEU cross-section on operating frequency for different FF designs [73, 74]. With transistor current and SET pulse width being affected by threshold voltage, it is highly possible for the SEU cross-section of the DFF designs with different $V_T$ options to have different frequency dependences. For a master-slave DFF (shown in Figure 3.12) operated at GHz range of frequencies, there are two types of upsets in the DFF - upsets in the on-hold stage of the DFF (termed as static upsets) and SET-induced upsets from transparent stage of the DFF (termed as logic upsets). With the transparent stage of the DFF acting like a

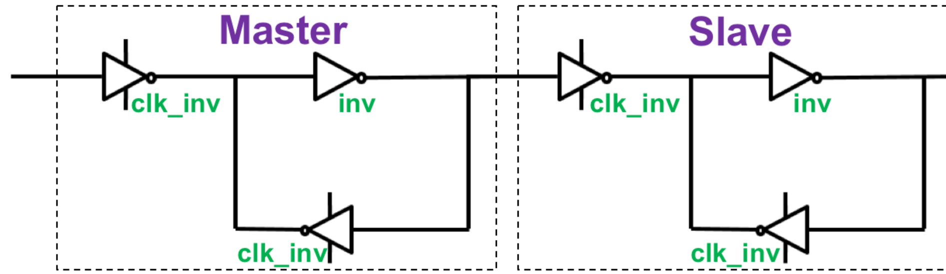



Figure 3.12: Master-Slave Configuration for a Conventional DFF Design.

logic circuit, the SET-induced upset cross-section (or logic upset cross-section) is related to several masking factors, such as electrical masking, logical masking and temporal masking, and has been estimated to be directly related to frequency and SET pulse width [75, 76]:

$$P_{error} = \frac{t_{pw} + t_{SH}}{T + t_{pw}} \tag{3.5}$$

where $t_{pw}$ is the SET pulse width, $t_{SH}$ is the setup-and-hold time, $T = 1/f$ is the clock period.

### 3.6.1 Experimental Details

For evaluating effects of $V_T$ variations on logic upsets, the 14/16-nm bulk FinFET DFF designs were operated at high frequencies to measure the logic SEU cross-sections. These

DFF designs consist of master and slave stages, with one being on-hold stage and another being transparent stage. The transparent stage acts like logic circuits and SET-induced errors become an important portion as frequency increases. Additionally, identical 4-bit comparator logic circuits were designed with different $V_T$ options for the 14/16-nm combinational logic circuits. These logic SEU measurement circuits were implemented in C-CREST configuration [61], as described in Section 3.1.1.

Heavy ion tests were carried out at LBNL with 16 MeV/nucleon cocktail in vacuum, at normal incidence, and at room temperature. Tests were carried out over a frequency range from 2.5 MHz to 1.3 GHz at a supply voltage of 800 mV for DFFs, DICE FFs and combinational logic circuits. The logic inputs for comparator circuits are $A_3A_2A_1A_0 =$ "1000" and $B_3B_2B_1B_0 =$ "0110". The SEU cross-sections as a function of frequency presented below for FFs and logic circuits were obtained with $^{124}Xe^{+43}$ irradiation and the total fluence was run up to $5 \times 10^7\ /cm^2$.

### 3.6.2 Experimental Results for DFF Designs

Results presented in former sections are mostly static upsets since static upsets dominate over dynamic upsets at low frequencies. Figure 3.13 shows the test results of the SEU cross-sections of DFF designs with different $V_T$ options as a function of frequency. As frequency increases, the number of logic upsets starts to increase and may eventually dominate the overall SEU cross-section. For all four designs, the SEU cross-section in-

Table 3.7: Normalized Slope of SEU Cross-Section Curve of DFFs

| SVT | LVT | iLVT | ULVT |
|---|---|---|---|
| 1.00 | 0.80 | 0.80 | 0.38 |

creases with increasing frequency. Since the logic upsets are directly related to SET pulse width, $V_T$ options that yield longer SET pulse width will show faster increase for SEU cross-section as a function of frequency. The SET pulse width is inversely related to the restoring current drive. As a result, the SVT DFF design will have the longest SET pulse

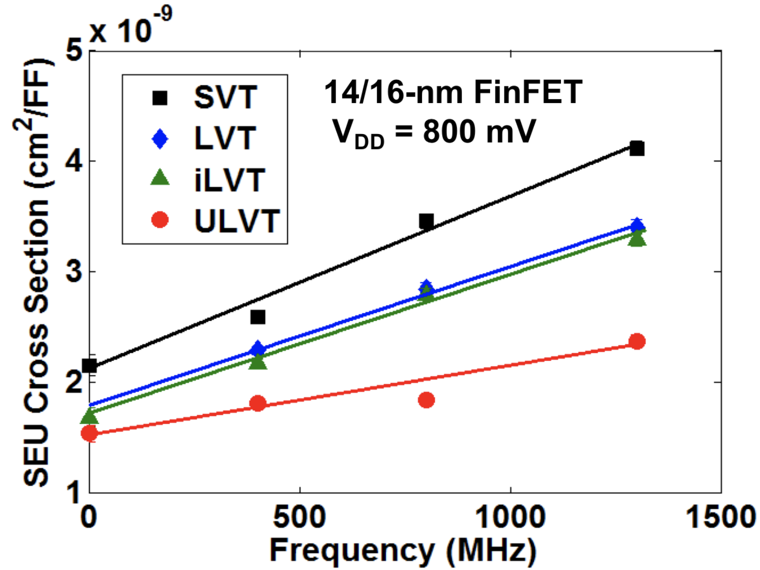



Figure 3.13: Heavy-ion induced SEU cross-section as a function of frequency for the 14/16-nm DFF with different $V_T$ values.

width and ULVT DFF design will have the shortest SET pulse width among all these $V_T$ options. The normalized slope for each $V_T$ option is listed in Table 3.7. As expected, the SVT design shows the highest slope for the SEU cross-section curve as a function of frequency. For ULVT DFF design, the percent increase in SEU cross-section at 1.3 GHz from 2.5 MHz is $\sim$50% while for SVT DFF design, it is $\sim$94%. Assuming that all errors at 2.5 MHz are static errors, this implies that the number of logic errors is almost equal to that of static errors at 1.3 GHz for the SVT design. While for the ULVT design, the number of logic errors is only about half of static errors at the same operating frequency. These curves can help designer make the best $V_T$ choice for specific circuits operated at different frequencies within the range investigated. For example, if frequency goes so high that the dynamic power consumption dominates the overall power consumption, decreasing $V_T$ will lead to increase in standby power consumption, which may not contribute much to overall power consumption, but the SEU cross-section will be reduced significantly.

### 3.6.3 Experimental Results for Logic Circuits

With very few logic gates present in the transparent stage of the DFF, the significant increase in logic errors indicates that they may dominate at GHz range of frequencies. With the combinational logic circuits designed and tested, $^{124}Xe^{+43}$-induced SEU cross-section of frequency tests for 4-bit comparator logic circuits based on different $V_T$ options are shown in Figure 3.14. As DICE FFs are used in the C-CREST structure, the static upsets should be minimal and the logic errors will dominate. The DICE FF design was designed such that sensitive node pairs are placed wide apart to eliminate most upsets. The CREST design implemented with DICE FFs, identical to the ones used for C-CREST designs, showed zero errors for all the tests conducted at 2.5 MHz. The errors observed in C-CREST design at low-frequencies are, thus, all generated from the logic blocks. For high frequency operations, errors from DICE FF were subtracted when calculating logic SEU cross-section (equations are listed in Section 3.1.1). As expected, for these designs, the SEU cross-section increases with frequency and the SVT design shows the highest slope, indicating highest upset probability and longest SET pulse width. The normalized slopes are listed in Table 3.8. The SVT comparator logic SEU cross-section has a slope that is 43% higher than that of the LVT design and 64% higher than that of the ULVT design. The best $V_T$ option can be selected based on power, speed, and SEU performance requirements for specific circuits according to the test results.

Table 3.8: Normalized Slope of SEU Cross-Section Curve of Comparator Logics

| SVT | LVT | ULVT |
|---|---|---|
| 1.00 | 0.70 | 0.61 |

According to above results, threshold voltage also affects logic upsets significantly. For circuits designed to operate at different frequencies, the optimization of power and SEU response can be different and designers should make choices accordingly.

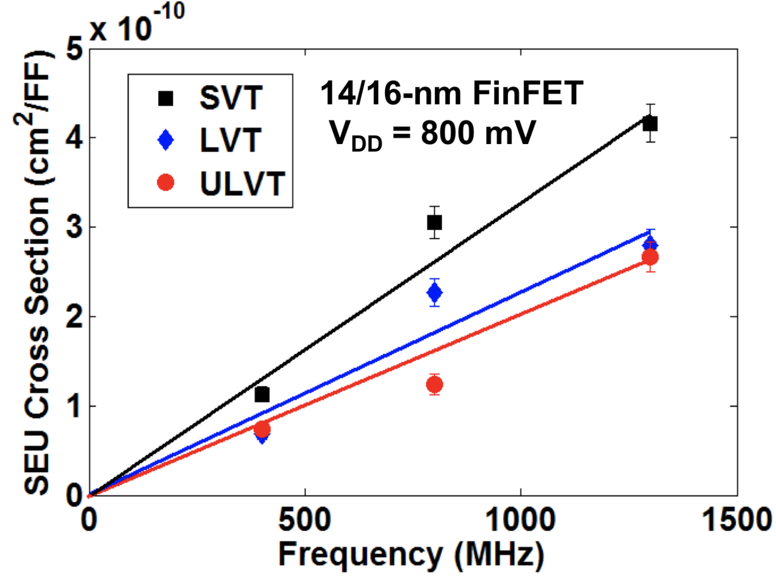



Figure 3.14: Heavy-ion induced SEU cross-section as a function of frequency for 14/16-nm 4-bit comparator logic circuit with different $V_T$ values.

## 3.7 Design Guidelines

As $V_T$ changes, dynamic power is not affected significantly but the static power is changed. Increasing $V_T$ value decreases static power while decreasing $V_T$ increases it since static power is affected by subthreshold leakage current, as shown in the following expression [15]:

$$P_{static} = I_{leakage} \cdot V_{DD} \propto 10^{(V_{GS}-V_T)/S} \cdot V_{DD} \tag{3.6}$$

where S is the sub-threshold slope. Various SEU responses for DFF design with different $V_T$ options have been obtained, which enables a combined power, speed and SEU response analysis for design guidelines to meet circuit performance requirements with least penalty. For the 20-nm bulk planar DFF, SEU response shows an decrease as $V_T$ increases, which indicates designers can achieve better power and SEU performance at the same time by simply select the DFF with HVT option. For the 14/16-nm bulk FinFET DFF, there is a tradeoff between power and SEU performance, which requires further analysis. Following subsections provide simulation results and analysis for power, speed and SEU performance

tradeoffs for the 14/16-nm DFF design with different $V_T$ options. Similar analysis can be carried out for designs in different technology nodes to obtain optimized option for power, speed and SEU performance.

### 3.7.1 Simulations for Power Consumption and Gate Delay

Simulations for power consumption and gate delay were carried out at different supply voltages and frequencies with the 14/16-nm FinFET transistor models from the Arizona State University Predictive Technology Model (ASU PTM) set using Cadence tool suite [65, 66]. Simulation results are listed in Table 3.9 and Table 3.10.

Table 3.9: Power Consumption (nW) for DFF with Different $V_T$ Options across Supply Voltage and Frequency

| Frequency (MHz) | Supply Voltage (mV) | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|---|
| 0 (Static) | 800 | 7.708 | 33.17 | 110.2 | 415 |
| 0 (Static) | 700 | 4.894 | 22.42 | 74.78 | 283 |
| 0 (Static) | 600 | 2.733 | 14.74 | 49.39 | 187.7 |
| 0 (Static) | 550 | 1.824 | 11.96 | 39.64 | 150.9 |
| 2.5 | 800 | 10.17 | 34.67 | 120.4 | 464 |
| 2.5 | 700 | 7.464 | 23.2 | 81.11 | 314.8 |
| 2.5 | 600 | 5.659 | 15.06 | 53.04 | 207.5 |
| 2.5 | 550 | 4.893 | 14.6 | 42.37 | 166.2 |
| 400 | 800 | 322.5 | 369.2 | 459.9 | 780.5 |
| 400 | 700 | 237.4 | 268.7 | 329.5 | 549.1 |
| 400 | 600 | 181.6 | 188.4 | 227 | 372.6 |
| 400 | 550 | 141.1 | 154.4 | 185 | 301.8 |
| 800 | 800 | 642.7 | 709 | 816.9 | 1156 |
| 800 | 700 | 474.1 | 517.8 | 590 | 822.6 |
| 800 | 600 | 340.2 | 364.1 | 409.1 | 562.3 |
| 800 | 550 | 280.4 | 300 | 334.3 | 456.2 |
| 1300 | 800 | 1037 | 1138 | 1262 | 1629 |
| 1300 | 700 | 762.5 | 829.2 | 916.8 | 1167 |
| 1300 | 600 | 557.4 | 586.9 | 641.7 | 803.1 |
| 1300 | 550 | 448.9 | 481.9 | 523.9 | 655.3 |

Table 3.10: Gate Delay (ps) for DFF with Different $V_T$ options across Supply Voltage

| Supply Voltage (mV) | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|
| 800 | 17.76 | 14.11 | 13.08 | 12.25 |
| 700 | 21.11 | 15.71 | 14.27 | 13.11 |
| 600 | 27.43 | 18.3 | 16.14 | 14.45 |
| 550 | 33.1 | 20.3 | 17.51 | 15.41 |

The overall power and gate delay can be expressed in following equations [15]:

$$\begin{aligned} Power &= P_{dynamic} + P_{static} = \alpha \cdot C \cdot V_{DD}^2 \cdot f + \beta \cdot V_{DD} \cdot 10^{-V_T/S} \\ Delay &= \frac{\gamma \cdot C \cdot V_{DD}}{(V_{DD} - V_T)^2} \end{aligned} \tag{3.7}$$

Therefore, power consumption decreases with increasing $V_T$ and decreasing supply voltage and frequency. Gate delay decreases with decreasing $V_T$ and increasing supply voltage but is independent with frequency, which is consistent with simulation results. At static operations, dynamic power is excluded and the overall power mainly comes from static power. As frequency increases, dynamic power increases. By subtracting from the power at static mode, dynamic power and static power can be separated. $V_T$ options mainly affects static power, with smaller effects on capacitance that slightly changes the dynamic power.

### 3.7.2 SEU Cross-Sections for DFF with Different $V_T$ options

SEU performance characterization results are listed in Table 3.11 and Table 3.12. With these results, case study for design guidelines can be carried out to provide designers with better idea on $V_T$ option selection for different applications.

### 3.7.3 Case Study

With results available in this work, three cases have been studied as examples to guide designers in choosing $V_T$ options for different applications. Situations can be more complex

Table 3.11: Alpha-Particle-Induced SEU cross-Section ($\times 10^{-11}$ $cm^2/FF$) for DFF with Different $V_T$ Options across Supply Voltage at 2.5 MHz

| Supply Voltage (mV) | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|
| 800 | 0.61 | 0.48 | 0.36 | 0.30 |
| 700 | 1.10 | 0.83 | 0.67 | 0.52 |
| 600 | 2.34 | 1.65 | 1.20 | 1.11 |
| 550 | 3.21 | 2.35 | 1.75 | 1.45 |

Table 3.12: $^{124}Xe^{+43}$-Induced SEU cross-Section ($\times 10^{-9}$ $cm^2/FF$) for DFF with Different $V_T$ Options across Frequency at Nominal Supply Voltage

| Frequency (MHz) | SVT | LVT | iLVT | ULVT |
|---|---|---|---|---|
| 2.5 | 2.16 | 1.82 | 1.69 | 1.54 |
| 400 | 2.60 | 2.29 | 2.18 | 1.82 |
| 800 | 3.46 | 2.85 | 2.80 | 1.84 |
| 1300 | 4.12 | 3.41 | 3.29 | 2.38 |

in real applications and are simplified in this work for a general idea of design guidance. Similar analysis can be carried out for other specific applications.

Case 1: A circuit includes DFF designs that operate at 2.5 MHz, which has requirements that alpha-particle-induced SEU cross-section is less than $1.5 \times 10^{-11}$ $cm^2/FF$ and per DFF delay is less than 15 $ps$. With these constraints, designs meet specifications are LVT DFF operated at 800 mV, iLVT DFF operated at 800 mV and 700 mV, ULVT design operated at 800 mV, 700 mV and 600 mV (other voltages between 600 mV to 800 mV are not discussed). The power consumption of these designs are listed in Table 3.13. The best option is to use LVT design at 800 mV, with power consumption of 34.67 nW per DFF.

Table 3.13: Case Study 1

| Design | LVT @ 800 mV | iLVT @ 800 mV | iLVT @ 700 mV | ULVT @ 800 mV | ULVT @ 700 mV | ULVT @ 600 mV |
|---|---|---|---|---|---|---|
| Power (nW) | 34.67 | 120.4 | 81.11 | 464 | 314.8 | 207.5 |

Case 2: A circuit includes DFF designs that operate at 2.5 MHz, which has requirements

that power consumption of each DFF is less than 150 nW and per DFF delay is less than 15 $ps$. This design need to get SEU sensitivity as low as possible. With these constraints, designs meet specifications are LVT DFF operated at 800 mV, iLVT DFF operated at 800 mV and 700 mV (other voltages between 600 mV to 800 mV are not discussed). The power consumption of these designs are listed in Table 3.14. The best option is to use iLVT design at 800 mV, with SEU cross-section per DFF of 0.36 $\times 10^{-11}$ $cm^2/FF$.

Table 3.14: Case Study 2

| Design | LVT @ 800 mV | iLVT @ 800 mV | iLVT @ 700 mV |
|---|---|---|---|
| SEU cross-Section ($\times 10^{-11}$ $cm^2/FF$) | 0.48 | 0.36 | 0.67 |

Case 3: A circuit designed for space use includes DFF designs that operate at a frequency no less than 800 MHz, in which power consumption is increased significantly compared to designs at low frequencies. The circuit has requirements that equivalent $^{124}Xe^{+43}$-induced SEU cross-section is less that $2.5 \times 10^{-9}$ $cm^2/FF$ and per DFF delay is less than 15 $ps$. For nominal supply voltage operation, only ULVT DFF operated at 800 MHz and 1300 MHz meet these requirements. To reduce power consumption, an operating frequency of 800 MHz should be chosen, with power consumption of 1156 nW per DFF. With additional SEU response data, if the ULVT design operated at lower voltages also meets SEU performance specification, lower voltage can be applied and power consumption can be reduced significantly since dynamic power dominates at high frequencies.

Table 3.15: Case Study 3

| Design | ULVT @ 800 MHz | ULVT @ 1300 MHz |
|---|---|---|
| Power (nW) | 1156 | 1629 |

## 3.8 Summary

Threshold voltage is an important factor that affects power, speed and SEU performance of microelectronic systems. In this chapter, $V_T$ effects on SEU responses of DFF in the 20-nm bulk planar and the 14/16-nm bulk FinFET technology nodes have been evaluated through irradiation tests and circuit-level simulations. For high-LET particle irradiations, effects of $V_T$ on low-frequency SEU cross-sections are not significant in both technologies. For low-LET particle irradiation for the 20-nm bulk planar DFF, increased $V_T$ leads to decreased SEU cross-section, which means increasing $V_T$ is an efficient way to decrease both power and SE sensitivity. For low-LET particle irradiation for the 14/16-nm bulk FinFET DFF, increased $V_T$ results in increased SEU vulnerability. Tradeoffs have to be made to achieve either lower power or better speed and SEU vulnerability. Based on simulation results, different $V_T$ effects are due to different changing rates in SET pulse width and feedback loop delay as $V_T$ changes in the DFF design, which is mainly caused by the difference in the physical structure, doping level, transistor size, and transistor spacing. $V_T$ effects on logic upsets in DFF and logic circuits were also investigated, showing higher increasing slope for higher $V_T$ options compared to lower $V_T$ options. With these characterizations and simulation results for power and delay, case study have been carried out to provide design recommendations when choosing $V_T$ options for specific applications.

# Chapter 4

# Effects of Well Structure on Single-Event Upset Responses for FinFET Technologies

Triple-well technology provides better isolation of transistors from the substrate to reduce substrate noise coupling and enable easier threshold voltage adjustment for specific applications [19, 20, 21]. For FinFET technologies, physical structure changes significantly compared to planar technologies and charge collection mechanism evolves. The additional deep-n-well introduced by triple-well technology further alters the charge-collection mechanism, thus leading to unpredictable SEU responses in FinFET technologies. In this chapter, the SEU responses for FF designs with dual- and triple-well structures in a 14/16-nm bulk FinFET technology will be characterized to show the effect of well structure on FF SE vulnerability in this technology. 3D TCAD simulations will be carried out to explore the underlying charge collection mechanism for dual- and triple-well designs, understanding how well structure affects SEU responses in FinFET technologies.

## 4.1 Test Circuits

Test chips were fabricated in a 14/16-nm bulk FinFET technology at a commercial foundry. FF chains with dual-well and triple-well guard-gate FF designs were implemented in CREST configuration [57]. The guard-gate FF was designed with a two-input Transition AND Gate (TAG) in which one input is delayed with two inverters [77]. Figure 4.1 shows the schematic design of a Guard-Gate FF. It is a radiation-tolerant design and eliminates all SET pulses shorter than the delay for the second input. The die size was $2\ cm \times 2\ cm$. Low threshold voltage (LVT) transistors were used in all FF designs. The test structure and supplemental clock generation, error detection and latch circuits are the same as shown in Figure 3.1. All sub-circuits other than shift registers were designed with Triple Modular Redundancy (TMR) to eliminate all errors from support circuits.

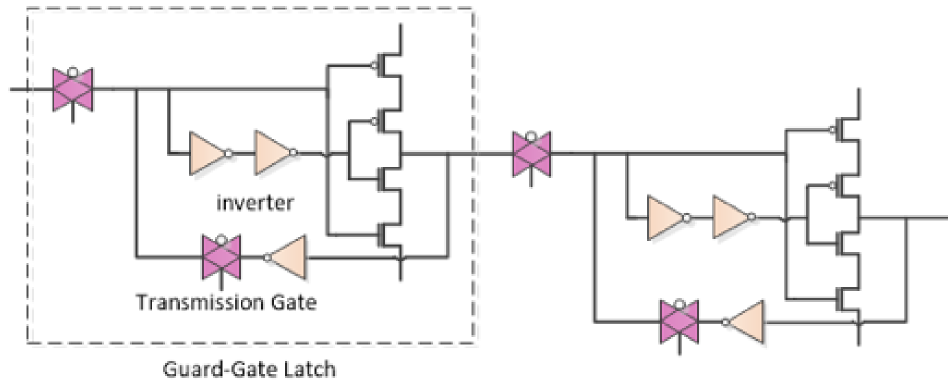



Figure 4.1: Schematic design of a Guard-Gate FF [58].

## 4.2 Heavy-ion Irradiation

### 4.2.1 Experimental Details

Heavy ion tests were carried out at Lawrence Berkeley National Laboratory (LBNL) with 10 $MeV/nucleon$ cocktail. Particle LET values range from 0.89 $\sim$ 46.92 $MeV \cdot cm^2/mg$, as listed in Table 4.1. All heavy-ion tests were conducted in vacuum with normal

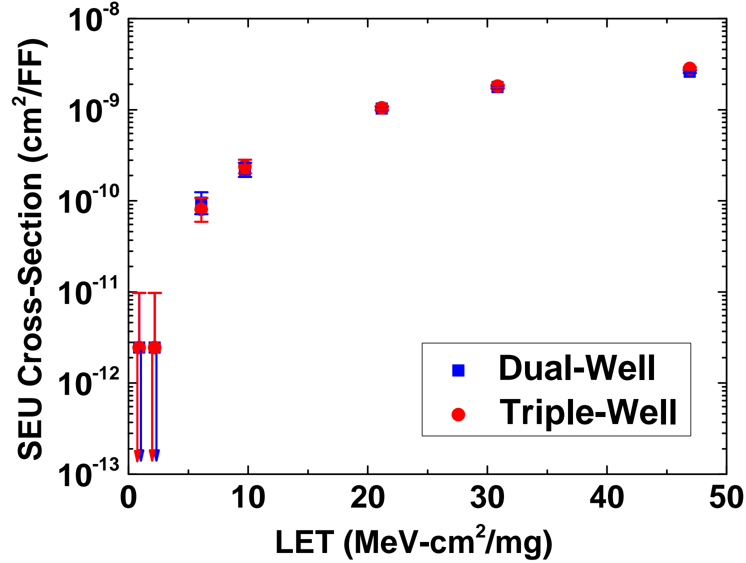
Table 4.1: 10 MeV/nucleon Cocktail Components

| Ion | Energy ($MeV$) | LET ($MeV \cdot cm^2/mg$) | Range ($\mu m$) |
|---|---|---|---|
| $^{11}B^{+3}$ | 108.01 | 0.89 | 305.7 |
| $^{18}O^{+5}$ | 183.47 | 2.19 | 226.4 |
| $^{29}Si^{+8}$ | 291.77 | 6.09 | 141.7 |
| $^{40}Ar^{+11}$ | 400.00 | 9.74 | 130.1 |
| $^{65}Cu^{+18}$ | 659.19 | 21.17 | 108.0 |
| $^{84}Kr^{+24}$ | 885.59 | 30.86 | 109.9 |
| $^{124}Ag^{+34}$ | 1039.42 | 46.92 | 90.0 |

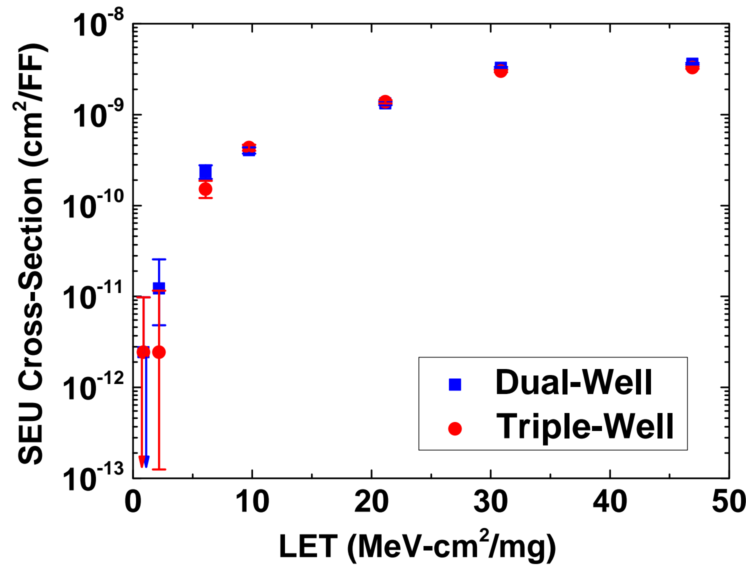
incidence and at room temperature. The input of the shift register chains was set to logic “0” to eliminate possible errors due to ion hits on clock tree from the final error counts. Supply voltage was varied from 600 mV to 800 mV. The nominal supply voltage for this technology is 800 mV. All tests were conducted with the shift registers being clocked at 2.5 MHz of frequency.

### 4.2.2 Experimental Results

Figure 4.2 shows the SEU cross-section test results for dual-well and triple-well guard-gate FF designs with particle LET ranging from 0.89 $\sim$ 46.92 $MeV \cdot cm^2/mg$. When the




(a) $V_{DD} = 800\ mV$



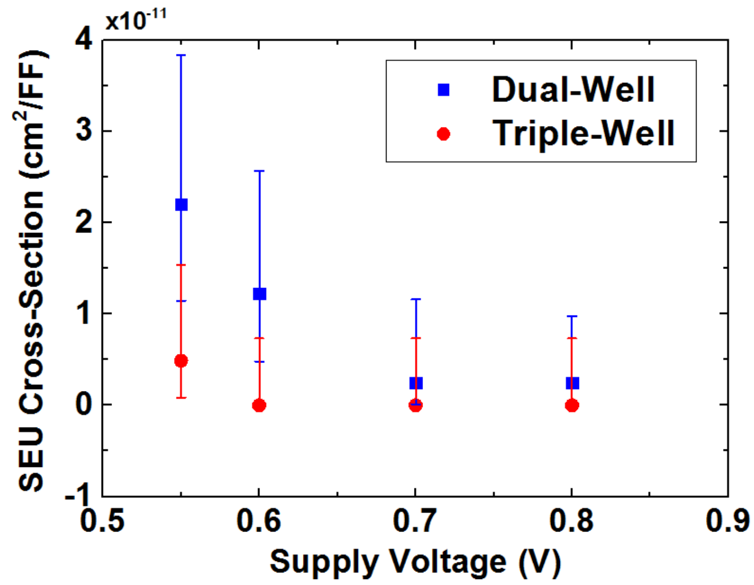

(b) $V_{DD} = 600\ mV$

Figure 4.2: Heavy ion-induced SEU cross-sections of dual-well and triple-well FF designs with guard-gates as a function of LET values for different voltage operations.

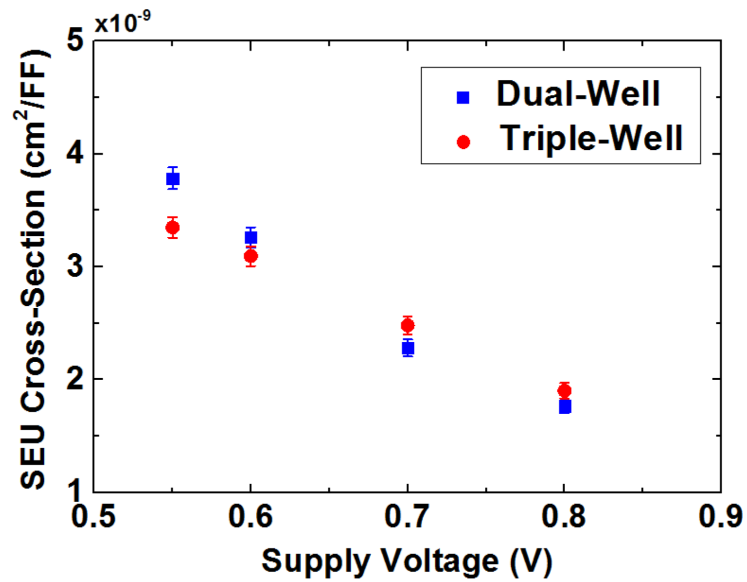
error counts are less than 100, a 95% confidence level was used to calculate error bars

while for error counts larger than 100, error bars represent 1 $\sigma$ standard error [64]. Figure 4.2 (a) results are for operation at the nominal supply voltage of 800 mV. At this supply voltage, both dual- and triple-well designs show similar SEU cross-sections and no errors were observed for particles with LET values of 0.89 and 2.19 $MeV \cdot cm^2/mg$. For low-LET particle strikes, average SET pulse widths are narrower compared that generated by high-LET particle strikes. When these SET pulses are generated in a guard-gate design, SET pulses with width less than two-inverter delay will be masked. Results shown that at nominal supply voltage, most pulses generated by particles with LET value less than 2.19 $MeV \cdot cm^2/mg$ are eliminated by the guard-gate design for both dual- and triple-well structures. Figure 4.2 (b) shows results for the supply voltage of 600 mV. The SEU cross-sections are similar for both dual-well and triple-well designs for particles with high LET values, but for particles with low-LET values, the triple-well design shows better SEU performance than the dual-well design, which indicates charge collection in the dual-well design generated more SET pulses longer than two-inverter delay and caused SEUs in the guard-gate design.

To clearly show the effects of well-structure on SEU responses of FF designs, low- and high-LET particle-induced SEU cross-sections across a voltage range are plotted separately, as shown in Figure 4.3. For low-LET $^{18}O^{+5}$ irradiation, no upsets observed at nominal supply voltage. As voltage reduces, the triple-well guard-gate FF starts to show superior SEU performance than the dual-well design. For high-LET $^{84}Kr^{+24}$, the difference between SEU responses of the dual- and triple-well designs becomes smaller since high-LET particles deposit large amount of charge for collection and generate wide SET pulse width for most strikes. At supply voltage of 700 mV and 800 mV, the dual-well design shows slightly lower SEU cross-section while at lower supply voltages, the triple-well design shows lower SEU probability.



(a) $^{18}O^{+5}$ ($2.19\ MeV \cdot cm^2/mg$)



(b) $^{84}Kr^{+24}$ ($30.86\ MeV \cdot cm^2/mg$)

Figure 4.3: Heavy ion-induced SEU cross-sections of dual-well and triple-well FF designs with guard-gates as a function of voltage for particles with different LET values.

## 4.3 Alpha Particle Irradiation

### 4.3.1 Experimental Details

To further investigate low-LET particle irradiations, alpha particle radiation tests were carried out at Vanderbilt University, using the 1 $cm \times 1$ $cm$ size 5.4 $MeV$ 10 $\mu Ci$ $^{241}Am$ button source. The alpha source was put right above the IC with an air gap less than 1 mm. The alpha emissivity at this distance was determined to be $\sim$1000 $alpha/mm^2/sec$ with a mean energy of $\sim$5 MeV, so the LET value of alpha particles is less than 1 $MeV \cdot cm^2/mg$. The operational frequency of the shift registers was 2.5 MHz with input to the shift register held at logic "0". The supply voltage was varied from 550 mV to 850 mV to investigate the SEU performance of these FF designs at room temperature.

### 4.3.2 Experimental Results

A comparison of the SEU cross-sections for dual-well and triple-well guard-gate FF designs is shown in Figure 4.4. Due to the radiation-tolerant design of guard-gate FF

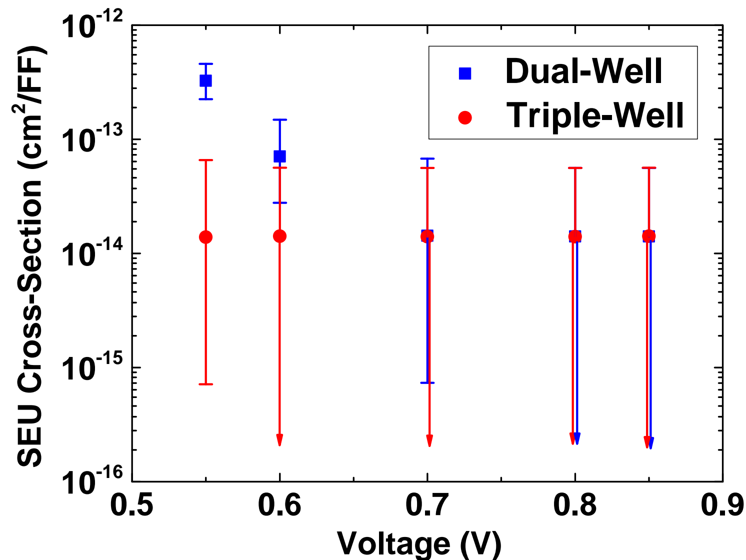



Figure 4.4: Alpha particle-induced SEU cross-sections of dual-well and triple-well guard-gate FF designs as a function of supply voltage.

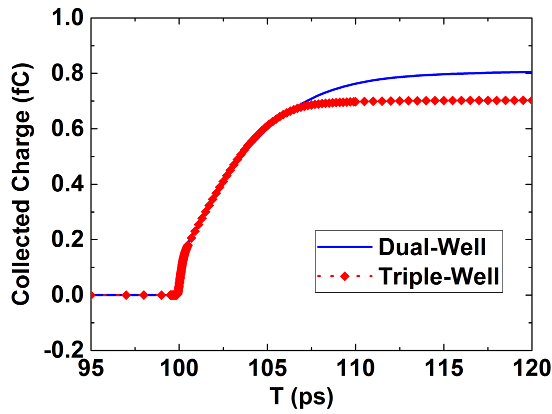
(most pulses that are shorter than two-inverter delay do not cause an upset), very few errors were observed at the nominal supply voltage. The dual-well design starts to show errors at a supply voltage of 700 mV while the triple-well guard-gate FF does not show errors until the supply voltage is reduced to 550 mV. Data shown in Figure 4.4 clearly show the superior performance of triple-well designs over dual-well designs for alpha particles at reduced supply voltages. This is consistent with low-LET heavy-ion irradiation results.

## 4.4 Simulations and Discussion

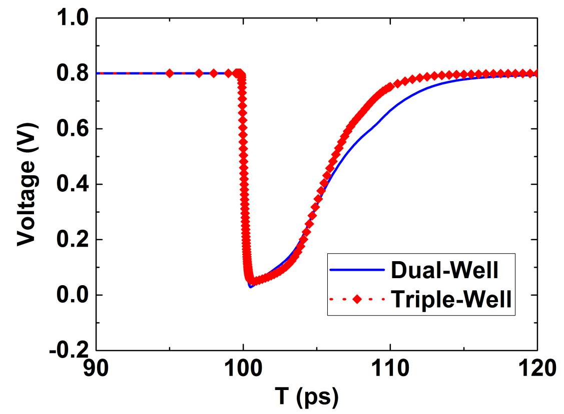
### 4.4.1 3D TCAD Simulations for 14/16-nm Bulk FinFET Technology

Simulations were carried out using Synopsys Technology Computer-Aided Design (TCAD) tools. The FinFET devices use a two-fin structure and the electrical characteristics were calibrated against the ASU PTM [66]. The heavy-ion tracks were modeled as gaussian tracks with characteristic radius of 10 *nm* and deposition time of 50 $fs$. More details of the model and parameters, such as recombination and meshing, can be found in [78]. The modeled heavy-ion particle LET values are 1 and 60 $MeV \cdot cm^2/mg$. All the reported simulations are for normal incidence particle hits at the drain area of an OFF-state NMOS FinFET of an inverter structure. Simulation variations include particle LET value and supply voltage.

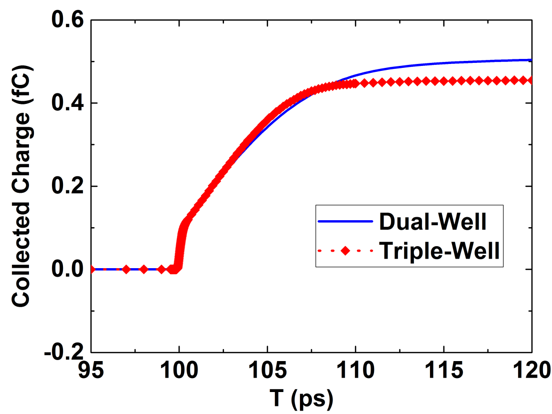
Figure 4.5 shows the collected charge and the SET pulse width for dual-well and triple-well designs at supply voltages of 800 mV and 600 mV for a particle LET value of 1 $MeV \cdot cm^2/mg$. As shown in the figure, the saturation value of the collected charge for the triple-well design is less than that of the dual-well design. For a FinFET structure, charge collection is less and charge-sharing effect is reduced compared to a planar structure due to the narrow connection between the drain region and the substrate [56]. With the presence of the third well, more charge will be confined and charge sharing between adjacent transistors will increase, but charge collection from outside the deep n-well is eliminated. Besides, the deep-n-well provides additional charge sink and collects confined charge. These



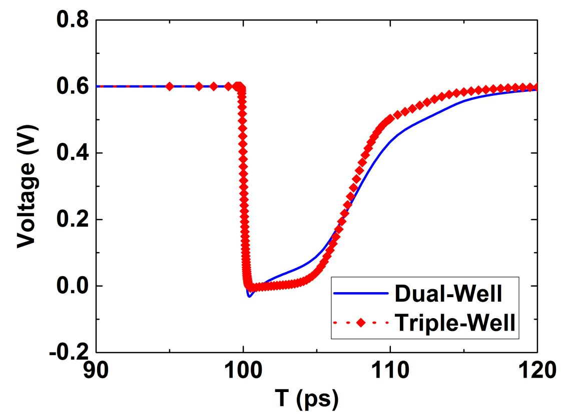

(a) Charge Collection at $V_{DD}$ = 800 mV




(b) SET Pulse Width at $V_{DD}$ = 800 mV




(c) Charge Collection at $V_{DD}$ = 600 mV



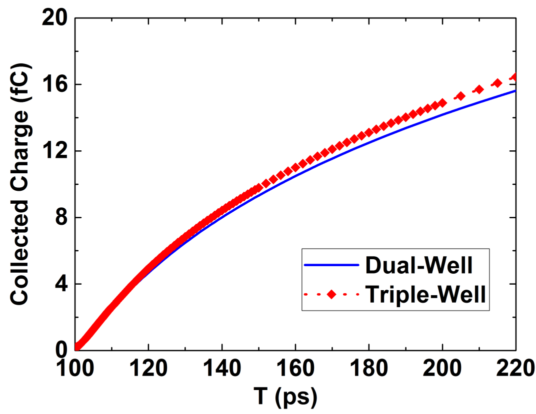

(d) SET Pulse Width at $V_{DD}$ = 600 mV

Figure 4.5: Collected charge and SET pulse width for dual-well and triple-well designs when a particle with LET = 1 $MeV \cdot cm^2/mg$ strikes the drain of an inverter with OFF-state NMOS.

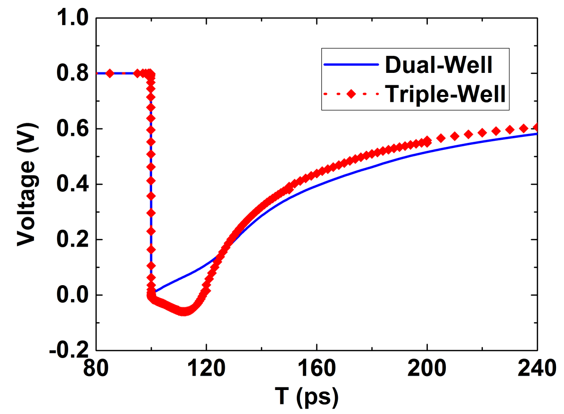
are competing factors and the dominant one determines the trend of overall charge collection. For low-LET particles, the charge-sharing effect is insignificant (with less deposited charge compared to high-LET particles) while the ranges of particles are longer and charge deposits further than high-LET particles (outside the deep n-well), which may lead to the triple-well design collects less total charge than the dual-well design. However, for modern memory cells, the saturated collected charge (mostly dominated by a long current diffusion tail) alone is no longer sufficient to determine the SEU response of the cell because dif-

fusion may go on far longer than circuit response time [79]. Collected charge value must be used along with resultant SET pulse width to determine SEU response of the cell. As shown in Figure 4.5, the Full-Width-Half-Max (FWHM) SET pulse width for both of the designs at nominal supply voltage show similar values. For $V_{DD}$ = 800 mV, the simulated SET pulse widths (at 0.4 V) for both dual- and triple-well designs are similar (∼5ps). Both designs also exhibit similar charge collection at 105 ps. This observation is important because it explains the similar SEU cross-sections observed in the experiments for both dual- and triple-well FF designs at low-LET values at nominal supply voltage. As supply voltage reduces to 600 mV, the pulse width increases by ∼50% while the feedback loop delay increases by ∼25% (3.10), leading to an increased SE vulnerability. The SET pulse width may get closer to the pulse width threshold that can cause an upset compared to nominal supply voltage operation. Simulation results show that for lower operating voltage ($V_{DD}$ = 600 mV), the triple-well design has a slightly shorter (∼5%) FWHM SET pulse width compared to the dual-well design. For SET pulses with width around the threshold, small differences in pulse width can result in observable differences in SEU responses, as shown in Figure 4.3 (a) and Figure 4.4, where a decrease in SEU cross-section of the triple-well design at low-LET values are observed compared to the dual-well design.

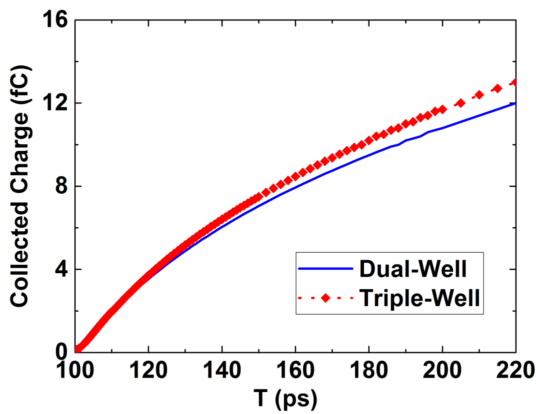
For high-LET particles (for example, LET of 60 $MeV \cdot cm^2/mg$), the collected charge and the SET pulse width are also different for dual- and triple-well designs, as shown in Figure 4.6. For high-LET particles, charge collection due to charge sharing increases with increased deposited charge. As the ranges of high-LET particles decrease, there is less portion of charge deposited outside the deep n-well. Combining these contributing factors, the triple-well design has more charge collected than the dual-well design according to simulation results. However, the collected charge and SET pulses for most strikes for both designs are significantly wider than the feedback loop delay to cause upsets (to a first degree, SET pulse width needs to be comparable to the feedback loop delay of the latch to cause an upset). Since both FF cells will probably experience an upset for such a particle,



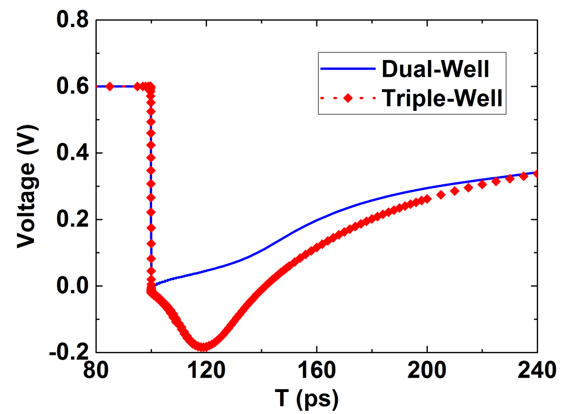

(a) Charge Collection at $V_{DD}$ = 800 mV




(b) SET Pulse Width at $V_{DD}$ = 800 mV




(c) Charge Collection at $V_{DD}$ = 600 mV




(d) SET Pulse Width at $V_{DD}$ = 600 mV

Figure 4.6: Collected charge and SET pulse width for dual-well and triple-well designs when a particle with LET = 60 $MeV \cdot cm^2/mg$ strikes the drain of an inverter with OFF-state NMOS.

difference in SEU cross-section will be very small for two designs despite different charge collection and SET pulse widths.

The drain charge collection values for the dual- and triple-well design at $t = 100\ ps$ after particle strikes are listed in Table 4.2 and the triple-well design collects less charge than the dual-well one for low-LET particle strikes. For high-LET particles strikes at reduced supply voltages, although the triple-well design collects more charge than the dual-well design, the ${}^{84}Kr^{+24}$ irradiation results show lower SEU cross-section for the triple-well

Table 4.2: Charge Collection of Dual- and Triple-Well OFF-State NMOS Inverters

| Design | Supply Voltage (mV) | Charge (fC) @ LET = 1 $MeV \cdot cm^2/mg$ | Charge (fC) @ LET = 60 $MeV \cdot cm^2/mg$ |
|---|---|---|---|
| Dual-Well | 800 | 0.81 | 14.2 |
| Triple-Well | 800 | 0.70 | 14.9 |
| Dual-Well | 600 | 0.53 | 10.8 |
| Triple-Well | 600 | 0.45 | 11.7 |

design. This is mainly due to single-event upset-reversal (SEUR) mechanism [51, 52]. Although the charge-sharing effect is reduced in FinFET technologies [56], presence of the third well of the triple-well design increases charge sharing between NMOS transistors inside the same well due to charge confinement. Figure 4.7 show a schematic design of a conventional D-latch with input = “0”. When clock = “1”, N3 and P4 are on while N4

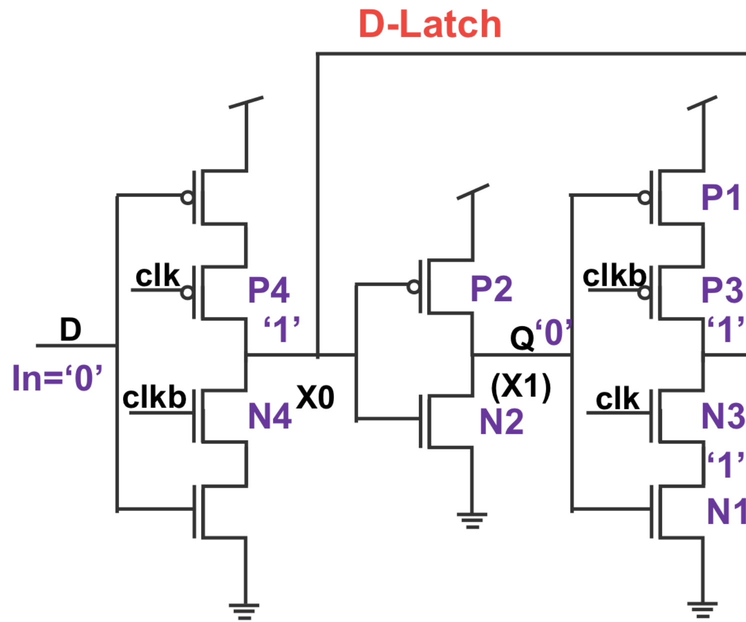



Figure 4.7: Schematic design of a conventional D-latch.

and P3 are off. The latch is in hold stage. When the OFF-state NMOS N1 gets stricken and collects charge, an SET pulse will be generated, causing an upset in the cell if enough charge is collected. This pulls node “X0” from “1” to “0”. N2 is turned off and P2 is turned on, which leads to node “Q” from “0” to “1”. If N2 is inside the same deep-n-well as

N1, confined charge inside the p-well provides more charge to be collected by N2 through delayed diffusion process. If N2 collects enough charge to pull back node “Q” to “0” and recover node “X0” to “1”, the upset in the D-latch disappears. The SEUR mechanism can happen when the separation between transistors is small and charge confinement is high enough (a combination of these factors), leading to reduced triple-well SEU cross-section even with higher charge collection compared to the dual-well design.

### 4.4.2 Comparison between Planar and FinFET technologies

3D TCAD inverter cells were also developed in 40-nm and 28-nm CMOS technologies for both dual-well and triple-well structures. The electrical characteristics of planar devices were calibrated to 40-nm and 28-nm PDK. Simulations of drain charge collection for the dual-well design, drain and deep-n-well charge collection of the triple-well design when a particle (LET = 1 $MeV \cdot cm^2/mg$) strikes the OFF-state NMOS inverter were carried out at nominal supply voltages ($V_{DD}$ = 1.1 V for the 40-nm technology, $V_{DD}$ = 900 mV for the 28-nm technology and $V_{DD}$ = 800 mV for the 14/16-nm technology) for three technologies. Results are listed in Table 4.3. For the 40-nm and 28-nm CMOS technology nodes, the drain area of the triple-well design collects more charge than that of the dual-well design due to charge confinement. The charge collected by the deep-n-well (additional charge sink path) is comparable or less than the drain charge collection with presence of the third well. On the contrary, the deep-n-well becomes the preferred sink of charge dissipation in the triple-well design for the 14/16-nm FinFET node, with more confined charge being collected by the third-well. The effect of the additional charge sink outweighs enhanced charge collection that can be caused by charge confinement, leading to the drain area collecting less charge and subsequently lower SE vulnerability compared to the dual-well design. This is mainly due to the differences in physical structure of FinFET and planar transistors. The narrow connection between drain and substrate greatly decreases the charge collection from the substrate, reducing the effect of charge confinement and enhancing the effect of

additional charge sink.

Table 4.3: Charge Collection of Dual- and Triple-Well OFF-State NMOS Inverters for Three Technologies with A Particle Strike (LET = 1 $MeV \cdot cm^2/mg$)

| Technology Node | Design | Charge (fC) @ Drain | Charge (fC) @ Deep-N-Well |
|---|---|---|---|
| 14/16-nm | Dual-Well | 0.81 | — |
| 14/16-nm | Triple-Well | 0.70 | 1.68 |
| 28-nm | Dual-Well | 2.57 | — |
| 28-nm | Triple-Well | 3.32 | 2.72 |
| 40-nm | Dual-Well | 2.77 | — |
| 40-nm | Triple-Well | 6.50 | 2.67 |

## 4.5 Summary

Triple-well technique has been widely used for isolation and threshold-voltage adjustment by the semiconductor industry. In this chapter, SEU responses of dual-well and triple-well guard-gate FF designs in the 14/16-nm bulk FinFET technology node were characterized. Results show that both alpha-particle and heavy-ion-induced SEU cross-sections exhibit insignificant differences at nominal supply voltage between triple-well and dual-well designs. At reduced supply voltages, the triple-well design shows lower SEU cross-section than the dual-well design for low-LET particle irradiation, especially for alpha particles. Simulations results show significant differences in charge collection and SEU responses for FinFET nodes compared to planar nodes. For previous planar nodes, the drain area collects more charge in the triple-well design due to charge confinement with the presence of the deep-n-well and the triple-well designs show inferior SEU performance than the dual-well designs. For the 14/16-nm bulk FinFET technology, the third well in the triple-well design acts as the preferred sink for charge dissipation. The drain area in the triple-well design actually collects less charge compared to the dual-well design because the effect of additional charge sink outweighs charge confinement effect, leading to superior SEU performance of the triple-well design than the dual-well design for low-LET particle irradiations at reduced

supply voltages. The differences are mainly caused by the significantly differences in physical structures. With the superior (or at least similar) SEU characteristics of the triple-well design in FinFET technologies, designers can apply the triple-well technique for specific applications to provide better isolation without scarifying SEU performance.

# Chapter 5

## Stability of Designer-Controlled Parameter Effects against Temperature and Angular Incidence

Some operation conditions for microelectronic systems are not controllable but have to be faced with. From a designer's perspective, the advantage of selected designer-controlled parameters should remain against different operational conditions that the IC may encounter. Effects of supply voltage variations have been included in former chapters. In this chapter, effects of temperature variations and particle incident angles on SEU vulnerability of the 14/16-nm FinFET FF designs will be investigated. With 3D TCAD and circuit-level simulations and theoretical analysis, underlying mechanisms for temperature and angular effects on SEU responses will be revealed. With $V_T$ and well-structure effects against temperature and incident angle being revealed, designers can choose $V_T$ and well options more properly with temperature and angular effects take into consideration.

### 5.1 Temperature Effects

With scaling down of CMOS technology, the operating temperature of high performance ICs is steadily increasing due to increased power density. The resultant increased die temperature significantly degrades carrier mobility and $V_T$, leading to changes in the transistor currents [80, 81, 82, 83]. Reduced transistor currents increase SET pulse width and logic gate delays. The degradation rates with temperature for these two competing factors (SET puSEU responselse width and logic gate delay) determine the overall SER for a given FF design. Previous results on planar technologies have shown significant increases in FF SER with increasing temperature [84, 85]. Compared to planar transistors, FinFET transistors may experience even higher operating temperatures due to self-heating effects [86]. Since soft errors are the most pressing reliability problem for ICs fabricated in ad-

vanced technology nodes, and most of these ICs operate at elevated temperature, it is very important to understand the effects of temperature on SEU responses.

### 5.1.1 Background

To first order, when an SET pulse width exceeds the feedback loop delay of the FF cell, an upset will occur. Thus, the SEU response for FF cells depends on transistor current, nodal capacitance, and SET pulse width. Varying temperature causes changes in the carrier mobility and $V_T$ [87, 88, 89] through changes in phonon scattering and the Fermi level. These two competing factors mostly determine the overall temperature effect on transistor currents. The temperature dependence of transistor currents can vary for different technology, material and structures [80, 81, 82, 83]. Reductions in transistor current may result in a longer slightly SET pulse width after an ion strike and a slightly longer feedback loop delay for an FF cell. A longer SET pulse width increases SEU vulnerability, while a longer feedback loop delay decreases it. Similarly, an increase in transistor current leads to a shorter SET pulse width (decreasing SEU vulnerability) and a shorter feedback loop delay (increasing SEU vulnerability). These competing factors determine the final SEU response of the FF cell.

The transistor current is directly related to the carrier mobility and supply voltage and inversely related to the $V_T$. At older technology nodes, the changes in transistor currents due to changes in $V_T$ are small because percent changes in $V_{GS} - V_T$ are small (ratio of $V_T$ to supply voltage is small). On the contraty, decreases in carrier mobility due to increasing temperature strongly influence the transistor currents. As technologies scale, supply voltages have been reduced considerably. This has resulted in increased influence of changes in $V_T$ on transistor current with temperature. When the temperature effect of $V_T$ outweighs that of carrier mobility, the transistor currents will increase as temperature increases, leading to the cell delay decreasing with increasing temperature. This inverted temperature dependence (ITD) is called temperature effect inversion (TEI) [90]. At ad-

vanced technologies, temperature dependence for individual transistors with different $V_T$ are also different. For an industrial 65-nm, low-power technology node, the logic gate delay of high $V_T$ transistors decreases with temperature, but for low $V_T$ transistors, the logic delay remains constant or increases with temperature [45]. For a specific technology, as temperature changes, the transistor current and cell delay will vary due to the competing mechanisms of the carrier mobility and $V_T$.

### 5.1.2 Simulations and Implications

3-D TCAD and circuit level simulations were carried out to investigate the temperature dependence of transistor currents, SET pulse width and feedback loop delay for both the 20-nm bulk planar and the 14/16-nm bulk FinFET nodes. The Cadence tool suite was used with the foundry-supplied PDK to carry out circuit-level simulations. Figure 5.1 shows the simulation results for transistor currents for the 20-nm technology node at low and high temperatures at 850 mV. The transistor current increases with temperature, but the increases are very small as the temperature increases from 27 °C to 127 °C. Transistor current sim-

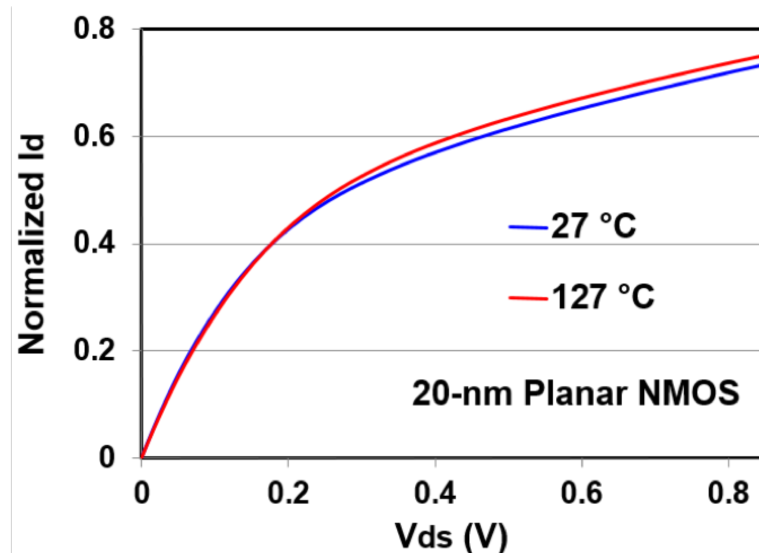



Figure 5.1: Circuit-level simulation results for transistor currents at different temperatures for the 20-nm node with nominal supply voltage of 850 mV.

ulation results for the 14/16-nm technology node with varying temperatures are shown in

Figure 5.2. A small decrease in current is observed with an increase in temperature. TEI and different $V_T$ values are responsible for the transistor current differences in response to increased temperature.

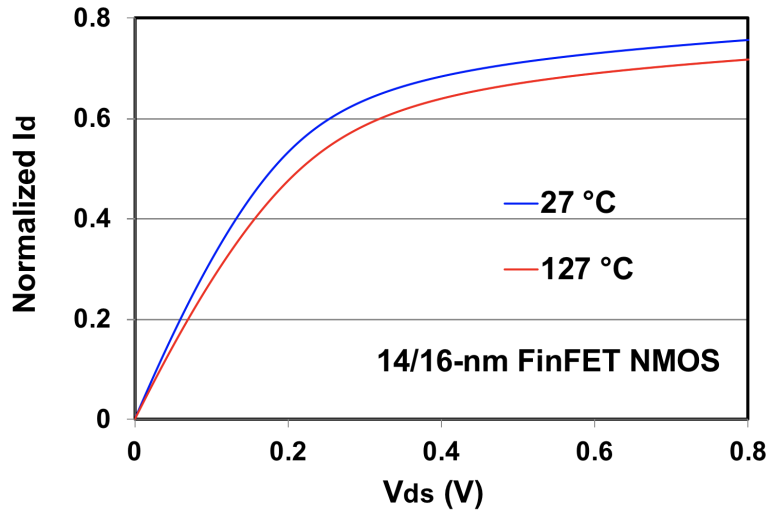



Figure 5.2: Circuit-level simulation results for transistor currents at different temperature for the 14/16-nm node with supply voltage of 800 mV.

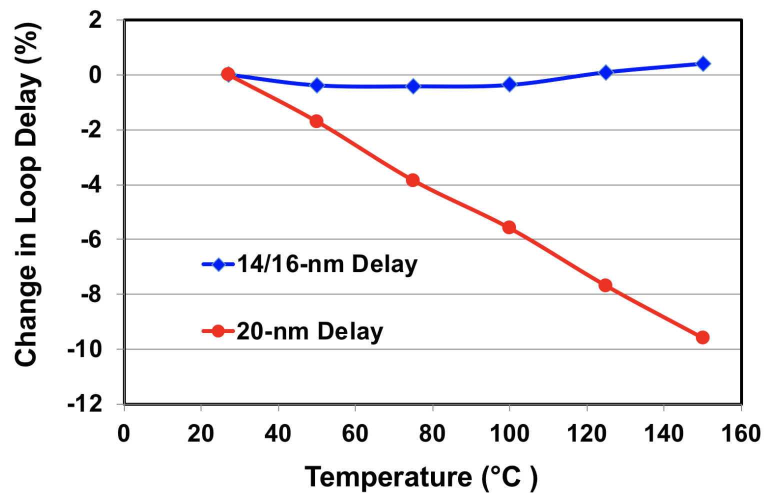



Figure 5.3: Circuit-level simulation results showing variations in feedback loop delay for a conventional DFF design for 20-nm planar ($V_{DD}$ = 850 mV) and 14/16-nm FinFET ($V_{DD}$ = 800 mV) technology nodes.

Figure 5.3 shows circuit-level simulation results for the changes in the feedback loop delay as a function of temperature for a conventional DFF design in the 20-nm planar

and the 14/16-nm FinFET technologies. For the 20-nm planar node, the FF loop delay decreases by 9.6% when temperature increases from 25 °C to 150 °C. However, for the 14/16-nm FinFET node, feedback loop delay only changes by about 0.4% for the same DFF design.

Figure 5.4 shows the circuit-level simulation results of SET pulse widths for a particle hit (strikes with a low-LET particle with the LET value close to that of alpha particles, about 1 $MeV \cdot cm^2/mg$) on an inverter for the 20-nm technology. The bias dependent model was used to model the single-event strike [67]. The increases in transistor current when

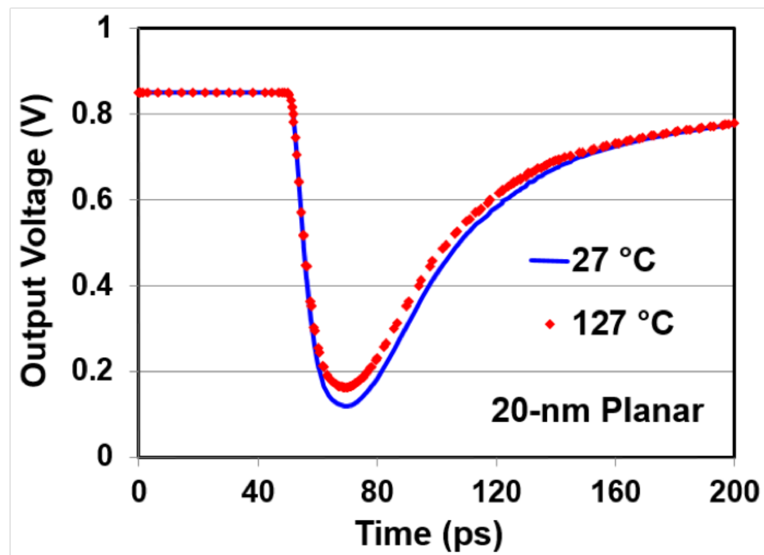



Figure 5.4: Circuit-level simulation results for SET pulse widths at different temperatures for a low-LET particle striking an inverter design on a 20-nm node with a supply voltage of 850 mV.

temperature is raised from 27 °C to 127 °C will result in a small decrease in the full-width-half-max pulse width of the transient. Besides, the increasing carrier recombination rates [91] will also reduce the SET pulse width (the collected charge will decrease). The two factors together lead to a decrease in the SET pulse width. 3D TCAD simulation results of SET pulse width for a low-LET particle striking an inverter for the 14/16-nm bulk FinFET technology node are shown in Figure 5.5. Reduced transistor currents for the 14/16-nm node will increase the SET pulse width while increased recombination rates will

reduce it. The changes in restoring current drives are compensated by the changes in carrier recombination rates, resulting in insignificant changes in overall SET pulse width.

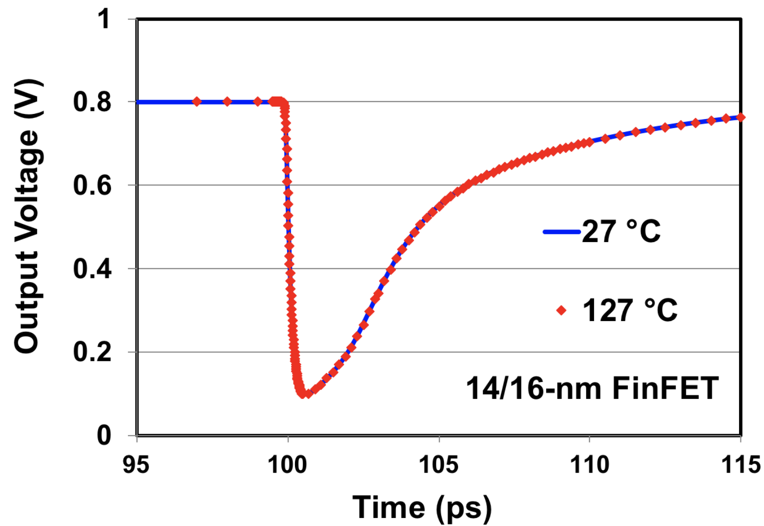



Figure 5.5: 3D-TCAD simulation results for SET pulse widths at different temperatures for a low-LET particle striking an inverter design on a 14/16-nm node with a supply voltage of 800 mV.

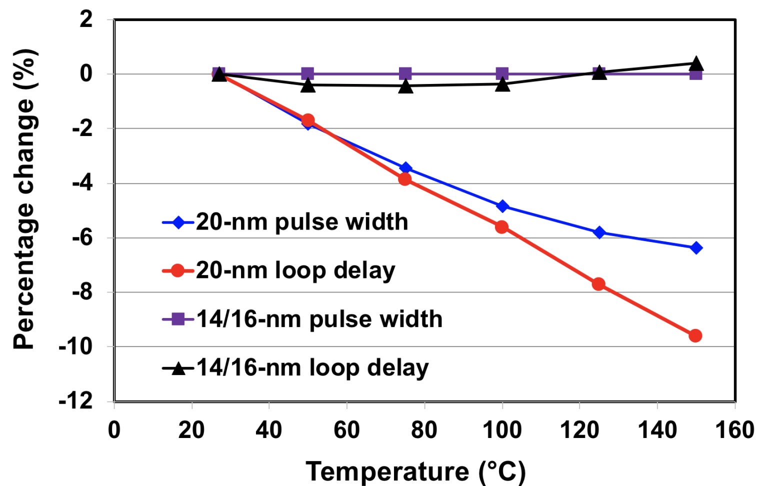



Figure 5.6: Circuit-level simulations showing variation comparison of feedback loop delay and SET pulse width for the 20-nm and the 14/16-nm nodes at nominal supply voltages.

Figure 5.6 shows the percentage change for the feedback loop delay and the SET pulse width for the 20-nm and the 14/16-nm node. For the 14/16-nm node, both SET pulse width and feedback loop delay show negligible changes with temperature over the range of inter-

est. This indicates that 14/16-nm FinFET DFFs will show very little dependence of SER on temperature within this range for low-LET particle irradiations. For the 20-nm node, the SET pulse width and the feedback loop delay decrease with increasing temperature. Larger decreases in feedback loop delay compared to that for SET pulse width indicate an overall increase in SER for the 20-nm planar DFFs under low-LET particle irradiations.

### 5.1.3 Experimental Details

Test chips were fabricated in both 20-nm bulk planar technology and 14/16-nm bulk FinFET technology at a commercial foundry. Chip design and test setups have been described in Chapter 3. Irradiation was carried out at Vanderbilt University using the $1\ cm \times 1\ cm$ size $5.4\ MeV$ $10\ \mu Ci$ $^{241}Am$ foil button source (as shown in Chapter 3). The die was heated from the backside using a temperature adjustable heat gun. A hand-held laser thermometer was used to monitor the die temperature.

Tests were carried out for temperatures ranging from room temperature to 135 °C. The temperature was carefully controlled with variations less than 5 °C. Characteristics of the foil alpha source do not vary significantly within this temperature range [92]. The shift registers were continuously clocked at a frequency of 2.5 MHz with input equal to logic "0". For the 20-nm conventional LVT DFF (nominal $V_{DD}$ is 850 mV), supply voltage was varied from 750 mV to 950 mV. For the 14/16-nm node, the nominal $V_{DD}$ is 800 mV. For the conventional LVT DFF at the 14/16-nm node, $V_{DD}$ was varied from 500 mV to 800 mV. Tests for FF designs with different $V_T$ options and well structures were also carried out to evaluate the stability of $V_T$ and well-structural effects on SEU responses against temperature. Tests were carried out at 570 mV, with temperature increasing from 25 °C to 115 °C.

### 5.1.4 Experimental Results

Figure 5.7 shows the normalized test results for the conventional DFF designed in the 20-nm planar technology node. Error bars represent standard deviation (each data point contains thousands of errors so the error bars are very small and can hardly be seen in this figure). The decrease in supply voltage decreases the transistor current and the critical

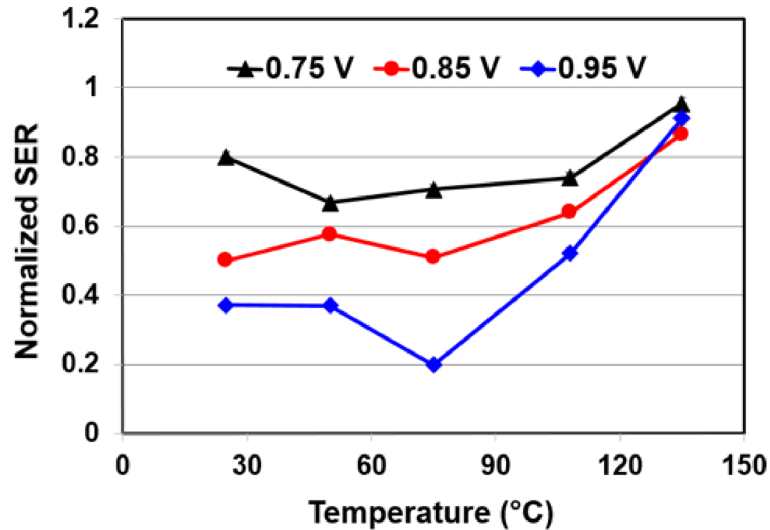



Figure 5.7: Normalized SER as a function of temperature with different supply voltages for the 20-nm conventional DFF.

charge for the DFF cell, resulting in an increase in SER. For this design, the increase in SER was minimal (or a small decrease) up to 80 °C for all supply voltages. As temperature continues increasing, SER start to increase. An increase in temperature decreases both carrier mobility and $V_T$. A decrease in carrier mobility decreases the transistor current while a decrease in $V_T$ increases transistor current, which modifies the SET pulse width and feedback loop delay. Changes in transistor current due to both of these parameters may cause a cross-over point at which changes in transistor current may reverse. For SER curve of $V_{DD}$ = 950 mV in Figure 5.7, the SER values show a decreasing trend at lower temperatures (less than $\sim$ 75°C), but at higher temperatures (beyond $\sim$ 75°C), SER values show an increasing trend. These results are caused by difference in the rate at which SET pulse width and feedback loop delay are affected. For operations at $V_{DD}$ = 750 mV and

$V_{DD}$ = 850 mV, the cross-over point can move and the difference in SET pulse width and feedback loop delay can change, which may finally lead to SER increasing or decreasing at lower temperatures. For the highest temperature tested (135 °C), the SER increased to ∼1.7x for nominal supply voltage operation. The SER increases to ∼1.2x for 750 mV and ∼2.5x for 950 mV supply voltages.

For the 14/16-nm FinFET LVT DFF, the SER change is very small (less than 20% and within the error bars, as shown in Figure 5.8) across the temperature range tested for voltage ranging from 500 mV to 800 mV. For the 14/16-nm node, the changes in feedback loop delay and SET pulse width over the temperature range tested is insignificant, resulting in almost constant SER across the temperature range.

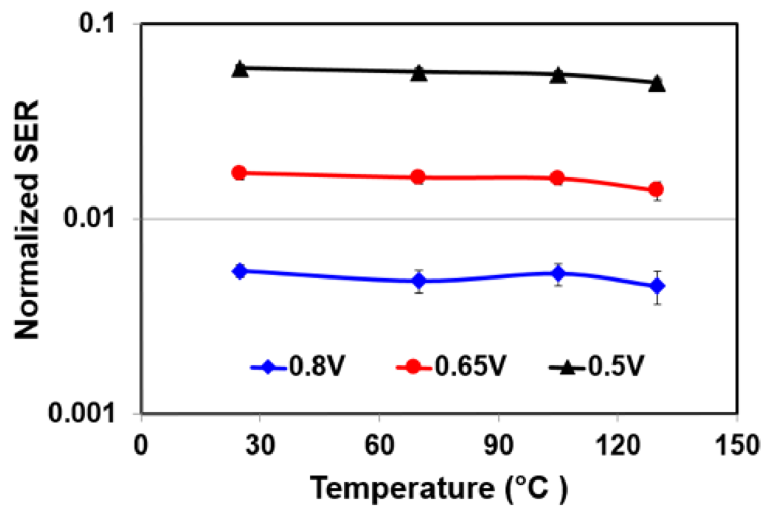



Figure 5.8: Normalized SER as a function of temperature with different supply voltages for the 14/16-nm conventional LVT DFF.

Figure 5.9 shows the normalized values of SER as a function of temperature for nominal $V_{DD}$ for the 20-nm planar and 14/16-nm FinFET nodes together. Normalization is with respect to the SER value at room temperature for each technology. According to Figure 5.9, SER of the planar node has a strong dependence on temperature. But for the FinFET node, the SER change is negligible, within the error bars.

For the 14/16-nm nodes, additional temperature tests were carried out for FF designs

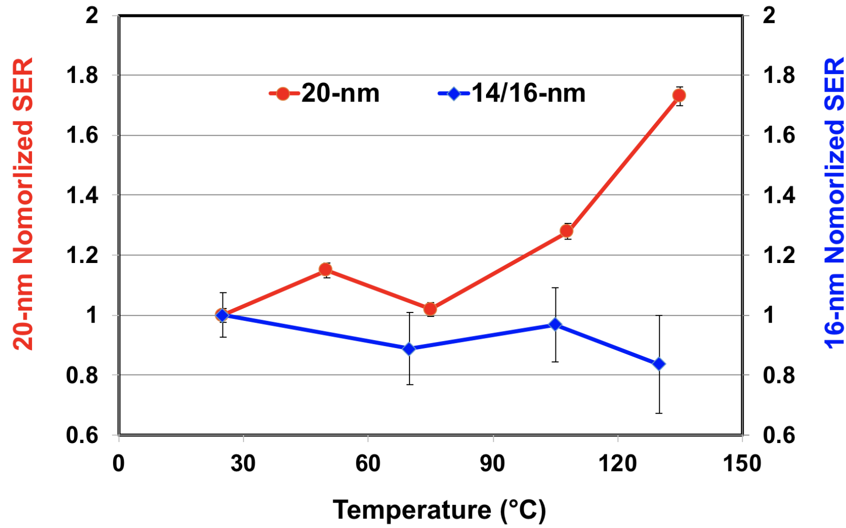



Figure 5.9: Normalized SER as a function of temperature showing changes for 20-nm planar and 14/16-nm FinFET LVT DFF designs at norminal supply voltages.

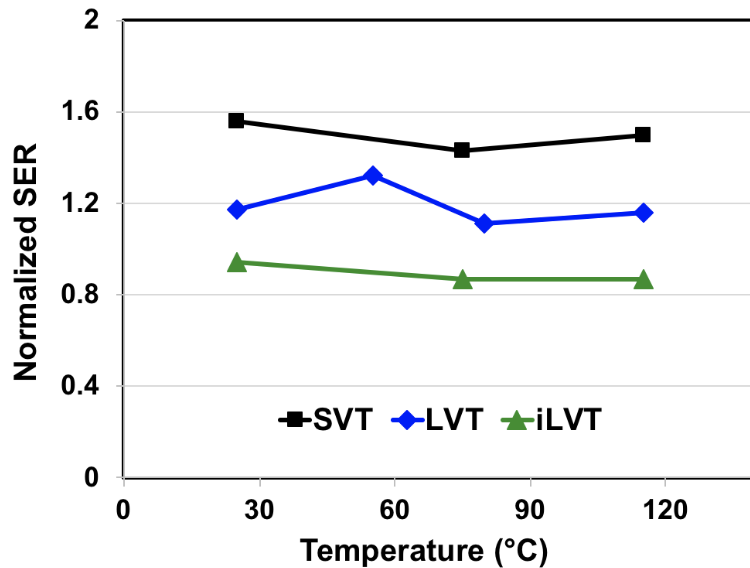



Figure 5.10: Normalized alpha-induced SER as a function of temperature of conventional DFF with different $V_T$ options at $V_{DD}$ = 570 mV.

with different $V_T$ options and well structures. Figure 5.10 shows normalized SER results as a function of temperature for conventional DFF with different $V_T$ options. Results show similar temperature dependence of SEU responses for DFF with different $V_T$ options for the 14/16-nm node, with DFF with SVT option showing highest SER among three designs.

Temperature effects on SER is insignificant for all $V_T$ options, which indicates the stability of $V_T$ effects against temperature.

Figure 5.11 shows the alpha particle-induced SEU cross-sections of dual-well and triple-well guard-gate FF designs as a function of temperature. Similarly, temperature effects on SEU responses are minimal for both dual- and triple-well designs. The triple-well guard-gate design continuously shows superior SEU performance across the temperature range than the dual-well one. The advantage of SEU performance for the triple-well process remains against temperature range from 25 °C to 115 °C.

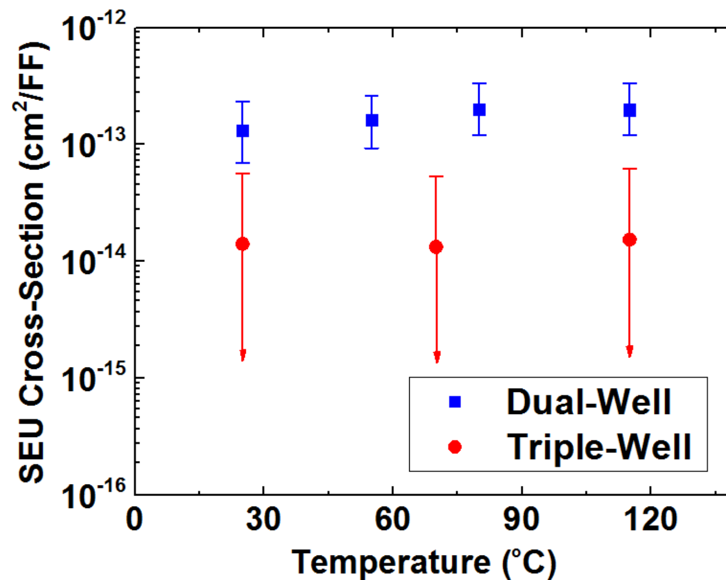



Figure 5.11: Alpha particle-induced SEU cross-sections of dual-well and triple-well guard-gate FF designs as a function of temperature at $V_{DD}$ = 570 mV.

## 5.2 Angular Effects

In a radiation environment, the incident particles come from all angles. Effects of such angular incidences on charge collection, single-event latchup (SEL), single-bit upsets (SBU) and multiple-bit upsets (MBU) in dynamic random access memory (DRAM), static random access memory (SRAM), latch, and FF designs with different radiation sources have been studied for planar technologies [93, 94, 95, 96, 97, 98, 99, 100, 101]. These

results indicate that angle of incidence is an important factor to be included in device and circuit-level SE reliability assessment. For FinFET technologies, the physical transistor structure has been changed significantly from planar technologies and charge collection is reduced significantly. Angular effects on SEU vulnerability for FinFET technologies can be very different from that for planar technologies, necessitating the investigation of angular effects on SEU responses for new FinFET technologies.

### 5.2.1 Background

The overall effect of angular incidence is a strong function of the physical dimensions of the diffusion/active regions on an IC. Since such physical dimensions in all three directions change significantly for each new technology node, it is very important to evaluate each new technology against angular incidence of particles for developing predictive models for SE mechanisms and failures.

For planar technologies, it has been shown that the angle of incidence strongly influences the amount of charge collected at a circuit node. The collected charge may come from an ion hit to the semiconductor region associated with the node itself or due to charge sharing from the ion hit on an adjacent semiconductor region. The angle of incidence affects the charge track characteristics (charge track length in active Silicon regions particularly) due to the fact that the drain region is a rectangular slab and the charge track length within active Silicon region created by the incident particle is dependent on the angle of incidence. Additionally, the angular incidences are more likely to result in multiple nodes collecting charge compared to normal incidence [102, 103, 104, 105, 106]. Most design techniques for SEU mitigation are not effective when collected charge increases or multiple nodes collect charge resulting from angular incidence [98, 100]. Results from previous work on planar technologies show significant change in SEU error rates due to incident angle for 90-nm Dual Interlocked Cell (DICE latch) [98] and 40-nm SRAMs [101].

For FinFET technologies, the charge collected at a circuit node for angular incidences

will be affected by the thin fin region (narrow active Silicon region) and the narrow connection to the substrate. The length of the charge track within active Silicon region will change depending on the ion-hit position and the angle of incidence for FinFET technologies. The significant differences in transistor physical structure further necessitate the need for angular testing for FinFET technologies.

### 5.2.2 Angular Effects Analysis from Geometry View

#### 5.2.2.1 Angular Effects on a planar transistor

For bulk planar technologies, drain, source and channel regions of an individual transistor reside within the bulk region, whereas a bulk FinFET transistor has only a narrow connection from these regions to the bulk region. Figure 5.12 shows the structure for a planar transistor when ionizing particles are incident on the IC at normal incidence and at angles. The direction of the incident particle when it is incident parallel to power rails,

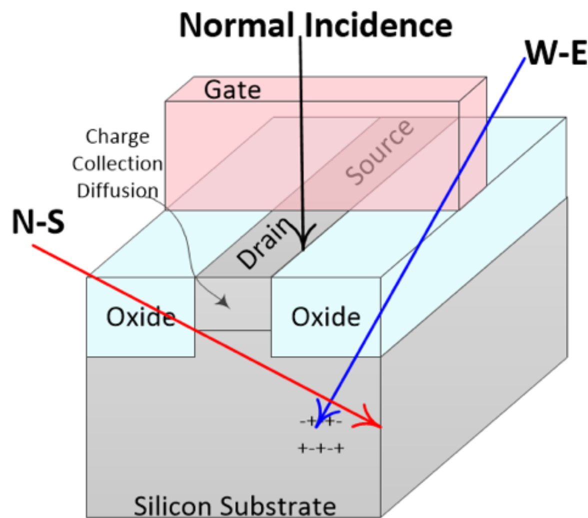
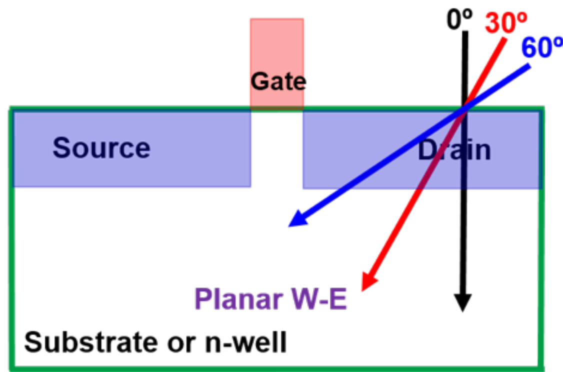
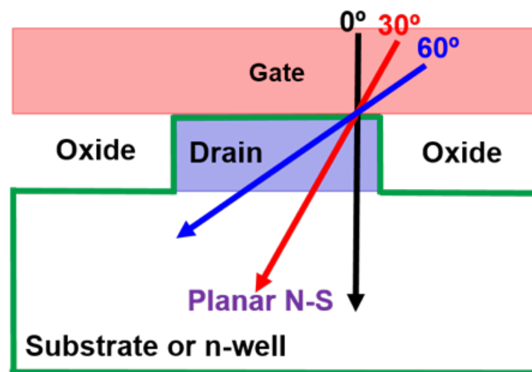



Figure 5.12: Incident ions from N-S, W-E directions and normal incidence on a transistor in a planar technology, after [107].

is termed as West-to-East (W-E) in this work and the angle of incidence is termed as tilt tangle. Similarly, North-to-South (N-S) refers to the direction that is incident perpendicular to power rails and the angle of incidence is termed as roll angle. Figure 5.13 shows




(a) N-S view and W-E incidence




(b) W-E view and N-S incidence

Figure 5.13: Cartoon cross-section views of a planar transistor from different aspects with particles incident from different directions.

the cross-section views of a planar transistor with W-E and N-S directions clearly marked for incident ions. For the hit transistor, the ion tracks go through the drain region and may extend into the substrate. In both W-E and N-S directions, different incident angles can change the charge track length within a drain region and subsequently affect the charge collection, as shown in Figure 5.13. Assuming a rectangular parallelepiped (RPP) sensitive volume [108, 109], the amount of charge collected for an angular ion incidence for a planar transistor is more than that for a normal incidence because of the inverse cosine law yielding longer charge track length within the specific region. Incorporating charge collection by diffusion and the small geometry of this structure (particles may exit through the side of the junction), correction models have been developed for charge deposition and

charge collection [110, 111]. Others have shown the deviation of charge collection from the inverse cosine law but charge collection still increases with increasing angles [112].

Collected charge for an incident ion from W-E or N-S direction does not make a significant difference for the hit region for planar technologies as both directions show similar charge track variations with increasing angle. However, W-E or N-S incidence can affect charge-sharing characteristics depending on the physical arrangement (layout) for transistors. For angular cases, the angle of incidence can decrease the distance between the charge track and the drain region of some adjacent transistors. So charge collected by transistors nearby will vary significantly depending on the angle of incidence and the physical placement of transistors.

#### 5.2.2.2 Angular Effects on a FinFET transistor

Figure 5.14 shows the 3D structure of a FinFET transistor and angular incidences for W-E and N-S directions. Figure 5.15 shows the cross-section views of a FinFET transistor

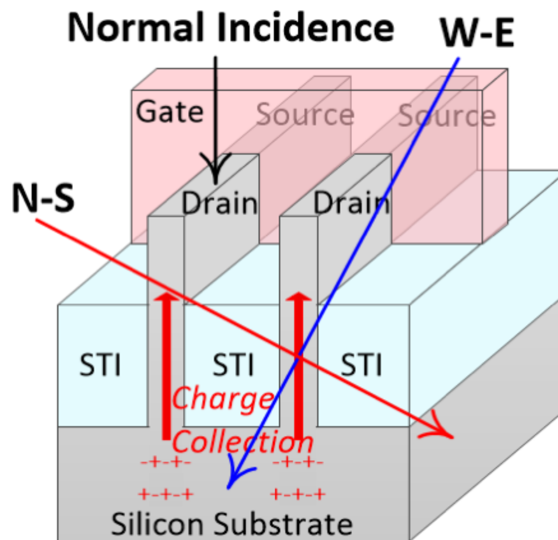
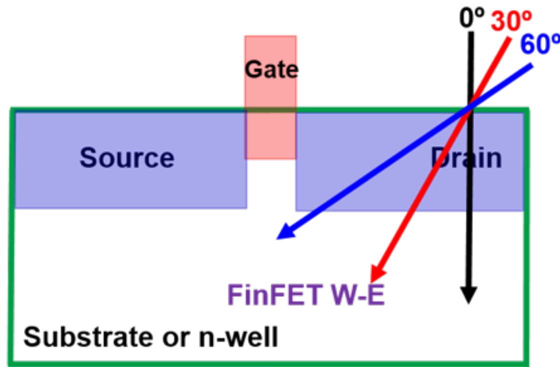
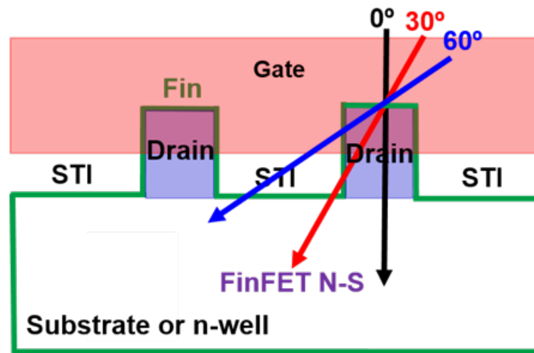



Figure 5.14: Incident ions from N-S, W-E directions and normal incidence on a transistor in a FinFET technology, after [107].

with 2-fins from N-S and W-E directions with particles incident from W-E and N-S directions, respectively. For the following discussion, it is assumed that the charge track length




(a) N-S view and W-E incidence




(b) W-E view and N-S incidence

Figure 5.15: Cartoon cross-section views of a FinFET transistor from different aspects with particles incident from different directions.

is longer than the fin height (which should be true for most heavy-ion strikes). For tilt angle (W-E direction) incidence, the charge track (shown in Figure 5.15(a)) is very similar to that in a planar transistor. As a result, the collected charge will increase as the angle of incidence is increased - similar to planar technologies.

For roll angle incidence, since the fin width is much smaller than the fin height, incident particles will traverse through the fin and may exit to surrounding insulators depending on the angle of incidence, as shown in Figure 5.15(b). In this case, as the roll angle increases, the charge track length within the active Silicon region actually decreases and will equal to fin width when $\theta = 90^{\circ}$. As a result, the charge collection will actually decrease as roll angle increases. If the LET value of the particle is close to LET threshold of the storage cell, such a change in collected charge will significantly change the SEU cross-section.

This is very different from what has been observed in planar technologies. For planar technologies, the absence of fin makes differences in charge track length between tilt and roll angles negligible. As a result, the different behaviors for tilt angles and roll angles of SEU cross-section in [98] were mainly caused by charge sharing for planar technologies.

The charge-sharing effect of a FinFET technology is also different from planar technologies. For a transistor that is adjacent to the hit transistor, charge sharing will certainly occur in a FinFET technology if the particle comes at a sharp enough angle to traverse through multiple fins or pass underneath another transistor. When a particle traverses through multiple fins, the charge collected at each transistor will follow the behavior discussed above (shorter charge track length for larger roll angles). When a particle traverses through one fin and passes underneath another transistor, charge collected by the second transistor may be reduced compared to that for planar node due to the narrow connection between the drain region and the bulk. As a result, charge sharing will be reduced for FinFET technologies compared to planar technologies for angular incidences. This reduced charge-sharing effect at the FinFET node has been seen in SRAM cells where MCU size was used to show the extent of charge sharing between adjacent cells [56].

### 5.2.3 Simulations and Discussion

A 3D TCAD model of a 14/16-nm bulk FinFET D-latch based on dual-well technology was simulated in the Synopsys suite of TCAD tools. The electrical characteristics of the FinFET devices were calibrated against the ASU PTM [66]. The D-latch is a standard latch that contains two back-to-back inverters with a transmission-gate in-between, as shown in Figure 5.16. The critical charge of the DFF design constructed with this D-latch was simulated to be $\sim 1.75\ fC$ at nominal supply voltage ($V_{DD}$= 800 mV) and room temperature using a commercial 14/16-nm PDK. All the transistors in the D-latch were modeled in TCAD. The heavy-ion track was modeled as a gaussian track with characteristic radius of 10 *nm* and deposition time of 50 $fs$. More details of the model and parameters used

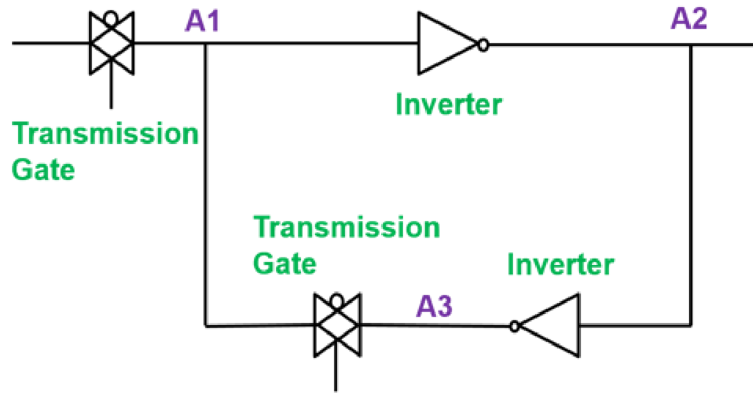
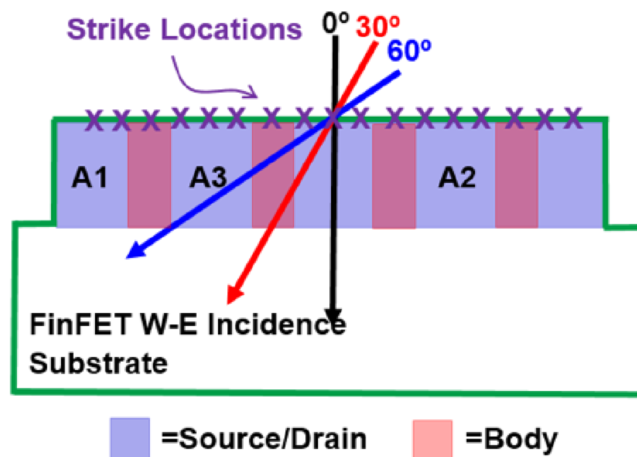
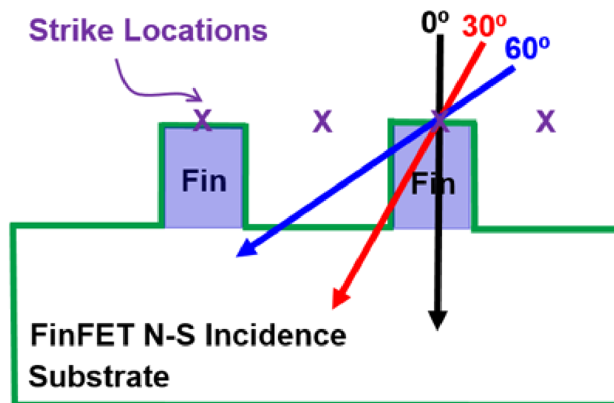



Figure 5.16: Schematic design of the 14/16-nm bulk FinFET D-latch.




(a) N-S view and W-E incidence, along the length of active silicon for a single fin




(b) W-E view and N-S incidence, across different fins

Figure 5.17: Cartoon cross-section views of strike locations in TCAD simulation. Strike location varies every 20-nm. Nodes are identified to match the nodes in the schematic.

for TCAD simulations can be found in [78]. The modeled heavy-ion particle LET is 1.2 $MeV \cdot cm^2/mg$. All ion hit locations were on NMOS transistors.

In the W-E case, 17 total strike locations were simulated across the latch. An ion strike was carried out at every 20 *nm* distance along the row of NMOS transistors for three different angles, as shown in Figure 5.17(a). The number of upsets simulation results are shown in Table 5.1. With increasing angle of W-E incidence, the upset probability shows slight increases (12.5% and 37.5%) for low-LET particle strikes. The increase in upset probability is due to the longer charge track length within the active Silicon region and the resultant increased charge collection with increasing tilt angle.

In the N-S case, 4 total strike locations were simulated and the strike locations are shown in Figure 5.17(b). The strike locations are 20 *nm* apart. The simulation results are shown in Table 5.2. With increasing angle of N-S incidence, the upset probability decreases for low-LET particle strikes. The decrease in upset probability is due to shorter charge track length within active Silicon region and subsequently decreased charge collection with increasing roll angle.

Table 5.1: Upset at Different Strike Locations for W-E Incidence

| Directions | Angle of Incidence | # of Strike Locations | # of Upsets |
|---|---|---|---|
| W-E | 0° | 17 | 8 |
| W-E | 30° | 17 | 9 |
| W-E | 60° | 17 | 11 |

Table 5.2: Upset at Different Strike Locations for N-S Incidence

| Directions | Angle of Incidence | # of Strike Locations | # of Upsets |
|---|---|---|---|
| N-S | 0° | 4 | 3 |
| N-S | 30° | 4 | 2 |
| N-S | 60° | 4 | 1 |

### 5.2.4 Experimental Details

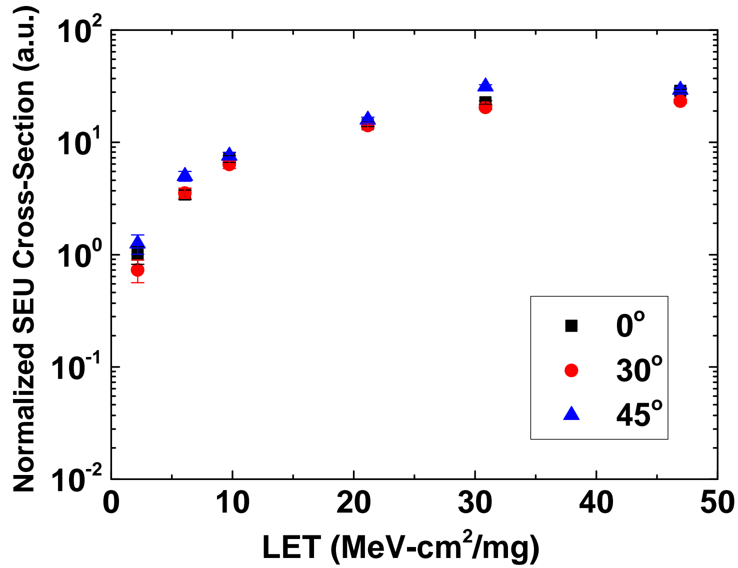
Test chips were fabricated in a commercial 14/16-nm bulk FinFET technology. The nominal gate length of is 16 nm, with 2 fins per transistor. A conventional DFF design with a cell area of $\sim 1.27\ \mu m^2$ was implemented in CREST configuration [57] with 8K stages, as described in Chapter 3. Irradiations were carried out at LBNL with 10 $MeV/nucleon$ in vacuum with particles of LET values ranging from $1 \sim 50\ MeV \cdot cm^2/mg$, as listed in Table 5.3. The test IC was operated at nominal supply voltage ($V_{DD}$ = 800 mV) and at room temperature with input to the shift registers held at 0 V. During testing, the shift registers were continuously clocked at a frequency of 2.5 MHz. Incident direction included normal incidence, W-E (tilt angle) and N-S (roll angle) incidences at angles of 30° and 45° . The total fluence of all tests were run up to $5 \times 10^7\ /cm^2$ to obtain reasonable SEU statistics. Angular tests have been done for conventional DFF designs with different $V_T$ options, dual- and triple-well guard-gate FF designs.

Table 5.3: 10 MeV/nucleon Cocktail Components

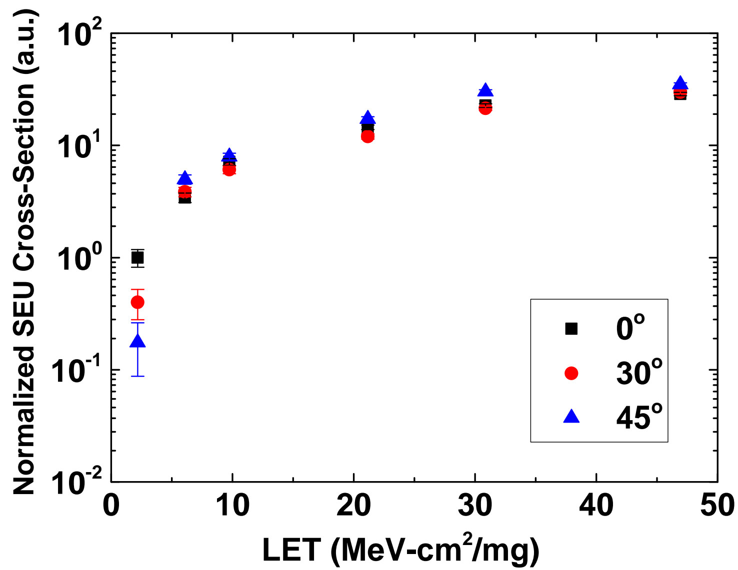
| Ion | Energy ($MeV$) | LET ($MeV \cdot cm^2/mg$) | Range ($\mu m$) |
|---|---|---|---|
| $^{18}O^{+5}$ | 183.47 | 2.19 | 226.4 |
| $^{29}Si^{+8}$ | 291.77 | 6.09 | 141.7 |
| $^{40}Ar^{+11}$ | 400.00 | 9.74 | 130.1 |
| $^{65}Cu^{+18}$ | 659.19 | 21.17 | 108.0 |
| $^{84}Kr^{+24}$ | 885.59 | 30.86 | 109.9 |
| $^{124}Ag^{+34}$ | 1039.42 | 46.92 | 90.0 |

### 5.2.5 Experimental Results

Figure 5.18 shows the normalized SEU cross-section results for all three angles as a function particle LET values for the LVT DFF. Data is normalized to the SEU cross-section induced by the lowest-LET particle used in tests ( $^{18}O^{+5}$, LET=2.19 $MeV \cdot cm^2/mg$) at normal incidence. Error bars represent standard errors. For low-LET particle irradiations,




(a) W-E direction of incidence (tilt angle)




(b) N-S direction of incidence (roll angle)

Figure 5.18: Normalized SEU cross-sections as a function of LET with different angular incidence for conventional DFF.

different trends of SEU cross-section at tilt and roll angles are found. For tilt angle (W-E direction) of incidences, the SEU cross-section shows a slight increase with increasing angle, as shown in Figure 5.18(a). According to simulation results, increasing tilt angle leads to small increases in upset probability, which is consistent with experimental results. For roll

angle (N-S direction) of incidences, the SEU cross-section decreases with increasing angle of incidence. This is due to the reduced charge track length within active Silicon region, and subsequently collected charge and upset probability. For high-LET particle strikes at W-E and N-S incidences, the trends of SEU cross-sections are very similar. Although the charge track lengths in the active Silicon region are different for different incident angles, the charge collected is large enough to cause an upset in DFF designs for most incidences. For N-S incidence, the incident ion passes under the adjacent transistor (or adjacent fin), resulting in collected charge at multiple nodes. As the LET value of incident particle increases, the increases in SEU cross-section due to charge sharing are more significant than the decreases due to shorter track length with increasing roll angles. As a result, the SEU cross-section for N-S direction also increases slightly as angle of incidence is increased for high-LET particle irradiations. The increases in SEU cross-section are smaller than those observed for planar technologies because of reduced charge-sharing effects in FinFET technologies [56].

Figure 5.19 shows the normalized SEU cross-section as a function W-E and N-S incident angle for $^{18}O^{+5}$ with LET value of 2.19 $MeV \cdot cm^2/mg$. For W-E incidence, the SEU

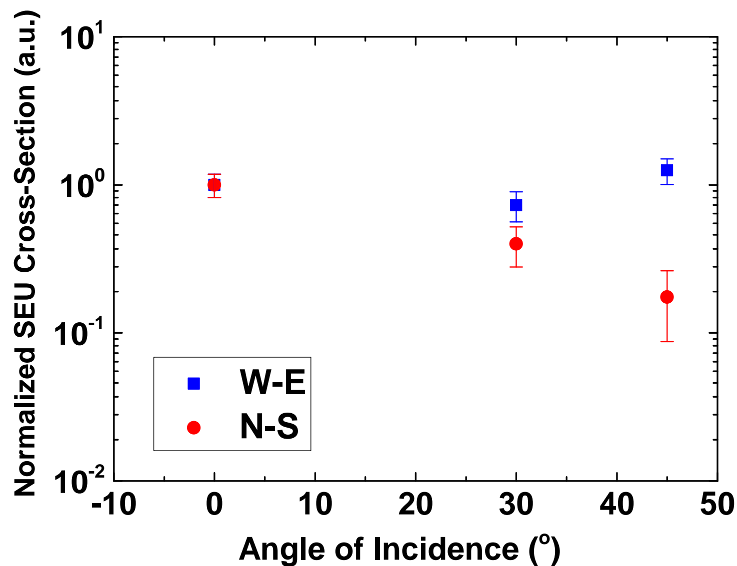
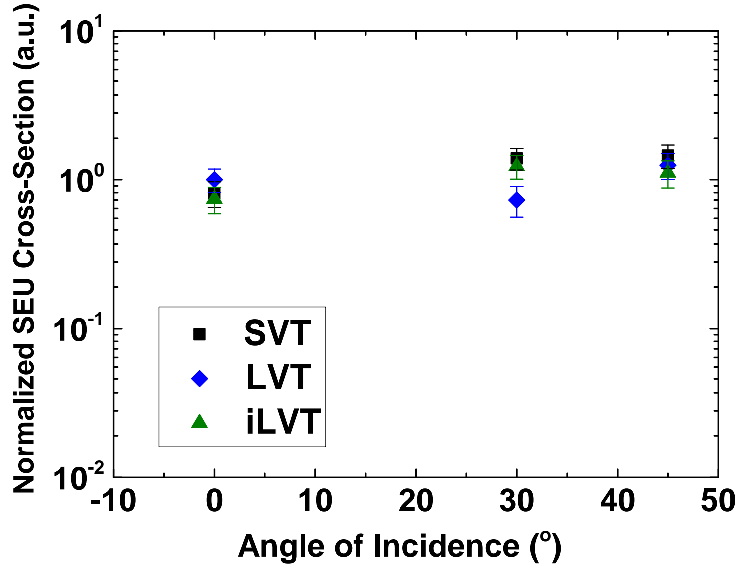



Figure 5.19: Normalized SEU cross-sections as a function incident angle when $^{18}O^{+5}$ hit on DFF (LET = 2.19 $MeV \cdot cm^2/mg$).

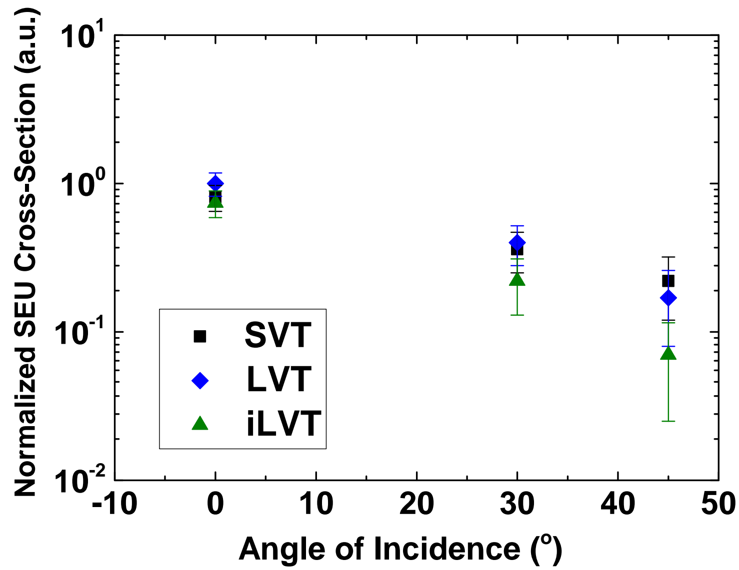
cross-section does not increase significantly. For N-S direction, the SEU cross-section decreases with increasing angle. The SEU cross-section for W-E direction is higher for a given angle than that for N-S direction because of the larger volume of active Silicon available in W-E direction strikes (the width of drain region) compared to that for N-S direction strikes (width of the fin region). So the LET threshold for N-S direction is higher than that of W-E direction incidence because of less charge collection for N-S incidences compared to W-E incidences.

Additional angular tests were carried out for FF designs with different $V_T$ options and well structures. Since the differences in SEU vulnerability diminishes as particle LET value increases, only low-LET particle irradiation test results were plotted. Figure 5.20 shows the normalized SEU cross-section for DFF with different $V_T$ options as a function of incident angle for $^{18}O^{+5}$ with LET value of 2.19 $MeV \cdot cm^2/mg$. The SEU cross-section of three $V_T$ options are very close because the particle LET may be higher the the LET threshold. For W-E incidence, as shown in 5.20(a), the SEU cross-section changes insignificantly as incident tilt angle increases from 0° to 45° for all three $V_T$ designs. Figure 5.20(b) shows the results of N-S strikes, all three $V_T$ options show SEU cross-section decreases as roll angle increases. The decreasing rates are similar, within error bars. Angular effects mainly depend on the FinFET transistor structure. $V_T$ option is not affecting the angular dependence of SEU cross-sections for DFF designs.

Figure 5.21 shows the normalized SEU cross-section for the guard-gate FF with dual- and triple-well structure as a function of incident angle for $^{29}Si^{+8}$ with LET value of 6.09 $MeV \cdot cm^2/mg$, since for guard-gate design short SET pulses are eliminated and few upsets were observed for lower-LET particles during testing. At this LET value, SEU responses are very similar at normal incidence (difference only shows at reduced supply voltages for low-LET particles). As tilt angle increases, the SEU cross-section increases slightly for both dual-well and triple-well designs and the increasing rate is similar, within error bars. For N-S incidence, the triple-well design shows a slight decrease as expected




(a) W-E direction of incidence (tilt angle)




(b) N-S direction of incidence (roll angle)

Figure 5.20: Normalized SEU cross-sections as a function incident angle when $^{18}O^{+5}$ hit on DFF with different $V_T$ options (LET = 2.19 $MeV \cdot cm^2/mg$).

while the dual-well design didn't show any difference in SEU response. The possible reason for the difference is that the dual-well design has lower LET threshold and higher SEU vulnerability and angular effect on the dual-well design has diminished for irradiation particle with LET = 6.09 $MeV \cdot cm^2/mg$. For the triple-well design, the LET threshold is

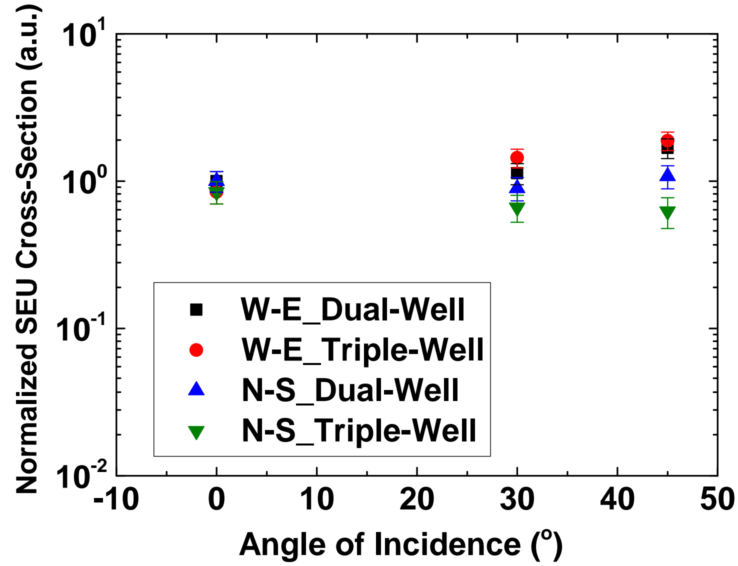



Figure 5.21: Normalized SEU cross-sections as a function incident angle when $^{29}Si^{+8}$ hit on dual- and triple-well guard-gate FF (LET = 6.09 $MeV \cdot cm^2/mg$).

around 6.09 $MeV \cdot cm^2/mg$ and slight difference can be seen. From above results, the triple-well design remains good SEU performance (either remains or better) as it is at normal incidence.

## 5.3 Summary

Some environment conditions are not under convenient control in real applications and have to be taken into consideration when choosing proper process parameters for high performance circuits. In this chapter, effects of operating temperature and particle incident angle on SEU responses have been investigated with simulations and experimental validations (alpha-particle or heavy-ion irradiations) for FF designs in the 14/16-nm bulk FinFET technology. Results indicate: 1) temperature effects on SEU responses are insignificant because both SET pulse width and feedback loop delay change insignificantly across the temperature range as temperature increases for alpha-particle irradiations; 2) different $V_T$ options and well structures do not affect the temperature dependence of SEU responses; 3) SEU vulnerability increases with incident tilt angle but decreases with roll angle due to

changes in charge track length in active Silicon region and the overall charge collection for low-LET particle irradiations; 4) angular effects remain similar for FF designs with different $V_T$ options and well structures. With these characterizations and analysis, designers can choose the proper designer-controlled parameters with increased confidence in FinFET technologies.

# Chapter 6

# Conclusion

Effects of designer-controlled parameters on SEU responses for FF designs in FinFET technologies have been investigated for the first time. SEU characterizations have been carried out in a 14/16-nm bulk FinFET technology node to evaluate $V_T$ and well-structure effects on FF SEU performance across wide ranges of supply voltage, frequency, temperature and particle incident angle. Experimental results from characterization on a 20-nm planar node or from previous published work have been used for comparison. Through 3D TCAD or circuit-level simulations, the underlying mechanisms for effects of these parameters on SEU responses for different technologies have been revealed. With simulation and experimental results, design recommendations have also been provided for specific applications.

This work has several major findings.

1. For high-LET particle irradiations, $V_T$ dependence of SEU responses is not significant for both 20-nm bulk planar and 16-nm bulk FinFET technologies. For low-LET particle irradiations, effects of $V_T$ options on SEU responses significantly depend on technology. For the 20-nm bulk planar DFF, the highest $V_T$ option yields to the lowest SEU cross-section, which means increasing $V_T$ is an efficient way to decrease both power and SE sensitivity. For the 14/16-nm bulk FinFET DFF, increased $V_T$ results in increased SEU vulnerability. Tradeoffs have to be made to achieve either lower power or better speed and SEU performance. Circuit-level simulations clearly show that different $V_T$ effects for different technologies under low-LET particle irradiations are due to different changing rates in SET pulse width and feedback loop delay as $V_T$ changes in the DFF design, which is mainly caused by the difference in the physical structure, doping level, transistor size, and transistor spacing. Besides,

higher $V_T$ options lead to higher increasing slopes as frequency increases for DFF and logic circuits due to increased SET pulse width compared to lower $V_T$ options.

2. Effects of well structure on SEU responses for FinFET technologies is very different from that of planar technologies. For the 14/16-nm bulk FinFET technology, SEU cross-section exhibits insignificant differences at nominal supply voltage between triple-well and dual-well designs but the triple-well design shows lower SEU cross-section than the dual-well design at reduced supply voltages for low-LET particle irradiations, especially for alpha particles. Results show significant differences in charge collection and SEU response trends for FinFET nodes compared to planar nodes. For previous planar nodes, the drain area collects more charge in the triple-well design due to charge confinement with the presence of the deep-n-well and the triple-well designs show inferior SEU performance than the dual-well designs. For the 14/16-nm bulk FinFET technology, the third well in the triple-well design acts as the preferred sink for charge dissipation and the drain charge collection in the triple-well design is less than that for the dual-well design for low-LET particle strikes because the effect of additional charge sink outweighs charge confinement effect, leading to superior SEU performance of the triple-well design than the dual-well design for low-LET particle irradiations. The differences are mainly caused by the significantly differences in physical structures. With the superior (or similar) SEU characteristics of the triple-well design than the dual-well design in FinFET technologies, designers can apply the triple-well technique for specific applications to provide better isolation without scarifying SEU performance.

3. Effects of operating temperature on SEU responses of FF designs in the 20-nm bulk planar and the 14/16-nm bulk FinFET technology are also different, which has been verified with alpha-particle irradiations. For the 20-nm node, FF SEU cross-section increases with increasing temperature. Simulation results show that feedback loop

delay decreases faster than the SET pulse width as temperature increases, leading to increased SEU vulnerability for low-LET particle irradiations. However, for the 14/16-nm node, experimental results show minimal temperature dependence of FF SEU responses. Simulation results on SET pulse width and feedback loop delay show insignificant changes in these two factors with low-LET particle strikes, leading to little temperature dependence of the SEU responses. For FF designs with different $V_T$ options and well structures, temperature dependences of SEU responses are not affected, indicating the SEU performance stability of $V_T$ options and well structures against operating temperature.

4. Effects of particle incident angle on SEU responses in FinFET technologies show significantly different trends compared to previous planar technologies for N-S incidences for low-LET particle irradiations. For the 14/16-nm bulk FinFET technology, SEU vulnerability of FF designs increases slightly with tilt angle (W-E incidences), which is similar to planar technologies. For N-S incidences, SEU cross-section decreases with increasing roll angle under low-LET particle irradiations due to reduced charge track length in active Silicon region and the overall charge collection, which is very different from the planar nodes. This is mainly due to the significant differences between planar and FinFET transistors and reduced charge-sharing effect in FinFET technologies. Geometric analysis and TCAD simulations confirm the conclusion. Angular effects remain similar for FF designs with different $V_T$ options and well structures, which confirms the stability of of $V_T$ options and well structures against incident angle.

The first characterization of effects of designer-controlled parameters on SEU responses for FinFET technologies in this work provides better understanding of underlying mechanisms and SEU vulnerability in FinFET technologies, allowing designers to have a better idea of which designer-controlled parameters to choose at the beginning of designing circuits to meet performance specifications.

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