# ELECTRONIC PROPERTIES AND RELIABILITY OF THE $SiO_2$/SiC INTERFACE

By

John Rozen

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Approved:

| | |
|---|---|
| Professor Leonard C. Feldman | Physics and Astronomy, Vanderbilt University |
| Professor Richard F. Haglund Jr. | Physics and Astronomy, Vanderbilt University |
| Professor John R. Williams | Physics, Auburn University |
| Professor Bridget R. Rogers | Chemical Engineering, Vanderbilt University |
| Professor Ronald D. Schrimpf | Electrical Engineering, Vanderbilt University |

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A mes parents et à mon frère

A Renaud et à sa famille

To Tim and Emily

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## TABLE OF CONTENTS

Page

DEDICATION . . . iii

ACKNOWLEDGEMENTS . . . iv

LIST OF TABLES . . . ix

LIST OF FIGURES . . . x

INTRODUCTION . . . 1

Part One: Review

I. SiC MATERIAL AND DEVICE PROPERTIES . . . 5

- Overview . . . 5
- 1.1. Semiconductor Properties . . . 5
- 1.2. SiC Device Physics . . . 9
  - 1.2.1. Critical field and blocking voltage . . . 9
  - 1.2.2. SiC power MOSFET . . . 11
- 1.3. Technology status and challenges . . . 14
  - 1.3.1. SiC wafer quality . . . 15
  - 1.3.2. The gate oxide . . . 16
  - 1.3.3. The $SiO_2$/SiC interface . . . 18
- References . . . 31

II. MOS PHYSICS . . . 37

- Overview . . . 37
- 2.1. Drift Conduction and Breakdown . . . 38
- 2.2. Charge Transport and Trapping in the Oxide . . . 41
  - 2.2.1. Band and hopping conduction in amorphous dielectrics . . . 41
  - 2.2.2. Transport in $SiO_2$ . . . 44
  - 2.2.3. Trap charging kinetics . . . 46
  - 2.2.4. $SiO_2$ bulk trapping and interface state generation . . . 47
- 2.3. Injection Mechanisms . . . 52
  - 2.3.1. Quantum tunneling . . . 53
  - 2.3.2. Thermionic emission . . . 57
  - 2.3.3. Frenkel-Poole emission . . . 58
  - 2.3.4. Fowler-Nordheim tunneling . . . 60
  - 2.3.5. Internal photoemission . . . 63
  - 2.3.6. Radiation-induced carriers . . . 65

2.4. MOS Capacitance . . . . . . . . . . 69
2.4.1. Nature of charges . . . . . . . . . . 69
2.4.2. Interface population . . . . . . . . . . 71
2.4.3. Small signal capacitance . . . . . . . . . . 73
2.4.4. Capacitance-Voltage measurements . . . . . . . . . . 74
References . . . . . . . . . . 78

Part Two: Original Research

III. $SiO_2$ GROWTH KINETICS ON SiC: A PRESSURE DEPENDENCE STUDY . 82

Overview . . . . . . . . . . 82
3.1. Motivation . . . . . . . . . . 82
3.2. Growth Kinetics . . . . . . . . . . 85
3.3. Experiments . . . . . . . . . . 89
3.4. Results and Discussion . . . . . . . . . . 91
3.4.1. Initial oxidation . . . . . . . . . . 91
3.4.2. Extraction of growth parameters . . . . . . . . . . 93
3.4.3. Electrical properties of the interface . . . . . . . . . . 98
3.5. Summary . . . . . . . . . . 100
References . . . . . . . . . . 101

IV. SUPPRESSION OF ELECTRON-INDUCED INTERFACE STATE GENERATION IN NITRIDED $SiO_2$ ON SiC . . . . . . . . . . 103

Overview . . . . . . . . . . 103
4.1. Motivation . . . . . . . . . . 103
4.2. Experiment . . . . . . . . . . 104
4.3. Results . . . . . . . . . . 105
4.4. Discussion . . . . . . . . . . 108
4.5. Summary . . . . . . . . . . 110
References . . . . . . . . . . 110

V. INCREASE IN OXIDE HOLE TRAP DENSITY ASSOCIATED WITH NITROGEN INCORPORATION AT THE $SiO_2$/SiC INTERFACE . . . . . . . . 113

Overview . . . . . . . . . . 113
5.1. Motivation . . . . . . . . . . 113
5.2. Experimental and Theoretical Methods . . . . . . . . . . 115
5.3. Results . . . . . . . . . . 118
5.3.1. Hole Injection . . . . . . . . . . 118
5.3.2. Charge Annealing . . . . . . . . . . 120
5.4. Discussion . . . . . . . . . . 122
5.5. Summary . . . . . . . . . . 124
References . . . . . . . . . . 124

VI. DENSITY OF INTERFACE STATES, ELECTRON TRAPS, AND HOLE TRAPS, AS A FUNCTION OF NITROGEN CONTENT IN $SiO_2$ ON SiC . . . . . . . . . 127

Overview . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 127
6.1. Motivation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 127
6.2. Experiments . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 129
6.3. Results and Discussion . . . . . . . . . . . . . . . . . . . . . . . 132
6.3.1. Kinetics of the nitrogen uptake . . . . . . . . . . . . . . . . 132
6.3.2. Impact of temperature and slow re-oxidation . . . . . . . 137
6.3.3. Progressive reduction of the interface state density . . . . 137
6.3.4. Suppression of electron-induced interface state generation 145
6.3.5. Increase in hole trap density . . . . . . . . . . . . . . . . 147
6.4. Summary . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 150
References . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 151

VII. ACCELERATED BREAKDOWN OF THERMAL OXIDES GROWN ON IMPLANTED SiC . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 154

Overview . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 154
7.1. Motivation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 154
7.2. Time-Dependent Dielectric Breakdown . . . . . . . . . . . . . . . 157
7.3. Experiments . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 160
7.4. Results and Discussion . . . . . . . . . . . . . . . . . . . . . . . 163
7.5. Summary . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 167
References . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 168

CONCLUSION . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 170

Appendices

A. OXIDATION STATION . . . . . . . . . . . . . . . . . . . . . . . . . . 174

B. AUTOMATED CARRIER INJECTION . . . . . . . . . . . . . . . . . . . 188

C. TDDB SETUP . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 194

## LIST OF TABLES

Table | Page

1.1. Comparison of 4H-SiC and Si physical constants. . . . . . . . . . . . . . . . 6

2.1. Key constants for interactions between 10 keV photons and electrons in solids. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 67

3.1. Equilibrium concentration of molecular oxygen in $SiO_2$ at 1150 °C. . . . . 88

3.2. Critical thickness for SiC oxidation. . . . . . . . . . . . . . . . . . . . . . . . 93

3.3. SiC oxidation parameters: $\tau$ at 1150 °C . . . . . . . . . . . . . . . . . . . . 94

3.4. SiC oxidation parameters: parabolic rate constant $B$ at 1150 °C . . . . . . 94

3.5. SiC oxidation parameters: linear rate constant $B/A$ at 1150 °C . . . . . . 94

4.1. Some defects predicted by theory to relax upon electron capture and their ability to be passivated by nitrogen. . . . . . . . . . . . . . . . . . . . . . . . 109

7.1. Samples used for roughness and TDDB measurements. . . . . . . . . . . . 161

# LIST OF FIGURES


Figure — Page

1.1. (a) Basic SiC structural unit. (b) Closed-packed hexagonal arrays used to reconstruct the SiC polytypes. . . . . 5

1.2. Energy gaps and relative band-offsets of Si, $SiO_2$, and common SiC polytypes. . . . . 7

1.3. Hexagonal unit cell. Common orientations used to grow oxides on SiC. Relative Si and C contents are indicated. . . . . 8

1.4. Evolution of the thickness of oxides grown on three different faces of 4H-SiC at 1150 °C in dry $O_2$. . . . . 8

1.5. Schematic of a n-channel SiC power DMOSFET. The components of the specific ON resistance are shown. . . . . 11

1.6. Achievable specific ON resistance as a function of the designed blocking voltage for Si and 4H-SiC devices. The impact of the interface quality is shown. Also, values measured on SiC MOSFETs are reported. . . . . 13

1.7. Schematic of the density of traps at the oxide/semiconductor interface. The relative positions of the conduction and valence band edges are indicated. After Schöner *et al.* . . . . . 20

1.8. $D_{it}$ obtained by CV (triangles) and conductance (circles) measurements as a function of the energy within the band-gap of 6H- and 4H-SiC. . . . . 22

1.9. Different defects that can theoretically occur at the $SiC/SiO_2$ interface and their respective energy levels in the 4H-SiC band-gap. . . . . 25

1.10. Interface trap densities in the upper half of the 4H-SiC band-gap obtained after different post-oxidation anneals. . . . . 26

1.11. Improved channel mobilities after NO annealing extracted from MOSFETs fabricated on different faces of 4H-SiC. . . . . 27

2.1. Different regimes of drift conduction and electrical breakdown. . . . . 38

2.2. Schematic of atomic coordination in an amorphous solid. . . . . 41

2.3. ”Alpine” model of the influence of disorder upon the band structure of a dielectric. . . . . 42

2.4. Expected variation of carrier mobility with energy, in the case of a disordered semiconductor. . . . . 43

2.5. A model of hole trapping and detrapping in $SiO_2$ suboxide bond. After Lelis *et al.* . . . . . . 49

2.6. Energy gain associated with a proton binding at a Si-O-Si bridge or at a Si-N-Si bridge. . . . . . 50

2.7. Quantum tunneling probabilities from the conduction band of Si and 4H-SiC as a function of the depth in $SiO_2$. . . . . . 54

2.8. Band diagram of a MOS structure showing the evolution of an electron tunneling front in the oxide induced by a positive gate bias. . . . . . 55

2.9. Flatband voltage instability in $SiO_2$/SiC MOS capacitor. Charge tunnels in and out when bias is reversed. . . . . . 56

2.10. One-dimensional potential-energy diagram illustrating the Frenkel-Poole effect. . . . . . 59

2.11. Energy-band diagram, between the emitter surface and $SiO_2$, used in the Fowler-Nordheim derivation. . . . . . 60

2.12. Theoretical Fowler-Nordheim injection current densities in $SiO_2$ from different emitters. . . . . . 62

2.13. Photoemission current as a function of gate bias; theoretical and experimental 64

2.14. Schematic representation of ionization processes in silicon dioxide. . . . . 66

2.15. Fractional yields of electron-hole pairs generated in $SiO_2$ by various radiation sources. . . . . . 68

2.16. (a) Four categories of oxide charges in the MOS system. (b) Energy levels at the oxide/semiconductor interface. . . . . . 70

2.17. (a) Energy-band diagram at thermal equilibrium for an ideal MOS system. (b) Total charge in a p-type Si substrate as a function of the gate bias. . 72

2.18. Impact of fixed charge and of interface states on the CV trace. . . . . . 73

2.19. (a) MOS CV measurement setup. (b) High and low frequency capacitance signals measured as a function of gate bias. . . . . . 75

2.20. Emission time constants at 23 °C and 350 °C of traps with different capture cross-sections. . . . . . 77

3.1. $SiO_2$ thickness on the (0001) Si-face of 4H-SiC as a function of time for dry oxidation performed at 1150 ° in flowing oxygen (1 atm) with an without alumina. . . . . . 84

3.2. Oxide thickness as a function of time for dry thermal oxidation of 4H-SiC at 0.25, 0.5, 1, 2, and 4 atm at 1150 °C on the C-face, a-face, and Si-face. 90

3.3. Deviation from the Deal-Grove model at small times and thicknesses. . . 92

3.4. Linear and parabolic rate constant at 1150 °C as a function of pressure (0.25 to 2 atm) for the C-face, a-face, and Si-face, of 4H-SiC. . . . . . . . 95

3.5. Linear rate constant at 1150 °C as a function of pressure (0.25 to 4 atm) for the Si-terminated face of 4H-SiC. . . . . . . . . . . . . . . . . . . . . . . . 96

3.6. Oxide thickness on the Si-face of 4H-SiC as a function of the product of pressure and time at 1150 °C for 0.25, 1, and 4 atm. . . . . . . . . . . . . 97

3.7. Measured interface trap densities in the upper part of the band-gap for oxides on the Si-terminated face of 4H-SiC grown in different conditions: same rate, or same temperature, or in the presence of alumina. . . . . . . 99

4.1. Schematic of the electron injection conditions and of the resulting charge trapping in the bulk of $SiO_2$ and at the $SiO_2$/SiC interface. . . . . . . . . 104

4.2. Effective density of trapped charge, as a function of the injected electron density in unpassivated and nitrided $SiO_2$ on 4H-SiC. . . . . . . . . . . . 106

4.3. Photo-CV hysteresis of unpassivated and nitrided oxides on SiC, before and after electron injection. . . . . . . . . . . . . . . . . . . . . . . . . . . . 107

5.1. Effective charge density trapped upon carrier injection by three different techniques: 10 keV X-rays, 10 eV VUV photons, and Fowler-Nordheim tunneling. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 117

5.2. Evolution of the photo-CV hysteresis of a NO-annealed oxide on SiC; before/after hole injection, and after neutralization of the trapped positive charge. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 119

5.3. Positive charge annealing via thermal emission and electron injection in nitrided oxides on SiC. . . . . . . . . . . . . . . . . . . . . . . . . . . . . 121

5.4. Atomic configurations resulting from N and NO incorporation in $SiO_2$. Hole capture leads to a change in the position of the corresponding energy levels. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 123

6.1. Schematic of the electrical connections of the designed automated injection setup. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 131

6.2. SIMS profiles for the samples annealed in NO for 7.5 min, 30 min and 120 min. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 133

6.3. N area density as a function of NO annealing time calculated by integrating the SIMS N signal. . . . 134

6.4. Density of interface states and positive charge trapping in control samples and in one annealed in NO for 2 hours. . . . 138

6.5. Density of interface states of a control sample (2 hours Ar at 1175 °C) and of some annealed for 7.5, 15, 30, and 120 minutes in NO. . . . 139

6.6. $D_{it}$ reduction, and normalized $D_{it}$ reduction, after nitrogen saturation at the $SiO_2$/SiC interface. . . . 140

6.7. Evolution of the $D_{it}$ at different energy levels as a function of the area density of nitrogen incorporated by NO annealing, and normalized passivation cross-sections extracted form fits. . . . 142

6.8. Effective charge trapped upon electron injection in an unpassivated oxide, and in oxides annealed for 15 and 60 minutes in NO. . . . 146

6.9. Effective trapped charge upon hole injection in oxides annealed for various times in NO. . . . 147

6.10. Positive trapped charge, following fixed injections conditions, as a function of N area density . . . 148

6.11. ESR spectra of oxides before and after NO annealing on Si and SiC . . . 149

7.1. (a) Different regimes in a current density vs. oxide field curve. (b) Extrapolation of the mean time to failure at operating fields. . . . 158

7.2. Sample layout for TDDB measurements. . . . 162

7.3. Schematic of the TDDB electrical connections. . . . 163

7.4. AFM images of the (0001) SiC surface of implanted samples after activation anneal. . . . 164

7.5. SIMS profile of the nitrogen concentration in implanted SiC samples. . . . 165

7.6. (a) Cumulative percent failure as a function of stress time, and (b) mean times to failure, of devices fabricated on different surfaces. . . . 166

A.1. Quartz tube at high temperature. . . . 174

A.2. Schematic of the oxidation setup. . . . 175

A.3. Picture of the oxidation setup. . . . 175

A.4. List of the major components of the oxidation setup. . . . 176

A.5. Picture of the inlet side of the oxidation tube, and of the control units. . 177

A.6. Schematic of the high purity oxidation tube. . . . . . . . . . . . . . . . . 178

A.7. Schematic of the quartz sample holder. . . . . . . . . . . . . . . . . . . . . 178

A.8. Pictures of the custom-built regulator panel, the selection valves, the in-line filters, and the mass-flow controllers. . . . . . . . . . . . . . . . . . . . 179

A.9. Aluminum support for five 1/4" Swagelok valves SS-4BK. . . . . . . . . . 180

A.10. Aluminum support for five MKS controllers 1179A. . . . . . . . . . . . . 180

A.11. Picture of the furnace vacuum line. . . . . . . . . . . . . . . . . . . . . . 181

A.12. Schematic of double-bubbler design. . . . . . . . . . . . . . . . . . . . . . 182

A.13. Picture of custom-built bubbler. . . . . . . . . . . . . . . . . . . . . . . . 182

A.14. Thick-wall tube for high pressure oxidation. . . . . . . . . . . . . . . . . . 184

A.15. Pictures of high pressure oxidation setup. . . . . . . . . . . . . . . . . . . 184

A.16. High pressure oxidation procedure - page 1 . . . . . . . . . . . . . . . . . 185

A.17. High pressure oxidation procedure - page 2 . . . . . . . . . . . . . . . . . 186

A.18. High pressure oxidation procedure - page 3 . . . . . . . . . . . . . . . . . 187

B.1. Picture of the CV probe station under UV illumination. . . . . . . . . . . 188

B.2. Picture of the automated injection setup. . . . . . . . . . . . . . . . . . . 189

B.3. Some key components of the injection setup. . . . . . . . . . . . . . . . . 189

B.4. Hg lamp spectrum, and broadband mirror reflectance. . . . . . . . . . . . 190

B.5. Electrical connections of the automated injection setup. . . . . . . . . . . 191

B.6. Screen capture of the LabVIEW program designed for automated injection. 193

C.1. Picture of a TDDB sample contacted by the probe card and the normal probe. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 194

C.2. Picture of the TDDB setup. . . . . . . . . . . . . . . . . . . . . . . . . . 195

C.3. List of parts used in the TDDB setup. . . . . . . . . . . . . . . . . . . . . 195

C.4. Pictures of the TDDB probe station and of the custom-built hot chuck. . 196

C.5. Schematic of the TDDB probe card. . . . . . . . . . . . . . . . . . . . . . 197

C.6. Picture of the TDDB probe card. . . . . . . . . . . . . . . . . . . . . . . . 197

C.7. Schematic of the TDDB setup electrical connections. . . . . . . . . . . . . . 198

C.8. Custom LabVIEW program controlling TDDB measurements. . . . . . . . 200

# INTRODUCTION

Energy efficiency is a primary concern in modern society because of increasing power consumption and decreasing natural resources. Indeed, in 2005 the worldwide power consumption was 15 TW ($15\times10^{12}$ Watts), nearly doubling the value from 1980.[a] About 90 % of the energy is currently generated by burning fossil fuels, a non-renewable resource. This process also leads to the massive release of pollutants in the atmosphere.

A global effort has been started towards the implementation of energy efficient electronics. In particular, there is much interest in silicon carbide (SiC), a large band-gap semiconductor which enables the control of high voltage signals with an efficiency orders of magnitude higher than the widespread silicon-based devices. Moreover, the reduced cooling requirements of SiC devices allow for less bulky and lighter components. These advantages over silicon have triggered the attention of the electricity distribution and generation industry, of the transportation sector, and of the military. Active research has been dedicated to silicon carbide since the 1990's. As a result, bipolar SiC transistors and diodes have become commercially available very recently. Already, major automotive companies plan to use SiC-based power converters in hybrid vehicles within the next decade. However, SiC technology is still very young and many obstacles remain to be overcome in order to take full advantage of the material potential. In particular, oxide-based devices, such as field-effect transistors, still need to be optimized before their release on the market.

Even though silicon carbide has been preferred over other wide band-gap semiconductors because of its unique ability to grow a thermal oxide, challenges lie in the quality of the dielectric and of the $SiO_2$/SiC interface. The high fields present in high-power devices increase the electrical stress in the oxide. The properties of the oxide/semiconductor interface directly affect the device resistance, which has to be minimized to guarantee efficiency.

[a] Source: Energy Information Administration, official energy statistics from the U.S. government, http://www.eia.doe.gov

Furthermore, the oxide and the interface have to withstand operating conditions without changing the specifications of a device.

This thesis focused on the electrical properties and the reliability of the oxide and its interface with silicon carbide. In particular, the effects of processing parameters, such as (i) implant activation, (ii) oxidation conditions, and (iii) post-oxidation anneal, are considered. Measurements are performed on metal-oxide-semiconductor (MOS) capacitors formed on 4H-SiC, the most widely used polytype.

(i) The high-temperature dopant activation anneal, following implantation in SiC, leads to the roughening of the surface which is subsequently oxidized. From time-dependent dielectric breakdown measurements (TDDB), it is found that this greatly reduces the lifetime of oxide-based devices. However, this reduction can be prevented by protecting the surface during high temperature activation, using a carbon cap, or by polishing the SiC surface afterwards.

(ii) The effects of oxidation rate and temperature on the interface properties are studied independently by adjusting the oxygen partial pressure during thermal growth. This enables the study of oxidation kinetics on SiC by mean of the Deal-Grove model, which is found to apply above a critical oxide thickness.

(iii) The main issue addressed in this work is the impact of nitrogen on the aging of devices. Indeed, post-oxidation anneals in nitric oxide (NO) have been adopted by the SiC research community because it introduces nitrogen at the interface, yielding the passivation of defects and improved device performance. Injection of excess carriers by tunneling, photoemission, and irradiation, are used to characterize the degradation of device with unpassivated or NO-annealed oxides. The results reveal that nitrogen can be beneficial or detrimental to the reliability of an oxide-based SiC device depending on the polarity of trapped carriers. Attempts are made to identify the responsible mechanisms by varying the density of incorporated nitrogen, so as to optimize both the mobility and the reliability.

The findings and the analysis reported in the thesis have led to the publication of three peer-reviewed manuscripts; in *Applied Physics Letters*, in the *Journal of Applied Physics* and in the *IEEE Transactions on Nuclear Science*. A fourth manuscript has been accepted for publication and other submissions will follow. During this research effort, three experimental setups, detailed in the appendices, have been designed and implemented for (high pressure) semiconductor oxidation, automated carrier injection, and time-dependent dielectric breakdown measurements.

The thesis is divided in two parts. *Part One* includes a review of silicon carbide properties (Chapter I) and metal-oxide-semiconductor physics (Chapter II). Particular emphasis is put on the characteristics of SiC field-effect transistors, on the understanding of the $SiO_2$/SiC interface, and on the transport and injection mechanisms in amorphous gate dielectrics. *Part Two* consists of the studies on the properties and the the reliability of the oxide and the interface: pressure dependence of $SiO_2$ growth kinetics (Chapter III), impact of nitrogen incorporation on electron (Chapter IV) and hole (Chapter V) trapping, dependence of interface properties on nitrogen density (Chapter VI), and accelerated breakdown on implanted surfaces (Chapter VII). The results, and the current understanding of the physical processes involved, are summarized in the Conclusion.

**PART ONE**

# A REVIEW OF SiC TECHNOLOGY AND METAL-OXIDE-SEMICONDUCTOR PHYSICS


| | | |
|---|---|---|
| Chapter I: | SiC material and device properties | 5 |
| Chapter II: | MOS physics | 37 |

# CHAPTER I

# SiC MATERIAL AND DEVICE PROPERTIES

## Overview

SiC is the only compound of silicon and carbon known to date. Its structure leads to a wide energy gap and to an excellent thermal conductivity. As explained in this chapter, these properties and the fact that it can grow a thermal oxide makes SiC suitable for high-power devices that can work in extreme conditions. In order to reach that goal however, many issues remain to be addressed. The ones considered here are the quality of the SiC wafers, the properties of the $SiC/SiO_2$ interface, and the reliability of the gate oxide.

## 1.1 Semiconductor Properties

Silicon carbide can exist under various crystal structures called polytypes.[1] They all have a common building block: the Si-C tetrahedron [Figure 1.1(a)]. It consists of one Si atom bonded to four C atoms (or one C bonded to four Si). The Si-C bond length is 1.89 Å, indicating a stronger atomic interaction than in silicon crystals in which the Si-Si bond

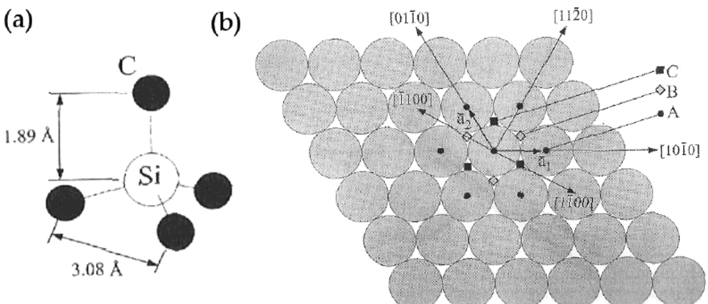



**Figure 1.1:** (a) The basic structural unit in SiC is a tetrahedron of four carbon atoms with a silicon atom in the middle. (b) A close-packed hexagonal plane of spheres, with centers at points marked $A$; a second and identical plane can be placed atop the first plane, with centers over either the points marked $B$ or the points marked $C$.[1]

**Table 1.1:** Key constants of 4H-SiC and silicon.[1,2,3,4]

| Quantity | 4H-SiC | Silicon |
|---|---|---|
| Band-gap $E_g$ (eV) | 3.26 | 1.12 |
| Electron mobility $\mu_e$ (cm$^2$ V$^{-1}$s$^{-1}$) | 1000 | 1400 |
| $\mu_\perp/\mu_\parallel$ | 0.8 | 1 |
| Hole mobility $\mu_h$ (cm$^2$ V$^{-1}$s$^{-1}$) | 115 | 471 |
| Electron effective mass $m^*/m_0$ | 0.29-0.42 | 0.26 |
| Critical field $\xi_c$ (MV/cm) | 2.2 | 0.3 |
| Dielectric constant $\epsilon_s/\epsilon_0$ | 6.5-6.7 | 11.7 |
| Young's modulus $Y$ (GPa) | 100-750 | 47 |
| Thermal conductivity $\theta$ (Wcm$^{-1}$K$^{-1}$) | 3.7 | 1.5 |
| Debye temperature $T_d$ (K) | 1300 | 640 |

length is 2.35 Å. Indeed, SiC is a stiffer material than Si as revealed by Young's modulus (see Table 1.1 for a comparison of key constants of Si and SiC). This and the fact that carbon is a lighter atom, leads to the promotion of lattice vibrations, giving SiC a higher thermal conductivity.

The polytypes can be constructed by stacking a close-packed planar hexagonal array of the Si-C tetrahedra joined to each other at the corners [Figure 1.1(b)]. Following the addition of each plane, the upper tetrahedra can be aligned between the bottom ones in two different ways. $A$ is taken as the reference plane and the added planes are denoted $B$ or $C$ depending on their alignment. Furthermore, the tetrahedra can be rotated by 180 degrees along the stacking direction. If it is the case, the planes are labeled $A'$, $B'$ and $C'$. There are some restricting rules but it is clear that there are many stacking sequences possible and indeed, over 250 polytypes have been reported. However, the resulting lattice structure can only be cubic, hexagonal or rhombohedral. Cubic SiC is called 3C because it is made of the recurring stacking sequence ABC. An example of hexagonal SiC is the 4H polytype made of the sequence ABA'C'. Although all crytalline structures yield a wide band-gap, 4H-SiC is the preferred electronic material because it has the widest band-gap ($\simeq$ 3.3 eV) among

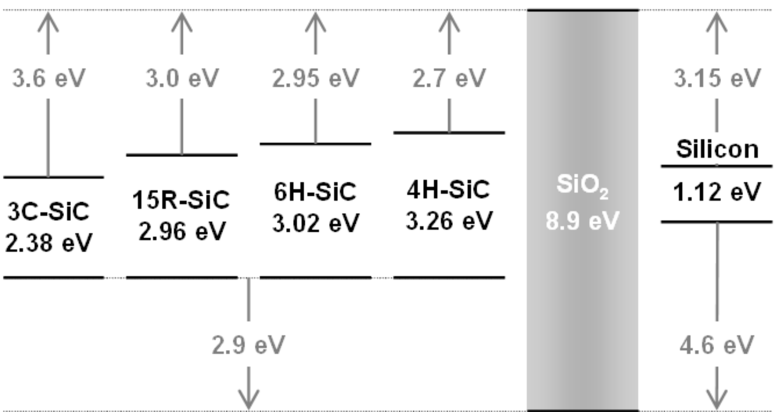



**Figure 1.2:** Energy gaps and relative band-offsets of Si, $SiO_2$, and common SiC polytypes. Compiled from results by Afanas'ev *et al.*[5]

the common polytypes (see Figure 1.2) and because it has a high electron mobility which is nearly isotropic.

The hexagonal unit cell is shown in Figure 1.3. The most commonly used crystal faces for device processing are the (0001) Si-face, the $(000\overline{1})$ C-face and the $(11\overline{2}0)$ a-face. They each have a different density of silicon and carbon atoms; the Si-face has 100% Si atoms, the C-face has 100% C atoms and the a-face has 50% of each. This leads to distinct oxidation rates and interface properties.

As in the case of silicon, $SiO_2$ can be grown thermally on SiC, which makes it the best candidate wide band-gap material for electronics application as the Si technology and tools can be directly transferred to its processing. Oxide thicknesses obtained by dry oxidation at 1150 °C on the three faces and on silicon (100) are shown as a function of time in Figure 1.4. Such a high temperature is required in order to grow oxides in reasonable time. Indeed, the oxidation is up to 10 times slower on the Si-face than on Si (100) but it is only 5 times slower on the C-face as the $SiO_2$ growth rate on SiC scales with the carbon surface areal densities. Such distinctive kinetics can be related to the complex oxidation process which requires the ejection of carbon. A net oxidation reaction can be written as

$$2\ \mathrm{SiC} + 3\ \mathrm{O_2} \rightarrow 2\ \mathrm{SiO_2} + 2\ \mathrm{CO} \tag{1.1}$$

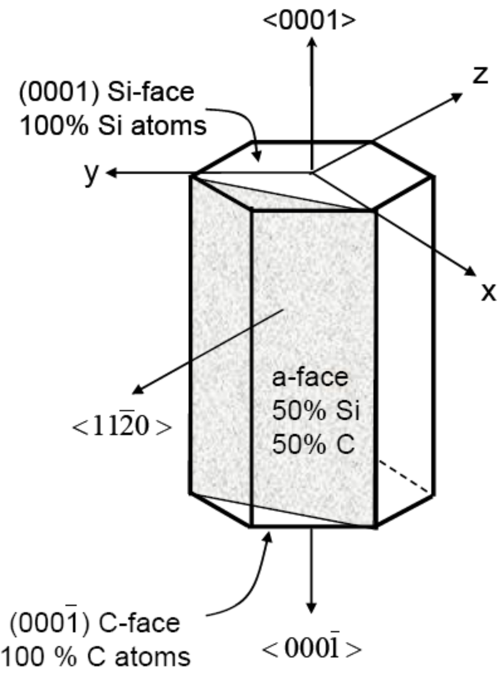



**Figure 1.3:** Hexagonal unit cell. Common orientations used to grow oxides on SiC. Relative Si and C contents are indicated.[6]

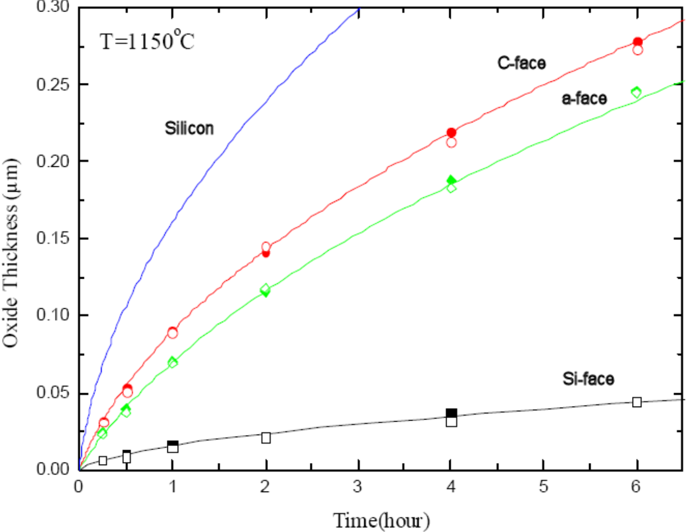



**Figure 1.4:** Evolution of the thickness of oxides grown on three different faces of 4H-SiC at 1150 °C in dry $O_2$. Values are measured by ellipsometry (filled symbols) or Rutherford backscattering (empty symbols). Silicon (100) is shown as a reference.[6]

As on Si, oxygen inserts in the semiconductor to form $SiO_2$ but some of it is also necessary to remove carbon via CO out-diffusion. It will be shown in Chapter III that SiC oxidation can be modeled using the Deal-Grove kinetics derived for Si.

Another benefit of having a thermal oxide is that the quality of the $SiO_2$/SiC interface, a critical parameter in oxide-based devices, is expected to be better than in the case of a deposited dielectric. However, the complex oxidation process can lead to a variety of interface defects. Surface conditioning, oxidation conditions and post-oxidation anneals have therefore proven to be key in the realization of a SiC technology. The impact of these steps on interface quality and device reliability is the subject of this Thesis.

## 1.2 SiC Device Physics

SiC is suitable for high-power devices that can outperform Si technology. Indeed, the operating voltages of Si-based electronics are limited by the breakdown field of the material ($\simeq 3\times10^5$ V/cm) and by the resulting maximum blocking voltage of PN junctions.

### 1.2.1 Critical field and blocking voltage

The kinetic energy of carriers is proportional to the electric field. In solids, they are thermalized by phonon interactions which yields a finite carrier velocity at low fields. When the field exceeds a critical bulk value $\xi_c$, the rate at which a carrier gains energy is faster than the rate at which it can exchange it with the lattice. In that case, hot carriers in a semiconductor can reach energies of the order of the band-gap and induce breakdown via the multiplication of electron-hole pairs, a phenomenon called avalanche. The energy of the phonon distribution is therefore key in determining the critical field; the higher the phonon energy, the higher the field at which carriers can be thermalized. The Debye temperature $T_d$ can be used to estimate the average phonon energy. The critical field is therefore expected to be larger in SiC than in Si, according to the values of $T_d$ reported in Table 1.1. Indeed, $\xi_c$ is measured at $2.2\times10^6$ V/cm in 4H-SiC, an order of magnitude higher than in Si. Note

that since SiC and Si are indirect band-gap semiconductors, the phonons are also involved in the inter-band transitions associated with impact ionization. Transport and breakdown mechanisms are discussed in more details in the first section of Chapter II.

The blocking voltage of PN junctions in reverse bias is limited by the current of minority carriers that can lead to an avalanche process in the space-charged region.[7,3] This breakdown mechanism is similar to the one described in the bulk of the material. In the case of a one-sided junction (e.g. n doping $\ll$ p doping), the reverse bias leads to the depletion of carriers almost exclusively in the lowly doped region. If the highly doped region is grounded and a large positive bias $V_d \gg E_g/q$ is applied to a lowly n-doped region, the width of the depletion layer in the step junction approximation is given by

$$x_d = \sqrt{\frac{2\epsilon_s V_d}{qN_d}} \tag{1.2}$$

where $N_d$ is the density of positively charged donor atoms, $\epsilon_s$ is the dielectric constant of the semiconductor and $q$ is the elementary charge. The value of the electric field reaches a maximum $\xi_{max}$ at the junction

$$\xi_{max} = -2\,\frac{V_d}{x_d} = -\sqrt{\frac{2qN_dV_d}{\epsilon_s}} \tag{1.3}$$

Assuming that avalanche breakdown occurs when $\xi_{max}$ reaches the critical field $\xi_c$, it can be deduced from Eq.(1.3) that the maximum blocking voltage that can be supported by the PN junction is

$$V_c = \frac{\epsilon_s \xi_c^2}{2qN_d} \tag{1.4}$$

The maximum achievable blocking voltage for a given dopant concentration is therefore expected to be about 30 times more in a SiC PN junction than in an Si diode.

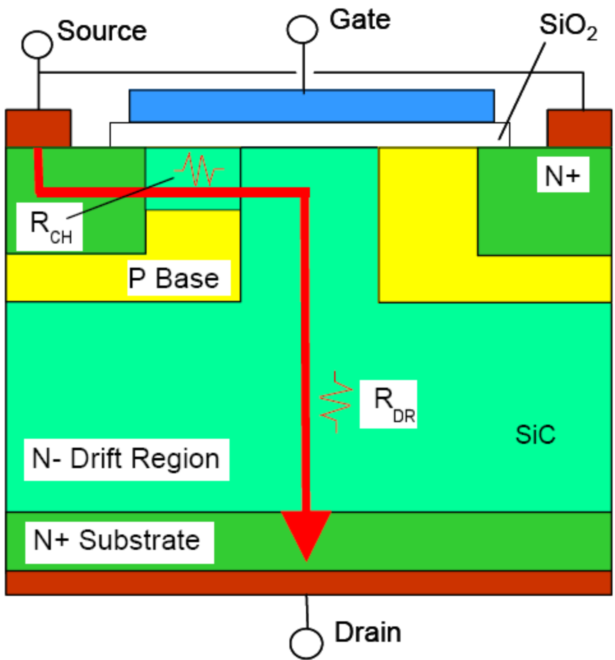



**Figure 1.5:** Layout of a n-channel SiC power DMOSFET. In the OFF state, the PN junction formed by the drift region and the base supports the positive drain voltage, there is no current. In the ON state, a positive bias applied to the gate leads to an inversion layer and to the formation of a channel in the base region, allowing current to flow between the source and the drain.[8]

### 1.2.2 SiC power MOSFET

The layout of a n-channel vertical double-implant metal-oxide-semiconductor field-effect transistor (DMOSFET) is illustrated in Figure 1.5. The channel regions are formed by a base P implant in a $N^-$ substrate. A shallower $N^+$ implant follows to form the source regions. The $N^-$ region remaining after the base and source implants is called the drift region. The drain contact is made at the bottom of the device.

In the OFF state, the source and the gate are grounded so that the PN junction, established by the base layer and the drift region, is reverse-biased with respect to the positive drain voltage $V_d$. The depletion layer extends in the drift region as its doping level is lower than the one of the base.

In the ON state, a positive bias is applied to the gate so that an inversion layer forms in the base region below the gate oxide and current flows between the source and the drain. As

there is a resistance associated with the device, energy can be dissipated. Since this results in signal loss and local heating, the specific resistance (in $\Omega$ cm$^2$), which is the resistance normalized by the active area, should be minimized. In this section, two of the main components of the total specific ON resistance are discussed: the drift specific resistance and the channel specific resistance.

If the current spread in the drift layer is neglected,[9] the specific drift resistance $R_{dr}$ equals the product of the drift region thickness and of the resistivity $r_{dr}$

$$r_{dr} = \frac{1}{q\mu_{dr}N_d} \tag{1.5}$$

where $\mu_{dr}$ is the majority carrier mobility in the drift region (in cm$^2$V$^{-1}$s$^{-1}$). As the thickness of the drift region is only limited by the extent of the depletion region in the ON state, the latter should be minimized for given operating voltage $V_d$. This can be achieved by adjusting the doping level so that $V_d = V_c$. From Eq.(1.4), the optimum concentration $N_d^*[V_d]$ is such that

$$qN_d^* = \frac{\epsilon_s \xi_c^2}{2V_d} \tag{1.6}$$

and from Eq.(1.2)

$$x_d^* = \frac{2V_d}{\xi_c} \tag{1.7}$$

It can then be shown that

$$R_{dr}^* = r_{dr}^* x_d^* = \frac{4V_d^2}{\mu_{dr}\epsilon_s\xi_c^3} \tag{1.8}$$

Accordingly, the optimum specific resistance $R_{dr}^*$ in SiC at a given blocking voltage is about 400 times lower than in silicon. Also, the necessary drift layer thickness $x_d^*$ is about an order of magnitude smaller, i.e. only several microns in devices designed to block voltages in the kV range.

The theoretical limits for the specific resistance in silicon and 4H-SiC are shown in Figure 1.6, together with the values extracted from actual SiC-based devices. It is seen that

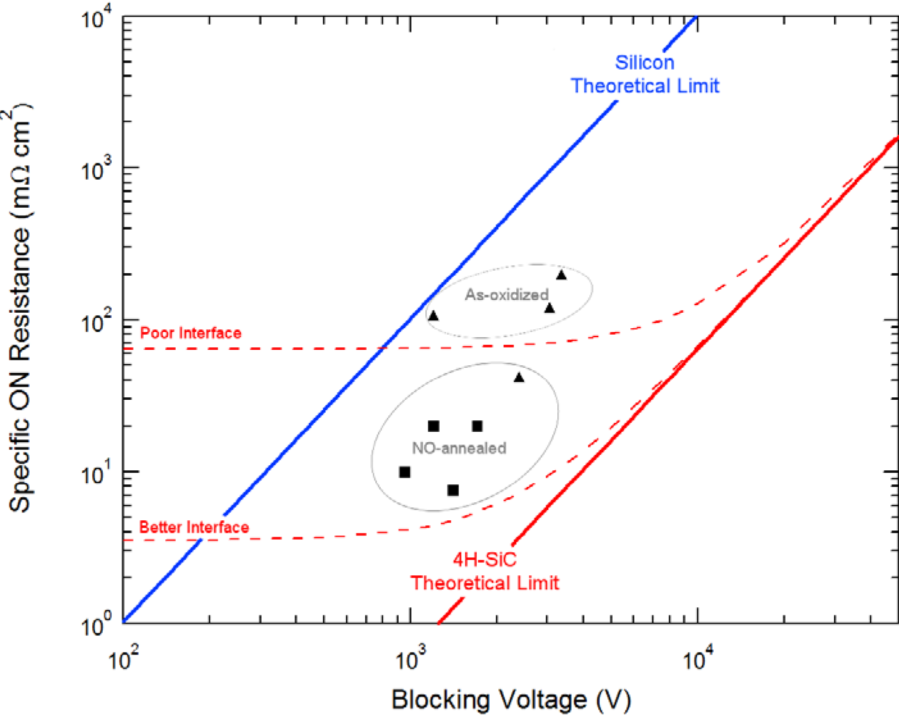



**Figure 1.6:** Achievable specific ON resistance as a function of the designed blocking voltage for Si and 4H-SiC devices. The continuous lines indicate the theoretical limits set by the drift resistance alone. The dotted lines show the impact of the channel resistance on the total resistance for a poor (as-oxidized) and a better (NO-annealed) interface. The symbols correspond the values extracted from actual SiC MOSFETs fabricated before[10,11,12] (triangles) and after[13,14,15,16] (squares) 2001.

the specific resistances of the devices can be much lower than the Si limit, but are still not close to the predicted values for SiC. There are three reasons for this. (i) The mobility in the drift region is limited by the quality of the available substrates as briefly mentioned in the next section. (ii) Although the vertical MOSFET design minimizes the oxide field in the OFF state, gate leakage can still affect the maximum blocking voltage which means that the achievable specific resistance depends on the quality and the reliability of the oxide and of the $SiO_2$/SiC interface. This will be explained in more detail. (iii) Other components of the specific resistance can dominate at lower blocking voltages, in particular the one related to the channel formed in the base region.

The specific ON resistance of the channel $R_{ch}$ is inversely proportional to the inversion charge density $Q_{ch}$ (in C/cm$^2$) and to the channel mobility $\mu_{ch}$. The exact expression is

derived from the saturation current[3,7] which yields[9]

$$R_{ch} = \frac{L\,P}{\mu_{ch} Q_{ch}} = \frac{\epsilon_{ox} L\,P}{\mu_{ch} \xi_{ox}} \tag{1.9}$$

where $\epsilon_{ox}$ is the oxide dielectric constant, $\xi_{ox}$ is the oxide field in the ON state, $L$ is the channel length and $P$ is the cell pitch. Again, the values of $L$ and $P$ have to be optimized in the design and $\xi_{ox}$ is limited by the reliability of the oxide. By taking typical values for these parameters ($L = 1\,\mu$m, $P = 20\,\mu$m and $\xi_{ox} = 3\,$MV/cm),[9] one can estimate the impact of $R_{ch}$ on the total specific resistance. This is shown in Figure 1.6 where the sum of the drift resistance and the channel resistance for 4H-SiC is plotted as a function of the designed blocking voltage (dashed lines). Two different values of $\mu_{ch}$ were used: 3 and 55 cm$^2$V$^{-1}$s$^{-1}$. They correspond to the known values for the "poor" as-oxidized interface and the "better" NO-annealed interface on the 4H-SiC (0001) Si-face. Details on the post-oxidation nitric oxide (NO) treatment are given in the next section. As predicted by Eq.(1.9), increasing the channel mobility allows for a lower specific resistance. Indeed, SiC MOSFETs fabricated using the NO process have a specific resistance closer to the theoretical limit. As, the channel resistance does not directly depend on the blocking voltage, it sets a lower limit on the achievable total resistance of a device. Although the use of NO enables SiC MOSFETs to compete with Si at even lower voltages, the currently achievable channel mobility is still only about 5 % of the SiC bulk value, suggesting that there is room for improvement. This can be achieved by further reducing the amount of interface defects and by optimizing the post-implantation anneals necessary to activate the dopant.

### 1.3 Technology status and challenges

SiC-based devices can outperform Si in high-power applications. However, their properties are still far from being optimum, due in part to the quality of the substrate, of the oxide and of the interface. Now that the feasibility of high-power MOSFETs has been demonstrated, their reliability is attracting some interest. In particular, the role and the

impact of NO annealing is still under active investigation since it was implemented as part of device fabrication only after the year 2000.

In this section, the status of SiC is briefly reviewed in terms of the properties of the available substrates, of the thermal gate oxide, and of the SiC/$SiO_2$ interface. It will be shown that although, considerable progress has been made in the last decade towards the implementation of an oxide-based SiC technology, there is still room for considerable improvements.

### 1.3.1 SiC wafer quality

Although SiC substrates have been commercially available only since the last decade, tremendous progress has been made regarding the quality and the size of the wafers. In about 15 years, the diameter of commercial SiC wafers has increased from 1 inch to 4 inches. This has led to a substantial reduction in material cost.

Two growing steps are required during the synthesis of electronic-grade single-crystal SiC substrates. First, a SiC boule is formed using physical vapor transport (PVT) of Si and C from a heated SiC poly-crystalline source onto a seed crystal.[17] Wafers are then obtained by slicing the SiC boule. Because of the hardness of the material, polishing is achieved using CMP (chemical-mechanical polishing).[18] Note that residual stress can lead to a wafer bow which can affect processing steps such as lithography.[19] For electronic applications, a high quality epi-layer, tens of microns thick, is then grown by high temperature chemical vapor deposition (CVD) typically using silane ($SiH_4$) and propane ($C_3H_8$).[20] Hot wall reactors have enabled uniformity of the epi-layer over large wafers and growth rates around 50 $\mu$m/h.

In order to reduce the amount of stacking faults, crystals are commonly grown along the $< 0001 >$ c-axis.[21] This leads to another major issue: micropipes. They are hollow-core dislocations extending throughout the substrate and act as "killer" defects limiting the yield of operating devices. Fortunately, improvements in growth techniques have led to

the reduction of their density from over $1000/cm^2$ in the 1990's to approximately 0 in 2007 in commercially available wafers. Polytype inclusions have been limited as well by off-axis epitaxial growth (typically 8° for 4H-SiC); it yields surface steps where homo-epitaxy can take place. Unfortunately, this also leads to an increased surface roughness and to step-bunching during high temperature implant annealing which affect channel mobility and oxide reliability. However, these effects can be minimized by using a carbon cap during the activation anneals or by subsequently polishing the surface, as shown in Chapter VII. Recent advances in SiC CVD growth enable the synthesis of high quality on-axis crystals which could suppress the need for surface steps.[22]

Other structural defects still strongly affect device properties. In particular, plane dislocations can reduce the achievable blocking voltages and stacking faults have been shown to limit long-term reliability of SiC diodes and to propagate upon operation.[19] Also, point defects such as vacancies can play a significant role in limiting the carrier lifetime which is intimately related to the bulk mobility.[23,24] Note that the bulk mobility is about an order of magnitude lower in p-type than in n-type SiC which currently makes n-channel MOSFETs the preferred devices. However, in order to expand the benefits of SiC technology, progress towards the fabrication of CMOS (complentary n- and p-channel MOSFETs) should be made.

Because the wafer quality limits the value of the bulk mobility and of the critical field, the achievable specific drift resistance is still higher than it could be [Eq.(1.8)]. One outstanding issue for materials grower is therefore to keep improving the techniques towards the further reduction of the defect density in order to optimize device properties and reliability.

### 1.3.2 The gate oxide

There is no evidence of any difference in the properties of the bulk of the thermal oxide grown on SiC as compared to that grown on Si. Indeed, it has been proven that SiC oxidation yields stoichiometric $SiO_2$ whose density, refractive index, dielectric constant

and breakdown strength are very similar to the ones of Si thermal oxides.[25] In particular, since C removal occurs during oxidation, the bulk of the oxide is essentially carbon free, as measured by the most sensitive analytical techniques.

However, as the growth kinetics are different, the thermal budget required to form a gate oxide of a given thickness on SiC is about ten times more than in the silicon case. Accordingly, CVD oxides can be deposited to reduce processing time, but a thermal $SiO_2$ layer is still necessary to ensure the quality of the interface. As shown in Chapter III, thermal growth itself can be accelerated by using high oxygen pressures. This allows for the oxidation of quality gate oxides in shorter times and/or at lower temperatures.

During oxide-based device operation, charge buildup in $SiO_2$ can result from carrier injection (see Chapter II for details on injection mechanisms). This leads to threshold voltage instabilities, to mobility degradation and ultimately to oxide breakdown, i.e device failure. It is therefore important to recognize in which conditions charge buildup can occur and how it affects the properties of a device.

As discussed earlier, in the OFF state of a DMOSFET, an electric field is present in the gate oxide and it can limit the achievable blocking voltages. This is related to the breakdown field of $SiO_2$ ($\simeq$ 10 MV/cm) and to gate leakage currents that can occur via tunneling or emission of carriers from the gate contact. Also, even if the oxide field is negligible above the base region, tunneling of majority carrier can take place and they can potentially trap in the dielectric within a few Ångströms of the interface.

In the ON state, a bias is applied to the gate in order to form an inversion layer in the base region. In the presence of high fields, this can lead to minority carrier injection from the semiconductor into the oxide via Fowler-Nordheim tunneling. As shown in Chapter II (Section 2.3.4), the distance $x_t$ a carrier has to tunnel in order to leak through the gate dielectric can be approximated by $\phi_{bo}/\xi_{ox}$, where $\phi_{bo}$ is the appropriate band-offset (in Volts) between the semiconductor and $SiO_2$. The tunneling probability depends exponentially on $x_t$. As illustrated in Figure 1.2, the band-offsets of 4H-SiC relative to $SiO_2$ are smaller than

the ones of Si.[5] For a given oxide field, this yields a leakage current in $SiO_2$ on 4H-SiC that is always larger than in $SiO_2$ on Si. This raises particular concerns for n-channel devices as the offset between the conduction bands of 4H-SiC and $SiO_2$ is only about 2.7 eV, promoting electron tunneling from the semiconductor towards the positively biased gate contact.

The injection of carriers in the ON state and in the OFF state leads to charge trapping in the oxide, to remote Coulomb scattering and to interface degradation. The density of electron and hole traps is therefore a key factor that determines device stability and reliability. In particular, it is found (Chapter IV) that the NO annealing required for interface improvement, also suppresses trap-assisted tunneling and prevents negative charge trapping. As the tolerance on electron leakage current is higher, the blocking voltage can be increased in both n- and p-channel devices. Also, in the ON state of n-channel devices, the gate bias can be increased. Therefore, NO annealing can lead to reduced energy dissipation and/or longer mean time to failure. However, it turns out that NO treatments greatly enhance hole trapping (Chapters V and VI). This is, of course, a major concern for the p-channel devices in the ON state but it can also affect the preferred n-channel devices in the OFF state as a hole accumulation layer is formed at the base/dielectric interface where most trapping takes place. Understanding of the $SiO_2$/SiC interface is therefore required in order to further improve the quality of oxide-based SiC devices.

### 1.3.3 The $SiO_2$/SiC interface

Unlike the properties of the $SiO_2$ bulk, the ones of the interface between the oxide and the semiconductor depend strongly on the substrate and on its orientation. The quality of the interface is directly reflected in the channel mobility of MOSFETs, a critical parameter for devices, as described earlier.

#### Scattering mechanisms

The true (Hall) mobility $\mu$ is defined as

$$\mu = \frac{q\tau}{m^*} \tag{1.10}$$

where $\tau$ is the mean scattering time responsible for the finite speed $\overline{v} = \mu\xi$ of the carrier in a solid. As various processes can induce scattering, $\tau$ can be decomposed into

$$\frac{1}{\tau} = \sum_i \frac{1}{\tau_i} = \frac{1}{\tau_{ph}} + \frac{1}{\tau_{Cb}} + \frac{1}{\tau_{lt}} + \frac{1}{\tau_{rg}} + ... \tag{1.11}$$

The contributing processes considered here are respectively carrier-phonon interactions, Coulomb scattering by charged centers, carrier trapping or recombination, and surface-roughness-induced scattering. From Eqs. (1.10) and (1.11), it results that the true mobility can also be written as

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu_i} \tag{1.12}$$

The dominating scattering process can usually be identified from the dependence of the mobility on the temperature and on the electric field.[3]

At the oxide/semiconductor interface, defects and surface-induced states can lead to localized energy levels within the band-gap. In the case of n-channel devices, an electron inversion layer is formed when the amplitude of the positive gate bias is large enough for the Fermi level to be close to the semiconductor conduction band edge at the interface (see Chapter II, Section 2.4.2). In that region, it implies that most levels lying within the band-gap are filled with electrons which reduces the density of free carriers and yields negatively charged centers. Ultimately, it leads to a reduced carrier lifetime and to enhanced Coulomb scattering. Therefore, the mobility in the channel is expected to be lower than in the bulk (e.g. the drift region). In the case of as-grown $SiO_2$ on 6H- and 4H-SiC, $\mu_{ch}$ is indeed a fraction of $\mu_{dr}$; about 25 and 1% respectively.[26] A good interface, like H-passivated $SiO_2$ on

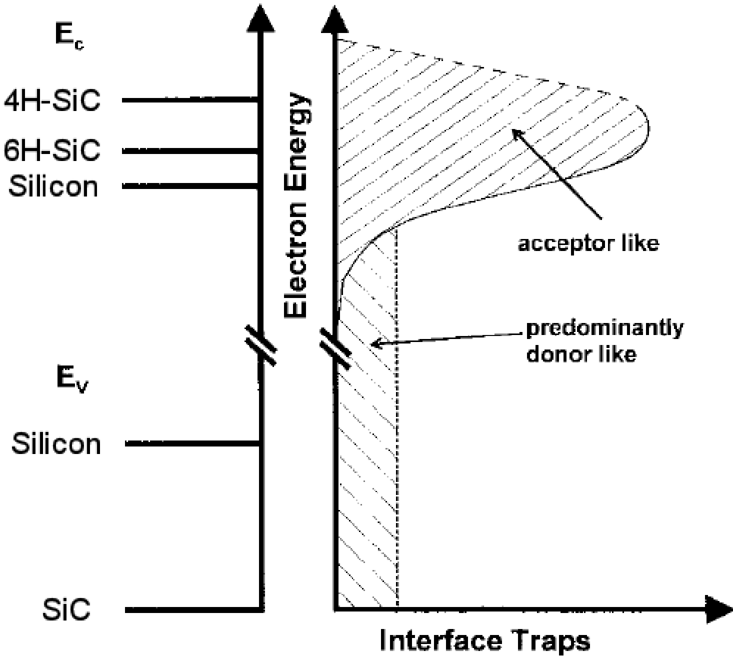



**Figure 1.7:** Schematic of the density of traps at the oxide/semiconductor interface. The relative positions of the conduction ($E_c$) and valence band edges ($E_v$) are indicated. 4H-SiC is sensitive to a larger amount of states than 6H-SiC and silicon. Illustration modified from a publication by Schörner *et al.*[27]

Si, can lead to mobilities that are only 50% less than in the bulk. [Unless specified, all the the values given in this section correspond to lightly doped n-channel devices with oxides grown on the (0001) Si-face of silicon-carbide.]

### Interface defects

The poor quality of the as-grown $SiO_2$/SiC interface has two origins: the wide SiC band-gap and the presence of carbon.

The energy gap of silicon-carbide makes it sensitive to a wider range of defects than silicon. At $SiO_2$/Si interfaces, electrically active defects include Si- dangling bonds on the substrate side,[28,29] and oxygen vacancies in the transition region of the oxide (Si-Si suboxide bonds).[30] The Si- dangling bonds can be passivated by hydrogen.[31,32] In addition, a large density of levels located about 2.8 eV below the $SiO_2$ conduction band edge has been

observed,[33,34,35] but since they are located within the Si conduction band, they do not affect the channel mobility at $SiO_2$/Si interfaces. In the case of SiC, electron spin resonance (ESR) measurements have not yet identified Si- dangling bonds at the interface.[36] Moreover, hydrogen passivation alone seems quite ineffective.[37,38,39,40] Although they cannot be ruled out, this suggests that Si- dangling bonds are not a dominant defect at $SiO_2$/SiC interfaces. On the contrary, suboxide bonds could contribute to the density of electrically active levels. The bonding-antibonding splitting depends on the length of the Si-Si bonds. Only bonds longer than 2.35 Å, the normal length in a Si crystal, can contribute to levels within the silicon band-gap. These are effectively passivated by hydrogen as-well. In the case of SiC, even the short bonds lead to active interface states because of the relative positions of the band edges (Figure 1.2). Theory suggests that these short bonds cannot readily be passivated by hydrogen.[37]

Similarly, the fact that the n-channel mobility in 4H-SiC devices ($\leq 10$ cm$^2$V$^{-1}$s$^{-1}$) is lower than in 6H-SiC devices ($\leq 100$ cm$^2$V$^{-1}$s$^{-1}$) can be attributed to levels located above the 6H-SiC conduction band edge and below the 4H-SiC conduction band edge, as these levels will trap carriers only at the $SiO_2$/4H-SiC interface. This is in good agreement with Hall mobility measurements which indicate a much larger reduction ($\simeq 90\%$) of the free electron density at $SiO_2$/4H-SiC interfaces when compared to $SiO_2$/6H-SiC interfaces ($\simeq 10\%$).[26] Those results also suggest that the density of states is largest close to the 4H-SiC conduction band edge. This gives rise to the qualitative picture for the distribution of levels illustrated in Figure 1.7. Capacitance-voltage (CV) and conductance measurements, which can resolve the energy distribution of the traps, show that the density of interface states ($D_{it}$) is indeed rising in the upper part of the SiC band-gap and is an order of magnitude higher close the conduction band edge of 4H-SiC as compared to 6H-SiC, respectively $\simeq \times 10^{13}$ and $\times 10^{12}$ cm$^{-2}$eV$^{-1}$ for as-grown oxides (Figure 1.8). Since the 4H-SiC n-channel mobility is found to increase with temperature (from 200 to 475K), it can also be inferred that the main mechanism limiting charge transport is Coulomb scattering of the remaining

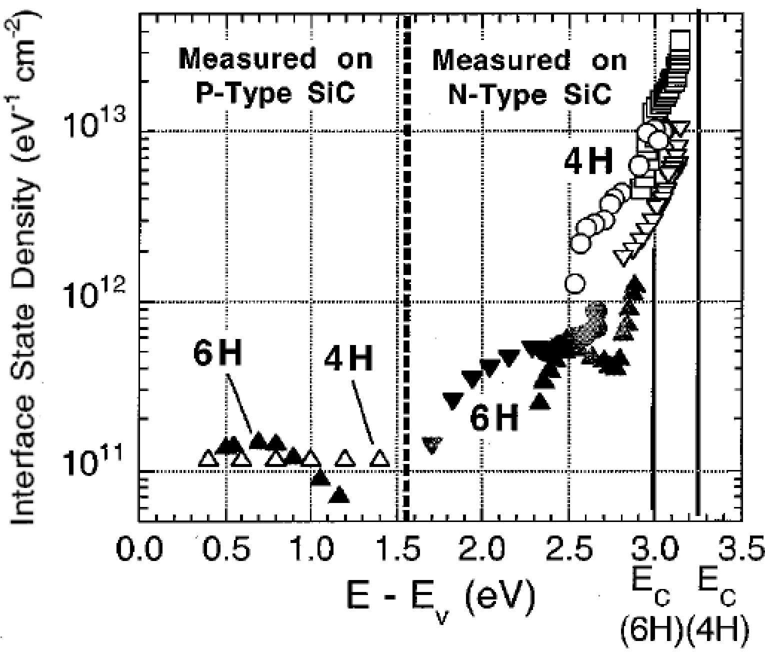



**Figure 1.8:** $D_{it}$ obtained by CV (triangles) and conductance (circles) measurements as a function of the energy within the band-gap of 6H- (filled symbols) and 4H-SiC (empty symbols). The $D_{it}$ at oxide interfaces formed on the Si-face of the two polytypes are similar throughout the gap and rises sharply between their conduction band edges.[45]

free carriers induced by the negatively charge centers. On the other hand, the 6H-SiC n-channel mobility decreases when temperature rises (from 200 to 500K), revealing a phonon limited transport, less affected by interface traps. Note that the high density of states located between the 4H- and 6H-SiC conduction band edges have not been assigned to a particular defect (suboxide bonds are a possibility). In any case, they correspond to the levels previously observed at Si interfaces located 2.8 eV below the $SiO_2$ conduction band edge which is indeed 0.1 eV below the 4H-SiC conduction band edge and therefore within the band-gap of that polytype. Since they have a slow response time and a wide energy distribution, it has been inferred that these states are due to near-interface defects within the oxide.[41,42,43,44] If they are $SiO_2$-related, it could explain why they are present on both Si and SiC. So although 4H-SiC is preferred over 6H-SiC for its greater bulk mobility, the high density of states corresponding to slow border traps fall within its band-gap only, which yields a lower inversion mobility and a higher channel resistance at as-oxidized interfaces.

The second reason for the high defect density at the as-grown $SiO_2$/SiC interface is the complex oxidation process [Eq.(1.1)] involving the release the carbon. It turns out that although the oxide appears free of carbon, it is not ideally removed from the interface during oxidation. Indeed, several techniques like Rutherford backscattering (RBS),[46,47,48,49] X-ray photo-electron spectroscopy (XPS),[50,51,52,53,54,55] transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS),[56,57,58] surface enhanced Raman spectroscopy,[59] and spectroscopic ellipsometry,[60] all have shown excess carbon present at the interface in a $Si_xC_yO$ transition layer which is found to extend about 1 nm into the oxide. Accordingly some C-related defects are expected to contribute to the $D_{it}$. ESR, the preferred tool for the identification of atomic configurations, has led to the detection of unsaturated, three-fold coordinated carbon, that might be referred to as C- dangling bonds.[36,61] In addition, XPS suggests the presence of C-C and Si-O-C bonds.

If slow near-interface defects are considered responsible for the high density of shallow states close to the conduction band edge of 4H-SiC, C-related defects may explain the trap levels within the rest of the band-gap. In particular, such defects would also explain the larger $D_{it}$ observed deep in the gap when the oxide is grown on C-containing faces such as the a-face (50% C atoms) and the C-face (100% C atoms) when compared to the Si-face (0% C atoms).[62] As these lower energies correspond to the ones of graphitic inclusions in diamond, a carbon cluster model has been proposed.[33] Excess carbon atoms could aggregate at the $SiO_2$/SiC interface, forming graphitic clusters of different sizes. The $\pi$ orbital of $sp^2$-bonded carbon is expected to give levels whose energy depends on the cluster size. Small C-clusters would have energies in the lower part of the gap and large ones would have a graphite-like energy distribution spanning the gap. A third C-related level in the upper part of the gap has been attributed to 3C-SiC inclusions at the $SiO_2$/4H-SiC surface. As the combined contributions of small C-aggregates, graphitic regions and 3C-inclusions could explain the shape of the $D_{it}$, the C-cluster model constitutes an interesting framework for the understanding of the interface. On the experimental front, atomic-force microscopy

(AFM),[63,64] performed after the removal of the oxide, TEM and EELS, have hinted the presence of carbon particles. However, *in situ* XPS studies, performed during oxidation,[52] reveal that there is no graphite layer exceeding 0.1 monolayer, and recent high-resolution TEM observations[44] categorically ruled out the existence of graphitic particles above the size of 7 Å, these values being limited by the resolution of the techniques. Accordingly, carbon clusters have not been directly observed at $SiO_2$/SiC interfaces. In any case, measurements indicate that they would not exceed a few atoms. If such small C-aggregates exist, their corresponding energy levels would depends strongly on their environment which is not accounted for in the isolated C-cluster model.

Theoretical simulations of the detailed $SiO_2$/SiC interface are therefore a useful complementary tool helping researchers to consider specific defects. Theory provides equilibrium atomic configurations, their charge-exchange properties and their corresponding trap levels. Before describing some theoretical predictions, it should be mentioned that such computations need to be considered carefully. Indeed, the extensive work that has been performed in that field relies on density-functional theory (DFT) which is unable to directly reproduce the real values of semiconductor band-gaps and therefore the calculated energy levels of atomic configurations are not expected to be 100% accurate. Also, the energy of a given defect strongly depends on its surroundings and on its localization relative to the $SiO_2$/SiC interface. Accordingly, the calculated values for each stable configuration refer to specific cases. Moreover, the theoretical work is based the identification of equilibrium defect configurations at a static interface and, therefore, considers the oxidation kinetics only to a certain extent. All that being said, the theoretical results provide a general understanding of the possible defects and of their impact on the density of interface states.

Some of the predicted defects and their respective energy levels within the 4H-SiC bandgap are illustrated in Figure 1.9. A more complete list of defects can be found in publications resulting from studies led by S. T. Pantelides,[65,66,37] and P. Deák.[67,68,69,70] Carbon is found to be stable in variety of configurations at the interface. For example, a single carbon can

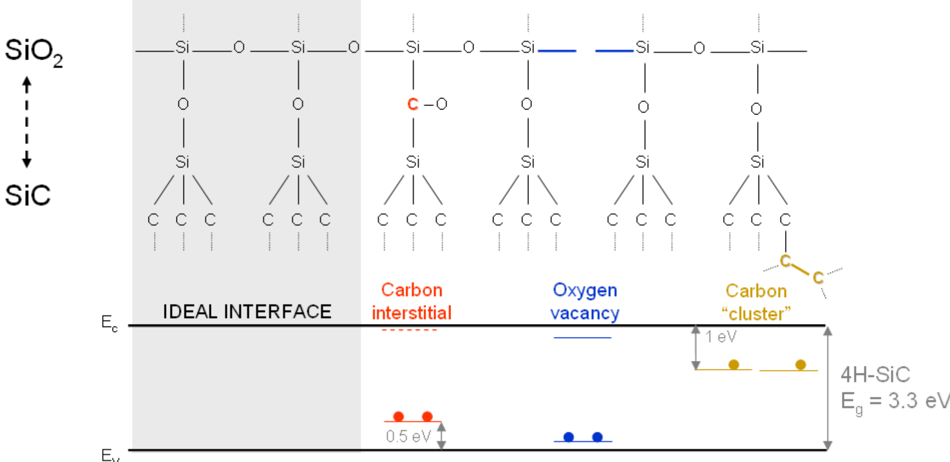



**Figure 1.9:** Different defects that can occur at the SiC/$SiO_2$ interface and their respective energy levels in the 4H-SiC band-gap. From results published by Wang, Pantelides *et al.*[37]

insert in a Si-O-Si bridge in two ways: by forming Si-C-Si with an oxygen protrusion or by forming Si-O-C-Si with the carbon weakly linked to a Si atom on a neighboring ring. These defects are found to be stable in the neutral and negatively charged states respectively. Split carbon interstitials sharing a Si-site on the substrate side could also occur. Note that that this yields a "C-cluster" of at most 6 atoms. In fact, DFT has demonstrated that large aggregates are not stable at the interface and simulations of the oxidation process have indicated that their size is limited by C-removal,[71] in good agreement with the experimental results mentioned above. Another proposed location for correlated carbons is a C-site on the substrate side. It has been proposed that this defect is so stable that it can "grow" into the oxide and result in a C-C bond linking two adjacent Si-C-O-Si bridges. The mentioned defects involve three-fold coordinated C atoms and could therefore explain the ESR signal. The unsaturated carbon in these stable configurations yields a level in the upper part of the 4H-SiC band-gap and one close to the valence band edge. Accordingly, these specific defects, unique to the $SiO_2$/SiC interface, correlate with the presence of excess carbon observed at the interface and could indeed explain the measured $D_{it}$.

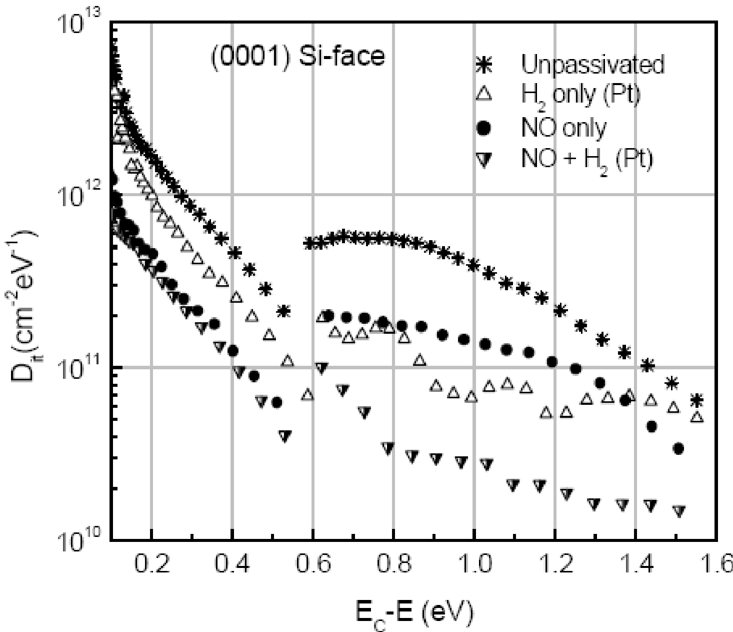



**Figure 1.10:** Interface trap densities in the upper half of the 4H-SiC band-gap obtained after different post-oxidation anneals. Discontinuities near $E_c$-E $\simeq$ 0.6 eV are the result of CV measurements taken at 23 °C and 300 °C, to extract $D_{it}$ below and above 0.6 eV from the conduction band edge respectively .[37]

**Interface passivation**

Oxidation and post-oxidation conditions can affect the $D_{it}$ distribution within the 4H-SiC band-gap. Both Ar anneals,[72] performed at growth temperature, and a re-oxidation,[73] performed at lower temperatures (around 900 °C), lead to a slight reduction of deep states. This has been associated with the removal of some of the excess carbon without any additional oxide growth and therefore without the generation of any new C-related defects. Also, wet oxidations can lead to a lower $D_{it}$ toward the center of the gap when compared to dry $O_2$ but still does not remove the slow near-interface states responsible for the poor 4H-SiC device properties.

The effects of water correlates with results from hydrogen post-oxidation anneals (POA) which have been performed before or after gate contact deposition. As mentioned earlier, hydrogen is very effective at the $SiO_2$/Si interface because it is able to passivate Si- dangling bonds and to insert into long Si-Si bonds, leading to the reduction of the $D_{it}$ from about

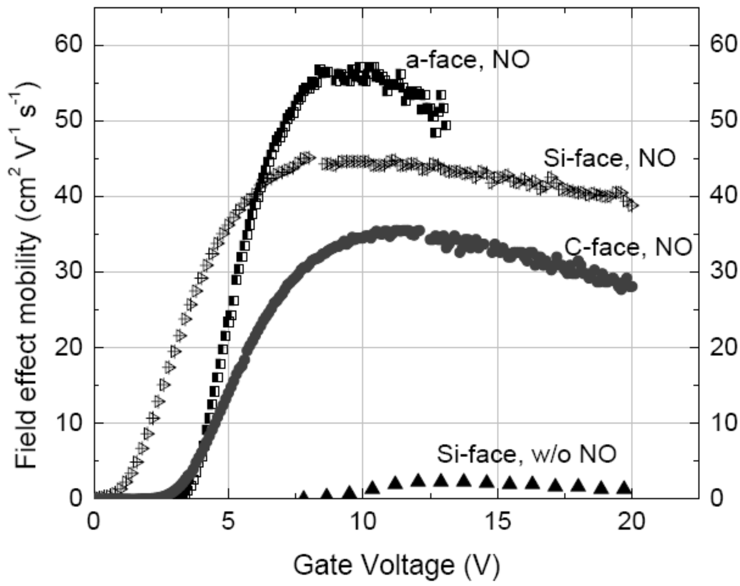



**Figure 1.11:** Improved channel mobilities extracted from MOSFETs fabricated on different faces of 4H-SiC. The Si-face mobility prior to NO annealing is shown as a reference.[74]

$10^{11}$ to $10^{10}$ cm$^2$eV$^{-1}$ in the middle of the Si gap. A high channel mobility, approaching half the value of the bulk mobility is then achieved. In the case of SiC, hydrogen has a limited effect that is confined to deep interface states which are only reduced down to about $10^{11}$ cm$^{-2}$eV$^{-1}$, even in the presence of a catalyst cracking $H_2$ into very reactive radicals [Figure 1.10].[37,38,39,40] Hydrogen does not affect the slow near-interface states. This demonstrates once again the difference between the $SiO_2$/Si and $SiO_2$/SiC interfaces. As Si- dangling bonds and long Si-Si bonds do not dominate the $D_{it}$ at SiC interfaces, hydrogen POA is not as efficient for SiC. Following $H_2$ exposure at 400 °C, C-H bonds have been detected by ESR at the $SiO_2$/SiC interface.[61] This correlates with some theoretical predictions,[37] and suggests that $H_2$ could bind to a minority of C-related defects, explaining the small but beneficial effect on the $D_{it}$.

In 1997, the group of S. Dimitrijev, at Griffitth University in Australia, demonstrated that high temperature (1100 °C) NO annealing reduces the $D_{it}$ at $SiO_2$/6H-SiC interfaces.[75] In 2000, Chung *et al.*[73] published results on the effects of NO at the $SiO_2$/4H-SiC interface revealing that, in addition to removing deep states, it is also very efficient at reducing the

density of slow states (by a factor of ten), Figure 1.10, and leads to an order of magnitude increase in the channel mobility to about 50 $cm^2V^{-1}s^{-1}$, Figure 1.11. This breakthrough discovery, which originated from the joint effort between Auburn University and Vanderbilt University, led to the adoption of the NO process by the scientific and industrial communities as it enables the fabrication of high quality oxide-based SiC power devices. Because it was introduced very recently, the understanding of the NO POA benefits are not totally understood and are the subject of active research at universities and companies around the world.

The impact of NO annealing has been attributed to the bonding of nitrogen at the interface (see Chapter VI). Indeed, medium energy ion scattering (MEIS),[6] nuclear reaction analysis (NRA),[76] secondary ion mass spectroscopy (SIMS),[77] and EELS,[58] have shown that NO POA leads to a nitrogen profile located at the $SiO_2$/SiC interface and extending at most 1.5 nm into the oxide. This length is comparable to the one of the transition layer observed after oxidation. The density of incorporated nitrogen is between $10^{14}$ and $10^{15}$ atoms/$cm^2$. Other ways that have been used to introduce N are plasma nitridation,[78] and $NH_3$ or $N_2O$ POA.[75,79,76,80] Plasma nitridation has led to similar improvements of the channel mobility but incorporates N throughout the oxide which could be detrimental to its reliability (see Chapters V and VI). Amonia ($NH_3$) shows benefits as well but incorporates unnecessary hydrogen and nitrogen in the oxide. Nitrous oxide ($N_2O$) only gets N at the interface but is not as efficient as nitric oxide (NO). This is because in both cases N incorporation is related to the cracking of NO molecules. $N_2O$ quickly decomposes into a small fraction of NO and a large fraction of $N_2$ and $O_2$ at high temperature, yielding a re-oxidation process negating the effect of nitrogen.[81]

Following NO exposure at high temperature, the amount of excess carbon at the $SiO_2$/SiC interface is reduced. In particular, AFM images reveal a smoother surface after the etching of an oxide that has been NO-annealed,[64] and XPS measurements indicate a reduction of the C-related compounds at the interface and the formation of Si-N and C-N bonds.[50] Ac-

cordingly the benefits of nitrogen could have two origins: N binding at defect sites and/or the removal of three-fold coordinated atoms following N substitution. The binding of N at unsaturated C- and potential Si-sites, could result in the formation of strong bonds eliminating defect levels from the gap. Substitution of three-fold C or Si by N could totally transform a given atomic configuration and therefore affect its corresponding energy levels as well. Theoretical studies of N affinity with defect sites located at the $SiO_2$/SiC interface have indeed shown that nitrogen could substitute for either Si or C atoms.[37,70] In particular, unlike hydrogen, nitrogen is predicted to be efficient at passivating short Si-Si suboxide bonds and C-C pairs of correlated carbons, the defects that are most likely responsible for the high $D_{it}$ and the poor mobility at as-grown interfaces. However, each substitutional nitrogen atom brings an extra valence electron to the system. A three-fold coordinated N has a lone pair of electrons in its outer shell. As it replaces Si or C, it is expected to remove the dangling bonds levels in the upper part of the 4H-SiC band-gap but also to induce a donor level associated with the lone pair close the valence band of the semiconductor. This could explain why NO annealing is very efficient in the upper part of the 4H-SiC band-gap but does not lead to clear improvement close to the valence band. In any case, this is apparently less critical for the mobility of n-channel devices whose value mostly depends on the reduction of the high density of levels close to the 4H-SiC conduction band, which is achieved by NO POA.

It should be noted that different forms of POA can also reduce the $D_{it}$ at interfaces formed on the a-face and on the C-face of 4H-SiC, yielding higher channel mobilities as well,[74] see Figure 1.11. In particular, the inversion mobility measured at interfaces formed on the a-face has been shown to improve to more than 100 $cm^2V^{-1}s^{-1}$ in some cases,[82,83] which is twice the mobility obtained on the Si-face after NO annealing. Therefore, even if the Si-face had been preferred prior to the introduction of POA, efforts should be put into the study of alternative faces as the picture has changed. UMOSFETs for example depend on the a-face channel mobility and although they were dismissed early,[9] they present several

advantages worth considering in light of the benefits of post-oxidation anneals. In addition, note that the a-face typically does not have a mis-cut which yields limited surface roughening during implant annealing, and reduced minority carrier scattering.

#### Process optimization

Three particular fabrication steps of oxide-based SiC devices are considered here. They are briefly discussed in terms of their respective impact on device quality and reliability.

*Channel implant.* In the DMOSFET design a double implant is required to form the base (channel) and source regions. Subsequently, a high temperature anneal (around 1500 °C) is required to activate the dopants. Problems associated with the implantation are ion-induced defects in the channel region and surface roughening upon annealing. Unfortunately, doping cannot be achieved by driving in the dopants because of the low diffusion coefficients of such atoms in SiC. One way to avoid this problem is to use a UMOSFET design in which the base and the source regions are formed by successive CVD epi-growths. However, UMOSFETs present issues of their own such as field crowding in sharp corners of the trench oxide.[9] The high temperature annealing in implanted devices also leads to surface roughening because of Si emission and step-bunching. The latter process originates from the presence of surface steps at the surface of SiC substrates that are grown off-axis in order to avoid polytype inclusions.[21] Following the growth of a gate oxide over the implanted region, the original surface roughness results in a lower inversion mobility and in a shorter mean time to failure (MTTF). In Chapter VII, it is shown that the roughness can be avoided by the use a carbon cap during implant annealing or by polishing the surface afterwards. These two techniques result in a MTTF comparable to the one of oxides grown on un-implanted smooth surfaces.

*Gate oxide growth.* The conditions at which the gate oxide is formed affect the quality of its interface with SiC. Recently, it has been reported that placing alumina in the vicinity of SiC during oxidation leads to growth rates that are up to ten times faster. Also, the interface formed with this process can lead to a lower $D_{it}$ and to a high channel mobility.[84,85,86] In

Chapter III, a study of the impact of the rate alone (no alumina, fixed temperature) on the quality of the interface, performed using dry oxidation at different $O_2$ partial pressures, is presented. In this work, the validity of Deal-Grove kinetics, widely applied to Si-oxidation, was tested as well. The implementation of a high pressure setup enables the growth of gate oxides on SiC at reduced thermal budgets.

*NO annealing.* The introduction of nitrogen at the $SiO_2$/SiC interface via post-oxidation NO annealing, leads to a reduced ON resistance associated with the channel in oxide-based devices. As shown in Figure 1.6, this allows the SiC power devices to out-perform silicon devices for operating voltages down to a few hundred Volts. Moreover, NO annealing leads to faster and sharper turn-on characteristics, which is important for the realization of high frequency devices.[87] Now that the benefits of the NO POA have been established, it is important to optimize the nitridation process in order to avoid excess nitrogen at the interface. Also, as the small band-offsets between SiC and $SiO_2$ raise concerns about the gate leakage upon operation, the impact of nitrogen on the stability of device properties has to be determined. The results in Chapter IV and V indicate that NO annealing can be beneficial or detrimental to long-term operation depending on the polarity of the carriers leaking through the gate. In particular, nitridation can lead to large threshold voltage instabilities when holes are trapped in the near-interface region. This motivates the understanding of the link between passivation and degradation, studied in Chapter VI, in order to achieve both interface quality and long-term device reliability.

### References

[1] K. Jarrendahl and R. F. Davis, *SiC Materials and Devices*, pp. 1–20, Academic Press London, 1998.

[2] J. B. Casady and R. W. Johnson, *Solid State Electronics* **39**, 1409 (1996).

[3] R. Muller and T. Kamins, *Device Electronics for Integrated Circuits*, Wiley New York, 2003.

[4] N. T. Son, W. M. Chen, O. Kordina, A. O. Konstantinov, B. Monemar, E. Janzen, D. M. Hofman, D. Volm, M. Drechsler, and B. K. Meyer, *Applied Physics Letters* **66**, 1074 (1995).

[5] V. V. Afanasev, M. Bassler, G. Pensl, M. J. Schulz, and E. S. von Kamienski, *Journal of Applied Physics* **79**, 3108 (1996).

[6] S. Dhar, *Ph.D. Thesis*, Vanderbilt University, 2005.

[7] S. M. Sze, *Semiconductor Devices, Physics and Technology*, Wiley New York, 1981.

[8] S. Dhar, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, *MRS Bulletin* **30**, 288 (2005).

[9] A. Agarwal, S.-H. Ryu, and J. Palmour, *Silicon Carbide: Recent Major Advances*, pp. 785–811, Springer, 2004.

[10] Y. Li, J. A. Cooper, and M. A. Capano, *Materials Science Forum* **389-393**, 1191 (2002).

[11] S. H. Ryu, A. Agarwal, M. Das, L. Lipkin, J. Palmour, and N. Saks, *Materials Science Forum* **389-393**, 1195 (2001).

[12] M. Imaizumi, Y. Tarui, H. Sugimoto, K. Ohtsuka, T. Takami, and T. Ozeki, *Materials Science Forum* **389-393**, 1203 (2002).

[13] D. Peters, SiC power devices for industrial inverters, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[14] R. Green, A. Ogunniyi, D. Ibitayo, G. Koebke, M. Morgenstern, A. Lelis, and C. Dickens, Evaluation of 4H-SiC DMOSFET's for high power electronics applications, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[15] K. Matocha, Z. Stum, S. Arthur, G. Dunne, and L. Stevanovic, 950 V 4H-SiC MOSFETs: DC performance and gate oxide reliability, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[16] K. Yamashita, K. Egashira, K. Hashimoto, K. Takahashi, O. Kusumoto, K. Utsunomiya, M. Hayashi, M. Uchida, C. Kudo, M. Kitabatake, and S. Hashimoto, Normally-OFF 4H-SiC power MOSFET with submicron gate, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[17] V. A. Dimitriev and M. G. Spencer, *SiC Materials and Devices*, pp. 21–76, Academic Press London, 1998.

[18] S. Monnoye, D. Turover, and P. Vicente, *Silicon Carbide: Recent Major Advances*, pp. 699–710, Springer, 2004.

[19] M. G. Spencer, J. Palmour, and C. Carter, *IEEE Transactions on Electron Devices* **49**, 940 (2002).

[20] A. Schoner, *Silicon Carbide: Recent Major Advances*, pp. 229–250, Springer, 2004.

[21] N. Ohtani, M. Katsuno, T. Fujimoto, and H. Yashiro, *Silicon Carbide: Recent Major Advances*, pp. 137–162, Springer, 2004.

[22] P. G. Neudeck and J. A. Powell, *Silicon Carbide: Recent Major Advances*, pp. 179–206, Springer, 2004.

[23] N. T. Son, M. Wagner, C. G. Hemmingson, L. Storasta, B. Magnusson, W. M. Chen, S. Greulich-Weber, J.-M. Spaeth, and E. Janzen, *Silicon Carbide: Recent Major Advances*, pp. 461–492, Springer, 2004.

[24] K. Danno, D. Nakamura, and T. Kimoto, Lifetime-killing defects in 4H-SiC epilayers and lifetime control by electron irradiation, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[25] C. Raynaud, *Silica Films on Silicon Carbide: a review of electrical properties and device applications*, pp. 1–31, Elsevier, 2001.

[26] N. S. Saks, *Silicon Carbide: Recent Major Advances*, pp. 387–410, Springer, 2004.

[27] R. Schorner, P. Friedrichs, D. Peters, and D. Stephani, *IEEE Electron Device Letters* **20**, 241 (1999).

[28] E. H. Poindexter, *Semiconductor Science and Technology* **4**, 961 (1989).

[29] C. R. Helms and E. H. Poindexter, *Reports on Progress in Physics* **57**, 791 (1994).

[30] P. M. Lenahan and P. V. Dressendorfer, *Journal of Applied Physics* **55**, 3495 (1984).

[31] K. L. Brower, *Physical Review B* **38**, 9657 (1988).

[32] K. L. Brower, *Physical Review B* **42**, 3444 (1990).

[33] V. V. Afanas'ev, F. Ciobanu, G. Pensl, and A. Stesmans, *Silicon Carbide: Recent Major Advances*, pp. 343–372, Springer, 2004.

[34] V. V. Afanas'ev and A. Stesmans, *Physical Review Letters* **78**, 2437 (1997).

[35] V. V. Afanas'ev and A. Stesmans, *Journal of Physics: Condensed Matter* **9**, L55 (1997).

[36] J. L. Cantin, H. J. von Bardeleben, Y. Shishkin, Y. Ke, R. P. Devaty, and W. J. Choyke, *Physical Review Letters* **92**, 15502 (2004).

[37] S. Wang, S. Dhar, S.-r. Wang, A. C. Ahyi, A. Franceschetti, J. R. Williams, L. C. Feldman, and S. T. Pantelides, *Physical Review Letters* **98**, 026101 (2007).

[38] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, *Physica Status Solidi A* **162**, 321 (1997).

[39] J. Campi, Y. Shi, Y. Luo, F. Yan, and J. H. Zhao, *IEEE Transactions on Electron Devices* **46**, 511 (1999).

[40] P. Friedrichs, E. P. Burte, and R. Schörner, *Journal of Applied Physics* **79**, 7814 (1996).

[41] S. Dimitrijev, P. Tanner, and H. B. Harrison, *Microelectronics Reliability* **39**, 441 (1999).

[42] V. V. Afanas'ev, A. Stesmans, M. Bassler, G. Pensl, and M. J. Schulz, *Applied Physics Letters* **76**, 336 (2000).

[43] T. E. Rudenko, I. N. Osiyuk, I. P. Tyagulski, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, *Solid State Electronics* **49**, 545 (2005).

[44] E. Pippel, J. Woltersdorf, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, *Journal of Applied Physics* **97**, 034302 (2005).

[45] J. A. Cooper Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, *IEEE Transactions on Electron Devices* **49**, 658 (2002).

[46] S. Dhar, Y. W. Song, L. C. Feldman, T. Isaacs-Smith, C. C. Tin, J. R. Williams, G. Chung, T. Nishimura, D. Starodub, T. Gustafsson, and E. Garfunkel, *Applied Physics Letters* **84**, 1498 (2004).

[47] T. Okawa, R. Fukuyama, Y. Hoshino, T. Nishimura, and Y. Kido, *Surface Science* **601**, 706 (2007).

[48] D. J. Hayton, T. E. Jenkins, P. Bailey, and T. C. Q. Noakes, *Semiconductor Science and Technology* **17**, L29 (2002).

[49] C. Radtke, I. J. R. Baumvol, and F. C. Stedile, *Physical Review B* **66**, 155437 (2002).

[50] H. Li, S. Dimitrijev, D. Sweatman, H. B. Harrison, P. Tanner, and B. Feil, *Journal of Applied Physics* **86**, 4316 (1999).

[51] A. Ekoue, O. Renault, T. Billon, L. Di Cioccio, and G. Guillot, *Materials Science Forum* **433**, 555 (2003).

[52] C. Virojanadara and L. I. Joahnsson, *Surface Science* **505**, 358 (2002).

[53] C. Virojanadra and L. I. Johansson, *Journal of Physics: Condensed Matter* **16**, 1783 (2004).

[54] B. Hornetz, H.-J. Michel, and J. Halbritter, *Journal of Materials Research* **9**, 3088 (1994).

[55] G. G. Jernigan, R. E. Stahlbush, and N. S. Saks, *Applied Physics Letters* **77**, 1437 (2000).

[56] K. C. Chang, N. T. Nuhfer, L. M. Porter, and Q. Wahab, *Applied Physics Letters* **77**, 2186 (2000).

[57] K. C. Chang, L. M. Porter, J. Bentley, C. Y. Lu, and J. Cooper, J., *Journal of Applied Physics* **95**, 8252 (2004).

[58] K. C. Chang, Y. Cao, L. M. Porter, J. Bentley, S. Dhar, L. C. Feldman, and J. R. Williams, *Journal of Applied Physics* **97**, 104920 (2005).

[59] W. Lu, L. C. Feldman, Y. Song, S. Dhar, W. E. Collins, W. C. Mitchel, and J. R. Williams, *Applied Physics Letters* **85**, 3495 (2004).

[60] T. Iida, Y. Tomioka, K. Yoshimoto, M. Midorikawa, H. Tukada, and M. Orihara, *Japanese Journal of Applied Physics, Part 1* **41**, 800 (2002).

[61] J. L. Cantin and H. J. von Bardeleben, *Materials Science Forum* **527**, 1015 (2006).

[62] S. Dhar, L. C. Feldman, S. Wang, T. Isaacs-Smith, and J. R. Williams, *Journal of Applied Physics* **98**, 014902 (2005).

[63] S. Dimitrijev and P. Jamet, *Microelectronics Reliability* **43**, 225 (2003).

[64] S. Dimitrijev, H. B. Harrison, P. Tanner, K. Y. Cheong, and J. Han, *Silicon Carbide: Recent Major Advances*, pp. 373–386, Springer, 2004.

[65] S. Wang, M. Di Ventra, S. G. Kim, and S. T. Pantelides, *Physical Review Letters* **86**, 5946 (2001).

[66] S. T. Pantelides, S. Wang, A. Franceschetti, R. Buczko, M. Di Ventra, S. N. Raashkeev, L. Tsetseris, M. H. Evans, I. G. Batyrev, L. C. Feldman, et al., *Materials Science Forum* **527**, 935 (2006).

[67] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, *Physical Review B* **72**, 115323 (2005).

[68] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, *Physical Review B* **71**, 235321 (2005).

[69] P. Deák, T. Hornos, C. Thill, J. M. Knaup, A. Gali, and T. Frauenheim, *Materials Science Forum* **556-557**, 541 (2007).

[70] P. Deak, J. M. Knaup, T. Hornos, C. Thill, A. Gali, and T. Frauenheim, *Journal of Physisics D: Applied Physics* **40**, 6242 (2007).

[71] T. Onhuma, A. Miyashita, M. Iwasawa, M. Yoshikawa, and H. Tsuchida, Dynamical simulation of SiO2/4H-SiC interface on C-face oxidation process: from first principles, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[72] E. G. S. von Kamienski, F. Portheine, J. Stein, A. Golz, and H. Kurz, *Journal of Applied Physics* **79**, 2529 (1996).

[73] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. D. Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, *Applied Physics Letters* **76**, 1713 (2000).

[74] S. Dhar, S. R. Wang, A. C. Ahyi, T. Isaacs-Smith, S. T. Pantelides, J. R. Williams, and L. C. Feldman, *Materials Science Forum* **527**, 949 (2006).

[75] H. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman, *Applied Physics Letters* **70**, 2028 (1997).

[76] K. McDonald, M. B. Huang, R. A. Weller, L. C. Feldman, J. R. Williams, F. C. Stedile, I. J. R. Baumvol, and C. Radtke, *Applied Physics Letters* **76**, 568 (2000).

[77] K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2719 (2003).

[78] H. Yano, Y. Furumoto, T. Niwa, T. Hatayama, Y. Uraoka, and T. Fuyuki, *Materials Science Forum* **457**, 1333 (2004).

[79] K. Chatty, V. Khemka, T. P. Chow, and R. J. Gutmann, *Journal of Electronic Materials* **28**, 161 (1999).

[80] K. McDonald, *Ph.D. Thesis*, Vanderbilt University, 2001.

[81] K. McDonald, L. C. Feldman, R. A. Weller, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2257 (2003).

[82] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, T. Suzuki, and K. Fukuda, *IEEE Electron Device Letters* **23**, 13 (2002).

[83] E. Okuno, T. Endo, T. Sakakibara, and S. Onda, a-face channel MOSFET of low ON resistance, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

[84] E. Ö. Sveinbjörnsson, G. Gudjonsson, F. Allerstam, H. Ö. Ólafsson, P.-Å. Nilsson, H. Zirath, T. Rödle, and R. Jos, *Materials Science Forum* **527**, 961 (2006).

[85] F. Allerstam, G. Gudjónsson, H. Ö. Ólafsson, E. Ö. Sveinbjörnsson, T. Rödle, and R. Jos, *Semiconductor Science and Technology* **22**, 307 (2007).

[86] M. K. Das, B. A. Hull, S. Krishnaswami, F. Husna, S. Haney, A. Lelis, C. J. Scozzie, and J. D. Scofield, *Materials Science Forum* **527-529**, 967 (2006).

[87] C. Y. Lu, J. A. Cooper Jr., T. Tsuji, G. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, *IEEE Transactions on Electron Devices* **50**, 1582 (2003).

# CHAPTER II

# MOS PHYSICS

## Overview

In Chapter I, it was shown how the quality of the oxide/semiconductor interface affects the properties of an oxide-based device (e.g. through the channel mobility). Also, it was mentioned that the stability of the device upon charge buildup in the gate oxide is a key parameter defining long-term reliability. In this Thesis, both the properties of the interface and the reliability of the oxide are studied using metal-oxide-semiconductor (MOS) capacitors. They are two-terminal devices containing the active section of MOS field-effect transistors (i.e. the gate metal and dielectric, the oxide/semiconductor interface, and the channel region). The trapping properties of thermally grown oxides are characterized by using accelerated carrier injection techniques coupled with capacitance-voltage (CV) measurements. A method also used to study the density of electrically active defects at the oxide/semiconductor interface.

The aim of Chapter II is to introduce the properties of MOS structures and the characterization techniques relevant to this work. The chapter is organized as follows. In Section 2.1, low field and high field conduction are described together with electrical breakdown. Section 2.2 discusses transport and trapping mechanisms of charges in amorphous gate dielectrics; in particular, properties of $SiO_2$ and of its interface with semiconductors in the presence of excess carriers are highlighted. A brief review of different charge injection mechanisms is made in Section 2.3; some corresponds to the origin of leakage currents through gate dielectrics and some can be used as accelerated techniques to study oxide charge buildup and interface state generation. Finally, in Section 2.4, it is explained how CV measurements can probe both the density of oxide trapped charge and of interface states.

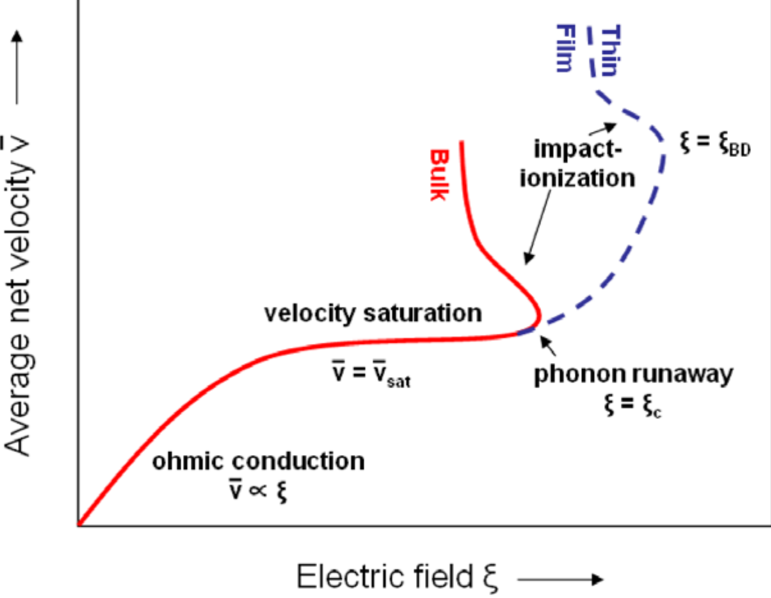



**Figure 2.1:** Different regimes of drift conduction. $\xi_c$ is the breakdown field in the bulk and $\xi_{bd}$ is the thickness dependent breakdown field in thin films or junctions.

### 2.1 Drift Conduction and Breakdown

In the absence of an electric field, a free carrier possesses a thermal energy, equal to 3/2 $k_b T$ which induces a random motion ($T$ is the temperature and $k_b$ is Boltzmann's constant). Elastic collisions of various nature, at time intervals $\tau$, make the average net velocity of the carrier $\overline{v}$ null in a bound system.

If the energy band to which the carrier belongs is only partially occupied, the application of an electric field $\xi$ leads to the displacement of the Fermi sphere,[1] meaning that the carrier can acquire an average net momentum $\overline{p}$ in the direction of the field and $\overline{v}$ becomes

$$\overline{v} = \mu\xi \tag{2.1}$$

the proportionality factor is the carrier mobility $\mu = q\tau/m^*$, with the effective mass $m^*$ describing carrier displacement in a given periodic potential. The current density $J$ (in A/cm$^2$) resulting from the drift of carriers, whose density is $N_{eh}$ (in cm$^{-3}$), is then given

by

$$J = qN_{eh}\,\overline{v} = qN_{eh}\,\mu\xi \qquad (2.2)$$

There are different regimes of drift conduction,[2,3,4,5,6] as illustrated in Figure 2.1 where the net velocity is plotted as a function of the electric field.

At low fields, the random thermal motion of the carrier is only slightly perturbed as its net velocity is smaller than its thermal velocity. This regime corresponds to $1/2\,m^*\,\overline{v}^{\,2} \ll 3/2\,k_bT$. The carrier then interacts elastically with phonons, exchanging momentum. In that regime, the mean time between collisions $\tau$ is not field dependent. From Eq.(2.1), this implies a linear dependence between the net speed of the carrier and the electric field. It corresponds to ohmic conduction.

At higher fields, so that $1/2m^*\,\overline{v}^{\,2} \simeq 3/2k_bT$, the carrier net velocity approaches its thermal velocity. It then becomes "hot" and is thermalized by means of inelastic phonon scattering. These interactions prevents the energy of the carrier from exceeding that of the lattice. In this regime, mobility is limited by phonons as the corresponding mean scattering time $\tau_{ph}$ becomes inversely proportional to $\xi$. This leads to a saturation of the velocity at

$$\overline{v}_{sat} \simeq \sqrt{\frac{2\hbar\omega_p}{m^*}} \qquad (2.3)$$

where $\omega_p$ is the angular frequency of the thermalizing phonon mode. As the carrier provides energy to the lattice, Joule heating takes place and thermal breakdown is susceptible to occur.

Ultimately the electric field becomes high enough, $\xi = \xi_c$, so that the rate at which the carrier gains energy

$$r_g = \frac{\tau q^2 \xi^2}{2m^*} \qquad (2.4)$$

becomes faster than the rate at which it can release it to the lattice. Therefore, the speed of the carrier keeps increasing. This threshold is referred to as phonon runaway.

In dielectrics and semiconductor another process can then occur when the kinetic energy of the carriers approaches the value of the band-gap: impact-ionization. Taking the example of an electron moving in the conduction band, it can reduce its energy by inducing an electron-hole pair. This leads to the multiplication of free carriers and the current increases. The ionization rate $\alpha$ is defined as the number of electron-hole pairs induced by a carrier per unit distance. This rate depends on the electric field and is negligible below the critical field $\xi_c$ required for phonon runaway. Assuming that $\alpha$ is similar for both holes and electrons, the multiplication factor $M$ can be approximated by[7,8]

$$M = \frac{1}{1 - \int_0^{x_0} \alpha dx} \tag{2.5}$$

where $x_0$ is the thickness of the region in which the electric field is present. Avalanche breakdown takes place when the integral approaches one, corresponding to $\xi = \xi_{BD}$. In the thick film limit, this can happen as soon as $\alpha$ is non-negligible and $\xi_{BD} = \xi_c$. So $\xi_c$ is the intrinsic breakdown field of a material. In thin films or junctions, the field $\xi \geq \xi_c$ should be large enough so that a carrier can gather enough energy within the distance $x_0$ to induce substantial impact-ionization. The breakdown field $\xi_{BD}$ then becomes thickness dependent. In $SiO_2$, Arnold *et al.* have shown that the breakdown field exceeds the intrinsic field ($\simeq 7$ to 10 MV/cm) for thicknesses less than 30 nm.

During normal operation of an oxide-based device, even small voltages applied to the gate can induce leakage currents by mean of injection mechanisms described later in this chapter (Section 2.3). The excess carriers can then become trapped in the oxide. This eventually leads to high local fields that can induce breakdown and device failure. The process is then described in terms of charge to breakdown. This critical trapped charge density is a function of the gate bias.

## 2.2 Charge Transport and Trapping in the Oxide

Because of the large $SiO_2$ band-gap, drift currents in the gate oxide of a device can only be achieved by excess carriers either injected from the electrodes or generated in the dielectric by high energy particles. As the thermal oxide is amorphous, transport properties of these carriers are peculiar. It shall be shown that their transport is indeed trap-mediated. Bulk trapping in $SiO_2$ and interface state generation by excess carriers are then discussed.

### 2.2.1 Band and hopping conduction in amorphous dielectrics

In both metals and semiconductors, conduction is achieved by delocalized carriers whose energies fall within a continuous energy band induced by the periodicity of the crystal lattice. If the material is a pure and ideal crystal, the current is only limited at low fields by elastic phonon scattering, when assuming large carrier lifetimes and low carrier densities. Accordingly, the mobility $\mu$ depends explicitly on the phonon distribution, on the temperature (impacting phonons and carrier thermal velocities), and on the effective mass $m^*$.[2]

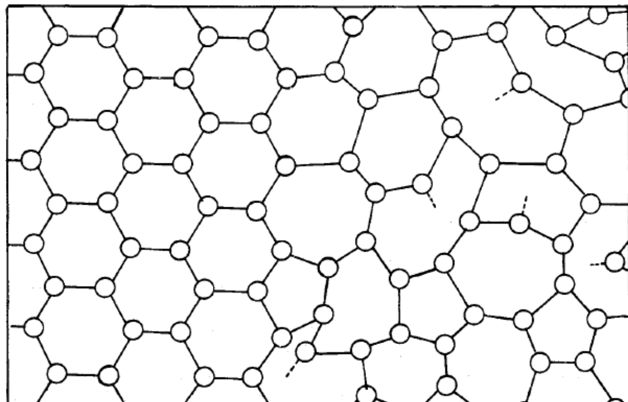


**Figure 2.2:** Ordered (left) and disordered (right) regions of a lattice. Local coordination is largely retained throughout, with the disorder appearing as a consequence of small distortions in individual bond lengths and angles. Unsatisfied "dangling" bonds occur in the case of a small fraction of sites in the disordered lattice.[9]

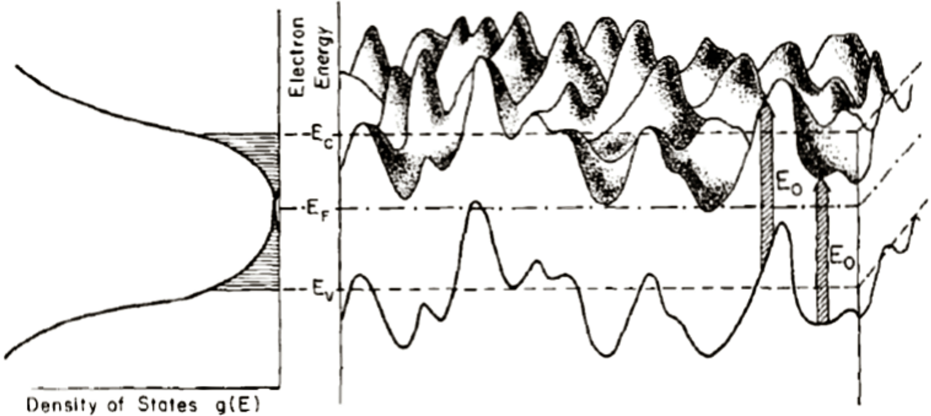



**Figure 2.3:** "Alpine" model of the influence of disorder upon the band structure of a dielectric. The dotted lines indicate the effective band edges and Fermi level.[11]

In the case of amorphous dielectrics, as there is no long range order, Bloch's theorem does not apply and the notions of bands and band-gap seem elusive. However, they can possess properties similar to semiconductors such as an optical absorption threshold, hinting the existence of a forbidden energy gap.[10] This is because, in spite of being amorphous, their short-range atomic configurations around a particular site is fairly well defined and can be similar to that of the corresponding crystalline phase. Long-range ordering of the lattice is destroyed by slight variations in bond lengths and bond angles, as illustrated in Figure 2.2. These variations can induce local defects such as dangling bonds and vacancies. Because of the difference in their local surroundings, similar defects are not expected to induce states of identical energies.

The local order in an amorphous dielectric can induce energy bands and a gap that is reasonably well defined at any particular point, indeed yielding a fairly precise onset for optical absorption. The variations in the lattice lead to the modulation of the local atomic potentials and of the relative position the band edges across the solid. The so-called "Alpine" model, Figure 2.3, gives a visual understanding of these properties.

One of the consequences of having bands that are not aligned throughout a solid is the presence of localized band-tail states in the bulk.[9] To that, one can add the discrete

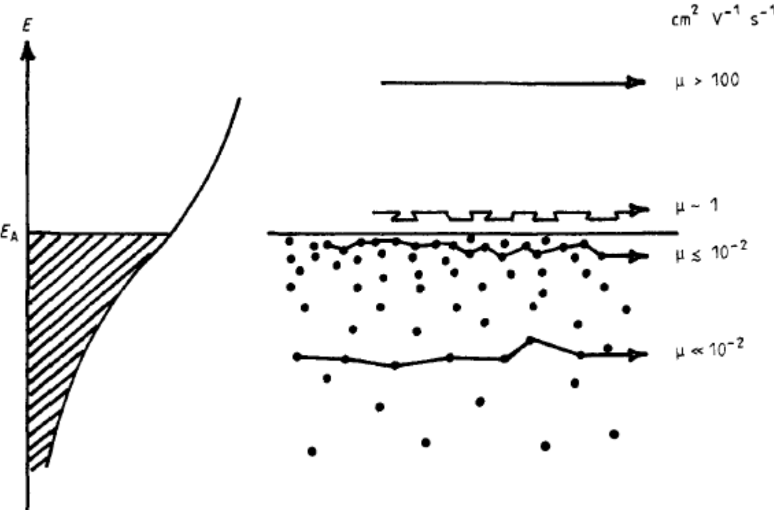



**Figure 2.4:** Expected variation of carrier mobility with energy, in the case of a disordered semiconductor.[9]

levels associated with the randomly distributed defects. Because some of these states are located below the effective conduction band edge and above the effective valence band edge, they can trap electron and holes respectively. In fact, since the density of traps can be as high as the density of atoms, they can be located within a few Ångströms of each other enabling direct tunneling between localized levels. In the presence of an electric field, excess carriers can then proceed from one electrode to the other by a trap-mediated mechanism called hopping conduction, as illustrated in Figure 2.4 in the case of electrons. Unlike the mobility associated with band conduction, the mobility of the hopping process $\mu_h$ depends on the average distance between traps $\overline{R}$ and on their energy levels $q\phi_t$ relative to the band edge.[2]

$$\mu_h \propto e^{-2\overline{R}/R_0} e^{-q\phi_t/k_b T} \tag{2.6}$$

where $R_0$ is the equivalent of the Bohr radius for localized carriers and $T$ is the temperature. The exponential dependence of $\mu_h$ on $\overline{R}$ and $\phi_t$ originates from the tunneling and emission probabilities from the traps. From Eq.(2.6), it can then be understood that mobilities associated with a trap-assisted transport will be smaller than in the case of band conduction by delocalized carriers. In particular, theoretical estimations indicate that band and hopping

mobilities are always respectively larger and smaller than 1 $cm^2V^{-1}s^{-1}$. The dependence on temperature of these mobilities are also different although they both depend on phonon interactions.[9,2]

Interestingly, trap-mediated conduction leads to the anomalous dispersion of carriers observed experimentally in amorphous dielectrics.[9,12] Indeed, regardless of the transport mechanism, the spread of a discrete packet of carriers $\Delta l$, induced by random motion, is expected to be proportional to

$$\Delta l \propto (Dt)^{1/2} \tag{2.7}$$

where $t$ is the time elapsed and $D$ is the diffusion constant related to the mobility by the Einstein relation

$$D = \frac{k_b T \mu}{q} \tag{2.8}$$

However, in amorphous dielectrics, the exponent in Eq.(2.7) can differ from 1/2. With the use of a random walk model, this has been related to the wide distribution of tunneling times between traps as carriers spend a different time in different locations.[13] The deviation from 1/2 of the exponent extracted from measurements is therefore an indication of the uniformity of the trap distribution in space and energy.

### 2.2.2 Transport in $SiO_2$

It is challenging to extract intrinsic transport properties in amorphous dielectrics because of the large densities of defects. Indeed these defects can trap carriers, reducing lifetime and mobility by Coulomb scattering, and can ultimately mediate conduction as explained earlier.

The evolution of the photo-current induced by a short X-ray pulse has been used by Hughes to measure the intrinsic mobilities of both electrons[14,15] and holes[12,16] in $SiO_2$. The observed lifetimes $\tau_{lt}$ correspond to the mean time after which carriers become trapped, yielding extrinsic defect-mediated conduction. Note that intrinsic conduction can itself

be trap-mediated because of the existence of localized levels in a defect-free amorphous dielectric.

The low field intrinsic mobility of electrons in fused quartz was found to be 20±3 $cm^2V^{-1}s^{-1}$ at 300 K. The temperature dependence and the value of the intrinsic mobility indicate that electron transport is initially achieved by band conduction as it depends on phonon scattering only. The measured electron lifetime varied from 10 to 14 nsec. Actually, in the case of oxides less than 100 nm, biased at fields of the order of 1 MV/cm, electrons are swept out of the dielectric within a few tens of picoseconds. Since this is orders of magnitude smaller than the lifetime, it implies that for such conditions intrinsic band conduction is the only transport mechanism for electrons, allowing their fast transit through $SiO_2$ thin films.

In contrast, it can take several milliseconds for the holes to be collected at the negatively biased electrode. This is because even the intrinsic hole transport is trap-mediated, and therefore has a low mobility estimated at 300 K to be between $2\times10^{-5}$ $cm^2V^{-1}s^{-1}$ and $4\times10^{-9}$ $cm^2V^{-1}s^{-1}$ in thin $SiO_2$ films thermally grown on Si. The large difference between these values can be related to the degrees of amorphicity which is expected to be strongly dependent on materials synthesis. Unlike the electron mobility, the intrinsic hole mobility is found to increase with temperature, the dependence indicates a phonon-assisted transport which is characteristic of hopping conduction.[2] Hughes proposed that at short times a hole hops as a small polaron from one oxygen non-bonding orbital (lone-pair state) to one of the nearest-neighbor orbital. At times greater than $\tau_{lt} \simeq 70\, nsec$, the excess holes are eventually trapped at structural defects and the transport continues as tunneling from one defect to another. The decay of the photo-current indicates that, in fused quartz, these defects have a density of approximately $10^{19}$ $cm^{-3}$, which implies an average distance of about 20 Å. This could correspond to oxygen vacancies (Si-Si bonds), a bulk oxide defect identified as an hole trap by spin resonance (ESR) measurements.[17] The long-term transport that is defect-mediated has been shown to give rise to an anomalous dispersive behavior and to

yield a large variation in the transit times of holes across amorphous $SiO_2$.

In summary, transport mechanisms of electrons and holes in amorphous $SiO_2$ are very different. Electron transport is achieved exclusively by band conduction in thin films, allowing for short transit times. Hole transport is achieved by hopping conduction between intrinsic localized levels or between defect states. As the velocity of holes is orders of magnitude slower than electrons, they spend much more time in the oxide. They are therefore more likely to interact with the lattice and to generate "fixed" charge and/or interface states as described next.

### 2.2.3 Trap charging kinetics

Information about trap densities and charging kinetics in a gate dielectric can be obtained in a MOS structure from measuring the evolution of the effective trapped charge $N_{eff}$ (in $cm^{-2}$), deduced from capacitance-voltage (CV) measurements (see Section 2.4), in the presence of an excess current density $J$ (in $A/cm^2$), induced by the accelerated injection techniques discussed in Section 2.3.

To first order, the trapping rate is proportional to the amount of available sites for charge capture,[18]

$$\frac{dN_{eff}}{dt} = \frac{N^* - N_{eff}}{\tau_c} \tag{2.9}$$

where $N^*$ is the total areal density of traps (in $cm^{-2}$) and $\tau_c$ is a characteristic time (in sec) defined as

$$\tau_c = (\overline{v}\sigma n_e)^{-1} \tag{2.10}$$

which is inversely proportional to the average velocity of carriers $\overline{v}$ (in cm/sec), to the capture cross section $\sigma$ (in $cm^2$), and to the carrier density $n_e$ (in $cm^{-3}$) present in the oxide. If it is assumed that $\overline{v}$ is approximately equal to the drift velocity

$$\tau_c = q(\sigma J)^{-1} \tag{2.11}$$

and the solution of Eq.(2.9) can be written as

$$N_{eff} = N^*(1 - e^{-t/\tau_c}) = N^*(1 - e^{-\sigma\rho}) \quad (2.12)$$

where $\rho$ is the total areal density of injected charge (in $cm^{-2}$).

In practice, the determination of capture cross-sections and trap densities can be complicated by the presence of sites of different natures and by field- or photo-induced detrapping. In the previous derivation, $N_{eff}$ constitutes an apparent fixed charge but it can also include a contribution from interface states generated upon injection. For $SiO_2$ on silicon, the amount of oxide trapped charge and of generated interface states can be easily separated. However, in the case of SiC, this can be challenging because of the large times required for charge emission from deep interface states, as discussed in Section 2.4.4.

### 2.2.4 $SiO_2$ bulk trapping and interface state generation

The dominant bulk electron trap in $SiO_2$ has been shown to be water-related as its density scales with the intentional, or residual, vapor pressure present during growth of the gate oxide.[18,19] The water-related traps are originally neutral and become negatively charged upon electron capture. The cross section extracted from trapping kinetics is estimated to be of the order of $1.5\times10^{-17}$cm$^2$. Once captured, the negative charge cannot be removed by photo-excitation which indicates that the trapping is induced by an electrochemical reaction that locally modifies the structure of the oxide. Indeed, it has been shown that electron trapping is accompanied by the desorption of neutral hydrogen atoms from $SiO_2$. The process is understood as followed. First, water can lead to the formation of hydroxyl groups at Si-O-Si bridges

$$\equiv\text{Si–O–Si}\equiv + \text{H}_2\text{O} \rightleftharpoons 2 \equiv\text{Si–OH} \quad (2.13)$$

Subsequently, an electron can be captured at an hydroxyl site, inducing a fixed charge and the release of neutral hydrogen

$$\equiv\text{Si–OH} + e^- \rightleftharpoons \equiv\text{Si–O}^- + \text{H} \tag{2.14}$$

Because neutral atomic hydrogen is not expected to be stable in the oxide,[20] two hydrogen atoms probably bind and leave as a $H_2$ molecule. After negative charge buildup, annealing in either vacuum or dry $H_2$ at 200 °C ($H_2$ does not chemically react with $SiO_2$ at temperatures below 350 °C) does not produce any detectable change in the negative charge density. But annealing at 200 °C in a wet ambient results in the complete discharge of the oxide. Indeed, neutral hydroxyl groups are then (re-)formed at each negatively charged sites.

In the case of holes, although their transport is mediated by traps throughout the oxide bulk, excess positive charge appears to be stable only close to the $SiO_2$ interfaces with the metal and with the semiconductor.[18] According to ESR measurements, positive charge trapped in the oxide resides on three-fold coordinated silicon atoms $O_3\equiv Si^+$, which correspond to E' centers.[17] Interestingly, the hole traps can be neutralized by subsequent electron injection, indicating that the hole trapping process is reversible and does not involve external species such as water. However, the electron annealing appears to be only a compensation effect rather than true annealing because the local positive charge is neutralized but only partially removed. This led to a model introduced by Lelis *et al.*[21] which is illustrated in Figure 2.5. They propose that a hole can be trapped by a strained Si-Si bond in the oxide (A), inducing relaxation of the defect, a positively charged trivalent silicon atom and a neutral trivalent silicon atom with an unpaired electron (B). An external electron can then complete the valence shell of the latter and induced a compensating negative charge localized on the atom (C). From there, the extra electron can either be re-emitted from the defect, leaving it positively charged, or lead to true annealing by bond reformation.

If hydrogen is present at the $SiO_2$/Si interface, switching states can be generated by both electrons and holes which can break Si-H bonds and induce Si- dangling bonds ($Si_3\equiv Si\bullet$, $P_b$

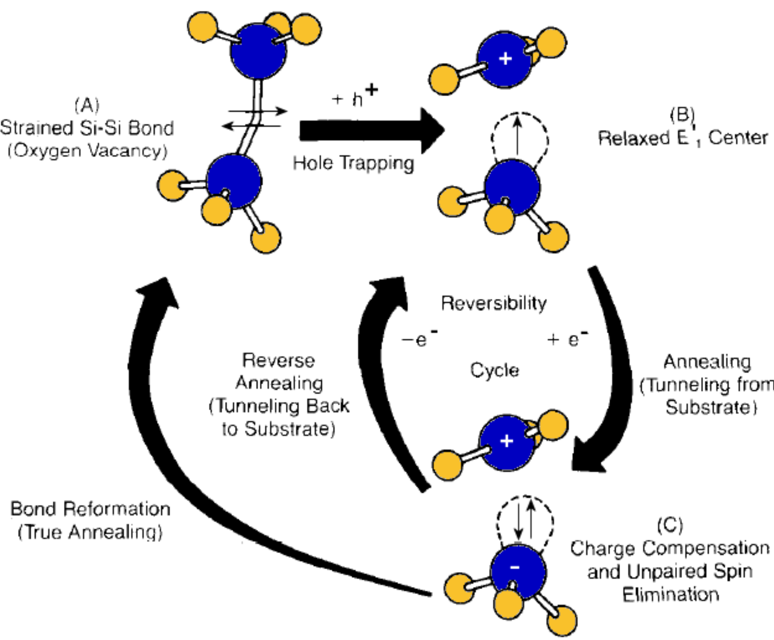



**Figure 2.5:** A model of the hole trapping [(A) to (B)] and detrapping [(C) to (A)] processes are indicated, along with intermediate compensation/reverse-annealing phenomena [(B) to (C) and (C) to (B)]. Illustration adapted from Lelis *et al.*[21]

centers) detected by CV and identified by ESR.[17] The dangling bonds can be (re-)passivated following an anneal in $H_2$ between 350 °C ($H_2$ starts reacting with $SiO_2$) and 550 °C (peak of thermal hydrogen desorption).[22] The bond-breaking mechanisms are different for electrons and holes. Only hot electrons have been found to release hydrogen from Si-H, they are thought to progressively excite vibrational stretch modes ($\Delta E \simeq 0.26$ eV) up to a critical dissociation energy ($\simeq 2.4$ eV).[23,24] On the other hand, even low energy holes can weaken the bond by trapping at a Si-H site. Interestingly, the generation of such interface states by holes tunneling at low fields from silicon within a few Ångströms of $SiO_2$ is accompanied by the buildup of a positive oxide charge at E' centers (e.g. this yields negative bias temperature instability, NBTI).[17] It has been proposed that these effects are correlated.[25,26,27] According to some models, a hole could release a positively charged hydrogen atom which can then induce a "fixed" charge in the near-interface region by interacting with a Si-O-Si bridge (forming an hydroxyl group) or with a Si-Si bond (similarly to what has been described

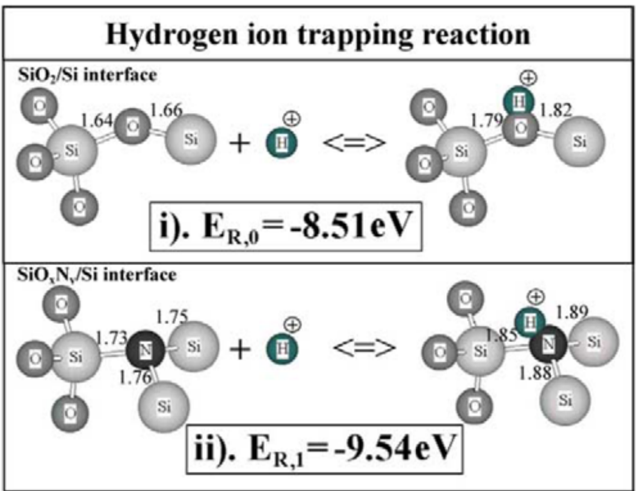



**Figure 2.6:** Energy gain associated with a proton binding at a Si-O-Si bridge (i) or at a Si-N-Si bridge (ii). Calculations suggest that the second process is favored. Bond lengths (in Å) are indicated. From a publication by Tan *et al.*[28]

above in the case of a hole). These processes correspond to the generation of $P_b$ centers

$$\mathrm{Si_3{\equiv}Si{-}H + h^+ \rightleftharpoons Si_3 {\equiv}Si\bullet + H^+} \tag{2.15}$$

followed by

$$\mathrm{H^+ + {\equiv}Si{-}O{-}Si{\equiv} \rightleftharpoons {\equiv}Si^+\ OH{-}Si{\equiv}} \tag{2.16}$$

or by

$$\mathrm{H^+ + {\equiv}Si{—}Si{\equiv} \rightleftharpoons {\equiv}Si^+\ \bullet Si{\equiv} + H} \tag{2.17}$$

In the case of nitrided $SiO_2$ on Si, the positive charge buildup in the near-interface region induced by holes is enhanced.[25,26,29,30,28,27] One possible reason is that the affinity of a positively charged hydrogen atom released from the interface with a Si-N-Si bridge is higher than its affinity with a Si-O-Si bridge [Eq.(2.16)]. This would make the entire $H^+$-release-binding process energetically favored in nitrided oxides, as illustrated in Figure 2.6. However, measurements indicate that the amount of positive charge trapped in the near-interface region exceeds the amount of induced interface states in nitrided oxides.[26] This

suggests that another trapping process, which does not involve the binding of hydrogen, can occur. Actually, this agrees with experimental and theoretical results presented in this Thesis (Chapters V and VI). In $SiO_2$ grown on SiC, it is found that the hole trap density scales with the nitrogen content at the oxide/semiconductor interface when the N concentration does not exceed the one corresponding to a $Si_3N_4$ monolayer. As the band-gap of $Si_3N_4$ falls within the one of $SiO_2$, it is expected that an intermediate $SiO_xN_y$ transition layer will induce hole traps in the oxide.[31] In particular, it is proposed that nitrogen can incorporate in the oxide forming Si-N-Si or Si-NO-Si bridges with an oxygen protrusion. First-principles calculations (Chapter V) show that in these configurations, nitrogen possesses a lone pair of electrons that can capture a hole. As recent ESR measurements reveal that the majority of the positive charge trapped in nitrided $SiO_2$ resides on Si atoms back-bonded to nitrogen atoms ($K_N$ center),[32] a likely mechanism is,

$$\equiv\text{Si–}\ddot{\text{N}}\text{O–Si}\equiv + \text{h}^+ \rightleftharpoons \equiv\text{Si}^+ \bullet\ddot{\text{N}}\text{O–Si}\equiv \tag{2.18}$$

with the charged silicon bonded to some other nitrogen atoms in the $SiO_xN_y$ transition layer. It is indeed possible that after the hole is captured by the lone-pair state of the nitrogen, the positive charge becomes localized on a Si atom, weakening the corresponding Si-N bond.

To conclude this brief overview of the effects of excess carriers in $SiO_2$, it is important to note that not everything is well understood. On one hand, it is known that bulk electron traps are related to the water content, that positive trapped charge resides in E' centers ($O_3 \equiv Si^+$), and that holes or electrons can generate states at the $SiO_2$/Si interface by inducing $P_b$ centers ($Si_3 \equiv Si\bullet$). On the other hand, the details of atomic-scale mechanisms associated with charge trapping and interface state generation are still not clear. Therefore, the processes described by Eqs. (2.13) to (2.18) should be considered only as tentative and the reader should be aware that other models can be found in the literature.

### 2.3 Injection Mechanisms

The aging of devices and their usage can affect their properties and lead to failure. The ability of a device to be stable under operation conditions is characterized by its reliability. The main factor that degrades an oxide-based device is the buildup of charges in the gate dielectric and the generation of interface states, both due to in part to excess carriers leaking through the gate. These processes lead to the reduction of the inversion channel mobility, to threshold voltage instabilities, and ultimately to the electrical breakdown of the gate oxide.

In practice, the charge buildup is very slow because the leakage current through the oxide is intentionally minimized. However, the presence of excess carriers into the dielectric is impossible to avoid, even at low fields, because of some injection mechanisms. In order to accelerate the degradation processes and study the long-term stability of an oxide-based device within hours, some of these injection mechanisms can be used; the results are then extrapolated to the actual operation conditions. There are various accelerated techniques, each requiring a relatively different electric field in the oxide. In the case of wide band-gap semiconductors, some of the methods employed in Si cannot be applied (e.g. avalanche injection) but advantage can be made of the smaller band offsets between them and the dielectric.

In this section, some of the injection mechanisms occurring at low and high oxide fields are reviewed: quantum tunneling, thermionic emission, Frenkel-Poole emission, and Fowler-Nordheim tunneling. Processes that require the interaction of high energy photons or particles are then introduced: internal photoemission and radiation-induced carriers. All mechanisms are shown to impact oxide-based devices in different ways. In particular, the three latter ones prove to be fit for accelerated injection in controlled conditions.

### 2.3.1 Quantum tunneling

Even in the absence of an electric field, there is a probability $T_t$ for a carrier of energy $E$ to be transmitted through a constant potential of energy $q\phi_{bo}$ and of length $x_t$. In the case of a MOS structure, it can be assumed that $T_t$ gives the probability for a free carrier to penetrate a distance $x_t$ into the gate oxide. The value $q\phi_{bo}$ then corresponds to the energy band offset between the oxide and the metal, or between the oxide and the semiconductor.

The quantum-mechanical transmission probability is given by[7]

$$T_t = \left[1 + \frac{(q\phi_{bo})^2 sinh^2 \kappa x_t}{4E(q\phi_{bo} - E)})\right]^{-1} \tag{2.19}$$

where $\kappa$ is the wave vector

$$\kappa = \sqrt{\frac{2m(q\phi_{bo} - E)}{\hbar^2}} \tag{2.20}$$

with $\hbar$ the Planck constant and $m$ the mass of the carrier. Since Eq.(2.19) is derived for free carriers, one could assume that in a bound system it applies using $m = m^*$, the effective mass, and $E = 3/2\,kT$, the average kinetic energy of free carriers.

To compare the electron tunneling probabilities into $SiO_2$ from the conduction band edges of Si and SiC, values for $q\phi_{bo}$ were taken as 3.2 eV and 2.7 eV respectively. The curves are shown in Figure 2.7. It can be seen that in both cases, the wave function of the carriers extends into the oxide ($T_t$[5 Å]$\simeq$ 1%). In ultra-thin gate dielectrics, direct tunneling can therefore be an issue, yielding a base intrinsic leakage current. Here, the analysis is restricted to oxides tens of nanometers thick and direct tunneling has another impact.

If traps are present in the oxide, electron tunneling from the electrodes can lead to the capture of carriers and, therefore, to charge buildup. At equilibrium, the rate at which electrons tunnel in and out of these traps is the same and the profile of occupied traps will be similar to $Q_0 T_t[x]$ with $x$ being the distance within the oxide and $Q_0$ the density of traps (in $cm^{-3}$). If a small positive bias is applied on the gate, the rate at which electrons tunnel in from the semiconductor will dominate. A displacement current $J_{in}$ will then be

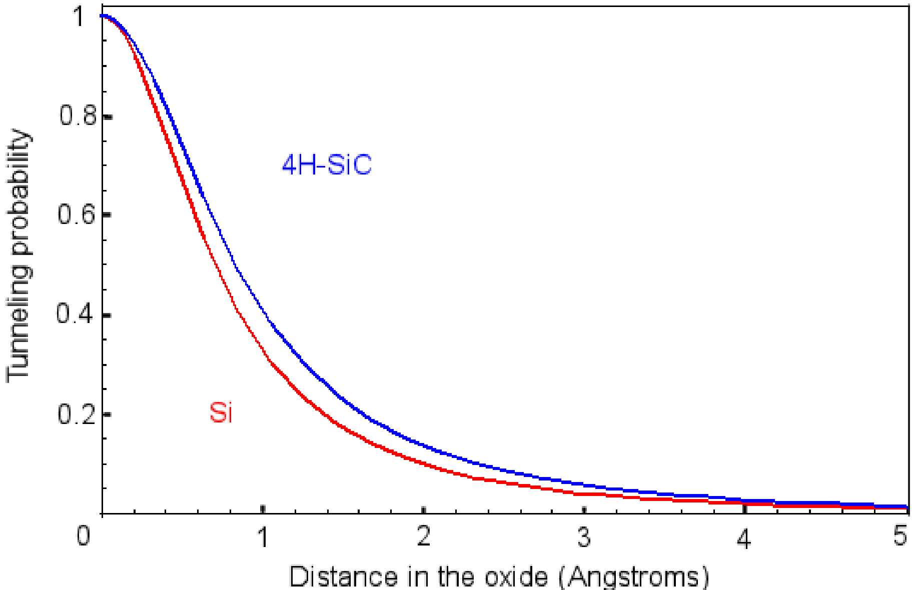



**Figure 2.7:** Tunneling probabilities from the conduction band of Si and 4H-SiC as a function of the depth in $SiO_2$ calculated from Eq.(2.19) using $m^* = 0.5\,m$.

observed and the profile of occupied traps $Q_t[x,t]$ will be a function of time and will extend progressively into the oxide. The rate at which traps are getting filled at any position is given by

$$\left.\frac{dQ_t[x,t]}{dt}\right|_{in} = \frac{T_t[x](Q_0 - Q_t)}{\tau_{in}} \tag{2.21}$$

where $\tau_{in}$ is a characteristic rate. Using the boundary condition $Q_t[x, t = 0] = 0$, the solution of Eq.(2.21) is

$$Q_t[x,t]|_{in} = Q_0\,(1 - e^{-t\,T_t/\tau_{in}}) \tag{2.22}$$

The position in the oxide at which the rate is maximum is $x_m$, the tunneling front (see Figure 2.8)

$$\left.\frac{d^2Q_t[x,t]}{dt\,dx}\right|_{in\,@\,x=x_{m,in}} = 0 \tag{2.23}$$

Noting that for $\kappa x \gg 1$, the tunneling probability has the form $T_t = a\exp(-bx)$, one finds[33]

$$x_{m,in}[t \geq t^*_{in}] = \frac{1}{b}\,ln\left(\frac{at}{\tau_{in}}\right) \tag{2.24}$$

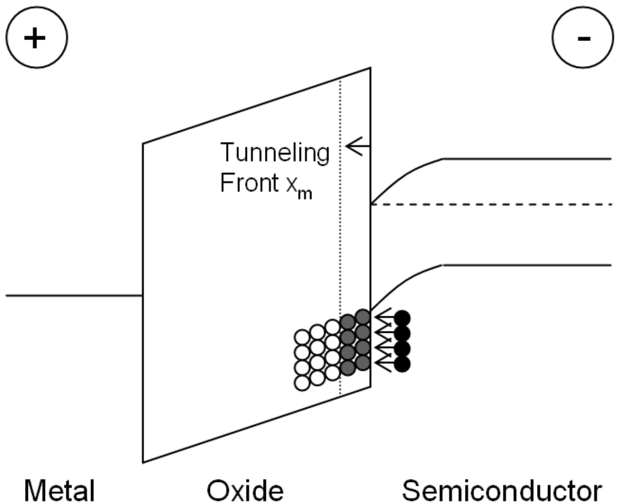



**Figure 2.8:** Band diagram of a MOS structure showing the evolution of an electron tunneling front in the oxide induced by a positive gate bias.

for times $t \geq t^*_{in}$ such that the logarithmic argument is $\geq 1$. If the distance of the tunneling front is much smaller than the oxide thickness, the effective trapped charge (in $\mathrm{cm}^{-2}$) can be approximated by

$$N_{eff,in}[t \geq t^*_{in}] = x_{m,in}\,\mathrm{Q}_0 + N^*_{eff,in} = \frac{\mathrm{Q}_0}{b}\, ln\left(\frac{at}{\tau_{in}}\right) + N^*_{eff,in} \tag{2.25}$$

where $N^*_{eff,in}$ is the effective trapped charge at $t = t^*_{in}$. The displacement current density induced by electrons tunneling in is then

$$J_{in}[t \geq t^*_{in}] = q\mathrm{Q}_0\,\frac{dx_{m,in}}{dt} = \frac{q\mathrm{Q}_0}{bt} \tag{2.26}$$

A similar derivation can be made to predict the evolution of the tunneling front when the bias is reversed and the electrons tunnel out of the traps back into the semiconductor. All the expressions have the same form but constants (e.g. $\tau_{out}$) can have different values.

The impact of the gate bias on the near-interface trapped charge is shown in Figure 2.9. The measurements were made on a 4H-SiC MOS structure. First, a positive bias was applied on the gate for 60 minutes, the field in $SiO_2$ was approximately 1.5 MV/cm. Electrons could

then tunnel in from the semiconductor into near-interface oxide traps. The amplitude of the effective trapped charge is proportional to $ln(t)$ as predicted by Eq.(2.25). Subsequently, a negative bias was applied to induce a similar oxide field of opposite polarity. The electrons could then tunnel out of the traps back into the semiconductor. This process is much faster, suggesting that $\tau_{out} \ll \tau_{in}$. Note that within the time frame of the measurements, at most $2{\times}10^{12}$ charges per $cm^2$ can be exchanged between the semiconductor and the oxide. This data demonstrates that even at low fields, when there is no leakage current through the oxide, trapping can occur.

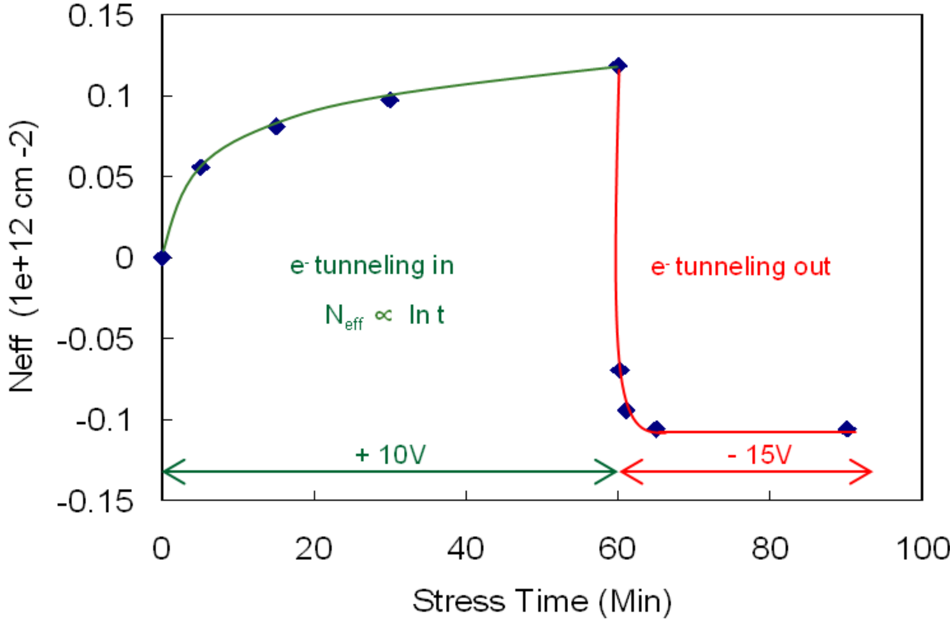



**Figure 2.9:** Measured effective trapped charge in $SiO_2$ as a function of time. The oxide was thermally grown on 4H-SiC (no post-oxidation anneal). A positive bias on the metal gate leads to electrons tunneling in near-interface oxide traps and a subsequent negative bias leads to electrons tunneling out. The field in the oxide was approximately 1.5 MV/cm in both cases.

### 2.3.2 Thermionic emission

Thermionic emission is a process that induces a current through the oxide even in the absence of an electric field ($\xi_{ox} = 0$). It constitutes the base intrinsic leakage current. The process originates from the energy distribution of carriers in the metal and the semiconductor. Temperature indeed induces a spread in the level occupancy and a fraction of electrons can have an energy well above the Fermi level or the conduction band edge. For example, all the electrons in the conduction band of a semiconductor that possess and energy higher than $E_c + q\phi_{bo}$, can leak into the oxide. The induced current $J_{TE}$ then depends on their velocity $v_x$ in the direction perpendicular to the gate oxide.[7]

$$J_{TE} = \int_{E_c+q\phi_{bo}}^{\infty} q v_x \, dn \tag{2.27}$$

where $n[E]$ is the density of occupied states at a given energy. This distribution is ideally obtained by integrating the product of the density of states by the Fermi-Dirac distribution function. In order to relate velocity to energy, it can be assumed that all the energy of electrons in the conduction band is kinetic so that

$$E - E_c = \frac{1}{2} m^* v^2 \tag{2.28}$$

Equation (2.27) then leads to

$$J_{TE}|_{\xi_{ox}=0} = A^* T^2 \, exp\left(-\frac{q\phi_{bo}}{k_b T}\right) \tag{2.29}$$

where $A^*$ is the effective Richardson constant for thermionic emission (in $A.cm^{-2}K^{-2}$) given by

$$A^* = \frac{4\pi q m^{**} k_b^2}{h^3} \tag{2.30}$$

where $m^{**}$ depends on the isotropy of the effective mass. For free electrons, the Richardson constant $A$ is 120 $A.cm^{-2}K^{-2}$, in n-type Si $A^* \simeq 2.1 \times A$ and in SiC $A^* \simeq 1.2 \times A$.[7,34]

If an electric field is present in the oxide, the deformation of the barrier due to the image force potential needs to be taken into account (see Section 2.3.4). The complete equation becomes

$$J_{TE} \, = \, A^{*}T^{2}\, exp\left(-q\,\frac{\phi_{bo} - \sqrt{q\xi_{ox}/4\pi\epsilon_{ox}}}{k_{b}T}\right) \tag{2.31}$$

From Eq.(2.31), the current estimated to be due to thermal emission in $SiO_2$ on Si or SiC at room temperature is found to be negligible. For materials leading to small band-offsets however (e.g. $HfO_2$ on Si), the thermal current can be of the order of pA/cm$^2$. To reach this range, 4H-SiC devices would have to be heated up to about 500 °C. So in the case of $SiO_2$ on Si or SiC, oxide leakage currents at low fields and temperatures (i.e. less than 500 °C) are likely to be dominated by an extrinsic ohmic component such as defect mediated transport (e.g. at the edge of domain boundaries in the oxide).

### 2.3.3 Frenkel-Poole emission

At high fields, an extrinsic current in the oxide can be due to the emission of carriers not from the electrodes but from localized states within the oxide. If the energy of a trap is $q\phi_t$ from the conduction band edge of the oxide, and the Coulomb potential of the localized carrier at a distance $x$ from the trap is $\phi[x > 0] = q/4\pi\epsilon_{ox}x$, there is no energy minimum outside the trap location, so that the electron cannot escape. In the presence of an electric field, the potential energy profile is modified (see Figure 2.10) and becomes[2]

$$-\, q\phi_{FP}[x > 0] \, = \, -\, q\xi_{ox}x \, - \, \frac{q^{2}}{4\pi\epsilon_{ox}x} \tag{2.32}$$

and on the right side of the trap, there is a finite distance at which the barrier height is maximum. From Eq.(2.32), this height is found to be

$$\phi^{*}_{FP} \, = \, \phi_{t} \, - \, \sqrt{\frac{q\xi_{ox}}{\pi\epsilon_{ox}}} \tag{2.33}$$

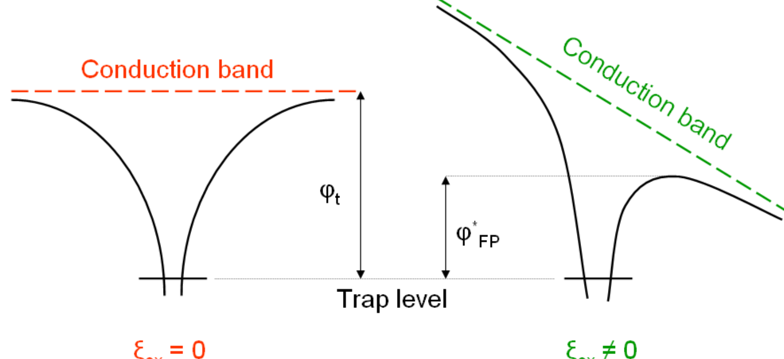



**Figure 2.10:** One-dimensional potential-energy diagram illustrating the Frenkel-Poole effect. The work required to free a trapped carrier to the oxide conduction band in the absence of a field $\xi_{ox}$ is $q\phi_t$ and is reduced to $q\phi^*_{FP}$ when a field is applied.

Accordingly, the amount of carriers available for conduction becomes proportional to the thermal emission probability from the traps and therefore to $exp(-q\phi^*_{FP}/k_bT)$ as previously derived[Eq.(2.29)]. This yields the expression for the current density

$$J_{FP} \propto \xi_{ox}\, exp\left(-q\,\frac{\phi_t - \sqrt{q\xi_{ox}/\pi\epsilon_{ox}}}{k_bT}\right) \tag{2.34}$$

The form of $J_{FP}$ is similar to the one of $J_{TE}$ given in Eq.(2.31). Indeed both processes are driven by thermal emission. However, in the case of the Frenkel-Poole mechanism, there are three main differences. First, once the carriers are available they will process by drift conduction, yielding the pre-exponential $\xi_{ox}$ factor. Second, the Coulomb interaction to which an emitted carrier is subjected is induced by a fixed charge and not an image charge, yielding a factor of 4 difference in the square root. Finally, Frenkel-Poole emission is defect-mediated and it can therefore be considered an extrinsic process. It constitutes an intermediary mechanism between full band conduction and trap-to-trap hopping. Carriers can be constantly provided by the electrodes but charge emission from trap centers to the conduction band (or valence band in the case of holes) becomes the limiting process. Currents of the form $J_{FP}$ dominate at high temperatures and at high fields. They can be isolated from other components to the total current density by identifying the linear region in a plot of $ln(J/\xi_{ox})$ versus $\sqrt{\xi_{ox}}/T$.

### 2.3.4 Fowler-Nordheim tunneling

At high enough oxide fields, carriers from the semiconductor or the metal can tunnel through a fraction of the oxide and lead to an intrinsic leakage current $J_{FN}$. As illustrated in Figure (2.11), the image potential prevents an electron of the emitting electrode from being stable in the conduction band of the oxide. However, when an electric is applied, the potential energy of the carrier is given by

$$-q\phi_{FN}[x>0] \;=\; -q\xi_{ox}x \;-\; \frac{q^2}{16\pi\epsilon_{ox}x} \tag{2.35}$$

where $q\phi_{bo}$ is the energy band offset. The potential barrier height is then reduced to

$$\phi_{FN}^{*} \;=\; \phi_{bo} \;-\; \sqrt{\frac{q\xi_{ox}}{4\pi\epsilon_{ox}}} \tag{2.36}$$

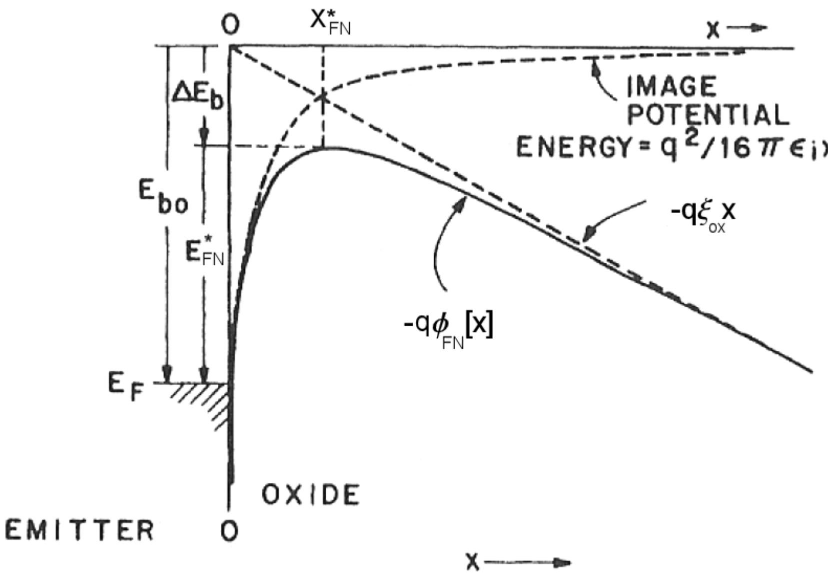



**Figure 2.11:** Energy-band diagram between the emitter surface and $SiO_2$. The zero field barrier height at $x = 0$ is $E_{bo} = q\phi_{bo}$. The barrier lowering is due to the combined effects of the electric field and of the image force.[7]

and the potential energy is maximum at

$$x^*_{FN} = \sqrt{\frac{q}{16\pi\epsilon_{ox}\xi_{ox}}} \tag{2.37}$$

As the conduction band of the oxide is bent, it crosses the energy level corresponding to the one of free carriers in the emitter. Therefore, the distance $x_t$ to tunnel in order to efficiently leak to the other electrode can be much less than the oxide thickness at high fields. This value is approximately

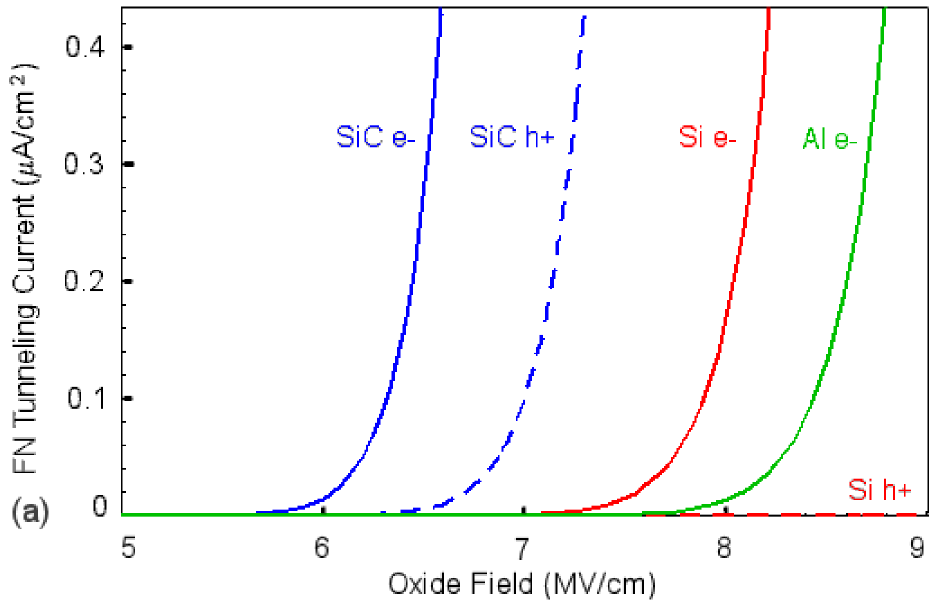
$$x_t \simeq \frac{\phi_{bo}}{\xi_{ox}} \tag{2.38}$$

Because the potential is not constant over the tunneling region, the transmission probability is different from the one given earlier [Eq.(2.19)] and the use of the WKB approximation is required to derive it.[2,35] The tunneling current density then becomes[36]

$$J_{FN} = \frac{q^3 m}{16\pi^2\hbar m^*_{ox}\phi_{bo}}\, \xi^2_{ox}\, exp\left(-\frac{4\sqrt{2qm_{ox}}\phi^{3/2}_{bo}}{3\hbar\xi_{ox}}\right) \tag{2.39}$$

where $m$ is the free electron mass and $m^*_{ox}$ is the effective mass in the oxide. From Eq. (2.39) it can be deduced that typical values of $\xi_{ox}$ required to induce currents of about 1 $\mu$A/cm$^2$ are of the order of 7 MV/cm. This is very close to the breakdown field of $SiO_2$ ($\simeq$ 10 MV/cm) and it is also enough to generate hot carriers in the oxide that could lead to the formation of electron-hole pairs.[5,6]

Fowler-Nordheim injection occurs at high fields and is not likely to be encountered in normal operating conditions, except in ultra-thin dielectrics. It can be used however as an accelerated technique to study the trapping behavior and the reliability of MOS structures. Some theoretical values of the injection current densities into $SiO_2$ are shown in Figure (2.12). Electrons can be injected from 4H-SiC at lower fields than from Si because of the smaller conduction band-offsets. In SiC, the probability to induce impact ionization during electron injection is then reduced, limiting the compensating positive charge that could occur from electron-hole pairs being generated. Interestingly, holes can be injected from the valence band of SiC and not from the one of Si at fields lower than 10 MV/cm.



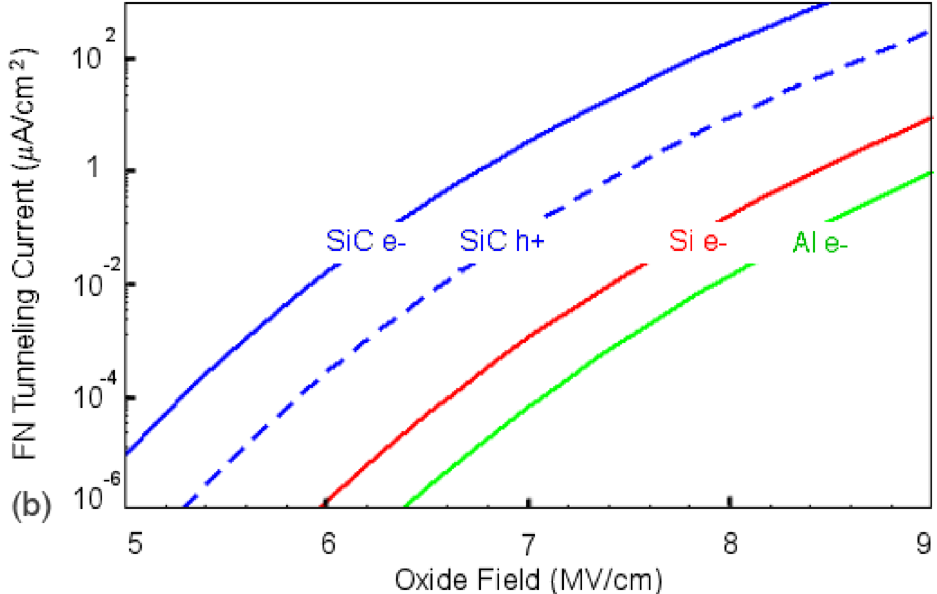




**Figure 2.12:** Injection current densities in $SiO_2$ calculated from Eq.(2.39) for holes and electrons, using $m^*_{ox} = 0.5\,m$. The emitters were chosen as the 4H-SiC conduction band (electrons) and valence band (holes), the Si conduction band (electrons) and valence band (holes), and the Al Fermi level (electrons).Linear (a) and logarithmic (b) scales.

### 2.3.5 Internal photoemission

Internal photoemission is an injection process that originates from the interactions of carriers with low energy photons. Therefore, it is not likely to occur during normal operation, unless desired, but like Fowler-Nordheim, it can be used as an accelerated method.

A light source that has energy of the order of the band offset can induce the emission of carriers from the metal or the semiconductor into the oxide. Still referring to Figure 2.11, the minimum photon energy required can be estimated from Eq.(2.36);

$$h\nu_{min} = q\phi_{bo} - q\sqrt{\frac{q\xi_{ox}}{4\pi\epsilon_{ox}}} \tag{2.40}$$

where $\nu$ is the light frequency. In practice, the minimum energy is slightly larger because of the three different mechanisms involved in photoemission: electron photo-excitation, transport to the emitter surfaces, and escape over the energy barrier. These three steps define the quantum yield $Y$ which is the number of excited electrons per photon absorbed.

Since the excited electrons have to physically go over the barrier located at a finite length $x^*_{FN}$, the photo-current is then expected to be proportional to

$$J_{IPE} \propto P\,Y\,exp\left(-\frac{x^*_{FN}}{l}\right) \tag{2.41}$$

where $P$ is the absorbed light power and $l$ is the electron scattering length ($\simeq$ 34 Å in $SiO_2$). Indeed, a complete derivation, which includes the excitation of the electron energy distribution by photons (explicit form of $Y$), leads to a current expressed as a function of the oxide field of the form[18]

$$J_{IPE} \propto P\left(h\nu - q\phi_{bo} - \sqrt{\frac{q^3\xi_{ox}}{4\pi\epsilon_{ox}}}\right)^{\varrho} exp\left(-\sqrt{\frac{q}{16\pi\epsilon_{ox}\xi_{ox}l^2}}\right) \tag{2.42}$$

where the exponent $\varrho$ is a parameter depending on the origin of the injected carriers in the band; for electrons injected from the metal or from the conduction band of Si, $\varrho = 2$.

A typical photo-current plotted as a function of negative gate bias is shown in Figure 2.13. It appears that the behavior is very different from the Fowler-Nordheim case [Eq. (2.39)], in which the dependence is exponential. From Eq. [2.40] it is clear that the minimum energy $h\nu_{min}$ of the light source required to inject a carrier is of the order of the band offset and that only a small field is needed. Therefore, this technique can selectively inject electrons in electrical conditions comparable to the ones of practical device operation. It should be noted that because of the absorption coefficient of the light, a thin metal gate is required (usually less than 30 nm) and a limited number of carriers can be injected from the semiconductor side. In particular, the hole quantum yield is orders of magnitude smaller than for electrons.

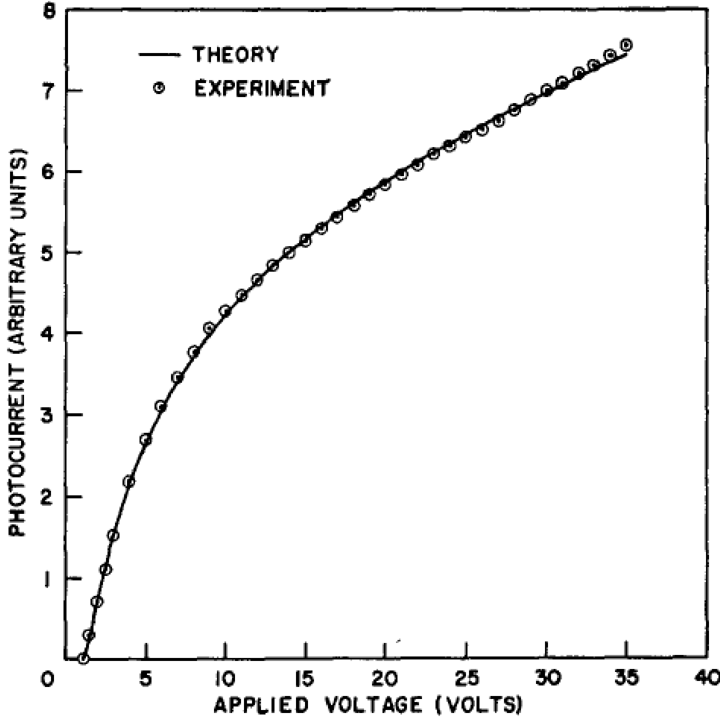



**Figure 2.13:** Photo-current in arbitrary units as a function of negative gate bias comparing the calculated and measured dependence.[18]

### 2.3.6 Radiation-induced carriers

The interactions of high energy particles and photons with electronic devices can lead to deterioration and failure.[18,37] Applications in which circuitry can be exposed to radiation include space modules, nuclear reactors, and military equipment. A famous example the Telstar communication satellite which failed in 1962 after passing through the Van Allen belts, a torus of energetic charged particles around earth.

There are two main mechanisms leading to device failure when an oxide-based device is exposed to radiation. First, high energy particles such as neutrons can collide with the nuclei of the lattice atoms and induce displacement damages. These defects can be permanent and if they are located in the active region, they will reduce carrier lifetime. Second, energetic radiation can result in the generation of electron-hole pairs throughout the structure. Excess carriers in the dielectric can then be trapped, modifying the device properties, and ultimately lead to breakdown.

As, high energy photons do not lead to displacement damage, their use in a controlled environment corresponds to an accelerated technique that can be used to study the properties of a gate dielectric in the presence of excess carriers, very much like the methods previously described.

There are three different mechanisms leading to ionization of a material by photons, they are illustrated in Figure 2.14. The one that dominates for a particular radiation source is defined by the energy of the photons. Photons with energies of a few electron-volts, corresponding to the band offsets between the gate oxide and the metal or the semiconductor, can inject carriers in the dielectric. When the photon energy exceeds the one of the oxide band-gap ($\simeq$ 9 eV for amorphous $SiO_2$), they directly generate electron-hole pairs in the oxide by mean of the photo-electric effect. A photon then interacts with an electron and promotes it to the conduction band of the material as its energy is entirely absorbed. In a Compton scattering event, which occurs at higher photon energies, only some of the energy of the incident photon is transferred to the electron, and it can produce several electron-hole

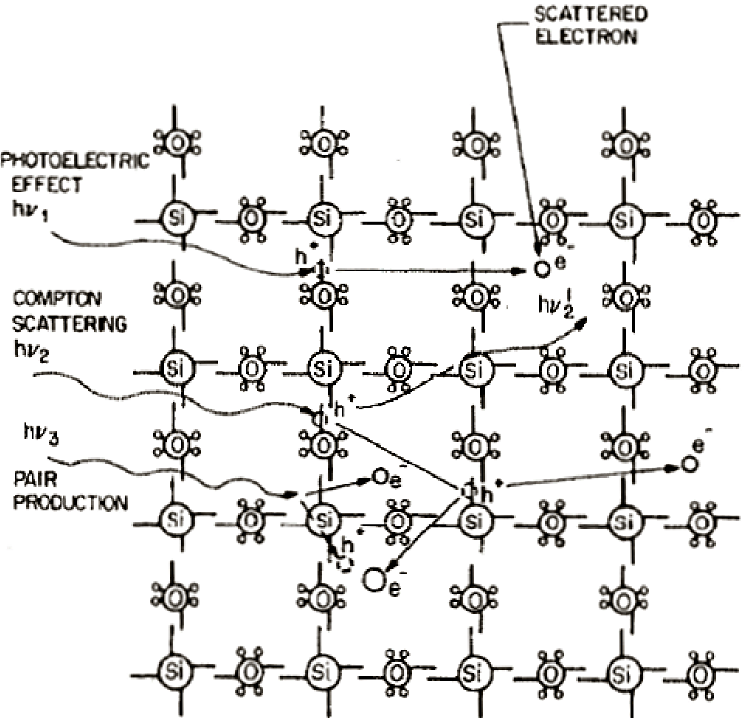



**Figure 2.14:** Schematic representation of ionization processes in silicon dioxide. After Gwyn.[18]

pairs until it is completely absorbed. When the energy of the incident photon exceeds 1.02 MeV, it can interact with the Coulomb field of the nuclei and induce an electron-positron pair, the photon is then completely annihilated.

In the case of 10 eV VUV (vacuum ultra-violet) and 10 keV X-ray photons, electron-hole pairs are the result of the photo-electric effect. However, the details of the process are very different for these two radiation sources. As the energy of VUV photons barely exceeds the one of the $SiO_2$ band-gap, they are absorbed within 10 nm of the oxide and they can only promote electrons from the top of the valence band to the bottom of the conduction band. X-rays however are energetic enough to span several microns and knock electrons out of the core shells of atoms. The subsequent transition of electrons from the outer shells to the core shells, generate additional X-rays. Since the binding energy of a core electron is of the order of 1 keV, most of the absorbed photon energy ($\geq$ 9 keV) is transferred to

the kinetic energy of the emitted secondary electron. The secondary electrons generated by X-rays can then induce electron-hole pairs themselves by progressively losing their excess energy to the lattice. So, an absorbed 10 keV photon will ultimately lead to the generation about a thousand times more electron-hole pairs than a 10 eV photon, because of secondary processes.

**Table 2.1:** Constants for interactions between 10 keV photons and electrons.[38,39,40]

| Quantity | $SiO_2$ | Si | 4H-SiC | Al | Mo | Au |
|---|---|---|---|---|---|---|
| $M_{a,\gamma}$ ($cm^2$/g) | 19.3 | 34.5 | 24.9 | 28.9 | 90.1 | 123.0 |
| $dE_{e^-}/dx$ (eV/nm) | 4 | - | - | - | - | - |
| $E_{pair}$ (eV) | 18 | 3.63 | 7.5 | x | x | x |

The details of the device structure, the X-ray photon mass attenuation coefficient ($M_{a,\gamma}$ in $cm^2$/g), the secondary electrons stopping power ($dE_{e^-}/dx$ in eV/nm), and the average energy required to induce ionization ($E_{pair}$ in eV), determine the total amount of generated electron-hole pairs within a given oxide thickness. The average energy $E_{pair}$ required by high energy particles to induce an electron-hole pair is always larger than the band-gap. This is because of momentum conservation and phonon interactions. In $SiO_2$, $E_{pair} \simeq 18$ eV. Some other constants are listed in Table 2.1. Using the mass attenuation coefficient $M_{a,\gamma}$, one finds that the penetration depth of 10 keV photons in $SiO_2$ is about 220 $\mu$m. It can be shown that in a free-standing 50 nm oxide, approximately 2 X-ray photons out of 10,000 will be absorbed; each of the induced secondary electrons will generate electron-hole pairs. In a real device, the contribution from secondary electrons coming from the gate metal and the semiconductor need to be counted. If the structure consists of a 50 nm thick Al gate, on top of the 50 nm oxide grown on Si, the total amount of induced electron-hole pairs will approximately double.

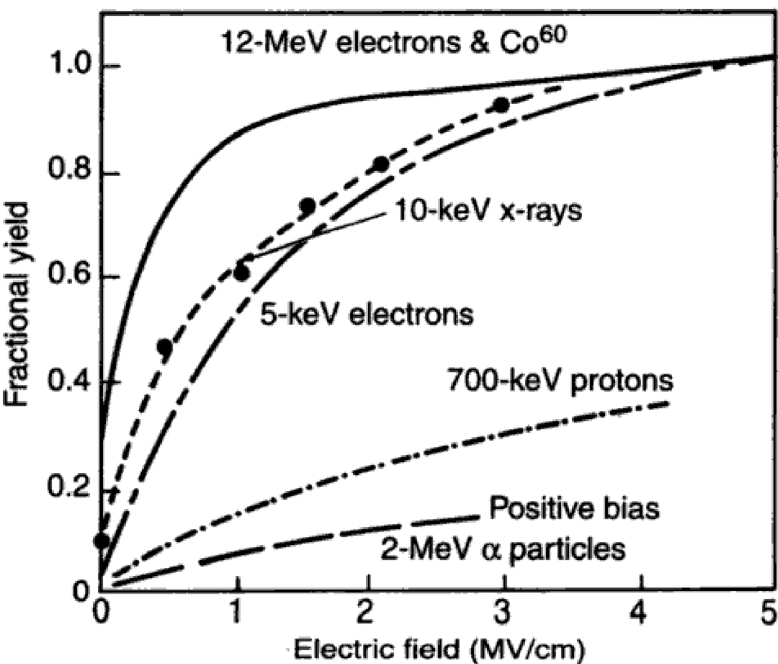



**Figure 2.15:** Fractional yields of electron-hole pairs generated in $SiO_2$ by various radiation sources.[37]

The unit used to define the energy absorbed by a material per unit mass is the rad (radiation-absorbed dose). One rad corresponds to 100 erg/g (1 erg = $10^{-7}$ joules). Note that a transistor in a earth satellite passing repeatedly through the Van Allen belts could absorb approximately 1 Mrad per year. Radiation setups are calibrated so that the parameter that defines the desired exposure time is $R$, the absorbed dose rate in $SiO_2$ [rad($SiO_2$)/s]. The generation rate of electron-hole pairs (in $cm^{-2}$ $s^{-1}$) in a free standing $SiO_2$ thin film ($< 220$ $\mu$m) is then given by

$$r_{pair} = \rho_{ox}\, x_{ox}\, \frac{R}{E_{pair}} \tag{2.43}$$

where $\rho_{ox}$ is the density of the oxide (about 2.3 g/cm$^3$) and $x_{ox}$ is the oxide thickness. Accordingly, if one chooses to deposit 1 Mrad($SiO_2$) in the structure mentioned above (Al/$SiO_2$/Si), it will induce about $1{\times}10^{14}$ pairs/cm$^2$, when accounting for the doubling of the rate due to secondary electrons from the metal and the semiconductor.

When a bias is applied on the gate during irradiation, the electric field in the oxide $\xi_{ox}$

will induce a current by separating electrons and holes, and by driving them to opposite electrodes. The fractional yield $F_y$ is the fraction of pairs that do not recombine. As shown in Figure 2.15, $F_y$ depends on the type of radiation and on the field. The current density is then

$$J_{RAD} = 2qF_y r_{pair} \tag{2.44}$$

If the Al/$SiO_2$/Si structure is biased such that $\xi_{ox}$= 1.5 MV/cm and the absorbed dose rate from 10 keV X-rays is given by R = 500 rad/sec, $r_{pair}$ [from Eq.2.43] is approximately $2.5\times10^{10}$ pairs/sec and $F_y$ (from Figure 2.15) is about 0.7. Using an extra factor of 2 because of the secondary electrons from the metal and the semiconductor, Eq.(2.44) yields $J_{RAD} \simeq 20$ nA/cm$^2$ in good agreement with experimental values.[18]

## 2.4 MOS Capacitance

Different methods can be used to study the charge at the interface and in the bulk of the oxide in a metal-oxide-semiconductor (MOS) structure.[18] This section will focus on the hi-lo capacitance-voltage (CV) technique. It requires a description of the different charges present in a MOS system and of the dependence of the interface states population on the applied voltage.

### 2.4.1 Nature of charges

There are four categories of charges present in the oxide of a MOS structure [Figure 2.16(a)]. First, there are the mobile ions which are light charged atoms introduced during processing. These can move if a bias is applied to the structure and are therefore susceptible to modify the characteristics of the device upon operation. Their presence can be minimized by surface conditioning prior to the oxide growth and by post-oxidation passivation processes.

The oxide trapped charge is the result of carrier trapping in oxide defects in the bulk of the oxide. To first order, the density of such defects can be considered constant, the

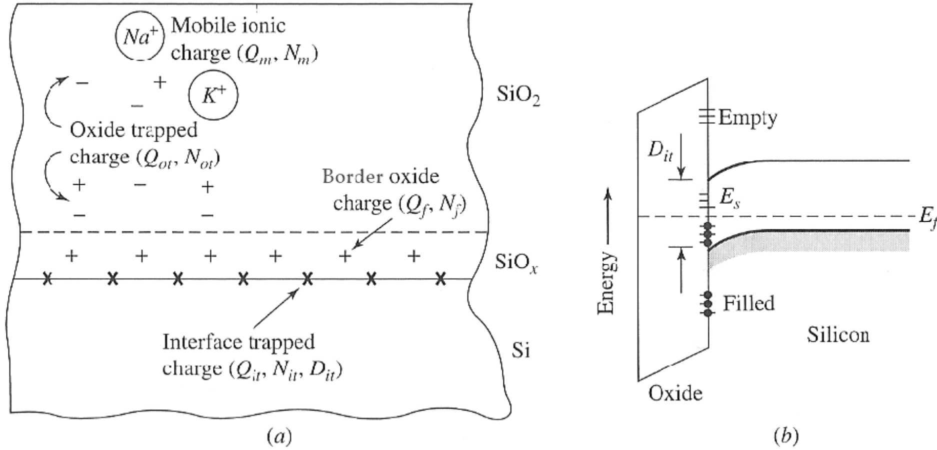



**Figure 2.16:** (a) Four categories of oxide charges in the MOS system. (b) Energy levels at the oxide/semiconductor interface.[8]

density of occupied defects varies. Indeed, a small leakage current through the structure (see description on injection mechanisms in Section 2.3) could enhance the charge trapped in the dielectric (see description of trapping mechanisms in Section 2.2.3 and 2.2.4) and therefore modify the properties of an oxide-based device.

The interface can result in an interlayer which possesses fixed charge and defects with levels within the semiconductor band-gap (near-interface or border states). The charge in the border states can be exchanged with the semiconductor but its distance from the interface, can make it a slow process.[41]

Finally, there is the interface charge which originates in carriers from the semiconductors trapped in levels induced by the defects right at the interface. These levels can readily be filled and unfilled with a time constant depending only on their position within the gap of the semiconductor. Their density is noted $N_{it}$ (in $\mathrm{cm}^{-2}$) which is the integral of $D_{it}$ (in $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$), their density at a given level in the gap.

It will be shown that the hi-lo CV technique is sensitive to all charges. However, only the density of some interface states can be directly quantified. Indeed, the applied voltage modifies the relative position of the Fermi level at the oxide/semiconductor interface, and therefore the number of occupied states [Figure 2.16(b)]. The variation in trap oc-

cupancy impacts the measured capacitance. Also, it will be explained how the technique can be applied to estimate the bulk oxide charge. One needs to keep in mind that it is a probing method and that the number of injected carriers in the bulk of the oxide during a measurement is neglected as well as its effect on the position of mobile ions.

### 2.4.2 Interface population

If an unbiased MOS structure is at equilibrium, the Fermi level must be constant throughout the layers. Since the work functions of the components are usually different, this results in a charge balance between the metal and the semiconductor. Therefore, the density of carriers at the oxide/semiconductor interface differs from the one in the semiconductor bulk and the energy bands are bent in the interfacial region [Figure 2.17(a)]. The bias required to flatten the bands, equalizing the charge density throughout the semiconductor, is the flatband voltage $V_{fb}$. If the oxide and the interface are ideal, none of the charges discussed above are present, the field is constant in the oxide and $V_{fb}$ simply depends on the difference $\Phi_{ms} = \Phi_m - \Phi_s$ between the work functions of the metal and the semiconductor. In practice, this is never the case and the flatband voltage can be expressed as[8]

$$V_{fb} = \Phi_{ms} - \frac{q}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \mathrm{Q}_{ox}[x]\, dx \tag{2.45}$$

where $\mathrm{Q}_{ox}$ is the oxide charge density (in cm$^{-3}$) which depends on the position $x$, $x_{ox}$ is the oxide thickness and $C_{ox}$ is the oxide capacitance per unit area. Since in general the position of the bulk charge is not known, Eq. (2.45) can be written

$$V_{fb} = \Phi_{ms} + \frac{qN_{eff}}{C_{ox}} \tag{2.46}$$

where $N_{eff}$ is the effective charge density, a practical number which corresponds to an equivalent charge density at the interface.

For a n-type semiconductor, gate voltages $V_g$ higher than $V_{fb}$ result in an increase

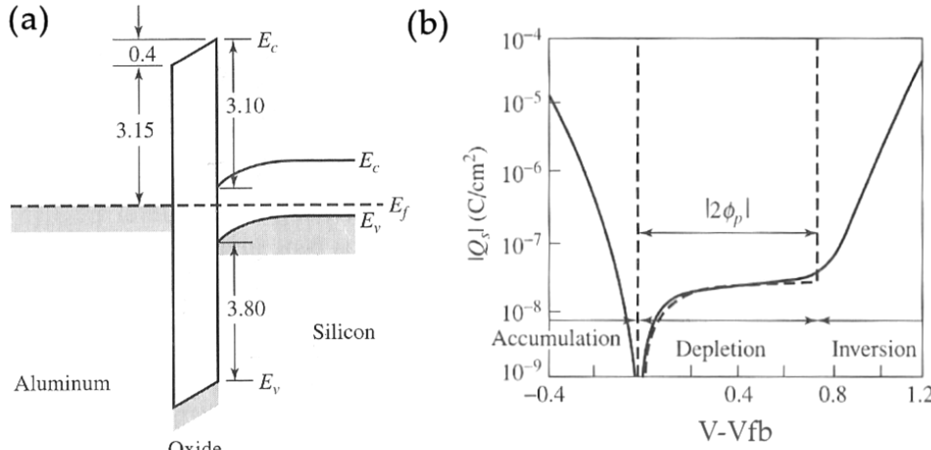



**Figure 2.17:** (a) Energy-band diagram at thermal equilibrium for an ideal MOS system. (b) Total charge in a p-type Si substrate as a function of the gate bias.[8]

of the electron density at the oxide/semiconductor interface and the capacitor is in the accumulation regime. When the bias is less than the flatband voltage, the majority carriers are pushed away from the interface; this is the depletion regime. Consequently, there is a positively charged transition layer due to the ionized doping atoms. The length of this layer increases when the bias is lowered until the Fermi level is close enough to the valence band ($V_g = V_t$) to generate a hole layer at the interface; this is the inversion regime. Strong inversion starts when the distance between the Fermi level and the valence band at the interface equals the one between the Fermi level and the conduction band in the bulk of the semiconductor. The same logic applies to p-type semiconductors. A plot of the total charge in the semiconductor as a function of the gate bias is shown in Figure 2.17(b).

If the generation of minority carriers is too slow compared to a characteristic measurement time, the inversion layer is not formed and one enters the deep depletion regime. Since the generation time increases exponentially with the energy gap, inversion can only be obtained in wide band-gap semiconductor MOS structures when they are exposed to UV light during the voltage sweep, or when the measurement is made at high enough temperature.

### 2.4.3 Small signal capacitance

When the structure is biased from accumulation to depletion, the position of the Fermi level changes at the oxide/semiconductor interface and the defect states can capture or emit electrons. So, the value of the flatband voltage depends on the total charge, and the population of switching states depends on the gate bias. It should then be clear that $N_{eff}$ and $D_{it}$ can be extracted from a voltage sweep. A good way to do so, is by probing the capacitance dependence on the bias.

A MOS structure is indeed a capacitor since the charge area density present on both sides of the oxide $Q$ (in C/cm$^2$) varies with the gate bias $V_g$. When the device is in accumulation or in inversion, the capacitance per unit area $C$ is equal to the one of the oxide $C_{ox}$. However, in the depletion (and deep depletion) regime, the capacitance depends on the length $x_d$ of the depletion region and therefore on the voltage. The equivalent circuit is two capacitors in series and the measured value is

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{x_d}{\epsilon_s} \tag{2.47}$$

where $\epsilon_s$ is the dielectric constant of the semiconductor.

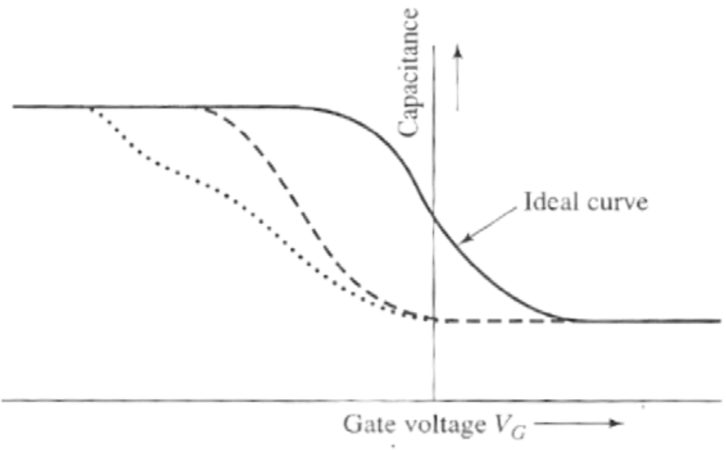



**Figure 2.18:** Fixed charge in the oxide causes the CV curve to translate and switching states cause its distortion.[8]

A typical set of CV curves for a p-type wide band-gap semiconductor is shown in Figure 2.18. The continuous curve is the ideal capacitance; there is no charge in the oxide and no switching state. The dashed line results from the addition of fixed positive charge in the oxide. In practice, this shift can be related to $N_{eff}$ by the relation

$$\Delta V_{fb} = \frac{qN_{eff}}{C_{ox}} \tag{2.48}$$

Finally, the doted curve is due to the presence of switching states. Their effect is to distort the curve because the amount of charge present right at the interface depends on the voltage. When the the capacitor is in flatband condition, the extra charge adds to $N_{eff}$, and the curve is shifted even more than in the previous case. As deep depletion is reached, traps empty and the dotted line meets the dashed line. This distortion allows the extraction of the $D_{it}$ as explained below. It should be clear that the fast border states could also switch during the measurement; therefore, the real $D_{it}$ can be over-estimated.

### 2.4.4 Capacitance-Voltage measurements

Capacitance can be measured in various conditions.[18] One can probe it as function of frequency and deduce the $D_{it}$ from the time dependence of the interface response (conductance method) or one can compare a CV curve at a given frequency to an ideal simulated curve and extract the parameters (Terman's method). Here, a third method is described: simultaneous high-frequency (AC) and low-frequency (quasi-static) CV measurements. It is known as the hi-lo technique; the setup is illustrated in Figure 2.19(a).

A constant amplitude small AC signal $V_{ac}$ is added to a DC one $V_{dc}$, so that the gate bias is given by $V_g = V_{dc} + V_{ac}$. The sweep of the DC bias is performed in a staircase fashion. It will be shown later that the limit of the technique comes from the AC angular frequency $\omega_{ac}$ and from the DC ramp rate $\Delta V_{dc}/\tau_{dc}$. A vector ammeter measures the resulting current. The total current density (in A/cm$^2$) is $J_{ac} + J_{dc}$.

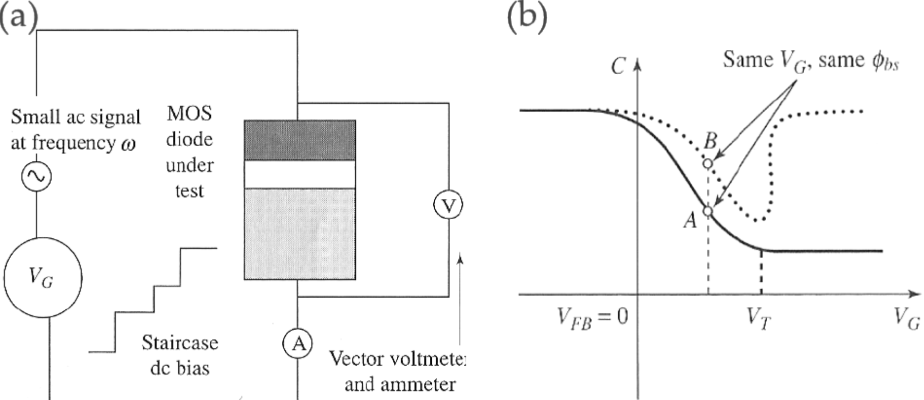



**Figure 2.19:** (a) MOS CV measurement system; the voltmeter and ammeter measure both the magnitude and the phase of the signal. (b) Simultaneous $C_h$ (continuous line) and $C_q$ (dotted line) measured as a function of voltage.[8]

The definition of the capacitance is

$$C = \frac{Q}{V_g} \tag{2.49}$$

The quasi-static capacitance $C_q$ can be extracted from the displacement current resulting from a small change in $V_{dc}$.

$$C_q = \frac{\Delta Q}{\Delta V_{dc}} = \frac{\int_0^{\tau_{dc}} J_{dc}\, dt}{\Delta V_{dc}} \tag{2.50}$$

and the high-frequency capacitance $C_h$ can be extracted from the amplitude of the AC signal

$$C_h = \frac{dQ/dt}{dV_{ac}/dt} = \frac{J_{ac}}{dV_{ac}/dt} = \frac{J^*_{ac}}{V^*_{ac}\,\omega_{ac}} \tag{2.51}$$

where $J^*_{ac}$ and $V^*_{ac}$ are respectively the amplitude of the AC current density and the amplitude of the AC bias.

A typical set of high and low frequency curves is shown in Figure 2.19(b) for p-type silicon. The reason why $C_h$ does not reach inversion is that the frequency $\omega_{ac}$ is typically 1 MHz, much faster than the generation rate. As explained earlier, in the case of wide band-gap semiconductors, even $C_q$ does not reach inversion. In any case, the $D_{it}$ is extracted

from the CV behavior in the depletion regime where the two curves are different because of the response time of the switching states. Indeed, as the bias is swept from accumulation to depletion, the traps emit their charges when the Fermi level at the interface crosses the corresponding energy in the band-gap. This emission affects the displacement current and, therefore $C_q$, but since those interface states do not subsequently fill and empty, they are not detected in $C_h$. At a given DC bias, the energy band bending (q$\phi_{bs}$) at the interface is the same for $C_q$ and $C_h$, and their difference reveals the $D_{it}$ value at the corresponding energy. Indeed,

$$\frac{1}{C_q} = \frac{1}{C_{ox}} + \frac{1}{qD_{it} + \epsilon_s/x_d} \tag{2.52}$$

and similarly for the high frequency capacitance

$$\frac{1}{C_h} = \frac{1}{C_{ox}} + \frac{1}{\epsilon_s/x_d} \tag{2.53}$$

which leads to the density of interface states at a given level

$$D_{it} = \frac{1}{q}\left(\frac{1}{C_q} - \frac{1}{C_h} + \frac{x_d}{\epsilon_s}\right)^{-1} - \frac{\epsilon_s}{qx_d} \tag{2.54}$$

The value of the corresponding trap energy, and the value of the depletion layer length, can be calculated using Berglund's method.[42]

Finally, it should be noted that the emission time of the traps on which the hi-lo method is based also sets the limit of the technique. Indeed, in a n-type material, for energy levels very close to the conduction band the emission time is so fast that charges can follow the high frequency signal and the two capacitances are therefore equal. And for deep levels, the emission time is so long that the traps cannot follow the DC signal and therefore do not empty. Subsequently, there is an energy window in which the method is valid; the upper limit (deep states) is set by the ramp rate $\Delta V_{dc}/\tau_{dc}$ and the lower limit (shallow sates) is set by the frequency $\omega_{ac}$. These limits can be calculated for n-type materials using the

expression for the emission time of an electron

$$\tau_n = \frac{1}{\sigma_n v_t N_c} exp\left(\frac{E_c - E}{k_b T}\right) \tag{2.55}$$

where $\sigma_n$ is the capture cross section of an electron by an interface trap, $v_t$ is the thermal velocity of an electron, $N_c$ is the density of states in the conduction band, $E_c$ is the energy of the conduction band edge, and $E$ is the energy level in the gap. At room temperature, the assumed valid window is between 0.2 eV and 0.6 eV from the band edges for a ramp rate of 0.1 V/s and a 1 MHz frequency. At 300 °C, this window is between 0.7 eV and 1.9 eV.[43] Therefore, the complete energy gap of wide band-gap semiconductors can be probed by measuring $D_{it}$ at different temperatures (see Figure 2.20).

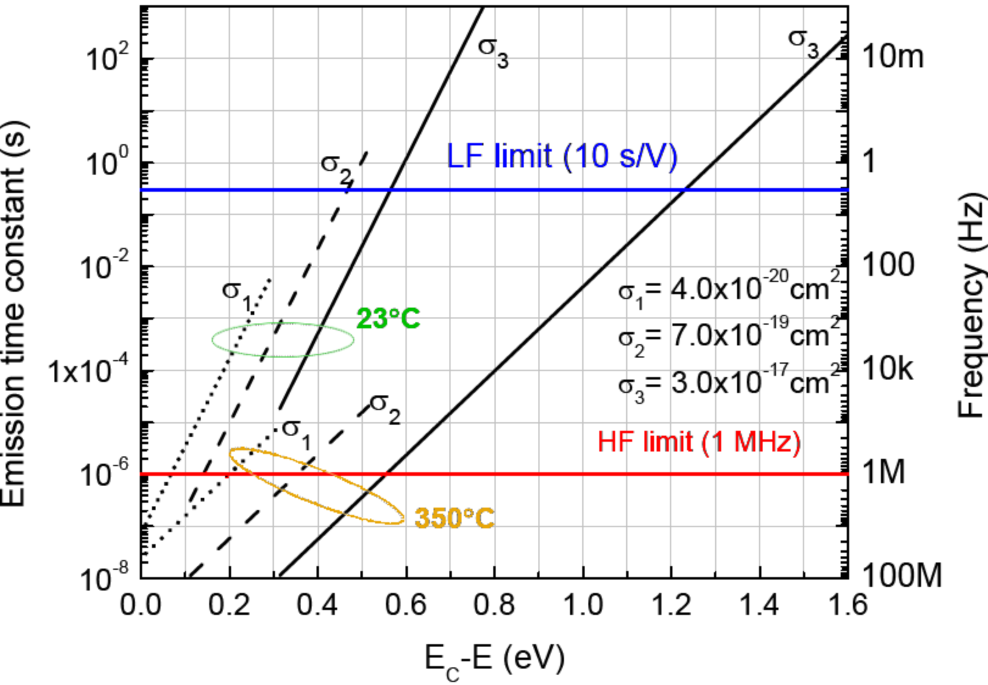



**Figure 2.20:** Emission time constants at 23 °C and 350 °C of traps with different capture cross-sections. $E_c$-E is the energy within the gap measured from the conduction band edge. Low-frequency (LF) and high-frequency (HF) limits of the hi-lo CV techniques are indicated. Courtesy of Sarit Dhar.

## References


[1] C. Kittel, *Physique de l'état solide (Solid State Physics)*, Dunod, 1998.

[2] J. J. O'Dwyer, *The Theory of Electrical Conduction and Breakdown in Solid Dielectrics*, Oxford University Press, 1973.

[3] W. T. Lynch, *Journal of Applied Physics* **43**, 3274 (1972).

[4] M. Sparks, D. L. Mills, R. Warren, T. Holstein, A. A. Maradudin, L. J. Sham, E. Loh Jr., and D. F. King, *Physical Review B* **24**, 3519 (1981).

[5] D. Arnold, E. Cartier, and D. J. DiMaria, *Physical Review B* **45**, 1477 (1992).

[6] D. Arnold, E. Cartier, and D. J. DiMaria, *Physical Review B* **49**, 10278 (1994).

[7] S. M. Sze, *Semiconductor Devices, Physics and Technology*, Wiley New York, 1981.

[8] R. Muller and T. Kamins, *Device Electronics for Integrated Circuits*, Wiley New York, 2003.

[9] J. M. Marshall, *Reports on Progress in Physics* **46**, 1235 (1983).

[10] R. J. Powell and G. F. Derbenwick, *IEEE Transactions on Nuclear Science* **18**, 99 (1971).

[11] H. Fritzsche, *Journal of Non-Crystalline Solids* **6**, 49 (1971).

[12] R. C. Hughes, *Physical Review B* **15**, 2012 (1977).

[13] H. Scher and E. W. Montroll, *Physical Review B* **12**, 2455 (1975).

[14] R. C. Hughes, *Physical Review Letters* **30**, 1333 (1973).

[15] R. C. Hughes, *Physical Review Letters* **35**, 449 (1975).

[16] R. C. Hughes, *Applied Physics Letters* **26**, 436 (1975).

[17] P. M. Lenahan and P. V. Dressendorfer, *Journal of Applied Physics* **55**, 3495 (1984).

[18] E. H. Nicollian and J. R. Brews, *Metal Oxide Semiconductor, Physics and Technology*, Wiley-Interscience, New-York, 1982.

[19] E. H. Nicollian, C. N. Berglund, P. F. Schmidt, and J. M. Andrews, *Journal of Applied Physics* **42**, 5654 (2003).

[20] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, *Applied Physics Letters* **86**, 142103 (2005).

[21] A. J. Lelis, T. R. Oldham, H. E. Boesch Jr., and F. B. McLean, *IEEE Transactions on Nuclear Science* **36**, 1808 (1989).

[22] K. Machida, N. Shimoyama, J. I. Takahashi, Y. Takahashi, N. Yabumoto, and E. Arai, *IEEE Transactions on Electron Devices* **41**, 709 (1994).

[23] J. H. Stathis and D. J. DiMaria, *Applied Physics Letters* **61**, 2887 (1992).

[24] Z. Liu, L. C. Feldman, N. H. Tolk, Z. Zhang, and P. I. Cohen, *Science* **312**, 1024 (2006).

[25] D. K. Schroder and J. A. Babcock, *Journal of Applied Physics* **94**, 1 (2003).

[26] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam, *IEEE Transactions on Electron Devices* **54**, 2143 (2007).

[27] J. B. Yang, T. P. Chen, S. S. Tan, C. M. Ng, and L. Chan, *Journal of The Electrochemical Society* **154**, G255 (2007).

[28] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, *Microelectronics Reliability* **45**, 19 (2005).

[29] A. E. Islam, G. Gupta, S. Mahapatra, A. T. Krishnan, K. Ahmed, F. Nouri, A. Oates, and M. A. Alam, Gate leakage vs. NBTI in plasma nitrided oxides: characterization, physical principles, and optimization, in *Proceedings of the International Electron Devices Meeting*, 2006.

[30] T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and D.-L. Kwong, *IEEE Electron Device Letter* **24**, 150 (2003).

[31] K. Muraoka, K. Kurihara, N. Yasuda, and H. Satake, *Journal of Applied Physics* **94**, 2038 (2003).

[32] J. P. Campbell, P. M. Lenahan, C. J. Cochrane, A. T. Krishnan, and S. Krishnan, *IEEE Transactions on Device and Materials Reliability* **7**, 540 (2007).

[33] P. J. McWhorter, S. L. Miller, and W. M. Miller, *IEEE Transactions on Nuclear Science* **37**, 1682 (1990).

[34] C. F. Pirri, S. Ferrero, L. Scaltrito, D. Perrone, S. Guastella, M. Furno, G. Richieri, and L. Merlin, *Microelectronic Engineering* **83**, 86 (2006).

[35] N. Mott and I. Sneddon, *Wave Mechanics and its Applications*, Oxford University Press, 1948.

[36] R. K. Chanana, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, J. R. Williams, and R. A. Weller, *Applied Physics Letters* **77**, 2560 (2000).

[37] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides*, World Scientific, 1999.

[38] J. W. Mayer and E. Rimini, editors, *Ion Beam Handbook for Material Analysis*, Academic Press, 1977.

[39] M. J. Berger and S. M. Seltzer, Stopping powers and ranges of electrons and positrons (2nd. Ed.), Technical report, National Bureau of Standards, 1983.

[40] R. C. Alig and S. Bloom, *Journal of Applied Physics* **49**, 3476 (1978).

[41] D. M. Fleetwood, P. S. Winokur, R. A. Reber Jr., T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, *Journal of Applied Physics* **73**, 5058 (1993).

[42] C. N. Berglund, *IEEE Transactions on Electron Devices* **13**, 701 (1966).

[43] J. A. Cooper Jr., *Physica Status Solidi (A), Applied Research* **162**, 305 (1997).

# PART TWO

## STUDIES ON THE PROPERTIES AND THE RELIABILITY OF THE $SiO_2$/SiC INTERFACE


| | | |
|---|---|---|
| Chapter III: | Pressure dependence of $SiO_2$ growth kinetics on SiC | 82 |
| Chapter IV: | Impact of nitrogen incorporation on electron trapping | 103 |
| Chapter V: | Impact of nitrogen incorporation on hole trapping | 113 |
| Chapter VI: | Dependence of interface properties on nitrogen density | 127 |
| Chapter VII: | Accelerated oxide breakdown on implanted surfaces | 154 |

# CHAPTER III

# $SiO_2$ GROWTH KINETICS ON SiC: A PRESSURE DEPENDENCE STUDY

## Overview

Dry oxidations performed between 0.25 and 4 atm at 1150 °C are used to characterize the pressure dependence of the growth kinetics of $SiO_2$ along three orientations of the 4H-SiC polytype. The growth curves are studied using the Deal-Grove model. The extracted linear and parabolic constants are found to scale linearly with the oxygen pressure up to 2 atm. However, the data indicates that the (0001) Si-face exhibits a retarded growth rate above 2 atm. It is also found that like Si, there is a critical oxide thickness below which the linear-parabolic model does not apply. This value is estimated to be between 36 and 40 nm for $SiO_2$ on 4H-SiC, and is apparently independent of the crystal orientation and oxidation pressure. The extracted critical thickness and its properties are similar to that on Si, suggesting that the fast growth regime is dictated by the nature of the oxide. Finally, variable pressure enables a decoupling of the growth rate and of the oxidation temperature so that their impact on the density of interface states ($D_{it}$) can be studied independently. Using the 4H-SiC (0001) Si-face, it is shown that (i) at a given temperature (1150 °C), an increased growth rate does not reduce the $D_{it}$, and that (ii) at a given oxidation rate ($\simeq$ 5nm/h), the $D_{it}$ is reduced by a higher processing temperature.

The content of this chapter has been published in part in the Journal of Applied Physics.[1]

## 3.1 Motivation

The formation of passivating layers is a topic of particular interest in all electronic materials system. In semiconductors, the creation of a high quality passivating and insulating layer is the critical step for high performance MOSFETs and other surface sensitive de-

vices.[2] The classic example is the formation of the $SiO_2$ layer on silicon, which underlies all of silicon MOS technology. The growth of the oxide layer has its roots in the so called "linear-parabolic" description of Deal and Grove.[3] Although still not completely understood, particularly with respect to the growth of the initial monolayers of the oxide,[4,5,6] the Deal-Grove (D-G) model nicely describes oxide growth kinetics in terms of experimental and theoretical parameters, such as temperature and oxygen pressure. This model of growth, and its agreement with experiment, forms an underpinning for all silicon oxidation that has stood the test of time.

As mentioned in the previous chapters, silicon carbide is a wide band-gap semiconductor that also forms a silicon dioxide passivating layer upon oxidation. Considerable effort in recent years has shown that this insulating layer is essentially pure $SiO_2$, and forms a sufficiently good surface termination to allow SiC MOSFETs.[7] Such SiC based devices promise operation at extreme voltages and temperatures useful in a wide variety of applications not accessible to silicon.[8,9] The oxidation process for SiC is significantly more complicated as the growth rates are a strong function of crystal face and the fundamental process requires elimination of the carbon species.[10,11,12,13] Nevertheless it has been shown that the growth kinetics are Deal-Grove like (linear-parabolic), so that they can be described within their original framework.[10,14,15,16,17,18,19] SiC oxidation is a vital step in the ultimate realization of a SiC technology and requires the same scrutiny as has been given to silicon, namely a test of oxidation models with significant parameter variation.

In this chapter, results of the pressure dependence of dry 4H-SiC oxidation above and below the standard 1 atmosphere are presented. It is observed that the predicted pressure dependence of the D-G model is well verified in almost all cases, with the oxygen pressure varying from 0.25 to 4 atmospheres. Detailed experimental results are presented and analyzed in terms of SiC oxidation models. Some interesting deviations from the predicted pressure dependence are observed on the (0001) Si-face, the most commonly used surface for devices.

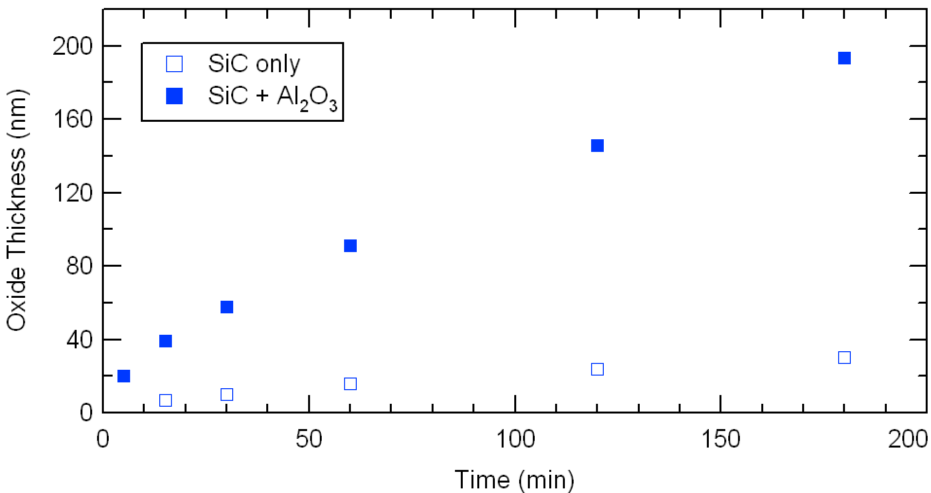



**Figure 3.1:** $SiO_2$ thickness on the (0001) Si-face of 4H-SiC as a function of time for dry oxidation performed at 1150 ° in flowing oxygen (1 atm). The growth rate in the presence of alumina (containing alkali metals) is about five time faster.

These results have additional significance in light of the current interest in the $SiO_2$/4H-SiC system. In particular, oxidation in the presence of alumina including various metallic impurities results in a higher oxidation rate (see Figure 3.1) and in an improved electrical interface over that grown in a conventional system (no alumina). The mechanism for this improvement is not yet understood, but it has been hypothesized that the enhanced rate might be directly responsible.[20,21,22,23] One can imagine different trade-offs between the expulsion of carbon and growth of the oxide that may favor the high rate process, or other catalytic mechanisms. The results reported here allow a direct examination of the growth rate dependence of the electrical properties at a given temperature (1150 °C). It is found that the interface state density, a critical factor in device performance, is not improved by faster growth rates between 0.2 and 0.6 eV from the 4H-SiC conduction band edge. However, increasing the processing temperature (from 1000 to 1150 °C), while maintaining the growth rate constant via pressure adjustment, leads to reduced $D_{it}$ within that energy window.

The study described here provides a significant verification of the applicability of D-G -like parametrization of SiC oxidation, with a few outstanding anomalies. It supplies the

basis for scaling to new regimes of temperature and pressure in applications, as well as new data to be tested by SiC oxidation models.

### 3.2 Growth Kinetics

In this section, the linear-parabolic model for Si oxidation is introduced and is then applied to the SiC system, accounting for a more complex substrate. From these equations, the expected pressure dependence of the growth rate is extracted.

The linear-parabolic model for silicon oxidation, proposed by Deal and Grove,[3] relies on the assumption that the flux of oxidant molecules is constant across the gas, the oxide, and the interface. It predicts the combination of two growth regimes, each governed by a different rate-limiting mechanism. The anticipated relationship between the $SiO_2$ thickness $x$, oxidation time $t$, and growth parameters is as follows;

$$x^2 + A\,x = B\,(t + \tau) \tag{3.1}$$

where $\tau$ defines the time it takes to grow the layer of oxide present on the surface prior to an oxidation step. The constants $B$ and $A$ are defined below, in the case of a first-order oxidation reaction.

$$B \equiv \frac{2D_{eff}C^*}{M} \tag{3.2}$$

and

$$A \equiv 2\,D_{eff}\,(\frac{1}{K} + \frac{1}{H}) \tag{3.3}$$

Here, $D_{eff}$ is the effective diffusion coefficient of the oxidant species through the oxide, $C^*$ is the equilibrium concentration of the oxidant in the oxide, $M$ is the number of incorporated oxidant molecules per unit volume of the oxide layer, $K$ is the reaction rate coefficient of the oxygen at the semiconductor surface, and $H$ is the gas transport coefficient for the oxidant

molecules in the gas phase. Equation (3.1) can be put in the form;

$$x[t] = \frac{-B}{2\,B/A} + \frac{B}{2}\sqrt{\frac{1}{(B/A)^2} + \frac{4\,(t+\tau)}{B}} \tag{3.4}$$

At the extremes of rate-limiting processes, Eq.(3.4) reduces to simplified expressions. When the oxide is thin, growth is limited by the reaction rate, and thickness is a linear function of time; the proportionality factor being $B/A$, the linear rate constant. At large thicknesses, the rate is governed by the diffusion of oxidant species through the oxide and growth enters a parabolic regime characterized by $B$, the parabolic rate constant.

Although in the D-G model $\tau$ is used to describe a layer of oxide present on the semiconductor before oxidation, it can also be related to a regime of fast growth rate that does not behave according to linear-parabolic kinetics.[4,5,6] At small times and at thicknesses less than $\sim 35$ nm, the oxide growth rate is exponential and gradually becomes linear as in the D-G model. This critical thickness highlights a regime where linear-parabolic kinetics are not valid.

The D-G model can also be applied, with modifications, to the more complicated SiC oxidation. The derivation accounts for the outdiffusion of the CO gas that is a byproduct not present in Si oxidation.[10] The new linear rate constant is

$$\frac{B}{A} \simeq \frac{C^{*}K_f}{M} \tag{3.5}$$

where $K_f$ is the forward reaction rate constant.

In SiC oxidation, the rate limiting step of the parabolic regime is unclear. If the $O_2$ indiffusion is limiting, then the parabolic rate constant becomes

$$B \simeq \frac{2D_{O_2}C^{*}}{1.5M} \tag{3.6}$$

using an additional factor of two, in accordance with recent corrections to the previously published model. If the outdiffusion of the CO byproduct gas slows the process, then the

parabolic rate constant is expressed as

$$B \simeq \frac{2D_{CO}C^*}{M}\frac{K_f}{K_r} \tag{3.7}$$

where $K_r$ is the reverse reaction rate constant, and $D_{CO}$ is the diffusion coefficient of the CO gas through the oxide. Here, $B$ and $B/A$ are effective parabolic and linear rate constants, derived by assuming a single-step first-order oxidation reaction. In practice, they could describe a multi-step process of competing elements. Their value accounts for the overall rate-limiting speed and not the individual steps in the oxidation process. SiC experiments show that the time needed to grow an oxide thickness similar to one grown on Si is increased and that the linear rate constant is smaller on all faces, indicating a slower oxidation reaction process.

The pressure dependence of growth rate in the D-G model arises from the expressions for the linear and parabolic rate constants, which are both linearly proportional to the equilibrium concentration of oxidant species. By Henry's law

$$C^* = k_h p \tag{3.8}$$

where $p$ is the partial pressure of the oxidant species and $k_h$ is Henry's Law constant. Therefore, $B$ and $B/A$ are predicted to be linearly proportional to the oxidant partial pressure. Expected equilibrium values for $C^*$ at various pressures are reported in Table 3.1. Henry's law constant is calculated from reported values of $C^*$ for $SiO_2$ grown at 1000 °C and 1 atm on Si.[2] At 1150 °C, $k_h$ is 4.52 $10^{16}$ $\text{cm}^{-3}\text{atm}^{-1}$.

Accounting for the pressure dependence in Eq.(3.4), a relationship between oxide thickness, time, and pressure can be established;

$$x[t,p] = -\frac{\beta}{2\alpha} + \sqrt{\frac{\beta^2}{4\alpha^2} + \beta\, p(t+\tau)} \tag{3.9}$$

where $\beta$ and $\alpha$ are proportionality constants of $B$ and $B/A$, respectively, to pressure. This

**Table 3.1:** Equilibrium concentration of $O_2$ in the oxide ($10^{16}$ cm$^{-3}$) at 1150 °C.

| Pressure (atm) | 0.25 | 0.5 | 1 | 2 | 4 |
|---|---|---|---|---|---|
| $C^*$ | 1.13 | 2.26 | 4.52 | 9.04 | 18.08 |

shows that oxide thickness is a function of the product of time and pressure in the case of a single first-order oxidation reaction. For a desired thickness, only the product of $p$ and $(t + \tau)$ must remain constant, enabling control of the oxidation rate with pressure, at a given temperature. Increasing the oxygen partial pressure reduces the time (i.e. the thermal budget) needed to reach a given thickness, leading to faster and lower-cost fabrication of devices.

The temperature dependence of the growth kinetics arises from the diffusion coefficients and from the reaction rate constants, all of which describe thermally activated processes. As a consequence both the linear and parabolic rate constants are proportional to $exp(-E_a/k_bT)$ where $E_a$ is an activation energy, $k_b$ is Boltzmann's constant and $T$ is the temperature. The temperature dependence is therefore reflected in the parameters $\alpha$ and $\beta$. From Eq.(3.9), it can then be concluded that, while the temperature is varied, the growth rate can be maintained constant via pressure adjustment.

In summary, there are two main benefits resulting from the control of the oxygen pressure in an oxidation station. First, the thermal budget can be reduced by increasing the pressure at a given temperature. Second, the oxidation temperature and the growth rate can be decoupled, allowing for the study of their respective impact on the quality of the oxide and of its interface with the semiconductor.

## 3.3 Experiments

The 4H-SiC samples are 5mm×5mm, cut from single-side polished (0001)/(000$\overline{1}$) oriented (research grade, $n$-type, 8° off axis), and (11$\overline{2}$0) oriented (research grade, $n$-type, on axis) wafers obtained from Cree Inc.

Samples were cleaned by TCE, acetone, methanol, and HF, in successive steps. Some of the (0001) Si-face substrates, selected for electrical measurements, were further cleaned using the standard RCA steps.

All samples were oxidized in a 55 mm OD thick-walled glass tube inside a Thermcraft 3-zone furnace. They were loaded at 900 °C an ramped up to oxidation temperature at 1 atm in flowing Ar (thickness measurements) or in flowing $O_2$ (electrical measurements). Dry oxidations were performed at 0.25, 0.5, 1, 2, and 4 atm (100% oxygen).

For runs below 1 atm, a flow of 0.05 L/min was maintained with an adjustable bellow valve coupled to a vacuum pump. Oxidations at 1 atm were performed in $O_2$ flowing at 0.25 L/min. High pressure oxidations utilized an adjustable release valve and an oxygen flow of 0.05 L/min. Following oxidation, the tube was brought back to 1 atm and Ar was flown. The samples used for electrical characterization were then annealed for 30 min at oxidation temperature. Details on the oxidation setup are given in Appendix A.

Oxide thicknesses were measured using a M-2000DI, J.A. Woollam Co. Inc., spectroscopic ellipsometer. For oxides thinner than 15 nm, Rutherford back-scattering (RBS) and ion channeling were used to confirm ellipsometry measurements, which were found to be in good agreement. Once the thicknesses were obtained, the same samples were put back into the tube for further oxidation.

Al metal gate contacts (500 $\mu m$ in diameter) were evaporated on the Si-face samples oxidized at 0.25, 1, and 4 atm used for electrical measurements in order to obtain MOS capacitors. Simultaneous high and low frequency capacitance-voltage (CV) measurements were then performed using a Keithley model 82 to determine the interface state density, as described in Chapter II (Section 2.4.4).

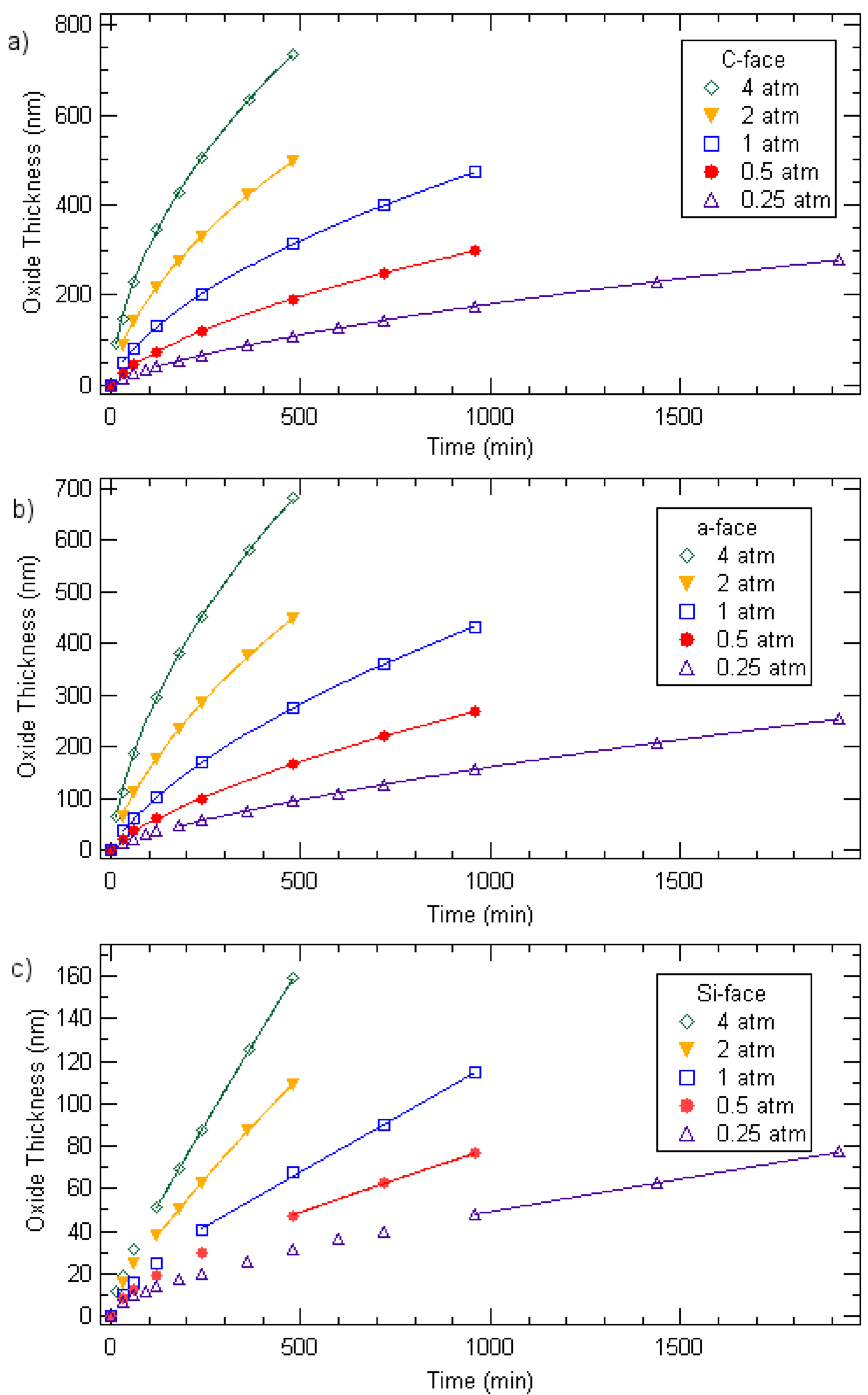



**Figure 3.2:** Oxide thickness as a function of time for dry thermal oxidation of 4H-SiC at 0.25, 0.5, 1, 2, and 4 atm at 1150 °C on the a) $(000\overline{1})$ C-terminated face, b) $(11\overline{2}0)$ *a*-face, and c) (0001) Si-terminated face. Solid lines are D-G fits to thicknesses above $X_c$.

## 3.4 Results and Discussion

In this section, a critical thickness for the oxidation of 4H-SiC is first identified. This results in a $\tau$ parameter that must be used to accurately describe oxide growth on SiC when using a linear-parabolic model. The extracted values of the linear and parabolic rate constants at different pressures are then reported and an anomaly on the Si-face at 4 atm is highlighted. Finally, this section demonstrates the decoupled effects of growth rate and temperature on the $D_{it}$ at the $SiO_2$/SiC interface. Growth data at 1150 °C for all pressures and substrate orientations is shown in Figure 3.2.

### 3.4.1 Initial oxidation

As previously noted, the parameter $\tau$ is related to a critical thickness below which the D-G model does not apply. While it is not normally used in the modelling of SiC oxidation, this study shows that growth curves at small thicknesses deviate from a linear-parabolic regime similarly to $SiO_2$ on Si as illustrated in Figure 3.3. Therefore, all fits to the linear-parabolic model must exclude points below the determined critical thickness $X_c$.

Several methods exist for determining the critical thickness.[4] The most appropriate to these results is fitting the oxidation data to the D-G equation from point ($X$,$t$) to the largest point taken ($X_f$,$t_f$). If ($X$,$t$) is less than the critical thickness, then the growth deviates from linear-parabolic kinetics and the fit will have a large error. When $X$ corresponds to $X_c$, the error in the fit is minimized as no non-linear contribution from the accelerated growth is considered. The point where constant fit error begins is taken to be the critical thickness.

Table 3.2 shows the results of applying the above technique to the 0.25 atm data. The uncertainty in these values comes from the limited number of measured thicknesses. Reported ranges are the closest data points on either side of $X_c$. Error propagation prevents thickness measurements for samples oxidized less than 15 min apart. Data from 0.25 atm represents the most precision as there are a greater number of points below the critical

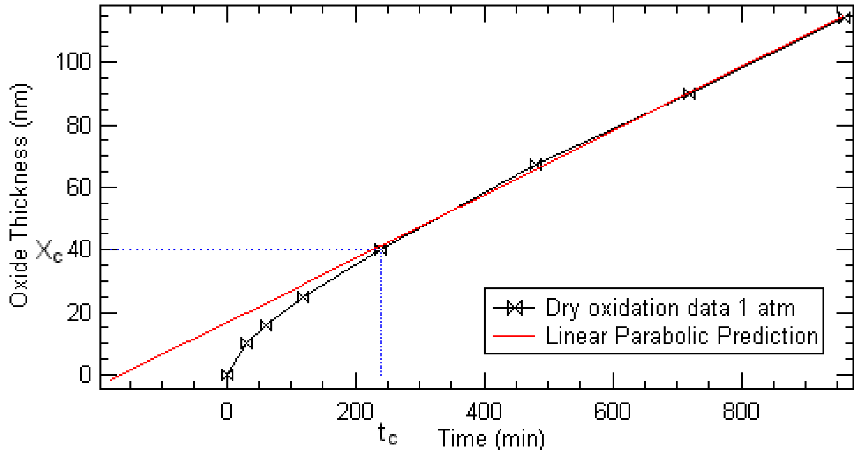



**Figure 3.3:** The fit of the linear-parabolic relationship to oxidation data in dry oxygen at 1 atm on the (0001) Si-face at 1150 °C. Point ($X_c$, $t_c$) denotes the onset of the linear-parabolic kinetics. The deviation from the Deal-Grove model at small times and thicknesses is evident.

thickness and yields the values reported. From the results, there is no evidence that $X_c$ changes with pressure. Therefore, all growth curves are fit to the D-G equation [Eq.(3.4)] excluding thicknesses less than $X_c$ ($\simeq$ 36 nm) and incorporating $\tau$.

Not only is the extracted value of $X_c$ similar to the one reported for Si (35 nm),[4] but it also appears to be independent of crystal orientation and oxidation pressure. This agrees well with the recent results of Yamamoto *et al.* who reported that the extent of the accelerated growth on SiC does not vary with oxidation temperature either.[24] These properties of the critical thickness are analogous to those observed in the case of silicon oxidation.[5,6] Since the reaction mechanisms are so different between Si and SiC, this suggests that the fast-growth regime is dictated by the nature of the oxide. This important conclusion should help elucidate the physics behind accelerated growth and should be tested against existing models.[25,26,27,28] For example, it has been proposed that when the bare surface of Si is exposed to $O_2$, oxygen molecules can diffuse into the semiconductor, accelerating the growth.[6] However, the solubility of molecular oxygen in SiC is two orders of magnitude smaller,[29,30] which likely invalidates that particular model. Although it is outside the scope of this chapter, a more extensive discussion is of course required to consider all existing models.

**Table 3.2:** Critical thickness $X_c$ (nm)

| Face | Oxide Thickness |
|---|---|
| $C - face$ | 34-42 |
| $a - face$ | 36-46 |
| $Si - face$ | 36-40 |

### 3.4.2 Extraction of growth parameters

As mentioned above, the pressure dependence of the oxidation kinetics is reflected in the linear and parabolic rate constants. These are extracted using Eq.(3.4) and 36 nm as a critical thickness. The results are reported in Tables 3.3, 3.4, and 3.5. Note that the values of $\tau$ are not negligible, stressing the fact that this parameter should be used when modeling SiC oxidation by a linear-parabolic equation. Figure 3.4 shows the linear and parabolic rate constants plotted as a function of pressure and their fit to a linear relationship. As described in Section 3.2, the constants' linear scaling with pressure is predicted by the D-G model and Henry's law. The fact that the values for $B$ of both the C- and $a$- faces are almost equal at any given pressure suggests that, from Eqs. (3.6) and (3.7), the CO outdiffusion is not the rate-limiting step in SiC oxidation in those cases. Indeed, the $O_2$-indiffusion-limited parabolic rate constant is not orientation-dependent, while the CO-outdiffusion-limited parabolic rate constant scales with the ratio of reaction rate constants which are unique to each face. Moreover, in the case of 1 atm dry oxidation at 1150 °C, the parabolic rate constant for Si divided by 1.5 [normalizing factor, see Eqs. (3.2) and (3.6)] is approximately 330 $nm^2$/min, similar to the values obtained on the C-face and on the $a$-face as shown in Table 3.4. Accurate values for the parabolic rate constant on the Si-face could not be obtained because the thickness of the oxide on this face was insufficient to reach the onset of the parabolic growth regime.

**Table 3.3:** $\tau$ (min) at 1150 °C

| Pressure (atm) | 0.25 | 0.5 | 1 | 2 |
|---|---|---|---|---|
| $C-face$ | 46.75 | 12.93 | 11.12 | 7.88 |
| $a-face$ | 50.22 | 20.47 | 11.23 | 8.94 |
| $Si-face$ | 347.19 | 186.46 | 95.09 | 31.83 |

**Table 3.4:** Parabolic rate constant $B$ (nm$^2$/min) at 1150 °C

| Pressure (atm) | 0.25 | 0.5 | 1 | 2 |
|---|---|---|---|---|
| $C-face$ | 75.65 | 151.79 | 327.4 | 713.99 |
| $a-face$ | 75.22 | 157.46 | 343.99 | 755.69 |

**Table 3.5:** Linear rate constant $B/A$ (nm/min) at 1150 °C

| Pressure (atm) | 0.25 | 0.5 | 1 | 2 |
|---|---|---|---|---|
| $C-face$ | 0.29 | 0.77 | 1.64 | 3.54 |
| $a-face$ | 0.23 | 0.51 | 1.02 | 2.03 |
| $Si-face$ | 0.04 | 0.08 | 0.13 | 0.26 |

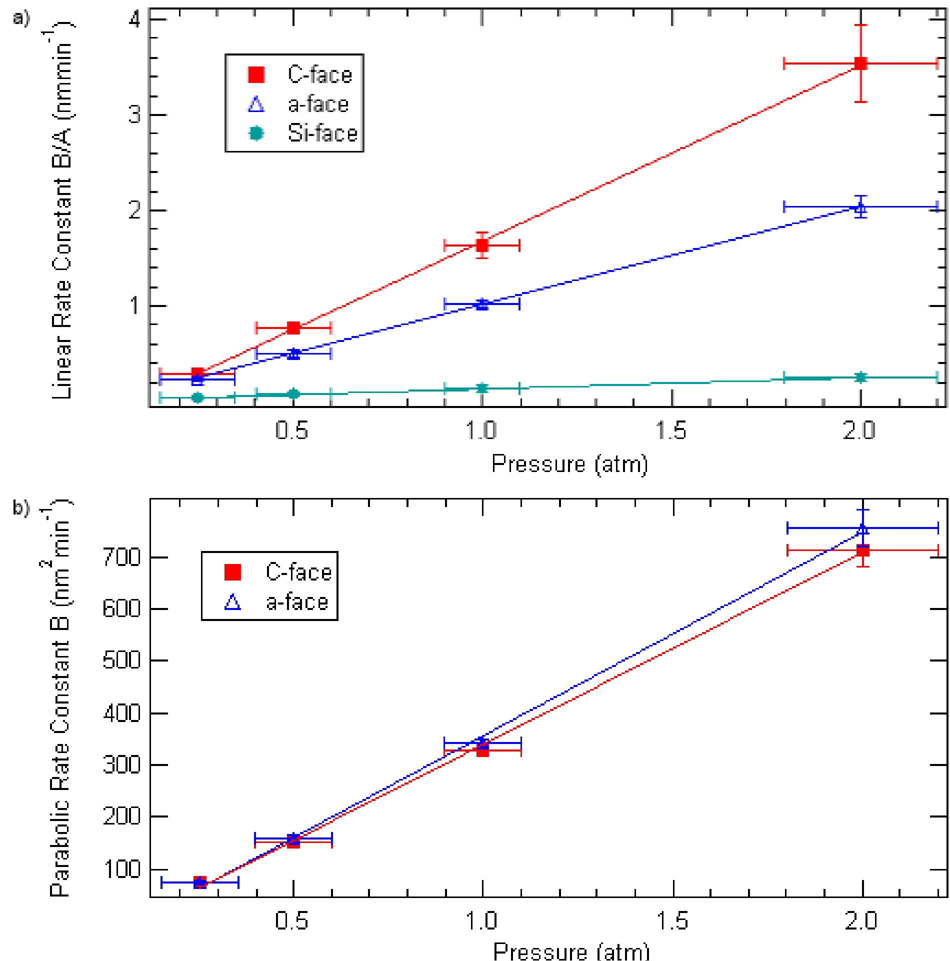



**Figure 3.4:** a) Linear rate constant at 1150 °C as a function of pressure for the $(000\overline{1})$ C-, $(11\overline{2}0)$ *a*-, and (0001) Si-faces of 4H-SiC. b) Parabolic rate constant at 1150 °C as a function of pressure for the $(000\overline{1})$ C- and $(11\overline{2}0)$ *a*-faces of 4H-SiC. The pressure dependence of the constants is modeled well by a linear law between 0.25 and 2 atm.

The linear rate constant $B/A$ also scales linearly with the pressure for all three studied SiC faces between 0.25 atm and 2 atm. In this regime, the differences in $B/A$ between faces are more pronounced because the kinetics are governed by the reaction rate constant, which depends on crystal orientation. Actually, the linear reaction rate seems to scale with the density of carbon atoms on the surface. Indeed the ratio of B/A for the C-face to the *a*-face is about 1.6, which is close to the ratio of the amount of carbon on the two faces (1.21 to 0.74 $10^{15}$ atoms $cm^{-2}$). Ideally, the Si-face has no carbon on the surface and the rate is considerably smaller.[10] These observations suggest that the carbon, which distinguishes the

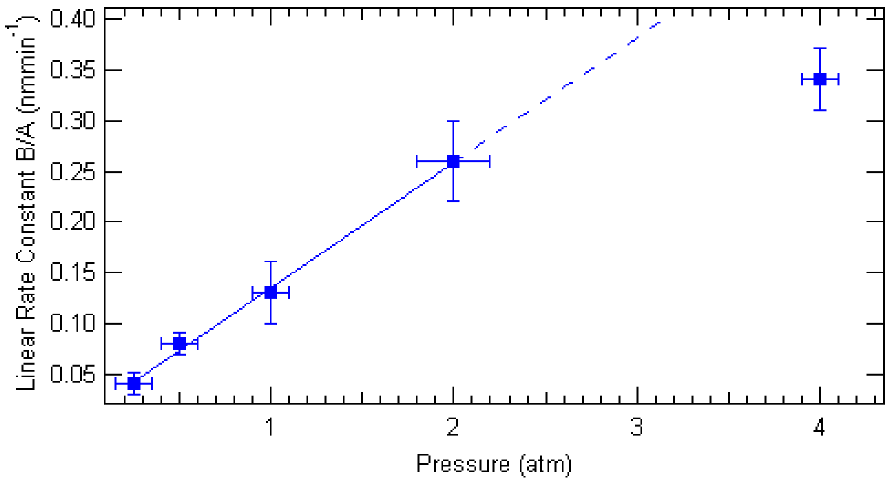



**Figure 3.5:** Linear rate constant at 1150 °C as a function of pressure for the (0001) Si-terminated face. The line is the linear fit to $B/A$ from 0.25 to 2 atm. The 4 atm point does not fall on the curve, which reveals a sublinear pressure dependence in that range.

$SiO_2$/SiC system from the $SiO_2$/Si system, plays a key role in the oxidation process and might be the reaction rate determining factor.

So far, the 4 atm data has been omitted because the lack of thicknesses measured below the onset of the parabolic regime prevents the accurate extraction of the rate constants for the *a*-face and the C-face. However, the Si-face could be analyzed up to that pressure.

While it was shown that the pressure dependence of the reaction rate between 0.25 to 2 atm can be modeled by a linear law, this no longer holds at 4 atm on the Si-face, as evidenced in Figure 3.5. Indeed, the linear rate dependence is then more accurately described by $p^{0.4}$. To better illustrate this change in behavior, thickness vs. pressure×time curves are plotted for 0.25, 1, and 4 atm in Figure 3.6. According to Eq.(3.9), these curves will be shifted along the normalized time axis in the presence of a nonzero $\tau$. However, at a given thickness, the slopes (proportional to the growth rate) are expected to be equal. This is of course, if the dependence of the rate constants on the pressure is linear. Thus, such normalized curves allow to test the D-G model and Henry's law using the raw data, as no fit is needed. Note that the normalized slopes for the C- and *a*-faces (not shown, all curves are atop each others because of smaller $\tau$ values) agree well over all pressures and it

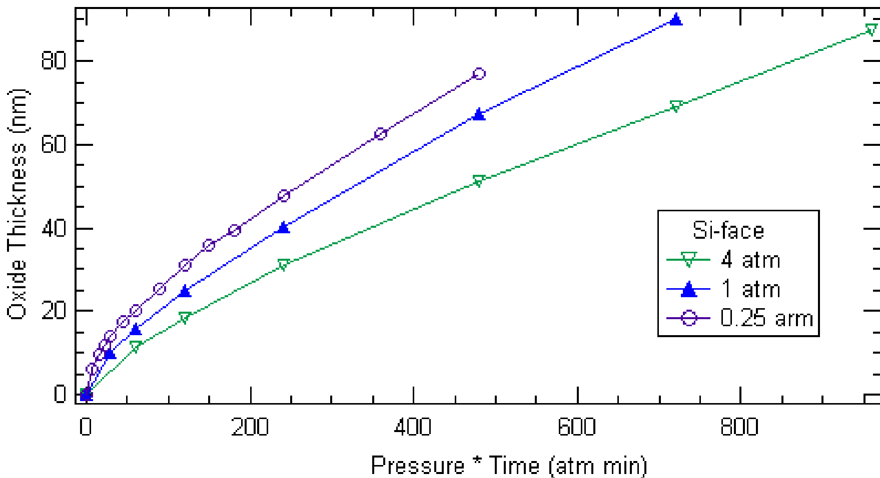



**Figure 3.6:** Oxide thickness on the (0001) Si-face as a function of the product of pressure and time at 1150 °C for 0.25, 1, and 4 atm. The reduced slope of the 4 atm data at any given thickness indicates a retarded growth rate at this pressure (i.e. a sublinear pressure dependence). Lines here are guides for the eye.

can be assumed that their growth rates depend linearly on pressure up to 4 atm. For the Si-face however, the normalized slope is almost equal at 0.25 and 1 atm but is smaller at 4 atm. This supports the sublinear pressure dependence of the rate constant at 4 atm shown in Figure 3.5, which was extracted from the D-G fit.

Sublinear pressure dependence of the growth rate has been observed in some cases for Si oxidation,[31,32,33] and attempts have been made to relate it to specific reaction mechanisms.[34,35] In particular, such a dependence is expected if several oxidation reactions (of different orders) involving the decomposition of $O_2$ molecules into atomic oxygen take place simultaneously. Under specific assumptions, Ghez and van der Meulen have shown[34] that if the insertion of atomic oxygen is the primary oxidation process, the growth rate becomes proportional to $p^{0.5}$. As oxidation reactions involving both atomic and molecular species are thought to occur in parallel, the dependence is predicted to be of the form $p^{\gamma}$, where the value of $\gamma$ is between 1 and 0.5, depending on the dominating reaction. The same conclusions can be applied to SiC oxidation; if the sublinear pressure dependence is observed on the Si-face only, it could mean that the $O_2$ reaction rate is so slow in that case that it

allows for secondary reactions (e.g. the inclusion of atomic oxygen) to weigh more in the overall process.

Another possible explanation for the sublinear pressure dependence is that the slow reaction rate on the Si-face leads to a reaction-limited regime which extends over larger $SiO_2$ thicknesses. Consequently, the $O_2$ concentration gradient across the oxide is small ($C_{O_2}$ at the interface is close to $C^*$) even for thicker oxides, which requires the indiffusion of more oxygen molecules to achieve equilibrium. Increasing the pressure exacerbates this phenomenon and it could be that although Henry's law is still valid (as suggested by the *a*-face and the C-face data), the time required to achieve equilibrium becomes too long and the oxidation is not a steady-state process.

### 3.4.3 Electrical properties of the interface

Measuring the $D_{it}$ of $SiO_2$/SiC interfaces with similar oxide thicknesses ($\simeq$ 40 nm), all grown at at 1150 °C using different $O_2$ pressures, allows a test of the hypothesis that an increased growth rate will enhance the interface quality. After performing CV measurements on the samples, it is concluded from Figure 3.7(a) that increasing the growth rate does not decrease the $D_{it}$ and that oxidizing at 4 atm actually increases the number of traps within the upper part of the band-gap. The increase in $D_{it}$ at 4 atm coincides with the Si-face anomaly. This could be the result of a different rate limiting process in the high pressure oxidation regime of the Si-face. A process that could lead to a wider transition layer and/or to C buildup at the interface, subsequently increasing the $D_{it}$. In any case, it can be inferred that increased growth rates observed in metal-enhanced oxidation (MEO) processes do not directly contribute to the $D_{it}$ reduction and that some other mechanisms, such as interactions with a metal impurity (e.g. sodium), must be responsible for improving the inversion layer mobility.[20,22,21,23]

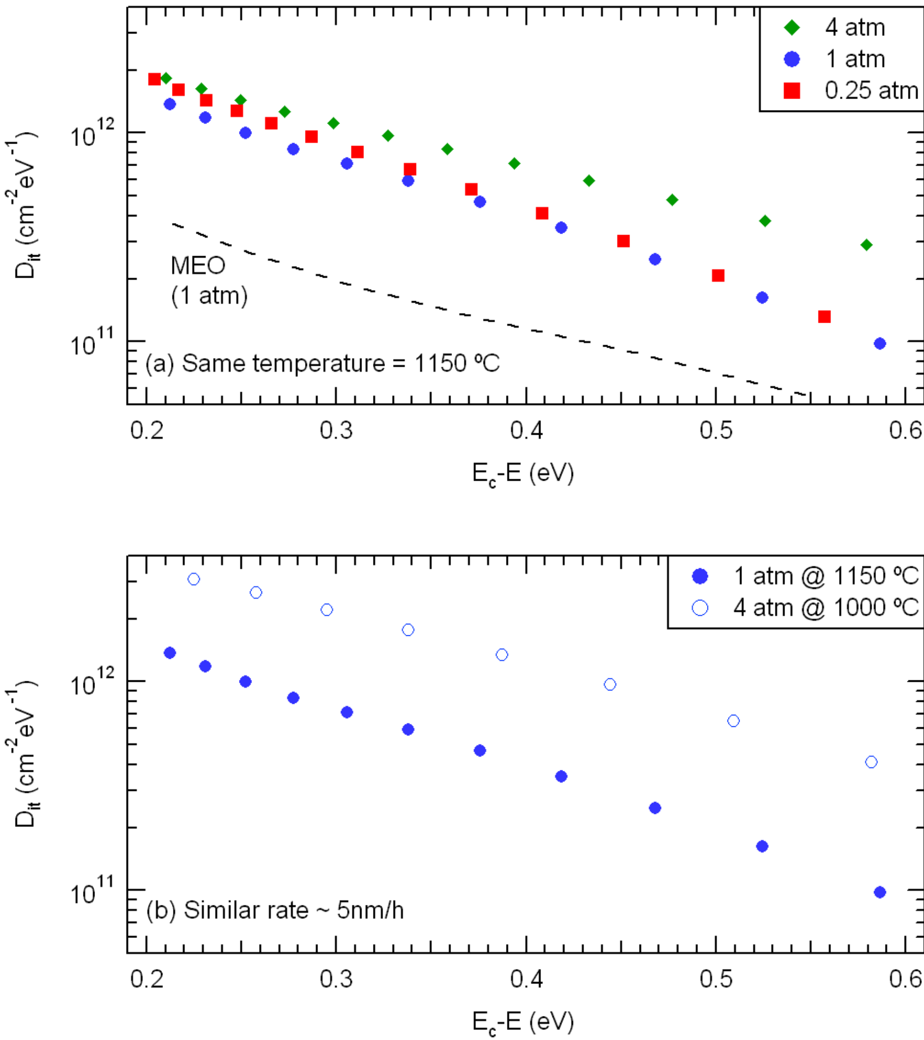



**Figure 3.7:** Measured interface trap densities in the upper part of the band-gap for oxides grown on the (0001) Si-terminated face; (a) at the same temperature (1150 °C) but different rates, (b) at similar rates ($\simeq$ 5 nm/h) but different temperatures. From (a), it can be seen that increasing the rate (i.e. the pressure) does not lead to lower defect densities as it is the case when alumina (MEO) is present during oxidation.[20] From (b), it is concluded that low oxidation temperatures make the interface worse.

As shown in Figure 3.7(b), the $D_{it}$ was also measured on samples oxidized at two different temperatures; 1000 and 1150 °C. The $SiO_2$ growth rates were kept similar ($\simeq$ 5 nm/h) using an oxygen pressure of 4 and 1 atm respectively, yielding similar thicknesses. It can be seen that the lower oxidation temperature leads to a consequent increase in the $D_{it}$ throughout the monitored energy window.

### 3.5 Summary

In this chapter, it was shown that between 0.25 and 4 atm, the kinetics of thermal oxidation of 4H-SiC at 1150 °C can be studied using the Deal-Grove linear-parabolic model. As in the case of silicon, there is a critical thickness (36 to 40 nm) below which D-G kinetics do not apply. Therefore, it is necessary to employ $\tau$ to properly characterize oxide growth.

Agreements of the critical thickness on all faces and with Si, as well as its lack of sensitivity to processing parameters, hint that the departure from the linear-parabolic model at small thicknesses may be a property of $SiO_2$ only.

The linear and parabolic rate constants scale linearly with pressure up to 2 atm for all faces. However, at 4 atm, the Si-face growth rate is better predicted by a sublinear law, revealing the presence of a different rate limiting process. This process is suspected to increase the density of interface defects.

Using variable pressure, it was also determined that enhancing the growth rate at a given temperature does not decrease the density of interface states within the monitored energy window, and that the accelerated growth in the presence of alumina is probably not by itself responsible for better device properties.

Increasing the oxidation pressure not only allows for accelerated growth rates at a given temperature but also enables the oxidation of SiC at lower temperatures in shorter times. However, the interface state density at a given rate appears to increase at lower processing temperatures.

## References


[1] E. A. Ray, J. Rozen, S. Dhar, J. R. Williams, and L. C. Feldman, *Journal of Applied Physics* **103**, 023522 (2008).

[2] E. H. Nicollian and J. R. Brews, *Metal Oxide Semiconductor, Physics and Technology*, Wiley-Interscience, New-York, 1982.

[3] B. E. Deal and A. S. Grove, *Journal of Applied Physics* **36**, 3770 (1965).

[4] H. Z. Massoud, J. D. Plummer, and E. A. Irene, *Journal of The Electrochemical Society* **132**, 1745 (1985).

[5] H. Z. Massoud and J. D. Plummer, *Journal of The Electrochemical Society* **132**, 2685 (1985).

[6] H. Z. Massoud, J. D. Plummer, and E. A. Irene, *Journal of The Electrochemical Society* **132**, 2693 (1985).

[7] S. Dhar, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, *MRS Bulletin* **30**, 288 (2005).

[8] H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, *Journal of Applied Physics* **76**, 1363 (1994).

[9] Y. S. Park, editor, *SiC Materials and Devices*, Academic Press London, 1998.

[10] Y. Song, S. Dhar, L. C. Feldman, G. Chung, and J. R. Williams, *Journal of Applied Physics* **95**, 4953 (2004).

[11] M. Di Ventra and S. T. Pantelides, *Physical Review Letters* **83**, 1624 (1999).

[12] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, *Physical Review B* **71**, 235321 (2005).

[13] S. T. Pantelides, S. Wang, A. Franceschetti, R. Buczko, M. Di Ventra, S. N. Raashkeev, L. Tsetseris, M. H. Evans, I. G. Batyrev, L. C. Feldman, et al., *Materials Science Forum* **527**, 935 (2006).

[14] A. Rys, N. Singh, and M. Cameron, *Journal of the Electrochemical Society* **142**, 1318 (1995).

[15] K. Kakubari, R. Kuboki, Y. Hijikita, H. Yaguchi, and S. Yoshida, *Materials Science Forum* **527**, 1031 (2006).

[16] Z. Zheng, R. E. Tressler, and K. E. Spear, *Journal of The Electrochemical Society* **137**, 854 (1990).

[17] Z. Zheng, R. E. Tressler, and K. E. Spear, *Journal of The Electrochemical Society* **137**, 2812 (1990).

[18] J. A. Costello and R. E. Tressler, *Journal of the American Ceramic Society* **69**, 674 (1986).

[19] I. C. Vickridge, D. Tromson, I. Trimaille, J. J. Ganem, E. Szilágyi, and G. Battistig, *Nuclear Instruments and Methods in Physics Research B* **190**, 574 (2002).

[20] M. K. Das, B. A. Hull, S. Krishnaswami, F. Husna, S. Haney, A. Lelis, C. J. Scozzie, and J. D. Scofield, *Materials Science Forum* **527-529**, 967 (2006).

[21] G. Gudjonsson, H. O. Olafsson, F. Allerstam, P. A. Nilsson, E. O. Sveinbjornsson, H. Zirath, T. Rodle, and R. Jos, *IEEE Electron Device Letters* **26**, 96 (2005).

[22] F. Allerstam, G. Gudjónsson, H. Ö. Ólafsson, E. Ö. Sveinbjörnsson, T. Rödle, and R. Jos, *Semiconductor Science and Technology* **22**, 307 (2007).

[23] E. Ö. Sveinbjörnsson, G. Gudjonsson, F. Allerstam, H. Ö. Ólafsson, P.-Å. Nilsson, H. Zirath, T. Rödle, and R. Jos, *Materials Science Forum* **527**, 961 (2006).

[24] T. Yamamoto, Y. Hijikata, H. Yagushi, and S. Yoshida, *Japanese Journal of Applied Physics* **46**, L770 (2007).

[25] H. Z. Massoud and J. D. Plummer, *Journal of Applied Physics* **62**, 3416 (1987).

[26] H. Z. Massoud, *Solid State Electronics* **41**, 929 (1997).

[27] M. Uematsu, H. Kageshima, and K. Shiraishi, *Journal of Applied Physics* **89**, 1948 (2001).

[28] T. Watanabe, K. Tatsumura, and I. Ohdomari, *Physical Review Letters* **96**, 196102 (2006).

[29] J. Gass, H. H. Müller, H. Stüssi, and S. Schweitzer, *Journal of Applied Physics* **51**, 2030 (1980).

[30] M. Di Ventra and S. T. Pantelides, *Journal of Electronic Materials* **29**, 353 (2000).

[31] Y. J. Van der Meulen, *Journal of the Electrochemical Society* **119**, 530 (1972).

[32] L. N. Lie, R. R. Razouk, and B. E. Deal, *Journal of The Electrochemical Society* **129**, 2828 (1982).

[33] H. Kageshima, K. Shiraishi, and U. M., *Japanese Journal of Applied Physics* **38**, L971 (1999).

[34] R. Ghez and Y. J. van der Meulen, *Journal of The Electrochemical Society* **119**, 1100 (1972).

[35] M. Uematsu, H. Kageshima, and K. Shiraishi, *Japanese Journal of Applied Physics* **39**, L952 (2000).

# CHAPTER IV

# SUPPRESSION OF ELECTRON-INDUCED INTERFACE STATE GENERATION IN NITRIDED $SiO_2$ ON SiC

## Overview

The flatband voltage stability of $SiO_2$/SiC MOS capacitors upon electron injection can be enhanced by the introduction of nitrogen in a thermal gate oxide. In this chapter, it is shown that it originates from the suppression of negative charge buildup in interface states during injection. The role of nitrogen in this effect, and how it might be linked to the passivation of interface defects, is then discussed.

The content of this chapter has been published in Applied Physics Letters.[1]

## 4.1 Motivation

Among wide band-gap semiconductors that can be used in high-power devices, silicon carbide stands out as one of the most promising materials because, like silicon, it has a stable native oxide, namely $SiO_2$. However, the poor quality of the as-grown $SiO_2$/4H-SiC interface results in an inversion mobility that is two orders of magnitude smaller than the bulk mobility. As explained in Chapter I (Section 1.3.3), this reduction has been attributed to the complexity of the interface and to the resulting large number of defect levels in the energy gap.[2,3,4,5,6,7] It was also mentioned that the incorporation of nitrogen greatly decreases the density of interface states,[6,7,8,9,10,11,12,13,14] subsequently enhancing device performance.

Another benefit of nitridation is that it can lead to improved reliability.[15,16,17,18] Indeed, negative charge buildup upon electron injection is much less pronounced in nitrided oxides than in unpassivated oxides where most of the charge is thought to be trapped in generated acceptor states.[19,20,21] Further progress requires understanding of the impact that the

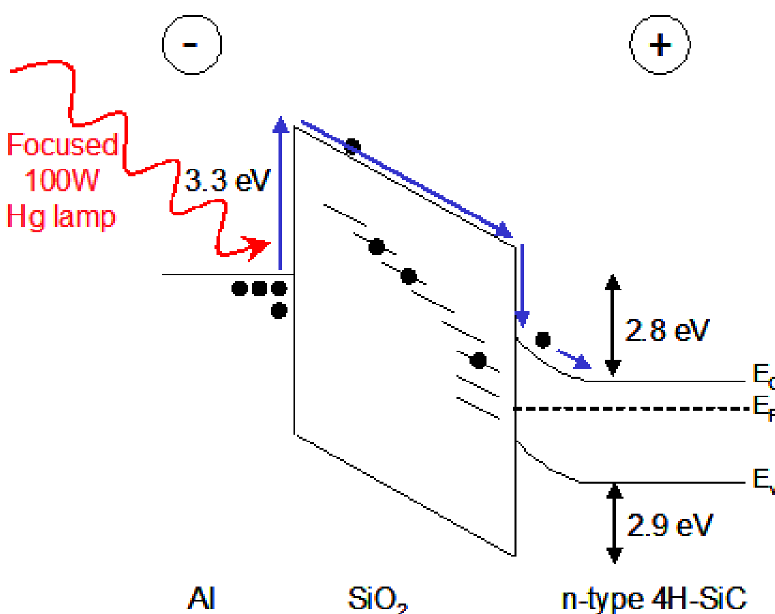



**Figure 4.1:** Schematic of the electron injection conditions and of the resulting charge trapping in the bulk of $SiO_2$ and at the $SiO_2$/SiC interface. The energy values refer to the relevant band offsets between the metal, the insulator and the semiconductor.

passivating nitrogen has on the aging of SiC-based devices.

In this chapter, it is shown that the origin of the nitrogen-induced reliability improvement lies in the suppression of interface state generation upon electron injection into NO-annealed oxides. The results are discussed in terms of specific defects responsible for negative charge trapping in the as-grown oxides and the ability for nitrogen to passivate them.

### 4.2 Experiment

Oxides were grown on the Si-face of n-type ($5\times10^{15}$ cm$^{-3}$ N doping) 4H-SiC wafers purchased from Cree Inc. The RCA cleaning sequence was performed prior to the oxidation in dry $O_2$ at 1150 °C for 4.5 or 8 hours, yielding $SiO_2$ thicknesses of 40 and 60 nm respectively. The samples were then annealed in Ar for 30 minutes. One of the thicker oxides was subsequently passivated in NO at 1175 °C for 2 hours. Finally, semi-transparent Al electrodes, having a 500 $\mu$m diameter and a thickness less than 30 nm, were evaporated onto the oxides.

Internal photoemission, described in Chapter II (section 2.3.5), was used to inject electrons from the metal at a current density of approximately 5 $10^{-7}$ A/cm$^2$ using focused radiation of a 100 W mercury lamp (see Figure 4.1). The applied oxide field necessary to achieve the injection under these conditions was less than -2 MV/cm. The flatband voltage variation and the density of interface states (between 0.2 and 0.6 eV below the SiC conduction band edge)[22] were monitored through simultaneous quasi-static and high-frequency (100 kHz) capacitance-voltage (CV) measurements,[23] as described in Section 2.4, using a Keithley Model 82 CV system.

The hysteresis of the high-frequency CV curves was used to detect the energetically deep interface states and the slow border states. The CV trace is obtained using the following sequence. The semiconductor interface is first driven from accumulation into deep depletion. Then, the capacitors are exposed to a low intensity UV-light pulse leading to the formation of an inversion layer and to the detrapping of deep/slow states by hole capture.[24] Finally, the semiconductor surface potential is swept from depletion towards accumulation.

More details on the oxidation station and on the CV setup can be found in Appendices A and B.

## 4.3 Results

The effective charge density per unit area $N_{eff}$ trapped upon injection is calculated from the flatband voltage shift $\Delta V_{fb}$ using the relation $N_{eff} = C_{ox}\,\Delta V_{fb}/q$ [from Eq.(2.48)] and is plotted in Figure 4.2 for the different samples; $C_{ox}$ is the oxide capacitance per unit area and $q$ is the elementary charge.

The different trapping rates of the two unpassivated oxides for doses below $2{\times}10^{16}$ cm$^{-2}$ reveal the contribution of bulk electron traps. For larger doses, the similar slopes indicate a thickness independent electron trapping phenomenon occurring at the interface. Therefore, the effective charge can be expressed by $N_{eff} = N_{ot} + N_{it}$ to include the bulk ($ot$) and interface contributions ($it$). Assuming a single process in the dielectric, both the cross

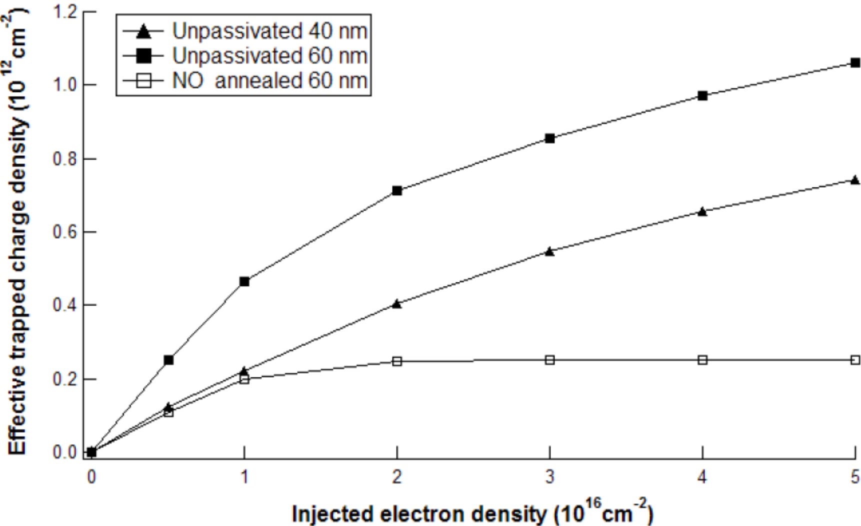



**Figure 4.2:** Effective density of trapped charge, deduced from the flatband voltage shift, as a function of the injected electron density. The trapped charge saturates in the nitrided oxide.

section $\sigma_{ot}$ and the effective density of oxide traps per unit area $N^*_{ot}$ can be deduced from first order kinetics (see Section 2.2.3);

$$N_{eff}[\rho_e] \;=\; N^*_{ot}\,(1 - e^{-\rho_e \sigma_{ot}}) \;+\; N_{it}[\rho_e] \tag{4.1}$$

where $\rho_e$ is the injected charge density and $N_{it}[\rho_e]$ describes the trapping occurring at the interface. Noticing that only the first term of Eq.(4.1) is thickness dependent, one finds that the difference between the effective trapped charge densities in the two unpassivated oxides (40 and 60 nm) directly scales with

$$\Delta N_{eff} \;\propto\; (1 - e^{-\rho_e \sigma_{ot}}) \tag{4.2}$$

regardless of the positions of the bulk-trapped charge centroids which yield the proportionality constant. From Eq.(4.2), the cross section is estimated to be $\sigma_{ot} \;\simeq\; 1.3{\times}10^{-16}$ cm$^2$.

(a) Unpassivated oxide

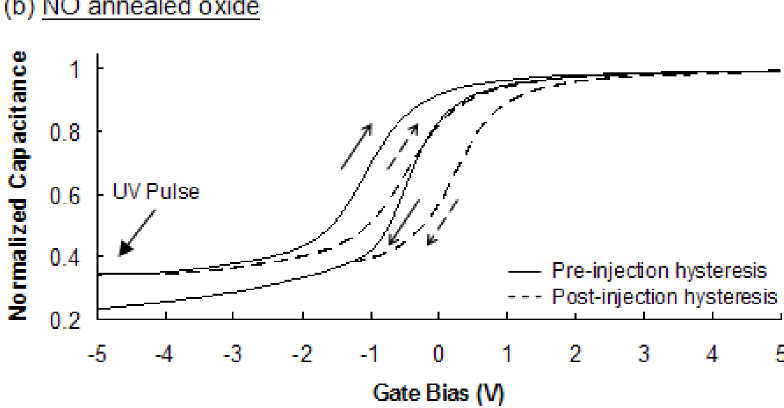



**Figure 4.3:** CV hysteresis of the 60 nm unpassivated (a) and nitrided (b) oxides before and after injection of 5 $10^{16}$ electrons per $cm^2$. The constant hysteresis width observed in panel (b) shows that interface states are not generated in the nitrided sample.

The CV hysteresis before and after electron injection [shown in Figure 4.3(a)], indicates that some of the trapped negative charge can be released upon creation of an inversion layer, revealing its proximity to the interface. Also, the fact that the post-injection hysteresis can be cycled, and is wider than the initial one, indicates that there is a new/different trap level that can be occupied by electrons. Finally, because the hysteresis widening occurs towards positive voltages, these traps are identified as acceptor states.

Using the width of the hysteresis to deduce the apparent increase in interface states in both of the unpassivated samples, it is found that $N_{it}$ approaches $10^{12}$ $cm^{-2}$ for the larger doses. This result is consistent with the previously reported values and proves that a large part of the observed voltage shift is related to the trapping in generated interface states.

Note that the density of interface states with levels between 0.2 eV and 0.6 eV is also enhanced by electron injection. This results in a change of the CV curve stretch-out. However, the increase in the density of fast states is at most $10^{11}$ cm$^{-2}$ for the doses used, and does not contribute to the hysteresis, which is mostly sensitive to deep interface states and slow border states.

It is clear that the net electron trapping in the 60 nm nitrided oxide is greatly reduced. Also, there is a saturation of the captured charge for doses above $2\times10^{16}$ cm$^{-2}$, suggesting the absence of interface state buildup. Moreover, the curve can be fitted by a single exponential [first term of Eq.(4.1)], which yields $N_{ot}^{*} \simeq 2.4\times10^{11}$ cm$^{-2}$ and $\sigma_{ot} \simeq 1.9\times10^{-16}$ cm$^{2}$. This capture cross section is close to the one found for the unpassivated samples, which suggests that the trapping still occurs in the bulk of the oxide but not at the $SiO_2$/SiC interface.

The evolution of the hysteresis shown in Figure 4.3(b) confirms this hypothesis since its width remains constant during injection, indicating that no additional interface traps are generated by the injected electrons. The CV curve shift is caused by the negative charge trapped in the bulk of the oxide.

### 4.4 Discussion

The fact that the density of states does not increase in the NO-annealed samples during electron injection is an indication that the degradation of unpassivated interfaces is related to precursor defects. It is clearly of interest to seek a specific atomic level configuration that can display such a behavior. This precursor state has to meet four criteria; (i) it must occur in the $SiO_2$/SiC interfacial region as evidenced by the CV hysteresis, (ii) it must be passivated in the presence of NO at 1175 °C, (iii) it must result in an energy level within the gap of 4H-SiC when exposed to flowing low-energy electrons, (iv) the induced state cannot be readily passivated by $H_2$ at 400 °C as shown by Afanas'ev *et al.*[21]

As mentioned in Chapter II (Section 2.2.4), an analogous behavior during electron in-

**Table 4.1:** Some defects predicted by theory to relax upon electron capture and their ability to be passivated by nitrogen. The induced energy levels are measured from the conduction band edge of 4H-SiC.

| *Precursor defect* | Trivalent Oxygen | Single C interstitial | Pair of C interstitials |
|---|---|---|---|
| *Induced level (eV)* | 0.6[a] | 0.3 | <0.1 |
| *N passivated* | Yes[a] | Yes | Yes |
| *References* | | 6 | 3,13 |

jection has been observed in silicon devices passivated with hydrogen. In that case, flowing electrons induce the release of the passivating species, leaving dangling bonds as "new" interface states.[25] Here, the degradation of the as-oxidized, unpassivated $SiO_2$/SiC interface is observed. Also, silicon-like $P_b$ centers (Si dangling bonds) have not yet been identified at the studied (0001) SiC surfaces. There is some evidence for carbon dangling bonds from paramagnetic resonance techniques, they result in C-H bonds after intentional hydrogen passivation.[26] It is therefore possible that the effects of electron injection reported here is not associated with adventitious hydrogen bond-breaking.

Instead, it is envisioned that when the unpassivated $SiO_2$/SiC interface is exposed to a low-energy electron flow, some defects trap a negative charge and then relax to a more stable configuration, generating an acceptor state that can be detected by subsequent measurements without being affected by the probing charge exchange. Accordingly, defects that have been suggested by theory to meet the criteria listed above are now considered. Detailed computational studies on defect relaxation have been published by Wang *et al.*[7] and Knaup *et al.*[4,14] Additional simulations have been performed for this study, following

the method described in a previous publication.[7] Table 4.1 lists three defects that, according to calculations, could occur at the interface, have originally no level within the gap of 4H-SiC, and are predicted to relax upon electron capture. The calculated states resulting from the trapping of one electron (trivalent oxygen and single carbon interstitial) or four electrons (pair of carbon interstitials) are reported, all appear in the SiC band gap. Moreover, the listed defects are thought to be prone to nitrogen passivation. Of course, each of these configurations requires further examination. In particular, it should be noted that no relationship between fixed positive charge, which we expect to be associated with trivalent oxygen, and electron trapping has been observed.[27] Also, the capture of four electrons, predicted to lead to the relaxation of the pair of carbon interstitials, is likely to be a low-probability event. Further theoretical and experimental work is needed to clearly identify the pertinent atomic configuration.

### 4.5 Summary

In conclusion, it has been shown in this chapter that the reduced negative charge trapping upon electron injection in nitrided oxides on 4H-SiC correlates with the absence of interface state generation. In unpassivated oxides, the resulting charge buildup could be due to the trapping of electrons in meta-stable defects and to the transition of the levels to within the gap after relaxation. Nitrogen is thought to passivate these defects, thus improving the reliability of the NO-annealed oxides.

Further insight on the role of nitrogen in this effect can be found in Chapter VI, where the dependence of interface state generation on the N density is reported.

### References


[1] J. Rozen, S. Dhar, S. Wang, S. T. Pantelides, V. V. Afanas'ev, J. R. Williams, and L. C. Feldman, *Applied Physics Letters* **91**, 153503 (2007).

[2] V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans, *Journal of Physics: Condensed Matter* **16**, S1839 (2004).

[3] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, *Physical Review B* **71**, 235321 (2005).

[4] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, *Physical Review B* **72**, 115323 (2005).

[5] S. Wang, M. Di Ventra, S. G. Kim, and S. T. Pantelides, *Physical Review Letters* **86**, 5946 (2001).

[6] S. T. Pantelides, S. Wang, A. Franceschetti, R. Buczko, M. Di Ventra, S. N. Raashkeev, L. Tsetseris, M. H. Evans, I. G. Batyrev, L. C. Feldman, et al., *Materials Science Forum* **527**, 935 (2006).

[7] S. Wang, S. Dhar, S.-r. Wang, A. C. Ahyi, A. Franceschetti, J. R. Williams, L. C. Feldman, and S. T. Pantelides, *Physical Review Letters* **98**, 026101 (2007).

[8] H. Li, S. Dimitrijev, D. Sweatman, H. B. Harrison, P. Tanner, and B. Feil, *Journal of Applied Physics* **86**, 4316 (1999).

[9] S. Dimitrijev, P. Tanner, and H. B. Harrison, *Microelectronics Reliability* **39**, 441 (1999).

[10] P. Jamet, S. Dimitrijev, and P. Tanner, *Journal of Applied Physics* **90**, 5058 (2001).

[11] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. D. Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, *Applied Physics Letters* **76**, 1713 (2000).

[12] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, *Applied Physics Letters* **82**, 568 (2003).

[13] K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2719 (2003).

[14] P. Deák, T. Hornos, C. Thill, J. M. Knaup, A. Gali, and T. Frauenheim, *Materials Science Forum* **556-557**, 541 (2007).

[15] H. F. Li, S. Dimitrijev, and H. B. Harrison, *IEEE Electron Device Letters* **19**, 279 (1998).

[16] H. Li, S. Dimitrijev, D. Sweatman, and H. B. Harrison, *Microelectronics Reliability* **40**, 283 (2000).

[17] J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, *IEEE Electron Device Letters* **21**, 298 (2000).

[18] S. Chakraborty, P. T. Lai, and P. C. K. Kwok, *Microelectronics Reliability* **42**, 455 (2002).

[19] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. J. Schulz, *Microelectronic Engineering* **28**, 197 (1995).

[20] E. G. S. von Kamienski, F. Portheine, J. Stein, A. Golz, and H. Kurz, *Journal of Applied Physics* **79**, 2529 (1996).

[21] V. V. Afanas'ev, A. Stesmans, M. Bassler, G. Pensl, M. J. Schulz, and C. I. Harris, *Journal of Applied Physics* **85**, 8292 (1999).

[22] J. A. Cooper Jr., *Physica Status Solidi (A), Applied Research* **162**, 305 (1997).

[23] E. H. Nicollian and J. R. Brews, *Metal Oxide Semiconductor, Physics and Technology*, Wiley-Interscience, New-York, 1982.

[24] A. Goetzberger and J. C. Irvin, *IEEE transactions on Electron Devices* **15**, 1009 (1968).

[25] J. H. Stathis and D. J. DiMaria, *Applied Physics Letters* **61**, 2887 (1992).

[26] J. L. Cantin, H. J. von Bardeleben, Y. Shishkin, Y. Ke, R. P. Devaty, and W. J. Choyke, *Physical Review Letters* **92**, 15502 (2004).

[27] V. V. Afanas'ev and A. Stesmans, *Physical Review Letters* **80**, 5176 (1998).

# CHAPTER V

# INCREASE IN OXIDE HOLE TRAP DENSITY ASSOCIATED WITH NITROGEN INCORPORATION AT THE $SiO_2$/SiC INTERFACE

## Overview

Nitrogen incorporation at the $SiO_2$/SiC interface via high temperature NO annealing leads to the passivation of electrically active interface defects, yielding improved inversion mobility in the semiconductor. However, it is shown here that such nitrided oxides can possess a larger density of hole traps than as-grown oxides, which is detrimental to the reliability of devices (e.g. can lead to large threshold voltage instabilities and to accelerated failure). Three different charge injection techniques are used to characterize this phenomenon in metal-oxide-semiconductor structures: X-ray irradiation, internal photoemission and Fowler-Nordheim tunneling. Some nitrogen-based atomic configurations that could act as hole traps in nitrided $SiO_2$ on SiC are discussed based on first-principles density functional calculations.

The content of this chapter has been accepted for publication in the Journal of Applied Physics.[1]

## 5.1 Motivation

As reviewed in Chapter I, silicon carbide receives considerable attention for its potential use in high-power devices due to its high achievable blocking voltages and good thermal conductivity, making it superior to Si for a wide range of such applications. It is also preferred over other wide band-gap semiconductors because of its unique ability to grow a thermal $SiO_2$ gate oxide. A significant stepping-stone towards the feasibility of SiC metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been the incorporation of nitrogen

in the gate dielectric via post-oxidation anneals which yields a tenfold reduction of electrically active defects at the complex $SiO_2$/4H-SiC interface and a significant increase in channel mobility (see Section 1.3.3). Although the atomic-scale mechanisms remain unclear, this effect has been attributed to the removal of threefold coordinated excess carbon and to the passivation of suboxide bonds.[2,3,4,5,6,7,8,9]

Following this improvement, it is important to study the impact of nitrogen on the reliability of the gate oxide and of the $SiO_2$/SiC interface. In particular, oxide charge buildup during device operation, yielding threshold voltage instabilities in MOSFETs and ultimately inducing oxide breakdown, is a major concern inherent to the properties of the wide band-gap semiconductor. Indeed, the band offsets of SiC with respect to $SiO_2$ are smaller than in the case of silicon which leads to a more efficient charge injection into the oxide under similar operation conditions.[10] Moreover, it has been shown that hole emission from SiC is mediated by some states in the oxide band-gap resulting in an even lower effective energy barrier.[11] Furthermore, as described in Chapter II (Section 2.3), the use of power devices at higher fields and temperatures increases the tunneling and thermal emission probabilities of carriers not only from the semiconductor but from the gate metal as well.[12] The characterization of the impact of injected charges on the oxide and the $SiO_2$/SiC interface after nitrogen incorporation is therefore crucial to the establishment of SiC MOSFETs as commercial devices. Ideally, this should be understood at the atomic level and in terms of nitrogen bonding configurations.

In the previous chapter, it was shown that oxides subjected to high temperature nitric oxide (NO) annealing do not result in the generation of interface states upon electron injection, a process which is observed in as-grown oxides.[13] This explains results previously observed by research groups which reported the enhanced negative charge buildup in as-grown oxides when compared to nitrided oxides under such conditions.[14,15,16]

In this chapter, the responses of NO-annealed and as-grown oxides exposed to holes injected via three different techniques are compared and it is found that nitrogen incorporation

can be detrimental to the reliability of oxide-based devices. The nature of the enhanced net positive charge buildup in nitrided samples observed following X-ray irradiation[17] is interpreted as promoted hole trapping based on results from metal-oxide-semiconductor (MOS) structures subjected to internal photoemission and Fowler-Nordheim tunneling. The total deposited charge and the amount of generated interface states are deduced from capacitance-voltage (CV) measurements. Charge annealing results in the neutralization of the trapped charge and in the removal of the generated (near-) interface states. Defects responsible for such behavior are considered and the role of nitrogen is discussed in light of first-principles calculations.

## 5.2 Experimental and Theoretical Methods

For these experiments, 35 to 60 nm thick oxides were grown at 1150 °C in flowing oxygen on the (0001) Si-face of RCA cleaned n-type and p-type 4H-SiC wafers (doping $\simeq 5\times10^{15}$ cm$^{-3}$) obtained from Cree, Inc. The samples were then annealed for 30 min in argon at the same temperature. Some were subsequently exposed to NO for 2 hours at 1175 °C. The oxidation setup is described in Appendix A.

X-ray irradiation was performed using a 10 keV source while a positive bias ($\xi_{ox} \simeq$ 1.5 MV/cm) was maintained on the DC sputtered 200 nm thick Mo/Au metal gate stacks. In Chapter II (section 2.3.6) it was explained that, under these conditions, electron-hole (e-h) pairs are induced in the oxide by secondary photo-electrons from the metal and the semiconductor, and by direct interaction of X-ray photons with $SiO_2$. Accordingly, 1 Mrad ($SiO_2$) is estimated to generate about $10^{14}$ e-h pairs in the oxide, the majority of which (about 70%) do not recombine as they are effectively separated by the electric field. An oxide field of similar amplitude ($\xi_{ox} \simeq 1.5$ MV/cm) was used for the devices subjected, under $N_2$ ambient, to 10 eV (vacuum ultraviolet, VUV) photons emitted by a Kr resonant discharge lamp through a $MgF_2$ window; those samples had semi-transparent (15 nm thick) evaporated Au electrodes. To selectively inject holes in a third set of devices, advantage

was taken of the small band offset between the 4H-SiC and $SiO_2$ valence bands ($\simeq$ 2.9 eV vs. 4.7 eV in the case of Si) and of the reduced effective barrier yielding the onset of Fowler-Nordheim hole tunneling observed in p-type samples at approximately -6 MV/cm.[11,18] The reader is referred to Chapter II (Section 2.3.4) for more details on this injection mechanism. Here, a low intensity UV-light (< 3.5 eV) was used to generate an inversion layer, source of tunneling holes, in the negatively biased n-type substrates. Those samples had thin Al (< 30 nm) evaporated gate contacts.

Two methods were used to neutralize the trapped positive charge: isochronal annealing and electron injection. Isochronal annealing was performed under positive bias ($\xi_{ox} \simeq$ 1.5 MV/cm) using 10 minute steps at temperatures between 25 °C and 175 °C. As in the previous study (Chapter IV), electrons were injected at low fields (< 3 MV/cm) using the focused radiation of a 100 W mercury lamp to emit free carriers from the semi-transparent metal gate (see details on internal photoemission in Section 2.3.5). The large attractive Coulomb neutralization cross section of trapped holes in $SiO_2$ allowed for a limited electron dose, assuring no significant background trapping of negative charge.[19]

All CV measurements were performed at room temperature using a Keithley model 82 or a HP 4275A LCR meter. The change in effective charge was deduced from shifts in the flatband voltages ($V_{fb}$) of the CV curves taken from accumulation to deep depletion [Eq.(2.48)]. The density of interface states ($D_{it}$), between 0.2 and 0.6 eV from the SiC band edges, was monitored through simultaneous quasi-static and high-frequency (100 kHz) CV,[20] as described in Section 2.4.4. Like in the study presented in Chapter IV, the hysteresis of the high-frequency curves was measured to detect energetically deep interface states and slow border states as a low intensity UV-light pulse was used to form an inversion layer prior to the sweep towards accumulation.[21]

First-principles calculations were performed by applying density-functional theory, with the pseudopotential method,[22,23,24] to supercells representing a $SiO_2$/4H-SiC interface,[2] or amorphous $SiO_2$.[25] The exchange-correlation effects were treated with the generalized

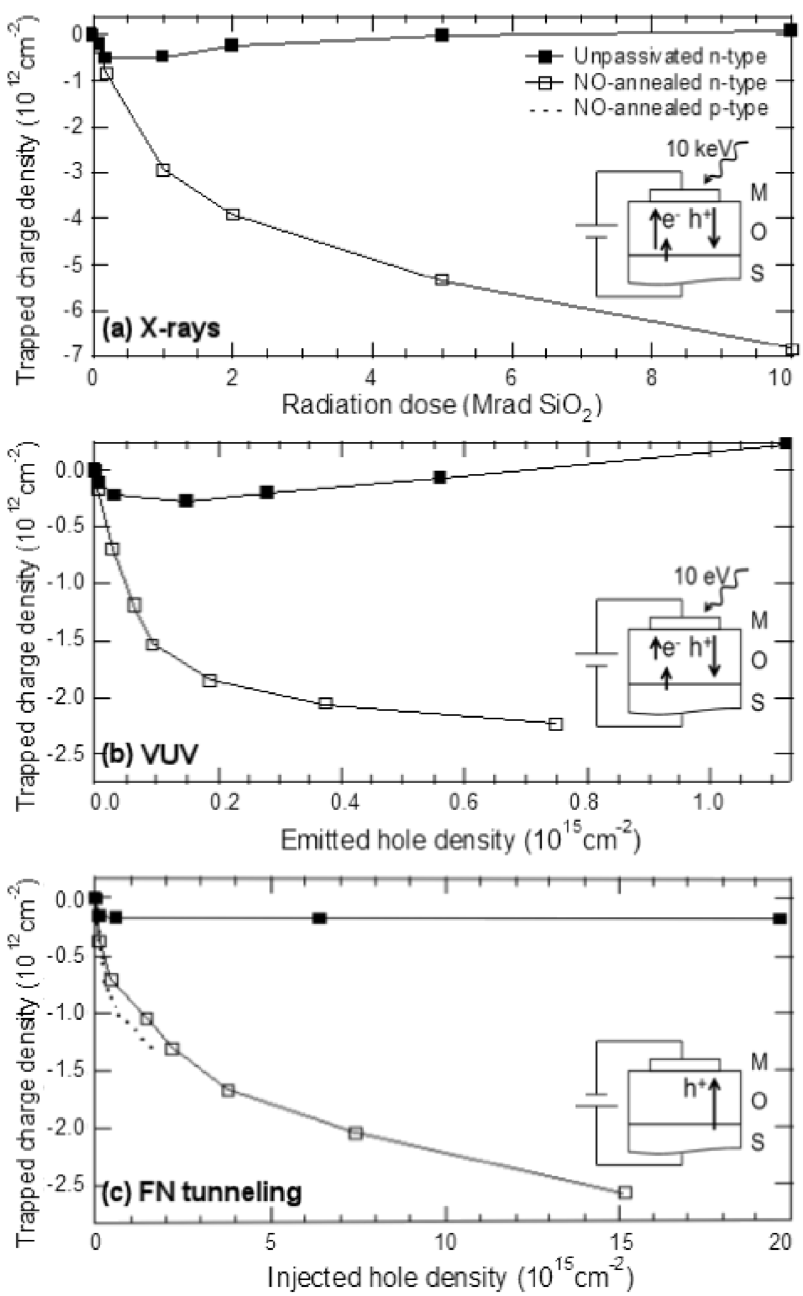



**Figure 5.1:** Effective charge density trapped upon carrier injection by three different techniques; (a) 10 keV X-rays under positive gate bias, $\xi_{ox} \simeq 1.5\,\text{MV/cm}$, (b) 10 eV VUV photons under positive gate bias, $\xi_{ox} \simeq 1.5\,\text{MV/cm}$, and (c) Fowler-Nordheim tunneling under negative gate bias, $\xi_{ox} \simeq -6\,\text{MV/cm}$. The trapped charge density is calculated as $\Delta V_{fb}\, C_{ox}/q$, where $C_{ox}$ is the oxide capacitance and $q$ is the elementary charge; negative values imply net positive charge trapping.

gradient-corrected exchange-correlation functionals given by Perdew and co-workers.[26] The Vanderbilt ultrasoft pseudopotentials were adopted. A plane-wave energy cutoff of 396 eV and the Γ point in the Brillouin zone were used for the calculations. Relaxation of the atomic structures was performed for each configuration via a conjugate-gradient technique using the total energy and the Hellmann-Feynman forces on the atoms.[22] While all the atoms in the supercells representing amorphous $SiO_2$ and defects were fully relaxed, only the $SiO_2$ layer and the top four SiC layers for the structures involving the $SiO_2$/4H-SiC interface were relaxed. The equilibrium configurations were assumed when the forces on the atoms were smaller than 0.05 eV/Å.

## 5.3 Results

### 5.3.1 Hole Injection

The effective trapped charge density resulting from the different injection techniques is shown in Figure 5.1. It is clear that in all cases the nitrided samples exhibit a larger net positive trapping. The turn-around behavior observed in as-oxidized samples [Figure 5.1(a) and 5.1(b)] reveals the presence of background electron trapping which yields charge compensation. Indeed, the trapping of negative charge in the bulk of the oxide, and/or the generation of interface acceptor states, can counter-balance the positive charge deposited by holes. Therefore, the sources of electrons must be identified and the background trapping must be quantified in order to highlight the response of the oxide relative to holes alone.

*X-rays* generate electron-hole pairs throughout the oxide.[27,20] The positive bias drives the holes to the semiconductor interface as electrons are swept towards the metal. Therefore, some negative charge trapping should be expected. Post-irradiation (10 Mrad $SiO_2$) isochronal anneals lead to the neutralization of the positive charge.[17] The remaining negative charge due to background effects has been estimated to be approximately $2\times10^{12}$ cm$^{-2}$ in as-oxidized samples and $9\times10^{11}$ cm$^{-2}$ in nitrided samples.

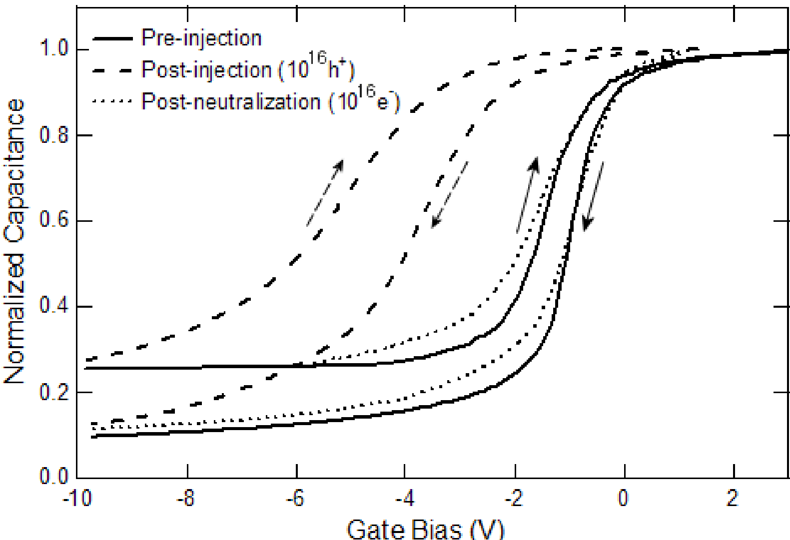



**Figure 5.2:** Evolution of the photo-CV hysteresis of a NO-annealed n-type sample. A low intensity UV pulse was applied at -10 V, prior to the sweep towards accumulation, in order to form an inversion layer and empty deep/slow states.

*Kr lamp 10 eV photons* are mostly absorbed in a thin oxide layer beneath the metal ($SiO_2$ skin depth at this energy is approximately 10 nm),[28,29] which implies that most electrons finding their way to the $SiO_2$/SiC interface are the ones tunneling from the n-type semiconductor in accumulation.[30] This background effect is quantified by biasing the samples in the dark; this yields the trapping of at most $2\times10^{11}$ electrons/cm$^2$ in all samples within the time frame of the experiments (see Figure 2.9, Section 2.3.1).

*Fowler-Nordheim tunneling* is performed with a negative bias on the gate ($\xi_{ox} \simeq -6\,\text{MV/cm}$). This field is insufficient to inject electrons from the metal,[11] or to induce hot carriers in the oxide.[31] Moreover, the absence of a turn-around in the unpassivated sample [Figure 5.1(c)] confirms that there are no compensating electrons.

It is concluded that in the case of X-rays and 10 eV photons, the amount of positive trapped charge in as-oxidized samples is of the same order as the negative one and that there is no background effect due to electrons in the samples subject to Fowler-Nordheim tunneling. In all cases, the net positive trapped charge in nitrided capacitors by far exceeds the compensating negative charge which indeed means that the NO-annealed oxides trap holes more efficiently. Also, from the evolution of the CV stretch-out,[17] and of the photo-CV

hysteresis width (Figure 5.2), it is deduced that states are generated as well. Since no such increase in the $D_{it}$ between 0.2 eV and 0.6 eV from the semiconductor band edges could be detected, it is inferred that mostly deep states and/or border states are generated. Note that these induced states also lead to larger flatband voltage shifts in the nitrided p-type sample shown in Figure 5.1(c).

### 5.3.2 Charge Annealing

In order to understand the nature of the excess positive charge in nitrided samples, post-injection charge annealing was performed. Isochronal annealing leads to the removal of positive charges via the thermal emission of holes.[32,33] The emission probability at each temperature $p^*_{em}[T]$ is calculated from flatband voltage shifts of NO-annealed capacitors,

$$p^*_{em}[T] \; = \; \frac{Q^*_{trap}[T - \Delta T] - Q^*_{trap}[T]}{Q^*_{trap}[T - \Delta T]} \tag{5.1}$$

where $Q^*_{trap}[T] = Q_{trap}[T, \Delta T, \Delta t]$ is the remaining positive trapped charge density measured after each temperature step $\Delta T$ (i.e. 25°C) of duration $\Delta t$ (i.e. 10 min). Assuming that the charge annealing occurs predominantly via thermal emission of holes (even at room temperature, no significant neutralization by electrons tunneling from the semiconductor into positively charged states was detected within $\Delta t$),

$$p^*_{em}[T] \; \equiv \; \Delta t \, e_{th}[T] \; \propto \; \Delta t \; T^2 \, e^{-E_a/kT} \tag{5.2}$$

where $e_{th}$ is the thermal emission rate at equilibrium. It yields an activation energy $E_a$ of approximately 0.3 eV [Figure 5.3(a)]. If holes emit only into the oxide valence band, this energy corresponds to an effective trap energy level relative to the valence band edge of $SiO_2$. This suggests that at least some of the trap states induced by nitrogen incorporation are located within the valence band of SiC. Also, it is seen that positive charge neutralization is completed at 150 °C and that the use of devices around (or above) that temperature might prevent the observed charge buildup.

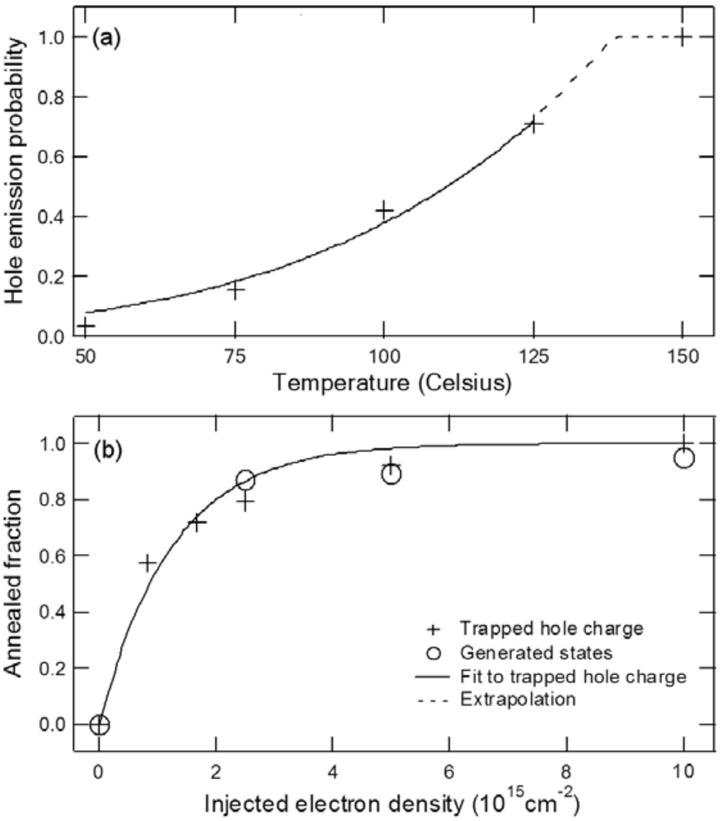



**Figure 5.3:** Positive charge annealing in NO-treated capacitors. (a) Probability of hole emission as a function of temperature deduced from flatband recovery during isochronal annealing. (b) Fraction of the positive charge and of the generated states annealed as a function of the injected electron density.

Another way to remove the positive charge accumulated after hole injection is to inject electrons. The dose dependence of the annealed charge fraction $F_a$ in nitrided samples, exposed to photo-injected electrons ($|\xi_{ox}| < 3\,\mathrm{MV/cm}$), is shown in Figure 5.3(b);

$$F_a[t] \, = \, 1 - \frac{Q_{trap}[t]}{Q_{trap}[t=0]} \tag{5.3}$$

where $Q_{trap}[t]$ is the remaining positive trapped charge after injecting the oxide with electrons for a time $t$. Eq (5.3) can be used to estimate the neutralization cross-section $\sigma$, assuming a single-process rate equation (field-induced detrapping was not observed at 1.5 MV/cm);

$$F_a[t] \, \equiv \, (1 - e^{-Jt\sigma}) \tag{5.4}$$

where $J$ is the current density of electrons (see derivation in Section 2.2.3). The value of $\sigma$ is found to be of the order of $8{\times}10^{-16}$ cm$^2$, close to the measured range for hole annihilation cross-sections in $SiO_2$ on Si.[19]

Interestingly, it is observed that the amount of generated switching states, calculated from the photo-CV hysteresis,[34] is also reduced upon charge removal. This is seen in Figure 5.2 where the width and the position of the hysteresis after electron-induced annealing are very close to their pre-injection values. Moreover, the annealing rate of the generated switching states seems to match the one of the positive trapped charge [Figure 5.3(b)]. These observations suggests a correlation between the density of trapped charge and the (near-) interface states generation upon hole injection.

### 5.4 Discussion

The origin of hole trapping in as-oxidized $SiO_2$ on SiC has been previously discussed in terms of E' centers,[35] which are partly responsible for positive charge buildup in $SiO_2$/Si systems,[36] as described in Chapter II (Section 2.2.4). Also, high oxidation temperatures increase the amount of oxygen vacancies (E' precursors) in gate oxides on Si.[37] However, recent electron spin resonance (ESR) experiments, described in the next chapter, indicate that NO annealing of $SiO_2$ grown on SiC does not lead to a higher density of E' precursors, as evidenced by the E' signals measured in X-ray irradiated as-grown and NO-treated oxides.

It is concluded that NO-induced E' centers are not the cause for enhanced hole trapping in nitrided oxides. Alternatively, it is considered how the binding of nitrogen, taking place mostly at the interface (see Chapter VI), might induce atomic configurations having energy levels that can act as hole traps.

Theory suggests that the passivation of the interface is achieved in part by substitution of threefold coordinated carbon atoms by nitrogen which removes the C dangling bond states in the upper part of the SiC band-gap.[2] It also results in doubly occupied levels that are located below the SiC valence band edge, but within the $SiO_2$ band-gap. In addition, a

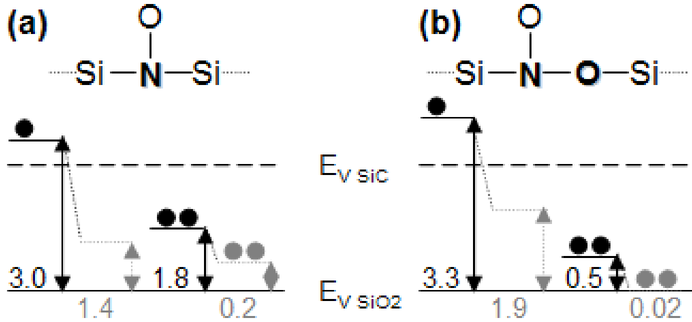



**Figure 5.4:** Configurations resulting from N and NO incorporation in $SiO_2$. The energy of the corresponding levels, are noted in eV. Before trapping (labeled in black), they each have a singly occupied level and a doubly occupied level. The capture of a hole leads to a lowering of the energy states (labeled in grey). The calculated energy levels are adjusted using the experimental value $\simeq$2.9 eV for the valence band offset between 4H-SiC and amorphous $SiO_2$.

threefold nitrogen atom has a singly occupied lone pair state, which is located in the lower part of the SiC band-gap. This state could act as a trap. After capturing a hole, it becomes empty and its energy level moves down towards the $SiO_2$ valence band edge, as does the one of the doubly occupied state. Depending on the nature of the defects and on their distance from the interface, the relaxation, and/or the electric field associated with the capture of a hole, can affect the measured $D_{it}$. This process could explain the results of recent ESR studies which reveal that the excess positive charge in nitrided oxides on Si resides on a silicon atom bonded to some nitrogen atoms in the $SiO_xN_y$ transition layer.[38,39]

Two defect configurations involving N in the oxide are considered here (Figure 5.4). They may be formed when N or NO replaces interstitial C or CO. The one in Figure 4(a) can also be formed when a Si-Si suboxide bond is inserted by NO. Interestingly, these configurations can result from N or NO insertion in an ideal stoichiometric oxide as well, in which case nitrogen generates states (including hole traps) within the $SiO_2$ band-gap previously free of defect levels.

### 5.5 Summary

It has been shown in this chapter that the incorporation of nitrogen in dry oxides grown on SiC via high temperature NO annealing leads to a density of hole traps significantly larger than the one measured in as-grown oxides. A model that correlates this increase with the bonding of nitrogen atoms in the interfacial layer is proposed. Indeed, first-principle calculations suggest that the resulting nitrogen lone pairs of electrons can act as hole traps. For device applications, it is of interest to optimize N incorporation in order to avoid excess nitrogen content over and above that required for defect passivation at the $SiO_2$/SiC interface, so that both interface state density and charge buildup are reduced.

The impact of the N content on the $D_{it}$ and on the density of hole traps is reported in Chapter VI.

### References


[1] J. Rozen, S. Dhar, S. K. Dixit, F. O. Roberts, H. L. Dang, S. Wang, S. T. Pantelides, V. V. Afanas'ev, J. R. Williams, and L. C. Feldman, *Accepted for publication in the Journal of Applied Physics* (2008).

[2] S. Wang, S. Dhar, S.-r. Wang, A. C. Ahyi, A. Franceschetti, J. R. Williams, L. C. Feldman, and S. T. Pantelides, *Physical Review Letters* **98**, 026101 (2007).

[3] H. Li, S. Dimitrijev, D. Sweatman, H. B. Harrison, P. Tanner, and B. Feil, *Journal of Applied Physics* **86**, 4316 (1999).

[4] S. Dimitrijev, P. Tanner, and H. B. Harrison, *Microelectronics Reliability* **39**, 441 (1999).

[5] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. D. Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, *Applied Physics Letters* **76**, 1713 (2000).

[6] P. Jamet, S. Dimitrijev, and P. Tanner, *Journal of Applied Physics* **90**, 5058 (2001).

[7] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, *Applied Physics Letters* **82**, 568 (2003).

[8] K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2719 (2003).

[9] P. Deák, T. Hornos, C. Thill, J. M. Knaup, A. Gali, and T. Frauenheim, *Materials Science Forum* **556-557**, 541 (2007).

[10] V. V. Afanasev, M. Bassler, G. Pensl, M. J. Schulz, and E. S. von Kamienski, *Journal of Applied Physics* **79**, 3108 (1996).

[11] V. V. Afanas'ev and A. Stesmans, *Applied Physics Letters* **77**, 2024 (2000).

[12] R. Singh and A. R. Hefner, *Solid State Electronics* **48**, 1717 (2004).

[13] J. Rozen, S. Dhar, S. Wang, S. T. Pantelides, V. V. Afanas'ev, J. R. Williams, and L. C. Feldman, *Applied Physics Letters* **91**, 153503 (2007).

[14] H. Li, S. Dimitrijev, D. Sweatman, and H. B. Harrison, *Microelectronics Reliability* **40**, 283 (2000).

[15] J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, *IEEE Electron Device Letters* **21**, 298 (2000).

[16] S. Chakraborty, P. T. Lai, and P. C. K. Kwok, *Microelectronics Reliability* **42**, 455 (2002).

[17] S. K. Dixit, S. Dhar, J. Rozen, S. Wang, R. D. Schrimpf, D. M. Fleetwood, S. T. Pantelides, J. R. Williams, and L. C. Feldman, *IEEE Transactions on Nuclear Science* **53**, 3687 (2006).

[18] R. K. Chanana, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, J. R. Williams, and R. A. Weller, *Applied Physics Letters* **77**, 2560 (2000).

[19] D. A. Buchanan, M. V. Fischetti, and D. J. DiMaria, *Physical Review B* **43**, 1471 (1991).

[20] E. H. Nicollian and J. R. Brews, *Metal Oxide Semiconductor, Physics and Technology*, Wiley-Interscience, New-York, 1982.

[21] A. Goetzberger and J. C. Irvin, *IEEE transactions on Electron Devices* **15**, 1009 (1968).

[22] M. C. Payne, M. P. Teter, D. C. Allan, T. A. Arias, and J. D. Joannopoulos, *Review of Modern Physics* **64**, 1045 (1992).

[23] G. Kresse and J. Furthmüller, *Computational Materials Science* **6**, 15 (1996).

[24] D. Vanderbilt, *Physical Review B* **41**, 7892 (1990).

[25] S. Wang, M. Di Ventra, S. G. Kim, and S. T. Pantelides, *Physical Review Letters* **86**, 5946 (2001).

[26] J. P. Perdew, J. A. Chevary, S. H. Vosko, K. A. Jackson, M. R. Pederson, D. J. Singh, and C. Fiolhais, *Physical Review B* **46**, 6671 (1992).

[27] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides*, World Scientific, 1999.

[28] R. J. Powell and G. F. Derbenwick, *IEEE Transactions on Nuclear Science* **18**, 99 (1971).

[29] A. R. Stivers and C. T. Sah, *Journal of Applied Physics* **51**, 6292 (1980).

[30] A. J. Lelis, S. Potbhare, D. Habersat, G. Pennington, and N. Goldsman, *Integrated Reliability Workshop Final Report, 2006 IEEE International* , 160 (2006).

[31] D. Arnold, E. Cartier, and D. J. DiMaria, *Physical Review B* **45**, 1477 (1992).

[32] P. J. McWhorter, S. L. Miller, and W. M. Miller, *IEEE Transactions on Nuclear Science* **37**, 1682 (1990).

[33] V. Danchenko, U. D. Desai, and S. S. Brashears, *Journal of Applied Physics* **39**, 2417 (1968).

[34] V. V. Afanas'ev, A. Stesmans, M. Bassler, G. Pensl, M. J. Schulz, and C. I. Harris, *Journal of Applied Physics* **85**, 8292 (1999).

[35] V. V. Afanasev and A. Stesmans, *Applied Physics Letters* **69**, 2252 (1996).

[36] P. M. Lenahan and P. V. Dressendorfer, *Journal of Applied Physics* **55**, 3495 (1984).

[37] W. L. Warren, D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, P. S. Winokur, R. A. B. Devine, and D. Mathiot, *Applied Physics Letters* **64**, 3452 (1994).

[38] J. P. Campbell, P. M. Lenahan, C. J. Cochrane, A. T. Krishnan, and S. Krishnan, *IEEE Transactions on Device and Materials Reliability* **7**, 540 (2007).

[39] J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Applied Physics Letters* **91**, 133507 (2007).

# CHAPTER VI

# DENSITY OF INTERFACE STATES, ELECTRON TRAPS, AND HOLE TRAPS, AS A FUNCTION OF NITROGEN CONTENT IN $SiO_2$ ON SiC

## Overview

Nitridation of the $SiO_2$/SiC interface yields immunity to electron injection (Chapter IV), as well as an increase in hole trap density (Chapter V). To identify the physical mechanisms associated with these two effects, the amount of incorporated nitrogen is varied by adjusting the NO annealing time. This allows to compare the evolution of the density of interface states, electron traps, and hole traps, as a function of nitrogen content. The results reported here indicate that nitrogen (i) suppresses electron-induced interface state generation by passivating precursor defects, and (ii) increases the density of hole traps by forming a SiON transition layer.

## 6.1 Motivation

In the previous chapters, it has been shown that although high temperature nitric oxide (NO) annealing improves the quality of the $SiO_2$/4H-SiC system by reducing the interface state density ($D_{it}$) and by suppressing electron-induced interface state generation,[1] the incorporation of nitrogen in the dielectric also yields a large density of hole traps.[2,3] Although, it could lead to the buildup of anomalous positive charge in all oxide-based devices, this drawback of nitridation will particularly affect p-channel MOSFETs which require a negative bias on the gate upon operation. Indeed, this will promote hole injection from the semiconductor in inversion via tunneling and/or emission (see Section 2.3). Moreover, the use of SiC devices at high temperature (e.g. 150 °C) is expected to increase the gate leakage current.[4]

Positive charge buildup in the dielectric due to negative bias and temperature has been widely studied in Si-based pMOSFETs and is referred to as negative bias temperature instability (NBTI).[5] In silicon devices, nitrogen may be incorporated in the oxide as well, not to reduce the interface state density (which is achieved by hydrogen passivation), but to limit dopant diffusion and reduce gate leakage.[6,7] However, as in SiC devices, nitridation can lead to electron immunity and increased hole trapping.[8,9,10,11,12] The latter is commonly observed during NBTI measurements (Section 2.2.4). It is therefore useful to see if the properties of NO-annealed $SiO_2$/SiC structures can be studied within the wider Si framework.

The nature of the electron and hole traps in $SiO_2$ on SiC is the subject of this chapter. Trap densities in the gate dielectric of metal-oxide-semiconductor (MOS) capacitors are characterized as a function of the amount of nitrogen incorporated in $SiO_2$. The nitrogen content is controlled by the duration of the NO anneal that follows the thermal growth of the gate oxide. The resulting nitrogen concentrations are measured by secondary ion mass spectroscopy (SIMS). Charge injections of both electrons and holes are performed using photoemission, X-ray irradiation and Fowler-Nordheim tunneling. To complement this study, some electron spin resonance measurements (ESR) were performed in order to trace the atomic configuration of the charged defects. Correlations are made between the reduction of $D_{it}$, the generated interface states and the trapped hole densities, quantities measured by CV measurements. On one hand, it is found that the $D_{it}$ and the amount of interface states generated during electron injection are both reduced by the incorporation of nitrogen in a similar way. On the other hand, the density of positive charge trapped during hole injection and X-ray irradiation (under positive gate bias) increases linearly with the amount of nitrogen. These observations indicate that electron immunity is related to the passivation of interface defects and that the NO-induced hole trap density is a property of the nitrogen binding configurations, implying that each nitrogen atom could act as a hole trap and that their presence in the near-interface region is probably undesirable. Control

samples show that neither the higher temperature used for nitridation nor the slow re-oxidation taking place during the NO anneal can explain the observed behaviors, confirming that the nitrogen is solely responsible. These conclusions are in good agreement with the partial understanding of the nitrided interface introduced in the preceding chapters.[1,2,13,3]

## 6.2 Experiments

*Sample preparation*

The substrates used in the experiments are n-type 4H-SiC ($N \simeq 5 \times 10^{15}$ cm$^3$) purchased from Cree Inc. They were dipped in TCE, acetone, methanol, and BOE (buffered HF), prior to performing the standard RCA cleaning steps. Oxidation was achieved in flowing $O_2$ at 1150 °C for 7 hours and followed by an Ar anneal at the same temperature for 30 minutes, yielding an oxide thickness of the order of 50 nm on the polished (0001) Si-face, as determined by CV and ellipsometry. Nitridation was performed via NO annealing at 1175 °C. In order to incorporate varying amounts of nitrogen, the NO exposure was adjusted between 0 and 120 minutes. The thermal budget was maintained constant for all nitrided samples by using Ar prior the introduction of NO so that they all spent a total time of 2 hours at that temperature. These samples are labeled *NO_x* (where $x$ is the NO exposure time in min). In addition, two control samples were fabricated. To test the impact of the higher temperature, they were removed after the 1150 °C Ar anneal (never exposed to 1175 °C, nor nitric oxide). One of them was then further oxidized at 1175 °C in a flowing $N_2$:$O_2$ (9:1) mixture to characterize the impact of the slow re-oxidation taking place during NO anneals, without incorporating nitrogen. These two samples are labeled *Ar_30* and *N2O2_120* respectively. Semi-transparent Al gate contacts ($\leq$ 30 nm thick and $\simeq$ 500 $\mu$m diameter) were evaporated to form MOS capacitors on the (0001) face. Finally, a drop-etch using BOE was performed to remove the oxide grown on the back side, and to ensure good ohmic contact to the substrate sputtered Au, or colloidal Ag paste, was used. The description of the oxidation setup can be found in Appendix A.

*Nitrogen content*

The profile and the density of incorporated nitrogen in NO-annealed samples were determined at EAG labs (Hightstown, NJ 08520, USA) using SIMS. The nitrogen concentrations are calibrated against a thermal silicon dioxide standard that has been ion-implanted with nitrogen. The depth scale has been calibrated against a crater measurement on the same standard sample.

*Carrier injection*

Charge injection into the gate oxide was achieved at room temperature using three of the techniques previously described in Chapters IV and V.[1,2,3] (i) Electron injection was performed at low fields using the focused radiation of a 100 W mercury lamp to emit free carriers from the negatively biased metal gate ($V_g = -10\,\mathrm{V}$, leading to an electric field in the dielectric $|E_{ox}| < 2\,\mathrm{MV/cm}$). (ii) Holes were injected via Fowler-Nordheim tunneling from the semiconductor kept in inversion by a negative gate bias and a low intensity UV light. (iii) Electron-hole pairs were generated by a 10 keV X-ray source while a positive bias was maintained on the gate to attract the electrons and push the holes to the $SiO_2$/SiC interface ($V_g = 7.5\,\mathrm{V}$ and $E_{ox} \simeq 1.5\,\mathrm{MV/cm}$).

CV measurements were performed at room temperature to monitor the $D_{it}$ and the flatband voltage $V_{fb}$ during charge injection. The $D_{it}$, between 0.2 and 0.6 eV from the SiC conduction band edge, was extracted from quasistatic and high frequency (100 kHz) CV curves taken simultaneously from accumulation to depletion using a Keithley model 82 setup (see Section 2.4). The change in flatband voltage upon injection $\Delta V_{fb}$ was monitored by the shift of the high frequency CV curve measured at flatband capacitance and was re-normalized to the shift a 50 nm oxide would yield, so that all samples can be directly compared. The effective density of trapped charge is calculated as $C_{ox}\,\Delta V_{fb}/q$ where $C_{ox}$ is the oxide capacitance and $q$ is the elementary charge. This results in a negative value for positive trapped charge and in a positive value for negative trapped charge.

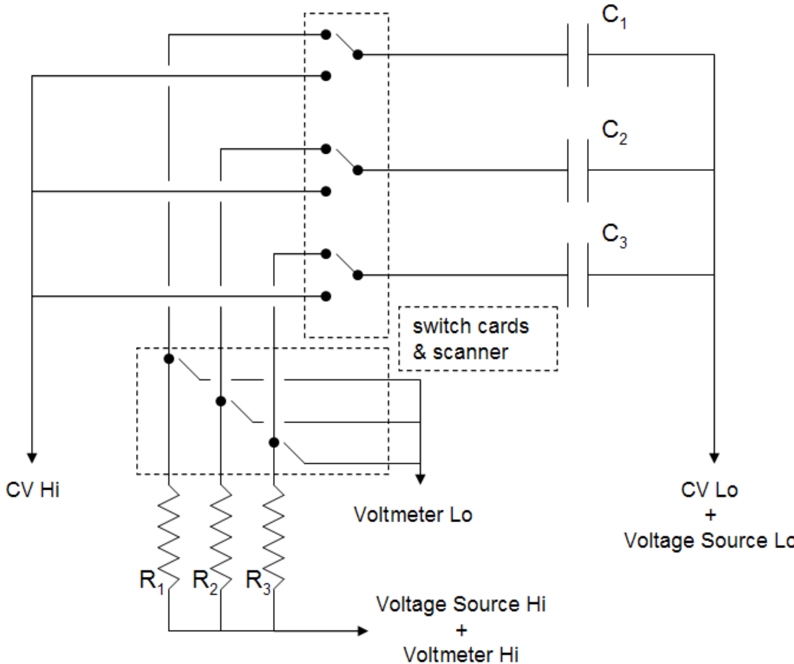



**Figure 6.1:** Schematic of the electrical connections of the designed automated injection setup. Capacitance-voltage measurements and monitored charge injection can be performed in sequence. Up to three devices are tested simultaneously. A custom LabVIEW program controls the units and processes the data.

In order to optimize the measurements, electron injection via photoemission, hole injection via Fowler-Nordheim, and intermediary CV characterization were automated and performed on up to three devices simultaneously. The setup designed for these experiments, illustrated in Figure 6.1, is described in details in Appendix B. High-frequency switch cards (Keithley 7062) are used together with a controller (Keithley 705) to alternate CV measurements and charge injection. The high-frequency CV sweeps (Keithley 590) are performed on each device sequentially from accumulation to depletion. During the injection steps, the required bias (Keithley 236) is applied to the devices, which are connected in parallel. The total injected charge for each device is obtained by integrating the current calculated from the potential differences measured sequentially by a digital multi-meter (Keithley 706) across resistors (100 MΩ) connected in series. The value of the resistors was to chosen to give a good accuracy for currents of the order of nA ($\simeq$ 500 nA/cm$^2$), while maximizing the fraction of voltage dropped across tested devices ($>90\%$). During the CV measure-

ment steps, the low intensity UV lamp was kept on when performing Fowler-Nordheim hole injection experiments, but the high intensity UV beam was blocked by a shutter when performing photoemission of electrons. A custom LabVIEW program was implemented to control the units and process the data.

*Spin resonance*

For spin resonance measurements, oxides on the (000-1) C-face of 6H-SiC and the (001) face of Si were grown in the conditions described above. Some of them were then annealed for 2 hours in NO at 1175 °C, yielding an $SiO_2$ thickness of about 275 nm and 425 nm on SiC and Si respectively. In order to charge the defects, the samples were irradiated with 5 to 10 Mrad ($SiO_2$) using the 10 keV X-ray source. X-band ESR measurements were made at 30 K. The g-value, characteristic of the ESR signal, was calculated from the applied field at resonance.[14]

## 6.3 Results and Discussion

### 6.3.1 Kinetics of the nitrogen uptake

The evolution of the nitrogen profile and concentration in the samples exposed to NO at high temperature were monitored as a function of annealing time. The SIMS data for samples *NO_7.5*, *NO_30* and *NO_120* is shown in Figure 6.2. The peaks correspond to the nitrogen profiles, the associated concentrations are labeled on the left axis. The carbon (C) and oxygen (O) concentrations are plotted in arbitrary units (right axis). In order to have the three nitrogen profiles on the same graph, their respective C and O signal were aligned so that the position of the peaks can be studied relative to the $SiO_2$/SiC interface.

In all cases, the nitrogen is located at the interface. Indeed, it can be seen that the relative position of the peaks remains constant. This indicates that, during the slow re-oxidation associated with the NO annealing, the nitrogen peak moves with the interface toward the semiconductor as more Si and C atoms are consumed by the formation of $SiO_2$ ($\simeq$ 1 nm/min). Oxides annealed using $N_2O$ lead to the same observation.[15,16] Other

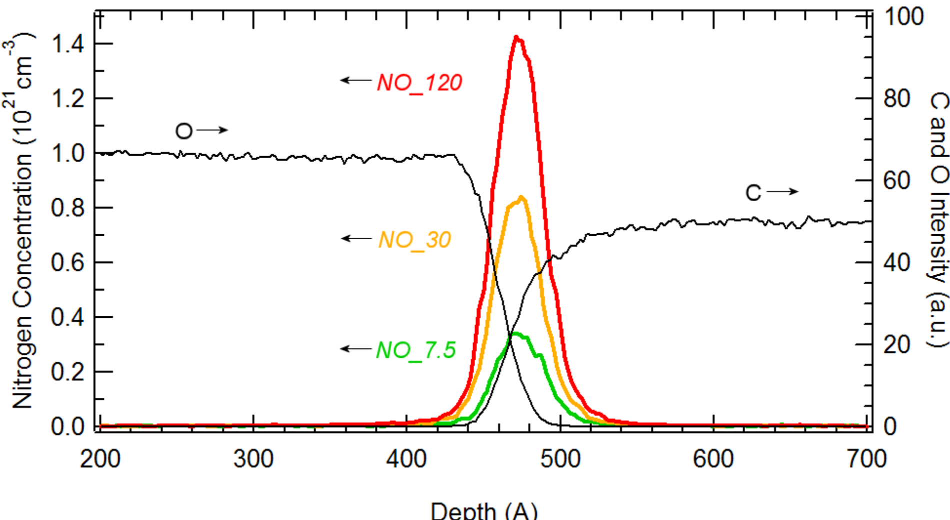



**Figure 6.2:** SIMS profiles for the samples annealed in NO for 7.5 min, 30 min and 120 min.

techniques like $NH_3$ annealing and plasma nitridation, incorporate nitrogen throughout the $SiO_2$, which reveals that the kinetics of NO and $N_2O$ anneals are peculiar.[17,18,19] In addition, for NO and $N_2O$, the incorporation rates scale with the oxidation rates when comparing nitrogen uptake on the Si-face, a-face, C-face of SiC, and on silicon.[20] All this suggests that the nitrogen uptake results from the dissociation of NO at the oxide/semiconductor interface during NO and $N_2O$ anneals.

Also, the width of the SIMS nitrogen peaks calculated at half maximum (FWHM) is constant for all measured annealing times. It implies that the extent of the region in which nitrogen is incorporated remains the same. Note that the extracted values of $\simeq$ 3 nm is limited by the technique as there are several processes impacting SIMS depth resolution: collision cascades cause intermixing of the ions at the interface and artificial profile broadening, the stress and the density at the interface can affect the sputtering rate of the primary beam, the ionization yield can change in that region... In fact, it has been shown from electron energy-loss spectroscopy (EELS) that the nitrogen is located within at most 1.2 nm of the $SiO_2$/SiC interface, the resolution limit of the technique.[20,21] The localized dissociation of NO, the passivation of defects, and/or the release of interfacial stress could explain the accumulation of nitrogen in that region only.

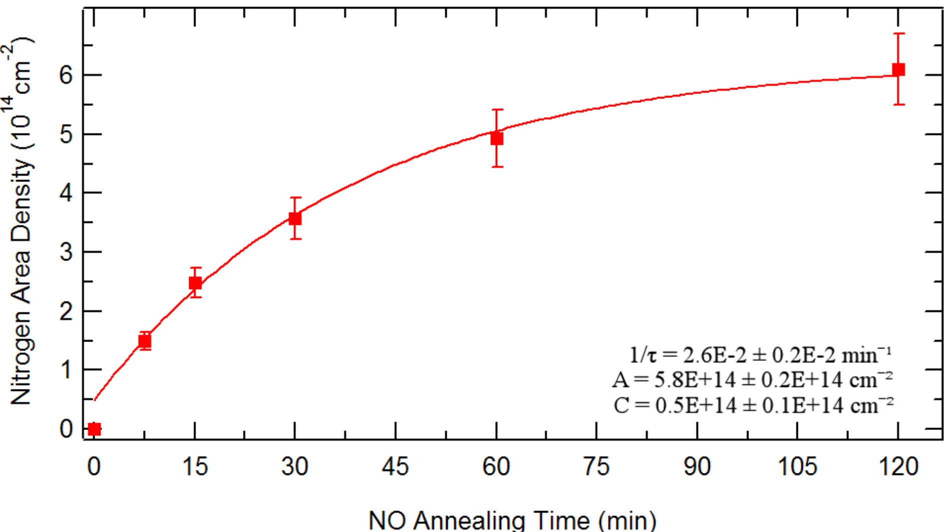



**Figure 6.3:** N area density as a function of NO annealing time calculated by integrating the SIMS N signal. The curve is the fit by Eq.(6.3), the resulting values of the parameters are listed.

In order to study the evolution of the nitrogen incorporation rate, the N area density $\eta$ (in atoms/cm$^2$) was extracted as a function of the NO annealing time $t$ (in minutes) from the SIMS data (Figure 6.3). The values were obtained by subtracting the background noise at detection limit ($\simeq 10^{18}$ cm$^{-3}$ seen in the sample *NO_0*) prior to integrating the N signal. In previous experiments, the error on the absolute values of the area density deduced from SIMS was estimated to be around 20% by a cross-calibration with nuclear reaction analysis (NRA).[22] However, the relative error for each point, i.e. the reproducibility, is of the order of 5%.

The data is analyzed by a first-order rate equation which is obtained in part by assuming that a density $\eta_0$ of binding sites is available for nitrogen at the interface at $t = 0$ and that the change in N area density per unit time is proportional to a binding rate $1/\theta_b$ (in cm$^3$/min), to the NO concentration $C_{NO}$ in the oxide (in molecules/cm$^3$),[a] and to the the number of sites left unoccupied at time $t$;

$$\frac{d\eta}{dt} = \frac{\eta_0 - \eta}{\theta_b} C_{NO} \tag{6.1}$$

[a]The equilibrium concentration of gas in a solid is directly proportional to the one in the gas phase according to Henry's law, Eq.(3.8).

However, it is believed that the process is not that straightforward. In particular, it has been shown that the nitrogen incorporated at the $SiO_2$/SiC interface via NO and $N_2O$ anneals is not stable against re-oxidation,[15] i.e. it is removed in the presence of $O_2$. This affects the kinetics of the nitrogen uptake because there is always a source of oxygen during NO and $N_2O$ exposure at high temperature.[22] For flowing anneals at 1175 °C, the remaining molar fraction of NO is about 50% as it partially decomposes into $N_2$ ($\simeq$ 25%) and $O_2$ ($\simeq$ 25%). Therefore, in addition to the atomic oxygen resulting from the dissociation of the NO molecules at the interface, there is molecular oxygen in the system. This explains the slow re-oxidation taking place in parallel with the nitrogen incorporation. It also implies that the N saturation value comes in part from a balance between incorporation and removal. In the case of $N_2O$, the re-oxidation rate is even faster because it decomposes quickly into NO ($\simeq$ 10%), $N_2$ ($\simeq$ 60%), and $O_2$ ($\simeq$ 30%). Accordingly, the molar ratio of $O_2$ to NO is 0.5 and 3 during NO and $N_2O$ annealing respectively. Because of the faster re-oxidation rate in the latter case, an order of magnitude less N is incorporated.[16]

A kinetic model assuming the total nitridation rate ($d\eta/dt$) to be proportional to the NO concentration and inversely proportional to the $O_2$ concentration has been previously derived.[20] However, it did not consider saturation of the binding sites as in Eq.(6.1). If one assumes that N removal is primarily due to the molecular oxygen,[b] and that processes such as the formation of a diffusion barrier are not dominant,

$$\frac{d\eta}{dt} = \frac{\eta_0 - \eta}{\theta_b} C_{NO} - \frac{\eta}{\theta_r} C_{O_2} \tag{6.2}$$

where $\theta_r$ is the N removal rate and $C_{O_2}$ is the concentration of molecular oxygen. The general solution of Eq.(6.2) is of the form

$$\eta[t] = A\,(1 - e^{-t/\tau_b}) + C \tag{6.3}$$

[b] Note that if removal from the atomic oxygen is considered, an additional term needs to be added to Eq.(6.2). The equation will keep the same form and have a similar solution.

where $C$ is an offset constant, $A$ is the saturation area density and $1/\tau_b$ is an effective characteristic rate (in $\text{min}^{-1}$). From Eq.(6.2), $A$ and $\tau_b$ are defined by

$$A = \eta_0 \frac{1}{1 + \frac{C_{O_2}}{C_{NO}} \frac{\theta_b}{\theta_r}} \tag{6.4}$$

$$\tau_b = \frac{1}{\frac{C_{NO}}{\theta_b} + \frac{C_{O_2}}{\theta_r}} \tag{6.5}$$

Note that Eqs. (6.2), (6.4) and (6.5), could be simplified by assuming a proportionality factor between the oxygen and the nitric oxide concentration.

The fit of the data by Eq.(6.3) for $t > 0$, shown in Figure 6.3, yields values for the characteristic rate and $C$ that are about $2.6{\times}10^{-2}$ $\text{min}^{-1}$ and $0.5{\times}10^{14}$ $\text{cm}^{-2}$ respectively. The offset ($C$) could be explained by the errors in the absolute values of $\eta[t > 0]$. The nitrogen saturation density is estimated at approximately $5.75{\times}10^{14}$ $\text{cm}^{-2}$, in good agreement with previously published values.[16,22,23,24]

It should be noted that although Eq.(6.3) can model the evolution of the nitrogen concentration in the present case, it does not predict the decrease of $\eta$ which has been observed, is some cases, for longer annealing times.[20,22] In fact, the amount of binding sites available is likely to be of the form

$$\eta_0 = \sum_i \eta_{0i} \tag{6.6}$$

where $\eta_{0i}$ are the contributions from sites of different nature: interface defects, bulk defects, strained $SiO_2$... During the slow re-oxidation taking place while introducing nitrogen, it is possible that some properties of the oxide and of the interface will change, implying that $\eta_0$ is not a constant but a function of time as well. So it could be that the equilibrium value of $\eta_0$ during nitridation is lower than the one at $t = 0$.

### 6.3.2 Impact of temperature and slow re-oxidation

In this section the effects of the higher temperature used during NO exposure, and of the slow re-oxidation that occurs in parallel, are studied in order to isolate the role of the nitrogen on the properties of the oxide and of the interface. In order to do so, the $D_{it}$, as well as the hole and electron trapping behaviors, are monitored in four different samples: sample *Ar_30* (processed at 1150 °C, never exposed to NO), sample *N2O2_120* (post-oxidation anneal at 1175 °C in $N_2$:$O_2$ mixture, 9:1, for 2 hours), sample *NO_0* (post-oxidation anneal at 1175 °C in Ar for 2 hours), and sample *NO_120* (post-oxidation anneal at 1175 °C in NO for 2 hours).

The interface state densities of these samples are plotted in Figure 6.4(a). It can be seen that neither the temperature, nor the re-oxidation, impacts the $D_{it}$ as much as the NO anneal. This is in agreement with plasma nitridation experiments from which the nitrogen alone is shown to achieve NO-like $D_{it}$.[17] In Figure 6.4(b), the effective trapped charge ($C_{ox}\Delta V_{fb}/q$) is shown as a function of the injected hole density. The NO-annealed samples are found to possess a hole trap density much larger than any other ones. Finally, only the NO-annealed sample prevents the generation of interface states and of the resulting negative charge trapping upon electron injection (not shown).

It is therefore concluded that the binding of nitrogen at the $SiO_2$/SiC interface is solely responsible for the reduction in $D_{it}$, for the electron immunity, and for the increased hole trap density. The data presented in the following sections are interpreted in these terms.

### 6.3.3 Progressive reduction of the interface state density

The interface state densities between 0.2 and 0.6 eV from the conduction band edge are plotted in Figure 6.5 for different NO annealing times. The upper curve corresponds to the base $D_{it}$ obtained from sample *NO_0* annealed in Ar at 1175 °C for 2 hours ($D_{it}^0$). It can be seen that the high temperature NO treatment is efficient at progressively reducing the amount of electrically active levels throughout the monitored energy window.

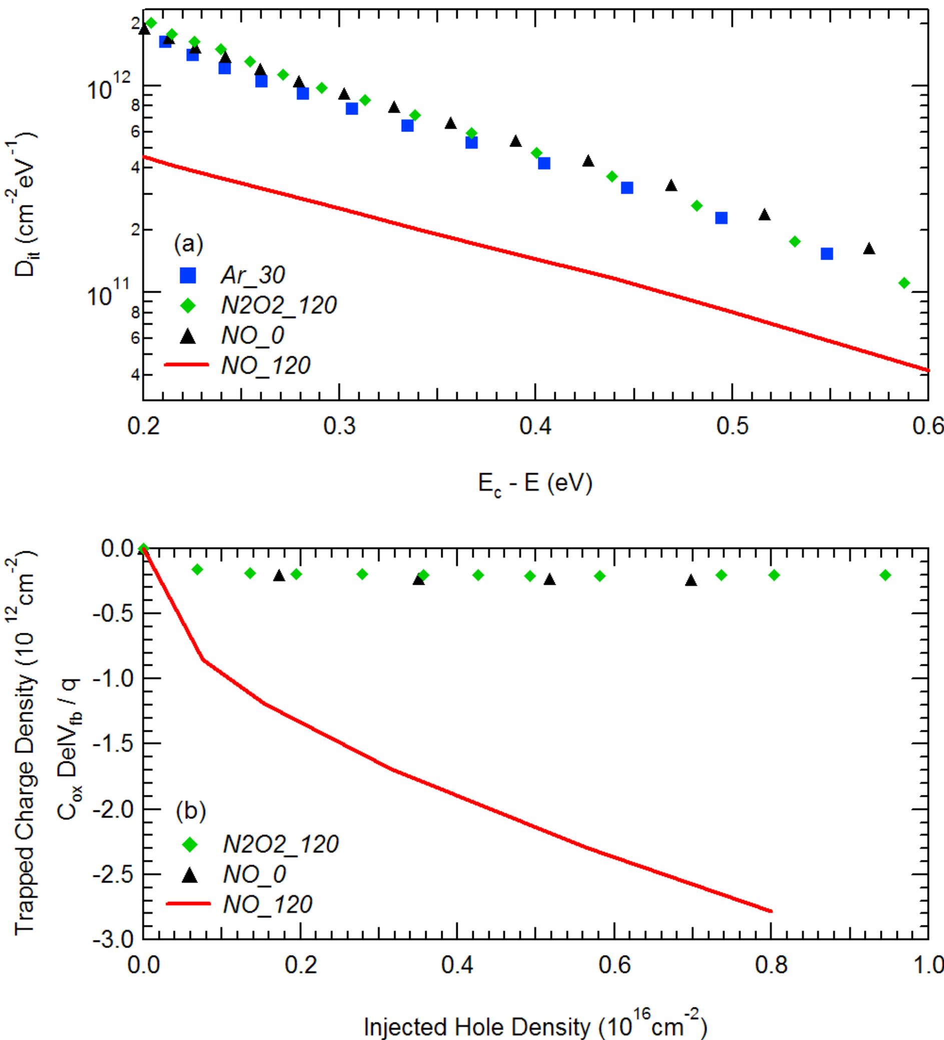



**Figure 6.4:** Density of interface states (a) and positive charge trapping (b) in the control samples and in the one annealed in NO for 2 hours. The temperature and the slow re-oxidation have no significant effect on the properties, only the nitrogen incorporated during the NO anneal does.

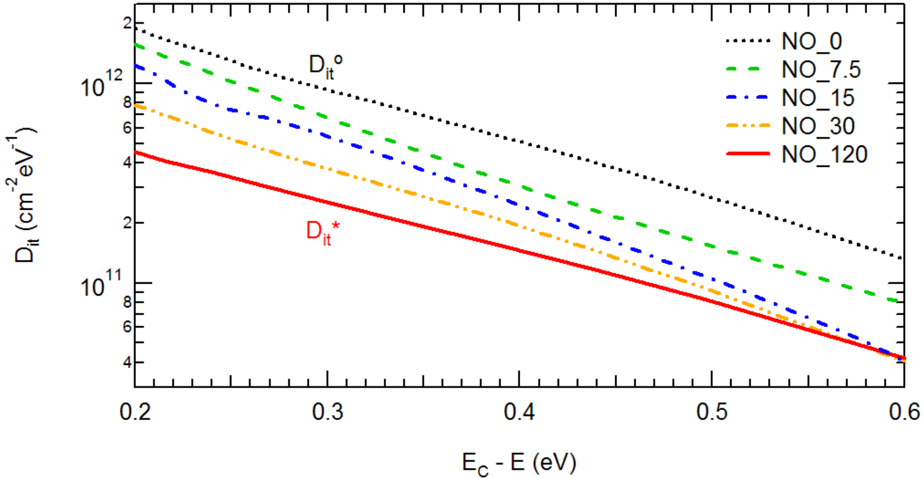



**Figure 6.5:** Density of interface states of the control sample (2 hours Ar at 1175 °C) and of the ones annealed for 7.5, 15, 30, and 120 minutes in NO. $D_{it}^{0}$ and $D_{it}^{*}$ refer to the $D_{it}$ prior to NO annealing and at N saturation respectively.

Because the impact on the $D_{it}$ of the temperature and of the slow re-oxidation have been shown to be negligible compared to the observed impact of NO anneals, this reduction is attributed to the passivation and/or the removal of defects by nitrogen binding at the interface. Theory suggests that nitrogen can indeed substitute for three-fold coordinated atoms or bind at defect sites, which reduces the $D_{it}$ in the upper part of the 4H-SiC band-gap,[13] as described in Chapter I (Section 1.3.3). These defects could be of different nature and therefore have different energy levels, explaining the efficiency of nitrogen over a wide energy range. For example, single carbon interstitials at the interface or silicon suboxide bonds in the oxide (of various lengths) are expected to have levels close to the conduction band edge. Also, carbon clusters at the interface (8 atoms or less) are thought have levels located deeper in the gap. All these defects can theoretically be passivated by nitrogen. This is supported by experiments, such as X-ray photoelectron spectroscopy measurements (XPS), which indicate that NO anneals lead to the reduction of excess carbon, and to the formation of C-N and Si-N bonds while complex oxide/carbon states are removed.[25,26]

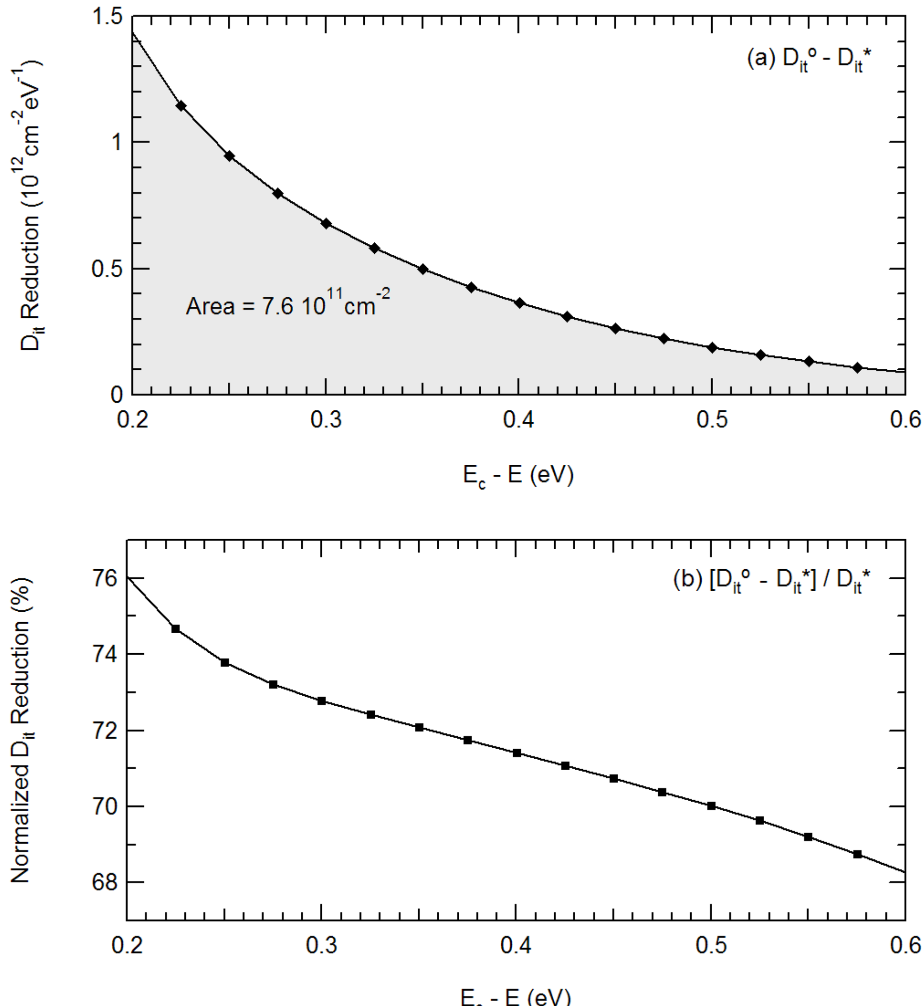



**Figure 6.6:** $D_{it}$ reduction (a), and normalized $D_{it}$ reduction (b), after nitrogen saturation at the $SiO_2$/SiC interface.

The obtained $D_{it}$ values can be fit by an exponential function which has the form

$$D_{it}[E_c - E] = D_0 \, e^{-B(E_c - E)} \tag{6.7}$$

where $E$ is the energy of the level, $E_c$ is the energy at the conduction band edge, $D_0$ is a pre-exponential constant, and $B$ an exponential argument. It is observed that, although deeper levels seem to reach saturation early, the value of $B$ does not change much as a function of nitrogen content. Indeed, the fits lead to an average $B$ of 7.2 $\text{eV}^{-1}$ with a standard deviation of 0.9 $\text{eV}^{-1}$. This indicates that the shape of the $D_{it}$ profile remains similar during nitridation and that the amplitude $D_0$ is progressively reduced. The difference between $D_{it}^0$ and the $D_{it}$ at N saturation ($D_{it}^*$) is shown in Figure 6.6(a). It reveals that N removes more levels towards the conduction band edge. This is only because their density is higher prior to NO annealing. Indeed, the reduction of the $D_{it}$ normalized by $D_{it}^0$, Figure 6.6(b), indicates that the efficiency of nitrogen is comparable throughout the monitored energy window, as it removes about 70% of all levels. This suggests that the corresponding defects are of similar nature. However, the shape of the curve indicates that levels within 0.3 eV of the conduction band could be associated to a distinct category of atomic configurations. Actually, it has been observed that the $D_{it}$ of unpassivated samples rises very sharply in that region,[27] and reaches a value of several times $10^{13}$ $\text{cm}^{-2}$ $\text{eV}^{-1}$, which cannot be predicted by Eq.(6.7). These shallow states are thought to originate mostly from Si-Si suboxide bonds and to be very sensitive to nitrogen incorporation.[28] Another important parameter to extract, is the total density of levels removed after NO annealing between 0.2 and 0.6 eV. This is done by integrating the curve in Figure 6.6(a). It yields a value of approximately $7.6\times10^{11}$ $\text{cm}^{-2}$ which is only about 0.1% of the N area density at saturation. Even when considering the shallow states and the levels in the rest of the band-gap, it appears that there are two orders of magnitude more nitrogen incorporated than there are defects to passivate. This surprisingly large number will be discussed below.

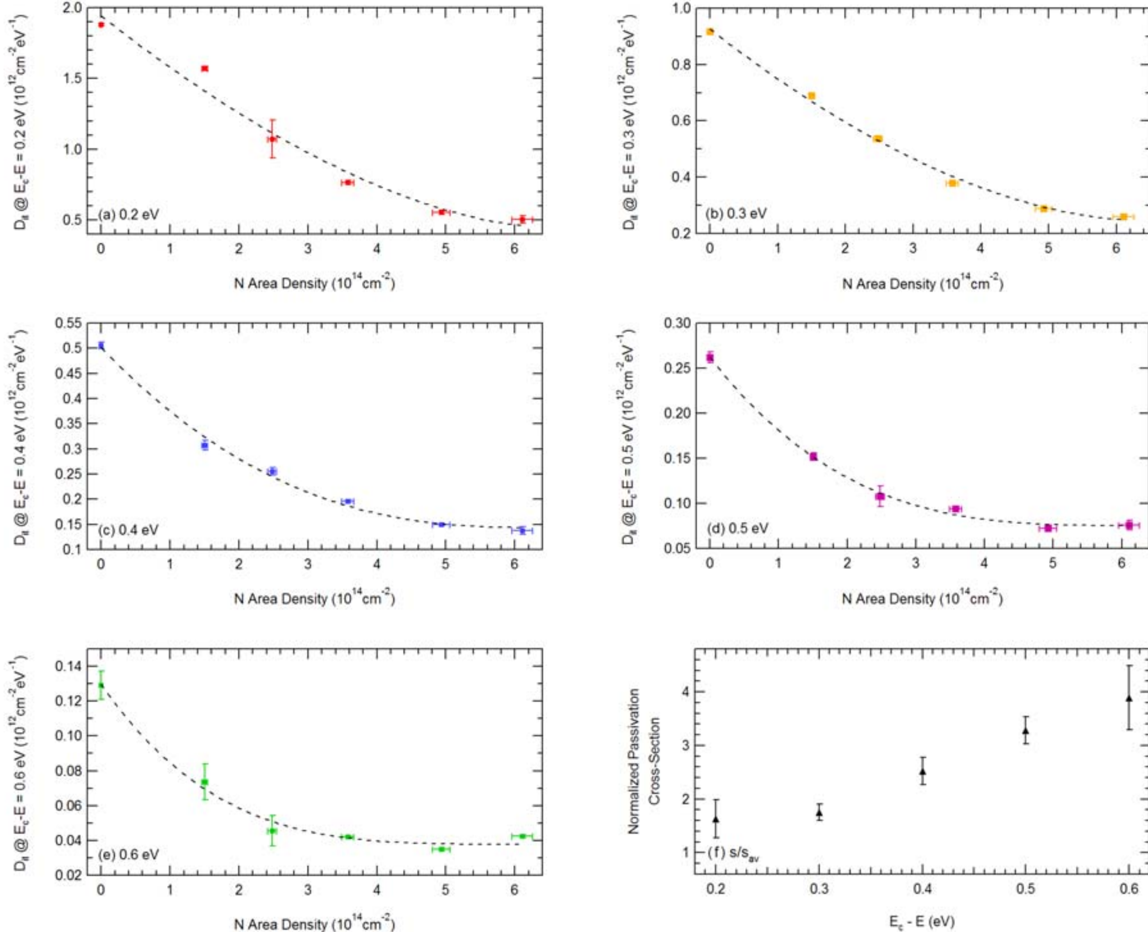



**Figure 6.7:** (a) to (e); evolution of the $D_{it}$ at different energy levels as a function of the area density of nitrogen incorporated by NO annealing. The amount of nitrogen required to achieve saturation seems to be less for levels deeper in the gap, it varies from $\simeq 5\times10^{14}$ cm$^2$ at $E_c - E = 0.2$ eV to $\simeq 3\times10^{14}$ cm$^2$ at $E_c - E = 0.6$ eV. The dashed lines are fits by Eq.(6.12). (f) Normalized passivation cross-sections extracted form the fits.

The evolution of the $D_{it}$ at specific levels is shown as a function of the nitrogen area density in Figure 6.7(a-e). This allows to study the kinetics of the passivation at different energies. A passivation model has previously been derived by McDonald *et al.*[23] It assumed the reduction in size of carbon clusters which progressively moved the defect levels deeper in the band-gap. This does not seem to apply to the data presented here as there is no evidence of a step formation in $D_{it}$ vs $\eta$ (the nitrogen area density) for deeper levels, which motivated the model. On the contrary, in this work, the density of deeper levels is found to saturate faster. It should be noted that the processing of the samples was different in the two experiments. McDonald *et al.* used a wet oxidation to grow the oxides, as well as a re-oxidation process; they report a higher $D_{it}^0$ and $D_{it}^*$ which is likely related to the presence of other dominant defects.

Here, it is proposed that to first order N removes levels within the studied energy window without inducing any. Therefore, the passivation rate is expected to be proportional to a cross-section $s_j$ (in cm$^2$) and to the density of available binding sites $D_j$ (in cm$^{-2}$) of type $j$. It should also be inversely proportional to the sum of $s_j D_j$ over all competing locations. This leads to the differential equation

$$\frac{dD_j[\eta]}{d\eta} = -\frac{s_j(D_j[\eta] - D_j^*)}{\sum_i s_i(D_i[\eta] - D_i^*)} \tag{6.8}$$

where $D_j^*$ is the remaining density when $\eta$ reaches $\eta^*$, the N area density at saturation. It can be solved for all sites by defining an average cross-section

$$s_{av} = \frac{\sum_i s_i(D_i - D_i^*)}{\sum_i(D_i - D_i^*)} \tag{6.9}$$

noting that

$$\sum_i(D_i - D_i^*) = \eta^* - \eta \tag{6.10}$$

Using Eqs. (6.9) and (6.10), Eq.(6.8) becomes

$$\frac{dD_j}{d\eta} = -\frac{s_j\,(D_j - D_j^*)}{s_{av}\,(\eta^* - \eta)} \tag{6.11}$$

which can be solved exactly with the boundary condition $D_j[0] = D_j^0$;

$$D_j[\eta] = (D_j^0 - D_j^*)\left(\frac{\eta^* - \eta}{\eta^*}\right)^{s_j/s_{av}} + D_j^* \tag{6.12}$$

A particular solution of Eq.(6.8) arises when $s_j = s_{av}$, as Eq.(6.12) then yields a linear relationship between $D_j$ and $\eta$. From the definition of the average cross-section, Eq.(6.9), $s_j = s_{av}$ could occur either coincidentally, or if all cross-sections are equal, or if the nitrogen occupancy of a dominating binding site ($D_j - D_j^* \simeq \eta^*$) is studied.

When $D_j$ corresponds to an atomic configuration that is electrically active, it can be interpreted as the density of levels at a given energy $E_j$, $s_j$ becoming a passivation cross-section. Indeed, Eq.(6.12) is found to successfully model the evolution of the $D_{it}$ at the extracted levels considered in Figure 6.7(a-e). The obtained normalized cross-sections ($s_j/s_{av}$) are shown in Figure 6.7(f). Their increasing values for levels deeper in the band-gap correspond to the earlier saturation of the $D_{it}$ at these energies. It indicates that although the density of corresponding defects is small prior to nitridation when compared to the rest of the band-gap, they could be binding sites favored by N. Moreover, a distinction can be made between the levels within 0.3 eV of the conduction band edge and the ones deeper in the band-gap. Indeed, ones between 0.2 and 0.3 eV have similar passivation cross-sections. This again suggests that they relate to a separate category of defects.

Note that if more than one nitrogen atom is required to remove a level, say $\alpha$N, the $D_{it}$ at $E_j$ would correspond to $D_j/\alpha$. Could this explain why there are apparently two orders of magnitude more N incorporated than there are defects to passivate? It is hard to conceive, because it would not only imply that there is a progressive redistribution of the energy levels, which is not observed here between 0.2 and 0.6 eV, but also that apparently

about 100 N atoms are needed to remove a single defect level. Instead, it is possible that the binding of nitrogen is not driven by defect passivation but by the formation of a SiON layer at the interface ($\eta^* \simeq 1$ monolayer). Nitrogen can indeed be incorporated in $SiO_2$, regardless of the interface state density. For example, it can bind in the bulk of the oxide following plasma or $NH_3$ nitridation.[17,18,19] In the case of NO-annealing, the fact that nitrogen resides at the interface is related with the cracking of NO molecules in that region and with the re-oxidation process, as explained earlier. Moreover, similar characteristics of the nitrogen uptake are observed at the $SiO_2$/Si interface which is very different from the $SiO_2$/SiC one.[16]

In fact, nitridation is known to generate $D_{it}$ in the case of Si and to increase NBTI, indicating that N binding can have drawbacks.[9,10,11,12] This correlates with the theoretical calculations which predict that N can disturb a perfect oxide by inserting within a Si-O-Si bridge which yields an oxygen protrusion and a new defect level close to the valence band edge of 4H-SiC.[13,3,2] Therefore, the majority of the nitrogen incorporated at the $SiO_2$/SiC is probably not associated with defect passivation and could be detrimental to the interface. Actually, this excess nitrogen is thought to enhance hole trapping in the NO-annealed samples as discussed in a following section.

### 6.3.4 Suppression of electron-induced interface state generation

In this section and the next, the effective trapped charge density $N_{eff}$ (in cm$^{-2}$) is calculated from the flatband voltage shifts ($C_{ox}\Delta V_{fb}/q$) upon injection in several capacitors. In order to perform an average, the following analytical expression is used to fit the data from each device;

$$N_{eff}[\rho] = N_1(1 - e^{-\sigma_1 \rho}) + N_2(1 - e^{-\sigma_2 \rho}) \tag{6.13}$$

where $\rho$ is the injected charge density (in cm$^{-2}$). This equation, which assumes that there are two kinds of trapping event occurring in parallel, is found to accurately describe the experimental curves. The two trap area densities are $N_1$ and $N_2$, they have a capture cross-section equal to $\sigma_1$ and $\sigma_2$ respectively (in cm$^2$).

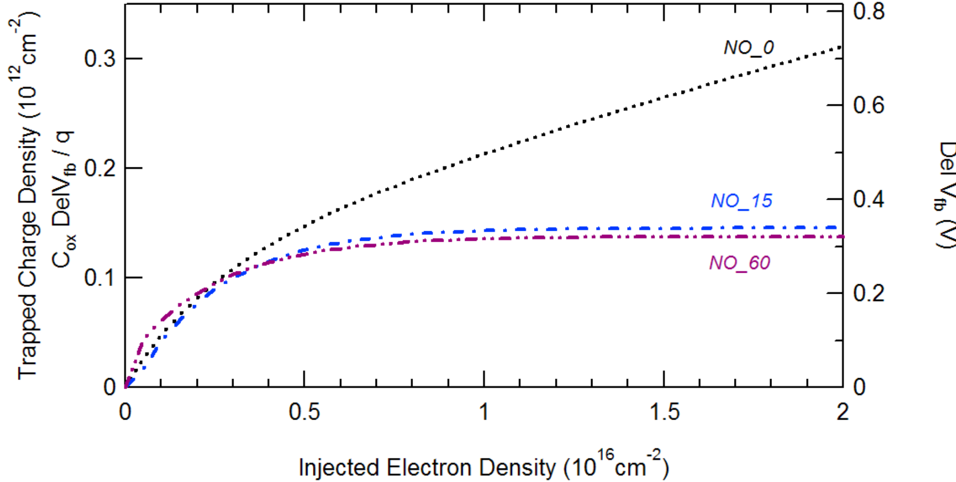



**Figure 6.8:** Effective charge trapped upon electron injection in an unpassivated oxide (*NO_0*), and in oxides annealed for 15 and 60 minutes in NO.

The effective charge densities trapped upon electron injection are plotted in Figure 6.8 for devices having three different nitrogen contents (0, $2.5\times10^{14}$ and $5\times10^{14}$ cm$^{-2}$) corresponding to various NO exposure time (0, 15 and 60 minutes). It can be seen that in the unpassivated sample (*NO_0*) the trapped charge shows no sign of saturation within the monitored window. This has been associated with electron-induced generation of acceptor states at the $SiO_2$/SiC interface (Chapter IV). This phenomenon is immediately suppressed, even for the shortest NO annealing times, as the curves extracted from samples *NO_15* and *NO_60* are identical within statistical errors. In these samples, only background electron trapping, i.e. from the oxide bulk, is thought to remain. From Eq.(6.13), the density of bulk traps is estimated to be around $1.2\times10^{11}$ cm$^{-2}$ and to have a trapping cross-section of about $3.9\times10^{-16}$ cm$^{-2}$, in good agreement with the previous measurements (Section 4.3). The cross-section associated to interface state generation is found to be about $2\times10^{-17}$ cm$^{-2}$.

As the suppression of interface state generation is achieved for $\eta < \eta^*$, it resembles the passivation of electrically active defects by nitrogen, these observations concur with the hypothesis that NO-annealing passivates precursor interface defects susceptible to electron trapping.

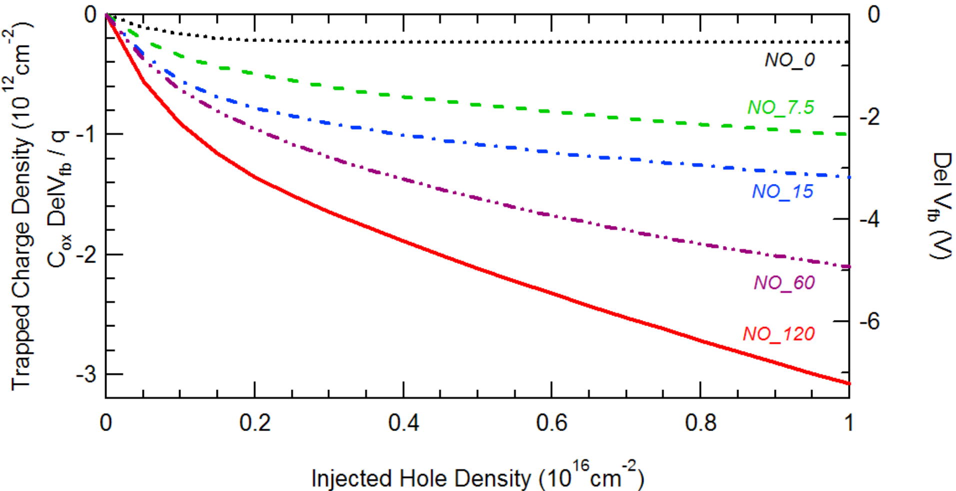



**Figure 6.9:** Effective trapped charge upon hole injection in oxides annealed for various times in NO.

### 6.3.5 Increase in hole trap density

The effective charge trapped upon Fowler-Nordheim hole injection, after various NO annealing times, is plotted in Figure 6.9. The backgound trapping observed in the unpassivated sample (*NO_0*) is found from Eq.(6.13) to correspond to a trap density of around $2.3\times10^{11}$ cm$^{-2}$ which has a hole capture cross-section of about $1.2\times10^{-15}$ cm$^{-2}$. The introduction of nitrogen at the interface leads to additional hole traps, with capture cross-section between $10^{-17}$ and $10^{-16}$ cm$^{-2}$.

Clearly, the amount of N-induced hole traps scales with the NO annealing time. This is emphasized in Figure 6.10 where the effective density of charge trapped after injecting $10^{-16}$ holes per cm$^2$ is plotted as a function of the N area density $\eta$. The trapping resulting from 5 Mrad ($SiO_2$) under positive gate bias is shown as well. Both curves reveal a linear dependence of the hole trap density on $\eta$ up to N saturation in the oxide. This is similar to observations on Si from NBTI measurements.[9] The fits indicate a rate ($dN_{eff}/d\eta$) of approximately $5\times10^{-3}$ traps created per N atom incorporated. This should be taken as a lower limit since not all traps have captured a hole following the described injection conditions. The values extracted from Eq.(6.13) indicate that the total hole trap density is above $3\times10^{12}$ cm$^{-2}$ following N saturation at the interface. This value should also be

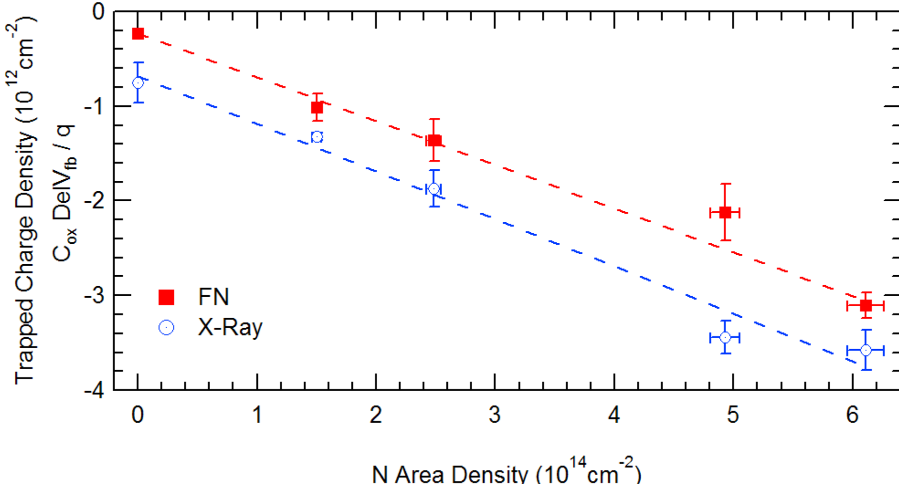



**Figure 6.10:** Effective trapped charge after the injection of $10^{-16}$ holes per cm$^2$ by Fowler-Nordheim tunneling (FN) and after 5 Mrad ($SiO_2$) exposure under positive bias (X-Ray), as a function of the N area density.

considered as a lower limit because of the field-induced detrapping that can occur during Fowler-Nordheim injection.

In any case, the measured densities suggest that the hole traps induced by nitrogen do not correspond to the passivation of any single level within 0.2 to 0.6 eV from the 4H-SiC conduction band edge. It could however be related to defects having levels between 0.2 eV and the conduction band. Suboxide Si-Si bonds (oxygen vacancies) are thought to be among such defects.[13] As they are E' center precursors, their density can be monitored by ESR measurements.[29] It can be seen in Figure 6.11 that NO annealing actually reduces the number of E' centers in oxides grown on both Si and SiC. Therefore, high temperature NO exposure does not increase the density of oxygen vacancies in $SiO_2$.

In addition, it should be noted that, although the density of trapped positive charge is proportional to the amount of incorporated nitrogen, it is stable against the formation of the electron accumulation layer in the n-type SiC substrates. This suggests that the traps are not located precisely at the interface but within about 1 nm, the extent of the N profile in the oxide estimated from EELS.[20,21] In fact, a configuration involving nitrogen has recently been identified as a dominating hole trap in nitrided $SiO_2$ on Si.[30,31] It results

from the incorporation of nitrogen in the oxide network, forming a SiON transition layer at the semiconductor interface. As similar chemistry is expected to occur on a SiC substrate, it suggests that the hole traps are not associated with the passivation of a particular defect but to the binding of N in the interfacial region. This could explain the large density of hole traps and its linear dependence to the N area density up to the saturation of nitrogen in the oxide. Such a scenario is supported by first-principle calculations, discussed in Chapter V, which show that the bonding of nitrogen in $SiO_2$ results in a lone-pair state close to the valence band edge of 4H-SiC (within the valence band of Si). This level is predicted to act as a hole trap.[2]

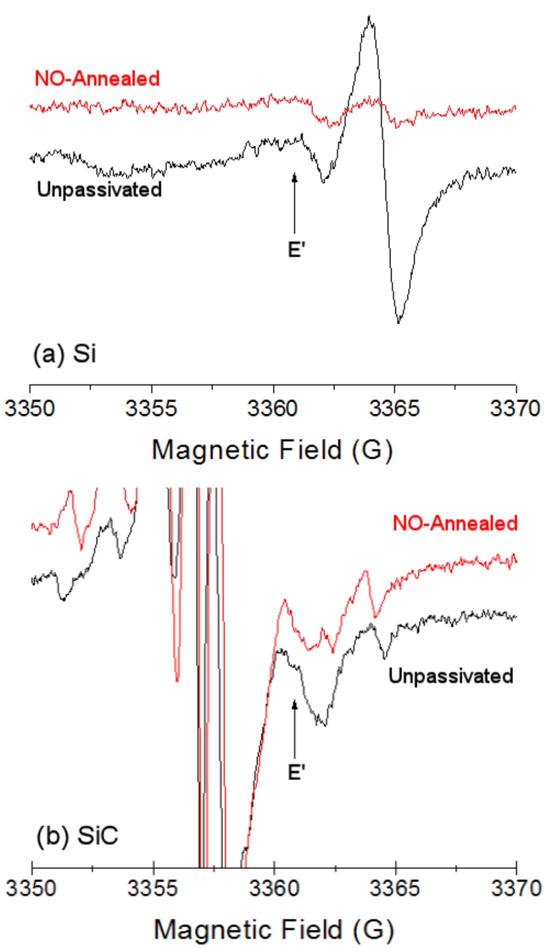



**Figure 6.11:** ESR spectra of the oxides before and after NO annealing on Si (a) and SiC (b). The arrows indicates the E' signal shown to decrease after nitrogen incorporation.

## 6.4 Summary

It has been shown that high temperature NO anneals of $SiO_2$ on SiC lead to the incorporation of nitrogen, resulting from the dissociation of NO molecules, exclusively at the oxide/semiconductor interface. The N area density saturates around $6\times10^{14}$ cm$^{-2}$, a value thought to originate from the competition between N binding at host sites and N removal during the slow re-oxidation occurring in parallel. The kinetics have been modeled by a first-order rate equation.

The higher temperature of the NO process and the resulting slow re-oxidation have been shown to have little impact on the properties of the oxide and of the interface. It is therefore concluded that the binding of nitrogen at the interface is solely responsible for the decrease in $D_{it}$, for the electron immunity, and for the increase in hole trap density.

The evolution of the density of interface states at a given level as a function of the N area density has been shown to be well described by a derived passivation model up to the minimum $D_{it}$. The reduction rates are proportional to a passivation cross-section and to the amount of levels prior to nitrogen incorporation, which ultimately leads to the removal of about 70% of the states between 0.2 and 0.6 eV from the 4H-SiC conduction band edge. The deeper levels seem to be minimized faster, which indicates that there is no progressive lowering of the energy of defect levels within the SiC band-gap when the described processing steps are used.

On one hand, the interface state generation upon electron injection is suppressed after the smallest N area density introduced. It suggests that it is related to the passivation, or the removal, of precursor defects at the interface. On the other hand, the incorporation of nitrogen progressively increases the hole trap density up to the largest N content achievable. The amount of hole traps and their generation rate by N shows that these traps do not originate from the passivation of any given defect within the 0.2 to 0.6 eV window. In addition, the density of oxygen vacancies has been shown to be reduced after the NO annealing, which rules out their role in the enhanced hole trapping. Because the positive

trapped charge is stable against the formation of an electron accumulation layer, it is thought that the hole traps originate from the formation of a SiON layer extending about 1 nm into the oxide.

Although the exact nature of all the nitrogen bonding configurations following NO exposure remains to be identified, it appears that part of them, related or not with defect passivation at the interface, play a role in the positive charge buildup during hole injection. Accordingly, it is reasonable to assume that the same nitrogen-induced levels are responsible for enhancing the positive trapped charge observed during NBTI measurements on nitrided $SiO_2$ on silicon. In particular, the hole trap densities scale linearly with the N content in both systems. In the case of Si, nitrogen can be moved away from the interface by a re-oxidation process to reduce NBTI without negating the N-related enhanced oxide properties. However, in the case of SiC, the presence of nitrogen at the interface is necessary to passivate or remove defects, and to increase the channel mobility of oxide-based devices. The resulting hole trapping therefore seems unavoidable, and the tolerance on the stability of device characteristics has to determine the amount of nitrogen required.

**References**


[1] J. Rozen, S. Dhar, S. Wang, S. T. Pantelides, V. V. Afanas'ev, J. R. Williams, and L. C. Feldman, *Applied Physics Letters* **91**, 153503 (2007).

[2] J. Rozen, S. Dhar, S. K. Dixit, F. O. Roberts, H. L. Dang, S. Wang, S. T. Pantelides, V. V. Afanas'ev, J. R. Williams, and L. C. Feldman, *Accepted for publication in the Journal of Applied Physics* (2008).

[3] S. K. Dixit, S. Dhar, J. Rozen, S. Wang, R. D. Schrimpf, D. M. Fleetwood, S. T. Pantelides, J. R. Williams, and L. C. Feldman, *IEEE Transactions on Nuclear Science* **53**, 3687 (2006).

[4] R. Singh and A. R. Hefner, *Solid State Electronics* **48**, 1717 (2004).

[5] D. K. Schroder and J. A. Babcock, *Journal of Applied Physics* **94**, 1 (2003).

[6] T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and D.-L. Kwong, *IEEE Electron Device Letter* **24**, 150 (2003).

[7] A. E. Islam, G. Gupta, S. Mahapatra, A. T. Krishnan, K. Ahmed, F. Nouri, A. Oates, and M. A. Alam, Gate leakage vs. NBTI in plasma nitrided oxides: characterization, physical principles, and optimization, in *Proceedings of the International Electron Devices Meeting*, 2006.

[8] P. T. Lai, J. P. Xu, and Y. C. Cheng, *IEEE Transactions on Electron Devices* **46**, 2311 (1999).

[9] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, *Microelectronics Reliability* **45**, 19 (2005).

[10] D. S. Ang and S. Wang, *IEEE Electron Device Letters* **27**, 914 (2006).

[11] J. B. Yang, T. P. Chen, S. S. Tan, C. M. Ng, and L. Chan, *Journal of The Electrochemical Society* **154**, G255 (2007).

[12] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam, *IEEE Transactions on Electron Devices* **54**, 2143 (2007).

[13] S. Wang, S. Dhar, S.-r. Wang, A. C. Ahyi, A. Franceschetti, J. R. Williams, L. C. Feldman, and S. T. Pantelides, *Physical Review Letters* **98**, 026101 (2007).

[14] F. J. Feigl, W. B. Fowler, and K. L. Yip, *Solid State Communications* **14**, 225 (1974).

[15] K. Chatty, V. Khemka, T. P. Chow, and R. J. Gutmann, *Journal of Electronic Materials* **28**, 161 (1999).

[16] K. McDonald, M. B. Huang, R. A. Weller, L. C. Feldman, J. R. Williams, F. C. Stedile, I. J. R. Baumvol, and C. Radtke, *Applied Physics Letters* **76**, 568 (2000).

[17] H. Yano, Y. Furumoto, T. Niwa, T. Hatayama, Y. Uraoka, and T. Fuyuki, *Materials Science Forum* **457**, 1333 (2004).

[18] A. Yankova, L. Do Thank, and P. Balk, *Solid-State Electronics* **30**, 939 (1987).

[19] G. J. Dunn and P. W. Wyatt, *IEEE Transactions on Nuclear Science* **36**, 2161 (1989).

[20] S. Dhar, L. C. Feldman, K. C. Chang, Y. Cao, L. M. Porter, J. Bentley, and J. R. Williams, *Journal of Applied Physics* **97**, 074902 (2005).

[21] K. C. Chang, Y. Cao, L. M. Porter, J. Bentley, S. Dhar, L. C. Feldman, and J. R. Williams, *Journal of Applied Physics* **97**, 104920 (2005).

[22] K. McDonald, L. C. Feldman, R. A. Weller, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2257 (2003).

[23] K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, and J. R. Williams, *Journal of Applied Physics* **93**, 2719 (2003).

[24] S. Dhar, Y. W. Song, L. C. Feldman, T. Isaacs-Smith, C. C. Tin, J. R. Williams, G. Chung, T. Nishimura, D. Starodub, T. Gustafsson, and E. Garfunkel, *Applied Physics Letters* **84**, 1498 (2004).

[25] H. Li, S. Dimitrijev, D. Sweatman, H. B. Harrison, P. Tanner, and B. Feil, *Journal of Applied Physics* **86**, 4316 (1999).

[26] P. Jamet, S. Dimitrijev, and P. Tanner, *Journal of Applied Physics* **90**, 5058 (2001).

[27] V. V. Afanas'ev, A. Stesmans, M. Bassler, G. Pensl, and M. J. Schulz, *Applied Physics Letters* **76**, 336 (2000).

[28] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, *Applied Physics Letters* **82**, 568 (2003).

[29] P. M. Lenahan and P. V. Dressendorfer, *Journal of Applied Physics* **55**, 3495 (1984).

[30] J. P. Campbell, P. M. Lenahan, C. J. Cochrane, A. T. Krishnan, and S. Krishnan, *IEEE Transactions on Device and Materials Reliability* **7**, 540 (2007).

[31] J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Applied Physics Letters* **91**, 133507 (2007).

# CHAPTER VII

# ACCELERATED BREAKDOWN OF THERMAL OXIDES GROWN ON IMPLANTED SiC

## Overview

During the fabrication of SiC power DMOSFETs, dopant implantation is required to form the base and the source regions. The subsequent high temperature activation anneal induces surface roughness if the substrate is left unprotected. It is shown in this chapter that the mean time to failure (MTTF) of oxide-based devices, extracted from time-dependent dielectric breakdown (TDDB) measurements, is limited by the surface roughness of the substrate prior to the thermal growth of the gate dielectric. Two techniques are shown to independently improve the long-term reliability by allowing for a smoother surface: carbon capping during the dopant activation, and post-annealing chemical-mechanical polishing.

## 7.1 Motivation

As reviewed in Chapter II (Section 2.3), various injection mechanisms are the cause of excess current in a gate oxide atop a semiconductor surface. The case of $SiO_2$ thermally grown on 4H-SiC is of particular interest in this regard. On one hand, SiC has advantages over Si for some high voltage and high temperature applications as it possesses a larger breakdown field and remains an extrinsically doped semiconductor up to about 1300 °C, as opposed to about 400 °C for silicon. On the other hand, both the achievable blocking voltage of a power MOSFET and its ON resistance are limited by the allowable oxide field, determined by the reliability of the gate dielectric (see Sections 1.2 and 1.3.2). Indeed, in the blocking state, the oxide field can be several times the one present in the semiconductor because of the ratio of the dielectric constants, implying that field in the PN junction can be

limited by the dielectric strength of the oxide and not by the critical field of the semiconductor. In the ON state, the saturation current scales with the gate bias, so that the oxide field once again can limit the efficiency of the device. The concerns about the reliability of $SiO_2$ on 4H-SiC originate from the small band offsets between the wide band-gap semiconductor and the dielectric: approximately 2.7 and 2.9 eV separate the conduction bands and the valence bands respectively. Furthermore, the effective carrier injection barriers can be even lower because of the presence of defects and because of high temperature operation which enhances emission.

Three consequences of oxide charge trapping, resulting from carrier injection, can be used to determine the maximum allowable oxide field: the stability of the characteristics voltage (see Chapters IV, V and VI), the reduction of the channel mobility, and the mean time to failure (MTTF). Failure occurs when the oxide trapped charge reaches a threshold inducing dielectric breakdown. Previous studies on SiC-based devices reveal that to achieve a MTTF greater than 100 years, the oxide field cannot exceed 3 to 5 MV/cm at 150 °C.[1,2,3] Although this is true for a variety of SiC substrates and processing conditions, it is important to mention some factors affecting the MTTF: (i) substrate doping, (ii) post-oxidation annealing, and (iii) surface roughness. (i) Doping matters because the nature and the charging kinetics of electron and hole traps in the oxide are different. In particular, it was shown that the MTTF of nitrided oxides on p-type SiC is lower than on n-type SiC biased into accumulation.[2,3] In light of the results presented in Chapters V and VI, it indicates that the large N-related oxide hole trap density could limit the stability as well as the long-term reliability of a device. (ii) Nitridation of the gate oxide has been shown to increase the MTTF of oxides subject to electron injection from the semiconductor; i.e. n-type SiC MOS capacitors in accumulation and n-channel SiC MOSFETs in the ON state.[2] This correlates with the conclusions of Chapter IV which state that the generation of acceptor states (electron traps) at the interface is suppressed following NO annealing.

The impact of surface roughness (iii) on the MTTF is a concern because of the high temperature anneals ($\simeq$ 1500 °C) required to activate the dopants following the double implant that forms the base (channel region) and and the source in a SiC DMOSFET. During the anneal, both surface atom emission and step bunching can occur leading to a very rough surface on which the gate oxide is subsequently grown by thermal oxidation. Activation anneals are usually performed in an inert gas but residual oxygen can lead to the removal of Si and/or C by the formation of SiO and/or CO (gas) molecules, this process is called active oxidation, as opposed to passive oxidation (i.e. oxide growth). Indeed, active oxidation occurs at high temperatures and low oxygen pressures. At 1500 °C, atom emission from the SiC surface occurs for residual oxygen pressure less than about 10 torr ($\simeq$ 0.01 atm).[4,5] Note that it is to preserve the integrity of the SiC surface that SiC wafers are usually ramped up to the desired temperature in oxygen, prior to thermal growth. In Chapter I (Section 1.3.1), it was mentioned that the SiC wafers are commonly synthesized off-axis to avoid polytype inclusions, and therefore possess surface steps. At high temperatures, the diffusion of surface atoms is enabled, leading to the formation of larger features, a phenomenon called step-bunching. It has been shown that the roughness following the implant anneal can reduce the MTTF of devices by order of magnitudes.[3] In addition, it is detrimental to the channel mobility. Therefore it is desirable to implement techniques limiting atom emission and diffusion at high temperatures. In fact, it was shown recently that the roughening can be suppressed by performing the activation annealing in $SiH_4$ overpressure,[6] or with an AlN cap,[7] or using rapid thermal annealing (RTA).[8]

In this chapter, two other processes are investigated: Ar activation anneals in the presence of a carbon cap and chemical-mechanical polishing (CMP) of uncapped surfaces after the anneal. The roughness is characterized using atomic force microscopy (AFM) and the MTTF is determined by time-dependent dielectric breakdown (TDDB) measurements performed at 150 °C on MOS capacitors formed on the (0001) Si-face of n-type 4H-SiC biased in accumulation ($\xi_{ox} \simeq 6.5$ MV/cm). It is shown that both the use of a carbon cap and

CMP can reduce the surface roughness, leading to a MTTF similar to the one measured for oxides grown on a smooth un-implanted (epitaxial) SiC surface. The results obtained on capacitors can be directly extended to n-channel DMOSFETs in the ON state as previously demonstrated.[2]

The TDDB technique is first briefly introduced. It is followed by the description of the experimental methods and by the presentation of the results.

### 7.2 Time-Dependent Dielectric Breakdown

During TDDB measurements, a series of devices are biased in parallel and the cumulative fraction of the ones having failed is recorded as a function of time at a given gate oxide field. The MTTF is then obtained and the results are extrapolated to operating conditions.

In order to obtain data within reasonable time, say a few days or a few weeks, the TDDB measurements are performed at oxide fields high enough so that the excess current is not negligible. To show the different conduction regimes, a plot of the current density measured as a function of oxide field obtained on a single n-type MOS capacitor in accumulation is shown in Figure 7.1(a). At low fields, only a small leakage current is measured. During operation, it is that current that ultimately leads to device failure via excess carrier trapping in the oxide. At high enough field, Fowler-Nordheim (FN) tunneling, which depends exponentially on the gate bias, tends to dominate (see Section 2.3.4). It is that regime that is used for TDDB measurements as the fluence of injected carrier can be orders of magnitude more than at low fields. For still greater oxide fields, impact ionization can occur and the current increases even faster (see Section 2.1). Ultimately, the field is so high that the hot carriers induce damage in the oxide, yielding destructive breakdown.

The extent of the FN regime and the shape of the curve depends on the effective barrier height for carrier injection. As a result, plots such as the one shown in Figure 7.1(a) can be used to determine this barrier and to compare it to the relevant band offset. For example the energy barrier for electron injection measured on oxides grown on the Si-face of 4H-SiC

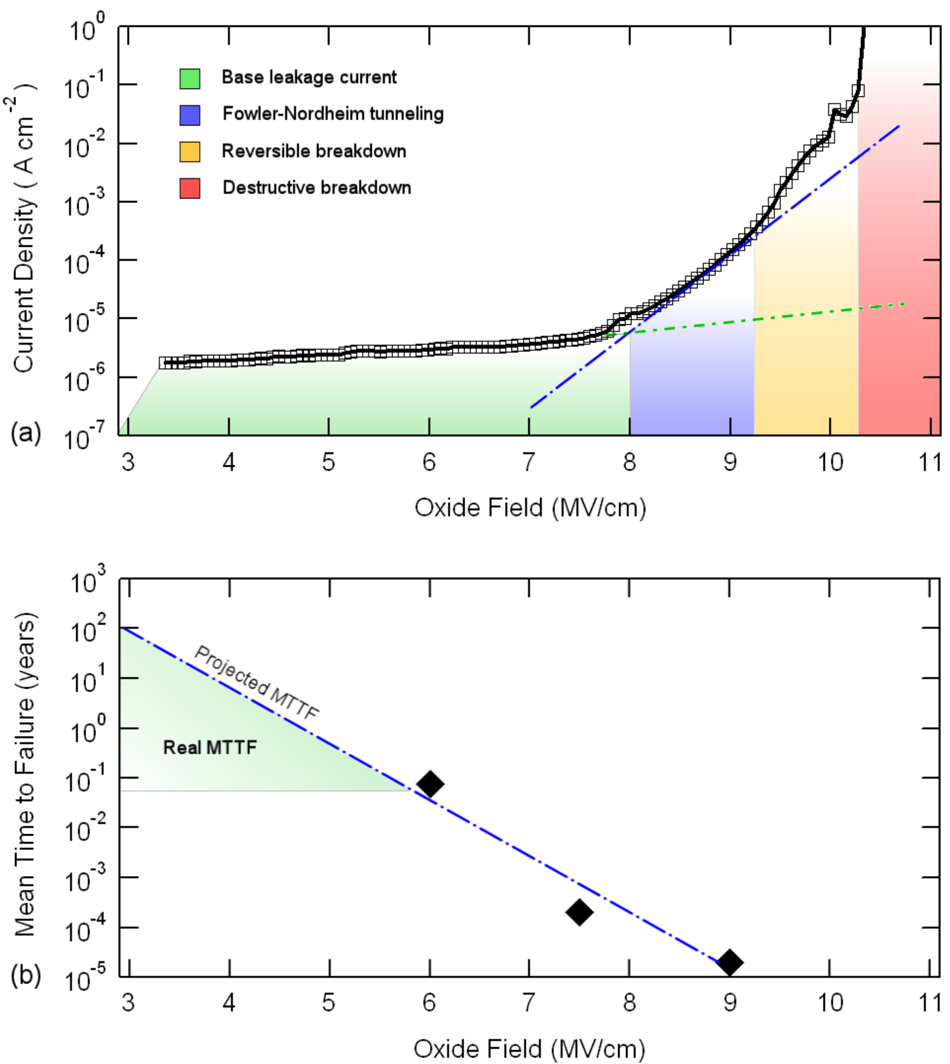



**Figure 7.1:** (a) Different regimes in a current density vs. oxide field curve taken at room temperature on a NO-annealed oxide grown on the (0001) Si-face of epitaxial n-type (N doping $\simeq 5{\times}10^{15}$ cm$^{-3}$) 4H-SiC biased in accumulation. During TDDB measurements, accelerated breakdown is obtained by using fields high enough so that Fowler-Nordheim (FN) tunneling occurs. Note that in a state of the art device the base leakage current can be orders of magnitude less, so that the FN tunneling starts around 6 MV/cm. (b) Extrapolation of the MTTF at lower fields corresponding to operating condition. The data shown was measured on nitrided oxides at 145 °C with poly-Si gate contacts [substrate same as in (a)].

is found to be about 2.6 eV for both as-oxidized and NO-annealed $SiO_2$, close to the 2.7 eV conduction band offset measured by internal photoemission.[9] Interestingly, only nitrided oxides grown on the C-face of 4H-SiC possess low enough base leakage current so that a clear FN regime is observed. However, the extracted barrier height is only about 2.2 eV, suggesting that even in the latter case, the high density of interface defects yields trap-assisted tunneling. This is another reason why oxides grown on the Si-face are preferred for devices as their corresponding MTTF is orders of magnitude larger. It should be noted that injection barrier heights extracted using FN tunneling are subject to errors for two main reasons. First, the effective mass of carriers in the oxide, used in the calculation, has not been determined with great precision and the available values span an order of magnitude.[10] Second, as the charge distribution in the oxide is not known, the calculated electric field could be very different from the actual local field the interface where injection takes place. The field induced by a gate bias $V_g$ is estimated by

$$\xi_{ox} = \frac{V_g - \phi_{ms}}{x_{ox}} \tag{7.1}$$

where $x_{ox}$ is the oxide thickness and $\phi_{ms}$ is the work function difference between the gate contact and the semiconductor. In an ideal charge-free oxide, the flatband voltage $V_{fb}$ equals the work function difference so that when $V_g = V_{fb}$, the field in the oxide is zero. However, in the presence of oxide charge or even interface states, the field is no longer negligible in the oxide at flatband ($V_{fb} \neq \phi_{ms}$) because the charge has to be mirrored entirely in the metal. In Eq.(7.1), it is assumed that the charge is localized at the oxide/semiconductor interface, which is not always true. The consequences of the oxide field uncertainty also extends to the results of TDDB measurements.

As mentioned above, several devices are monitored at the same time during TDDB measurements. One device is considered ”failed” when a threshold current is measured through the corresponding gate oxide. The cumulative fraction of biased dots that has failed is then extracted as a function time. There are three classes of devices: the ones that

were bad to start with, the ones experiencing "extrinsic" breakdown (early failure), and the ones experiencing "intrinsic" breakdown (only limited by the oxide properties).[1] If a structural defect is present in the substrate, it can overlap with the gate area of a particular device yielding extrinsic breakdown. The mechanism referred to as "intrinsic" breakdown is also defect-mediated but the defects are inherent to a particular fabrication scheme. Accordingly, the fraction of "intrinsic" devices increases when the gate area is reduced as the probability for the active region to overlap with a structural defect becomes small. The mean time to failure is extracted by isolating the "intrinsic" breakdown distribution and by estimating the time at which half those devices have failed.

The MTTF can be measured at various oxide fields within the extent of the FN regime. At a given temperature, the failure time can then be extrapolated to smaller fields to estimate the MTTF at operating conditions, as illustrated in Figure 7.1(b). The extrapolation is usually made using the assumption that the MTTF depends exponentially on the field (blue line). However, it should be realized that this is reasonable only within the extent of the FN regime. Because of the presence of a base leakage current, the low field MTTF is expected to be overestimated by such an approximation. Consequently, the real MTTF lies somewhere between the exponential approximation and the highest value measured experimentally (green region).

In the study of the impact of the surface roughness on the MTTF presented below, such an extrapolation is not necessary because all samples are compared at a given oxide field.

## 7.3 Experiments

The (0001) Si-face of 4H-SiC substrates obtained from Cree Inc. were used for the experiments. They possess a 10 $\mu$m n-doped (N $\simeq 5\times10^{15}$ cm$^{-3}$) epitaxial layer. Some samples were subject to a series of implants (100 keV to 700 keV) in order to obtain a N concentration around $10^{20}$ cm$^{-3}$ extending within 1 $\mu$m from the SiC surface. Those samples were then annealed at 1550 °C to activate the dopant. During the anneal, one

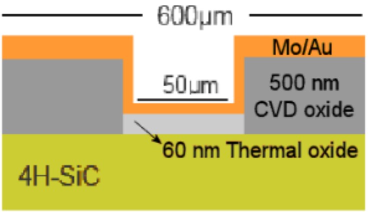
**Table 7.1:** Samples used for roughness and TDDB measurements.

| Sample label | Doping | Surface treatment |
|---|---|---|
| *Epi* | $n^-$ epitaxial | none |
| *Rough* | $n^+$ implanted | 1550 °C anneal |
| *Polished* | $n^+$ implanted | 1550 °C anneal then CMP |
| $C - cap$ | $n^+$ implanted | 1550 °C anneal with C-cap |

set of samples was protected by a carbon cap obtained by baking out a spin-coated photoresist (label = $C - cap$).[11] Of the samples annealed without a cap, some were subsequently polished by CMP (label = *Polished*) at NovaSiC (Chambery, France). The others were left with their roughened surface (label = *Rough*). Un-implanted and un-annealed samples were also used as control (label = *Epi*). The various samples are listed in Table 7.1.

The nitrogen profile was characterized by secondary ion mass spectroscopy (SIMS). The root-mean-square (RMS) roughness of the (0001) surface resulting form the previous treatments was measured by atomic-force microscopy (AFM) using a Nanoscope from Digital Instruments. In the case of the protected samples, the carbon cap was first removed by a low temperature re-oxidation.

For TDDB measurements, MOS capacitors were fabricated on RCA cleaned 1×1 cm substrates after implantation and activation anneal, as illustrated in Figure 7.2. First, a 500 nm field oxide was formed by chemical vapor deposition (CVD) at Northrop Grumman Corp. Using photo-lithography and buffered hydrofluoric acid (BOE), circular 50 $\mu$m diameter windows were then opened in the thick oxide to expose the SiC surface. Subsequently, thermal oxides were grown in flowing oxygen at 1150 °C and passivated in NO for 2 hours at 1175 °C. The target gate oxide thickness was approximately 60 nm. Finally, circular 600 $\mu$m gate contacts were deposited by successive plasma sputtering of Mo and Au. Each TDDB sample contains 36 of the fabricated MOS capacitors (orange). In addition, 9 large area



(a) Single Capacitor

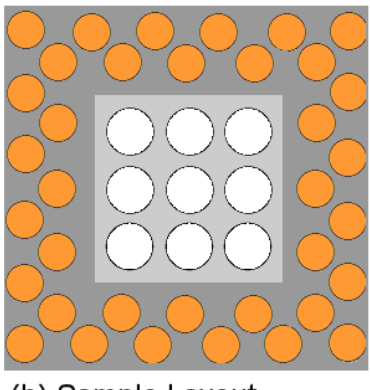

(b) Sample Layout

**Figure 7.2:** (a) Cross-section of a single MOS capacitor with a small area gate oxide. (b) Sample layout containing 36 devices for TDDB measurements and 9 large area devices for capacitance measurements.

capacitors (white) were formed in the center (no field oxide), so that capacitance-voltage (CV) measurements could be performed to determine the exact thermal oxide thickness using a Keithley model 82 setup. The back of the samples were etched to expose the SiC surface and allow electrical contact.

A schematic of the TDDB electrical connections is shown in Figure 7.3. Prior to a measurement, a sample was placed on a thermally insulated hot chuck which temperature was raised to 150 °C via a Eurotherm unit controlling a plate heater. The Cu chuck served as the negative electrode and ohmic contact with the back side of the SiC sample was ensured by the use of a colloidal Ag solution. Each capacitor was connected to the Hi output of the power supply (Keithley 228A) using a probe card custom made by Alpha-Probe Inc. The positive gate bias was set to correspond to an oxide field of 6.5 MV/cm, using Eq.(7.1). The current in each device was measured by a digital multi-meter (Keithley 193). This was

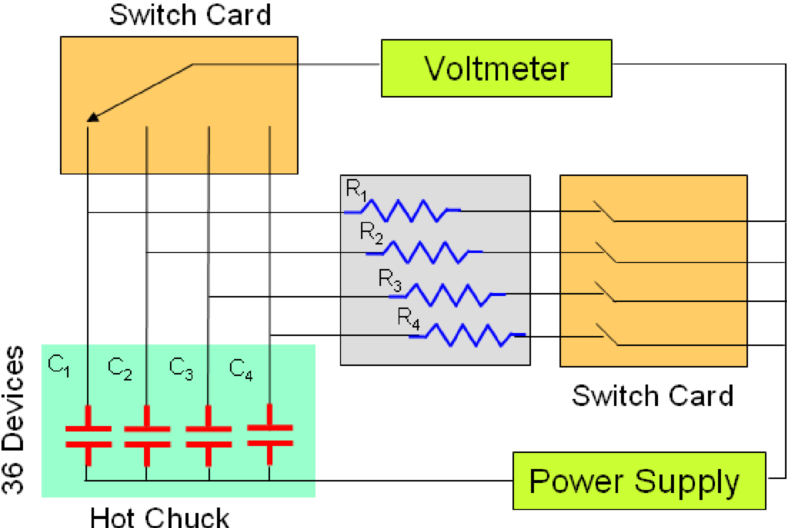



**Figure 7.3:** Schematic of the TDDB electrical connections. The units are controlled by a custom LabVIEW program allowing remote monitoring and yielding the cumulative percent failure as a function of time.

done by successively probing the voltage drop across 10 kΩ resistors placed in series with the capacitors using switch cards (Keithley 7053) powered by a scanner (Keithley 706). The units were controlled by a custom LabVIEW program designed for data acquisition and remote monitoring. The soaking time was set so that all dots were measured at least once every 40 seconds in the early stage of the measurements. When the current exceeded 0.088 A/cm$^2$ across a particular capacitor up to three consecutive times, it was considered failed, removed from the measurement, and electrically disconnected to avoid local Joule heating. The compiled data yielded the cumulative percent failure as a function of stress time. Further details on the implemented TDDB setup can be found in Appendix C.

## 7.4 Results and Discussion

Images of the implanted and annealed samples are shown in Figure 7.4. The roughness of the (0001) SiC surface is also indicated. The *Rough* sample possesses the largest RMS value of approximately 6 nm as both surface diffusion and surface atom emission were enabled during the high temperature dopant activation. The sample protected by the carbon cap

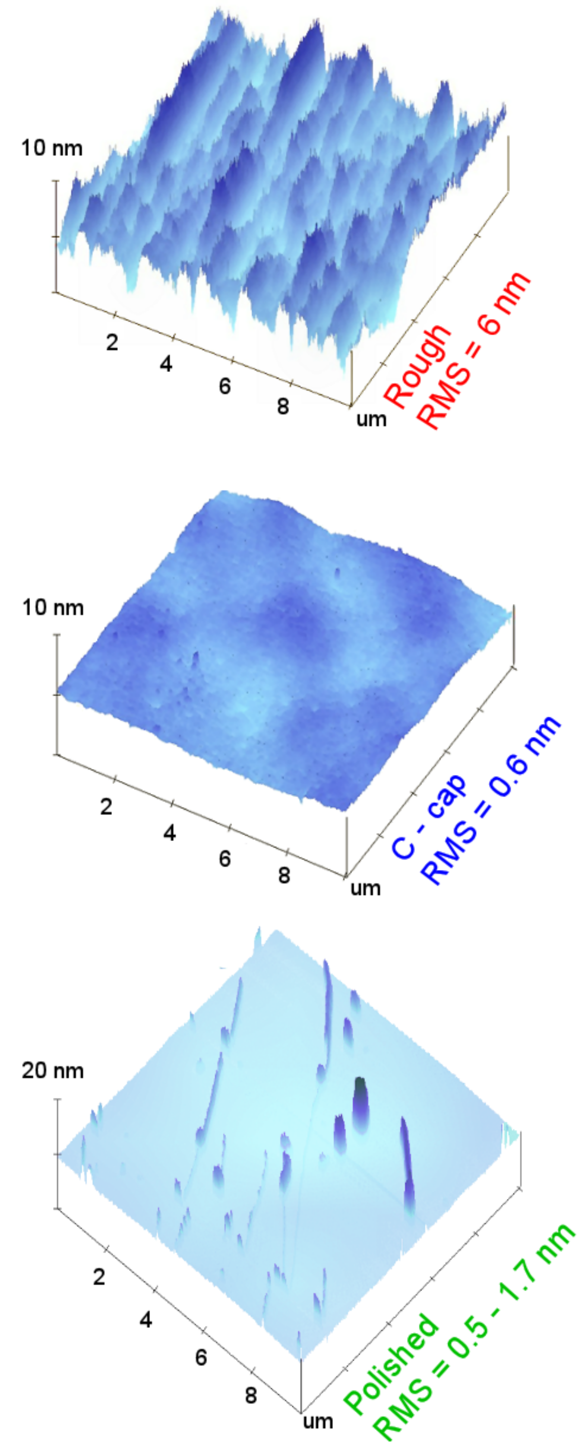



**Figure 7.4:** AFM images of the (0001) SiC surface of implanted samples after activation anneal. The extracted RMS roughness is indicated next to each 10×10 $\mu$m scan.

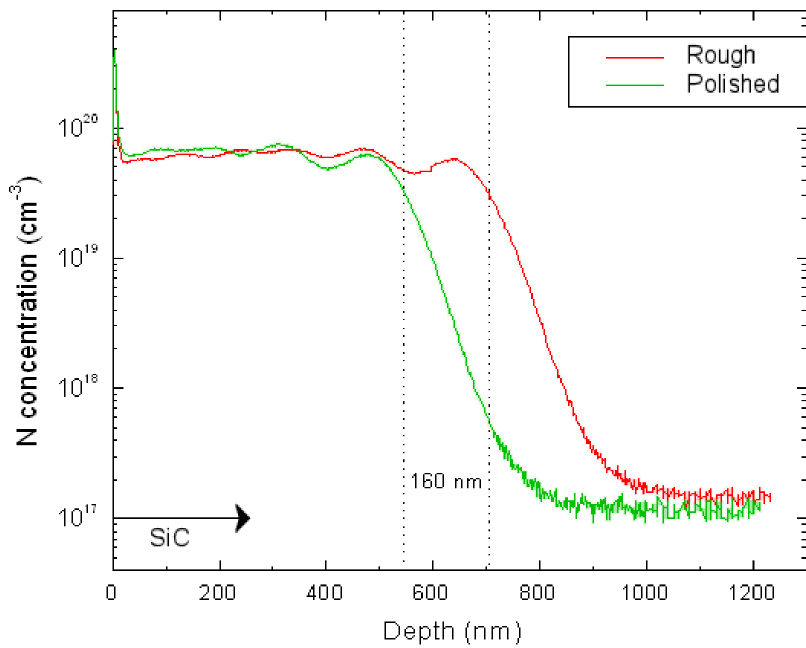



**Figure 7.5:** SIMS profile of the nitrogen concentration in implanted SiC samples. The CMP process removed about 160 nm of material.

exhibits a 0.6 nm roughness, which is similar to the one of the *Epi* sample (not shown). The carbon layer prevented both emission and surface reconstruction. The *Polished* surface corresponds to the *Rough* surface following CMP. It can be seen that it is overall smoother although some local non-uniformities increase the average roughness from 0.5 to 1.7 nm.

The amount of material removed by the polishing process can be deduced from the N SIMS profile shown in Figure 7.5. In the *Rough* sample, the nitrogen implant led to a constant dopant density of about $6\times10^{19}$ cm$^{-3}$ up to 650 nm into the semiconductor. After polishing, the shift of the profile reveals that about 160 nm of material was removed. Since the non-uniformities observed on the SiC surface of the *Polished* sample are of the order of 10 nm high, it can be concluded that these features are induced by the CMP process and are not remains of the *Rough* surface.

A series of MOS capacitors fabricated on each surface was tested using TDDB measurements at 150 °C. To calculate the positive gate bias necessary to induce an estimated oxide

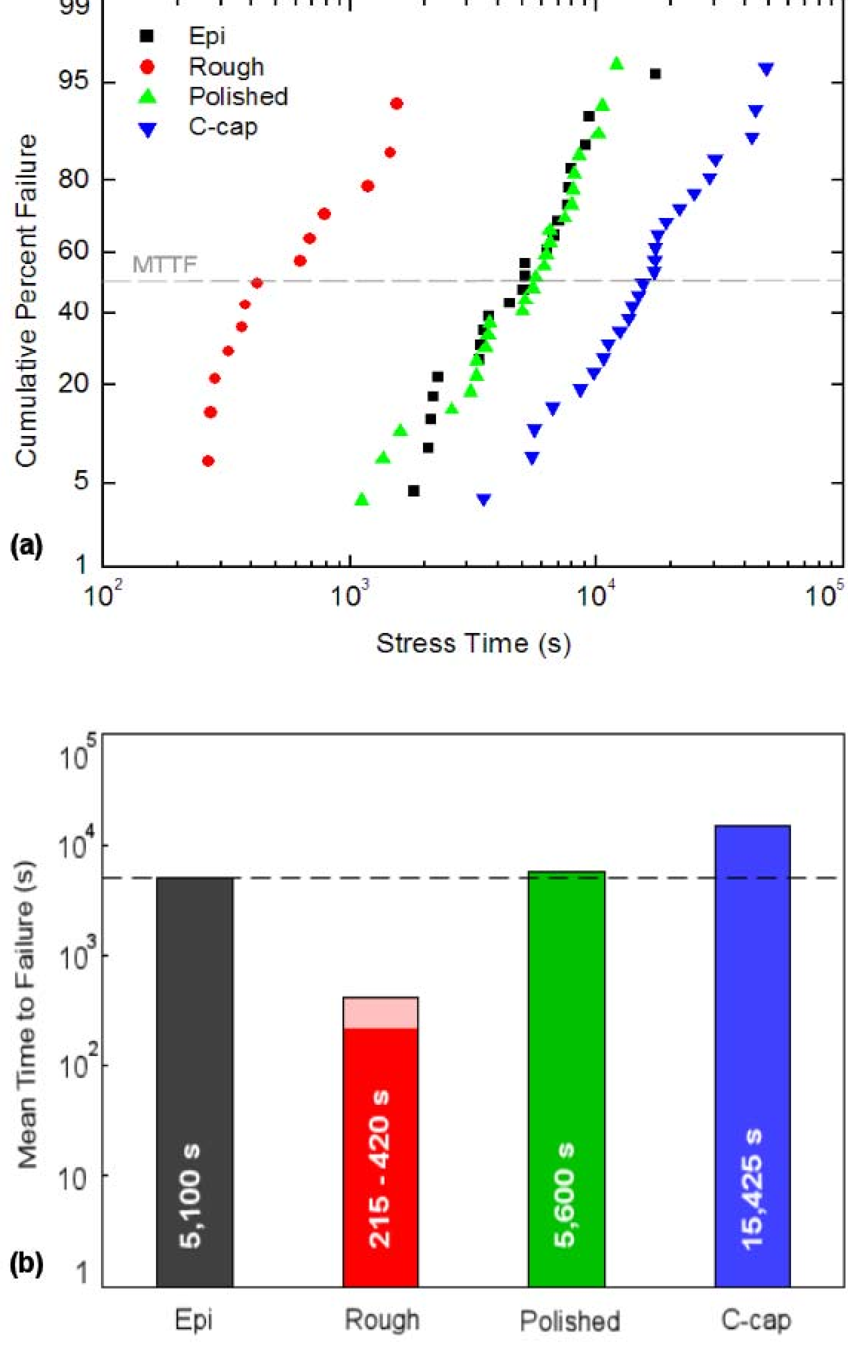



**Figure 7.6:** (a) Cumulative percent failure as a function of stress time compiled from the "intrinsic" breakdown events. (b) Mean times to failure of devices fabricated on the different surfaces.

field of 6.5 MV/cm, using Eq.(7.1), the capacitance of large area devices was first measured to determine the thermal oxide thickness. Although all samples were oxidized together, it appears that the implanted samples ($x_{ox} \simeq 57$ nm) resulted in a slightly faster growth rate than the *Epi* sample ($x_{ox} \simeq 50$ nm).

The "intrinsic" breakdown events for each sample were isolated by assuming a Weibull distribution function for the failure probability.[12] This yields a line on a probability plot of the cumulative percent failure vs. time on a logarithmic scale.[1] The re-normalized data is shown in Figure 7.6(a). The mean time to failure was then extracted from the time at which half the "intrinsic" devices had failed in each sample. The results are shown in Figure 7.6(b). The uncertainty of the MTTF for the *Rough* sample originate from the overlap between the "extrinsic" and "intrinsic" events due to the fast degradation of even the best devices on that surface. Note that for all the other samples, it was found that nearly all breakdown events were "intrinsic", indicating that a gate with a 50 $\mu$m diameter is a viable choice. This confirms other recent observations.[13]

Clearly, the MTTF increases when the surface roughness of implanted SiC surfaces is reduced. In particular, the *Rough* sample yields a MTTF more than one order of magnitude smaller than all the others, in agreement with previous studies.[3] The *Polished* and the $C-cap$ samples lead a MTTF of the same order as the *Epi* sample. The smaller MTTF on the *Polished* surface, when compared to the $C-cap$ surface, could be due to the non-uniformities observed by AFM. As for the *Rough* sample, sharp features are likely to induce defects and/or field variation in the thermal oxide, accelerating breakdown.

### 7.5 Summary

It was shown in this chapter that the long-term reliability of devices fabricated on implanted SiC depends on the dopant annealing conditions and on the subsequent surface treatment. Indeed, the mean time to failure extracted from TDDB measurements is inversely proportional to the RMS roughness calculated from AFM scans.

Two techniques were successfully used to reduce the roughness on implanted surfaces. It was demonstrated that a protective carbon layer can prevent surface reconstruction, yielding a roughness similar to the one of an un-annealed sample. Also, chemical-mechanical polishing was used after dopant annealing of an unprotected surface, yielding a smoother surface. However, some uniformities were observed in that case.

As the carbon capping leads to the smoothest surface, to the largest MTTF, and is the easiest to implement, it should be adopted in the fabrication of oxide-based SiC devices requiring implantation so that their lifetime can be increased by at least an order of magnitude.

## References


[1] M. M. Maranowski and J. A. Cooper Jr, *IEEE Transactions on Electron Devices* **46**, 520 (1999).

[2] S. Krishnaswami, M. K. Das, A. K. Agarwal, and J. W. Palmour, *Materials Research Society Symposium Proceeedings* **815**, J8.4 (2004).

[3] S. Krishnaswami, S.-H. Ryu, B. Heath, A. Agarwal, J. Palmour, B. Geil, A. Lelis, and C. Scozzie, *Materials Science Forum* **527-529**, 1313 (2006).

[4] Y. Song, *Ph.D. Thesis*, The City University of New York, 2001.

[5] Y. Song and F. W. Smith, *Applied Physics Letters* **81**, 3061 (2002).

[6] I. Sankin, J. B. Casady, J. B. Dufrene, W. A. Draper, J. Kretchmer, J. Vandersand, V. Kumar, M. S. Mazzola, and S. E. Saddow, *Solid State Electronics* **45**, 1653 (2001).

[7] K. A. Jones, P. B. Shah, K. W. Kirchner, R. T. Lareau, M. C. Wood, M. H. Ervin, R. D. Vispute, R. P. Sharma, T. Venkatesan, and O. W. Holland, *Materials Science and Engineering* **B61**, 281 (1999).

[8] J. Senzaki, S. Harada, R. Kosugi, S. Suzuki, K. Fukuda, and K. Arai, *Materials Science Forum* **389-393**, 795 (2002).

[9] V. V. Afanasev, M. Bassler, G. Pensl, M. J. Schulz, and E. S. von Kamienski, *Journal of Applied Physics* **79**, 3108 (1996).

[10] V. V. Afanas'ev and A. Stesmans, *Applied Physics Letters* **77**, 2024 (2000).

[11] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, *Materials Science Forum* **457-460**, 933 (2004).

[12] W. Weibull, *Journal of Applied Mechanics* **18**, 293 (1951).

[13] J. Senzaki, A. Shimazoto, M. Okamoto, K. Kojima, K. Fukuda, H. Okumura, and K. Arai, Gate-area dependence of SiC thermal oxides reliability, in *Proceedings of the International Conference on Silicon Carbide and Related Materials, Otsu Japan*, 2007.

# CONCLUSION

The findings associated with this thesis have added to the understanding of the $SiO_2$/SiC interface. Physical mechanisms associated with oxide and interface properties have been proposed, and practical solutions to some processing issues were demonstrated. This work therefore contributes in several ways to the wider research effort toward the realization of reliable SiC oxide-based devices. The main conclusions are gathered below.

*Oxidation Rate and Temperature (Chapter III)*

The implementation of an oxidation setup in which the pressure can be adjusted between 0.25 and 4 atm, allowed to study thermal oxide growth kinetics on SiC. The linear-parabolic model, developed by Deal and Grove for silicon, was found to apply to the $SiO_2$/SiC system. However, a few outstanding anomalies were identified. First, the model does not describe oxidation kinetics below a critical thickness, which is estimated to be about 35 nm, same as on Si. Like on silicon, this value appears independent of substrate orientation, oxygen partial pressure, and growth temperature. It indicates that the fast-growth regime is a property of $SiO_2$ alone. This conclusion could help understand the physics of the accelerated process. Second, it is found that the growth rate scales with oxygen pressure, as expected from Henry's law, up to 2 atm. Interestingly, at 4 atm the pressure dependence appears sublinear on the (0001) Si-face of 4H-SiC. This could be the result of another oxidation mechanism starting to dominate, or of the deviation from equilibrium kinetics.

Varying the oxidation pressure also allows for the decoupling of the growth rate and temperature. Their respective impact on the electrical properties of the $SiO_2$/SiC interface could then be studied separately. On one hand, it was shown that increasing the rate does not yield a lower density of interface states between 0.2 and 0.6 eV from the 4H-SiC conduction band edge. On the other hand, increasing the temperature from 1000 to 1150 °C, greatly reduces the interface state density within that energy window.

As a processing tool, a high pressure oxidation station enables SiC device fabrication at lower temperature and/or for shorter time, reducing the thermal budget.

*Nitrogen Impact on Performance and Reliability (Chapters IV to VI)*

The impact of nitrogen at the $SiO_2$/SiC interface on the stability of oxide-based device properties was investigated using accelerated injection of electrons and holes. In addition, the variation of the incorporated nitrogen density was used to study the processes associated with interface passivation and its degradation upon operation.

Nitrogen is found to be solely responsible for the large reduction of interface states in the upper part of the 4H-SiC band-gap. The $D_{it}$ is minimized prior to nitrogen saturation which occurs around $6{\times}10^{14}$ cm$^{-2}$, as deduced from SIMS measurements. It reveals that a large amount of nitrogen, that is not necessary to interface state passivation, is incorporated in the oxide, yielding a thin ($< 1$ nm) SiON transition layer between SiC and $SiO_2$. This excess nitrogen can be detrimental to the reliability of the oxide.

Electrons were injected in the gate oxide of MOS capacitors from the metal using internal photoemission. It was found that the flatband voltage stability, observed in nitrided samples, is due to the suppression of interface state generation upon injection. In unpassivated oxides, precursor defects are thought to act as electron traps, whose relaxation upon capture yields acceptor states within the 4H-SiC band-gap. The density of induced electron traps is found to be reduced by progressive incorporation of nitrogen in a way similar to $D_{it}$ reduction. This suggests that nitrogen makes electrically inactive precursor defects that would otherwise lead to the generation of interface states.

Holes were injected at high oxide fields by Fowler-Nordheim tunneling, and at low oxide fields by X-ray and VUV irradiation. All techniques indicate a drawback of nitrogen incorporation via NO annealing; it leads to a large amount of hole traps in the oxide, likely in the near interface region. This effect can be directly related to nitrogen as the positive charge trapping rate scales linearly with the incorporated nitrogen density up to N saturation. The

excess nitrogen forming the SiON transition layer, not necessary to interface passivation, could be responsible. First-principle calculations attribute the effect to the bonding of nitrogen in the oxide, which is proposed to yield a lone pair state in the lower part of the SiC band-gap. This singly occupied state is thought to act as a hole trap.

These important observations demonstrate that the standard NO annealing step should be optimized to limit the incorporated nitrogen so that both interface state and hole trap densities are minimized. Indeed, excess nitrogen should be avoided in order to enhance the reliability of SiC oxide-based devices.

*Implant-Related Surface Roughness and Device Failure (Chapter VII)*

Time-dependent dielectric breakdown measurements revealed that when gate oxides are thermally grown on a rough implanted SiC surface, their mean time to failure can be reduced by one order of magnitude when compared to devices fabricated on smooth surfaces. The roughening of the surface, during the high temperature implant anneal, can be prevented by protecting the SiC surface with a carbon cap, obtained by baking out a spin-coated photo-resist. Another technique that can be used is chemical-mechanical polishing of the semiconductor after activation annealing. However some non-uniformities of the polishing process appeared to affect the lifetime of the devices. Accordingly, carbon capping, the easiest solution to implement, should be adopted in the fabrication process of SiC-based devices in order to enhance their long-term reliability.

# APPENDICES

## DESCRIPTION OF THE IMPLEMENTED SETUPS

Appendix A: Oxidation station 174
Appendix B: Automated carrier injection 188
Appendix C: TDDB setup 194

# APPENDIX A

# OXIDATION STATION

As illustrated in Figures A.1 to A.3, the oxidation station built for $SiO_2$ growth on SiC consists of a 2" diameter tube placed in a three-zone split furnace with a 6" long hot zone. The feeding lines are made of stainless steel and the exhaust lines are made of PFA which enables the use of corrosive gases. Gas tanks of nitric oxide (NO) and hydrogen chloride (HCl) are placed in a gas cabinet that also possesses a reserve for hydrogen ($H_2$). A purging system was included in the gas regulating panels. Oxygen ($O_2$), argon (Ar), and nitrogen ($N_2$), can also be fed to the quatz tube. The flow of oxidizing, annealing, and passivating gases, can be regulated by electronically actuated mass-flow controllers. Also, the tube is connected to a vacuum pump to prevent contamination and enable low pressure processing.

A thick quartz tube can be placed in the furnace and can be connected to an alternative exhaust panel so that oxidations at pressures up to 4 atmospheres can be performed.

This appendix gathers pictures and schematics of the setup. The constituents of the oxidation station, listed in Figure A.4, are divided in four groups, so that they can be described separately: furnace & tube, feeding lines, vacuum line, and exhaust lines. Finally, the extra components needed for variable pressure oxidation are introduced.

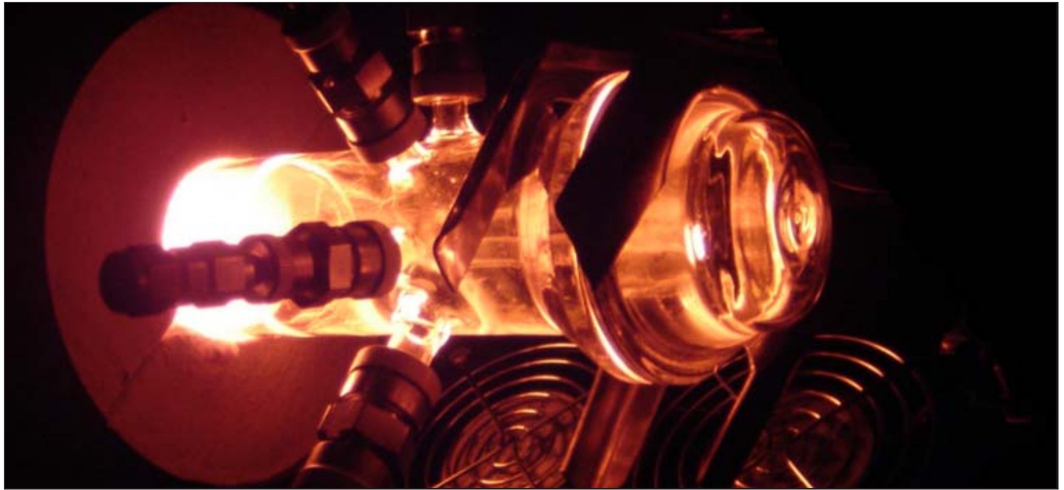


**Figure A.1:** Quartz tube at high temperature. Feeding and vacuum lines are seen.

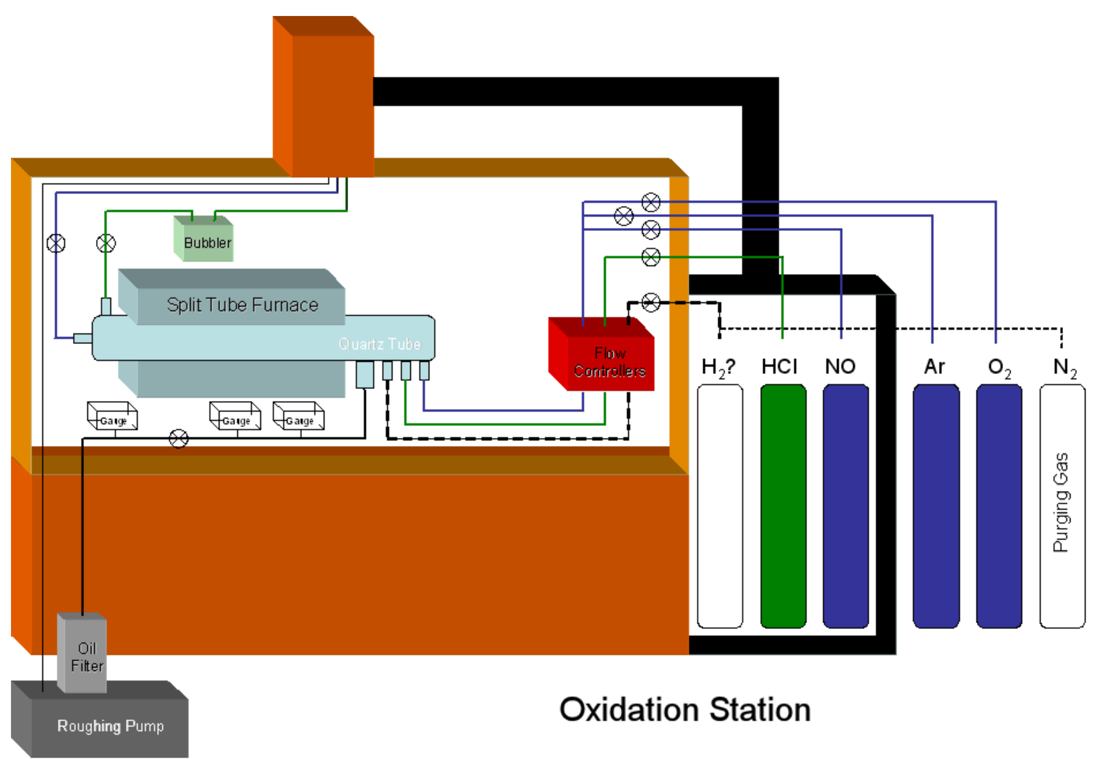



**Figure A.2:** Schematic of the oxidation setup.

**Figure A.3:** Picture of the oxidation setup.

| Item | | Description | Fit | Size | Mat | Manufacturer / Seller | Model # |
|---|---|---|---|---|---|---|---|
| **Furnace** | | | | | | | |
| Three-zone split furnace | | 12” long, 2+” ID, 1200 ˚C, 2000 W | | | | Thermcraft | TSP-3-0-12-3C-J8359/1A |
| Furnace controller | | Eurotherm one 2404 + two 2404(e) + three 2116FM | | | | Thermcraft | 3120115E17SPC226488 |
| Quartz tube | | IDxOD=50x55mm Length=26” - High purity quartz 214 | | | | General Electrics | |
| Fan – stand | | 2 speeds | | | | Electrix / Allied Electronics | 3037 M609 / 593-3037 |
| Fan - square | | Equipment cooling fan 45 cfm | | | | Commonwealth / McMaster | FP-108JC S1 / 1976K71 |
| Fittings | | Ultra-Torr vacuum fittings 1/4” - 3/8” - 1/2” | | | SS | Swagelok | |
| **Inlet Side** | | | | | | | |
| Gas cabinet | | Three bottles vented cabinet | | | | Matheson Semi-Gas | |
| Gas regulator | | Corrosive gases | NPT | 1/4” | SS | Concoa | 4225341-01-330 |
| Deep purge | | Purging tee for corrosive gases | NPT | 1/4” | SS | Concoa | 5023 009-01-660 |
| Tubing | | 1/4” stainless steel tubing | | 1/4” | SS | Valex | T4A-S-.25X10-A7 |
| Fittings | | Tube and NPT | | 1/4” | SS | Swagelok | |
| Valves | | Bellow valves | Tube | 1/4” | SS | Swagelok | SS-4BK |
| Filters | | 0.5 microns dry filters | Tube | 1/4” | SS | Swagelok | SS-4F-05 |
| Mass-Flow controllers | | Corrosive gas compatible 1.2L/m | Tube | 1/4” | SS | MKS | 1779A-13CS1BK |
| - Power Supply | | 4 channels multi-gas controller | | | | MKS | 647B |
| Flexible tubing | | Connect to quartz tube - bellow | Tube | 1/4” | SS | Swagelok | |
| **Vacuum Side** | | | | | | | |
| Vacuum pump | | Two-stage rough rotary pump | QF | 25 | SS | Edwards | E2M5 |
| Oil trap | | Prevents oil backstreaming | QF | 25 | SS | Kurt J. Lesker | TAS4CS-100QF |
| Tubing | | 1/2" stainless steel tubing | | 1/2” | SS | Valex | T4A-S-.5X10-A7 |
| Fittings | | QF flange fittings and tube fittings | | | SS | Kurt J. Lesker + Swagelok | |
| Valve | | Bellow valve | Tube | 1/2” | SS | Swagelok | SS-8BK |
| Thermocouple gauge | | Rough vacuum - pump side | NPT | 1/8” | SS | Kurt J. Lesker | OEM DV-6M (KJL-6000) |
| - Controller | | | | | | Kurt J. Lesker | KJL-205NT |
| Manometer Gauge | | Torr vacuum - tube side | QF | 16 | SS | Kurt J. Lesker | KJL-912151 |
| - Controller | | | | | | Kurt J. Lesker | KJL-902-020 |
| Convection gauge | | mTorr vacuum - tube side | QF | 16 | SS | Kurt J. Lesker | KJL-912162 |
| - Controller | | | | | | Kurt J. Lesker | KJL-902178 |
| Flexible tubing | | Connect to quartz tube - bellow | Tube | 1/2” | SS | Swagelok | |
| **Outlet Side** | | | | | | | |
| Tubing | | 3/8” PFA tubing | | 3/8” | PFA | Swagelok | |
| Valves | | Needle valve | Tube | 3/8” | PFA | Swagelok | PFA-4RPS6 |
| Fittings | | Tube fittings | Tube | 3/8” | PFA | Swagelok | |
| **Variable Pressure Oxidation** | | | | | | | |
| Quartz tube | | IDxOD=19x25mm Length=26” - High purity quartz 214 | | | | General Electrics | |
| Fittings | outlet | Tube fittings and NPT fittings (no UT) | | 1/4” | SS | Swagelok | |
| Tubing | outlet | 1/4” stainless steel tubing (no flexible) | | 1/4” | SS | Valex | T4A-S-.25X10-A7 |
| Valve | outlet panel | Bellow-sealed valve | Tube | 1/4” | SS | Swagelok | SS-4H |
| Relief valve | outlet panel | Adjustable 10 to 225 psi | Tube | 1/4” | SS | Swagelok | SS-RL3S4 |
| Gauge LP | outlet panel | Low pressure analog -30 to 0 Hg | NPT | 1/4” | SS | McMaster | 38595K11 |
| Gauge HP | outlet panel | High pressure digital 0 to 100 psi | NPT | 1/4” | SS | McMaster | 3834K13 |
| Gauge HP | outlet panel | High pressure analog 0 to 160 psi | Tube | 1/4” | SS | Swagelok | PGI-63B-PG160-LAQX-J |

**Figure A.4:** List of the major components of the oxidation setup. The fitting type, size, and material, are noted *Fit, Size, and Mat* respectively. Stainless steel is noted *SS*. Tube fittings are compression (Swagelok) type fittings, with sleeves and ferrules.

### Furnace and oxidation tube

The furnace (shown in Figure A.5) is a three-zone split furnace purchased from Thermcraft Inc. It plugs in a regular 110 V outlet and draws up to 2000 W. The maximum operating temperature is 1200 °C. The heat is provided by coils embedded in cement. Six thermocouples, and separate power lines, allow to control the three zones independently using the external unit based on Eurotherm PID (proportional, integral, differential) modules shown in Figure A.5. The temperature is quasi uniform over the central 6" hot zone as the surrounding 3" shielding zones are adjusted to minimize heat loss.

The tube (55 mm OD) and the sample holder are made of high purity quartz to minimize sodium contamination, see schematics on Figures A.6 and A.7. During operation, both ends of the tube are cooled by air circulation to prevent damage of the viton sealing o-rings. The connections to the feeding, vacuum, and exhaust lines, are made via Ultra-Torr fittings which enable vacuum-tight glass-to-metal, or glass-to-plastic, connections.

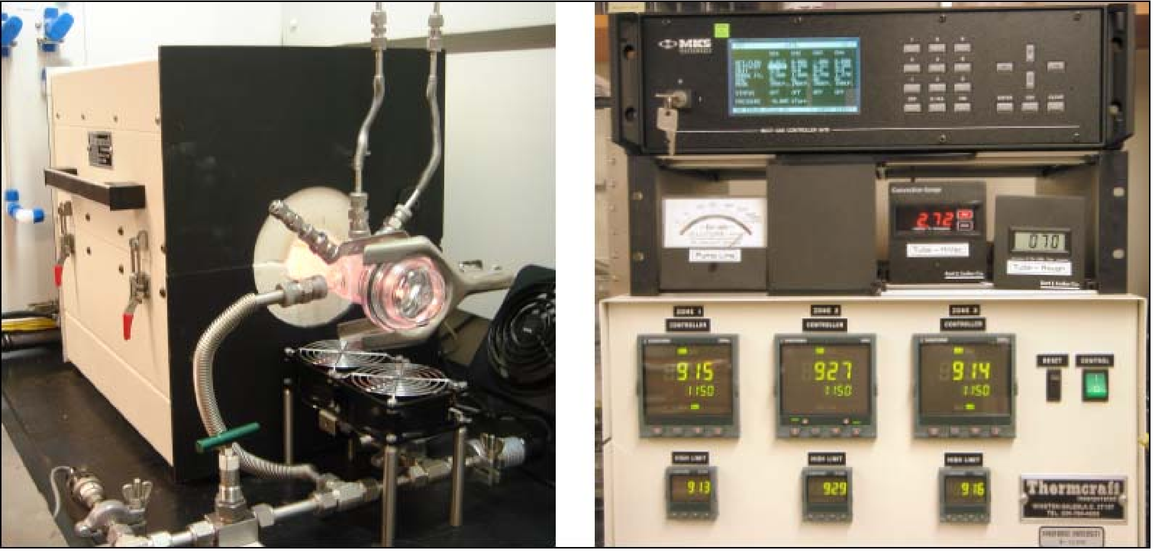



**Figure A.5:** Left: furnace, oxidation tube, inlets and vacuum lines. Right: Control units (furnace, gauges, and mass-flow controllers).

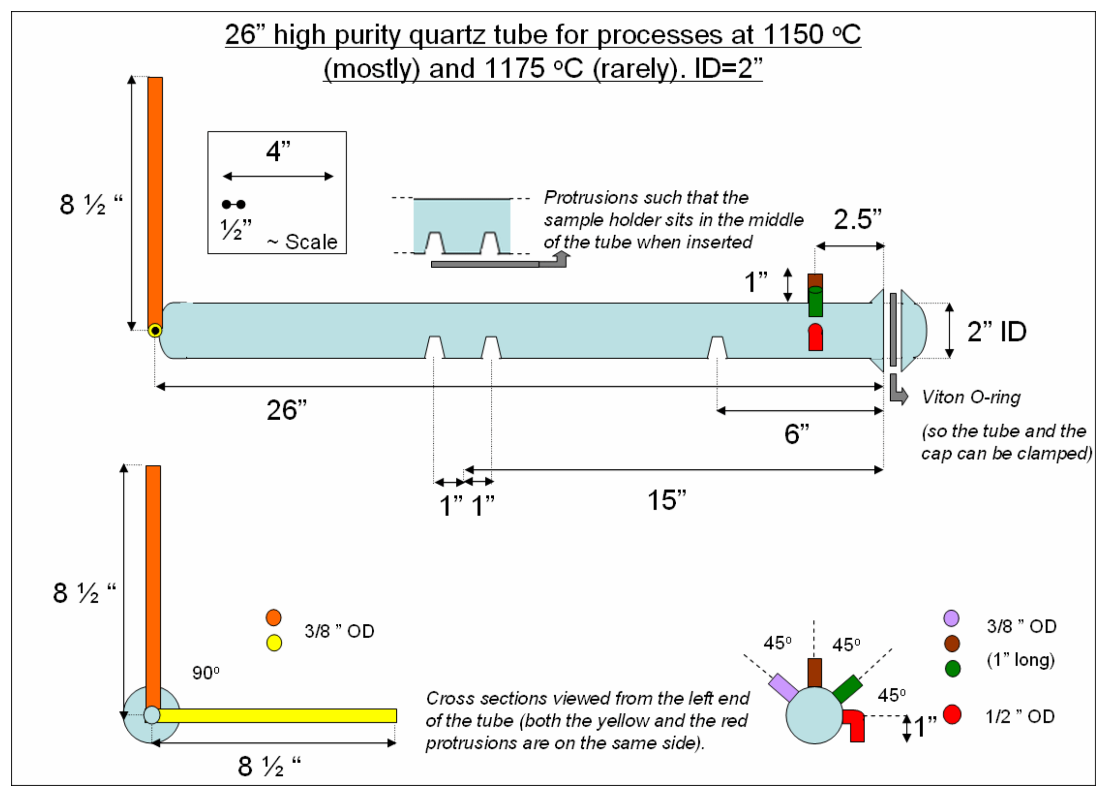



**Figure A.6:** Schematic of the high purity oxidation tube.

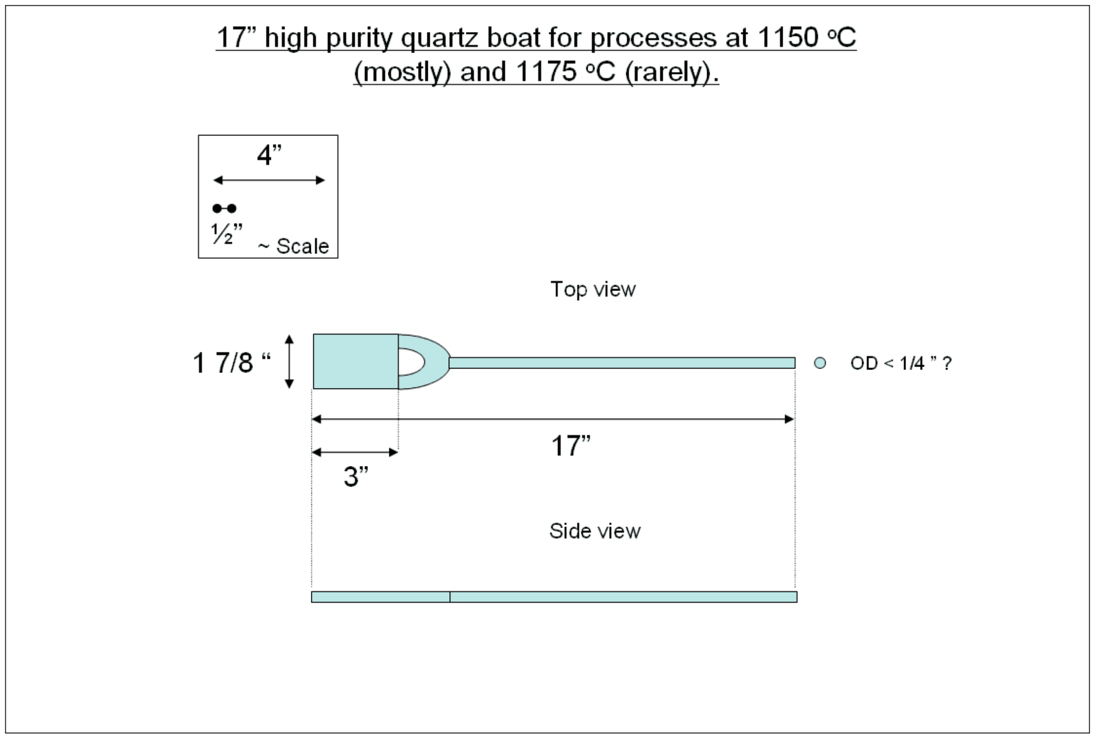



**Figure A.7:** Schematic of the quartz sample holder.

### Feeding lines

The corrosive gases are placed in a vented cabinet and are connected to the fume hood, where the furnace resides, by uninterrupted lines. The control panels for these gases were custom built, see Figure A.8. A purging tee allows for safe removal of toxic gases without the need for a pumping system. Indeed, a purging gas, i.e. flowing nitrogen, can clear the high pressure line once the hazardous gas bottle is closed. The purging gas can also flow through the oxidation tube.

A set of bellow valves, shown in Figure A.8, allows for the selection of the processing gas(es) on two different tube inlets. The flow through the two inlets can be regulated separately via mass-flow controllers. A provision for a third line was implemented. The lines are filtered to avoid tube contamination. The diagrams for designed aluminum supports are shown in Figures A.9 and A.10. The connections to the quartz tube are made using flexible bellow tubing to prevent stress in the glass.

**Figure A.8:** Left: custom-built regulator panel for hazardous gases. Right: selection bellow valves, in-line filters, and mass-flow controllers.

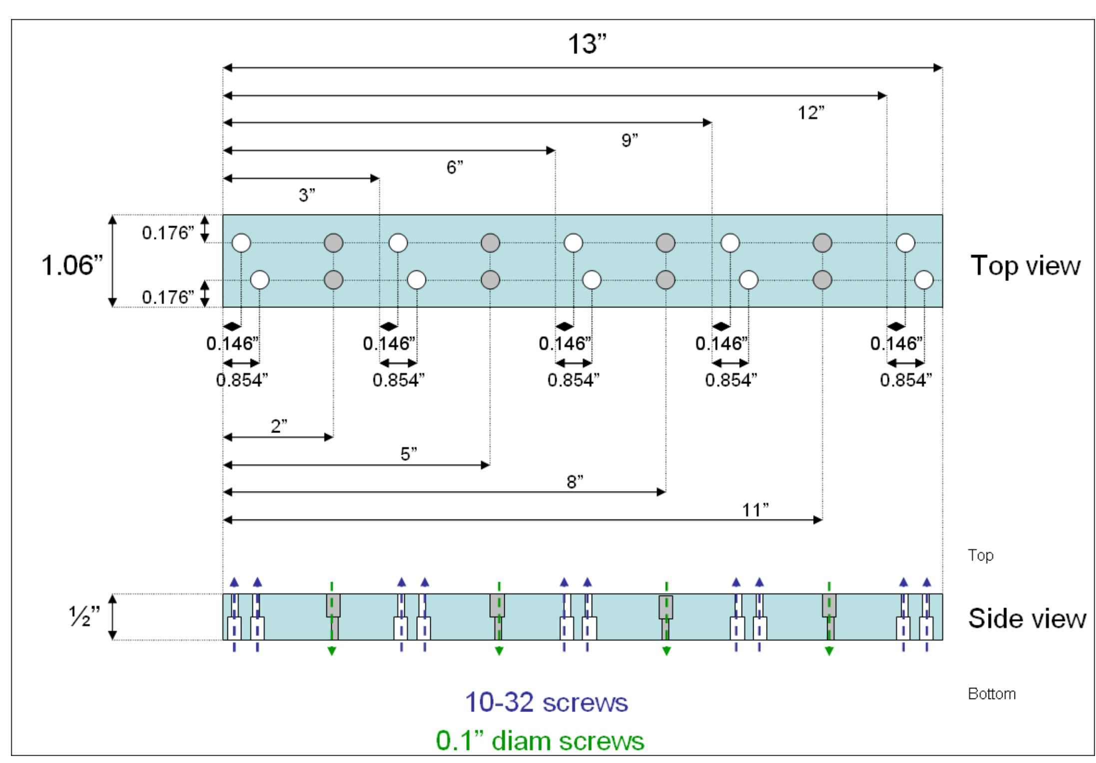



**Figure A.9:** Aluminum support for five 1/4” Swagelok valves SS-4BK.

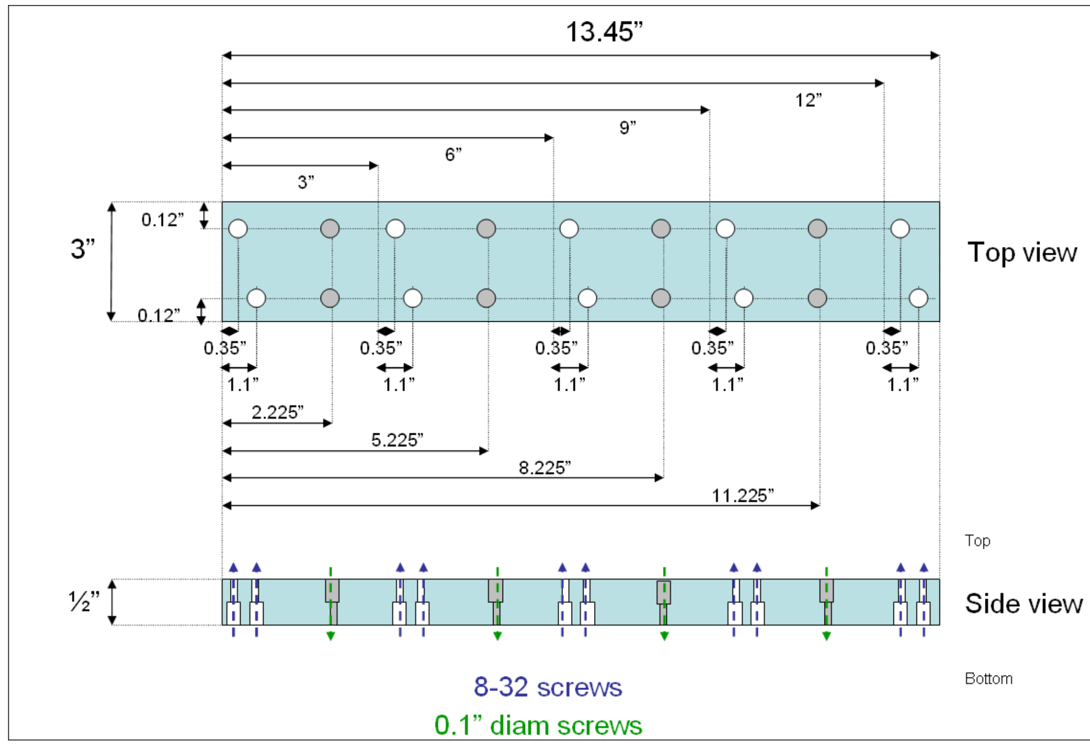



**Figure A.10:** Aluminum support for five MKS controllers 1179A.

### Vacuum line

The vacuum pump is connected to an oil trap to avoid tube contamination. Flexible tubes and QF (KF) connectors are used to connect the trap to a 1/2" OD stiff stainless line. A bellow valve separates the tube side from the pump side, as illustrated in Figure A.11. On the pump side, a thermocouple gauge is installed. On the tube side, both a manometer and a convection gauge are used to monitor tube vacuum in the Torr and mTorr range respectively. A flexible bellow stainless steel tube makes the connection to the 1/2" vacuum outlet of the quartz tube using an Ultra-Torr fitting.

### Exhaust lines

The quartz tube outlets are connected to PFA 3/8" tubing via Ultra-Torr fittings. This material is used to avoid corrosion from the hot hazardous gases being exhausted. PFA needle valves allow flow control. There are two exhausts: one goes straight to the vent, the other is directed through a glass bubbler (shown in Figures A.12 and A.13). The bubbler can be used to prevent back-flow or to filter hazardous gases. For example if HCl is flown, a reaction with submerged marbles ($CaCO_3$) in the bubbler will retain the chlorine.

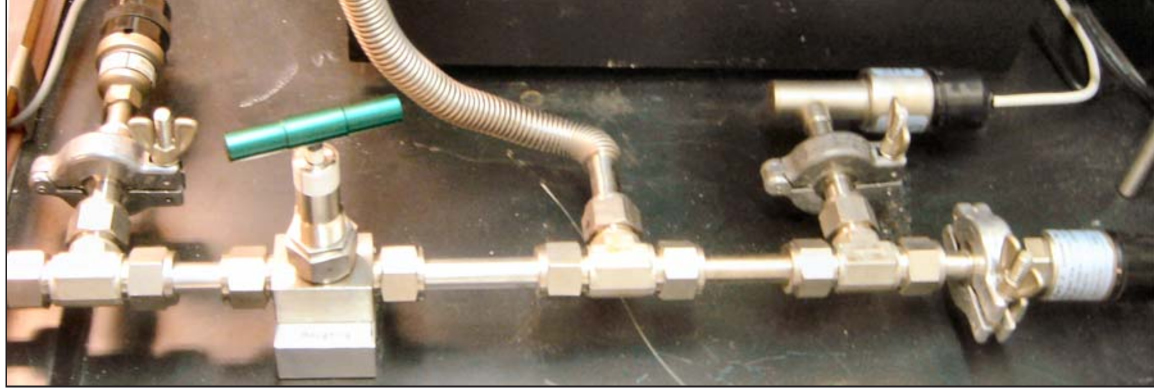


**Figure A.11:** End of vacuum line. From left to right: thermocouple gauge, bellow valve, connection to quartz tube, manometer gauge, convection gauge.

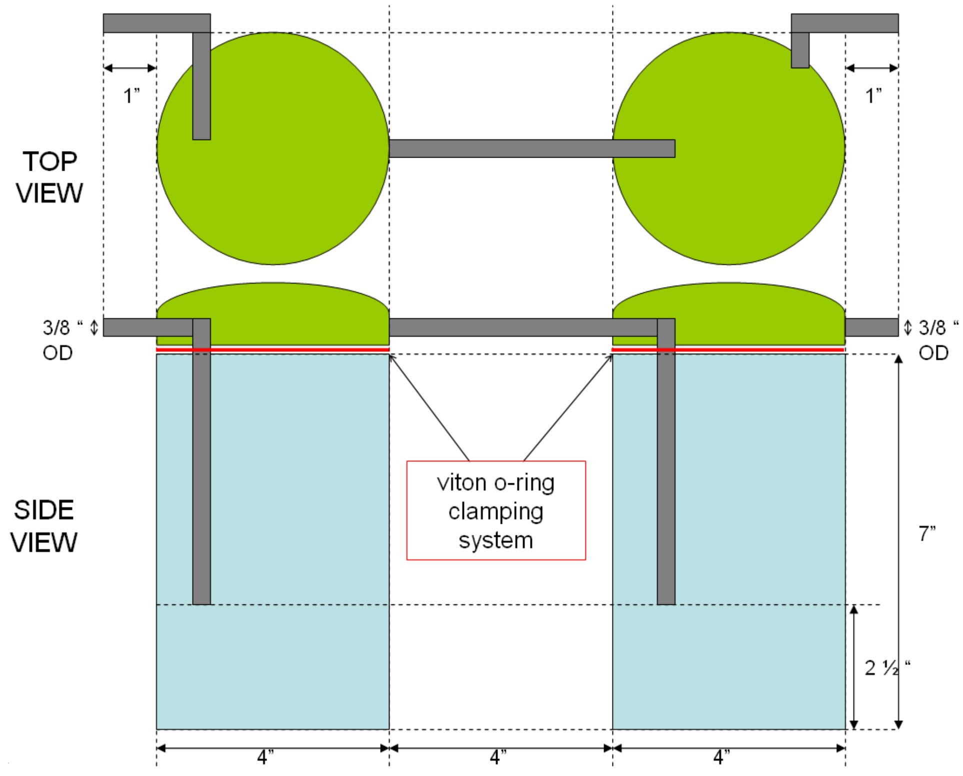



**Figure A.12:** Schematic of double-bubbler design.

**Figure A.13:** Picture of custom-built bubbler.

### Variable pressure oxidation

Various modifications to the setup can be made to enable high pressure oxidation. Low pressure processing was already possible as the mass-flow controllers can independently mix two gases, leading to a given partial pressure. The vacuum system can also be used to pump out the tube. The bellow valve between the pump and the tube, can be used as a leak valve, enabling low pressure processing in flowing conditions.

The wall thickness of the tube used for high pressure oxidation (see Figure A.14) is 3 mm, more than 10% of 25 mm, the outside diameter. This implies that the tube is rated for usage at positive pressures up to 100 psi ($\simeq$ 6.8 atm). To avoid weakening the tube, quartz flanges were fused on both side, so that the inlet(s) and outlet ports lie on separate metal caps. The glass-to-metal connections are achieved by viton o-rings and three-screw clamps. The tube is centered in the furnace thanks to thermally insulating fiberglass. Both ends are connected to 1/4" stainless steel rigid tubing, using NPT and compression fittings (Ultra-Torr connectors and flexible tubing cannot be used for high pressure operation). Transparent plastic shields are mounted on both sides of the furnace to prevent injury in case the tube bursts. The modified oxidation station is shown in Figure A.15.

The exhaust line is different from the one described previously. The gas is directed to a pressure control panel, located outside the hood for safety reasons (see Figure A.15). From this panel, the pressure can be set, monitored, and released. The panel consists of a measuring gauge, on the tube side, and of a bellow valve and an automatic relief valve connected in parallel. The pressure relief valve can be adjusted between 10 and 225 psi ($\simeq$ 0.7 and 15.3 atm). It has two main uses. First, it keeps the pressure from exceeding a set value, preventing gas buildup and eventual explosions. Second, it enables flowing gas processes at higher pressure, increasing the quality attainable by static processes.

The tube can also be used for low pressure oxidations, in which case, the vacuum pump is connected to the inlet cap, similarly to the regular oxidation setup.

A procedure for high pressure oxidation is shown in Figures A.16 to A.18.

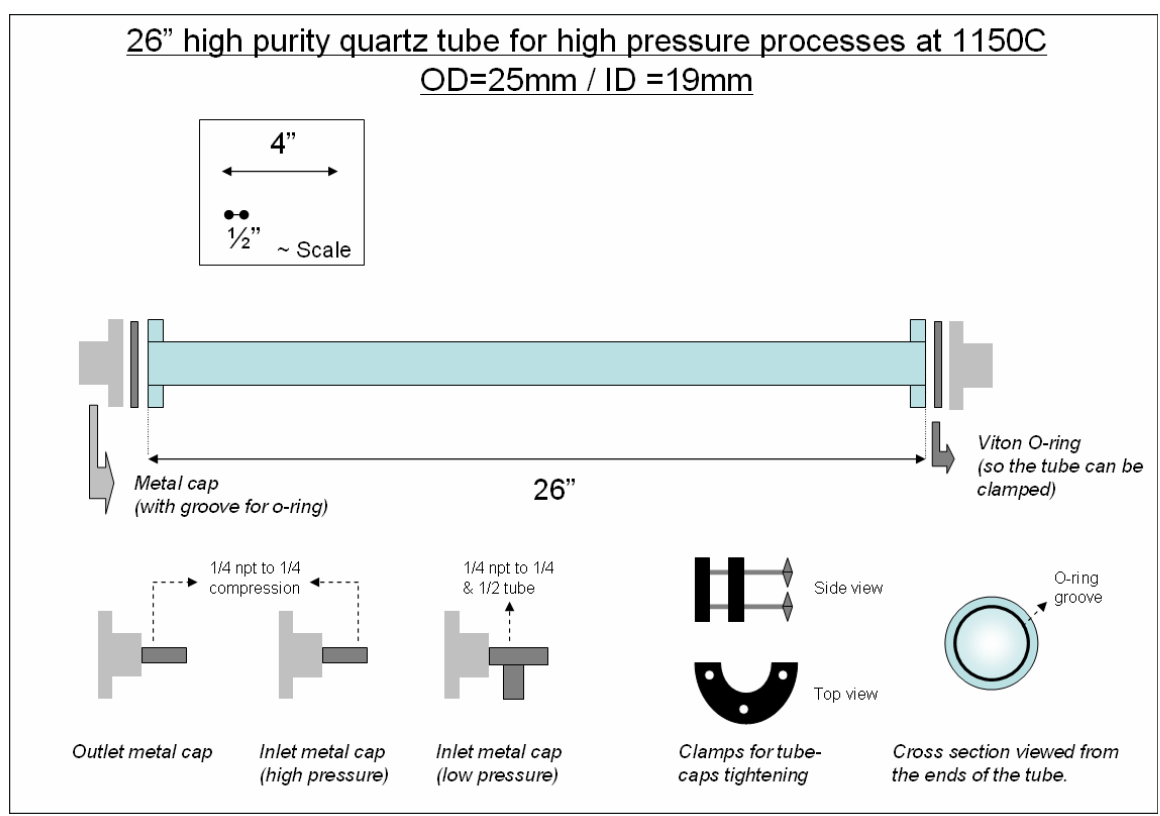



**Figure A.14:** Thick-wall tube for high pressure oxidation.

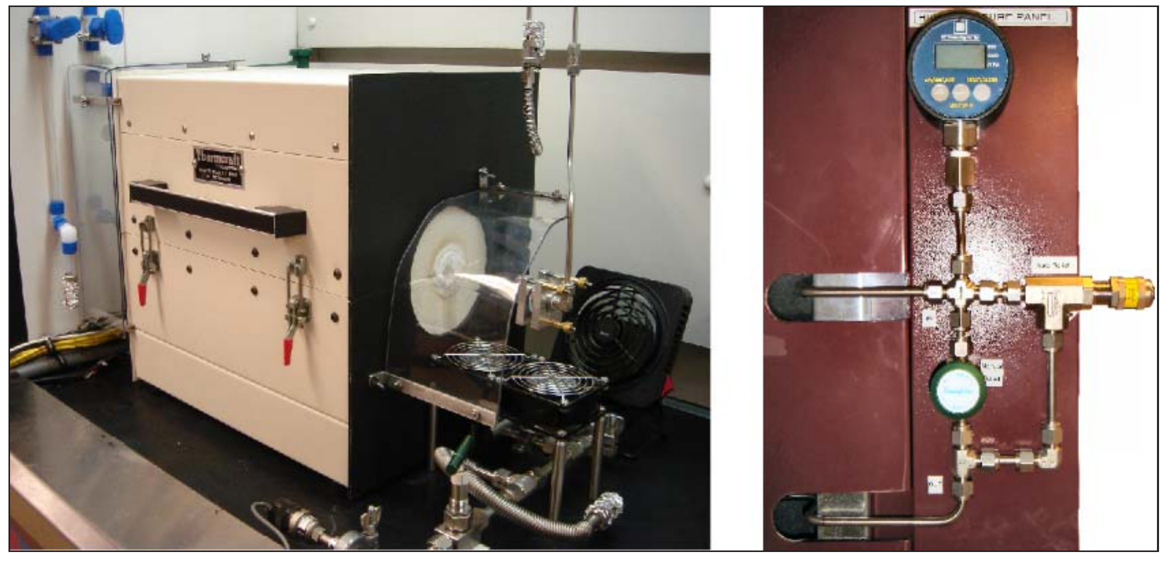
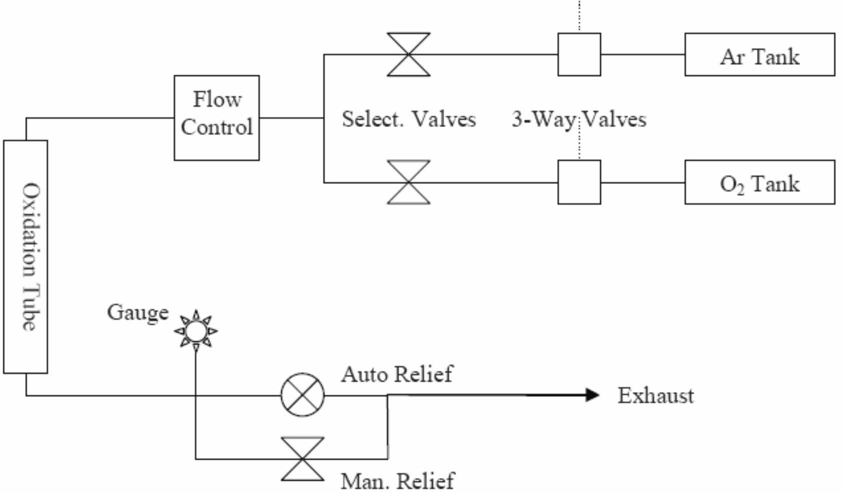


**Figure A.15:** Left: high pressure oxidation setup (shields, thick tube, three-screw clamp...). Right: pressure control panel.

# High Pressure Oxidation Setup – Usage Procedure

Experiment Schematic:




Safety Measures:

1. A sign should be posted at the door to warn lab users
2. There must be 2 operators in attendance
3. No other process can be run in the lab during operation
4. All lab users must wear safety goggles and a lab coat
5. The hood must be emptied and closed when the tube is pressurized
6. The polycarbonate shield must be in place
7. All cooling fans must be on
8. The delivery pressure must be set slightly higher (< 1 atm) than the target pressure
9. The automatic relief valve should be adjusted to the target pressure (see procedure)
10. The tube is rated at 100 psi and should not be pressurized above 50 psi (relative pressure)

Idle Conditions:

The tube should be at 600C and pressurized at +1 atm (relative, = 2 atm absolute) with argon. All manual valves should be closed, flow should be off and the automatic relief valve should be set to +1 atm (see procedure). Cooling fans must be on.

Pressure Units:

NB: Relative pressure is defined with standard conditions as reference (1 atm absolute). All gauges indicate relative pressure.

1 atm ≈ 1 bar ≈ 100 kPa ≈ 14.7 psi

John Rozen Page 1 1/24/2007

**Figure A.16:** High pressure oxidation procedure - page 1

Procedure:

1. Open all valves on the $O_2$ delivery side of the tube (bottle, regulator, 3-way and select. valve)
2. Set the delivery pressure to 20 psi (if pressure is too high, release and adjust after step 3)
3. Set the flow to 0.250 L/min
4. Open the manual relief valve
5. Wait 5 min
6. Open all Ar valves on the delivery side (regulator at 20 psi) except the selection valve
7. Close the $O_2$ selection valve and open the Ar one

→ Purging gas is flowing (check meter) and the tube is at lab pressure (check gauge)

8. Unscrew the horseshoe clamp and open one side of the tube
9. Take boat out progressively (≈ 1 min) and place samples on
10. Put boat back in progressively (≈ 1 min) and position samples in the center of the tube
11. Close cap with o-ring in place and tighten the clamp carefully as much as possible

→ Purging gas is flowing with samples in

12. Wait 5 min
13. Close manual relief
14. Wait for the pressure to reach +1 atm and turn off the flow
15. If pressure holds proceed, if not repeat steps 11-15 (check o-ring alignment and tightening)
16. Turn on flow
17. Open manual relief

→ Leak check performed, purging gas is flowing and tube is at lab pressure

18. Set the Ar and $O_2$ regulators pressure to a same value slightly higher than the target pressure
19. Adjust the automatic relief valve to reach a pressure in the tube slightly higher than desired
20. Turn off the flow
21. Adjust the automatic relief valve to the desired value
22. See if pressure holds (if not, small flow might be required to maintain pressure)
23. Turn on flow
24. Open manual relief

→ Auto relief adjusted, purging gas is flowing and tube is at lab pressure

25. Let Ar flow for 15 min
26. Ramp up the temperature to the desired value
27. When target is reached, close the Ar selection valve and open the $O_2$ one
28. Wait 5 min
29. Close the manual relief
30. When target pressure is reached, turn off or limit the flow for quasi-static oxidation

→ The tube is pressurized with oxygen and oxidation is being performed

31. When oxidation is finished, set flow to 0.250 L/min
32. Adjust automatic relief valve to +1 atm
33. Open manual relief
34. Close the $O_2$ selection valve and open the Ar one
35. Ramp down temperature to 900C to switch samples or to 600C if oxidation is finished

→ Oxidation is complete, temperature is ramping down, Ar is flowing, tube is at lab pressure

36. Remove the clamp and take out samples progressively ≈ (1 min)
37. Put the boat back in progressively (≈ 1 min) and tighten the clamp
38. If samples are still in restart procedure from step 12 / To go to idle conditions, see below

John Rozen Page 2 1/24/2007

**Figure A.17:** High pressure oxidation procedure - page 2

## Set to Idle Conditions:

1. Let Ar flow for 5 min
2. Close the manual relief
3. When +1 atm is reached in the tube, turn off the flow
4. If the pressure holds proceed, if not re-align and tighten o-ring
5. Close all manual valves on both the oxygen and argon lines

→ Tube is pressurized at +1 atm, flow is off, valves are close, temperature is 600C, fans are on
→ Hood is closed with warning sign

---

## Technical Specifications:

O-rings are -212 viton military specs
Tube is GE quartz 19 mm ID, 25 mm OD (3 mm wall thickness)
All metal tubing, fittings and valves used are stainless steel and rated well above 100 psi
The shield is made out of polycarbonate
Pressure gauge has a 160 psi range with +/- 2.4 psi precision (Swagelok PGI-63B-PG160-LAQX)

## Testing Conditions:

The tube should be tested at room temperature at twice the operating relative pressure using Ar

---

## Emergency Contacts:

| | | |
|---|---|---|
| Vanderbilt Emergency Services | 615-322-2745 | 911 (from campus phone) |
| Tony Hmelo | 615-343-7212 | 3-7212 |
| John Rozen | 334-398-2804 | 3-4438 |
| Sarit Dhar | 615-397-6743 | 7-6743 |

John Rozen    Page 3    1/24/2007

**Figure A.18:** High pressure oxidation procedure - page 3

# APPENDIX B

## AUTOMATED CARRIER INJECTION

In this appendix, the setup designed for automated capacitance-voltage (CV) and carrier injection (Figures B.1 and B.2) is described. Three devices can be tested simultaneously under low or high intensity UV illumination.

Some modules have been added to the base Keithley model 82 setup which is normally used with the Interactive Characterization Software (ICS) for simultaneous high and low frequency measurements. In addition, light sources are needed to enable internal photoemission, from the metal gate of a device, or Fowler-Nordheim tunneling of minority carriers. A custom program is used to control and monitor the experiments.

Three components of the setup are introduced separately: the optics, the electronics, and the acquisition software. A list of key items used for the implementation is shown in Figure B.3.

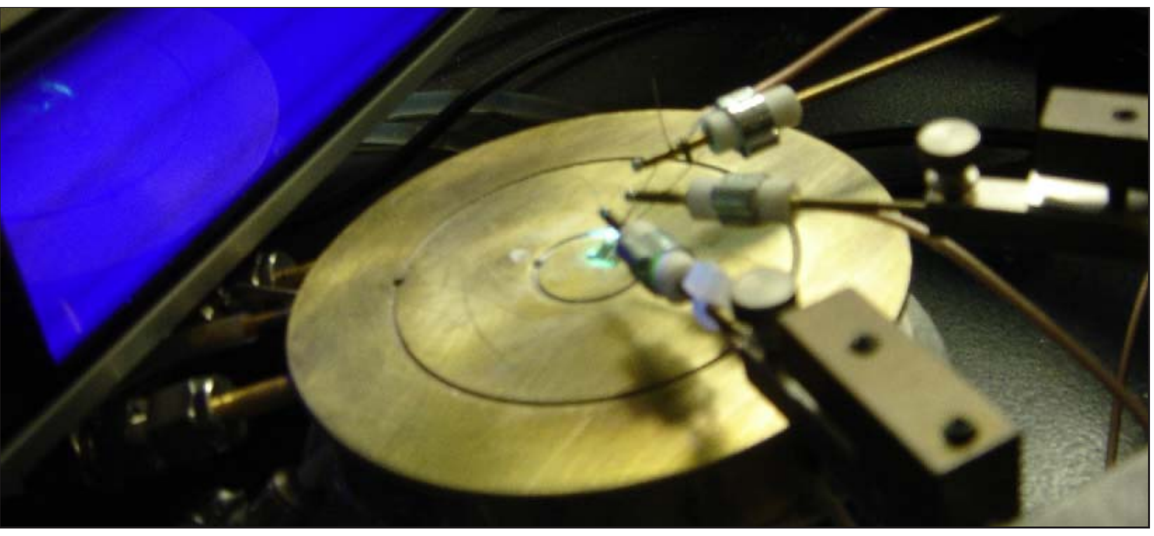


**Figure B.1:** Picture of the CV probe station under UV illumination.

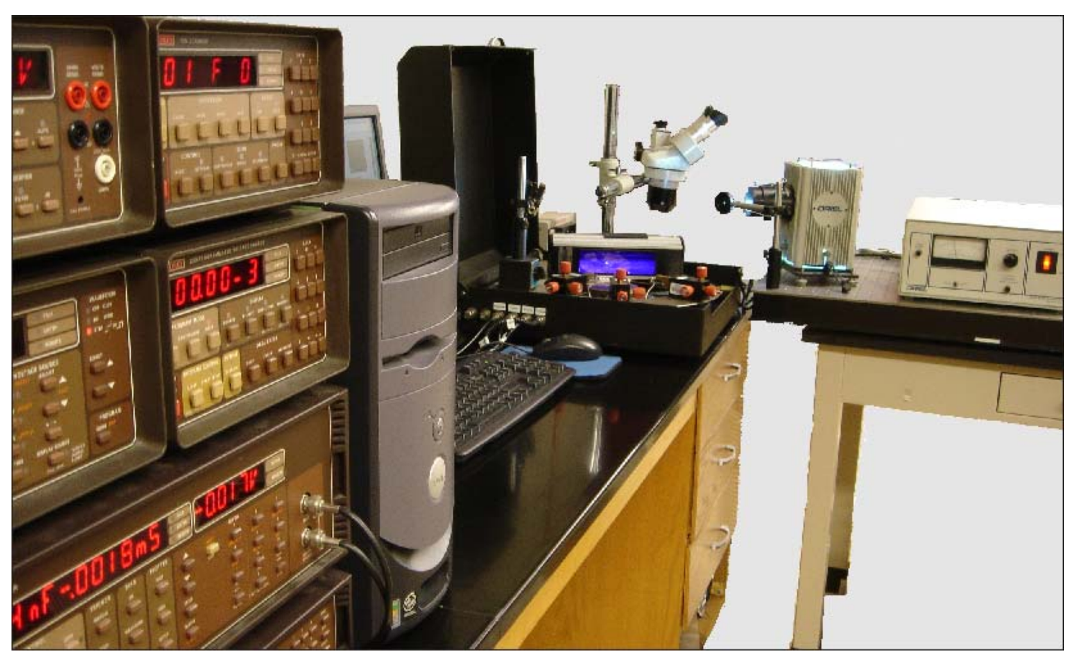


**Figure B.2:** Picture of the automated injection setup.

| Item | Description | Manufacturer / Seller | Model # |
|---|---|---|---|
| **Optics** | | | |
| Mercury lamp | 100 Watts | Oriel / Newport | 6281 |
| Lamp housing | Xe and Hg housing up to 100 W, with reflectors | Oriel / Newport | 60000 |
| UV condensing lens | Adjustable UV focusing assembly mounted on housing | Oriel / Newport | 60006 |
| Power supply | Power to lamp housing 50 to 200 Watts | Oriel / Newport | 68806 |
| UV mirror | Al coated, 2" diameter, pyrex, broadband 250 -600 nm | Newport | 20D20AL.2 |
| Handheld UV light | 2 wavelengths: 254 and 365 nm, 6 Watts, unfocused | Spctra Line | ENF-260C |
| **Probe Station** | | | |
| Probes | 3 degrees of freedom | Signatone | S-725-HTR |
| Chuck assembly | Temperature control, electrical shielding | Signatone | S-1043-406-D3 |
| Temperature controller | Thermocouple, power supply, water circulation | Signatone | S-1043 |
| Stereo Microscope | Magnifications: 10X and 30X (with 10X eyepieces) | Meiji | EMT-2 |
| **CV Setup - KY Model 82** | | | |
| Quasi-static meter | Measures low frequency capacitance (staircase) | Keithley | 595 |
| CV analyser | Measures high frequency capacitance (100kHz/1MHz) | Keithley | 590 |
| Voltage source | Programmable source to exend bias range | Keithley | 230 |
| Remote coupler | Input coupler for sumaltenous hi-lo CV measurements | Keithley | 5951 |
| Wiring | Low noise BNC cables (co-axials) | Keithley | K-4801 |
| Interface | IEEE 488 | | |
| Software | Interactive Characterization Software | Metrics | ICS |
| **Automated Injection** | | | |
| DMM | Digital multi-meter to probe voltage drop of resistors | Keithley | 196 |
| Scanner | Two slots, 20 channels | Keithley | 705 |
| Scanner cards | High frequency cards, 10 channels, BNC connectors | Keithley | 7062 |
| Source / Measure unit | Current and voltage, power supply and meter | Keithley | 236 |
| Connector box | Custom built connector BNC connector box | | |
| Resistors | Resistors in series with capacitors, 100 MΩ, 1% | | |
| Wiring | Low noise BNC cables (tri-axials and co-axials) | Keithley | K-4801 (co-axial) |
| Interface | IEEE 488 | | |
| Software | Custom LABView program (also controls KY 590) | National Instruments | |

**Figure B.3:** Some key components of the injection setup.

**Optics**

Two UV light sources are used for carrier injection. The radiation of a 100 W mercury lamp is focused on a sample using a condenser lens and an aluminum coated broadband mirror. The beam diameter is of the order of 1 cm, the active region of the bulb. Maximizing the light power density is critical to the amplitude of the electron quantum yield in the gate metal of a device. The spectrum of the mercury lamp is shown in Figure B.4, together with the reflectance of the broadband mirror. It can be seen that the light source provides quite a few peaks in the UV (below 400 nm), enabling the emission of electrons from the gate metal into the oxide of a MOS structure. In that region, the reflectivity of the mirror is between 80 and 90 %. Note that the light intensity can be increased by aligning reflectors in the Oriel lamp housing and by reducing the beam length so that air absorption is minimized.

To form an inversion layer in a wide band-gap semiconductor MOS structure, a low intensity handheld UV lamp from Spectra Line is used. Two single wavelengths can be selected: 365 nm (3.4 eV) and 254 nm (4.9 eV). The sources are unfocused and their power is only 6 W. This is not sufficient to induce photo-injection.

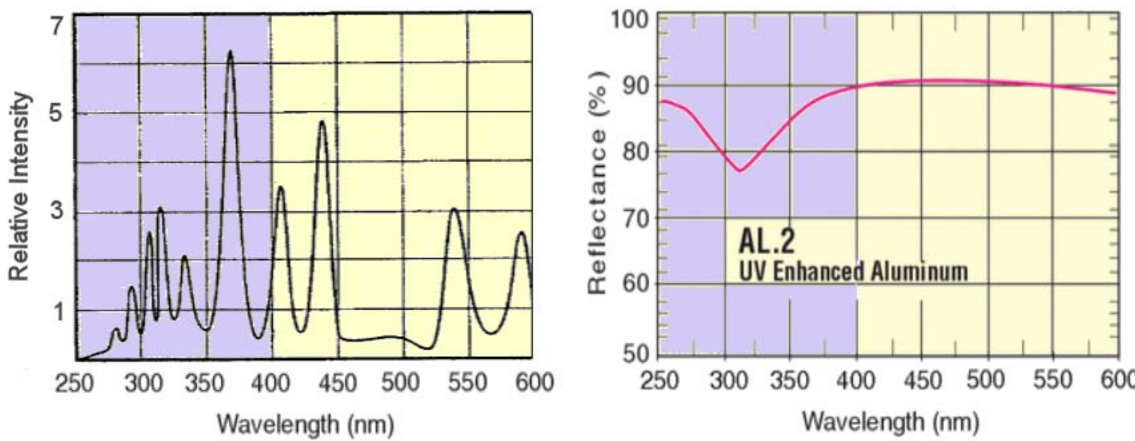



**Figure B.4:** Left: Hg lamp spectrum. Right: reflectance of the Newport 20D20Al.2 mirror.

## Electronics

A schematic of the electrical connections is shown in Figure B.5. The units used for the automated setup are the high frequency CV analyzer (Keithley 590), a voltage source/current measure unit (Keithley 236), a digital multi-meter (Keithley 196), switch matrix cards (Keithley 7062), and a scanner (Keithley 705). Connections are made via low noise cables.

Resistors are placed in series with the devices being tested on the probe station, in order to sequentially measure individual currents using the multi-meter. Their value is chosen so that the accuracy of the current reading is maximized without affecting the voltage drop across a device.

The matrix cards enable various operation modes during a measurements. (i) High frequency CV measurements can be performed one device at a time. (ii) Each device can be individually biased to find desired current/voltage conditions. (iii) All devices can be biased simultaneously while currents are probed sequentially using the resistors and the multi-meter.

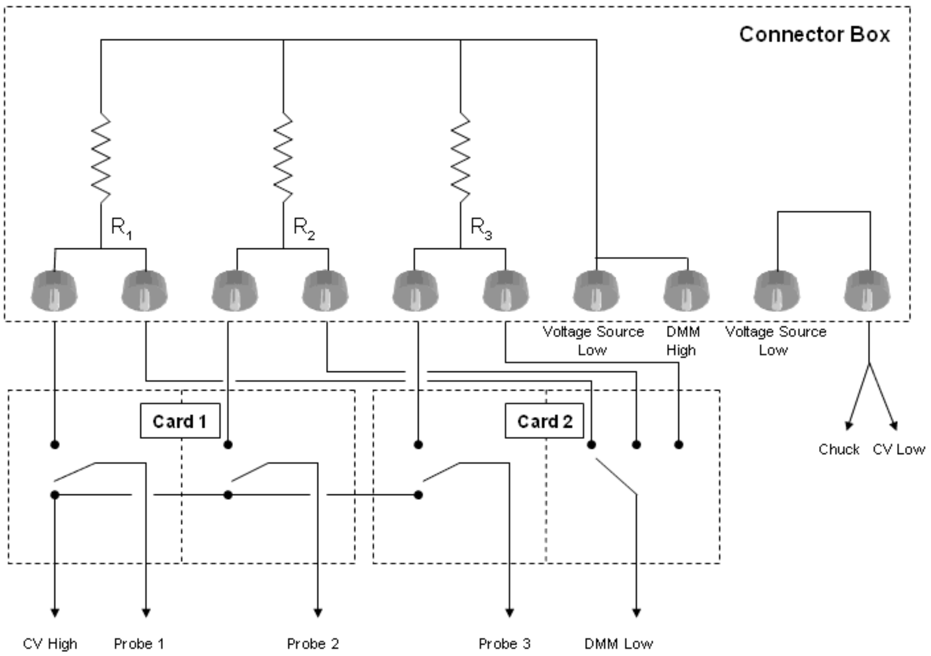



**Figure B.5:** Electrical connections of the automated injection setup.

### Acquisition software

A custom program was implemented using the LabVIEW software from National Instruments. A screen capture of the control panel can be seen in Figure B.6. The program provides test equipment control, data acquisition, and data analysis. It has an interactive interface to enable user input while running. The measurements steps performed are briefly introduced.

First, each connected device is tested individually. A capacitance-voltage trace is taken prior to finding the injection conditions, which is achieved by progressively increasing the bias until a set current target is reached. The program informs the user of the success (or failure) of this operation so that the dot can be re-measured, replaced, or discarded. Failure occurs when the measured current exceeds a value set to identify oxide breakdown or defective devices.

Once the injection conditions have been found for all dots, a chosen bias is applied simultaneously to the selected devices. Meanwhile, the current flowing through each device is extracted by successively measuring the voltage drop across the resistors. These currents are integrated separately to obtain the individual injected carrier densities. Periodically, the bias is interrupted and CV traces are taken on each device to calculate the flatband voltage shifts. Note that the CV acquisition window is adjusted to follow the trace in a subsequent measurement.

As seen in Figure B.6, some of the real-time program outputs are the individual CV plots, flatband voltage shifts vs. injected carrier density, and current vs. stress time.

The experiment is terminated when all dots have failed. Several files are then automatically saved, they contain all CV traces, current data...

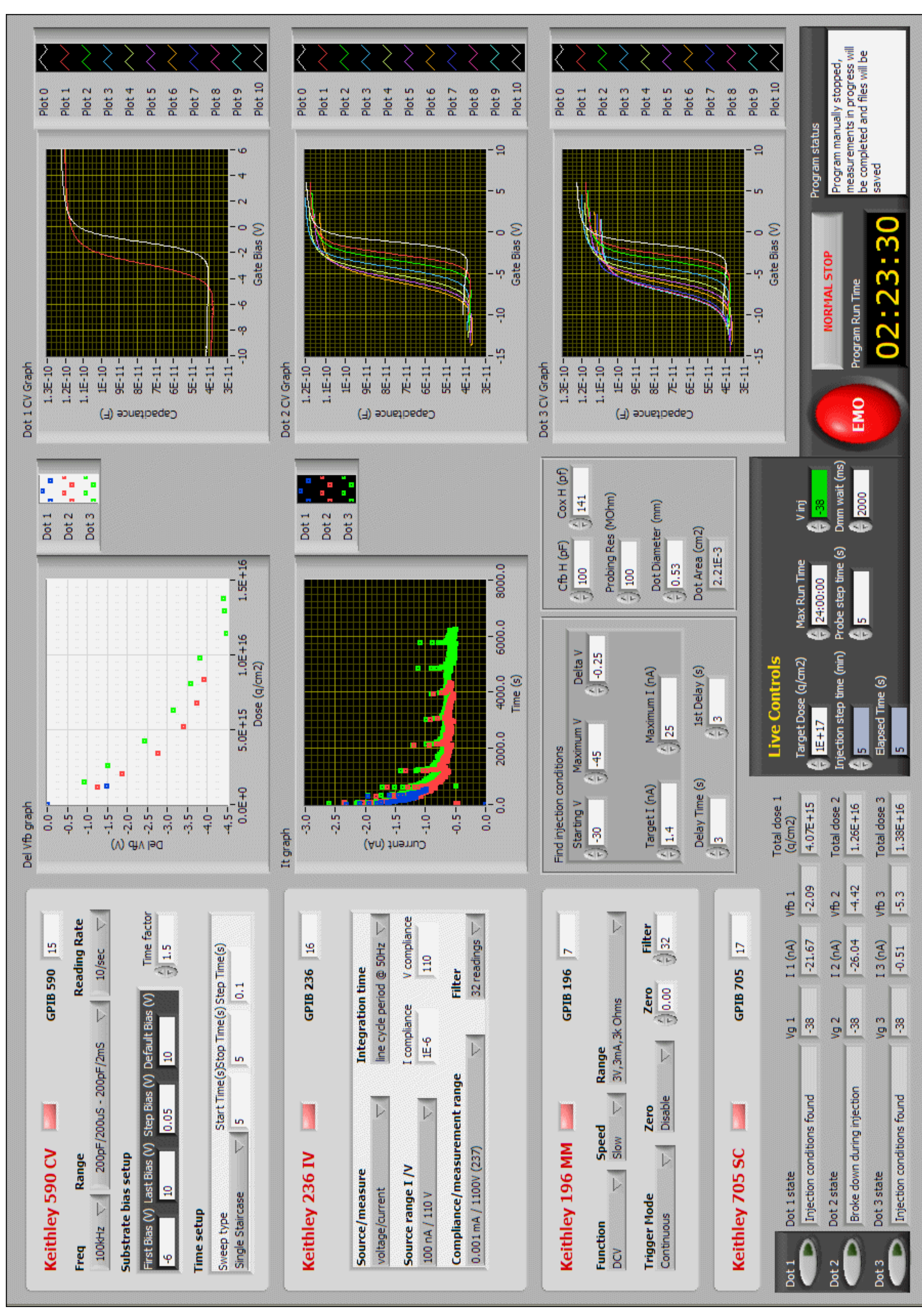



**Figure B.6:** Screen capture of the LabVIEW program designed for automated injection.

# APPENDIX C

## TDDB SETUP

The setup designed for time-dependent dielectric breakdown (TDDB) measurements described here, see Figures C.1 and C.2, enables the accelerated testing of 36 devices in parallel at temperatures up to 400 °C.

The probe station includes a specially designed hot chuck and a custom probe card. A connector box acts as the hardware interface between the devices and the test units, allowing parallel voltage stressing and iterative current measurements via switch matrix cards. The units are controlled by a custom LabVIEW program which has a real-time interactive display and outputs the cumulative percent failure as a function of stress time. In addition, the RealVNC software is installed on the host machine to control and monitor measurements remotely as they can last for days or weeks at a time.

Three parts of the TDDB setup are briefly discussed: the probe station, the electronics, and the acquisition software. A list of essential setup components is shown in Figure C.3.

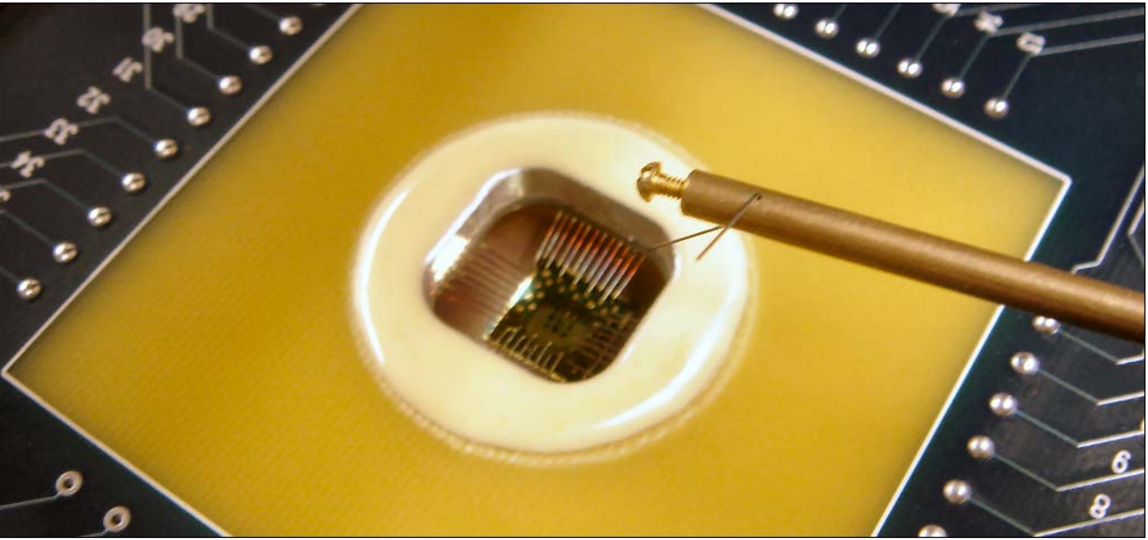


**Figure C.1:** Picture of a TDDB sample contacted by the probe card and the normal probe.

**Figure C.2:** Picture of the TDDB setup.

| Item | Description | Manufacturer / Seller | Model # |
|---|---|---|---|
| **Probe Station** | | | |
| Translation stage | XY translation probe station + custom card holder | Alessi Industries | |
| Stereo miscroscope | Mounted on stage, 22.5X, 80X, 450X, (10X eyepieces) | Bausch and Lomb | MicroZoom |
| Normal probe | For two-point contact check - customized | Rucker and Kolls | 222 |
| Probe card | Custom 36 terminals probe card for high temperature | Alpha Probes | WO# 34306 |
| Copper chuck | Alloy 101, extreme temperature, electronic grade | McMaster-Carr | 8312K12 |
| Disc heater | 200 Watts, half sheat, 120 V, up to 400 °C | Chromalox / McMaster-Carr | 3559K25 |
| Thermocouple | K-type with high temperature sleeves | McMaster-Carr | 9251T93 |
| Thermal insulation | Ceramic fiber blanket, up to 1260 °C | McMaster-Carr | 93315K42 |
| Temperature controller | PID control / disc heater power supply | Eurotherm | 3216 |
| **Electronics** | | | |
| Voltage source | Voltage/current source - applies bias to tested devices | Keithley | 228A |
| DMM | Digital multi-meter to probe voltage drops of resistors | Keithley | 193 |
| Scanner | 10 slots, 100 channels | Keithley | 706 |
| Scanner cards | High current cards, screw connectors, 10 channels | Keithley | 7053 |
| Ribbon cables | To probe card: 20 wires / To scanner cards 15 wires | Digi-Key | AE20M / AE15M -X-ND |
| D-Sub connectors | 15 contacts, male on card side / female on box side | Digi-Key | HMU15HND / HFU15HND |
| Socket connectors | 20 contacts, both sides of cable from probe card to box | Digi-Key | HSC20H-ND |
| Pin connectors | 20 contacts, box side of probe card connections | Digi-Key | HPL-20H-ND |
| Resistors | Metal film, 10 kΩ 1%, 1/4 W, axial | Digi-Key | P10.0KCACT-ND |
| Connector box | Used for inter-connecting units, cards, resistors | Frame from Digi-Key | HM739-ND |
| Capacitor test box | 36 packaged capacitors / switches to test tddb setup | Frame from Digi-Key | HM736-ND |
| Scanner test box | 10 resistors to test electromagnetic switches of cards | | |
| Interface | IEEE 488 | | |
| Software | Custom LabVIEW program | National Instruments | |

**Figure C.3:** List of parts used in the TDDB setup.

### Probe station

The probe station is illustrated in Figure C.4 (left). The chuck is mounted on a translation stage. The probe card height is controlled independently. A normal probe is used to check individual electrical contacts.

The chuck, shown on the right side of Figure C.4, was specially designed for this application. The copper used is oxygen free, allowing for high temperature experiments. It is 2" in diameter and 3/4" tall, back and top surfaces are polished. A disc heater is attached to the bottom of it by a centered a screw. The chuck is mounted on the probe station using a three-point spring loaded system enabling surface alignment with the probe card. Ceramic connectors between the three mounting screws and the copper prevent heat dissipation and electrical conduction (chuck serves as common). A Eurotherm unit controls the temperature by adjusting the output power to the heater according to the reading of the thermocouple attached to the chuck.

The 36-probe card was custom built by Alpha-Probes Inc. (see Figure C.5 and C.6). It was designed for high temperature measurements. A card sleeve had to be added to the probe station.

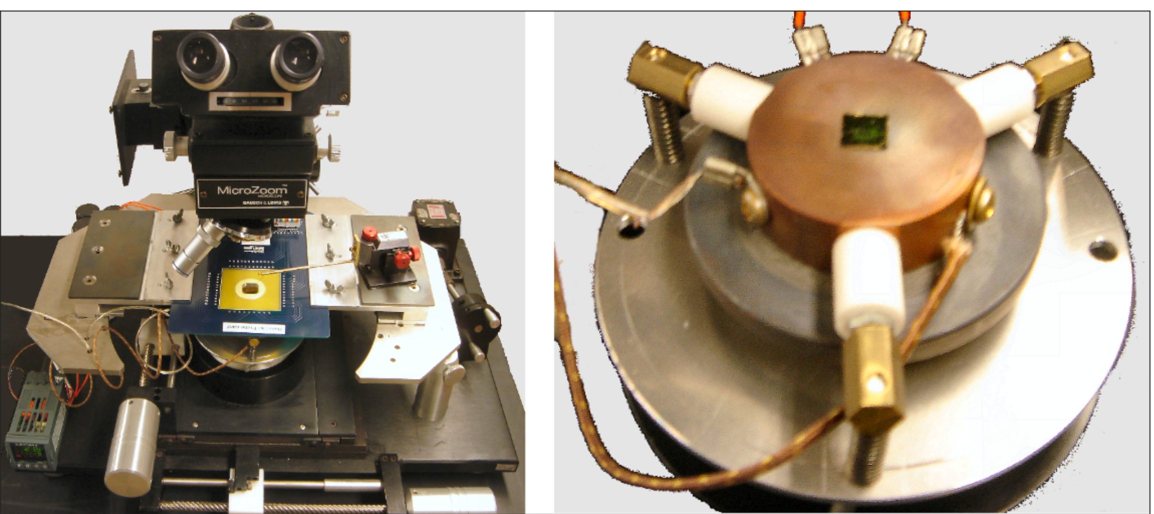



**Figure C.4:** Left: probe station. Right: custom-built hot chuck.

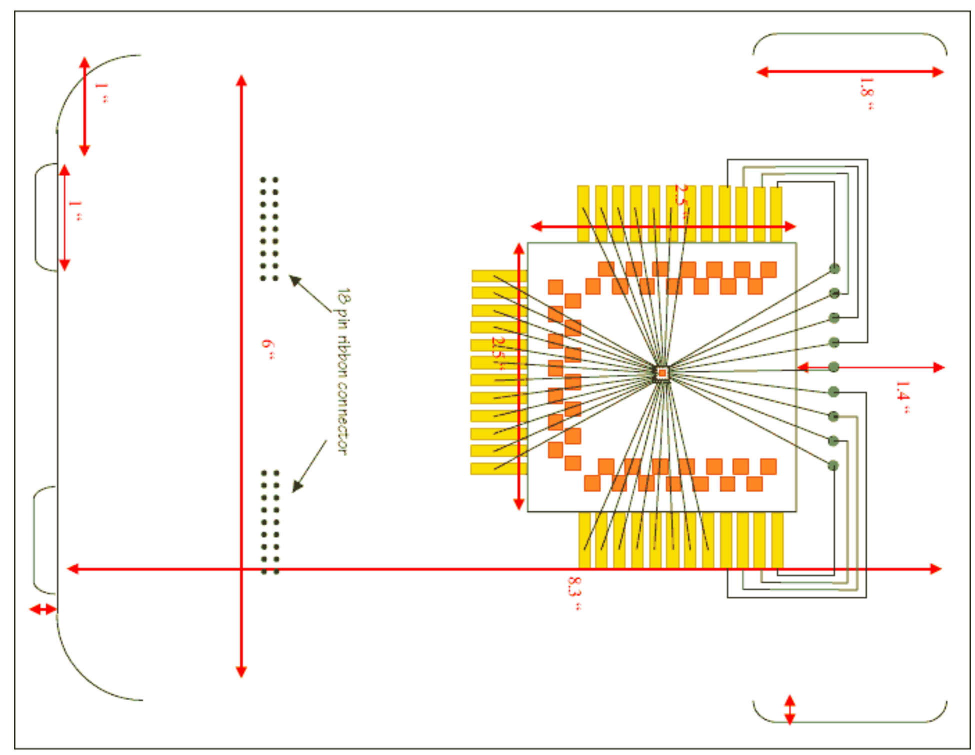



**Figure C.5:** Schematic of the TDDB probe card.

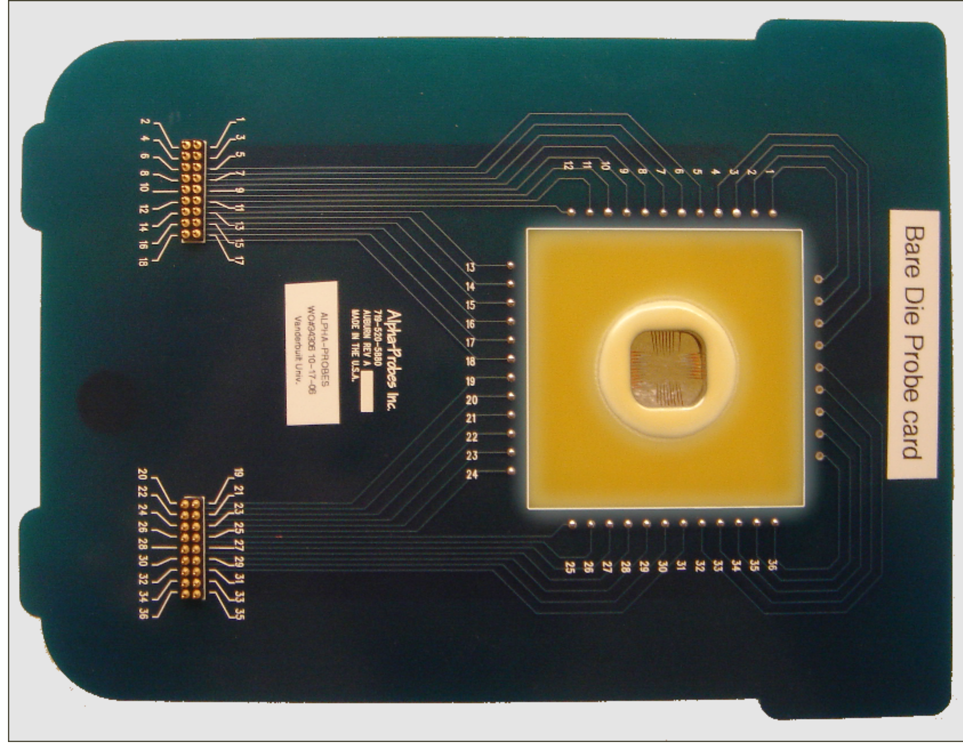



**Figure C.6:** Picture of the TDDB probe card.

## Electronics

A schematic of the electrical connections is shown in Figure C.7. Resistors (10 kΩ) are positioned in series with the tested devices so that individual currents can be probed successively by a multi-meter (Keithley 193) using switch matrix cards (Keithley 7053) and a scanner (Keithley 705). The bias is applied simultaneously to the desired devices using another set of switch cards and a power supply (Keithley 228A). The 36 probes carry the high output signal and the copper chuck is the common low.

As illustrated in the diagram, two ribbon cables connect the probe card to the box. For clarity, the schematic is shown only for the first ten devices. Two 10-channel matrix cards are used. The first one enables the multi-meter (DMM) reading via a ribbon connector carrying the low input of the DMM and the individual signals on the probe side of the resistors. The second switch card allows for the removal of a deficient device from the experiment as it controls the individual bias connections. When the device is disconnected, both of its electrodes are shorted to avoid noise in the measurements. Indeed, parasitic signal propagates easily in ribbon connectors so their length is kept minimum as well. This also reduces additional resistance, preventing errors in the current reading.

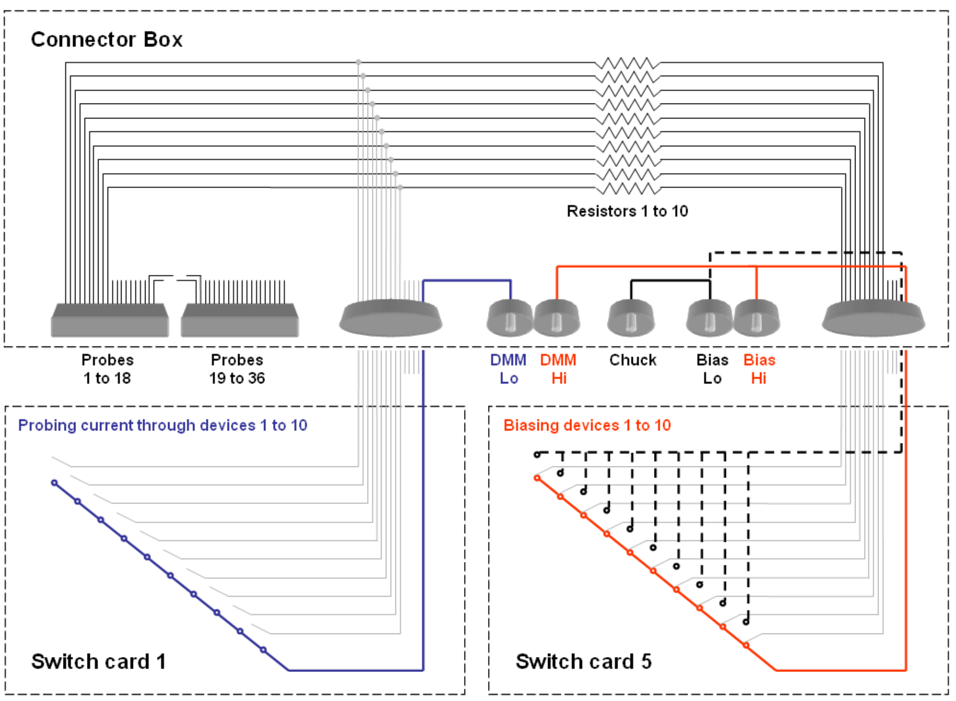



**Figure C.7:** Schematic of the TDDB setup electrical connections.

### Acquisition software

A screen capture of the custom-designed acquisition program is shown in Figure C.8. It allows for real-time monitoring and control of the TDDB measurements.

First, the contact between the individual probes and the devices are checked by the user using a small bias and two-point measurements with the normal probe. The user can signal missing contacts to the program so that the corresponding dots are not included in the experiment (no measurement, no bias).

Then, a set bias is applied simultaneously to all contacted devices and the individual currents are extracted from the voltmeter, sequentially measuring the potential differences on the resistors. One scan loop is completed when one measurement is made on each working device. To avoid wearing down the electrical switches, the time between loops is proportional to the total time elapsed. Since scans are more frequent at short times, it has a limited effect on the data time-resolution. The display shows which dot is being probed and an indicator bar indicates how close the last current reading is from the critical value.

When a threshold current is reached (checked three consecutive times), the corresponding dot is considered "failed" and is removed from the experiment (measurement and bias). The program keeps track of the individual failure times to output cumulative percent failure vs. stress time.

Because the loss of contact between a device and a probe can be a concern, a subroutine is included in the program to allow the interruption of the scans. In the meantime, the working devices are still biased so that the normal probe can be used for the two-point check. Before resuming the scans, the user can enter eventual bad contacts. Corresponding dots are then removed from the measurements and the cumulative percent failure is renormalized.

The experiment ends when all dots have failed.

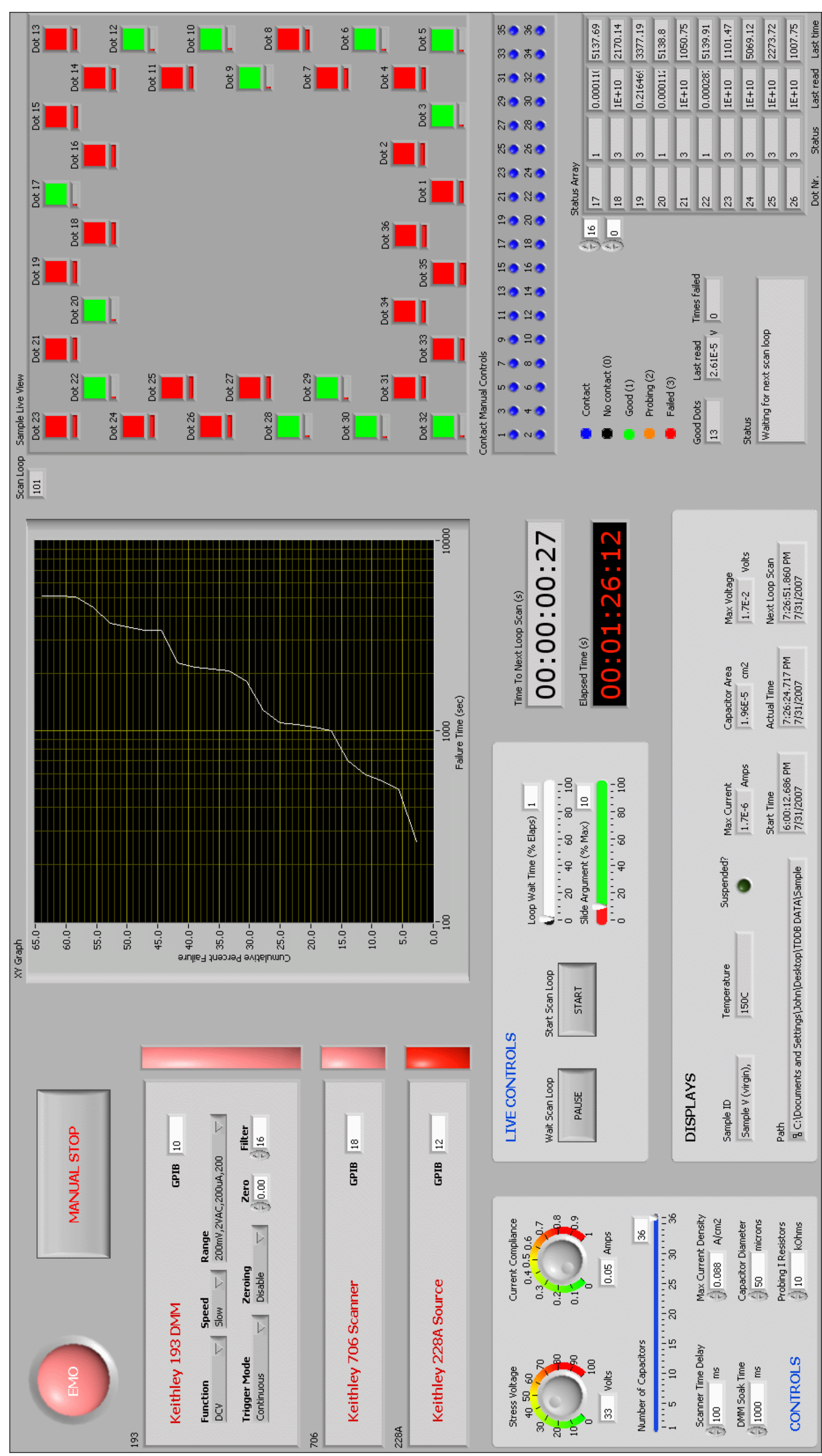



**Figure C.8:** Custom LabVIEW program controlling TDDB measurements.