RADIATION-INDUCED CHARGE TRAPPING STUDIES OF ADVANCED Si AND SiC BASED MOS DEVICES

By

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CHAPTER I

INTRODUCTION

1.1 Thesis Introduction

Ionizing radiation exposure of metal-oxide-semiconductor (MOS) devices can alter their electrical performance, sometimes leading to failure. Permanent failure modes such as total dose effects occurring due to continuous exposure to radiation and temporary effects occurring from a transient high-energy particle radiation, viz. single event effects, are some of the most commonly studied device failure mechanisms in the domain of radiation effects and reliability. Radiation species in the form of electrons, photons, neutrons, protons and other heavy ions are omnipresent in a space environment. Electronic systems in satellites deployed in space and in other areas, prone to radiation exposure, run the risk of suffering from these aforementioned damage events during everyday operation. Hence it is extremely important to carefully design radiation-hardened electronics in satellites used for inter-planetary space exploration, communication, navigation, and surveillance purposes. Additionally advanced weaponry, instrumentation in nuclear power plants and detectors in high-energy radiation physics also have to be manufactured considering the ill effects of radiation exposure [1].

The consequences of radiation damage have been studied over many years to understand the physics associated with the device failure. Careful research to decipher the fundamental mechanisms has resulted in an enormous growth of this field of science. Furthermore these radiation studies have led to a better understanding of the commonly

observed intrinsic defects in the MOS device structures. As a consequence the generation, evolution and annealing of processing related, as well as radiation-induced defects, have been well understood from the perspective of a typical poly-Si/SiO_2/Si MOS device configuration [1]. However these studies need to be extended further to the current technology trends, which predict substitution of these traditional materials in future MOS devices designed for high as well as low operating voltages.

In the realm of microelectronics, there has always been increased pressure to improve the operational speed and efficiency in semiconductor devices. This has stimulated enhanced research activity in the device community with regard to materials and electronics for advanced technologies. MOS devices have been at the forefront of the silicon technology revolution, owing to their ubiquitous use in integrated chips (ICs). From a materials perspective, the IC manufacturing industry owes a great deal of its success to the existence of the silicon (Si) and the ability to grow a thermal oxide on silicon, i.e., silicon dioxide (SiO_2). The continuing demand for device scaling and high-power electronics has raised concerns over the use of conventional materials in the device architecture. Efforts are underway to change the poly-Si/SiO_2/Si combination in the integrated circuits as each material has its own limitations in their functionality for future devices.

Silicon as a device substrate, has dominated electronic materials for the past forty years. However silicon is not ideal for high power and high temperature applications where a wider band gap and a higher thermal conductivity are desirable [2, 3]. Some important areas highlighting such widespread applications would be electric power transmission and distribution, aircrafts, spacecrafts, ships and other instrumentation that

require superior radiation hardness. Wide band-gap semiconductors with band-gap larger than 2 eV viz. silicon carbide (SiC), diamond and the group III-nitrides are the potential replacements, are capable of better performance under such extreme environments. SiC seems to be the leading contender owing to its commercial availability and ease of integration into the state-of-the-art complementary-metal-oxide-semiconductor (CMOS) fabrication sequence. This primarily is due to its ability to oxidize thermally to form the gate oxide (SiO_2), like silicon [4, 5]. Additionally, silicon carbide (SiC) possesses unique physical properties that are extremely favorable for high temperature and high-power electronics [2, 3]. This has led to the growth of SiC in the domain of power metal-oxide-semiconductor field effect transistors (MOSFETs) similar to the existing Si power MOSFETs [6].

A good quality interface (SiO_2/SiC) and a high quality bulk oxide are important factors in determining the eventual use of these materials for SiC-based MOSFETs. Following oxidation, the densities of interface traps in SiO_2/SiC structures typically are on the order of 10^{12} - 10^{13} cm^{-2} eV^{-1}. Our group, and a few others, has successfully demonstrated a reduction in these densities using NO, H_2 and NO+H_2 post oxidation interface passivation techniques for SiC based MOS devices. Defects at the interface have been significantly reduced by orders of magnitude to 10^{11} cm^{-2} eV^{-1} [7-15]. With improvements in device quality, reliability is the next key factor to address, which can help determine the practical use of these devices. In this thesis, we report the effect of this interfacial nitrided layer to charge accumulation/trapping using radiation as a tool to generate electron-hole pairs (EHPs) in the oxide. The first part of the thesis deals with understanding the response to radiation induced charge trapping as a function of NO

treatment in MOS devices fabricated using SiC a device substrate for high power applications.

The second part of the thesis includes materials configuration, which is about to alter the traditional poly-Si/SiO_2/Si gate stack mainly, for low power electronics. It relates to examining the reliability of high-κ dielectrics, which was recently announced as the group of materials that would power the device-scaling trend to satisfy Moore's law for the 45 nm and 32 nm technology generations [16, 17]. Gate dielectrics, a key component in electronic devices have been extensively studied in the semiconductor industry. Silicon dioxide has been the gate dielectric material of choice for the industry for the sequential CMOS process. The ability to thermally grow good quality SiO_2 has enabled it to serve the device scaling until the 65 nm technology generation. It exhibits desirable properties like excellent interface quality, low trap density, high thermal stability, thickness controllability, and good reliability.

The shrinking of device dimensions into the deep sub-micron regime has introduced a multitude of problems for the continued usage of SiO_2 in future MOS devices. Serious challenges are being faced due to fundamental limitations of SiO_2, which are almost impossible to overcome in the fabrication and device operation domain. Scaling has resulted in the thicknesses of these dielectrics being reduced down to a couple of monolayers, which not only aggravates the gate leakage current problem but also raises doubts over the uniformity of these films over a 300 mm wafer. The gate leakage increases to values of more than 100 A/cm^2, well above the specification limits of the International Technology Roadmap for Semiconductors (ITRS), especially for low power technologies [18]. The predominant contribution in the rapid increase of the gate

leakage current arises from direct tunneling of carriers between the electrodes for oxides with physical thicknesses below 2 nm. This results in increased off-state leakage current flowing in these devices leading to heat dissipation problems. Various aspects of circuit performance such as stand-by power, operational speed, and noise margin of a CMOS inverter are affected [19]. Additionally, increased boron penetration effects in these thin oxides pose as a major reliability issue for the pMOSFETs. Several other reliability issues like Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), and carrier injection studies due to increased electric fields across the oxides have become increasingly important due to the thinning of these oxides. One reliability problem where an improvement is observed is in the total dose radiation tolerance of these devices due to a significant reduction in the volume of the oxide material. However other reliability concerns and device operational issues far outweigh the improvement of the total dose response. Hence the change to these high-κ materials was determined to be required and industry has begun the replacement of SiO_2 with these alternative gate dielectric materials.

The introduction of high-κ materials in MOS devices has been referred to as the biggest and most important change in the electronics industry in forty years. Hafnium oxide due to its high dielectric constant has been considered one of the possible replacements for SiO_2, to enable future device scaling [19]. Oxides with a higher κ value use a thicker film to achieve the same capacitance. Ideally this reduces the on/off state leakage current flowing through the devices relative to a SiO_2 layer yielding the same capacitance. Oxides physically thicker than 1 nm SiO_2 but with a considerably smaller equivalent oxide thickness (EOT) are being introduced for the 45 nm and 32 nm

technology nodes. The EOT is represented as the thickness of the dielectric in terms of SiO_2 by normalizing its physical thickness with the ratio of its dielectric constant with that of SiO_2 ($\kappa = 3.9$).

$$t_{EOT} = t_{high-\kappa} \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \tag{1.1}$$

Reliability has been of major concern in these devices. It is extremely important to address the issue of reliability in these devices as it involves altering the conventional poly-Si/SiO_2/Si configuration by replacing the gate oxide (SiO_2) with an alternative gate dielectric and the gate electrode (poly-Si) with a metal (TiN/RuO_2/TaN among others) for reasons discussed later in the chapter. Threshold voltage shifts due to charge trapping during processing and subsequent usage in extreme environments can alter the operational characteristics in these devices [20-28]. Owing to a higher dielectric constant, the pressure on oxide thinning has eased out. However the prospect of using thicker oxides has resurrected the total dose radiation response issue due to the increased vulnerability of these devices to radiation damage. Furthermore, it is important to fundamentally understand the behavior of this new set of materials with their exposure to incoming radiation. The introduction of metals as the gate electrode instead of poly-Si may also affect the damage in these thin oxides due to dose enhancement effects as will be discussed in further detail in this thesis. It is of great significance to the radiation effects community to achieve a better understanding of the charge trapping characteristics of these materials and a determination of how they compare to the traditional SiO_2 based devices. Due to the increased certainty of these devices being the building blocks of

electronic components in future space components, total dose response is one of the areas under extensive scrutiny. In the second part of this report we pursue this objective by investigating the reliability of these devices from the perspective of charge trapping under bias stress and under conditions of exposure to x-ray irradiation.

By combining the aforementioned parts of the thesis concerning the radiation responses of these two material systems, this dissertation aims to provide additional information for establishing reliable design rules for future MOS devices intended for both, high and low operating voltage when exposed to a radiation environment. This chapter starts with a brief introduction about fundamental material properties of the two material systems in question (SiO_2/SiC for high power and HfO_2/Si for low power electronics) followed by experimental results in the forthcoming chapters.

1.2 Materials introduction

1.2.1 Silicon Carbide (SiC) – candidate material for high power devices

Silicon carbide is a suitable candidate for high temperature and high power electronics for a variety of reasons, namely, larger band-gap, higher thermal conductivity and higher critical field as compared to silicon [2, 3]. With its potential use at higher temperatures, wider band-gap offers the advantage of lower leakage currents. Furthermore, the detrimental effects of device heating on its performance can be significantly minimized due to higher thermal conductivity. A higher critical field as compared to Si serves to lower the on-resistance for high power devices. The power dissipation relationship of $P = I^2 R_{on}$ explains the role of the on-resistance (R_{on}) in these devices. The on-resistance is the total resistance from the source to drain in the linear

portion of the on-state of device operation. It consists of resistances from the source, channel, drift, drain and the source and drain contact regions. A detailed representation of these regions in a SiC Power MOSFET is as shown in Figure 1.1. The predominant

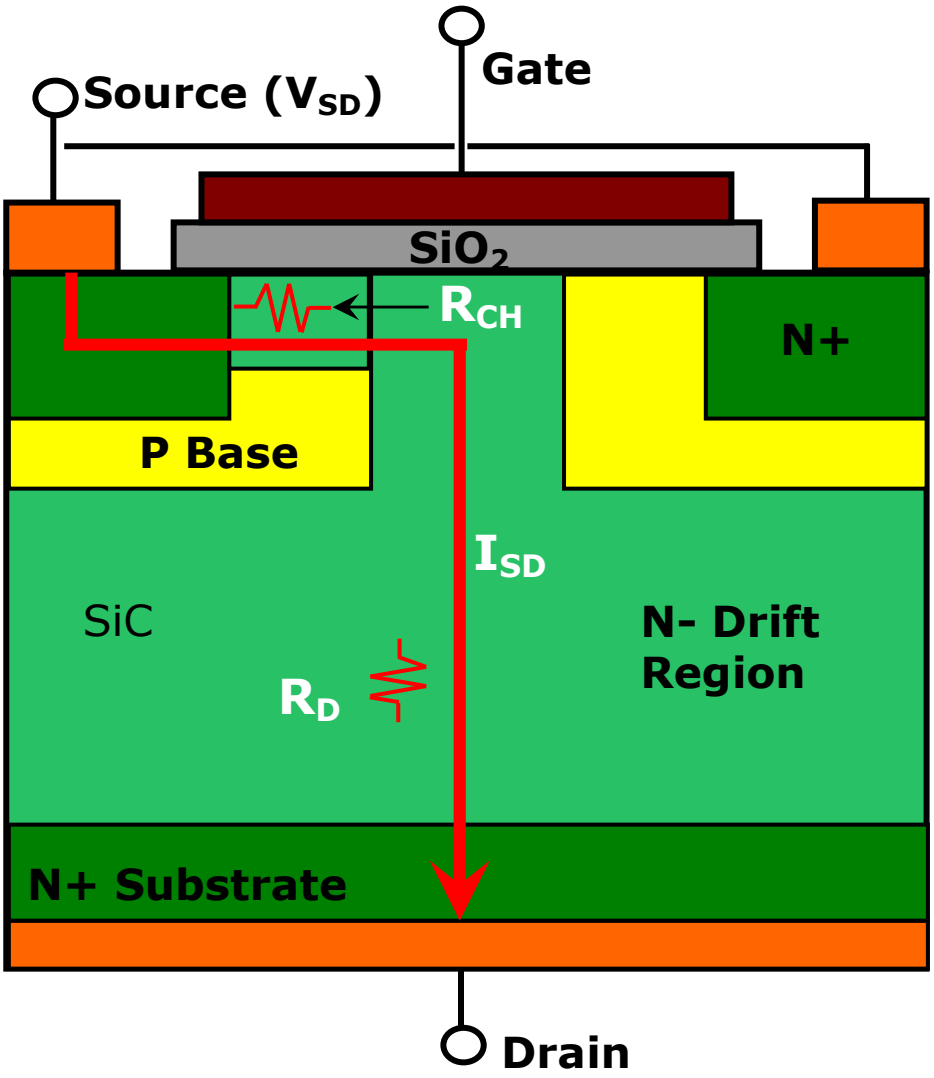

Figure 1.1. Schematic diagram of a vertical power MOSFET. *n*-inversion channel formed by the application of a positive gate voltage. The arrow indicates the flow of electrons from source to drain.

contribution to the resistance comes from the region with a higher breakdown voltage, the drift region, due to its relatively low doping. The low doping leads to the space charge region being formed mostly in the drift region at the body-drift *p-n* junction under bias

with the applied voltage across it. The specific on-resistance (on-resistance multiplied by the area) of the drift region, and thus the ideal specific on-resistance, is given by

$$R_{on,sp} = \frac{4V_{BD}^2}{\varepsilon_s \mu_n E_{BD}^3} \tag{1.2}$$

where V_{BD} is the expected breakdown voltage, ε_s is the permittivity of SiC, μ_n is the bulk carrier mobility, and E_{BD} is the critical breakdown field [3]. This specific on-resistance needs to be minimized as shown in Figure 1.1. The breakdown field in the denominator of equation 1.2 can be imagined in terms of the critical field (E_c) that can be sustained by the drift region before breakdown. The thickness of this drift region is defined by the amount of depletion in the ON mode of the device. With low doping in the drift region, the depletion width is larger as $x_d \propto (N_d)^{-1/2}$. The doping can also be adjusted such that the maximum field that can be applied is close to the critical field at which avalanche breakdown occurs E_c. Since $E_c \propto (E_g)^{1/2}$, the higher E_g of SiC allows for a higher critical field that can be applied before breakdown occurs. Hence this factor of a higher E_{BD} plays a significant role in reducing the $R_{on,sp}$ as shown in equation 1.2. Hence with higher breakdown fields (~ 7 times) than silicon, the device functions at higher voltages with a lower on-resistance.

Crystallographically SiC consists of bilayers of tetrahedrally bonded silicon and carbon atoms. It may be composed of layers with the same stoichiometry but a variable order of stacking along the stacking direction, the c-axis. This phenomenon of one-dimensional polymorphism is called polytypism. Silicon carbide has more than 200 polytypes. The most common are 3C, 4H, 6H, and 15R with the alphabetic notations referred to as Ramsdell's notations, relating to the crystal structure with C meaning Cubic, H – Hexagonal, and R – Rhombohedral and so on. Different polytypes show

different band gaps with 3C having a band gap of 2.4 eV and 4H with a band gap of 3.3 eV. The 4H-SiC is most suitable for high power applications due to its wider band-gap and higher and isotropic electron mobility [29].

A quantitative comparison elucidating the advantages of 4H-SiC compared to Si is as shown in Table 1.1 [30-33]. A symbolic representation of the stacking sequence of 4H-SiC is as shown in Figure 1.2. 4H-SiC MOSFET technology usually involves crystal

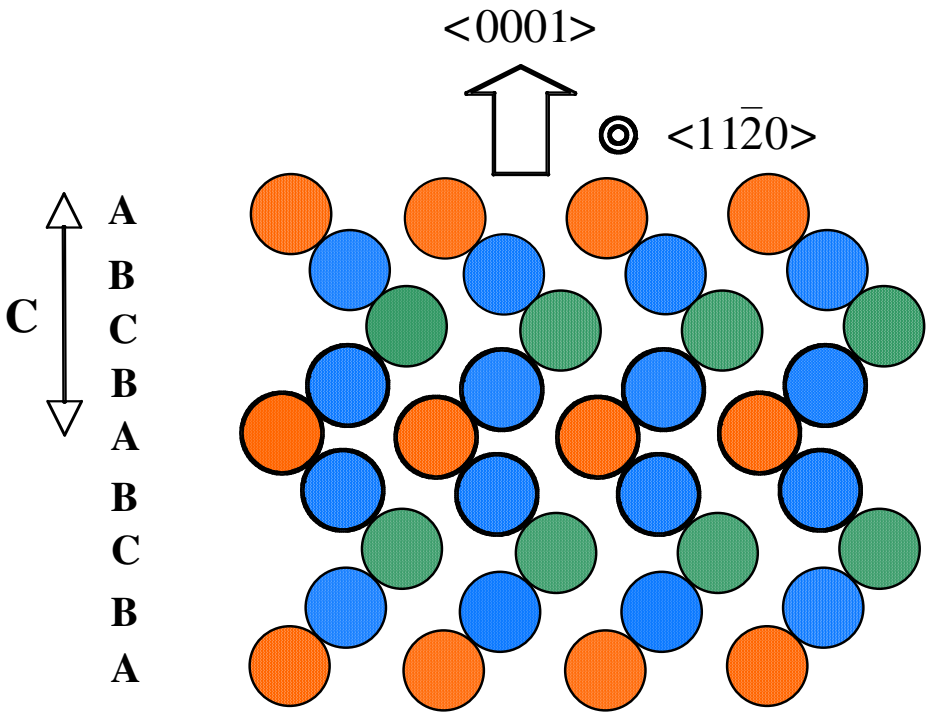

Figure 1.2. Figure showing the (11$\bar{2}$0) plane of the 4H-SiC polytype showing the Si-C bilayers with a height c of the 4H unit cell of about 10.05 Å (Figures adopted from http://matsunami.kuee.kyoto-u.ac.jp).

faces of either (0001) Si-face, (11$\bar{2}$0) a-face, or (000$\bar{1}$) C-face. The faces are as shown schematically in Figure 1.3. The (0001) Si-face is a basal plane in the hexagonal close

Table 1.1 A quantitative comparison highlighting the advantages of 4H-SiC compared to Si [30].

Property	Si	4H-SiC	
Lattice constant (Å)	a = 5.43	a = 3.073, c = 10.05	
Band gap (eV) at 300 K	1.12	3.26	
Dielectric constant (ε_r)	11.9	9.7	
Intrinsic carrier density (cm^{-3})	1.45×10^{10}	8.2×10^{-9}	
Electron mobility (cm^2/V-s)	1417	$\mu_{e\perp c}$	$\mu_{e\parallel c}$
		880	800
Hole mobility (cm^2/V-s)	471	≤ 120	
Electron effective mass ($\frac{m_{\perp e}}{m_0}$); (density of states calculations)	1.08	0.45	
Hole effective mass ($\frac{m_{\perp e}}{m_0}$); (density of states calculations)	0.55	0.66*	
Thermal conductivity (W/cm-s)	1.5	4.5	
Saturation carrier velocity (cm/s)	1.0×10^7	2.0×10^7	
Critical field	0.3	2.0	
Specific on-resistance (relative to Si)		3×10^{-3}	

pack structure with all the surface atoms consisting of Si atoms. The opposite face of this basal plane is $(000\bar{1})$ C-face, which is C-terminated. The $(11\bar{2}0)$ a-face is a non-polar face with 50 % C and 50 % Si atoms in the plane as represented by the shaded area in the figure. Most previous studies have considered the (0001) Si-face as epitaxial growth

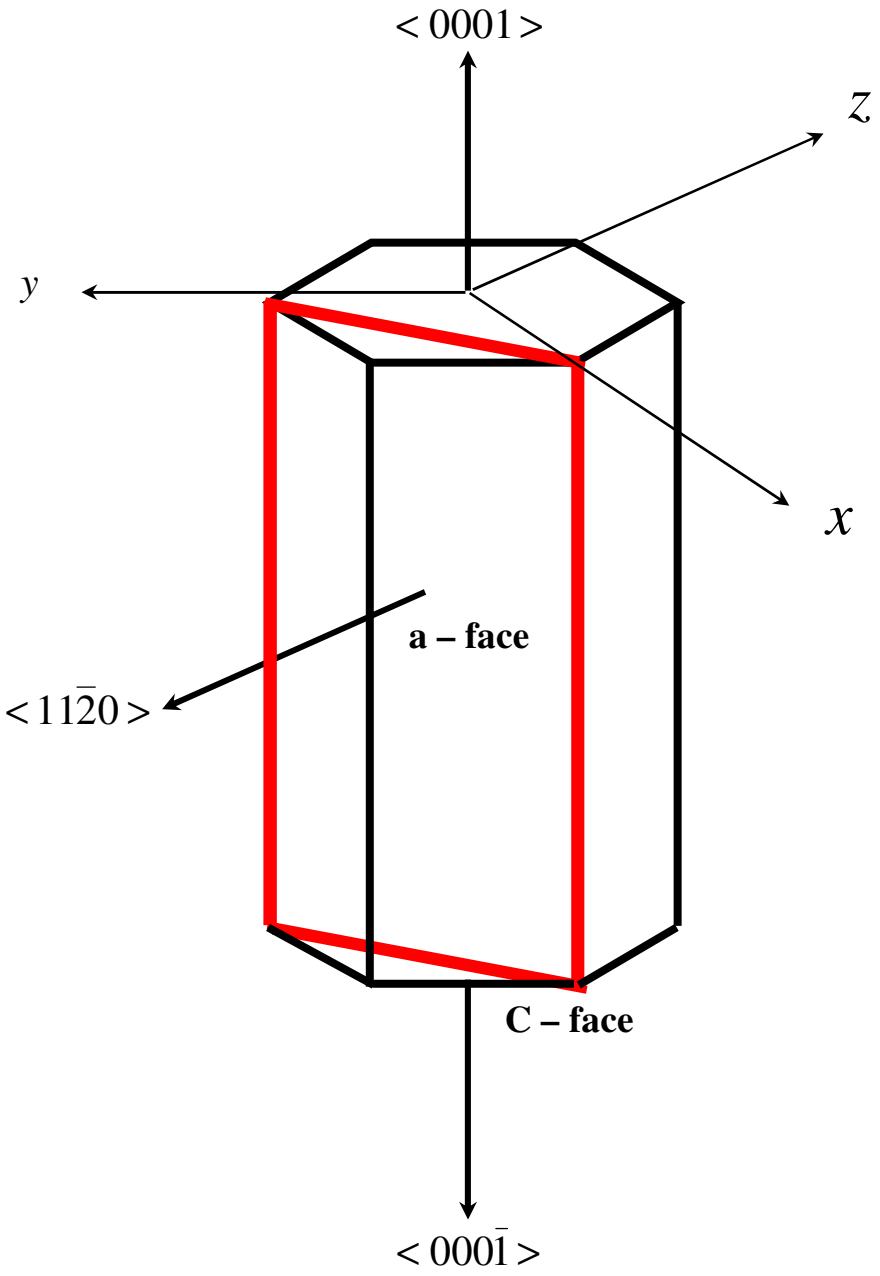

Figure 1.3. The (0001) Si-, (11$\bar{2}$0) a- and (000$\bar{1}$) C- faces of SiC.

techniques are more developed on this face. Owing to a better technical understanding of the Si-face we have tried to address the reliability concerns on this particular face in this study. However from the perspective of inversion layer mobility, it has been reported that the highest mobility occurs for the (11$\bar{2}$0) a-face.

In comparison with silicon, where the channel mobility is about one third of its bulk mobility, the highest reported channel mobility in SiC is about 100 cm^2/Vs for 6H and 20 cm^2/Vs for 4H prior to any post-oxidation annealing treatment. These are much lower than Si when compared with the respective bulk values of 400 cm^2/Vs and 800 cm^2/Vs respectively. The low effective channel mobilities are largely due to higher interface trap densities (D_{it}) near the conduction band edge, large problem in *n*-type 4H-SiC as compared to the *n*-type 6H-SiC [34]. Figure 1.4 shows the interface trap density as a function of the band-gap for 4H and 6H-SiC as measured using the Hi-Lo Capacitance-

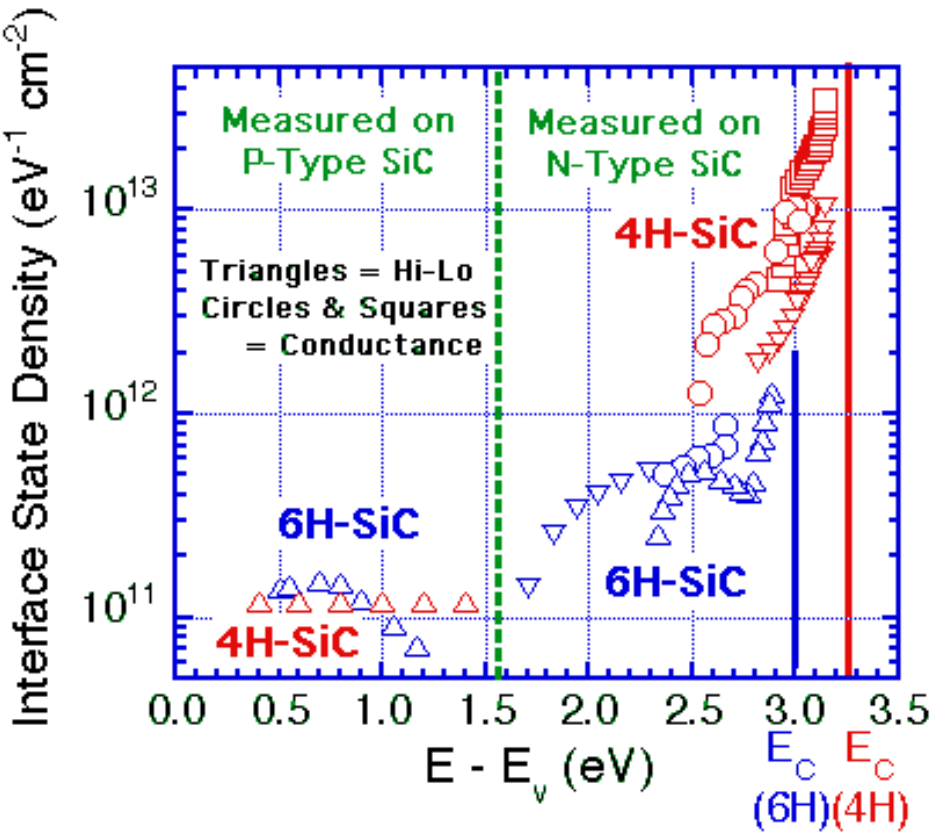

Figure 1.4. Interface trap density across the bandgap in 4H and 6H-SiC, as measured by the Hi-Lo CV technique (triangles) and the AC conductance technique (circles and squares) [34].

Voltage (C-V) and AC conductance techniques as measured by Das *et al.* [34]. In 6H-SiC with E_g ~ 2.9 eV, most of the defect states lie above the conduction band edge, while for 4H-SiC (E_g ~ 3.3 eV), these fall into the forbidden gap. Nitrogen incorporation at the interface has proven to be a reliable way to enhance the inversion layer mobility using post oxidation anneals in NO and N_2O [7-14]. In some cases a further improvement was achieved by following this with an annealing step in H_2 ambient [15]. In the future course of the thesis we limit ourselves to discussions on the 4H-SiC polytype. It was observed that mobility enhancements achieved due to post oxidation annealing treatments on SiO_2/4H-SiC were strongly dependent on the crystal face with the maximum mobility being achieved with NO+H_2 treatment for the a-face SiC. Figure 1.5 shows the field effect mobility on lateral test MOSFETs on two of the crystal faces (Si-face and a-face) after both the passivation procedures [30]. With continuous improvement in the device quality and mobility values, SiC is on the verge of application for high power devices, and we address the reliability issue from a radiation tolerance point of view. We report the first observation of enhanced positive charge trapping in nitrided devices and discuss the need to optimize the nitrogen content during post oxidation anneals to improve reliability in these device structures.

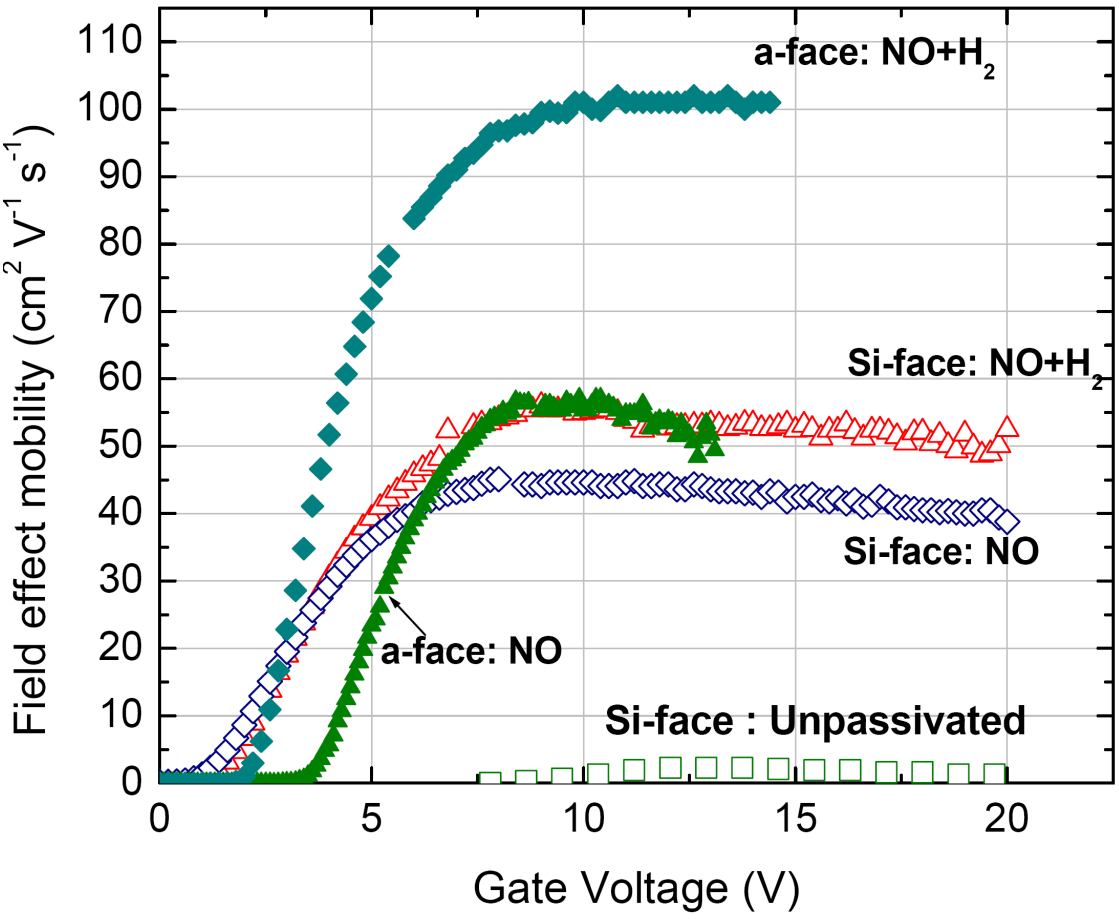

Figure 1.5. Plot of the improvement in the field effect mobility as a function of gate voltage for the Si-face and a-face 4H-SiC samples with different passivation procedures [30].

1.2.2 Hafnium Oxide (HfO_2) – future candidate material for low power devices

The continual scaling of devices follows the famous prediction by Dr. Gordon Moore in the 70's, which is now referred to as the Moore's Law where he mentioned that the total number of devices on a chip would double every 2 years. The trend has been maintained (Figure 1.6) [16, 17]. As mentioned previously this has resulted in better integrated circuit functionality at lower cost. One reason for this successful scaling is the excellent material and electrical properties of the dielectric (SiO_2). The concept of packing more transistors on a single chip necessitates constant thinning of this dielectric for each generation. Figure 1.7 shows the decreasing feature size and gate oxide thickness over the years [35]. With technologies reaching below the 90 nm, a number of roadblocks are being encountered to keep pace with the Moore's law of scaling. Ultrathin silicon dioxide and its nitrided alternatives not only have fundamental limitations, but it is increasingly difficult to manufacture and control. Direct tunneling of electrons between the electrodes through the oxide increases the off-state leakage current [19]. At high fields in the oxide, the tunneling current is predominantly Fowler Nordheim, where $V_i = E_i d > \Phi_B$ (Φ_B = barrier height) and at low fields direct tunneling is observed, where $V_i = E_i d < \Phi_B$ [36, 37]. The direct tunneling current is a strong function of the thickness of the material and its band offsets. The transmission probability (T) is given by [36, 37].

$$T = \left\{ 1 + \frac{E_0^2 \sinh^2 kW}{4E(E_0 - E)} \right\}^{-1} \tag{1.3}$$

and,

$$k = \left\lfloor \sqrt{\frac{2m(E_0 - E)}{\hbar^2}} \right\rfloor$$

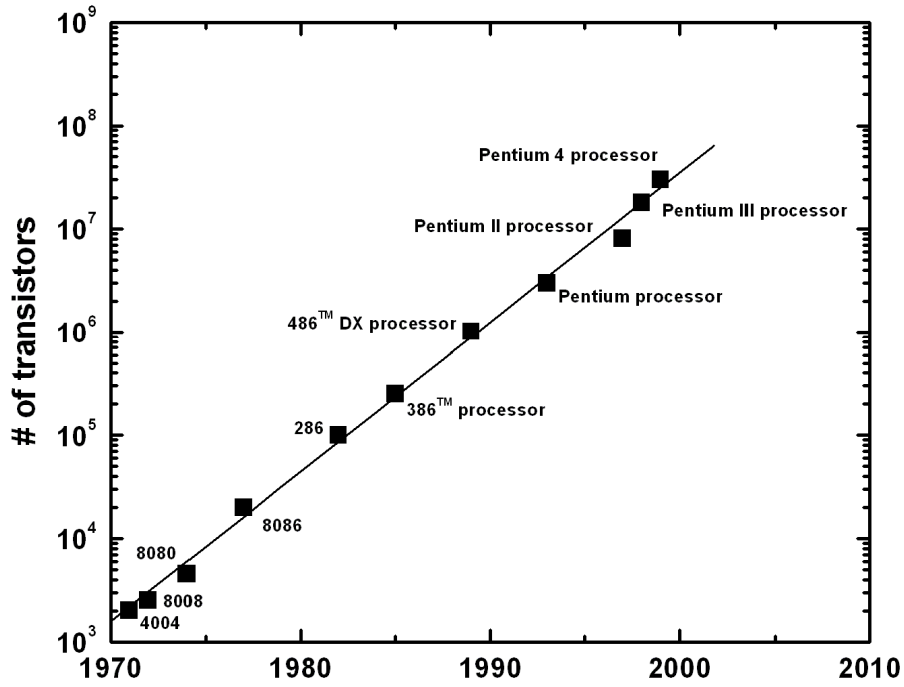

Figure 1.6. Plot showing number of transistors increasing over the years in Intel transistors [35].

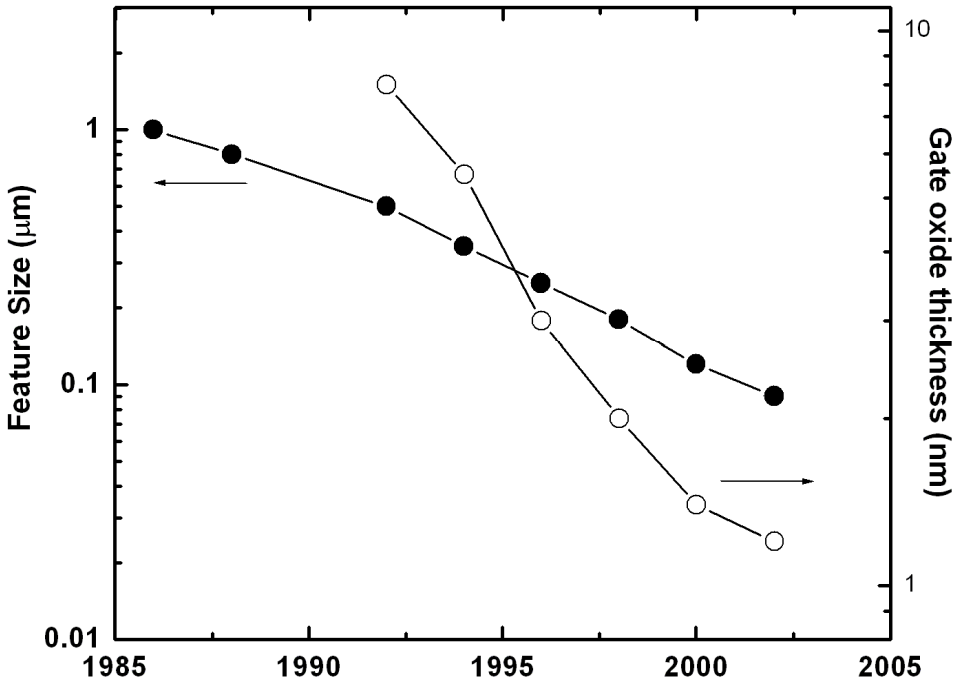

Figure 1.7. Plot of the decreasing feature size for the respective technology node with decrease in gate oxide thickness (secondary Y axis) over the years [35].

where, E_0 is the band offset, E is the energy of the incoming particle and W is the material thickness. Hence with thinner SiO_2, the predominant form of leakage is from direct tunneling of carriers. From the materials point of view we need to recall that the limit for thickness scaling of SiO_2 is about 0.7 nm for the full band gap of SiO_2 bulk to be formed. However with the inclusion of interface roughness this number increases to 1.2 nm [38]. This reduced band offset can additionally increase leakage current in these thin dielectrics. Figure 1.8 highlights the gate leakage problem with a simulated tunneling current in the MOS structure plotted as a function of potential drop in the oxide (V_{ox}) for

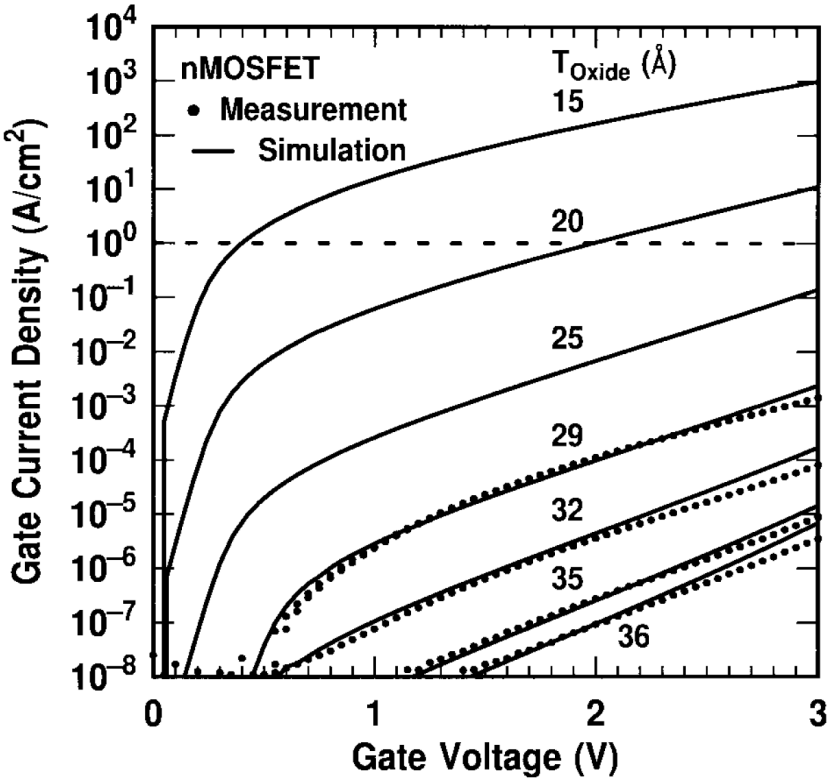

Figure 1.8. Simulation results of gate tunneling current for various SiO_2 thicknesses [39].

various SiO_2 thicknesses [39]. Reliability also becomes a problem in these thin devices because current flowing through these oxides during its operation can result in generation of defects in the bulk of the oxide as well as at the SiO_2/Si interface. When a critical density is reached, breakdown (or quasi-breakdown) can occur resulting in failure of the device [40-42]. This phenomenon was explained using a percolation model approach from the time-to-breakdown distributions of ultrathin layers of SiO_2 by Degraeve *et al*. [43, 44].

The Semiconductor Industry Association (SIA) has established some of the technical goals to be achieved for technologies below 90 nm node as shown in Table 1.2. These include introducing new gate stack materials and integration processes for the CMOS fabrication scheme, including surface and interface control.

Table 1.2 The SIA roadmap for future technology nodes

Year	2007	2010	2013	2016
Technology mode	65	45	32	22
L_{gate} (MPU)	35 nm	25 nm	18 nm	13 nm
EOT (nm) MPU	0.9	0.7	0.6	0.5
Gate-leakage (nA/μm) @ 100 °C	230	330	1000	1670
Nominal V_{DD} (V)	1.1	1.0	0.9	0.8

1.2.2.(i) Other high-κ dielectrics

A search for a material beyond the conventional thermally grown SiO_2 has brought a multitude of alternative gate dielectric materials into contention. They enable

the scaling with a higher dielectric constant (κ) wherein the capacitance (C) can be maintained the same by increasing the thickness (d) of the gate dielectric (Eq. 1.4).

$$C = \frac{\kappa \varepsilon_0 A}{d} \tag{1.4}$$

This increase in thickness of the gate oxide reduces the leakage by orders of magnitude, at the same time keeping a considerably low effective oxide thickness (EOT). Figure 1.9 shown below compares the leakage current density J_g decrease for a high-κ material with an EOT equivalent to that of SiO_2 with t_{phys} = 15 Å [19].

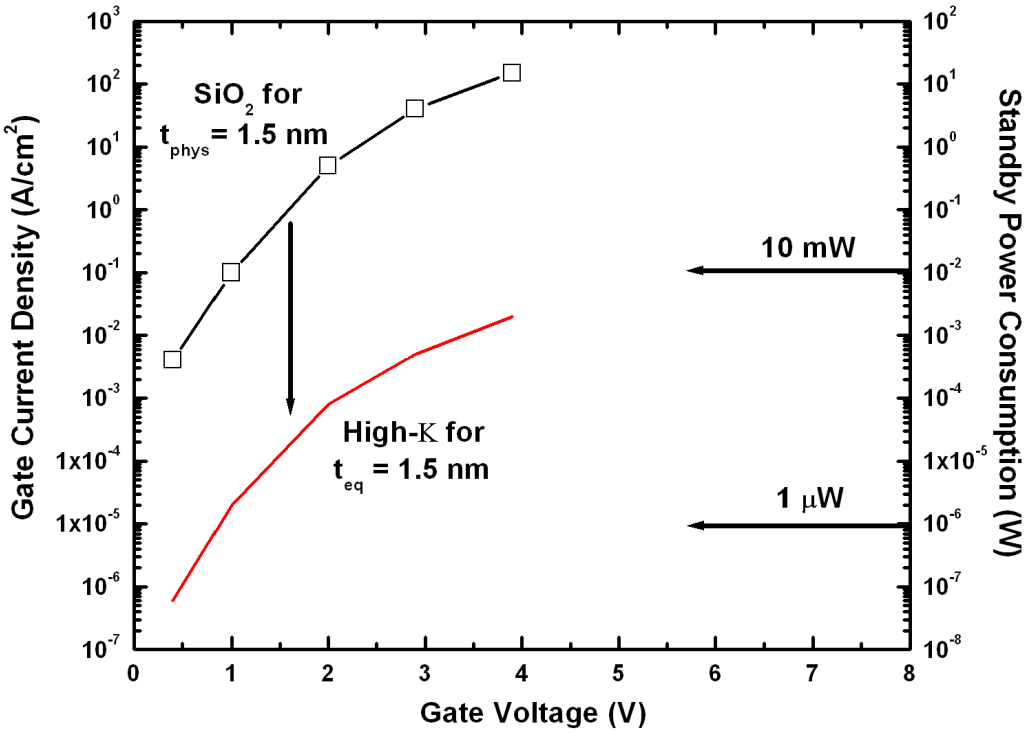

Figure 1.9. Comparison of gate current densities for t_{phys} = 1.5 nm SiO_2 as against t_{eq} = 1.5 nm for high-κ as a function of gate voltage. This highlights orders of magnitude reduction in J_g thereby leading to a reduction in standby power consumption (alternate Y axis) [19].

Alternative gate dielectrics involve a wide range of materials with κ ranging from 4 to sometimes higher than 100. For evaluating its material properties, we broadly classify them into three different categories, moderate-κ ($4 < \kappa < 10$), high-κ ($10 < \kappa < 100$) and ultra high-κ ($\kappa > 100$). In the forthcoming section we consider a couple of materials of interest in each category for further discussion.

One of the ultra high-κ materials, BST ($(Ba, Sr)TiO_3$) with $\kappa \sim 300$ has been investigated by various groups for DRAM [45] as well as MOS applications [46]. Large hysteresis is one of the major issues in these materials and the formation of a low-κ interfacial layer interferes with the objective of achieving a lower EOT. Additionally due to increased κ, the short channel MOSFET cross-section for the dielectric appears more like a rectangle instead of a sheet which requires the channel potential to be controlled not only by the gate but also by the source and drain [47]. Although these issues can be taken care of with a reduced effective κ due to the low-κ interfacial layer, several other issues have to be sorted out for these materials to be introduced into the MOS fabrication line.

In the category of moderate-κ materials, Si_3N_4 stands out as one of the most suitable materials to substitute SiO_2 due to excellent interface and better reliability [48, 49]. But the relatively low-κ value of ~ 7.5 is not necessarily ideal for long-term scaling. Al_2O_3 is a similar candidate with $\kappa \sim 10$ with large band offsets and well-behaved MOSFET characteristics but shows poor carrier mobility owing to interfacial fixed charges [50, 51]. This results in a higher D_{it}, which is related to the mobility degradation from Coulomb scattering [52]. Hence its candidacy is hampered by a combination of these problems with a not so high κ value. Finally various materials with a high κ value

($10 < \kappa < 100$) were studied as replacements for SiO_2. Investigations carried out on Ta_2O_5 and TiO_2 ($\kappa \sim 80$) revealed the thermal instability of these oxides to Si when exposed to high temperatures of processing and fabrication [53-59]. Studies by Hubbard and Schlom elucidate the thermodynamic stability of binary metal oxides on silicon [60]. In this work, the Gibb's free energy calculations were carried out for reduction of metal oxides and silicide/silicate formation. These show that BeO, ZrO_2 and MgO are thermodynamically more stable as compared to the others. Physical and chemical similarity between Zr and Hf results in identical stability being observed for HfO_2. The similarity is observed in both having approximately the same atomic and ionic radii, (ionic radii for Hf^{4+} ~ 0.78 Å and Zr^{4+} is ~ 0.79 Å), and under ambient pressure, both oxides undergo a phase change from monoclinic to tetragonal to cubic structure (with the same space group in each case) as the temperature increases [61]. Hence ZrO_2 and HfO_2 stand out as the best possible alternatives for SiO_2 in the MOS configuration [62, 63].

Another important aspect to consider during the selection of an alternative dielectric material is the inverse relationship between the dielectric constant κ and energy gap E_g with this being one of factors that define the band offsets between the oxide and the semiconductor. Figure 1.10 shows different oxides and the trend of the dielectric constant with its band gap [19, 64]. Oxides with a higher κ value are composed of elements with a higher atomic number (transition metals) in the periodic table. In the case of these transition metals, the atomic d orbitals are partially filled, which tends to introduce levels with high density of states in the oxide band gap between the anti-bonding and bonding states, which reduce the overall band gap of the dielectric. This

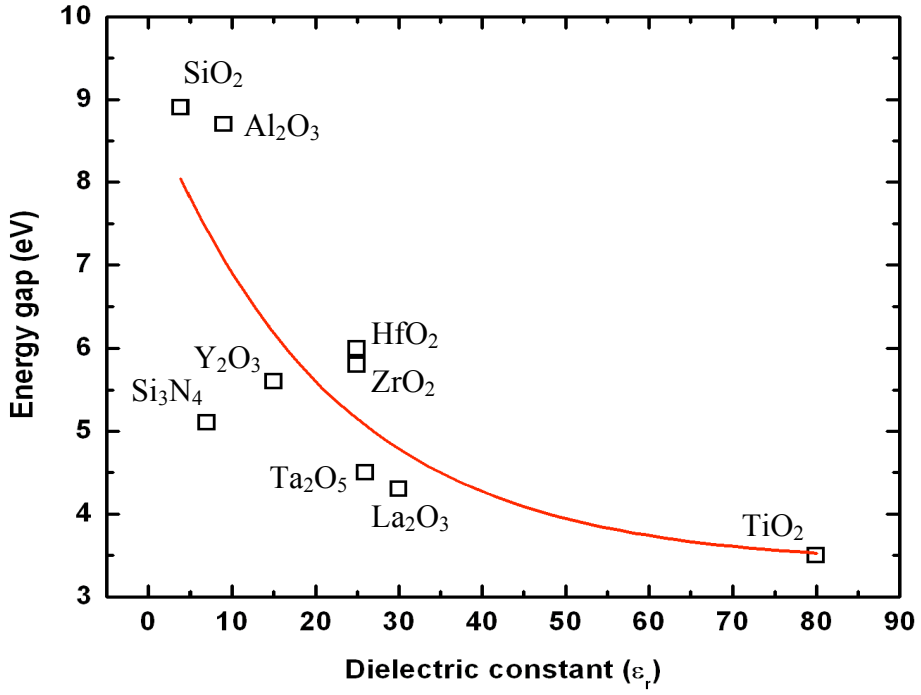

Figure 1.10. Figure showing the trend of reduction of band gap (Eg) with increase in the dielectric constant (ε_r) for various alternate dielectric materials [19, 63].

additionally results in lowered conduction and valence band offsets between the oxide and the underlying silicon, which directly contributes to the increase in leakage current. Figure 1.11 shows a schematic representation of the band gap of various alternate gate dielectrics and its band offset with silicon [64]. Hence the high-κ dielectric has to be wisely chosen and/or the interface has to be appropriately engineered to take advantage of these new materials. Table 1.3 shows the comparison of the fundamental material properties of HfO_2 and ZrO_2. Although ZrO_2 and HfO_2 have similar dielectric constants ($\varepsilon \sim 25$ for both) and similar band gaps ($E_{g(ZrO_2)} \sim 5.8$ eV and $E_{g(HfO_2)} \sim 6.0$ eV), ZrO_2 was seen as less appropriate due to its reduced thermodynamic stability as compared to HfO_2.

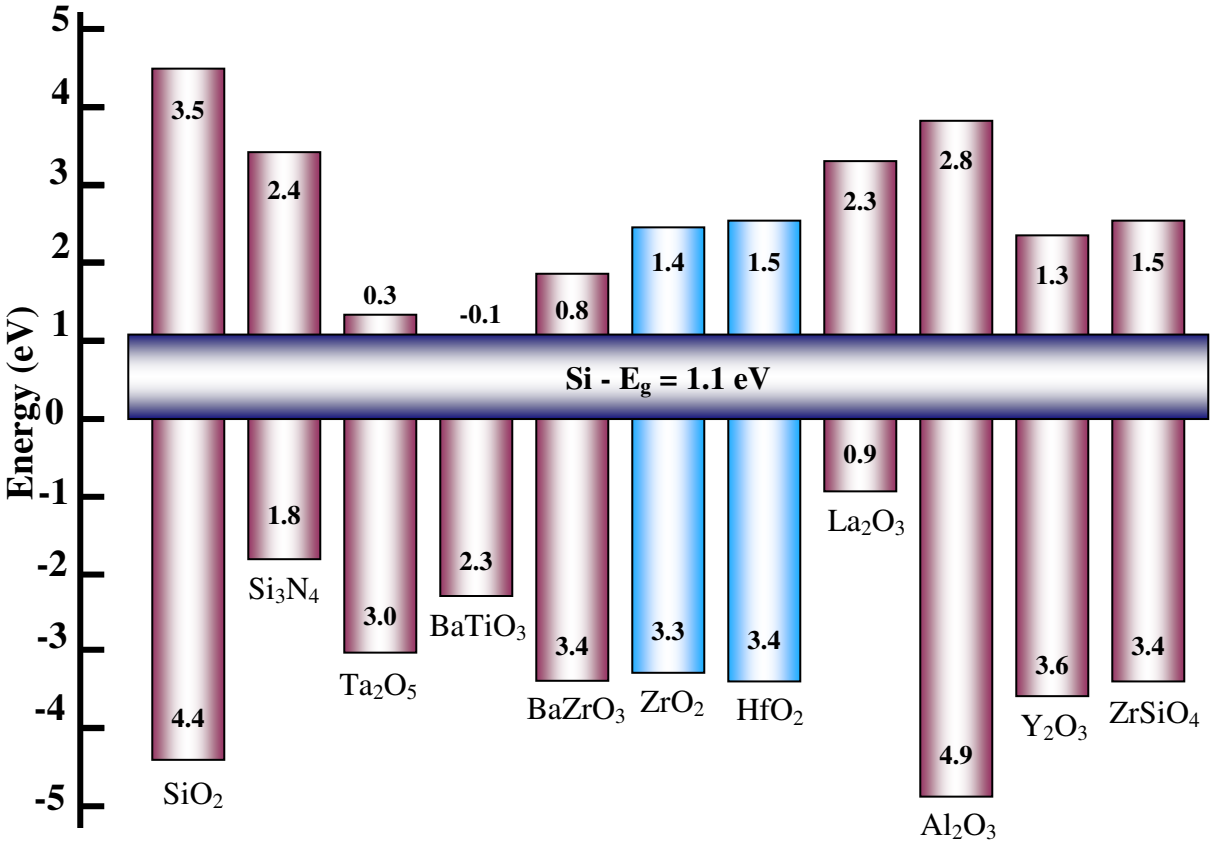

Figure 1.11. Schematic diagram of the band gap of various alternate dielectrics with its band offset for Si [63].

HfO_2 has a more negative Gibbs energy of formation (cf – 260 kcal/mol) as compared to ZrO_2 (cf – 248 kcal/mol) [65]. On contact with silicon, this property was found to reduce interface mixing and prevent/minimize the silicate/silicide formation upon post-formation treatments such as source/drain dopant activation anneals. This enhanced thermal stability has led to HfO_2 as the leading contender [19, 66]. Furthermore, with intense research over the past few years it has been shown that HfO_2 in the form of silicates (to increase thermal budget) and nitrides (to avoid dopant diffusion into the oxide) can be scaled down to an EOT $\leq$ 10 Å to enable device scaling for a couple of technology generations. This report involves the reliability studies undertaken with pure HfO_2 as the gate dielectric in the MOS devices studied.

Table 1.3 Comparison of material properties of SiO_2, HfO_2, and ZrO_2

Material Properties	SiO_2	HfO_2	ZrO_2
Dielectric constant (ε_r)	3.9	~ 25	~ 25
Band gap (eV)	9	6.0	5.8
Conduction band offset (eV)	3.5	1.5	1.4
Valence band offset (eV)	4.4	3.4	3.3
Refractive index	1.46	2.2	2.05
Density (g/cm^3)	2.27	9.68	6.1
Lattice constant (Å)	-	5.11	5.1
Lattice mismatch with Si	-	~ 5.7 %	6 %
Thermal expansion coefficient	0.5×10^{-6} K^{-1}	5.3×10^{-6} K^{-1}	8×10^{-6} K^{-1}

1.2.3 Gate electrode materials

It is important to note that another constituent (gate electrode) of the conventional gate stack of the poly-Si/SiO_2/Si combination had to be changed in order to realize the use of these high-κ oxides. This must be taken into account in reliability studies such as radiation effects, since the total dose in the ultrathin oxide regimes is dominated by the materials around it, as will be discussed in later chapters. Metal gates have replaced poly-Si mainly in order to avoid dopant penetration and poly-Si depletion effects in the ultrathin EOT regimes. Moreover in the case of metal gate electrodes, issues of interlayer mixing at the oxide/gate electrode interface, which reduces the net capacitance of the stack, is drastically reduced. The absence of a poly-Si gate improves the thermal budget by eliminating the need for gate electrode dopant activation anneals. Two approaches are normally employed for the selection of a gate metal, either using a single mid-gap gate metal (TiN – our case) or the use of dual metal gates. Mid-gap gate metals are chosen for having a symmetrical threshold voltage (V_T ~ 0.5 V) for both nMOS and pMOS based devices. In this thesis we present studies involving TiN as the gate metal. On the other hand, use of dual metal gates such as Al for nMOS and Pt for pMOS, reduces this V_T to ~ 0.2 – 0.3 V, a desirable value for below 90 nm technology generation. It is however necessary to consider the unavoidable oxidation of Al at high temperatures and the cost and ineffective adherence of Pt to these gate oxides. This has resulted in using metals such as RuO_2 or nitrided metal gates such as TaN owing to their appropriate work functions, thermal stability with the oxide, low sheet resistance and easy integration into CMOS fabrication [19].

1.3 Thesis outline

This chapter has provided an introduction to the fundamental properties of this new set of materials, which serve to define the future gate stack combination. An attempt has been made to encompass some of the background details into the evolution of these material systems to challenge the existing semiconductor materials domain. Chapter II briefly explains the terminologies with insights into the physical nature and understanding of the processing and radiation induced traps. These are discussed for both, the oxide bulk as well as for the interfaces. It builds on the long existing and relatively well-known literature of radiation response of SiO_2/Si based devices and reviews the current understanding of the SiO_2/SiC and HfO_2/Si based device structures exposed to incoming radiation.

Chapter III describes the materials analysis and pre-irradiation characterization performed on SiO_2/SiC system as a part of this thesis. It also includes a short description of the various analytical techniques used in our group to profile the nitrogen content at the SiO_2/SiC interface. MOS characterization performed for pre-irradiation D_{it} analysis is also included as a part of this chapter.

Chapter IV describes the first observation of enhanced positive charge trapping of nitrided SiO_2/SiC based MOS devices, and their comparison to the response of non-nitrided samples. It includes results from other reliability tests, which confirm the consistency between different experimental techniques. The results indicate a need to optimize the nitrogen content during the post-oxidation passivation procedures to strike a balance between reductions in the D_{it} and simultaneously provide a considerable hardness assurance to radiation effects and other reliability issues.

Chapter V includes several physical characterizations as a part of pre-irradiation measurements performed to verify the stoichiometry and oxide (bulk and interlayer) thicknesses. MOSFET characterization studies undertaken prior to radiation exposure are also discussed.

Chapter VI deals with bias stress and the ionizing radiation response of hafnium based oxides on silicon. The majority of the previous work was done on MOS capacitors with most of them performed on thicker gate oxides. In this work we aim to study the reliability of these state-of-the-art MOS transistors fabricated using an industry standard sequential CMOS process flow. The device response is studied as a function of positive and negative electric fields, with varying bulk oxide and interlayer thicknesses.

Chapter VII describes the results from the radiation induced charge trapping studies performed as a function of varying bulk HfO_2 and SiO_2 interlayer (IL) thicknesses. These studies identify enhanced trapping in the bulk of the oxide apart from discussing additional trapping in the SiO_2 interlayer in thicker HfO_2-based MOSFETs.

Finally in the last chapter, Chapter VIII, we summarize the findings from the experimental results. With this work we hope to provide a useful contribution to the field of reliability physics for materials, which are likely to play a pivotal role in future high and low power devices. We believe this will improve our current understanding of radiation effects and reliability in these devices and eventually design better devices for the future.

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CHAPTER II

RADIATION BASICS & BACKGROUND LITERATURE

2.1 Basics of Radiation Effects

Exposure to ionizing radiation generates electron-hole pairs (EHPs) in semiconductors as mentioned in the previous chapter. In MOS devices, we however worry about device degradation due to these EHPs generated in the oxides. In this chapter we present the mechanisms associated with the interaction of these charged species, predominantly with the gate dielectrics. This interaction depends on the type, kinetic energy of the incoming radiation, charge state and the mass of the incoming projectile and similarly it will also be affected by the mass, atomic number (Z) and density of the target material [1].

The incident species can consist of photons, electrons, protons or any other heavy nuclei, and for matters of relevance to this thesis we restrict our discussion to photon interactions. An incoming photon can interact with matter in three different ways, namely, photoelectric effect, Compton effect and pair production [2]. In the case of photoelectric effect, the incident photon interacts with an electron from the inner shell of the target atom and loses all of its energy thereby ejecting the electron from the atom. This electron is a free electron, often termed as a photoelectron, and has energy equivalent to the energy of the incoming photon minus its binding energy. The photoelectron further traverses through the material to create EHPs. Compton scattering involves higher energy photons, which interact with the atom, thereby releasing part of its

energy in creating a Compton electron and the remaining energy of the photon being still available to create additional free carriers. Pair production occurs at very high energies of E > 1.02 MeV, wherein the incident photon creates an electron and a positron pair and the photon is completely annihilated. Figure 2.1 provides the probability of each of these events occurring as a function of energy of the projectile and the Z of the target material

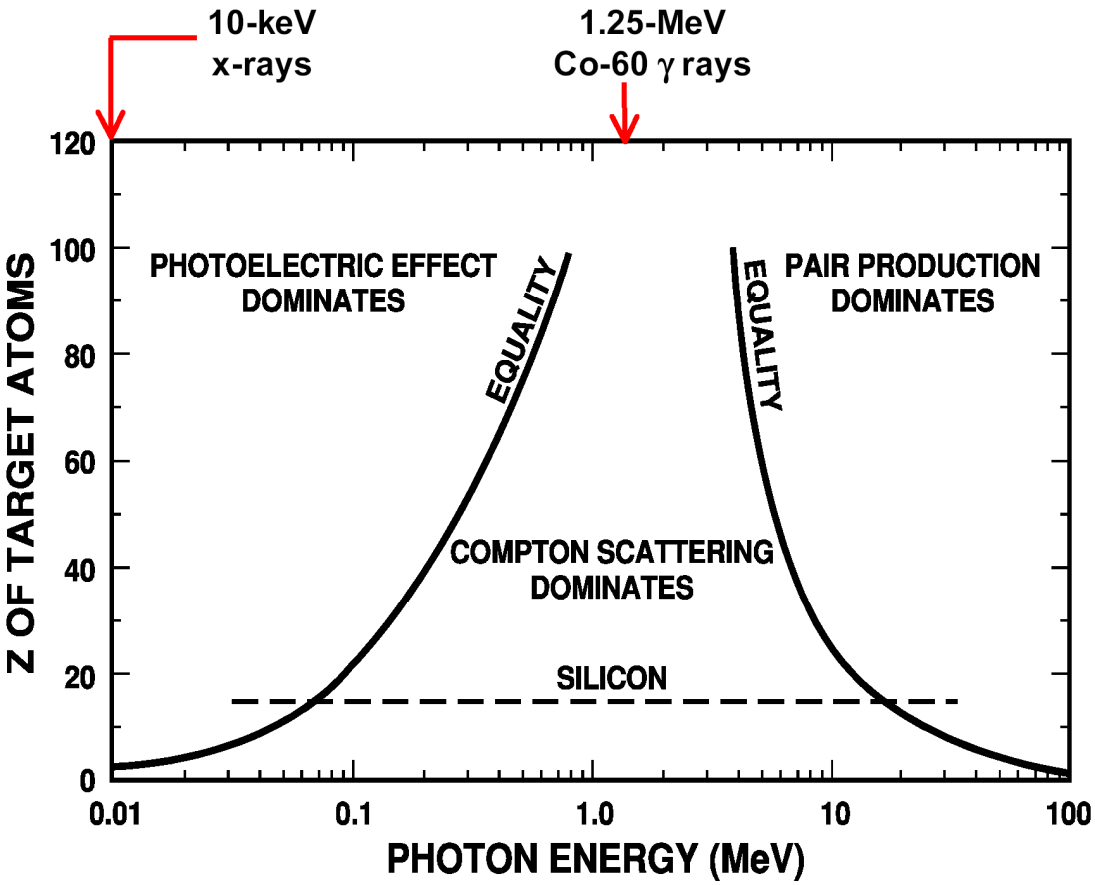

Figure 2.1. The probability of different mechanisms of photoelectric effect, Compton scattering and pair production occurring for different Z of the target material as a function of the incoming photon energy [1].

[3]. For the photon energy ranges considered in this thesis, photoelectric effect is the major contributing phenomenon for the creation of EHPs.

Electrons and holes generated in the gate and the isolation dielectrics can either recombine or be trapped at defects in the oxides. The percentage that escapes

recombination is a strong function of the electric field and is commonly referred to as charge yield [2, 4]. A significantly large field will be more efficient in the separation and hence the charge yield can be higher owing to a reduced recombination of radiation-induced charges [4, 5]. The phenomenon of charge trapping in the oxide with cumulative radiation dose is known as total ionizing dose (TID) effect, which further leads to altering the electrical performance of the device. This trapping is highly dependent on the processing conditions and the quality of the gate oxide. In this chapter we will emphasize on the nature and mechanisms of charge trapping in the gate oxides and use radiation as a tool to understand the oxide quality.

It is important to note that other effects such as single event effects (SEE) also form a substantial part of the radiation effects and reliability studies for devices used in modern day technologies. These are triggered by the dense plasma of EHPs generated from the incoming projectile that follow the path of the projectile. They are broadly classified into soft and hard errors. Soft errors such as single event upsets (SEU) are generated when a logic state of the circuit is changed. The hard errors lead to permanent damage due to a large amount of energy deposited in a small area of the dielectric, frequently referred to as single event gate rupture (SEGR) or from high current conditions arising from the passage of protons and other heavy ions leading to single event latch-ups (SEL). There are other forms of single event related device failures depending on the nature of the device, the details of which can be found elsewhere [6, 7]. We however restrict all of the future discussions to TID effects, the focus of this dissertation.

2.2 Total Ionizing Dose (TID) effects

Charging of oxides (gate, field and isolation) occurs by the mechanisms as described pictorially in the form of band diagrams in Figure 2.2 [8]. We consider a simple case where a positive voltage is applied on the gate metal and the applied field induces band bending in the MOS device as shown in the corresponding figure. A 10 keV

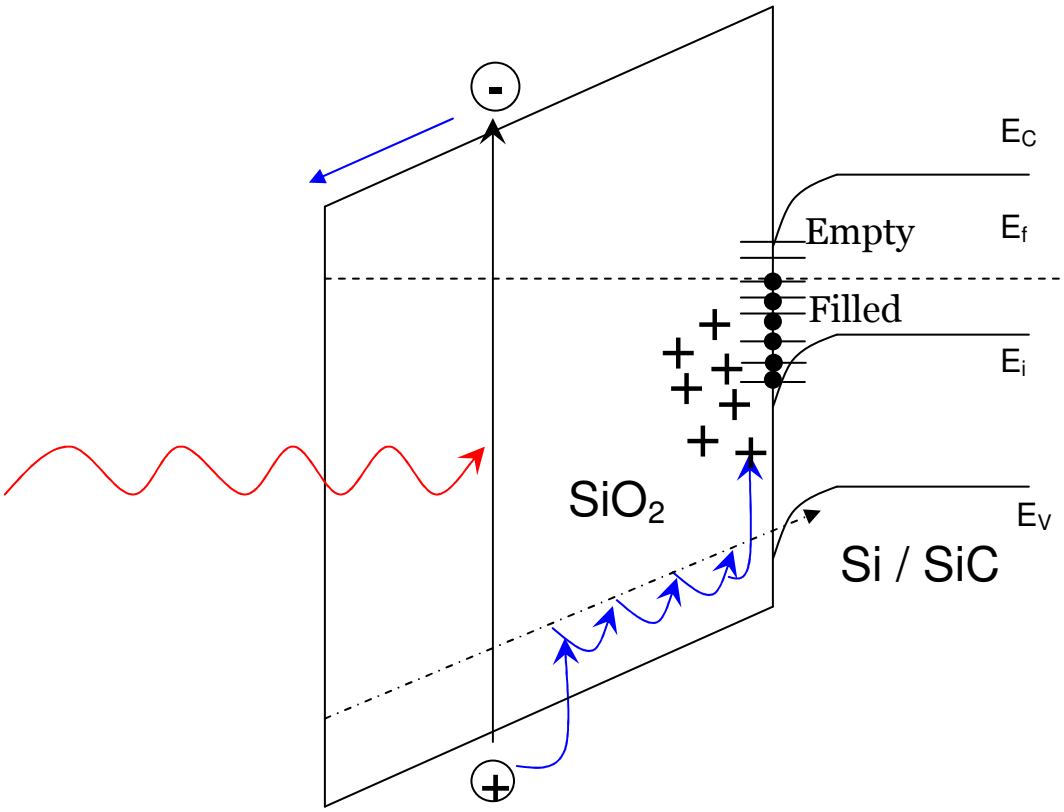

Figure 2.2. Schematic representing the fundamental radiation induced EHP generation with bulk hole trapping and movement of the charge centroid to the interface under bias [8].

photon (Aracor x-rays) traversing through this device configuration deposits its energy by generating photoelectrons via the photoelectric effect, which in turn create EHPs throughout the system. The photoelectron deposits its energy in the oxide by losing ~ 17

to 18 eV (in SiO_2) [9-11] for each EHP. A certain fraction of the EHPs undergo recombination, from the remaining charge most of the electrons in the oxide are swept away, depending on the applied field direction (built-in field, if none applied), in this case, towards the gate metal. This occurs in time scales of a few picoseconds assisted by the high mobility of electrons in the oxide. The slower drifting holes get trapped in the micro-structural defects and pre-existing traps in the oxide. These further transport slowly towards the oxide/Si interface through localized states in the oxide [5]. Electrons tunneling from Si very close to the interface or thermal emission from the trap sites can neutralize/decrease a certain fraction of these holes while others remain deep in the oxide as positive oxide trap charges [12-14]. These trapped charges can cause a shift in the threshold voltage and increase gate leakage in these devices. Another form of trapped charge commonly referred to as interface trapped charge arises from the charges trapped at the unsatisfied Si dangling bonds (without H passivation) at the oxide/Si interface. According to widely accepted models, these can increase with radiation due to the release of hydrogen in the bulk from hole hopping and its subsequent interaction with another hydrogen at the interface to form H_2 thereby leaving an unsatisfied dangling bond at the interface [15-21]. At threshold, these are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors, as will be discussed further in detail.

In general, these two types of charging in the bulk and at the near interface/interface region can modify the electrical performance of a MOSFET as shown in Figures 2.3a and 2.3b. Figure 2.3a shows an n-channel MOSFET (*p*-type Si substrate) under the influence of a positive gate bias (V_G^+), which causes a high enough electric field

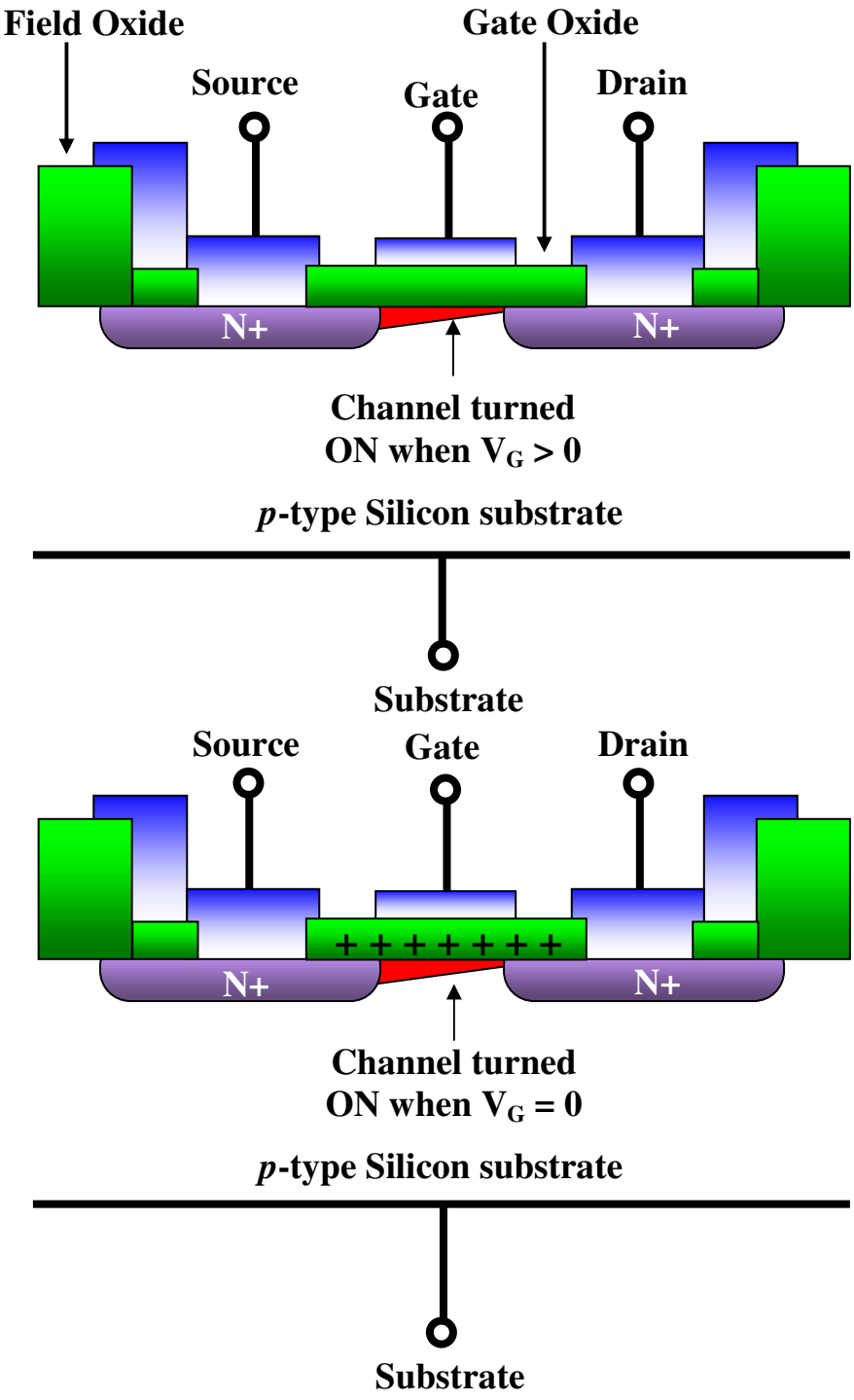

Figure 2.3a. Cross-section of a nMOSFET (p-type Si substrate) before irradiation with inversion conditions at positive gate voltage ($V_G > 0$). Figure 2.3b. showing the same structure after exposure to radiation results in inversion conditions even at zero gate bias ($V_G = 0$) due to trapped positive oxide charge [1].

to create an inversion channel when the gate voltage exceeds the threshold voltage (V_T). This along with a potential difference applied between the source and drain regions, results in a current flowing between the terminals. Hence the applied gate voltage controls the formation of the inversion channel in the MOSFET structure. Now consider Figure 2.3b where the radiation has introduced positive charges in the oxide as discussed before with the centroid of the charge very close to the oxide/Si interface. This generates additional space charge fields at the Si surface, which leads to offsets or shifts in the turn-on voltage of the MOSFET. For a significant positive trap charge, the device can be turned 'ON' even at zero gate bias as shown in the figure. This leads to an increase in the static power supply (OFF state) for the IC, which may lead to device failure. Charge trapping in the field oxides and SOI-buried oxides also cause similar problems with increases in the OFF-state leakage current.

2.3 Nature and mechanism for charge trapping

2.3.1 Oxide-Trapped Charge (N_{ot})

Zaininger [22] and Grove and Snow [23] put forth a simple model for the oxide trapped charge wherein they mentioned that EHPs are created by breaking Si-O bonds under irradiation. Some of them recombine, and the remaining electrons get swept towards the metal gate under a positive gate bias. The holes move by an anomalous stochastic hopping transport under the influence of a field towards the Si substrate. Some of them may be annealed (short-term or transient recovery) depending on field and temperature, while a significant portion of them may be trapped in long-term trapping sites close to the interface. The predominant contribution to the trapped oxide charge

comes from this positive charge trapping, as thermally grown oxides are known to have low concentrations of electron traps [24]. The fraction of hole trapping is also a function of the oxide-processing conditions [16]. A primary oxide defect in SiO_2, which induces hole trapping, is known as an E' center or an oxygen vacancy as verified by Electron Spin Resonance (ESR). It is identified as a trivalent silicon atom with an unpaired electron in a dangling orbital, back-bonded to three other oxygen atoms [25, 26]. The oxygen vacancy can be formed by damage caused during dopant implantation or during various post-oxidation annealing treatments, which may cause out-diffusion of oxygen at higher temperatures thereby generating more E' centers [27]. Different configurations of the E' centers were discussed by Warren *et al.* [28]. The most widely accepted precursor is the E'_γ center, which has been deemed responsible for the oxide-trapped charge (N_{ot}) in SiO_2 [25, 29, 30]. The creation of this E' center by radiation-induced trapping can be expressed in the simplest chemical form as shown below

$$\equiv Si - Si \equiv +h \xrightarrow{irradiation} \equiv Si \quad \bullet Si \equiv \qquad (2.1)$$

The precursor bridging-oxygen vacancy on the left of the equation provides a weak strained bond configuration for the two silicon atoms. This system, after trapping a hole under irradiation, becomes an Electron Paramagnetic Resonance (EPR) active state by giving rise to $^{+}Si \equiv O3$ and another Si with a dot denoting the dangling orbital. Pictorial representation of the precursor and the EPR active state is as shown in Figure 2.4. It is evident that the positively charged silicon after hole trapping relaxes into a planar configuration while the neutral Si relaxes towards the vacancy. The radiation-induced

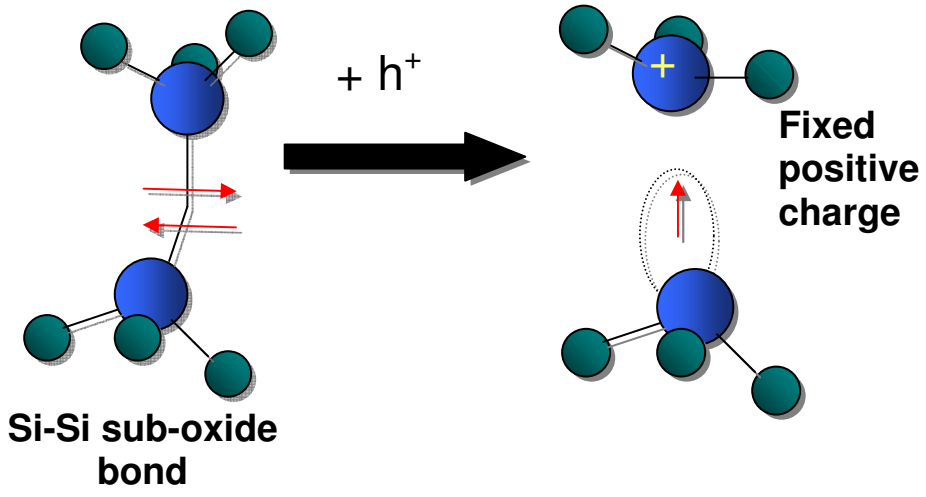

Figure 2.4. Mechanism showing the formation of the E' center from a Si-Si sub-oxide bond (O_2 vacancy) [8].

oxide trapped charge in the case of SiO_2 based devices is predominantly positive. For a typical C-V measurement on a MOS device on Si following irradiation, when the Fermi level is at mid-gap the acceptor and donor like traps are charged neutral hence the voltage shifts on the C-V curve at mid-gap (ΔV_{mg}) is entirely due to these oxide charges trapped in the bulk/near interfacial region of the oxide. Hence at mid-gap, the voltage shift due to total oxide trap charge (ΔV_{ot}) increase is given by the Winokur and McWhorter technique [31, 32] where

$$\Delta V_{ot} = \Delta V_{mg} \tag{2.2}$$

The total increase in the number of oxide traps (ΔN_{ot}) at mid-gap is given by

$$\Delta N_{ot} = -C_{ox}\frac{\Delta V_{mg}}{qA} \tag{2.3}$$

The change in interface trap charges over time following irradiation is discussed in the forthcoming section. It was further verified from gamma ray irradiation/annealing

experiments that the trapping (irradiation)/recovery (annealing) of mid-gap voltage shift (ΔV_{mg}) correlated to the increase/decrease in the E'_{γ} signal thereby supporting the model for the cause of bulk oxide charge trapping [26].

In the case of SiO_2/SiC based samples, the bulk of the oxide was believed to be similar to stoichiometric SiO_2 as employed in Si based devices. Hence the radiation induced bulk defects were presumed to be similar, as will be shown in Chapter IV. However the interface is completely different from the Si-based interface, with the presence of extensive defects often assumed to be of excess carbon. This could lead to a difference in the charge trapping characteristics in the non-nitrided SiO_2/SiC samples itself. Additionally the presence of a larger band gap opens the possibility of exposing additional states in the gap that were not a matter of concern in Si. Previous radiation experiments have addressed some of these issues mostly in 3C [33] and 6H [34], with some literature in 4H-SiC [35-38]. In the work included in this thesis, we report the first observation of enhanced positive charge trapping under radiation for nitrided 4H-SiC MOS capacitors under the influence of an applied field. The nitridation of these samples can add to the complexity as the presence of nitrogen at the interface and near-interface region can improve/degrade the trapping observed in the non-nitrided case. Another factor is the high temperature processing (~ 1150 °C) and growth of these oxides as compared to the traditional SiO_2/Si processing temperatures of 900 °C to 1000 °C may increase the concentration of E'_{γ} centers. Chapter IV essentially addresses the aforementioned concerns in these devices, which are potential candidates for high-temperature and high-power electronics.

For the second category of samples of HfO_2/Si, the issue of understanding the charge trapping using radiation, and its comparison to SiO_2 based devices, is even more challenging. This is mainly due the bulk and the interface of the oxide; both are completely different from SiO_2/Si. One of the main issues being that the oxide is not thermally grown for the alternative gate dielectrics and their susceptibility to polycrystallization during post metallization treatments can cause additional trapping. The other being the oxygen deficiency in the SiO_2 interlayer (IL) that results from oxygen uptake during the high-κ growth and processing [39]. These can influence further charge trapping. The knowledge and understanding of defects in SiO_2/Si based devices have been established over the years with a plethora of experiments conducted to investigate their nature. However for HfO_2 although a lot of previous research (mostly on capacitors) has been undertaken to understand charge-trapping behavior under radiation in HfO_2/Si based devices [40-44], a similar proficiency in the understanding is still lacking for these alternative gate dielectrics, especially for the response of MOSFETs. To address this issue Chapters VI and VII deal with the radiation response of these HfO_2-based MOSFETs. These are studied in the ultrathin EOT range of less than 2.5 nm thickness corresponding to the regimes of importance in the CMOS industry.

2.3.2 Interface-Trapped Charge (ΔN_{it})

Interface charge trapping was described initially by a two-stage model by McLean [18]. He proposed that during the first stage, the radiation generated holes free hydrogen ions in the SiO_2 bulk as they move to the SiO_2/Si interface. In the second stage these undergo a dispersive hopping transport to the interface, react with hydrogen at the

interface, releasing H_2 thereby creating an interfacial Si dangling bond [18]. A graphical representation of the mechanism is as shown in Figure 2.5.

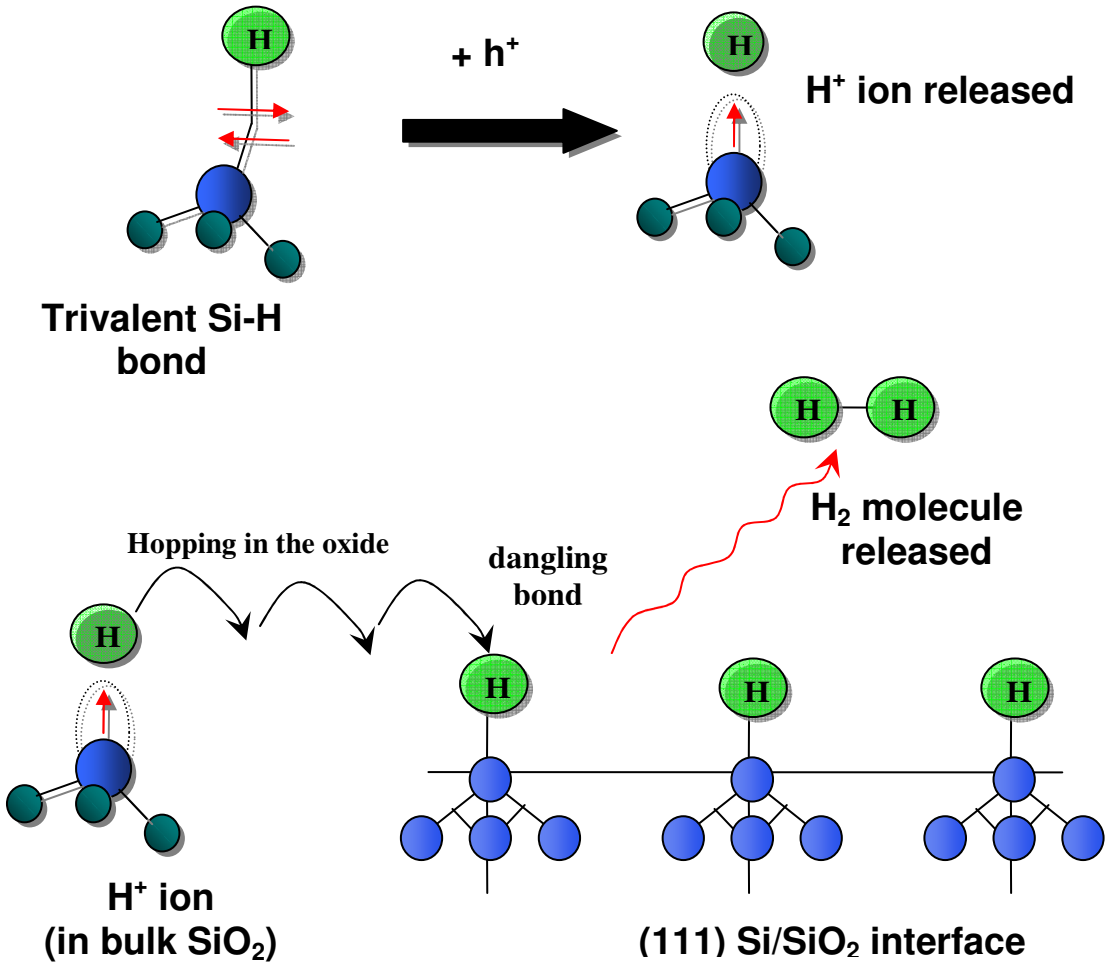

Figure 2.5. Mechanism showing the formation of the P_b center defect structures at the Si/SiO_2 interface as described in the literature using the hydrogen model [8].

This model was consistent with the results of several others [15, 17, 19, 20, 45-47]; a modification was put forth by Griscom [48] wherein he argued that chemical reaction is possible even with a neutral hydrogen where an electron is provided from the substrate to support the model proposed by McLean. This interfacial dangling bond was the prime reason for the generation of states in the middle of the Si band gap at the

SiO_2/Si interface. The chemical reactions that are usually deemed responsible for the hydrogen induced interface trap creation are represented as

$$H^+ + H - Si \equiv Si \longrightarrow H_2 + Si^+ \equiv Si \tag{2.4}$$

Alternatively, atomic hydrogen reacts as

$$H^+ + e^- \rightarrow H^0 \text{ and} \tag{2.5}$$

$$Si \equiv Si - H + H^0 \rightarrow \quad Si^- \equiv Si + H_2 \tag{2.6}$$

Here Si^- is a dangling bond. In the case of the proton as shown in equation 2.4 the electron is supplied by the Si substrate for the formation of H_2 [49]. The time, temperature and field dependence of the interface trap-generation was studied using different electrical techniques; however ESR was one of the most important physical techniques used for determining the structure of these individual defects.

The ESR techniques revealed defects identified as P_b centers, which were responsible for the interface trap generation. Initially, two different P_b centers were observed on Si (100), P_{b0} and P_{b1} namely, which were found to be process-induced interface traps as schematically represented in Figures 2.6a and 2.6b for the (100) and (111) Si faces [25, 26, 29, 30, 50]. Figure 2.6a for the Si (111) face shows that the physical structure of the P_{b0} center is a Si back bonded to three other Si atoms in the substrate with the fourth dangling orbital normal to the interface extending into the oxide. For the (100) face as shown in Figure 2.6b, the structure for P_{b0} is similar, except that the dangling bond extending into the oxide is at an oblique angle instead of being normal [51, 52]. For the P_{b1} defect, a few researchers have speculated its physical structure with a Si

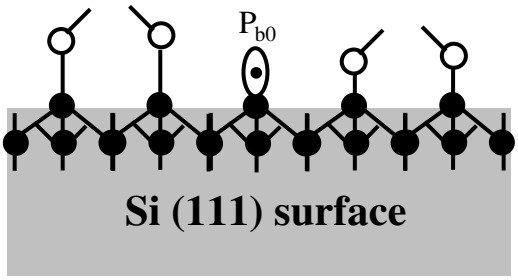

Figure 2.6a. Schematic representing the structure of a P_{b0} defect center shown here as a Si dangling bond extending in a normal direction into the oxide and attached to three other Si atoms in the substrate at the SiO_2/Si (111) interface [52].

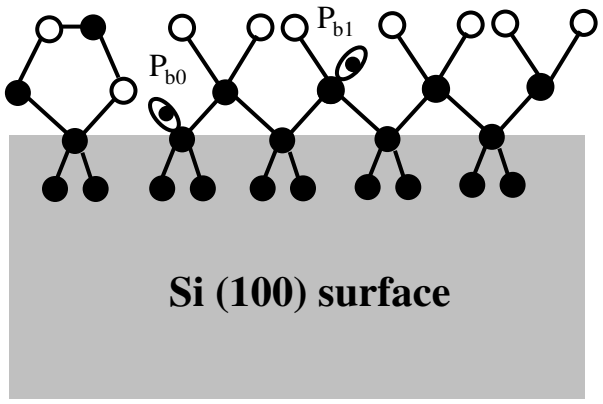

Figure 2.6b. Schematic representing the structure of a P_{b0} defect center shown here as a Si dangling bond at an oblique angle attached to three other Si atoms and a P_{b1} defect represented as a Si dangling bond attached to two other Si atoms and an oxygen atom at the SiO_2/Si (100) interface [52].

back-bonded to two other silicon and an oxygen atom with a dangling bond into the oxide [51, 52] but a better understanding of these defects are being pursued [53]. Additional radiation experiments revealed no observed increase in the P_{b1} ESR signal following

radiation doses on the SiO_2 based samples. It was further suggested by Stesmans [54] that these were electrically inactive defects. Further investigations revealed that the P_{b1} signal increased with significantly higher doses as compared to doses for P_{b0} [55]. The P_{b0} signal increased linearly with increasing doses as observed by Lenahan *et al.* on Si (100) surfaces [56]. Lenahan also observed a correlation between ΔD_{it} and the P_{b0} during irradiation as well as isochronal annealing measurements [50]. The increase in the P_{b0} signal (interface traps) can be explained with the widely accepted hydrogen model as mentioned previously which leads to a time dependent increase in the ΔN_{it} following irradiation.

Interface traps can be charged or discharged depending on the location of the Fermi level in the band gap, which can be modified by the bias applied to the semiconductor (band-bending). Interface traps in the upper portion of the band gap are considered to be acceptor type and are negatively charged when filled and neutral when empty. Similarly, the interface traps in the bottom portion of the band gap are donor type and are neutral when filled and positively charged when empty. Thus for silicon, the interface traps are charge neutral for a device biased at mid-gap [57, 58]. However the change in the number of interface traps (ΔN_{it}) between mid-gap and flatband can be represented using the charge separation technique as [31, 32]

$$\Delta N_{it} = C_{ox}\frac{(\Delta V_{fb} - \Delta V_{mg})}{qA} \tag{2.7}$$

where ΔV_{fb} and ΔV_{mg} refer to the change in the flatband voltage and mid-gap voltages respectively, C_{ox} is the absolute capacitance in F and A is the area of the gate metal contact.

The interface traps cause negative threshold voltage shifts for p-channel transistors and positive threshold voltage shifts for n-channel transistors. Mobility degradation is also observed owing to coulomb scattering from the trapped charges flowing in the inversion layer [20, 59]. These further affect the timing parameters of an IC and decrease the drive of the transistors.

Regarding this thesis, the interface issues are completely different for the case of SiO_2/SiC and somewhat similar for HfO_2/Si, both relative to SiO_2/Si. For SiO_2/SiC, it is important to note that not only can the interface have defects but also the presence of carbon can give rise to a variety of defects at the interface [60-63], which will be discussed in detail in Chapter IV. In SiC, the time constants for the interface charges to respond to the gate bias sweep below E_c-E = 0.6 eV to mid-gap are extremely large [64]. Hence the response to detrapping when the Fermi level bends deeper in the band gap is very minimal, and these charges tend to appear as fixed charges as will be discussed in detail in Chapter IV. Chapter IV also explains the role of nitrogen at the interface/near-interface and its effect on charge trapping from radiation [65]. However these results call for the need to undertake comprehensive spectroscopic studies to understand the defect nature in these wide-band gap semiconductor structures. In the second system of HfO_2-based structures the interfacial region is more SiO_2-like due to an intentional thermal SiO_2 layer grown to reduce the interface trap density (D_{it}), thereby improving the mobility. However, the D_{it} still appears to be in the range of 10^{12} eV^{-1} cm^{-2}, which leads to almost negligible interface trap charge increase due to the already pre-existing higher density of defects. Additionally the ultrathin dielectric layers considered in these MOSFETs and the reduced band offsets, contribute to the observed volatility of the

radiation induced trapped charge owing to neutralization/annihilation of a significant number of these near interface/interface charges [66]. A detailed quantitative analysis is provided in Chapter VI of this dissertation.

2.3.3 Border traps

The term "border traps" was first introduced by D. M. Fleetwood in 1992 [67] and a more comprehensive explanation was given in the 1993 paper [68]. They are simply explained as near interfacial oxide traps that are able to exchange charge with the underlying silicon on the time scale of the measurements. The location of these traps is very close to the interface and their response to the electrical sweep make them look like interface traps. It was concluded that the trapping/detrapping of these border traps was a strong function of the measurement delay during the C-V and I-V sweeps. Measurements of *1/f* noise suggested that the noise signal was almost entirely from near interfacial traps and that ambiguities had to be resolved to distinguish these from actual interface traps [69-71]. Hence the coining of this term for near-interfacial oxide traps provided a much-needed update to the terminology for the oxide traps developed by the Deal committee [72]. There is still some uncertainty on the exact structure of these border traps and it is possible that the relevant defect structure may vary for different materials and processing. In this work we discuss about these kinds of traps to explain the transient charging/discharging in the alternative high-κ devices under bias stress, which exist more importantly owing to the oxygen deficient, SiO_2 interlayer in these devices. A schematic representation of the location of these traps is as shown below in Figure 2.7 [68].

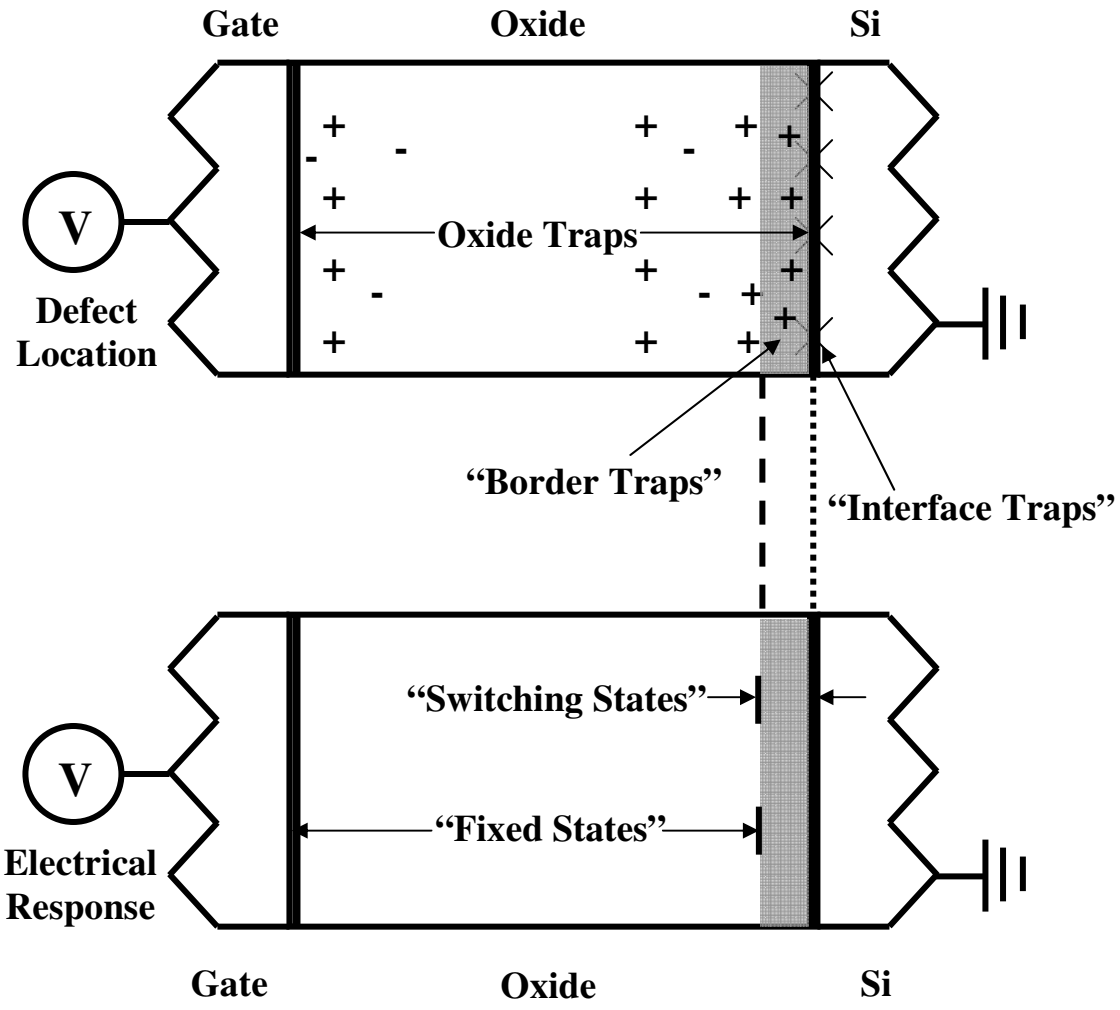

Figure 2.7. Image highlighting a pictorial representation of the traditional oxide and interface traps and traps closer to the interface (border traps), which can respond to the gate bias under the time scale of the measurements [68].

2.4 Annealing/Recovery studies

Different kinds of annealing studies have been employed to understand the activation energies for the recovery behavior in the gate oxides after a particular total dose. Isothermal annealing is studied at constant temperatures for varying times and

isochronal annealing is studied at constant time intervals for varying temperatures. Zaininger found that most of the recovery in SiO_2/Si based devices took place between 150 °C and 300 °C [73]. The basic process of annealing proceeds by two mechanisms, tunneling and thermal excitation. The tunneling probability, which is a strong function of the distance, is the dominant mechanism at room temperatures, but thermal emission plays an important role at higher temperatures [14]. This fact has been verified by various Thermally Stimulated Current (TSC) experiments by Fleetwood *et al.* and others [14, 68, 74-79]. We have performed isochronal annealing studies on our samples of SiO_2/SiC after nitridation to determine the activation energy using a model described in Chapter IV. In the case of HfO_2/Si based devices most of the trapped charge was annealed at room temperatures by reversing the bias on the electrodes, which agrees with tunneling being the dominant annealing mechanism owing to reduced band offsets.

This dissertation includes most of the terminologies and mechanisms discussed in this chapter for charge trapping and annealing. We find correlations between the existing literature on SiO_2/Si system and the two advanced systems studied (SiO_2/SiC and HfO_2/Si). Interesting similarities and differences are discussed in the subsequent chapters.

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CHAPTER III

NITROGEN PROFILING & MOS CHARACTERIZATION FOR SiO_2/4H-SiC DEVICE STRUCTURES

3.1. Overview

Materials characterization (physical and electrical) of the SiO_2/SiC materials with and without NO passivation has been performed by numerous techniques. Medium Energy Ion Scattering (MEIS) [1], Nuclear Reaction Analysis (NRA) [2, 3], Secondary Ion Mass Spectroscopy (SIMS) [4], and Electron Energy Loss Spectroscopy (EELS) [2, 5], have been used previously to profile the nitrogen content in these material systems. Room temperature C-V, high temperature C-V and photo-CV are some of the techniques that have been used for electrical characterization of as-oxidized and NO annealed SiO_2/SiC MOS structures [6-10]. In this chapter we summarize the previous work done on physical characterization that support our results on the radiation effects. We have performed two of the three electrical characterizations as mentioned above namely Hi-Lo Capacitance-Voltage (C-V) [11] and photo-CV [6] measurements. The objective of the first part of the thesis which requires the understanding of radiation induced charge trapping response of N in a SiO_2/SiC configuration is very much dependent on the location and the content of nitrogen in the SiO_2/SiC structure. This chapter includes profiling results and electrical response, followed by discussion of the results for each of the technique used to understand the role of nitrogen from the perspective of materials analysis and device characterization.

3.2. Physical characterization of as-oxidized and NO annealed SiO_2/SiC

One of the main objectives of this thesis is to understand the response to radiation induced charge trapping for SiO_2/SiC based devices after subjecting them to NO induced interface passivation. Typically SiC oxidation is performed at 1150 °C followed by a NO anneal at 1175 °C. Not only is it important to know the role nitrogen plays at the interface, but it is of value to quantify the nitrogen profile and content in the MOS system. Several groups have been actively involved in the studies of nitrogen passivation at the SiO_2/SiC interface with some of initial work described in Ref. [12, 13]. Nitrogen profiling included in this chapter is mostly based on previous work done within the research group and reported by McDonald *et al.* [3, 4, 14] and Dhar e*t al.* [1, 2, 15]. These profiling methods assume significance to this thesis since the samples prepared for this dissertation work were exposed to the same oxidation and NO post oxidation annealing (POA) treatments (similar instrumentation and growth recipe) as the ones used in these previous studies. Studies carried out in our group have verified the nitrogen content using primarily four different physical characterization techniques. These are NRA, EELS, SIMS, and MEIS and the corresponding concentrations for the nitrogen at the SiO_2/SiC interface were mentioned within the sensitivity limits of these experimental techniques.

3.2.1. Nuclear Reaction Analysis (NRA)

A detailed investigation using nuclear reaction analysis (NRA) for nitrogen quantification is elaborately described by McDonald *et al.* [3]. It involved measuring the nitrogen content using nuclear reaction analysis (NRA) using the $^{15}N(p,\alpha)\,^{12}C$ reaction at

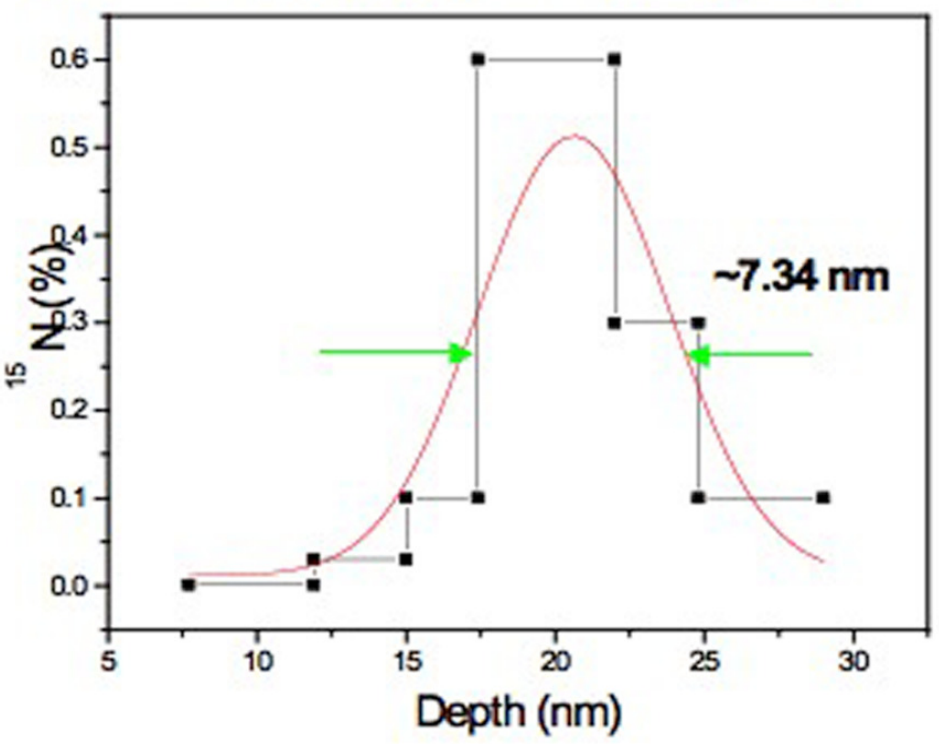

Figure 3.1. Concentration profiles of ^{15}N in SiO_2/SiC annealed in 10 mbar of $^{15}N^{18}O$ at 1000 °C for 4 h. The origin corresponds to the surface; the SiO_2/SiC interface is at ~ 30 nm [2, 3].

E_p = 1 MeV and alpha particle detection at 180°. Si-face samples were prepared using wet oxidation procedure at 1150 °C for 30 min with $^{15}N^{18}O$ post oxidation annealing at 1000 °C for 4h at 10-mbar pressures. Figure 3.1 shows the profile of the nitrogen detected as a function of depth into the oxide, with the thickness of the oxide being ~ 30 nm. The areal density of ^{15}N for this sample was measured to be ~ 2 x 10^{14} cm^{-2} for the

4h anneal sample. Similar studies performed by Dhar *et al.* [2] further explains the nitridation anisotropy as a function of the different crystal faces of SiC detected using NRA and SIMS analysis. In these studies, the content of ^{15}N measured by NRA on the Si-face was about (1.62 ± 0.1) x 10^{14} cm^{-2} and higher density was achieved for the C-face of about (4.8 ± 0.2) x 10^{14} cm^{-2}. Only 10 % difference was found between the densities for the a-face and the C-face. It was concluded that the concentration of nitrogen follows the trend for oxidation rates for the crystal faces. Improved depth resolution was obtained electron energy loss spectroscopy (EELS) as will be discussed in the next section.

3.2.2 Electron Energy Loss Spectroscopy (EELS)

The N elemental profiles as performed by Chang *et al.* [5] and Dhar *et al.* [2] are as shown in Figure 3.2 obtained on the Si- and the C-face annealed for 2h in NO after the dry oxide growth. Samples similar to the NRA samples were fabricated for the EELS experiments with the only difference being that these samples were annealed under flowing ^{14}NO gas at 1 atm unlike the NRA samples, which were annealed at 100 Torr. This showed up as a factor of 2 in the nitrogen concentration between the two techniques. Spatially, a higher N concentration (3.5 x 10^{14} cm^{-2} for Si-face) was measured close to the interface followed by a constant level of the N profile. Both the EELS and NRA were in agreement within experimental error limits thereby confirming the presence and spatial location of nitrogen at the SiO_2/SiC interface.

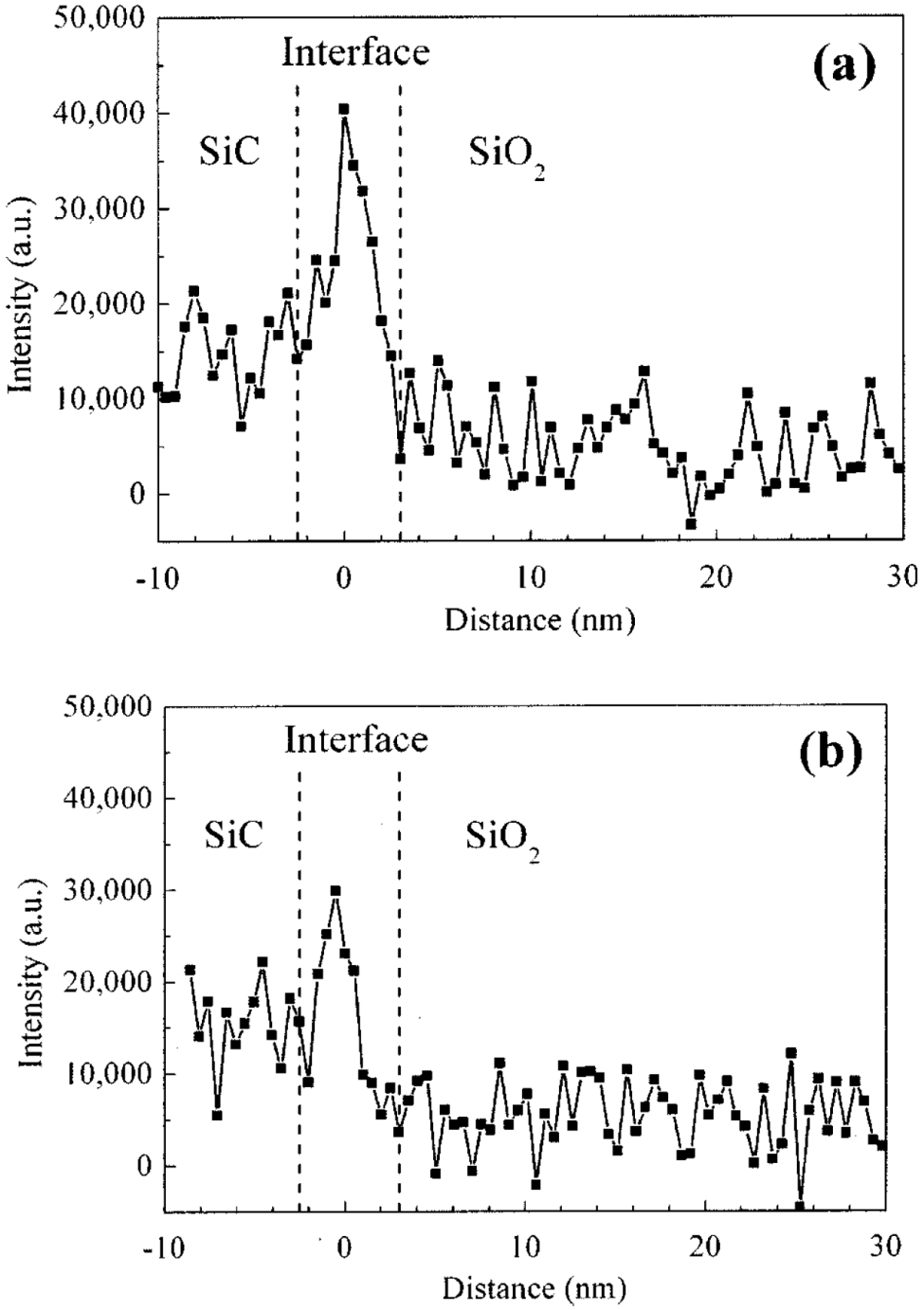

Figure 3.2. The nitrogen intensity profile as obtained by EELS at the SiO_2/4H-SiC interface of a NO-annealed C-face (a) and Si-face(b) sample showing that N is detected only at the interface [2, 5]. Artifacts resulting from inadequate background subtraction of the EELS spectrum yield positive values of N intensity for positions outside the interface region.

3.2.3 Secondary Ion Mass Spectroscopy

Si-face *p*-type 4H-SiC samples were exposed to dry oxidation at 1150 °C for 30 min followed by NO anneal at 1150 °C for 4h at pressures of 100 Torr (with ^{15}NO) and 1

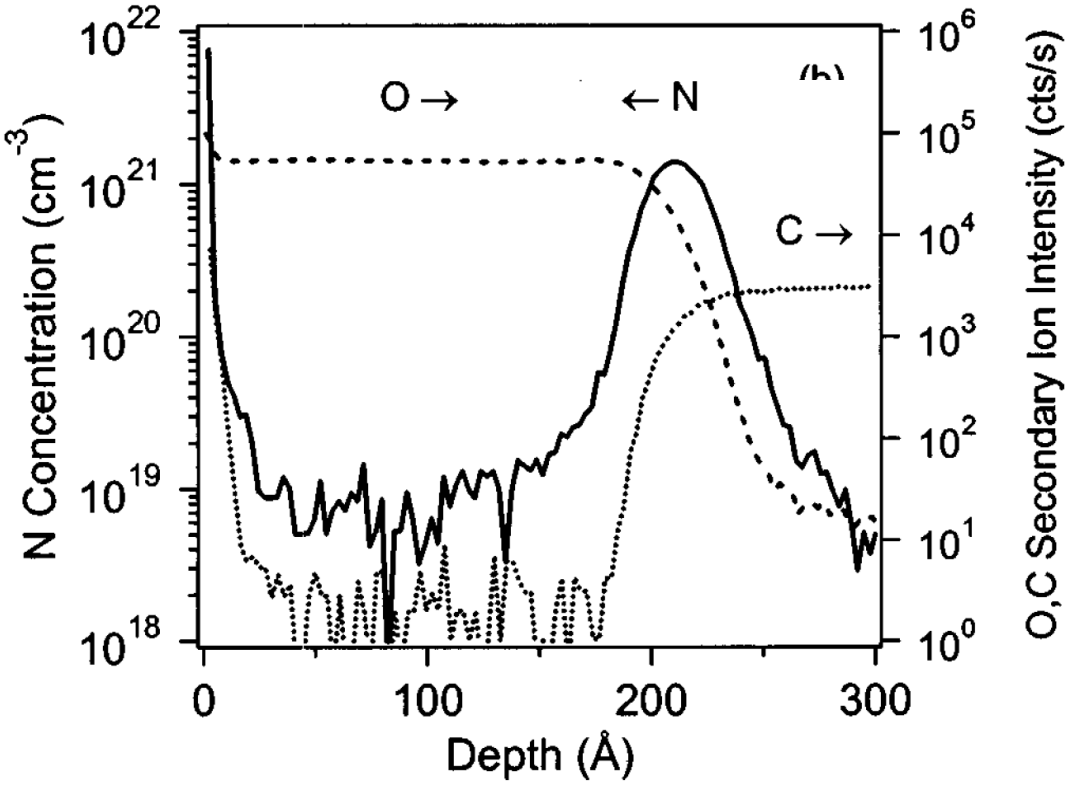

Figure 3.3. SIMS profiles of SiO_2/4H–SiC annealed in NO at 1150 °C at 1 atm for a period of 4h. The N areal density is 4.8 x 10^{14} cm^{-2} with an oxide depth of 20.3 nm [4].

atm (with flowing ^{14}NO) according to the studies performed by McDonald *et al.* [4]. Figure 3.3 shows SIMS profile of the sample annealed at 1 atm with an oxide thickness of ~ 20 nm. It is evident from the figure that nitrogen accumulates at the SiO_2/SiC interface in these samples. The N areal density was measured to be ~ 4.8 x 10^{14} cm^{-2} at an oxide depth of 20.3 nm as shown in the figure. These were studied as a function of oxide thickness and it was found that the N peak moves with the interface as the oxide grows

into the SiC for higher thicknesses thereby elucidating the influence of N at passivating the interface.

3.2.4. Medium Energy Ion Scattering (MEIS)

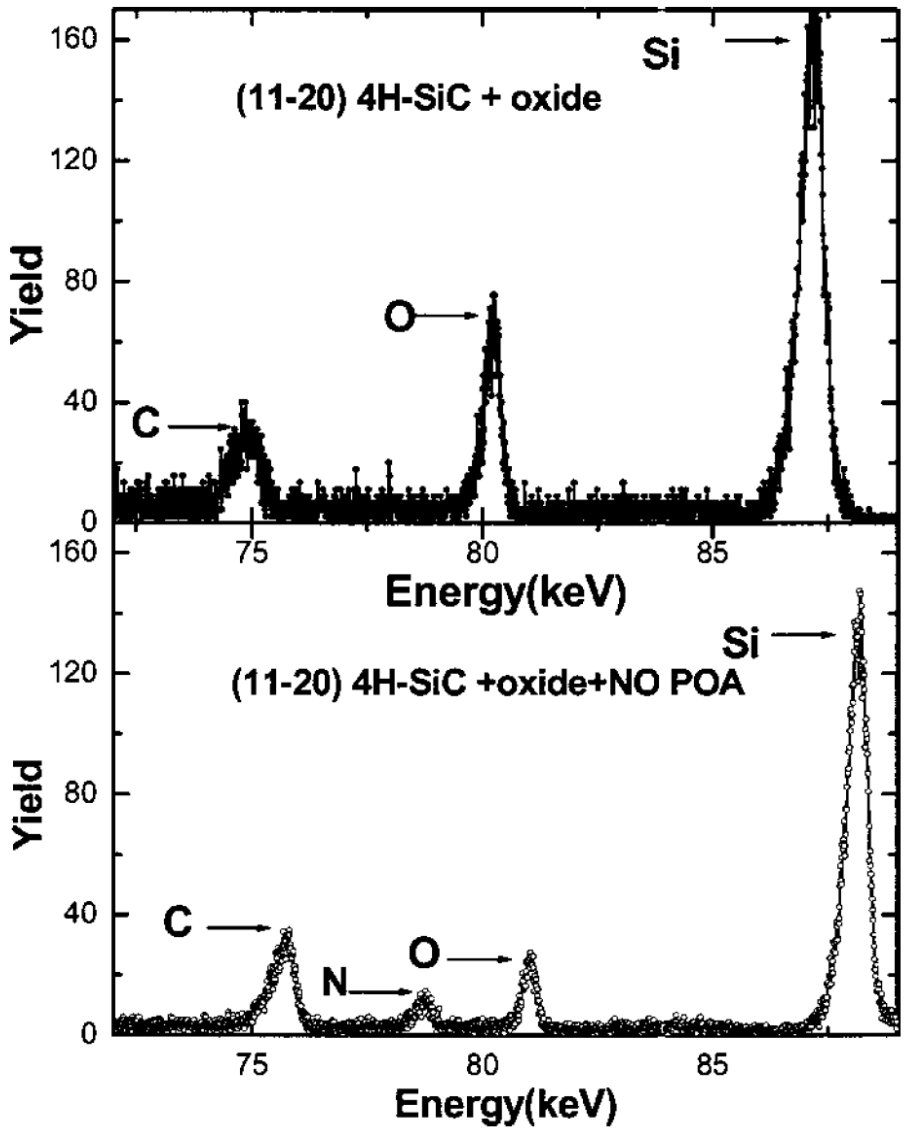

Figure 3.4. MEIS spectra of ($11\bar{2}0$) 4H–SiC; Sample as-oxidized at 1150 °C (top) compared to a sample that underwent a NO POA at 1175 °C for 2 h after the oxidation (bottom). Nitrogen incorporation at or near the interface can be observed from the spectra. The difference in amount of oxygen in the two samples is due to different thickness resulting from etching of the oxide [1].

4H-SiC of the $(11\bar{2}0)$ polytype (a-face) was used to fabricate samples for MEIS analysis [1]. The samples after a standard clean, were subjected to routine oxidation for 4h at 1150 °C in dry oxygen followed by NO POA process at 1175 °C in flowing Ar for 2 h. A standard sample was made by annealing in Ar at the oxidation temperature for 30 min after oxidation. 100 keV H^+ ions were used at a normal incidence and 125° scattering geometry for the analysis. For improved interface resolution the oxide layer was carefully etched using HF to thin down the oxide. Figure 3.4 shows the MEIS spectra for both the as-oxidized and the nitrided 4H-SiC a-face samples. Nitrogen incorporation at or near the interface was confirmed as seen from the figure. The areal density calculated from the area under the peak revealed an estimate of 6.6 x 10^{14} at/cm^2 for the data on the a-face. Similar measurements were done on the Si-face and the areal density was found to be a little higher with nitrogen content of 1.16 x 10^{15} at/cm^2 at the interface. This layer of nitrogen was found to be very close to the interface (within 1 nm) as measured from the full width half maximum of the MEIS spectrum, within the depth resolution limits of the system [1, 10].

All the aforementioned four techniques confirm the presence of N with areal densities and distribution values close to each other. These results assure a similar profile and concentration values for the samples studied in the radiation response studies. The pre-irradiation electrical characterization results of our NO annealed capacitor structures serve as evidence to the fact that nitrogen was involved in reducing the D_{it} in the nitrided samples as compared to the as-oxidized ones. This crucial evidence of D_{it} reduction, thereby proving the 'N' presence before irradiation, is an important factor as the radiation

response is strikingly different for the NO annealed samples as compared to the as-oxidized ones.

3.3 Electrical characterization of as-oxidized and NO annealed SiO_2/SiC

The pre-irradiation electrical behavior of the capacitors was analyzed using Hi-Lo Capacitance-Voltage (C-V) [11] and photo-C-V measurements [6]. The photo C-V technique was employed to measure the buildup of slower interface traps. Pre-irradiation characterization was done for comparison of hysteresis and prominent features of the C-V curves with the post-irradiation curve. These features on the C-V curves are indicative of slow interface traps and near interface (border) traps [6, 16]. The effect of NO passivation on the reduction in the interface trap density (D_{it}) was verified using the C-V technique [11, 17] as shown in Figure 3.6.

3.3.1 Room temperature Hi-Lo C-V technique

MOS capacitors for the electrical measurements were prepared on 4H-SiC Si-face substrates. Commercially available 4H-SiC (*n*-type, (0001) Si-face) substrates with nitrogen doping of 5 x 10^{15} cm^{-3}, were used. A 10 μm thick epitaxial layer was grown on these n^+ substrates. Before the oxidation step, samples were cleaned using an industry standard RCA cleaning procedure. Approximately 34 nm thick oxides were grown by performing dry oxidation at 1150 °C for 4 h. The samples were annealed in flowing Ar for 30 min at the same temperature after oxidation. Some of the samples were subsequently nitrided at 1175 °C in flowing NO for 2h. The gas was changed back to Ar and the temperature ramped down to 900 °C before removing the samples from the

furnace. Two layers of gate metal, namely 100 nm of Mo followed by 100 nm of Au, were deposited by DC sputtering. Circular MOS capacitor contacts with diameters of 350 μm and 700 μm were patterned and defined using standard photolithography and lift-off techniques [18]. The capacitors were characterized using simultaneous hi-lo capacitance

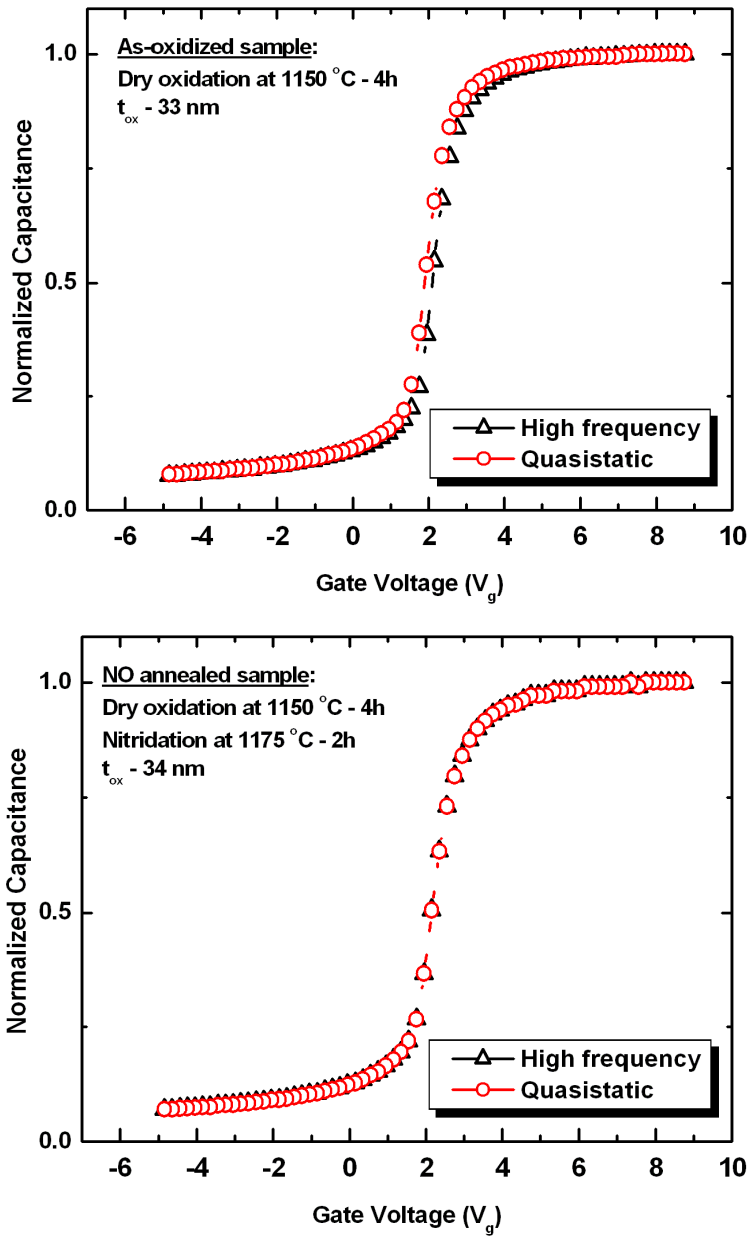

Figure 3.5. 100 kHz C-V curves showing the high frequency (black curve) and the quasistatic (red curve) plotted for an as-oxidized (3.5a) and NO annealed sample (3.5b).

voltage (C-V) measurements to measure the effective oxide charge and interface trap density (D_{it} calculated by comparing the high frequency-100 kHz and quasi-static measurements) before irradiation. Figures 3.5a and b show the pre-irradiation high frequency (C_H) and quasi-static (C_Q) C-V curves plotted [18] for both the nitrided and the non-nitrided Si-face 4H-SiC samples. The slight shift between the C_H and C_Q for a given gate voltage for the as-oxidized samples is an indication of a high density of interface defects (D_{it}) in these samples. For Figure 3.5b, the both the capacitance curves follow simultaneously for the gate bias sweep with no offset thereby indicating a reduction in the D_{it}. Nitridation on different crystalline faces of 4H-SiC has been effective in the reduction in the net negative charge at the interface owing to the NO anneal. Prior studies have discussed the evidence of carbon clusters, oxycarbides, suboxides and Si and C dangling bonds at the interface [19, 20]. It has been proposed that N passivates these traps at the interface thereby decreasing the net negative charge at the SiO_2/SiC interface [4, 9, 14]. It is also important to note that these C-V curves do not invert as shown in the figures, with the evidence of a slope that continues with increasing d.c bias. The condition is referred as deep depletion and it occurs since the thermal generation rate of SiC at room temperature is too low for the inversion layer to form in a reasonable period of time [6, 17]. This might lead to misleading calculations of interface traps for the device and this problem is normally tackled by using techniques such as photo-CV, which will be discussed later in the chapter.

Figure 3.6 shows a plot of interface trap density D_{it} ($eV^{-1}cm^{-2}$) extracted as a function of energy from the conduction band edge (E_c-E) in eV. It shows that the D_{it} before nitridation was measured to be on the order of 3 x 10^{12} eV^{-1} cm^{-2} and following

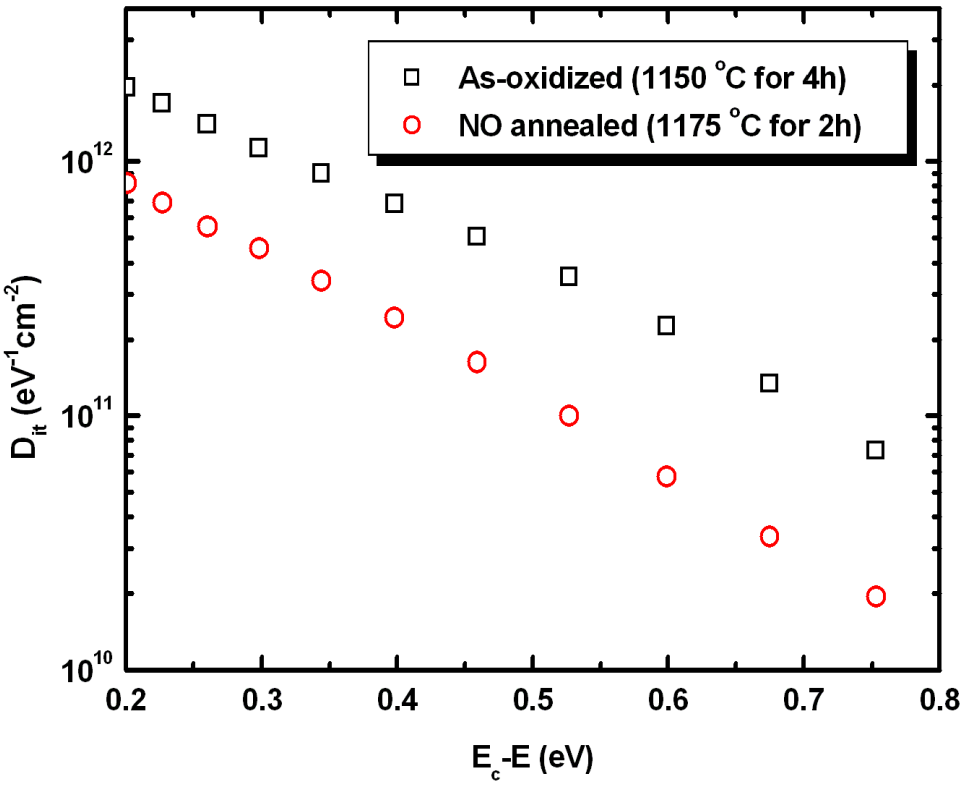

Figure 3.6. Comparison of the D_{it} in $eV^{-1}cm^{-2}$ between the as-oxidized and the NO annealed sample plotted as a function of distance from the conduction band edge (E_c-E) in eV.

nitridation is reduced by almost an order of magnitude to 7 x 10^{11} eV^{-1} cm^{-2} at E_c-E = 0.2 eV. Figure 3.7 shows that this D_{it} reduction is more pronounced near the band edges as compared to the states deeper in the band gap. This D_{it} reduction is also true for the a-face samples as observed by Dhar *et al.* following NO annealing on oxides grown on $(11\bar{2}0)$ face of 4H-SiC [1]. The authors also mention about the presence of nitridation anisotropy that exists depending on the crystal face of 4H-SiC under observation. A crystal face dependent variation before nitridation in the absolute number of defects at the SiO_2/SiC interface leads to a corresponding difference in the degree of N passivation for the different faces of 4H-SiC [2]. Furthermore, it was observed that for both Si-face and

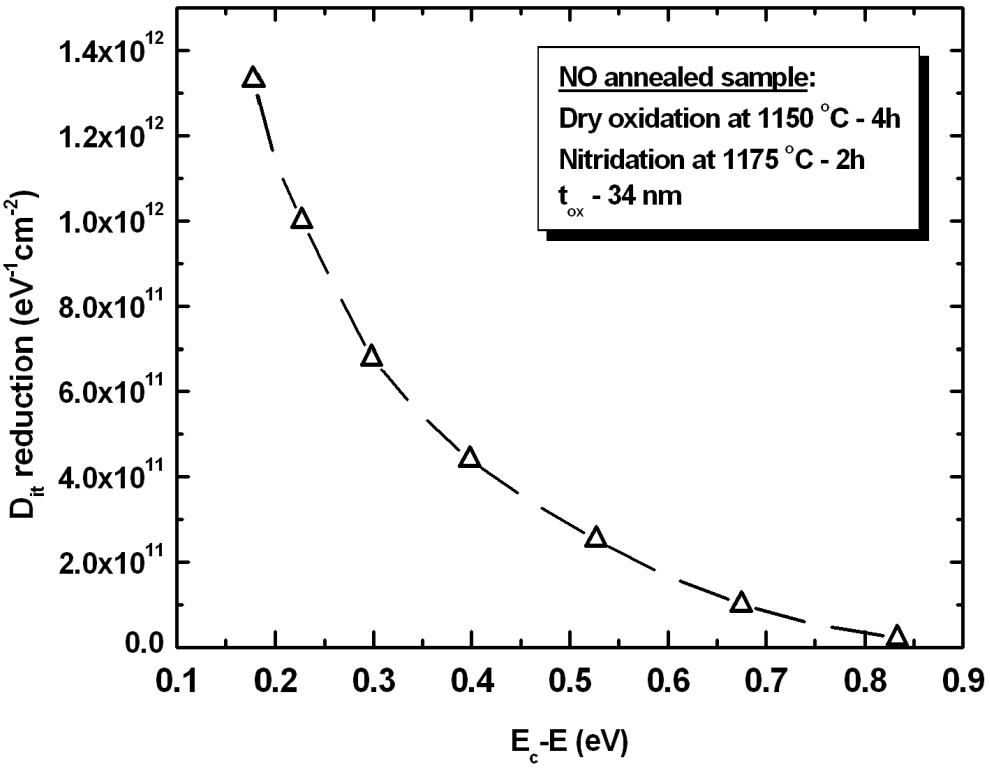

Figure 3.7 D_{it} reduction in $eV^{-1}cm^{-2}$ between the as-oxidized and the NO annealed sample plotted as a function of distance from the conduction band edge (E_c-E) in eV.

the a-face, N plays a critical role in the upper half of the 4H-SiC band gap, close to the conduction band edge due to its increased ability to reduce the interface trap density appreciably more for states up to E_c-E ~ 0.6 eV [10]. The D_{it} curves are plotted only to the limit of E_c-E of 0.6 eV since the data below this energy window are not reliable for understanding C-V measurements done at room temperature.

At room temperature the interface traps 0.6 eV away from the conduction band edge trap/emit carriers as a function of the d.c. bias sweep thereby responding to the Fermi level position. For carriers trapped in deep states at E_c-E > 0.6 eV, the time constants are too large (several years) at room temperature and they do not respond to the

gate bias sweeps. These time constants increase exponentially with energy from the band edge [6]. In our case (*n*-type 4H-SiC), the time constant for electron emission from an interface trap into the conduction band can be written as [6, 21]

$$\tau_e(E) = \frac{1}{\sigma_e \upsilon_T N_c} \exp\left(\frac{E_c - E}{kT}\right) \tag{3.1}$$

where σ_e is the capture cross-section for electrons, υ_T is the electron thermal velocity, N_c is the effective density of states in the conduction band, $(E_c - E)$ is the energy location of the interface trap relative to the conduction band edge, *k* is the Boltzmann's constant, and *T* is the absolute temperature. Hence the charges trapped in these interface traps remain trapped and appear as fixed charge on the time scales of the measurements thereby not creating a substantial stretch-out in the C-V curve [6].

3.3.2 Photo-CV measurement technique

An alternative technique of photo-CV (capacitance measured under UV exposure) [22] was employed for better understanding of slower interface traps deeper in the band gap. Figure 3.8 shows the photo-CV measurements done on Si-face samples as a part of pre-irradiation characterization for the capacitors. These were done for the NO annealed and as-oxidized samples. The procedure involves sweeping the curves first from accumulation to deep depletion (thermal generation rate is low for inversion), which refers to the lower curve. The bias was held in deep depletion at a particular voltage for a long time with the UV lamp now turned ON. This results in photo-generation, which creates the inversion layer and the capacitance slowly rises to a higher equilibrium value on the C-V meter. After this layer is formed, the light is switched off and the sample is swept back to accumulation. These were performed on samples NO annealed for 2h at

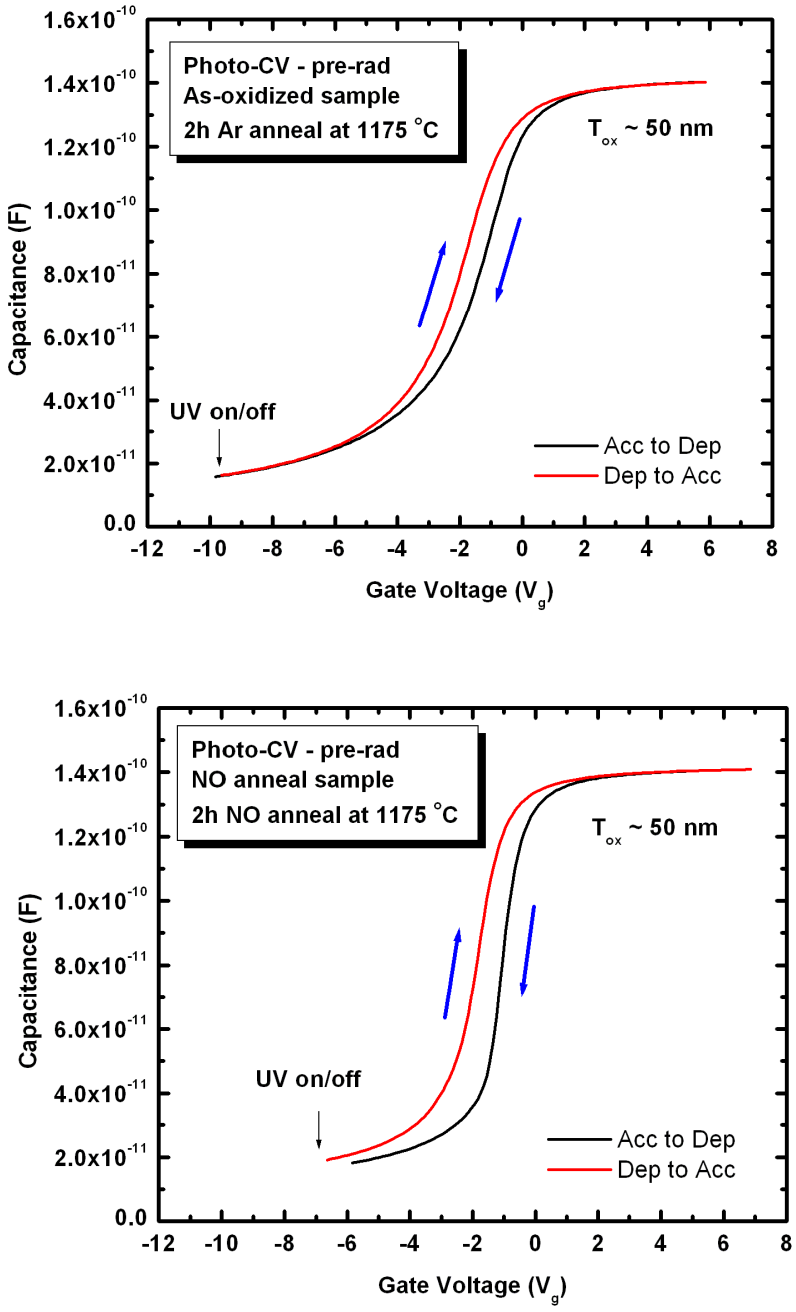

Figure 3.8. Photo-CV done by performing a accumulation to depletion gate sweep followed by UV excitation in depletion and sweeping back from depletion to accumulation after turning UV light off for as-oxidized (3.8a) and nitrided (3.8b) SiO_2/4H-SiC MOS capacitors. The oxide thicknesses for these samples were ~ 50 nm.

1175 °C with an oxide thickness of ~ 50 nm. The stretch-out is reduced substantially after NO annealing as seen from the photo-CV curves in Figure 3.8a and b, which is an

indication of D_{it} reduction with annealing in these capacitors.

3.4 Conclusion

These pre-irradiation device characterizations were performed to understand the quality of the oxide and the device behavior before and after NO annealing. The results of materials analysis from previous studies unequivocally verify the presence of nitrogen at the SiO_2/SiC interface. Our electrical studies show that this nitrogen incorporation correlates with an improvement in the device behavior of NO annealed structures.

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CHAPTER IV

TOTAL DOSE RADIATION RESPONSE OF NITRIDED AND NON-NITRIDED SiO_2/4H-SiC MOS CAPACITORS

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4.1 Abstract

The total dose radiation response of nitrided and non-nitrided *n*-type 4H-SiC is reported for metal oxide semiconductor capacitors exposed to 10-keV X-rays under positive bias. The radiation response is affected strongly by differences in the SiC band

gap and interface/near interface SiO_2 trap density from typical Si MOS devices. Significantly higher net trapped positive charge densities were observed in nitrided *n*-SiC MOS capacitors compared to the non-nitrided samples. The mechanisms contributing to the differences in the charge trapping in these devices are discussed. Differences in the interfacial layer between SiO_2/Si and SiO_2/SiC are responsible for the observed dissimilarities in charge trapping behavior.

4.2 Introduction

Silicon has been the most widely used semiconductor material and has remained largely unchallenged in the microelectronics industry for the past several decades. However, silicon is not ideal for some high power applications where a larger energy gap and higher thermal conductivity are desirable. Silicon carbide (SiC) possesses unique physical properties that are extremely favorable for high temperature and high-power electronics. For the 4H-SiC polytype, properties include a wide band gap (~3.3 eV), high thermal conductivity (4.5 W cm^{-1} s^{-1}), high electron saturation velocity (2.0×10^7 cm s^{-1}) and a high breakdown field (2.0 MV cm^{-1}) [1], [2]. The ability to grow thermal oxides (SiO_2) using conventional thermal oxidation (like Si) is a major advantage for the development of SiC metal oxide semiconductor field effect transistors (MOSFETs) [3], [4]. Recent developments in SiC device technology have opened up the aerospace and aircraft domains for SiC based power electronics, where these devices could be utilized for substantial weight savings and enhanced jet engine performance. Among the numerous SiC polytypes (that is, having the same chemical composition, but with different crystal structures from different stacking orders), 4H- and 6H-SiC are

commercially available in a quality considered appropriate for device applications. Of the different forms of SiC, the 4H-SiC polytype is considered the most desirable as compared to the others due to its significantly higher and more isotropic bulk carrier mobility [5]. This work focuses on the effects of ionizing radiation on the charge trapping behavior of MOS capacitors fabricated on 4H-SiC substrates.

Historically, 4H-SiC MOSFETs suffered from low inversion channel mobilities due to extremely high pre-irradiation interface trap densities (D_{it}) close to the 4H-SiC conduction band-edge ($D_{it} > 10^{13}$ cm^{-2} eV^{-1}). Annealing in hydrogen, which is a key in improving the quality of the interface in SiO_2/Si is not effective in the case of SiC [6]. Alternatively, nitridation of the SiO_2/SiC interface has emerged as the most effective solution to reduce the pre-irradiation interface trap densities. Nitridation via post-oxidation annealing in NO results in significant reduction of D_{it} ($D_{it} \sim 10^{12}$ cm^{-2} eV^{-1} at E_c-E ~ 0.1 eV) and subsequently improves channel mobility [7]-[10]. For applications in radiation environments, it is important to study the radiation tolerance of 4H-SiC MOS devices. In this paper, we report the x-ray radiation response of positively biased (E_{ox} = ~ +1.5 MV/cm) nitrided and non-nitrided 4H-SiC MOS capacitors grown on the (0001) Si face. We compare the results of these irradiations to previously published data for grounded irradiations and find significant differences, mainly due to enhanced hole trapping [11]-[14]. These results provide new insights into the nature of charge trapping at the SiO_2/SiC interface.

4.3 Experimental section

Commercially available 4H-SiC (n-type, (0001) Si-face) substrates with nitrogen doping of 5 x 10^{15} cm^{-3}, were used to fabricate the MOS capacitors. A 10 µm thick epitaxial layer was grown on these n+ substrates. Before the oxidation step, samples were cleaned using an industry standard RCA cleaning procedure. Approximately 34 nm thick oxides were grown by performing dry oxidation at 1150 °C for 4 h. The samples were annealed in flowing Ar for 30 min at the same temperature after oxidation. Some of the samples were subsequently nitrided at 1175 °C in flowing NO for 2h. The gas was changed back to Ar and the temperature ramped down to 900 °C before removing the samples from the furnace. Two layers of gate metal, namely 100 nm of Mo followed by 100 nm of Au, were deposited by DC sputtering. Circular MOS capacitor contacts with diameters of 350 µm and 700 µm were patterned and defined using standard photolithography and lift-off techniques. A schematic diagram of the capacitor stack is as shown in Figure 4.1.

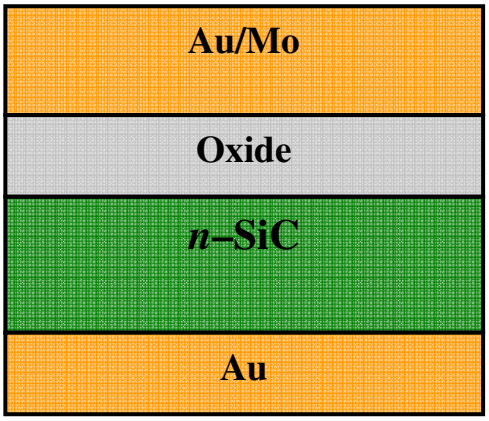

Figure. 4.1. Schematic diagram of the capacitor stack with Au/Mo gate metal contact, ~ 34 nm thermal oxide, 4H – SiC substrate, and Au back contact.

The capacitors were characterized using capacitance voltage (CV) measurements to measure the effective oxide charge and interface trap density (D_{it} – calculated by comparing the high frequency and quasistatic measurements) before irradiation [15]. Pre-irradiation CV measurements on the nitrided and non-nitrided capacitors verified the effect of nitrogen incorporation in reducing the interface trap density (D_{it}) from ~ 7×10^{12} cm^{-2} eV^{-1} to 1×10^{12} cm^{-2} eV^{-1} at E_c-E = 0.2 eV after nitridation.

Nitrided and non-nitrided SiC MOS capacitors were irradiated in an ARACOR 10-keV X-ray source at a dose rate of 31.5 krad (SiO_2)/min. Post-irradiation characterization was performed by similar CV measurements. The irradiations were performed as a function of bias and dose for the two different samples. The samples were exposed at room temperature to doses of 30 to 10,000 krad(SiO_2) at a positive bias (E_{ox} = ~ 1.5 MV/cm) during irradiation. The CV curves were measured at 100 kHz at room temperature with a ramp rate of 0.5 V/s for the dc voltage sweeps. The shifts in these curves were compared with the pre-irradiation high-frequency curves for calculating radiation-induced charge buildup. The Winokur and McWhorter charge separation technique was used for further analysis [16]. For Si MOS devices, the midgap voltage shift, ΔV_{mg} is frequently assumed to be proportional to the increase in oxide-trap charge density. The stretchout in the CV curves between midgap and flatband along the voltage axis, commonly referred to as ΔV_{it}, was used to estimate the increase in the interface trap density following the irradiations [16]-[18]. It should be noted that midgap voltage shifts for a wide band-gap material such as SiC include significant contributions from deep interface traps (which appear as fixed charge) in addition to the oxide trapped charge, as we discuss further below. Hence, effects that usually would be observed in the threshold

or flatband voltage for Si MOS devices can be observed in midgap voltage for SiC MOS devices. In addition, in SiC, the major fraction of ΔV_{it} arises from interface traps with energy levels between flatband and ~ 0.6 eV from the conduction band edge [19]. This contrasts with Si where the energy levels of the interface traps measured from CV analysis are located between flatband and inversion. In order to further investigate the radiation-induced charge, isochronal annealing studies were performed by annealing at a positive bias of 5 V at temperatures from 25 °C to 175 °C [20]. The sample was heated in 25 °C steps and held at the respective temperatures for 10 min before cooling back down to room temperature for CV measurements. The contributions from the positive and the negative charges were extracted from these measurements.

4.4 Results and Discussion

4.4.1 Fundamental band gap and interlayer differences in SiO_2/Si and SiO_2/SiC

It is important to understand the basic differences between the SiO_2/Si and the SiO_2/SiC MOS systems before addressing the radiation damage behavior. As the bulk of the oxide grown on SiC is stoichiometrically similar to oxides grown on Si, bulk hole trapping is expected to be similar to the trapping in SiO_2/Si capacitors when exposed to radiation. On the other hand, the SiO_2/SiC interface is markedly different than Si. In addition, there exists a considerable difference in the band gap and band offsets of Si and SiC with respect to SiO_2. A detailed schematic diagram of the band gap of SiC and Si with respect to SiO_2 is shown in Figure 4.2. Note that certain intrinsic defects common to both the SiO_2/Si and SiO_2/SiC system may fall within the band gap of SiC, but not in Si. Furthermore, in SiC, the response times of the interface traps during the CV sweep

increase exponentially with energy from the band edge. As a consequence, interface traps deeper in the SiC band gap (E_c-E ~ 0.6 eV to E_c-E ~ midgap for n-SiC), appear as fixed charge, as they do not respond to changes in the applied bias during the time scale of the CV measurements [19].

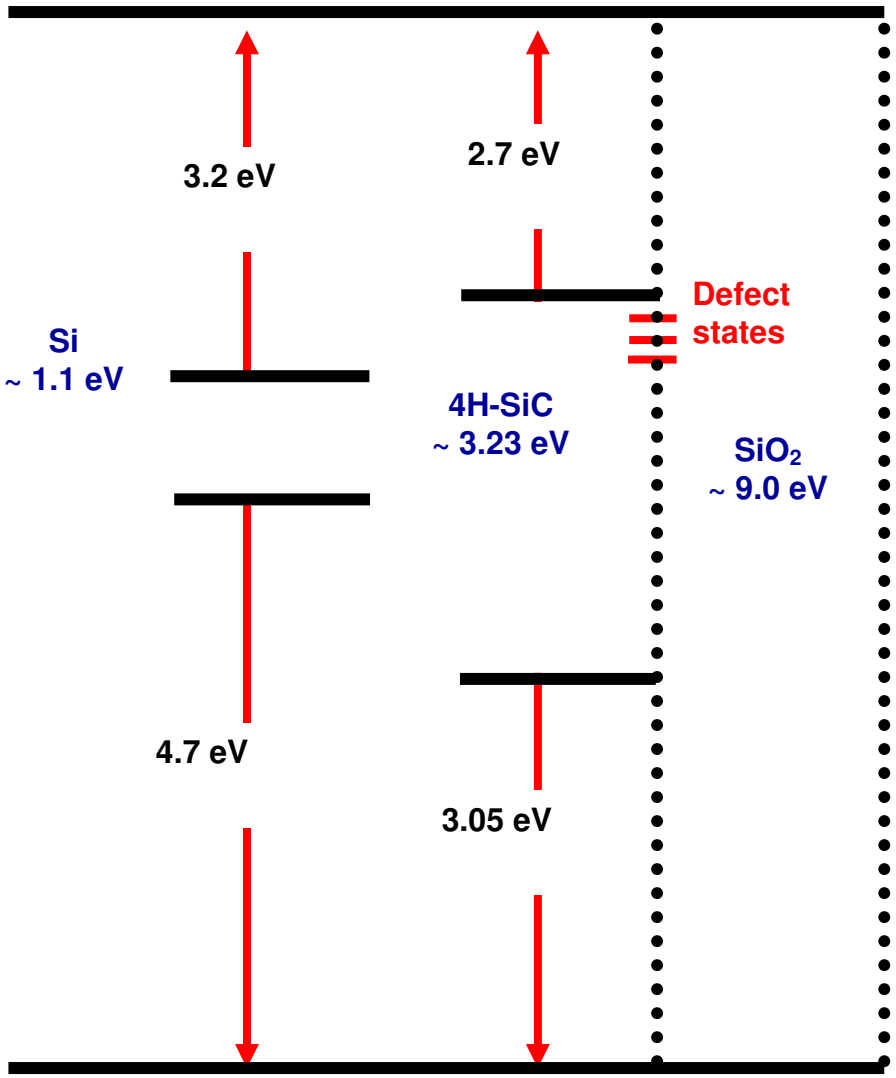

Figure 4.2. Schematic band diagram of Si, 4H-SiC and SiO_2 shows that the wider band gap in the case of 4H-SiC results in more interface trap buildup being observed which otherwise would have figured outside the Si band gap.

4.4.2 Radiation results (nitrided & non-nitrided)

Figures 4.3 and 4.4 show the radiation response of nitrided and non-nitrided SiO_2/4H-SiC samples under positive bias. For the non-nitrided devices, initially the CV curves shift to the left due to a predominance of trapped positive oxide-trap charge, but then shift to the right with higher doses owing to the buildup of negative charge. Contrary to the non-nitrided case, the nitrided samples continued to show a monotonic increase in the net positive charge for all irradiation doses up to 10 Mrad(SiO_2), as evident from Figure 4.4.

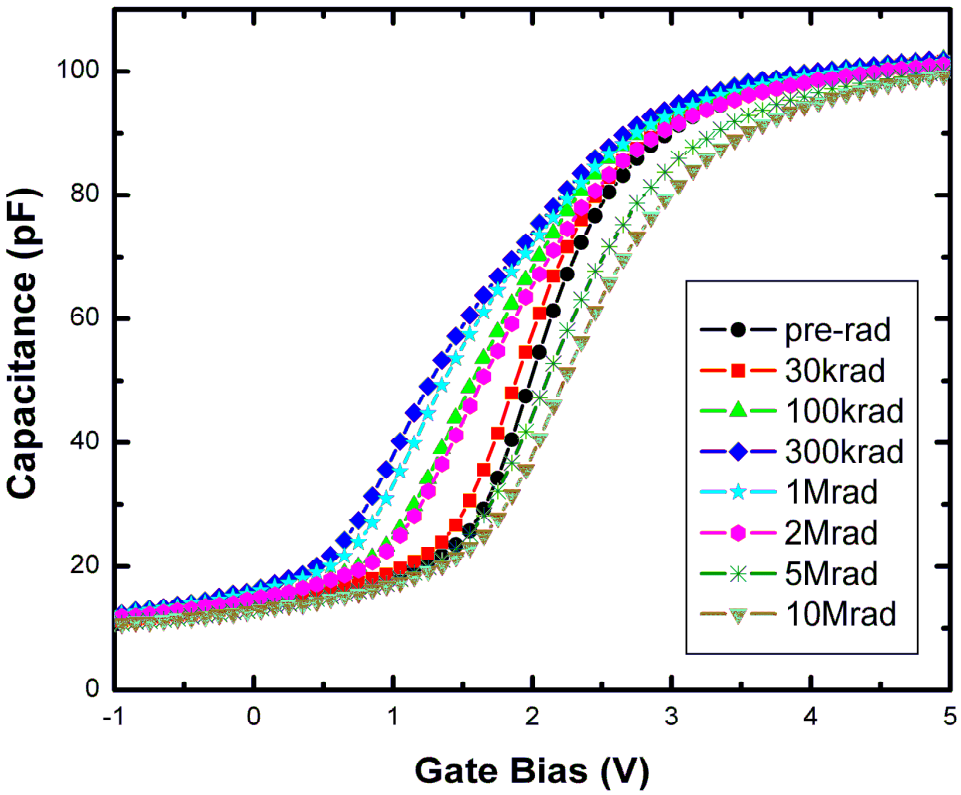

Figure. 4.3. 100 kHz CV curves showing first positive charge trapping, and then a turnaround from positive to negative charge trapping for non-nitrided capacitors biased at 1.5 MV/cm.

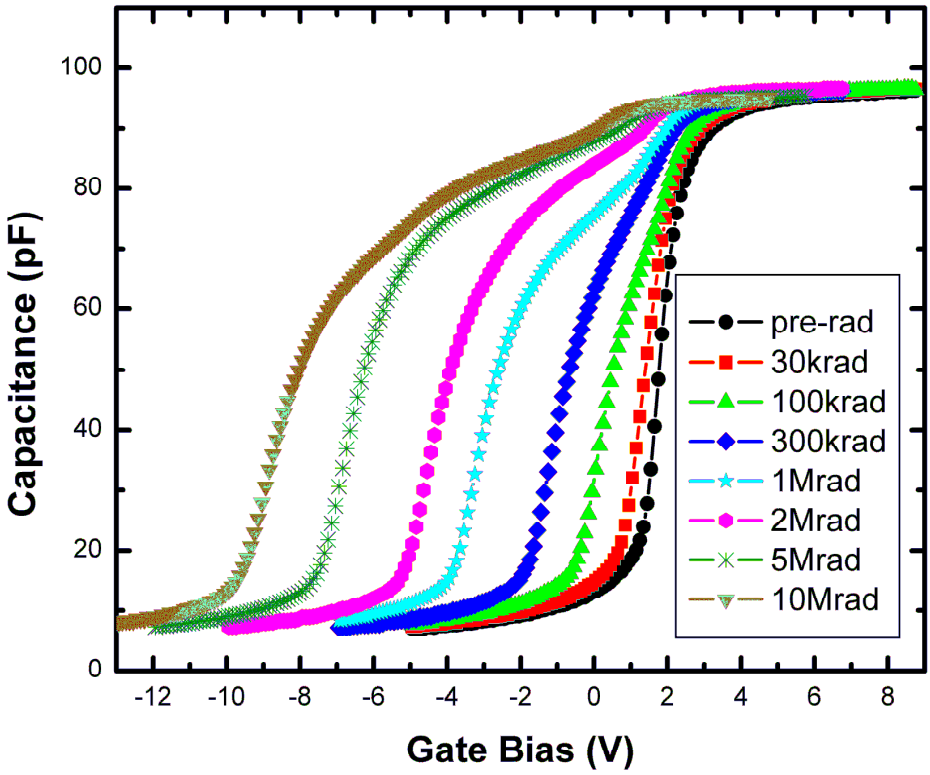

Figure. 4.4. 100 kHz C-V curves showing the increased positive charge trapping for positively biased (E_{ox} = ~ + 1.5 MV/cm) nitrided capacitors.

ΔV_{mg} and ΔV_{it} are plotted as functions of dose for both sample types in Figures 4.5 and 4.6, respectively. The turnaround in ΔV_{mg} is seen clearly for the non-nitrided devices at doses above ~ 300 krad(SiO_2) in Figure 4.5; indicating lower net trapped positive oxide-trap charge than the nitrided devices. For higher doses, negative charge trapping dominates for the non-nitrided devices. Hence a charge compensation effect is observed for the non-nitrided samples similar to earlier work using electron injection [21]. The turnaround from net positive to negative charge trapping in midgap voltage for the non-nitrided samples can be attributed to deep interface trap buildup (E_c-E ~ 0.6 eV to

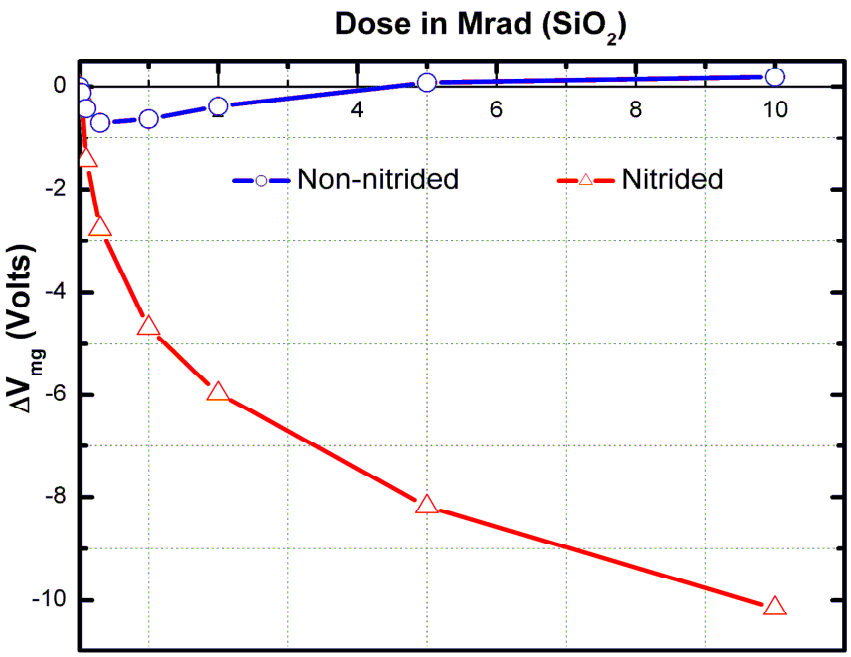

Figure 4.5. Voltage shifts (ΔV_{mg}) as a function of dose in Mrad(SiO_2) for nitrided and non-nitrided samples positively biased at 1.5 MV/cm.

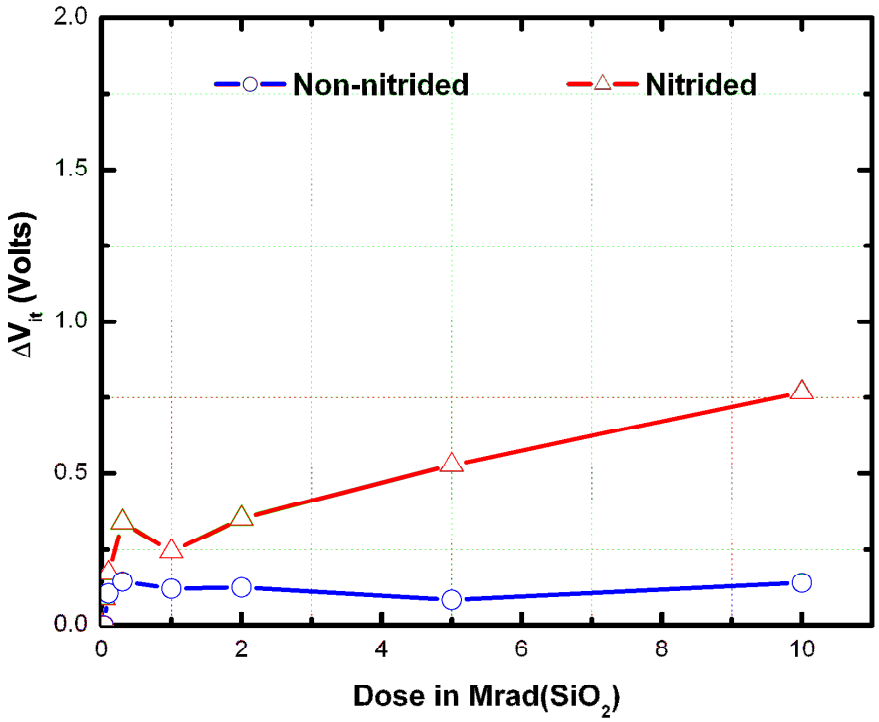

Figure 4.6. Voltage shifts (ΔV_{it}) as a function of dose in Mrad(SiO_2) for nitrided and non-nitrided samples positively biased at 1.5 MV/cm.

midgap) and/or negative charge buildup due to near-interfacial electron traps [12], [13], [22]. The precursors to these electron traps may not be charged during pre-irradiation characterization when the Fermi level sweeps through the band gap, but become charged due to ionizing radiation. Earlier studies have reported interface trap buildup at non-nitrided SiO_2/SiC interfaces resulting from electron injection via photo and Fowler-Nordheim methods [21]-[24]. A significant density of acceptor states was observed at the SiO_2/SiC interface after electron injection as compared to SiO_2/Si [21], [23]. This was tentatively ascribed to the presence of excess carbon in the form of carbon clusters with sp^2 bonding at the SiO_2/SiC interface. Thus, the turnaround observed in the midgap voltage plotted in Figure 4.5 may be due to the result of compensation of positive charge from both negatively charged deep interface traps and near-interface electron traps.

In the nitrided case, the midgap voltage shifts due to the increase in the oxide trap charge with increasing dose and do not show a turnaround effect. Net positive charge trapping continues to the highest dose studied. Hence, the nitridation process and/or the nitrided interlayer, on the order of ≤ 1 nm from the SiO_2/SiC interface, must contribute in an essential way to the observed differences in trapping between the nitrided and the non-nitrided samples [25]. The ΔV_{mg} was observed to be about –10 V at 10 Mrad(SiO_2) for the nitrided capacitors. This does not appear to reach saturation, indicating the possibility of more hole trapping for doses above 10 Mrad(SiO_2). The values of ΔV_{it} estimated from the differences in the flatband and midgap voltage shifts indicate a small increase in interface-trap density in both cases (nitrided and non-nitrided), plotted as a function of dose in Figure 4.6, however once again we caution that this measures only relatively shallow interfaces traps in SiC MOS devices, with deeper traps contributing to midgap

voltage shifts, in contrast to Si MOS devices, where the full interface-trap distribution contributes to ΔV_{it}.

Photo-CV was performed on a different set of nitrided and non-nitrided samples fabricated using the same procedure as described earlier in this chapter. The oxide grown this time was ~ 50 nm. These MOS capacitors were exposed to a 5 Mrad(SiO_2) total radiation dose. Photo-CV curves were measured before and after the final x-ray dose for investigating the hysteresis. Figure 4.7 shows the post-irradiation hysteresis observed using photo-CV for these two samples. On comparison with the pre-irradiation photo-CV hysteresis for the two samples (Figure 3.8), clearly the non-nitrided samples did not show a large increase in the hysteresis (~ 0.5 V) at flatband. The nitrided sample on the other hand showed a significant increase of ~ 3 V in the hysteresis measured at flatband condition following the x-ray dose. These results indicate the presence of slower interface traps deeper in the band gap which can respond to the gate bias after UV-exposure thereby indicating a substantial increase in the number of these states with a 5 Mrad(SiO_2) x-ray dose.

4.4.3 Enhanced positive charge trapping in F-N tunneling and VUV experiments

Charge injection studies using Fowler-Nordhiem (F-N) tunneling and internal photoemission were performed by Rozen *et al.* to verify the enhanced positive charge trapping in the nitrided SiO_2/4H-SiC MOS capacitors, as originally observed in the x-ray studies. These measurements reproduced the hole trapping effect as shown in Figure 4.8. These figures show a trend similar to the x-ray results with trapped charge density in both these experiments plotted as a function of emitted/injected hole density.

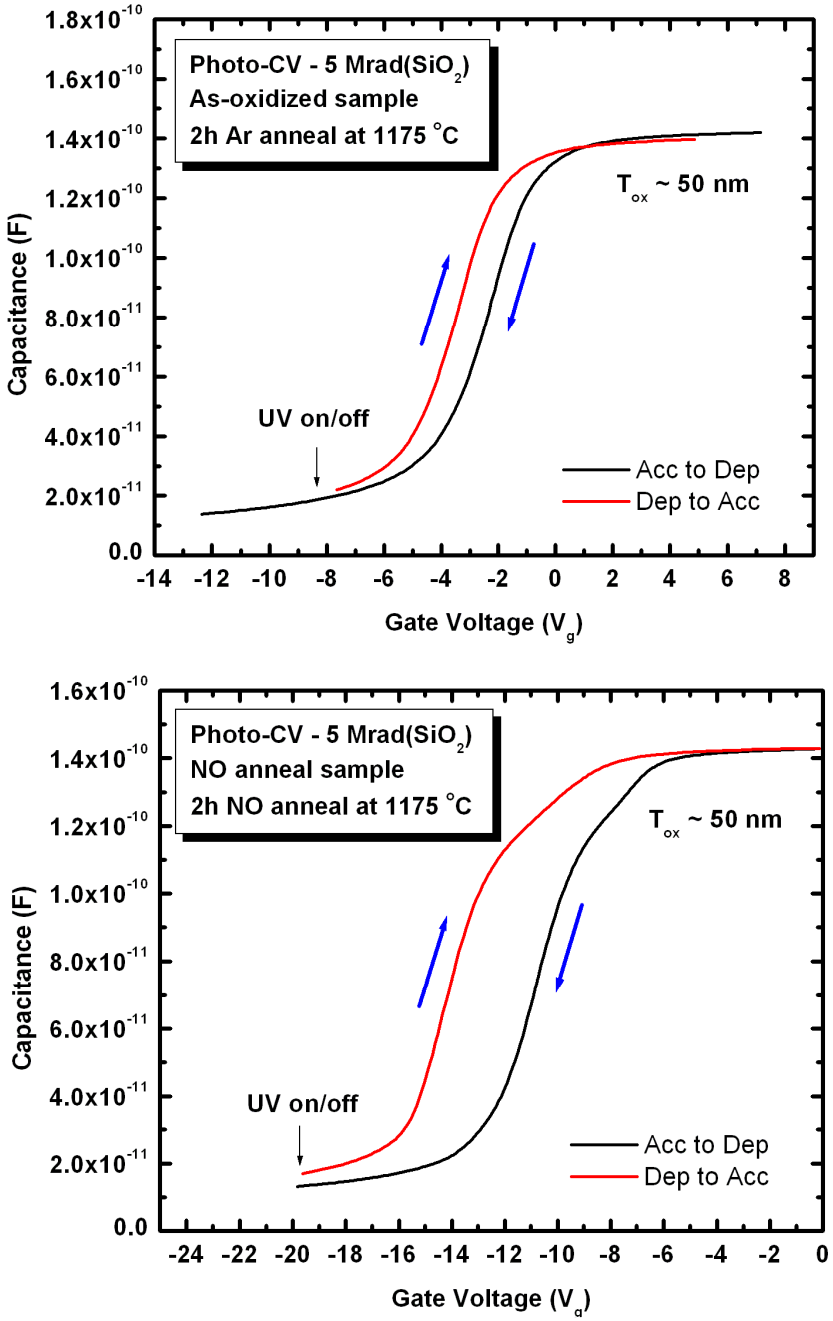

Figure 4.7. Photo-CV done by performing a accumulation to depletion gate sweep followed by UV excitation in depletion and sweeping back from depletion to accumulation after turning UV light off for as-oxidized and nitrided SiO_2/4H-SiC MOS capacitors after a 5 Mrad(SiO_2) x-ray dose at + 1.5 MV/cm oxide field. The oxide thicknesses for these samples were ~ 50 nm.

The details of the experiments and the relevant discussion for the findings are described in Ref. [26]. The magnitude of the charge trapping is not the same as the x-rays since the x-ray fluence is relatively high as compared to the injected/emitted charges. It is also important to note the similarity in the charge trapping behavior for the non-nitrided

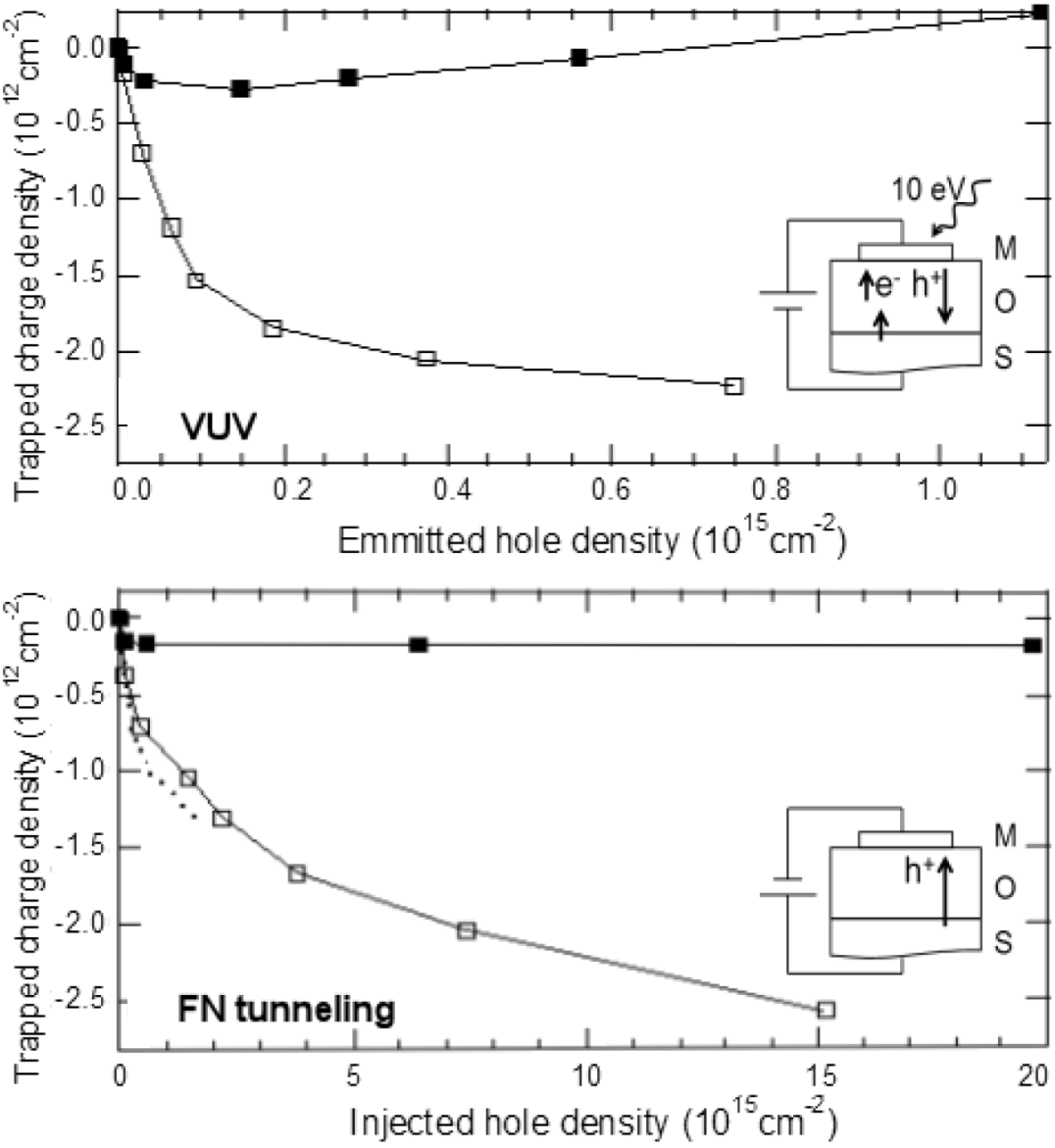

Figure 4.8. Plot of the trapped charge density versus emitted hole density (VUV) /injected hole density (F-N tunneling) for the nitrided 4H-SiC MOS capacitors Ref. [26].

samples in all of the three charge-trapping methods described here. Charge trapping is an undesirable device attribute, but the nitrogen content is necessary for device performance. This excellent agreement in the charge-trapping trend for both the nitrided and the non-nitrided samples using different techniques strongly suggests the need to optimize the nitrogen content for better reliability in these devices. It necessitates the need to arrive at optimum nitrogen content in order to strike a balance between D_{it} reduction and improved reliability following post oxidation annealing treatments in these devices.

4.4.4 Mechanisms for enhanced positive charge trapping in nitrided capacitors

We first note that much larger shifts in the nitrided SiC MOS devices observed here are larger than in previous studies of devices irradiated without bias [11]-[14], owing to the increased charge yield for biased irradiation, as opposed to unbiased irradiation [27]. One possible reason for the extremely large positive oxide-trap charge densities in these devices is the large oxygen vacancy density that is expected from the extremely high oxidation temperatures necessary to grow SiO_2 on SiC. Previous electron-paramagnetic resonance, electrical, characterization, and thermally stimulated current (TSC) studies have shown a strong correlation between high oxidation temperatures, high oxygen vacancy densities, and large net positive-oxide-trap charge buildup [28]-[30], at least in the absence of the charge compensation processes observed in the non-nitrided devices above in Figures 4.3 and 4.5. Indeed, detailed TSC studies of nitrided oxides have shown a significant enhancement of O-vacancy related hole trapping in reoxidized nitrided oxides for Si MOS devices [31].

We now discuss other mechanisms unique to SiC for the enhancement in midgap voltage shifts in the nitrided devices that is suggested by recent experimental and theoretical work. Oxidation of SiC to form SiO_2 requires the removal of C (typically in the form of CO that leaves the growing oxide) [32]. Some of the C, however, inevitably remains at the interface and forms defect structures. Nitridation in NO plays a significant role in passivating the fast interface traps, presumably by removal of π-bonded carbon, and also is known to eliminate slow trap centers in the near interfacial region of SiC [33], [34]. This reduction occurs over the entire band gap of SiC, although most drastically near the conduction band edge. This pronounced reduction of the density of interface and near-interface electron traps at nitrided interfaces means there is less compensation of the positive charge trapped in the bulk of the oxide and hence no evidence of turnaround for the nitrided capacitors. Moreover, extensive theoretical calculations [35], done using density-functional theory (local-density approximation with generalized gradient corrections for exchange-correlation, ultra-soft pseudo-potentials, plane-wave basis sets, and large supercells; details of the supercells are reported in Ref. [30]), combined with available experimental evidence and prior analysis, have led to the conclusion that the SiO_2/SiC interface contains a transition layer that can best be described as a Si-C-O bonded amorphous network composed of Si-O-Si bridges, and direct Si-Si, C-C, and Si-C bonds [35]. Si atoms would be primarily fourfold-coordinated because C atoms would preferentially occupy sites with threefold coordination, in which case they can be referred to as C dangling bonds (amorphous carbon has both three- and four-coordinated C; amorphous SiC contains C dangling bonds but there is no evidence for Si dangling bonds). Thus, the primary defect structures that can produce localized energy levels in the

SiC band gap are isolated C dangling bonds, C dangling-bond complexes (e.g., a C-C bond where both C atoms are threefold coordinated), and Si-Si bonds (the latter are true defects in the SiC/SiO_2 interface, whereas they appear as defects at the Si/SiO_2 interface only when they are longer than normal Si-Si bonds). C dangling bonds have localized levels in the SiC band gap. Si-Si bonds, depending on the bond length, may have both a bonding and an antibonding level in the SiC band gap (bottom and top of the band gap, respectively).

It has further been proposed that nitrogen passivation of interface traps occurs because it is energetically favorable for N to replace threefold-coordinated C and Si atoms (N always prefers threefold coordination, whereas C assumes both, with a slight preference for three, as in graphite versus diamond). The result is a Si-C-N-O bonded interlayer [35]. New calculations, using density functional theory suggest that the threefold-coordinated N at the SiC/SiO_2 interface results in a localized level at ~ 0.5 eV from the valence band edge of SiC due to the N lone pair. This lone pair can trap holes under ionizing radiation, thereby enhancing the effects of increased positive charge trapping in the NO passivated samples.

Finally, we note that it is likely that the nitrogen also reduces the densities of interface defects that appear as fixed charge in SiC devices, but would show up as interface traps in Si devices, consistent with observations of the effects of nitridation on oxides on Si [36]-[38]. The absence of charge compensation via interface-trap buildup would show up as increased midgap voltage shifts in the nitrided devices.

4.4.5 Annealing studies

Owing to the similar densities in the range of 10^{12} cm^{-2} for both positive and negative charges, the compensation effect explains the apparent superior radiation hardness of non-nitrided SiC MOS structures as described elsewhere [39]. This counterbalance between the two charges in the non-nitrided samples was verified from isochronal annealing studies [20] conducted at + 5 V bias as evident from the C-V curves in Figure 4.9.

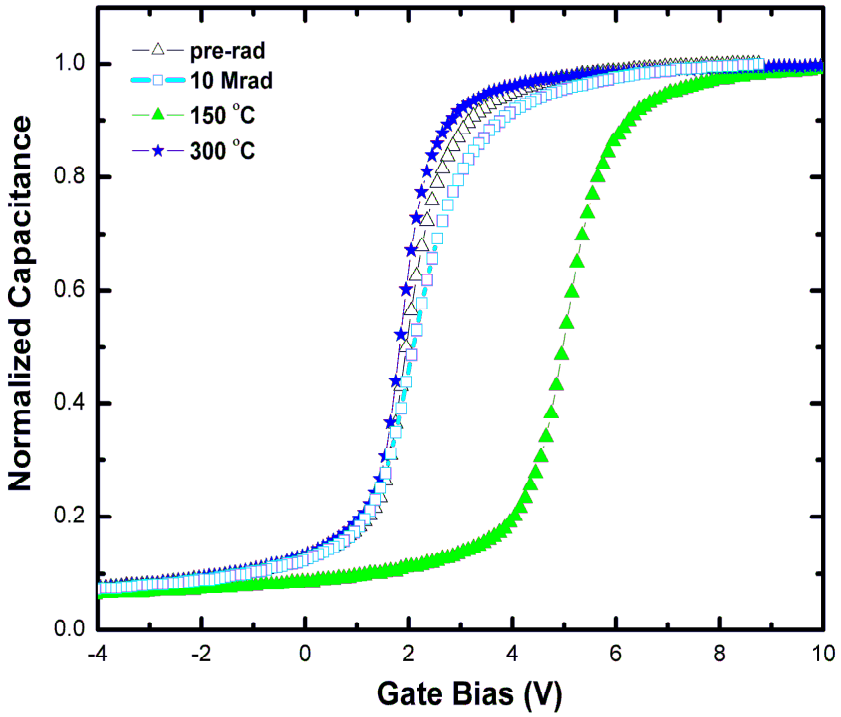

Figure 4.9. C-V curves plotted for the annealing cycles for non-nitrided capacitors with pre-irradiation (--Δ-- open triangles), 10 Mrad(SiO_2) (--o-- open circles), 150 °C anneal (--▲-- closed triangles) and 300 °C anneal (--★-- closed stars) indicating the compensation effect.

The figure shows pre-irradiation and post-irradiation C-V curves measured after 10 Mrad(SiO_2). The elevated temperature annealing studies were performed after two

weeks of room temperature annealing with all of the positive charges annealed at 150 °C. A significant portion of the negative charge annealed at higher temperatures (~ 300 °C). This was confirmed from the isochronal annealing measurements. The C-V curves begin to shift towards positive voltages with every 25 °C temperature increase (all curves not shown), indicating a decrease in the net-trapped positive oxide trap charge. Finally, at 150 °C, the C-V curves no longer shift with increasing temperature, and the curve remains on the positive side of the pre-irradiation curve until significantly higher temperatures are reached (direct annealing to 300 °C, as described further).

This validates the hypothesis of the existence of both positive and negative charges, with only the negative contribution present after a 150 °C anneal. The C-V curves still exhibit stretch-out, compared to pre-irradiation curve, even after annealing at 150 °C. The temperature was further increased directly to 300 °C, this time with no bias applied, and the C-V curve shifted back to its pre-irradiation position and the radiation-induced stretchout disappeared. This confirms the annealing of interface trapped charge at higher temperatures and is consistent with earlier reports [21], [23]. The possibility of electron injection during the annealing cycles was probed by biasing the pre-irradiated devices at + 5 V for 10 min at 100 °C and no change in the C-V behavior was observed.

Annealing studies were also conducted on nitrided samples, with the detrapping of most of the predominant positive charge observed between 25 °C and 175 °C. These studies were performed using the same procedure as for the non-nitrided samples as described above. We introduce a model for obtaining a activation energy for the annealing of the predominant positive charge in the nitrided samples. Removal of positive charges occurs by hole emission during these isochronal annealing studies

[40],[41]. The probability of this emission $p_{em}(T)$ is determined from the shift in the flatband voltage in these NO-annealed capacitors.

$$p_{em}(T) = \frac{Q_{trap}(T - \Delta T) - Q_{trap}(T)}{Q_{trap}(T - \Delta T)} \tag{4.1}$$

where $Q_{trap}(T - \Delta T)$ is the number of trapped charges present at the starting temperature before each temperature increase, $Q_{trap}(T)$ is the amount of charges remaining at end of each annealing step, ΔT represents the temperature increase of 25 °C under a positive bias of E_{ox} ~ 1.5 MV/cm. As a control experiment it was observed that there was no evidence of electron tunneling induced neutralization from the semiconductor at room temperature at the fields mentioned above over a period of 20 mins. Hence assuming that charge annealing occurs from thermal emission at increased temperatures we can write the equation for activation energy as mentioned below

$$p_{em}(T) \equiv \Delta t e_{th}(T) \propto \Delta t T^2 e^{-E_a / kT} \tag{4.2}$$

where e_{th} is the thermal emission rate, Δt is the incremental hold time of 10 minutes at each temperature and E_a is the activation energy. A fit to the curve of $p_{em}(T)$ vs T for the activation energy as shown in Figure 4.10, yields E_a of approximately 0.3 eV. Hence if we assume that holes emit into the valence band of SiO_2, this energy represents a state above the SiO_2 valence band edge. This indicates that some of the states introduced from nitrogen incorporation fall within the band gap of SiC.

These curves did not shift to the right of pre-irradiation as much as the non-nitrided samples did after the 175 °C anneal. These studies suggest the presence of

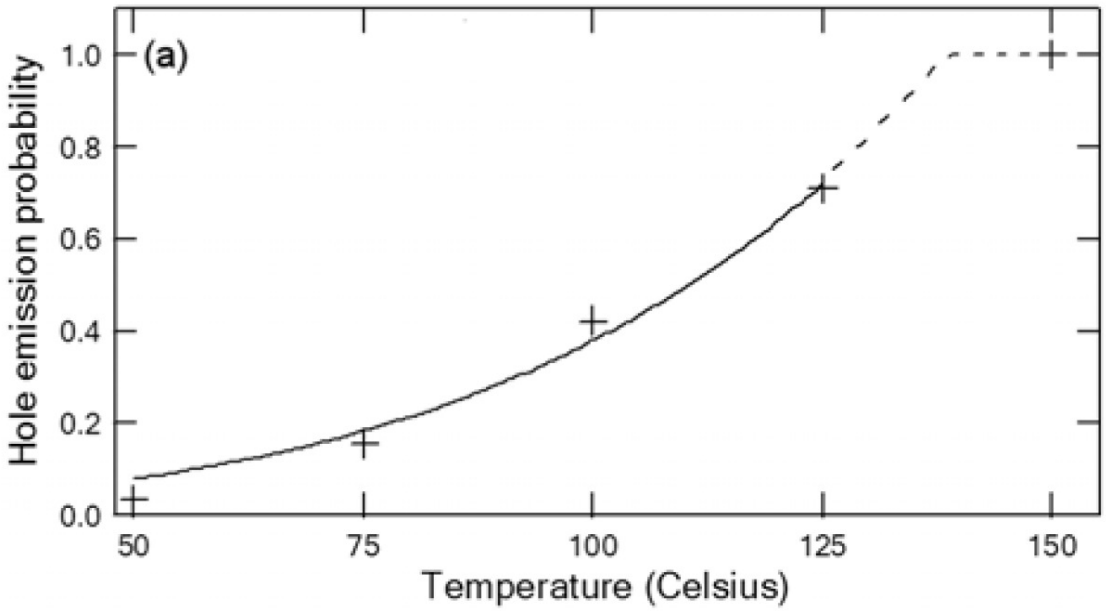

Figure 4.10. A fit for extracting the activation energy for the model describing the dependence of the hole emission probability on temperature during the isochronal annealing cycle Ref. [26].

exceedingly high positive charge and reduced negative charge contribution for the nitrided samples. The loss of the stretchout and return of the CV curve to its pre-irradiation position (curves not shown) was verified by annealing further from 175 °C to 300 °C, similar to the non-nitrided samples. Hence the post-irradiation annealing studies confirm the presence of positive and negative charge contributions to the C-V behavior in the nitrided and non-nitrided SiC MOS capacitors.

4.5 Conclusion

The total ionizing dose response of nitrided and non-nitrided SiO_2/SiC capacitors under positive bias was studied. Negative charge trapping in non-nitrided SiO_2/SiC devices was found to be significantly higher than for typical SiO_2/Si MOS structures. The high oxidation temperatures required to grow SiO_2 on SiC lead to high oxygen vacancy

densities. For the nitrided MOS capacitors, higher net positive charge build-up was observed, consistent with a lower density of interface and near-interface electron traps. Theoretical calculations also suggest a nitrogen lone pair present in the proximity of the valence band edge of SiC may increase positive trapped charge in the nitrided devices. It is also likely that these devices exhibit a decrease in interface defects that would appear as interface traps in Si devices, but function as negative fixed charge in SiC owing to its wider band gap.

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CHAPTER V

PHYSICAL AND ELECTRICAL CHARACTERIZATION FOR THICKNESS AND STOICHIOMETRY DETERMINATION IN HfO_2 /SiO_2 BASED ADVANCED GATE STACKS

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5.1 Abstract

HfO_2-based dielectrics with SiO_2 interlayers (ILs) were investigated for stoichiometry and thickness verification. Physical and electrical characterizations were performed as a function of varying bulk HfO_2 and SiO_2 IL thicknesses. These ion beam

and XRR measurements validate the oxide growth and deposition parameters with results indicating the thickness values of the HfO_2 bulk and the SiO_2 interlayers to be close to the targeted ones. Out-diffusion of Si and O is verified by the experimental results of Medium Energy Ion Scattering. Capacitance values are consistent with silicate formation in the dielectric. Current-Voltage (I-V) measurements provide additional information about the quality of the device and its operation.

5.2 Introduction

High-κ gate dielectrics on Si wafer can result in a high concentration of interface and near interface defects due to its thermodynamic instability, which can ultimately affect device performance [1]. Interface engineering schemes have been extensively studied over the past few years to tackle such intermixing issues [2, 3]. The introduction of a thin SiO_2 interlayer (IL) and/or its nitrided alternatives before the high-κ deposition improves the interface quality at the expense of reduced capacitance. Future metal-oxide-semiconductor (MOS) devices are likely to incorporate the thin oxide layer to improve the inversion layer mobility in these high-κ devices. The presence of nitrogen in the form of doping in the interlayer can have additional benefits like lower leakage and higher drive currents [1]. The high-κ gate dielectric included in this study is hafnium oxide (HfO_2), the material recently announced by Intel and IBM as the potential gate dielectric that would enable future scaling. Hafnium oxide is usually deposited using Atomic Layer Deposition (ALD) for better control of thickness and improved homogeneity of the thin films. It is extremely important to investigate the quality, composition and thickness of this oxide and its IL thickness values post metal gate deposition for establishing a reliable

CMOS recipe. This work concentrates on the physical and electrical characterization of varying thicknesses of bulk HfO_2 layers and SiO_2 ILs. We find excellent agreement between these techniques within ~ 10-15% experimental uncertainty for the various bulk and IL thicknesses studied. This study has been carried out as a part of this dissertation work, which concentrates predominantly on the radiation induced charge trapping response of HfO_2-based MOSFETs. These MOSFETs were fabricated using the same recipes as the ones used for making samples for materials analysis.

Radiation induced charge trapping is a strong function of the thickness of the dielectric facing the beam. Charge trapping occurring from radiation in the gate dielectric can be significantly altered due to the presence of an interlayer, a dielectric-dielectric interface and their intermixing issues. Hence it is important to reliably understand the materials structure of the system for interpreting the charge trapping characteristics of these oxide structures under radiation and bias stress. This work concentrates on these issues specifically as a part of pre-irradiation characterization for these advanced gate dielectric materials.

5.3 Experimental section

5.3.1 Sample preparation

Bare oxide films of varying bulk and IL thickness were fabricated for pre-irradiation materials and electrical (C-V) characterization. The HfO_2 samples were deposited by the controlled Atomic Layer Deposition (ALD) technique at SEMATECH. Before the high-κ deposition, an intentional SiO_2 interlayer (IL) was thermally grown (for thicker ILs) or by ozone treatment (for thinner ILs) on the bare Si wafers. The

sample matrix for pre-irradiation characterization of $HfO_2/SiO_2/Si$ included four different configurations of varying bulk and interlayer oxide thicknesses as shown in Table 5.1a. All the samples except for sample 1 were exposed for post deposition anneal (PDA) treatments. MOSFETs were fabricated by depositing similar films using the same ALD process for complete device characterization. For the MOSFET fabrication, the (001) Si wafers were subjected to an industry standard CMOS process flow for the gate oxide deposition. This was followed by gate metal deposition with subsequent PDA treatments. The transistors fabricated for device characterization are as shown in Table 5.1b.

Table 5.1a. Sample configuration for materials analysis with different HfO_2 bulk and SiO_2 interlayer (IL) thicknesses

Samples	t_{HfO2} (nm)	t_{SiO2} (nm)	PDA treatment
Sample 1	3.0	1.1	No PDA
Sample 2	7.5	1.1	NH_3 700 °C 30T 60s
Sample 3	3.0	2.0	NH_3 700 °C 30T 60s
Sample 4	7.5	3.0	NH_3 700 °C 30T 60s

Table 5.1b. Sample configuration for device characterization with different HfO_2 bulk and SiO_2 interlayer (IL) thicknesses

Samples	t_{HfO2} (nm)	t_{SiO2} (nm)	PDA treatment
Sample 1	3.0	1.1	NH_3 700 °C 30T 60s
Sample 2	7.5	1.1	NH_3 700 °C 30T 60s
Sample 3	3.0	2.0	NH_3 700 °C 30T 60s

Radiation induced charge trapping is a strong function of the composition of the oxide film. Apart from verifying the thicknesses of the bulk HfO_2 and SiO_2 interlayers, some additional insight into the composition of the dielectric layers can help in understanding the reason for charge trapping variation between these layers. This part of the chapter reports the results of several analytical techniques such as Rutherford Backscattering Spectrometry (RBS-annular and grazing geometries), Channeling, X-Ray Reflectometry (XRR), Medium Energy Ion Scattering (MEIS), and Capacitance-Voltage (C-V) measurements that were performed to verify the thicknesses and the composition in these bare HfO_2 (with SiO_2 IL) samples. The relative concentrations of Hf, O and Si are verified using ion beam techniques like RBS and MEIS.

Capacitor structures were fabricated with Al gate metal deposited by thermal evaporation and Au was sputtered for a large area back metal contact. MOS transistors were also fabricated using the state of the art 65 nm technology node for pre-irradiation MOSFET characterization. In the following section results from all of these techniques are discussed in further detail.

5.3.2 Physical Characterization

5.3.2a Rutherford Backscattering Spectroscopy (RBS)

Rutherford Backscattering Spectroscopy (RBS) relies on the interaction of a projectile atom (M_2) of energy (E_0) with a target atom (M_1) resulting in a simple elastic collision. This interaction results in the projectile being scattered back at an angle (θ) depending on its differential scattering cross-section ($d\sigma/d\Omega$) with an energy (E_1) that is defined by the kinematic factor (K). The kinematic factor (K) is given by

$$K = E_1 / E_0 = \left[\frac{(M_2^2 - M_1^2 \sin^2 \theta)^{1/2} + M_1 \cos\theta}{M_2 + M_1} \right]^2 \qquad (5.1)$$

Hence the energy of the outgoing projectile is characteristic of the mass of the target atom. This is the basic principle for the elemental identification of an unknown target atom. The integrated area under the spectrum for the respective element can be related to the amount of material that interacts with the incoming projectile. The elemental yield (Y) as given in the equation 5.2 depends on the average differential scattering cross-section, σ (integral of $d\sigma/d\Omega$ over the solid angle of the detector), the areal density of the scattering element(s) (Nt in at/cm^2), the total number of incident particles (Q) and detector solid angle (Ω) [4-6].

$$Y = \sigma\Omega.Q.Nt \qquad (5.2)$$

This is the fundamental formula used for calculating the bulk HfO_2 and SiO_2 IL thicknesses (Nt) mentioned in this chapter. Table 5.2 shows the average differential scattering cross-sections and the kinematic factors calculated for an incoming 1.8 MeV ^{4}He beam backscattered in an annular geometry (θ = 180°) for the elements considered in this investigation.

A 1.8 MeV He^+ beam from a Van de Graaff electrostatic accelerator was used to perform the RBS analysis. The detector was placed in an annular geometry at an exit angle of θ ~ 175°. A 100 keV Bi implanted sample with a calibrated areal density of ~ 4.8 x 10^{15} at/cm^2 was used for routine calibration prior to performing RBS measurements on the HfO_2 samples.

Table 5.2. Average differential scattering cross-sections and kinematic factors calculated for an incoming ^{4}He beam at 1.8 MeV backscattered in the annular (180°) geometry

Elements	Differential scattering cross-section (mb/sr)	Kinematic Factor (K)
	180°	180°
Hf	8175.2	0.91
O	90.25	0.36
Si	301.47	0.56

In order to accurately determine the total Hf and O peaks from the amorphous SiO_2 and the nanocrystalline HfO_2 layer, channeling along <100> was conducted for all the samples using the annular detector geometry. The areal densities of Hf, O and Si (IL) performed in an aligned (non-random) direction are mentioned in the next section. As shown below channeling studies provide a better estimation of the areal densities for the two films (HfO_2 and SiO_2).

5.3.2b. Channeling measurements along <100> Si-substrate direction

For an accurate thickness determination of the HfO_2 bulk it is necessary to measure the total O counts with minimal error, which includes counts from HfO_2 bulk as well as SiO_2 IL. According to channeling theory, the backscattered energy spectrum is considerably different for an aligned crystal compared to amorphous/nanocrystalline material. The scattering yield of an aligned spectrum is reduced by almost two orders of

magnitude with a peak at a position corresponding to scattering from surface atoms. This is due to the shadow cone formed and channeling, which results in the incoming ^{4}He ions interacting with primarily the surface atoms; and atoms deeper into the crystal escape direct beam interactions due to this shadowing effect in a crystalline lattice. The backscattering yield from an amorphous/nanocrystalline layer coincides with a random spectrum. As the ion beam traverses deeper into an aligned crystalline substrate the yield is considerably reduced, but is still higher than a perfectly crystalline lattice [4, 6]. This is due to multiple scattering that occurs as the beam traverses the amorphous HfO_2/SiO_2 layer. Multiple scattering refers to the small angle scattering events that result in angular directions outside the critical angle (ψ) for a specific thickness of the nanocrystalline material [4, 6]. This latter phenomenon is important to consider as we relate these events to the increase in the intrinsic Si surface peak in the channeling analysis.

Channeling analysis was performed with He^+ at 1.8 MeV on all the samples along the <100> channel direction with backscattered counts collected using both annular as well as grazing angle detectors. Ion channeling was performed by aligning the sample for axial channeling along the normal <100> crystal direction, after mounting the sample on a two axis goniometer. Figure 5.1 shows the plot of annular random and channeling spectrum for the 3 nm HfO_2/1 nm SiO_2 sample. Using equation 5.2 and a known standard, the areal density of Hf atoms was calculated for the four samples (Table 5.4). The area under this peak is independent of the orientation of the sample due to its nanocrystalline nature as shown in Figure 5.1 for the 3 nm HfO_2/1 nm SiO_2 sample. In channeling analyses, the error values are minimized due to a more pronounced O peak observed, which assists in performing better background subtraction owing to a reduction

in the Si background counts as evident from Figure 5.1.

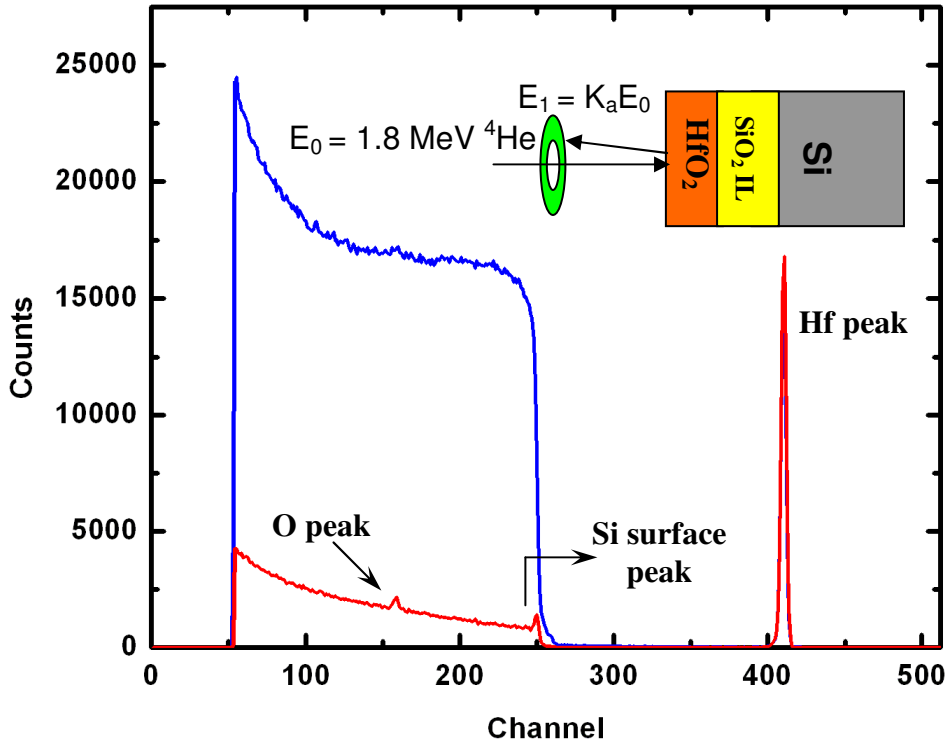

Figure 5.1. Rutherford Backscattering (RBS) spectrum of a 3 nm HfO_2/1 nm SiO_2 layered dielectric stack in a random (blue curve) and along a <100> channeling (red curve) direction. It is important to notice that the O peak which is not as conspicuous in the random is much more evident in a channeled spectrum thereby reducing the background subtraction error for accurate estimation of O counts.

The scattering minimum yield ($\chi_{\min}$) measured for the crystalline silicon was used as a figure of merit to understand the degree of channeling, which is given by [4, 6]

$$\chi_{\min_{<100>}} = \frac{Yield_{<100>channel}}{Yield_{random}} \tag{5.3}$$

where $Yield_{<100>channel}$ refers to the backscattered counts for a given set of channel numbers (energy scale) collected in a <100> channeling direction and $Yield_{random}$ is the counts in a random direction for the same set of channel numbers. The $\chi_{\min}$ with statistical errors along the <100> channel for all the samples in the annular geometry is as

shown in Table 5.3. The increased χ_{min} as compared to single crystal silicon (typically ~ 4 %) is due to multiple scattering from nanocrystalline HfO_2 and the amorphous SiO_2 layer as discussed previously. Note that χ_{min} increases with increase in overall film thickness (bulk + IL).

Table 5.3. Channeling minimum yield % χ_{min} for all the four samples measured along the <100> channel dierction using an annular detector.

	t_{HfO_2/SiO_2}	% χ_{min} (180°- Annular)
Sample 1	3 nm/1.1 nm	6.11 ± 0.04
Sample 2	7.5 nm/1.1 nm	10.62 ± 0.06
Sample 3	3 nm/2 nm	6.95 ± 0.05
Sample 4	7.5 nm/3 nm	12.36 ± 0.06

Table 5.4 shows the concentration of Hf in at/cm^2 with statistical errors and can be compared to the Hf expected for the deposition recipe used. The total O concentration after background subtraction is shown in Table 5.5 with statistical errors. The expected values for total O according to the CMOS fabrication recipe are also given. Assuming a perfect stoichiometric 1:2 ratio for the Hf:O, the corresponding oxygen remaining in at/cm^2 is as shown in Table 5.6 with the error propagation taken into consideration. The remaining oxygen was presumably the contribution from the SiO_2 IL with the expected contribution for the O in the SiO_2 IL shown in the adjoining column assuming a perfect stoichiometric SiO_2. We report an exceptional agreement in these numbers with the expected values including the respective errors being very close to the calculated values.

We hereby confirm the values of the bulk HfO_2 and the SiO_2 IL as estimated from the growth parameters to be largely consistent with the calculated values.

Table 5.4. The measured and expected concentration of Hf in at/cm^2 tabulated for the annular detector geometry for the all the four samples studied with the statistical errors

	t_{HfO_2/SiO_2}	Hf expected (10^{15} at/cm^2)	Hf measured (10^{15} at/cm^2)
			180°
Sample 1	3 nm/1.1 nm	8.24	8.29 ± 0.03
Sample 2	7.5 nm/1.1 nm	20.6	20.20 ± 0.05
Sample 3	3 nm/2 nm	8.24	8.10 ± 0.03
Sample 4	7.5 nm/3 nm	20.6	20.72 ± 0.05

Table 5.5. The measured and expected concentration of total O in at/cm^2 (including HfO_2 and SiO_2 IL) tabulated for the annular detector geometry for the all the four samples studied with the statistical errors

	t_{HfO_2/SiO_2}	O_{total} expected (10^{15} at/cm^2)	O_{total} measured (10^{15} at/cm^2)
			180°
Sample 1	3 nm/1.1 nm	21.28	21.90 ± 2.01
Sample 2	7.5 nm/1.1 nm	46.0	45.50 ± 2.42
Sample 3	3 nm/2 nm	25.28	24.23 ± 2.32
Sample 4	7.5 nm/3 nm	54.4	55.08 ± 2.92

Table 5.6. The measured and expected concentration of remaining O in at/cm^2 after subtracting the HfO_2 contribution assuming a 1:2 ratio for Hf to O tabulated for the annular detector geometry for the all the four samples studied with the statistical errors

	t_{HfO_2/SiO_2}	Interlayer O expected (10^{15} at/cm^2)	Interlayer O measured (10^{15} at/cm^2)
			180°
Sample 1	3 nm/1.1 nm	4.84	5.32 ± 2.01
Sample 2	7.5 nm/1.1 nm	4.84	5.10 ± 2.42
Sample 3	3 nm/2 nm	8.80	8.02 ± 2.32
Sample 4	7.5 nm/3 nm	13.2	13.6 ± 2.92

Further investigations were performed to estimate the silicon contribution for this interlayer as extracted from the Si surface peak. Studies performed by Bongiorno *et al.* [7-9] to determine the intrinsic Si surface peak in a SiO_2/Si configuration along a specific channeling direction at various energies suggest that the total Si surface peak yield is given by

$$Y_{surface-peak} = Y_{intrinsic-Si} + Y_{reconstructed-Si} \quad (5.4)$$

Earlier studies by Feldman *et al.* [10] and Stensgaard *et al.* [11] about the Si surface peaks combined with the recent studies from Bongiorno *et al.* [9] predict the intrinsic Si surface peak at 1.8 MeV ^{4}He along a <100> channeling direction to be ~ 1.1 x 10^{16} at/cm^2. Previous studies also mention the presence of reconstructed Si which accounts for ~ 3 ML (monolayers) i.e. ~ 2.04 x 10^{15} at/cm^2 of Si contributing to the total silicon surface peak yield at these energies. This contribution remains relatively constant

irrespective of the SiO_2 layer thickness [7, 9]. Taking into account these numbers and comparing them with the numbers obtained from the surface peaks in our analysis of gate oxides reveal the presence of excess Si contribution in the measured Si surface peaks. These were calculated using the equation below [7, 9]

$$Y_{excess} = Y_{surface-peak} - (Y_{SiO_2-IL} + Y_{intrinsic-Si} + Y_{reconstructed-Si}) \quad (5.5)$$

As a first approximation the Si yield for SiO_2 IL was estimated from the remainder of the O yield as shown in Table 5.6 assuming a perfect stoichiometric SiO_2. The intrinsic and the reconstructed values remain the same as mentioned earlier. After accounting for these contributions using equation 5.5 we observe excess Si contribution in the surface peak as mentioned in Table 5.7.

Table 5.7. The measured concentration in at/cm^2 from the Si surface peak of total Si, Si in SiO_2 assuming a 1:2 Si to O ratio from the 'O remaining' numbers in Table 5.6, and excess Si deduced from equation 5.5 tabulated here for annular geometry for the all the four samples studied with the statistical errors as mentioned in the table. The background subtraction, which may involve a significant amount of error was performed as pictorially represented in Figure 5.2 and 5.3.

	t_{HfO_2/SiO_2}	Si surface peak (10^{15} at/cm^2) at 180°	Si in SiO_2 (10^{15} at/cm^2) at 180°	excess Si (10^{15} at/cm^2) at 180°
Sample 1	3 nm/1.1 nm	18 ± 0.03	2.66 ± 1.0	5.5
Sample 2	7.5 nm/1.1 nm	29 ± 0.03	2.55 ± 1.2	16.04
Sample 3	3 nm/2 nm	23 ± 0.03	4.01 ± 1.1	10.77
Sample 4	7.5 nm/3 nm	32 ± 0.04	6.8 ± 1.5	19.59

One probable reason for the increased Si contribution, as already mentioned, is owing to the enhanced multiple scattering in the HfO_2 bulk. We also speculate the presence of some strain at the HfO_2/SiO_2 interface or in the SiO_2 IL due to the scaling of the excess Si with the HfO_2 bulk grown on top, which may cause an increase in the surface peak yield. There may be additional errors in the values for the reconstructed-Si owing to great deal of intermixing that occurs in the SiO_2 IL with the deposition of a bulk HfO_2 layer on the top of the thermal oxide. One of the largest sources of error apart from the statistical error lies in the background subtraction for estimating the total Si yield in the Si surface peak [11]. Figures 5.2 and 5.3 show the method adopted for subtracting the background from the Si surface peak for determining the amount of 'excess Si'. All these sources of errors

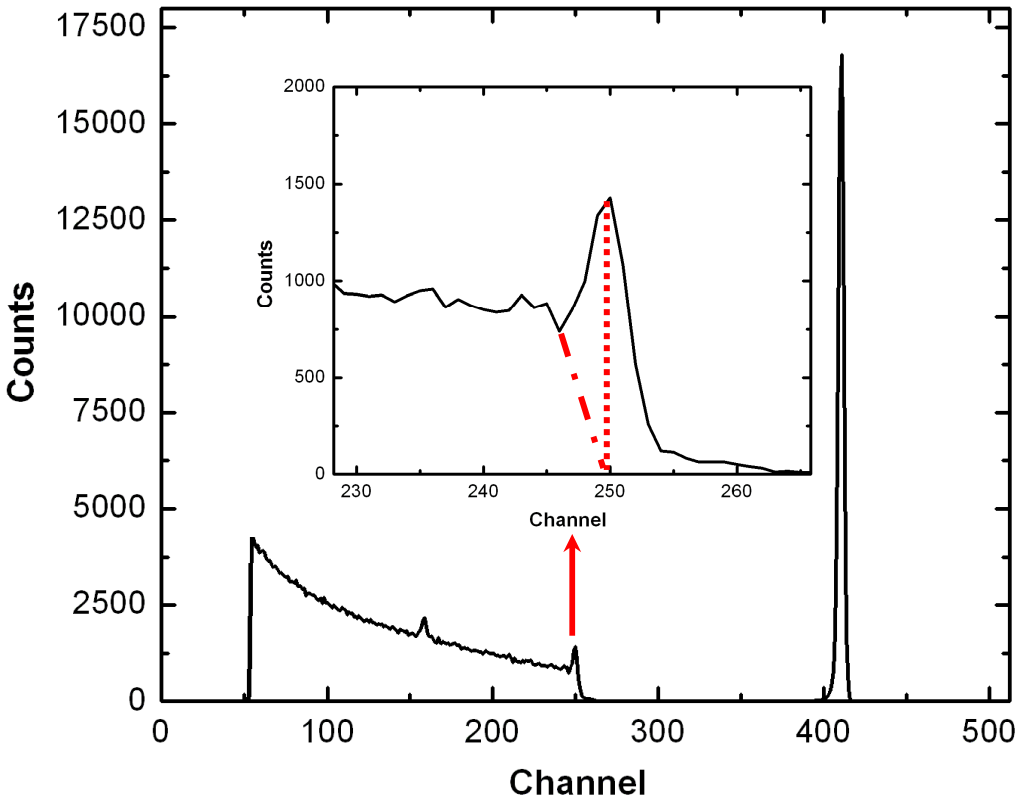

Figure 5.2. Annular RBS spectrum of a 3 nm HfO_2/1 nm SiO_2 layered dielectric stack in a <100> channeling direction. Inset shows the schematic of the background subtraction done to estimate the yield of Si surface peak.

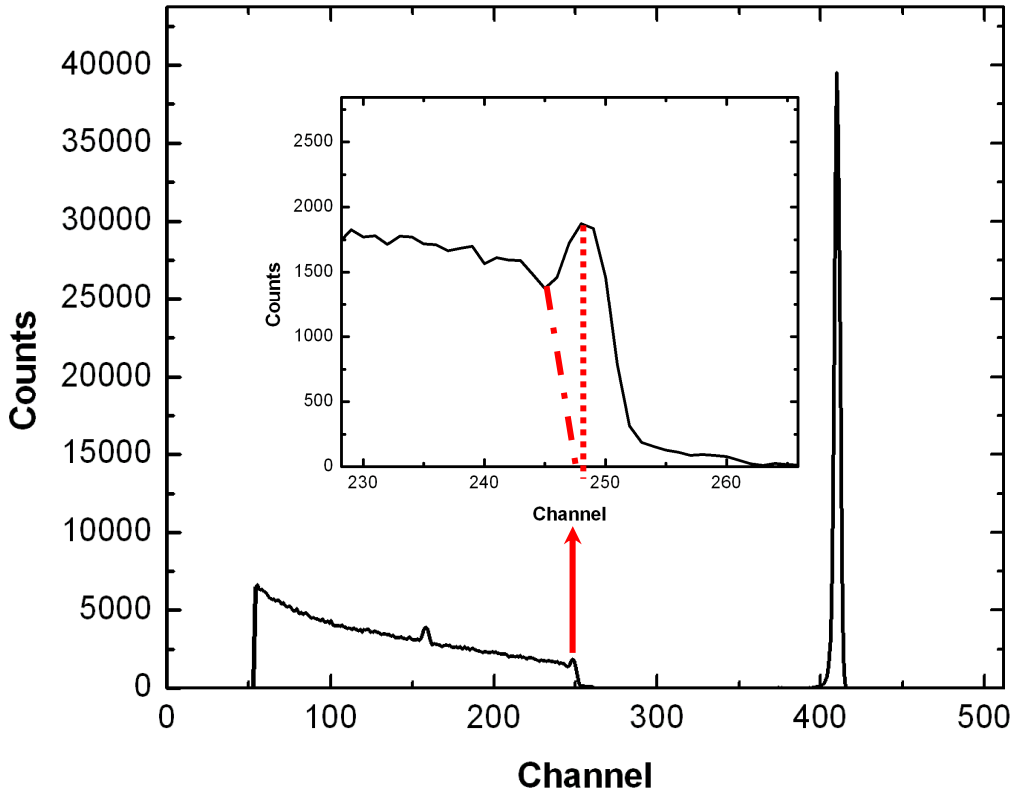

Figure 5.3. Annular RBS spectrum of a 7.5 nm HfO_2/1 nm SiO_2 layered dielectric stack in a <100> channeling direction. Inset shows the increased yield of Si surface peak due to multiple scattering and possible strain effects in the SiO_x IL.

as discussed above can overestimate the excess Si yield in these samples.

To summarize, RBS in combination with channeling was efficiently used to verify the grown sample structures as to gate oxide and IL thicknesses. It is important to know the amount and quality of material exposed to x-ray irradiations for studying its charge trapping characteristics. Furthermore, the issues of interface mixing as a function of increased HfO_2 bulk thickness adds to the complexity in understanding the charge trapping and hence it is necessary to investigate the thickness and quality of each gate dielectric stack to identify the possible reasons for the differences in the total dose response. This characterization technique has been a key tool in achieving these goals for

investigating the device response as discussed in Chapter VI and Chapter VII.

5.3.2c. X-Ray Reflectometry (XRR)

X-ray Reflectometry (XRR) is a noninvasive way of monitoring the thickness of thin film structures. This technique can be applied equally well to amorphous, crystalline and polycrystalline structures [12]. It relies on the difference in the electron densities between the substrate and the thin film. Specular x-ray reflectance is used to characterize the electron density profile. This technique is very useful for HfO_2 since it has a much higher electron density than the Si substrate underneath. It is however difficult to measure the interlayer thickness as there is insufficient electron density variation between SiO_2 and the Si substrate. Hence we report thickness results only for bulk HfO_2 using this technique.

The XRR measurements were taken using a BedeMetrix^{TM}-L tool [13]. A monochromatic x-ray beam was set at a grazing angle with the HfO_2/SiO_2 layers. The x-rays reflect from film as well as the interlayer and forms interference fringes (Kiessig fringes) from which the film thickness, density and roughness can be calculated. The angle at which the sudden drop in the intensity occurs is known as the critical angle and is proportional to the electron density. The number of fringes in the reflectivity profile is a function of the thickness of the film, the denser the profile (the smaller the fringe spacing), thicker the film.

XRR for our samples was measured using a 250 μm incident beam and detector slits, scanning θ-2θ up to ~ 4° with the specular reflection captured. This XRR data is further autofit using a simulation model taken from the Bede REFS program with

accurate data fitting and parameter optimization [14]. This work uses a single layer model to fit the targeted 3 nm HfO_2 and a two-layer model with denser HfO_2 on top to fit the targeted 7.5 nm HfO_2 samples. Table 5.8 summarizes the modeled results.

Table 5.8. XRR results derived from a simulation model used to fit the measured data for estimating the HfO_2 bulk thickness for all the samples under study. The 3 nm HfO_2 layer was modeled using a single layer model whereas the 7.5 nm HfO_2 samples were modeled using a two layer model as shown in the table

Sample	Target High-κ film thickness [nm]	HfO_2 thickness [nm]	HfO_2 density [g/cm^3]	HfO_2 roughness [nm]
1	3.0	2.93	13.9	0.43
2	7.5	1.05	14.3	0.45
		6.05	10.2	0.89
3	3.0	2.75	15.4	0.28
4	7.5	0.88	16.9	0.5
		6.28	11.0	0.76

The thicknesses of the bulk HfO_2 including the film roughness as shown in the table are in close agreement with the HfO_2 thicknesses measured using RBS/Channeling studies. There is a significant density variation observed in these measurements as compared to the ones mentioned in Ref. [15]. These are potentially due to the following reasons. The tools used for the XRR measurements for the results mentioned in Ref. [15] are different from the ones used for these measurements. Hence an instrumentation

variation with some offset in the measuring parameters can be expected. Additionally, the samples in the Ref. [15] were fabricated using $HfCl_4$ as the precursor, whereas the samples in these measurements were fabricated using the method as described in Ref. [16]. Furthermore, one of the most significant contributions to the error comes from the difficulty in measuring accurate densities for extremely thin films using XRR technique. Careful beam alignment is necessary as the measurements are very sensitive to the alignment. Improper beam position can result in a substantial error (~ ±10%) in the density especially in the case of measurement of extremely thin films. However for films with low roughness, this technique provides an accurate estimation of oxide thickness.

5.3.2d. Medium Energy Ion Scattering (MEIS)

The MEIS measurements were performed at the Laboratory for Surface Modification at Rutgers University as a part of the materials study for these high-k samples. MEIS is another powerful technique used in surface science to study the structural and compositional properties of surfaces and thin films. It is a high resolution, low energy version of the RBS technique. In this technique, the fundaments of beam interactions between the incident ion and the target nuclei remain the same as RBS as described in section 5.3.2a. Similar to the RBS, energy analysis of the exiting ions leads to the distinction of various masses. Light ions (usually p^+ and He^+) with energy of 40-400 keV are incident along a channeling direction. Structural and compositional information is gathered from the energy and angle resolved detection of the backscattered ions.

In our experiment, 130 keV H^+ ions from a 400 keV High Voltage Engineering

ion implanter were used to conduct the MEIS analysis. After surface scattering, ions from the horizontal scattering plane were collected into a Toroidal Electrostatic Analyzer (TEA). Opposite voltage polarities were applied on the deflecting plates to drive the ions towards a Position Sensitive Detector (PSD). Focusing of the TEA was performed to focus ions with the same energy leaving the surface from the same spot but along different directions as well as ions exiting along horizontal parallel directions to arrive at the same spot on the PSD. Micro-channel plates in the PSD enable the creation and amplification of an electron cloud resulting from ions hitting these plates. This electron cloud further impinges on the multi-anode collector, which computes the angle and energy of the incident ions from the relative amounts of charge collected.

Figures 5.4 and 5.5 show the MEIS spectra collected for two of the four samples (3 nm HfO_2/1 nm SiO_2, and 7.5 nm HfO_2/1 nm SiO_2) under scrutiny in this chapter for stoichiometry and thickness verification. The black lines indicate the actual spectrum with the peaks for the lower Z elements (Si and O) zoomed up (10 x) for easy identification of the peaks. The red curve riding over the actual spectrum is a simulation, which was fit to a layered distribution of hafnium oxide and hafnium silicate throughout the dielectric stack as shown in the figure adjacent to the actual spectrum for each of the sample. Table 5.9a and 5.9b show the Hf, O and Si at/cm^2 as calculated from the MEIS fits as shown in Figures 5.4 and 5.5. The expected Hf and O numbers remain the same as the ones mentioned for the RBS results for all the samples.

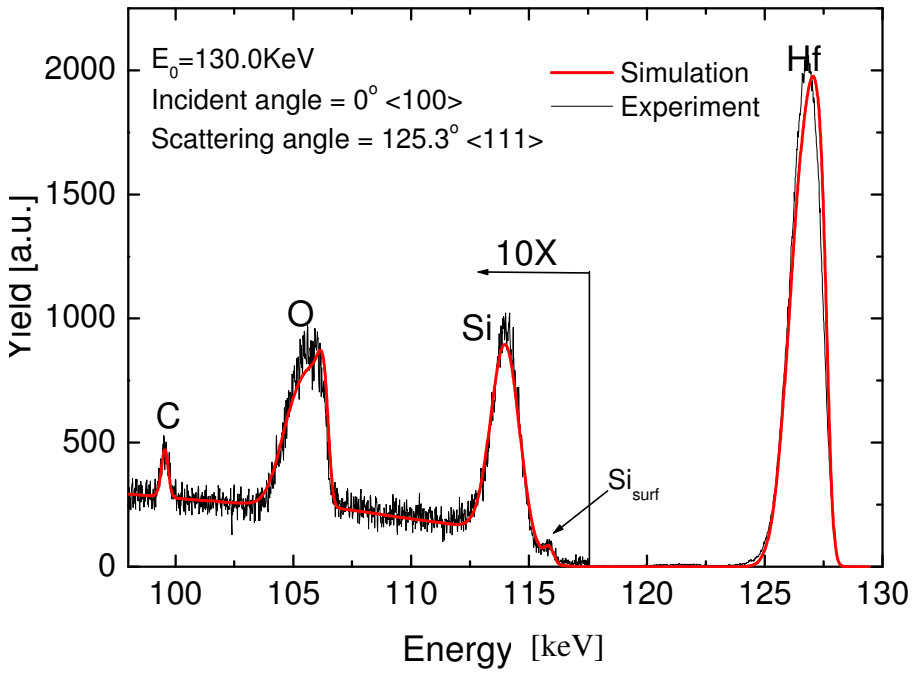

Figure 5.4. MEIS spectrum of a 3 nm HfO_2/1 nm SiO_2 sample with the black curve depicting the actual spectrum. The red curve is a simulation fit to the layered gate stack that best fits the measured spectrum.

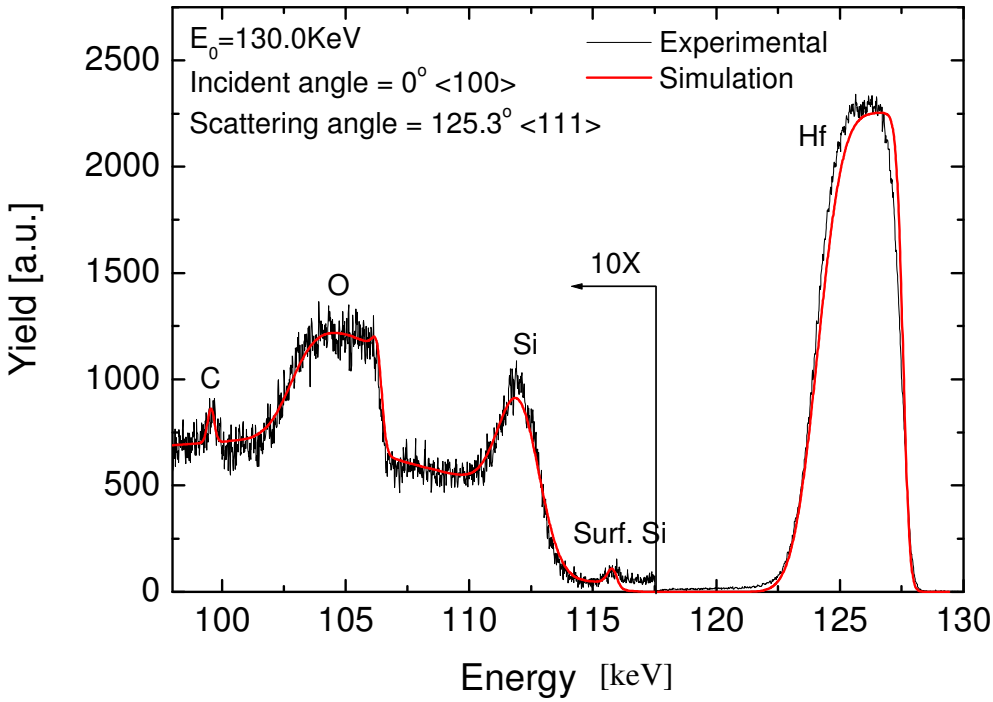

Figure 5.5. MEIS spectrum of a 7.5 nm HfO_2/1 nm SiO_2 sample with the black curve depicting the actual spectrum. The red curve is a simulation fit to the layered gate stack that best fits the measured spectrum.

Table 5.9a. The concentration of Hf, O and Si in at/cm^2 estimated from the simulation fit to the MEIS spectrum for each of the layer in the dielectric stack for the sample with 3 nm HfO_2/1 nm SiO_2

Element	Concentration $\times 10^{15}$ [at/cm^2]
Hf	$\mathbf{0.36(Hf_{0.3}Si_{0.2}O_2)+0.40(Hf_{0.5}Si_{0.05}O_2)+6.90(HfSi_{0.02}O_2)+0.66(Hf_{0.7}Si_2O_2)}$ = 8.32
O	$\mathbf{1.82(Hf_{0.3}Si_{0.2}O_2)+1.61(Hf_{0.5}Si_{0.05}O_2)+13.81(HfSi_{0.02}O_2)+1.90(Hf_{0.7}Si_2O_2)+3.23(SiO_2)}$ = 22.37
Si	$\mathbf{0.18(Hf_{0.3}Si_{0.2}O_2)+0.04(Hf_{0.5}Si_{0.05}O_2)+0.14(HfSi_{0.02}O_2)+1.90(Hf_{0.7}S_2O_2)+1.61(SiO_2)}$ = 3.87

Table 5.9b. The concentration of Hf, O and Si in at/cm^2 estimated from the simulation fit to the MEIS spectrum for each of the layer in the dielectric stack for the sample with 7.5 nm HfO_2/1 nm SiO_2.

Element	Concentration $\times 10^{15}$ [at/cm^2]
Hf	$\mathbf{0.16(Hf_{0.3}Si_{0.2}O_{1.6})+0.41(Hf_{0.5}Si_{0.2}O_{1.6})+ 19.38(HfSi_{0.05}O_{1.6})}$ = 19.95
O	$\mathbf{0.88(Hf_{0.3}Si_{0.2}O_{1.6})+1.32(Hf_{0.5}Si_{0.2}O_{1.6})+ 31.02(HfSi_{0.05}O_{1.6})+3.6(SiO)}$ = 36.82
Si	$\mathbf{0.11(Hf_{0.3}Si_{0.2}O_{1.6})+0.17(Hf_{0.5}Si_{0.2}O_{1.6})+ 0.97(HfSi_{0.05}O_{1.6})+3.6(SiO)}$ = 4.85

The areal density of Hf (at/cm^2) is in very good agreement with the Hf numbers measured using RBS. The O at/cm^2 is in fair agreement as compared to the values measured using RBS. The observed variation may be from some sputtering occurring in the low energy

spectrum during measurements and/or non-uniformity in the oxide layer thickness. The Si surface peaks in these spectra are indicative of Si out-diffusion into the bulk oxide layer towards the surface of bulk HfO_2. It is important to note that the Si at/cm^2 mentioned in these tables are for total Si that is distributed throughout the whole of the layered dielectric stack. It does not include the contribution from the reconstructed and intrinsic Si surface peak as discussed in RBS measurements. The MEIS results also confirm the intermixing in the interlayer and the O out-diffusion into the bulk of the HfO_2 thereby forming a sub-stoichiometric SiO_x interlayer. These results are consistent with previous results, which discuss the depletion of O from the SiO_2 IL during the growth of a thicker HfO_2. These results additionally indicate increase in the O vacancies in the SiO_x interlayer in thicker HfO_2 samples with the possibility of the presence of defects that may exist owing to the presence of Si diffused from the SiO_2 IL underneath in the HfO_2 layer.

5.3.3 Electrical characterization of HfO_2-based MOS capacitors and MOSFETs

Electrical measurements were done using C-V analysis for pre-irradiation characterization [17]. These were done primarily to verify the thicknesses of the bulk and SiO_2 IL before radiation damage experiments were performed. Circular dots of Al gate metal with 0.5 mm diameter were deposited with a shadow mask on bare oxide wafers using thermal evaporation. A Signatone hi-lo frequency C-V station was used to perform the C-V analysis for measuring the accumulation capacitance (C_{ox}). Effective capacitance was modeled as two capacitances in series and the theoretical capacitance was calculated with the values of $\kappa_{HfO_2} \sim 24$ corresponding to pure HfO_2 and $\kappa_{HfSi_xO_y} \sim 7$ for hafnium silicates with $\kappa_{SiO_2} \sim 3.9$ for SiO_2 [1]. Different values for κ were considered, as the real

value of κ is unknown owing to the silicate formation in the bulk of the dielectric as shown in the histogram in Figure 5.6. MEIS studies indicate the intermixing in these

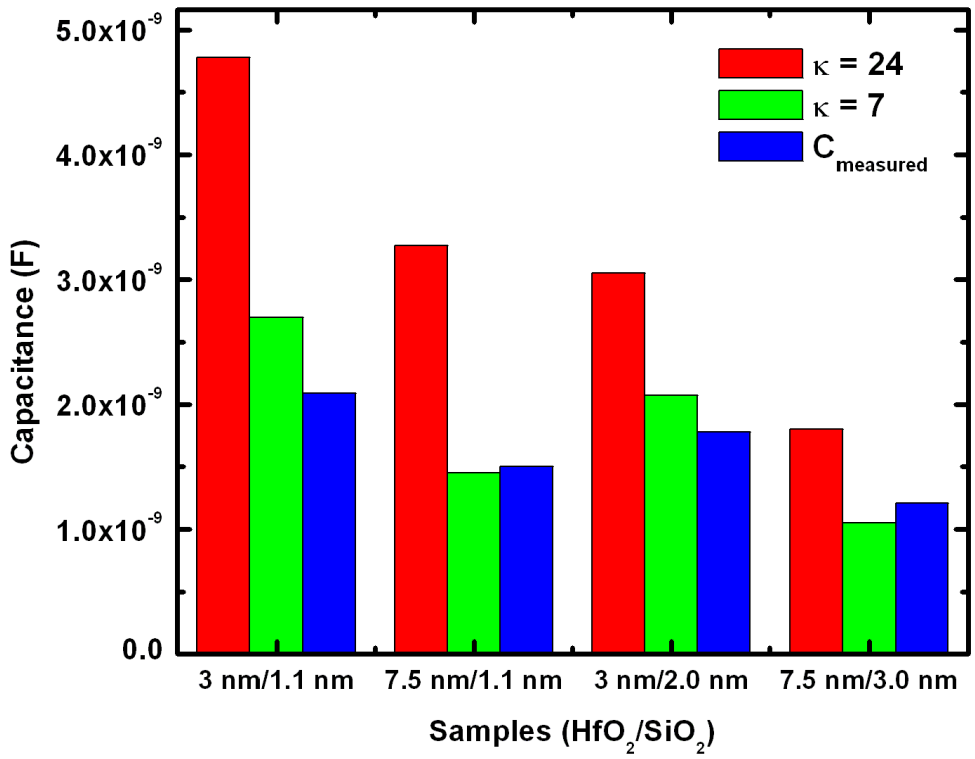

Figure 5.6. Histogram of the maximum capacitance (C_{ox}) that can be achieved modeled as two capacitances in series for $C_{HfSixOy}$ and C_{SiO2} with different dielectric constant values (κ ~ 24, and 7) due to Si intermixing into the bulk of HfO_2 as compared to the actual C_{ox} measured on the four different samples involved in this study.

samples and the κ values for comparison were taken from previous studies of variation in the bulk HfO_2 dielectric constant as a function of Si concentration [18, 19]. The lowest achievable capacitance value is mentioned by considering an admixture of hafnium silicate and SiO_2 with about 50 % Si in-diffusion, which is close to the value measured by MEIS for Si in the bulk of the dielectric. This calculated capacitance values were

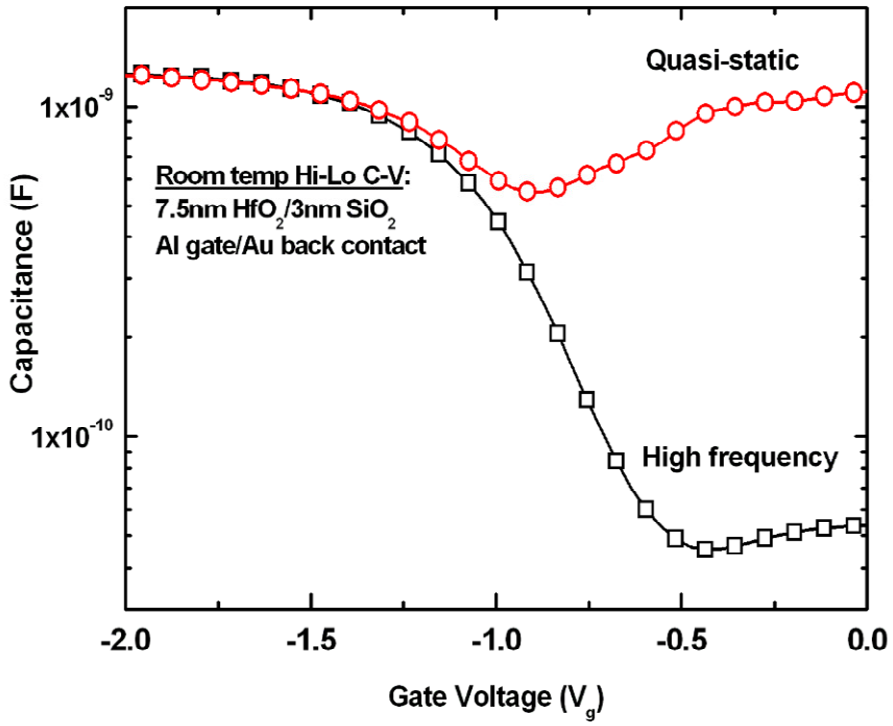

Figure 5.7. 100 kHz room temperature high frequency and quasi-static C-V curves measured for a 7.5 nm HfO_2/3.0 nm SiO_2 MOS capacitor.

compared to the experimentally measured value as shown in Figure 5.6. Figure 5.7 shows a sample Hi-Lo C-V curve measured for the 7.5 nm HfO_2/3 nm SiO_2 IL samples. These results show that the capacitances measured using C-V show a slight variation with the values calculated using theoretical methods as mentioned above. The disagreement might be due to the Si intermixing in the dielectric, which might lead to reduced dielectric constant hence a low measured capacitance (C_{ox}) value as compared to the theory. Previous materials analysis studies performed by several authors on the HfO_2 and ZrO_2 growth on Si reveal the variation in the κ-value as a function of the Hf/Si ratios [18, 20]. Our MEIS results as mentioned previously also strongly support of our C-V results with the evidence of Si uptake into the bulk of the HfO_2 during the growth of the high-κ oxide

as well as during post deposition anneal.

MOSFETs were fabricated at SEMATECH using the same CMOS recipe as the one used for the gate oxide deposition for materials analysis. This was followed by lithography, dopant implantations in the source-drain regions, source-drain dopant activation anneal, interface passivation procedures and a 700 °C post deposition anneal (PDA) in N_2 to fabricate *p* and *n*-MOSFETs with respective well doping on a *p*-type Si substrate. In the following paragraph we briefly describe the *I-V* characterization conducted on these transistors to measure the threshold voltage (V_T) and the sub-threshold characteristics prior to bias stress and radiation dose experiments. All the samples under investigation were drawn to the 65 nm technology node. The results mentioned below are for MOSFETs with a physical gate oxide thickness of ~ 7.5 nm HfO_2/1 nm SiO_2 and W/L of 10 µm/0.25 µm. Routine *I-V* characterization was performed to investigate the device behavior including the drive current and the gate leakage in these MOSFETs. The 3 nm HfO_2/1 nm SiO_2 showed the highest leakage current followed by the 7.5 nm HfO_2/1 nm SiO_2 smaples with the lowest leakage achieved for the 3 nm HfO_2/2 nm SiO_2 transistors at E_{ox} = +3 MV/cm. These leakage currents varied from nanoamperes to picoamperes for the different thicknesses under investigation. The I_{ds}-V_{gs} curves for the 7.5 nm HfO_2 MOSFETs with W/L of 10 µm/0.25 µm are as plotted below. Figures 5.8 and 5.9 are for *n*MOSFETs and *p*MOSFETs respectively with a drain voltage of 100 mV applied for the carrier flow from source to drain (potential gradient) and source and substrate terminals grounded. The off-state I_{ds} is on the order of a few fA as can be seen from the figures. Figures 5.10 and 5.11 show the I_{ds}-V_{ds} characteristics for different gate voltages from V_g = ± 0.8 to ± 2.0 V for the same *n* and *p*MOSFETs

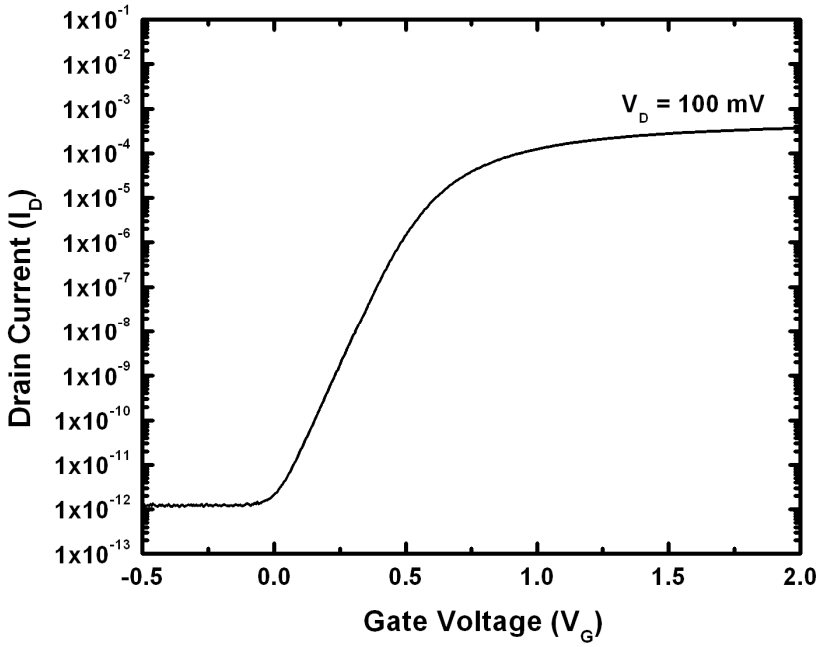

Figure 5.8. Pre-rad I_{ds}-V_{gs} curves for a *n*MOSFET with W/L = 10 µm/0.25 µm measured as a function of V_{ds} = 100 mV. These were measured for *n*MOSFETs with t_{phys} = 7.5 nm HfO_2/1 nm SiO_2.

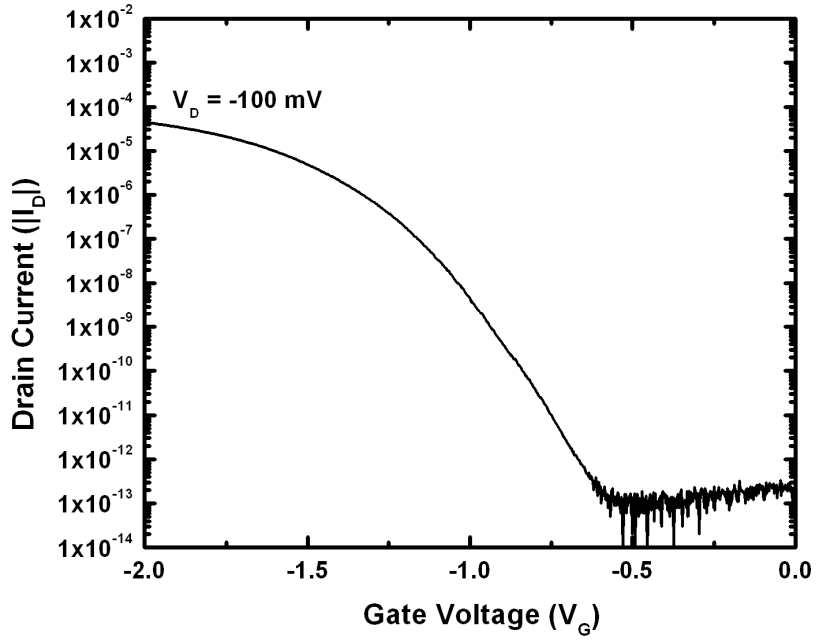

Figure 5.9. Pre-rad I_{ds}-V_{gs} curves for a *p*MOSFET with W/L = 10 µm/0.25 µm measured as a function of V_{ds} = -100 mV. These were measured for *p*MOSFETs with t_{phys} = 7.5 nm HfO_2/1 nm SiO_2.

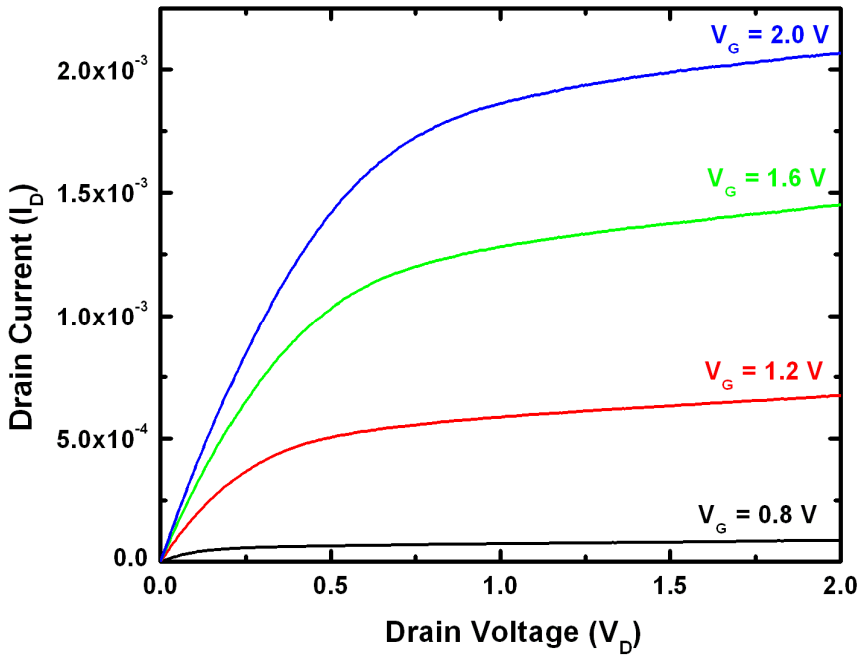

Figure 5.10. Pre-rad I_{ds}-V_{ds} curves for a *n*MOSFET with W/L = 10 µm/0.25 µm measured as a function of different gate voltages (V_g = 0.8 to 2.0 V). These were measured for *n*MOSFETs with t_{phys} = 7.5 nm HfO_2/1 nm SiO_2.

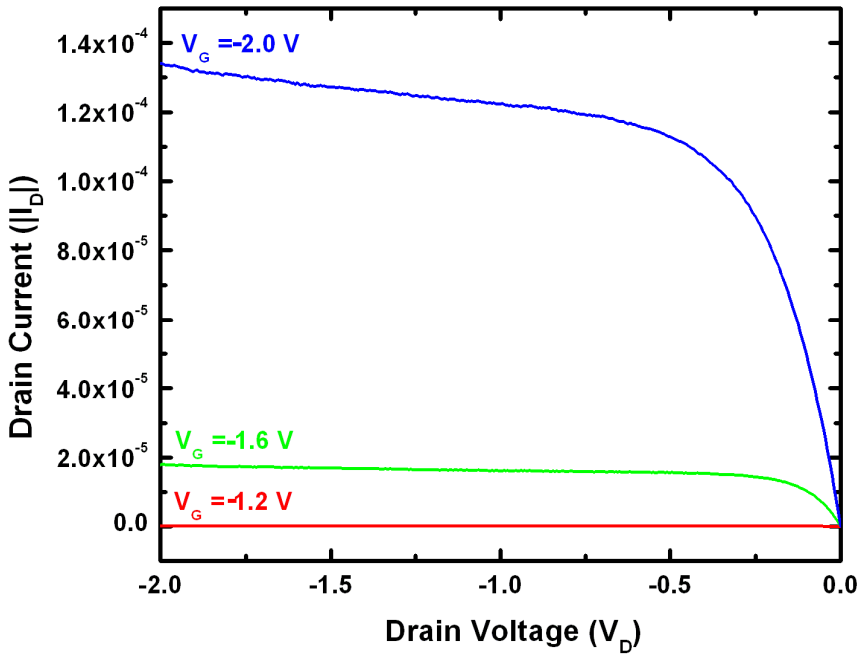

Figure 5.11. Pre-rad I_{ds}-V_{ds} curves for a *p*MOSFET with W/L = 10 µm/0.25 µm measured as a function of different gate voltages (V_g = -1.2 to -2.0 V). These were measured for *p*MOSFETs with t_{phys} = 7.5 nm HfO_2/1 nm SiO_2.

respectively. The source and the substrate currents were also monitored and were found to be on the order of a few pA in these transistors. All these preliminary investigations were performed as a part of the pre-irradiation characterization in these devices with different HfO_2 and SiO_2 IL thicknesses. The selection of the device for radiation experiments was performed by choosing devices with minimal gate leakage and off-state drain current.

5.4 Conclusion

The chapter provides detailed information on the materials and device quality of samples used in the radiation experiment. Intermixing and diffusion issues can change the composition of the dielectric thereby altering its trapping characteristics. Hence it is important to ascertain and verify the thicknesses and composition of the oxide layers in these devices, especially due to the inclusion of the interlayer in the dielectric stack. These results underpin the comparisons made in the future chapters for the observed variation in the radiation response between the different transistor structures.

Acknowledgements

We thank Prof. T. Gustaffson from Rutgers University for engaging in stimulating discussions on the physical characterizations. We also thank W. Augustyniak and Prof. T. Hmelo for all the help and technical expertise provided during the course of the experiments. This work was supported by the Air Force Office of Scientific Research (AFOSR) through the MURI program.

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CHAPTER VI

RADIATION INDUCED CHARGE TRAPPING IN ULTRATHIN HfO_2-BASED MOSFETS

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6.1 Abstract

Radiation induced charge trapping in ultrathin HfO_2-based n-channel MOSFETs is characterized as a function of dielectric thickness and irradiation bias following exposure to 10 keV X-rays and/or constant voltage stress. Positive and negative oxide-

trap charges are observed, depending on irradiation and bias stress conditions. No significant interface-trap buildup is found in these devices under these irradiation and stress conditions. Enhanced oxide-charge trapping occurs in some cases for simultaneous application of constant voltage stress and irradiation, relative to either type of stress applied separately. Room temperature annealing at positive bias after irradiation of transistors with thicker gate dielectric films leads to positive oxide-trapped charge annihilation and/or neutralization in these devices, and net electron trapping. The oxide thickness dependence of the radiation response confirms the extreme radiation tolerance of thin HfO_2 dielectric layers of relevance to device applications, and suggests that hole traps in the thicker layers are located in the bulk of the dielectric. A revised methodology is developed to estimate the net effective charge trapping efficiency, f_{ot}, for high-κ dielectric films. As a result, estimates of f_{ot} for Hf silicate capacitors and Al_2O_3 transistors in previous work are reduced by up to 18 %.

6.2 Introduction

Gate dielectric scaling allows for continuing increases in circuit speed and packing density for CMOS integrated circuits (ICs) [1]. To date, traditional silicon dioxide (SiO_2) and its nitrided alternatives have made this scaling possible at the expense of increases in the off-state leakage current and resulting increases in the power dissipation [2]. To overcome these limits, alternative gate dielectrics are being widely studied and are on the verge of commercial adoption. They allow a physically thicker dielectric layer to be used, while providing capacitance equivalent to SiO_2. Hafnium oxide (HfO_2), with relative dielectric constant ~15 to 26, depending on processing and

alloying techniques, is a leading candidate to replace SiO_2 in modern CMOS technologies [3]. While significant performance improvement was achieved recently [4], it is important to establish increased reliability in these materials and devices [5]-[9]. Significant reliability concerns include negative bias temperature instability (NBTI), time dependent dielectric breakdown (TDDB) [10],[11], carrier injection [12]-[16], and radiation induced charge trapping [17].

Extensive studies of radiation damage on SiO_2-based MOSFETs have been reported [18],[19]; however, similar studies on HfO_2-based devices are somewhat limited. Early work on HfO_2 and/or Hf silicate-based devices concentrated on studying the radiation response of thicker dielectrics, primarily using capacitors [17],[20],[21]. In an ionizing radiation environment, hole trapping is usually the dominant source of radiation-induced oxide-trap charge in SiO_2-based devices, with some electron trapping possible at high radiation doses and/or for extreme electrical stressing conditions, due to low capture-cross section neutral electron traps in the oxides [22],[23]. In contrast, recent work demonstrates the existence of a significant number of bulk electron traps in HfO_2 with much higher capture cross sections than in SiO_2, which can affect the charge trapping significantly [24]-[29]. This trapping can depend strongly on device processing and dielectric layer thickness [21],[26]. Hole trapping studies on capacitors, mostly on thicker hafnium oxides, suggest the presence of processing induced defects both in the SiO_x interlayer and in the bulk of the hafnium oxide [30]-[35].

In this work we investigate radiation-induced charge trapping and trapped charge compensation and/or annihilation effects during post-irradiation annealing for HfO_2-based MOSFETs (< 2.5 nm Effective Oxide Thickness - EOT) with varying bulk HfO_2

thicknesses (3 nm and 7.5 nm). The combined effects of radiation exposure and trapped charge injection during and after irradiation are found to be extremely strong functions of bias, with charge injection during electrical stress either adding to or offsetting the radiation-induced charge trapping, depending on the detailed exposure and injection conditions. Ultrathin HfO_2 gate dielectrics are found to be quite radiation tolerant, and more resistant to charge injection for typical operating bias conditions than thicker dielectrics. These results are encouraging for future applications of ultrathin HfO_2 in radiation environments. In addition, we suggest modifications of a previous expression developed by Felix *et al*. [20] to estimate the charge trapping efficiency of high-κ dielectric layers, and provide significant revisions to literature estimates of trapping efficiencies for Hf silicate and Al_2O_3.

6.3 Experimental Details

TiN/HfO_2 gate stack *n*MOSFETs were fabricated on Si (100) 200 mm wafers using a standard CMOS transistor process flow, which includes a 1000 °C/10 s dopant activation. The HfO_2 dielectric was deposited on top of a chemical oxide (~ 1 nm) using atomic layer deposition chemistry, TEMA (tetrakis ethyl methyl amino) Hf+O_3, followed by a post-deposition anneal in N_2. The transistors examined in this work were fully processed standard high-κ MOSFETs fabricated in a 65 nm technology. The transistors under investigation had a width to length ratio (*W/L*) of 10 μm/0.25 μm. Figure 6.1 shows the cross-section of a standard *n*MOSFET used in these experiments. Capacitance-voltage (*C-V*) measurements were performed on capacitors on the same die as the transistors to enable accurate measurement of the EOTs. The SiO_x interlayer (IL)

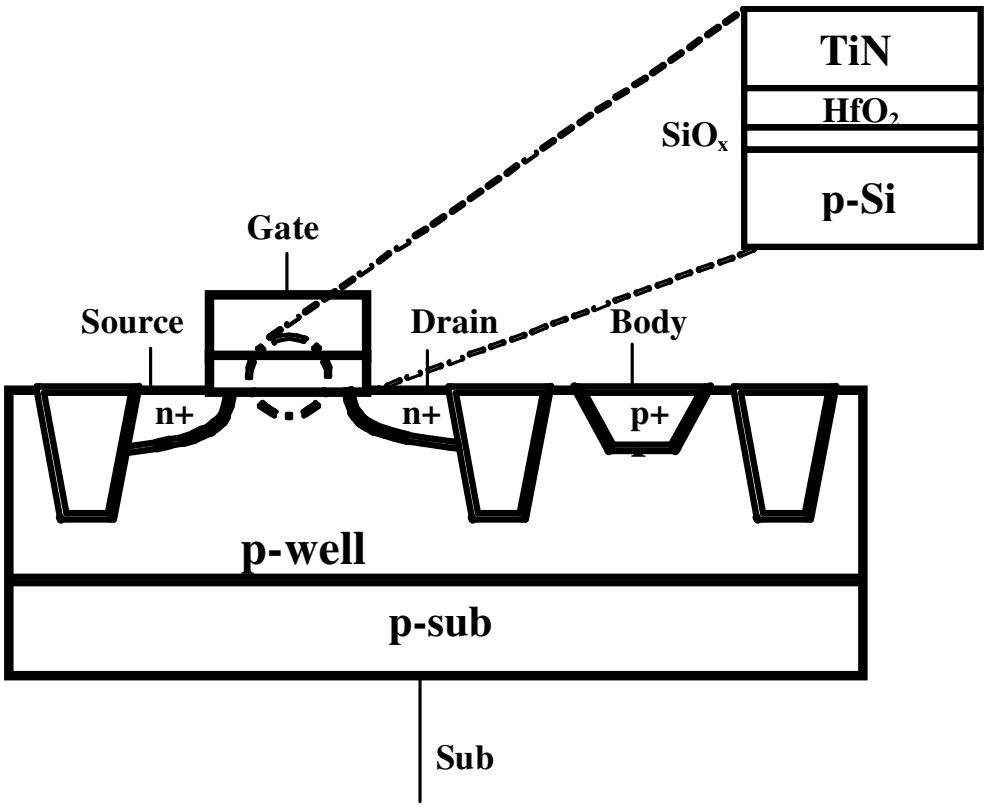

Figure 6.1. Cross-section of the nMOSFET examined in this work. The inset shows a detailed view of the high-κ gate stack with a SiO_x interlayer.

thickness as confirmed from Transmission Electron Microscopy (TEM) was ~ 1 nm. The EOTs of the gate stacks with t_{phys} = 7.5 nm and t_{phys} = 3.0 nm physical high-κ thicknesses were measured to be 2.3 nm and 1.5 nm, respectively.

The devices were exposed to 10 keV X-rays in an ARACOR irradiator under different gate bias conditions (negative, positive, and zero bias) with the other three terminals grounded. Die-level samples were irradiated to a cumulative dose of 10 Mrad(SiO_2) at a dose rate of 31.5 krad(SiO_2)/min, with bias applied by probe contacts that were located so as not to shadow the beam. Current-voltage (*I-V*) characteristics were measured using an Agilent 4156 semiconductor parameter analyzer. All biased

irradiations, voltage stresses, and electrical characterizations were done in-situ in the ARACOR system to minimize experimental sources of error due to measurement delays and probe contact. Standard threshold voltage shifts, subthreshold current-voltage (*I*-V) curves, and leakage current values were measured after each step in X-ray dose. Constant voltage stress (CVS) studies were performed on time scales comparable to those required for the 10 Mrad(SiO_2) irradiations. These tests were performed to separate the contributions of bias-induced charge trapping/creation [36] in these oxides from radiation-induced shifts. There were no significant changes in the subthreshold *I-V* curve stretchout for the irradiation or stress results reported here, as illustrated below. Thus, no significant irradiation or stress induced interface trap buildup is observed in these devices [37],[38]. This is not unusual for HfO_2 [17],[21],[25], although significant interface-trap buildup has been observed in other types of devices processed differently [39],[40]. Electric fields (E_{ox}) were corrected for gate (TiN)-to-silicon work function; gate biases of +2 V/-2 V for 7.5 nm devices correspond to E_{ox} values of ~ 2.7 MV/cm and –2.0 MV/cm, and gate biases of +1 V/-1 V for 3 nm devices are equivalent to E_{ox} values of ~ 3 MV/cm and -1.9 MV/cm, respectively.

6.4 Results and Discussion

6.4.1 Pre-irradiation measurements

Pre-irradiation I_{ds}-V_{gs} curves were measured at V_{ds} = 0.1 V; standard linear threshold voltage V_T measurements were performed. The pre-irradiation V_T values were ~ 0.75 V and ~ 0.45 V for the thicker and the thinner oxides, respectively. Gate leakage currents measured on the transistors were on the order of ~ 1 pA for the t_{phys} = 7.5 nm and

~ 30 nA for the t_{phys} = 3.0 nm oxide samples at V_{gs} = +1 V; these levels are consistent with expectations for these material layer thicknesses [2]-[12].

6.4.2 Total dose results for 7.5 nm and 3.0 nm oxides

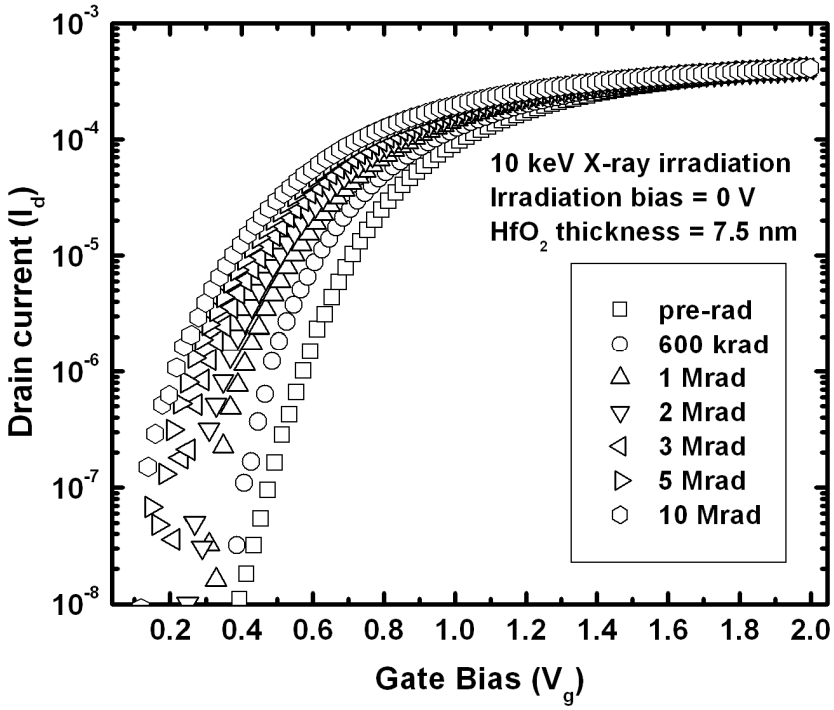

Figure 6.2a. I-V characteristics as a function of x-ray dose at 0 V irradiation bias for a dielectric thickness of 7.5 nm.

Figures 6.2a and 6.2b show I_{ds}-V_{gs} curves to a total dose of 10 Mrad(SiO_2) for devices with 7.5 nm and 3 nm oxides, irradiated at 0 V gate bias. The 7.5 nm sample in Figure 6.2a exhibits a threshold voltage shift (ΔV_T) of –0.35 V at 10 Mrad(SiO_2). This corresponds to a net oxide-trap charge density projected to the interface, ΔN_{ot}, of ~ 3.2 x 10^{12} cm^{-2} [37],[38]. The midgap technique of Winokur and McWhorter was used to separate the contributions of interface and oxide trap charge from the *I-V* curves [37],[38]. The dominant contribution to the V_T shifts (ΔV_T) was due to oxide trap charge

(ΔV_{ot}), with only minimal contribution from the interface traps (ΔV_{it}) [37],[38] in Figure 6.2a. The radiation-induced shifts for the thinner sample in Figure 6.2b were much

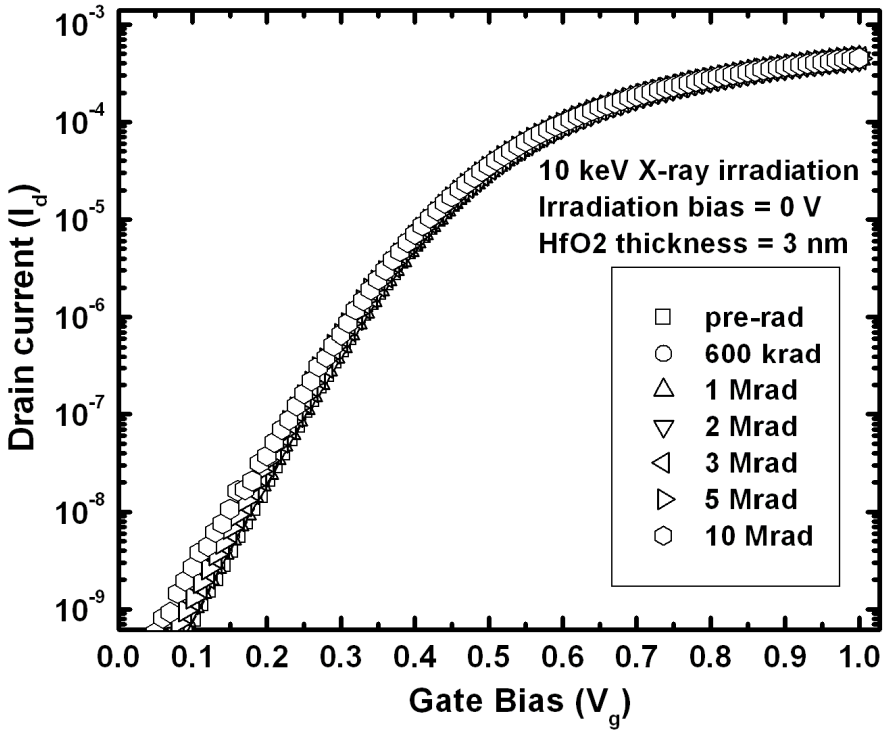

Figure 6.2b. I-V characteristics as a function of x-ray dose at 0 V irradiation bias for a dielectric thickness of 3.0 nm.

smaller than for the thicker oxides, consistent with the reduction in oxide-trap charge trapping during irradiation of ultrathin SiO_2 of equivalent physical thickness [18],[20]. Figures 6.3 and 6.4 summarize the zero, negative, and positive bias radiation-induced threshold voltage shifts for the 7.5 nm and the 3 nm gate oxides, respectively. The charge trapping in the 7.5 nm devices in Figure 6.3 is much greater than in the 3 nm samples in Figure 6.4 in all cases; the 3 nm devices are quite radiation tolerant, showing less than 25 mV shift for all doses and bias conditions. As discussed below, the 3 nm devices were

stable against applied-bias induced charge trapping on the time frames of the radiation

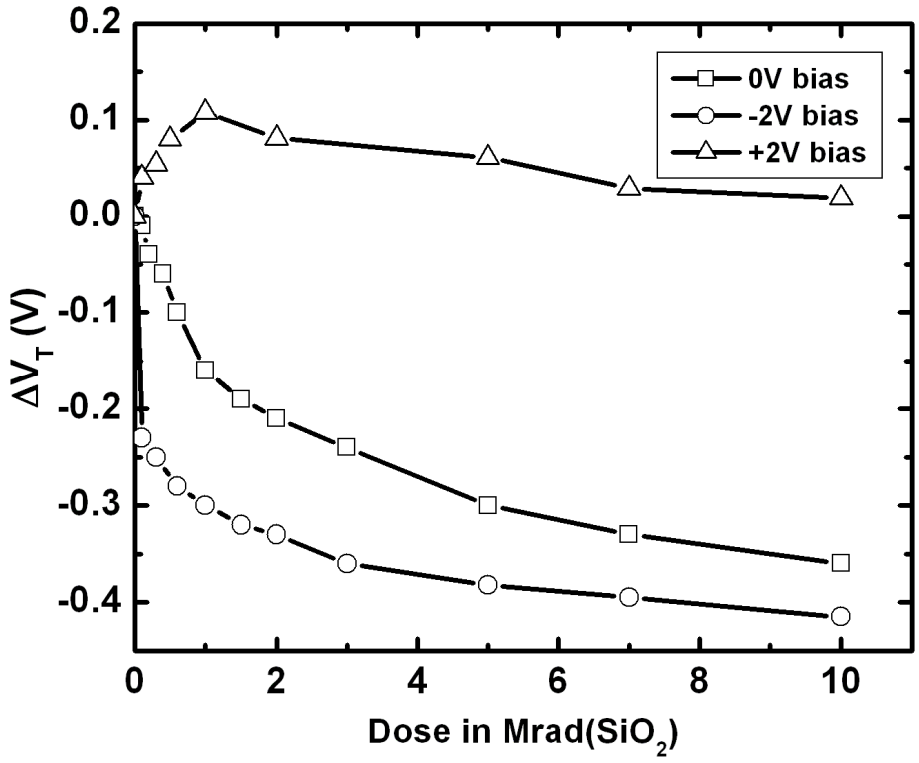

Figure 6.3. ΔV_T due to CVS + irradiation at different gate bias conditions for a 7.5 nm gate oxide transistor.

exposures in Figures 6.3 and 6.4. In contrast, the positive and negative bias responses for the thicker oxides in Figure 6.3 were found to be a combination of radiation- and stress-induced charge trapping. In neither type of sample did the gate leakage current vary significantly during irradiation for any bias condition. The lack of significant charge trapping in the 3 nm devices in Figure 6.4 confirms that the stable charge trapping in the thicker devices is most likely a result of traps in the HfO_2 bulk, since the IL layers are processed similarly in the two kinds of films. Note that these are pure HfO_2 based devices, and the bulk HfO_2 almost certainly crystallizes during the high-temperature post-

deposition anneal treatments. The oxides following these anneals are in the form of phase separated individual nano-crystallites. The grain boundaries form a source for electrically

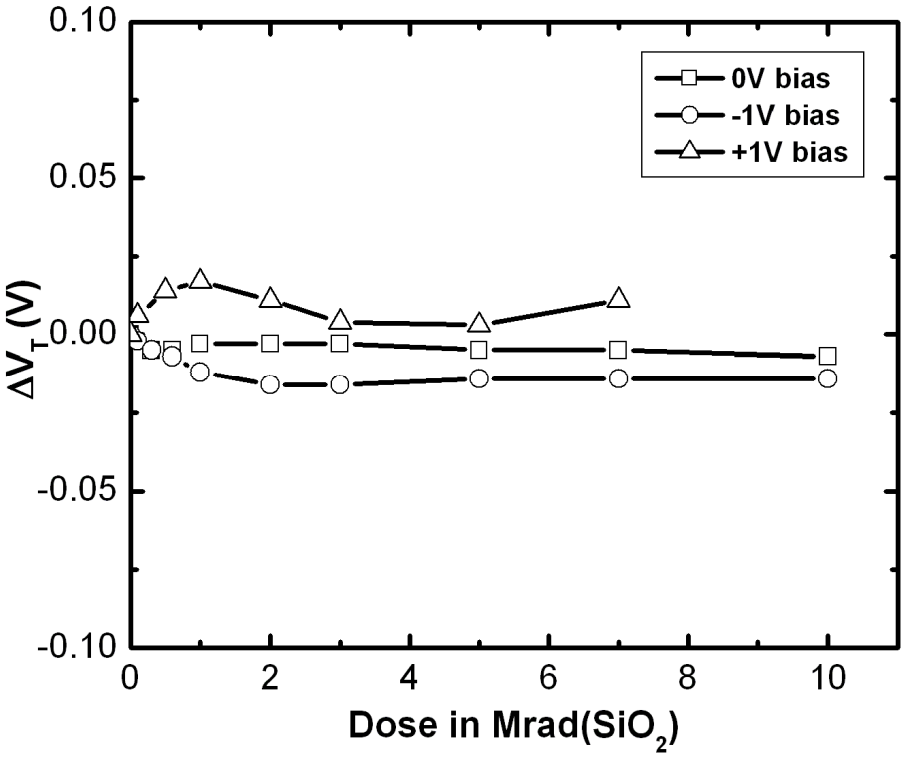

Figure 6.4. ΔV_T due to CVS + irradiation at different gate bias conditions for a 3.0 nm gate oxide transistor.

active defects created during the oxide processing [41]. Oxygen vacancies and interstitials, which form the primary defect states in the oxide, can segregate along these grain boundaries and introduce localized electron and hole trapping levels in the HfO_2 band gap [26],[41]-[44].

6.4.3 Constant Voltage Stress (CVS) and biased irradiations

Controlled CVS experiments were conducted on the transistors of different oxide thicknesses (t_{phys} = 7.5 nm and t_{phys} = 3.0 nm), owing to the observed charging of the thicker dielectric layers with time under bias, even without irradiation. This charging is possibly due to shallow electron and hole traps in HfO_2 dielectric films, which (as discussed above) are located mostly in the bulk of the film [26]-[33] under these stress conditions, as evidenced by a lack of stable charge trapping in the thinner dielectric layers. It is also possible for this trapping to occur in the SiO_2 interlayer, which may not show up as a detectable voltage shift in the 3 nm HfO_2 samples owing to an increased leakage in these thinner dielectrics, which can cause annihilation/neutralization of these trapped charges. It is necessary to note that the reduced band offsets (E_{CBO} ~ 1.5 eV and

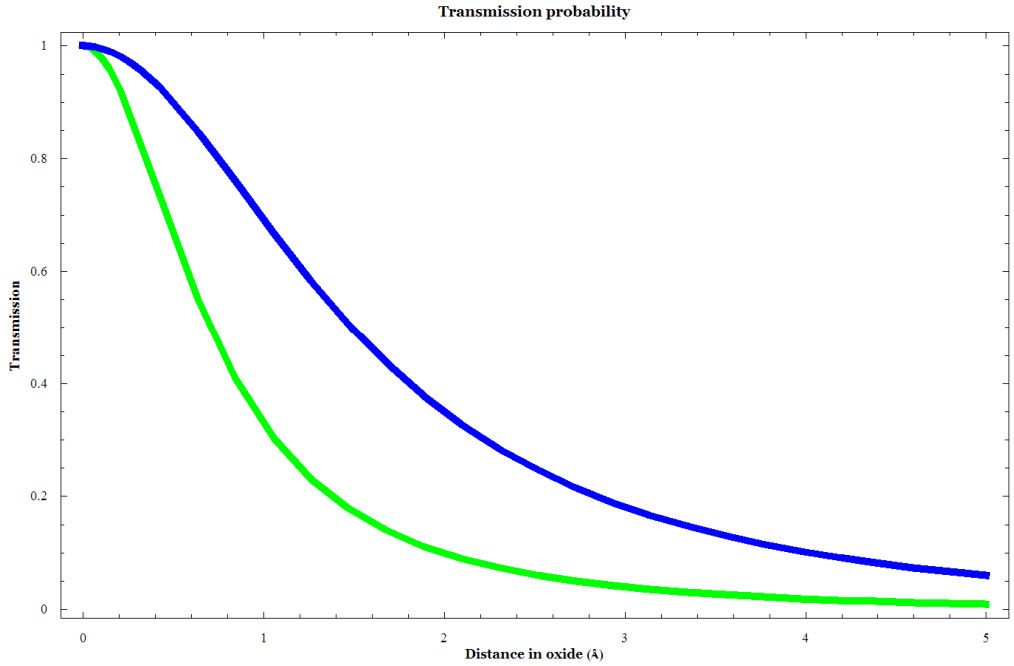

Figure 6.5. Transmission probability plotted as a function of distance into the oxide for both SiO_2 (green curve) and HfO_2 (blue curve) on Si. It is evident from the figure that the tunneling probability is much higher for HfO_2 as compared to SiO_2 owing to the reduced band offsets of E_{CBO} ~ 1.5 eV on Si.

E_{VBO} ~ 3.4 eV) in the HfO_2 samples play a significant role in the tunneling of charges that causes transient trapping and detrapping in the HfO_2/SiO_2 layers [45-47]. Fundamentally the transmission (tunneling) probability can be solved quantum mechanically for SiO_2 and HfO_2, using equation 1.2 as shown in Chapter I [48]. The Figure 6.5 plotted using this equation shows that, for HfO_2 the tunneling probability is much higher than SiO_2 owing to reduced band offsets but improves with higher thicknesses. The presence of a thin ~ 1 Å SiO_x interlayer does not serve as a good blocking electrode for avoiding the tunneling of charges. Theoretical investigations reveal that a SiO_2 thickness of ~ 7 Å is required for a complete formation of a O-Si-O bond taking into consideration its bond angles, which with the addition of roughness can increase to ~ 1.2 nm [49]. This is in support of the observed transient charging (in 7.5 nm MOSFETs) near the interface in these dielectric layers. Additionally, the increase of O deficiency (vacancies) in this interlayer with the growth of HfO_2 and their intermixing effects results in the formation of hole as well as electron traps that can act as trapping centers for carriers tunneling from Si under bias stress [50]. Furthermore, the presence of the HfO_2/SiO_2 interface in addition to traditional SiO_2/Si interface can also be one of the reasons for the observed threshold voltage shifts of ± 0.15 V for the corresponding negative and positive bias stress conditions.

1) Negative CVS and irradiation

Transistors with 7.5 nm oxides were stressed at negative, positive, and zero bias for a total of 5 h, which matches the time under bias during 10 Mrad(SiO_2) irradiation. A fresh set of transistors with the same *W/L* ratio was used for all of the biased irradiations.

The 0 V measurements serve as a control to determine whether room temperature storage or the sequence of *I-V* sweeps performed to characterize the transistor response is changing the device characteristics measurably on the time frame of the measurements. No shifts in the *I-V* curves occurred with storage in air with the gate electrode grounded and repeated measurements for either the 7.5 nm or 3 nm samples on the time frames of the irradiations in Figures 6.2-6.4.

Figure 6.6 shows CVS at -2 V (squares) and the combined effects of -2 V bias and irradiation (circles). The time scale on the top axis is matched to the time required for the dose in Mrad(SiO_2) on the bottom axis for irradiation. Negative CVS on the 7.5 nm samples for 5 h at room temperature resulted in a maximum value of ΔV_T of ~ -0.15 V.

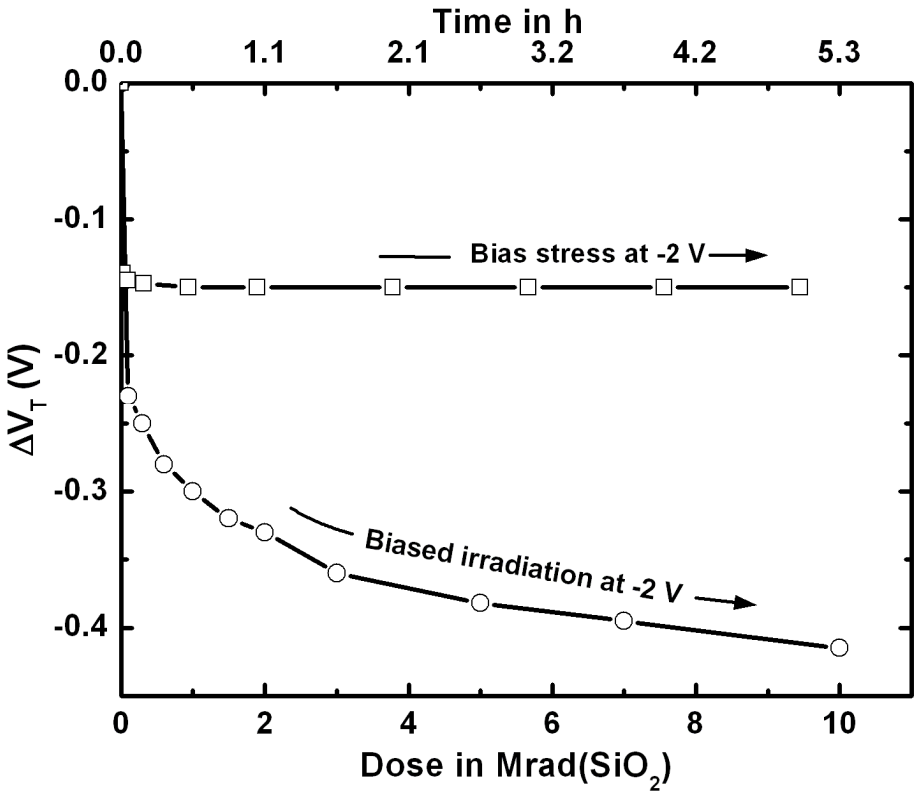

Figure 6.6. Threshold voltage shifts (ΔV_T) due to CVS (-2 V) and CVS (-2 V) + irradiation on 7.5 nm samples. The bottom x-axis shows the dose in Mrad(SiO_2). The top x-axis shows the time during CVS.

The threshold voltage V_T decreases rapidly at very short times during CVS (< 60 s) and then saturates. The maximum shift corresponds to a net value of ΔN_{ot} of ~ 1.4×10^{12} cm^{-2}. The combined effects of irradiation and CVS lead to approximately three times greater degradation (ΔV_T = ~ –0.42 V; ΔN_{ot} of ~ 3.8×10^{12} cm^{-2}).

The V_T shift during negative CVS is due to the tunneling of holes from the *p*-Si. The reduced experimental HfO_2/Si valence band offset of ~ 3.2 eV (theoretical ~ 3.4 eV), compared to ~ 4.8 eV for SiO_2/Si, increases the tunneling probability as mentioned earlier [45]-[47]; the relatively large shifts at room temperature for small fields indicate there must be shallow hole traps in the HfO_2 [26]-[33].

2) Positive CVS and irradiation

S

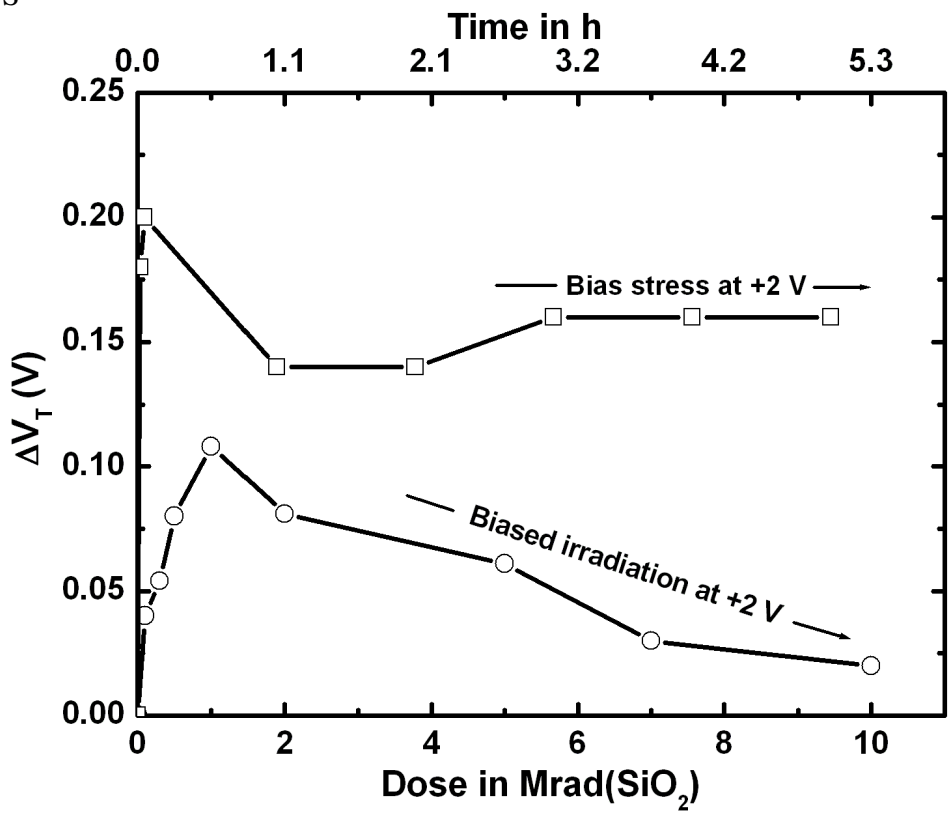

Figure 6.7. Threshold voltage shifts (ΔV_T) due to CVS (+2 V) and CVS (+2 V) + irradiation on 7.5 nm samples. The bottom x-axis shows the dose in Mrad(SiO_2). The top x-axis shows the time during CVS.

Similar CVS and combined irradiation/CVS experiments were also performed under positive bias. As shown in Figure 6.7, for CVS only (squares), a positive ΔV_T is observed. This is due to electron trapping in pre-existing traps in the HfO_2 film [36],[51]. The electron injection from the Si dominates as compared to the hole injection from the metal under positive gate bias due to lower conduction band offsets (~ 1.5 eV) on the oxide/Si interface as compared to the metal/oxide interface (~ 2.3 eV) [45]-[47]. Additionally, the presence of an enhanced moment arm effect at the oxide/Si interface makes charge near the Si interface more effective in shifting the threshold voltage than charge near the gate interface. Intrinsic electron traps can also be present due to the Jahn-Teller splitting of the Hf bonding site, which can introduce defects in the HfO_2 band gap as shown by previous studies [52],[53]. Net negative charge builds up to a dose of 1 Mrad(SiO_2) as a result of CVS induced electron trapping. For higher doses, radiation-induced positive charge trapping in the bulk HfO_2 or the SiO_x interlayer neutralizes and/or offsets this electron trapping, leading to a decrease in the magnitude of the positive threshold voltage shifts observed in Figure 6.7. This shows that bias-induced electron trapping dominates over radiation-induced hole trapping for these devices and irradiation conditions.

6.4.4 Biased Annealing Studies

Following irradiation, the annealing characteristics of the 7.5 nm gate oxide devices were measured at room temperature for different annealing biases. Both the irradiation and annealing were done in-situ with the recovery process monitored immediately after irradiation. Samples were exposed to the three different bias conditions (zero, positive and negative) during irradiation, and annealing was characterized for

different gate biases [54]. Figures 6.8 and 6.9 illustrate the injection-induced recovery in these devices for two irradiation and annealing bias combinations. Table 1 summarizes the net oxide-trap charge density projected to the interface (ΔN_{ot}) after irradiation and anneal/recovery for all biases studied in this work. Similar trends in electron and hole trapping are observed for similar irradiation and bias conditions to Figures 6.8 and 6.9.

1) -2 V Irradiation/+2 V Annealing

Figure 6.8 shows results for a 7.5 nm device that was irradiated at negative bias and annealed at positive bias [39]. The figure demonstrates the absence of any detectable electron trap creation during post-irradiation annealing. This can be verified from the fact

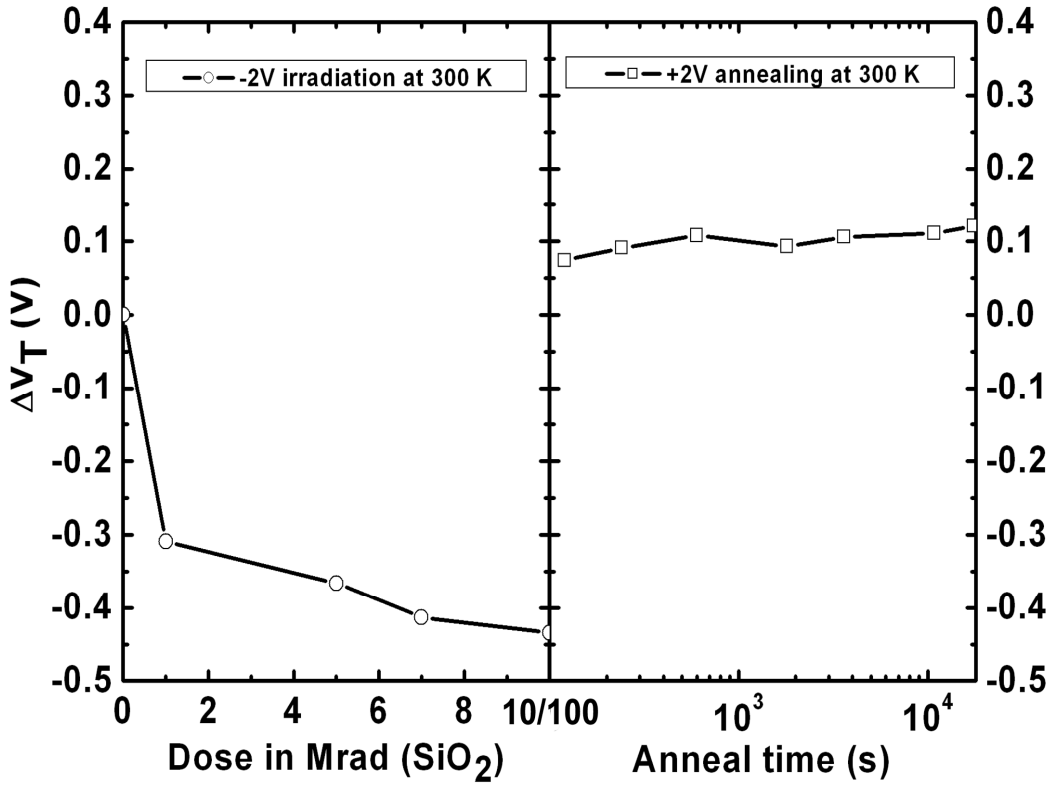

Figure 6.8. ΔV_T as a function of irradiation and annealing for 7.5 nm devices exposed to 10 Mrad(SiO_2) at -2 V bias and annealed at room temperature at +2 V bias.

that positive bias stress only (Figure 6.7) shows comparable magnitudes of threshold voltage shift as that of this sample (during +2 V anneal). Electron tunneling during the post-irradiation anneal annihilates or compensates [18] the irradiation and stress-induced trapped holes, and additionally traps electrons to produce a net ΔV_T of +0.12 V (equivalent to a net charge of ~ 1.1×10^{12} cm^{-2}) at the conclusion of the irradiation and annealing sequence.

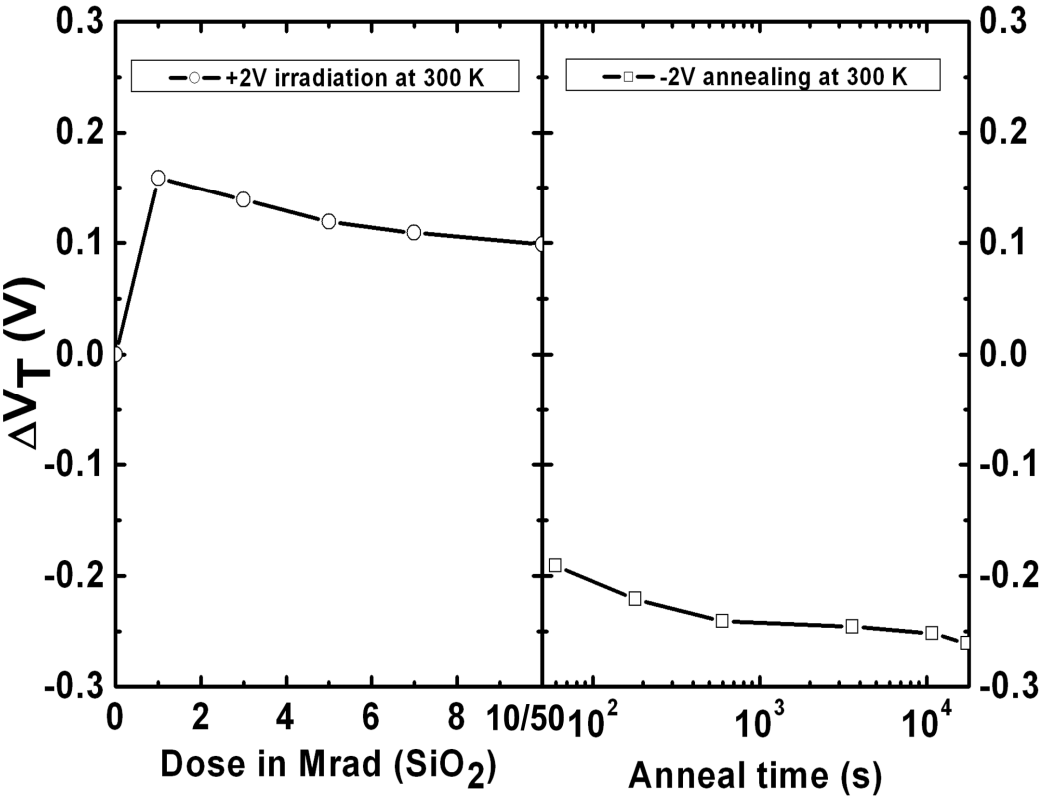

Figure 6.9. ΔV_T as a function of irradiation and annealing for 7.5 nm devices exposed to 10 Mrad(SiO_2) at +2 V bias and annealed at room temperature at -2 V bias.

2) +2 V Irradiation/-2 V Annealing

Figure 6.9 shows the opposite irradiation and annealing bias pair. In contrast to Figure 6.8, the threshold voltage first shifts positively during irradiation (net electron

trapping), and negatively during anneal (net hole trapping). During the -2 V annealing, the sample continues to trap positive charge, although at a decreasing rate at the end of the 5 h time period. The net shift is much more than that observed for bias-only stress at -2 V with no irradiation (Figure 6.6). This illustrates that radiation-induced trapped holes during the positive bias irradiation are not being annihilated by the electron trapping. Instead, their effects are compensated. The additional hole injection during the -2 V anneal in turn more than fully compensates these electrons. As a result, the maximum threshold voltage shift at the end of the measurement is ~ -0.26 V. The reversal of the net-trapped oxide charge from the annealing experiments highlights the volatile nature of the charge resulting from charge injection in these devices. Hence, the values shown here reflect only the relatively more stable trapped charge that is present after typical current-voltage measurements (typically requiring 30-60 s to complete) are performed.

Table 6.1. Irradiation and annealing conditions for the annealing experiments performed. Values of ΔN_{ot} (cm^{-2}) are summarized for 10 Mrad(SiO_2) X-ray irradiation at a dose rate of 31.5 krad(SiO_2)/min. Values of ΔN_{ot} (cm^{-2}) following room temperature anneal are also shown for times of 1 min and 5 h.

	Irradiation/Annealing bias (V)	ΔN_{ot} (cm^{-2}) (after irradiation)	ΔN_{ot} (cm^{-2}) (after annealing)	
			1 min	5 h
A	-2/-2	3.2×10^{12}	3×10^{12}	3.1×10^{12}
B	-2/0	3.1×10^{12}	2×10^{12}	2×10^{12}
C	-2/+2	3.7×10^{12}	$- 0.8 \times 10^{12}$	$- 1.1 \times 10^{12}$
D	0/+2	2.7×10^{12}	$- 1.4 \times 10^{12}$	$- 1.35 \times 10^{12}$
E	+2/-2	$- 0.9 \times 10^{12}$	1.7×10^{12}	2.4×10^{12}

6.5 Net Effective Charge Trapping Efficiency

Estimates of net effective charge-trapping efficiency in high-κ dielectrics as projected to the Si/oxide interface have been obtained previously using an expression presented originally by Felix *et al*. [20]:

$$f_{ot} = \frac{-\Delta V_{ot}\varepsilon_{ox}}{q\kappa_g f_y t_{eq} t_{phys} D} \tag{6.1}$$

Here f_{ot} is the net effective radiation-induced oxide-trap charge trapping efficiency, ΔV_{ot} is the threshold-voltage shift due to oxide-trap charge, ε_{ox} is the dielectric constant of SiO_2, $-q$ is the electron charge, κ_g is the number of electron-hole pairs generated per unit dose per unit volume in the dielectric layer, f_y is the charge yield, t_{eq} is the equivalent SiO_2 dielectric thickness, t_{eq} is the physical dielectric thickness, and D is the dose deposited in the dielectric layer. It is especially important to note that dose enhancement effects typically have been neglected in the application of equation 6.1 in previous studies of high-κ devices [20],[54].

We now critically re-examine the assumptions that underlie equation 6.1. This approach assumes that the trapping defects are associated with the initial materials fabrication and are not caused by the impinging radiation. During X-ray irradiation, photoelectrons are generated in the gate metal, the gate dielectric, and the substrate. Electron-hole (e-h) pairs are ultimately generated in the gate dielectric layer by the secondary electrons generated by the incident X-rays impinging on the dielectric layer and its immediately surrounding materials. For the structure depicted in Figure 6.1, the ultrathin gate dielectric is surrounded by the much thicker Si substrate and a relatively

thick TiN gate contact, each of which has an effective Z less than HfO_2. For 10-keV X-rays, the actual electron contribution produced in the very thin HfO_2 layer is very small compared to the much thicker adjacent materials; as a result, the dose in the gate dielectric is determined almost entirely by the Z of the surrounding materials [55]-[58]. For Si, Z = 14; for Ti, Z = 22; and for N, Z = 7. With an estimation error that is less than other experimental uncertainties (primarily in the charge yield, as discussed below), we can approximate the dose deposited in the gate dielectric layers in this study as the dose deposited in Si. (The actual dose is slightly larger because the effective Z is not the arithmetic mean of 22 and 7, 14.5, but weights the higher Z Ti more heavily than the N. Offsetting this somewhat is the much thicker Si layer thickness than the TiN layer thickness. Hence, we have used the Si dose as a reasonable approximation of the effective dose in the dielectric layer after secondary electron equilibration.) This contrasts with the equilibrium SiO_2 dose typically quoted in the literature for convenience, and used in previous estimates of charge trapping efficiency in high-κ materials [20],[54]. The dose in Si is ~ 1.8 times higher than the equilibrium SiO_2 dose [55]-[58], which affects the value of D in equation 6.1 significantly. Interestingly, because of the relative layer thicknesses and dose enhancement and roll-out effects at these low radiation energies, differences in the relative stopping powers of electrons in HfO_2 and SiO_2, which are significant, do not enter the estimate of dose in these devices, at least to first order.

It is also possible to develop an improved estimate of the charge generation rate in HfO_2 over that developed by Felix *et al*. [20],[54], which used a simple ratio of the SiO_2 and high-κ dielectric band gaps to estimate an average energy per electron hole pair of ~ 11 eV. Instead, we estimate the average energy per electron-hole pair in HfO_2 from the

Shockley-Klein equation to be ~ 15 [59],[60], since the average energy per e-h pair decreases much more slowly for band gaps above ~ 5 eV than for lower band gaps [59],[60]. This provides an improved value of κ_g of ~ 9.2×10^{12} $cm^{-3}rad^{-1}(HfO_2)$, which is ~ 27% lower than the value obtained using the method of Felix *et al*. [20],[54].

The final remaining source of uncertainty in estimating the effective trapping efficiency in these devices is the charge yield. Because of the significant charge injection during positive-bias and negative-bias irradiations, the most easily compared data that are suitable for obtaining trapping efficiency estimates for the 7.5 and 3 nm oxides are the 0 V data in Figures 6.2-6.4. At 0 V, the electric field is dominated by the TiN-to-Si work function difference initially, and then changes with time as charge is trapped in the bulk of the dielectric layer. Moreover, literature estimates of charge yield to date are limited to SiO_2 [57],[61]. Because of these uncertainties, it is difficult to know the charge yield in HfO_2 at the same level of accuracy as the other parameters in equation 6.1. Hence, more study is warranted on this important topic. Consistent with values of charge yield observed in 0 V irradiations for thinner oxides in [57],[61], we estimate f_y to be ~ 0.35 ± 0.05 in the 0 V irradiations for the 7.5 nm oxides. For the 3.0 nm oxides the value of f_y was estimated to be ~ 0.45 owing to a higher field (~ 1 MV/cm) in the oxide at 0 V. After incorporating the new values for κ_g, f_y and D, and using the ΔV_T shift at 500 krad(SiO_2) for the zero bias irradiations, the estimated net trapping efficiencies for these devices and irradiation conditions are ~ 45 ± 6% for the 7.5 nm devices and ~ 13% for the 3.0 nm devices.

In studies by Felix *et al*. [20],[62], the estimated value including uncertainties in charge yield (f_y) was revised to ~ 0.35 ± 0.05 (instead of 0.2 in [20]) for a field of ~ 0.3

MV/cm for the silicates and the value ~ 0.45 was maintained for ~ 1 MV/cm field on the aluminum oxide based transistors in [62]. Table 6.2 provides revised estimates at a dose of 500 krad(SiO_2) for the Hf silicates and at 1000 krad(SiO_2) for the Al_2O_3 based transistors. These data are based on the revised calculations of dose that incorporate dose enhancement, as well as revised estimates of κ_g and the charge yield (f_y), as mentioned above.

Table 6.2. Previous and revised estimates (correcting κ_g, f_y and D) of trapping efficiencies with a weighted average of ~ 1.73 (Al-Si) for the dose enhancement factor calculated for $HfSiO_x$ capacitors [20] and Al_2O_3 capacitors [62].

Gate material	Dose Enhancement, relative to SiO_2	Dielectric type	Previous estimates % f_{ot}	Revised estimates % f_{ot}
Al	1.73	HfSiO	28	10 - 13
Al	1.73	Al_2O_3	31	14

6.6 Conclusion

We find that stress-induced charge trapping can significantly modify the irradiation and annealing response of transistors with 7.5 nm HfO_2 dielectric layers. Under positive irradiation or stress bias, electron trapping dominates; under negative bias, hole trapping dominates. Reversing the bias during irradiation or anneal quickly leads to a change in sign of threshold voltage shifts due to charge injection into process-induced electron and hole traps in these devices. Transistors built with ultra-thin HfO_2 (such as the 3 nm gate oxide devices) are much less sensitive to irradiation or bias stress than

devices with 7.5 nm dielectrics. These thin-dielectric devices are more technologically relevant for future integrated circuit fabrication, and clearly are very promising candidates for radiation-hardened microelectronics. We also have developed improved estimates of dose and charge generation rates in high-κ dielectrics exposed to 10-keV x-ray irradiation, which enable improved estimates of charge trapping efficiency over those previously obtained in the literature. The remaining, dominant source of uncertainty in these estimates is the charge yield in high-κ devices.

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CHAPTER VII

HOLE TRAPPING IN HfO_2-BASED MOSFETS AS A FUNCTION OF VARYING HfO_2 AND SiO_2 INTERLAYER (IL) THICKNESSES

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7.1 Introduction

In the realm of microelectronics, there has always been increased pressure to improve the operational speed and efficiency in semiconductor devices. MOS devices have been at the forefront of the silicon technology revolution, owing to their ubiquitous

use in integrated chips (ICs). The gate dielectric scaling in each successive technology generation allows for continuing increases in circuit speed and packing density for integrated circuits (ICs). Upcoming CMOS technology generations of 45 nm technology and below require shrinking the physical dimensions of devices in all respects [1]. Traditional silicon dioxide (SiO_2) and its nitrided alternatives have made this scaling possible at the expense of increases in the off-state leakage current and resulting increases in the power dissipation [2]. To overcome these limits, alternative gate dielectrics are being widely studied and on the verge of commercial adoption. Hafnium oxide (HfO_2), with dielectric constant ~15 to 26, is one of the potential candidates to replace SiO_2 in modern CMOS fabrication [3]. HfO_2-based MOSFETs have recently been announced as devices that would power the 45 nm and the 32 nm technology nodes. A thin (~ 1 nm) SiO_2 interlayer (IL) forms an integral part of this gate stack. This results in a better interface with reduced intermixing of the HfO_2 at the expense of decrease in the effective dielectric constant [4]. Reliability aspects of charge trapping in these dual oxide layer devices have been extensively studied using bias stress mechanisms [5-7]. Radiation acts as an alternative tool to investigate the charge trapping response of these devices. The layer contributing predominantly to this charge trapping in the dual oxide layer stack is still a matter of debate. It is of scientific interest to know the fundamental contribution to charge trapping for each of the constituent materials and its location in the gate dielectric. Our results indicate the presence of predominant hole trapping in both, the interlayer as well as in the bulk as confirmed from the radiation induced charge trapping response of these dielectric layers as a function of varying bulk HfO_2 and SiO_2 IL thicknesses. These results additionally verify the possibility of increase in the O

vacancies in the SiO_2 IL with the growth of a thicker HfO_2 on the top which can cause increased interlayer hole trapping. Furthermore, we discuss the presence of charge neutralization from direct tunneling induced leakage currents in these devices due to reduced band offsets, which can lead to underestimation of the pure charge trapping response of the individual materials in these gate dielectric layers.

In charge trapping/buildup studies of HfO_2 gate dielectrics, both electron and hole trapping have been reported in the literature. Theoretical studies have predicted the negative U behavior of O^{2-}, which supports its amphoteric nature acting as a hole as well as an electron trap [8, 9]. Recent reliability studies have described electron trapping in these oxides with a very high trapping cross-section as compared to traditional SiO_2 [6, 10-14]. This trapping can depend strongly on device processing and dielectric layer thickness [11, 15]. Previous charge trapping studies in HfO_2-based MOS capacitors and some recent work on MOSFETs, have reported positive charge trapping on both thinner and thicker hafnium oxides, thereby suggesting the presence of processing induced defects both in the SiO_x interlayer and in the bulk of the hafnium oxide [16-22]. Recent probing of the location of these traps and some previous work have concentrated more on the non-sotichiometric SiO_x interlayer being the primary source for the trapping in these oxides [23-25]. In our recent work on HfO_2-based MOSFETs, radiation induced hole trapping was found to be significantly more in the thicker devices (7.5 nm HfO_2/1 nm SiO_2) as compared to thinner samples (3 nm HfO_2/1 nm SiO_2) [21]. Increased leakage current from direct tunneling in the 3 nm HfO_2/1 nm SiO_2 samples was one of the main reasons for the observation of negligible shifts in the thinner HfO_2 samples due to possible annihilation/neutralization effect of trapped charges in the dielectric. However

additional confirmation is required to identify the layer contributing predominantly to the radiation induced charge trapping. In this chapter we try to answer this equivocal problem by investigating the radiation induced charge trapping in these MOSFETs as a function of bulk HfO_2 and SiO_2 IL thicknesses. The thicknesses of the gate dielectrics studied here are 7.5 nm HfO_2/1 nm SiO_2, 3 nm HfO_2/1 nm SiO_2 and 3 nm HfO_2/2 nm SiO_2 as shown in the schematic diagram in Figure 7.1. From the observed results of these three samples we try to address the issue of individual layer contribution to the substantial positive charge trapping in these gate dielectrics.

7.2 Experimental section

Non-metal covered (bare) oxide films for materials characterization were grown using the same oxide growth recipe that was used for transistor fabrication used in the total dose experiments. Extensive material characterization experiments on these oxides were performed using different techniques like Rutherford Backscattering Spectroscopy (RBS), Channeling, Medium Energy Ion Scattering (MEIS) and X-Ray Reflectance (XRR) as described in detail in Chapter V [26, 27]. These measurements were performed to verify the bulk HfO_2 and the SiO_2 IL thicknesses and stoichiometry of the individual layers. Samples for Capacitance-Voltage (C-V) analysis were fabricated by depositing Al gate metal dots using a shadow mask in an evaporator and Au back contacts were sputter deposited after a back oxide etch. C-V measurements were performed to compare the measured and the calculated theoretical capacitances.

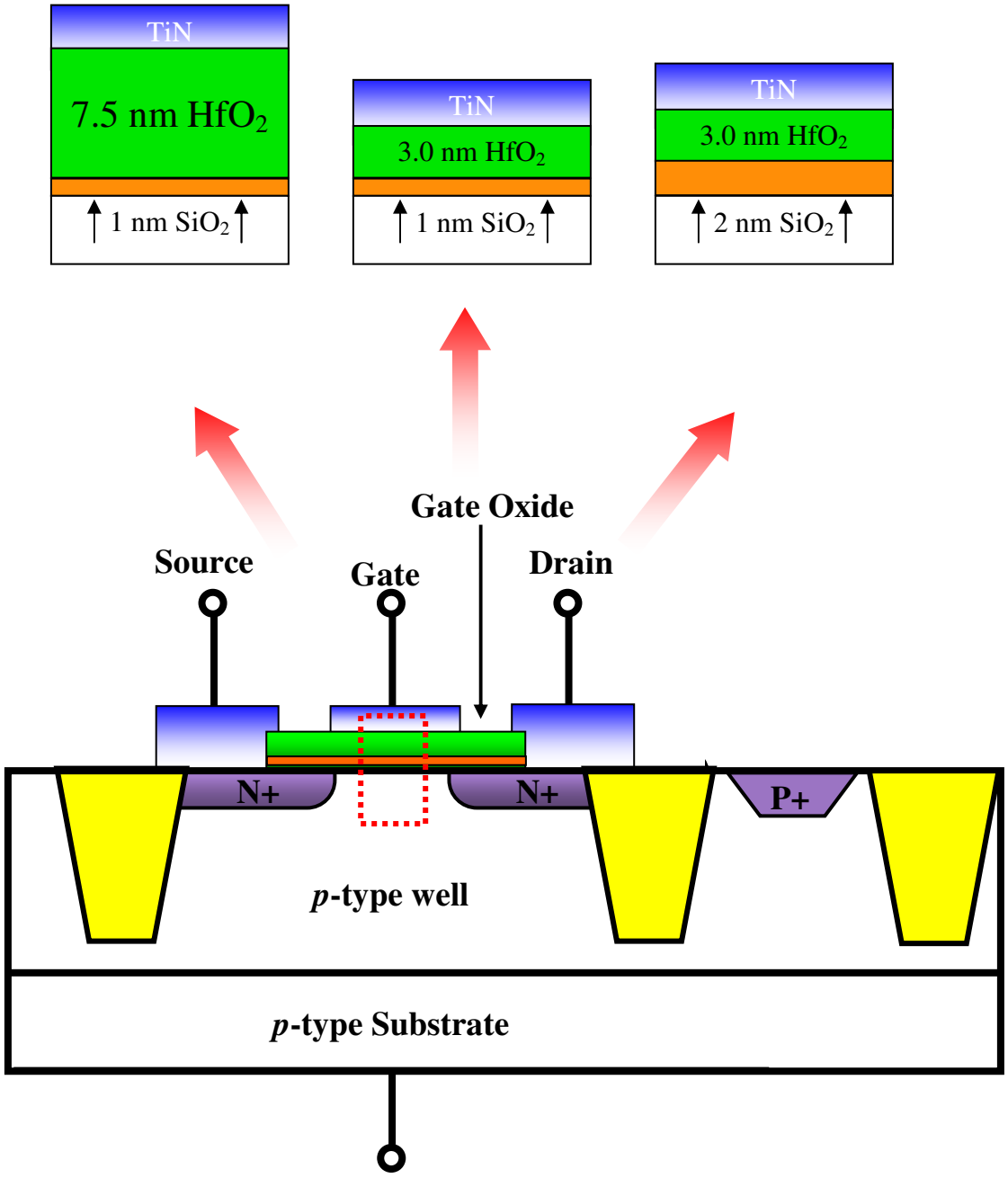

Figure 7.1. Cross-section of a HfO_2-based *n*MOSFET (*p*-type Si substrate). Inset showing the three different thicknesses of HfO_2 bulk and SiO_2 interlayers (IL) included in this study.

The total dose experiments were performed on MOS transistors. The high-κ MOSFETs examined in this work were fabricated using industry standard CMOS process flow in a 65 nm technology. TiN/HfO_2 gate stack *n*MOSFETs were fabricated on Si

(100) 200 mm wafers using a standard CMOS transistor process flow, which includes a 1000 °C/10 s dopant activation. Approximately 1 nm chemical oxide and ~ 2 nm thermal oxide was grown for the two different interlayer samples followed by HfO_2 deposition using atomic layer deposition (ALD) chemistry using TEMA (tetrakis ethyl methyl amino) Hf+O_3, followed by a post-deposition anneal in N_2. Three different MOSFETs with varying bulk and ILs were fabricated by this technique (7.5 nm HfO_2/1 nm SiO_2, 3 nm HfO_2/1 nm SiO_2, 3 nm HfO_2/2 nm SiO_2). The transistors under investigation in these samples had a width to length ratio (*W/L*) of 10 μm/0.25 μm.

Control experiments of constant voltage stress (CVS) were performed on time scales comparable to those required for the 10 Mrad(SiO_2) irradiations for all the three sample configurations. These tests were performed to separate the contributions of bias-induced charge trapping/creation [5] in these oxides from radiation-induced shifts. Standard threshold voltage shifts, subthreshold current-voltage (*I-V*) curves, and leakage current values were measured after each step in X-ray dose as well as after each interval of bias stress in the CVS measurements. Gate biases were corrected for the TiN-Si work functions in order to determine the field across the oxides. Following this compensation, the applied voltages of +2 V/-2 V for 7.5 nm/1 nm devices correspond to E_{ox} values of ~ 2.7 MV/cm and –2.0 MV/cm; gate biases of +1 V/-1 V for 3 nm/1 nm devices are equivalent to E_{ox} values of ~ 3 MV/cm and -1.9 MV/cm; and gate voltages of + 1.25V/-1.25 V correspond to E_{ox} values of ~ 3 MV/cm and ~ - 2 MV/cm for the 3 nm/2 nm devices.

An ARACOR irradiator with a 10 keV x-ray source was used to irradiate the die-level samples under negative and positive gate bias conditions with the other three

terminals grounded. These were irradiated to a cumulative dose of 10 Mrad(SiO_2) at a dose rate of 31.5 krad(SiO_2)/min, with bias applied by probe contacts that were located so as to avoid shadow effect of the beam. An Agilent 4156 semiconductor parameter analyzer was used to measure the current-voltage (*I-V*) characteristics. All biased irradiations, voltage stresses, and electrical characterizations were done in-situ in the ARACOR system to minimize experimental sources of error due to measurement delays and probe contact thereby resulting in better reproducibility of results.

7.3 Results

7.3.1 Materials analysis

RBS/Channeling results for all the samples are as mentioned in Tables 5.4 to 5.7 in section 5.3.2a and 5.3.2b of Chapter V. These results confirm the measured thickness to be close to the targeted thickness as expected from the growth recipe. MEIS measurements performed on two of the samples (7.5 nm HfO_2/1 nm SiO_2 and 3 nm HfO_2/1 nm SiO_2) indicate some intermixing of the HfO_2 and SiO_2 layers which thereby changes the bulk composition and invariably alters the κ-value. XRR measurements verified the bulk thicknesses for all the samples as mentioned in Chapter V. C-V measurements revealed C_{ox} values, which were much lower than the theoretical C_{ox} assuming two capacitances in series for the two stacked oxide layers (refer Figure 5.6 of Chapter V). This difference was consistent with some intermixing and a smaller dielectric constant of the total dielectric.

7.3.2 Constant Voltage Stress (CVS)

Constant voltage stress of positive and negative fields as mentioned above on the physically thickest sample (7.5 nm HfO_2/1 nm SiO_2) and the thicker IL (3 nm HfO_2/2 nm SiO_2) sample produced some threshold voltage shifts when stressed to a period of 5h. For the 7.5 nm HfO_2 transistors, transient trapping and detrapping was observed depending on the bias polarity. This was observed to be very instantaneous with the application of the bias stress. A threshold voltage shift (ΔV_T) of ± 150 mV was consistently observed for these samples with a negative V_T shift (positive charge trapping) for negative gate voltage and vice versa. Figures depicting these results can be found in Chapter VI. The constant voltage stress induced shifts for the 2 nm IL devices are as shown in Figure 7.2. Both the bias polarities produce minimal negative threshold voltage shift indicating some positive charge trapping in some of the transistors. We would like to add that these effects are not substantial to arrive at a definite conclusion about these shifts for both the gate biases. The shifts were found to be close to zero considering experimental error and device-to-device variation limits as indicated from the experimental error bars in Figure 7.2. These results additionally prove the absence of any substantial metal injection in these devices under the oxide fields studied in this work. For the physically thinnest sample, there were no detectable shifts observed for similar bias stress conditions. The bias induced trapping, if any, was possibly neutralized by the increased leakage currents on the order of a 100-150 nA flowing through these devices during constant voltage stress (CVS) and/or *I-V* measurements.

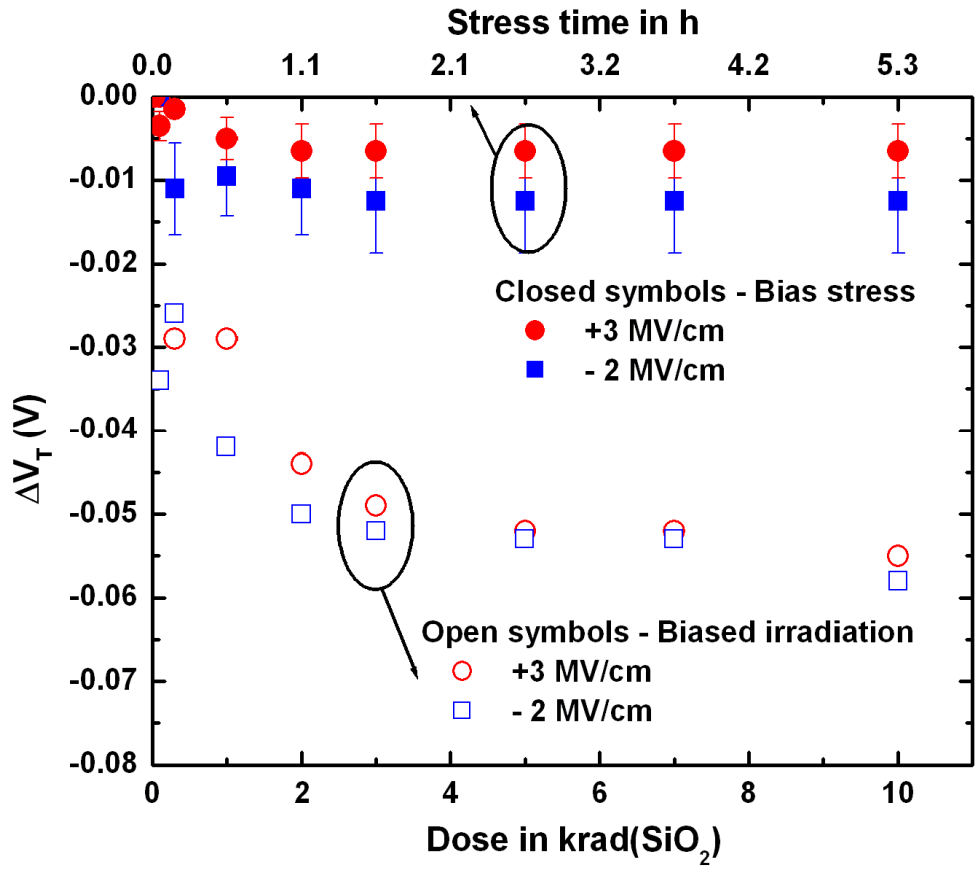

Figure 7.2. The figure shows threshold voltage shifts (ΔV_T) due to bias stress at + 3MV/cm and -2 MV/cm with experimental error bars (closed symbols) and biased x-ray irradiations (open symbols) at the same electric fields as the bias stress experiments. The irradiations were performed up to a total dose of 10 Mrad (SiO_2) at dose rate of 31.5 krad(SiO_2)/min.

7.3.3 Total dose results

Radiation exposure of these sample sets under the bias conditions of -2 MV/cm as shown in Figure 7.3 resulted in predominant positive charge trapping with a maximum ΔV_T ~ 400 mV observed in 7.5 nm HfO_2 samples up to a total dose of 10 Mrad(SiO_2). The leakage currents during the measurements in the 7.5 nm samples were on the order of J_g ~ 0.1 A/cm^2. It was found that with repeated *I-V* sweeps, partial recovery (~ 50 %) was observed due to annihilation/neutralization from substrate injection of negative charges

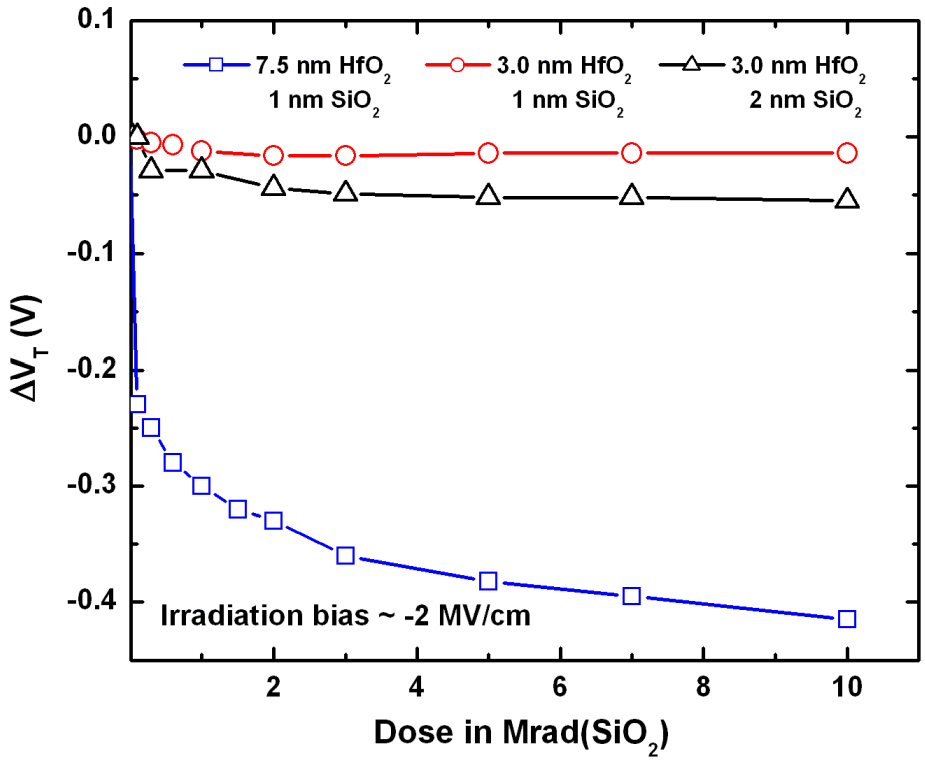

Figure 7.3. The figure shows a comparison of the threshold voltage shifts (ΔV_T) between the three different samples (3 nm/1 nm, 3 nm/2 nm, 7.5 nm/1 nm) as a function of x-ray dose under -2 MV/cm electric field. The irradiations were performed up to a total dose of 10 Mrad (SiO_2) at dose rate of 31.5 krad(SiO_2)/min for all the samples.

during the repeated gate bias sweeps in the 7.5 nm HfO_2 samples. This hints at significant number of these charges being present very close to the interface, like border traps [28] in the SiO_2 interlayer that can exchange charge with silicon on the time scale of the measurements. It is however important to note that a residual shift of ~ 200 mV shift was found to be relatively stable to subsequent sweeps. Owing to a high leakage (J_g ~ 3-5 A/cm^2) induced neutralization (during *I-V* measurements) for the 3 nm/1nm samples, no radiation induced shifts were observed with radiation dose up to 10 Mrad(SiO_2). Similar irradiation and pre and post-irradiation measurements were performed on the 3 nm HfO_2/2 nm SiO_2 samples. For the 3 nm HfO_2/2 nm SiO_2 samples, the leakage currents at

the gate biases studied were found to be on the order of ~ 20 pA (J_g ~ 8 x 10^{-4} A/cm^2). These thicker IL samples showed a consistent negative voltage shift of ~ 50 mV during the irradiations up to a total dose of 10 Mrad(SiO_2) at the oxide fields studied. This indicates predominant positive charge trapping with radiation dose under minimal injection conditions. Relative to the thinner interlayer samples (7.5 nm HfO_2/1 nm SiO_2) where injection dominates the initial part of ΔV_T vs. dose curve, this sample illustrates the pure radiation response of such a system.

For the radiation response of samples under positive gate bias conditions (E_{ox} ~ +3 MV/cm) as shown in Figure 7.4, the thickest samples show predominant electron

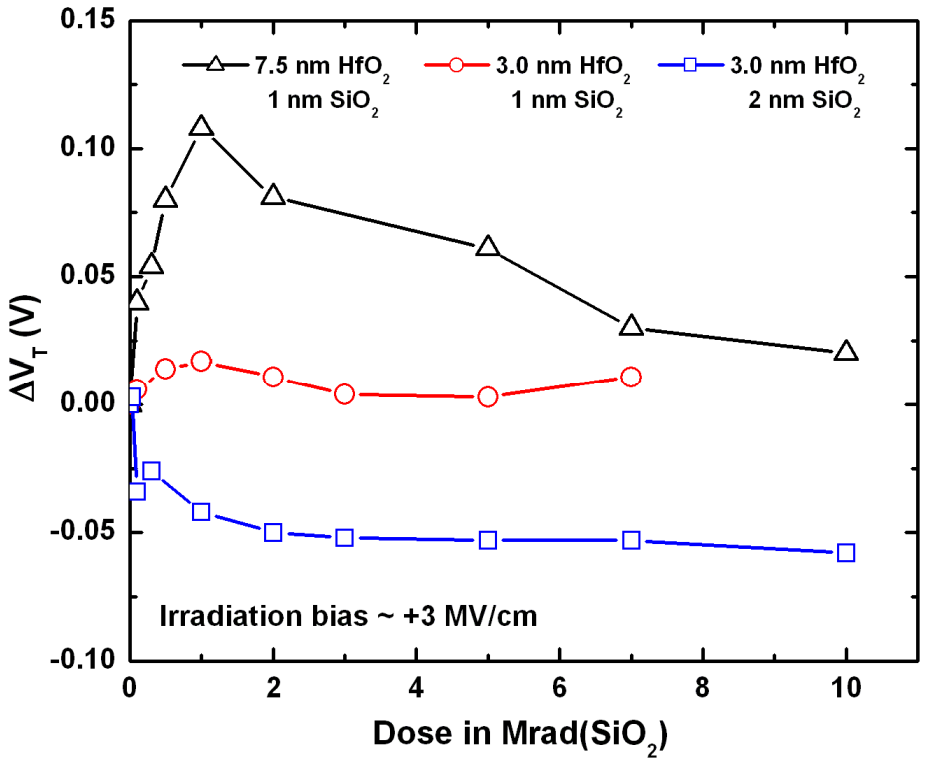

Figure 7.4. The figure shows a comparison of the threshold voltage shifts (ΔV_T) between the three different samples (3 nm/1 nm, 3 nm/2 nm, 7.5 nm/1 nm) as a function of x-ray dose under +3 MV/cm electric field. The irradiations were performed up to a total dose of 10 Mrad (SiO_2) at dose rate of 31.5 krad(SiO_2)/min for all the samples.

trapping from instantaneous injection occurring from the inversion condition in Si. However this is observed at low doses as the ΔV_T is dominated initially by electron injection as compared to the radiation induced bulk hole trapping. At higher cumulative doses, this trend is altered owing to the increased positive charge accumulation in the bulk as well as in the IL, which offsets the ΔV_T observed from carrier injection. For the thinnest samples there was minimal change in the ΔV_T shifts owing to neutralization probability arising from enhanced gate leakage in these samples [21]. The radiation response of the thicker IL samples at E_{ox} ~ +3 MV/cm was almost identical to its response to a negative bias irradiation as discussed earlier. The net positive charge saturates at a maximum ΔV_T shift of ~ 50 mV (similar to the negative bias irradiation) as shown in Figure 7.4. Hence irrespective of the bias polarity during CVS and irradiations, the devices with thicker interlayer continue to trap excess positive charge. The gate leakage currents did not change during the whole course of the irradiations for all the samples.

There were no detectable shifts in the subthreshold *I-V* curve behavior for the irradiation or stress results reported in this work. This confirms the absence of interface trap buildup in these MOSFETS under the irradiation and stress conditions. Similar results have been reported previously with minimal interface trap build up in these materials owing to a higher pre-existing density of defects at the interface (N_{it} ~ 10^{12} cm^{-2}) [18, 19].

7.4 Discussion

The 7.5 nm HfO_2/1 nm SiO_2 samples exhibit threshold voltage shift (ΔV_T) under constant voltage stress due to charge injection dominated by the silicon surface condition of accumulation/inversion, which leads to the transient trapping and de-trapping. For 3 nm HfO_2/1 nm SiO_2 MOSFETs, absence of threshold voltage shift is due to enhanced leakage current which neutralizes/annihilates the injection charge on the time scale of the conventional D.C. I_{ds}-V_{gs} measurements. High leakage is predominantly from increased probability of direct tunneling in these devices even in the presence of ~ 1 nm SiO_x interlayer. This phenomenon is discussed with Figure 6.5 highlighting the tunneling probability in case of the HfO_2 based devices in Chapter VI.

Theoretical calculations reveal that it takes ~ 0.7 nm for the complete band gap formation of SiO_2, with interface roughness this value can even approach 1.2 nm [29]. Hence for the thinner IL samples, the reduced band offsets play a significant role in the substrate charge injection. For the 7.5 nm samples, injection from the gate metal, if any, was overshadowed by the Si-substrate induced charge injection. Additionally, it is important to realize that V_T shift is defined by the position of charge centroid in the dielectric. Substrate injection charges in this case being closer to the interface dictates the threshold voltage shift more as compared to charges tunneling from the gate metal into traps located closer to the metal/oxide interface [21]. Furthermore, the physically thicker HfO_2 aids in this respect thereby not altering the V_T shifts from the perspective of charges tunneling from the gate electrode. It is however critical to determine the possibility of injection from the gate metal, hence the bias stress evaluation of the thicker interlayer serves as an ideal sample to determine this probability. The 2 nm SiO_2 IL in these

samples acts as a better blocking electrode thereby minimizing (although not completely eliminating) the substrate charge injection in these bias conditions as shown in Figure 7.2. The absence of threshold voltage shift under bias stress is also indicative of negligible charge injection from the metal electrode in all the samples studied in this work.

On exposure of these devices to x-rays, the photons interact with the dielectric and generate photoelectrons (direct ionization), which further creates electron hole pairs (EHPs) in the oxide. In these thin oxides however the secondary photoelectrons from the metal and the silicon contribute to substantial EHP creation in the dielectric. A significant number of these EHPs recombine due to the applied electric field; the remainder of them gets trapped. This quantity is defined by the term "charge yield" which alters the *C-V* and *I-V* characteristics of the device. The total dose results as measured from the *I-V* sweeps for the three different sample structures are as shown in Figure 7.3 and Figure 7.4 for E_{ox} ~ -2 MV/cm and E_{ox} ~ +3 MV/cm respectively for comparison. The enhanced positive charge trapping in the 7.5 nm HfO_2 samples is owing to an increased bulk oxide as well as increase in the oxygen vacancies in the SiO_2 IL from a thicker HfO_2 growth. The oxygen vacancy argument is explained by Ryan *et al.* [23] and Bersuker *et al.* in their recent studies [30]. According to their investigation, the growth of a thicker HfO_2 layer (longer high temperature exposure of the IL) results in the formation of a sub-stoichiometric SiO_x interlayer which can form amphoteric traps as mentioned previously in the chapter. These results are also verified by the MEIS results for our samples, which indicate the formation of this sub-stoichiometric layer for the 7.5 nm HfO_2 samples and a relatively stoichiometric SiO_2 in the thinner HfO_2 samples. Theoretical investigations by

various authors predict the diffusion of oxygen vacancies and interstitials from the bulk HfO_2 to the Si interface. These studies also mention about their eventual segregation at this interface being thermodynamically and kinetically favorable [31-33]. This additionally supports the formation of a SiO_x IL during the HfO_2 deposition and post deposition anneal as already observed by the MEIS technique. However the residual trapping of ~ 200 mV in the 7.5 nm samples also hints at some bulk hole trapping in these MOSFETs. Fundamentally, if all of these charges were to be distributed in the interlayer, we would expect no net ΔV_T shift from the gate bias sweep owing to the high leakage from the quantum mechanical tunneling (reduced conduction band offset E_{CBO} ~ 1.5 eV) within ~ 1 nm from the Si substrate into the oxide. The very existence of the remnant V_T shift is a strong indication of some bulk hole trapping apart from the increased SiO_2 IL trapping in thicker HfO_2 samples, which is consistent with previous studies [18, 19, 21]. This inference is also strongly supported by the results of earlier investigations about the observation of defects in the bulk of the HfO_2, which are responsible for the positive charge trapping [20, 34, 35]. However the nature of the defect has been speculated to be similar to the E_γ' center (similar to Si-Si oxygen vacancies observed in the traditional SiO_2/Si) from the EPR measurements [20]. The work described in this chapter combined with the understanding on the previous studies on the defect identification suggests the presence of Hf-Hf (bridging O vacancy) to be a possible defect state distributed in the bulk of the HfO_2. Theoretical studies also predict oxygen vacancy and interstitial defects in the bulk of hafnium dioxide at various energy levels in the HfO_2 band gap, which could be a potential reason for the observed residual threshold voltage shift [8]. The 3 nm HfO_2/1 nm SiO_2 sample shows negligible voltage shifts with

total dose. However the presence of a thinner bulk HfO_2 accompanied by a possible reduction in the O vacancies in the SiO_2 IL owing to the reduced growth of HfO_2 bulk (3 nm instead of 7.5 nm) cannot serve as a direct explanation to this reduced charge trapping. This is due to increase in the leakage current in the 3 nm HfO_2/ 1 nm SiO_2 samples, which can neutralize/annihilate the trapped charge thereby resulting in negligible shifts in these samples. Hence a comparison of the total dose results of these samples with the thicker IL samples (~ 2 nm SiO_2) can help gain a better understanding on the radiation induced charge trapping in these layered dielectrics. With a completely evolved band gap of ~ 9 eV, the minimal charge injection and neutralization reveals the pure radiation response in these devices. These thicker IL (~ 2 nm SiO_2) devices with a threshold voltage shift of ~ 50 mV at 10 Mrad(SiO_2) indicate minimal radiation induced trapping owing to reduced volume of bulk HfO_2. Additionally, the presence of a thinner HfO_2 bulk oxide (shorter exposure time for SiO_2 IL at higher temperature) on the 2 nm SiO_2 layer does not leach this interlayer of any substantial O thereby producing less O vacancies in the IL.

The radiation response of this sample can be imagined to be the worst-case scenario for the 3 nm HfO_2/1 nm SiO_2 sample if one were to measure the pure radiation response without bias/leakage current induced neutralization. This brings an interesting observation that considering this scenario, the trapping in the 3 nm /1 nm samples will not scale with HfO_2 thickness. Furthermore, it is important to consider that ~ 400 mV shift observed under 10 Mrad(SiO_2) x-ray dose in the 7.5 nm sample is probably underestimated as the currents at the gate bias studied were around 3-5 nA (J_g ~ 0.1 A/cm^2), which can cause some leakage induced annihilation/neutralization of the trapped

charge. This additionally offsets the scaling of the trapped charge from the perspective of increase in bulk HfO_2 thickness for the 7.5 nm HfO_2 samples. This probably is one of the other reasons for the argument supporting the enhanced IL trapping in the thicker HfO_2 MOSFETs. Hence the total dose response of the physically thickest sample (7.5 nm HfO_2/ 1 nm SiO_2) and the thicker IL sample (3 nm HfO_2/ 2 nm SiO_2) and our MEIS results combined with the previous studies suggest that a significant amount of trapping occurs in the SiO_x interlayer with the growth of a thicker bulk HfO_2. The presence of residual trapping ~ 200 mV on the time scale of the measurements following the *I-V* sweeps are indicative of additional bulk hole trapping.

Finally, the radiation response of the thicker IL samples at E_{ox} ~ +3 MV/cm agree with the results of the 7.5 nm HfO_2/1 nm SiO_2 samples at similar oxide fields wherein it was concluded that the predominant trapping in the dielectric stack is positive which offsets the initial bias induced negative injected charge from the silicon at higher doses. This can be seen from absence of any negative charge trapping for the total dose response at +3 MV/cm on the 2 nm SiO_2 IL samples. We would also like to add that probability of neutralization of the trapped charge during the D.C. current voltage measurements is significantly high and the bias stress and the radiation response could be considerably underestimated for all the samples. The use of faster techniques like pulsed I_d-V_g and frequency dependent charge pumping methods can provide a better estimate of these trapped charges.

7.5 Conclusion

From the radiation responses of the three different samples under investigation we conclude that the sub-stoichiometric SiO_x interlayer and the HfO_2 bulk contains a significant number of hole traps which affects the radiation response in these systems. The transient trapping and de-trapping observed in these samples suggest the presence of border traps in the form of O vacancies in the SiO_2 IL which affects the bias stress and total dose response. The observation of residual trapping in the thicker bulk HfO_2 samples clearly indicates the substantial contribution of the bulk HfO_2 layer to this hole trapping. For the future technology nodes (< 1 nm EOT), these issues do not pose a real problem as reduced volume of the gate oxide will cause less charge trapping as can be seen from our 3 nm HfO_2/1 nm SiO_2 samples. However trapping, if any, will be neutralized/annihilated by the increased tunneling induced gate leakage in these devices.

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CHAPTER VIII

SUMMARY AND CONCLUSIONS

To summarize, the radiation response of the two material systems (SiO_2/SiC and HfO_2/Si) discussed in this dissertation work has highlighted the major issues associated with charge trapping in these future high power and low power candidate materials from a reliability perspective. This thesis includes the first observation of predominant hole trapping in nitrided SiO_2/SiC MOS devices when subjected to x-ray irradiations. Nitrogen incorporation at the interface with high temperature NO annealing at 1175 °C passivates electrically active interface defects as measured from the decrease in the D_{it} (10^{13} $eV^{-1}cm^{-2}$ to 10^{12} $eV^{-1}cm^{-2}$), thereby enhancing the inversion layer mobility. Although this significantly improves the device characteristics for SiO_2/SiC based MOS devices, it suffers from its susceptibility to enhanced hole trapping thereby questioning its reliability.

The enhanced positive charge trapping with irradiation in the presence of nitrogen at the SiO_2/SiC interface was subsequently confirmed with similar trends in Fowler-Nordheim and VUV (Very Ultra Violet) photo-injection studies. These studies suggest that high temperature growth in conjunction with the presence of ~ 1 nm thick nitrided interface results in an increased density of hole traps that can hamper device operation and its long-term reliability. Non-nitrided samples exhibit an improved radiation response owing to reduced positive charge trapping due to the absence of nitrogen and/or the

neutralization/annihilation of this reduced positive trap charge with some electron trapping at the interface/near interface defects.

Isochronal annealing studies performed on nitrided samples provide an activation energy E_a ~ 0.3 eV for device recovery. Theoretical calculations reveal the presence of a nitrogen lone pair present in the proximity of the valence band edge of SiC, which may be one of the reasons for the observed positive charge trapping in these devices. More elaborate spectroscopic studies are required to identify the defects responsible for the enhanced positive charge trapping in these nitrided SiO_2/SiC based MOS devices. Finally our results stress on the need to optimize the nitrogen content in these material systems in order to strike a balance between reducing the density of defects at the interface (D_{it}) and improving its operational reliability.

Studies of radiation and bias stress induced charge trapping in low power candidate material systems of HfO_2/SiO_2/Si have underlined the fundamental issues that can affect device reliability in these gate stacks. The presence of the SiO_2 interlayer (IL) adds to the complexity of understanding the pure radiation response in these high-κ MOSFETs. The introduction of SiO_2 IL was important from the perspective of device operation as it serves to reduce the remote phonon scattering (soft optical phonon coupling with carriers) and remote coulombic scattering (increased trapped charge) in these devices thereby improving its mobility. The bias stress response indicated towards the presence of significant electron and hole traps in the sub-stoichiometric SiO_x IL, which can alter the device threshold voltage thereby affecting its electrical characteristics. Additionally, the response to radiation of HfO_2/Si material system also confirmed the

presence of net hole trapping in the bulk as well as in the SiO_x interlayer (IL), which can be detrimental to device performance.

Radiation response of gate oxides, which is a strong function of the material thickness and processing, apart from nature and energy of the ionizing species and oxide fields during radiation, require adequate controlled experiments to be performed to understand the former parameters to analyze and compare between different device structures. Materials analysis undertaken to verify the gate oxide and IL thickness confirm the targeted results from the growth recipe. RBS, MEIS and XRR results were found to be in agreement for verification of these thicknesses. Furthermore, MEIS results indicate towards the presence of some intermixing in these samples during HfO_2 growth and high temperature post deposition anneals which can affect the desired device capacitance. The deviation of the accumulation capacitance measured using Hi-Lo C-V measurements from the calculated theoretical value strongly hints towards the possibility of this poorly understood intermixing phenomenon. These intermixing issues in the interlayer and in the oxide bulk can play a significant role in defining the charge trapping characteristics in these layered gate dielectric stacks during the bias stress and radiation studies.

Lastly, these studies performed as a function of HfO_2 bulk and SiO_2 IL thicknesses under different fields supports previous literature on the presence of predominant hole trapping both in the bulk as well as in the SiO_2 IL under radiation conditions. The annealing/neutralization of these radiation induced trapped charges with bias reversal strongly implies the charge injection induced recovery in the devices from reduced band offsets. The direct tunneling of these charges from the Si substrate under

such low fields explains the volatility of the trapped charge in these devices. The incorporation of dose enhancement effects due to the metal gate and underlying Si in these thin dielectrics provide refined estimates of net effective charge trapping efficiency in these gate dielectrics. Finally, as seen from the charge trapping response of the thinner HfO_2 MOSFETs, these reliability issues do not pose a major problem for the gate dielectric thicknesses that will be used for future technology generations.