NEW INSIGHTS INTO THE TOTAL DOSE RESPONSE OF FULLY-DEPLETED PLANAR AND FINFET SOI TRANSISTORS

By

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CHAPTER I

INTRODUCTION

Silicon-On-Insulator (SOI) technology provides more advantageous performance over bulk technology for harsh-environment applications, in particular space and military systems [1]. SOI devices typically are less vulnerable to single event effects (SEE) than comparable bulk devices because the buried oxide (BOX) layer reduces the collection volume. However, the total ionizing dose (TID) response of SOI devices is more complicated than that for bulk devices. Indeed, additional charge in SOI devices can be trapped in the BOX. This charge can lead to a large increase in drain-to-source leakage current [2, 3, 4]. This drain current (I_D) increase is sometimes high enough to produce a high current state in which the device can be turned ON for gate voltages lower than the threshold voltage (V_{th}). As dose levels increase, for SOI *n*-channel metal-oxide-semiconductor (NMOS) devices with floating bodies, the high off-state current may be observed even with a negative gate voltage (V_{gf}) applied. This parasitic conduction has been described as a latch of the back gate transistor, triggered by the trapped charge in the oxide when it occurs at high dose levels [5], or as the result of impact ionization at moderate dose levels [1, 6-8]. However, the precise mechanism that causes this effect is still a matter of debate; it likely depends on the specific device characteristics as well as the operating conditions. A simulation-based model has been proposed recently [3]. This model shows how the combined effects of band-to-band tunneling (BBT) and trapped charge buildup in the buried oxide (BOX) affect the leakage current in irradiated fully-depleted SOI (FDSOI) devices, particularly for negative gate-to-source voltages [3].

In the second chapter, we describe the different models that have been published to explain the high current state in irradiated FDSOI devices. Moreover, we describe the contributions of this work to understanding the latch state and other TID effects in both irradiated planar FDSOI devices and FinFETs. The third chapter presents the fundamental operation of a bulk MOSFET device, explaining the limitations of the bulk technology and the motivation for an alternative technology, i.e., SOI technology. The fourth chapter presents an overview of radiation environments, in particular space environments. The basic radiation effects on SOI material are described. In chapters five and six, we validate experimentally the model proposed in [3]. We also report the effects of gate length and drain bias on the off state drain leakage current of irradiated FDSOI *n*-channel MOSFETs. The experimental results are interpreted using the model proposed in [3]. Indeed, for negative gate-source voltages, the drain leakage current increases with the drain voltage because the electric field in the gate-to-drain overlap region increases. The off-state current in these devices increases with total ionizing dose due to oxide trapped charge buildup in the buried oxide, enhanced by the BBT mechanism. The experimental data show that these effects are more significant for devices with shorter gate-lengths. Experimental and simulation results suggest that the BBT-generated holes are more likely to drift all the way from the drain to the source in shorter devices, enhancing the drain leakage current, while they tend to tunnel across the gate oxide in longer devices. Although the studied devices were fabricated in a FinFET technology, they were wide enough to behave like planar devices. Therefore, in order to extend the TID study to more advanced devices, results obtained from irradiated FinFETs with narrower fins (40 nm and 80 nm) and shorter gate length (100 nm) are reported. Previous work [7] reported that FinFETs

with very long gate length (10 μm) and narrower fin widths are more tolerant to TID than those with wider fin widths. Our results demonstrate that FinFETs fabricated in very deep submicron gate-length follow this trend. The dependence of threshold-voltage and subthreshold-swing degradation on fin width in irradiated 100-nm gate-length *n*-channel FinFETs is reported.

CHAPTER II

BACKGROUND AND OBJECTIVES

2.1 Background

Total ionizing dose effects cause positive charge to be trapped in the buried oxide in SOI devices, as evidenced by the negative shift of the back-gate *I-V* characteristics [8]. The positive trapped charge in the BOX can lead to a large increase in the drain-to-source leakage current via back-channel activation [8], as illustrated in Fig. 2.1 [2].

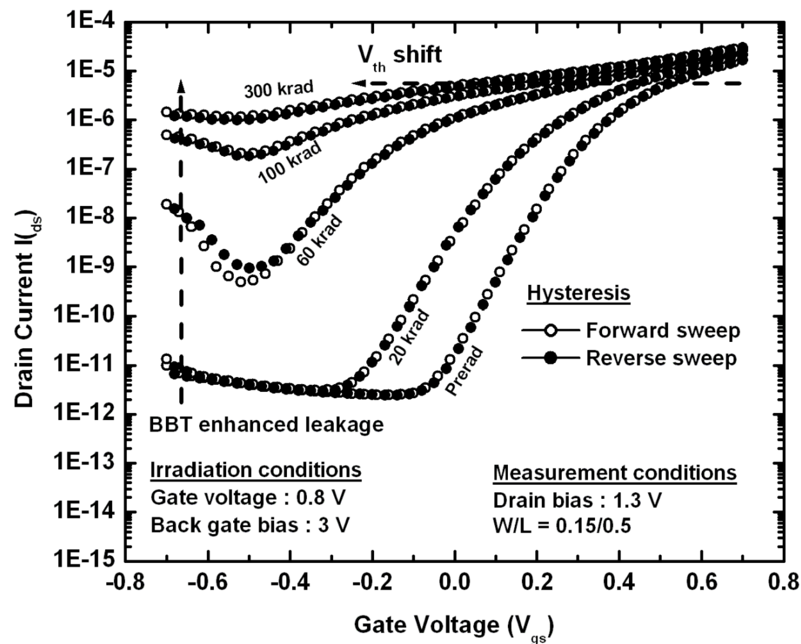

Fig. 2.1: Semilog plot of I_d-V_{gs} characteristics plotted as a function of x-ray dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min. The drain was biased at 1.3 V and the gate length was 0.5 μm [2].

Plotted in Fig. 2.1 are drain currents vs. V_{gf} characteristics for both forward and reverse gate voltage sweeps, obtained from measurements on irradiated mesa-isolated FDSOI devices [2]. The figure shows that, as dose levels increase for these NMOS de-

vices with floating bodies, high drain currents may be observed even with a negative gate voltage applied [2]. This "latch" state has been explained differently depending on the amount of trapped charge in the BOX and the value of the applied drain voltage.

2.1.1 *Leakage current enhancement at low dose levels and high drain voltages in irradiated FDSOI parts*

The parasitic conduction illustrated in the figure above has been attributed to a "latch" of the back gate transistor, triggered by impact ionization at moderate dose levels and high drain voltages [4, 8, 9]. At high drain voltages, a high electric field can appear at the front silicon surface in the gate-to-drain overlap region. The electric field accelerates electrons to very high speeds. These electrons create electron-hole pairs, through avalanching. The generated electrons are swept toward the drain, increasing the drain current, while the holes drift toward the floating body. The excess of holes in the floating body eventually forward biases the source/body junction [6]. Electron injection from the source into the body triggers the parasitic bipolar transistor conduction along the back channel where the potential is decreased by positive charge trapping in the BOX [6].

2.1.2 *Leakage current enhancement at high dose levels and low drain voltage in irradiated FDSOI parts*

The observed "latch" state illustrated in Fig. 2.1 has been ascribed to the positive trapped charge buildup in the buried oxide when it occurs at high dose levels and low drain bias [1, 6, 9, 10]. Simulated electron density in 50-nm FDSOI devices demonstrates how the trapped charge in the BOX is able to invert the back channel, producing a conductive path along the Si/BOX interface [9]. The front gate threshold voltage shift is consistent with the coupling of trapped charge in the buried oxide to front-gate threshold

voltage shifts [8]. The variation of both threshold voltages is expressed by the following equation [8]:

$$\Delta V_{Tf} = k\Delta \tag{2.1}$$

where k is the coupling coefficient, and ΔV_{Tf} and ΔV_{Tb} are the threshold voltage shifts of the front and back gates, respectively. k is given by:

$$k = \frac{C_{Si} C_{box}}{C_{fox}(C_{Si} + C_{box} + C_{it})} \tag{2.2}$$

where C_{it} is the capacitance due to interface traps, and C_{fox} and C_{Box} are the front gate oxide capacitance and the buried oxide capacitance, respectively.

2.1.3 *Leakage current enhancement at low dose level and low drain voltage in irradiated FDSOI parts*

A model for the off-state leakage current in irradiated FDSOI MOSFETs, supported by 2D simulations, has been proposed recently. This model shows how the combined effects of band-to-band tunneling (BBT) and trapped charge buildup in the buried oxide (BOX) affect the leakage current in irradiated FDSOI devices, particularly for negative gate-to-source voltages [3].

Fig. 2.2 illustrates the processes proposed in reference [3] to explain the characteristics demonstrated in Fig. 2.1. When the gate-to-drain voltage becomes increasingly negative, a high electric field is created at the surface of the gate-to-drain overlap region. This results in a BBT process that increases the gate-induced drain leakage (GIDL) current

[11]. The high electric field generates electron-hole pairs via band-to-band tunneling, as shown in Fig. 4.3 [3].

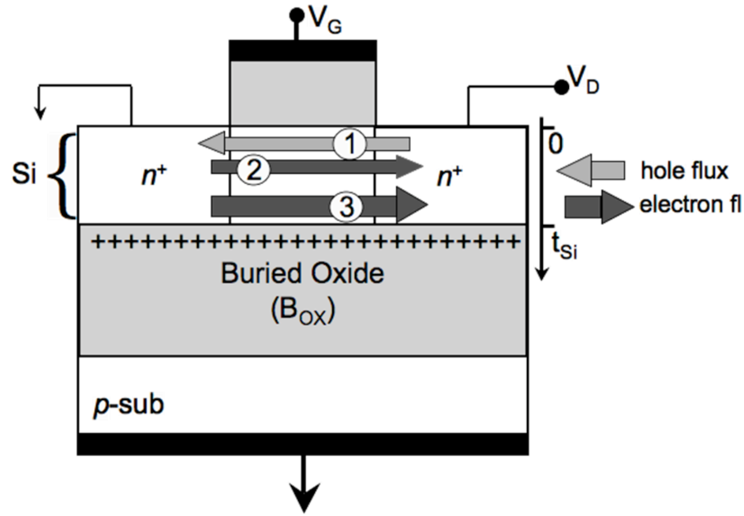

Fig. 2.2: Cross section illustrating the three currents related to the drain current increase in an irradiated FDSOI transistor [3]. Arrow 1 represents the flux of BBT generated holes into the body. Arrow 2 represents the electrons back-injected into the body caused by the source-to-body barrier decrease and arrow 3 represents the flux of electrons that arises as a result of the positive trapped charge buildup in the buried oxide via back-channel activation [3].

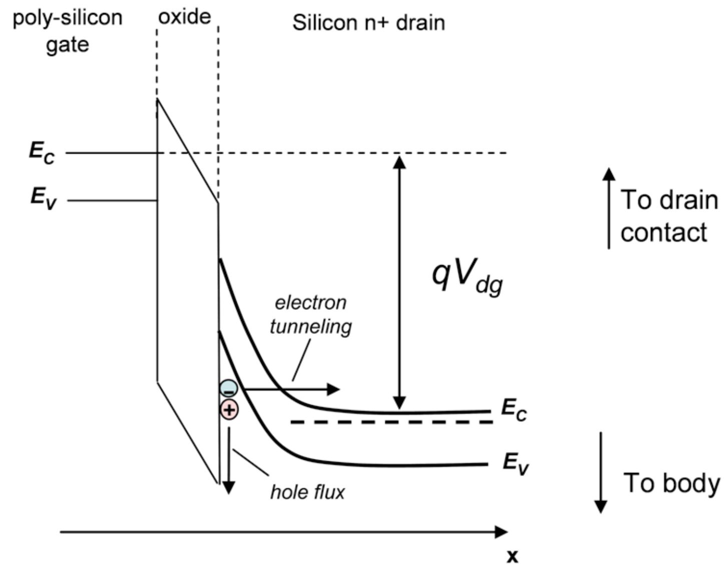

Fig. 2.3: Energy band diagram corresponding to the BBT process [3].

As electrons drift toward the drain, the holes move into the body (arrow labeled "1" in Fig. 2.2). If the transporting holes reach the source, the body-to-source junction becomes forward biased, allowing the injection of electrons into the body (arrow labeled "2" in Fig. 2.2). The last process, illustrated by the arrow labeled "3", represents the primary component of the increased drain leakage current. According to the model, the combined effects of radiation-induced trapped charge in the BOX and the increase in body potential relative to the source reduce the back-gate threshold voltage through the body effect, thereby increasing electron flow from source to drain along the back-side interface [3].

2.2 Objectives

The observed high current state is still an open question. While the previous models are able to explain the phenomena at limited ranges of dose levels and drain voltages, or restricting the analysis to simulations, more experimental work, supported by simulation, is required to extend the understanding of the phenomena to low dose levels and low drain voltages.

In this thesis, we examine the total dose response of planar fully depleted SOI MOSFETs fabricated in a FinFET technology as functions of both drain bias and gate length. The I_D for negative V_{gf} increases with the drain bias and decreases with the gate length. The model proposed in [3] is used to explain the new experimental results reported here, related to both the drain bias and gate length dependencies in irradiated fully depleted devices. The mechanisms that are involved include: band-to-band tunneling (BBT), positive charge trapping in the BOX, direct tunneling through the thin gate oxide, and short-channel effects.

In order to extend our TID understanding to more advanced FinFETs, devices with narrower fins (40 nm and 80 nm) and shorter gate lengths (100 nm) were critically studied. Both the threshold-voltage shift and the subthreshold swing (SS) were analyzed as functions of device dimensions and total dose. The threshold voltage shift increases with dose for wider devices, while the shifts reported for narrower devices are very small. Devices with wider fins require more voltage to turn on the channel for increasing dose levels, whereas the SS barely changes with dose for narrower devices.

CHAPTER III

SILICON ON INSULATOR (SOI) TECHNOLOGY

The first metal-oxide-semiconductor field-effect transistor (MOSFET) was a semiconductor-on-insulator (SOI) device, according to the historical patent of Lilienfeld dated from 1926 [12]. The first working MOSFET was realized only in 1960 when technology permitted the fabrication of good quality gate oxides [12]. SOI technology came into the picture again by the 1990s, and was good enough to be used in personal-computer microprocessors by the late 20th century [12]. In this chapter we talk about the basic operation of a bulk MOSFET device. Limits of bulk technology are cited, demonstrating the motivation for SOI technology. We introduce the SOI technology, explaining the physics of SOI devices. A brief discussion about future SOI devices is presented.

3.1 Bulk technology

CMOS integrated circuits are usually built on bulk silicon substrates. This is mainly because of the ability to grow good quality oxide on silicon [13]. In general, a MOSFET has four terminals: gate, drain, source and substrate. According to the applied gate voltage V_g, the device can be on or off. When $|V_g|$ is high enough to create an inversion layer in the channel of a MOSFET, the drain voltage $|V_D|$ can accelerate these carriers (electrons for a *n*-channel MOSFET and holes for a p-channel MOSFET) between the source and the drain. The device is conductive when $|V_g| \geq |V_T|$, where V_T is the threshold voltage. The subsequent analysis in this thesis is presented in terms of the *n*-channel MOS-

FET (or *n*-channel SOI MOSFET) because of its greater importance. Three operating regimes can be considered for a MOSFET [13]. In the Ohmic region, for $V_D \leq V_g - V_T$, I_D is described by [13]:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right] \quad , \tag{3.1}$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W is the channel width, and L is the channel length. As V_D increases beyond the voltage $V_g - V_T$, the current saturates and the drain current is expressed by the equation (3.2):

$$I_{Dsat} = \mu_n C_{ox} \frac{W}{2L}(V_G - V_T)^2 \quad , \tag{3.2}$$

where I_{Dsat} is the drain saturation current. A MOSFET can be conductive even though the gate voltage is lower than the threshold voltage. In most instances, this subthreshold conduction is part of the normal device operation and it is described by the subthreshold swing (typically given in mV/decade). The current below threshold can also be large because of (among other reasons): impact ionization for high drain voltages [14], band-to-band tunneling [14], direct tunneling for very thin oxides [15], or latchup [12]. Latchup is one of the most hazardous effects for bulk MOSFETs because they are fabricated in such a way that the active area of the device can interact directly with the substrate. Latchup consists of undesirable triggering of PNPN thyristor structures intrinsically present in bulk MOSFETs. Fig. 3.1 shows a latchup path in a bulk CMOS inverter. The figure also shows the parasitic capacitance between the source and drain regions and the substrate.

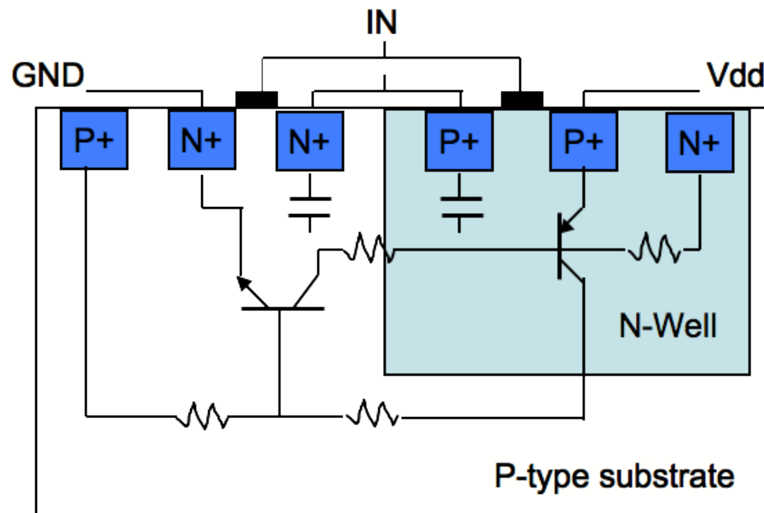

Fig. 3.1: Cross section showing the latchup path in bulk CMOS inverter [12].

3.2 SOI technology

For silicon-on-insulator (SOI) technology, a thick buried oxide layer, usually silicon dioxide (SiO_2), is inserted below the active region to prevent parasitic effects experienced in bulk devices, in particular latchup, by isolating the active area from the substrate. Latchup is ruled out because there is no current path to the substrate. The parasitic capacitors between the source and drain and the substrate are potentially reduced thanks to the buried oxide layer. Thereby, the device is faster [12]. Fig. 3.2 shows an SOI CMOS inverter.

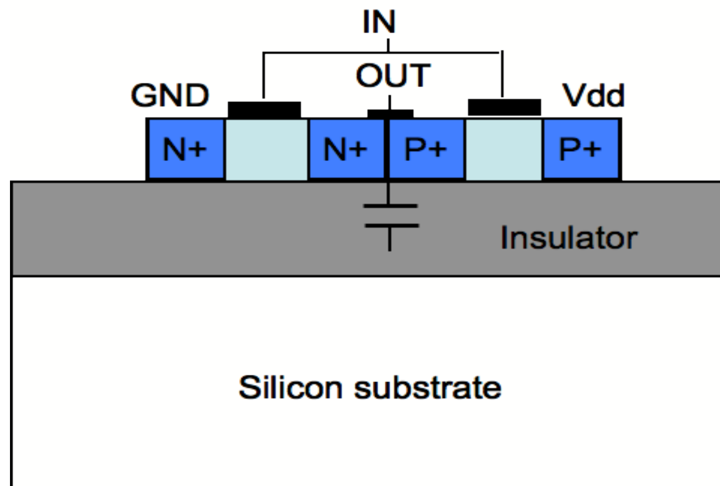

Fig. 3.2: Cross section of an SOI CMOS inverter [12].

The functioning of an SOI device is similar to its bulk counterpart; however, tasks can be completed faster and with lower energy consumption.

3.2.1 *Planar devices*

3.2.1.1 Partially depleted devices

In an SOI MOSFET, the thickness of the silicon film determines the physics of the device operation. When the silicon film thickness t_{si} in the channel is larger than the maximum depletion width x_{dmax}, where x_{dmax} is expressed by equation (3.3), the device is considered to be partially depleted (PD) [12].

$$x_{d\,\max} = \sqrt{\frac{4\varepsilon_{si}\phi_F}{qN_a}}, \tag{3.3}$$

where ε_{si} is the silicon permittivity, ϕ_F is the Fermi potential (see equation (3.4)), N_a is the silicon film doping per unit volume and q is the elementary charge [12].

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{3.4}$$

where k is the Boltzmann constant, T is the temperature in K and n_i is the intrinsic carrier concentration per unit volume [12].

3.2.1.2 Fully depleted devices

When t_{si} is lower than x_{dmax}, the silicon film is completely depleted and the device is considered to be fully depleted (FD). In this case, there is an interaction between the front interface and the back interface, i.e., a coupling effect. In other words, applying a back

gate voltage can affect the top-gate electrical characteristics, in particular the front threshold voltage.

In the absence of a body contact, i.e., a silicon film contact, SOI devices exhibit floating body effects. These effects can be seen in PD as well as in FD SOI devices. They can be explained by several scenarios. One of these contexts is the open-base NPN bipolar transistor between the drain and source in an n-channel SOI device. Among several unwanted parasitic effects, such as short channel effects [16], these body effects can be related to the insufficient control of the gate over the body in an SOI device. In this direction, new SOI device architectures were brought to light, focusing on increased control of the body region.

3.2.2 *FinFET devices*

In an unceasing attempt to increase current drive, control short channel effects, and improve total ionizing dose (TID) tolerance, SOI MOS transistors have developed from planar single gate SOI MOS devices into three-dimensional devices with multi gate structures.

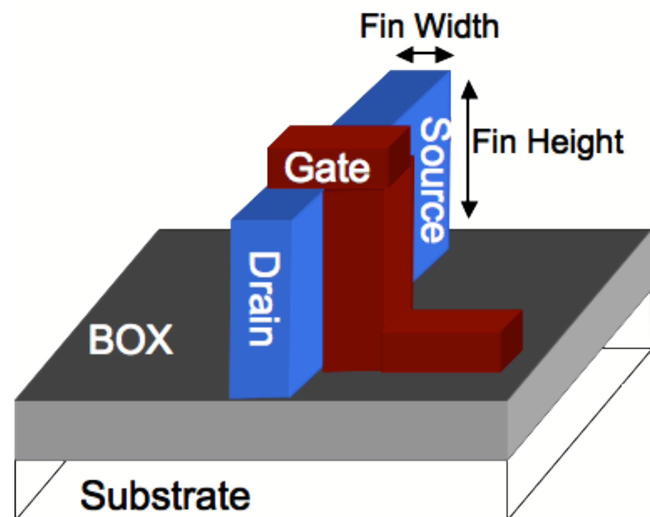

Fig. 3.3: Finfet MOS structure [12].

Fig. 3.3 shows the structure of a FinFET device, one of the first multi-gate SOI MOS devices to be realized [17]. One of the most promising applications of SOI devices is in zero capacitance random access memory cells (ZRAMs). The idea behind this is using the charging and discharging of the floating body (silicon film) to store the logic states 1 and 0 instead of using an additional capacitance as used in a classical dynamic random access memory (DRAM). In this thesis we use devices fabricated in a FinFET technology. Devices with wider fins behave more like planar devices while devices with narrower fins behave more like FinFETs devices. Both fin dimensions are investigated in this work.

This section was dedicated to the functioning of SOI devices without considering radiation effects. In order to evaluate the TID response of SOI devices in harsh environments, a detailed study of these extreme environments and how they affect the device operation is required.

CHAPTER IV

RADIATION BASICS AND BACKGROUND OF SOI DEVICES

Electronics in space are exposed to different types of ionizing radiation. Ionizing radiation interacts with the matter, creating electron-hole pairs in both semiconductors and insulators. The cumulative effects of the absorbed energy are called total ionizing dose (TID) effects, which are considered to be a serious reliability problem for MOS devices. This chapter focuses in more detail on total dose effects in SOI devices. We start the chapter with an overview of radiation environments, especially space environments. The basics of radiation effects on SOI MOSFET devices will be critically studied.

4.1 Radiation environments

4.1.1 *Space*

The space radiation environment is composed of charged and uncharged particles. Charged particles lead to both ionization and displacement damage, while uncharged particles produced only displacement damage through their direct interactions. Displacement damage refers to the absence of an atom from its normal lattice position due to an incident high energetic particle, which creates vacancies and interstitials [18]. The space environment is distinguished by its very low dose rates [19]. It is impossible to give a single description of the space radiation environment, as all kind of charged and uncharged particles with very different fluences and fluxes can be found in space, depending on the particular mission. The fluence is the number of particles dN that penetrates a sphere having

a section of *dS* equal to unity [20], i.e., equation (4.1) [20]. The flux is the number of particles crossing a surface per unit time [20]. The flux is expressed by equation (4.2) [20].

$$Fluence: \phi = \frac{dN}{dS}(cm^{-2}), \tag{4.1}$$

$$Flux: \dot{\phi} = \frac{d\phi}{dt}(cm^{-2}.s^{-1}), \tag{4.2}$$

We can distinguish three categories of radiation in space [21]. First, there are particles with high flux (~10^{12} particles/cm^2.s) and low energy (~10^{-2} MeV), which are easy to stop because of their low energies. These particles are mainly electrons, protons and helium. They are usually found in the solar wind [21, 22].

Second, there are particles with very low flux (~10^{-2} particles/cm^2.s) and very high energy (~10^6 MeV). This type of particle has a low probability of interaction with matter. This category of particles consists of protons and heavy ions and is found generally in cosmic rays [21, 22].

Finally, there are particles with intermediate flux and energy. This category of particles consists mostly of electrons and protons. The main sources for these particles are the Van-Allen Belts and solar flares [21, 22]. The particles corresponding to this class are considered to be very harmful to electronics in space as the particles are numerous and hard to stop [21].

4.1.2 *ARACOR*

In order to predict the total dose response of a device in a radiation environment, space for instance, practical laboratory measurements are used to simulate the radiation

environment of interest. Several radiation sources can be used for this purpose such as ^{60}Co (γ-rays) and x-ray generators. An ARACOR model 4100 semiconductor irradiator was used in this work. The ARACOR x-ray test system is used to investigate TID effects on individual microelectronic devices. This system produces 10 keV x-rays energies with dose rates ranging from 2 to 200 krad(Si)/min. The system is capable of providing x-ray characterization of fabricated die or packaged devices with lids removed. Inside the ARACOR is an x-ray tube. An electron gun inside the tube shoots high-energy electrons at a target made of heavy atoms. X-rays emerge as a result of the incident electrons bombarding the target [23].

4.2 Basics of radiation effects

4.2.1 *Interaction radiation-matter*

X-rays are electromagnetic radiation that can be produced by "Bremsstrahlung" atomic process in packets of energy (hν) called "photons" [23]. Photons interact with target atoms through the photoelectric effect, Compton scattering and pair (electron-hole) production [24]. When the incident energetic photon transfers all of its energy to an inner shell electron of the target atom, an electron or a photoelectron is ejected with a kinetic energy equal to that of the incident photon minus the electron ionization energy [25]. The ionization energy is the required energy to extract an electron from a neutral atom. In the case of the Compton effect, only a part of the incident photon energy (hν) is transferred to a peripheral electron. The photon is changed so that it has a lower energy (hν') [25, 21]. Electron-hole pairs are created when the incident photon energy is very high. Fig. 3.1 summarizes the three mechanisms as functions of the photon energy and the atomic number (Z) of the target atom. In our case the primary photon-matter interaction is through

the photoelectric effect as the x-ray energies given by the ARACOR irradiator are 10 keV.

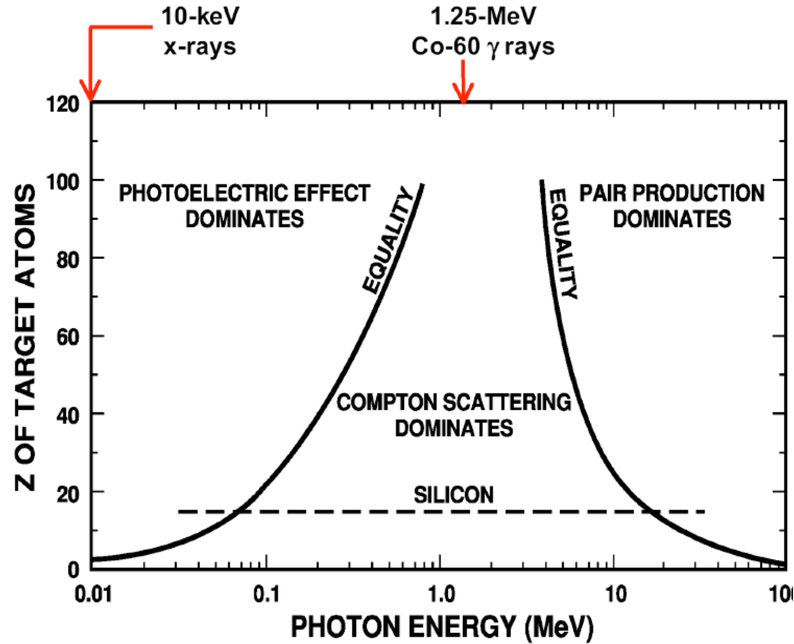

Fig. 4.1: Illustration of three photon interactions as function of the photon energy and the atomic number of the traget atom [25, 34].

4.2.2 *Generalities and units*

The absorbed dose D is defined as the ratio of dE to dm, where dE is the energy deposited by the radiation in the mass dm [26].

$$D = \frac{dE}{dm}(Gy), \tag{4.3}$$

The SI dose unity is Gray (G), but the old unit "rad" is still used in many situations, including this work [26].

1 Gy = 1 $J.Kg^{-1}$ 1 Gy = 100 rad

The dose rate is defined as the derivative of the dose with respect to time. It is expressed in $Gy.s^{-1}$.

$$\dot{D} = \frac{dD}{dt}(Gy.s^{-1}), \tag{4.4}$$

4.2.3 *Evolution of charge in the oxide*

Insulators are the most sensitive device regions for TID irradiation. The charge created in an irradiated insulator may have a significant effect, as the original free charge density in an insulator is very low [21]. In the subsequent paragraphs we discuss irradiation of SiO_2. Immediately after the charge creation in an irradiated material, recombination between a portion of the created electrons and holes takes place [21]. Electrons and holes that escape recombination drift in opposite directions (if there is any electric field). When the electric field is very low, almost all the electrons and holes recombine. As electron mobility is relatively high (μ_n = 20 cm^2 (Vs)$^{-1}$ for SiO_2) [13], they are very quickly swept from the oxide. Holes on the other hand, with very low mobility ($\mu_p \sim 10^{-8}$ cm^2 (Vs)$^{-1}$ for SiO_2) [13], move very slowly and often are trapped in the oxide.

4.2.4 *Defects in the oxide*

Silicon oxide is the most important material after silicon that is used in integrated circuits. The oxide is, among others: the gate material in MOS devices, the isolation material for local oxidation of silicon (LOCOS), fill for shallow trench isolation (STI), and the buried oxide (BOX) used in SOI devices. Even though good quality oxides can be made, defects can affect the electrical properties of the oxide. For example, defects may trap some of the holes that escape from the initial recombination. The holes that are trapped in these defects form fixed or mobile charge that modifies the electrical characteristics of the device. A detailed review of this charge will be given in the next section.

4.3 Total ionizing dose (TID) effects

4.3.1 *Charge in the oxide*

Five types of trapped charges can be found in an irradiated gate oxide. This charge can be divided into two groups depending on whether the trapped charge is able to communicate with the silicon. In the first group, we find the positive fixed charge (Q_f) mostly induced by processing [13, 21]. Then there is the mobile charge (Q_m) exhibited in the form of alkaline ions, such as sodium ions (Na^+). Irradiating a device induces another component of charge (positive) called oxide trapped charge (Q_{ot}). Q_{ot} is a direct result of hole trapping in the oxide after the initial recombination. Interface-trapped charge (Q_{it}) is charge in electronic states at the SiO_2/Si interface whose charge state is determined by the surface potential [21]. The last form of charge in the oxide is border traps [27]. A fine line separates the border traps from the classical interface traps as they are very (3 nm) close to the interface Si/SiO_2 and can communicate with the silicon. However, border traps are structurally related to oxide trapped charge.

4.3.2 *Threshold voltage shift*

- **MOSFETs**

As radiation-induced charge builds up in the gate oxide of a MOSFET, the threshold voltage shifts. Indeed, adding positive charge in the oxide by irradiation produces electrostatic effects equivalent to applying a positive gate voltage. Positive charge in the gate oxide of an *n*-channel MOSFET can reduce the threshold voltage such that the device is turned on even when no voltage is applied to the gate. Parasitic current also may flow in regions of the silicon underneath the STI, contributing to the source-drain leakage current and adding to the conventional drain current.

• **SOI MOSFETs**

SOI MOSFETs are fabricated with a buried oxide (BOX) layer separating the active device from the substrate. Compared to bulk-Si MOSFETs, SOI devices exhibit superior single event upset (SEU) tolerance and performance, due to the reduced collection volume [1]. Indeed, the BOX in SOI devices plays a major role in reducing the drain/body and the source/body junction areas. Single event upset is a transient local effect that consists of corrupting an electrical state [28].

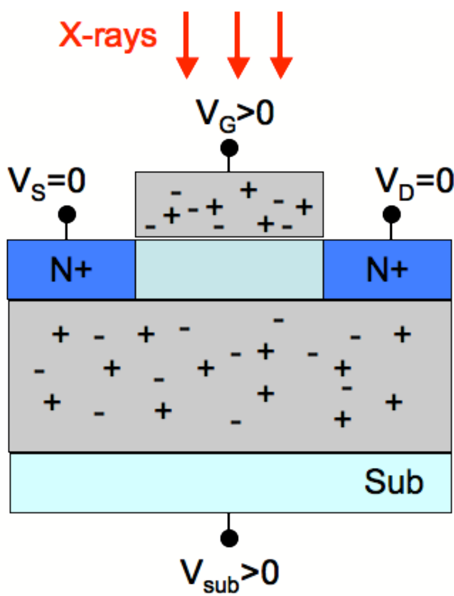

Fig. 4.2.a: Creation of pair's electron hole in the oxide areas immediately after irradiation exposure (t_0).

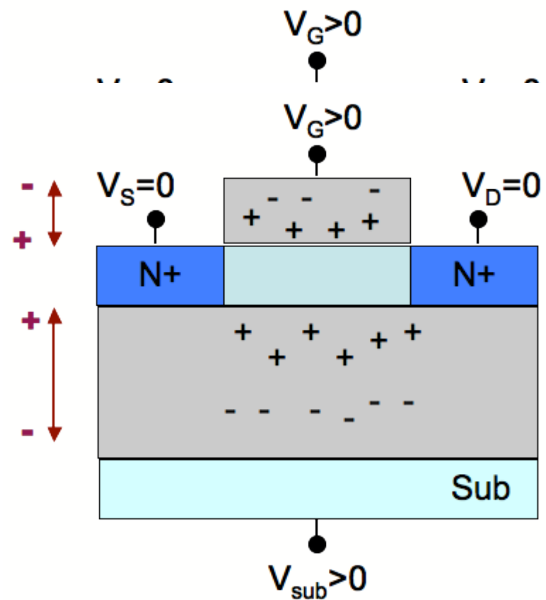

Fig. 4.2.b: Transport of carriers according to the electric fields orientation in the oxide areas ($t_1 > t_0$).

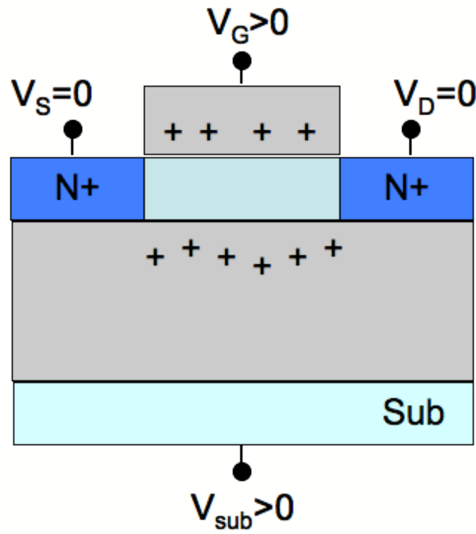

Fig. 4.2.c: Electrons are swept quickly toward the positive potential regions. Some of the holes are trapped in the oxide regions ($t_2>t_1$).

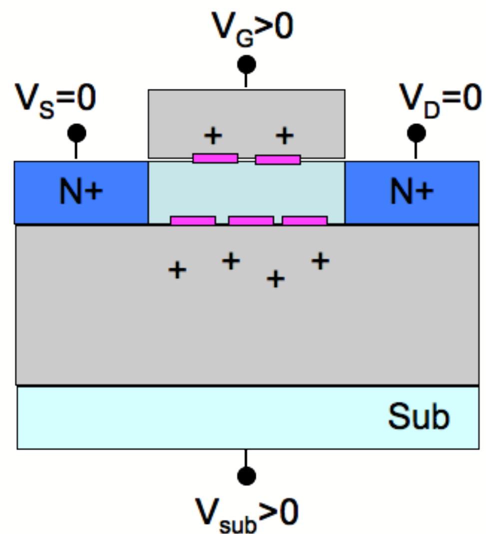

Fig. 4.2.d: Some of the trapped holes anneal by tunneling or thermal emission.

In this work, we consider total dose effects rather than transient effects. Plotted in Fig. 4.2 is the evolution of charge in the gate oxide and the buried oxide (BOX) as functions of time in an irradiated SOI MOSFET. All planar devices in this work were irradiated with a positive back gate voltage of 3 V. Hence, the positive substrate voltage in the figures above. As the figures show, in an irradiated SOIMOSFET not only the gate oxide is considered but the BOX layer also has to be taken into account. An n-channel SOI MOSFET is more vulnerable to TID effects than an n-channel bulk MOSFET because of charge trapping in the BOX layer. Charge trapped in the BOX can invert the back channel and produce coupling effects between the front and back gates in FD SOI devices. If there is sufficient charge, high leakage current appears even for negative gate voltages. The following chapters examine this phenomenon experimentally. The gate length and drain bias dependencies are examined experimentally and supported with simulations. On

the other hand, experiments on FinFETs showed higher TID tolerance than planar devices. Subsequent chapters describe irradiation results on both technologies, i.e., planar devices and FinFETs.

CHAPTER V

EXPERIMENTAL RESULTS

In this chapter we describe the experimental details for planar SOI MOSFETs and FinFETs. TID results for both technologies are presented. Gate length and drain bias dependencies are investigated for planar devices, while fin width dependency is examined for FinFETs.

5.1 Experimental details

5.1.1 *Device details*

Standard UNIBOND® SOI wafers were used as starting material. The silicon film (SOI) thickness and the BOX thickness were 58 nm and 150 nm, respectively.

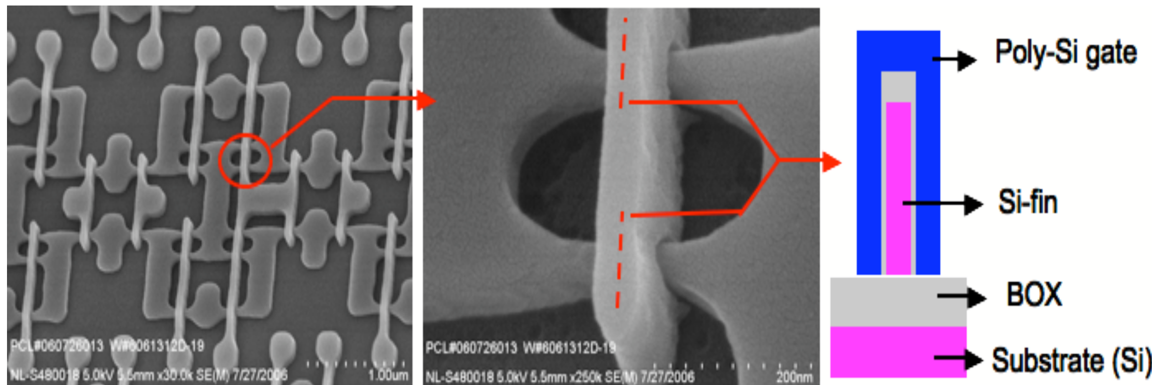

Fig. 5.1: Scanning Electron Microscopy (SEM) of an SRAM cell built in a finFET technology (on the left). One of the mesa-isolated finFETs used in this work, with 2 fins, is illustrated in the middle of the figure. A cross section of the finFET is displayed on the right.

Plotted in Fig. 5.1, on the left, is a scanning electron microscope (SEM) picture of a Static Random Access Memory (SRAM) built in a FinFET technology. The mesa-isolated fully depleted (FD) FinFET presented in the middle of Fig. 5.1 is one of the de-

vices used in this work. An illustrative schematic of the cross section of the FinFET is displayed on the right of the figure. The silicon top layer was *p*-type (2 × 10^{15}/cm^3). These devices were fabricated in a FinFET technology. Both devices with wider and narrower fin widths were investigated. Devices with sufficiently wide channels behave like mesa-isolated planar devices, while samples with narrower fin widths behave like FinFET devices. After active patterning, the wafers went through a 700 °C H_2 anneal at 600 mTorr to smooth the etched surface and round the Si corners for mesa isolation. A 2-nm SiO_2 gate dielectric was grown by in-situ steam oxidation at 975 °C. A 7 nm TiSiN gate-electrode layer was deposited by LPCVD and capped with 100 nm of poly-Si.

5.1.2 *Experiments description*

Both the planar mesa-isolated SOI devices and FinFETs were exposed to 10 keV x-rays in an ARACOR x-ray system (see Fig. 5.2).

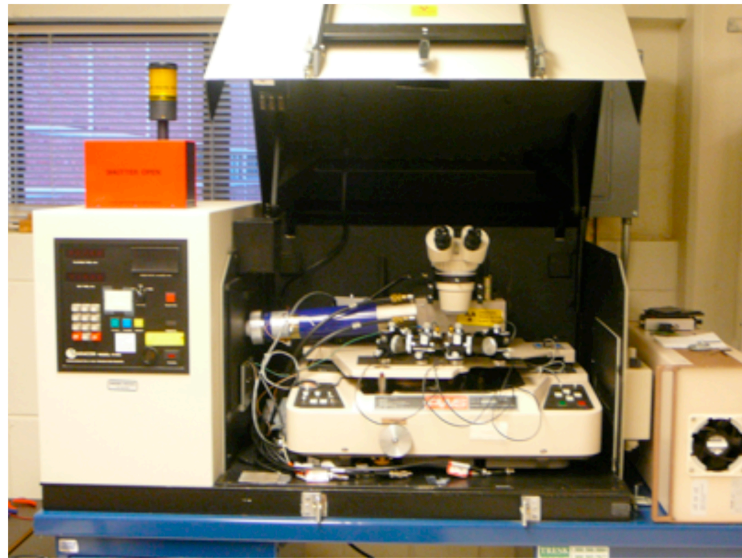

Fig. 5.2: ARACOR x-ray system (model 4100) used in this work.

All irradiations were conducted at a dose rate of 31.5 krad(SiO_2)/min. Post irradiation current-voltage (I_d-V_{gf}) characteristics were measured using an Agilent 4156 semiconduc-

tor parameter analyzer on un-packaged wafers. In-situ irradiations and *I-V* measurements were performed without removing the probes from the wafers. This reduced variations due to probe contact, thereby yielding better reproducibility in the results.

5.1.2.1 Planar devices

Planar devices were irradiated with floating body, a front gate voltage of 0.8 V, a back gate voltage of 3 V, and both drain and source grounded. The positive voltage was applied to the back gate to accelerate trapped charge buildup in the buried oxide by inverting the backside channel. To evaluate the proposed model for low dose levels and low drain voltages [3] described in the second chapter, a 0.5 μm gate length device was irradiated up to 300 krad(SiO_2) and was measured after each irradiation step at a drain bias of 1.3 V. In order to study the drain bias dependence, a 0.5 μm gate length device was irradiated up to a total dose of 100 krad(SiO_2). Post-irradiation measurements were performed after each irradiation step for several drain biases up to 1.6 V. The gate length dependence was studied using three samples with different gate lengths (0.5 μm, 1 μm, and 10 μm). These devices were irradiated separately up to 100 krad(SiO_2). Post irradiation measurements were performed after each irradiation step for a drain bias of 1.4 V. All planar devices used in this work have a gate width of 0.15 μm.

5.1.2.2 FinFETs

Narrower fin width FD SOI devices were irradiated as well to study the TID response of FinFET devices. 40 nm and 80 nm fin-width FinFETs, each composed of 20 fins in parallel, were investigated to study the fin-width dependency. The devices were irradiated with an off-state configuration: floating body, grounded front and back gates,

grounded source and a drain voltage of 1 V. Samples were irradiated to a cumulative dose of 500 krad(SiO_2).

5.2 Experimental results

5.2.1 *TID effects on planar FDSOI devices*

5.2.1.1 Drain leakage current enhancement in irradiated planar FDSOI devices

Plotted above in Fig. 2.1 are drain currents vs. front-gate voltage V_{gf} characteristics for a 0.5 μm gate length FDSOI *n*-channel MOSFET. For these measurements, the drain voltage was 1.3 V. Even though the gate oxide is very thin (2 nm), the front-gate threshold voltage (V_{Tf}) shifts significantly with total dose, due to electrical coupling between the channel and the radiation-induced charge in the BOX. The drain-source leakage current also increases for negative gate voltages (less than the threshold voltage). The increase in leakage current is attributed to the combined effects of BBT-generated carrier flux and the charge buildup in the BOX, as illustrated in Fig. 2.2. The results in Fig. 2.1 also reveal no hysteresis since the forward and the reverse gate sweep measurements produce almost the same results. These hysteresis measurements were performed to study the vulnerability of the FDSOI devices to impact ionization. It has been shown by Schwank *et* al. [1] that hysteresis in the *I-V* curves is one of the signatures of impact ionization as the gate voltage is swept from negative to positive and from positive to negative voltages.

5.2.1.2 Drain bias dependence in irradiated planar FDSOI devices

Another set of experiments was performed on a 0.5 μm device to study the drain bias dependence. Measurements were made for drain biases up to 1.6 V with a drain voltage increment of 200 mV.

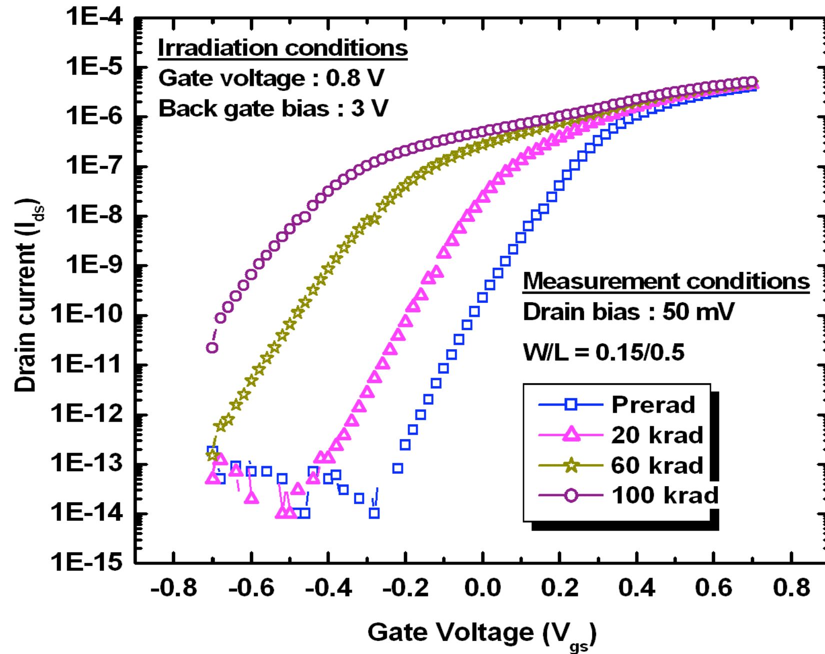

Fig. 5.3: Semi log plot of Id-Vgf characteristics at various x-ray doses. The drain was biased at 50 mV and the gate length is 0.5 μm [2].

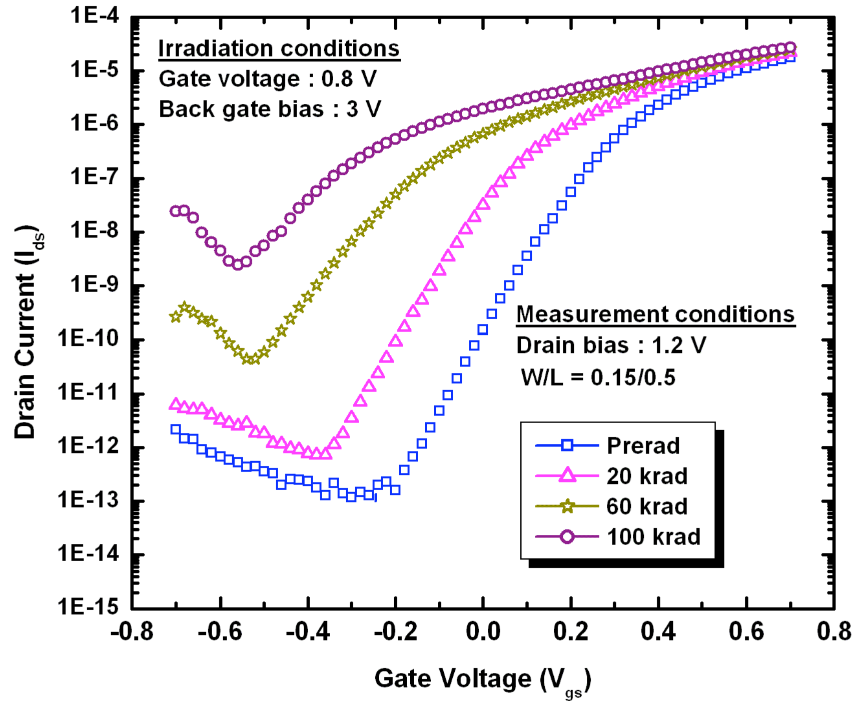

Fig. 5.4: Semi log plot of I_d-V_{gf} characteristics at various x-ray doses. The drain was biased at 1.2 V and the gate length is 0.5 µm [2].

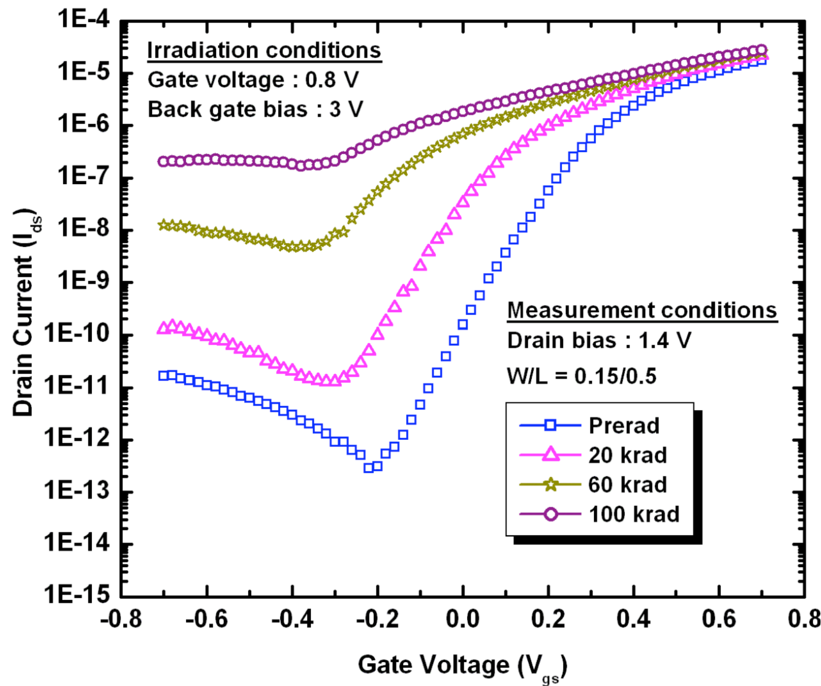

Fig. 5.5: Semi log plot of I_d-V_{gf} characteristics at various x-ray doses. The drain was biased at 1.4 V and the gate length is 0.5 µm [2].

For low drain biases (50 mV to 1 V), the response is dominated by a monotonic negative threshold voltage shift as the dose increases. This effect can be observed in Fig. 5.3, which plots the radiation response for a drain voltage of 50 mV. Fig. 5.4 shows that for higher drain biases, 1.2 V in this set of curves, the drain leakage current increases significantly. Fig. 5.5 shows the high current state described in the second chapter for negative gate voltages. This latter state appears even earlier at higher drain biases (e.g., V_d = 1.6 V).

5.2.1.3 Gate length dependence in irradiated planar FDSOI devices

Another important result observed in the experimental data is that the shorter gate length devices are more susceptible to radiation damage (i.e., greater V_{Tf} shifts and increase in off-state leakage currents are observed in the L_g = 0.5 μm devices).

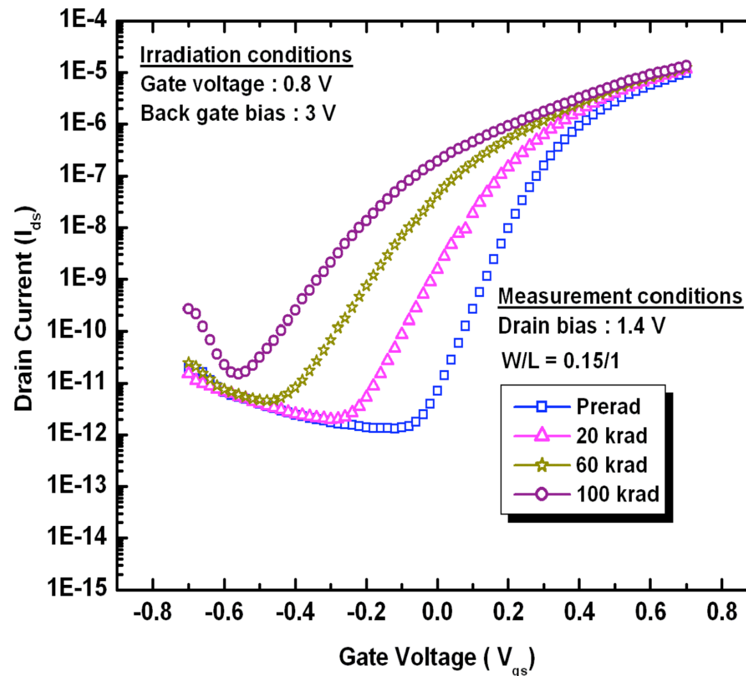

Fig. 5.6: Semi log plot of I_d-V_{gf} characteristics at various x-ray doses. The drain was biased at 1.4 V and the gate length is 1 μm [2].

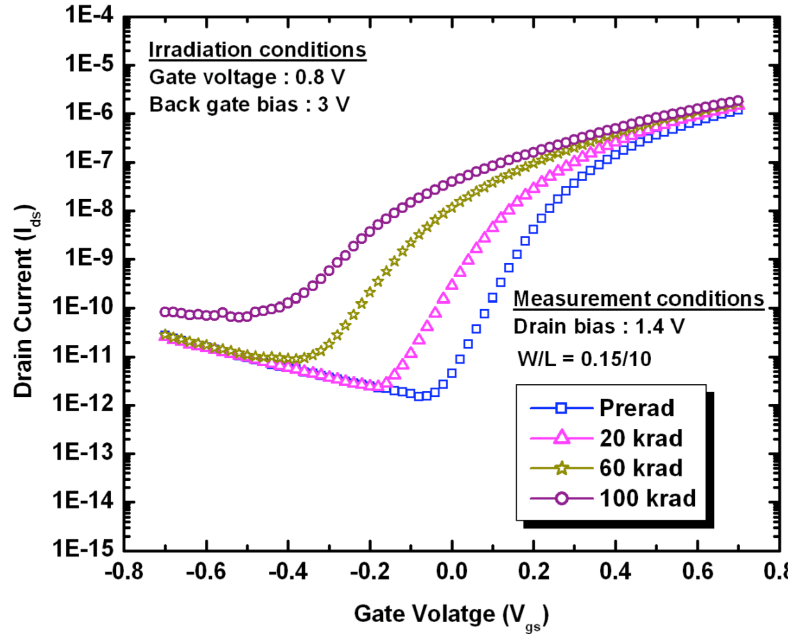

Fig. 5.7: Semi log plot of I_d-V_{gf} characteristics at various x-ray doses. The drain was biased at 1.4 V and the gate length is 10 µm [2].

Two additional sets of irradiations were performed on 1 µm and 10 µm gate length devices to compare the total dose responses of these devices as a function of gate length. As Figs. 5.5, 5.6 and 5.7 show, at a dose of 100 krad(SiO_2), a front gate bias of -0.7 V, and a drain bias of 1.4 V, the leakage current for the device having a gate length of 0.5 µm is 200 nA, while it is 263 pA for a device having a gate length of 1 µm and 83 pA for a device having a gate length of 10 µm. This higher leakage current for devices with shorter channels is consistent with experimental results presented in previous works [8, 10]. This phenomenon is analyzed in the following chapter.

5.2.2 *TID effects on FinFETs*

Recent works reported that very wide FinFETs behave like planar SOI transistors, where the coupling effects of the front and the back channel are dominant in the total

dose response [2]. The TID response of these devices depends on the device geometry, as well as the process details [2]. In other work, narrower FinFETs with very long channels (10 μm) exhibited higher tolerance to TID [7]. This resistance to TID-induced degradation exists because the additional lateral gates provide a high degree of control over the potential in the body [7]. In this section, we investigate mesa-isolated FD FinFETs with much shorter gate lengths (100 nm) than those considered in [7]. We examine the threshold voltage shift and the subthreshold swing (SS) of these devices functions of dose and fin width. Figs 5.8 and 5.9 plot the I_d-V_{gs} curves before exposure and after each irradiation step for *n*-channel FD FinFETs having a gate length of 100 nm and fin widths of 40 nm and 80 nm. For these measurements, the drain voltage was 1 V, the back gate (substrate) and source were grounded and the *p*-type body was floating. As the figures indicate, these advanced technology parts exhibit front-gate threshold voltage (V_{Tf}) shifts, which are induced by electrical coupling to radiation-induced charge buildup in the BOX [1, 2, 4, 6, 8-10]. By comparing the results in Figs. 5.8 and 5.9, one can observe that the threshold voltage shift for the device with a fin width of 80 nm (Fig. 5.9), is significantly higher than the threshold voltage shift exhibited in the 40 nm fin-width device (Fig. 5.8). An 80-nm fin-width device is more vulnerable to TID effects. The fin-width dependence, which is consistent with results reported in previous studies [7], is discussed in more detail in the following chapter.

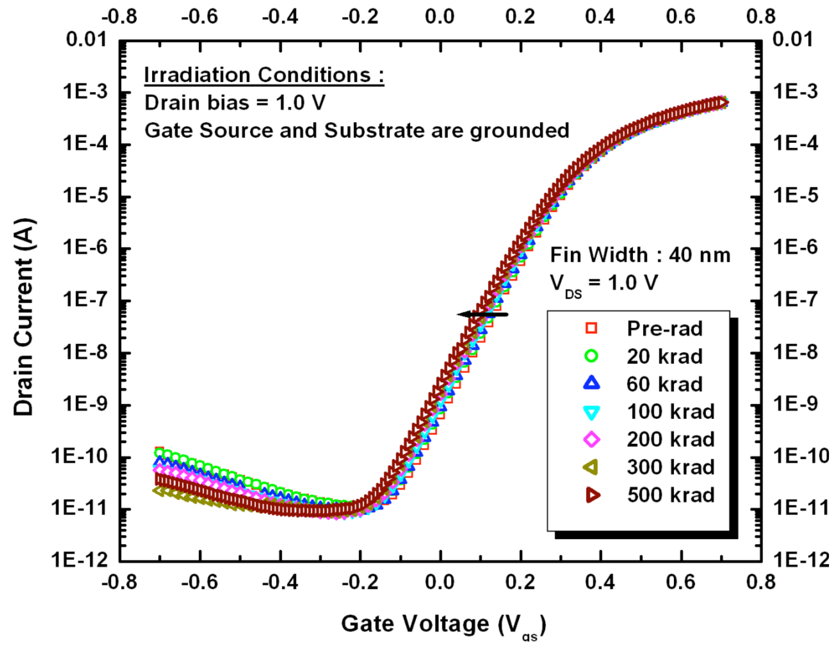

Fig. 5.8: Semilog plot of I_d-V_{gs} characteristics as a function of x-ray dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min. The drain was biased at 1.0 V and the fin width is 40 nm. The finFET includes 20 fins.

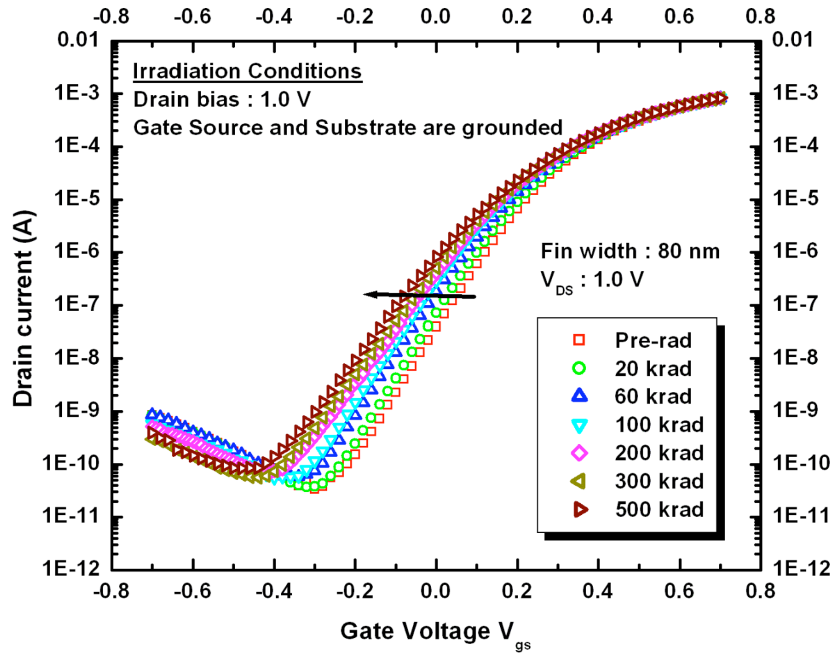

Fig. 5.9: Semilog plot of I_d-V_{gs} characteristics as a function of x-ray dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min. The drain was biased at 1.0 V and the fin width is 80 nm. The finFET includes 20 fins.

Conclusion

Four main experiments were presented in this chapter. The first experiment focuses on validating the combined effects of the trapped charge in the BOX and the BBT based model [3] by experimentally irradiating a 0.5 μm gate length planar SOI device up to a total dose of 500 krad(SiO_2). The device was characterized with a drain bias of 1.3 V and a grounded back-gate. The second irradiation set concentrates more on the drain bias dependency in irradiated planar SOI MOSFETs. A 0.5 μm gate length device was irradiated, up to a total dose of 100 krad(SiO_2), and characterized after each irradiation step for several drain biases up to 1.6 V. The third experiment was dedicated to study the gate length dependency in irradiated planar samples. Two more gate lengths, i.e., 1 μm and 10 μm gate length devices, were irradiated up to a dose of 100 krad(SiO_2). TID response comparison was achieved for a fix drain bias of 1.4 V. All planar samples were irradiated with floating body, grounded drain and source terminals, a gate voltage of 0.8 V and a back-gate (or substrate) voltage of 3 V. The last experiment was conducted to determine the FinFET TID response. Fin-width dependency was studied by comparing the radiation response of 40 nm and 80 nm fin-width 100 nm technology FinFET devices. The samples were irradiated up to a total dose of 500 krad(SiO_2) and characterized with a drain bias of 1 V. FinFET samples were irradiated with off state configuration. To summarize, the experimental results can be described by:

- Enhancement in the drain leakage current in planar SOI MOSFETs from the combined effect of BBT and trapped charge in the buried oxide [3].
- Increased drain leakage current in planar devices at higher drain voltages, resulting from greater field-induced BBT tunneling.

- Increased drain leakage current for planar SOI MOSFETs with shorter channels resulting from greater N_{ot} buildup in the buried oxide following irradiation [9, 10]. A new explanation is developed in the following chapter to explain the higher drain leakage current for shorter devices.
- Devices with narrower fin widths (FinFETs) are more tolerant to radiation effects than their planar counterparts even for shorter gate channel devices (100 nm). This is because of the additional lateral gates control over the body. The wider the fin width, the larger the threshold voltage shift.

CHAPTER VI

ANALYSIS OF TOTAL IONIZING DOSE RESPONSE OF PLANAR SOI DEVICES AND FINFETS

In this chapter, the effects of gate length and drain bias on the off-state drain leakage current of irradiated fully-depleted SOI *n*-channel MOSFETs are analyzed. The experimental results presented in the previous chapter are interpreted in this chapter using a model based on the combined effects of band-to-band tunneling (BBT) and the trapped charge in the buried oxide. For negative gate-source voltages, the drain leakage current increases with the drain voltage because the electric field in the gate-to-drain overlap region is increasing. The off-state current in these devices increases with total ionizing dose due to oxide trapped charge build up in the buried oxide, enhanced by the BBT mechanism. The experimental data show that these effects are more significant for devices with shorter gate-lengths. Experimental and simulation results suggest that the BBT-generated holes are more likely to drift all the way from the drain to the source in shorter devices, enhancing the drain leakage current, while they tend to tunnel across the gate oxide in longer devices. The TID response of FinFETs devices is investigated as function of fin width and total dose. Narrower fin width devices show higher tolerance to TID effects because of the additional control of lateral gates over the floating body. Lower threshold voltage shifts and subthreshold swing values are reported for narrower FinFETs.

6.1 TID effects on planar FDSOI MOSFETs

The simulation results used in this thesis were performed at Arizona State University by Ivan Esqueda. Device simulations on structures representative of the FDSOI *n*-channel

MOSFETs (i.e., l_g = 0.5 μm, 1 μm and 10 μm) tested in this study were performed with Silvaco's Atlas device simulator. The *p*-Si body of the simulated structures is uniformly doped with $N_a = 2 \times 10^{15}$ cm^{-3}. The source and drain regions are uniformly doped with $N_d = 1 \times 10^{18}$ cm^{3}. The gate oxide thickness (t_{ox}) is 2 nm, the buried oxide thickness (t_{box}) is 150 nm, the silicon film thickness (t_{si}) is 60 nm, and the gate overlaps the source and drain regions by 80 nm. These simulations were done using Silvaco's radiation effects module, a self-consistent field/charge-trapping model, which models ionizing radiation-induced transport and trapping of charge in the oxide.

6.1.1 *Drain bias dependence in irradiated FD SOI planar devices*

6.1.1.1 The gate-to-drain electric field affects the amount of holes generated via the BBT

Simulation results obtained using the BBT model show an increase in the off-state drain leakage current for negative gate voltages when the drain voltage is increased, which is consistent with the experimental data shown in Figs. 5.3, 5.4 and 5.5 in the previous chapter. The effects of drain voltage can be explained by the field dependence of BBT-induced carrier generation described by:

$$G_{BBT} = A(E_S)^{\sigma} e^{(-B/E_S)} \tag{5.1}$$

where A is a constant related to the effective mass of the electrons for Si, E_s is the magnitude of the local electric field at the front silicon surface in the gate-to-drain overlap region, and B is the tunneling probability constant (≈ 30 MV/cm) [3]. Since the electric field in the gate-to-drain overlap region is directly proportional to the applied drain bias, an increase in the drain voltage leads to an increase in the amount of generated carriers

due to BBT. The flux of BBT-generated holes into the body and across the source-body junction ($J_{p,BBT}$) is proportional to the carrier generation rate in (5.1).

6.1.1.2 The body potential increases the drain leakage current via decreasing the back channel threshold voltage

In a recent paper [3], it was shown that $J_{p,BBT}$ raises the electron quasi-Fermi level in the *p*-type body relative to the hole quasi-Fermi level, thereby raising the potential of the floating body relative to the source, V_{bs}. An increase in V_{bs} above 0 V reduces the threshold voltage at the back channel via the body effect. As the drain bias increases, more holes enter the body via the BBT process, further increasing the floating body potential, as shown in Fig. 6.1, where the potential is plotted vs. front gate voltage at various drain voltages.

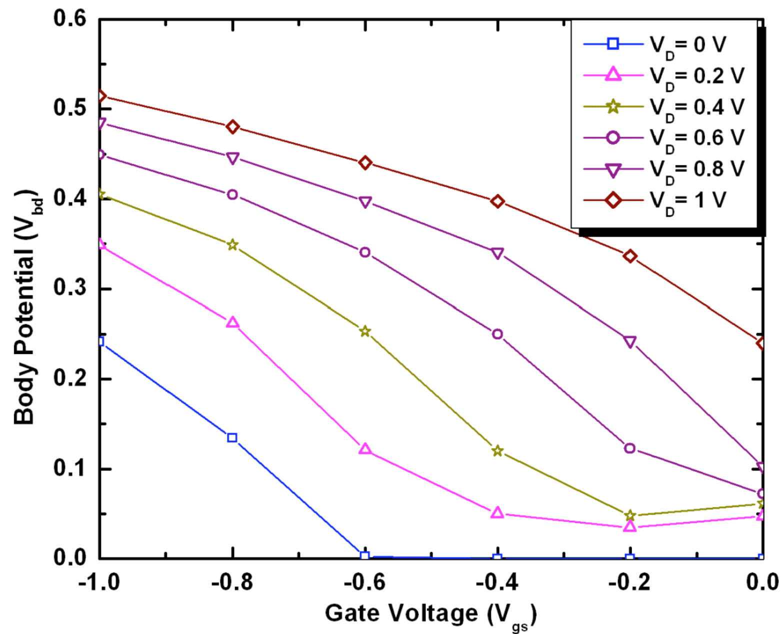

Fig. 6.1: Body potential as a function of V_{gf} for different V_d. Simulations with BBT model, V_s = 0, the back-gate voltage (V_{bg}) is grounded, and L_g = 0.5 μm [2].

The body potential in Fig. 5.6 was obtained from the split in the quasi-Fermi levels for holes and electrons in the body [29].

$$V_{bs} = \phi_{fp} - \phi_{fn} = \frac{(E_{fn} - E_{fp})}{q} \tag{4.2}$$

where V_{bs} is the body potential, ϕ_{fp} and ϕ_{fn} are respectively the quasi-Fermi potentials for holes and electrons, E_{fp} and E_{fn} are respectively the quasi Fermi levels for holes and electrons, and q is the elementary charge. In order to decrease the impact of the electric field associated with the drain and source junctions, the body potential was calculated in the silicon film halfway between the drain and the source. As mentioned previously, the combined effect of increased body potential and positive trapped charge in the buried oxide is a decrease of the back-side threshold voltage, V_{Tb}. Thus a higher body potential caused by increased drain bias further reduces V_{Tb} through the body effect, leading to greater drain leakage current at negative gate biases.

6.1.1.3 Drain bias dependence

The mechanisms that result in the drain bias dependence effect on the I_d-V_{gf} characteristics are investigated qualitatively through simulations. For these numerical studies, radiation damage is modeled by including a uniform fixed amount of positive trapped charge at the interface of the Si film and the BOX (i.e., back-side interface only). The plot in Fig. 6.2 shows the I_d-V_{gf} curves obtained through simulations for oxide trapped charge densities per unit area (N_{ot}) of 0 (pre-rad) and 5×10^{11} cm^{-2} (simulated post-rad). Including N_{ot} in the simulations (filled symbols in the figure), results in a shift of the V_{Tf} and an increase in the leakage current at negative gate voltages. Since there is no fixed charge added to the front oxide/Si-film interface, the shift in the front-gate threshold volt-

age comes directly from the coupling of the front and back gates (adding positive charge at the back interface is similar to applying a positive voltage to the substrate).

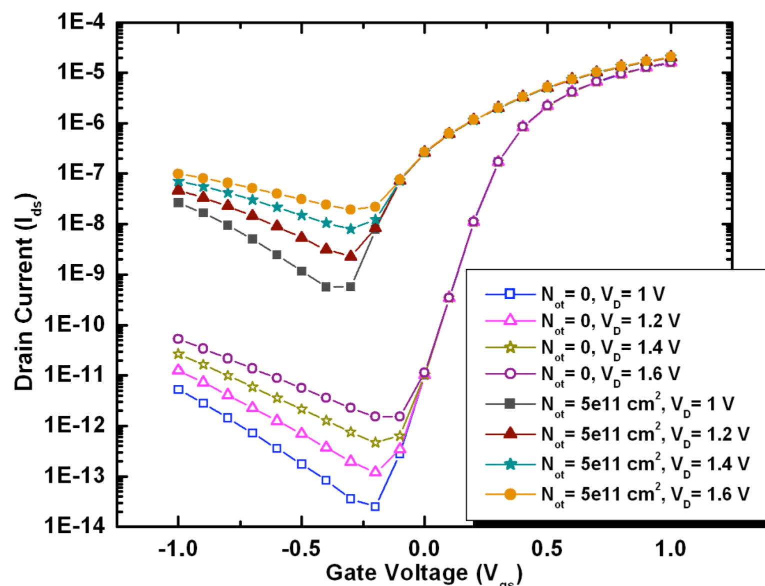

Fig. 6.2: I_d-V_{gf} curves for various V_d values. $V_s = V_{bg} = 0$ V, using BBT model in simulations. Results for $N_{ot} = 0$, 5×10^{11} cm^{-2} at the BOX/Si interface and $L_g = 0.5$ µm [2].

The effects of drain bias on the *I-V* characteristics are also shown in Figs. 5.1, 5.2, and 5.3. The simulations show that when the gate voltage is negative, the generation of carriers due to the BBT mechanism is significant, resulting in increased body potential and drain-to-source leakage. For the post-rad simulated curves this increase in drain-to-source current enhances the leakage as described above.

6.1.2 *Gate length dependency in irradiated FD SOI planar devices*

In this section, we examine the total dose response as a function of the gate length. The experimental data show a higher drain leakage current for shorter gate length devices (0.5 µm gate length in our case) as can be observed by comparing Figs. 5.5, 5.6 and 5.7. In [2], significantly more leakage current was observed in shorter gate length devices for

specific bias conditions during irradiation that result in a high electric field in regions near the back interface, therefore enhancing the amount of positive trapped charge in the BOX. For the experimental data presented here, the bias conditions during irradiation were 0.8 V at the front gate, 3 V at the back gate, and 0 V at the source and drain. For longer gate length devices, device simulations for this bias condition showed *no* significant gate length effect on the electric field near the back interface or on the amount of radiation-induced positive trapped charge in the BOX. This suggests that the gate length effects observed experimentally for longer gate length devices are caused by a different mechanism. As previously mentioned, holes, originating from BBT generation, that transport to the source increase the body-to-source potential, $V_{bs} > 0$ V. This enhances leakage current by reducing the back-gate threshold voltage via the body-effect. Our analysis shows that for the longer devices, this hole current across the body-to-source junction is suppressed.

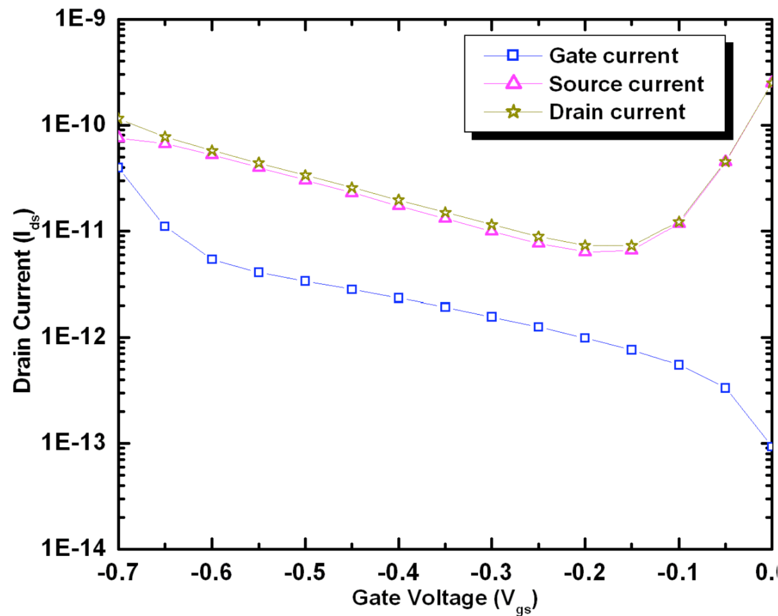

Fig. 6.3: I_D, I_s and I_g vs. V_{gf} (obtained experimentally) for the L_g = 0.5 µm, V_D = 1.4 V, $V_{bg} = V_s = 0$ V [2].

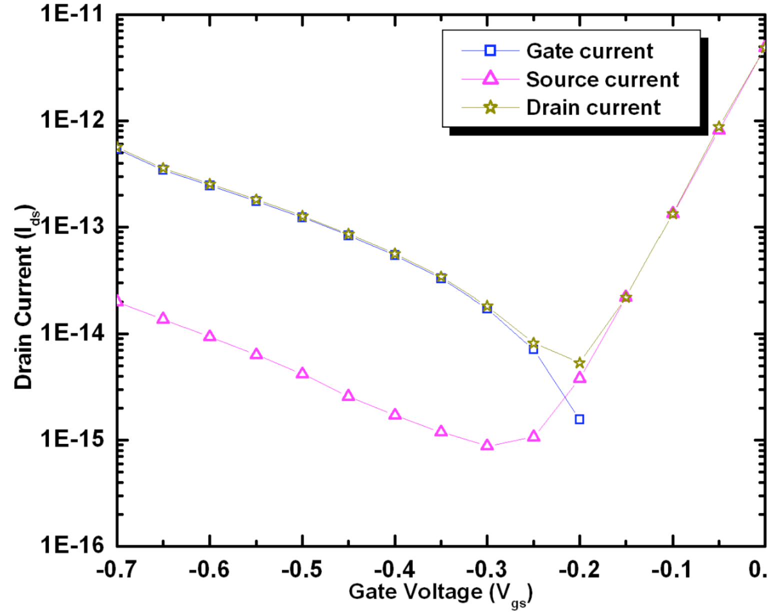

Fig. 6.4: I_D, I_s and I_g vs. V_{gf} (obtained experimentally) for the L_g = 10 µm, V_D = 1.4 V, V_{bg} = V_s = 0 V [2].

Measurements of the drain I_D, source (I_s) and gate (I_g) currents as the gate is swept negatively show that, for the shorter gate length devices (L_g = 0.5 µm), I_s and I_D are approximately equal with much lower I_g as can be seen in Fig. 6.3, whereas for longer gate length devices (L_g = 10 µm), see Fig. 6.4, the data indicate that I_g and I_D are comparable with a lower I_s. This suggests that for the L_g = 0.5 µm devices, hole conduction across the body-to-source junction is present via the mechanisms explained above. In contrast, for L_g = 10 µm, there is a significant current flow from drain-to-gate due to a tunneling mechanism across the thin gate oxide that suppresses the conduction of holes to the source. Thus, the experimental data show less increase in the drain leakage currents for the L_g = 10 µm devices as a function of dose since the radiation damage (i.e., buildup of charge at the back-side interface) is not enhanced by the BBT process. In other words, the tunneling current, which is proportional to the gate area, discharges the body more efficiently in longer transistors. Indeed, in longer gate length devices the electric field origi-

nating from the drain has a lower magnitude along the channel allowing BBT-generated holes to have a higher probability of tunneling across the gate oxide rather than continuing toward the source. Since the gate oxide thickness is 2 nm and the channel is 150 nm wide, the gate oxide tunneling process is likely to happen via direct tunneling through an almost trapezoidal barrier [15]. Thus, direct tunneling across the gate oxide is more probable for the longer gate length devices. Figs. 5.10 and 5.11 are qualitative simulation results of the drain I_D, source (I_s), and gate (I_g) currents as functions of the front gate voltage including the direct tunneling (DT) model for devices with L_g = 0.5 μm and L_g = 10 μm, respectively. As in the experiments, see Figs. 5.8 and 5.9, the 0.5 μm and the 10 μm gate length devices were simulated with a drain bias of 1.4 V.

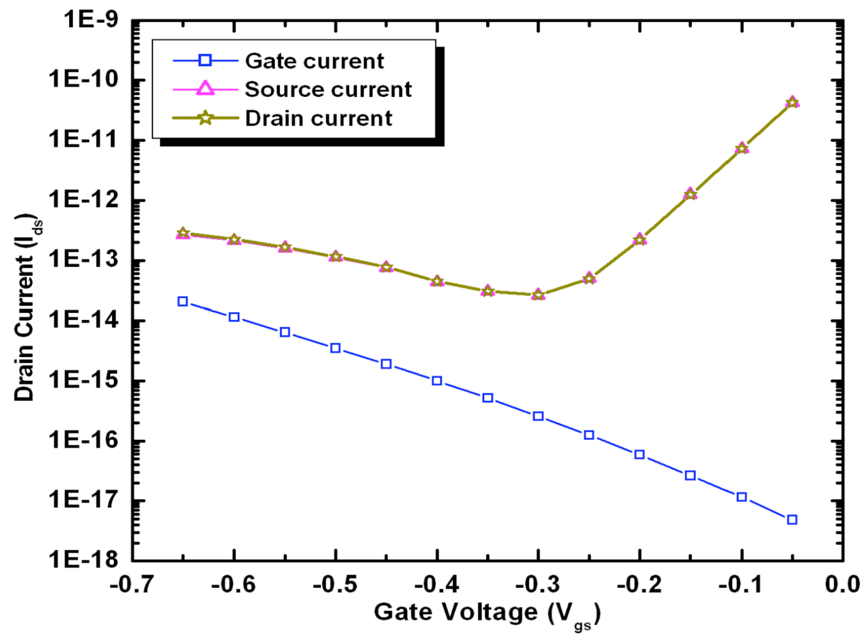

Fig. 6.5: Simulated I_d, I_s and I_g vs. V_{gs} for the L_g = 0.5 μm device. V_d = 1.4 V, V_{bg} = V_s = 0 V [2].

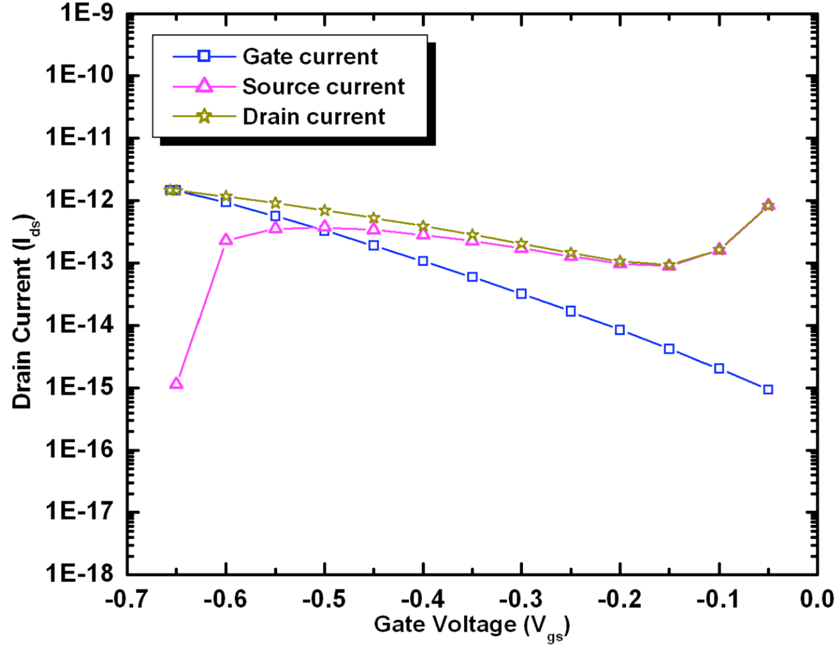

Fig. 6.6: Simulated I_d, I_s and I_g vs. V_{gf} for the L_g = 10 μm device. V_d = 1.4 V, V_{bg} = V_s = 0 V [2].

However, no trapped charge was included in the BOX. The results agree with the experimental data as conduction from source-to-drain is observed for simulations on the L_g = 0.5 structure, see Fig. 5.10, whereas simulations for the L_g = 10 μm structure, see Fig. 5.11, show that there is a significant gate-tunneling current that dominates over source-to-drain conduction. These results indicate that both BBT and DT mechanisms are involved in the radiation response of these devices. We finally note that in very short-channel MOSFETs the body potential increase, leading to accentuated radiation effects, is not only due to the positive BOX charging but also to the field penetration from the drain through the BOX and substrate.

6.2 TID effects on 100-nm gate channels FinFETs

In this section, we experimentally demonstrate that 100-nm gate length FinFETs with narrow fins are less sensitive to total ionizing dose than devices with wider fins.

This is the first demonstration of the fin-width effect in very deep submicron gate-length devices, and it follows trends reported for long-channel devices. The dependence on fin width occurs because the lateral gates help to control the back surface potential, hence the floating body effect. Larger (worse) subthreshold swing is confirmed for wider FinFETs, where the impact of non-uniform trapped charge in the oxide is more effective.

6.2.1 Threshold voltage shift

The fin-width dependence is consistent with previous results, where very long gate length (10 μm), gamma-shaped gate FinFETs were investigated. The higher tolerance of narrower FinFETs in [7] was explained by the additional lateral gate control that attenuates the coupling effects between the front and the back gates, thereby reducing the undesirable effects of the trapped charge in the BOX on the front gate. Fig. 6.4 illustrates the threshold voltage as a function of dose for both fin widths (40 nm and 80 nm) studied in this work. The threshold voltage for these parts, with a gate length of 100 nm, shows a slightly higher sensitivity to TID than the previously published data for 40 nm fin-width devices. The threshold voltage decreases consistently with dose for both fin widths examined in this work. This negative threshold voltage shift is due to the coupling effects between the front and back gates, enhanced by the fringing field originating in the drain [32]. This results in a larger shift in wider FinFETs, while narrower devices are more tolerant of TID effects, in agreement with previous work [7]. In narrower fin width devices, the lateral-gate effect is two-fold: (i) the gates control the floating body potential and, in particular, the surface potential at the back interface (fin-BOX), reducing the impact of both the vertical coupling effect and the fringing fields originating from the drain termi-

nal and (ii) the gates modify the field distribution in the BOX, further decreasing the amount of trapped charge. The lateral coupling effects dominate for narrower FinFETs.

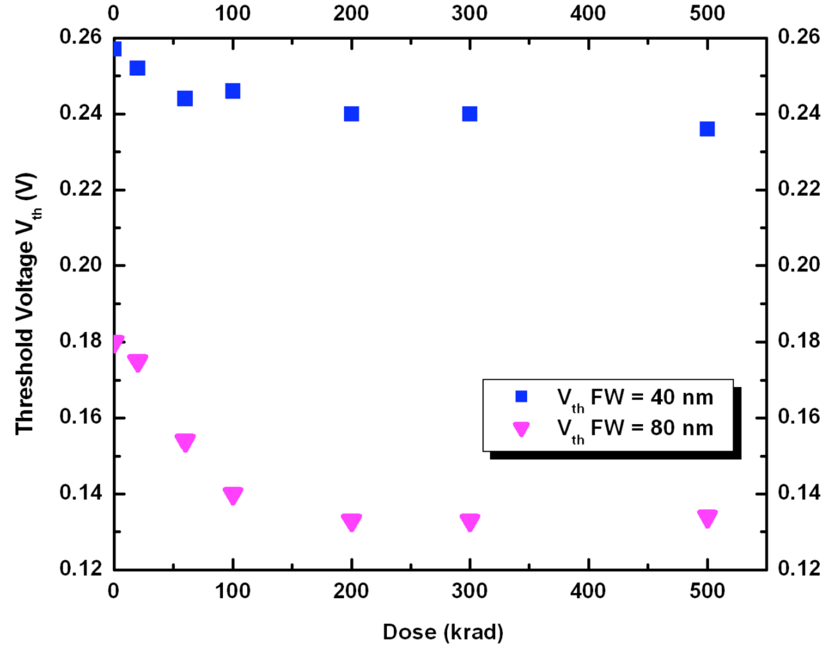

Figure 6.7: Threshold voltage as function of dose for 40 nm and 80 nm fin-width finFETs.

6.2.2 *Subthreshold swing shift*

Another important result observed in the experimental data is the reduction in the subthreshold swing (SS) in irradiated FinFETs. Fig. 6.5 shows the subthreshold swing of the studied devices as a function of dose for 40 nm and 80 nm fin-width devices. The subthreshold swing (SS = $dV_G/d\ (log\ I_D)$) is significantly different for the 40 nm and the 80 fin-width devices, with the narrow fin-width devices exhibiting better pre-irradiation SS, as well as less degradation. It has been demonstrated that the SS of FinFETs increases with the fin width for short-channel devices because of the additional coupling from the drain, which is consistent with the obtained experimental results.

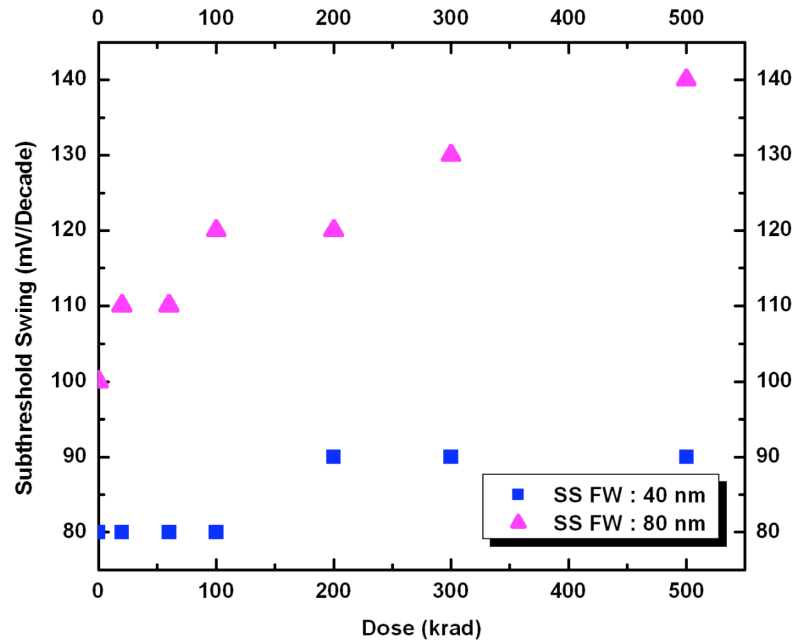

Fig. 6.8: Subthreshold swing $d(V_g)$ /d(log I_D) as function of dose for 40 nm and 80 nm fin-width finFETs .

As the dose increases, the wider FinFET requires more and more gate voltage to reach the conductive mode. Although some of the stretchout may be caused by interface-trap formation, it is more likely due to non-uniform radiation-induced oxide trapped charge [30]. The trapped charge in the oxide in wider devices affects the operating characteristics of the FinFETs more as the lateral coupling is not strong enough to prevent the floating body effects. The narrow and short channel FinFETs investigated in this work did not show any substrate bias effects that have been demonstrated to change the on-current dramatically through the radiation-induced series resistance modulation [31]. The virtual substrate voltage generated by the positive trapped charge in the BOX in the FinFETs studied in this work is not large enough to vary the parasitic series resistance. Further experiments and simulations are planned to analyze the threshold-voltage and subthreshold-swing degradation in FinFETs with a larger ranges of fin widths and gate lengths.

Conclusion

Comparing the radiation response of a 0.5 μm gate length planar FD SOI device for a range of drain biases up to 1.6 V illustrates that more off-state drain leakage current occurs for higher drain voltages, resulting from greater field-induced band-to-band tunneling process in the gate-to-drain overlap region. Shorter gate length planar devices (0.5 μm gate length devices) are more vulnerable to radiation-induced increases in off-state drain leakage, which can result from greater N_{ot} buildup in the buried oxide following irradiation [8, 10], or from the fact that in shorter gate length devices, the BBT holes generated drift toward the source creating an additional drain-source current, while in longer gate length devices, these holes tunnel across the gate oxide via the direct tunneling mechanism. This is because of the lower electric field originating from the drain along the channel. This latter result was experimentally demonstrated and explained with simulations. Narrower fin devices with shorter channels were examined as well, radiation response of 100 nm gate length FinFETs was investigated on 40 nm and 80 nm fin width devices as functions of total dose and fin width. Less significant threshold voltage shift was reported for narrower FinFETs (40 nm fin width). This was explained by the additional control of the lateral gates over the body. Our results suggest that more voltage is needed to turn on irradiated FinFETs with wider fins. This was explained by the non-uniform oxide charge trapping in irradiated FinFETs.

CHAPTER VII

CONCLUSION

The buried oxide (BOX) layer makes *n*-channel fully depleted silicon-on-insulator (FDSOI) transistors more susceptible than bulk transistors to total ionizing dose (TID) damage in deep submicron processes (< 130 nm) [32]. This is because TID causes positive charge to be trapped in the buried oxide, as evidenced by the negative shift of the back-gate *I-V* characteristics [4, 6, 7]. These parts exhibit front-gate threshold voltage (V_{Tf}) shifts that are caused by electrical coupling of radiation-induced charge buildup in the BOX to the front interface [2, 4, 9]. A high current state can take place in irradiated FD SOI devices as dose levels increase. In this thesis, we experimentally demonstrate that the combined effect of band-to-band tunneling with the positive trapped charge in the buried oxide is the origin of the drain leakage current increase in irradiated floating body mesa-isolated FDSOI devices for negative gate voltage and positive drain voltage. By comparing the radiation response of devices with different drain bias, we conclude that more off-state drain leakage current was observed for higher drain voltages resulting from greater field-induced BBT tunneling. Also, shorter gate length devices are more vulnerable to radiation-induced increases in off-state drain leakage resulting from greater N_{ot} buildup in the buried oxide following irradiation [9, 33]. Our experimental and simulation results for shorter gate length planar SOI devices suggest that the BBT-generated holes are more likely to drift all the way from the drain to the source in shorter devices, enhancing the drain leakage current, while they tend to tunnel across the gate oxide in longer devices. In order to extend the TID studies to more advanced technology parts.

Shorter (100 nm) gate length and narrower fin width (40 nm and 80 nm) FinFETs devices were investigated. The obtained irradiation results for FinFETs showed a higher tolerance to TID effects for FinFETs over their planar SOI devices counterparts. This was explained by the additional lateral gate control that attenuates the coupling effects between the front and the back gates, thereby reducing the undesirable effects of the trapped charge in the BOX on the front gate. The threshold voltage for these parts, with a gate length of 100 nm, shows a slightly higher sensitivity to TID effects than the previously published data for 40 nm fin-width devices. FinFETs with wider fin width (80 nm) behave more like planar devices with larger threshold voltage shifts and greater subthreshold swings. In narrower fin width devices, the lateral-gates control the surface potential at the back interface (fin-BOX), reducing the impact of both the vertical coupling effect and the fringing fields originating from the drain terminal. They also modify the field distribution in the BOX, further decreasing the amount of trapped charge. Thereby the lower threshold voltage shifts for narrower fin width devices. The lateral coupling effects dominate for narrower FinFETs. The obtained results also reported that larger voltages are needed to turn on wider fin width devices as dose levels increase. Although some of the stretchout in the $dV_g/d\log(I_D)$ curves may be caused by interface-trap formation, it is more likely due to non-uniform radiation-induced oxide trapped charge.

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