A CLOCK-GATED, DOUBLE EDGE-TRIGGERED FLIP-FLOP IMPLEMENTED WITH TRANSMISSION GATES

By

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CHAPTER I

INTRODUCTION

With the widespread use of mobile devices in modern society, power efficiency and energy savings become extremely important issues for designers. Normally, high-performance chips have high integration density and high clock frequency, which tend to dictate power consumption. Therefore, designs are needed that can consume less power while maintaining comparable performance.

Power consumption in the conventional CMOS digital circuit can be separated into three types of power dissipation [1]: (i) switching power, (ii) short-circuit power, and (iii) leakage power consumption. The switching power represents the power dissipated during the signal transitions when energy is drawn from the power supply to charge-up the device capacitances. Short-circuit power is produced during the moment that both the PMOS network and the NMOS network are simultaneously on in CMOS logic. The MOSFETs in CMOS logic normally will have some non-zero reverse leakage and sub-threshold current, which causes the leakage power consumption.

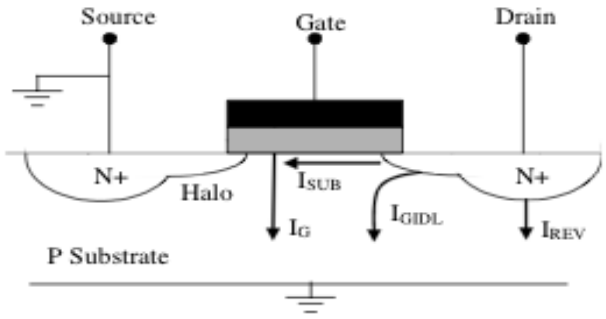


Figure 1: Four sources of leakage current in the MOSFET

The sum of switching power and short-circuit power can be categorized as dynamic power, while the leakage power also called static power dissipation [2]. The static power increases faster than dynamic power with the shrinking of feature size.

Static power

Since static power is a large fraction of total power consumption, reducing the static power must be addressed in device-level design. The sources of leakage power, as shown in Figure 1, can be categorized into four types: (1) reverse-bias-junction leakage, (2) gate-induced-drain leakage, (3) sub-threshold leakage, and (4) gate-oxide leakage. Among these leakages, the sub-threshold leakage and gate-oxide leakage dominate the total leakage current [3].

The gate-oxide leakage current is equal to

$$\boldsymbol{I_{ox} = K_2 W (V / T_{OX})^2 e^{-a(T_{ox}/V)}}$$

In this equation, $\boldsymbol{K}$ is the relative dielectric constant, $\boldsymbol{W}$ is the width of the transistor channel, $\boldsymbol{V}$ is the voltage supply, and $\boldsymbol{T_{OX}}$ is the gate oxide thickness. The formula shows

that $\boldsymbol{I_{ox}}$ is inversely proportional to the thickness of the gate oxide layer. The $\boldsymbol{T_{ox}}$ has been reduced with technology scaling, which increases the gate-oxide leakage. The emergence of high-*k* dielectric material helps to reduce the gate-oxide leakage current.

For sub-threshold leakage

$$\boldsymbol{I_{sub} = KWe^{\frac{-V_{th}}{nT}}\left(1 - e^{\frac{-V}{T}}\right)}.$$

Where $\boldsymbol{K}$ and $\boldsymbol{n}$ are constant, $\boldsymbol{V}$ is the supply voltage, $\boldsymbol{V_{th}}$ is the threshold voltage, and $\boldsymbol{T}$ is temperature. The leakage current $\boldsymbol{I_{sub}}$ increases exponentially when the threshold voltage $\boldsymbol{V_{th}}$ decreases. This relationship makes a problem for designers because as technology scales, the threshold voltage will be reduced when the supply voltage decreases.

There are four ways to reduce threshold leakage current:

- Remove the redundant parts from the design, and keep the transistor count as small as possible.
- Reduce the active transistor dynamically by power gating those idle elements.
- Use low threshold voltage devices on the critical path to meet performance requirement while placing high threshold voltage devices elsewhere to reduce the leakage waste.
- Control the temperature to cool the system.

Dynamic power

Although the static power has become an important part of total power, the dynamic power is still significant in the total consumption. Reducing the dynamic power is still critical for low-power design. This thesis focuses on the reduction of dynamic (i.e., switching) power in circuit-level design.

The switching power is calculated using the equation:

$$\boldsymbol{P = \alpha f C V^2},$$

where α is the switching activity, *f* is the frequency, *C* is the capacitance, and *V* is the supply voltage. Decreasing the supply voltage will increase the timing delay of the circuit, and may lead to an exponential increase in leakage power. Normally, the threshold voltage will decrease along with the drop of supply voltage. However, according to the calculations of the sub-threshold leakage formula, the threshold voltage has an exponential relationship with the leakage; capacitances are mostly affected by device characteristics [4]. Thus, this thesis attempts to minimize power though the perspective of decreasing α, the switching probability, and *f*, the clock frequency, while avoiding the reduction of overall system performance.

Flip-flops and power consumption

As a commonly used component in the digital system, flip-flops often appear in computational circuits or are used as registers in pipeline structures to store the data for additional processing. The conventional single edge-triggered flip-flop (SETFF), shown in Figure 2, is usually implemented by cascading two oppositely phased latches, and is

active on either the rising edge or the falling edge of the clock. During the first half of the clock cycle, the primary (transparent) latch loads the input. Then the data value is passed to the secondary latch during the next half of the clock cycle. To take advantage of that idle edge, double edge-triggered flip-flops (DETFF) have emerged. These flip-flops can operate at half of the clock frequency while maintaining the same data throughput compared to single edge-triggered flip-flops and will be described in Chapter II. In other words, the DETFF requires a lower clock frequency than the SETFF to achieve comparable performance [5].

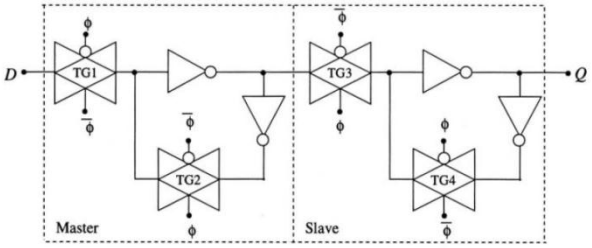


Figure 2: Generic single edge-triggered flip-flop implemented with transmission gates (SETFF)

As timing components, flip-flops capture data with the active edge of the clock signal; sometimes this capture is not necessary because the data value is unchanged. Because of the constant activity of the clock signal, timing components (i.e., latches and flip-flops) that respond on the clock transition are the most power-consuming components in the VLSI system [6, 7]. The most obvious power reduction is to prevent transitions made by the clock while the input data value matches the current state. So clock-gating techniques [8, 9] have been developed to disable unnecessary clock switching when there is no change on the input to the flip-flop.

Aims of this thesis

In this thesis, two designs have been proposed to reduce power consumption in flip-flops. First, a double edge-triggered flip-flop was implemented with transmission gates (T_DETFF). Second, a clock-gated double edge-triggered flip-flop (G_DETFF), based on T_DETFF, was also implemented. The clock-gating technique used in this thesis is designed to be more suitable for the double edge-triggered flip-flop. If the input is idle, then the proposed design G_DETFF saves up to 98% of the power when compared with the conventional SETFF; also G_DETFF can save 82% power when compared with T_DETFF while maintaining a sufficient timing response. When clock gating is suitable ($\alpha < 0.4$), the G_DETFF saves 33% of the energy on average versus a DETFF with pass transistors (P_DETFF) [10].

The rest of this thesis is organized as follows. Chapter II discusses power management in digital integrated circuit (IC) design. Chapter III reviews previous designs of DETFFs as well as clock-gating techniques. The proposed Design I: T_DETFF and Design II: G_DETFF are discussed in Chapter IV. Chapter V shows the simulation results, comparison, and analysis. The conclusion and future work are given in the last chapter.

CHAPTER II

POWER MANAGEMENT IN DIGITAL CIRCUIT DESIGN

Because of the pursuit by designers to improve digital system performance, various technologies have been invented to enhance the functionality or operating speed of the system. However, performance improvement techniques typically result in extra energy consumption. Reducing power without affecting system performance is an important issue not only for portable computers and mobile devices but also for high-end systems.

Power is commonly defined as the rate at which the system performs that work, and energy means the total amount of work a system performs over a period of time. Formulas are expressed as follows:

$$P = V * I, \quad (1)$$

$$E = P * T, \quad (2)$$

where P is power, E is energy, T is a certain amount of time interval, and W is the total work performed in that time. Thus, reducing power does not necessarily reduce energy. Because, from the formula, if lower power requires more the time to finish the same amount of the work, then the totally energy consumption may be even more than before [3].

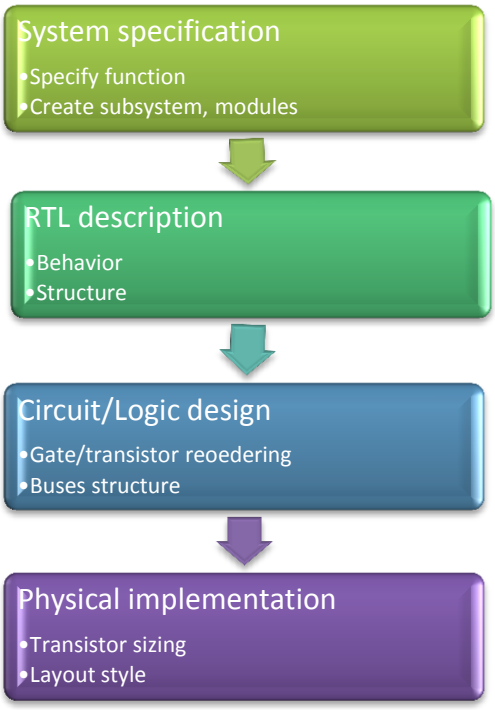


Figure 3: General ASIC design flow chat

The main Application-Specific Integrated Circuit (ASIC) design flow are categorized in Figure 3. The methodology for low-power CMOS design could be addressed from different perspectives [11]. These perspectives include: (1) system-level perspective, (2) RTL-behavioral perspective, (3) RTL-structural perspective, (4) circuit/logic-level perspective, and (5) physical-level perspective.

System-Level Perspective

This is the first step in top-down design flow. The power saving achieved in this level can be efficient and significant [12]. The core idea is to identify the working mode of each module in the system, and then selectively disable the idle modules. Therefore, the power wasted for idle conditions has been effectively controlled. Clock gating can be used at this level, where the clock signal is only provided to the modules that require it,

thereby reducing the dynamic power [13]. Power gating, which is broadly used as well, is also a very effective technique to reduce both dynamic power and leakage power. A header and a footer switch are inserted into voltage supply path to enable a sleep signal to selectively disconnect the logic block from the voltage supply [14].

Behavioral perspective

RTL design is the second stage for a top-down design; the functionalities of each module in the digital system are described and realized at this point. Power-saving methodologies from the behavioral perspective are more software dependent. According to the feature of each system, designers modify or choose the algorithm to reduce the number of times the most power-consuming operation is performed [15].

Dynamic voltage frequency scaling (DVFS) is a widely accepted power reduction technique at the behavioral level. This technique is software-based depending on certain scheduling algorithms. Supply voltage and frequency are dynamically scaled down for specific tasks to make the circuit operate at the lowest speed but satisfy performance requirements. [16]

Bus-encoding techniques could decrease signal transitions by using certain coding schemes, like Gray coding, to achieve the minimum switching activity. A Gray code makes sure the Hamming distance between two adjacent code words always equals one. So the power consumption could be reduced, especially when used on signal lines with large capacitances [11].

Structural Perspective

Structural perspective is another view that could minimize power consumption in RTL. There are two typical structures that are often used to reduce power. One is a parallel structure [17]. Several functional units, say *N* in parallel, allow the system to work on different or independent functions simultaneously, which reduces the clock frequency to *1/N*. However, duplicating the functional units requires more area to implement and results in the increase of capacitance due to the extra circuits. Thus, one has to make a trade-off an increase among power, area, and capacitance to satisfy the design requirements. The other architecture is a pipeline structure [18]. It controls the instruction flow in the data path to maximize the data throughput, so that the system could run at a lower clock frequency but has the same performance outcome. Therefore, if under the same speed constraint as a non-optimized structure, then the system with a pipeline structure could work at a lower clock frequency and save power. However, pipeline hazards because of certain dependencies, such as WAR (write after read), WAW (write after write) and RAW (read after write), may appear for certain algorithms.

Circuit/Logic-Level Perspective

Many research studies are focused on this level [4]. One technique is transistor reordering to minimize the switching activity [19]. The key idea is to keep the frequently switched transistors further from the output node to prevent unnecessary nodes charging and discharging. Logic gate restructuring aims to make all the gates have similar transition probabilities, and each path has similar delay time. Also, low-power flip-flops can be designed to reduce the power consumption of the state elements, which translates to power savings in the entire system [5, 10, 20, 21, 22,]. Low-swing buses are implemented by using two larger inverters to reduce the voltage swing for certain power-

hungry components and then amplify the voltage swing back to normal. Bus segmentation can minimize the bus capacitance by cutting the signal buses into shorter pieces. Clock gating and power gating can be applied either at the system level or the sequential/combinational circuit level.

Physical-level Perspective

Designers also can reduce the power at the layout level. For example, they can use transistor sizing, which reduces the transistor width of devices that are far away from the critical path to reduce devices capacitance. Also, the interconnection parasitic capacitance can be optimized to reduce power by proper routing among devices.

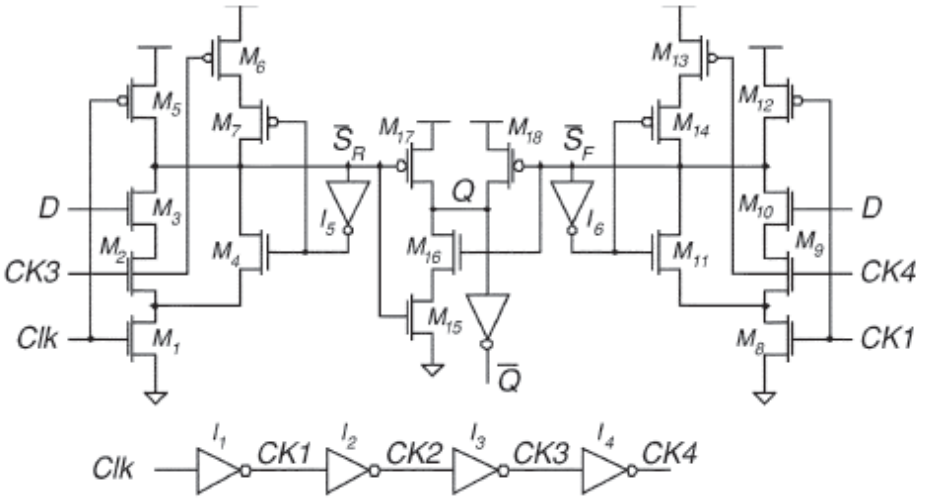
CHAPTER III

TECHNIQUES FOR DOUBLE EDGE-TRIGGERED FLIP-FLOPS AND CLOCK-GATING

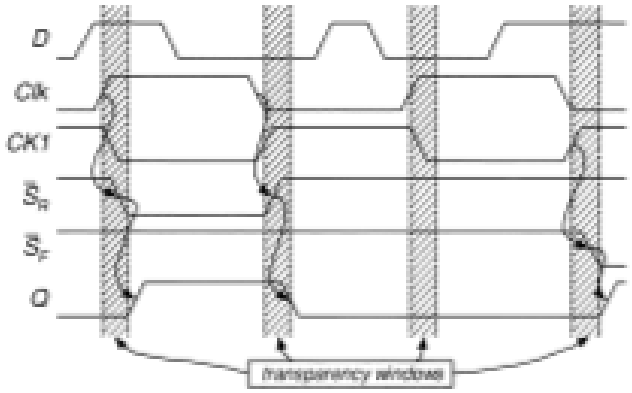
This chapter provides an overview of the literature associated with low-power design of flip-flops in digital integrated circuits. First, the mechanism for double-edge triggering in flip-flop design will be introduced. Then, the technique for clock gating within the flip-flop is described.

Review of double edge-triggered flip-flops

There are several ways to implement a double edge-triggered flip-flop. These methods can be categorized into two ideas. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip-flop to sample data on every clock edge. The designs described in Chapter IV are implemented with the second idea.



(a)



(b)

Figure 4: Symmetric pulse generator flip-flop [4]

For the flip-flops with a pulse generator scheme, the essential idea is to use an inverter chain to have a series of delayed clock signals. Based upon the timing difference of the clock edge and the delayed clock edges, the inserted circuitry will generate a new pulse. Thus, when those new pulses return to the flip-flop circuitry, the whole component becomes a double edge-triggered flip-flop. One implementation of this idea is the symmetric pulse generator flip-flop proposed by Nedovic et al. [5], shown in Figure 4. Nedovic's design uses an inverter chain to generate a pulse for every clock transition.

The design is composed by two symmetric parts; the left part responds on the rising edge of original clock signal, while the right part responds on the falling edge of original clock signal. During the rising edge of *CLK*, the *M1* and *M2* transistors are conducting, and *D* will be passed to output *Q*. After the transparent window, *M2* will be cut *OFF* because of the change at *CK3*. *M6* turns *ON*, and selectively holds the output at the correct value along with *M7* and *M4*. In the meantime, the other part just has *M12 ON*, which helps the output to hold the right value. The design has the same mechanism during the falling edge of *CLK*, but the two parts switch their roles. This method uses 32 transistors in total, and 16 transistors of them are controlled by the clock, which leads to additional power consumption.

Another implementation of the pulse generation idea is the conditionally pre-charged, double edge-triggered flip-flop proposed by Tsai et al. [20], shown in Figure 5. Node X, in middle of the circuit, can pre-charge only when the output is low to avoid unnecessary power consumption; it evaluates the output at each clock edge and stores the value until the next one by the generated pulses. However, both of Nedovic's and Tsai's design need a considerable increase in transistors for the implementation.

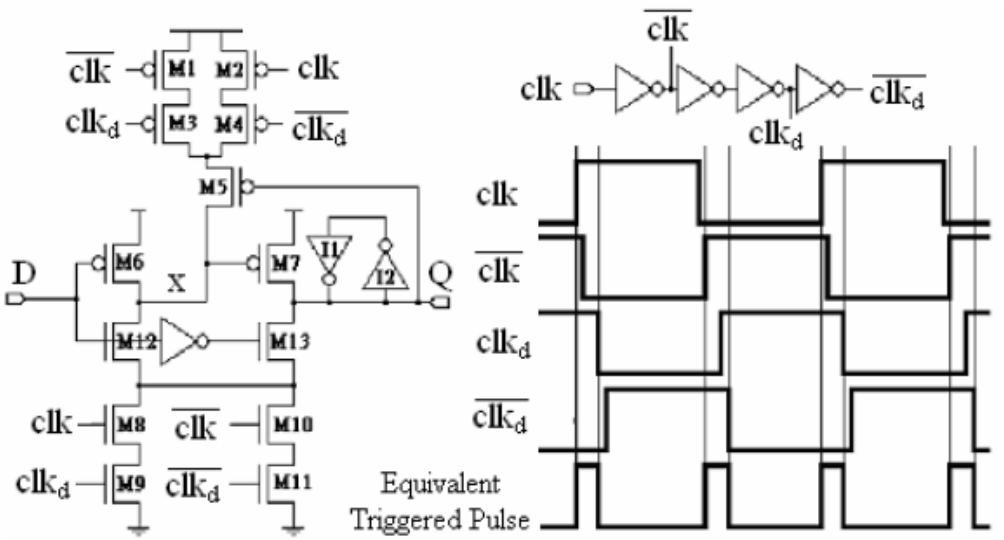


Figure 5: Conditional pre-charged double edge-triggered flip-flop with corresponding waveform for the clock pulse [20]

For the two-way data path idea, there are several existing designs. Hossain et al. [21] developed a static double edge-triggered flip-flop, as shown in Figure 6. This flip-flop has two stages to accomplish one data transfer. During Stage One (i.e., data transfer), when the clock is high, transistor MN1 is ON and transistor MN2 is OFF; the input value is passed to INV2. Because transistors MP2 and MN4 are ON as well, the value stored previously at the lower feedback loop will appear at the output. At Stage Two (i.e., path selection), when the clock goes from high to low, MN4 turns OFF, MN2 turns ON, and switch MN3 and MP1 are ON, while transistors MP2 and MN4 go OFF; thus the input data signal passes through transistor MN3 to the INV3, while the upper feedback loop saves the previous value in INV2 to pass to the output. This design kept the same transistor count as the conventional transmission gate based SETFF, but reduced the operating frequency by half when compared to the SETFF for a fixed data throughput.

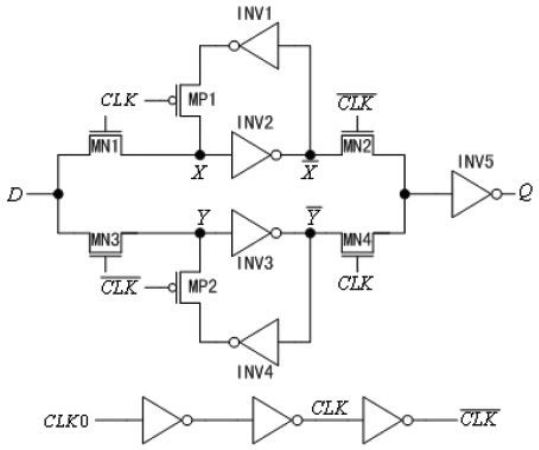
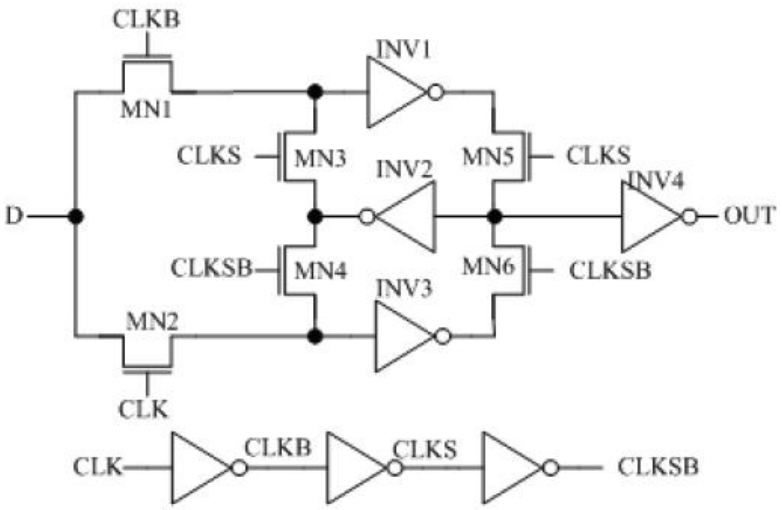


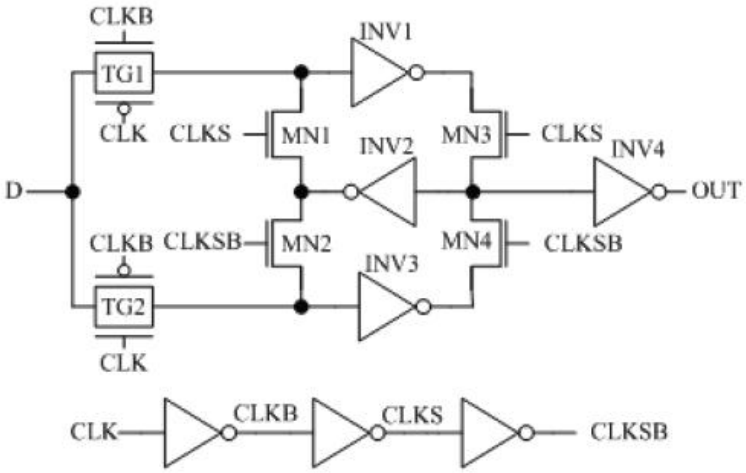
Figure 6: Static double edge-triggered flip-flop [21]

In Kuo et al. [22], two DETFFs are presented with the same design idea, but one is implemented with pass transistors (Figure 7a), and the other one is based on transmission gates (Figure 7b). When the clock is high, the input data to the lower path MN2 or TG2 is connected, and the value reaches INV3. In the meantime, because MN3 and MN5 are conducting, the upper loop is active. The node Q shows the value saved in the upper loop's last half cycle and vice versa when the clock turns to low. This design only needs 14 or 16 transistors, depending upon which gates are chosen.

However, a clock chain is required to produce the correct timing that enables the circuit to function; this requirement increased the entire power consumption of the design. Besides, the transmission gate implementation actually saves more power than the pass transistor one, although it has more transistors. This power savings is because pass transistors will send out weak logic values under some certain circumstances due to the threshold voltage. Those weak logic values may cause spikes or prolong the unstable time of the system, which will result in extra power consumption.



(a) Implement with pass transistors



(b) Implement with transmission gates
Figure 7: The Loop shared double edge-triggered flip-flop [16]

Another design developed by Yu [10] shown in Figure 8. This design will be referred to as P_DETFF, and it is used as the benchmark for the designs in Chapter IV. The P_DETFF design also follows the two data path idea. It connects two latches together in parallel, and uses pass transistors as switches to realize data transfer and perform path selection. When CLK form low to high, the switch MN1 and MN3 turns

ON, while MP1 and MP3 goes OFF. The input data will be passed into Node X, and stored at Node X by using a logic keeper (a feedback loop composed with an inverter and transistor). In the meanwhile, because MN3 is conducting, the value stored at Node Y on the last half clock cycle will be shown at output Q. The opposite occurs when the CLK signal turns from high to low.

Yu's design was compared with those previous DETFF designs [21, 22] in [10], and was shown to provide the best performance not only in power but also in area and speed. Therefore, Yu's DETFF is selected as the benchmark for the rest of this thesis. The merits of Yu's design include the following: (i) there is no need for a reversed clock signal, which is a true signal phase design and (ii) it requires only 12 transistors to implement the whole design.

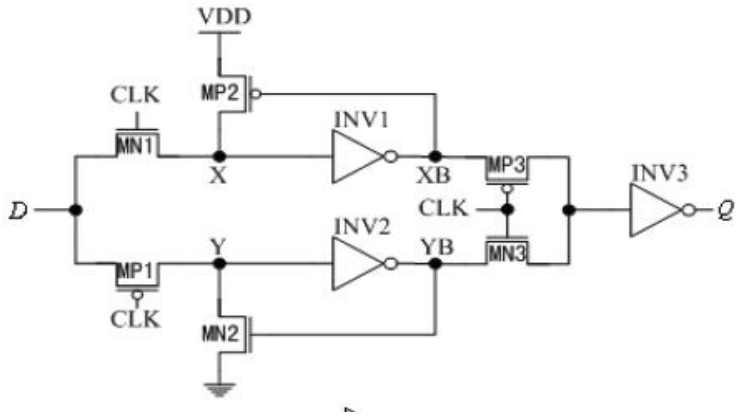


Figure 8: Benchmark I – Yu's design (P_DETFF)

However, the drawbacks of Yu's design are also obvious. First, the weak logic feature of pass transistors made the output of Yu's flip-flop take longer to reach stability, which will consume a lot of undesired power. This result can be verified in [22], and in the simulation results as well. Second, although P_DETFF requires fewer transistors, it

does not prove that the final area it required is the smallest. In order to satisfy the timing requirement of functionality, transistor MP1 and MP3 in Yu's design cannot use minimum-sized devices; they should be increased to 3 times larger than the minimum size.

Table 1 gives a comparison about the transistor count requirement between each implementation discussed in this section. Yu's design uses the fewest transistors.

Table 1 Transistor count summary of each implementation discussed

	Idea I Pulse generation		Idea II Two data path			
	Nedovic's [5]	Tsai's [20]	Hossain's [21]	Kuo's (a) [22]	Kuo's (b) [22]	Yu's [10]
# of Transistors	32	27	20	20	22	12

Clock gating techniques

The clock gating technique [23] has been developed to avoid unnecessary power consumptions, like the power wasted by timing components during the time when the system is idle. Specifically for flip-flops, clock gating means disabling the clock signal when the input data does not alter the stored data. It can be applied from the system level where the entire functional unit can be selectively set into sleep mode, or from the sequential/combinational circuit level where some parts of the circuit are in sleep mode while the rest of the block are operating.

Strollo et al. [8] proposed a gating logic for negative edge-triggered flip-flops, shown in Figure 9. It compares the input data D to output data Q and according to the comparison will disable those unnecessary clock switching. More specific for this clock-gating scheme, whenever the comparator detects the change at the input, the gated clock

signal will generate a pulse. Otherwise, the gated clock signal maintains logic high. If this clock-gating scheme is used on the double edge-triggered flip-flop, then the flip-flop will be triggered twice for every data transition, which causes extra power consumption.

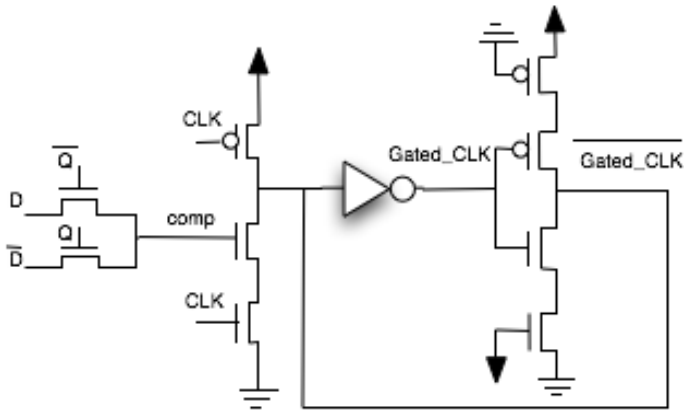


Figure 9: Clock gating technique for negative edge-triggered flip-flop

Seyedi et al. [9] developed a clock-gated, static pulse flip-flop, shown in Figure 10. The key idea of this design is to use an external circuit to generate a pulse when the input and output are different according the old clock signals. Like Strollo's clock-gating techniques, the Seyedi's design also can only respond at one specific edge, which is not suitable for DETFFs. Besides, the large number of transistors makes Seyedi's design a candidate for improvement.

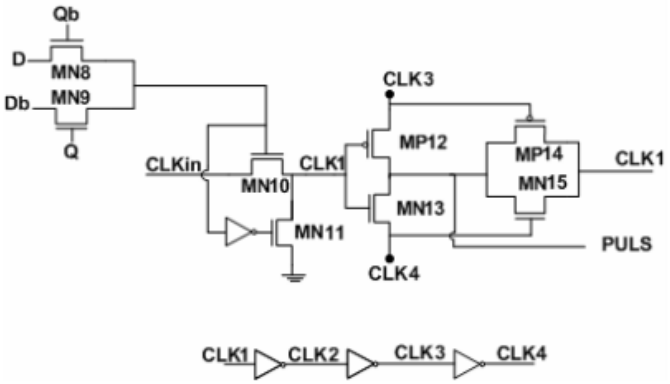


Figure 10: Clock gating part of Seyedi's design [9]

CHAPTER IV

PROPOSED DESIGNS AND IMPLEMENTATION

In this thesis, there are two designs. One is a double edge-triggered flip-flop built with the dual data path idea. It is called T_DETFF [24] that is based on transmission gates; the other one modifies T_DETFF with the addition of a new clock gating technique especially for double edge-triggered flip-flops, called G_DETFF [24]. In Chapter V, these two designs are compared with two benchmarks, Yu's design [10] and a generic single edge-triggered flip-flop at different operating conditions.

Optimized transmission gate-based double edge-triggered flip-flop (T_DETFF)

As discussed in Chapter III, using pulse generation for double edge-triggered flip-flops requires more transistors to achieve the proper functionality. Many of those transistors are related to the clock signal, which will increase the activity factor α, and cause increased power consumption. So the dual data-path idea was chosen as the targeted implementation scheme. Also transmission gates are used to diminish the undesirable threshold voltage effects that lead to the weak logic signals in pass transistors. Instead of using a loop comprised of two inverters and one transmission gate as the logic keeper, T_DETFF only uses an inverter and a PMOS transistor to keep the logic level. It is shown in Figure 11.

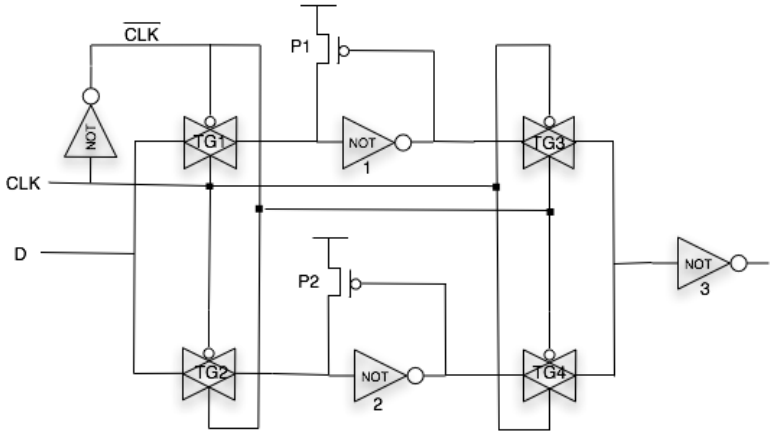


Figure 11: T_DETFF – Double edge-triggered flip-flop with transmission gates

Likewise, the two data paths are connected in parallel. The upper data path is triggered on the rising edge, and lower data path is triggered on the falling edge. An inverter and a PMOS transistor are used together to hold the logic level when the front transmission gate is closed. When the data value is high, the inverter switches the signal to low, which will make the PMOS transistor pull the data up to high. When the data value is low, the inverter switches the signal to high, which will isolate the data from V_{DD} and keep the value low. Both Yu's design [10] and the proposed DETFF have been implemented in the Cadence layout tool with NCSU CDK [25] at 0.5 µm technology. Because all the transistors in the proposed circuit are minimum size, the layout area has not increased significantly.

P_DETFF VS. T_DETFF: weak logic problem caused by pass transistor

The weak logic problem of Yu's design P_DETFF in Fig. 8 mentioned in Chapter III, can be seen in simulation waveforms (Figure 12). The weak logic "0" produced by the PMOSFET at the second stage of Yu's design prevents the output from returning to

logic 0 until the next clock resolves the problem. The peak of current flow in that amount of time has been prolonged, so the total power consumption increased when compared with the flip-flop implemented using transmission gates.

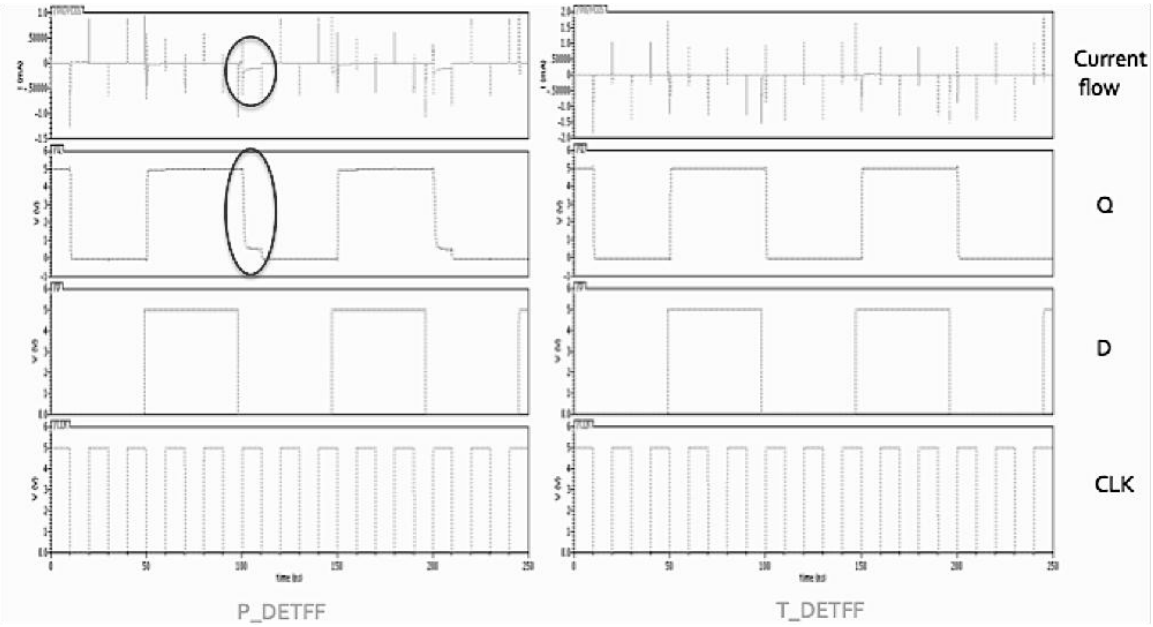


Figure 12: P_DETFF VS. T_DETFF simulation results – Weak logic problem of P_DETFF

Clock-gated double edge-triggered flip-flop with transmission gates (G_DETFF)

The G_DETFF contains two major parts, the T_DETFF and the clock-gating circuitry which includes a comparator and the clock-gating module (Figure 13). The data signal arrives into the T_DETFF and the comparator simultaneously, and the comparator checks the current data input D and the output Q. If D and Q are not equal, which means the input has changed since the last comparison, then an active gated clock signal will be generated by the clock gating circuitry, and the gated clock signal will be sent to the T_DETFF to trigger the storage. The input data will be passed through to the output. Otherwise, the entire system remains in the previous state.

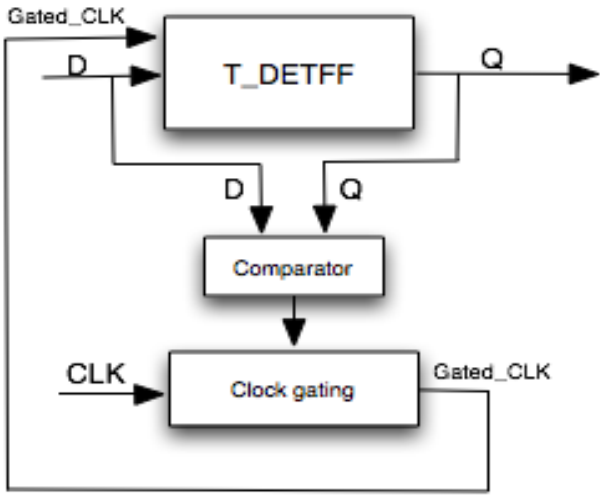


Figure 13: Block diagram of G_DETFF

The inside of the T_DETFF is Design I as shown in Figure 11. The clock-gating circuitry is implemented as Figure 14. To avoid the weak logic generated by pass transistors causing improper circuit operation, transmission gates are used to implement the comparator.

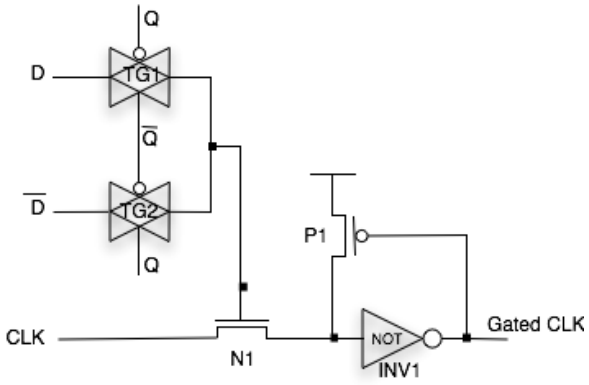


Figure 14: Proposed new clock gating technique

The comparator continuously monitors the input, D, and the output, Q. When D and Q are equal, that means the input has not changed since the last transition. Therefore,

a logic low signal will be transmitted to shut off switch N1. The gated clock signal stays inactive, as well as the remaining circuitry. Whenever the input changes, then D and Q will be different, and the comparator will transmit a logic high signal to turn on the switch N1. So the actual clock signal will pass through the switch N1. As soon as the gated clock signal is toggled, it will retrigger the main part of the G_DETFF. Then the input and output will be equal, which will shut the switch N1 off again. Normally, the system remains in a standby status when D equals Q. The logic keeper is used to maintain the gated clock signal during the standby period, and this structure corrects the weak logic "1" generated by the pass transistor NMOSFET. The proposed new clock-gating scheme only requires 8 transistors.

The actual implementation of the proposed G_DETFF is shown in Figure 15. It connects the output Q of the T_DETFF (which is also the Q of the G_DETFF) and data input to the input of the comparator. According to the comparison result and current clock signal, the gated clock signal is generated and sent back to the main flip-flop circuitry.

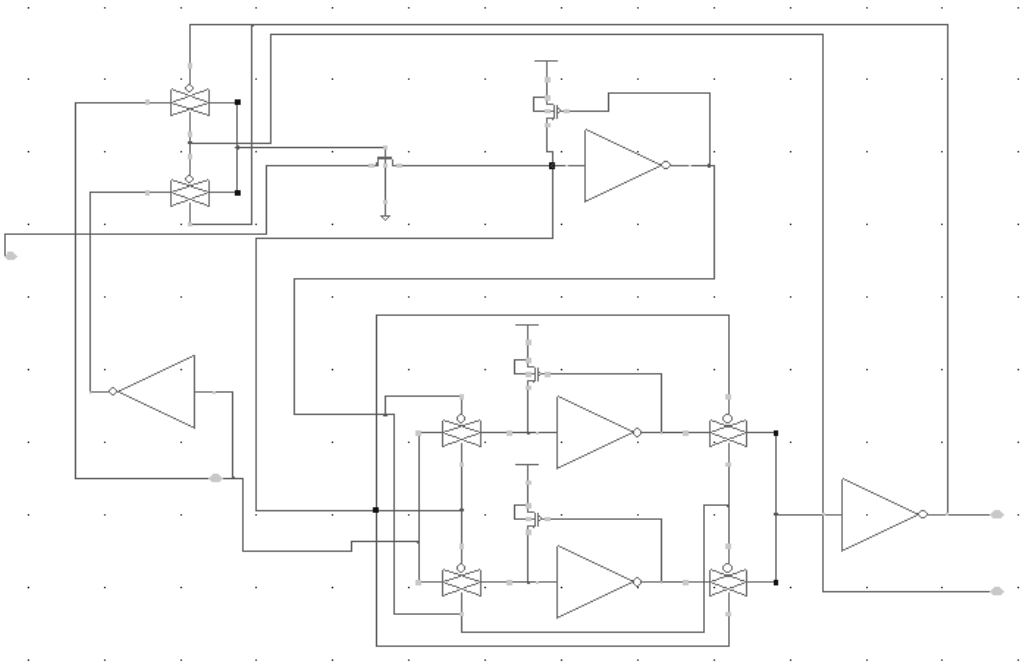


Figure 15: G_DETFF – Gated double edge-triggered flip-flop

Proposed clock gating technique vs. Generic clock gating technique

The previous clock gating techniques discussed in [8][9] generate a pulse, which triggers the double edge-triggered flip-flop twice for every single data transition. This effect makes the technique power-inefficient for double edge-triggered flip-flops. In order to save the power wasted on the redundant clock edges, the new clock gating technique was developed particularly for double edge-triggered flip-flops. The simulation waveforms (Figure 16) compare the two clock gating techniques. The current flow of the flip-flop shows that the proposed clock gating technique has better performance on power saving than the previous generic clock gating techniques.

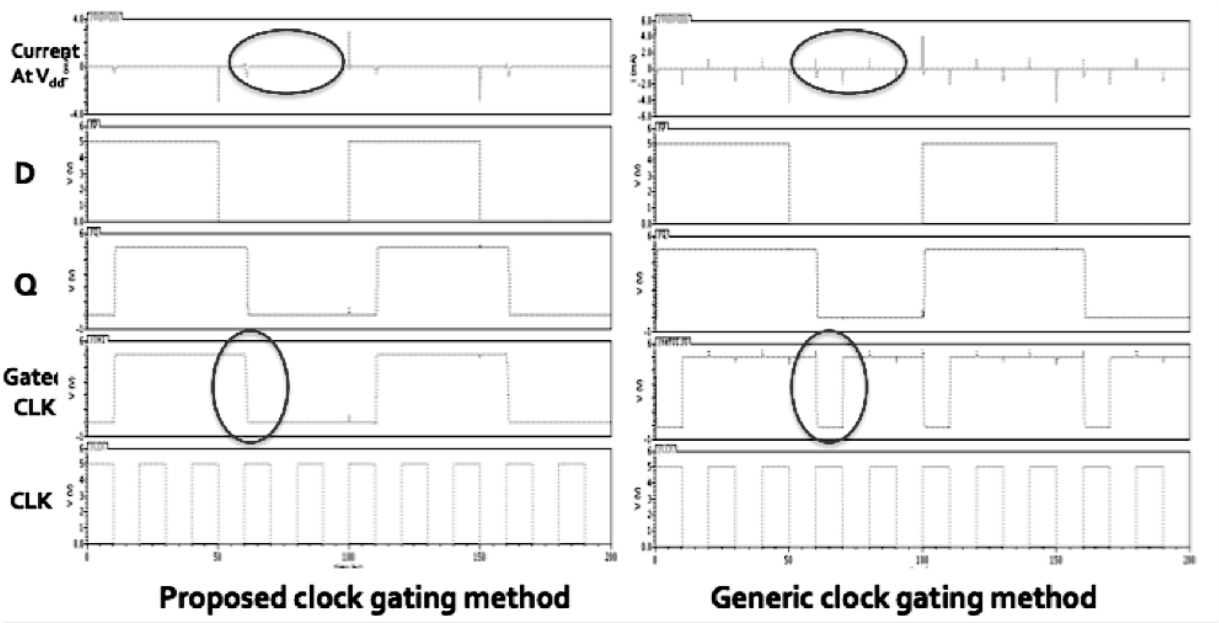


Figure 16: Proposed clock-gating technique vs. Generic clock-gating technique

The new technique removes the redundant gated clock signal transition. This signal is more suitable for a double edge-triggered flip-flop and saves more power.

CHAPTER V

CIRCUIT SIMULATION, ANALYSIS, AND COMPARISON

The proposed circuits and the benchmark circuits have been designed and implemented to the layout level with a 0.5 μm technology. This technology enables fabrication using the MOSIS Tiny Chip [26], and the proposed flip-flop is used in a 16-bit counter for future testing within an integrated circuit. The circuits were simulated using the SpectreS simulation tool with a supply voltage of 5 V at room temperature. A fixed value of 10 fF is used for the load capacitance.

Circuit simulation spanned the switching activity factor α, where

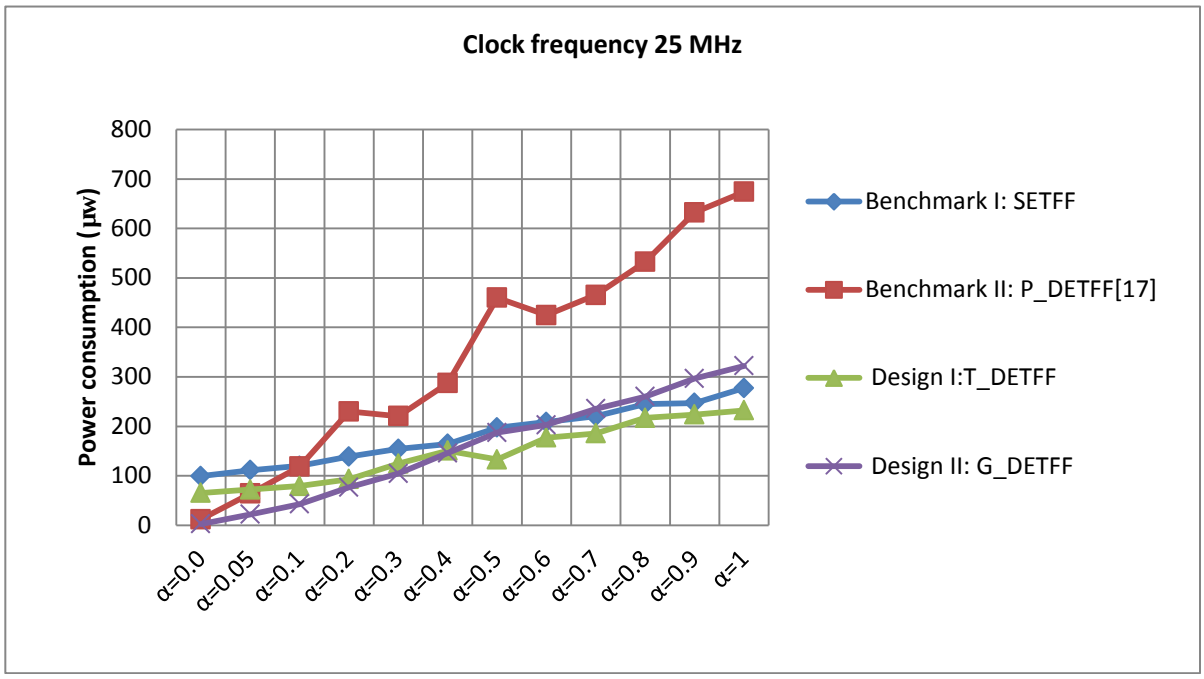
$$\boldsymbol{\alpha = Data\ switching\ frequency / Clock\ frequency},$$

from 0 through 1, at the following clock frequencies: (1) 25 MHz, (2) 50 MHz, and (3) 100 MHz. All the signals are in the shape of a periodic square waveform. For a fair comparison, the Benchmark I: SETFF operated at a doubled clock frequency to equalize the same data throughput.

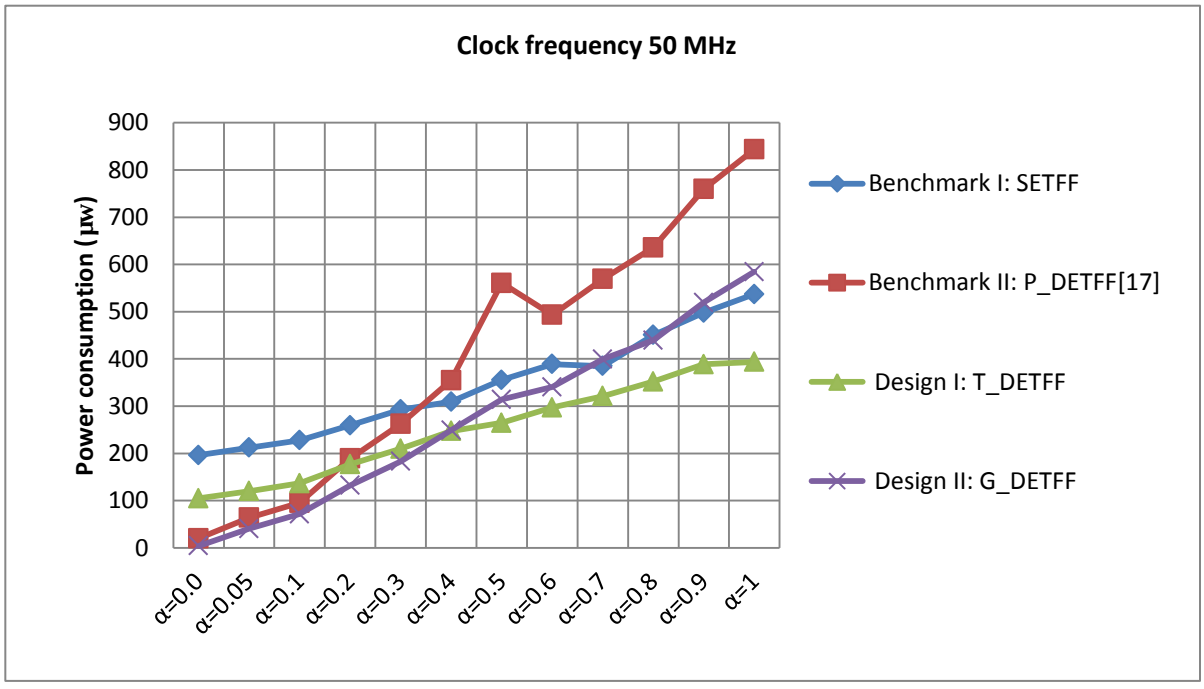
The Design I: T_DETFF and Design II: G_DETFF have been compared with Yu's design Benchmark II: P_DETFF [10] and Benchmark I: SETFF described in Figure 2. Power consumption has been calculated following this formula:

$$\boldsymbol{P = \frac{V_{dd} \cdot \int_0^T I_{dd}}{T}},$$

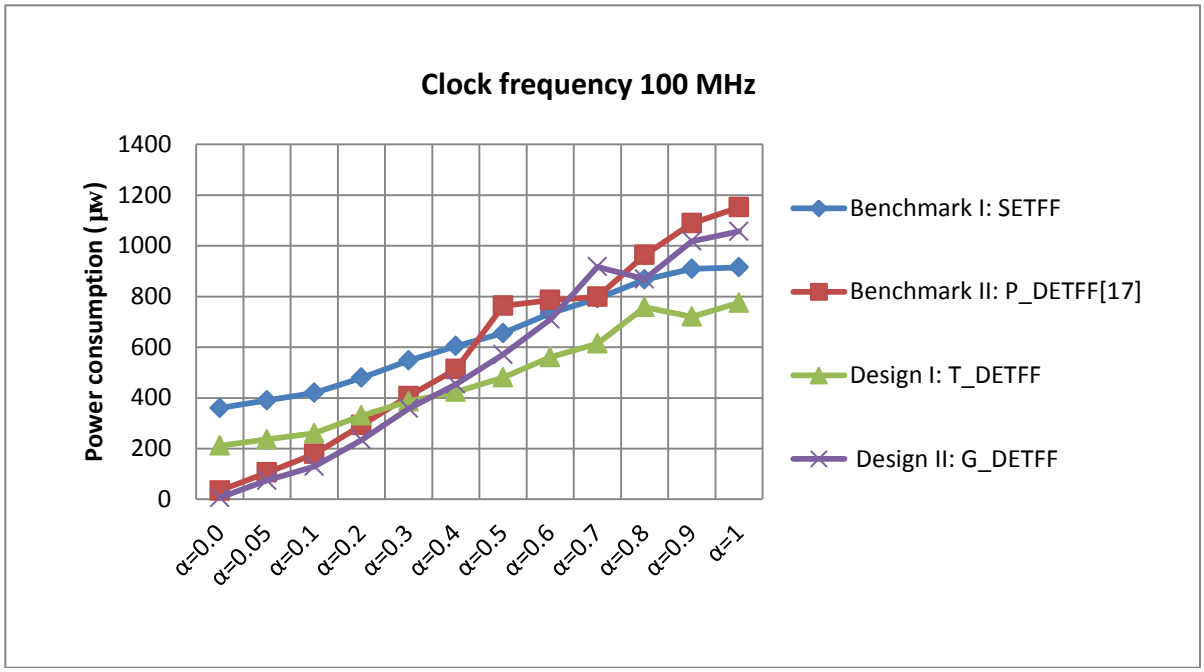
where V_{dd} is the supply voltage, I_{dd} is the supply current, and T is the period.


Clock frequency 25 MHz
Power consumption (µw)
800
700
600
500
400
300
200
100
0
α=0.0
α=0.05
α=0.1
α=0.2
α=0.3
α=0.4
α=0.5
α=0.6
α=0.7
α=0.8
α=0.9
α=1
Benchmark I: SETFF
Benchmark II: P_DETFF[17]
Design I:T_DETFF
Design II: G_DETFF

(a)


Clock frequency 50 MHz
Power consumption (µw)
900
800
700
600
500
400
300
200
100
0
α=0.0
α=0.05
α=0.1
α=0.2
α=0.3
α=0.4
α=0.5
α=0.6
α=0.7
α=0.8
α=0.9
α=1
Benchmark I: SETFF
Benchmark II: P_DETFF[17]
Design I: T_DETFF
Design II: G_DETFF

(b)

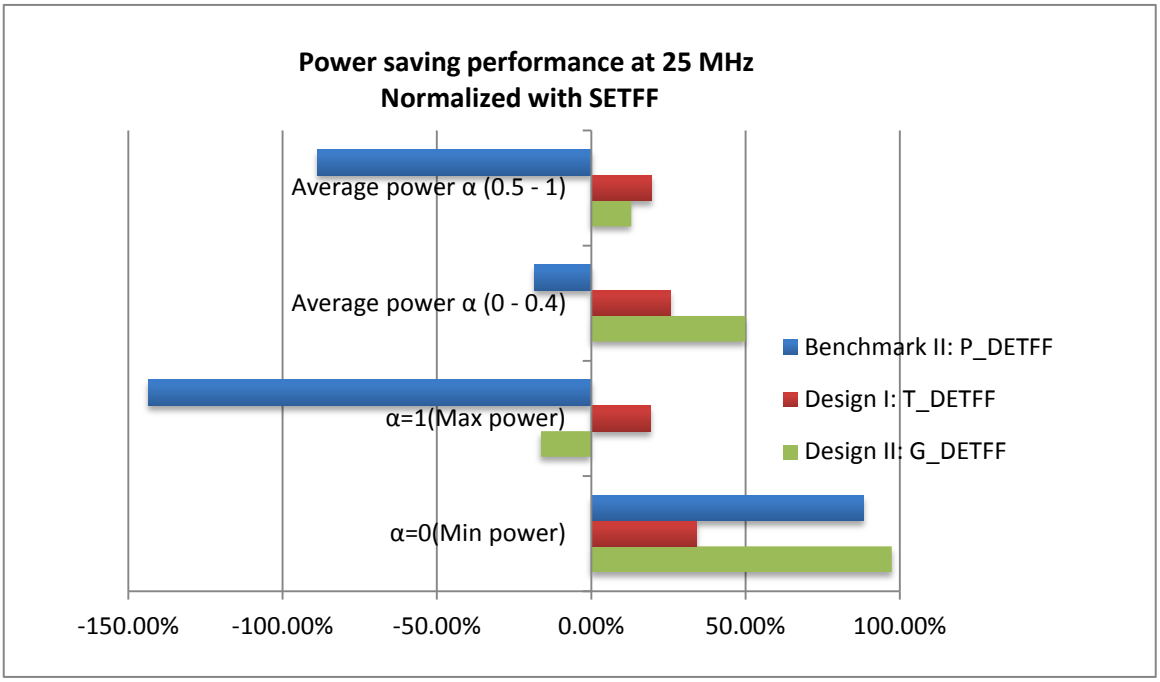


(c)

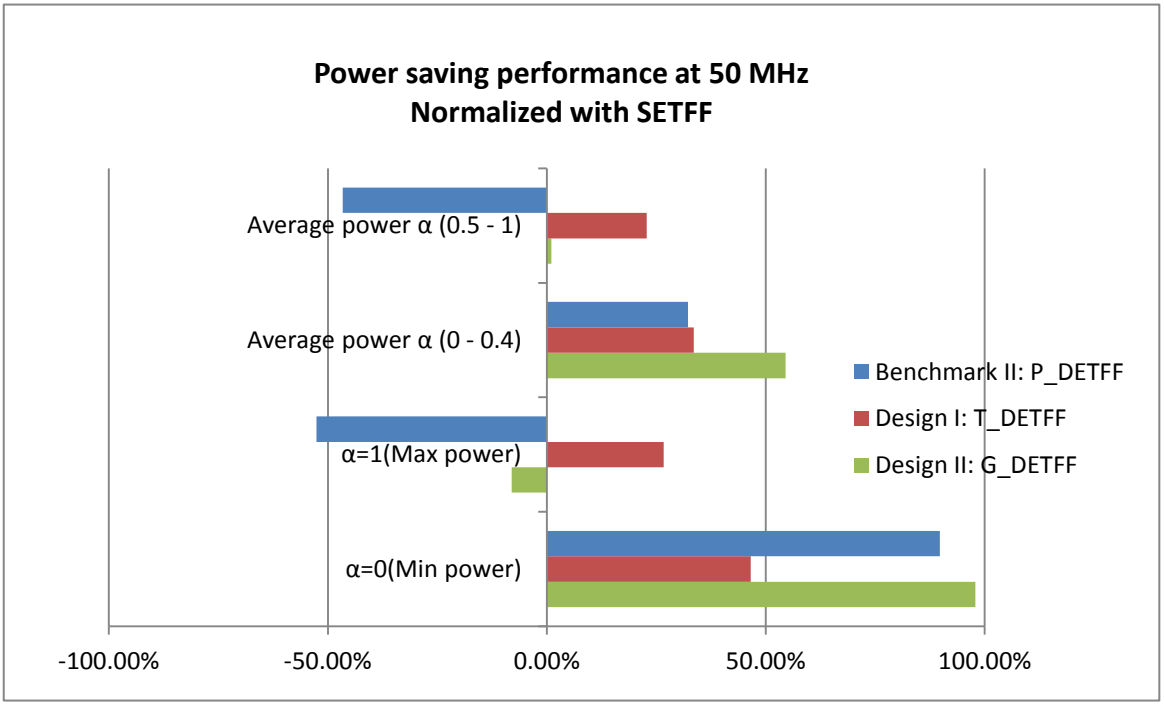
Figure 17: Simulation results of power dissipation under different input signal switching activity.

Figure 17 shows that all the designs share the same trend at different clock frequencies, but the power-saving capability of Design I and Design II is more apparent at lower clock frequencies. The Benchmark I: SETFF operates at double the clock frequency of DETFF's to match the same data throughput. The Benchmark I: SETFF almost always behaves worse than the proposed two designs. Benchmark II: P_DETFF performs well initially, but it becomes very power-hungry with increasing activity factor, especially for a lower clock frequency. So Benchmark I: SETFF is used as baseline for a good comparison.

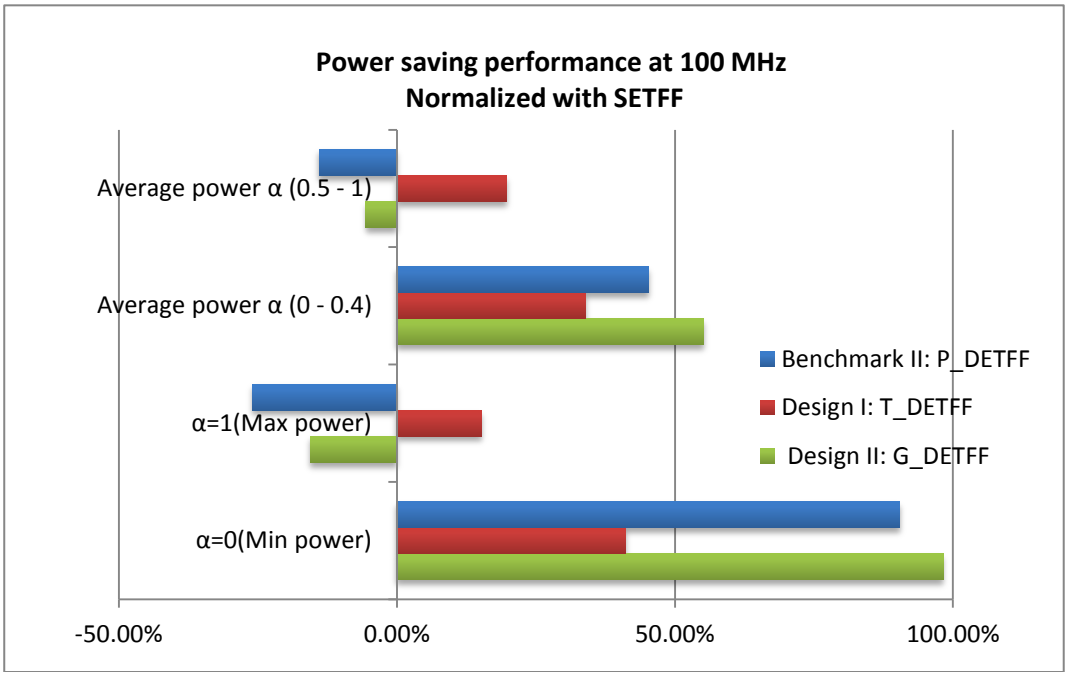
There is a crossover point, $\alpha = 0.4$, for Design I and Design II. When α is lower than 0.4, Design II has the better power-saving performance, and when α is greater than 0.4, Design I has the better power savings. Thus, the regions will be discussed separately.


Power saving performance at 25 MHz
Normalized with SETFF
Average power α (0.5 - 1)
Average power α (0 - 0.4)
α=1(Max power)
α=0(Min power)
Benchmark II: P_DETFF
Design I: T_DETFF
Design II: G_DETFF
-150.00%
-100.00%
-50.00%
0.00%
50.00%
100.00%

(a)


Power saving performance at 50 MHz
Normalized with SETFF
Average power α (0.5 - 1)
Average power α (0 - 0.4)
α=1(Max power)
α=0(Min power)
Benchmark II: P_DETFF
Design I: T_DETFF
Design II: G_DETFF
-100.00%
-50.00%
0.00%
50.00%
100.00%

(b)



(c)

Figure 18: Improvement of G_DETFF, T_DETFF, and P_DETFF in power reduction in 25MHz, 50MHz and 100MHz, normalized with SETFF at the same data throughput.

Figure 18 shows the improvement in power reduction of the four different flip-flops discussed in this paper at 25 MHz, 50 MHz, and 100 MHz. The higher comparison value, the better improvement on power saving. All the comparisons are made against the baseline Benchmark I: SETFF, and the results suggest that all circuits basically share the same trend on power saving performance for different clock frequencies. Design II: G_DETFF performs best in region $\alpha < 0.4$, and Design I: T_DETFF becomes more power efficient when α over 0.4.

Take clock frequency 50 MHz as an example. When α is less than 0.4, the G_DETFF saves 33.14% power compared with Yu's design (Benchmark II: P_DETFF), and saves 54.55% power compared with baseline benchmark SETFF on average. When the system is idle, G_DETFF can save up to 98% power of SETFF, and consumes 80% less power than P_DETFF.

When α is greater than 0.4, the proposed T_DETFF becomes more power efficient. Comparing with the conventional SETFF, the proposed T_DETFF saves 23% of the power consumption on average. When α = 1, (i.e., data changes every clock cycle) the T_DETFF saves 27% power compared with SETFF. The T_DETFF is not compared with P_DETFF because it performs worse than the baseline benchmark SETFF in this region.

The proposed Design I: T_DETFF and Design II: P_DETFF performed best at saving power in region $\alpha \leq 0.4$ and $\alpha > 0.4$ respectively. In Table 2, the two proposed designs are compared with Benchmark I: SETFF and with each other, across clock frequency from 25 MHz to 100 MHz. The data suggest that both of G_DETFF and T_DETFF have a stable outcome on power saving. Generally, the G_DETFF saves half power of SETFF and 1/3 power of T_DETFF on average when the data switching activity less than 0.4, which would benefit digital systems, like bridge sensors, where input data changes infrequently. T_DETFF saves around 1/5 power compared to the other two circuits on average, which makes it a good candidate for digital components, like counters, where data values switch with the clock signal.

Table 2 Comparison of Design I: T_DETFF and Design II: G_DETFF

	α ≤ 0.4(Average)		α > 0.4(Average)	
	G_DETFF vs. SETFF	G_DETFF vs. T_DETFF	T_DETFF vs. SETFF	T_DETFF vs. G_DETFF
25 MHz	50%	33%	19%	22%
50 MHz	54%	32%	23%	22%
100 MHz	55%	32%	20%	23%

The time required for a data value to appear on the output of the flip-flop (D-to-Q) is measured as a performance metric. Since D-to-Q latency depends on when the data transition occurs, the timing parameter CLK-to-Q is first measured, and according to the best and the worst case of D-to-Q, the average D-to-Q is calculated by using formula:

$$Average\ D\_Q = ClK\_Q + \frac{T}{4}.$$

Also, the PDP (Power Delay Product) is calculated by multiplying power consumption with average D_Q. Table 3 presents the final energy consumption of different flip-flops at a clock frequency of 50 MHz. The clock gating hinders Design I: G_DETFF somewhat on timing, and the Design II: T_DETFF has the best performance on timing.

However, the Design I: G_DETFF still the most energy-efficient alternative in region ($\alpha \leq 0.4$). Comparing with Benchmark II: P_DETFF and Benchmark I: SETFF in this region, it saves 1/3 and 1/2 the amount of energy respectively. When ($\alpha > 0.4$), the Design II: T_DETFF is the best one for saving power, and it saves 1/2 and 3/5 the amount of energy compared to Benchmark II: P_DETFF and Benchmark I: SETFF respectively. The Benchmark II: P_DETFF require the least area to implement. So there will be trade off that designers have to make between timing, power, and area.

Table 3: Comparison of timing, energy consumption, and areas

	Clk-to-Q (ns)	α ≤ 0.4 Average PDP (pJ)	α > 0.4 Average PDP (pJ)	Transistor count	Area (μm^2)
SETFF	0.37	2.6	4.5	16	111.2
P_DETFF	0.66	1.8	3.6	12	73.4
T_DETFF	0.22	1.7	1.8	16	116.4

G_DETFF	0.45	1.2	2.3	24	157.5

CHAPTER VI

CONCLUSION AND FUTURE WORK

In this thesis, a new clock gating technique and an optimized double edge-triggered flip-flop has been developed. The clock gating technique avoids unnecessary power dissipation from clock switching, and the implementation with transmission gates overcomes the drawbacks from the pass transistors to make the output signal clean and stable.

The Design I: T_DETFF was built based on transmission gates, which has better power savings when the data switching activity factor α range from 0.4 to 1. It consumes about 20% less power than SETFF, and 22% less power compared to G_DETFF.

The Design II: G_DETFF can save up to 98% of the power compared to Benchmark I: SETFF when the input is idle. Also, it decreases around 50% power consumption compared to SETFF, and around 33% power consumption compared to Design II: DETFF when α is in the range of (0 to 0.4).

For the final energy consumption, the clock frequency 50 MHz is used as an example. In the range of $\alpha \leq 0.4$, the G_DETFF saves 33% of the energy compared to the P_DETFF and 50% of the energy compared to the SETFF. The T_DETFF saves 50% compared to the P_DETFF and 60% compared to SETFF in the range of $\alpha > 0.4$. The simulation results suggest that the G_DETFF design is suitable for lower data switching cases, and the T_DETFF design is the best candidate for high data switching designs.

With the scaling of design technology, the supply voltage has decreased. The designs in this thesis must be implemented in nanometer technologies to verify the potential power reduction. Future work includes using the Oklahoma State University freePDK 45-nm system-on-chip library [27] to re-implement Design I and Design II to perform further analysis on the power and performance.

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