IMPACT OF TEMPERATURE ON SINGLE-EVENT TRANSIENTS IN DEEP SUBMICROMETER BULK AND SILICON-ON-INSULATOR DIGITAL CMOS TECHNOLOGIES

By

Matthew John Gadlage

Dissertation

Submitted to the Faculty of the

Graduate School of Vanderbilt University

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

May, 2010

Nashville, Tennessee

Approved:

Professor Ronald D. Schrimpf

Professor Bharat L. Bhuva

Professor Robert A. Reed

Professor W. Timothy Holman

Professor Senta V. Greene

ACKNOWLEDGMENTS

I have so many people that I would like to thank for making this work possible, but first and foremost I would like to thank my family for their incredible support and encouragement. I would also like to give a special thanks to my little brother, Dr. Mark Gadlage, who was able to share this entire graduate school experience with me.

Special thanks also go to all the past and present students of the RER group for all their help in this effort, especially Dr. Balaji Narasimham for aiding in the SET measurement circuit design, Jon Ahlbin for help with testing and TCAD simulations, and Vishwa Ramachandran for his incredible work with the extreme heavy-ion temperature testing. I would also like to thank all of the professors from the RER group who are not on my committee for all of the helpful discussions over the years.

I would also like to thank Dr. Ronald Schrimpf and Dr. Bharat Bhuva for being great mentors throughout this whole process. Also, I'd like to thank the rest of my committee; Dr. Robert Reed, Dr. Tim Holman, and Dr. Senta Greene for their help in finishing this dissertation.

I want to give a special acknowledge to some industry partners who helped make this work possible including Dr. Pascale Gouker at MIT Lincoln Laboratory for providing the SOI test circuits and beam time to test them and Robert Shuler of NASA Johnson Space Flight Center for help with the heavy-ion temperature testing.

A final thank you goes to NSWC Crane for their financial support of this effort and for providing me the opportunity to pursue this degree. I would especially like to thank Lydell Evans and Steven Clark of NSWC Crane for their encouragement and enthusiasm.

TABLE OF CONTENTS

LIST OF TABLES

Table Page

LIST OF FIGURES

CHAPTER I

INTRODUCTION

For over thirty years, ionizing particles have been affecting semiconductor reliability. In the 1970's, the first single-event effects due to cosmic rays [Bind-75, Pick-79] and alpha particles [May-78, May-79] were reported. With the rapid advancement in semiconductor technology since then, new single-event phenomena have emerged. In the late 1990's, advanced electronics became fast enough that a new effect in digital circuits, known as single-event transients (SETs) appeared. During the 2000's, researchers predicted that these SETs would become the dominant semiconductor electronic reliability issue [Shiv-02]. While some researchers predicted that the SET problem would become worse with each technology node [John-00, Gadl-04, Dodd-04, Nara-07], many seemingly conflicting results were reported. As one example, Baze et al. [Baze-06] measured the maximum time duration of these SETs in a 130-nm technology to be around 300 ps, while data published by Benedetto et al. [Bene-06] showed that SETs could be upwards of 2 ns in a nearly identical technology.

With the large amount of research on SETs, one aspect that has been mostly ignored has been the effect of temperature on the time duration of these transients. The temperature ranges over which some space missions need to operate can be extreme. Thus, the role of temperature for all radiation effects is of vital importance for space systems. For example, on the moon the temperature can range from -230° C to +120° C. So while it is known that SETs can be a reliability issue for space electronics, the impact

of temperature on these SETs remains largely unknown. Determining the effect of temperature on SETs is the key aspect of this dissertation. However, to understand fully how temperature will impact SETs, a complete understanding of SETs at room temperature is needed. As illustrated by the example of the Baze and Benedetto research, this alone is no easy task and is an ongoing active research area. In this dissertation, data from over a dozen experiments on ten SET test structures fabricated in a myriad of semiconductor technologies will be presented. The data from these test structures give valuable insight into how the SET problem is changing with each new technology. With the understanding gained from these data, some of the questions of why different researchers have reported seemingly conflicting results are answered. Finally with the answer to some of the questions, for the first time, how temperature affects the time duration of SETs is explored.

This dissertation begins with an introduction to semiconductor technology and the space radiation environment. SETs are defined in detail and their relationship to semiconductor reliability is explained. In the final section of Chapter II, an SET measurement circuit that is used throughout the dissertation is introduced. In Chapter III, factors affecting SETs at room temperature in “bulk” semiconductor technologies are discussed. An in-depth look at why different test circuits can give conflicting results is provided. The dissertation then looks at SETs in a different semiconductor process known as silicon-on-insulator (SOI) in Chapter IV. The data presented in Chapters III and IV set the foundation for the "heart" of the dissertation in Chapter V. In Chapter V, data on SETs in four different technologies taken over wide temperature ranges are presented. The mechanisms responsible for SETs changing with temperature are also discussed. In

Chapter VI, lessons learned from the mechanisms impacting SETs over temperature lead to the development of unique test structures and a set of data that experimentally confirm the key hypothesis presented in Chapter V. In the final chapter, a short data analysis is presented that helps define future directions for exploring the SET problem.

CHAPTER II

SINGLE-EVENT EFFECTS - BACKGROUND

Ionizing radiation can cause a considerable number of negative effects for space-based electronics. Different types of radiation effects include total-dose [Lera-99, Schw-02, Barn-05, Oldh-03, Alex-03, Glov-80], displacement-damage [Srou-88, Summ-92], and single-event effects [Pete-83, Pick-83, McNu-90, Sext-92, Mass-93]. In this dissertation, only single-event effects will be discussed. Single events can be classified into several types [Dodd-03] including: single-event upsets (SEUs), single-event latchup (SEL), single-event burnout (SEB), single-event gate rupture (SEGR), and single-event transients (SETs). Single-event transients can be broken down further into analog or digital SETs. This dissertation focuses primarily on digital single-event transients. A digital SET is nothing more than a glitch induced by a radiation event in a digital circuit. The mechanisms and conditions under which a digital SET can be a problem are discussed later in this chapter.

The rest of this chapter consists of: the scaling of digital CMOS technologies, the space radiation environment, single-event transient mechanisms, the difference between bulk and SOI (silicon-on-insulator) technologies, and single-event testing. The chapter concludes with a description of an SET measurement circuit that will be used throughout this dissertation.

CMOS Scaling

In the late 1950's, the first integrated circuit (IC) was developed by Jack Kilby of

Texas Instruments [Kilb-63]. Since then the number of transistors on an integrated circuit has been growing exponentially. The rapid growth in IC technology has led to significant improvement in both computer and mobile electronic functionality. A concept developed by Gordon Moore (the founder of Intel), known as Moore's law, has been used to describe the rapid advancement in the semiconductor industry [Moor-65]. One variation of Moore's law states that the number of transistors that can be placed on an IC doubles every two years. (Another interpretation of Moore's law states that processing power, speed, and number of DRAM cells double every 18 months to two years.) One side effect of the improvement in semiconductor technology has been that electronic devices have become more susceptible to certain radiation effects. In particular, the closer spacing of transistors, smaller nodal capacitances, and lower operating voltages associated with CMOS scaling have all led to enhanced susceptibility to single event

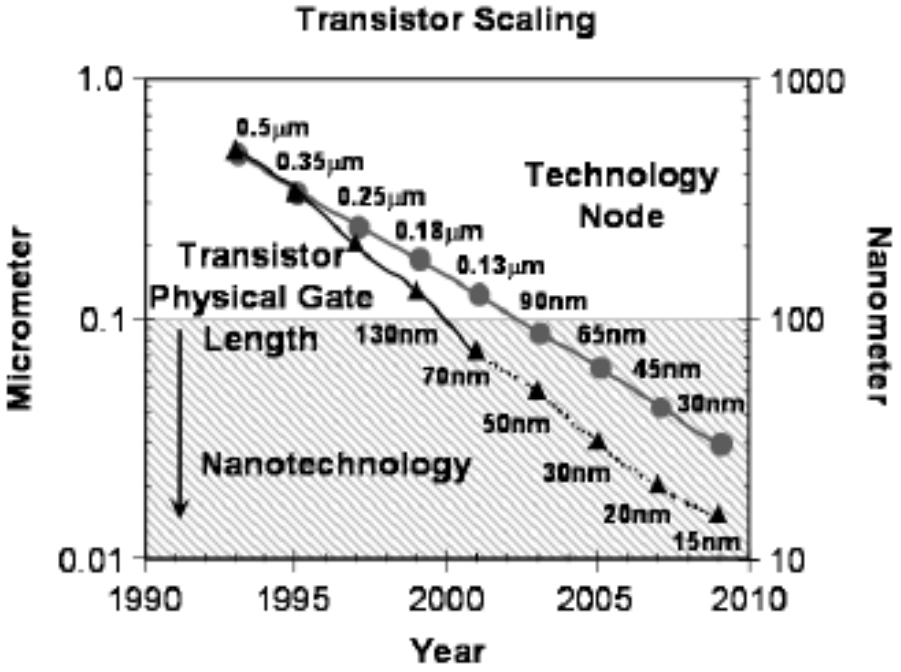

Fig. 2.1: A plot from Intel [Chau-05] showing how the physical gate length of a transistor has continued to shrink over the past two decades.

effects.

With every new semiconductor technology, a dimension known as the feature size is used to characterize that technology. The feature size is a measure of the smallest element possible on an IC fabricated in that technology. In advanced ICs, feature sizes are usually measured in nanometers. Traditionally, the smallest feature size was equal to the width of the gate (i.e., the distance from the drain to the source in a MOS transistor), however, in sub 100-nm technologies the effective width of the gate may actually be smaller than the feature size. In this dissertation, single-event transients will be discussed in technologies with feature sizes ranging from 180 nm down to 65 nm.

Space Radiation Environment

Advanced electronic devices often have to operate in harsh environments. Perhaps the harshest of these environments is the space environment. Outside the earth's atmosphere, spacecraft electronics face a constant bombardment of highly energetic particles. These energetic particles can come from one of three sources [Xaps-06]. The first includes particles trapped in the Earth's magnetic field in what are known as the Van Allen Belts. The second includes all radiation from the sun (typically emitted in bursts known as solar events). The final source of energetic particles is galactic cosmic rays that originate outside our solar system.

When one of these energetic particles passes through a material, it loses energy through interactions with the material. The energy loss is due primarily to the interactions of the particle with bound electrons in the material. These interactions cause the direct ionization of the material and the formation of a dense track of electron-hole

pairs. A commonly used term for the energy deposited by an ion as it passes through a material is linear energy transfer (LET). The LET is a measure of the energy deposited per unit length as a particle travels through a material. LET values are usually given in units of MeV-cm^2/mg, which is the energy deposited per unit length divided by the density of the target material. In space, the lower the LET of the energetic particle, the higher the probability it has of occurring. As seen in Fig. 2.2, a particle with an LET of 1 MeV-cm^2/mg is approximately 10 orders of magnitude more likely to occur than a particle with an LET of 100 MeV-cm^2/mg.

Highly energetic particles can also generate electron-hole pairs through a process known as indirect ionization (as opposed to the direct ionization process discussed in the previous paragraph). Indirect ionization occurs when an energetic particle causes a nuclear reaction with a material in an IC. The byproducts of the reaction create the

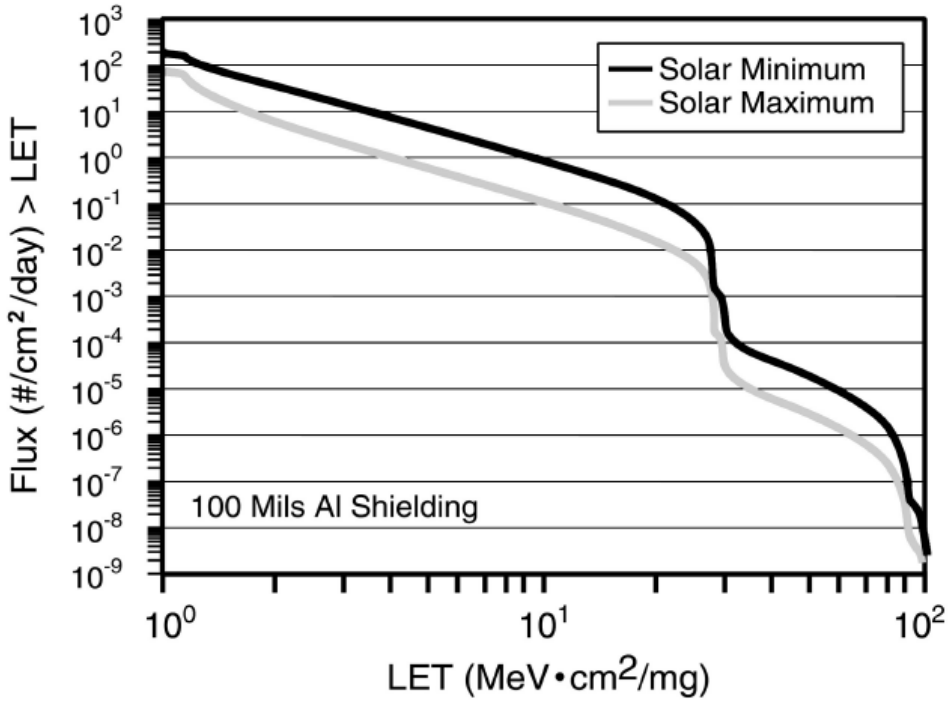

Fig. 2.2: Flux of energetic particles in space as a function of linear energy transfer (LET) [Xaps-06]

ionizing particles that directly create the electron-hole pairs. It is through this indirect ionization process that neutrons (and high-energy protons) are also able to cause single-event effects.

Single Event Mechanisms

By knowing the LET of the heavy ion generating charge through direct ionization, one can calculate the number of electron-hole pairs created if the ion strikes a silicon wafer. This knowledge goes a long way in helping to quantify single-event effects. In silicon, about 3.6 eV is needed to create one electron-hole pair. Knowing that the density of silicon is 2.42 g/cm^3, one can find the number of electron hole pairs created per ion track length (L) by using the following equation [Mavi-02]:

$$Q\ (fC) = 10.8 \times L\ (\mu m) \times LET\ (MeV\text{-}cm^2/mg)$$

Thus an ion with an LET of 1 MeV-cm^2/mg will leave approximately 10.8 fC along each micrometer of its track.

For generated charge to cause a single event, the charge has to be collected at a circuit node. Three primary mechanisms affect the amount of charge collected in an electronic device: drift, diffusion, and recombination. Drift describes the movement of charge (electrons and holes) in the presence of an electric field. Diffusion is the movement of charge due to a concentration gradient. Finally, recombination occurs when electrons and holes annihilate one another.

Charge is collected primarily only when an ionizing particle passes through a depletion region. Since depletion regions are largest around reverse-biased junctions, the sensitive region of a CMOS device is typically limited to the reversed-bias drain/well (or drain/substrate) junctions. The drift component of charge collection consists primarily of the charge collected promptly as the ion passes through the depletion layer. However, the ion track can cause a potential contour deformation that leads to the depletion layer extending deeper into the device in the direction of the ion track. This extension of the depletion layer is known as "funneling" and it results in the collection of additional charge [Hsie-81].

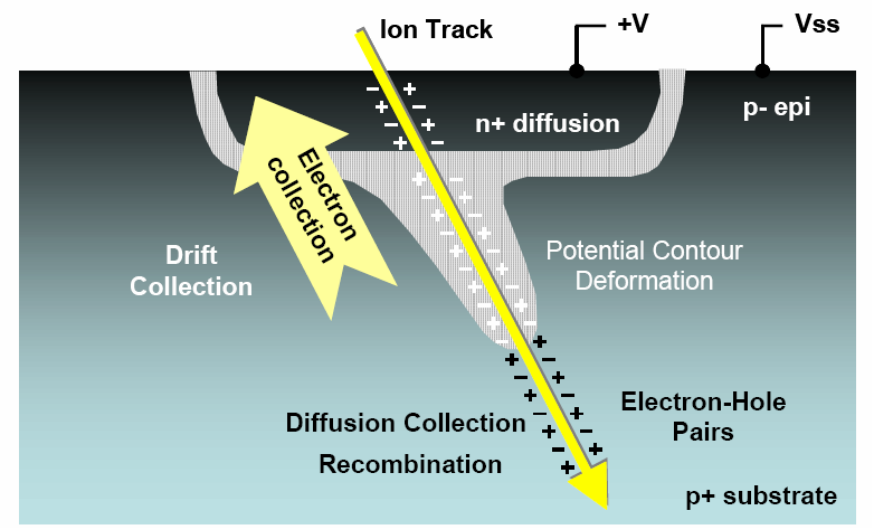

Fig. 2.3: Illustration showing the different charge collection mechanisms during a single event [Baum-05]

Bulk and SOI Technologies

In this dissertation, single-event transients in two types of semiconductor technology will be discussed: bulk and silicon-on-insulator (SOI). As the name "silicon-on-insulator" suggests, an SOI technology consists of a silicon layer on top of an insulating layer [Coli-01]. The insulating layer is typically silicon dioxide (SiO_2) (but can also be a

different insulator material such as sapphire). The transistors are placed in the silicon layer above the insulating layer. The addition of the insulating layer reduces parasitic capacitances and eliminates any latchup path. The insulating layer also limits the amount of charge that can be collected from a single event [Muss-01]. As illustrated in Fig. 2.4, the amount of charge that can be collected in an SOI technology is limited to the thickness of the silicon layer, whereas in a bulk technology charge generated up to several micrometers below the transistor can still be collected. Due to the reduced amount of collected charge in SOI processes (when compared to bulk), SOI has become a promising technology for use in environments where single event effects are of concern.

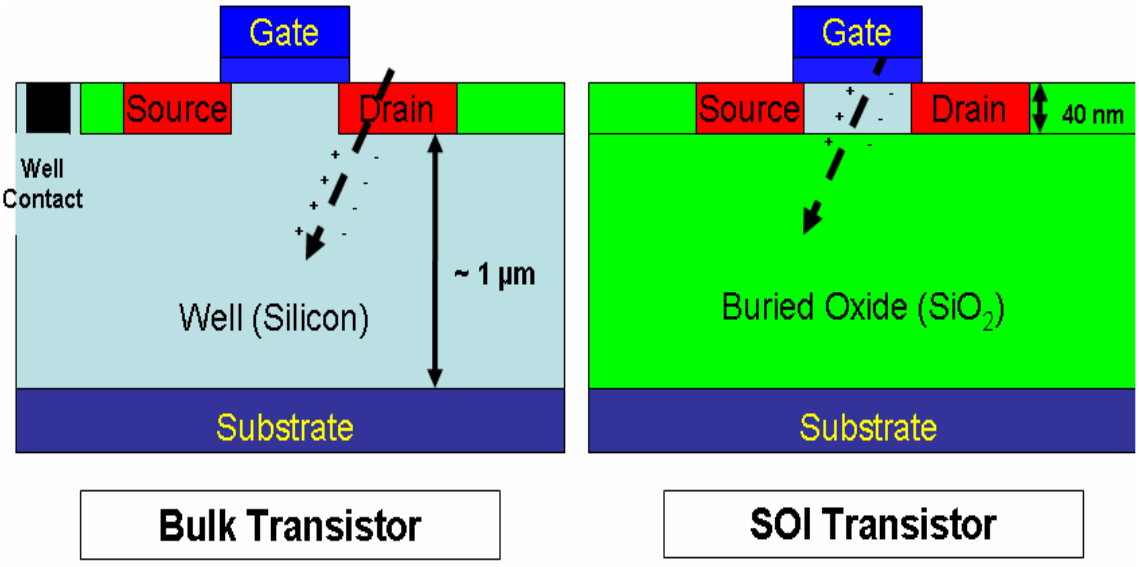

Fig. 2.4: Cross-section of a bulk and SOI transistor

An SOI technology can either be partially-depleted or fully-depleted. The simple difference between the two is that in a fully-depleted SOI (FDSOI) technology, the depletion region extends all the way to the buried oxide (BOX) of the device, while in a partially depleted SOI (PDSOI) technology the depletion layer does not extend all the

way to the BOX. Because of this, the thickness of the silicon layer in a FDSOI technology is typically thinner than the silicon layer of a PDSOI technology. Due to the thinner silicon layer and thus smaller volume available to collect charge, a FDSOI technology is often less susceptible to radiation effects than a PDSOI technology. One of the goals of this dissertation is to explore differences in SETs between bulk and FDSOI technologies.

Digital Single Event Transients

In a traditional digital circuit, two types of logic circuits can be defined: combinational logic and storage logic. Some examples of storage logic circuits include latches and flip-flops. In this type of circuit the error rate due to single events is almost independent of the clock frequency of the circuit. The latch or flip-flop's state can be flipped by an ionizing particle creating charge on a node regardless of the state of the clock signal at its input. Some examples of combinational logic circuits include NAND gates, XOR gates, and inverters. Single-event transients induced in the combinational logic circuits between storage cells can arrive at the input of the storage cell on the latching edge of the clock and be clocked in as erroneous data. Thus errors due to the combinational logic being hit by an ionizing particle depend on the clock frequency [Kaul-91, Reed-96, Buch-97]. The faster the clock, the more latching clock edges there are available to capture a transient signal.

The probability for a transient pulse to get latched as an incorrect data bit depends on its width [Baze-97, Mass-00]. Transient pulse propagation also depends on the state of the other combinational logic in its path. For example, if a transient pulse arrives at one

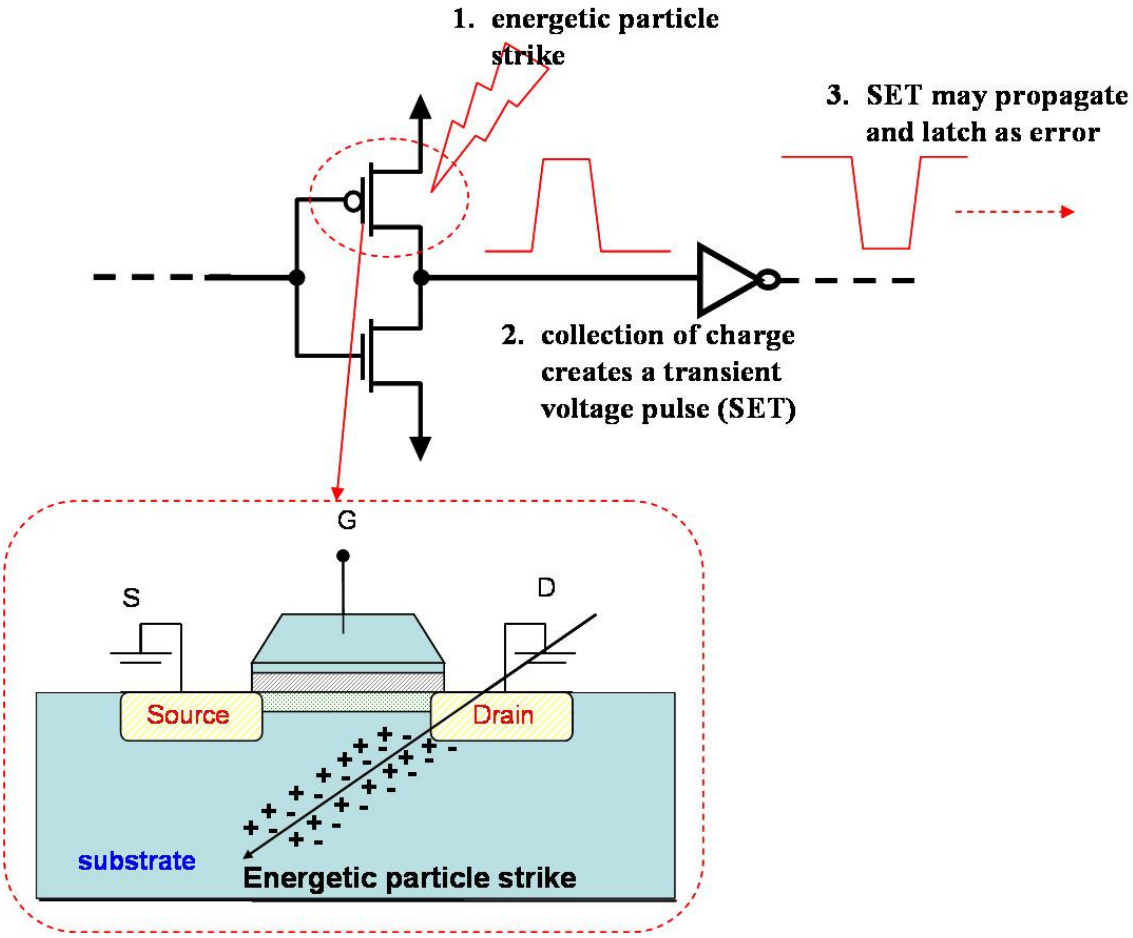

Fig. 2.5: Figure detailing how charge collected at a circuit node can create a transient signal that can propagate through a logic chain [Nara-08].

input of a NAND gate, but the other input of the NAND is at logic zero, then the transient pulse will not propagate through. Assuming the transient pulse propagates through the logic, the wider the pulse width, the greater the probability it has of arriving on the latching edge of the clock. If the transient pulse becomes longer than the time period of the clock, then every induced transient pulse will be latched. Fig. 2.6 illustrates how the width of an SET determines the probability of whether or not the SET will be latched. In this figure, the data will latch on the clock's falling edge. From the figure, one can see

how a wider SET width will lead to a greater probability of the SET arriving on the latching edge of a clock signal.

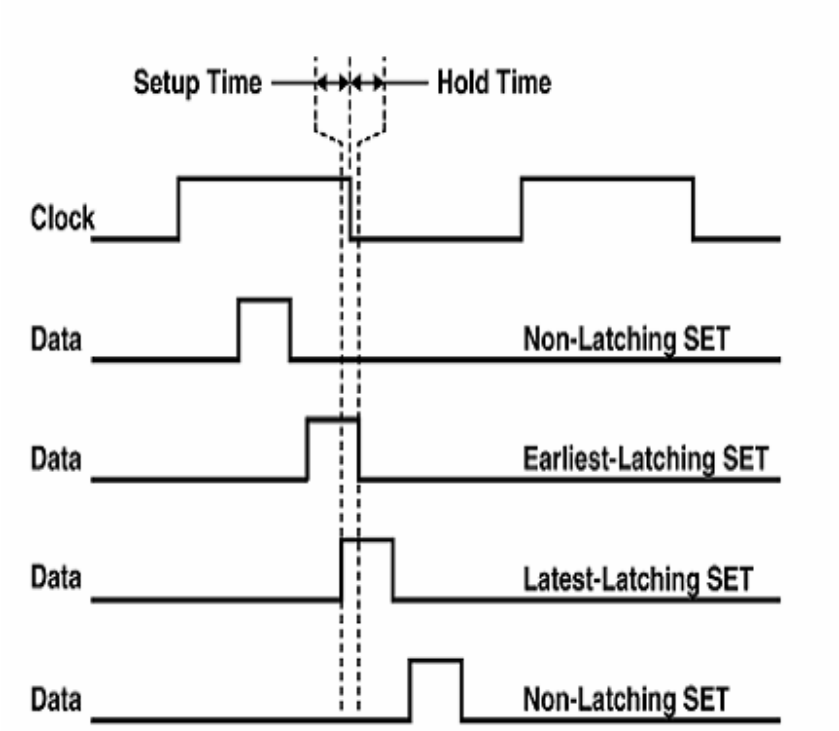

Fig. 2.6: SETs arriving at the latching edge of a clock can be recorded as incorrect bits [Mavi-02].

The impact of clock frequency and SET pulse widths on error rates is shown in Fig. 2.7. The data in the figure come from a test structure in which only the only errors came from SETs that arrived at the latching edge of a clock [Gadl-07]. In this figure, one can see that as the clock frequency is increased, the cross-section also increases. (The cross-section in this figure is the number of single events observed divided by the total fluence of particles.) Also in this figure, one can see that the lower operating voltages also increase the cross section. (The higher cross-section at the lower operating voltages can be attributed to an increase in SET width with decreasing voltage.)

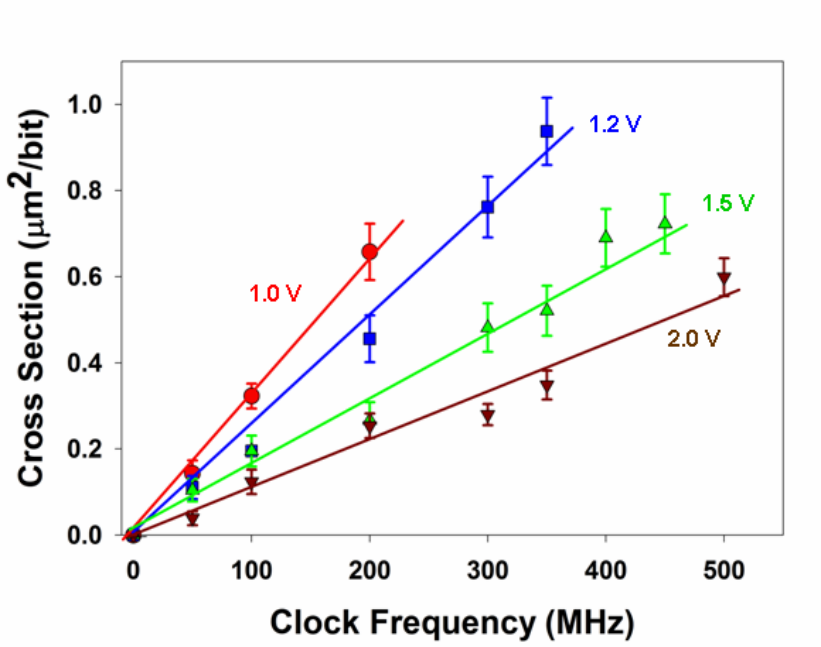

Fig. 2.7: Cross-section versus frequency for several different operating voltages [Gadl-07]

Single-Event Testing

To help quantify the effects of ionizing radiation in space on electronics, several facilities have been developed in the United States to perform single event testing [Buch-96, Duze-96]. In this work, four of these facilities will be discussed: (1) an 88' cyclotron at Lawrence Berkeley National Labs, (2) the Texas A&M University cyclotron, (3) a "microbeam" facility at Sandia National Labs, and (4) focused laser-based systems at the U.S. Naval Research Lab (NRL). (Note: these are not the only facilities available for single-event testing; a more complete list can be found in [Buch-96].) The Berkeley and Texas A&M facilities are both what are known as "broadbeam" facilities. Both of these cyclotrons are capable of accelerating ions of numerous atoms to energies ranging from 10 to 40 MeV per atomic mass unit (amu). To perform testing at these broadbeam facilities, electronic components are placed directly in the ion beam generated by the cyclotron. Single-event effects are monitored while the electronics-under-test are

operated. Typically at a heavy ion facility, one will record the data in terms of a "cross-section". A single-event cross-section from a "broadbeam" facility is usually defined as the number of errors (or single events) measured divided by the total fluence of particles.

Sandia National Laboratories' Ion Beams Materials Research Lab operates a tandem Van de Graaff accelerator which has several ion species. The Sandia "microbeam" facility is able to focus the ions to an area as small as a square micrometer. The focused lasers at NRL shrink a laser spot down to approximately one square micrometer [McMo-02]. Laser-induced carriers can be injected through the backside of a silicon die using a Two-Photon Absorption (TPA) technique or through the front of the device using a pulsed infrared laser [McMo-02]. An advantage of the TPA approach is its ability to interrogate SEE phenomena and circuit vulnerability through the wafer using backside irradiation, thereby eliminating interference from the metallization layer stack.

The key feature of using either the Sandia microbeam facility or the NRL laser based system is that one knows exactly where the single event occurs. The micrometer-sized laser spot or focused-ion beam can be maneuvered to strike various known locations in an electronic circuit. In a "broadbeam" such as at Berkeley or Texas A&M, the ion may strike any location of the device.

SET Measurements

As discussed previously, knowledge of SET pulse widths is crucial to determining the probability of an SET creating an error. Because of this, numerous researchers have attempted to experimentally measure digital SET pulse widths in deep submicron bulk technologies. Measuring SET pulse widths has been accomplished using several

techniques. SET pulses can be directly measured using high speed oscilloscopes [Ferl-06, Ferl-06-1, Pell-08]. However, such direct off-chip measurements are extremely difficult to perform because loading (and line) capacitances can significantly alter the SET shape. As a result, several on-chip SET measurements have been developed. Test structures developed by Baze et al. [Baze-06] and Eaton et al. [Eato-04] use a delay-based technique. The idea behind both techniques is that all transients shorter than a known delay will be filtered. Thus, once the delay becomes longer than the SET width, no SETs are measured. This provides an indirect way of measuring SET widths. In 2006, Narasimham et al. developed a technique that is able to directly measure digital SET pulses on-chip [Nara-06]. The Narasimham SET measurement technique will be used throughout this dissertation, and a complete description is given in this chapter.

Autonomous Pulse Capture and Measurement Structure

The autonomous SET measurement circuit characterizes SET pulse widths in units of inverter (or latch) delays. The idea behind the circuit is that as a transient signal propagates through a combinational logic chain, at any given time, the number of logic

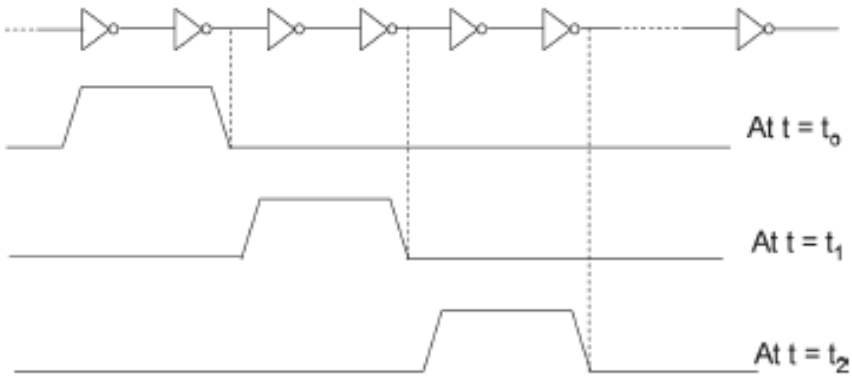

Fig. 2.8: Illustration detailing how an SET with a width of two inverters delays propagates through an inverter chain [Nara-06]

gates affected by the transient depends on its width. This is illustrated in Fig. 2.8. In this figure, an SET with a width of two inverter delays is shown. The autonomous SET measurement circuit effectively measures the number of inverters affected by a transient. If one knows the inverter delay, one can then determine the SET width that will be accurate to within ± one-half of the inverter delay.

To capture the number of inverters affected by an SET, a latch can be connected to the output of each inverter as shown in Fig. 2.9. As the SET travels through the inverter chain, the data in the latch corresponding to each inverter will change. However, once the SET propagates through, the inverter output, latch data will change back to their original states. One of the keys to making the SET measurement circuit work is the ability to capture and hold an SET.

To capture and hold a generated SET, the inverter stages in the measurement circuit can be created with pass and hold gates as shown in Fig. 2.10. The circuit shown in Fig 2.10 is self-triggering. When an SET generated in the target circuit arrives at the first stage, it continues to propagate through to the remaining stages and the delay. However,

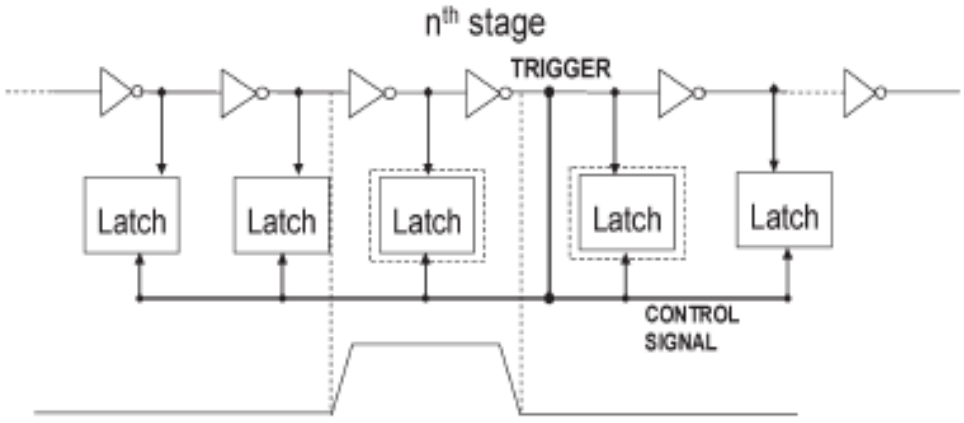

Fig. 2.9: An illustration of the technique used in the autonomous SET measurement circuit to capture pulse widths [Nara-06]

once the SET propagates through the delay, the S/R latch will change the value of the pass and hold signals. Once the pass and hold signals are set, the SET is essentially frozen in each stage. The output of each stage in Fig. 2.10 is connected to a latch (as shown in Fig. 2.10). The data stored in these latches represent the value of the SET width in units of stage delay. The outputs of these latches are connected to a parallel-in-serial-out shift register that enables one to get the SET pulse width data off the chip.

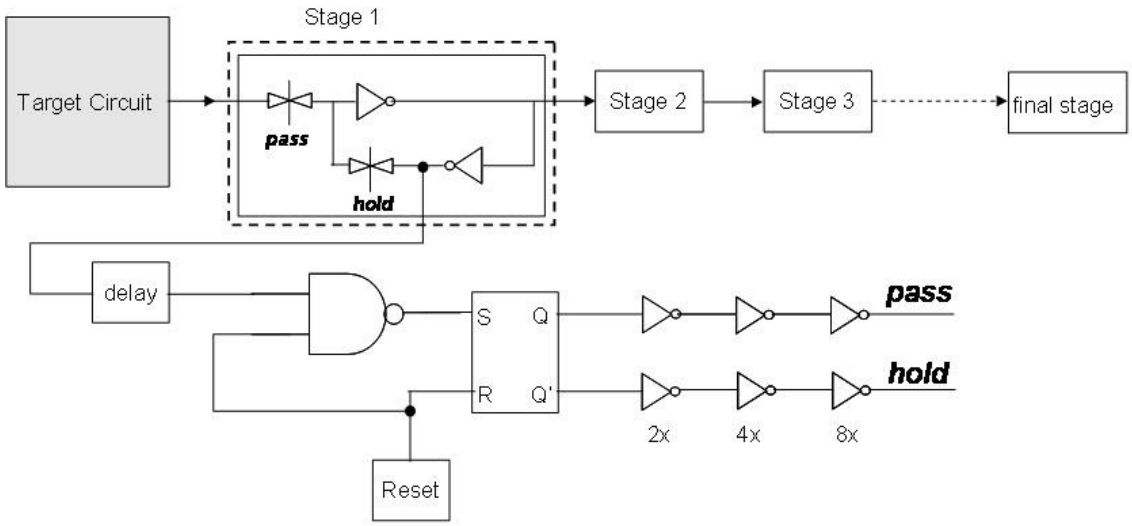

Fig. 2.10: Diagram of the complete self-triggering autonomous SET test structure with reset [Nara-06]

To determine the delay of each stage in the measurement circuit, a ring oscillator is created using the same latches as used in the measurement circuit. By determining the frequency of the ring oscillator one can determine the individual stage delay.

The target circuit used to "collect" SETs can be almost any combinational logic chain. For the results to be presented in this dissertation, a linear chain of 100 inverters was used as the target circuit in a 130-nm bulk technology, a chain of 1000 inverters was used for a 90-nm bulk technology, a chain of 200 inverters was used for a 180-nm fully-

depleted SOI technology, and a myriad of target circuits was used for a bulk 65-nm technology.

One minor issue with the autonomous SET measurement circuit is that it is unable to measure transients accurately that are shorter than a few latch stages. This issue has been reported in nearly every test structure that has utilized the autonomous SET measurement circuit [Nara-07, Nara-08, Gouk-08, Maki-09]. Narasimham attributed it to attenuation in the pulse capture latches and showed that for SETs greater than approximately three or four latch stages no attenuation occurred and the SET was measured correctly. The impact of this on the results presented in this dissertation is that if there are SETs generated smaller than three latch stages during testing, the measurement circuit will be unable to record them accurately.

CHAPTER III

SINGLE EVENT TRANSIENT PULSE WIDTH MEASUREMENTS IN DEEP SUBMICROMETER BULK TECHNOLOGIES

Introduction

As discussed in the previous chapter, knowledge of SET pulse widths is crucial to determining the probability of an SET creating an error. Because of this, a large amount of research has been performed measuring digital SET pulse widths in deep submicron bulk CMOS technologies. In this chapter, an overview of SET measurements and mechanisms that can affect those measurements in bulk technologies is given. In addition to giving a short review of previous measurements, SET measurement data will be presented from test structures fabricated in a bulk 65-nm technology. The data from these test structures are some of the first SET measurements ever performed in a 65-nm technology. Possible explanations for the differences in measured pulse widths between the technology nodes will be given. The data and analysis presented in this chapter will help set the foundation for the work dealing with SET width measurements over temperature that will be presented in Chapter V.

One item of key interest to the radiation effects community is knowledge of how SET pulse widths scale with technology. Since new technologies are only available approximately every two years, determining any trends with SET pulse widths has been a slow process. The maximum measured SET widths in several bulk technology nodes (all measured using the autonomous SET measurement circuit) are shown in Fig. 3.1. For each technology, the SETs were generated in a target circuit that consisted of a linear

chain of inverters. In this figure, one can see that significant differences in the maximum SET width between the technology nodes exist. However, no trend or even consistent results between the technology nodes is apparent.

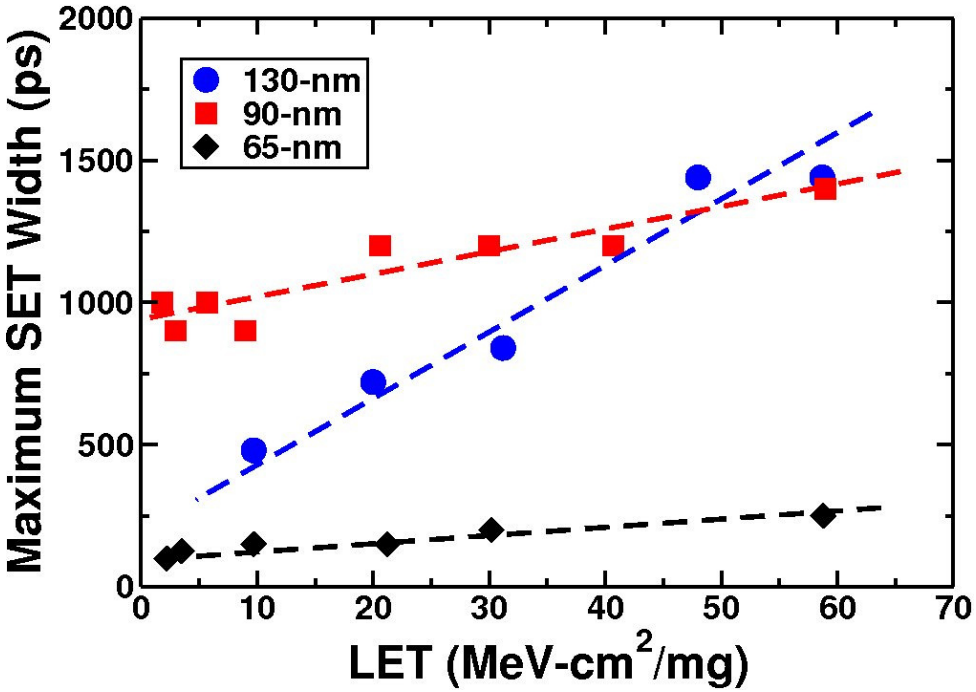

Fig. 3.1: Maximum SET widths measured in the 130-nm, 90-nm, and 65-nm test structures

Pulse Broadening in the 90-nm Test Structure

Perhaps the most glaring difference between the measurements shown in Fig. 3.1 is the long SET widths measured at small LET values in the 90-nm technology node. The long SETs measured at the small LET values are particularly troublesome since the smaller the LET value the higher the probability of seeing an event in space. A more in-depth look at the 90-nm results reveals the primary reason for the large SET widths at the small LET values.

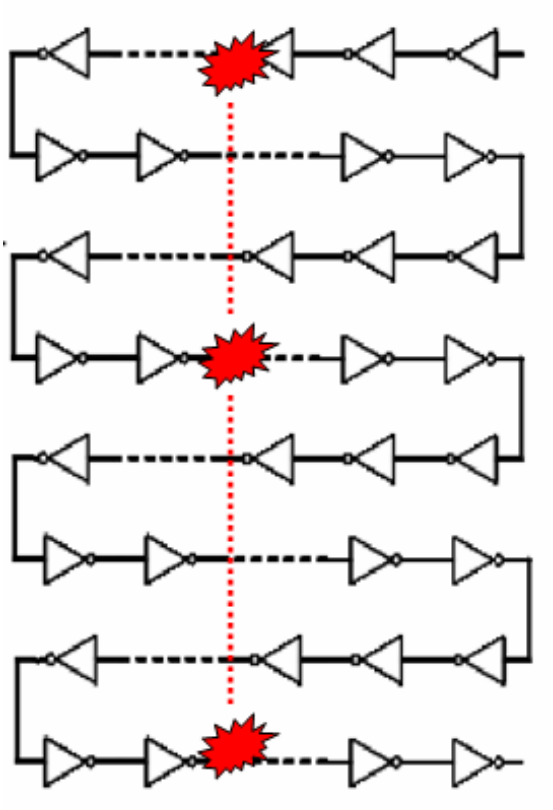

Fig. 3.2: Schematic of the 1000-inverter chain target circuit in the 90-nm test structure. The laser strike location was at the center of each row.

In the 130-nm circuit, the target circuit in which SETs are generated was a chain of 100 inverters. However, in the 90-nm circuit, the target was a chain of 1000 inverters. Recent work by Ferlet-Cavrois et al. [Ferl-07] and Massengill & Tuinenga [Mass-08] shows that transient signals can widen as they propagate through a combinational logic chain. A detailed description of the mechanisms behind this broadening effect is given by Massengill [Mass-08]. Obviously any broadening in the SET target circuit affects the SET measured by the measurement circuit.

To determine if the long SETs in the 90-nm circuit are due to pulse broadening, testing was performed using the two-photon focused laser at the Naval Research Lab [McMo-02]. The inverter chain in the 90-nm circuit consists of eight rows of 125

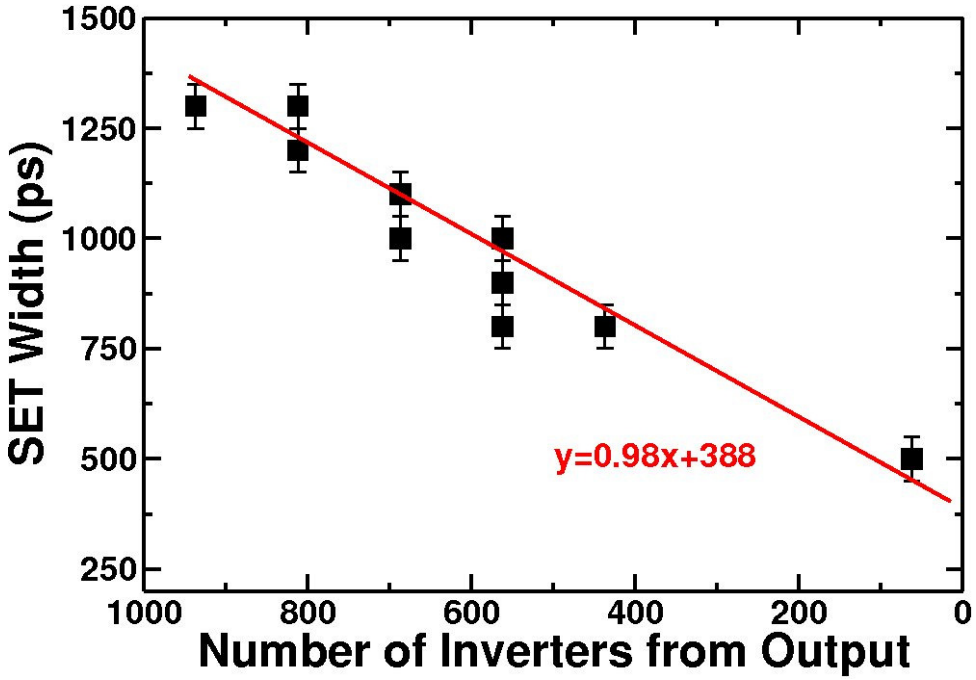

Fig. 3.3: Laser results from the 90-nm SET test structure. Using the same laser energy to strike different locations in the inverter chain shows that as the SET propagates through it widens at a rate of nearly 1 ps/inverter.

inverters. Using the same laser energy, SETs were measured for different strike locations in the center of each row in the inverter chain. The results are shown in Fig. 3.3. A fairly significant broadening effect is observed. The broadening rate was almost 1 ps/inverter. These results suggest that the large SET pulse widths observed at the small LETs for the 90-nm SET data are due to the layout of the target circuit.

The 130-nm test structure was also tested with the two-photon laser to look for pulse broadening. No pulse broadening was observed. If the broadening rate in the 130-nm circuit was the same as the 90-nm circuit (a reasonable assumption), the most any SET would be broadened in the 100-inverter chain would be 100 ps. 100 ps is on the order of the resolution of the measurement circuit for the 130-nm test structure.

Pulse Broadening in the 65-nm Test Structure

For the 65-nm SET pulse width measurements shown in Fig. 3.1, the target circuit also consisted of a linear chain of 1000-inverters (similar to the 90-nm test structures). To explore the impact of pulse broadening on the 65-nm SET measurements, an experiment was performed at the Sandia Microbeam Facility using 36 MeV oxygen ions with an LET of 5.4 MeV-cm^2/mg. The results of this experiment are shown in Fig. 3.4. In this plot, each point represents a location at which an SET was measured. The 1000 inverter chain target circuit was designed with 10 rows of 100 inverters. The first row of inverters is at the top of the figure and the inverter chain snakes around to the bottom row before it enters the measurement circuit. This plot clearly shows that SETs generated away from the measurement circuit are broadening as they propagate through the logic chain. Near the input the average measured SET is approximately 125 ps, and about halfway through the inverter chain the pulses become shorter than 75 ps. From these

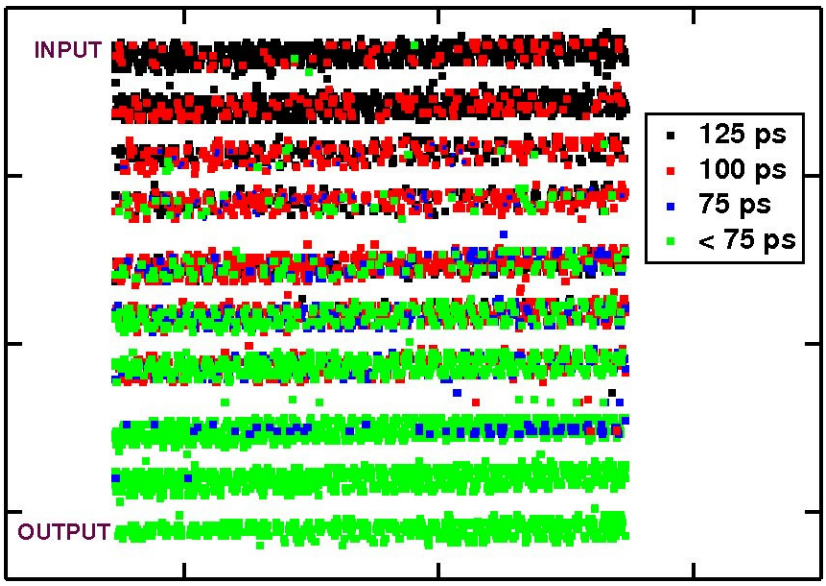

Fig. 3.4: SET measurements made on the 65-nm test structure at the microbeam facility

data, one can conclude that the broadening rate in this test structure is about 0.1 ps per inverter. This broadening rate is almost an order of magnitude less than that in the 90-nm test structure. The significance of this is that these results show that pulse broadening is not necessarily getting worse with technology scaling. The amount of pulse broadening depends on the circuit and layout design (not primarily the technology the circuit was designed in).

Not only can pulse broadening affect SET measurements, broadening can also impact the number of SETs measured. For example, in the 65-nm test structure an additional target circuit was designed with ten chains of 100 inverters "OR"-ed together to form a single output. Therefore, the average pulse broadening in this type of circuit should be about an order of magnitude less than in the linear 1000 inverter target chain circuit. In Fig. 3.5, the cross section to create an SET greater than 75 ps is plotted for the two different target circuits. The cross section is much smaller for the "OR"-ed circuit than

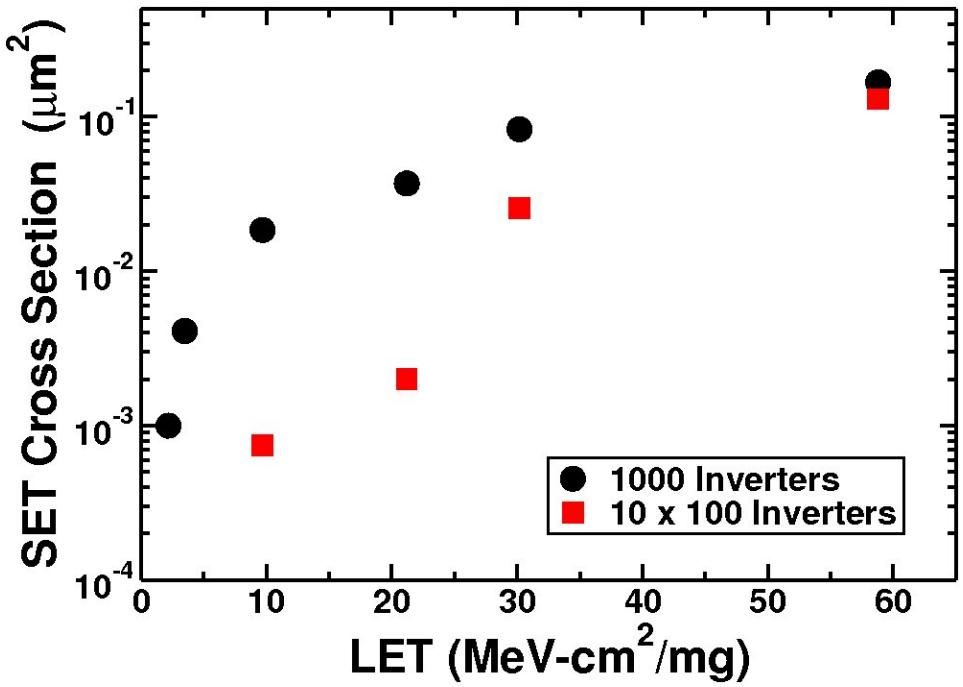

Fig. 3.5: SET cross-section comparison for the 1000-inverter chain target circuit and the 10x100 inverter chain target circuit.

for the 1000 inverter chain circuit even though the total sensitive area is approximately the same. The reason for this is that many of the smaller SETs generated in the 1000 inverter chain are able to broaden to a width greater than 75 ps whereas in the "OR"-ed circuit they are not.

With the broadening in the measurement circuits determined, one can now take a look at the generated SET widths. The generated pulse widths are the pulse widths that would be measured if there were no pulse broadening in the test structure. The generated SET widths are plotted in Fig. 3.6. By assuming that the maximum SETs measured in the 90-nm circuit were SETs that were generated near the input to the target circuit and had propagated through nearly 1000 inverters before they were measured, one can assume that by subtracting 1000 ps from the maximum SETs in Fig. 3.1 the generated SET width can be found. A similar analysis can be performed on the 65-nm results. The maximum generated SET width, as shown in Fig. 3.6, suggest that the pulse widths may actually be

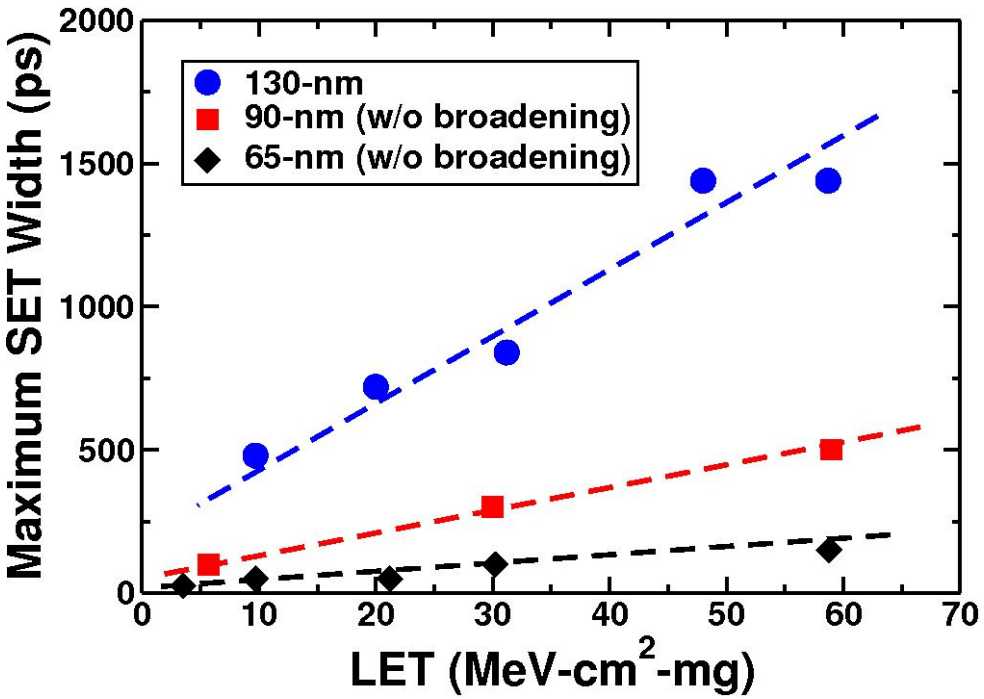

Fig. 3.6: Maximum generated SET pulse widths for the three test structures.

decreasing with technology node. However, in the next section, results will be presented that will show that this may not necessarily be the case.

Impact of the N-Well Contact on SET Widths

While the results presented in the previous section suggest that SET pulse widths will shrink with technology node, an observation of the mechanisms affecting charge generation and collection can give more insight into what to expect as feature size shrink. One of the predominant mechanisms causing long SET pulse widths in deep submicron bulk technologies is parasitic bipolar amplification. In any MOS structure, a parasitic bipolar transistor exists. An illustration of a parasitic PNP bipolar transistor in a PMOS device is shown in Fig. 3.7. When an energetic particle (heavy ion) strikes such a device, this bipolar transistor can turn on and lead to an enhancement in the charge collected. This increase in collected charge leads to an increase in SET width. Due to parasitic bipolar amplification, larger SET pulse widths are observed in pMOS devices than in nMOS devices. Parasitic bipolar amplification is more pronounced for a pMOS device in

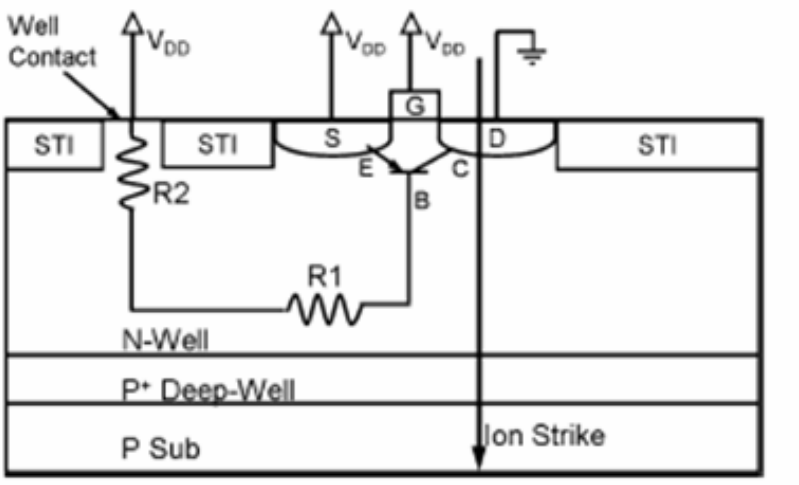

Fig. 3.7: Illustration of a parasitic bipolar transistor in a pMOS device [Olso-07]

an n-well with a p-substrate for a bulk, twin-well CMOS process like the ones that are studied in this work.

Amusan et al. [Amus-07] showed that the parasitic bipolar effect and the SET pulse width depend significantly on the well contact size and spacing. Amusan's results are shown in Fig. 3.8. As can be seen, SET pulse widths can be altered significantly by adjusting the well contact size. Amusan's simulations show that the maximum SET width can vary by up to 1 ns for the same technology just due to differences in the n-well contact size. These results are important because they suggest that SET measurements can depend more on the layout of the transistors than the technology node (or the minimum feature size at a technology node).

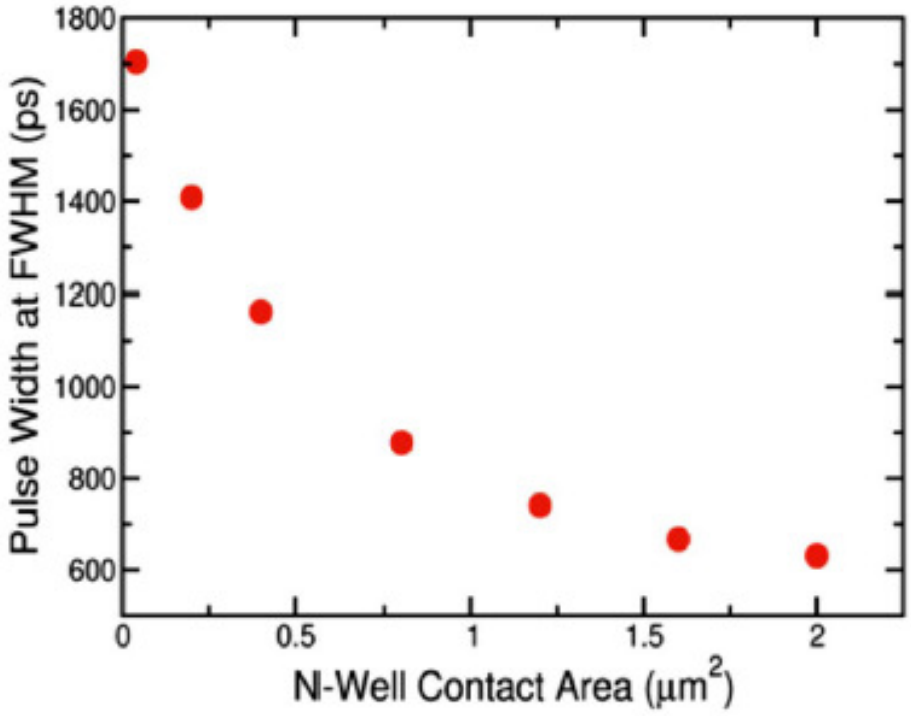

Fig. 3.8: Simulation Results by Amusan et al. showing how the well contact size can affect SET pulse widths [Amus-07].

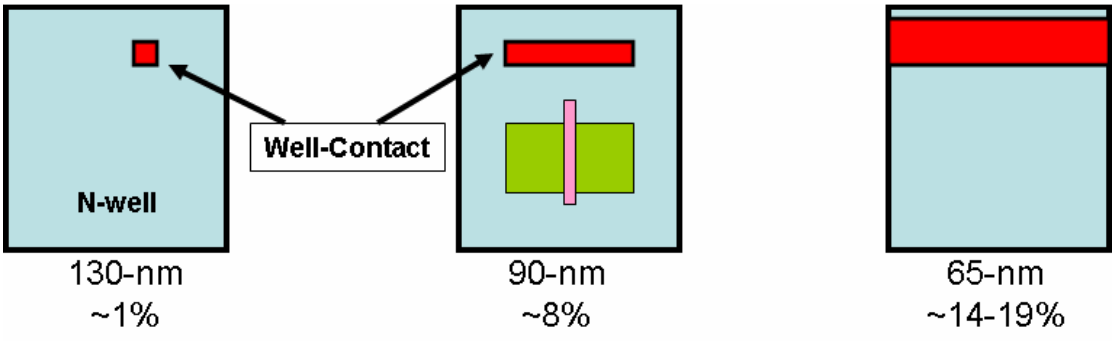

Fig. 3.9: Illustration of the well contacting scheme used for each of the test structures.

The results of Amusan et al. suggest that perhaps the smaller SET widths with the shrinking technology nodes may have little to do with the technology node itself but rather may be a function of how the n-well is contacted in the test structure. To further look into this, the well contact area for each of the test structures was measured and normalized to the total N-well area. In Fig. 3.9, an image of the well-contacting scheme for each test structure is shown. For each newer technology, the n-well was better

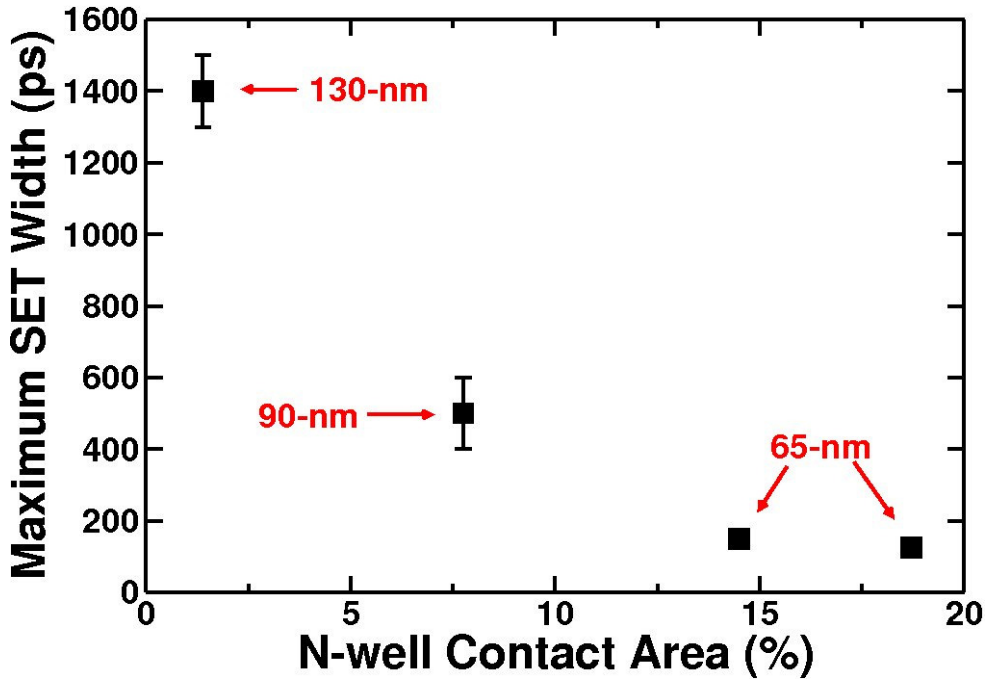

Fig. 3.10: Maximum SET widths plotted as a function of n-well contact area percentage.

contacted as seen by the ratio of the well-contact area to the total well area. In fact, if we plot the maximum SET width versus the contact area percentage, a plot (shown in Fig. 3.10) with a remarkable similarity to the one presented by Amusan et al. in Fig. 3.8 is found. The point of this analysis is to show that the smaller pulse widths measured with the newer technologies may not be related to the technology but rather may simply be a function of how the n-well is contacted. This well-contacting issue and its impact on the parasitic bipolar action will be discussed in the final chapter.

Transistor-to-Transistor Spacing

As feature sizes have scaled and the spacing between transistors has shrunk, a new mechanism has started to affect SET pulse widths. A mechanism known as "pulse quenching" [Ahlb-09] can occur when more than one device is able to collect charge. The end result of this mechanism is that the resulting pulse width ends up being shorter when two electrically-related transistors collect charge than when only a single transistor collects charge. To explore this mechanism at the 65-nm technology node, two test circuits were developed. In the first circuit, an inverter chain was designed with each inverter spaced 0.75 µm apart and with each pMOS transistor placed in the same n-well. The second circuit consisted of a schematically-identical inverter chain, but in this circuit the inverters were spaced 1.3 µm apart and each PMOS transistor was placed in its own n-well. The spacings, 0.75 µm and 1.3 µm, represent the minimum spacing for each configuration as allowed by the design rules of the technology. An illustration detailing the layout of the two inverter chains is shown in Figs. 3.11 and 3.12.

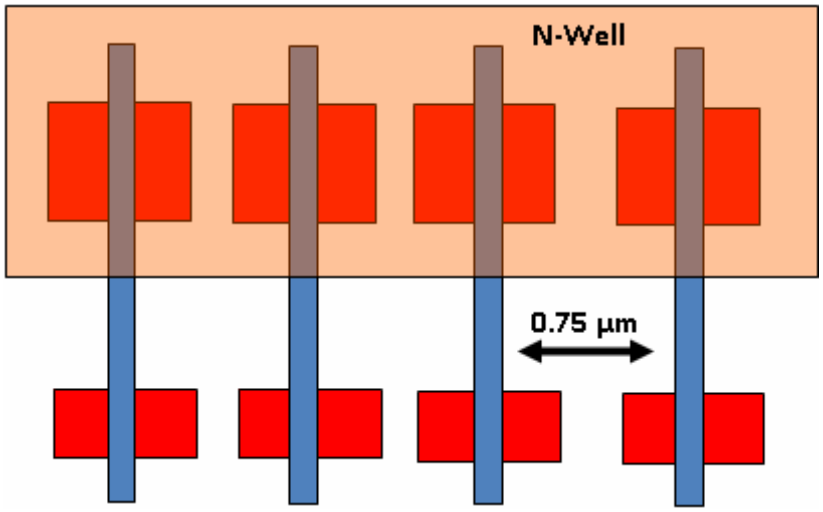

Fig. 3.11: Illustration of the layout of the same well inverter chain target circuit.

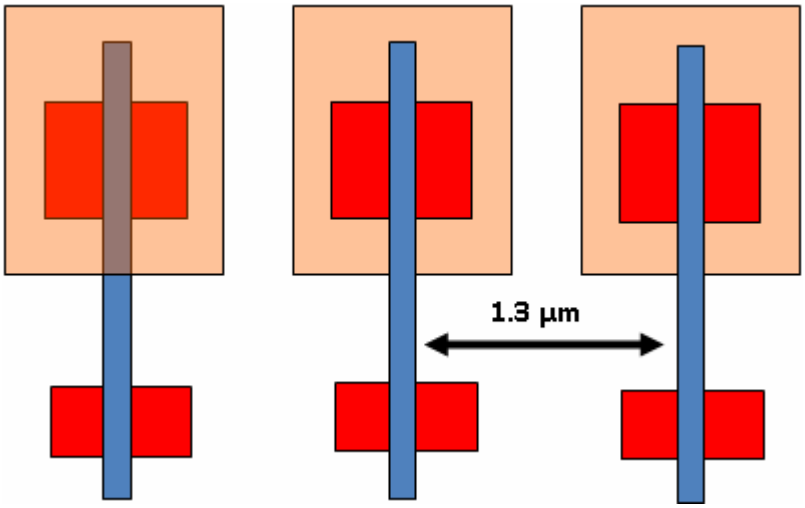

Fig. 3.12: Illustration of the layout of the separate well inverter chain target circuit.

The differences in measured pulse widths and SET cross section between the two circuits are dramatic. The average measured SET width versus LET is plotted in Fig. 3.13. The average SET width is approximately 40% shorter for the circuit with the closer transistor spacing. Perhaps even more significant than the shorter average width is the

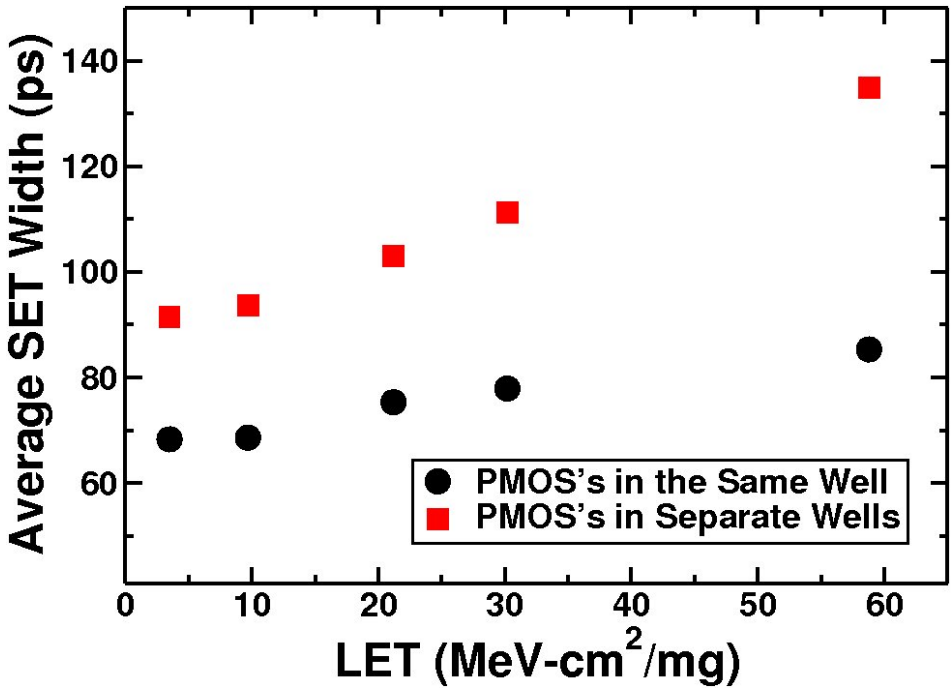

Fig. 3.13: Average measured SET width versus LET for the separate well and same well test 65-nm test structures.

smaller number of SETs observed with the same well circuit. In Fig. 3.14 a histogram of the measured SET widths for an LET of 60 MeV-cm^2/mg is shown. Not only are the SETs shorter in the same well circuit, but the number of SETs measured was about a factor of eight less.

To explore the differences in these two target circuits further, the Sandia Microbeam Facility was used. In Figs. 3.15 and 3.16, SET maps are shown for each of the circuits. In these figures each black dot represents a location of an observed SET event, and the tick marks are one micrometer apart. First, in the separate well circuit shown in Fig. 3.15, the error map clearly shows the location of each pMOS and nMOS transistor in the inverter chain. (Remember from Chapter II that only "off" devices with a reverse-biased drain are able to collect charge and create an SET.) However, as shown in the figure, the

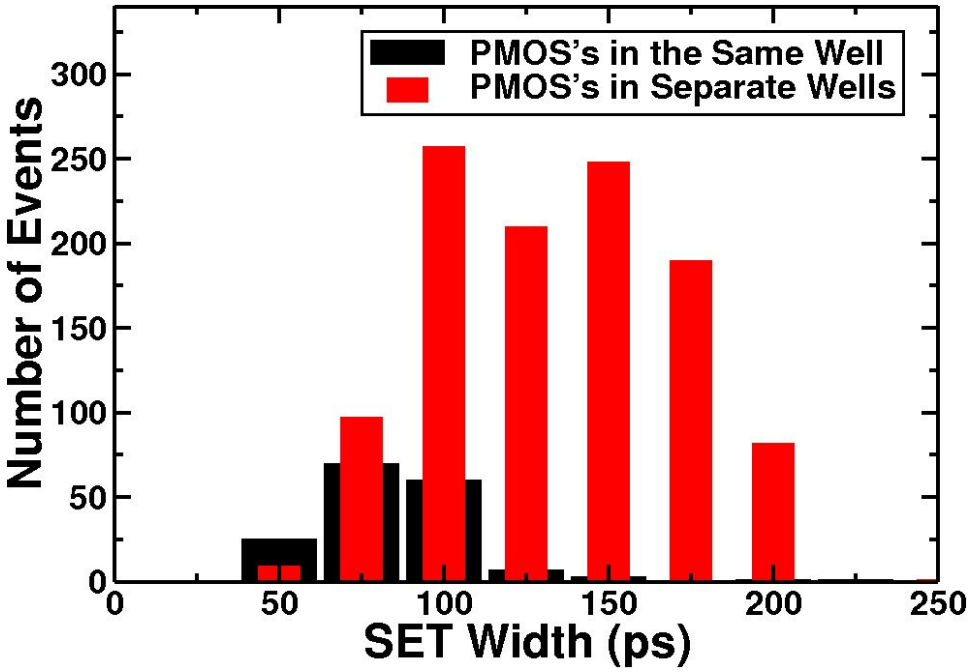

Fig. 3.14: Histogram of the measured SETs for the two 65-nm structures for an LET of 60 MeV-cm^2/mg.

area around each transistor that is able to collect charge is much larger than either the reverse-biased drain or the entire n-well. Amusan et al. [Amus-08] have shown that charge collection can take place as far away as two micrometers from the sensitive volume for large LET values (> 40 MeV-cm^2/mg). The microbeam results from the separate well circuit show charge collection about one micrometer away from the sensitive volume for a small LET value (~ 5 MeV-cm^2/mg).

The error map for the same well circuit is shown in Fig. 3.16. The X-Y scale in this figure is the same as in Fig. 3.15. In the same well circuit where each transistor is spaced only 0.75 µm apart, differences between the nMOS and pMOS devices are almost indistinguishable. These results help illustrate the fact that as feature sizes shrink and the

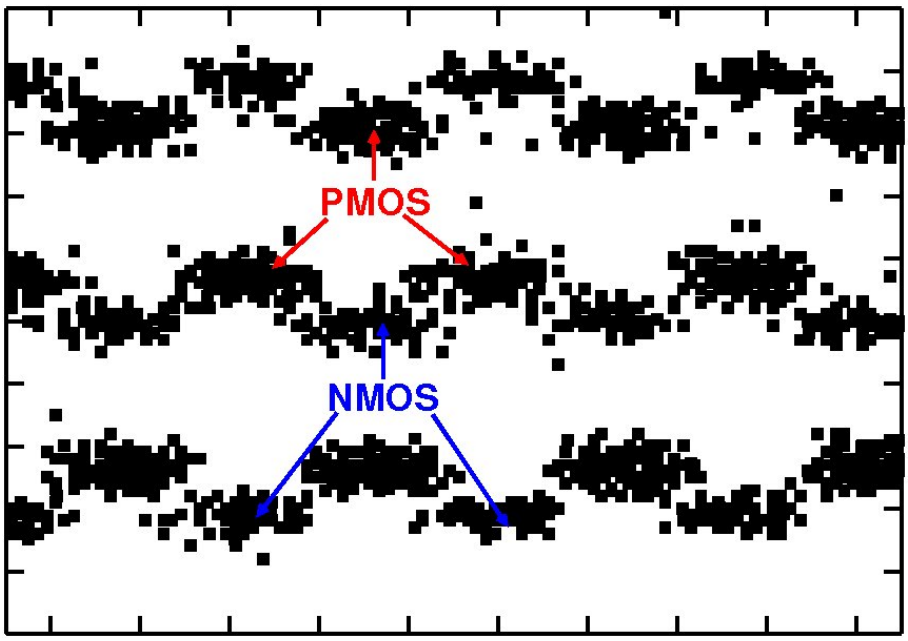

Fig. 3.15: SET error map of the separate well target circuit taken at the microbeam facility

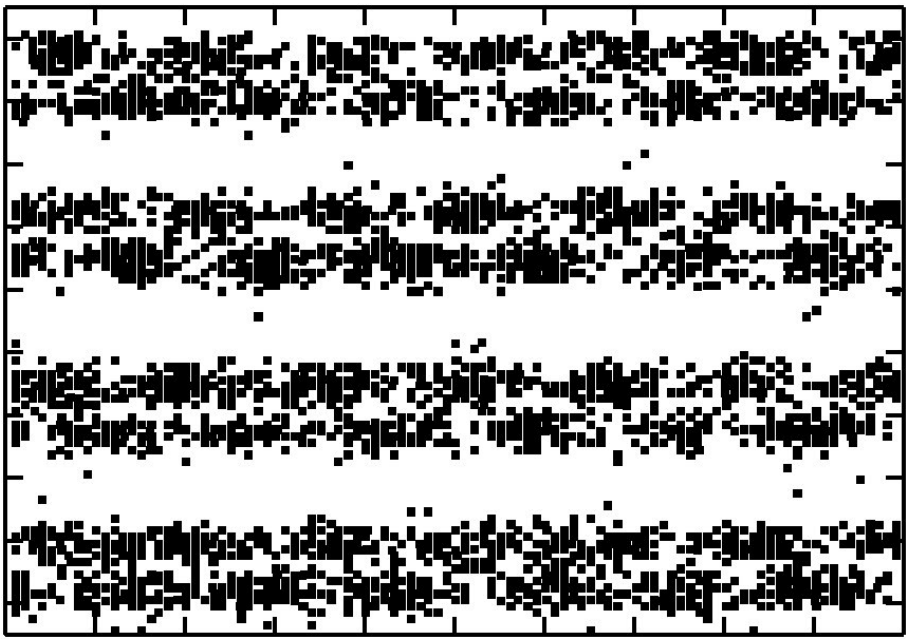

Fig. 3.16: SET error map of the same well target circuit taken at the microbeam facility.

transistors become closer spaced, one will no longer be able to view SETs in terms of a single device collecting charge and creating a transient, but rather as multiple devices

collecting charge and creating a transient. In devices such as SRAMs or DICE latches [Olso-05, Amus-08] where multiple-device charge collection leads to an increase in single event susceptibility, multiple device charge collection has the potential to reduce SET vulnerability.

Another interesting phenomenon that starts to appear as device spacing shrinks is the occurrence of multiple SETs from a single ion strike. During single event testing of the separate well target circuit, multiple SET events were observed at an incident angle of 60^{o}. (Interestingly, no multiple SET events were recorded for the same well target circuit.) Examples of some of the measured multiple SET events are shown in Fig. 3.17. This is the first time multiple SET events have ever been reported. The cross-section for multiple SETs is compared to the single SET cross-section in Fig. 3.18. At an incident angle of 60^{o}, the cross-section for multiple SETs is significantly smaller than single SET events. However, in a space environment where ions can strike a device from all

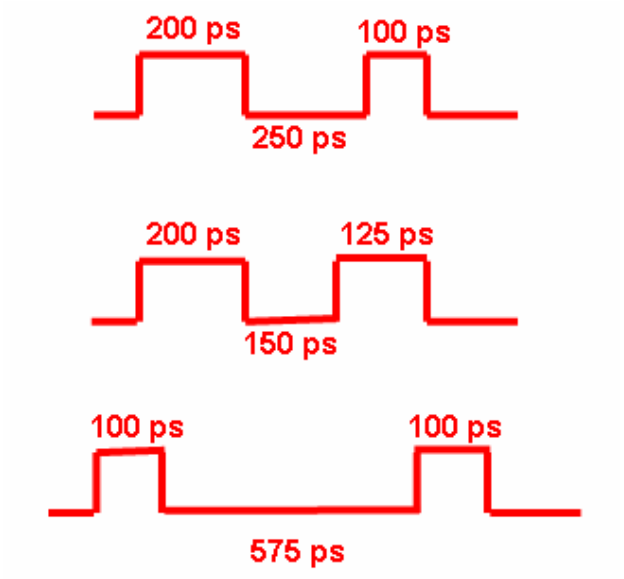

Fig. 3.17: Examples of some of the multiple SET events measured during heavy ion testing of the separate well circuit.

directions, multiple SETs may make up a significant portion of all SET events. Multiple SETs introduce an interesting dilemma for hardening since most SET hardening techniques use delay-based methods.

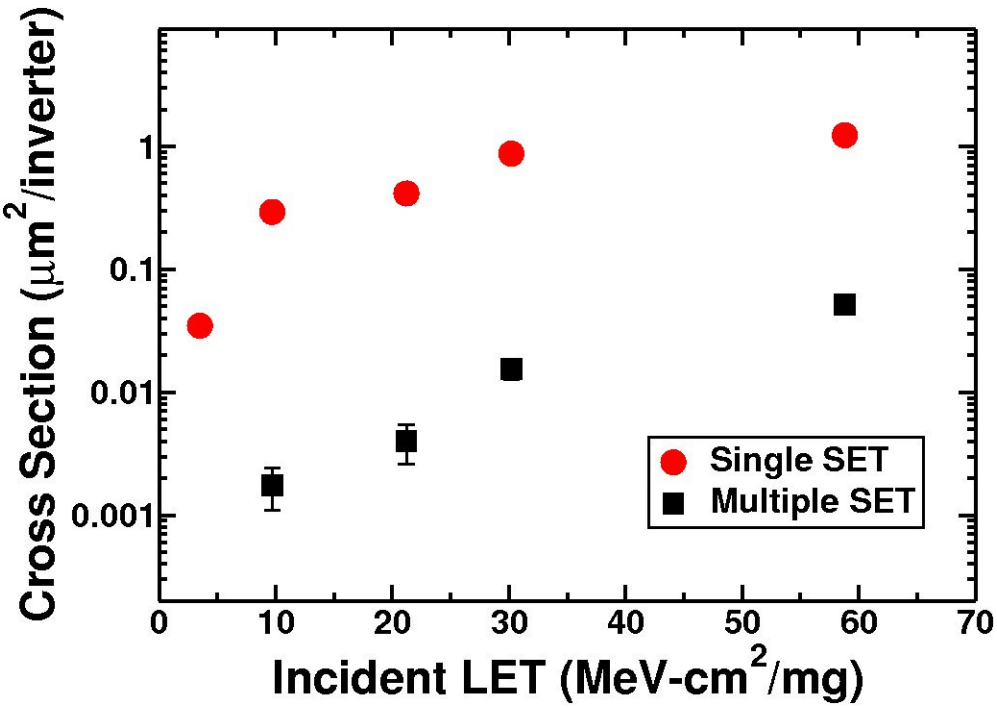

Fig. 3.18: Comparison of the multiple SET cross-section to the single SET cross-section for the separate well target circuit.

Conclusions

In this chapter, SET pulse widths in bulk technologies have been discussed. Three factors that can affect SET measurements were introduced: pulse broadening, parasitic bipolar amplification (which was shown to depend primarily on the n-well contact area), and transistor-to-transistor spacing. All of these factors were shown to combine to make scaling trends in SET pulse widths difficult to determine. Pulse broadening and parasitic bipolar amplification are especially important mechanisms that are considered in the rest of this dissertation. The pulse broadening effect is an important issue for floating body

SOI technologies (Chapter IV), and the parasitic bipolar effect becomes a significant issue as the temperature is increased (Chapter V).

CHAPTER IV

SINGLE-EVENT TRANSIENTS IN A 180-NM FULLY-DEPLETED SOI TECHNOLOGY

Introduction

As discussed in Chapter II, silicon-on-insulator (SOI) technologies present inherent advantages over bulk technologies when dealing with single-event effects. Previous work has shown that single-event transient pulse widths are significantly shorter in SOI technologies when compared to similar bulk technologies [Ferl-06]. In this chapter, SET pulse widths in a unique 180-nm fully-depleted SOI technology are examined. The results presented in this chapter are vital to understanding how temperature affects SET pulses in this technology (which are discussed in Chapter V).

One well-known issue for floating-body SOI devices is "pulse broadening" or "pulse stretching" [Ferl-07, Mass-08]. As illustrated in the previous chapter, this phenomenon may significantly increase SET pulse widths as the SET propagates through a circuit. Laser-induced SET results on test structures from the 180-nm fully-depleted SOI technology to be discussed in this chapter have been presented by Gouker et al. [Gouk-08]. Gouker et al.'s results have shown that for a circuit without body contacts, SET pulses can broaden at a rate of nearly 4 ps per inverter as they propagate through the circuit. (The body of an SOI transistor is simply the area under the gate and can either be floating or tied to a given potential with a body contact. In this chapter, both cases are discussed thoroughly.) Gouker et al. attributed the pulse widening to the floating body of

the transistors, and body contacts were shown to mitigate this effect. In this chapter, heavy ion-induced single-event transient pulse widths are experimentally measured in a 180-nm fully-depleted SOI process for devices with and without body contacts for the first time. Results clearly show a reduction in SET pulse widths and the number of measured SET pulses for the devices with body-contacts. TCAD (Technology Computer Aided Design) simulations are used to explain these experimental results. Additionally, the SET cross section of the fully-depleted SOI process with and without body-contacts is compared to the SET cross section of a bulk process.

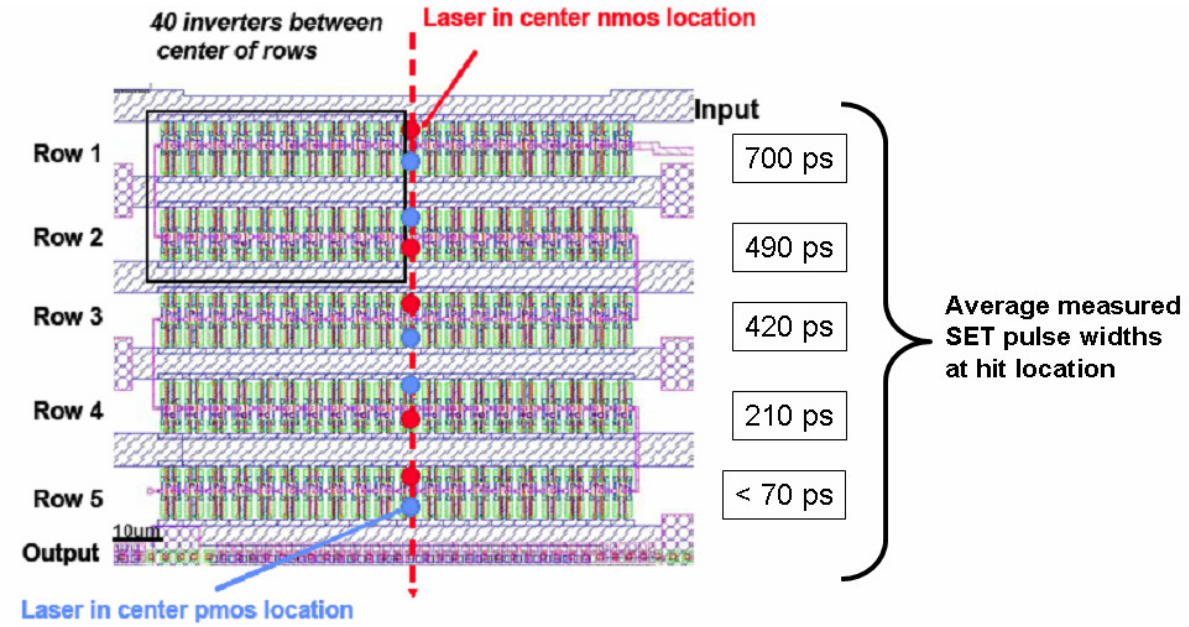

Fig. 4.1: Average measured SET widths for various strike locations in the inverter chain target circuit for the floating-body FDSOI test structure.

180-nm FDSOI Test Chip Description

The test circuits used to characterize the SET pulses were fabricated in a 180-nm FDSOI CMOS technology [Gouk-08] from MIT Lincoln Laboratory using the autonomous SET measurement technique discussed in Chapter II. The design consists of

a linear chain of 200 minimum-drive-strength inverters (the target circuit in which the SETs are generated) that terminates in the SET measurement circuit that records the occurrence of an SET and the pulse-width of the corresponding SET. The measurement circuit uses 25 inverter stages along with latches to store the number of inverters affected by each SET. With the individual latch stage delay of about 70 ps, this circuit allows measurement of SET pulses ranging from 70 ps to over 1 ns with a 35 ps measurement resolution [Gouk-08]. The test chips used in this work consisted of two target circuits. The first target circuit consisted of transistors in the inverter chain (target circuit) with source-body contacts. The second circuit was identical but the transistors did not have body contacts. In this technology, the silicon layer thickness is 40 nm. For comparison, in IBM's 65-nm partially-depleted SOI process, the SOI thickness is 60 nm [Rodb-07].

Heavy Ion Test Results

Heavy ion testing on SET test structures was performed using the 4.5 MeV/amu cocktail at Lawrence Berkeley National Labs using ions with LET values ranging from 7 to 100 MeV-cm^2/mg. Histograms of the pulse width distributions for the test structures with and without body-contacts for four different ions are shown in Figs. 4.2-4.5. As expected, the SET pulse widths show a wide distribution, similar to what has been observed in bulk technologies [Nara-07, Nara-08-1]. The data clearly show the presence of SET pulses longer than 1 ns for particles with an LET of 40 MeV-cm^2/mg in the floating body test circuit. For the circuit with the source-body contacts, very few transients with SET widths greater than 70 ps were measured. The longer pulse widths in the circuit with a floating body may be attributed to "pulse-broadening".

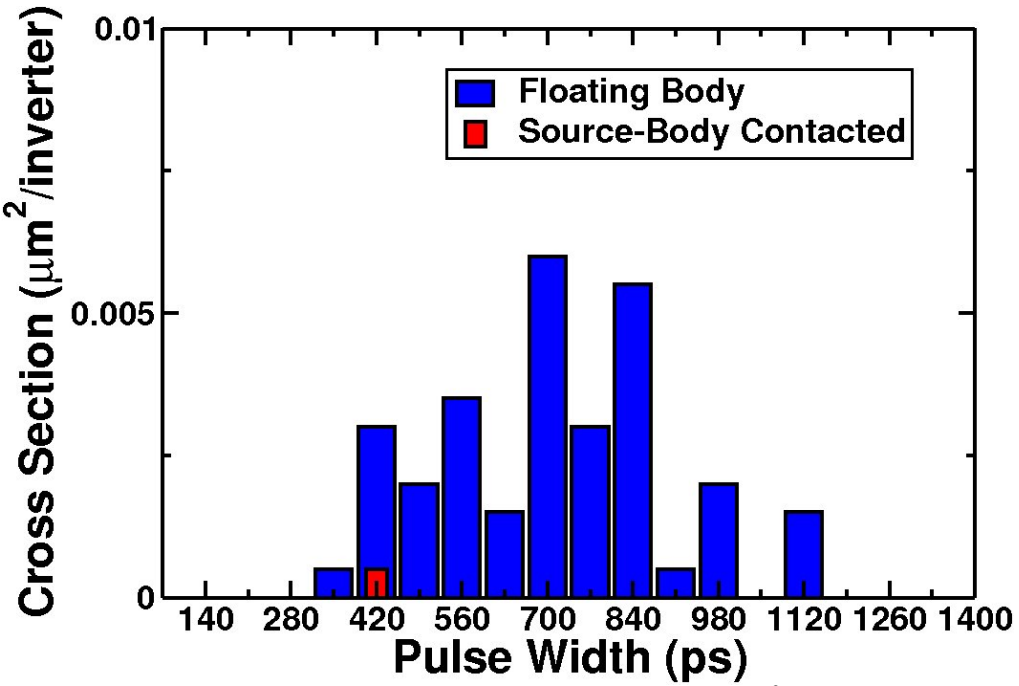

Fig. 4.2: SET pulse width distributions for argon (LET = 14 MeV-cm^2/mg, Fluence = 1x10^9 particles/cm^2). Note that not only are the pulse widths shorter for the circuit with source-body contacts, the total the number of counts is also significantly less.

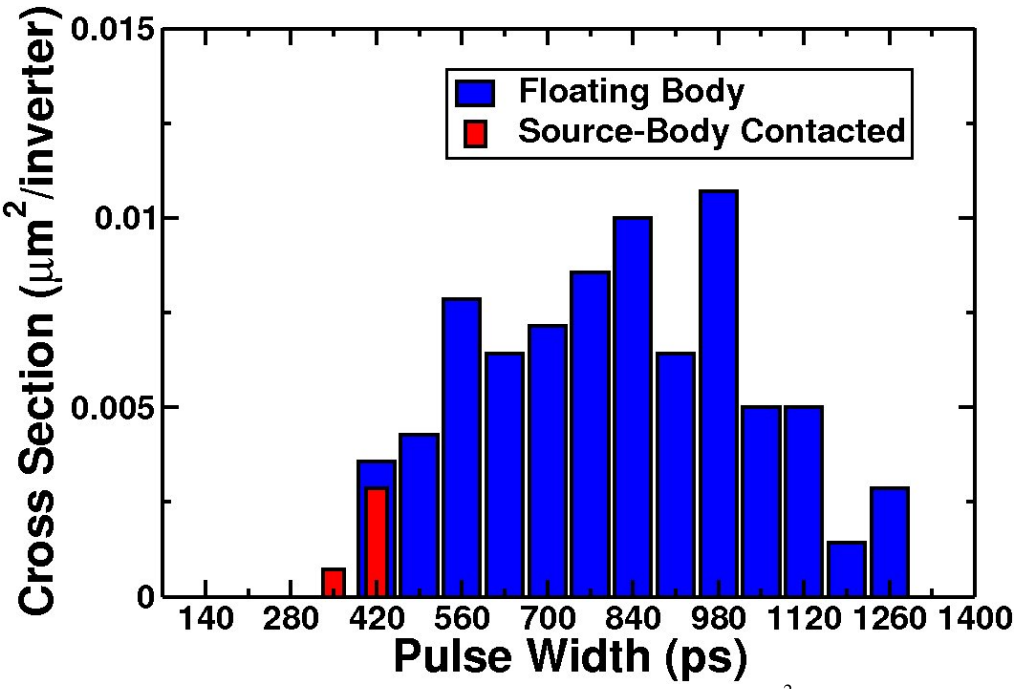

Fig. 4.3: SET pulse width distributions for krypton (LET = 40 MeV-cm^2/mg, Fluence = 7x10^8 particles/cm^2).

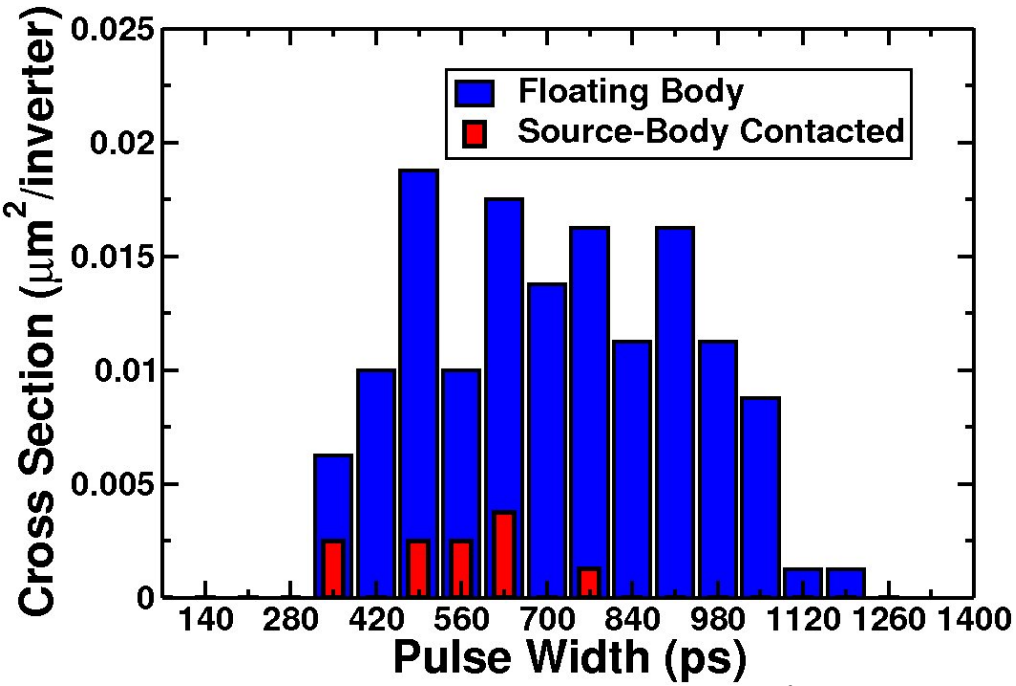

Fig. 4.4: SET pulse width distributions for xenon (LET = 69 MeV-cm^2/mg, Fluence = 4x10^8 particles/cm^2).

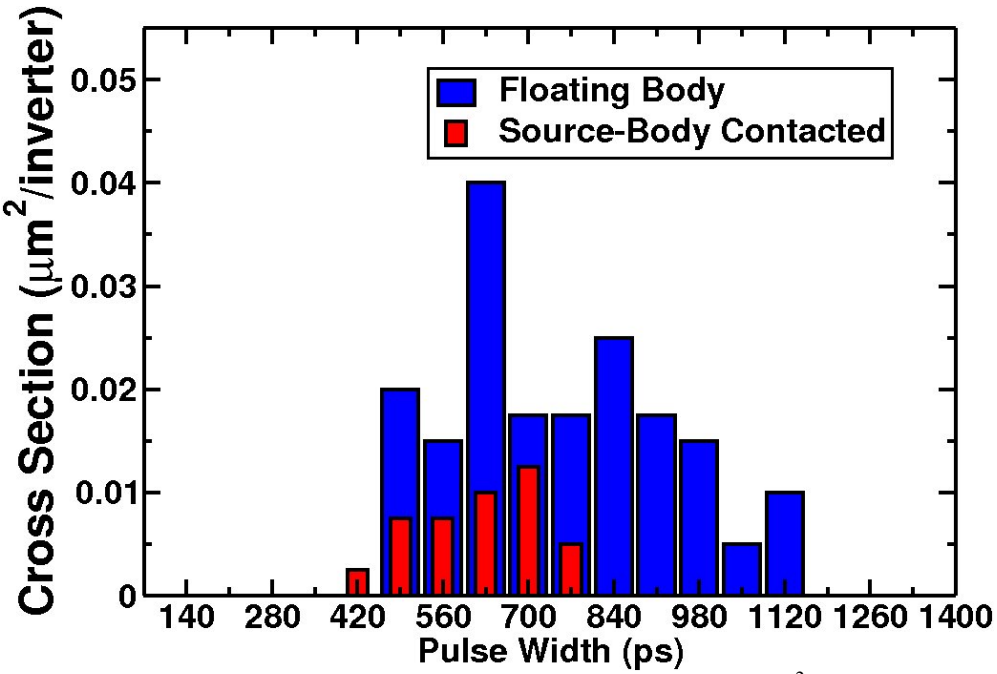

Fig. 4.5: SET pulse width distributions for bismuth (LET = 100 MeV-cm^2/mg, Fluence = 2x10^8 particles/cm^2).

To clarify the data shown in Figs. 4.2-4.5, the average measured pulse widths are plotted versus LET for both circuits in Fig 4.6. The average SET pulse width increases with LET for the source-body contacted circuit, but remains relatively constant for the floating-body circuit. This is due to the fact that for the floating-body circuit almost all of the measured SETs will have broadened from their initial width. As a result, the average measured SET width for the floating-body circuits is not an average of the generated SET width, but rather an average of the generated plus broadened SET width. In other words, the average SET width has been skewed by the broadening.

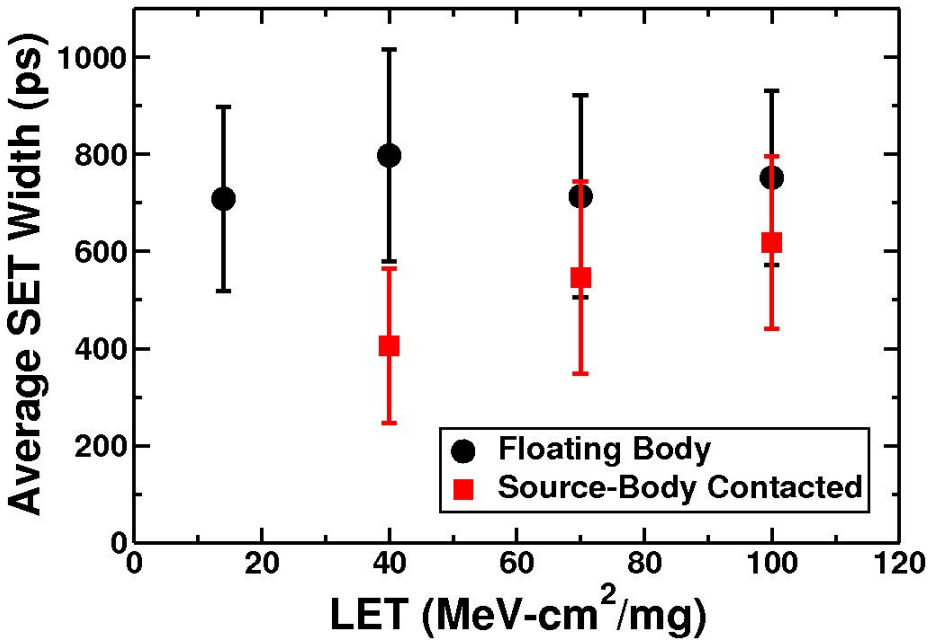

Fig. 4.6: Average SET pulse widths experimentally measured for the two target circuits. The error bars represent one standard deviation from the average.

Extracting SET Pulse Widths from the Floating Body Circuit

Since the SET pulse width broadening rate for the non body-contacted circuit is known, an attempt was made to determine the SET pulse width distribution in the absence of pulse broadening. By doing such an analysis, an approximation of the original

(non-broadened) SET distribution can be obtained. With a known broadening rate of approximately 4 ps per inverter, a generated SET of 280 ps may be measured as anywhere from 280 to 1080 ps wide, depending on where in the 200 inverter chain it was generated.

To perform this analysis, one first needs to create a reasonable distribution for the non-broadened SET pulse widths (shown as the blue curve in Fig. 4.7). By convolving the 4 ps increase per inverter stage with the possible non-broadened distribution, a likely-measured distribution can be obtained. The likely-measured distribution can then be compared to the real measured distribution. If the calculated likely distribution does not match the experimental results, new non-broadened distributions can be created until a close approximation of the measured distribution is found.

To further explain the broadening analysis, let there be 100 SETs generated in the target circuit with a width of 280 ps. The actual measured width of these SETs depends on where in the inverter chain the SET is generated. With a 4 ps per inverter broadening rate and a 200 inverter chain, these 280 ps randomly-generated SETs have a uniformly distributed probability of being measured anywhere from 280 ps to 1280 ps. Therefore each of the 14 bins between 280 ps to 1280 ps in the "With Broadening" histogram (shown in Fig. 4.7) would have approximately 7 events from the 100 events generated at 280 ps. By performing this same analysis on each bin in the "Without Broadening" histogram, the "With Broadening" histogram can be created. The "With Broadening" histogram can then be assumed to be the likely measured distribution for the original generated SETs.

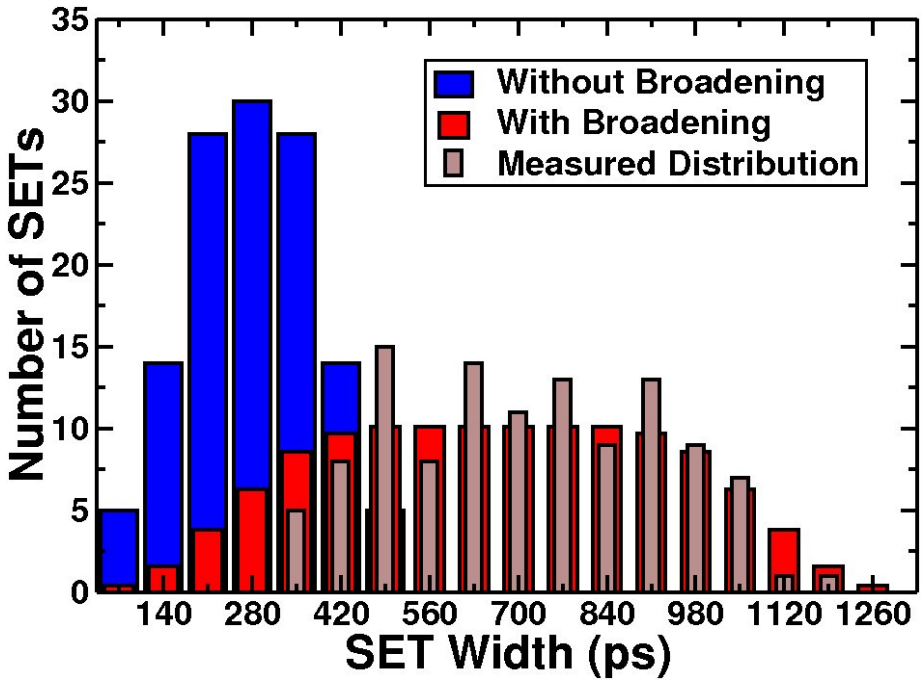

Fig. 4.7: Plots of a possible original distribution of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events.

Fig. 4.7 shows plots of a possible original distribution of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events. The average SET pulse width for the distribution without broadening is 280 ps. This average non-broadening SET width compares well with the average found during heavy ion testing for the source-body contacted circuit. This suggests that the generated SET pulse widths for the body-contacted and floating-body circuits are approximately the same.

The broadening analysis presented here can be performed on any SET measurement circuit with a large number of inverters where pulse broadening may be an issue. To separate the radiation effect (i.e., the SET pulse width at the node struck by an ion) from the circuit effect (the pulse broadening occurring before the SET measurement takes place), an analysis like the one in Fig. 4.7 must be performed. However, in order to

perform this analysis, the broadening rate first has to be determined. As mentioned in the previous chapter, the broadening rate can be determined through either pulsed-laser testing or using a focused-ion beam. In the next chapter, this same broadening analysis is performed on the 90-nm bulk SET measurements to determine the change in generated SET widths with temperature.

Mixed-Mode Simulations

Mixed mode simulations were performed using TCAD and SPICE models calibrated to measurements made on transistors fabricated in this 180-nm FDSOI technology. Measured I-V curves for the transistors are compared to the simulated I-V curves in Fig.

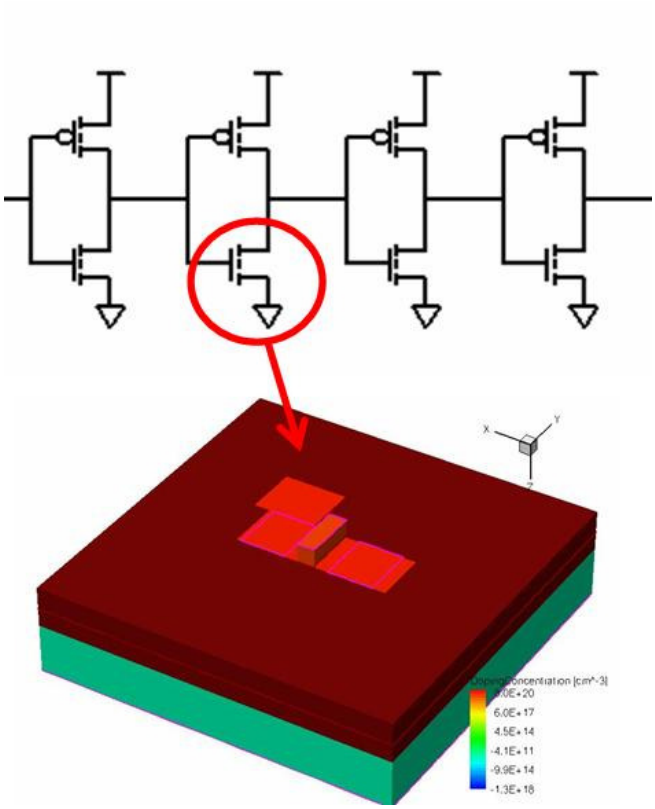

Fig. 4.8: Illustration of the mixed-mode model used for the simulations. The second nMOSFET in a four inverter chain was modeled in 3D TCAD, and the remaining inverters were modeled in SPICE.

4.9. For these simulations, the off-state nMOS (or pMOS) transistor of the second inverter in a four inverter chain was modeled using 3D-TCAD.

For the first set of simulations, the difference in generated SET pulse widths for a body-contacted device and floating-body device was compared. The results of these simulations are shown in Fig. 4.10. The incident ion LET was 40 MeV-cm^2/mg and the ion strike location was the center of the gate. This is the most sensitive region for an SOI device. To simulate the body-contacted device, an ideal contact was used to tie the body potential to ground. (Note: in the actual device, the body contact consists of an oppositely doped region next to the source that overlaps the edge of the gate, and is shorted to the source by self-aligned $CoSi_2$. The importance of this is that the body contact adds extra capacitance to the node which is not taken into account in this "simple" simulation that utilizes an ideal contact.) As seen in Fig. 4.10, the FWHM pulse is approximately the

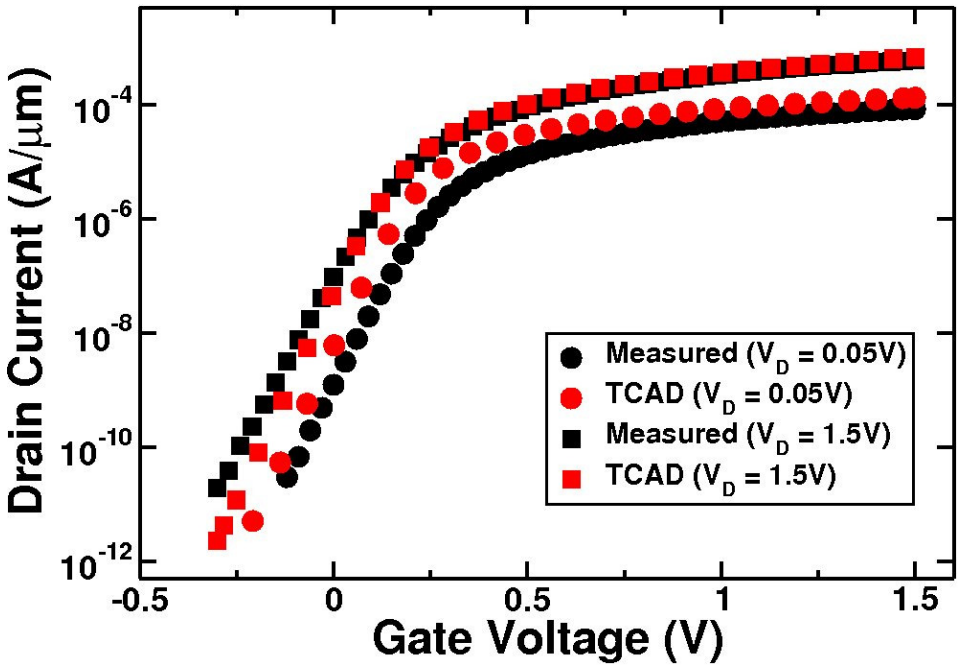

Fig. 4.9: Comparison of measured and simulated I-V curves for a device in this technology.

same for both floating-body and the ideal body-contacted devices. The generated SET pulse width at this struck node is less than 100 ps. This simulated SET width is shorter than the measured SET widths, but the main point of the simulations presented in this section is to look more at the trends than the actual SET pulse widths, and what is observed here is that simply grounding the body does not significantly alter the SET pulse width. This simulation suggests that differences in generated SET widths between the floating-body and body-contacted devices may be due more to the extra capacitance added with the body-contact than due to the body potential being simply tied to ground.

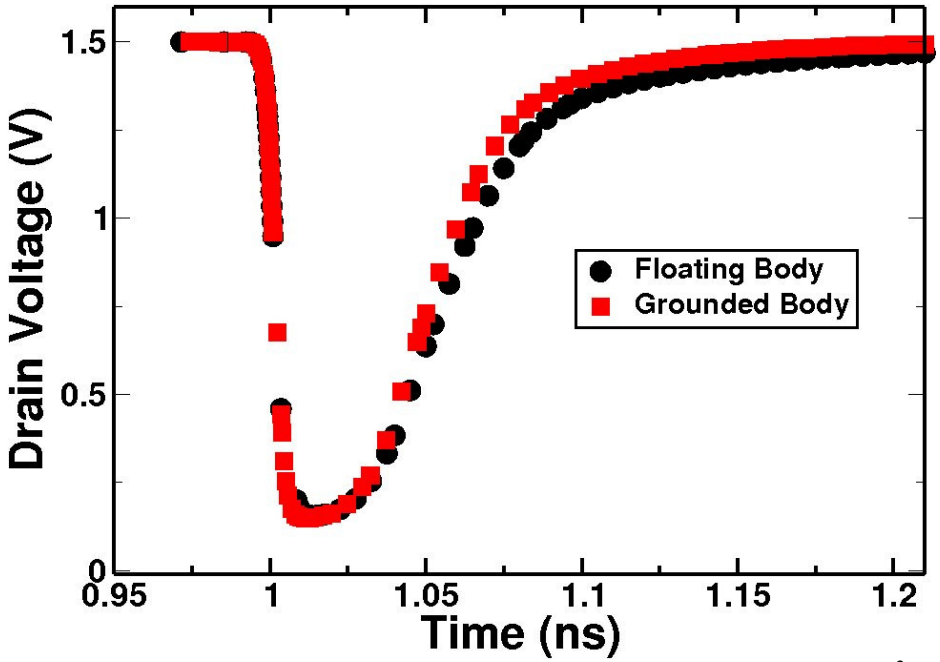

Fig. 4.10: Simulated SET pulse widths at the struck node for an LET of 40 MeV-cm^2/mg for the non-body contacted device and the body contacted device. The ion strike location in this simulation was the center of the gate.

In Fig. 4.11, the dependence on ion strike location for the floating-body device is shown. These simulations were also performed with an LET of 40 MeV-cm^2/mg. These simulations confirm that a transient is only produced when the ion strikes the body region

(i.e., the region under the gate) in these SOI devices. Identical simulations were also performed on the device with the ideal body contacts. The results were the same as those in Fig. 4.10 (i.e., the generated SET was approximately the same for both devices). The important difference is that in an inverter chain with body-ties, the smaller transients may attenuate as they propagate through the inverters in the target circuit. In the floating-body circuit, these transients may broaden as they propagate. The end result is that more transients that are greater than our minimum measurable width are recorded with the floating-body circuit. This leads to a larger heavy-ion cross section for the floating-body transistors.

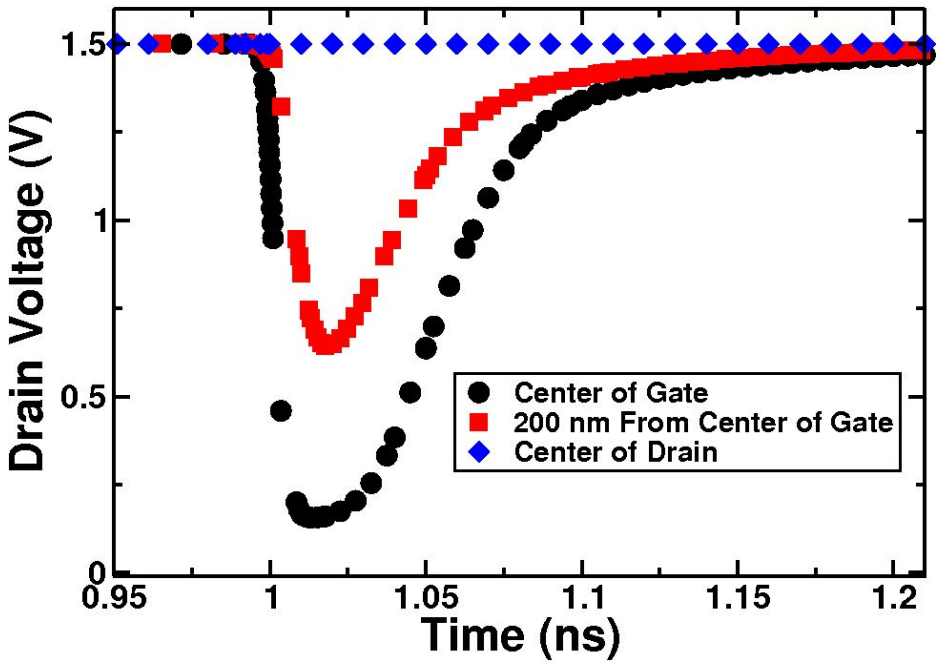

Fig. 4.11: Simulated SET pulse widths for the floating-body device showing the pulse width dependence on the ion strike location. As the strike location moves away from the center of the gate, the SET pulses become smaller. An ion strike at the center of the drain creates no SET.

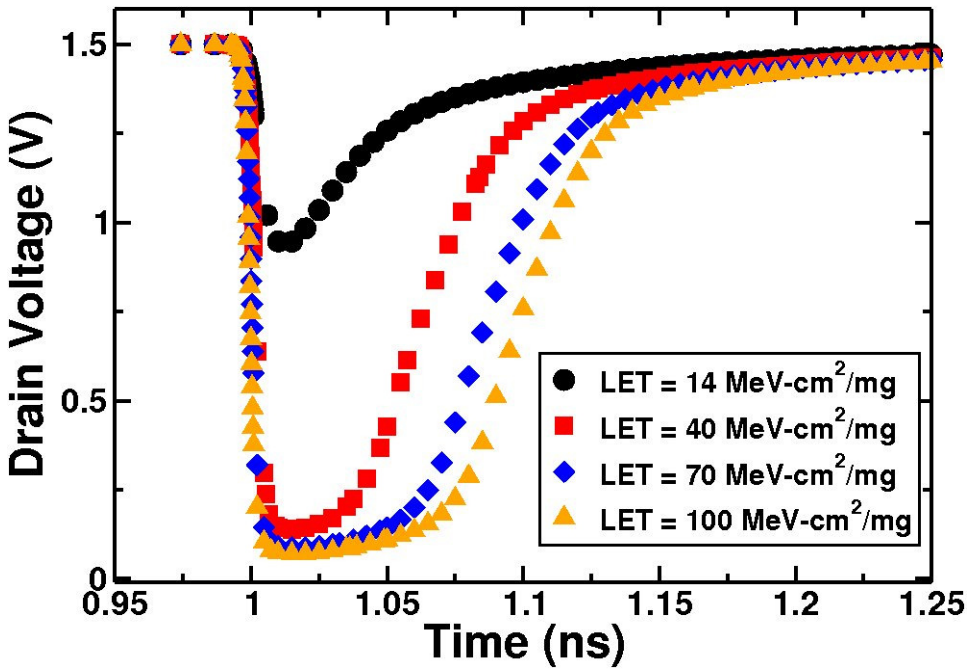

Fig. 4.12: Simulated SET pulse width distributions for strikes on the nMOS device for the ions used in testing.

The pulse width dependence on LET was also explored using TCAD simulations. The TCAD simulations were performed using the same LET's used during the heavy ion testing. A small dependence of SET pulse width on LET is observed in the simulated results presented in Fig. 4.12.

Simulations were also performed on a calibrated pMOS device. The simulated SET pulse widths were found to be significantly shorter in pMOS devices than in nMOS devices for every LET value. (Remember that, as discussed in the previous chapter, for bulk technologies, SETs induced in pMOS devices are often larger than SETs induced in nMOS devices.) The shorter simulated SETs in the pMOS devices correlate well with results presented by Gouker et al. [Gouk-08] where the threshold laser energy to create a transient in the pMOS device was approximately 2.5× the energy needed to create a transient in the nMOS device. A simulated SET strike (with an LET of 100 MeV-cm^2/mg) is shown in Fig. 4.13. The generated SET pulse is very small but is still large

enough to create a transient that is able to propagate through to the next inverter. Simulations were also performed using smaller LET values, for an LET value less than 70 MeV-cm^2/mg the generated SETs were not wide enough to propagate through more than a few inverters. However, in a floating-body inverter chain with 200 inverters (like in our test circuit); this very small generated SET could still broaden up to 800 ps (if the broadening rate was 4 ps/inverter and it was generated near the beginning of the 200 inverter chain).

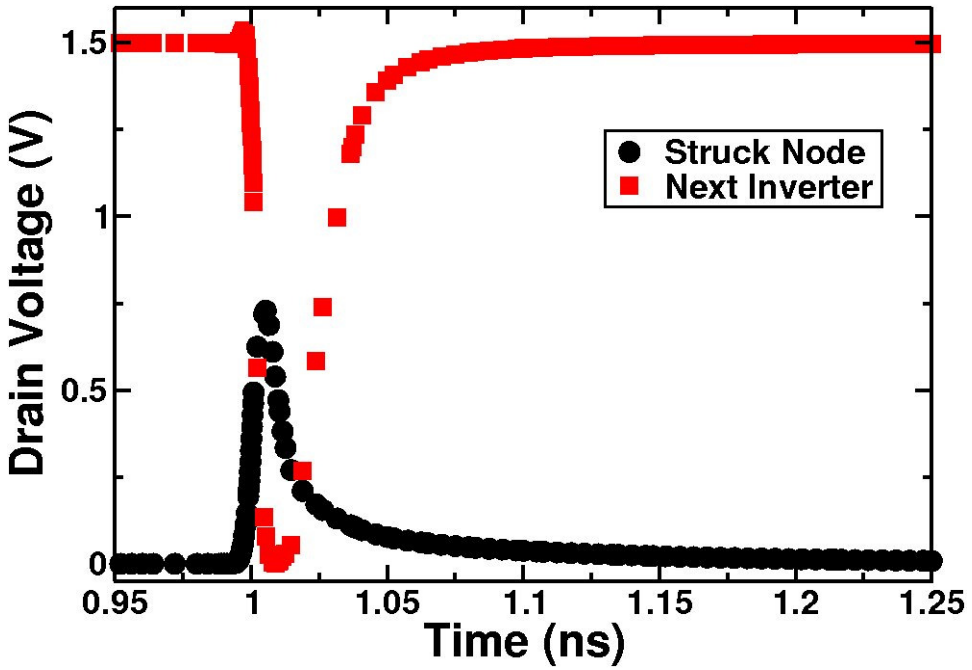

Fig. 4.13: Simulated SET pulse width for a strike on the pMOS device with an LET of 100 MeV-cm^2/mg.

Discussion

SETs widths over 280 ps have been experimentally measured in a 180-nm FDSOI process in an inverter chain with floating-body transistors and in an inverter chain with body-contacted transistors. The measured transient widths were found to be longer for

the floating-body circuit. This is primarily due to pulse broadening in the inverter chain. TCAD simulations were presented that suggest that at least some of the SETs may have been smaller than 200 ps, but the test circuit was unable to measure them accurately.

In general, the TCAD simulated pulse widths were shorter than the average measured pulse widths from the heavy ion experiment. There are numerous possible explanations for this. First of all, the SET measurement circuit was not able to accurately capture the small SETs. In other words, the small SETs may have been present in the experiment, and we were just unable to measure them. Secondly, subtle differences in the TCAD model can drastically alter simulated SET pulse widths. The TCAD model was calibrated to measured I-V curves (Fig. 4.9), but it's possible certain items (such as doping, ion strike profiles, etc.) may not have been a perfect match to the actual device and/or experiment. Overall, the goal of the simulations was to gain insight into trends. For example, it was observed that the nMOS transistors were more sensitive to single event hits than the pMOS transistors. The dependence of SET pulse width on the LET of the incident ion, the ion strike location, and simply grounding the body was also discussed.

For the majority of the TCAD simulations presented in this work, only the data from the struck node are shown. The main reason for this is that pulse broadening effects are not taken into account with usual SPICE models [Mass-08]. Since it is known that pulse broadening occurs in the floating-body devices, simulations that do not take this broadening effect into account are not completely accurate for data on SET propagation. In the floating body devices, it's possible that small SETs (like some shown in these TCAD simulations) may actually broaden (instead of attenuate) as they propagate.

Massengill et al. have presented a method to take into account pulse broadening in SPICE models, but it was not incorporated in this work [Mass-08].

To put this work into context of some previous SET measurements from bulk technologies discussed in Chapter III, the SET cross section can be compared to that of a bulk device. In Fig. 4.14, the cross section to produce a measurable SET in a 90-nm technology is compared to that of a 180-nm FDSOI technology. The data from the 90-nm technology are from the same test structure described in the previous chapter. The smallest measurable transient in the 90-nm technology was 100 ps. Even though the area of a transistor in the 180-nm technology is almost twice that of one in a 90-nm technology, the cross section is over an order of magnitude less. This is due to the fact that in SOI the area under the gate is the only area in which a reverse-biased junction exists to collect charge (as confirmed by the simulations shown in Fig. 4.11), whereas in

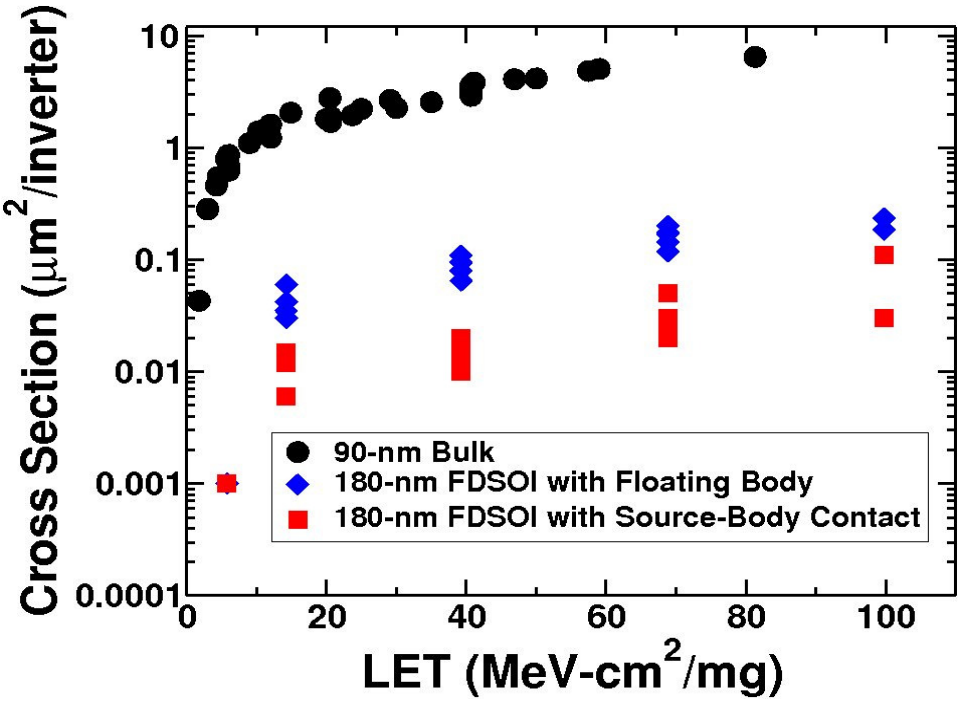

Fig. 4.14: Comparison of bulk and SOI SET cross-sections

a bulk technology reverse-biased junctions also exist between drains and substrate (or well). As seen in Fig. 4.14, SOI cross sections can be reduced even more by adding a body contact. However, the maximum measured SET pulse width for bulk and SOI circuits without body-ties circuits can be comparable due primarily to the pulse broadening effect.

Conclusions

In this chapter, heavy ion-induced digital single-event transient pulse widths in a fully-depleted SOI technology have been experimentally measured and simulated using TCAD. These are the some of the first heavy ion-induced SET pulse-width measurements for a 180-nm FDSOI technology. The long pulse widths in the floating-body circuit can be explained by pulse broadening as the transient propagates through the 200-inverter chain. TCAD simulation results show that the generated SET at the struck node is approximately the same for both a simple-grounded body and a floating-body device. However, due to pulse broadening in the floating-body circuit the transients measured in the floating-body circuit were larger than that of the body-contacted circuit. In the next chapter, this same test circuit will be tested at elevated temperatures to explore how the SET width changes as the temperature changes.

CHAPTER V

TEMPERATURE CHARACTERIZATION OF SINGLE-EVENT TRANSIENTS

Introduction

Space-borne electronic circuits are often required to operate in high radiation, extreme temperature environments. As previously discussed, single-event error rates are a strong function of SET pulse widths, and parameters that control SET pulse widths (drift, diffusion, bipolar effects, etc.) are strong functions of operating temperature. Experimental measurements of single-event phenomena over wide temperatures range are of vital importance to the radiation effects community [Alle-92, Ooka-97]. However, to date, very little research measuring the time duration of digital single-event transients over temperature has been performed. Simulation results, carried out by Shuming et al. [Shum-08] over a large temperature range in 180-nm bulk and 180-nm partially depleted SOI (silicon-on-insulator) processes show that SET pulse widths are expected to increase with temperature in bulk technologies, but not for SOI technologies. The main reason for the increase in the pulse width for the bulk process was suggested to be an increase in parasitic bipolar effects with increasing temperatures. In this chapter, the autonomous SET pulse-width measurement circuit is used to measure SET pulse widths as a function of operating temperature for each of the technologies discussed in the previous two chapters (65-nm bulk, 90-nm bulk, 130-nm bulk, and 180-nm fully-depleted SOI). Experimental and TCAD simulation results show an increase in SET pulse widths with temperature for the bulk processes, but not for the SOI process. This is the first time SET pulse-widths have been experimentally measured as a function of IC temperature in these

technologies.

130-nm Bulk

The measurement circuit used to characterize SET pulses was fabricated in a 130-nm bulk CMOS technology (from IBM). For the bulk 130-nm device, the target circuit consists of a linear chain of 100 minimum drive-strength inverters which is used to generate SETs. The measurement circuit follows the 100-inverter chain and consists of 32 latch stages connected to latches to store the number of inverters affected by each SET. With the individual inverter stage delay at room temperature of about 100 ps, this circuit allows measurement of SET pulses ranging from 100 ps to 2 ns with a 50 ps measurement resolution.

A ring oscillator consisting of pulse-measurement circuit latch stages was fabricated to obtain the precise delay of an individual latch stage. Since SET measurements were

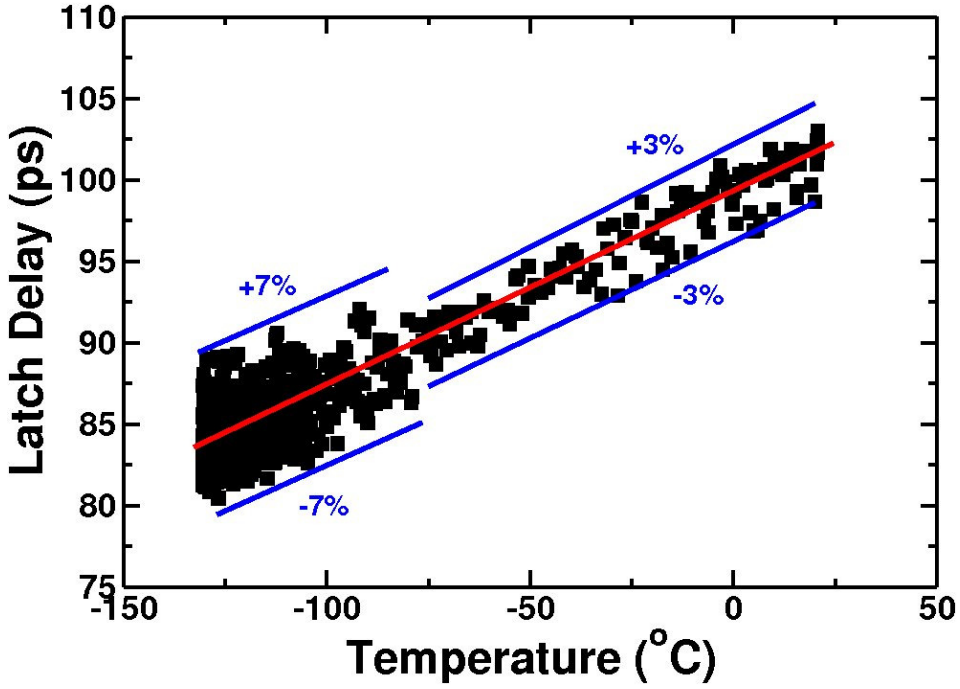

Fig. 5.1: 130-nm stage delay as a function of temperature.

going to be performed over a wide range of temperatures, it was imperative to measure the change in stage delay with temperature. Using the same test setup used for the heavy ion testing, the ring oscillator frequency was measured as a function of operating temperature. As seen in Fig. 5.1, the stage delay is approximately linear with temperature in the range to be considered in this work. Since the pulse width in the autonomous SET measurement circuit is found by multiplying the number of stages affected by the latch delay, any error in the latch delay will also add to the error in the SET width measurement. From Fig. 5.1, one can see that above -75° C, the latch delay measurements range by about 3%. Below -75° C, the range of latch delay measurements is somewhat larger (about plus or minus 7%). The larger spread in the stage delay measurements is due to an increase in jitter in the ring oscillator at the colder temperatures. Because this technology was not designed to be used at temperatures below -50° C, a significant increase in jitter in the ring oscillator at the extreme temperatures can be expected.

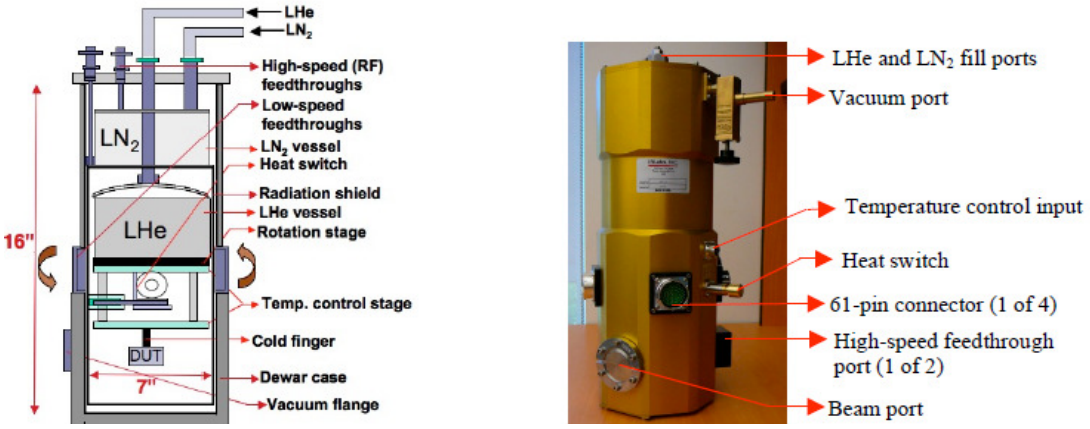

Fig. 5.2: Illustration and photograph of the cryogenic test system used in this work.

To explore the effect of temperature on SET pulse widths in this 130-nm technology, radiation testing was performed using a customized cryogenic single-event test system [Rama-08]. The bulk 130-nm test circuits were tested with heavy ions at the Texas A&M University Cyclotron facility over a temperature ranging from -135^{o} C up to room temperature (20^{o} C). The temperature of the IC was controlled in the test system via a cold finger (this cold finger is a piece of copper). One end of the cold finger contacted the package of the device–under-test, while the other end was connected to a liquid nitrogen vessel. The cold finger transferred heat between the device-under-test and the liquid nitrogen. Temperature measurements were taken using a sensor attached to the cold finger next to the device-under-test. The temperature reported in this section is the cold finger temperature as measured by the temperature sensor.

The circuit was tested with 2766 MeV xenon ions at normal incidence with an LET of 40.1 MeV-cm^2/mg and was exposed to an ion fluence of 5×10^7 particles/cm^2. This led

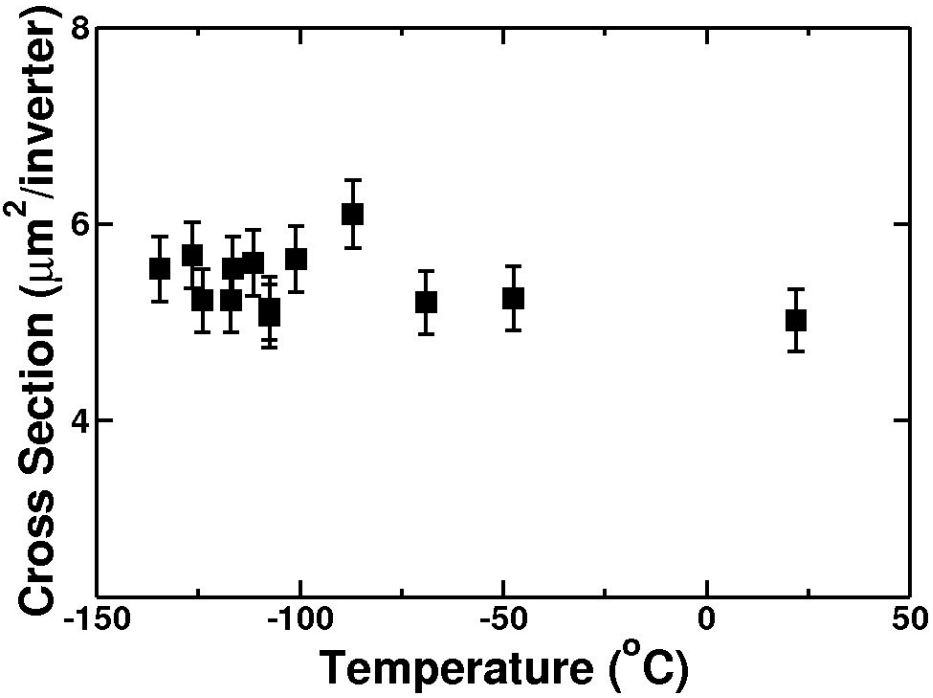

Fig. 5.3: SET cross-section as a function of temperature.

to approximately 200 SET events being measured at each temperature. The SET cross-section is plotted as a function of temperature in Fig. 5.3. The SET cross-section is equal to the number of SETs measured divided by the particle fluence. The SET cross-section does not change significantly with temperature. This implies that the sensitive volume needed to create an SET is effectively the same across the operating temperatures. In other words, the area in which charge is collected (around the sensitive drain) does not change with temperature.

A histogram of the measured SET pulse width distribution in units of latch delay at room temperature (20° C) is plotted in Fig. 5.4. To obtain the SET pulse widths, one multiplies the number of latches by the delay (shown in Fig. 5.1). The histograms (in units of latches) were almost identical for each temperature. In Fig. 5.5, the data from Fig. 5.4 is multiplied by the latch delay to form the SET pulse width histogram. In this

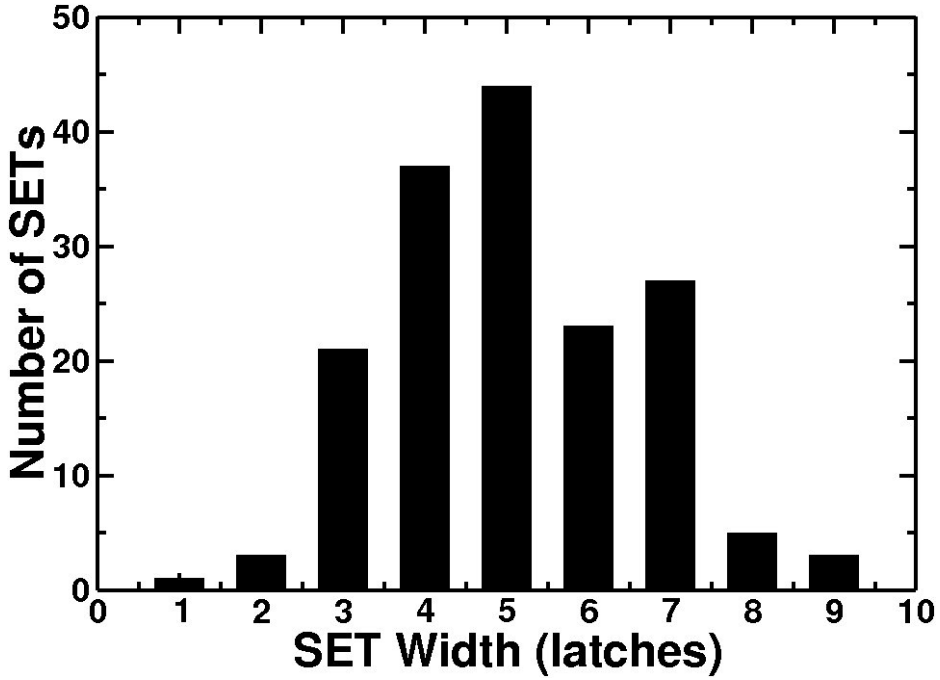

Fig. 5.4: Measured SET pulse width histogram at room temperature. The histograms (in units of latch delays) were similar for all temperatures.

figure, the error in the number of SET events is simply plus or minus the square root of the number of counts. The error in the SET width takes into account the 3% error in the latch delay measurements. Since the longer SET pulse widths require several latch stages to change, they have a larger error associated with them than the shorter SET widths.

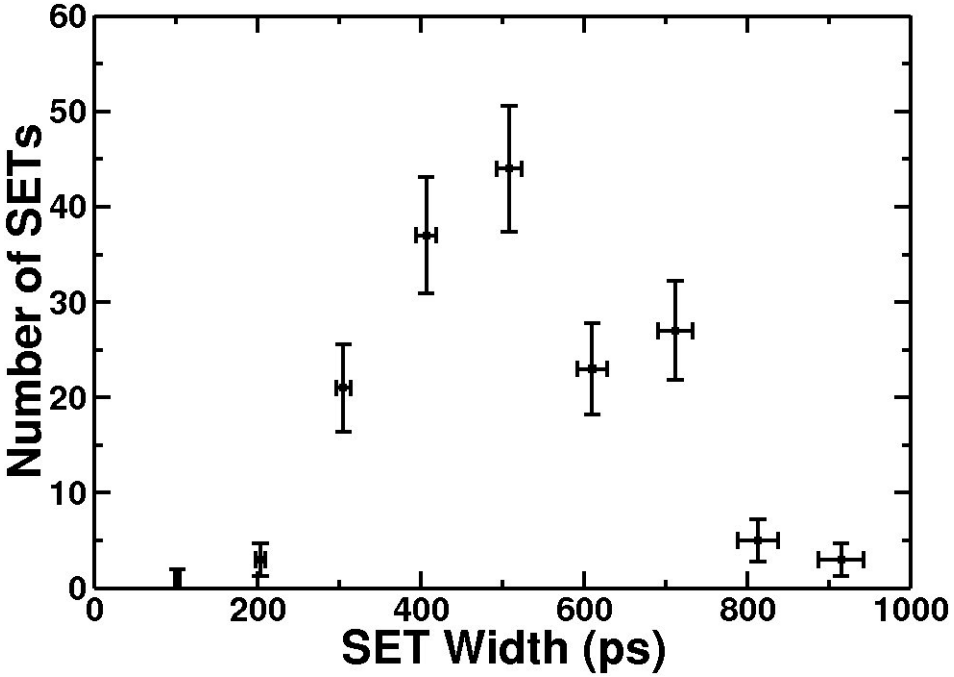

Fig. 5.5: Measured SET pulse width histogram (with error bars) at room temperature.

In Fig. 5.6, the average number of latch stages affected by SET pulses as a function of temperature is plotted. Note that the average number of latch stages affected shows little change as a function of temperature. To find the average SET width, the number of latch stages needs to be multiplied by the average latch delay for a given temperature. However, this requires propagating the two error sources to obtain the correct error in the SET width. To compound two error sources in an equation of the form f(x,y) = x*y, Equation 1 can be used. In this equation, x and y represent the latch delay and the average number of latches affected by an SET, and f(x,y) is the average SET pulse width.

$$\left[\frac{\Delta f(x,y)}{f(x,y)}\right]^2 = \left[\frac{\Delta x}{x}\right]^2 + \left[\frac{\Delta y}{y}\right]^2 \qquad (1)$$

By taking into account the two sources of error on the average SET width as a function of temperature, the cold temperature average SET pulse width data plotted with the both sources of error in the measurements included. With the additional 3% error in the latch delay measurements taken into account, the result is that for temperatures above -75^{o} C the error in the average SET width measurement is about ± 20 ps. In Fig. 5.7, one can see that for the very low (< -75^{o} C) temperatures, any change in SET width with temperature is within the error bars. However, as the temperature rises above -50^{o} C, the average SET width increases by an amount greater than the error. The average SET width increases from 385 ps (± 30 ps) at -135° C to over 500 ps (± 20 ps) at 20° C.

Another source of error not taken into account in this analysis is the quantization error of the measurement circuit. The quantization error is the unavoidable error due to the finite resolution of the measurement circuit. For example, since the measurement circuit has a resolution of ±50 ps, all transients within a time duration of 100 ps of each other may be measured as the same value. However, due to the fairly large spread in SET pulse widths measured (from 100 ps to 900 ps) and the large number of total counts in the SET width distribution, one can assume that this error is small. On the other hand, if the measurement resolution was much larger or the SET width distribution was smaller, this error may play a more significant role in the average SET width calculations.

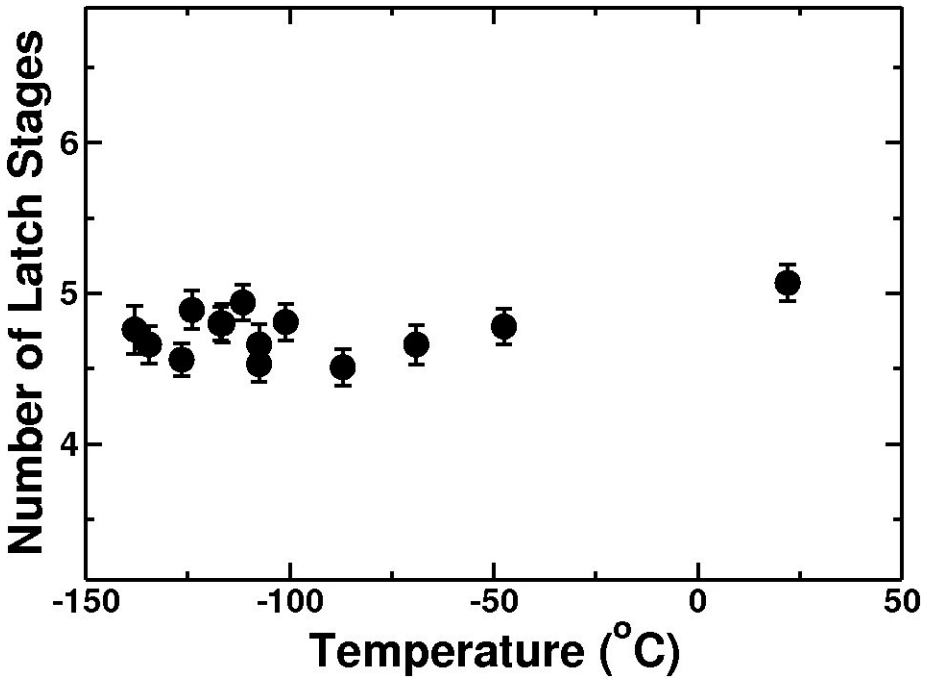

Fig. 5.6: Average SET pulse width in units of latch delays.

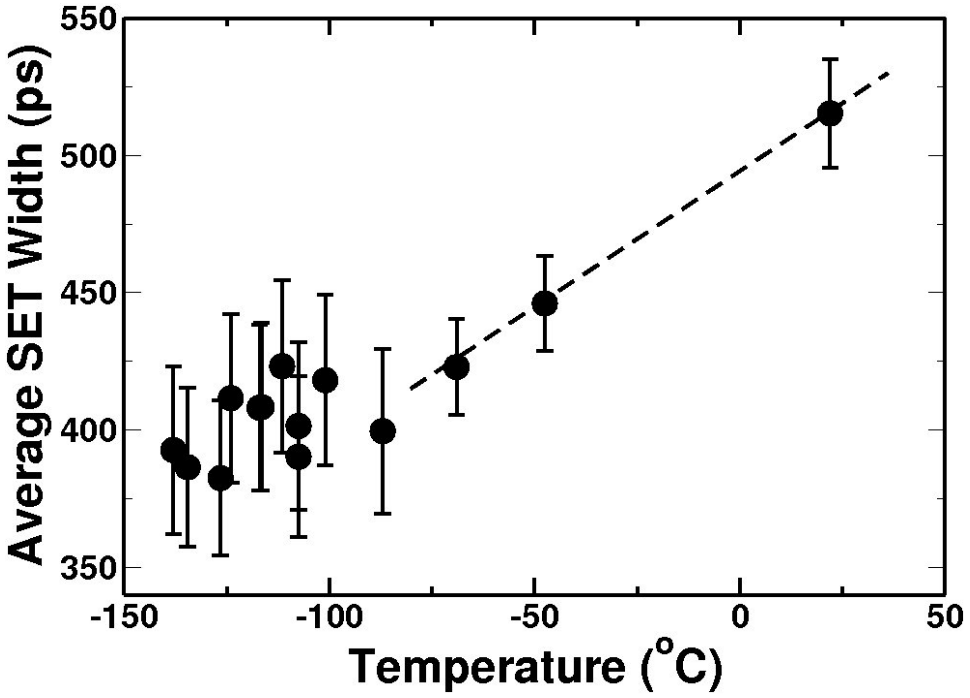

Fig. 5.7: Average SET pulse width for the cold temperature testing.

The bulk 130-nm test circuit was also tested with heavy ions at the Lawrence Berkeley National Labs cyclotron facility at elevated temperatures. For the elevated temperature testing, the circuit was tested with 906 MeV Krypton ions at normal incidence with an LET of 30.9 MeV-cm^2/mg. (Note that this is a slightly lower LET than was used for the cold temperature test.) The temperature of the IC was controlled through a resistive heater attached to the package. Temperature measurements were taken using a resistive sensor attached to the package. Ion exposures were carried out at temperatures of approximately 25°, 50°, 100°, and 150° C. The temperature reported for the elevated temperature testing is the package temperature as measured by the temperature sensor.

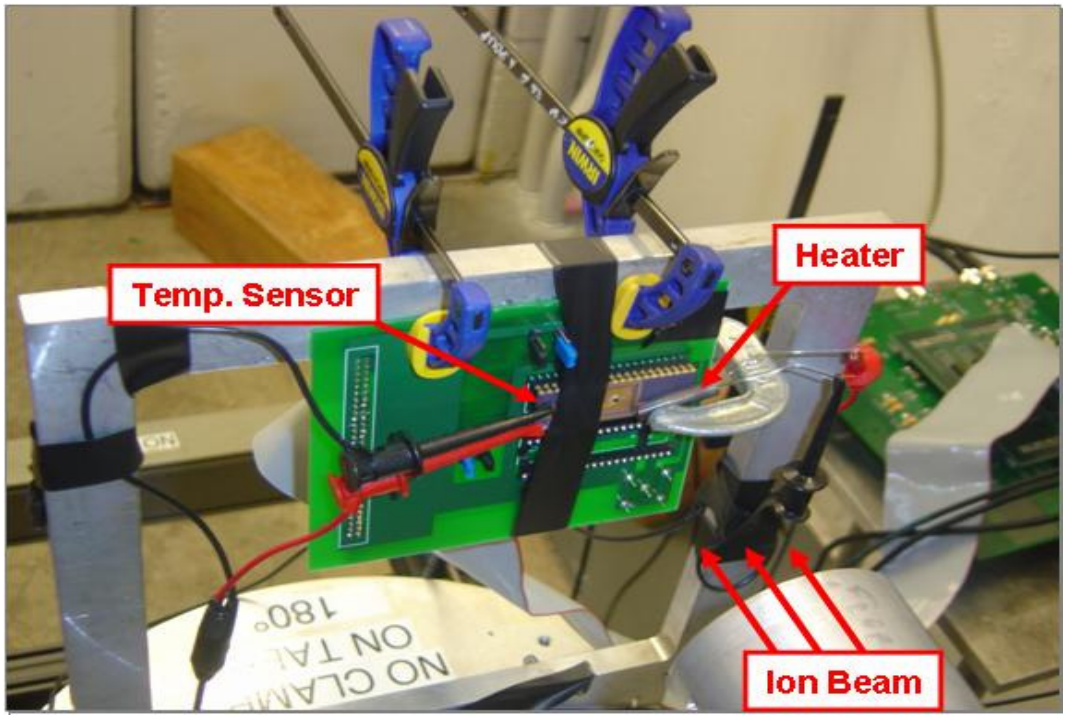

Fig. 5.8: Photograph of the test setup for all of the elevated temperature testing performed in this work.

A comparison of SET pulse-widths at the four different temperatures for exposures to krypton ions with LET of 30.9 MeV-cm^2/mg for the 130-nm test structure is summarized in Fig. 5.9. The pulse width distribution shifts towards a higher average value as the temperature increases. The same trend observed with the cold temperature data is also seen with elevated temperature data. SET pulse widths increase with temperature. Approximately 200 SET events were measured at each temperature. The circuit was exposed to an ion fluence of 10^8 particles/cm^2.

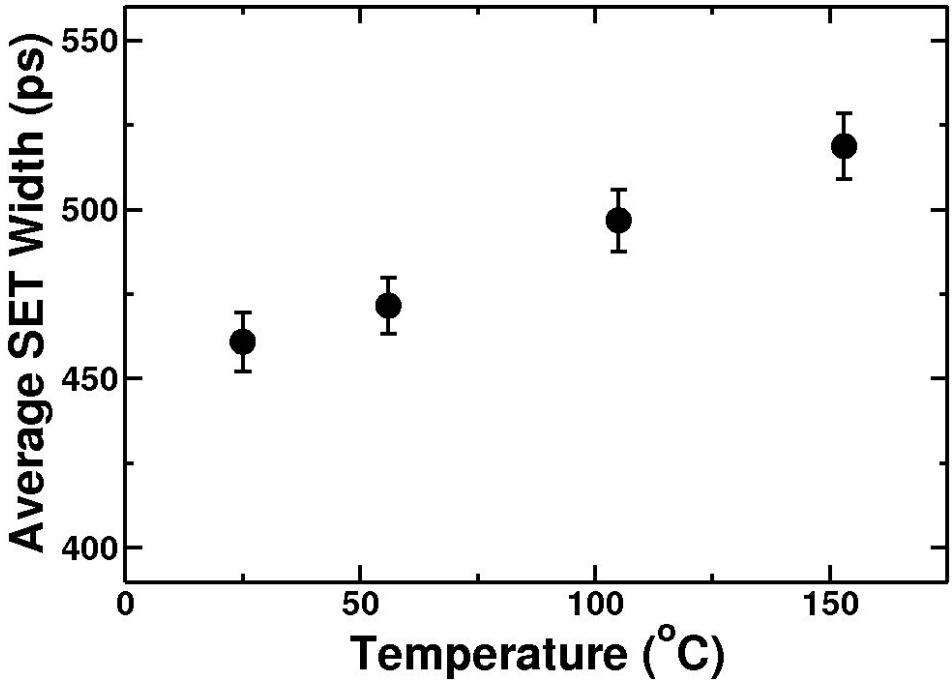

Fig. 5.9: Average SET pulse width for the elevated temperature testing of the 130-nm test circuits.

Mixed-mode simulations for a string of eight inverters designed using a calibrated 130-nm bulk model were performed to identify the factors responsible for pulse-width variations. For these simulations, both the off-state pMOS and nMOS transistors of the second inverter were modeled using a 3D-TCAD simulator (see Fig. 5.10). The pMOS

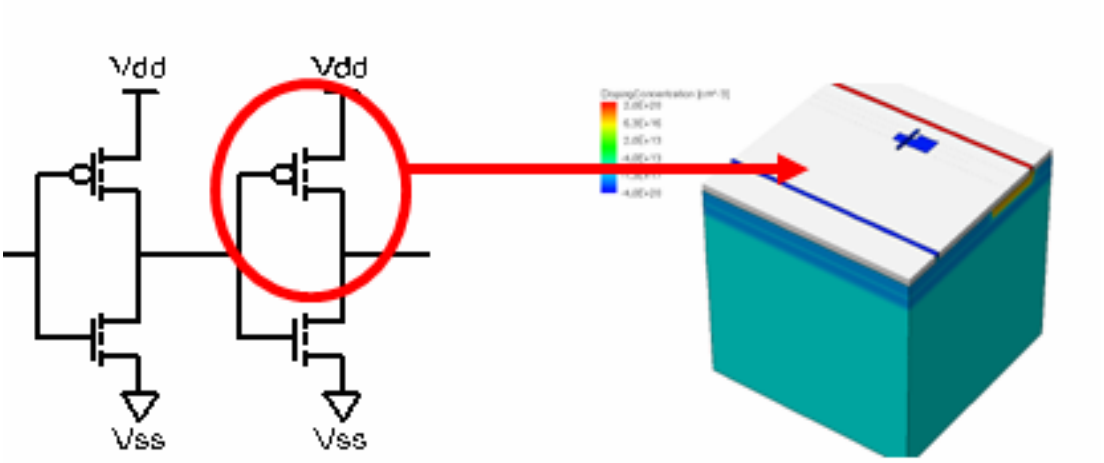

Fig 5.10: A 130-nm TCAD model used to study the effect of temperature on SET pulse widths using a mixed mode simulation. For the 130-nm bulk device, either the off state pMOS or nMOS device was modeled in 3D TCAD.

transistor has been previously found to be responsible for the longest SETs in this technology [Amus-07, Nara-08]. The normally incident ion LET was fixed at 31 MeV-cm^2/mg, which corresponds to about 0.3 pC of deposited charge per micrometer. The ion strike location was the center of the drain region. This is the most sensitive strike location for the device. The temperature in both the TCAD and compact models was varied from -50˚ C to 150˚ C. For the TCAD simulations, temperature-dependent physical models were used. These physical models included: Fermi-Dirac statistics, SRH recombination, Auger recombination, and the Philips mobility model. The charge deposited by the incident heavy-ions was modeled using a Gaussian radial profile with a characteristic 1/*e* radius of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps.

Fig. 5.11 shows a plot of the width of the pulse from a pMOS strike measured at the output of the struck inverter for five different temperatures. The trend for this device is

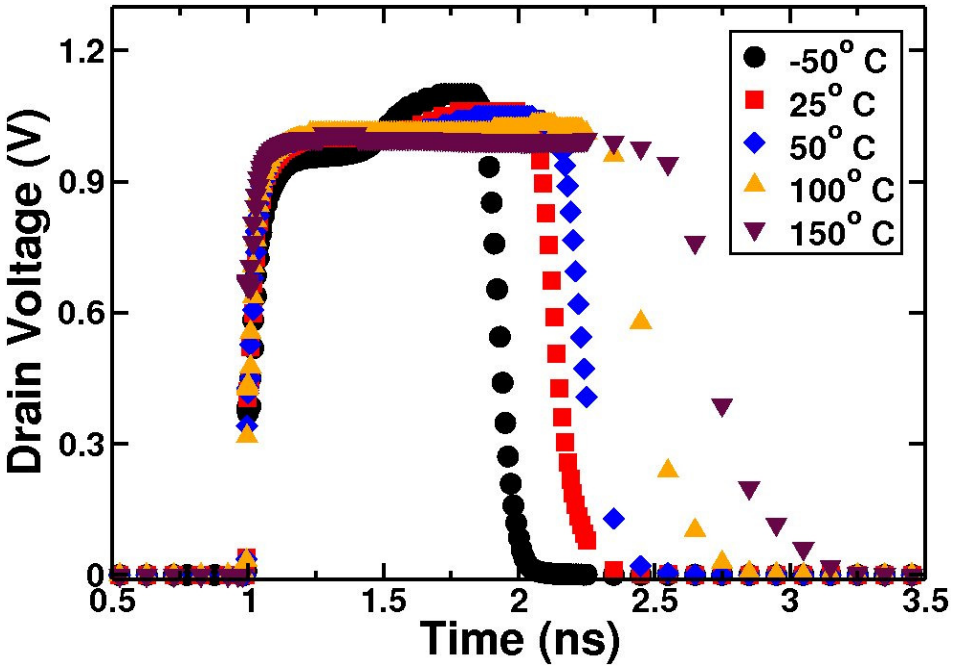

Fig. 5.11: Results of the 130-nm mixed-mode simulation of the pMOS device showing SET pulses on the struck node for five temperatures.

longer pulse widths with higher temperatures. Over the experimentally tested temperature range (25˚ C to 150˚ C), a large increase in pulse width is observed. SET widths for an nMOS strike are shown in Fig. 5.12. SETs originating in the nMOS devices show little change with temperature. The combined effect of nMOS and pMOS strikes would lead to an overall increase in average SET pulse widths with temperature. This correlates well with the increase in SET pulse widths seen in the experimental results.

To explore the effect of bipolar amplification on the pulse width, mixed-mode simulations were performed with the gate and source of the pMOS transistor removed. The remaining circuit is a reverse-biased diode. For this diode, all other charge collection mechanisms except the parasitic-bipolar mechanism will be present. Plots of the simulated drain current at the struck node of the pMOS device and the diode are shown in

Figs. 5.13 and 5.14. The increase in SET pulse width for the diode with temperature is noticeably smaller than that of the pMOS device. By integrating the drain current over time for the both the pMOS device and the diode, one can obtain the total charge collected at the drain node of each device due to the ion strike. To deterimine a bipolar enhancement factor, the total collected charge for the pMOS device can be divided by the total collected charge for the diode. This bipolar enhancement factor is plotted in Fig. 5.15. The simulations confirm that an enhancement in parasitic bipolar amplification with temperature is the primary cause for the increase in SET widths observed with the pMOS device.

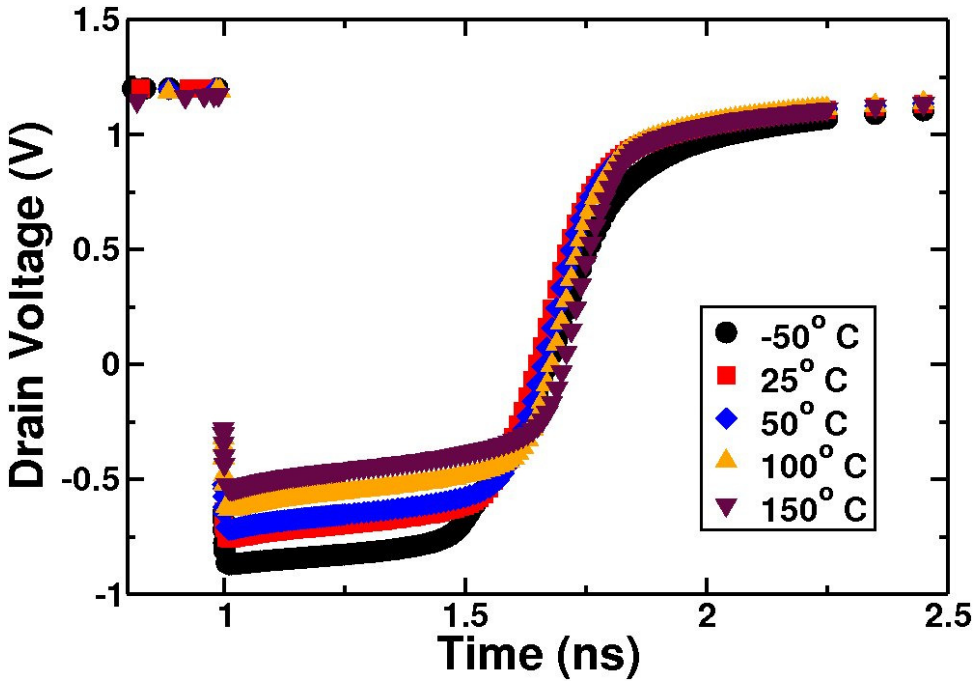

Fig. 5.12: Results of the 130-nm mixed-mode simulation of the nMOS device showing SET pulses on the struck node.

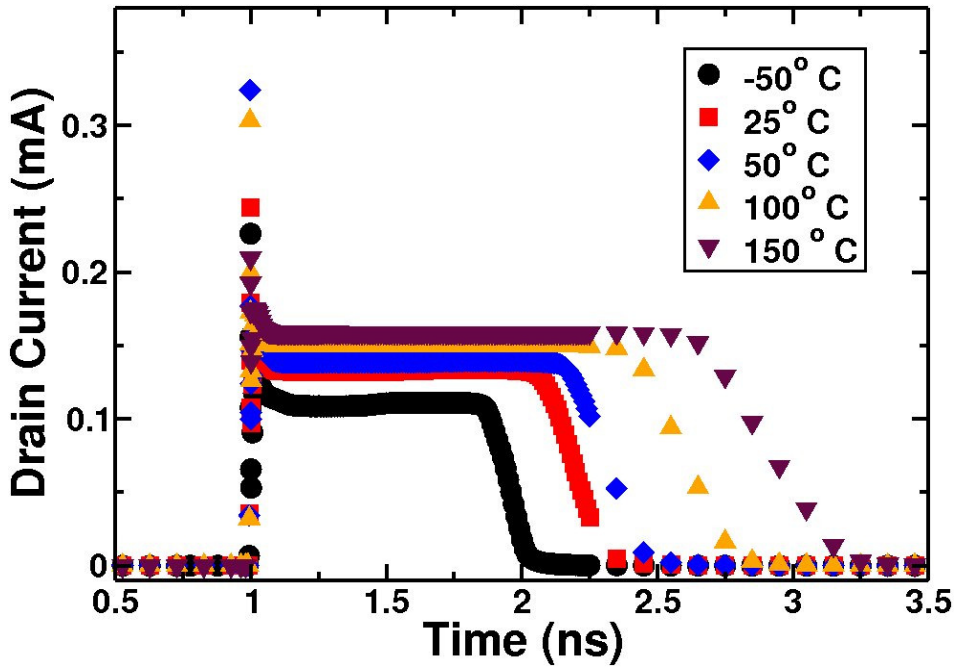

Fig. 5.13: Results of the 130-nm mixed mode simulation showing the drain current on the struck node of the pMOS device for five temperatures.

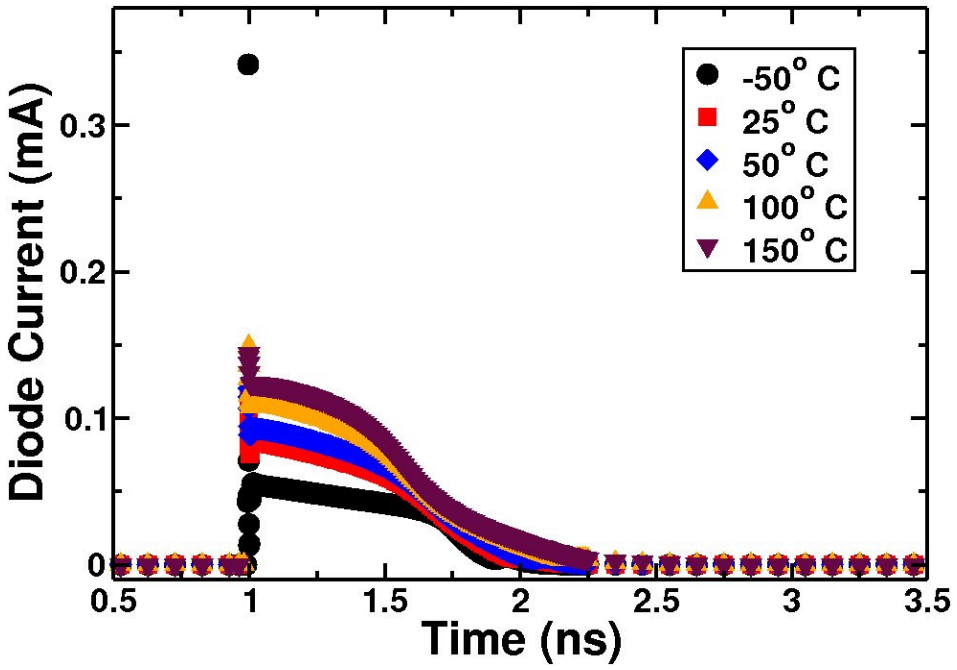

Fig. 5.14: Results of the 130-nm mixed mode simulation showing the current on the struck node of the p-diode for five temperatures.

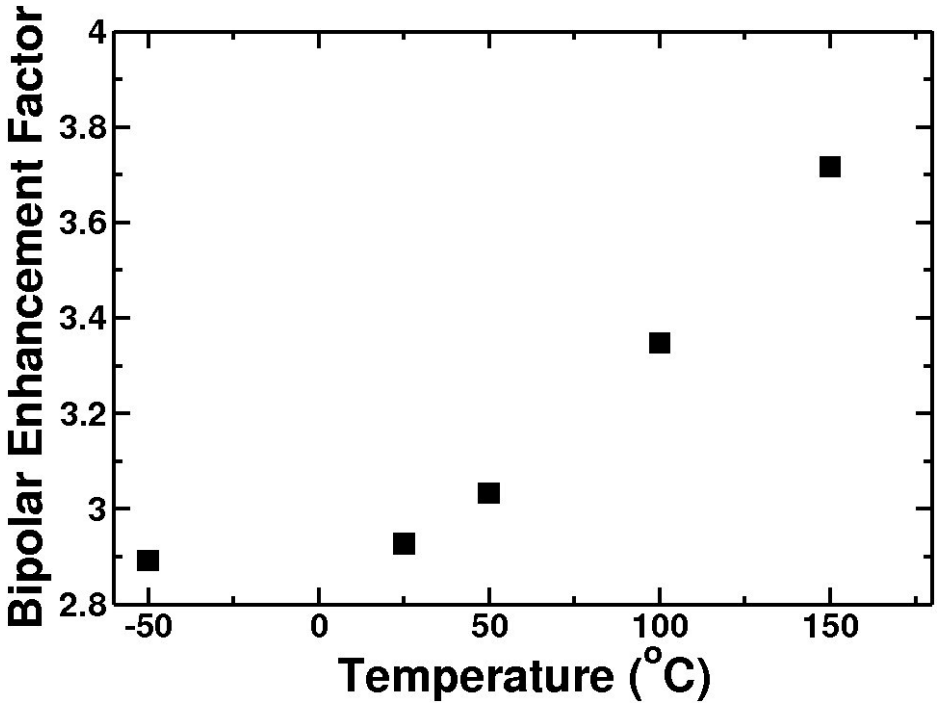

Fig 5.15: Bipolar enhancement factor plotted as a function of temperature.

90-nm Bulk

The measurement circuit was also used to characterize SET pulses in a 90-nm bulk CMOS technology. As a reminder, the 90-nm test circuit consists of a target circuit comprising a linear chain of 1000 minimum drive-strength inverters (as opposed to only 100 inverters for the 130-nm circuit). The individual inverter stage delay in this circuit at room temperature was also about 100 ps. The test circuit was tested with heavy ions at the Texas A&M University Cyclotron facility. The circuit was tested with 1934 MeV xenon ions with an LET (Linear Energy Transfer) of 52.3 MeV-cm^2/mg. The temperature of the IC was controlled in the same manner as was done with the elevated temperature 130-nm bulk experiment. Ion exposures were carried out at temperatures of 25°, 50°, and 100° C. Variations in inverter delays for this temperature range in this test structure were less than 8%, and were less than the measurement resolution.

A comparison of SET pulse widths at three different temperatures for exposures to xenon ions with LET of 52.3 MeV-cm^2/mg for the 90-nm bulk device is shown in Fig. 5.16. The pulse width distribution shifts towards a higher average value as the temperature increases for this bulk technology. The average measured SET pulse widths were 920 ps, 970 ps, and greater than 1260 ps at 25˚ C, 50˚ C, and 100˚ C, respectively. This represents more than a 37% increase in the average pulse width from 25˚ C to 100˚ C. The longest measured SET pulse width increased from 1.5 ns to 1.9 ns (longest possible measurement with this circuit as implemented here, based on the number of inverters in the measurement chain) with an increase in temperature from room temperature (?) to 100˚ C. As the limits of measurements were approximately 1.9 ns, some of the actual SET pulse width may be longer for 100˚ C measurements.

Heavy ion exposures were also performed at an incident angle of 50˚. Fig. 5.17 show the pulse width data for a xenon ion exposure at an incident angle of 50˚ (i.e., an effective LET of 81.3 MeV-cm^2/mg), displaying a similar trend as a function of temperature. The total ion fluence was kept constant for both exposures. The number of SET's varied with angle of incidence, but the number of SET's measured for the total fluence of ions, however, did not change with temperature. As observed with the 130-nm data, these results show that the operating temperature of the die has a significant impact on the SET pulse width, but not the cross section. This means that in a given environment, one would expect to find longer transients with increasing temperatures, but not necessarily more transients for these two technologies.

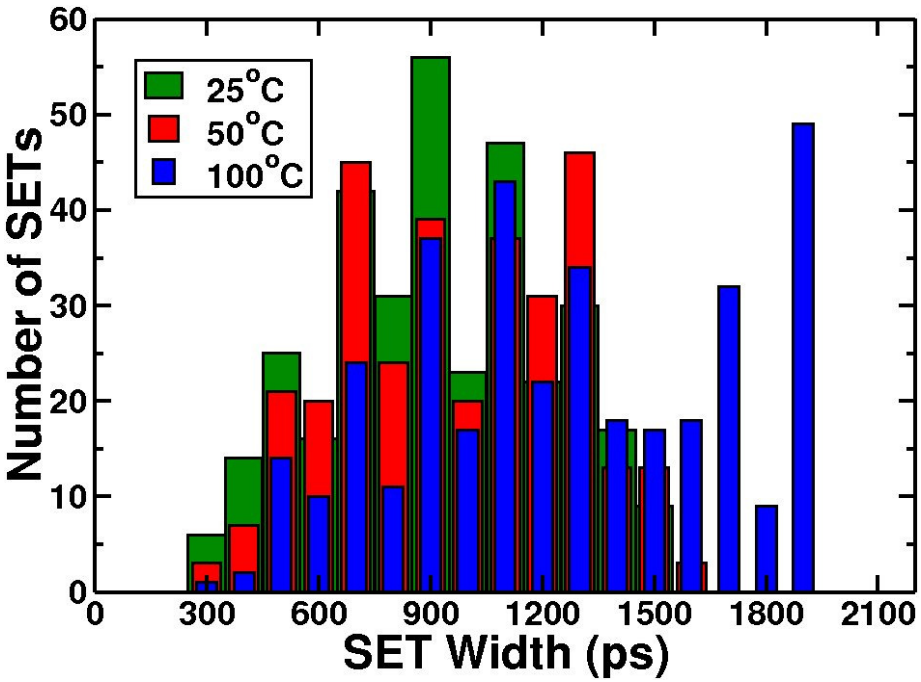

Fig. 5.16: 90-nm bulk SET pulse width distribution for xenon (LET=52 MeV-cm^2/mg) at temperatures of 25˚ C, 50˚ C, and 100˚ C. At 100^o C, some of the SETs were longer than the measurement limit of the test circuit.

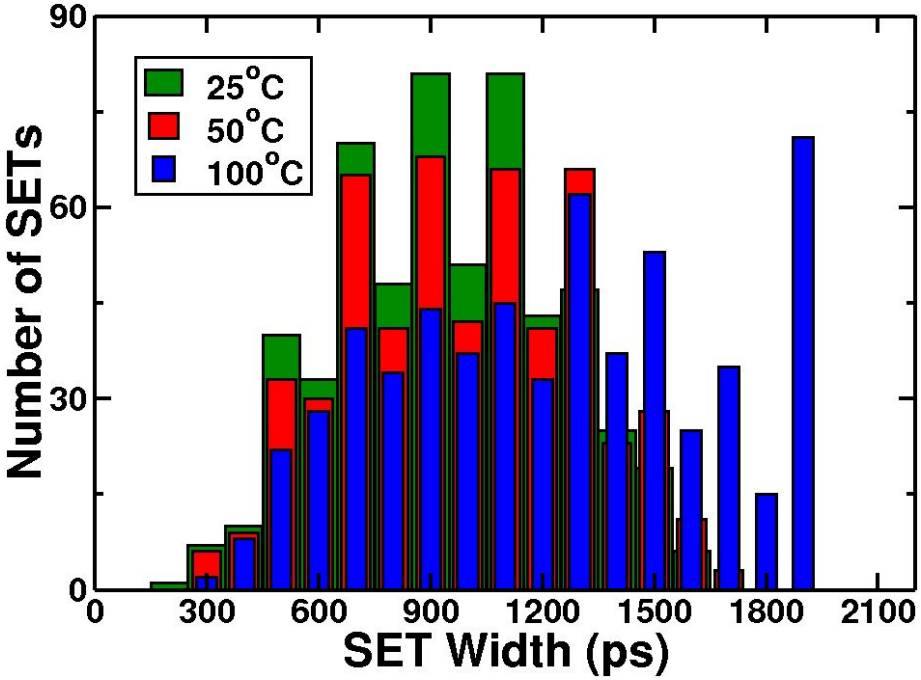

Fig. 5.17: 90-nm bulk SET pulse width distribution for xenon at an incident angle of 50^o (effective LET=81 MeV-cm^2/mg) at temperatures of 25˚ C, 50˚ C, and 100˚ C.

The same broadening analysis performed in the previous chapter on the FDSOI structure was also performed on the room temperature pulse width distribution for the 90-nm bulk circuit. Fig. 5.18 shows plots of a possible original distribution of SETs without pulse broadening for the room temperature (25^{o} C) results for an LET of 52 MeV-cm^{2}/mg, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events. The average SET pulse width for the distribution without broadening is about 400 ps.

The broadening analysis was also performed on the elevated temperature distributions. As can be seen in Fig. 5.19, this analysis suggests that the average generated SET widths increased from 400 ps at 25^{o} C to 700 ps at 100^{o} C. (Note: this analysis is only valid if the broadening rate is unchanged with temperature. Recent work has shown this to be the case [Mass-08].) If the broadening is unaffected by temperature, one can infer that the increase in measured SET pulse width with temperature is due to an increase in the width of the generated SET.

Obviously any error from the laser experiment (that was used to determine the broadening rate) and/or the curve fit in Fig. 5.18 would change the results of this broadening analysis. However, even a fairly large error (such as 20%) would only change the broadening rate by 0.2 ps. A 0.2 ps change in the broadening rate would change the maximum SET in Figs. 5.17 and 5.18 by approximately 200 ps. However, the average unbroadened SET width would only change by 100 ps. Since the individual stage delay in the measurement circuit was also about 100 ps, one can assume that the error in the broadening rate has little impact on the results of the analysis presented here.

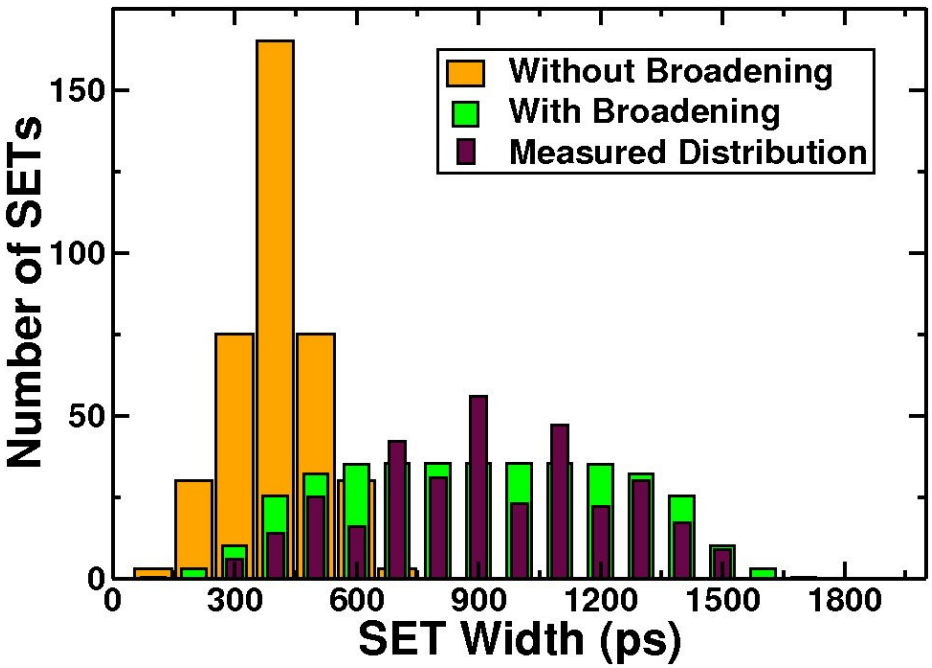

Fig. 5.18: Plots of a possible original distribution at 25° C of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events.

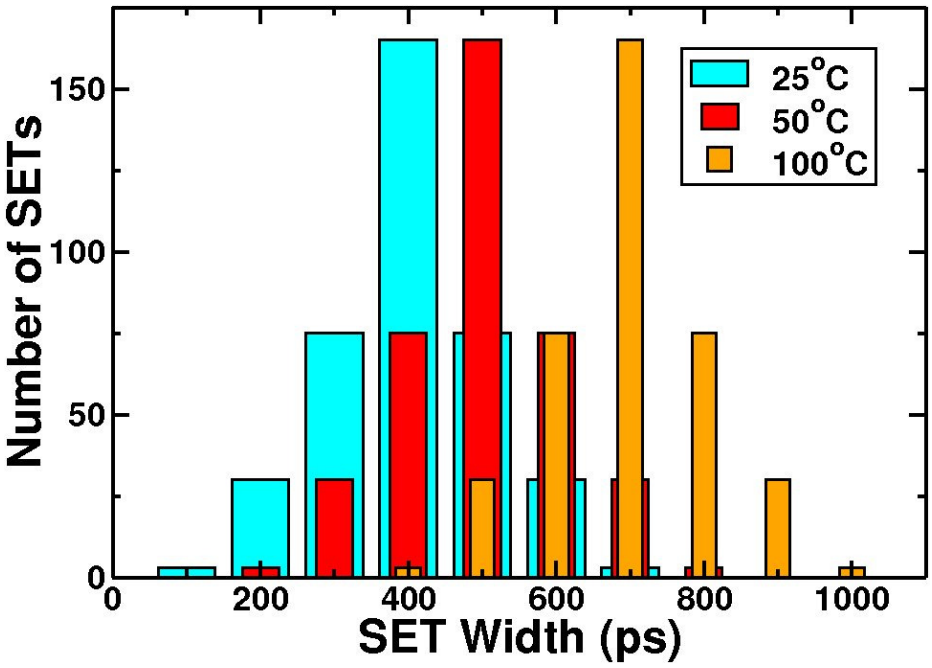

Fig. 5.19: Plots of a possible original distribution of SETs without pulse broadening for 25° C, 50° C, and 100° C.

Measurements of digital SET pulse widths show that an increase in temperature leads to an increase in SET pulse widths for a 90-nm bulk device. For this 90-nm bulk device, average values of SET pulse widths increased by as much as 37% when temperatures increased from 25˚ to 100 C˚. Due to the similarities between this process and the 130-nm process discussed earlier, one can conclude that the increase in SET pulse widths in this technology is also due to an enhancement in bipolar amplification as the temperature is increased.

65-nm Bulk

The 65-nm test structures were tested with heavy ions at the Lawrence Berkeley National Lab Cyclotron facility using xenon ions with an LET (linear energy transfer) of 58.8 MeV-cm^2/mg. Ion exposures were once again carried out at temperatures of 25°, 50°, and 100° C. Variations in inverter stage delays for this temperature range were recorded using a ring oscillator that was designed using the same inverter stages used in the measurement circuit. The ring oscillator frequency was measured at the temperatures used for the heavy ion experiment to determine the individual stage delay of the measurement circuit. The inverter stage delay increased linearly with temperature from approximately 25 ps at 25° C to 34 ps at 100° C.

Histograms of the measured SET pulse width distributions at three different temperatures for exposures to xenon ions for the same well and separate well 1000-inverter chain target circuit are shown in Figs. 5.20 and 5.21. As can be seen in the histograms, the SET pulse width distribution clearly shifts towards longer SET widths as the temperature is increased. The average measured SET pulse widths are shown in Fig. 5.22. More than an 80% increase in the average pulse width was observed in both circuits

as the temperature increased from 25˚ C to 100˚ C. The longest measured SET pulse width increased from 200 ps to 304 ps for the same well circuit. In the separate well circuit, the longest measured SET width increased to 200 ps to 408 ps.

The total ion fluence was 10^8 ions/cm^2 for each exposure. The number of SETs measured for the total fluence of ions for the same well circuit was 139 at 25° C, 163 at 50° C, and 235 at 100° C. For the separate well circuit, the total number of SETs measured was 710 at 25° C, 943 at 50° C, and 1041 at 100° C. The increase in the number of transients measured suggests that the sensitive volume (i.e., the area around each transistor that can collect enough charge to generate an SET) increased with temperature. Recall that SET measurements in similar inverter chains over temperature in 90-nm and 130-nm bulk technologies showed no increase in the number of SET events with temperature.

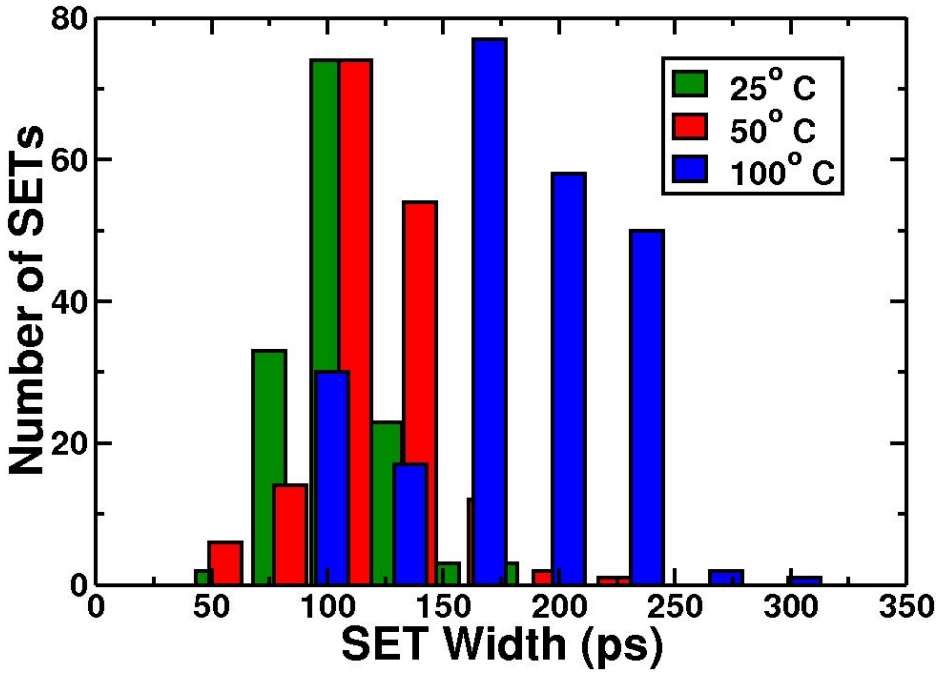

Fig. 5.20: Measured SET pulse width distribution for the same well inverter chain circuit. Note that as the temperature increases the distribution shifts to the longer SET widths

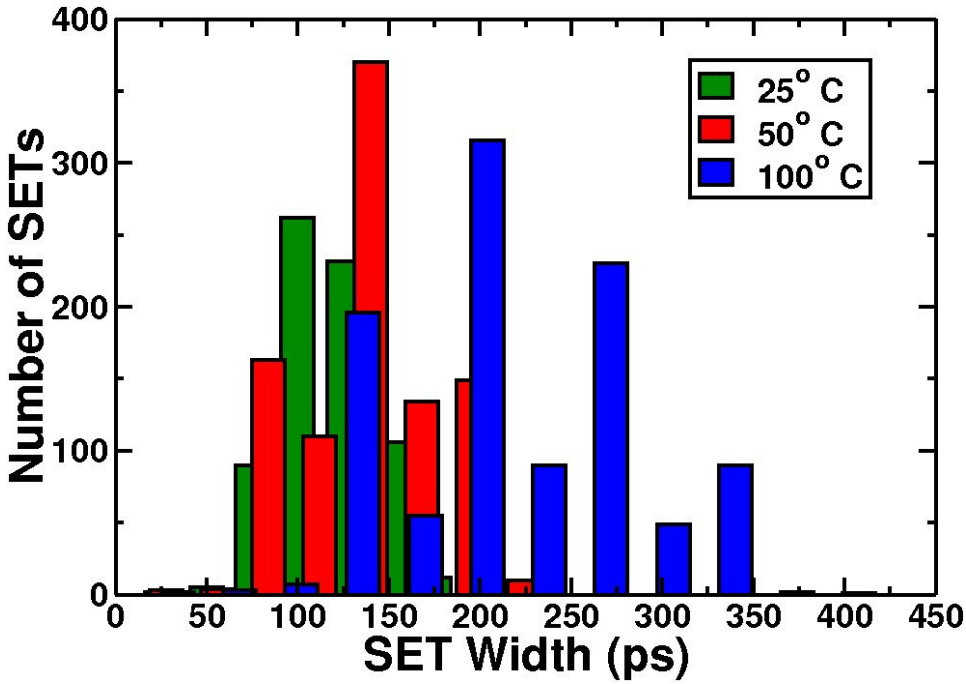

Fig. 5.21: Measured SET pulse width distribution for the separate well inverter chain circuit.

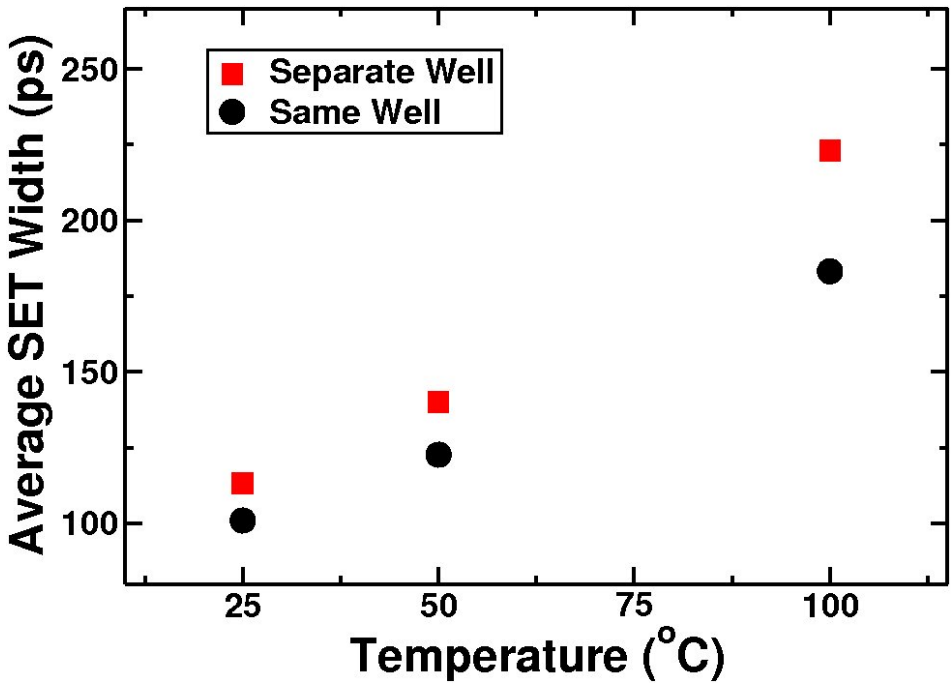

Fig. 5.22: Average SET width measurements as a function of temperature for the separate well and same well 1000-inverter chain target circuits.

180-nm Fully-Depleted SOI

The 180-nm FDSOI test circuit described in Chapter IV was also used to characterize SET pulses over temperature. The change in individual stage delay over the temperature range of the testing for this test chip was negligible. The FDSOI 180-nm test circuits were tested with heavy ions at the Texas A&M University Cyclotron facility with 1934 MeV xenon ions at normal incidence with an LET of 52.3 MeV-cm^2/mg. A similar comparison of SET pulse widths over temperature for the 180-nm FDSOI devices was performed as that described for the bulk devices. However, for the SOI device, the pulse-width distribution shows very little change as the temperature increases. The average measured SET pulse widths are 670 ps, 620 ps, and 620 ps at 25˚ C, 50˚ C, and 100˚ C, respectively. (Note: These averages include pulse broadening effects. The generated SET width is much smaller than the averages shown in the table. The effect of pulse broadening over temperature in this device is discussed later in this section.) As with the 90-nm and 130-nm bulk devices, the total number of SET's measured for a given ion fluence does not change with temperature. The operating temperature of the die does not affect the cross section in this technology.

Temperature	**Average SET**	**Max. SET**
25˚ C	670 ps	980 ps
50˚ C	620 ps	1050 ps
100˚ C	620 ps	1050 ps

Table 1: Average and maximum 180-nm FDSOI SET pulse width values for xenon (Effective LET=52.3 MeV-cm^2/mg) at temperatures of 25˚ C, 50˚ C, and 100˚ C.

Mixed-mode simulations for a string of inverters designed using a calibrated 180-nm FDSOI model (described in Chapter IV) were performed to further explore the effect of temperature on SET pulse width for this SOI technology. For these simulations, both the off-state pMOS and nMOS transistors of the second inverter were modeled using the same 3D-TCAD simulator used for the bulk TCAD simulations. The ion strike location was at the center of the gate (or body region) as this is the most sensitive region for these devices. The normally incident ion LET was fixed at 51 MeV-cm^2/mg (to match the LET used in the heavy ion testing), which corresponds to about 0.5 pC of deposited charge per micrometer.

The SET pulse width at the struck node for the three temperatures in the 180-nm FDSOI TCAD model is shown in Figs. 5.23 and 5.24 for the nMOS and pMOS devices, respectively. No significant trend is observed with increasing temperature in this

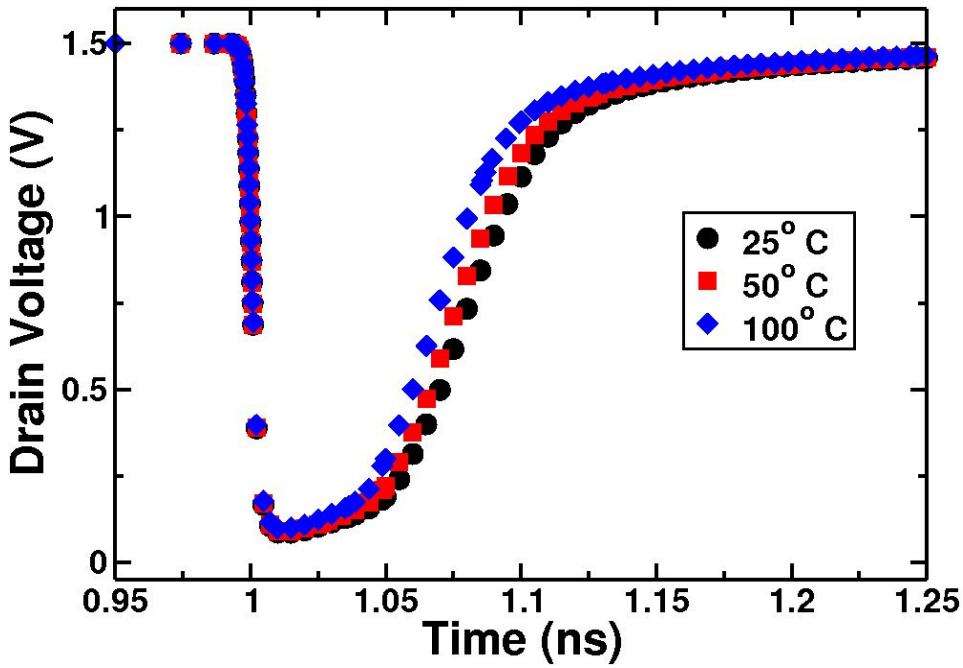

Fig. 5.23: Results of the 180-nm FDSOI mixed mode simulation for the nMOS device showing SET pulses on the struck node for 25˚ C, 50˚ C, and 100˚ C.

technology. Note that the simulated pulse-widths for the FDSOI technology are less than 100 ps, while the measured SET pulse-widths average more than 600 ps. This can be attributed to "pulse broadening", a well-known issue for floating body SOI devices as discussed in the previous chapter. Neither the experimental nor simulation results show a significant change in SET pulse width with temperature.

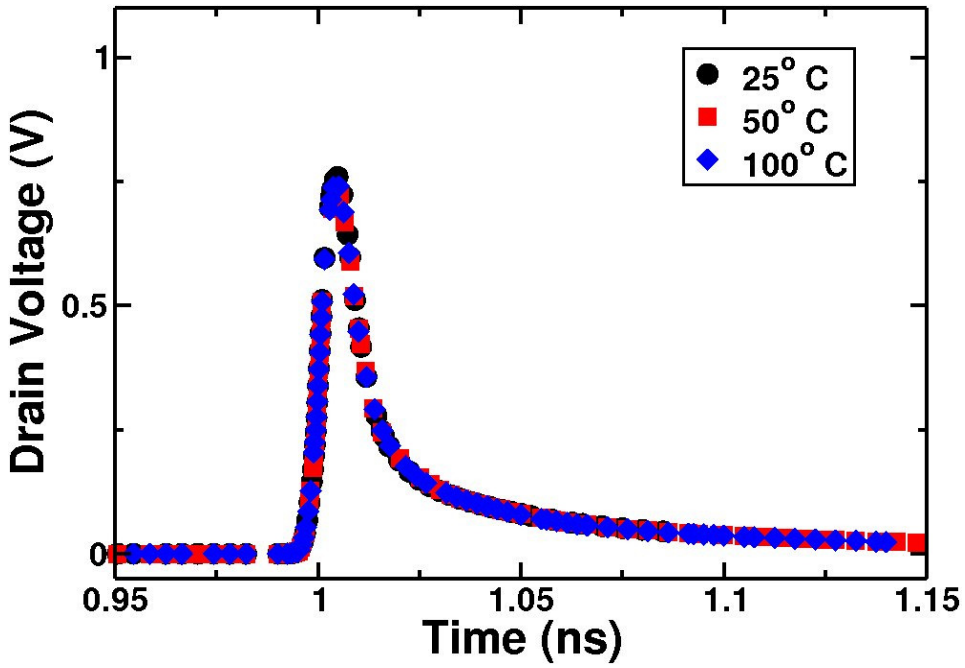

Fig. 5.24: Results of the 180-nm FDSOI mixed mode simulation for the pMOS device showing SET pulses on the struck node.

Since pulse "stretching" or "broadening" is a well-known issue for non-body tied SOI devices, an experiment was performed using the single-photon focused laser at the Naval Research lab to explore the effect of temperature on pulse broadening in this process. The test device was heated in a similar way as that used during the heavy ion testing. Using the focused laser pulse, nMOS transistors in the inverter chain were struck with the laser in different locations in the target circuit. Fig. 5.25 shows the pulse width as a

function of laser strike location for three different temperatures. The pulse width plotted is the average pulse width of approximately 10000 laser-induced SET events. Two important items to note from this data set are (1) the generated SET pulse width did not change significantly as a function of temperature (this confirms what was observed with the heavy ion testing and the simulations), and (2) the broadening also did not change with temperature. Massengill et al. [Mass-08] showed that pulse broadening in SOI is due to a body-bias-induced threshold voltage hysteresis. These results show that this hysteresis shows no change with temperature in this FDSOI process.

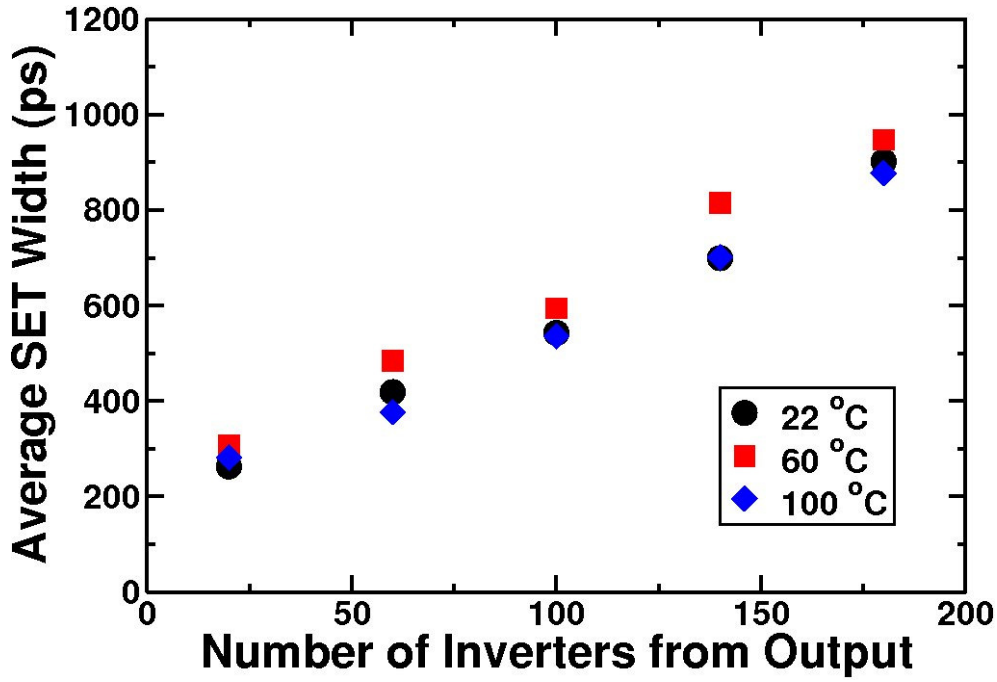

Fig. 5.25: Laser induced SET pulse width in a FDSOI process as a function of temperature.

Discussion

Drift, diffusion, and bipolar-amplification are three temperature-dependent factors affecting radiation-induced charge collection for semiconductor devices. The drift

component of charge-collection depends on mobility, which decreases with increasing temperature. However, the drift component of an SET current pulse is typically fairly short (on the order of tens of picoseconds). Thus for a SET lasting several hundred picoseconds, the drift component of charge collection does not significantly impact SET pulse-widths as temperature increases. The effect of temperature on SET pulse width through the diffusion current also tends to be negligible. Previous researchers have found the net effect of temperature on diffusion current resulting from a heavy ion strike to be small [Lair-02, Guo-04]. As a result, the increase in bipolar amplification with temperature is the main contributor to the increase in SET pulse widths seen in the bulk test circuits. Since bipolar amplification is less important for FDSOI devices than for either partially depleted or bulk devices [Ferl-02], there is no increase in SET pulse width with temperature for the FDSOI test chip.

The primary mechanism behind the parasitic bipolar mechanism in bulk CMOS devices is a change in the potential in the n-well region of the pMOS device due to an ion strike. This change in potential forward biases the source-body junction in the parasitic bipolar. The potential in the channel region of the device depends on the well-contacting scheme (as discussed in Chapter III) which in turn is a measure of how effective the contact is in being able to restore the potential in the body region after an ion strike. Changes in temperature affect this potential in two primary ways: (1) a change in temperature will cause a decrease in mobility which will increase the resistance from the well contact to the body, and (2) a change in temperature will also affect the voltage (V_{EB}) needed to forward-bias the bipolar. A description on how temperature affects the resistance is included in the final chapter, and DasGupta et al. [Dasg-07] give a detailed

description of how small potential changes can significantly impact the parasitic bipolar mechanism in bulk CMOS technologies.

In addition to the various charge collection mechanisms mentioned, another important factor affecting SET pulse widths is the drive current of the transistor that restores the struck node to its initial state. For an nMOS strike, the restoring transistor in an inverter would be the pMOS device (and vice versa for a pMOS strike). The drive strength of the restoring transistor depends on the channel mobility of the device (which decreases with increasing temperature). If the channel mobility decreases with increasing temperature, the drive strength would also decrease and cause an increase in SET widths for the same amount of generated charge. For the bulk 130-nm TCAD simulations, strikes on the nMOS device (as shown in Fig. 5.12) show almost no change in temperature. This suggests that if there is a change in drive strength of the pMOS device it's not significantly impacting the SET width. Likewise, in Figs. 5.13 and 5.14, the parasitic bipolar action is clearly shown to have a major impact on SET widths. While the nMOS drive strength may decrease slightly with increasing temperature, its impact is much smaller than the enhancement of bipolar amplification at the elevated temperatures.

To explore further how the restoring current changes with temperature, the maximum drive current for nMOS and pMOS device was simulated at different temperatures at the circuit-level for the 65-nm bulk technology. In Fig. 5.26, the drain currents for an nMOS device with a W/L ratio of 200 nm/50 nm and for a pMOS device with a W/L ratio of 400 nm/50 nm are plotted as a function of temperature. These W/L ratios correspond to the W/L ratios of the transistor in the inverter chain circuit. As can be seen, the drain current decreases with temperature, but the change from 20^{o} C to 100^{o} C is less than 6% for both

devices. These simulations show that the change in the restoring current with temperature has a small impact on SET widths compared to the enhancement in the parasitic bipolar with temperature. Simulations performed by Shuming et al. [Shum-08] in 180-nm bulk and SOI processes support the same conclusions.

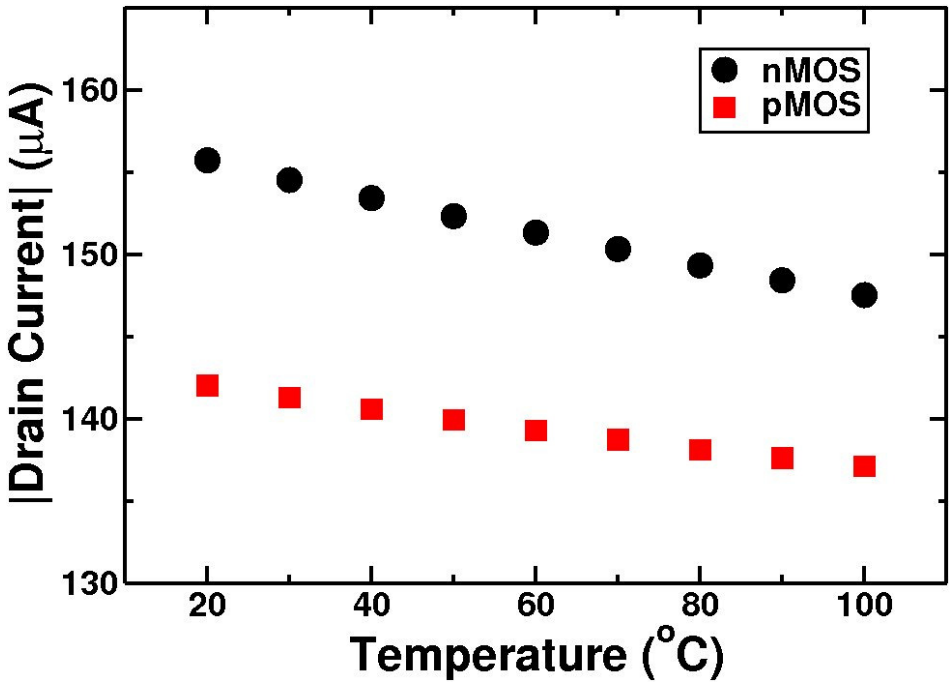

Fig. 5.26: Simulated drain current as a function of temperature for the 65-nm nMOS and pMOS devices used in the inverter chain target circuit.

Conclusions

Measurements and TCAD simulations of digital SET pulse widths show that an increase in temperature leads to an increase in SET pulse widths for the bulk processes studied here. Since mitigation approaches, and resulting error rates, are determined by the SET pulse-width distributions, an increase in SET pulse width may negate the mitigation efforts and increase error rates. This will lead to a significantly greater reliability issue for advanced technology ICs operating in high temperature environments.

Since bipolar amplification is less significant in the charge collection of the 180-nm FDSOI circuit studied in this work, SET pulse widths for our FDSOI circuit showed little change with temperature. The lack of increase in SET pulse widths with temperature is additional advantage of using a FDSOI technology in a high temperature environment where soft errors will be a concern.

CHAPTER VI

EFFECT OF TEMPERATURE ON SET PULSE WIDTHS INDUCED IN NMOS AND PMOS DEVICES

In the previous chapter, enhancement in the parasitic-bipolar action at elevated temperatures was shown to be the dominant mechanism that causes SET pulse widths to increase with temperature. In bulk CMOS processes with a p-substrate and an n-well, the simulation work has shown that the parasitic-bipolar effect is worse in pMOS transistors than in nMOS transistors, which results in larger pulse widths for SETs induced in pMOS transistors. Because of difficulties associated with SET width measurements, separate measurement of SETs induced in either pMOS transistors or nMOS transistors has not been reported before. In this chapter, SET pulse widths at elevated temperatures are measured for nMOS and pMOS transistors separately using two novel SET test circuits.

Test Structures

The unique test circuits used to experimentally differentiate between nMOS and pMOS strikes were an "N-hit" circuit and a "P-hit" circuit. Figs. 6.1 and 6.2 show a basic schematic of the "N-hit" and "P-hit" target circuits. The "N-hit" ("P-hit") target circuit consists of four chains of 100 NAND (NOR) gate/inverter blocks "OR"-ed together to form a single output. Each target circuit is followed by the 65-nm SET measurement circuit used for the previous 65-nm measurements in Chapters III and V. In both circuits, individual ion strikes on the inverters are unable to propagate through the logic chain due to logic masking. (Logic masking is a term used to describe a situation in

which a signal such as an SET is unable to propagate through a combinational logic block due to the state of the remaining logic. For example, in a two-input NAND gate, if one input is at a logic "0" the output will always be at a logic "1" no matter what the state of the other input to the gate is.) In the "N-hit" circuit stage shown in Fig. 6.1, an SET generated by an ion hit in one of the inverters will not propagate through the NAND gate and only an ion hit on an nMOS transistor in the NAND gate will propagate through the chain. All other SETs will be blocked and will not be measured. The "P-hit" target circuit works in a similar manner, with the NAND gates replaced by NOR gates.

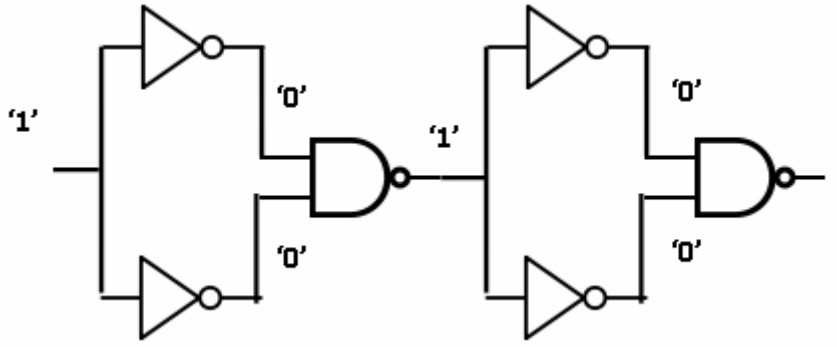

Fig. 6.1: Schematic of two of the blocks of "N-hit" target circuit. The target circuit used in this work consisted of four linear chains of 100 of these combinational logic blocks "OR"-ed together to form a single output.

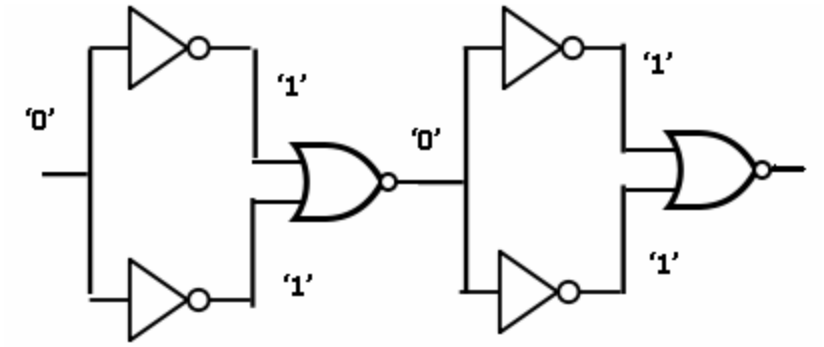

Fig. 6.2: Schematic of two of the blocks of "P-hit" target circuit. The target circuit used in this work consisted of four linear chains of 100 of these combinational logic blocks "OR"-ed together to form a single output.

One important item to take note of is the spacing of the two inverters in the "N-hit" and "P-hit" circuits. If the inverters are spaced close together in the layout, it may be possible for an ion strike to create a simultaneous SET on each inverter. If this were to happen, an SET may be able to propagate through either the NAND or the NOR gate, and as a result the circuit would no longer allow hits on nMOS or pMOS devices to be separated. To ensure that a transient was not induced on both inverters by a single ion, the inverters were placed on top and bottom of the NAND/NOR gates with a separation of 3.5 µm as shown in Fig. 6.3.

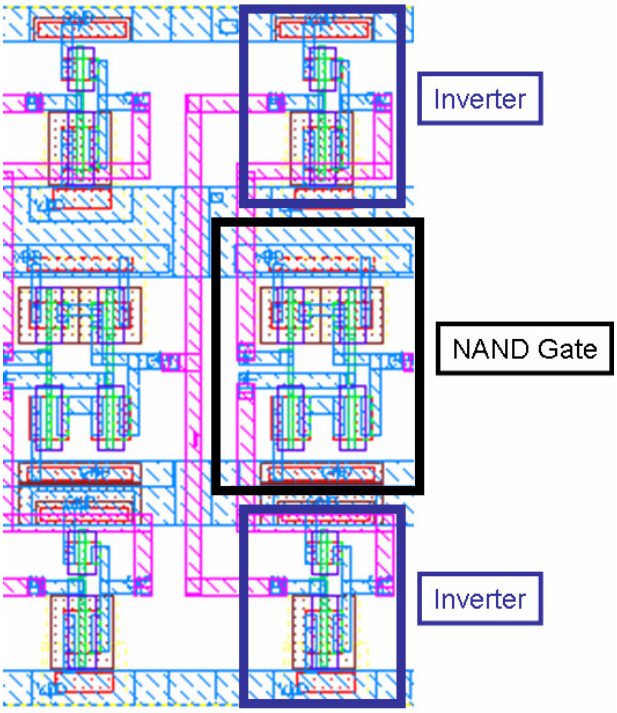

Fig. 6.3: Layout of two of the blocks of "N-hit" target circuit. The spacing between the two inverters needs to be large enough to ensure that an ion can not induce an SET on both at the same time.

Single Event Test Results

The test structures were tested with heavy ions at the Lawrence Berkeley National Lab Cyclotron facility at elevated temperature using xenon ions with an LET (linear

energy transfer) of 58.8 MeV-cm^2/mg. The temperature of the device under test (DUT) was controlled in a similar manner to the one used in Chapter V. Ion exposures were carried out at temperatures of 25°, 50°, and 100° C.

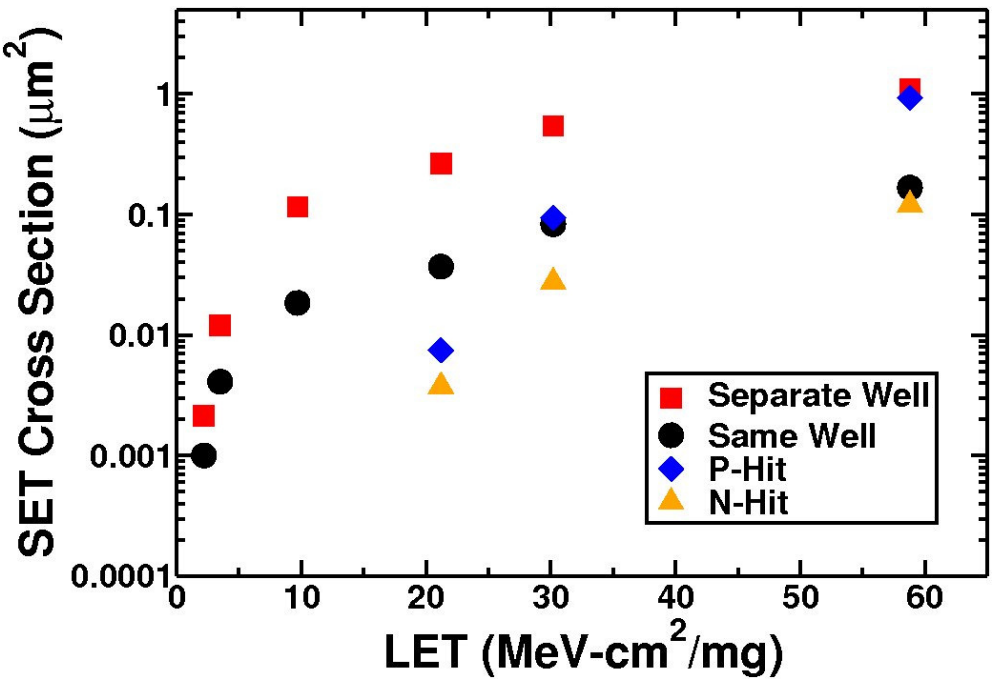

Fig. 6.4: SET cross section for the different 65-nm test structures. Note that the threshold LET for the "P-hit" and "N-hit" circuits are much larger than that for the inverter chain circuits.

For comparison purposes, the room temperature SET cross section for the inverter chain, "N-hit", and "P-hit" target circuits is shown in Fig. 6.4. The plotted SET cross section is simply the number of measured SETs divided by the total fluence of ions normalized to one logic block. For the inverter chain, the cross section is plotted per inverter, while for the "N-hit" and "P-hit" circuit the cross section is plotted per one NAND/NOR-inverter block combination. As seen in the plot, the threshold LET to create a measurable SET for the "N-hit" and "P-hit" circuits is much larger than for the inverter chain circuit. Also of note is that the cross section for the "P-hit" circuit is larger than

that of the "N-hit" circuit. One reason for this is that the size of the sensitive pMOS transistor in the "P-hit" circuit is much larger than the size of the sensitive nMOS transistor in the "N-hit" circuit. The W/L ratio of the sensitive pMOS transistor is 1.3 µm/50 nm, while the width of the sensitive nMOS transistor is 400 nm/50 nm. This means that the area of the sensitive pMOS transistor was over four times as large as the area of the sensitive nMOS transistor. As a result, the cross section for the "P-hit" circuit is almost four times as the cross section for the "N-hit" circuit.

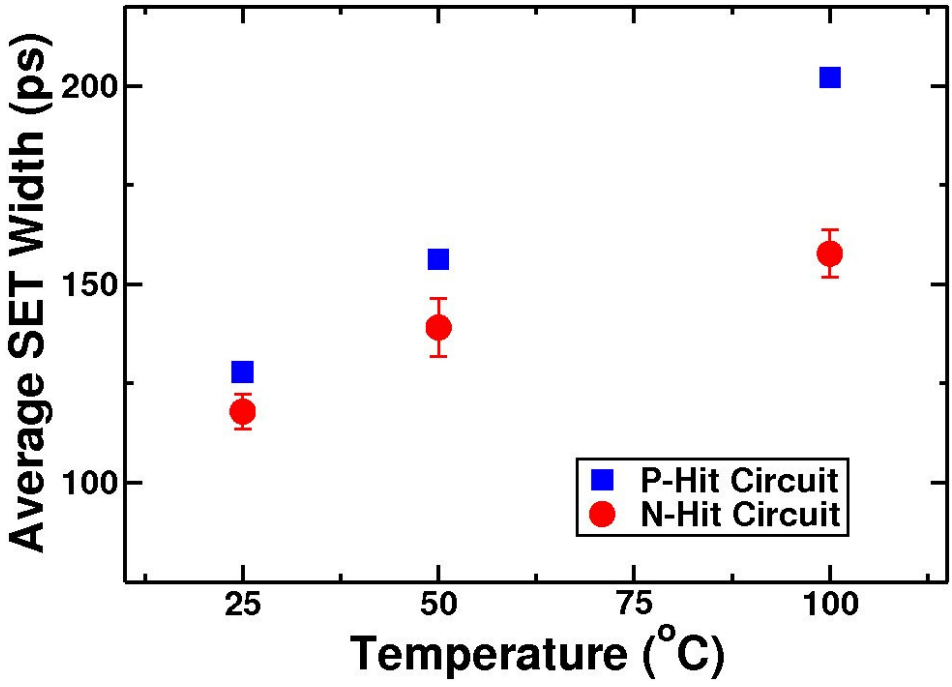

Fig. 6.5: Average SET width as a function of temperature for the "N-hit" and "P-hit" circuits.

In Fig. 6.5, the average measured SET width for the "N-hit" and "P-hit" circuit is shown. At room temperature the average SET width in the "P-hit" circuit was only slightly (~10 ps) larger than the average SET width in the "N-hit" circuit. However, the average SET width increased from 128 ps to 202 ps from 25° C to 100° C for the "P-hit"

circuit (58% increase), while the average SET width for the "N-hit" circuit increased from 118 ps to 158 ps (34% increase). The error bars for the "N-hit" data represent the standard error in the average measured width. The standard error is found by dividing the standard deviation by the square root of the number of counts.

In Figs. 6.6 and 6.7, the measured SET pulse width distributions for the "P-hit" and "N-hit" circuit are shown. Several important items to note from the histograms are: (1) the number of SETs measured for the "P-hit" circuit is about an order of magnitude larger than that for the "N-hit" circuit (this is also shown in the cross section in Fig. 6.4), (2) the shift in the SET width distribution towards longer SET widths with temperature is clear for the "P-hit" circuit, and (3) the change in SET width for the "N-hit" circuit is not quite as obvious. The changes in SET width for the "N-hit" circuit may not be apparent due to the small number of SET events measured.

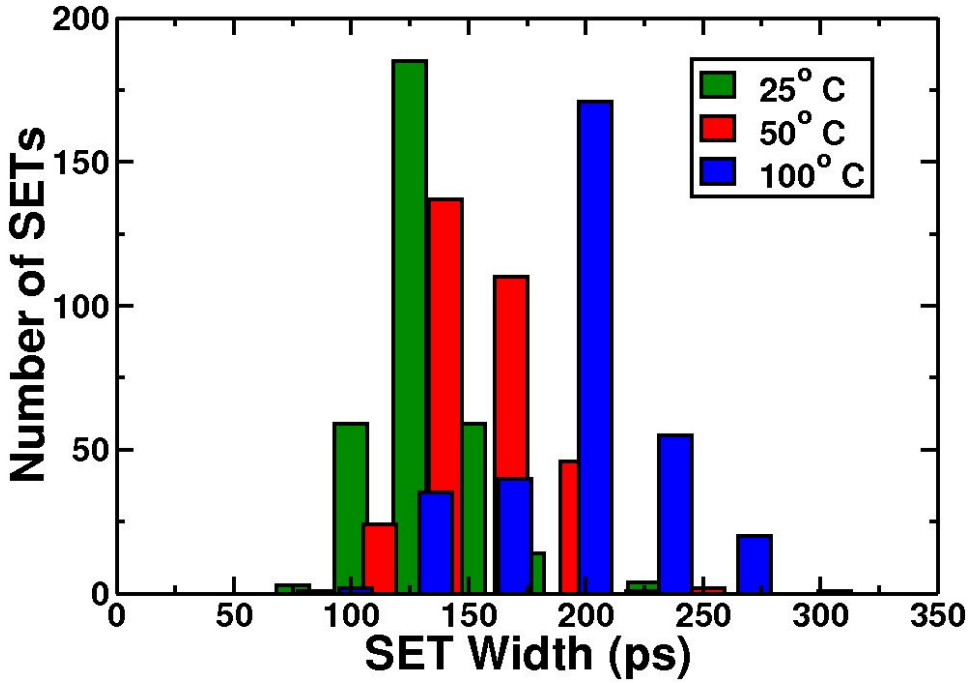

Fig. 6.6: Measured SET pulse width distribution for the "P-hit" circuit. Note that as the temperature increases the distribution clearly shifts to the longer SET widths.

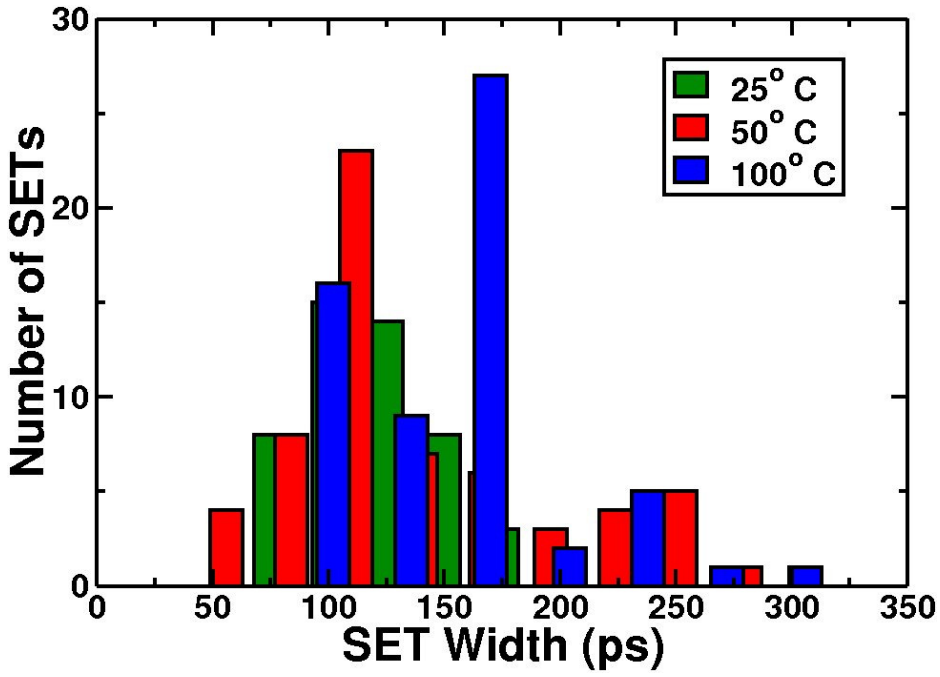

Fig. 6.7: Measured SET pulse width distribution for the "N-hit" circuit. Due primarily to the small number of SETs measured, changes in the SET width distribution are difficult to observe.

Conclusions

In this chapter, experimental measurements of heavy-ion induced single-event transient pulse widths in two unique test structures are presented at elevated temperatures. Results from unique test structures designed to separate transients from strikes on nMOS and pMOS transistors show that SET widths increase more with temperature for ion strikes on pMOS transistors than for ion strikes on nMOS transistors (58% compared to 34%). These results support the conclusions drawn in the previous chapter that showed that the predominant mechanism causing the increase in SET width with temperature was an enhancement in the parasitic bipolar device in pMOS transistors as the temperature is increased. The smaller increase in SET widths for the "N-hit" circuit with temperature could also be due to an enhancement in the parasitic NPN bipolar in the nMOS transistor. While the parasitic bipolar effect is not as pronounced for nMOS devices in twin-well CMOS processes as it is for pMOS devices [Amus-07,

Olso-07], the parasitic NPN structure is still there. Any enhancement of this bipolar device with temperature would also cause SET widths to increase in a similar manner to that of the pMOS transistor.

CHAPTER VII

CONCLUSIONS AND FUTURE RECOMMENDATIONS

Key Results and Findings

An SET measurement circuit has been used to measure SET pulse widths in four different technologies. For the first time, heavy-ion-induced SET pulse width measurements have been reported in a 65-nm bulk silicon technology and a 180-nm fully-depleted SOI technology. In addition to the room temperature measurements, some of the first-ever SET pulse width measurements over the military temperature range have been made. Along with the temperature data, simulations have been able to show that the reason for an increase in SET widths in bulk technologies with temperature is due primarily to an increase in bipolar amplification in pMOS devices. With this knowledge, unique test structures were fabricated and tested that were able to separate SETs induced in nMOS devices and pMOS devices. The elevated temperature data from these test structures confirm that temperature changes affect SETs induced in pMOS devices more than in nMOS devices.

Conclusions

SET pulse width measurements in bulk technologies depend on three factors. Due to this combination of factors, trends in SET widths with technology node have been difficult to determine. The first of these factors is pulse broadening. Pulse broadening is a term used to describe the widening of transient pulses as they propagate through a

circuit. This widening of the transient pulses can significantly affect SET measurements. In Chapter III, the broadening rate in a 90-nm SET test structure was determined through two-photon laser testing at the Naval Research Lab to be nearly 1 ps per inverter. Determination of the broadening rate helps explain why large SET widths were being measured at low LET values. Meanwhile in a 65-nm test structure the broadening rate was found through microbeam testing to be almost an order of magnitude less than in the 90-nm technology. When broadening rate is taken into account, the generated SET widths appear to be shrinking with each new technology.

Parasitic bipolar amplification is the second factor that affects SET pulse widths in bulk CMOS devices. By applying the work of Amusan et al. [Amus-07] that illustrated how the n-well contact area affected parasitic bipolar amplification to the maximum SET width data, a new graph was created that suggested that one reason for the smaller SET widths with each technology was due to the larger well-contacts used for each new test chip. This in-depth look at how parasitic bipolar amplification affects pulse widths leads one to conclude that the change in maximum SET widths with technology may have little to do with the technology itself but rather the way in which the n-well around the pMOS device is contacted.

Transistor-to-transistor spacing is last of the three factors that affect SET pulse widths. The close spacing of transistors can cause multiple devices to collect charge from a single ion with the end result being an SET width that is shorter than if only one of the devices is able to collect charge from an ion. The combined effect of all these mechanisms is that SET widths do not simply scale with technology, but rather show a significant dependence on the design of the circuit in which the measurement is made.

For silicon-on-insulator processes, generated SET widths and the rate at which SETs occur are often much smaller than in a comparable bulk process. In an SOI device, the only location a reverse biased junction exists to collect charge is under the gate. In the fully-depleted SOI structure studied in this work, pulse broadening is the main factor for the large SET widths measured. The broadening rate in the FDSOI process was much larger than the rate observed in any of the bulk processes. Another significant difference between the FDSOI structure and the bulk structures is that in the FDSOI circuits strikes on nMOS transistors create longer transients than strikes on pMOS transistors.

As the temperature increases, an increase in measured SET pulse widths is observed in all bulk technologies. The increase is attributed to an increase in parasitic bipolar enhancement in pMOS devices. The FDSOI devices show no increase in SET widths with temperature. The testing of unique "N-hit" and "P-hit" circuits provides experimental evidence that SETs induced in pMOS devices increase more with temperature than SETs induced in nMOS devices.

Future Work and Recommendations

In Chapter III, the impact the n-well contact size on maximum SET widths was discussed. With a better well contact the parasitic bipolar action is reduced and, as a result, the maximum SET widths are also reduced. In Chapters V and VI, the parasitic bipolar effect returned to be the main cause for the increase in SET widths with temperature. Following this line of reasoning, one may suspect that by better contacting the well, any increase in SET widths with temperature could be reduced. In Chapter III, in Fig. 3.10 the maximum SET width was plotted as a function of n-well contact area

percentage. The better the n-well contact, the lower the effective resistance from the n-well contact to the base of the parasitic bipolar transistor. This lowering of the resistance can also be applied to the temperature data. When the temperature increases, mobility decreases (in the temperature range of interest here), which in turn leads to an increase in resistance. With this change in resistance explaining most of the changes in data in this dissertation, the next logical step would be to try and find a way to tie it all together.

As a first attempt, one can try to plot the maximum SET widths for all the bulk technologies over all temperature ranges on the same graph. To do this, the graph would have to be plotted with the maximum SET width on the Y-axis, and some resistance factor on the X-axis. If the "N-well Contact Area Percentage" on the X-axis in Fig. 3.10 is changed to "Conductivity of the N-well", the room temperature data can be plotted in such a manner. The "Conductivity of the N-well" is a reasonable metric to use since by better contacting the n-well, the effective resistance between the n-well contact and the base of the parasitic bipolar is decreased (or equivalently the conductivity is increased). Since changes in mobility with temperature for doping levels used in fabrication processes are well known, it becomes feasible that one could adjust the conductivity

Test chip	N-well Contact Area/Total N-well Area (normalized)	Conductivity Factor at Room Temperature	Conductivity Factor at 100^{o}C (= decrease of 25% from room temperature)
130-nm	**0.0139**	**1.39**	**1.0425**
90-nm	**0.0776**	**7.76**	**5.82**
65-nm (Different well)	**0.145**	**14.5**	**10.875**
65-nm (Same Well)	**0.187**	**18.7**	**14.025**

Table 7.1: Conductivity factors used for Fig. 7.1.

factor for different temperatures by the same amount that mobility changes. For an n-doping level of 10^{17} cm^{-3} (the typical doping level of an n-well in a modern bulk technology), the electron mobility is about 800 cm^2/V-sec at 25° C, 720 cm^2/V-sec at 50° C, and 600 cm^2/V-sec at 100° C. Since the electron mobility decreases by about 25% from 25° C to 100° C, the conductivity factor for that doping level should also decrease by about 25%. The changes in doping and corresponding changes in the conductivity in the n-well are summarized in Table 7.1.

If this conversion of n-well contact area percentage to a conductivity factor is done, it becomes possible to plot almost all the maximum SET pulse width data from the bulk technologies presented in this dissertation in one concise plot. In Fig. 7.1, the maximum measured SET widths for all the bulk technologies at all the temperatures are plotted as a function of the conductivity factor of the n-well. This figure shows that all the data roughly fit a decreasing exponential curve.

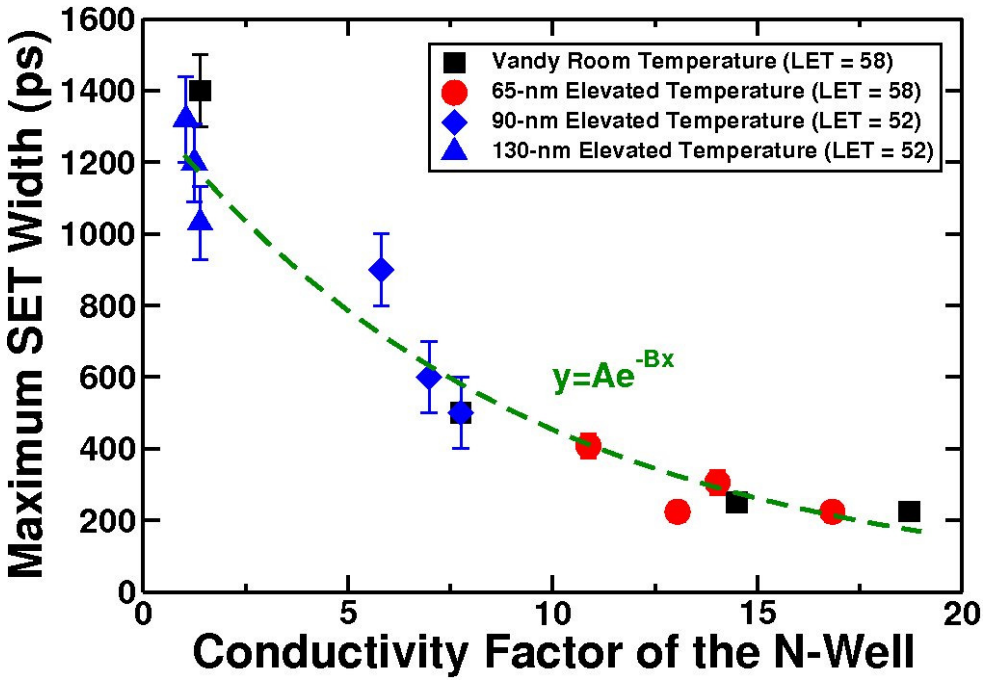

Fig. 7.1: Maximum SET width plotted as a function of the conductivity of the n-well.

While all the data fitting a single e^{-BX} curve may be nothing more than coincidence, there is some science behind it. An SET pulse width is dependent on the drain current of a struck node. If there is a parasitic bipolar that turns on during an ion strike, the drain current depends on the collector current of the parasitic bipolar. The collector current of a bipolar transistor (for a PNP) is proportional to $e^{-qV_{EB}/kt}$. V_{EB} depends on the resistance from the well contact to the base of the bipolar transistor (see Fig. 3.7). Therefore, perhaps it is not surprising that the SET widths fit an e^{-BX} curve where X is some measure of the resistance of the n-well.

The whole point of this short analysis is to suggest a new SET measurement structure. This new test circuit should have several inverter chains (with short logic paths to reduce any broadening effect) each with different n-well contact sizes. The resulting experiment should show shorter maximum SET widths with the better contact schemes. Perhaps more interesting though would be an elevated temperature test on this test structure. One would expect the best contacted n-well circuit to show less change with temperature than the circuits with the smaller well contacts. This test structure would then need to be duplicated in newer technologies, to allow one to determine experimentally true scaling trends in SET pulse widths.

REFERENCES

[Ahlb-09] J. R. Ahlbin, B. L. Bhuva, M. J. Gadlage, L.W. Massengill, B. Narasimham, and P. H. Eaton, "Single event transient pulse quenching in 130 nm CMOS logic," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3050-3056, Dec. 2009.

[Alex-03] D. R. Alexander, "Total ionizing dose effects in devices and circuits," *IEEE Trans. on Nucl. Sci.*, vol. 50, pp. 565–582, June 2003.

[Alle-92] M. L. Alles, L. W. Massengill, S. E. Kerns, K. L. Jones, J. E. Clark, and W. F. Kraus, "Effect of temperature-dependant bipolar gain distribution on SEU vulnerability of SOI CMOS SRAMS," in *Proc. IEEE 96*, 1992.

[Amus-07] O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, and J. R. Ahlbin, "Design techniques to reduce SET pulse widths in deep-submicron combinational logic," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2060-2064, Dec. 2007.

[Amus-08] O. A. Amusan, L. W. Massengill, M. P. Baze, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, and J. D. Black, "Single event upsets in deep-submicrometer technologies due to charge sharing," *IEEE Trans. Dev. and Mat. Rel.*, vol. 8, no. 3, pp. 582-589, Sept. 2008.

[Barn-05] H. Barnaby, "Total Dose Effects in Modern Integrated Circuit Technologies," *IEEE NSREC Short Course*, 2005.

[Baum-05] R. Bauman, "Single-Event Effects in Advanced CMOS Technology," *IEEE NSREC Short Course*, 2005.

[Baze-06] M. P. Baze, J. Wert, J. W. Clement, M. G. Hubert, A. Witulski, O. A. Amusan, L. Massengill, and D. McMorrow, "Propagating SET characterization technique for digital CMOS libraries," *IEEE Trans. on Nucl. Sci.*, vol. 53, no. 6, pp. 3472-3478, Dec. 2006.

[Baze-97] M. P. Baze and S. P. Buchner, "Attenuation of single event induced pulses in CMOS combinatorial logic," *IEEE Trans. on Nucl. Sci.*, vol. 44, no. 6, pp. 2217-2223, Dec. 1997.

[Bene-06] J. Benedetto, P. Eaton, D. Mavis, M. Gadlage, and T. Turflinger, "Digital single event transient trends with technology node scaling," *IEEE Trans. on Nucl. Sci.*, vol. 53, No. 6, Dec. 2006, pp. 3462-3465.

[Bind-75] D. Binder, E. C. Smith, and A. B. Holman, "Satellite anomalies from galactic cosmic rays," *IEEE Trans. Nucl. Sci.,* vol. NS-22, pp. 2675-2680, Dec. 1975.

[Buch-96] S. Buchner, D. McMorrow, J. Melinger, and A.B. Campbell, “Laboratory tests for single event effects,” *IEEE Trans. Nucl. Sci.*, vol. 43, no 2, pp. 678-686, Apr. 1996.

[Buch-97] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, “Comparison of error rates in combinatorial and sequential logic,” *IEEE Trans. on Nucl. Sci.*, vol. 44, no. 6, pp. 2209-2216, Dec. 1997.

[Chau-05] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M, Radosavljevic, “Benchmarking nanotechnology for high-performance and low-power transistor applications,” *IEEE Trans. on Nano.*, vol. 4, no. 2, pp. 153-158, Mar. 2005.

[Coli-01] J.-P. Colinge, “Silicon-on-Insulator Technology: Overview and Device Physics,” *IEEE NSREC Short Course*, 2001.

[Dasg-07] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf, and L. W. Massengill, L.W, “Effect of well and substrate potential modulation on single event pulse shape in deep submicron CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2407-2412, Dec. 2007.

[Dodd-03] P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[Dodd-04] P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, and J. R. Schwank, “Production and propagation of single-event transients in high-speed digital logic ICs,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3278-3284, Dec 2004.

[Duze-96] S. Duzellier and R. Ecoffet, “Recent trends in single event effect ground testing,” *IEEE Trans. Nucl. Sci.*, vol. 43, no.2, pp. 671-677, Apr. 1996.

[Eato-04] P. Eaton, J. Benedetto, D. Mavis, K. Avery, M. Sibley, and T. Turflinger, “Single event transient pulsewidth measurements using a variable temporal latch technique,” *IEEE Trans. Nucl. Sci.*, vol.51, no.6, pp. 3365-3368, Dec. 2004.

[Ferl-02] V. Ferlet-Cavrois, G. Gasiot, C. Marcandella, C. D'Hose, O. Flament, O. Faynot, J. du Port de Pontcharra, and C. Raynaud, "Insights on the transient response of fully and partially depleted SOI technologies under heavy-ion and dose-rate irradiations," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2948-2956, Dec. 2002.

[Ferl-06] V. Ferlet-Cavrois, P. Paillet, M. Gaillardin, D. Lambert, J. Baggio, J. R. Schwank, G. Vizkelethy, M. R. Shaneyfelt, K. Hirose, E. W. Blackmore, O.

Faynot, C. Jahan, and L. Tosti, "Statistical analysis of the charge collected in SOI and bulk devices under heavy ion and proton irradiation–implications for digital SETs," *IEEE Trans. Nucl. Sci.,* vol. 53, pp. 3242-3252, Dec. 2006.

[Ferl-06-1] V. Ferlet-Cavrois, R. Paillet, D. McMorrow, J. S. Melinger, A. B. Campbell, M. Gaillardin, O. Faynot, O. Thomas, G. Barna, and B. Giffard, "Analysis of the transient response of high performance 50-nm partially depleted SOI transistors using a laser probing technique," *IEEE Trans. Nucl. Sci.,* vol. 53, pp. 1825-1833, Aug. 2006.

[Ferl-07] V. Ferlet-Cavrois, P. Paillet, D. McMorrow, N. Fel, J. Baggio, S. Girard, O. Duhamel, J. S. Melinger, M. Gaillardin, J. R. Schwank, P. E. Dodd, M. R. Shaneyfelt, and J. A. Felix, "New insights into single event transient propagation in chains of inverters—evidence for propagation-induced pulse broadening," *IEEE Trans on Nucl, Sci.*, vol. 54, no. 6, pp. 2338-2346, Dec. 2007.

[Gadl-04] M. J. Gadlage, R. D. Schrimpf, J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Sibley, K. Avery, and T. L. Turflinger, "Single event transient pulse widths in digital microcircuits," *IEEE Trans. Nucl. Sci*, vol. 51, no. 6, pp. 3285–3290, Dec. 2004.

[Gadl-07] M. J. Gadlage, R. D. Schrimpf, B. Narasimham, B. L. Bhuva, P. H. Eaton, and J. M. Benedetto, "Effect of voltage fluctuations on the single event transient response of deep submicron digital circuits," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2495-2499, Dec. 2007.

[Glov-80] J. E. Glover, "Total ionizing dose effects in devices and circuits," *IEEE NSREC Short Course*, 1980.

[Gouk-08] P. Gouker, J. Brandt, P. Wyatt, B. Tyrrell, A. Soares, J. Knecht and C. Keast, D. McMorrow, B. Narasimham, M. Gadlage and B. Bhuva, "Generation and propagation of single event transients in 0.18 μm fully depleted SOI," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2854-2860, Dec 2008.

[Guo-04] G. Guo, T. Hirao, J. S. Laird, S. Onoda, T. Wakasa, T. Yamakawa, and T. Kamiya, "Temperature dependence of single event transient current by heavy ion microbeam on p+/n/n+ epilayer junctions," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2834-2839, Oct. 2004.

[Hsie-81] C.M. Hsieh, P. C. Murley, and R. R. O'brien "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices", IEEE Electron Device Letters, Vol. EDL-2, no. 4, pp. 103, April, 1981.

[John-00] A.H. Johnston, "Scaling and Technology Issues for Soft Error Rates", *IEEE Res. Conf. Rel. Proc.*, Oct. 2000.

[Kaul-91] N. Kaul, B. L. Bhuva, and S. E. Kerns, "Simulation of SEU transients in CMOS ICs," *IEEE Trans. Nucl. Sci*, vol. 38, no. 6, pp. 1514–1520, Dec. 1991.

[Kilb-63] J. Kilby, "Miniature Semiconductor Integrated Circuit", U.S. Patent 3,115,581, filed May 1959, issued December 1963.

[Lair-02] J. Laird, T. Hirao, S. Onoda, H. Mori, and H. Itoh, "Temperature dependence of heavy ion-induced current transients in Si epilayer devices," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 1389–1395, Jun. 2002.

[Lera-99] J-L. Leray, "Total Dose Effects: Modeling for present and future," *IEEE NSREC Short Course*, 1999.

[Maki-09] T. Makino, D. Kobayashi, K. Hirose, Y. Yanagawa, H. Saito, H. Ikeda, D. Takahashi, S. Ishii, M. Kusano, S. Onoda, T. Hirao, and T. Ohshima, "LET dependence of single event transient pulse-widths in SOI logic cell," *IEEE Trans. Nucl. Sci.*, vol. 56, pp. 202-207, Feb. 2009.

[Mass-93] L. W. Massengill, "SEU Modeling and Prediction Techniques," *IEEE NSREC Short Course*, 1993.

[Mass-00] L. W. Massengill, A. E. Baranski, D. O. Van Nort, J. Meng and B. L. Bhuva, "Analysis of single-event effects in combinational logic - simulation of the AM2901 bitslice processor," *IEEE Trans. Nucl. Sci.*, p. 2609, 2000.

[Mass-08] L. W. Massengill and P. W. Tuinenga, "Single-event transient pulse propagation in digital CMOS," *IEEE Trans. Nucl. Sci.*, vol.55, no.6, pp. 2861-2871, Dec. 2008.

[Mavi-02] D. G. Mavis and P. H. Eaton, "Soft error mitigation techniques for modern microcircuits," *Reliability Physics Symposium Proceedings, 2002. 40th Annual*, pp. 216-225, 2002.

[May-78] T. C. May and M. H. Woods, "A new physical mechanism for soft errors in dynamic memories," in *Reliability Physics Symp.* vol. 16, IEEE, 1978, pp. 33-40.

[May-79] T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. Electron Devices,* vol. ED-26, pp. 2-9, Jan. 1979.

[McMo-02] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci.,* vol. 49, pp. 3002-3008, Dec. 2002.

[McNu-90] P. McNulty, "Predicting Single Event Phenomena in Space," *IEEE NSREC Short Course*, 1990.

[Moor-65] G. E. Moore, "Cramming More Circuits on Chips," *Electronics*, vol. 38, no. 8, April 1965, also reprinted as "Cramming More Components Onto Integrated Circuits," *Proc. IEEE*, vol. 86, no. 1, pp. 82-85, Jan. 1998.

[Muss-01] O. Musseau and V. Ferlet-Cavrois, "Silicon-on-Insulator Technologies: Radiation Effects," *IEEE NSREC Short Course*, 2001.

[Nara-06] B. Narasimham, V. Ramachandran, B. L. Bhuva, R. D. Schrimpf, A. F. Witulski, W. T. Holman, L. W. Massengill, J. D. Black, W. H. Robinson, D. McMorrow, "On-chip characterization of single event transient pulse widths," *IEEE Trans. on Dev. and Mat. Rel.,* vol. 6, pp. 542-549, 2006.

[Nara-07] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, O. A. Amusan, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, J. M. Benedetto, and P. H. Eaton, "Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2506-2511, Dec. 2007.

[Nara-08] B. Narasimham, "Characterization of Heavy-Ion, Neutron and Alpha-Particle-Induced Single-Event Transient Pulse Widths in Advanced CMOS Technologies," Ph.D. Dissertation, 2008.

[Nara-08-1] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, O. A. Amusan, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, J. M. Benedetto, and P. H. Eaton, "Effects of guard bands and well contacts in mitigating long SETs in advanced CMOS processes," *IEEE Trans. Nucl. Sci.*, vol. 55, no.3, pp. 1708-1713, June 2008.

[Oldh-03] T. R. Oldham and F. B. Mclean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. on Nucl. Sci.*, vol. 50, pp. 483–499, June 2003.

[Olso-05] B. D. Olson, D. R. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. Doyle, and D. McMorrow, "Simultaneous Single Event Charge Sharing and Parasitic Bipolar Conduction in a Highly-Scaled SRAM Design," *IEEE Trans. on Nucl. Sci.*, vol. 52, pp. 2132-2136, Dec. 2005.

[Olso-07] B. D. Olson, O. A. Amusan, S. DasGupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, and D. R. Ball, "Analysis of parasitic PNP bipolar transistor mitigation using well contacts in 130 nm and 90 nm CMOS technology," *IEEE Trans. Nucl. Sci*, vol. 54, no. 4, pp. 894-897, Aug. 2007.

[Ooka-97] H. I. T. Ooka, "Temperature dependence of single-event charge collection in SOI MOSFET's by simulation approach," *IEEE Trans. Electron Devices*, vol. E80-C, no. 3, p. 417, Mar. 1997.

[Pell-08] J. A. Pellish, R. A. Reed, N. D. Pate, D. McMorrow, J. S. Melinger, J. A. Kozub, P. W. Marshall, A. K. Sutton, R. M. Diestelhorst, S. Phillips, J. D. Cressler, R. A. Weller, R. D. Schrimpf, A. D. Tipton, and G. F. Niu, "Radiation-induced current transients in SiGe HBTs," *IEEE Trans. Nucl. Sci.,* vol. 55, pp. 2936-2942, Dec. 2008.

[Pete-83] E. Peterson, "Single Event Upset in Space: Basic Concepts," *IEEE NSREC Short Course*, 1983.

[Pick-79] J.C. Pickel and J.T. Blandford, "Cosmic Ray Induced Errors in MOS Memory Cells," *IEEE Trans. Nucl. Sci*., NS-25, p. 1166, 1978.

[Pick-83] J. Pickel, "Single Event Mechanisms and Predictions," *IEEE NSREC Short Course*, 1983.

[Rama-08] V. Ramachandran, M. L. Alles, R. A. Reed, J. D. Black, J. A. Pellish, and D. G. Walker, "In-situ Cryogenic SEE Testing of High-Speed SiGe BiCMOS Devices", presented at the 6th International Planetary Probe Workshop, June 2008, Atlanta, Georgia, USA.

[Reed-96] R. A. Reed, M. A. Carts, P. W. Marshall, C. J. Marshall, S. Buchner, M. LaMacchia, B. Mathes, and D. McMorrow, "Single event upset cross sections at various data rates," *IEEE Trans. Nucl. Sci*., p. 2862, 1996.

[Rodb-07] K.P. Rodbell, D.F. Heidel, H.H Tang, M.S. Gordon, P. Oldiges, and C.E. Murray, "Low-energy proton-induced single-event-upsets in 65 nm node, silicon-on-insulator, latches and memory cells," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2474-2479, Dec. 2007.

[Schw-02] J. Schwank, "Total Dose Effects in MOS devices," *IEEE NSREC Short Course*, 2002.

[Sext-92] F. Sexton, "Measurement of Single Event Phenomena in Devices and ICs," *IEEE NSREC Short Course*, 1992.

[Shiv-02] Shivakumar, P.; Kistler, M.; Keckler, S.W.; Burger, D.; Alvisi, L., "Modeling the effect of technology trends on the soft error rate of combinational logic," *Dependable Systems and Networks, 2002. DSN 2002. Proceedings. International Conference on*, vol., no., pp. 389-398, 2002.

[Shum-08] C. Shuming, L. Bin, L. Biwei, and L. Zheng, "Temperature dependence of digital SET pulse width in bulk and SOI technologies," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2914-2920, Dec. 2008.

[Srou-88] J. R. Srour, "Displacement damage effects in electronic materials, devices, and integrated circuits," *IEEE NSREC Short Course*, 1988.

[Summ-92] G. P. Summers, "Displacement damage: mechanisms and measurements," *IEEE NSREC Short Course*, 1992.

[Xaps-06] M. Xapsos, "Modeling the Space Radiation Environment," *IEEE NSREC Short Course*, 2006.