Fabrication, Characterization, and Applications of Porous Silicon Metal-Oxide Nanocomposites

By

Joshua S. Fain

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Approved:

Sharon M. Weiss, Ph.D.

Cary L. Pint, Ph.D.

Ronald D. Schrimpf, Ph.D.

Robert A. Reed, Ph.D.

Ya-Qiong Xu, Ph.D.

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CHAPTER 1

INTRODUCTION

Presented in this dissertation are the investigations of multiple and diverse applications of a nanocomposite materials system composed of porous silicon (pSi) and transition metal oxides (TMOs). The pSi is taken to serve two main functions: 1) to confine the growth of the TMO to the nanoscale regime and 2) to play an active role in device performance. The pSi films utilized in this dissertation are formed by electrochemical etching of crystalline Si (cSi) wafers, resulting in the formation of vertically aligned nanoscale pores embedded within the cSi substrates. The TMOs used throughout this body of work are nickel oxide (NiO) and titanium dioxide (TiO_2), both of which are formed by thermal decomposition of solution-derived precursors which are previously deposited into the pSi pores. The primary application areas discussed here include nanoparticle synthesis, variable conductivity devices, and electrochemical energy-storage.

1.1 Porous Si

pSi is a versatile, high-surface area material with applications in optics,[1, 2] energy,[3-5] sensing,[2, 6-9] and biology.[10, 11] It is characterized by the presence of numerous void spaces, or pores, present on a Si surface. These pores can range in size from nanometers to microns in diameter which in turn will directly impact the optical, chemical, mechanical, and electrical properties. Some methods for forming pSi include anodic etching, stain etching, metal assisted chemical etching (MACE), and magnesiothermic reduction of silicates.[12] Depending on the fabrication technique employed, the pores may exhibit a high degree of order and uniformity in size and morphology or they may show wide variability in these features.

In the work presented in this dissertation, all pSi is derived by anodic etching which is an electrochemical technique performed directly on a crystalline Si (cSi) substrate. Anodic etching is a relatively simple process that allows for a high degree of control over the final pore size and depth through simple setting of the etch parameters (current, etch duration, electrolyte concentration, Si type). The result is the formation of aligned cylindrical pores embedded within a Si substrate that are similar in morphology, length, and size. Using this method, a wide range of pore sizes (~1nm to >1μm) and surface areas (~100 to ~900m^2/cm^3) are possible.[10, 13] **Figure 1.1** provides SEM cross-section images of pSi with widely varying pore sizes.

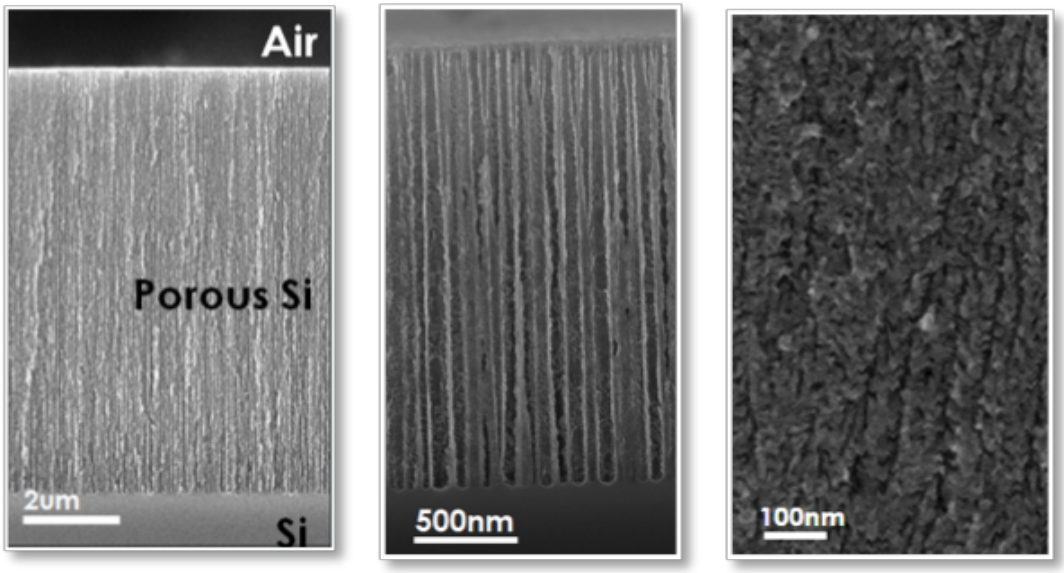

Figure 1. 1 Cross-section SEM images of pSi with different pore diameters dictated by the etching conditions. The left and middle images show the full pSi layers with pSi/Si interface at the bottom with cross-section pore sizes of about 40 and 100nm respectively. The right image is a close-up of a cross-section region of a pSi film with very small pores (<10nm diameter).

The process of anodic etching of Si takes place in an etch cell as depicted in **Figure 1.2**. In the figure, a Si wafer is placed on top of an Al-backplate which serves as an electrical contact between the Si and the positive terminal of the power supply. An electrolyte container constructed

of polytetrafluoroethylene (PTFE) is placed on top of the Si and filled with a hydrofluoric acid (HF) electrolyte. An opening in the bottom of the container allows contact between the electrolyte and the Si surface. A Pt counter-electrode is also submerged in the electrolyte solution and connected to the negative terminal to complete the circuit.

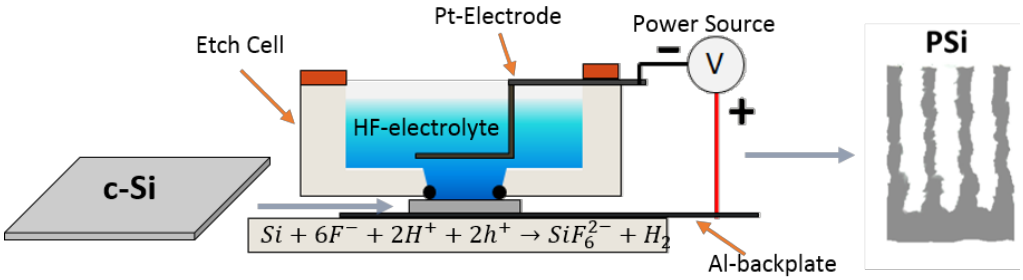

Figure 1. 2 Schematic depiction of the pSi etching set-up.

Applying a positive bias to Si (w.r.t. the Pt-electrode) will cause valence band holes (h^+) to migrate towards the Si/HF interface. The arrival of h^+ to Si surface atoms will allow F^- ions to penetrate an otherwise passivating hydride surface layer and bond to associated Si surface atoms. The Si—F bond is highly polar due to a significant difference in electronegativities: 1.90 and 3.98 for Si and F, respectively. Thus, once an initial Si—F bond is established rapid nucleophilic attack of the Si surface atom by additional F^- ions takes place, liberating the Si atom from the bulk.

There are two primary regimes for the corrosion of Si via anodic etching: *electropolishing* and *pore formation*. Electropolishing occurs at high bias when the arrival of F^- ions to the Si surface is slow compared to the arrival of the h^+. This occurs at high currents and/or low electrolyte concentrations. To compensate for the lack of F^-, the Si will oxidize and form an oxide layer which is easily removed in solutions of HF. If a pSi layer has been previously formed then electropolishing can be used to producing free-standing pSi films.

In the pore formation regime, F^- diffusion to the Si surface keeps pace with the arrival of h^+ and the corrosion process follows the half-reaction in **Equation 1.1** to form cylindrical voids in the Si surface.

$$Si + 6F^- + 2H^+ + 2h^+ \rightarrow SiF_6^{2-} + H_2 \quad 1.1$$

The role of H in the process is to provide a passivation layer on the Si surface which prevents removal of Si by F^- unless a positive bias is applied. This passivation layer occurs automatically in the electrolyte while no bias is applied. When bias is applied, the competing mechanism of etching and passivation causes pore formation and is largely responsible for the resulting pore morphology. The discussion presented above is only meant to provide some initial insight into the anodic pSi formation mechanism. For a more rigorous treatment, including the role of the passivation layer, as well as the dependence on bias, electrolyte concentration, Si type and doping concentration, and crystal-face dependence, the reader is referred to Sailor[14] and Canham.[12]

1.2. Transition-metal oxides

Oxides of the transition metals, elements with partially filled d-orbitals, are a diverse class of materials and include semiconductors (TiO_2, WO_3), insulators (NiO, MnO, CoO), conductors (TiO, VO, RuO_2), superconductors ($YBa_2Cu_3O_7$, $La_{2-x}Sr_xCuO_4$), as well as materials that exhibit metal-insulator-transitions (VO_2, Ti_2O_3, NbO_2). In addition to the electronic properties they also include ferromagnetic (CrO_2, $SrRuO_3$) and antiferromagnetic (NiO, MnO) materials, piezoelectrics ($PbZr_xTi_{1-x}O_3$), materials that exhibit giant magnetoresistance ($La_{1-x}Sr_xMnO_3$), and catalytic, chemiresistive, and electrochemically active materials ($LiCoO_2$, LiMnNiCoO, NiO, MnO_2, RuO_2, ZrO_2, TiO_2).[15] These materials have been implemented for a variety of applications such as Li-ion battery electrodes,[16, 17] pseudocapacitor electrodes,[18-21] sensors,[22-24] catalysis,[25, 26] photovoltaics,[27, 28] superconductors,[29] resistive memory,[30-34] optical modulators,[35] and

piezoelectric actuators.[34, 36, 37] Much focus in fabrication of transition-metal oxides (TMOs) is in their development at the nanoscale, as materials in this regime can exhibit properties that deviate from their bulk counterparts and provide a method of tuning device properties and opening up new application spaces. For instance, nearly all resistive memory devices are based on ion conduction, and only at the nanoscale are ion migration time scales usable for practical devices.[34] Another instance for nanoscale applications of TMOs is when charge-transfer across an interface is a fundamental process for device operation – batteries, pseudocapacitors, chemical and gas sensors. For such devices, increasing the surface area through nanostructuring can have a direct impact on device performance.[37-39]

Nickel Oxide

Nickel oxide (NiO) is the primary TMO used throughout this dissertation. In bulk, NiO is a wide bandgap ($E_g \approx 4.0$eV) material.[40] Stoichiometric NiO is insulating, but exhibits intrinsic p-type conductivity through the introduction of Ni-vacancies.[41] At the nanoscale, electronic and ionic conduction of NiO as well as its active surface area can be enhanced over that of bulk NiO, and in the last few decades, nanostructured forms have been investigated for applications such as battery and supercapacitor electrodes,[18, 42-46] chemical and gas sensors,[47-49] catalysis,[50] electrochromic thin-films,[51, 52] and resistive memory devices.[53-55]

A number of conventional fabrication methods for deriving metal oxides have also been employed to form NiO nanomaterials. These can largely be divided into physical or chemical methods. Physical methods are considered those that employ a vapor/gas phase to directly deposit and/or form NiO. Since NiO is the direct product of these processes a final heat-treatment step is not required to form NiO, as is typical of the chemical methods. Nonetheless, a heat-treatment step is often performed to improve crystallinity and/or sinter the product. The physical processes include methods such as sputtering,[56] metal-organic chemical vapor deposition (MOCVD),[55, 57, 58]

laser ablation,[59, 60] and thermal evaporation.[61] For nanomaterials, these methods can usually be implemented to result in the formation of highly controllable, high-purity, nanocrystalline thin-films. The disadvantage of these methods is that system complexity and the need for precision equipment can become cost prohibitive.

Chemical routes on the other hand are more cost-effective than the physical methods. These are also more amenable to producing a wider variety of dispersible nanostructures as well as thin-films. To a large extent, the various chemical methods follow similar steps for deriving NiO materials which includes 1) preparation of a solution, 2) precursor formation from the solution, and 3) thermal decomposition of the precursor to form NiO. Various methods have been used to prepare and/or deposit the solution/precursor which includes sol-gel,[62-64] solvo-thermal,[50, 65] precipitation,[66] electrochemical deposition,[18] spray-pyrolysis,[67] spin-coating,[64] and dip-coating/chemical bath deposition.[56, 64] Nearly all of the chemical-based methods require a final heat-treatment step to form NiO, and so regardless of the particular chosen route, these methods can collectively be classified as thermal decomposition methods.[68-72] The choice of temperature for the thermal decomposition step will have a direct impact on the final NiO product. A minimum temperature of 250ºC to 300ºC is usually required to form NiO from its precursor, but a general rule is that higher quality, low defect, sintered crystals are produced at higher temperatures while the smallest nanoparticles are produced at lower temperatures.

1.3 Initial discussion of NiO preparation method used throughout this work

In this dissertation, NiO is derived by thermal decomposition of a Ni-acetate precursor. This section provides some initial studies and discussion on the development of this precursor and the formation of NiO. Throughout the work presented in this dissertation, the NiO precursor is developed by dissolving Ni-acetate tetrahydrate (NAT) into 2-methoxyethanol (2MOE) resulting in the formation of a green solution. **Figure 1.3**a shows this solution when 1g of NAT has been

dissolved in 20mL of 2MOE (50mg/mL). The initial NAT was dissolved by adding it to the 2MOE and heating the mixture on a hot-plate set at 60ºC for 1hour while stirring with a magnetic stir bar at 300RPM. Allowing the solution to dry at room temperature results in the whitish green precipitate in **Figure 1.3**b. This precipitate appears identical in color to the initial NAT (not pictured) prior to its being dissolved in 2MOE.

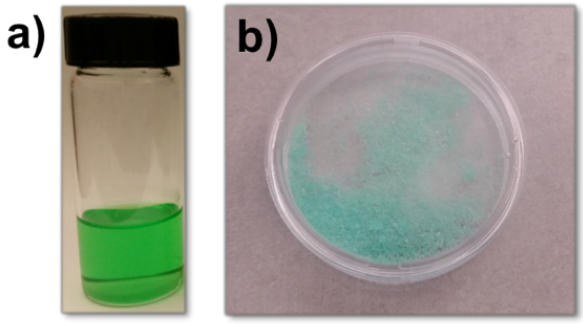

Figure 1. 3 (**a**) NiO precursor solution prepared by dissolving 1g of NAT in 20mL of 2MOE. (**b**) the remaining precipitate after allowing the solution in (a) to dry in air at RT.

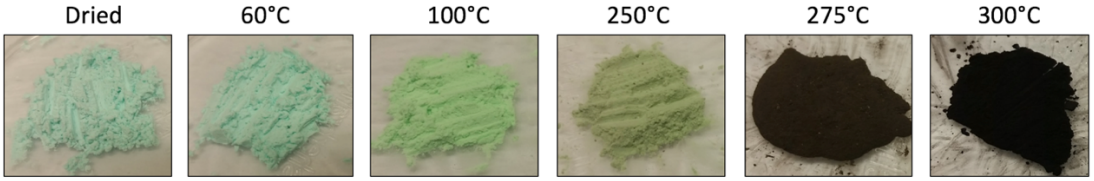

Figure 1. 4 powders of the precursor heated to the indicated temperatures.

A series of powders were prepared by pulverizing the precipitate from a solution of the precursor in a mortar and pestle. These powders were then heated to various temperatures up to 300ºC (**Figure 1.4**). In the figure, the *Dried* powder was just the pulverized precipitate without any heating. The 60ºC powder was prepared by heating the *Dried* powder to 60ºC on a hot-plate for 1hr in air. There appears to be almost no visible difference in the *Dried* and 60ºC powders. At temperatures of 100ºC to 300ºC the samples were heated to their respective temperatures in a

furnace for 6hrs in air. At 100ºC the powder is a vibrant green color, while at 250ºC the powder is a darker, yellowish green. At 275ºC and 300ºC the powders appear in the image to be black but upon close inspection they were actually a very dark green.

These samples were all investigated by XRD on a Rigaku Smart Lab XRD system using a Cu-Kα source with λ = 1.54058Å (**Figures 1.5** and **1.6**). The XRD spectra from the *Dried* powder (red) and 60ºC powder (green) from **Figure 1.4** along with a spectra from the NAT, prior to dissolving in 2MOE, are shown in **Figure 1.5**. All spectra in **Figure 1.5** are nearly identical indicating that the precipitate is in fact just recrystallized NAT. **Figure 1.6** shows the XRD spectra collected from the powder samples in **Figure 1.4** heated from 100ºC to 300ºC. From the powder heated to 100ºC there is a complete loss in the NAT crystal structure with very broad peaks located at ~25º, 40º, and 60º - 2theta. At 250ºC a similar XRD pattern is still observed but there does appear to emerge small NiO (111) and (200) peaks (ICDD 47-1049). These peaks are expected to form for NiO in the NaCl crystal structure. Heating at 275ºC, these and additional NiO peaks [(220), (311), and (222)] are clearly present, and at 300ºC they become even more prominent.

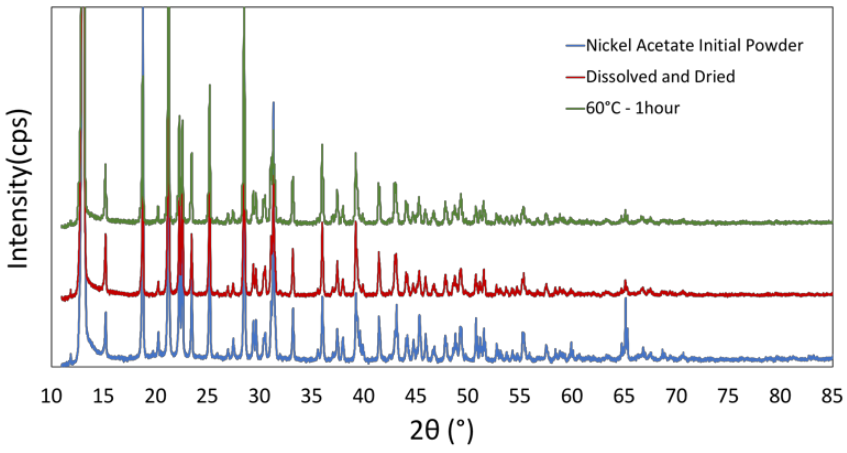

Figure 1. 5 XRD spectra collected from NAT powders before dissolving in 2MOE (blue), after dissolving in 2MOE and recrystallizing once solvent is evaporated at room temperature (red), and after heating the recrystallized powder to 60ºC for 1hour (green). The red and green spectra are from the Dried and 60ºC powders shown in Figure 1.4.

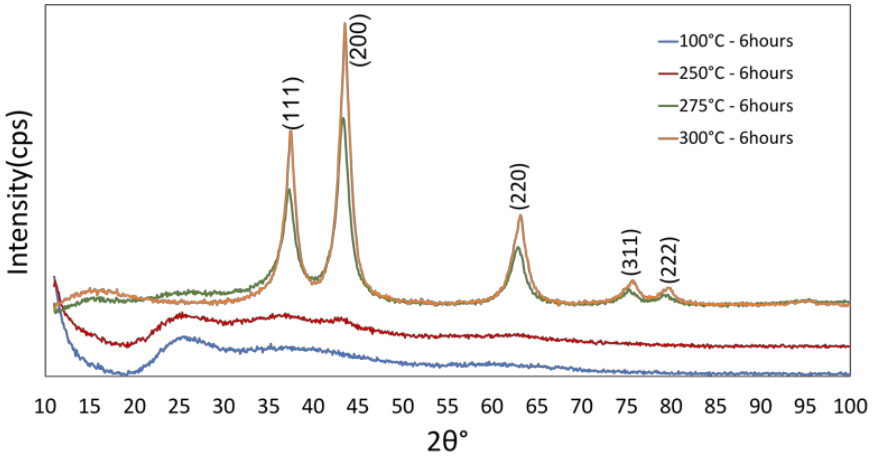

Figure 1. 6 XRD spectra of the powders from Figure 1.4 heated to temperatures of 100ºC to 300ºC. The labelled peaks correspond to NiO lattice planes in the NaCl crystal structure.

Figure 1.7 shows the results of thermogravimetric analysis (TGA) of NAT powder heated in air up to 400ºC at a ramp rate of 5ºC/min. The first mass loss step of 26.5% begins at temperatures just above 60ºC and is mostly complete by 100ºC. This mass loss is likely attributed to the dehydration of NAT, resulting anhydrous Ni-acetate.[73] Comparing to the XRD spectra, this is associated with the loss of a well-defined crystal structure at 100ºC. The subsequent gradual mass loss of 7.5% may be due to continued evaporation of residual H_2O. The 26% and subsequent 8.3% mass loss steps are associated with the formation of NiO and the removal of the remaining precursor constituents. A total remaining mass of 31.7% of the original mass is near the ideal 30% expected for the formation of NiO from NAT. From the XRD and TGA data it is concluded that dissolving NAT in 2MOE will result in the reformation of NAT when the solvent is evaporated at room temperature and that formation of NiO will begin to occur between 250ºC and 300ºC.

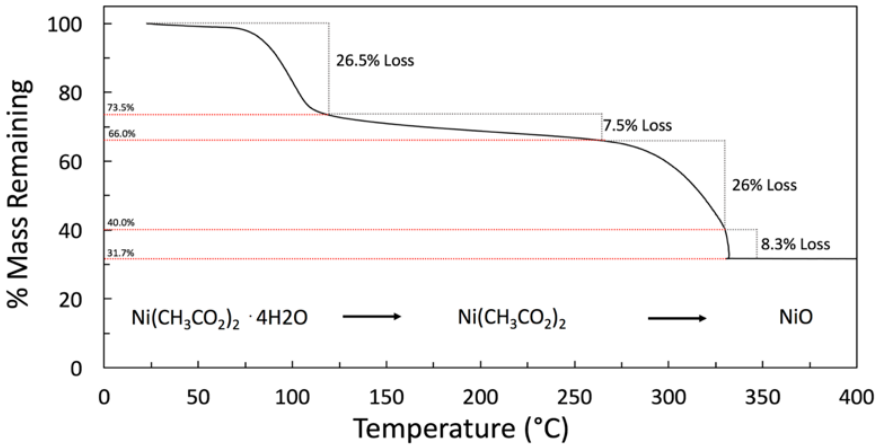

Figure 1. 7 TGA curve of nickel acetate tetrathydrate powder showing the calculated percent mass loss steps along with the likely remaining chemical constituents.

1.4 Methods

The following is a brief description of some of the techniques used for characterization and analysis in the subsequent chapters of this dissertation.

Porosity measurement by effective medium approximation

Porosity (P) of a porous material is the ratio of the total pore volume (V_p) to the total volume (V_T). In the work here, the porosity of pSi is determined by an effective medium approximation. The method is based on the fact that the effective refractive index of the pSi (n_{pSi}) layer is due to the refractive index of the relative amounts of the individual constituent materials (Si and air). Air is assumed to fill the void spaces (pores). According to the Bruggeman effective medium model, a layer containing two constituent components is related to the refractive index of each of the components by **Equation 1.2**.[14]

$$P\left[\frac{n_{air}^2 - n_{pSi}^2}{n_{air}^2 + 2n_{pSi}^2}\right] + (1-P)\left[\frac{n_{Si}^2 - n_{pSi}^2}{n_{Si}^2 + 2n_{pSi}^2}\right] = 0 \qquad 1.2$$

$n_{air} \approx 1$ and $n_{Si} \approx 3.8$ for wavelengths used in measurements here.[14] n_{pSi} is found by experiment.

n_{pSi} of a single-layer pSi film is easily determined by thin-film reflectance measurements. This method employs a white light source and detector situated normal to the surface. Fringes are produced in the reflectance spectrum due to the interference of light reflecting from the pSi surface and the pSi/Si interface. The condition for constructive interference is given by **Equation 1.3**.

$$m\lambda = 2n_{pSi}L \qquad 1.3$$

m is an integer that represents the spectral order of the peak/fringe, λ is the optical wavelength at the fringe maxima and *L* is the thickness of the pSi layer. The factor *2* arises because the path of the beam reflected off the pSi/Si interface travels a distance of *2L* in the pSi layer. According to **Equation 1.3**, the reflectance fringe maxima will be periodic in 1/λ [cm^{-1}]. The value of $2n_{pSi}L$ can be determined from the slope of the line from a plot of *m* vs. 1/λ or by performing an FFT on the spectra after replotting vs. 1/λ. From $2n_{pSi}L$, n_{pSi} can be determined once *L* has been measured. For additional details on this technique to determine pSi porosity see Sailor.[14]

X-ray diffraction

X-ray diffraction (XRD) is one of the most common techniques implemented in materials analysis for determining the crystal structure of a material. It is also commonly used for estimating the size of nanocrystals via the well-known Scherrer's equation. In a simple Bragg-Brentano XRD system, an X-ray beam of constant wavelength is emitted from a source over a range of angles. The beam is incident upon, and reflects off of a sample while a detector is also present. The detector follows the position of the reflected beam, and when the incident/reflection angle corresponds to a Bragg angle, a peak is detected in the intensity of the beam.

The simple explanation for the presence of these peaks is usually described by considering two lattice planes to be reflecting planes separated a distance *d* apart. In this case, a monochromatic x-ray beam incident on each surface will partially reflect off each plane at the

same angle. The reflected beams will constructively interfere when the total path difference between them is equal to an integer multiple (n) of the wavelength (λ) of the incident beam. This condition for constructive interference is given by the Bragg equation (**Equation 1.4**) where θ_B is denoted as the Bragg reflection angle.

$$n\lambda = 2dSin(\theta_B) \qquad 1.4$$

Similarly, the condition for destructive interference between two planes, when the reflected beams are 180º out of phase, is given by **Equation 1.5.**

$$(n + \frac{1}{2})\lambda = 2dSin(\theta_d) \qquad 1.5$$

Where θ_d is the angle of destructive interference.

If the Bragg condition is satisfied for any two adjacent planes in a family of planes, then it is valid for all planes in that family, since the path difference between all reflected beams will be some integer multiple of λ. Therefore, the intensity of the resulting Bragg peak will, to first order, be proportional to the number of reflecting planes. This situation however, is not true for any other angle. In fact, as the number of planes increases, then the range of angles at which destructive interference occurs will increase as well, and reduce the width of the Bragg peaks. This idea is the basis for size analysis via Scherrer's method.

To expound on this idea, an example is given similar to that found in Hammond.[74] If a 1D crystal of m equally spaced planes is considered, then at some angle that is a 'small' deviation from θ_B the condition for destructive interference will occur between reflections off the top plane and the plane half-way into the crystal (i.e. plane $m/2$). Representing the deviation from θ_B at which this occurs as $\delta\theta$ and plugging in for plane $m/2$, **Equation 1.5** can be restated as:

$$\left(\frac{m}{2}\right)\lambda + \frac{\lambda}{2} = \left(\frac{m}{2}\right) 2dSin(\theta_B + \delta\theta) \quad 1.6$$

If this condition is satisfied between planes *1* and *m/2*, then at this same angle it will also be satisfied between planes *2* and *1+m/2*, *3* and *2+m/2*, and so forth, all the way through the crystal. Therefore, at angles of $\theta_B + \delta\theta$, complete destructive interference will occur for the whole crystal. **Equation 1.6** can be expanded by the trigonometric identities and simplified by considering the small angle approximations $Sin(\delta\theta) = \delta\theta$ and $Cos(\delta\theta) = 1$ which results in

$$\left(\frac{m}{2}\right)\lambda + \frac{\lambda}{2} = \left(\frac{m}{2}\right) 2d[Sin(\theta_B) + Cos(\theta_B)\delta\theta] \quad 1.7$$

The terms $(m/2)\lambda$ and $(m/2)2dSin(\theta_B)$ on the LHS and RHS, respectively, are just the terms of the Bragg equation which cancel and **Equation 1.7** simplifies to

$$\frac{\lambda}{2} = \left(\frac{m}{2}\right) 2d[Cos(\theta_B)\delta\theta] \quad 1.8$$

Which can be rearranged:

$$md = \left(\frac{\lambda}{2\delta\theta\ Cos(\theta_B)}\right) \quad 1.9$$

Recognizing that *md* is the thickness, *t*, of the crystal, a relationship between θ_B, the peak width, $2\delta\theta$, and *t* is established.

$$t = \left(\frac{\lambda}{2\delta\theta\ Cos(\theta_B)}\right) \quad 1.10$$

In practice, the full-width-half-max value (β) is used instead of $2\delta\theta$. These values are nearly identical and peak fitting routines usually return width values in terms of β. Additionally, since $2\delta\theta$ is the angle at which the reflection intensity is zero, it can be somewhat ambiguous to measure.

$$t \approx \left(\frac{\lambda}{\beta\ Cos(\theta_B)}\right) \qquad 1.11$$

Equation 1.11 is only valid for 1D crystals. To account for real 3D crystals, a proportionality shape factor, *k*, is used with **Equation 1.11**. Calculated values of *k* can be found in the literature.[75] As a final note, Scherrer's equation is simple to implement but at best can only be accurately applied to crystallites less than a few hundred nanometers where line broadening can effectively correlate to crystallite size. Additionally, no information on the distribution of crystallite size can be extracted using this method as only a single-value is calculated, taken to be an average size. For a more thorough discussion of the topics of XRD crystallography and Scherrer's equation, the reader is referred elsewhere.[74, 75]

Optical absorption

In Chapter 2, UV-vis absorbance measurements are presented for NiO nanoparticles suspended in solution from which an estimation of their bandgap energy is made. In this section a brief description for the analysis of the energy bandgap from optical absorption is provided. The reader is referred to other texts for more rigorous discussion on this topic.[76, 77]

The transmittance, *T*, of electromagnetic radiation through a medium of thickness *L* is given by $T = I(L)/I_0$ where I_0 is the incident intensity and *I(L)* is the intensity at *L,* after passing through the medium. *T* is related to the absorbance (*A*) of the medium through Beer's law:

$$A = -Log_{10}[T] \qquad 1.14$$

Where *A* represents how much the radiation has been attenuated by passing through the medium. The attenuation can be due to reflection, absorption, and scattering. If the scattering losses are minimal in comparison to the total attenuation, and the reflection contribution can be eliminated

by first performing an experiment on a control sample, then A will be related to the optical absorption coefficient (α) through:

$$A = \frac{\alpha L}{Ln(10)} \tag{1.16}$$

where αL is the optical density and is related to T through $\alpha L = -Ln[T]$.

When electromagnetic radiation is incident on a semiconductor or insulator, then for photon energies greater than and near the band edge, absorption will be associated with an electron transition from the valence band to the conduction band. Therefore, the absorption spectrum of a sample provides a simple means for estimating its bandgap. For direct bandgap materials, such as NiO, with parabolic dispersion near the band-edge, the absorption, α, will increase proportional to the square root of the photon energy for energies above and in the vicinity of the bandgap

$$\alpha[h\upsilon] \propto \left(h\upsilon - E_g\right)^{1/2} \tag{1.17}$$

where h is Planck's constant, ν is the photon frequency, and E_g is the bandgap. Therefore, the linear region of a plot of α^2 vs. $h\nu$ in the vicinity E_g can be extrapolated and its intersection with the energy-axis will correspond to the E_g.

CHAPTER 2

NICKEL OXIDE GROWTH WITHIN POROUS SILICON BY THERMAL DECOMPOSITION OF NICKEL ACETATE PRECURSOR

In this chapter, the preparation of NiO produced by thermal decomposition of a Ni-acetate precursor deposited into pSi pores, is presented. NiO formation in pSi is initially studied over a range of annealing temperatures (300°C to 1100°C) with pSi films of the same average pore size (64nm diameter). X-ray diffraction (XRD) analysis was employed to confirm the crystal structure of the NiO and to estimate the average NiO crystallite size. The average crystallite size showed a dependence on decomposition/annealing temperature, increasing from approximately 10nm to more than 100nm. SEM image analysis confirmed the trend and provided reasonable confirmation of these XRD-determined sizes. It was also observed that when annealing at temperatures of 800°C and above, oxidation of the pSi occurs. At temperatures of 900ºC to 1100ºC significant deformation of the pores, due to oxidation, allowed the average NiO crystallites to grow larger than the original average pore size. The NiO crystallites grown in pSi are compared to NiO prepared on crystalline Si (cSi) substrates by thermal decomposition of the precursor over the same temperature range. These showed a distinctly different trend in the resulting NiO crystallite size vs. anneal temperature, and overall were larger than their pSi-grown counterparts.

A second study was conducted for NiO grown by the same process in pSi films with different average pore sizes (20 to 57nm diameters) heated to the same temperature of 700°C. The average NiO crystallite size was found to increase with average pSi pore size from 12nm to 26nm based on analysis of the XRD spectra. It was then demonstrated that NiO can be removed from the pSi by dissolution of the Si in an alkaline solution. Elemental mapping of liberated NiO using

a transmission electron microscope (TEM) with energy-dispersive x-ray spectroscopy (EDX) capabilities revealed crystallites to be composed of Ni and O, confirming successful removal of the NiO from the pSi. Furthermore, the fundamental optical bandgap energies of the extracted NiO crystallites were estimated from their absorption spectra, ranging in value from 3.90eV to 3.72eV, within the range of bandgap values often reported for NiO.[63, 78, 79]

2.1 Introduction

Some fabrication techniques for NiO nanomaterials and their potential application areas were presented in **Section 1.2**. To briefly reiterate, NiO nanomaterials have been explored for a wide range of applications including battery and supercapacitor electrodes,[18, 42-46] chemical and gas sensors,[47-49] catalysis,[50] electrochromic windows,[51, 52] and resistive memory devices.[53-55]

Fabrication techniques for depositing NiO nanomaterials have included both physical and chemical methods such as sputtering,[56, 78, 80] laser ablation,[59] MOCVD,[55] electrochemical deposition,[18, 43, 44] chemical bath deposition,[56] spray-pyrolysis,[67] and spin-coating.[63] The physical methods are attractive for producing nanocrystalline and nanoporous films, but these can be more costly compared to chemical/solution-based methods due to high equipment costs. Furthermore, production of other nanostructures using physical techniques will usually require additional measures, such as the implementation of a template on which NiO can be deposited.[57] In contrast, chemical processes are less costly and more amenable to direct production of novel nanostructures and singulated/dispersible nanoparticles in addition to thin-films.[56, 65, 66, 69, 81] Additional techniques such as electrospinning,[46] magnetically-assisted deposition,[47] or implementation of templates can been employed to develop more novel nanostructured materials as well as provide another measure of control over the dimensions.[82-84]

For most of the chemical methods a final thermal decomposition step of at least 250ºC to 300ºC is necessary to convert the precursor material to NiO.[18, 42, 49, 59, 63, 83, 85] In general, low

temperature annealing (<500°C) results in NiO with increased defect densities and active surface sites, while higher temperatures produce higher quality NiO - i.e. improved crystallinity and reduced defects and impurities.[65, 68, 72, 86] This can directly influence the optical, electronic, chemical, and magnetic behavior of the nanoparticles. Even so, enhanced defect densities might be favorable, as in the case of electrochemical energy-storage and chemical sensors in which crystalline defects may serve to provide enhanced conduction and increase the number of surface reaction sites.[44, 59, 78, 86-89] Additionally, the final NiO grain size is largely dependent on the anneal temperature and in many studies, to maintain NiO with grain sizes less than ~50nm it is desirable to keep annealing temperatures below 500°C.[65, 72, 83, 85, 86, 90, 91] Furthermore, when singulated/ dispersible or high-surface area nanomaterials are desired, such as nanoparticles and porous films, then low annealing temperatures are needed to prevent sintering. Therefore, a robust method capable of producing nanoparticles over a wide range of temperatures and sizes would be beneficial for adapting to the requirements of the various applications. In this respect, template-based approaches provide a promising path for producing NiO nanomaterials over a wide range of anneal temperatures while providing control over the final dimensions.

In general, templates are used to impart dimensional aspects of their structure onto other materials often by growth or deposition of the other materials into, around, or on top of the templating structure. In selecting a template, a number of factors are considered such as ease of template fabrication, the level of control over dimensional parameters of the template, the durability of the template under additional processing conditions, and the ability to remove the template from the templated material if needed. Numerous materials have been employed as templates for NiO including polymers, surfactants, porous anodic aluminum oxide/membranes (AAO or AAM), and pinewood.[52, 81, 83, 84, 92, 93] One of the most common template materials is AAO because it is durable and cheap, and it exhibits highly uniform nanoscale pores. Templates

such as AAO are good candidates for producing nanostructures as a they are capable of withstanding high temperatures and can be removed by dissolving in alkaline solutions. Additionally, it is simple to vary AAO over a wide range of pore sizes.[83, 93-95] Similar to AAO, anodically etched pSi is reasonably inexpensive, durable at high temperatures, easy to produce over a wide range of selectable average pore sizes, and can be removed in basic solutions, but its real promise over AAO is the path it provides for direct development of Si-integrated devices and materials as demonstrated in the subsequent chapters of this dissertation.[54, 96, 97]

In this chapter a systematic study on the growth of NiO within pSi films is presented. The reported process employs the thermal decomposition of a precursor deposited in pSi host templates. The process is shown to provide a measure of control over the size of the resulting nanoparticles through predetermined selection of the average pSi pore size. The pores are assumed to limit the size of nanoparticles by both physically restricting their growth and by limiting the amount of precursor available for formation into particles. Due to the size limiting effects of the pores, the average diameter of the NiO particles is restricted to sizes below the average pore size even at high temperatures (> 500°C).

Two separate studies were carried out to investigate aspects of the growth of NiO within pSi. In the first study, the effect of pSi to limit NiO growth over a range of annealing temperatures (300°C to 1100°C) was investigated using pSi films of the same average pore size (64nm diameter). In the second study, pSi films with different average pore sizes (~20nm to 57nm diameter) were used as templates while NiO was formed in each pSi film by annealing the precursor at 700°C. It is also shown here that once the NiO:pSi nanocomposites are prepared, it is possible to extract the NiO nanoparticles by dissolving the pSi in an alkaline solution.

2.2 Effect of annealing temperature on growth of NiO in porous Si

Fabrication

Porous Si

All pSi films were etched from (100) n^+-type Si wafers (Sb-doped, 0.01 Ω-cm). The etching solution was composed of 12.5% v/v HF (48-50% aqueous), 87.4% deionized water, and 0.1% NCW-1001 (30% w/w polyoxyalkylene alkyl ether). The standard anodic etching process described in Chapter 1 was carried out using a Keithley 2425 source-meter and custom LabVIEW routines. Each pSi film was etched at 25mA/cm^2 for 600s, producing porous layers approximately 7μm thick with an average pore opening diameter of 64nm. Prior to etching the sample layer, a sacrificial layer was etched into each wafer and then removed. This process was performed to minimize the necking phenomenon.[14] To elaborate, during pore formation, pores often widen to a near constant size as they propagate into the Si wafer. This results in pore openings that are smaller than the diameter of the pores just below the surface. To minimize this effect, the initial porous layer can be removed by applying a sufficiently high current that causes electropolishing of the surface. The electropolishing process performed here involved applying an initial current of 25mA/cm^2 for 30 seconds to form the sacrificial porous layer and then applying three high-current pulses of 275mA/cm^2 for three seconds each, which fully removes the layer. After removal of the sacrificial layer, the sample layer can be etched. Each step in this process was performed immediately after the preceding step without any replacement of the electrolyte or removal of the Si wafer.

NiO precursor preparation, deposition, and heat-treatment

The NiO precursor solution was prepared by dissolving nickel acetate tetrahydrate (NAT) into 2-methoxyethanol (2MOE) at a concentration of 50mg/mL (NAT/2MOE). The solution was stirred at 350RPM using a magnetic stir bar on a hot-plate set at 60°C for 1 hour to ensure complete dissolution of the NAT. Deposition of NiO into the pSi films was accomplished by submerging each film in 15mL of the precursor solution and evaporating out the solvent at 65°C on a hot-plate (18 to 24h). This process allows the precursor to precipitate into the pores. **Figure 2.1** shows cross-sectional SEM images of pSi before and after the precursor was deposited, demonstrating that the pores are nearly completely filled with the precursor. Following deposition of the precursor, the pSi films were then cleaved to get multiple samples from a single pSi film. Afterwards, each cleaved sample was annealed in air to a set maximum temperature (ramp rate of 12°C/min) and held at this temperature for 2hrs before passively cooling back to room temperature. Maximum temperatures ranged from 300°C to 1100°C. Next, the pSi surfaces were lightly polished by hand with 0.3µm grain alumina lapping films to remove any superficial NiO.

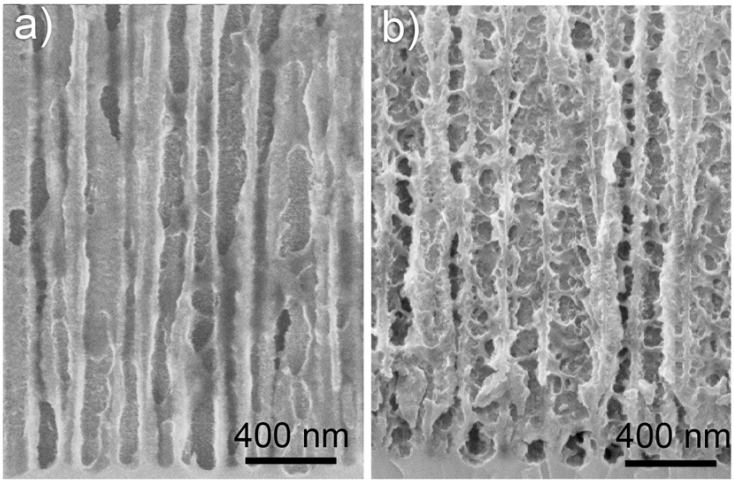

Figure 2. 1 Cross-section SEM images of pSi oriented with the pSi/air interfaces (out of view) on the top and the pSi/Si interfaces on the bottom: (a) before and (b) after NiO precursor deposition but prior to annealing. Near maximum filling of the pores is shown in (b). From Fain et al. 2015.[79]

The NiO crystallites formed inside the pSi films were compared to NiO formed on planar cSi substrates annealed over the same temperature range. These control samples were prepared by spin-coating the precursor solution onto the substrates at 2500RPM for 1min. The samples were then baked at 100°C for 1min to dry and remove residual solvent. Ten iterations of this spin-bake process were performed on each sample. After the cSi samples were coated, they were annealed alongside their pSi counterparts. It is noted that later experiments showed that only a single iteration of the spin-bake process was necessary as the dried precursor re-dissolves when additional precursor solution is added in the subsequent iterations.

Characterization

In this study, characterization of the pSi pore size was accomplished by using the image analysis software ImageJ (Rasband 1997-2014), on scanning electron microscopy (SEM) images of the pSi films. SEM images were collected on a Raith eLine tool. Characterization of NiO was performed by XRD and SEM image analysis. XRD was performed on each sample at the Center for Nanophase Materials Science (CNMS) at Oak Ridge National Laboratory using a PANalytical X'Pert Pro Powder Diffractometer with a Cu-kα x-ray source ($k\alpha_1$ λ = 1.540598Å). As discussed in **Section 1.4**, a common technique to estimate the size of nanocrystallites from XRD data is to employ Scherrer's equation,

$$D = \frac{k\,\lambda}{\beta\,Cos(\theta)} \tag{2.1}$$

relating the diameter of a nanocrystal D to the width of the diffraction peak where θ is the Bragg reflection angle in radians, λ is the x-ray wavelength, and β is the full-width-at-half-maximum of the peak in the diffraction pattern. In the equation, k is a unit-less shape factor.

Results

Pore Size Analysis

The specific details on the analysis of pSi pore size for this study are provided in Appendix A. A brief summary is provided here. Approximating the surface pore opening to be circular, image analysis on multiple images from multiple samples revealed pores to be normally distributed with a mean diameter of approximately 64nm and standard deviation of about 25nm. A typical example is provided in **Figure 2.2**, which shows a low magnification image with many pores in the field of view. The distribution of pore opening diameters determined by image analysis is shown in **Figure 2.2**b. The overlaid blue curve is the normal fit to the data.

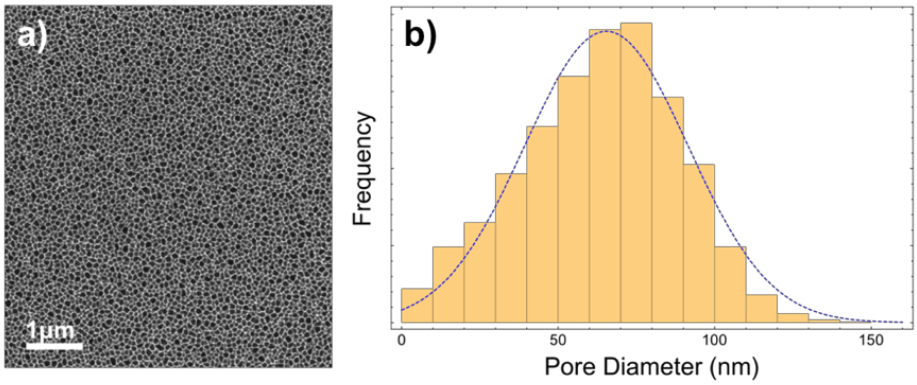

Figure 2. 2 (a) Low magnification SEM image of the pSi surface. (b) Distribution of pore diameters in (a) with a normal fit (blue line) overlaid. See Appendix A for more details.

X-ray Diffraction

Figure 2.3a shows XRD spectra collected over the range of 20° to 70° 2θ for NiO prepared in pSi and on planar cSi substrates after annealing at 700°C. XRD spectra for bare pSi and cSi samples (i.e., without NiO deposition) are also shown for comparison. The data are plotted on a $\log_{10}$ scale for ease of visually comparing the peaks in the plots. The samples with NiO exhibit peaks at 37.3°,

43.3°, and 62.9° 2θ corresponding to the (111), (200), and (220) peaks, respectively, of NiO in the expected cubic rock-salt crystal structure (ICDD 47-1049). For these samples, the largest peak is the (200) peak, and the intensity of this peak is much higher for the NiO annealed on planar cSi compared to the NiO annealed in pSi. This is expected, as more NiO is exposed to the beam on the cSi substrates than in the pSi films. Comparison of the XRD spectra for samples with and without NiO suggests that all other peaks are identified with Si/pSi.

Figure 2.3b shows the XRD spectra of the (200) peak of NiO in pSi (right) and on planar cSi (left), annealed at various temperatures. For ease of comparison, these spectra have been background subtracted and offset from each other. For both sets of spectra, the (200) peak tends to become sharper and increase in intensity with increasing temperature. There is a slight deviation in this trend for NiO on cSi at 800°C, but this is likely due to the fact that this sample was cleaved to a smaller size than the others, decreasing the total amount of exposed NiO and reducing the peak height. Nonetheless, it is not the height directly, but rather the width of the peak that is considered for calculation of the particle size from **Equation 2.1**. There is also obvious $k\alpha_1$ and $k\alpha_2$ peak splitting at the higher temperatures for NiO on cSi. Though the splitting is not obvious in the NiO:pSi spectra, the $k\alpha_2$ peak is still present but the peak widths are large and overlap occurs. Finally, the NiO:pSi spectra exhibits a Ni-metal (111) peak at 44.5° 2θ that increases with temperature. A possible reason for this may be that the Si behaves as an oxygen sink as temperature increases, depleting the NiO of enough oxygen such that regions of metallic Ni form. If this is the case, then it would be expected that the Ni peak would be more prominent in NiO samples formed in pSi as the surface area contact between NiO and Si is much greater than for NiO formed on planar cSi. This is indeed what is observed here.

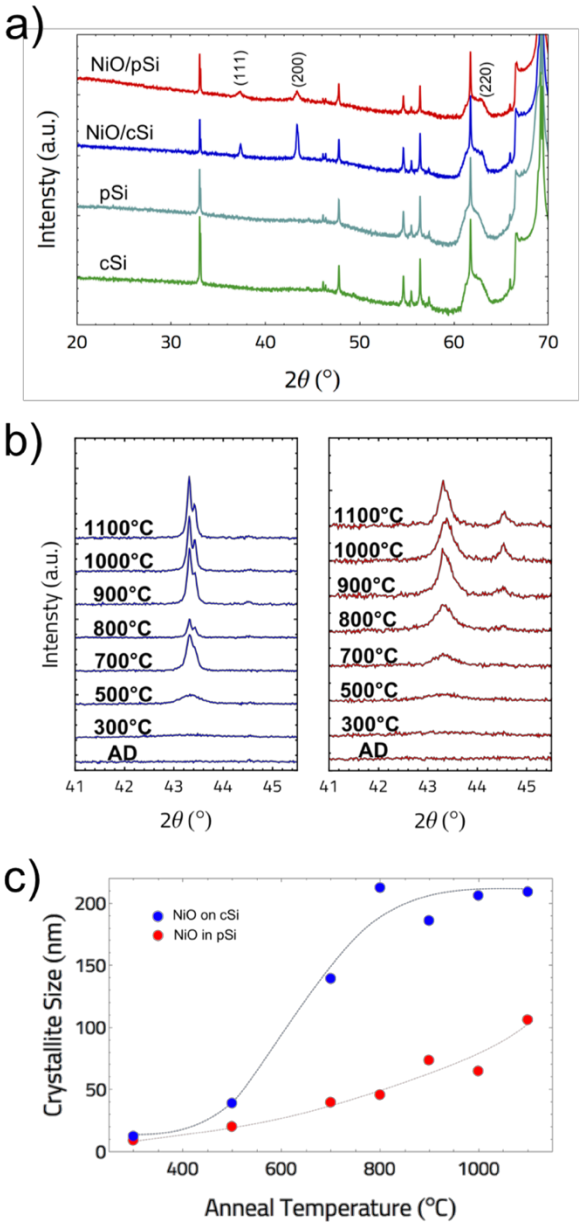

Figure 2. 3 (a) XRD spectra of NiO annealed at 700ºC on a planar cSi wafer (blue) and in pSi (red) with the NiO (111), (200), and (220) peaks labeled. XRD spectra of cSi and pSi are also provided for comparison. (b) XRD spectra of the NiO (200) peak on planar cSi (left) and in pSi (right), annealed at various temperatures. (c) Plot of the estimated NiO crystallite size vs. anneal temperature, calculated from application of eqn. (2.1) to the (200) peaks in (b). The curves are guides-to-the-eye and do not represent a fit of the data. Adapted from Fain et al. 2015.[79]

Size analysis of NiO crystallites grown on planar cSi substrates

Lorentzian peaks were fit to the NiO (200) kα_1 and kα_2 peak components in all spectra in **Figure 2.3**b. The relevant calculated fit parameters of the kα_1 peak component were then applied to **Equation 2.1** to estimate the NiO crystallite size. The shape factor, *k*, set to a value of ~0.9 in **Equation 2.1**.[75] **Figure 2.3**c provides a plot of the calculated NiO crystallite size vs. anneal temperature for NiO annealed on planar cSi wafers (blue) and in pSi (red). For NiO on planar cSi, the XRD calculated crystallite size increased only slightly in diameter from ~15nm at 300°C to 40nm at 500ºC. At 700°C, the calculated crystallite size increased more drastically to 140nm in diameter and then the size appears to level off around a diameter of 200nm by 800°C. The reason for this leveling off is better understood by considering the SEM images in **Figure 2.4**, to be discussed next.

Though **Equation 2.1** provides a simple method for the estimation of crystallite domain size over a large region (X-ray spot size >1cm^2), it is limited in application to crystallites with domain sizes less than a few hundred nanometers where line-broadening can be correlated to crystallite size and certain assumptions in the derivation can be applied, such as a constant reflected intensity of the x-ray beam at each reflected plane. This size limitation may be partially contributing to the apparent leveling off in the size for NiO on planar cSi in **Figure 2.3**c. Additionally, other sources of line-broadening such as lattice strain and system effects can obscure the calculation, but even with these limitations it is still a widely used technique that provides a simple estimate of the average crystallite size.

Figure 2.4 shows SEM images for NiO annealed at the indicated temperatures on planar cSi substrates. Clearly the particles are not uniformly distributed in size, particularly at higher temperatures with many particles shown that are much larger and smaller than the estimated size from XRD spectra. At 300°C, any discrete nanoparticles are too small to be visible at this scale,

as would be expected if sizes were consistent with those determined from XRD analysis (~15nm diameter). At 500ºC, small particles are clearly seen with sizes commensurate with those previously estimated from the XRD data. At 700°C, the particle size has increased significantly, consistent with the previous analysis and, from the surface, it seems the particles are mostly separated from each other. From analysis of a much larger region of the surface, the average lateral diameter of the particles at 700ºC is approximately 90nm with a large standard deviation of 41nm. This value is significantly smaller than the calculated particle size from the XRD, which was about 140nm. For the samples annealed at 1000°C, the average NiO particle diameter from SEM image analysis was approximately 190nm with a standard deviation of 80nm, close to the calculated value from the XRD data of ~207nm. From the SEM images at 800ºC and above, it appears that the particles have grown large enough such that they impinge on each other and significant sintering occurs, limiting further growth. This corroborates the leveling off of the data in the XRD size analysis in **Figure 2.3**c for NiO grown on planar cSi.

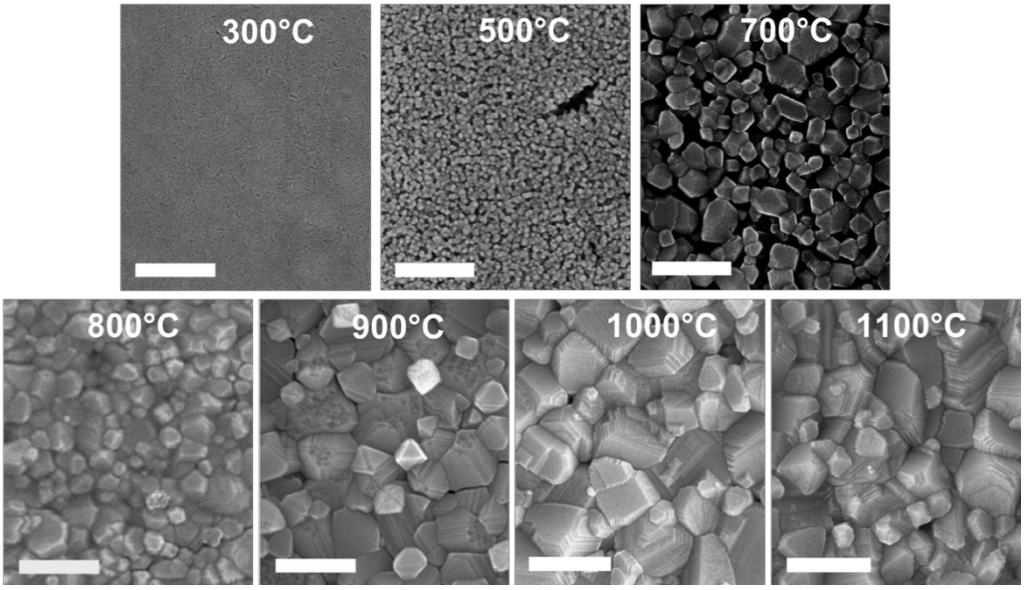

Figure 2. 4 SEM images of NiO particles grown on cSi substrates over the temperature range of 300 to 1100ºC. Scale bar = 400nm. Adapted from Fain et al. 2015.[79]

Though the results of SEM and XRD size analysis mostly agree, there are certain considerations to take into account. For one, the difficulty in measuring the size of the particles by analysis of SEM surface images lies in the fact that only a small sample of the particles are within the field of view, only the lateral dimensions are measured, many of the larger particles are covered or obscured by smaller particles that makes estimating the size difficult, and the particles are widely distributed in size and shape. Additionally, in applying **Equation 2.1**, a spherical shape was assumed, but clearly the SEM images show that the particles do not possess a well-defined and consistent shape, as some are elongated or possess sharp and jagged edges. It should also be emphasized that there is a distinction between crystallites/grains and particles. Crystallites are the domain corresponding to the ordered arrangement of the atomic lattice structure. For example, a polycrystalline particle would be a single particle composed of several crystallites with grain-boundaries existing where the individual crystallites meet. A single-crystalline particle would be composed of only one crystallite. The method of size analysis by XRD measures the crystallite size whereas SEM is a measure of the NiO particle size, which should be equivalent if the particles are single crystals and consistent in shape. Though there are obvious differences, both XRD and SEM analysis here reveal similar trends in NiO growth on cSi substrates as the annealing temperature increases and the calculated sizes mostly agree. To summarize, at 300ºC the particles are very small and increase in size only slightly as the anneal temperature increases to 500ºC. At 700ºC the particle size increases much more significantly, by several fold, and then size growth is minimal above 800ºC.

Crystallite size analysis of NiO grown in pSi

For NiO grown in pSi, application of **Equation 2.1** to the NiO (200) kα_1 peaks shown in **Figure 2.3**b (after extracting parameters from a Lorentz peak fit), produces the red curve in **Figure 2.3**c.

The crystallite domain size is ~10nm in diameter at 300ºC and increases much more gradually compared to the NiO on planar cSi with a value of only ~45nm at 800°C. Above 800ºC the increase in size with temperature is slightly enhanced and tops out at ~107nm in diameter at 1100ºC. Surface SEM images of NiO in pSi are shown in **Figure 2.5** for anneal temperatures of 300º, 500º, and 700ºC. At 300ºC any presence of NiO growth is difficult to see, as would be expected if particle sizes are comparable to the calculated crystallite domain size of approximately 10nm in diameter. At 500ºC, formation of small particles is apparent and they appear comparable in size to the values determined by XRD analysis of ~20nm in diameter. At 700ºC, the particles are more defined. As the annealing temperature increases further, the pSi experiences significant oxidation which made surface imaging difficult.

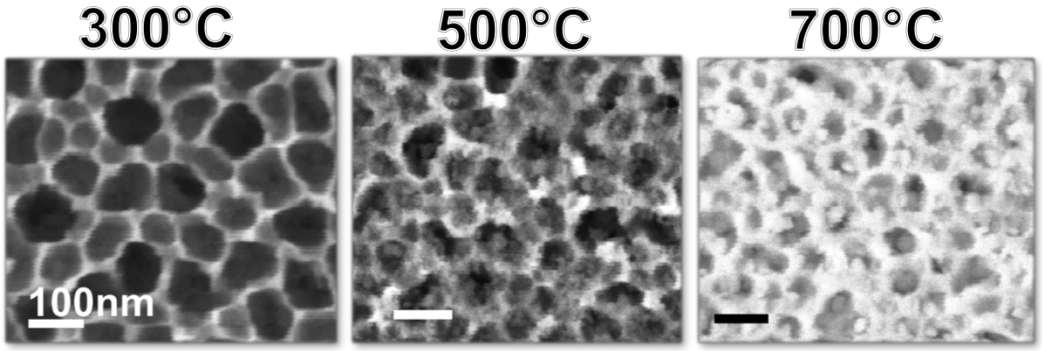

Figure 2. 5 Surface images of NiO grown in pSi at the labeled temperatures.

Cross-section images of samples are provided in **Figure 2.6**. At 300ºC there appears to be some material in the pores but it is difficult to make out distinct particles. This is similarly the case for the 500ºC sample. And although from the surface image in **Figure 2.5,** a few particles seem to be present, it would be expected that many more should be visible so it is possible that during cleaving of the pSi for cross-section imaging most of these fall out. At 800ºC, small particles are more obvious, clearly attached to the pore walls and evenly dispersed throughout the

porous layer. Additionally, it seems that the pSi has begun to oxidize which may be the reason more particles appear to be present, possibly due to the NiO becoming partially embedded into the oxidized pore walls. Furthermore, the oxidation layer has even begun to penetrate into the bulk Si layer as demarcated by the red dash. At 1000ºC and 1100ºC large particles are clearly visible and the oxidation front penetrates increasingly further into the Si substrate. Furthermore, significant deformation of the pores has occurred as a result of the oxidation. The more abrupt increase in NiO crystallite domain size at 1100ºC indicated from the XRD analysis in **Figure 2.3**c may be attributed to the oxidation induced deformation.

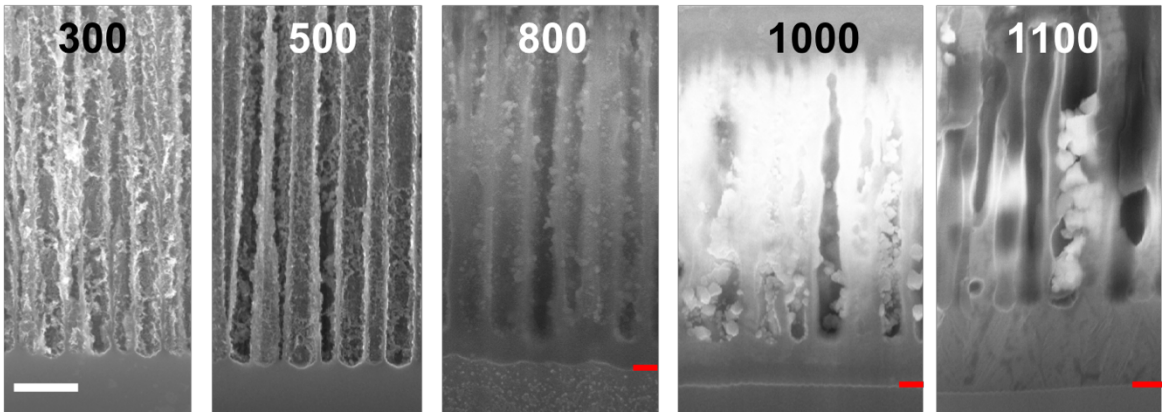

Figure 2. 6 Cross-section images of pSi with NiO particles present, annealed at 800ºC and 1000ºC. At 800ºC, the pSi has begun to oxidize but still maintains its apparent morphology. An oxide layer has also formed at the pSi/Si interface. At 1000ºC, extreme oxidation has occurred and has led to the deformation of the pores allowing particles to grow much larger. Scale-bar = 100nm (white line in the 300ºC image). Images corresponding to 300ºC and 500ºC are adapted from Fain et al. 2015.[79]

Discussion

In comparing the two sample sets, NiO on cSi and in pSi, it is clear that the pSi morphology restricts rapid growth of the NiO inside the pores. This is attributed to the constraining effects of the pores as well as the limited amount of accessible precursor in each pore. From the results of

XRD analysis shown in **Figure 2.3**c, at 300ºC the crystallite domain size is comparable between the sample sets (10-15nm in diameter) with the pores having little effect since the crystallite size is significantly smaller than the pore diameter. At 500ºC, the difference in crystallite size is modest with NiO on planar cSi having an average size of ~40nm in diameter while in pSi the average size is ~20nm in diameter. At 700ºC, the NiO crystallite sizes begin to diverge significantly with NiO produced on planar cSi having an average calculated size of 140nm in diameter while those formed in pSi are only about 40nm in diameter. At 800ºC, the NiO on planar cSi continues to exhibit a significant increase in size to just above 200nm in diameter while in pSi the size has only increased to ~47nm in diameter. Above 800ºC, the NiO particles on planar cSi do not appear to grow larger, possibly due to adjacent particles coming into hard contact and sintering preventing extended growth. In pSi, the NiO crystallites exhibit a slight enhancement in the increase of size with temperature attributed to the deformation of the pSi film due to oxidation. These trends are corroborated by SEM image analysis.

2.3 Effect of pore size on growth of NiO in porous Si

In this section, the growth of NiO nanoparticles within the interior of pSi films having different average pore sizes and formed at the same annealing temperature of 700°C is described.

Fabrication

Porous Si

The only difference in the etching process compared to the process described previously in **Section 2.2** is that the etch current is varied from sample-to-sample to achieve different average pore diameters. The Si wafers, etching solution, and etch duration were exactly the same, as well as the process to remove the sacrificial layer. The etch currents selected here were 12.5, 15, 17.5, 20,

and 22.5mA/cm^2. The final pSi films were approximately 7μm thick and pore sizes ranged from ~20nm to 57nm in average diameter as measured from SEM imaging of the surface openings.

NiO precursor preparation, deposition, and heat-teatment

The exact same NiO precursor solution of 50mg/mL NAT/2MOE was used and deposited according the process outlined in **Section 2.2**. After deposition of the precursor, an annealing temperature of 700ºC was used to form NiO in all samples.

Removal of NiO from porous Si

After characterizing the NiO in the pSi host matrices, the NiO particles were removed from their respective pSi films by dissolving the Si in an aqueous KOH solution (30% w/w) at room temperature for approximately 1 hour. The liberated NiO nanoparticles were then rinsed and suspended in deionized water by performing six iterations of centrifugation, removal of the supernatant, and replacement with deionized water. The rinsed particles were then filtered through 5μm syringe filters (Millipore Millex) to remove any large contaminants.

Characterization

XRD analysis was used for determining crystal structure and size, and was performed using the same PANalytical system described in **Section 2.2**. SEM images were collected on the same Raith eLine system described previously as well. TEM imaging and elemental analysis by EDX was performed on nanoparticles that were removed from the pSi host etched at 17.5mA/cm^2 using a FEI Tecnai Osiris TEM with EDX capabilities. Samples were prepared for imaging by drop-casting 2μL of the NiO nanoparticles suspended in water onto ultrathin carbon type-A (3-4nm) grids with removable Formvar (Ted Pella, Inc.). Optical absorbance measurements were also conducted on liberated NiO nanoparticles suspended in DI-H_2O over a wavelength range of λ =

200 to 600nm from which the bandgap could be estimated. The measurements were performed on a Varian Cary 5000 spectrophotometer.

Results and Discussion

Pore size analysis

Figure 2.7 shows cross-section and plan view SEM images of the pSi films with NiO nanoparticles investigated in this study. The etch current density is provided for each set of images. The average pore size increases with increasing etch current density from ~20nm to ~60nm in diameter, as determined from image analysis of the surface, resulting in a normal distribution of pore sizes. The relationship between average pore size and etch current is plotted in **Figure 2.8** with the error bars representing the standard deviation. From the cross-section SEM images, the pore morphology clearly changes from branched to more smooth/cylindrical pore walls as the etch current increases. This has been explained due to the passivating effects of the H-termination as discussed briefly in **Section 1.1** and elsewhere[14]. At low applied currents, the passivation of certain Si crystal planes by H reduces the likelihood of etching occurring in these directions, leading to branching. At higher applied currents, the passivation is less effective and the branching effect is minimal. For these samples, the transition in morphology appears to occur between 20 and 22.5mA/cm^2, and the morphology change is correlated with an increase in pore size from an average diameter of 35 to 57nm, based on surface image analysis. At lower currents, the increase in pore size with etch current is much more gradual and there even seems to be no significant difference in the average pore size and distribution between pSi etched at 17.5 and 20mA/cm^2.

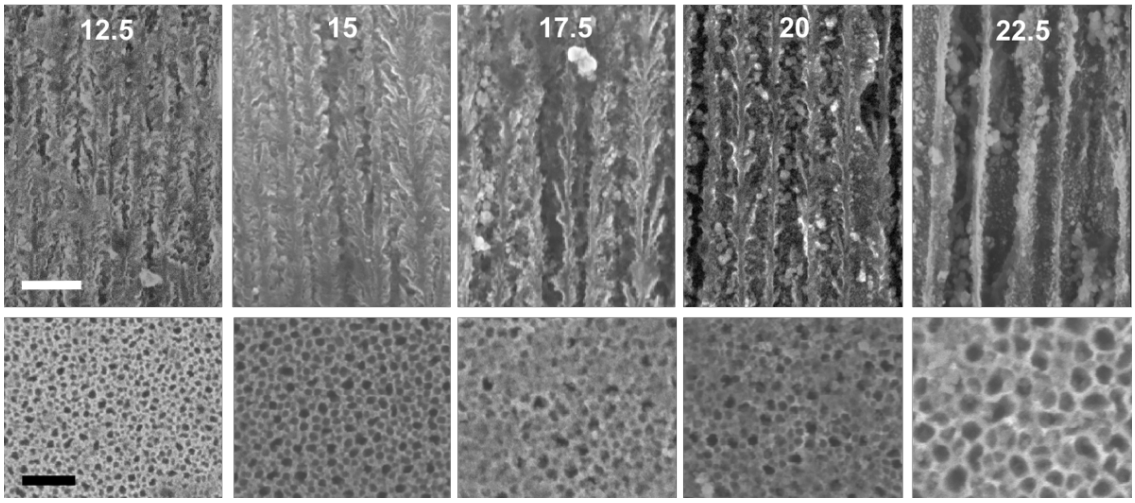

Figure 2. 7 SEM images of pSi etched at each current density in this study. (Top Row) cross-section. (Bottom Row) surfaces. Etch current is labelled at the top of the cross-section images (in units of mA/cm^2). NiO has already been deposited and formed in these samples as well. Scale bars = 200nm. Adapted from Fain et al. 2015.[79]

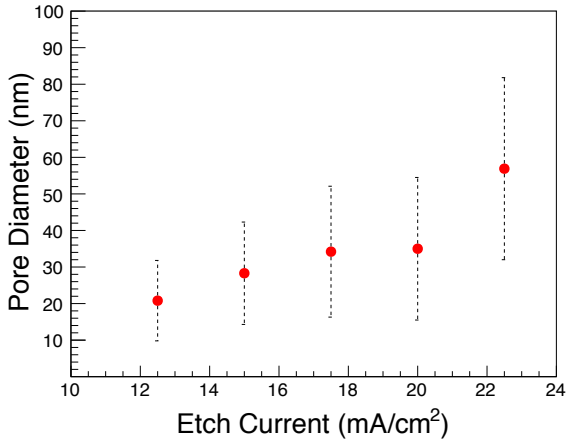

Figure 2. 8 Average pore diameter as a function of etch current density determined from image analysis of pSi surface SEM images. The error bars represent the standard deviation.

NiO crystallite size analysis

XRD spectra, after background subtraction, over the range of 25 to 55º 2θ are provided in **Figure 2.9**a for the samples prepared in study II. The peaks at 37.5º and 43.3º correspond to the (111) and (200) NiO peaks in the cubic rock salt crystal structure (ICDD 47-1049). All other peaks are

attributed to Si. The arrow indicates the direction of increasing pSi etch current. As the etch current increases, the NiO peaks become sharper, indicative of increasing crystallite domain size. This trend is consistent with the increasing pore diameter that results from the increasing etch current.

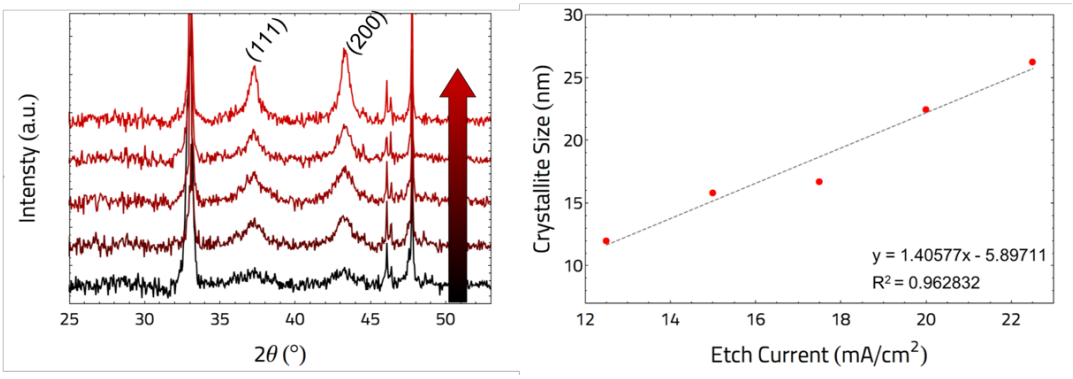

Figure 2. 9 (a) NiO (200) XRD peak for increasing pSi pore size. (b) plot of NiO crystallite size was estimated from the (200) peak in (a) vs. average pSi pore size. Adapted from Fain et al. 2015[79]

A plot of crystallite size vs. etch current is provided in **Figure 2.9**b. As in the previous section, these sizes were estimated from application of **Equation 2.1** based on parameters derived from Lorentzian fits of the $k\alpha_1$ (200) peak. Both $k\alpha_1$ and $k\alpha_2$ contributions were fit to the peak. The trendline added in **Figure 2.9**b suggests that there is a near linear relationship between crystallite size and etch current, with the average crystallite size ranging from ~12 to 26nm in diameter, but more experiments would be needed to confirm this trend. Plotting NiO crystallite domain size vs. pore size (not shown) resulted in a less well-defined trend, which may be attributed to the difficultly in accounting for pore morphological variations when estimating pore size. Possible error in the crystallite size approximation may be due to a number of factors, including experimental error, the fact that pore size does not directly account for variations in pore morphology, or the limitations inherent in approximating crystallite size using **Equation 2.1**.

TEM and elemental mapping of liberated NiO nanoparticles

Figure 2.10a provides a TEM image of NiO particles extracted from pSi films etched at 20mA/cm^2. These nanoparticles have diameters that range in size from about 20 to 30nm. The size estimates from TEM are in good agreement with the average crystallite domain size estimated from the XRD (200) peak (22nm). A high magnification image of a nanoparticle from this cluster, with diameter of ~20nm, is shown in **Figure 2.10**b. This particle, as well as others in this cluster, appear to be composed of a single-crystal, supporting the idea here that the crystal domain size and particle size are equivalent. **Figure 2.10**c shows an even higher magnification of the particle in (b) where the distance between planes of ~2Å is shown. This is consistent with the interplanar spacing of the (200) family of planes which is ~2.08Å based on XRD analysis, or half the NiO lattice constant of 4.16Å. Elemental mappings of nanoparticles from the same sample are shown in **Figure 2.11**, which provides visual confirmation that the particles are composed of Ni and O.

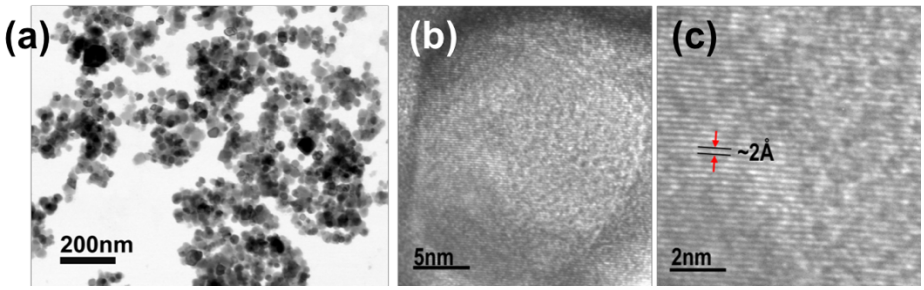

Figure 2. 10 (a) TEM bright field image of NiO nanoparticles extracted from a pSi film etched at 20mA/cm^2 (35nm pore diameter). (b) Magnified TEM image of a single NiO nanoparticle from (a) with a diameter of ~22 nm. (c) The nanoparticle in (b) magnified further showing the (200) lattice with spacing of ~2Å. (b) and (c) are from Fain et al. 2015.[79]

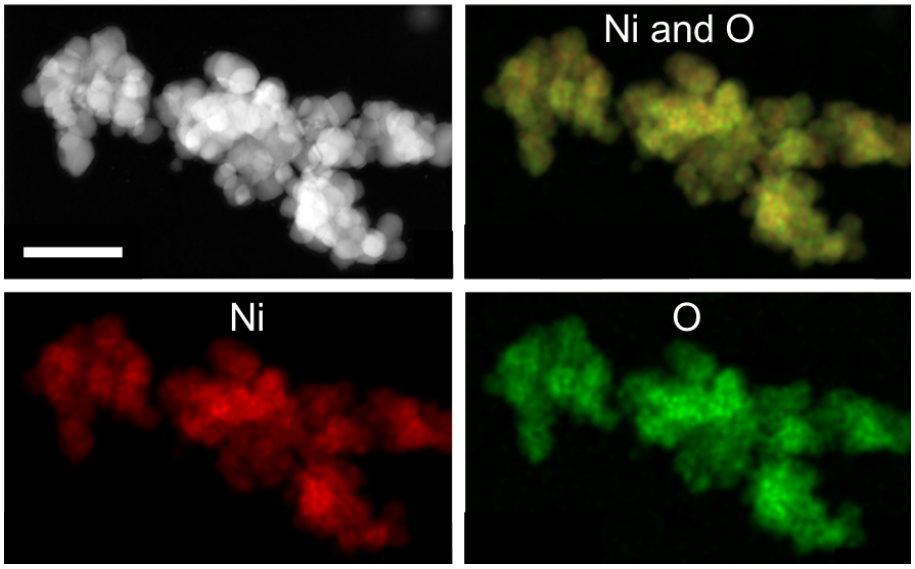

Figure 2. 11 Elemental mapping of a cluster of NiO particles showing uniform presence of Ni and O. Adapted from Fain et al. 2015.[79]

Optical absorption of liberated NiO nanoparticles and bandgap calculation

Optical transmission measurements were collected for all samples of NiO extracted from the pSi films and suspended in DI-H_2O. The normalized absorbance (A) spectra, calculated from the transmission data for each sample of NiO suspended in DI-H_2O is provided in **Figure 2.12**. From A, the absorption coefficient (α) can be calculated, as discussed in **Section 1.4**.

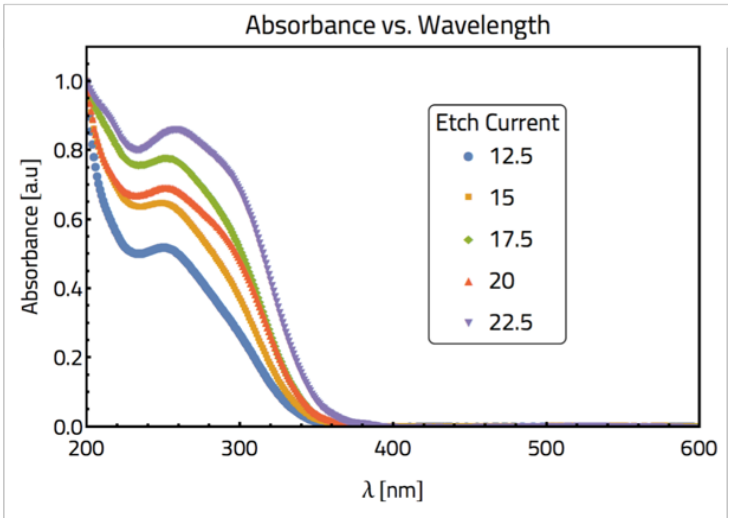

Figure 2. 12 Normalized absorbance spectra for NiO nanoparticles suspended in DI-H_2O. Adapted from Fain et al. 2015[79]

For direct bandgap materials, such as NiO, a plot of α^2 vs photon energy ($h\nu$) should be linear in the vicinity near and above the fundamental band gap (E_g), as discussed in **Section 1.4**. These are plotted for each sample in **Figure 2.13** and indeed are linear in the region shown. Extrapolation of the linear portion of each curve will cross the energy axis at E_g. These values are also provided in for each plot in **Figure 2.13**.

The fundamental bandgap energies determined from extrapolation of the plots in **Figure 2.13** decrease with increasing etch current, and thus particle size from 3.90eV (12.5mA/cm^2 - 10nm NiO crystallite diameter) to 3.72eV (22.5mA/cm^2 - 26nm NiO crystallite diameter). The theoretical value of the bulk bandgap of NiO is 4.0eV, however, experimental values ranging between ~3.4 to 4eV are often reported. The wide range of reported values is due to different fabrication techniques, presence of lattice defects, point defects, and size of the nanoparticles/nanocrystals.[63, 78, 79]

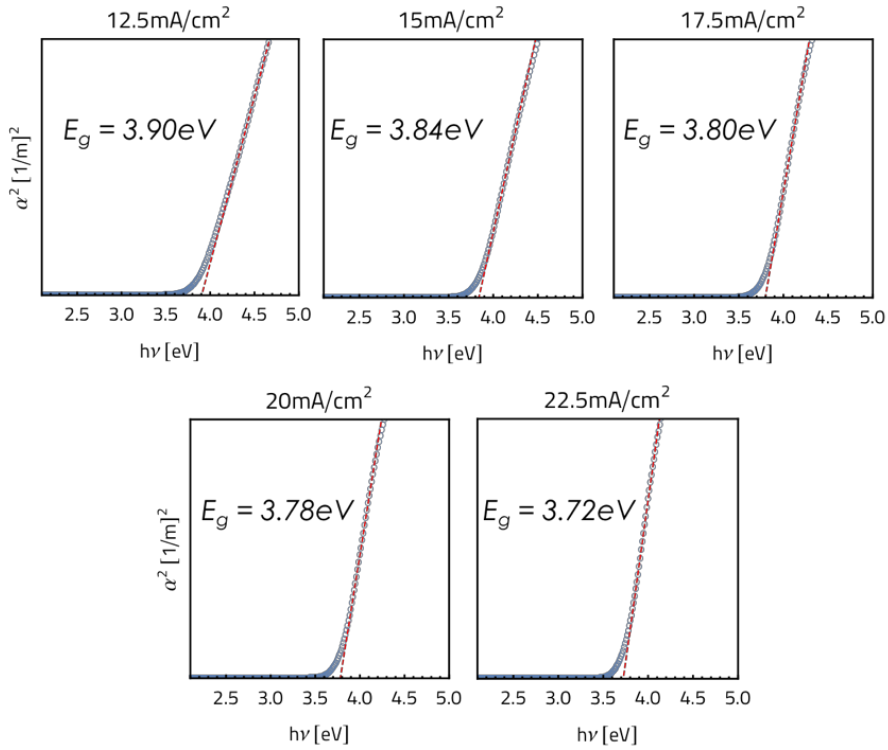

Figure 2. 13 Plots of α^2 vs. $h\nu$ derived from absorbance data for each sample of NiO nanoparticles extracted from pSi films etched at the labeled current density. In each plot, the red dashed line is a least-squares fit of the linear region of the curve used to extrapolate to the energy-axis where the intercept corresponds to E_g. Adapted from Fain et al. 2015.[79]

2.4 Conclusion

In this chapter, a process for chemically synthesizing NiO nanoparticles within the interior of pSi templates was presented. The pSi pores were demonstrated to limit the growth of NiO as well as preclude large-scale sintering of particles into polycrystalline films at elevated temperatures. In the first study described, NiO was synthesized by thermal decomposition of a Ni-acetate precursor over a temperature range of 300°C to 1100°C in pSi samples all etched at the same current density of 25mA/cm^2. The NiO formed in pSi was compared to NiO grown on planar cSi substrates over the same anneal temperature range. The average pore size of the pSi host film was determined by image analysis of the pore openings on the surface and the pore size was observed to be normally

distributed with a mean of 64nm ± 25nm. XRD analysis of the NiO in pSi and on planar cSi annealed at 700ºC revealed the presence of the (111), (200), and (220) peaks of NiO in the cubic rock-salt phase. Comparing the NiO (200) XRD peak of each sample revealed that the peak tends to become sharper as annealing temperature increased for both sets of NiO, which is indicative of increasing crystallite size. Application of Scherrer's equation (**Equation 2.1**) to the XRD data allowed simple estimation of the average NiO crystallite domain size which, in pSi, increased with increasing annealing temperature from about 10nm at 300ºC to 107nm at 1100ºC. Comparing this to the NiO crystallites produced on planar cSi samples, an increase in size from 15nm to >200nm over the same annealing temperature range was observed, confirming that the pSi serves to effectively limit the growth of the NiO nanocrystallites at high temperature. SEM image analysis further revealed that while NiO nanoparticles annealed at low temperatures on cSi can more or less grow unbounded at 800ºC and above, the particles are large enough to interact with neighboring particles and begin to sinter, restricting further growth.

A second study on the effects of pore size on the final size of the NiO nanoparticles grown within the pSi films was also conducted. In this study, pSi films were etched at different current densities (12.5 to 22.5mA/cm^2), producing films with average pore sizes of ~20nm to 57nm in diameter. In this study, all pSi films were annealed at the same temperature of 700ºC. XRD analysis provided estimation of NiO crystallite domain size, which ranged from ~10nm to 26nm in diameter. A near linear relationship between NiO crystallite size and pSi etch current was found, but further experiments are needed to verify this trend. Plotting NiO crystallite domain size vs. pore size, however, resulted in a less well-defined trend, which may be attributed to the difficulty in accounting for pore morphological variations when estimating pore size. In this study, the NiO was also extracted from their pSi host by dissolution of the pSi in a basic aqueous KOH, and the liberated NiO particles were then rinsed and suspended in water. TEM imaging of particles

extracted from the 17.5mA/cm^2 pSi film showed the particle sizes to be close to the values estimated by XRD analysis, and elemental mapping confirmed that only Ni and O were present in the particles. UV-vis absorption measurements on the extracted particles suspended in DI-H_2O allowed estimation of the E_g by extrapolation of the linear region of a plot of α^2 vs. $h\nu$ to the energy axis. These bandgap values decreased with increase in size of the particles from 3.90eV for an average particle diameter of 10nm to 3.72eV for an average particle diameter of 26nm. The estimated values of the E_g are also consistent with the range of bandgap values usually reported for NiO. Preparing NiO within the interior of pSi is demonstrated to be an effective template for permitting a measure of control in size and properties through simple selection of the pSi etching parameters and annealing temperature.

CHAPTER 3

INVESTIGATIONS ON VARIABLE CONDUCTIVITY BEHAVIOR IN NANOCOMPOSITE METAL OXIDE – POROUS SILICON

In this chapter, investigations of metal oxide:pSi nanocomposites for passive devices that exhibit variable conductivity are described. For this work, two metal oxides that are known to exhibit such characteristics were investigated – nickel oxide (NiO) and titanium dioxide (TiO_2).[53, 98] The NiO:pSi nanocomposite system was investigated first through collaborative efforts. The results of electrical characterization provided a framework for the development of a heuristic device-level model.[54] Next, TiO_2:pSi devices were prepared. These also exhibited variable conductivity, but to a much lesser extent than the NiO:pSi devices. Additionally, they showed evidence of a charge-storage component as well.

3.1 Introduction

Passive, nonvolatile, variable conductivity devices (*memristors*) developed from ionic/defect-conducting materials are capable of changing their resistance state with the application of a voltage and maintain their most recent state when the voltage is removed.[98] Depending on device type, the change in resistance may manifest as discrete states or as a continuum of states. Such devices have received increased attention in the past few decades for applications in resistive binary memory such as resistive-RAM, and for implementation as continuous-state analog memory technologies in applications of neuromorphic computing. [53, 99-105]

Transition metal oxides (TMOs) such as NiO, HfO_2, TiO_2, $SrTiO_3$, are one of the more extensively studied classes of materials for memristors.[30-34, 106] In materials such as these, the effect is due to ion/defect migration under the influence of an applied electric field. The particular

role ion migration plays may either be in the form of formation/breaking of electrically conductive filaments, or the varying spatial distribution of the ion/defect density upon application of a field. In this later case, the control of the defect spatial distribution may alter the resistivity of the material or alter a potential barrier at a junction.[33, 54, 98, 102, 106-109]

Due to the nature of ion/defect migration, memristive elements are almost exclusively developed from nanomaterials. Many of the materials investigated for memristors can behave as solid electrolytes at nanoscales, but in bulk, ion mobilities are essentially non-existent. This nanoscale effect has been postulated as due to increased sites for ionic hopping through the introduction of a higher density of lattice defects and nanograin boundaries.[106, 110, 111] Additionally, since ion migration is field-induced, higher voltages will be required to activate ion movement as the thickness of the active material increases. Furthermore, at high fields (>1MV/cm) it has been postulated that ion mobility will increase exponentially with increasing field strength, and such fields are easy to achieve at the nanoscale for modest voltages.[110] For instance, a 10nm thick film with 1V across it would result in a field of 1MV/cm. For applications of resistive-based memory, the exclusive operation at the nanoscale is a non-issue as smaller is generally preferred, but development of large-scale discrete memristors could also be of benefit and serve to extend the application space of these devices.

In the subsequent sections of this chapter the development of "large"-scale memristive devices from metal oxide:pSi nanocomposites is presented. The schematic in **Figure 3.1** depicts the cross-section of the idealized metal oxide:pSi composite formed into a memristor device. Each metal oxide/Si interface is envisioned to form a junction with a variable potential barrier, represented as alternately facing diodes in **Figure 3.1**. In this way the composite is viewed as an effective medium composed of individual memristor elements concatenated together such that their collective operation results in a macroscopic (μm-scale) memristive effects. Such device

sizes would make these too large to be practically competitive with current non-volatile memory elements, but it may be expected that larger discrete components would find use in numerous other implementations. Furthermore, given that these devices are fabricated directly embedded in a Si-wafer substrate, a simple path for integration is inherent in the device structure.

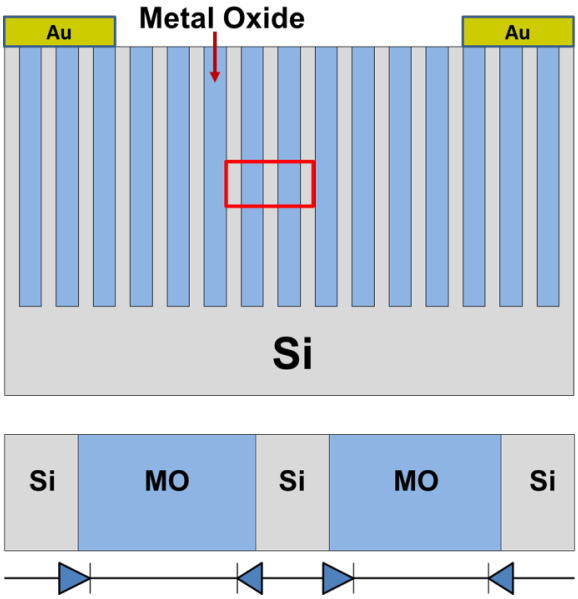

Figure 3. 1 (Top) Schematic of the cross-section of the ideal device structure showing Si pores (gray) filled with metal oxide (blue). Additionally, Au electrical contacts are present on the surface. (Bottom) Magnified view of the region outlined in red along with a simple circuit model representation of the Si/metal oxide interfaces which are envisioned to form alternately-facing diode junctions with a variable potential barrier due to ion migration.

3.2 Description of the mechanism

To briefly describe the mechanism presumed at play in the metal oxide:pSi composite, a single 1D metal oxide-filled pore is considered (**Figure 3.2**).[54] The model assumes that at each metal oxide/Si interface there exists an energy-barrier whose height is dependent on the number of defects present at the interface. **Figure 3.2**a depicts the initial state of the system. Due to the nanoscale nature of the system, it is assumed that the metal oxide in the pore is defect rich and that these defects are sufficiently distributed in space and energy such that electronic conduction readily occurs via site hopping. When a voltage is applied, one interface is effectively forward biased across which electronic conduction can readily take place. The opposite junction is reverse-biased, and blocks current. As the voltage continues to be applied, mobile defects migrate towards the reverse-biased interface and accumulate, resulting in a reduction of the effective barrier, and increasing the probability of emission across the junction as depicted in **Figure 3.1**b. Upon reversing the polarity of the applied voltage, initially the opposite interface is now reverse-biased and depleted of defects which will limit conduction until the voltage has been applied long enough for mobile defects to migrate to this interface and reduce the barrier (**Figure 3.1**c). In assuming such behavior, switching bias polarity results in an immediate change in the conductivity. This behavior is in contrast to the common filament-type mechanism which operates by setting up a conductive ion-channel between two electrodes. In this case the conductivity state is maintained after the polarity is reversed until some threshold voltage causes the filament to break. In the subsequent sections of this chapter, the development of nanocomposite metal oxide:pSi devices exhibiting variable conductivity with contact separations up to several 10s of μm's is presented.

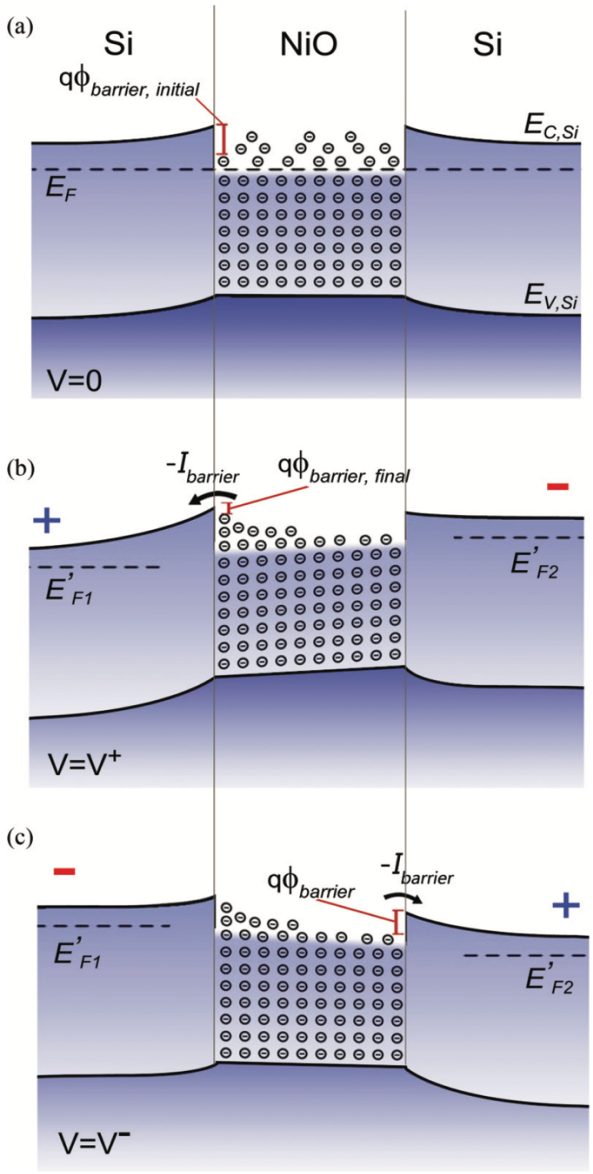

Figure 3. 2 Schematic band-gap description of the variable conductivity mechanism in a single metal oxide-filled pore. (a) The system is unbiased and defects (depicted here as circles) are uniformly distributed throughout the pore. (b) Applying a voltage causes charged defects (here, depicted to be negative) to migrate towards an interface. Accumulation of defects at the pore wall results in a reduction of an effective energy-barrier and electronic conduction more readily occurs across this junction. (c) The voltage polarity is reversed and initially the opposite interface is depleted of defects resulting in a barrier at this interface until enough time has elapsed for defects to migrate to this interface and reduce the effective barrier. From Mares et al. 2013.[54]

3.3 NiO:pSi nanocomposites

In this section, the fabrication of nanocomposite NiO:pSi films for investigation of variable conductivity is described. Electrical characterization by sinusoidal voltage sweep and a current saturation technique resulted in the observation of memristive behavior. The current saturation data were successfully fit to a device-level model as has previously been described in.[54]

Fabrication and materials characterization

Electrochemical etching of Si was performed in an PTFE etching cell as described previously in **Sections 1.1** and **2.2**, from (100)-oriented n^+-type Si (Sb-doped, 0.01-0.02-Ωcm) using an electrolyte solution of 25% aqueous hydrofluoric acid (48-50% v/v), 74.9% DI-H_2O and 0.1% NCW-1001 surfactant v/v. Etch current densities varied from 15 to 25mA/cm^2, producing films with pore openings of approximately 20 to 60nm in diameter as measured from surface image analysis. Etch duration was 240s and yielded pSi films approximately 3 to 4μm thick. The NiO precursor development and its deposition into the pSi films was performed by following the same process described in **Section 2.2** and repeated here for convenience.

The precursor was prepared by dissolving 1g nickel acetate tetrahydrate (NAT) in 20mL of 2-methoxyethanol (2MOE) while stirring at 300RPM with a magnetic stir on a hot-plate set to 60ºC for 1hour. Deposition was accomplished by submerging the pSi in about 15mL of the precursor solution while the solvent was evaporated at 65°C for 18 to 24hours on a hot-plate, filling the pores with precipitated precursor. After deposition, the samples were annealed at 700°C for 2 hours in air to form NiO within the pores. The surfaces of the samples were then lightly polished using 0.1μm-grain alumina lapping films to remove any continuous superficial NiO layer and prepare the surfaces for deposition of electrical contacts. Parallel and interdigitated planar Au electrodes were patterned and deposited by photolithography and thermal evaporation, respectively. Contact separations of 5μm and 20μm were tested.

Figure 3.3a shows an oblique angle SEM image of a fabricated device with Au electrodes deposited on the surface. **Figure 3.3**b provides elemental mappings by energy-dispersive x-ray spectroscopy (EDX) of the cross-section of a fabricated device. The mappings show the spatial distribution of the various elements present: Si, O, Ni and Au. Au is only present on the surface, as expected due to the electrode placement. Both O and Ni distributions are uniform throughout the pSi layer indicating effective infiltration of the precursor solution. XRD of a NiO:pSi device collected from a Scintag X1 system (Cu-kα, λ = 1.54056Å) is provided in **Figure 3.3**c. The labeled (111), (200), and (220) peaks indicate the expected cubic rock salt structure of NiO.

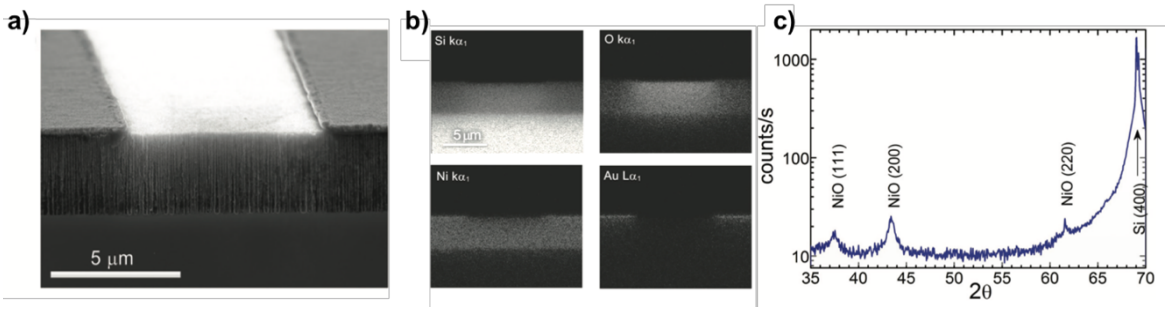

Figure 3. 3 (a) SEM image at an oblique angle of a NiO:pSi device showing the cross-section and surface with 5μm-separated Au-contacts. (b) Elemental mapping of the NiO:pSi cross-section showing the presence of Ni and O throughout the pSi layer. Au is present only at the electrical contacts. (c) XRD of a NiO:pSi device showing NiO in the cubic rock salt crystal structure. Adapted from Mares et al. 2013.[54]

Electrical Characterization

Electrical characterization was performed using a Keithley source-meter controlled by custom LabVIEW routines. Tungsten probes were used to make electrical contact to the electrodes.

Voltage sweep

A common technique employed to confirm variable conductivity is to perform a voltage sweep on a device. Such testing should result in an I/V hysteresis curve that is collapsed (pinched) at the origin. **Figure 3.4** shows such I/V curves for a NiO:pSi device, cycled here under a sinusoidal voltage at 0.1Hz and increasing amplitude from 0.5 to 5V. The voltage sweeps result in currents that are nearly symmetric about the origin. Such behavior would be expected as the device is symmetric with no preferred operation polarity. The device also shows an increase in the conductivity with increasing voltage amplitude when in the high resistance state. This is reasonable considering the proposed mechanism described in **Section 3.1** in which the continued accumulation of mobile defects at the NiO/Si interfaces causes the perpetual reduction in an effective potential barrier that allows increased charge flow.

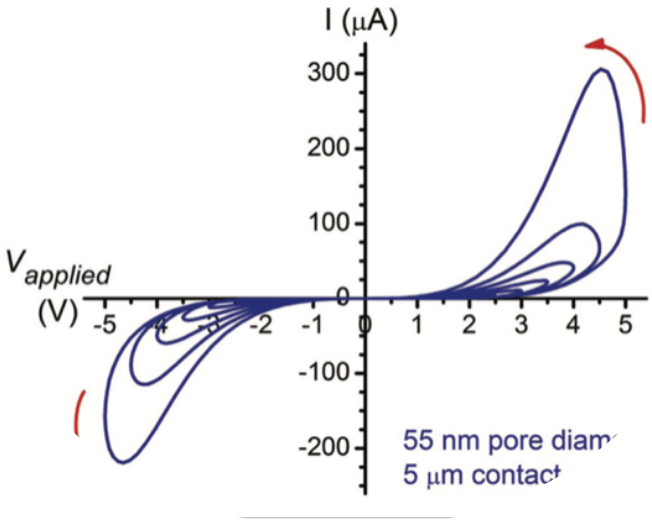

Figure 3. 4 Multiple I/V curves collected on a NiO:pSi device by sweeping the voltage at 100mHz while increasing the voltage amplitude. The characteristic pinched hysteresis behavior is observed. From Mares et al. 2013.[54]

Looking at the direction of the current, indicated by the arrows, the operational state of the device changes when polarity reverses, i.e. operation switches from a high-resistance state to low-resistance state. This behavior is accounted for in the model presented in **Section 3.1** when discussing the switching of the applied voltage polarity in **Figures 3.2**b and c. In contrast, devices operating under a mechanism of filament formation typically exhibit a crossing behavior, maintaining their conductivity state until a sufficient voltage magnitude is applied.

Current Saturation

Current saturation measurements, in which a constant voltage is applied while the resulting current is monitored, were performed on a NiO:pSi devices. Under such testing, memristive behavior was identified through the observation of a continually increasing current to some maximum value. As described previously in **Figure 3.1** this phenomenon is envisioned as a continuous reduction in an effective interfacial energy barrier to some minimum value. In the measurements presented here, testing was performed on a NiO:pSi device with 44nm pore diameter and 20μm contact separation. Constant voltage steps were held for 300s and ranged from 1 to 6V with a 0.2V step-size (0.5–3kV/cm in 0.1kV/cm increments). After each step, the polarity was reversed, holding the magnitude constant, and held for an additional 300s to effectively "reset" the device. These results are provided in **Figure 3.5**a with every other curve omitted for clarity. In **Figure 3.5**a, it is seen that at each voltage step the current increases exponentially with time. At higher voltages (> 3V), the current seems to level off, reaching a final maximum value that is dependent on the applied voltage. It is also seen that as the voltage increases, the time to reach the maximum current value decreases. Assuming the variation in current is due to the accumulation of ionic defects at the numerous NiO/Si interfaces, the current saturation behavior is indicative of faster transit of the defects across the NiO-filled pore with increasing applied voltage.

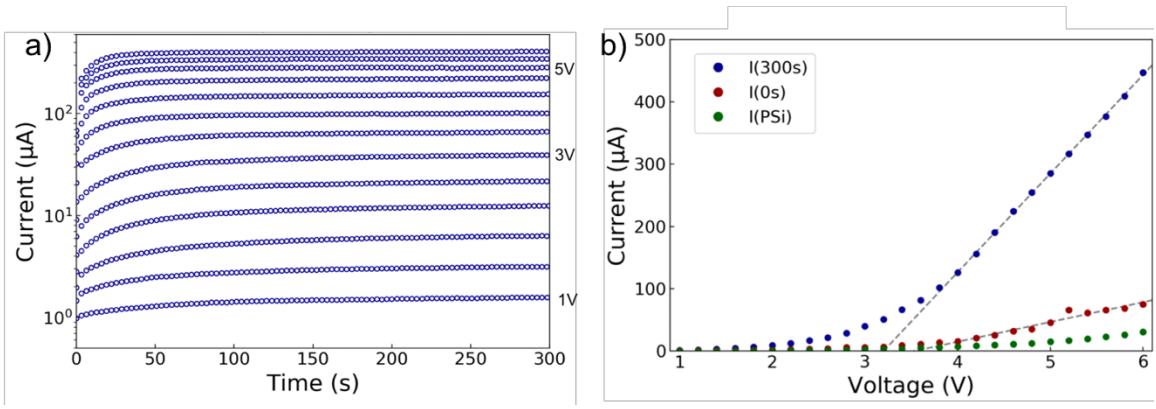

Figure 3. 5 (a) Current saturation curves for a NiO:pSi device subjected to voltages from 1 to 6V (0.2V steps). Each voltage step was applied for 300s after which the polarity was reversed while holding the magnitude constant in order to "reset" the device. Every other curve is plotted here. (b) I/V curves of the initial (red) and final (blue) currents from all data collected via chronoamperometry from 1 to 6V. The pSi (green) data corresponds to a pure pSi device with no NiO. Adapted from Mares et al. 2013.[54]

Figure 3.5b shows the I/V characteristics of the NiO:pSi device extracted from the current saturation data at the initial (0s) and final (300s) time points. For the curve tracing the final time points, the current shows an exponential increase with voltage up to about 4V, above which the current is nearly linear. This behavior may simply indicate that at low voltages (< 3V) the current fails to reach a maximum in the 300s window. The fact that the current increases linearly with voltage above 4V indicates that in this range, the final conductivity is constant. Performing a linear fit to the data for both the initial and final time points in the range of 4 to 6V, resistance values can be assigned from the inverse of the slope, giving approximately constant initial and final resistances of 32kΩ and 6kΩ respectively. Hence, an approximate 5x reduction in resistance occurs over the duration of the measurement (i.e., 300s). As a comparison, the I/V behavior of an identically etched pure pSi device with no NiO was also tested. The current in the pure pSi device is lower and the resistance is calculated to be ~100kΩ based on the slope of the curve at voltages greater than 4V.

Calculation of model parameters from current saturation

In this section, a mathematical description of a device-level model is provided, as reported by Mares et al.,[54] to give insight into the NiO:pSi device behavior. The relevant equations are given and the current saturation data was fit to the model in order to extract relevant parameters, including mobility and the change in effective barrier height. To begin, conduction through a Schottky-type interface is considered, as represented in **Equation 3.1**, where ϕ_b is an effective barrier assumed to vary with time for a given applied voltage: $\phi_b(t)$.

$$I = I_0\, e^{-q\phi_b/kT}\,[e^{\frac{qV_a}{nkT}} - 1] \tag{3.1}$$

In the analysis, when a voltage is first applied, $\phi_b(t)$ is at a maximum at t=0, labeled $\phi_{b,i}$. As $t \to \infty$, $\phi_b(t)$ tends towards a minimum, labeled $\phi_{b,f}$. The variation in $\phi_b(t)$ is described by **Equation 3.2**.

$$\phi_b(t) = (\phi_{b,i} - \phi_{b,f})e^{-t/\tau_{sat}} + \phi_{b,f} \tag{3.2}$$

The effective barrier is taken to change proportional to $\exp(-t/\tau_{sat})$. $\phi_b(t)$ can be plugged into **Equation 3.1** to give the time-dependent form of the current. The characteristic time, τ_{sat}, is related directly to the transit time of the defects across the pore.

Following the derivation by Mares et al.,[54] the ratio of the current at t = 0 and as $t \to \infty$, as represented in **Equation 3.3**, results in a constant term, dependent only on the maximum change in the effective barrier.

$$\frac{I(t\to\infty)}{I(0)} = e^{-q(\phi_{b,i}-\phi_{b,f})/kT} \tag{3.3}$$

From the initial and final currents in the current saturation curves in **Figure 3.5**b, the change in the effective energy barrier is calculated, after subtracting the pSi contribution to the current, as shown in **Figure 3.6**. The change in the effective barrier height increases linearly as the applied

voltage increases to about 3V, above which the data seems to converge to around 60meV. From 1 to 3V, the value is underestimated, which is attributed to the fact that the current did not reach a final maximum (saturation) value within the given test time as indicated from **Figures 3.5**b.

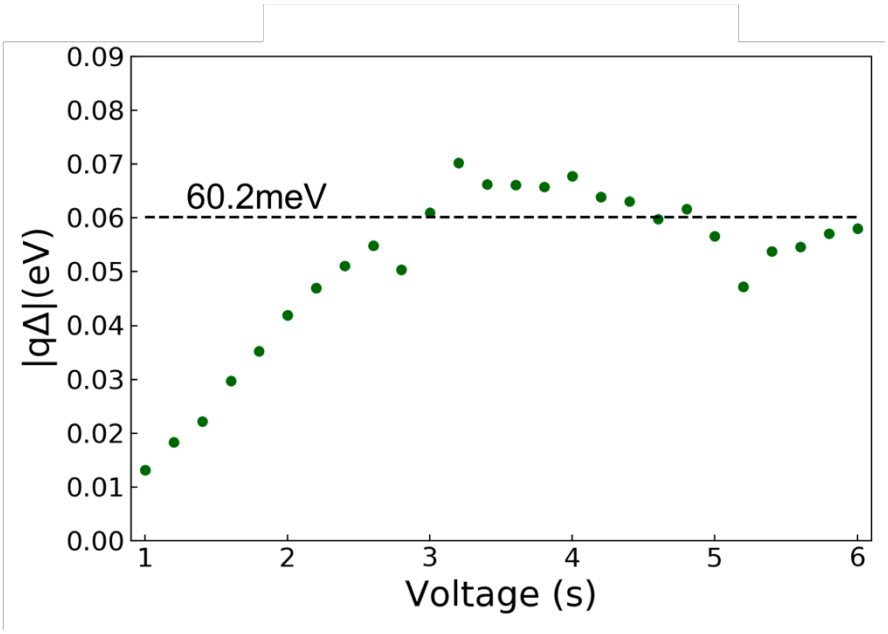

Figure 3. 6 Plot of the change in effective energy barrier calculated from the ratio of the initial and final currents in Figure 3.5b. For voltages above 3V, the current saturates and a consistent value of the effective energy barrier can be determined: 60meV. Adapted from Mares et al. 2013.[54]

Using the value for the change in barrier height from **Figure 3.6** of $q\Delta\phi$ = 60.2meV (average of values ≥ 3V), the data was fit to the simplified model provided in **Equation 3.4** using the non-linear fit routine in Origin. The constant voltage dependent term and the final energy barrier value were absorbed into the leading term I_o`.

$$I = I_o' \, Exp[-q\Delta\varphi \, e^{-\frac{t}{\tau_{sat}}}] \tag{3.4}$$

Fits of the data are provided in the left column of **Figure 3.7**. In **Figure 3.7**a, the fits overlay the data well except within the first few seconds where they seem to overestimate the current.

Nonetheless, the agreement is good and the avg. adjusted $R^2 = 0.960 \pm 0.017$. The values of τ_{sat} derived from the fit are provided in **Figure 3.7**b and appear to decrease linearly with increasing voltage. Under the assumptions here, τ_{sat} is related directly to the transit time of the mobile defects across the NiO-filled pore and therefore it is possible to estimate an ion mobility (μ_{ion}) using **Equation 3.5** where $v_{d,ion}$ is the ion drift velocity estimated by the average distance across the pore divided by τ_{sat} and $\mathcal{E}$ is the applied electric field, approximated from the applied voltage (V_{app}) divided by the contact separation (S).

$$\mu_{ion} = v_{d,ion}/\mathcal{E} \tag{3.5}$$

Here the average pore diameter is 44nm and the contact separation is 20μm. Using the τ_{sat} values in **Figure 3.7**b, μ_{ion} is derived (**Figure 3.7**c) where it is seen that μ_{ion} is around 1 to 2×10^{-10}cm^2/Vs.

Under the assumptions above, the fits in the left column of **Figure 3.7**a correspond to the behavior induced by a single defect type – defects with the same charge, mobility, and effective mass, however, it is probable that more than one defect type may contribute. In such a case, the total current in **Equation 3.4** would be taken to be the summation of multiple terms of the rhs of the equation (see Mares et al.)[54]. To test this hypothesis, a two-term fit to the data was also performed using a second identical term on the rhs of the model **Equation 3.4**. The results of this analysis are provided in the right column of **Figure 3.7**. This two-term fit appears to better agree with the model, especially at the first few seconds where the single-term fit appeared to deviate the most (**Figure 3.7**d). The two-term avg. adjusted R^2 improved to 0.992 ± 0.006. From the two-term fits, two distinctly different linear characteristic times, $\tau_{1,sat}$ and $\tau_{2,sat}$ were obtained (**Figure 3.7**e) from which two ion mobilities were calculated ($\mu_{1,ion}$ and $\mu_{2,ion}$) with approximate values of 5×10^{-11} and 3×10^{-10}cm^2/Vs. Use of a multi-term fit may be justified by the fact that high temperature studies have suggested multiple point defect types in the form of neutral, singly, and

doubly charged Ni vacancies are all present. This is only mentioned to give weight to the reasonableness of a multi-term fit and not as a proof that the contributing defect types are necessarily these.[41]

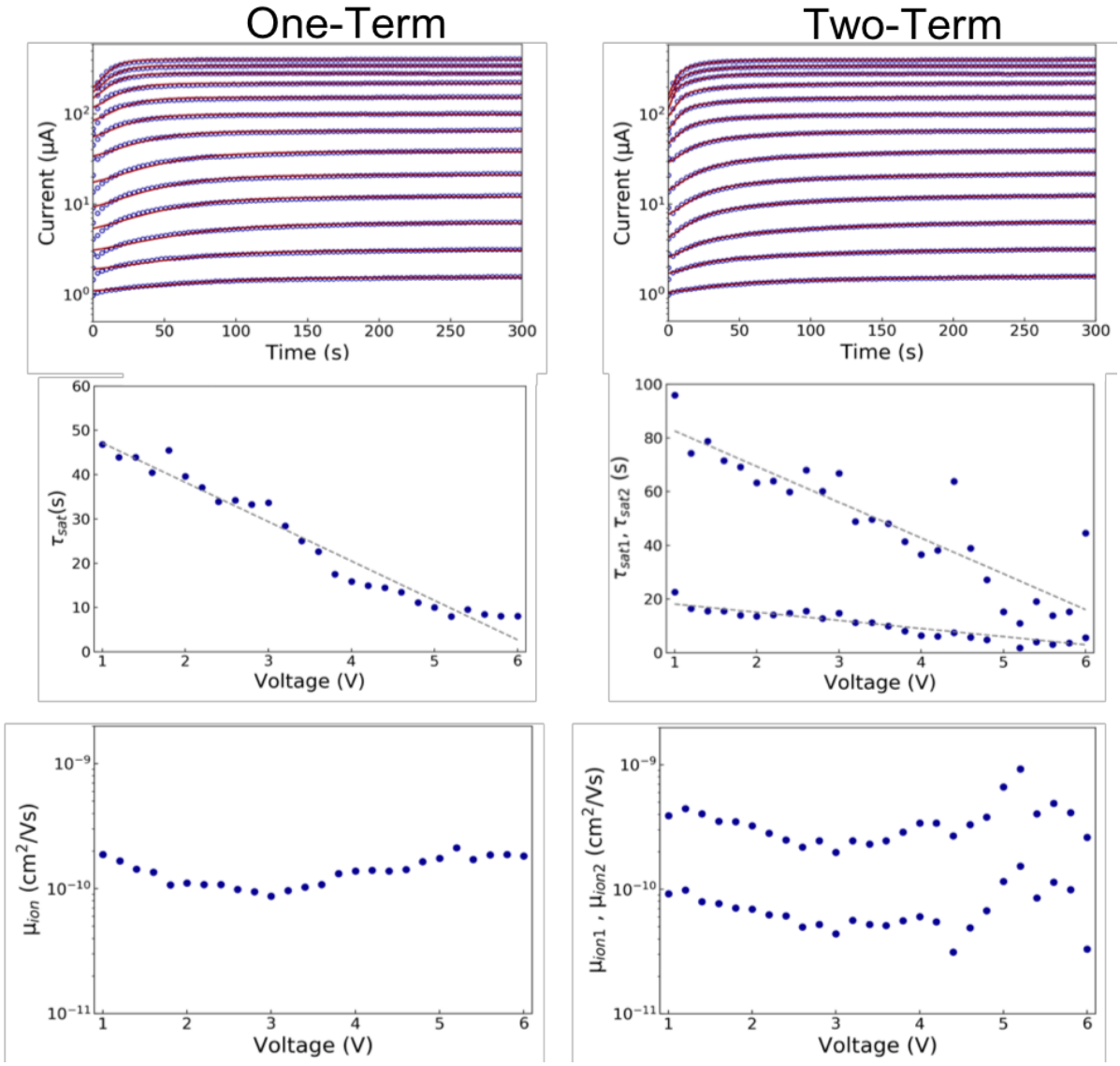

Figure 3. 7 (Left-Top) current saturation curves overlaid with a single-term fit. (Left-Middle) resulting plot of the characteristic time from the single-term fit, and (Left-Bottom) the calculated ion mobility with voltage from the single-term fit. (Right-Top) current saturation curves overlaid with a two-term fit. (Right-Middle) resulting plot of the characteristic time from the two-term fit, and (Right-Bottom) the calculated ion mobility with voltage from the two-term fit. Adapted from Mares et al. 2013.[54]

3.4 TiO_2:pSi nanocomposites

Building on the knowledge established in the fabrication and characterization of NiO:pSi, a second metal oxide, TiO_2, previously known to exhibit memristive properties was implemented in a pSi platform for similar investigation. The TiO_2:pSi devices were also shown to exhibit variable conductivity behavior, however, the additional presence of a charge-storage component was also present, unlike in the NiO:pSi devices.

Fabrication and materials characterization

Nanocomposite TiO_2:pSi films were fabricated from p-type Si wafers etched for 2000sec at a current density of 20mA/cm^2 from (100)-oriented p$^+$-type Si (B-doped, 0.01-0.02-Ωcm). The etching solution was comprised of 30% aqueous HF (48-50% v/v) and 70% EtOH v/v. The resulting pSi films had a pore depth of 30μm and average diameter of approximately 15nm. It is noted that these pSi films were much thicker than those used in the NiO study. This is because after annealing the samples to form TiO_2, more rigorous polishing was necessary to smooth the surfaces for electrode deposition. Unlike NiO which formed loosely attached particulates on the surface that are easily removed, the TiO_2 formed large particles/films that were both harder and firmly attached to the surface. Therefore, use of a polishing wheel and alumina lapping films with incrementally decreasing grain sizes (12μm to 0.3μm) implemented to smooth the surface.

TiO_2 was formed in the pores by thermal decomposition of a solution precursor. The precursor was prepared by dissolving 1g of titanium (IV) ethoxide into a solution of 10mL of isopropyl alcohol and 0.1mL of hydrochloric acid.[112, 113] The mixture was stirred for 30 minutes at 500RPM on a hot-plate set at 60°C to dissolve the titanium ethoxide. Deposition of the precursor into the pSi pores required submerging the pSi sample into the precursor at room temperature for 30 minutes after which the sample was removed. Any precipitate remaining on the surface was removed by rinsing with ethanol. The film was then placed on a hot-plate for 1 minute at 100°C

to evaporate residual solvent. The pSi sample was re-submerged in the precursor for an additional 30 minutes and the process was repeated to increase pore filling. The samples were annealed at 500°C, after which the surface was polished, as described at the beginning of this section. Au parallel electrical surface contacts were patterned by photolithography and deposited via thermal evaporation with a thin (few nm) Cr adhesion layer. A plan-view of a device with contact separation of 50μm is shown in **Figure 3.8**. **Figure 3.9** provides a cross-section SEM image of the entire 30μm thick pSi layer along with EDX elemental mapping of Si, O, and Ti throughout the layer along with the corresponding spectrum. The mapping shows Si and O to be distributed uniformly throughout the layer. Ti is also present throughout the layer, as well, but is mostly concentrated within 5 to 10μm of the surface. A non-uniform Ti distribution may be due to the fact that the pSi layer is too thick for full infiltration. Increasing the number of iterations of the deposition process may result in better infiltration.

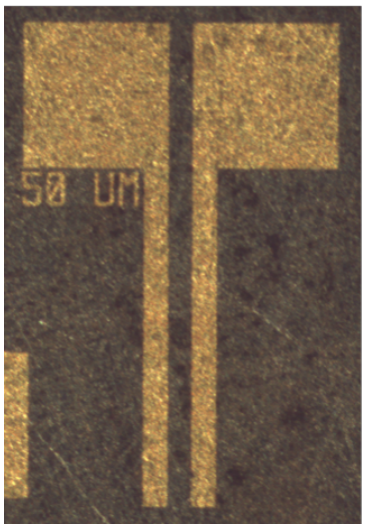

Figure 3. 8 Optical image of TiO_2:pSi device with 50μm separated parallel contacts.

XRD spectra were collected at the Center for Nanophase Materials Science (CNMS) at Oak Ridge National Laboratory using a PANalytical X'Pert Pro Powder Diffractometer (CuKα x-

ray source, λ= 1.54059Å). **Figure 3.10** shows XRD spectra of TiO_2 annealed on planar Si and in pSi at different temperatures over the 2θ range of 21º to 40º. In **Figure 3.10**, the red spectra correspond to TiO_2 on a planar cSi substrate annealed at temperatures ranging from 500ºC to 1100ºC. For planar Si samples, at temperatures of 500ºC and 700ºC the spectra exhibit peaks that are identified with the anatase phase (101) and (004) crystal planes at 25.2º and 37.8º, respectively. At temperatures of 900ºC and 1100ºC the spectra exhibit peaks identified to both the anatase and rutile phases with the rutile (110) and (101) peaks at 27.2º and 36º, respectively, becoming more prominent as the anatase peaks are reduced. The blue spectra correspond to TiO_2 annealed on pSi substrates at temperatures of 500ºC and 800ºC and exhibit no prominent, identifiable peaks associated with TiO_2. Additionally, at 800ºC increased oxidation of the pSi is likely occurring given the very broad background peak, in agreement with the results in chapter 2, which would further limit electronic conduction. The lack of TiO_2 XRD peaks in the pSi samples could be due to a highly disordered amorphous phase and/or extremely small crystallite sizes with very short-range order. The only peak present in the TiO_2:pSi samples correspond to that of Si as can be seen by comparing to the green Si spectra near 33º.

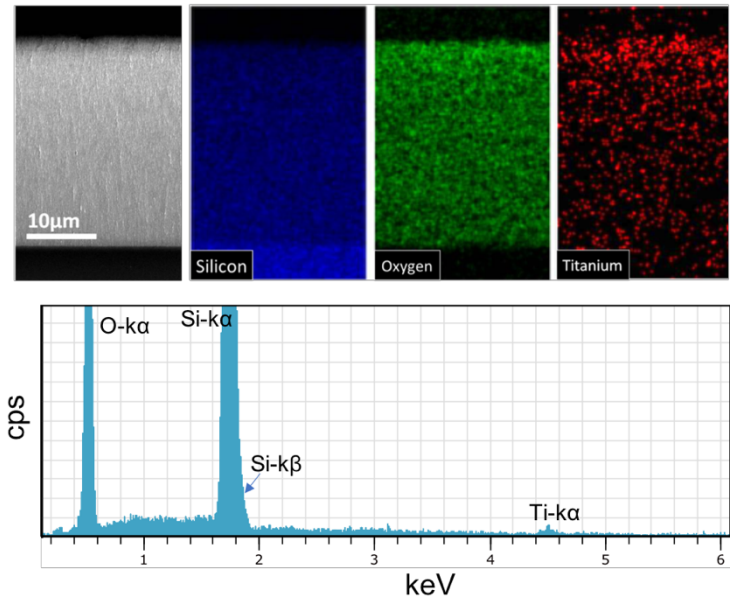

Figure 3. 9 (Top) SEM cross-section image of the full pSi layer along with elemental mapping of the Si, O, and Ti, throughout the layer. (bottom) The spectrum associated with the mappings.

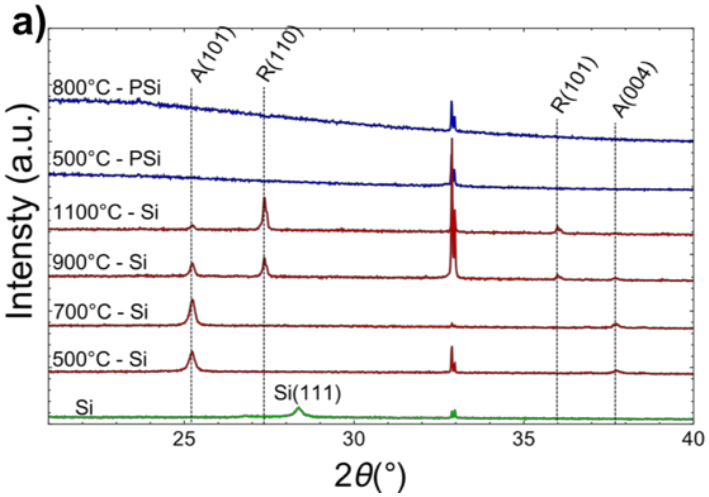

Figure 3. 10 XRD spectra over the range of 21° to 40°-2θ of the TiO_2 precursor annealed at different temperatures in pSi (blue) and on planar Si (red) as well as a bare Si substrate (green) for comparison.

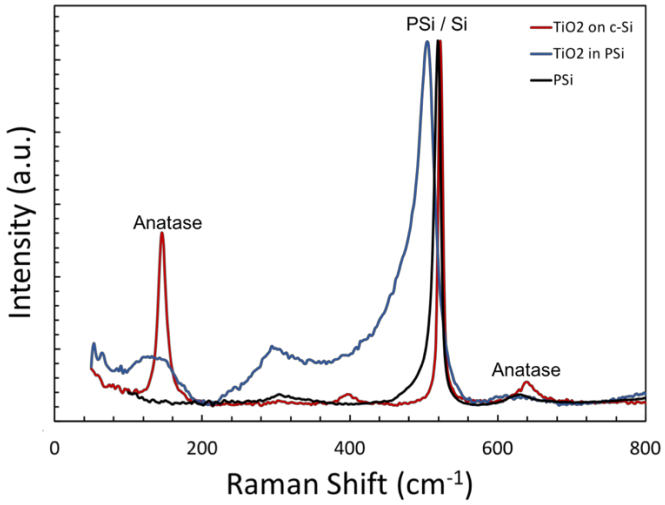

Figure 3. 11 Raman spectra of TiO_2 annealed at 500°C in pSi (blue) and on cSi (red). The strong peak around 144cm^{-1} in the TiO_2 on c-Si substrate corresponds to anatase. This peak is still present but much broader in the TiO_2:pSi composite and is not observed at all in a bare pSi sample (black). The bare pSi sample was etched at different conditions (45mA/cm^2) with a thickness of 4.6µm.

Raman spectroscopy was performed on TiO_2:pSi annealed at 500°C in pSi and on cSi (**Figure 3.11**). A sharp peak at 144cm^{-1} is observed for the TiO_2 sample annealed on planar cSi (red) corresponding to anatase.[114] This peak is very broad in the TiO_2 on pSi (blue) sample and is not observed in the pSi only sample. The large peak in the TiO_2 on cSi sample at 520cm^{-1} corresponds to Si which in the pSi only sample is shifted slightly down due to strain induced in the Si lattice. This peak is shifted much lower in the pSi sample with TiO_2, to 510cm^{-1} as the etching conditions were much different (20mA/cm^2, ~30µm thick) compared to the pSi only sample (45mA/cm^2, ~4.6µm thick). The other anatase peaks at 400 and 650cm^{-1} in the TiO_2 on cSi are much smaller, and are not observed in the TiO_2:pSi sample. The form of TiO_2 in pSi annealed at 500ºC seems to tend towards anatase, based on evidence from the Raman analysis, but it is likely a highly disordered system exhibiting amorphous and a short-range order.

Electrical characterization

Cyclic voltammetry

Figure 3.12 shows the I/V curves resulting from performing cyclic voltammetry (i.e. applying periodic linear voltage sweeps) for a TiO_2:pSi device with parallel contacts having a 50μm contact separation. The devices were cycled at 100mV/s, 500mV/s, and 1V/s over a range of voltage amplitudes from 15 to 30V, and normalized to the contact separation (3kV/cm to 6kV/cm). At 1V/s, and 500mV/s, the I/V curves exhibit variable conductivity with a measure of non-volatility indicated by the open loops at the far extents of each curve. There is also some evidence of charge-storage occurring indicated by the open loop centered at the origin.

In the I/V plots at 1V/s and 500mV/s, ignoring the charge-storage component for the moment, it can be seen that as the voltage increases in magnitude from 0V, the device is effectively in a high resistance state of 49.3 ± 3.4MΩ as determined from a least-squares fit of the linear region. As the voltage continues to rise, there is a transition to a low resistance state which is estimated to be 10.5 ± 2.4MΩ. At 100mV/s, there is no longer evidence of significant memristive behavior as the outer portions of the I/V curves have collapsed to single values. Such behavior may be expected under slow sweep rate conditions if there is a maximum change in the effective potential barrier as suggested from the NiO:pSi current saturation studies. At slow sweep rates, this point would be reached at lower voltages and any variation in conductivity beyond this point would be minimal. This, in effect, results in a measured current that ceases to change between increasing and decreasing portions of the voltage sweep.

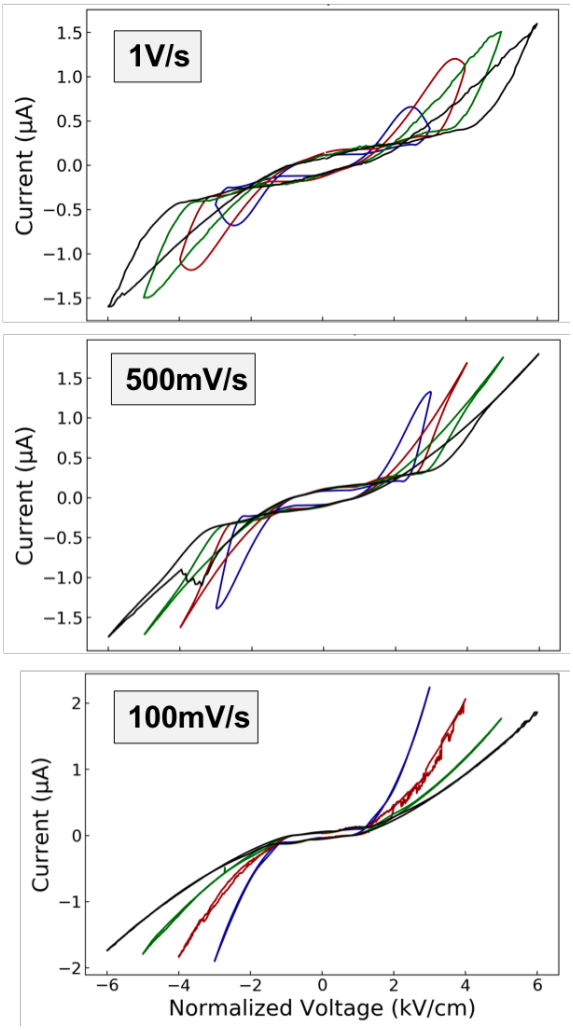

Figure 3. 12 I/V curves collected by performing cyclic voltammetry on a TiO_2:pSi device at the sweep rates indicated with maximum voltage amplitudes of 15V, 20V, 25V and 30V. Curves collected at higher sweep rates show the characteristic pinched hysteresis expected for memristor devices. All curves show evidence of a charge-storage component.

Another interesting observation in the 100mV/s I/V curves is that the conductivity seems to decrease as the maximum voltage increases. It would be expected that as the voltage increases the overall conductivity in the low resistance state would increase, or stay constant, as this would result in increased defects at the interface. However, clearly here the approximate slope of the curves above 6V decreases with increasing voltage amplitude from ~4MΩ to 13MΩ. A possible explanation is that competing mechanisms are at play, wherein the accumulation of defects at the

interfaces causes a reduction in an effective barrier, but the depletion of these defects at the opposite side causes an increase in the resistance of the TiO_2 as this region becomes more stoichiometric. Such behavior has been suggested as a reason for memristance in previous investigations of TiO_2.[98] The open loop centered about the origin for all I/V curves in **Figure 3.12** indicates the presence of a charge-storage component which prevents the hysteresis loop from being truly pinched at the origin. The charge-storage may be attributed to both an electric double layer (EDL) capacitance at the numerous TiO_2/Si interfaces due to the build-up of charge in the form of mobile ionized defects. Additionally, there may be some reversible redox reactions taking place across the interface. Such behavior has been suggested as inevitable in all ion conducting memristive devices.[115] This effect may have been occurring in the NiO:pSi devices as well but was not large enough to be observed.

Current Saturation

Current saturation experiments were carried out on a TiO_2:pSi device with 50μm parallel contacts at constant voltages of 2 to 30V with a step-size of 2V (0.4 to 6kV/cm, step of 0.4kV/cm). Each voltage step was held for 300s. The resulting current at each step is shown in **Figure 3.13**. After each 300s voltage step is applied the device is held at a constant 0V for an additional 300s before the next voltage step is applied. Therefore, between each voltage step, there is no reverse polarity "reset" voltage applied to the device. The reason for this was to test the charge-storage component that had already been observed in the CV curves in **Figures 3.12**.

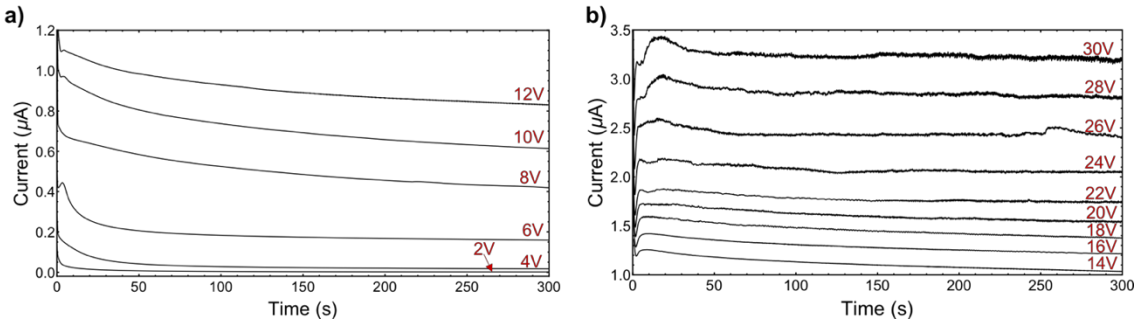

Figure 3. 13 Current saturation curves collected on a TiO_2:pSi device by applying constant voltage for 5 minutes. Voltages of 2V to 30V (2V steps) were applied. (**a**) currents collected from 2V to 12V, which exhibit almost entirely charge-storage behavior. (**b**) currents collected from 14V to 30V which show variable conductivity (memristive) behavior in addition to charge-storage.

Figure 3.13a shows the currents collected at voltages of 2 to 12V. These curves exhibit almost entirely charge-storage behavior indicated by the near continuous decay in the current for the entire 300s duration. At 6, 10, and 12V there does seem to be a small peak in the current around 5s indicative of a redox reaction. **Figure 3.13**b shows currents collected at 14 to 30V. For each of these currents, there is an initial decay within the first 3s, commensurate with charge-storage, followed by a rise in current which could be attributed to ion defect migration towards the TiO_2:pSi interfaces causing a change in the conductivity of the device. Several of these curves also show evidence of redox reaction peaks which are particularly obvious at about 20s into the currents collected at 28V and 30V.

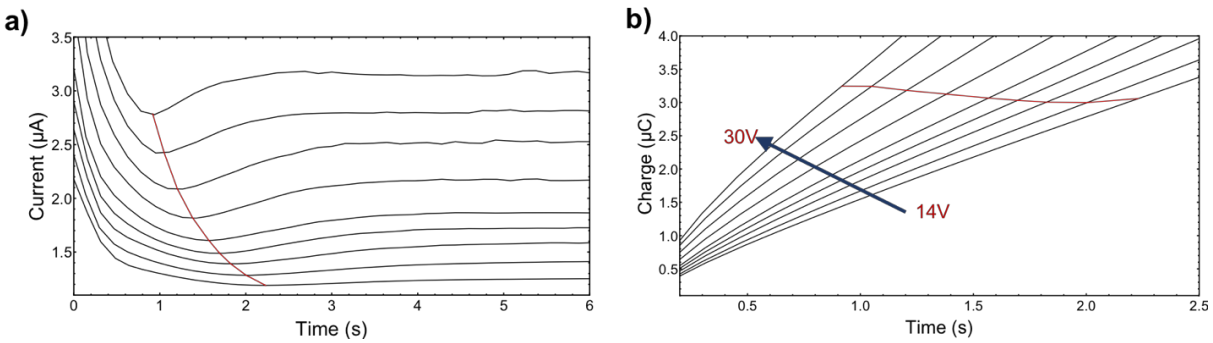

Figure 3. 14 (**a**) Initial 5s of each current saturation current collected from 14V to 30V on a TiO_2:pSi device. The red curve indicates the transition from the charge-storage region to the memristive region. (**b**) Integrated currents from (a) with the red cross-cut line tracing the point through each curve when the transition from charge-storage to memristive regime occurs.

Figure 3.14a shows the first 6sec of the currents collected from 14V to 30V. The red cross-cut line traces out the minimum value of each of the currents which demarcates the transition from the charge-storage regime to the memristive regime. A similar distinction of device behavior into these different regimes has also been described previously for $SrTiO_3$.[33] Integrating the currents in **Figure 3.14**a over the first few seconds results in the plot in **Figure 3.14**b. The red cross-cut here corresponds to the red line in (a) and seems to indicate that a near constant charge of ~3.1μC accumulates in the device prior to the onset of the memristive region at all voltages ≥ 14V.

Figure 3.15a shows selected 0V discharge curves after the indicated voltage has been applied. The 4V and 6V curves are provided to show that an exponential decay in the current is observed after these voltages have been applied similar to capacitive discharge. However, at 14V a battery-like redox shelf is appearing in the discharge curve associated with a reversible reaction. Similar behavior is observed after 30V, but only a slight increase in the current has occurred. The plot in **Figure 3.15**b was acquired by integrating the discharge currents after each voltage step and shows the total charge that accumulated with each voltage. The charge rises rapidly with increasing voltage from 2V to 8V and then begins to level off. From 14V to 20V the total charge

is nearly constant at about 6μC and from above 20 to 30V the accumulated charge only gradually rises with increasing voltage to about 6.4μC. This seems to indicate that the device only stores a maximum of ~6μC of charge, at least at the voltages tested here. The charging effects observed in the TiO_2:pSi device is in contrast to what was observed in the NiO:pSi device which showed no perceptible charging effect. This may be due to a difference in the charge-state of the mobile defects, the fact that the thickness of the TiO_2:pSi layer was ~8x larger which provides a much greater surface area over which charging could take place, or that obvious reversible redox reactions were occurring.

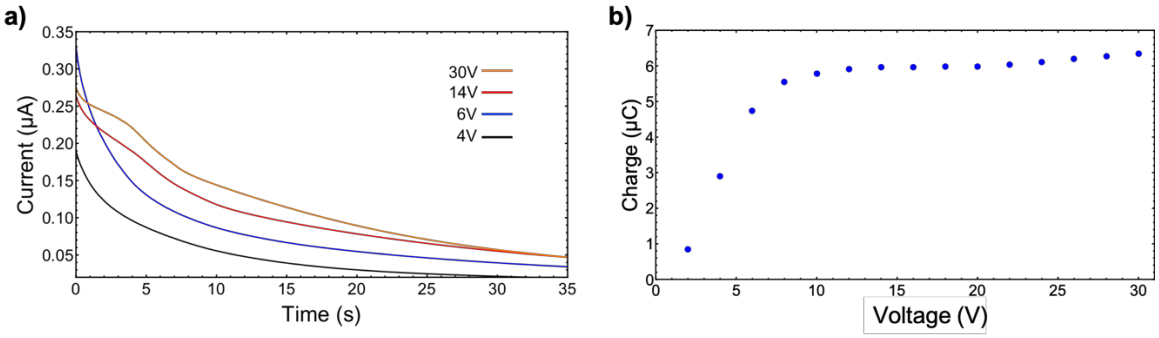

Figure 3. 15 (**a**) Selected 0V discharging current collected after each voltage step in Figure 3.13. (**b**) plot of the total integrated discharge currents (total stored charge) vs. voltage of the previously applied current saturation step.

3.5 Conclusion

In summary, both NiO:pSi and TiO_2:pSi nanocomposite devices have been investigated for possible application as memristors. XRD of NiO:pSi revealed the presence of the expected rock-salt crystal structure, while a combination of XRD and Raman spectroscopy analysis revealed TiO_2 to likely be amorphous or possibly possess short range anatase phase. Electrical characterization carried out by sinusoidal voltage sweep of a NiO:pSi device produced the characteristic pinched hysteresis I/V curve exhibited by memristive devices. Current saturation measurements on a

similar device produced a continuously increasing current up to some maximum value that is dependent on the applied bias. Analysis of this data suggested near constant initial and final resistance values of 32kΩ and 6kΩ, respectively, in the voltage regime above 4V. A device-level model was also described and fit to the current saturation data of the NiO:pSi device. The model considers that the accumulation of mobile ionic defects at the numerous NiO/Si interfaces causes a change in an effective energy barrier, which in turn causes an increase in charge-flow across the interface. A two-term fit of the model was shown to be sufficient to accurately fit the data, and from which the estimation of ionic defect mobilities in the NiO were estimated to be ~0.5 and 3 x 10^{-10} cm^2/Vs.

Investigation of the TiO_2:pSi devices by cyclic voltammetry also produced hysteresis I/V curves, but the presence of a significant charge-storage component prevented the full collapse of the curves at the origin. The charge-storage effect is attributed to electrochemical capacitive and reversible redox processes at the numerous TiO_2 – pore wall interfaces. The variation in conductivity was observed to be dependent on the sweep rate, with open, outer loops at higher rates of 1V/s and 500mV/s, but loops collapse to single values at 100mV/s. This was explained by considering that a maximal change in the effective energy barrier occurs at lower voltages when the sweep rate decreases. Current saturation measurements collected on TiO_2:pSi devices showed memristive behavior as well as charge-storage behavior. The total charge stored at each voltage was determined by integration of the 0V discharge curves after each voltage step. Above 8V, the total charge converges to approximately 6μC. It was also demonstrated that only at voltages of 14V and above was the presence of a memristive effect observed. However, even in this range, initial charging of the device up to ~3.1μC was necessary prior to the observation of memristance. The presence of the charge-storage component made direct fitting of the model to the TiO_2:pSi device data ambiguous. Even so, similarities in device behavior of both TiO_2:pSi and NiO:pSi

devices support the assertion that the underlying mechanism of ionic migration is directly applicable to the TiO_2:pSi system, as well. For instance, both TiO_2:pSi and NiO:pSi devices were found to be symmetric in their behavior (no preferred polarization of the electrodes), and both exhibit non-crossing I/V hysteresis behavior.

In summary, both metal oxide:pSi nanocomposites tested here have been demonstrated for memristive devices with much larger dimensions than those typically investigated. It is envisioned that each metal-oxide filled pore serves as a single element and their collective operation results in a macroscale effect at reasonably low electric fields. Such devices may not be viable for traditional memory applications, but it could be expected that other novel and unique applications would benefit from large-scale discrete devices. Furthermore, these devices are produced directly within a crystalline Si wafer making a path for simple integration feasible.

CHAPTER 4

INVESTIGATIONS OF NICKEL OXIDE DEPOSITED ONTO CARBON-COATED POROUS SILICON FOR ELECTROCHEMICAL ENERGY-STORAGE

In this chapter, nanocomposites of nickel oxide (NiO) / carbon-coated porous Si (C-pSi) are presented as a versatile platform for development of electrochemical energy-storage electrodes that are compatible with on-chip integration. The use of high surface area C-pSi as a constituent material facilitates the growth of NiO within the nanoscale pores to form electrochemically active nanoparticles. The properties of the nanocomposites are characterized by scanning electron microscopy (SEM), energy-dispersive x-ray spectroscopy (EDX), x-ray diffraction (XRD), and Raman spectroscopy. Three-electrode experiments are performed in an aqueous electrolyte and reveal a capacitive-like, charge-storage component superimposed on conventional battery-like Faradaic redox reaction peaks. A maximum capacity of 6.6μAh/cm^2 was observed, and a maximum capacitive contribution is measured to be near 25mF/cm^2, which is comparable to other reported supercapacitors for on-chip applications. Moreover, the rate performance is enhanced when operated in a capacitive regime (reduced voltage window) because charge-storage occurs at or near the surface of the active NiO in contrast to Faradaic reactions occurring within the interior of the NiO at higher voltages.

4.1 Introduction

Electrochemical energy-storage materials and structures for integration on-chip have received significant research interest for potential power solutions in a variety of applications including MEMS technologies, wireless sensor network systems, photovoltaic-cells, and implantable medical devices.[116-120] These on-chip energy-storage components are often referred to as micro-

batteries (MBs) or micro-supercapacitors (MSCs) depending on their operational mechanisms and behavior. Because batteries are capable of storing greater amounts of charge (i.e. energy), and supercapacitors are capable of charging and discharging more rapidly (i.e. operate at higher power) and have longer cycle life-time, these technologies can be complementary in their application areas.[116, 117, 121] Batteries rely on reversible Faradaic redox charge-transfer reactions between an electrolyte and an active electrode material (e.g., $LiFePO_4$ and graphite in Li-ion batteries, or $Ni[OH]_2$ in Ni metal-hydride batteries) in which active ions diffuse into the interior of the active electrodes. This diffusion process limits the charging rate, but can allow the entire bulk material to contribute to charge-storage. When battery electrodes are characterized by cyclic voltammetry (CV), redox reactions manifest as current peaks above a minimum potential that depends on the active material. Supercapacitors, on the other hand, have current/voltage behavior similar to traditional capacitors and exhibit a mostly rectangular CV profile. Supercapacitor electrodes are classified as either electric double layer capacitors (EDLCs) for which charge is stored by electrostatic adsorption at a polarized electrode/electrolyte interface, or as pseudocapacitors operating by ultrafast reversible Faradaic charge-transfer. Although the pseudocapacitive mechanism is similar to that of batteries, pseudocapacitance is commonly attributed to surface and/or near surface reactions that occur across a broad range of potentials.[122] EDLCs are most commonly implemented using various high surface area allotropes of carbon as the active materials.[123-125] Typical, pseudocapacitive materials include various nanostructured metal-oxides and conductive polymers.[18, 20, 43, 126-132]

For on-chip applications, electrochemical energy-storage components are typically fabricated on top of the chip or are separately attached to a Si-wafer after fabrication. However, a few approaches facilitate the formation of energy-storage components directly on the Si chip. For example, dry etching can be used to create Si channels for developing interdigitated electrodes and

electrochemical etching of Si can be used to create high surface area porous silicon (pSi) nanoscale scaffolds into which carbon and/or other electrochemically active electrode materials can be deposited. pSi is a particularly attractive platform for high surface area energy storage due to its tunable parameters of surface area, pore size, porosity, and thickness which can easily be controlled through appropriate selection of etch current, time, and etchant solution concentration. Advancements in recent years in the incorporation of passivating layers, such as carbon or titanium nitride, onto the surface of pSi films increase conductivity and mitigate corrosion, and have led directly to successful fabrication of pSi supercapacitors and Li-ion battery anodes.[3-5, 13, 97, 133, 134]

In the work presented here, C-pSi is combined with electrochemically active NiO nanoparticles to form a versatile electrochemical energy-storage platform embedded within a Si-wafer, providing a path for simple on-chip applications. While NiO nanomaterials have been studied extensively for pseudocapacitive charging, to my knowledge, no experimental demonstration of NiO nanoparticles inside pSi for electrochemical energy storage have been reported.[18, 44, 130] This chapter discusses the characterization of NiO:C-pSi electrodes prepared with different concentrations of a NiO precursor solution by three-electrode cyclic voltammetry (CV) and galvanostatic charge-discharge (GCD) measurements in 0.5M KOH(aq.). Charge-storage in the NiO:C-pSi electrodes is observed to occur via Faradaic reactions in the NiO in addition to a significant EDLC type charge-storage contribution by both carbon and NiO, as indicated by well-defined reaction peaks superimposed on a wide, rectangular CV profile. The best areal capacity of these prototype devices is found to be approximately 6.6μAh/cm^2, giving a volumetric capacitance of 14.3mAh/cm^3. The devices exhibit good stability up to 50mV/s by CV and 2mA/cm^2 by GCD measurements. Calculation of the average capacitance at potentials less than the onset of the Faradaic reaction peaks (< 350mV vs Ag/AgCl) gives values near 25mF/cm^2 at 0.1mA/cm^2, which is comparable to many reported MSC electrodes and an approximate 2.5-

fold enhancement over similarly prepared C-pSi electrodes with no active NiO. Investigations into this composite NiO:C-pSi for electrochemical energy-storage demonstrates the wide versatility of this platform for use in both battery and supercapacitor implementations on-chip.

4.2 Characterization

Materials characterization was carried out by numerous techniques, including scanning electron microscopy (SEM), which was performed on a Zeiss Merlin SEM tool with energy-dispersive X-ray (EDX) spectroscopy capabilities. Raman spectroscopy was performed on a Thermoscientific DXR Raman microscope with a 10X objective lens and a laser wavelength of 532nm at 1mW. The mass of each electrode was measured using a Mettler-Toledo microbalance scale with 0.01mg resolution. Powder X-Ray Diffraction (XRD) was performed on a Rigaku Smart Lab with a Cu-Kα source (λ = 1.54058Å).

Electrochemical characterization techniques (CV and GCD) were performed on a Metrohm Autolab multichannel instrument controlled via NOVA software. The CV and GCD area-normalized capacity was calculated by integrating the current with respect to the discharge time, as shown in **Equation 4.1**, where Q_t is the total discharge capacity in Coulombs, I is the current, and t is time.

$$Q_t = \int I \cdot dt \tag{4.1}$$

Equation 4.1 gives the charge in Coulombs. Conversion to the standard unit of Ampere • hours (Ah), the Coulomb charge is multiplied by the factor 1h/3600s. For both CV and GCD, the discharge time was taken to be the total time negative current was observed (CV) or applied (GCD). Capacitance was calculated by dividing the capacity (in Coulombs) by the discharge voltage window, as given in **Equation 4.2**, where ΔV is the discharging potential window (i.e., voltage window over which the current is negative) and C is the capacitance.

$$C = \frac{Q_t}{\Delta V} \tag{4.2}$$

Area and volume normalized capacity and capacitance were calculated by dividing each value by the electrode test footprint area and volume. The test footprint area of each electrode during 3-electrode characterization was 0.707cm^2. To clarify, when preparing electrodes, a large area of 7.54cm^2 was initially etched from which multiple electrodes could be prepared. The final test area of each electrode however is only 0.707cm^2. The thickness of the porous layer was ~4.6μm.

4.3 Fabrication

Figure 4.1 schematically illustrates the fabrication steps necessary to prepare the NiO:C-pSi electrodes. Photographs of electrodes through each stage of fabrication are provided in **Figure 4.2**. The first step depicted in **Figure 4.1** is the preparation of the pSi film, which as in the previous chapters, is carried out by electrochemical etching of a Si wafer using a Keithely 2425 source-meter and custom-built LabVIEW routines. Single crystal (100) p^+-type wafers (resistivity = 0.01 to 0.01Ω-cm) were used in this study. The etching solution was composed of 30% aqueous hydrofluoric acid (HF) solution (50:50 v/v HF:H_2O) and 70% EtOH. All pSi samples were etched at a current density of 45mA/cm^2 for 180s over a region of 7.54cm^2. The resulting pSi layer thickness was approximately 4.6μm ± 0.2μm thick. Image (1) in **Figure 4.2** shows a picture of the sample surface just after etching with the center circular region corresponding to the pSi. The nonuniformity in color indicates slight nonuniformity in the optical thickness across the pSi film. The silvery area surrounding the pSi is unetched Si. **Figure 4.3**a provides surface and cross-sectional SEM images of a freshly etched pSi sample. The cross-sectional image reveals that the vertically aligned pores possess an intricate morphology characterized by numerous small branches extending from the pore walls. The average pSi pore diameter was determined by image analysis of multiple SEM images of the pSi surface using ImageJ (Rasband 1997-2014) by

methods described in **Chapter 2** and **Appendix A**. **Figure 4.4** shows the resulting distribution of pore diameters which approximate a normal distribution (overlaid peak fit). The data mean pore diameter was found to be 15.9nm with a standard deviation of 7.3nm. The porosity of the pSi samples was measured to be approximately 65 to 70% based on an effective medium approximation (**Section 1.4**).

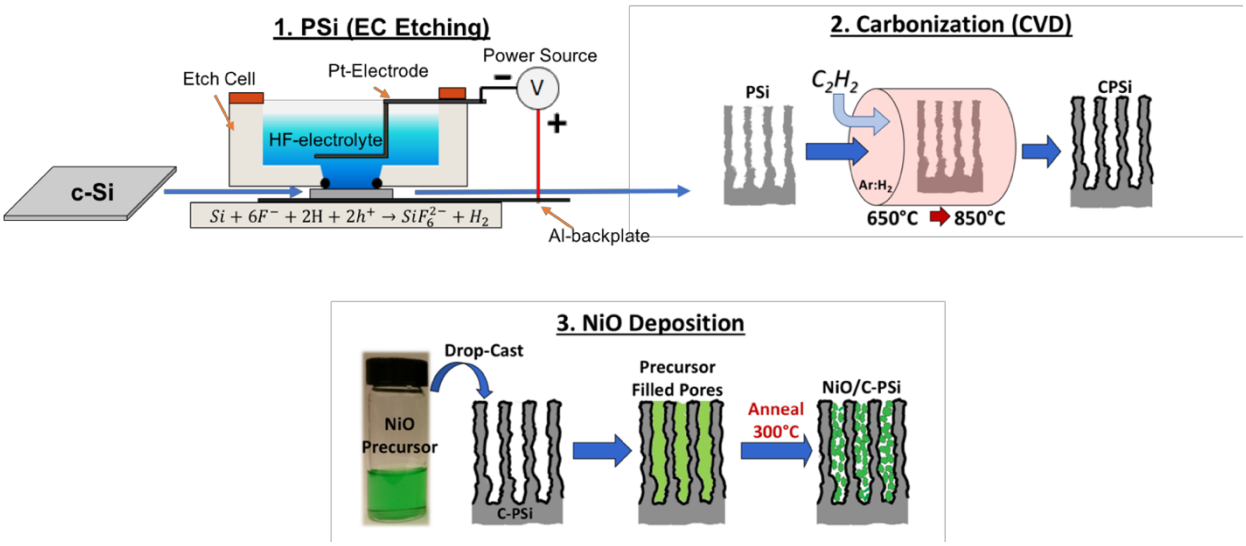

Figure 4. 1 Schematic illustration of the main fabrication steps involved in preparing NiO:C-pSi electrodes. (**1**) Electrochemical etching of pSi, which proceeds according to the reaction provided. (**2**) Deposition of a conformal carbon coating onto the pSi by CVD using acetylene (C_2H_2) as the carbon source in an Ar:H_2 atmosphere. (**3**) Deposition of NiO precursor solution on C-pSi by drop-casting, followed by drying in air at RT and subsequent annealing at 300ºC in air.

After etching, the sides of each sample were cleaved [image (2) in **Figure 4.2**]. Cleaving was necessary in order for the samples to fit the CVD system required for the carbonization step [step (2) in **Figure 4.1**]. Carbonization of the pSi is necessary in order to passivate the surface and prevent immediate corrosion in the basic KOH electrolyte used for electrochemical testing. The process for carbon deposition used here was developed by collaborators.[3] Briefly, the pSi samples are placed in a quartz tube which is evacuated to an internal pressure of 0.2 to 0.3 Torr, at which

point Ar is turned on and allowed to flow for several minutes at a rate of 1 SLM raising the internal pressure to about approximately 70 Torr. With Ar still flowing, the pressure in the tube is slowly returned to atmospheric pressure. H_2 gas is then turned on and allowed to flowed through the tube at a rate of 200sccm (5:1 Ar:H_2) and the temperature of the tube is raised to 650ºC. At 650ºC, acetylene, which is the carbon source, is turned on and flows at a rate of 10sccm and the temperature is allowed to rise to 750ºC at a ramp rate of 20ºC/min. The temperature is held at 750ºC for 10min after which the temperature is raised to 850ºC at the same ramp rate of 20ºC/min and held for an additional 10min. After the 850ºC step, the samples are allowed to cool back to room temperature in the furnace and the acetylene gas is turned off once temperature is below 650ºC with the other gasses still flowing for the duration of the cool down step. A picture of a pSi sample after carbon deposition is shown in image (3) of **Figure 4.2** where it is seen that the pSi region of the sample appears to be uniformly black. Surface and cross-section SEM images in **Figure 4.3**b reveal that after carbon deposition the open pores are preserved with a slight reduction in the size of the pore openings, consistent with previous reports of pSi with deposited few-layered graphitic coatings.[3, 135]

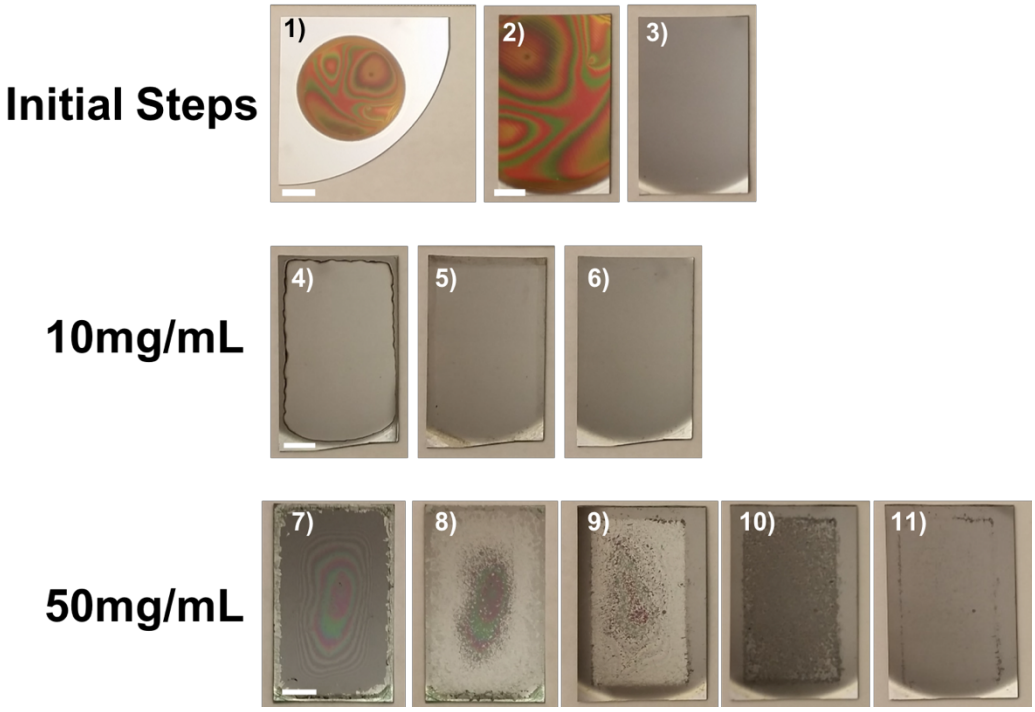

Figure 4. 2 Images of typical samples during processing where (1-3) correspond to pSi processing steps for all electrodes, (4-6) correspond to an electrode prepared with 10mg/mL solution precursor (scale bar = 5mm), and (7-11) correspond to electrodes prepared with 50mg/mL solution precursor (scale bar = 5mm). (**1**) The initial pSi sample with an etched region of 7.54cm^2. The silver colored regions are unetched Si (scale bar = 10mm). (**2**) The pSi sample cleaved to fit in the CVD tube furnace (scale bar = 5mm). (**3**) pSi after CVD carbonization. (**4**) 10mg/mL solution drop-cast and dried in air at RT with excess dried near the edges. (**5**) 10mg/mL sample after removal of excess precursor on edges with a damp cloth (dried precursor is water soluble). (**6**) 10mg/mL sample after annealing at 300°C. (**7**) 50mg/mL solution drop-cast and dried in air at RT. (**8**) The dried 50mg/mL film is thicker than the 10mg/mL electrode and flakes off with minimal disturbance. (**9**) 50mg/mL sample after excess precursor dried near the edges is carefully removed with a damp cloth. (**10**) 50mg/mL sample after annealing at 300ºC. A loosely attached black particulate film is present on the surface. (**11**) This excess would not contribute to performance and is removed simply by blowing off with N_2. Some of the NiO is not removed especially near the edges and may skew the effective mass loading.

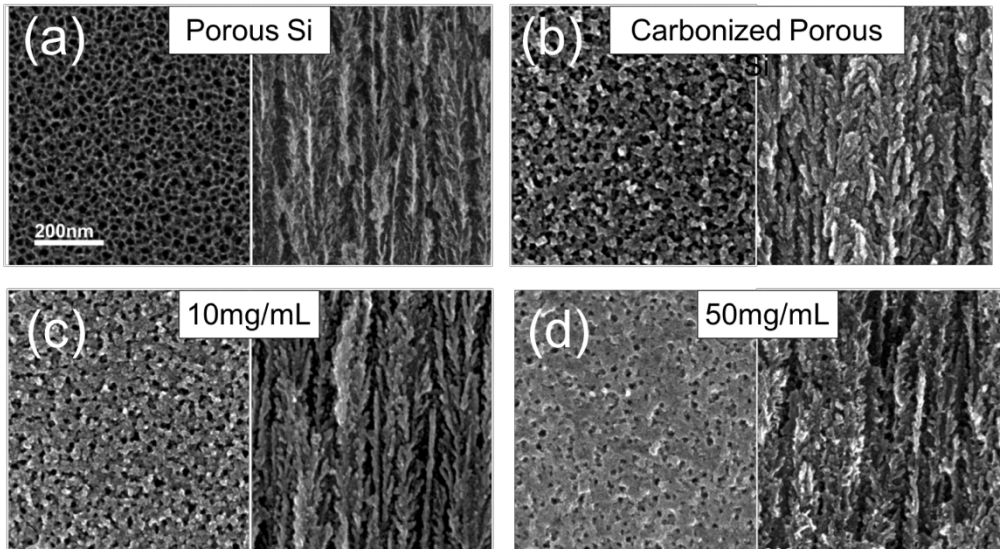

Figure 4. 3 SEM images showing electrodes in various stages of preparation. (**a**) Freshly etched pSi. (**b**) Post CVD carbonization. C-pSi electrodes with (**c**) 10mg/mL and (**d**) 50mg/mL NiO precursor deposited and annealed at 300ºC. In each pair of images, the left image shows the top view (surface) and the right image shows the cross-section. All images are at the same magnification.

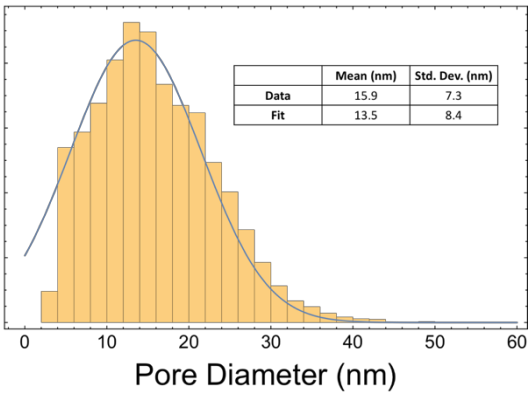

Figure 4. 4 Histogram and normal fit of the distribution of pore diameters determined from SEM image analysis of the pSi surface. The histogram was generated from multiple images at several different magnifications. See Appendix A for details on this process

NiO precursor preparation, deposition, and heat-treatment

For the studies here, two different concentrations of the NiO precursor were prepared to investigate the impact of concentration on the overall electrochemical performance of the electrodes. A precursor solution of 50mg/mL was prepared by dissolving 1g of nickel acetate tetrahydrate (NAT) into 20mL of 2-methoxyethanol (2MOE). A precursor of 10mg/mL was similarly prepared by dissolving 200mg of NAT into 20mL of 2MOE. To dissolve the NAT, both solutions were placed on a hot-plate at 60ºC and stirred with magnetic stir-bars at 300RPM for 1 hour. This process is identical to that described in the previous chapters for preparation of the NiO precursor.

A constant area-normalized volume of 30μL/cm^2 of the precursor was drop-cast onto the surfaces of each sample. The area used in the calculation was the total footprint area of each sample, including the small unetched Si regions and the C-pSi region. After drop-casting, the precursor was allowed to dry on the pSi surface in air at room temperature, which took 2 to 3hrs. Pictures of the samples at this stage are presented in images (4) and (7) in **Figure 4.2** for a 10mg/mL and a 50mg/mL sample, respectively. Except around the edge, the appearance of the sample with 10mg/mL deposited [image (4) of **Figure 4.2**] does not appear much different than the C-pSi sample before precursor deposition [image (3) of **Figure 4.2**]. The sample deposited with 50mg/mL of precursor [image (7) of **Figure 4.2**] obviously has a thin film on the surface. However, for the 50mg/mL sample, the film is thick enough that it easily cracks and flakes off when the sample is moved [image (8) of **Figure 4.2**].

Both the 10mg/mL and 50mg/mL samples show an excess of the precursor dried near the edges and with the appearance of a smoother more uniform deposition covering the rest of the sample. The edges were not included in the electrochemical testing and, therefore, to get an accurate measure of the areal density of the deposited precursor and final NiO mass, the excess precursor near the edges was removed. This was done by placing a damp cloth over the regions

to be removed; the deposited nickel acetate precursor readily dissolves and can be then be easily wiped away. Images (5) and (9) in **Figure 4.2** show 10mg/mL and 50mg/mL deposited samples, respectively, after the excess precursor is removed near the edges. The samples were then heated to 300ºC in air and held for 2hrs in a furnace to form NiO from the dried precursor. The annealing ramp rate was 5ºC/min. After the annealing step, the 50mg/mL samples had a significant amount of NiO particulates loosely formed on the surface [image (10) of **Figure 4.2**]. These particulates could easily be removed by blowing them off with N_2 gas [image (11) of **Figure 4.2**]. Annealing at 300°C has been shown to be an optimal temperature for NiO supercapacitor performance as the temperature is just high enough to remove residual precursor constituents while maintaining accessible active sites. Annealing at higher temperatures reduces the density of electrochemically active sites as the NiO becomes more crystalline and sintering is like begins to occur leading to a reduction in the surface area.[44]

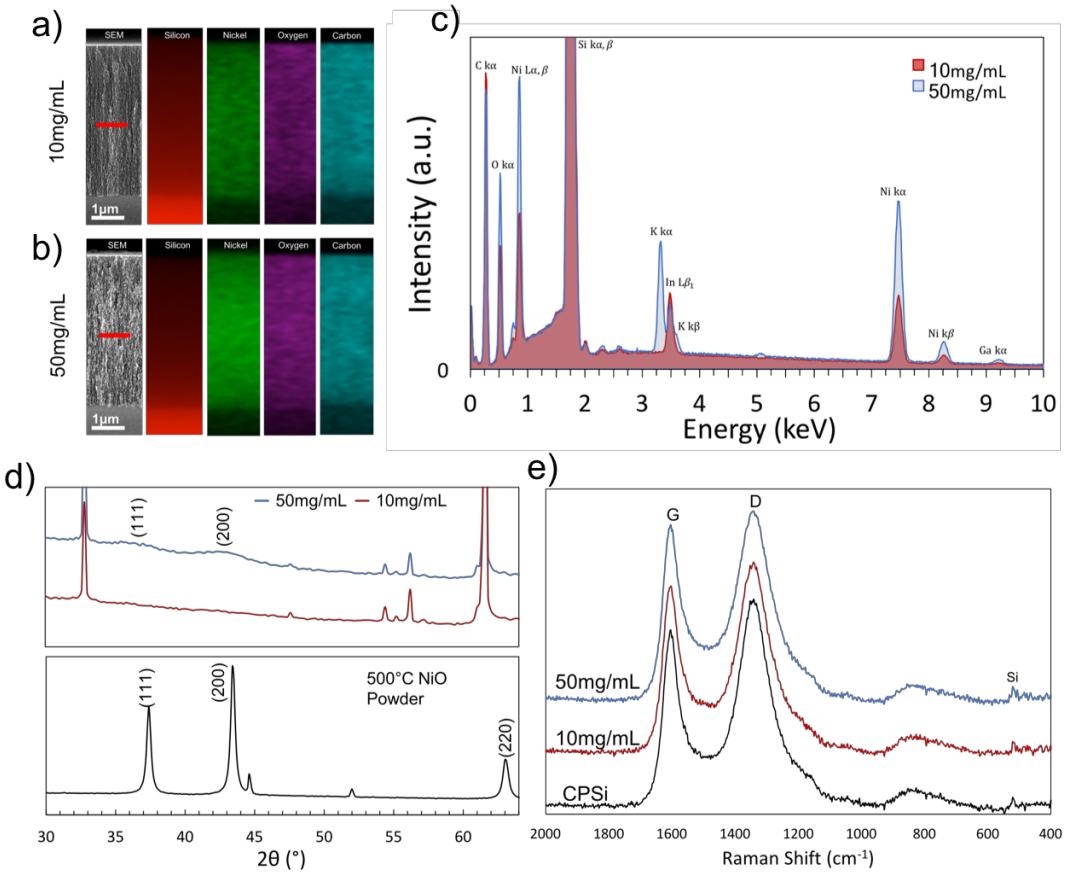

Figure 4. 5 Cross-sectional EDX mapping of the (**a**) 10mg/mL and (**b**) 50mg/mL NiO:C-pSi electrodes showing uniform distribution of Si, Ni, O, and C throughout the pSi layers. (**c**) EDX spectra collected from line-scans at the middle of the cross-sectional images in (a) and (b) (red lines) (**d - top**) XRD spectra of the 10mg/mL and 50mg/mL NiO:C-pSi electrodes with NiO peaks labeled on the 50mg/mL electrode spectra. All other peaks correspond to Si. (**d - bottom**) XRD spectrum of a NiO powder prepared by annealing a large amount of the dried NiO precursor. The non-labelled peaks correspond to Ni. (**e**) Raman spectra of 0mg/mL (C-pSi), 10mg/mL and 50mg/mL NiO:C-pSi electrodes.

SEM images of an annealed electrode prepared with the 10mg/mL precursor (**Figure 4.3**c) shows almost no difference in morphology compared to the C-pSi film **(Figure 4.3**b), while the electrode prepared with 50mg/mL of precursor (**Figure 4.3**d) exhibits a smoothing of the surface and reduction in the size of the pore openings, which can be attributed to the increased amount of NiO. Cross-sectional EDX mapping (**Figure 4.5**a and b) of 10mg/mL and 50mg/mL prepared electrodes show a near uniform distribution of Ni throughout the porous layer, indicating that the

precursor is evenly deposited into the pSi film at both concentrations. EDX spectra collected from line scans through the middle of the pSi layer, as indicated by the red lines in the cross-sectional SEM images of **Figure 4.5**a and b are provided in **Figure 4.5**c. From the EDX spectra, the intensity of the 10mg/mL Ni-kα peak is about 44% of that of the same peak in the 50mg/mL electrode. Though exact quantification of Ni present is difficult to determine by EDX, this value is close to the 46% value expected based on the mass loading of these particular samples (Table 4.1), and a similar case for the other Ni peaks. The presence of In and Ga peaks in the EDX spectra are due to small amounts of contamination from the eutectic deposited on the backside of the electrode for electrical contact during CV and GCD measurements. The K peak is attributed to residue from the KOH electrolyte that is used during electrochemical testing, although these particular regions had not yet been tested. To clarify this point, the samples are large enough that multiple regions can be tested for electrochemical performance without the need to cleave/scribe the samples into separate electrodes. After testing one of the regions on each electrode, EDX analysis was then conducted on a region of the electrode that had not yet been tested. However, when an electrode is tested it is afterwards rinsed with H_2O which may have caused some residual KOH to infiltrate pores in an untested region.

Table 4.1 displays the carbon and NiO mass-loading data for each sample prepared in this study. The final NiO mass-loading of 10mg/mL electrodes was measured consistently to be approximately 79μg/cm^2 across multiple devices with a standard deviation of only ~0.5μg/cm^2. For the 50mg/mL electrodes, the final NiO mass-loading ranged from approximately 114 to 183μg/cm^2. Such wide variation can be attributed to loosely bound NiO on the C-pSi surface. This causes the total NiO mass to vary between samples. Even so, the measured mass variation should not result in a difference in the overall electrochemical performance of the 50mg/mL

electrodes when normalized to spatial parameters as demonstrated through the consistency in the area-normalized performance of the electrodes in the electrochemical testing section.

Table 4. 1 Mass-Loading for each electrode sample prepared in this study.

Electrode Type	Mass Loading (µg/cm^2)	
	Carbon	***NiO***
Carbon-Only	290.6	
	255.2	
10mg/mL NiO precursor	226.1	79.7
	238.0	79.0
	290.9	78.5
50mg/mL NiO precursor	236.1	169.8
	260.3	183.0
	261.3	131.3
	229.5	114.4

XRD spectra of 10mg/mL and 50mg/mL NiO:C-pSi electrodes, as well as a NiO powder sample provided for comparison, are shown in **Figure 4.5**d. The powder sample was produced by annealing a large volume of the NiO precursor at 500ºC for 6hrs in air. The 2θ diffraction peaks in the powder sample at 37.3°, 43.3°, and 62.9º correspond to the (111), (200), and (220) crystal planes of the cubic rock salt phase of NiO (ICDD 47-1049). Although much lower in intensity and broader, the (111) and (200) diffraction peaks also appear in the XRD spectrum of the 50mg/mL electrode. No obvious NiO diffraction peaks are shown for the 10mg/mL electrode, which is likely due to the much lower amount of NiO present in the sample. All other obvious peaks present in the pSi samples are attributed to Si. Note that the broadening of the diffraction peaks in the XRD spectrum of the 50mg/mL sample is expected based on nanoscale confinement in the pSi pores that limits the growth of NiO nanoparticles to sizes less than the pore diameter,

and the small amount of precursor deposited as has been discussed in Chapter 2.[79] Typical Raman spectra of pSi electrodes after carbonization and after NiO formation are shown in **Figure 4.5**e. All Raman spectra show the usual carbon G and D peaks near 1600cm^{-1} and 1300cm^{-1}, respectively, corresponding to the sp^2 and sp^3 – hybridization, similar to other studies of CVD carbon-coated pSi.[3, 4, 135] The small Raman peak near 520cm^{-1} is due to Si. No obvious NiO Raman peaks were seen in any of the NiO deposited samples.

4.4 Electrochemical Characterization

Cyclic voltammetry

Electrochemical characterization of the NiO:C-pSi electrodes was carried out by three-electrode cyclic voltammetry (CV) with a Ag/AgCl reference electrode, a Pt-wire counter electrode, and 0.5M KOH(aq.) electrolyte. Initial stabilization cycles were performed at a rate of 20mV/s until the resulting CV profiles stabilized. Stabilization cycles allow for the activation of sites in the NiO as well as time for the maximum absorption of the electrolyte into the porous layer. **Figure 4.6** shows CV cycles of a 50mg/mL and 10mg/mL electrode collected at a scan-rate of 20mV/s after a sufficient number of cycles were performed to produce stable profiles. Redox peaks are clearly observable in both electrodes and are attributed to a change in Ni oxidation state ($Ni^{2+} \leftrightarrow Ni^{3+}$) accompanied by a reversible phase-transition according to the reaction:[18, 130, 136]

$$NiO + OH^- \leftrightarrow NiOOH + e^- \tag{4.3}$$

The electrode capacities are calculated to be 2.7μAh/cm^2 (10mg/mL) and 5.0μAh/cm^2 (50mg/mL), based on the CV curves shown in **Figure 4.6**. A higher capacity is observed in the electrode with the greater amount of NiO, as expected.

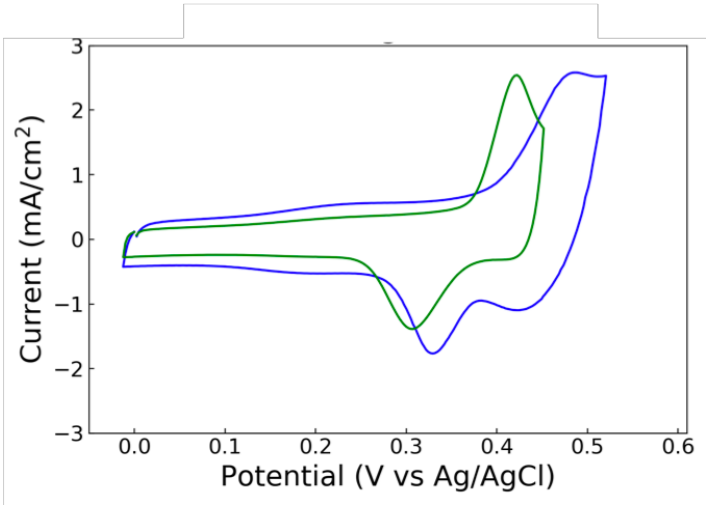

Figure 4. 6 CV cycles at 20mV/s of NiO:C-pSi electrodes prepared with 10mg/mL (green) and 50mg/mL (blue) NiO precursor. Both electrodes show redox peaks attributed to a change in Ni oxidation state.

The CV rate performance of the electrodes was investigated by increasing the scan-rate from 10 to 50mV/s. **Figure 4.7** shows the CV profiles for a 50mg/mL and 10mg/mL NiO:C-pSi electrode. For the 50mg/mL electrode, the capacity varies from 4.4 to 6.6μAh/cm^2 while the 10mg/mL electrode exhibits capacities that range from approximately 2.0 to 2.9μAh/cm^2. For both electrodes, the capacity generally increases as the scan rate increases. This is in contrast to most reported devices, which exhibit the opposite behavior. A possible reason for this effect could be that charge-leakage is occurring and this effect would be more pronounced at slower rates. Even so, this effect was not directly observed in the GCD experiments to be discussed later. These prototype NiO:C-pSi electrodes are a first investigation into this composite materials system for electrochemical energy-storage and it is likely the performance can be further improved through optimization of pore size, pore depth, and optimal fill-fraction of NiO.

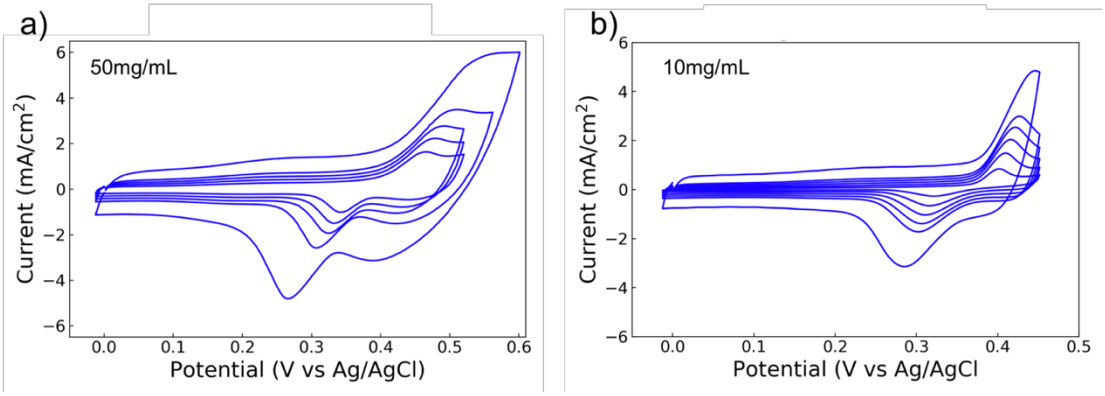

Figure 4. 7 CV curves obtained at scan rates of 10, 15, 20, 25, and 50mV/s on a (**a**) 50mg/mL and (**b**) 10mg/mL NiO:C-pSi electrode.

It is worth mentioning that cycling a 10mg/mL NiO:C-pSi electrode over a wider voltage window (**Figure 4.8**) showed an increase in the capacity up to 4X compared to the results shown in **Figure 4.7**b. However, with the increase in capacity, a significant and permanent change in the NiO occurs as the profile shape and redox peak potential changes. The CV curves become larger, more symmetric, and slightly shifted. These changes are attributed to continued activation of Ni sites deeper in the NiO, which increases the total amount of charging that occurs and is likely accompanied with a conversion of NiO to $Ni(OH)_2$. While such conversion is not wholly undesirable, as $Ni(OH)_2$ is the active material in Ni-based batteries, the complete degradation of the samples was observed to occur after only a few cycles once reaching the maximum capacity, and the electrode material appeared to degrade, presumably due to mechanical strain induced by phase conversion during cycling.

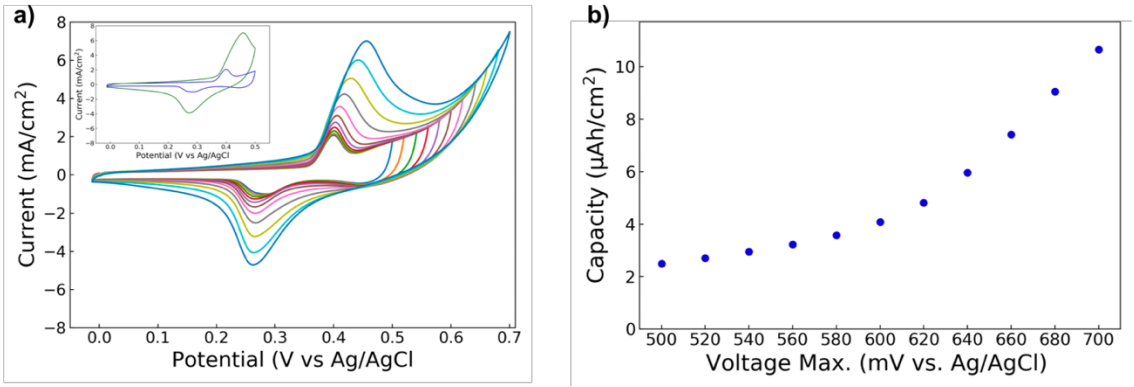

Figure 4. 8 (**a**) CV curves of a 10mg/mL electrode cycled at increasing maximum potentials from 500mV to 700mV (vs. Ag/AgCl). The inset shows two cycles to 500mV corresponding to before (blue) increasing the potential to 700mV and after (green) cycling to 700mV, which clearly shows that a permanent change in the cycling behavior has occurred, attributed to a phase transformation of the NiO likely to $Ni(OH)_2$. (**b**) Plot of the capacity of the electrode as a function of increasing potentials from (a).

Examination of the CV curves in **Figure 4.6** reveal that at potentials below the onset of the anodic peak (approximately 350mV vs. Ag/AgCl), the NiO:C-pSi electrodes exhibit almost entirely capacitive-like behavior. This capacitive behavior appears to contribute a significant component to the overall capacity. Previous studies have demonstrated that C-pSi can be exploited for EDLCs while NiO electrodes have been explored for pseudocapacitance, hence, it is not surprising that NiO:C-pSi electrodes should possess this capacitive component as well.[3, 4, 18] To investigate the electrode performance in the capacitive regime, the electrodes were cycled over a reduced window up to 340mV (vs. Ag/AgCl). CV curves collected from a 10mg/mL and 50mg/mL NiO:C-pSi electrode as well as a pure C-pSi electrode are shown in **Figure 4.9**a.

The CV curves in **Figure 4.9**a are mostly rectangular, as expected for capacitors, making the designation of a capacitance reasonable. In the NiO:C-pSi electrodes, however, there are broad reversible current peaks centered at ~200mV (vs. Ag/AgCl). This is attributed to pseudocapacitive charge-storage (i.e. surface and near-surface Faradaic reactions) and is not observed in the pure C-pSi EDLC electrode. Pseudocapacitive reactions of NiO are presumed to take place at active

surface sites at lower, and more widely distributed potentials than the reactions occurring deeper within the NiO that lead to more battery-like redox behavior, as shown by the larger prominent peaks in **Figures 4.6** and **4.7**. As a result, broad reaction peaks are observed in CV measurements over the reduced voltage window, giving rise to I/V curves resembling that of a capacitor. However, due to the nature of pseudocapacitive reactions, there is a slight dependence of capacitance on the voltage, and, therefore, the calculated capacitances will only constitute an average based on the total discharge capacity in this regime. The average electrode capacitances were calculated by applying a modified version of **Equation 4.2**: $C_{avg} = \Delta Q/\Delta V$. ΔQ is calculated from **Equation 4.1** and ΔV represents the discharging potential window of the CV curves (i.e. negative current portion).

The average capacitance for each electrode in **Figure 4.9**a was found to increase with the concentration of the initial NiO precursor (i.e. amount of NiO present). These were calculated to be 4, 11, and 18mF/cm^2 for the C-pSi, 10mg/mL NiO:C-pSi, and 50mg/mL NiO:C-pSi electrodes, respectively. The values are consistent across multiple devices of each type as shown in the plot of capacitance vs cycle number in **Figure 4.9**b for the initial 100 stabilization cycles. The consistency between devices demonstrates the high-degree of repeatability and robustness of the device fabrication process developed in this study.

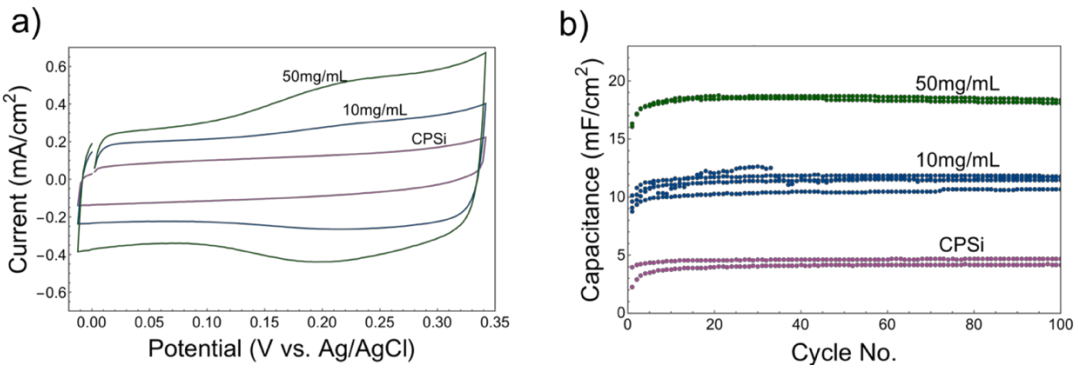

Figure 4. 9 (**a**) CV measurements of a 10mg/mL and 50mg/mL NiO:C-pSi electrode and a pure C-pSi electrode cycled at a reduced potential window of 340mV (vs. Ag/AgCl). The pure C-pSi electrode stores charge by the EDL mechanism while the NiO electrodes store charge by both pseudocapcitive and EDL mechanisms as indicated by the broad reversible reaction peaks. (**b**) Calculated average capacitance vs. cycle number for multiple samples of each device type tested in this study. The plot shows excellent consistency in device performance for devices of each type. The cycles correspond to the initial 100 stabilization CV cycles carried out at 20mV/s.

The rate performance of 50mg/mL and 10mg/mL NiO:C-pSi electrodes operating in the capacitive-regime was evaluated by CV over multiple scan-rates which are shown in **Figure 4.10**. The 50mg/mL electrode was cycled at 10, 15, 20, 25, 50, 100, 250mV/s. In the plot over the range of 25 to 250mV/s, there is only slight degradation in the performance as rate increases up to 100mV/s. This is indicated by the near identical shape of the curves. At 250mV/s, the electrode maintains appreciable capacitive charge-storage, though it has reduced slightly, indicated by the slight closing of the CV profile. Good stability of the NiO:C-pSi electrode at high-rates is evidence of fast surface and near-surface reactions rather than slower bulk reactions. Hence, it is believed that within the reduced voltage window, there is minimal diffusion of active ions into the interior of the NiO and no subsequent bulk phase transition occurs during charging/discharging.

The plot for the 50mg/mL electrode cycled at 10 to 25mV/s also shows good stability at low rates, however, in this plot the performance actually improves with increasing rate. This improvement with rate is possibly evidence of charge-leakage effects which are more pronounced

at lower rates. Near identical behavior was observed for the 10mg/mL electrode, except the electrode exhibited a lower overall capacitance. Additionally, the 10mg/mL electrode was only cycled to 200mV/s instead of 250mV/s. There was no intentional reason for this except that these devices were tested at different times.

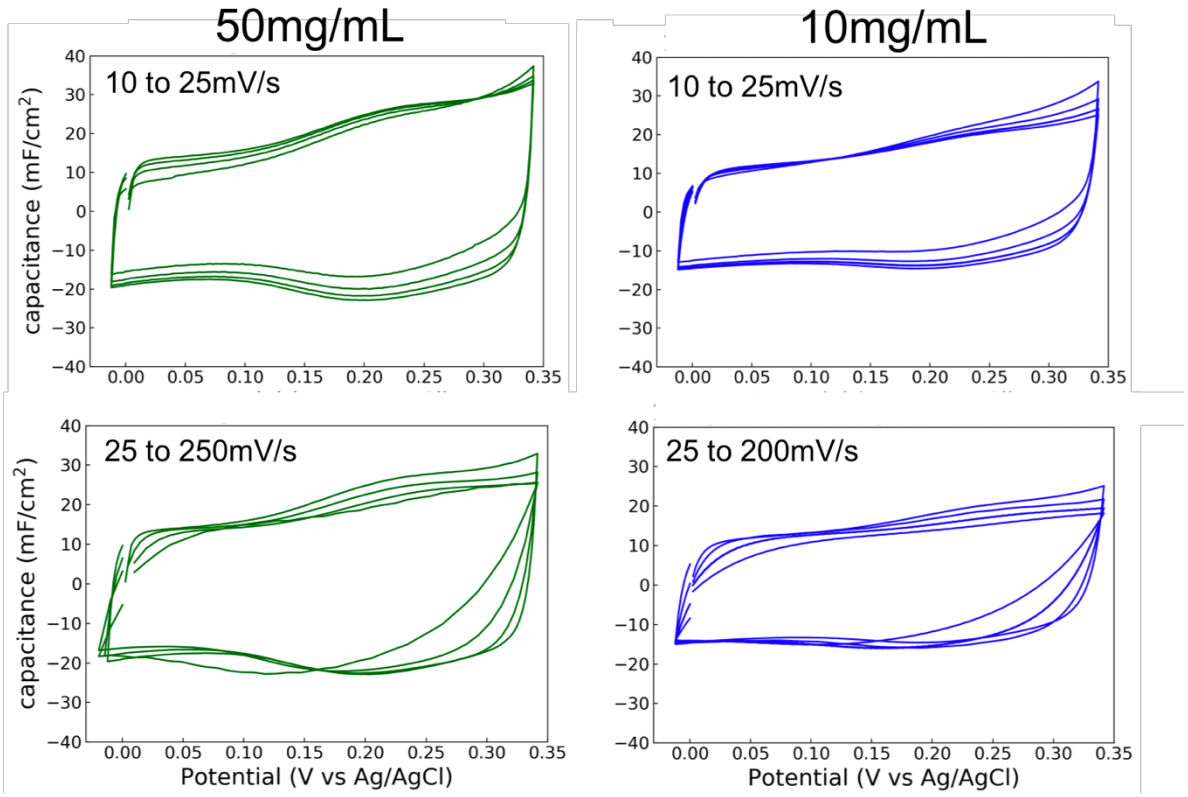

Figure 4. 10 CV curves of increasing rate for NiO:C-pSi electrodes prepared with (**left**) 50mg/mL and (**right**) 10mg/mL precursor concentrations. Scan-rate ranges are indicated in the plots.

Galvanostatic charge-discharge

Figure 4.11 provides discharge GCD curves for 50mg/mL and 10mg/mL NiO:C-pSi electrodes when charged to different maximum potentials at a rate of 400μA/cm^2. The 50mg/mL electrode was charged to potentials of 360, 380, 400, 420, 440, and 450mV (vs. Ag/AgCl). The 10mg/mL

electrode was charged to potentials of 340, 350, 360, 370, 380, 390, and 400mV (vs. Ag/AgCl). For both electrodes, at the highest charging potentials, there is a transition from linear (capacitive-like) discharging to more battery-like discharging signified by the presence of an increasingly prominent potential shelf which is indicative of Faradaic discharging reactions. The capacity of the 50mg/mL electrode increased with maximum charging potential from 2 to 4μAh/cm^2, and similarly, the 10mg/mL electrode increased from 1.4 to 2.4μAh/cm^2.

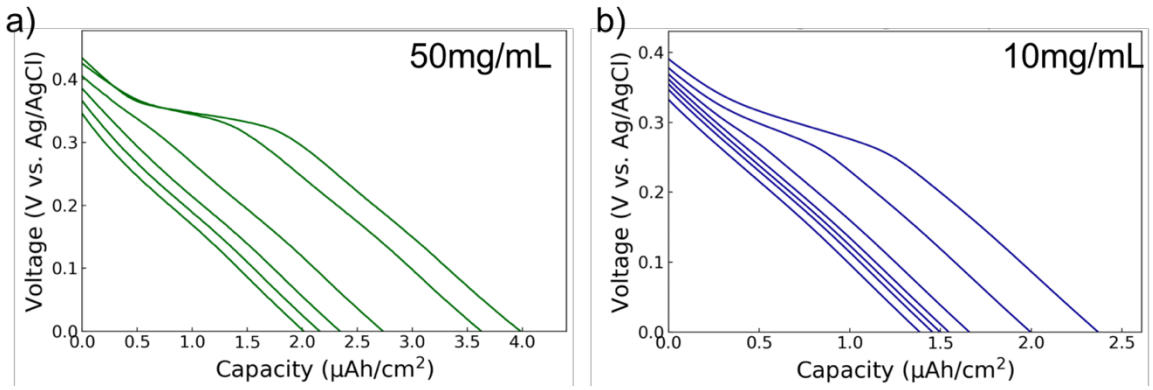

Figure 4. 11 Discharge curves collected by GCD at 400μA/cm^2 of (**a**) 50mg/mL and (**b**) 10mg/mL electrodes after being charged to increasingly higher potentials. The 50mg/mL electrode was charged to potentials of 360 to 450mV (vs. Ag/AgCl) and the 10mg/mL electrode was charged to potentials ranging from 340 to 400mV (vs. Ag/AgCl).

The GCD rate performance was subsequently evaluated by charging and discharging each electrode at currents ranging from 400μA/cm^2 to 2mA/cm^2. These discharge curves are provided in **Figure 4.12**. Maximum charging potentials of 400mV (vs. Ag/AgCl) for the 10mg/mL electrode and 450mV (vs. Ag/AgCl) for the 50mg/mL electrode were selected based on the previous experiments shown in **Figure 4.11**. Attempting to charge to much higher voltages, particularly at lower currents, would result in overcharging of the device and more rapid degradation. Both electrodes exhibit good stability up to 1mA/cm^2 with capacities that only decrease slightly with increasing current from ~2.4 to 2.3μAh/cm^2 for the 10mg/mL electrode and

4.0 to 3.7μAh/cm^2 for the 50mg/mL electrode. These GCD capacities are slightly less, but still consistent, with the values determined from CV measurements. At 2mA/cm^2, the performance degrades to 1.9μAh/cm^2 and 3.0μAh/cm^2 for the 10mg/mL and 50mg/mL electrodes, respectively. Degradation in the performance at higher rates is an indication that the diffusion and charge-transfer rate are not able to maintain pace with the current which will introduce increased charge-loss due to the resistance. This will result in a higher charging potential shelf and a lower discharging potential shelf, as observed here.

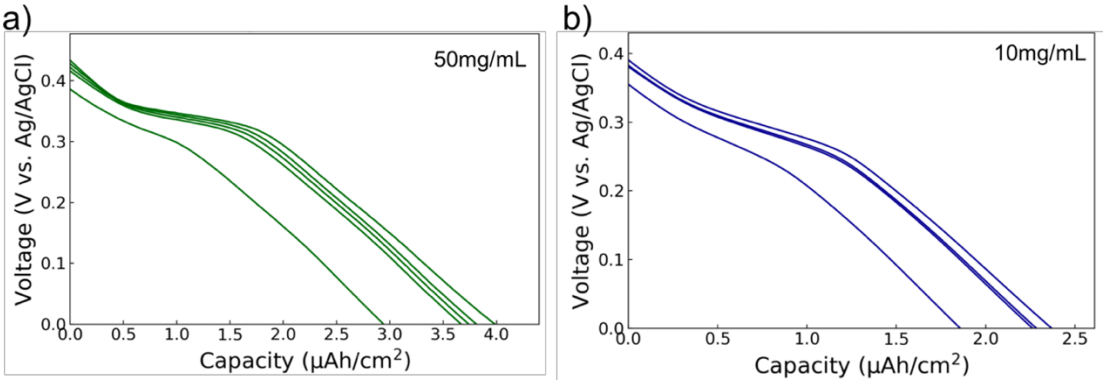

Figure 4. 12 GCD discharge curves for a (**a**) 50mg/mL and a (**b**) 10mg/mL electrode collected at currents ranging from 400μA/cm^2 to 2mA/cm^2. The 10mg/mL electrode was charged to a potential of 400mV (vs. Ag/AgCl) while the 50mg/mL electrode was charged to a potential of 450mV (vs. Ag/AgCl). These discharging curves show good stability for both electrode types over the range of currents tested with degradation setting in only at the highest current (2mA/cm^2).

Figure 4.13a shows charging and discharging cycles of each device type cycled only in the linear, capacitive, regime at 400μA/cm^2 to a maximum potential of 340mV (vs. Ag/AgCl). The charging and discharging times for each electrode in the plot increase, as expected from the CV analysis, with increasing concentration of the deposited NiO precursor. This is attributed to two effects: (1) there is likely an increase in the surface area with additional NiO nanoparticles

which is directly proportional to the EDL charging, and (2) with more accessible NiO there is an increase in the number of active surface sites for the pseudocapacitive reaction to take place.

A plot of the capacitance vs. current for each electrode cycled in the capacitive regime at different currents is provided in **Figure 4.13**b over the range of 100µA/cm^2 to 4mA/cm^2. For each electrode, the greatest capacitance was observed at 100µA/cm^2, which is approximately 10, 18, and 25mF/cm^2 for the C-pSi, 10 mg/mL NiO:C-pSi, and 50 mg/mL NiO:C-pSi electrodes, respectively. These values are comparable to, or even exceed that of many other reported on-chip micro-supercapacitor electrodes.[5, 137-140] Furthermore, the GCD rate performance shows that these electrodes exhibit excellent stability over the range of currents tested. In particular, there is only 7% degradation in the 50mg/mL NiO:C-pSi electrode with increasing rate, which is quite small compared to other reported devices that show high capacitance at low currents but degrade drastically as current increases only slightly.[141, 142]

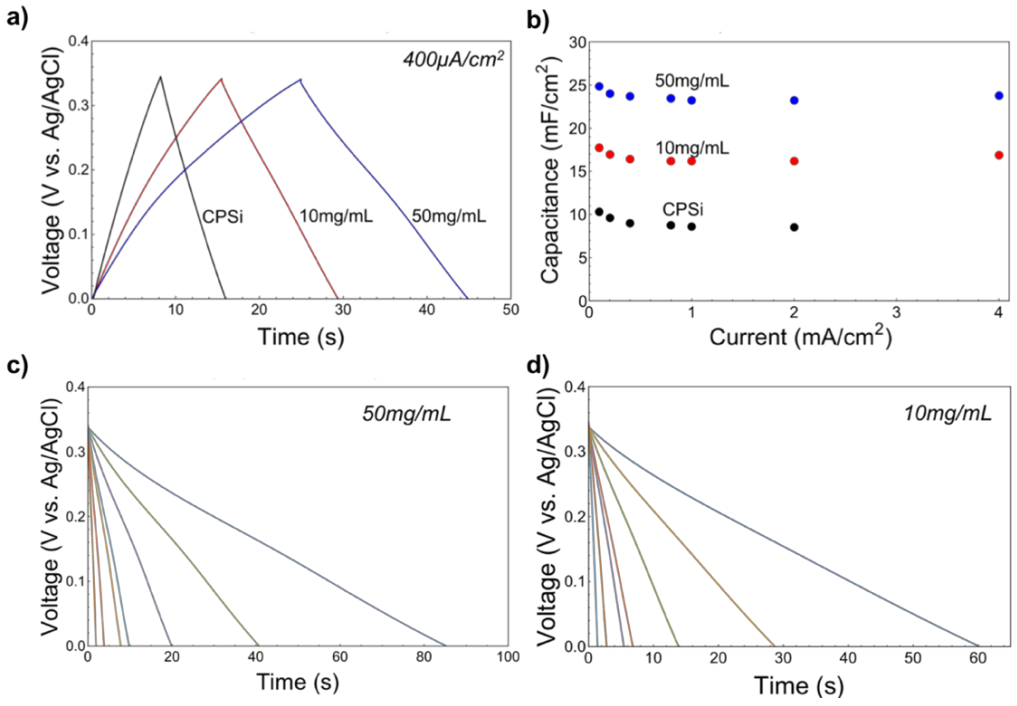

Figure 4. 13 (**a**) Three-electrode GCD curves collected at 400µA/cm^2 on each of the electrode types tested in this study. (**b**) A plot of the GCD discharge capacitance with

increasing current for each electrode type tested. The GCD discharge curves for the NiO electrodes used to calculate the capacitance in (b) are shown in (**c**) 50mg/mL and (**d**) 10mg/mL.

4.5 Conclusion

In summary, electrodes composed of C-pSi with NiO deposited on the surface, are presented as a versatile platform for development of electrochemical energy-storage devices that are compatible with on-chip integration. The use of high surface area C-pSi facilitates the growth of NiO within the nanoscale pores to form electrochemically active nanoparticles. The properties of the nanocomposites were characterized by SEM, EDX, XRD, and Raman spectroscopy. Three-electrode experiments are performed in an aqueous electrolyte on devices prepared with 10mg/mL and 50mg/mL NiO precursor concentrations. The devices were tested by CV and GCD and showed a significant capacitive-like charge-storage component superimposed on conventional battery-like Faradaic redox reaction peaks. A maximum capacity of 6.6μAh/cm^2 for the 50mg/mL electrodes and 2.9μAh/cm^2 for the 10mg/mL were observed by CV measurements. It was also shown using a 10mg/mL electrode that the capacity could be increased by nearly 4x by increasing the voltage window but this also results in degradation of the electrode within a few cycles after reaching this maximum. The maximum capacity of the 50mg/mL electrode when testing by GCD was 4.0μAh/cm^2 and the 10mg/mL electrode showed a maximum capacity of 2.4μAh/cm^2. Evaluation of just the capacitive contribution by GCD of the electrodes gives an average capacitance of 25mF/cm^2 for the 50mg/mL electrode and 18mF/cm^2 for the 10mg/mL electrode, which are both improved over the pure C-pSi electrode capacitance of 10mF/cm^2. These values are comparable to other reported supercapacitors for on-chip applications.

CHAPTER 5

SUMMARY

Presented in this dissertation were the investigations of multiple and diverse applications of a nanocomposite materials system composed of porous silicon (pSi) and transition metal oxides (TMOs). The primary application areas discussed were nanoparticle synthesis, variable conductivity devices (memristors), and electrochemical energy-storage electrodes. The pSi is envisioned to serve two main functions: 1) to confine the growth of the TMO to the nanoscale regime and 2) to play an active role in device performance. The pSi films utilized in this dissertation were formed by electrochemical etching of crystalline Si (cSi) wafers, resulting in the formation of vertically aligned nanoscale pores embedded within cSi substrates. The TMOs are formed from the thermal decomposition and subsequent annealing of precursors derived from solutions deposited into the pSi matrices. Throughout this dissertation, nickel oxide (NiO) was the primary TMO implemented, while titanium dioxide (TiO_2) was demonstrated for potential application to memristors.

In Chapter 2 it was demonstrated that pSi is effective at limiting the growth of NiO nanoparticles when derived by thermal decomposition and subsequent annealing of a Ni-acetate precursor. This was demonstrated over a range of annealing temperatures and pSi pore sizes, and compared to NiO grown by similar methods on planar crystalline Si (cSi) substrates. When NiO was grown in pSi films etched at the same rate producing films with average pore diameter of 64nm ± 25nm, and annealed over a range of temperatures from 300°C to 1100°C the resulting average NiO crystallite size increased from ~10nm to >100nm, as determined by employing Scherrer's equation (**Equation 2.1**) on the NiO (200) XRD peak. SEM imaging confirmed the

trend and also revealed deformation of the pSi pores due to oxidation of the Si. The increase in average NiO crystallite size beyond that of the average pSi pore size is attributed to this deformation which allowed extended growth. Over the same annealing temperature range, the NiO crystallites produced on planar cSi samples showed an increase in size from ~15nm to >200nm, as determined by Scherrer's equation (**Equation 2.1**). This trend is confirmed by SEM image analysis which further revealed that while NiO nanoparticles annealed at low temperatures on cSi grow more or less unbounded, at 800ºC and above, the particles are large enough to impinge on neighboring particles and begin to sinter, restricting further growth.

Growing NiO by annealing at the same temperature (700ºC) in pSi films with different average pore sizes (~20nm to 57nm) produced NiO crystallites that increased with pore size from ~10nm to 26nm average crystallite diameter. TEM imaging of particles extracted from the 17.5mA/cm^2 pSi film showed aggregated particles of ~20 to 30nm in diameter, close to the value estimated by XRD analysis. UV-vis absorption measurements on the extracted particles suspended in DI-H_2O allowed estimation of the optical bandgap which decreased with increase in size of the particles from 3.90eV to 3.72eV, consistent with values typically reported for NiO nanomaterials. The results of these studies demonstrate that utilizing the interior of pSi is an effective template permitting a measure of control in size and properties through simple selection of the pSi etching parameters and annealing temperature. Additionally, the methods developed in these studies for producing nanocomposite metal oxide:pSi materials were utilized in the subsequent chapters.

In chapter 3, both NiO:pSi and TiO_2:pSi nanocomposite devices were investigated for possible application as memristors. Electrical characterization carried out by sinusoidal voltage sweep of a NiO:pSi device produced the characteristic pinched hysteresis I/V curve recognized as the fingerprint of memristive devices. Current saturation (constant voltage) measurements produced a continuously increasing current up to some maximum value that is dependent on the

applied bias. Analysis of the current saturation data suggested near constant initial and final resistance values of 32kΩ and 6kΩ, respectively, in the voltage regime from 4V to 6V. A device-level model was also described and fit to the current saturation data of the NiO:pSi device which considers the accumulation of mobile ionic defects towards the numerous NiO/Si interfaces to cause a change in an effective energy barrier. This effect, in turn, causes a variation in charge-flow across the interface resulting in an increase in the overall current. A two-term fit of the model was shown to be sufficient to fit the data, and estimation of mobility of ionic defects in the NiO were estimated to be ~0.5 and 3 x $10^{-10}$$cm^2$/Vs.

Investigation of the TiO_2:pSi devices by cyclic voltammetry also produced hysteresis I/V curves, but the presence of a significant charge-storage component prevented the full collapse of the curves at the origin. The charge-storage effect is attributed to electrochemical capacitive and reversible redox processes at the numerous TiO_2 – pore wall interfaces. The variation in conductivity was observed to be dependent on the sweep rate, with open, outer loops at higher rates of 1V/s and 500mV/s. The outer loops collapse to single values at 100mV/s which could be explained by considering a similar interfacial-defect model as in the NiO:pSi devices. In this case, a maximal change in an effective potential barrier would occur at lower voltages as the sweep rate decreases resulting in observation of minimal to no change in the conductivity.

Current saturation measurements collected on TiO_2:pSi devices showed memristive behavior as well as charge-storage behavior. The total charge stored at each voltage was determined by integration of the 0V discharge curves after each voltage step. Above 8V, the total charge converges to approximately 6μC. It was also seen that only at voltages of 14V and above was the presence of a memristive effect observed. However, even in this range, initial charging of the device up to ~3.1μC was necessary prior to the observation of memristance. The presence of the charge-storage component made it difficult to directly fit the model previously described to the

TiO_2:pSi device data. However, similarities in device behavior of both TiO_2:pSi and NiO:pSi devices support the assertion that the underlying mechanism of ionic migration is directly applicable to the TiO_2:pSi system, as well. For instance, both TiO_2 and NiO:pSi devices were found to be symmetric in their behavior (no preferred polarization of the electrodes), and both exhibit non-crossing I/V hysteresis behavior. Furthermore, implementation of these model nanocomposite materials demonstrate a potential path for developing memristive devices at scales much larger (up to several 10s of μm's) than those at which the phenomenon is typically observed (10s of nm's or less). It is envisioned that each metal-oxide filled pore serves as a single element and their collective operation results in a macroscale effect. Such devices would not be viable for traditional memory applications, but it could be expected that novel and unique applications would benefit from large-scale discrete devices. Furthermore, these devices are produced directly within a crystalline Si wafer making a path for simple integration feasible.

In Chapter 4, electrodes composed of carbonized-pSi (C-pSi) with NiO deposited on the surface, were presented as a versatile platform for development of electrochemical energy-storage compatible for on-chip applications. Three-electrode experiments were performed in an aqueous electrolyte on devices prepared with different concentrations of the initially deposited NiO precursor (10mg/mL and 50mg/mL). The devices were tested by cyclic voltammetry (CV) and Galvanostatic charge-discharge (GCD) and showed a significant capacitive-like charge-storage component superimposed on conventional battery-like Faradaic redox reaction peaks. A maximum capacity of 6.6μAh/cm^2 for the 50mg/mL electrodes and 2.9μAh/cm^2 for the 10mg/mL were observed by CV measurements. It was also shown using a 10mg/mL electrode that the capacity could be increased nearly 4x by increasing the voltage window, but this also results in degradation of the electrode within a few cycles. The maximum capacity of the 50mg/mL electrode when testing by GCD was 4.0μAh/cm^2 and the 10mg/mL electrode showed a maximum

capacity of 2.4μAh/cm^2. Evaluation of just the capacitive contribution by GCD of the electrodes gives an average capacitance of near 25mF/cm^2 for the 50mg/mL electrode and 18mF/cm^2 for the 10mg/mL electrode, which are both improved over the pure C-pSi electrode capacitance of 10mF/cm^2. These capacitance values are comparable to other reported supercapacitors developed for on-chip applications.

In summary, metal oxide:pSi were demonstrated throughout this dissertation for multiple and diverse applications. The pSi platform which is developed directly on the surface of a crystalline Si wafer offers a unique and novel approach to developing nanomaterials and nanocomposites and is well-suited for direct integration on-chip. Furthermore, the ability to tune the pore size and pore depth, and thus the effective material parameters, through simple variation of the etch currents would allow for a wide range of tunable device behaviors.

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APPENDIX

A: DETAILS OF PORE SIZE MEASUREMENTS FOR CHAPTER 2

Assigning an accurate average pore size in pSi is challenging due to the wide distribution of apparent sizes, irregularly shaped pore openings, the intricate morphology within the pore interior, and initial widening of pores near the surface. Even so, certain definite features are observed across multiple samples, and here a description of how pore size estimation was carried out is provided for both studies discussed in chapter 2.

A.1 Anneal study

All pSi films prepared in the anneal study section were etched at a current density of 25mA/cm^2. One approach for determining pore size from surface images is to measure the area of the pore openings and calculate the diameter of a circle with equivalent area. This was the method employed in this study. For each pSi sample, multiple images at different magnifications were analyzed using ImageJ's – analyze particles function (Rasband 1997-2014). Prior to analysis, the images had to be processed in order for the software to distinguish pore openings from the interlocking Si network surrounding the pores. Each image that was analyzed for determining pore size was analyzed multiple times with slightly different image processing parameters applied prior to the analysis in order to ensure that the process settings did not significantly influence the resulting pore sizes values. These included differences in the adjustment of the brightness/contrast levels, whether an image smoothing function was employed, and implementing different filter types such as bandpass or Gaussian filters. Additionally, the image must be binary (black and white) prior to analysis which is accomplished using the threshold feature of ImageJ which was also varied between successive analyses. As an example, **Figure A.1** shows three different SEM images of a

pSi surface at different magnification levels and the corresponding histograms generated by performing the *Analyze Particle* function in ImageJ with different values for parameters used to process the image prior to analysis. The distributions become smoother and more Gaussian as the total number of pores in the field of view increases.

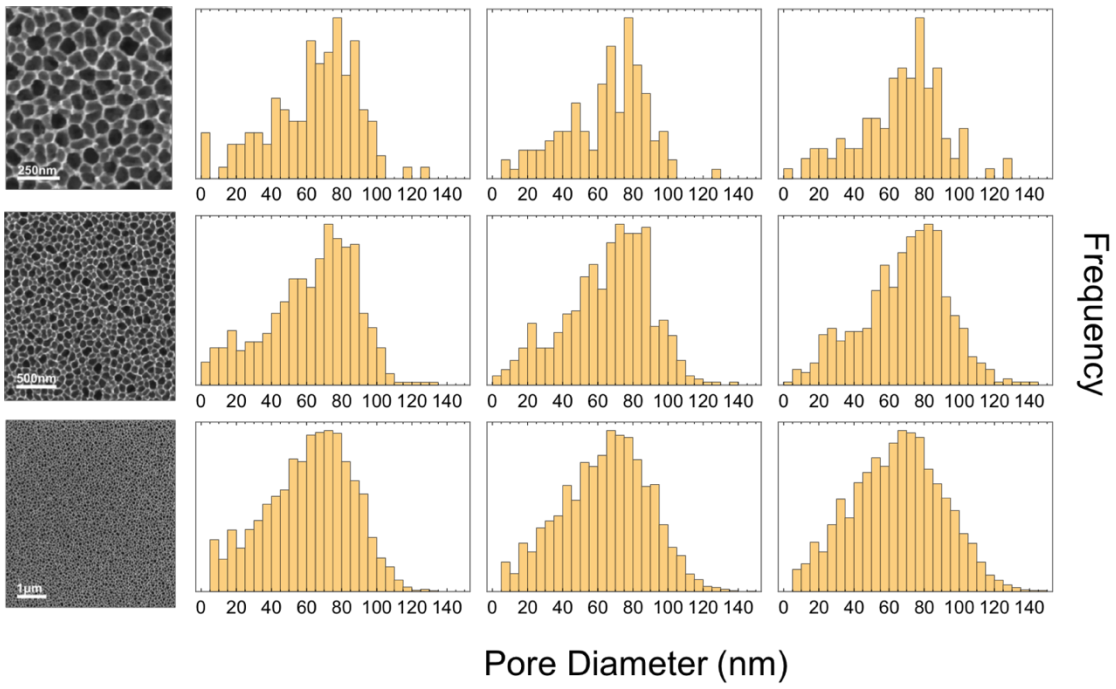

Figure A. 1 On the left are SEM images from the same pSi sample at different magnifications. Each row of histograms corresponds to the SEM image in that row. Each histogram in the same row was generated by applying different image processing parameters to the corresponding SEM image to prepare the images for analysis.

Further analysis on the histograms in the array in **Figure A.1** shows that the pore diameters approximate a normal distribution, but the degree to which this is apparent varies according to the number of pores within the field of view. The histogram in **Figure A.2** was generated by the concatenation the data in **Figure A.1**. Each row was concatenated first and then padded with multiple copies until the length of each data set was similar, so as to give the same weight to each data set. This histogram is fit with a normal distribution which seems to fit the data reasonably

well with a fitted mean of 68.9nm and standard deviation of 23.6nm. The data mean was 64.7nm with standard deviation of 24.8nm.

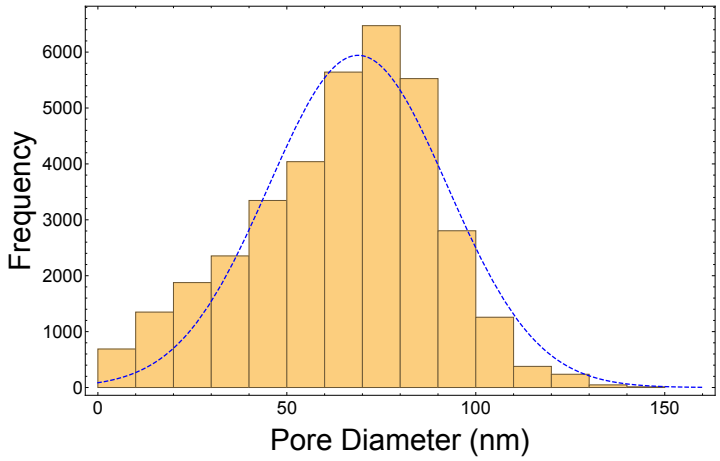

Figure A. 2 Histogram generated from concatenation of the data in Figure A.1. Prior to concatenation each data set in Figure A.1 was padded with multiple copies of itself to make the length of each individual data set a similar size so as not to give preferential weight to any of the individual data sets. The histogram is overlaid with a normal fit that agrees well with the data. The fitted mean is 68.9nm with a standard deviation of 23.6nm, and the data mean is 64.7nm with standard deviation of 24.8nm.

In **Figure A.3** the first data point for Sample No. 1 represents the average of the data means of each distribution in the histogram array in **Figure A.1**, and the error bar represents the standard deviation of these data means. The other two data points represent analysis on the other pSi films used in this study and demonstrate that pore size is very consistent across multiple samples with average pore diameter ranging between 63.5 to 64.7nm. The mean pore size between all the analyzed samples is indicated by the red dashed line which is approximately 64.1nm. The average standard deviation in the pore size of each sample was approximately 25 ± 5nm.

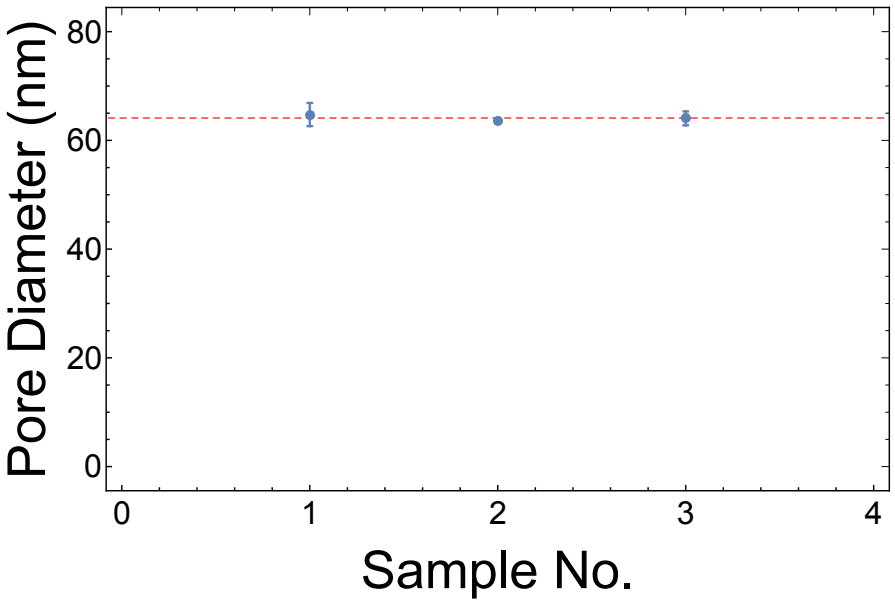

Figure A. 3 Plot of the average pore size of each sample determined by the method described for Figure A.1. Each data point corresponds to a different pSi sample. The error bars correspond to the standard deviation in the means between different analysis routines and magnifications for each sample. See description of Figure A.1 for details. This figure shows that there is good consistency in the average pore size between samples and that for each sample the processing parameters applied to the image prior to size analysis caused very little deviation in the final results.

In addition to measuring pore size from surface images, determination of pore widths was also attempted by measuring cross-section widths from side-profile SEM images of the pores. This was approached in two ways with comparable results. One method approximates the positions of the pore walls and then the distance is measured between adjacent pore walls as depicted in **Figure A.4**a for one sample. The other method employed involves determining the cross-sectional area outlined by the pore walls of each pore in an image and then dividing by the length of the pore, which should provide an average pore width. This method was performed in ImageJ using its *Analyze Particles* function which gives the area of the outlined cross-section of each pore. An example of an image analyzed by this method is shown in **Figure A.4**b which is just a conversion of the image in (a) to black (pores) and white (Si pore walls). ImageJ requires this conversion for

Analyze Particles. The first method described is simple while the second method is more involved but can take into account the pore morphology. Here, however, the morphology was simple as the pore walls were mostly straight. The results of applying these two methods to three different samples are shown in the plot in **Figure A.4**c. The first method (shown in blue) resulted in average widths between 129nm to 141nm while the second method resulted in widths from about 117nm to 129nm. Comparison to the pore diameters determined from surface analysis showed that cross-sectional analysis gives a much higher (< 2x) increase in the pore width. There are a few possible reasons for this difference: 1) the total number of pores that can be analyzed is much lower ~10 to 30 pores, whereas low magnification images of the surface could contain >4000 pores within the field of view, 2) the pores are not circular but irregularly shaped with many that can be significantly wider in one lateral direction than the other, and pores that are cleaved along this direction would have a much larger cross-sectional width than the estimated circular diameter from the surface, and 3) the effects of pore widening were not completely eliminated during electropolishing.

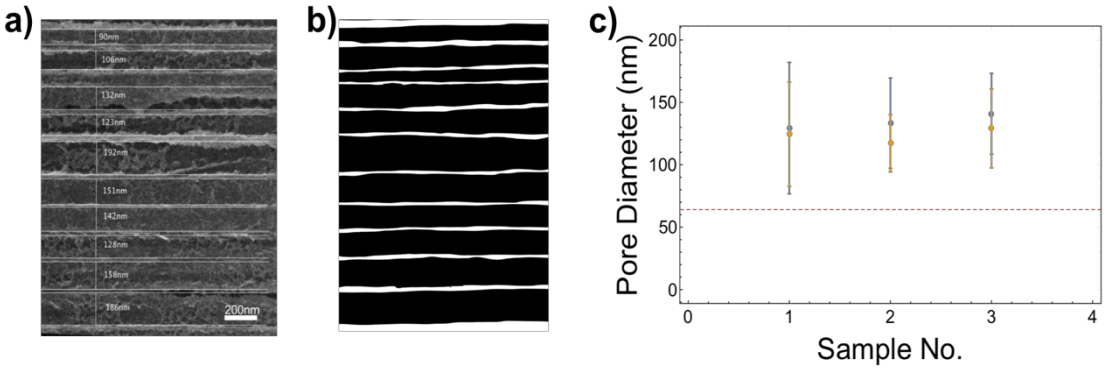

Figure A. 4 (**a**) cross-section image of pSi etched at 25mA/cm^2 with the location of the pore walls approximated by the white horizontal lines and the distance between the lines indicated by the vertical lines which correspond to the indicated measured width of the pores. (**b**) conversion of the image in (a) to black and white for analysis of the cross-sectional area of the pores in ImageJ. The cross-sectional areas are then divided by the length (horizontal width in the image) of the pores giving an estimate for the average diameter of each pore. (**c**) plot comparing the pore diameter calculated by both methods described in (a) and (b) for multiple samples. Each data point corresponds to the average from multiple images of a sample and the associated standard deviation. The red dashed line represents the average pore diameter determined from surface analysis.

A.2 Varying etch currents

For the second study, samples were etched at different current densities, which resulted in variations in pore sizes as shown in **Figure 2.7** in chapter 2. The surface analysis followed a similar approach to that presented in the section above. The distribution of pore diameters taken from surface images of the different samples are provided in **Figure A.5** with their respective fit and calculated values. Each histogram was generated from pore size values collected from multiple images at different magnification and concatenated (with padding) as described in the previous section. The calculated mean pore diameters range from an average of ~21nm to 57nm. The green data series in the plot in **Figure A.6** corresponds to the mean diameters estimated from the surface and the error bars represent the standard deviation. In the green data set in **Figure A.6** there is a gradual increase in pore diameter for etch currents of 12.5mA/cm^2 to 17.5mA/cm^2 showing mean pore diameter increasing from 21nm to 34nm, but between 17.5 and 20mA/cm^2 there is very little difference (34 to 35nm). This suggests there is very little difference between these etch currents in terms of its effects when etching pSi under the conditions described in chapter 2. This also appears to be the case from comparing the images in **Figure 2.7** in chapter 2. In going from 20mA/cm^2 to 22.5mA/cm^2 there is a significant jump in average pore diameter to 57nm accompanied by a smoothing of the pore walls and loss of intricacy in the morphology.

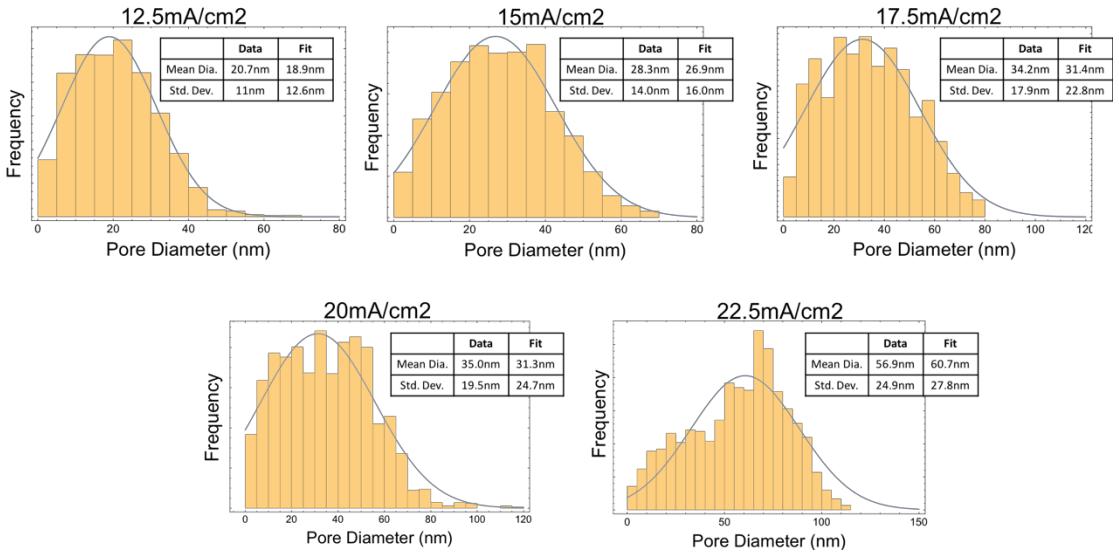

Figure A. 5 Distribution of pore diameters from SEM images of the surface of pSi films etched at different currents. Each curve is overlaid with a normal fit. The data and fitted means and standard deviations are provided for each distribution.

Cross-sectional analysis was less straightforward than in the previous section, particularly at lower etch currents, as the interior pore morphology has numerous protrusions and branches along the length of the pore walls and the pores are much smaller. This is apparent in the image for the 15mA/cm^2 sample in **Figure A.7**. The method of cross-sectional area analysis resulted in larger pore diameters than using a method of estimating the distance between adjacent pore walls. These methods are described in detail in the previous section. Additionally, simple estimation of an average location of the pore walls was not straightforward. This is opposite to that observed in the previous section, and is due to the intricacies in the pore morphology at low etch currents. For cross-sectional area analysis, the pore diameters increase from ~35 to 140nm, while estimating the distance between adjacent walls resulted in pore sizes increasing from ~30 to 120nm.

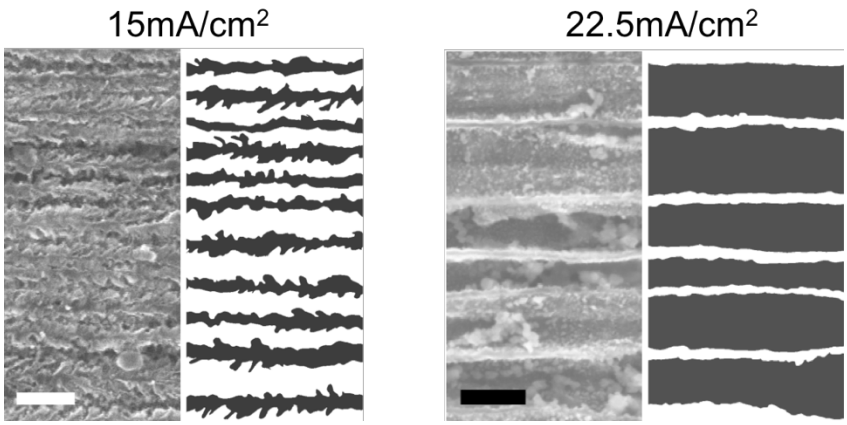

Figure A. 6 Cross-sections of pSi etched at 15mA/cm^2 and 22.5mA/cm^2. The pore morphology is very different between both samples, which make comparison of pore width by cross-section difficult. The black and white images are processed versions of the SEM images for cross-sectional area analysis as described for Figure A.4.

As in the surface analysis, the cross-sectional area analysis showed little difference between the pores etched at 17.5 and 20mA/cm^2 with mean pore sizes of 84 and 82nm, respectively. This is in agreement with the images shown in **Figure 2.7** in chapter 2, further confirming that there is little difference in the effects of these etch currents under the etching conditions presented in this dissertation.

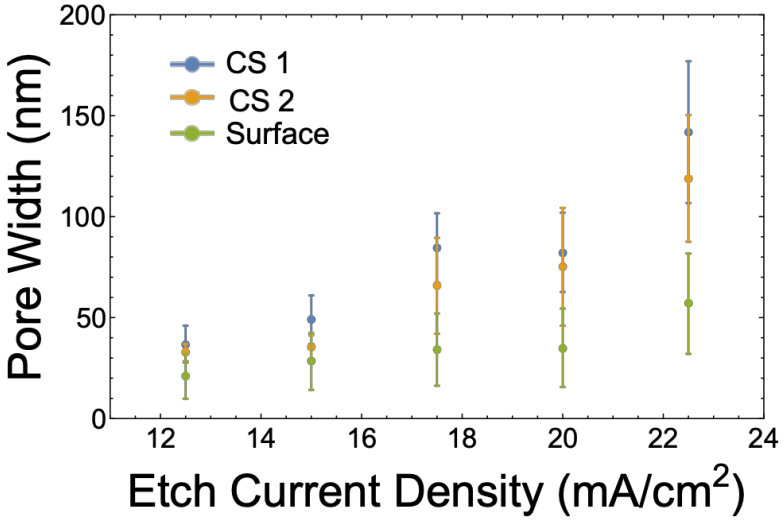

Figure A. 7 Plot of the estimated pore diameter vs. pore size. *Surface* corresponds to pore diameter estimated by surface analysis. *CS 2* is calculated from cross-section images by estimating the placement of the pore walls and measuring the distance between these estimates. *CS 1* is calculated corresponds from cross-section images by measuring the cross-sectional area of the pores within the image. See main text for details of each method.