Single-Event Upset Technology Scaling Trends of

Unhardened and Hardened Flip-Flops in Bulk CMOS

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CHAPTER I

INTRODUCTION

Section 1.1 Overview

A single event (SE) is caused by an ionizing particle that travels through silicon producing electron-hole pairs in an integrated circuit (IC). If the SE ion strike deposits charge near a transistor, the deposited charge may be collected by drift-diffusion processes, and potentially change the voltage of the circuit node associated with that transistor leading to single-event upsets (SEU) in memory storage elements or single-event transients (SET) in combinational logic that may be latched into memory [1]. For the advanced technologies, all environments, space as well as terrestrial, are vulnerable to single-event effects. Thus, designers must find methods to detect and mitigate these errors to ensure system integrity.

One area of focus for single-event effects (SEE) in ICs is flip-flop SEU error rates. Flip-flops are generally used as temporary data storage between operations in computer processing units (CPU) and in pipeline processor architectures. A SEU in a CPU's flip-flops can affect many operations resulting in errors at the output of the chip. When a semiconductor region in a flip-flop collects charge from a SE strike, an SET is produced in the flip-flop's latch circuit. If the SET is longer than the feedback loop delay of the latch, the data state of the latch is changed, resulting in an upset. The minimum amount of charge that must be collected to result in an SEU is called the critical charge (Q_{crit}). Typically, higher flip-flop Q_{crit} leads to increased SEU robustness for a design.

A flip-flop's Q_{crit} decreases if node capacitance, transistor drive current, or supply voltage decreases [2]. As CMOS technology feature sizes scale to smaller dimensions, transistor drive strength, node capacitance, and supply voltage decrease resulting in lower flip-flop Q_{crit}. As technology scaling continues, smaller amounts of charge are needed to cause upsets reducing the SEU robustness of flip-flops compared to older technologies. Such increased vulnerability has lead designers to find ways to either increase Q_{crit} through process changes or implement different flip-flop topologies to increase SEU robustness.

In the search for new SEU tolerant flip-flop topologies, designers harden flip-flops either through temporal [3] or storage-node redundancy [4] schemes. Temporal redundancy schemes employ multiple sampling of data at various times which requires multiple clocks and/or resistor-capacitance (RC) delays within the latch. Due to the speed penalties and complex clocking circuitry needed for temporal designs, redundant storage-node designs are favored among designers. For storage-node redundant designs, additional circuit is added to a flip-flop to increase the number of storage nodes. A latch in a flip-flop has only two data storage nodes, as shown in Figure 1, and is susceptible to SEUs even when charge is collected at any one of the circuit nodes. Figure 2 shows a dual interlocked cell (DICE) latch as an example of a redundant storage node latch that implements four storage nodes and will not upset from charge collection on a single node [4]. Of course, redundant storage node designs come at the cost of increased number of transistors, layout area, power, and lower operating speed of the design. As technologies scale, redundant node flip-flops have been shown to become more vulnerable to multiple node charge collection and designers have begun looking for alternatives to improve IC soft error rates (SER) [5]–[9].

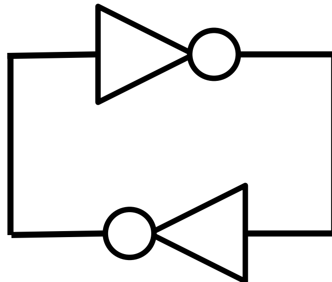

Figure 1. Schematic of a simple latch.

The goal of this work is to use experimental and simulation results for older technologies from literature and compare them to data from 40-nm and 20-nm technology nodes to establish SE trends in flip-flop designs. This work begins with a literary survey of various SE phenomena that cause flip-flop SEUs in hardened and unhardened designs. Then, background is given for different types of sources for SEEs and their relationship to SEUs in hardened and unhardened flip-flops. The remaining sections are divided between unhardened and hardened flip-flop sections to examine the trends separately.

Figure 2. Schematic of a DICE latch, a type of redundant storage node latch

Technology computer aided design (TCAD) simulations are used to examine various effects that can change the SEU cross section of a latch in a D flip-flop (DFF) with respect to various parameters that change as technology features sizes decrease. Experimental results for DFF designs show that the experimental SEU cross section decreases with technology scaling across the LET spectrum, which indicates that effects that will decrease a DFFs SEU cross section will dominate over the other effects that would cause the cross section to increase.

Hardened redundant storage node design experimental results show that the SEU cross section remains similar as technologies scale. TCAD simulations show that a combination of factors related to well potential modulation (WPM) activating the parasitic bipolar structure of pFETs is the dominating factor in determining the over SEU cross section.

Section 1.2 Background

Section 1.2.A. Single-Event Transients

When an ionizing particle deposits charge near an off transistor, a portion of the deposited charge may be collected by the transistor's source and drain junctions. If enough charge is collected to overcome the charge stored at the associated circuit node capacitance and the restoring current of the complementary transistors connected to the off-state transistor, the node voltage will be temporarily changed resulting in a single-event transient (SET). With sufficient amounts of collected charge, the SET amplitude can swing from rail-to-rail. The SET pulse width is proportional to the amount of charge collected by the off-state transistor, the circuit node capacitance, and restoring current transistor drive strength [10]–[14].

Technology feature size scaling, in part, aims to reduce node capacitance, transistor currents, and supply voltages to reduce power requirements and increase operating speeds. Reducing these three factors increases the likelihood of an ionizing particle to induce a rail-to-rail voltage transient. Benedetto et al., showed experimentally that as technologies scale, SET pulse widths and cross sections will increase with technology scaling and due to decreasing supply voltages in inverter strings [10]. Gadlage et al. showed that pulse broadening caused by long inverter chains and dissimilarities in well contacting in target inverter chains are affecting experimental data potentially skewing measured pulse widths to be longer than originally generated by SEs [15]. After taking into account factors affecting experimental results, SET pulse widths appear to decrease when scaling from 90-nm to 65-nm in bulk CMOS. Thus, there are conflicting results and the other works in this section provide insight as to how this may occur.

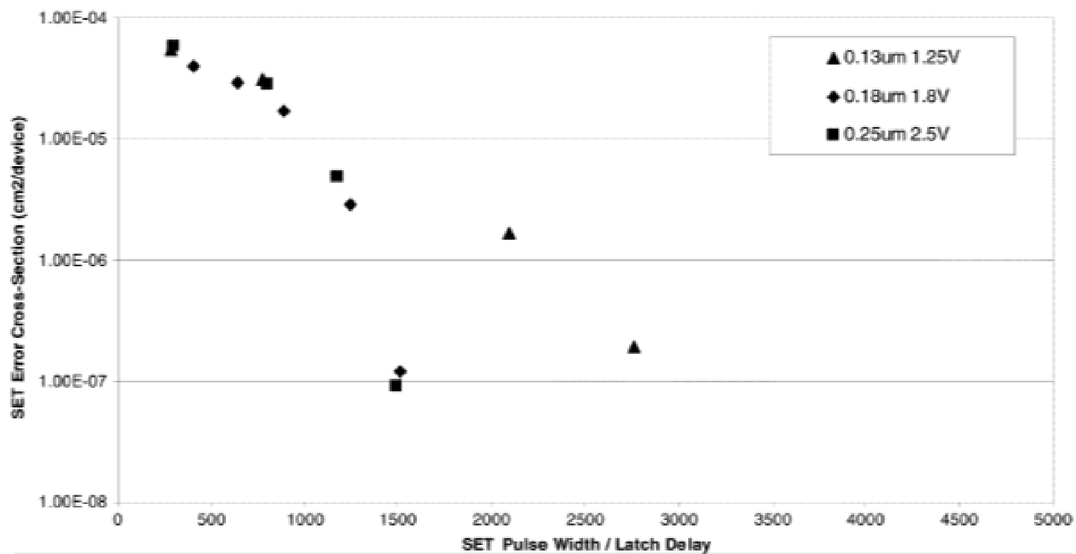

Figure 3. Inverter SE cross section vs. the ratio of SET pulse width to measurement latch circuit delay for an ion with LET of 60 MeV-cm^2/mg at three technology nodes from [10].

As technologies feature sizes decrease, transistor area and pitch decreases leading to higher transistor densities and more circuitry that can be implemented on an IC. This decrease in transistor pitch has greatly increased the probability that a single ionizing particle can deposit charge in the vicinity of multiple transistors and affect multiple

circuit nodes, commonly called charge sharing or multiple node charge collection, illustrated in Figure 4 [16]. Charge sharing has been demonstrated in multiple experiments to reduce SET pulse widths and cross sections in inverter strings [17]–[20]. Ahlbin et al. showed experimentally that when the effects of charge sharing are increased by not implementing guard bands (additional well contacts) in inverter strings, the SET pulse widths decrease compared to inverters with less charge sharing due to additional guard bands at 130-nm technology node, shown in Figure 5 [19]. Another mechanism, called pulse quenching, occurs in inverter strings when multiple logic gates electrically connected collect charge due to a single ion hit. Here the SET generated by the node that initially collects the SE deposited charge produces a SET and the charge collected by other electrically related logic gates in the path of the SET transient reduce the pulse width of the original SET pulse. As the probability of charge sharing, and subsequently pulse quenching, increases with scaling, circuit design methodologies may be developed that reduce overall SET pulse width to improve radiation hardening of flip-flops.

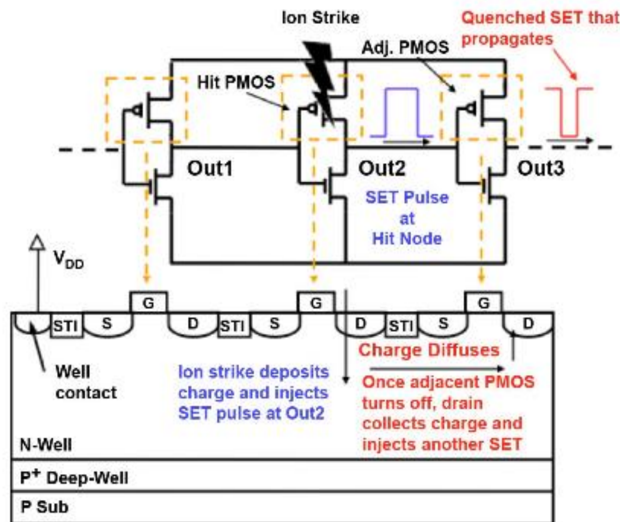

Figure 4. Illustration of charge sharing among pFETs in an inverter chain from [18]

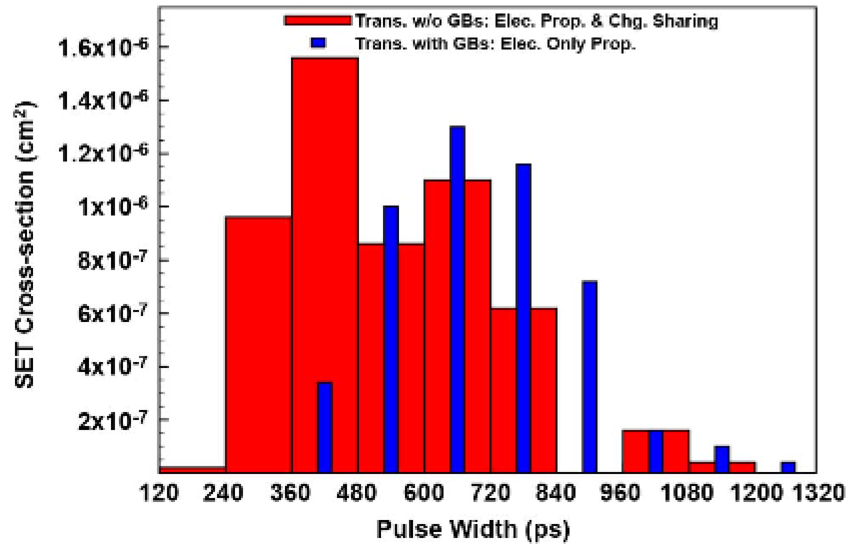

Figure 5. SET cross section vs. pulse width for inverter strings with and without guard bands in 130-nm bulk CMOS. The inverter strings without guards have a higher probability to share charge and reduce SET pulse widths from [18]

There is another effect that reduces SET cross sections due to increases in charge sharing and increased transistor densities due to scaling. Atkinson et al. showed experimentally that increased transistor densities can reduce SET cross sections of inverter chains [20]. The presence of dummy transistors placed around the inverter chain targets, illustrated in Figure 6, compared to isolated inverters can reduce the SET cross section by up to 70% in a 90-nm bulk CMOS process. The dummy inverters are able to collect charge from SE strikes far from the sensitive inverters and preventing a SET. Even though the presence of other transistors near the sensitive inverters may not reduce the SET pulse widths, increasing the presence of non-sensitive transistors near sensitive transistors can reduce the number of SETs. A higher probability of non-sensitive transistors reducing SET cross sections occurs as transistor densities increase with technology scaling.

It is important to note that SETs can cause SEUs in flip-flops in two ways: by occurring within the latch or propagating from logic circuits and being latched into the flip-flop at a clock edge. This work focuses on SETs that occur within the flip-flop creating an SEU. If the SET is longer than the feedback loop delay of the flip-flop's latch, an SEU will occur. With scaling, SET transients can become longer and have a higher probability of becoming an SEU, but increased probability of SET pulse quenching and

higher density of non-sensitive transistors in a flip-flop's latch may help to reduce the chance of SEUs occurring. In this report we explore how these mechanisms manifest into SEU cross sections as a function of technologies currently in use by the semiconductor industry.

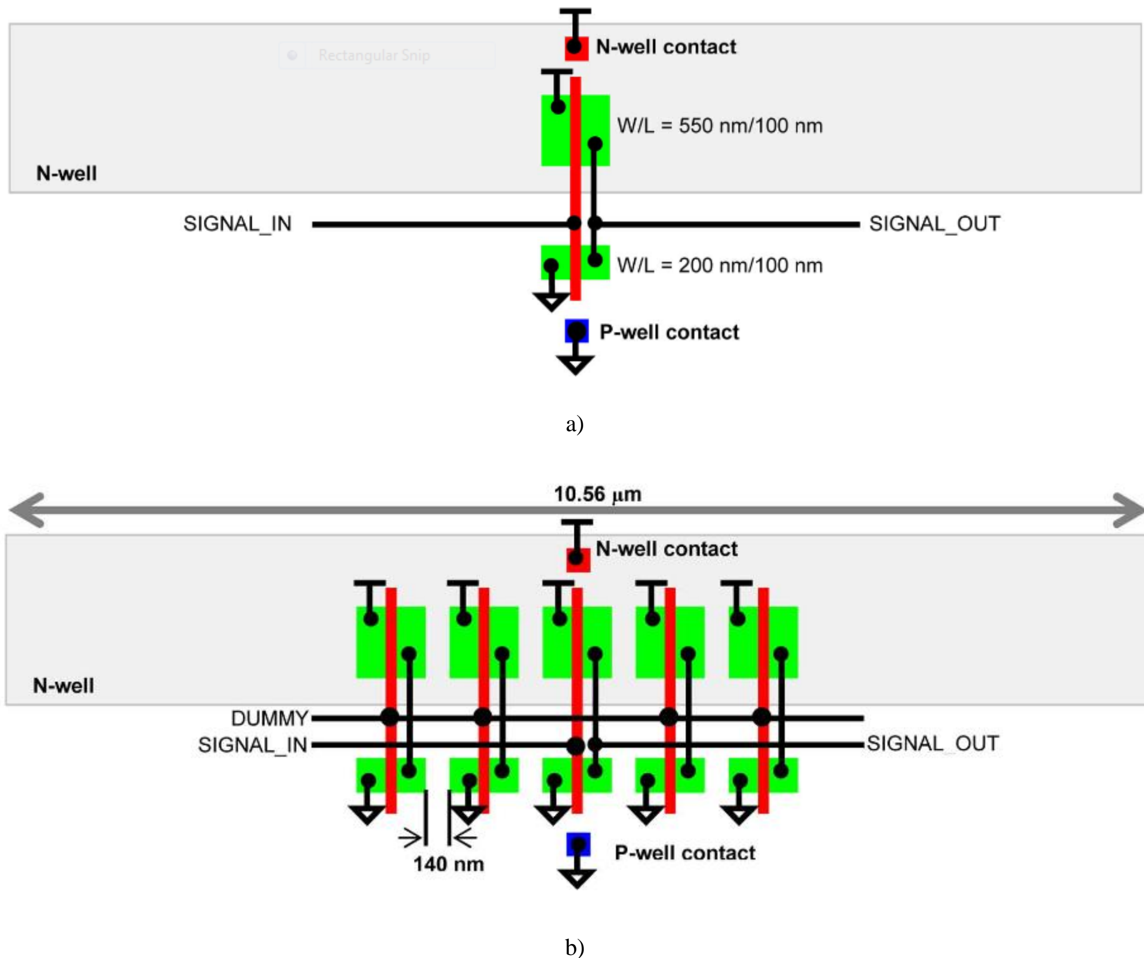

Figure 6. Illustration of inverter chain targets implemented in 90-nm bulk CMOS from [18] a) shows the inverter chains where the sensitive inverters are not surround by transistors. b) shows the inverter chains that are surrounded by dummy inverters.

The parasitic bipolar structure of MOSFETs have been shown to turn ON by SET inducing ion strikes as illustrated in Figure 7 [21]–[24]. A SE strike deposits charge that is collected by transistor and well-contacts. As well-contacts collect charge, a potential drop is formed from the strike location to the well-contacts. The longer the charge remains in the well, the longer the well potential is modulated causing the parasitic bipolar to turn ON for a longer time. The parasitic bipolar transistor injects current from the source into the drain increasing SET pulse widths. Ahlbin et al showed

experimentally that SET pulse widths can reach up to 4 ns if well-contacts are spaced 30 μm apart in inverter chains; but if strip contacts are used along the wells, SET pulse widths are limited to a maximum with of 600 ps [23]. Thus, proper well-contacting is important in reducing SET pulse widths.

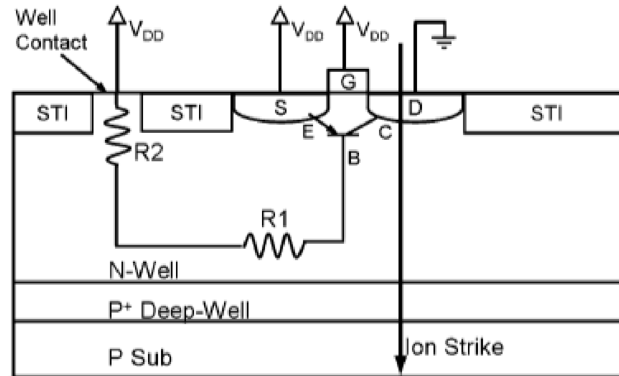

Figure 7. Illustration of parasitic bipolar of a pFET and resistances that affect bipolar activation from [20]

Section 1.2.B. Single-Event Upsets in SRAMs

Due to the similarities of some latches used in flip-flop designs and Static Random Access Memory (SRAM) cells, it is important to survey the SEEs and technology scaling effects in SRAMs. Both SRAM cells and latches (unhardened designs) are generally composed of cross coupled pair of logic gates (usually inverters) resulting in only two data storages nodes. If sufficient charge is deposited on one of the two storage nodes, an SET is generated. If the SET pulse width is longer that the feedback loop delay of the design, it will result in an SEU. Typically, the Q_{crit} for a latch is 10X to 100X higher than an SRAM cell at a given technology node [2]. The remainder of this section focuses on SEE trends vs. scaling seen in SRAM cells.

One metric used to judge SRAM sensitivity vs. technology scaling is Q_{crit} [2], [25]–[32]. Knowing the critical charge and the sensitive charge collection region of an SRAM cell, designers can estimate the single-event error-rate of a design. Technology scaling has been shown to reduce the Q_{crit} of SRAM cells, shown in Figure 8 [2], [31].

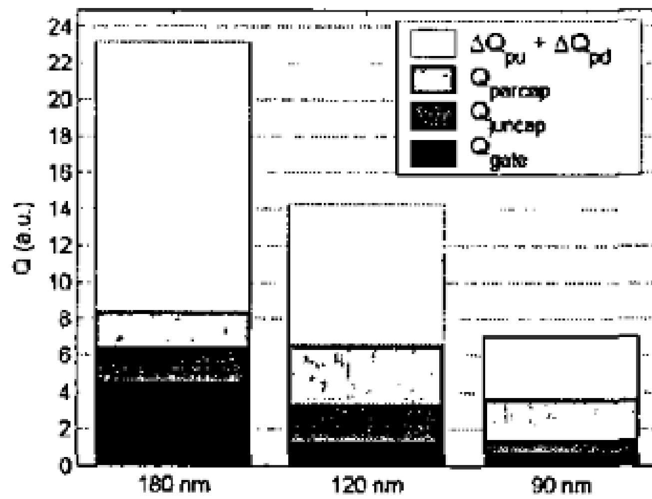

Figure 8. SRAM Q_{crit} vs. technology feature size from [25]. $Q_{pu} + Q_{pd}$ is the critical charge produced by the transistor drive currents and make up a significant portion of the total Q_{crit}.

SRAM neutron and alpha SER has been reported to increase or decrease with technology scaling and is mostly dependent on process parameters or circuit design. Seifert et al. showed SRAM neutron and alpha error rates decrease for feature sizes below 180-nm for various processes [2]. Other works show the SRAM alpha SER continues to increase until 65-nm and may continue decrease, but the neutron SER continually decreases below 180-nm [33], [34]. This shows there is some process and/or circuit affects in the technology scaling trends of SRAMs. Seifert et al. predictions shows at some point below 180-nm, the Q_{crit} of SRAM cells becomes very small that cells are easily upset and the soft error rate (SER) ultimately becomes a function of the SRAM cell area.

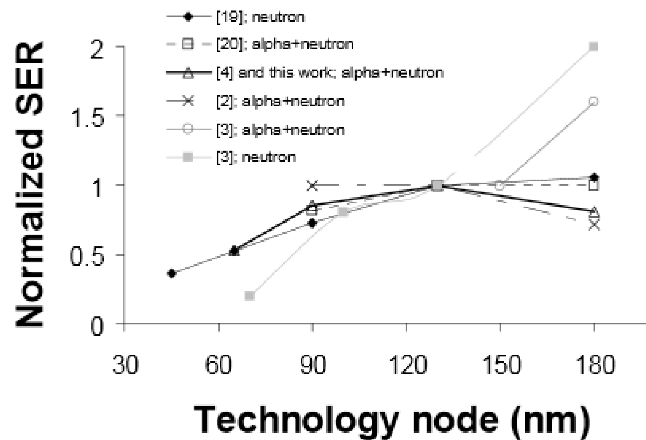

Figure 9. Normalized SER for SRAM cells vs. technology feature size for various works from [2].

Another consequence of smaller transistor areas that come with feature size scaling is the decreased distance between SRAM cells, resulting in an increased probability for charge sharing between multiple SRAM cells and the subsequent increase in multiple cell upsets [2], [25], [28], [35]–[39]. Multiple cell upsets (MCUs) in SRAM arrays can potentially defeat error-correcting code schemes leading to corruption of data. Gasiot et al. showed that SRAM MCUs have been attributed to well-potential modulation (sometimes called well-potential collapse) and is a major contributor to SRAM SER at 65-nm [39]. Seifert et al. has shown that MCUs can span up to 3 μm below 90-nm [40].

A way to study charge sharing effects on SRAM cell upset rates is by characterizing the difference between dual- and triple-well processes. Chatterjee et al. showed experimentally that SRAM implemented in triple-well can have lower SE single cell upsets (SCU) and multiple cell upsets (MCU) at LET values above 24 MeV-cm^2/mg [37]. For higher LET ion strikes, the amount of deposited charge results in longer perturbation of well-potential, allowing SRAM cells to upset twice (resulting in no upset). Thus, triple-well process enhances the charge sharing in the nFETs preventing SCUs and MCUs in the SRAMs compared to the dual well process at LET values above 25 MeV-cm^2/mg. For LET value below 24 MeV-cm^2/mg, the triple-well option perform worse than the dual-well option for both SCU and MCU due to lower probability of

charge sharing preventing upsets. Thus, charge sharing in SRAM cells can be an important mechanism in preventing SEUs at high LET values.

Section 1.2.C. Flip-flop SEU

There are many different ways to create unhardened flip-flops, but they are similar in that they use a feedback loop similar to an SRAM cell in the master/slave latches. Some flip-flop latches are almost identical to an SRAM cell. Thus, the mechanisms that cause SEUs in SRAM cells are similar for flip-flops. The technology scaling effects on flip-flops SE cross sections and SER have been studied in literature, but not as comprehensively as SRAM cells. This section looks at the literature studies of flip-flops, both unhardened and hardened.

Technology scaling trends have been reported for alpha and neutron experiments in flip-flops [2], [31], [38], [39], [41]–[43]. Seifert et al. showed experimentally that flip-flop alpha and neutron SER decreases for processes below 130-nm, shown in Figure 10 [2]. In the same paper, data compiled from different works is compared for flip-flops across technology nodes, but show some disagreement, shown in Figure 11. These results show that the flip-flop alpha and neutron SER will at best decrease or remain the same as technology scaling progresses.

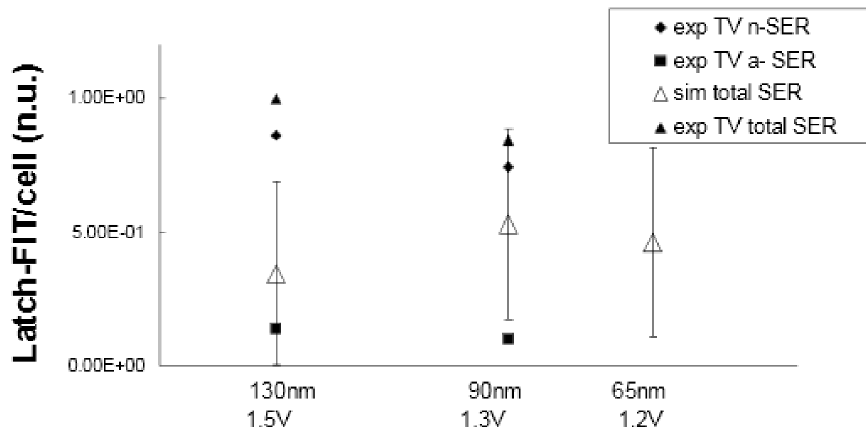

Figure 10. Flip-flop neutron (n-SER) and alpha (a-SER) for three technology nodes from [2].

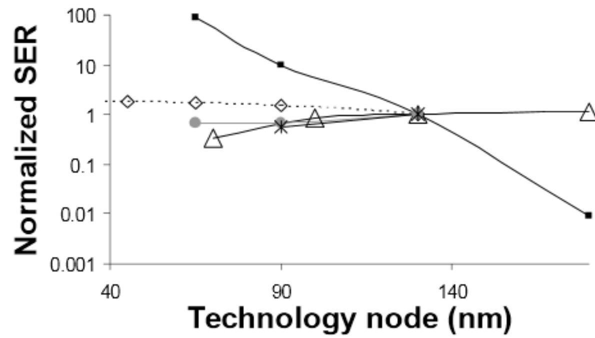

Figure 11. Calculated SER values vs. technology node compiled in [2].

Heavy-ion experiments for unhardened flip-flops have been conducted for various technology nodes, though they have never been directly compared [5], [8], [44]–[47]. In Figure 12, 90-nm bulk heavy-ion results for a range of LET values show the classical flip-flop cross section curve [5]. One thing that is common in all these works is that hardened flip-flop SE cross sections robustness is decreasing compared to unhardened flip-flops.

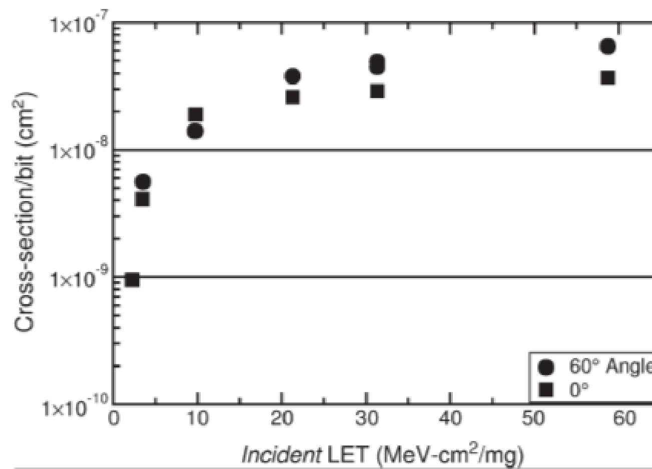

Figure 12. 90-nm heavy-ion SE cross section vs. LET from [5].

Amusan et al. showed that charge sharing can cause SEUs to occur in hardened flip-flops [5]. Figure 13 shows an example of how charge sharing can cause an upset in a simple latch; if charge is collected at an off pFET and an off nFET in the latch, an upset will occur. The charge required at both the nodes to cause an upset is lower than the

charge required for a single node upset. It has been shown that the amount of charge to upset a flip-flop by charge sharing decreases with technology scaling [48]. Since the probability for charge sharing increases with scaling, the probability of an upset due to charge sharing also increases with technology scaling.

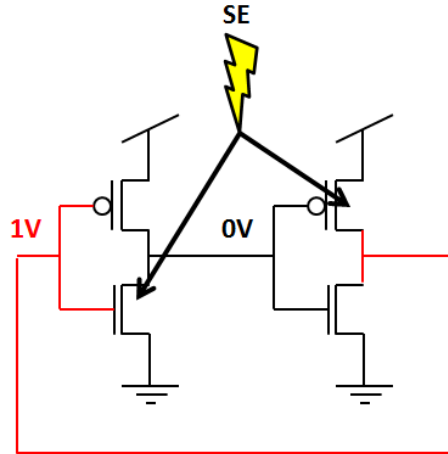

Figure 13. Example of charge sharing upsetting a latch. Charge collected at the pFET and nFET can cause a SEU.

Charge sharing has also been shown to prevent SEUs in unhardened flip-flops [47], [49]. Figure 14 shows an example of how charge sharing between the two pFETs in a latch can prevent an SEU. Kauppila et al. showed that charge sharing can reverse the original upset by collecting charge on the complimentary storage node [49]. Seifert et al. showed that if the distance is reduced between unhardened flip-flop storage nodes, charge sharing has a greater chance to reduce SE cross section of a design [47]. Thus, there are competing mechanisms in unhardened flip-flops that may increase or decrease the flip-flops SE cross section depending on layout and other factors as technology feature sizes become smaller.

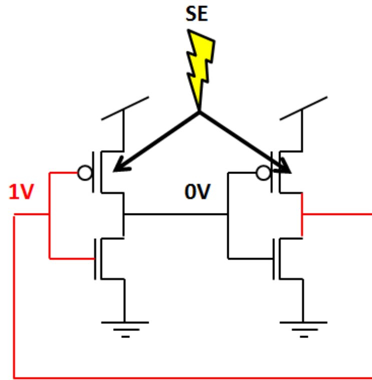

Figure 14. Example of charge sharing preventing an upset in a simple latch.

To improve the SE robustness of registers, flip-flop designs with redundant storage nodes, such as DICE, were developed [4]. The schematic for a DICE latch introduced by Calin et al. is shown in Figure 15. The transistors of the DICE latch are connected in such a way that charge collection on a single node will not result in an upset and the flip-flop will recover from all voltage perturbations caused by an incident ion. Amusan et al. have showed that for hardened flip-flops, such as DICE, SE robustness is very sensitive to the spacing between storage nodes of transistors [5], [46], [50]. This is mainly due to the charge sharing between two (or more) storage nodes of DICE-like designs. Charge-sharing renders these flip-flops vulnerable to single events. Because of this vulnerability, designers have looked for other redundant storage node designs to improve the SE reliability of flip-flops in bulk CMOS. These designs include Quatro [51], built-in soft error resilience (BISER) [52], SEU tolerant (SEUT) [53], Bistable Cross-coupled Dual-Modular Redundancy (BCDMR) [54], soft error immune latch (SEILA) [55], [56], and Layout Design through Error-Aware Transistor Positioning (LEAP) DICE [57], [58].

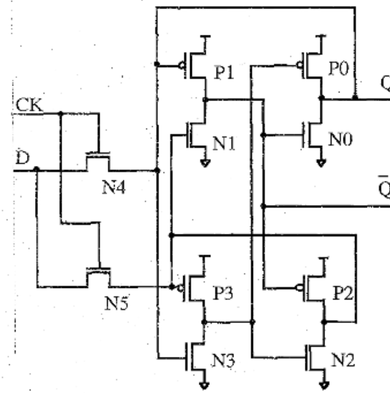

Figure 15. DICE schematic introduced by Calin et al. [4]

The Quatro latch created by Rennie et al. is similar to DICE, but with a small change in the schematic topology [54]. The Quarto schematic topology has two fewer sensitive node pairs per latch compared to a DICE-like topology [8], [54], shown in TABLE I. The fewer sensitive node pairs of the Quatro latch has been shown to produce a lower SE cross section in heavy-ion experiments in a 40-nm bulk process, shown in Figure 17. For neutron experiments, the Quatro latch performs better than a DICE-like latch as shown in TABLE II. Thus, by altering a DICE-like topology and reducing the number of sensitive node pairs it is possible to reduce the flip-flop cross section.

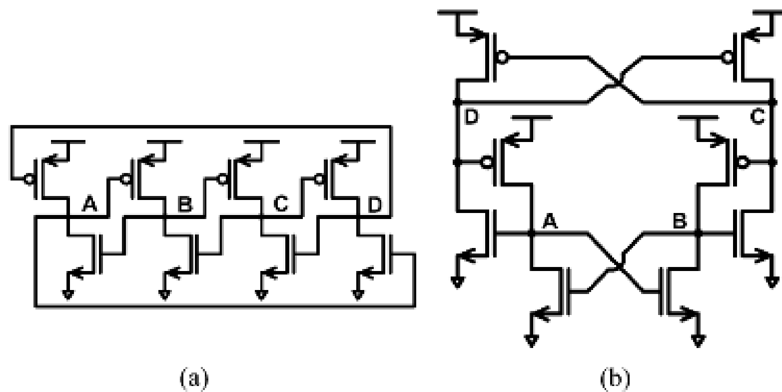

Figure 16. Schematic of a DICE latch (a) and Quatro latch (b) from [51]

TABLE I. Number of Sensitive Node Pairs in DICE and Quatro from [8]

Latch	# of sensitive node pairs for data at nodes A and C = logic 0 and nodes B and D = logic 1		
	NMOS-NMOS	PMOS-PMOS	NMOS-PMOS
DICE	1	1	12
Quatro	1 (N_B and N_D)	1 (P_A and P_C)	10

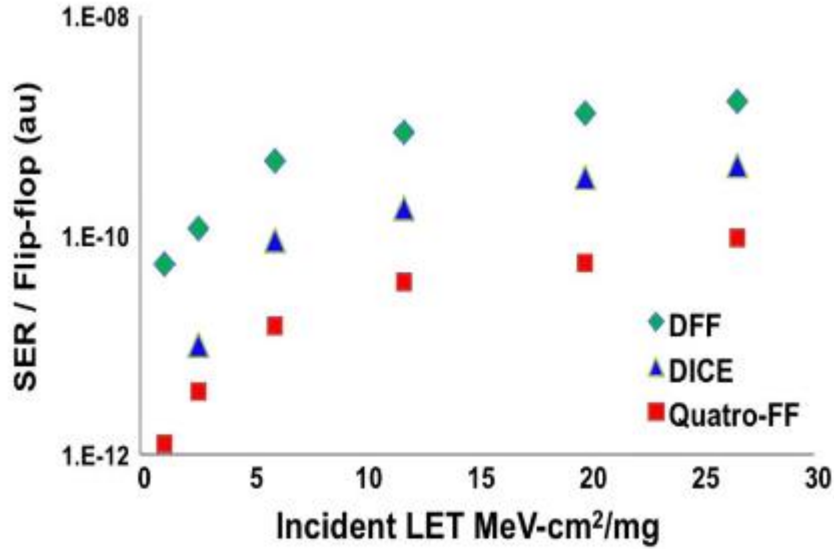

Figure 17. Heavy-ion cross section vs. LET at normal incidence for DFF, DICE, and Quatro in a 40-nm bulk process from [8]

TABLE II. Neutron experiment SER at 65-nm bulk from [50]

	area (um^2)	V_{DD} (V)	time (hr)	errors	cross-section (10^{-10} cm^2)	cross-section bound (10^{-10} cm^2)	SER (FIT/ Mbit)	SER bound (FIT/ Mbit)
DFF	9.9	1.0	2.1	2	1.27	1.91	338.8	508.2
		0.9	5.4	7	1.74	1.99	465.0	531.4
		0.8	16.2	28	2.34	2.43	625.1	647.4
Quatro	11.7	1.0	2.1	0	0.00	0.64	0.00	169.4
		0.9	5.4	1	0.25	0.50	66.4	132.9
		0.8	16.2	0	0.00	0.08	0.00	22.3
DICE	15.0	1.0	2.1	0	0.00	0.64	0.00	169.4
		0.9	5.4	2	0.50	0.75	132.9	199.3
		0.8	16.2	1	0.08	0.17	22.3	44.7

The SEUT design is similar to a DICE design, but uses a different clocking method to write the data to the latch and reduce power consumption, shown in Figure 18

[56]. Neutron experiments show that the SEUT has 30X smaller SER than an unhardened flip-flop, as shown in Figure 19.

Figure 18. Schematic of the SEUT latch from [53]

Figure 19. Neutron experimental results in 90-nm bulk for DFF (L1) and SEUT with different threshold voltage implants (L2-4) from [53]

SEILA latch is similar to the DICE design in that it also uses cross coupled multiple storage nodes and does not upset from charge collected on a single node [58], [59]. This method uses a C-element in place of one of the nFET-pFET pairs, shown in Figure 20. The C-element acts as a low pass filter (LPF) helping to block small transients from upsetting the latch, but this is only effective for small amount of charge and the author predicts this will not be useful for the space environment [62]. Neutron experiments show the SEILA latch can obtain ~50X reduction in SER compared to a standard DFF [58].

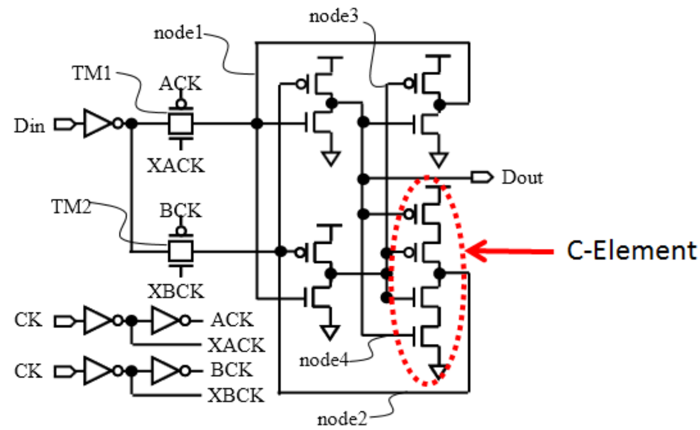

Figure 20. Schematic of SEILA latch after [54]

The BISER flip-flop design uses a slightly different approach from DICE by using a form of triple mode redundancy (TMR) to harden the flip-flop [55]. The BISER design uses two parallel flip-flops connected to a C-element, shown in Figure 21. When uncorrupted data is stored in both the two flip-flops, the C-element writes the correct data to the keeper latch. Due to the presence of the C-element, the keeper latch will retain the previously written correct value even if one of the flip-flop values is changed by a single event. If only the keeper latch is stuck by an ion, the data will be overwritten in the keeper latch by the two flip-flops controlling the C-element. If any combination of two of flip-flops or keeper circuit has erroneous data, an SEU will occur in the BISER design. Neutron experimental results for a BISER design show a 10X reduction in SER compared to the conventional DFF [57].

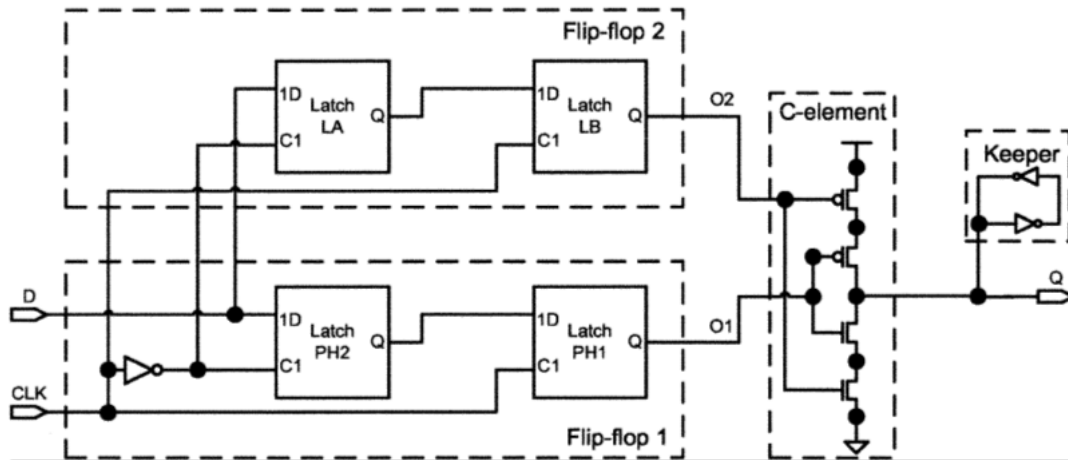

Figure 21. Schematic of the BISER design from [52]

The BCDMR design is similar to the BISER design, but with a small change to reduce the chance of SETs generated in the latches from creating an SEU at a clock edge [57]. The BCDMR design implements C-elements at the output of the master and slave stages, shown in Figure 22. Neutron experiments show that the BCDMR designs has a ~100X lower SER than the BISER at clock frequency of 300 MHz [57].

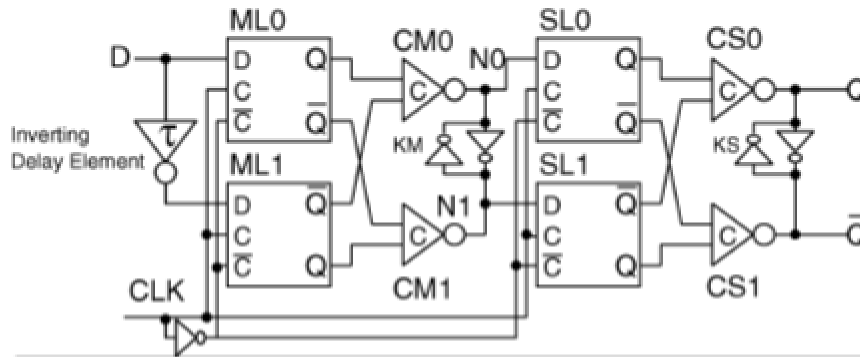

Figure 22. Schematic of the BCDMR design from [54]

The LEAP DICE uses a DICE schematic topology but places transistors in the layout to use charge sharing to prevent SEUs [60], [61]. The LEAP principle can be applied to any circuit by increasing the charge sharing between the nFETs and pFETs that drive a circuit node. When this is done, the resulting SET becomes smaller, as shown in Figure 23. In 180-nm bulk CMOS process, the LEAP DICE had ~2000X lower SER than a standard DFF and 5X lower SER than a standard DICE FF when exposed to neutrons [61].

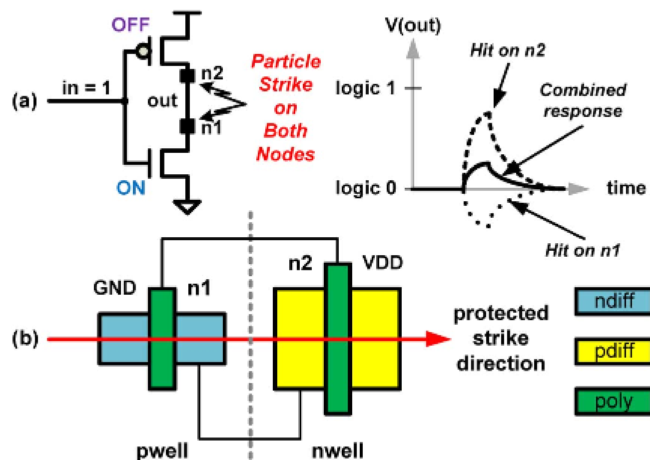

Figure 23. LEAP principle for an inverter with transistor alignment. (a) Reduced charge collection when a particle hits both NMOS and PMOS drain nodes of an inverter simultaneously. (b) Transistor alignment to reduce charge collection in the horizontal direction [57]

Many works have shown that multiple node charge collection from a single ion strike (charge sharing) can upset a DICE-like latch [4], [5], [8], [49], [52], [53], [63], [64]. Calin et al. showed in a 1.2 µm bulk epi process that a DICE latch can be upset in laser experiments with a upset laser energy threshold of 16.1 pJ (author estimates the LET is ~ 48 MeV-cm^2/mg) [63]. By increasing the distance between sensitive node pairs in the layout, it is possible to reduce the SE cross section of a DICE-like design [5], [49], [53]. Baze et al. showed in heavy-ion experiments that a DICE-like flip-flop design with 5-µm spacing between nodes is still susceptible to angular ion strikes.

Amusan et al. showed that charge sharing causing upsets in flip-flops mostly occurs between transistors in the same well (pFET-to-pFET or nFET-to-nFET) [24], [52]. Charge sharing occurs due to drift and diffusion of carriers deposited by an ion strike and well potential modulation activating the parasitic bipolar of the MOSFET structure. The use of guard bands and separate wells helps to reduce same well charge sharing. Charge sharing across the n-well/p-well boundary is less efficient than charge sharing in the same well, thus pFET-nFET charge sharing is less of a concern than pFET-pFET or nFET-nFET charge sharing [52].

All of these studies show that there are many different ways to harden a flip-flop design. However, all of these designs are susceptible to charge sharing and well-potential modulation effects. Charge sharing and well potential modulations may improve or worsen the overall single event error rate based on the design, layout, incident particle

type, deposited charge, etc. All of these factors must be considered before choosing a design for a given environment.

Section 1.2.D. Space and Terrestrial Environments

Different types of radiation are encountered in the space and terrestrial environments. The particles in both of these environments may either cause nuclear reactions in semiconductor materials producing secondary ionizing particles or deposit energy directly through Rutherford scattering. In either case, the end result of interest is the creation of electron-hole pairs in the semiconductor material. Since the deposited energy, and the resultant number of electron-hole pairs, is dependent on the incident particle type, it is important for the designer to understand how the charge is deposited.

In space, one set of radiation particles of concern are heavy ionizing particles, such as iron [65]. Figure 24 shows the integral flux of the heavy-ion LET spectrum at geosynchronous orbit. There is a wide range of ionizing particles of varying LET. The higher the LET of the particle, the more charge it can deposit and the more circuit nodes that can be affected by charge sharing [66].

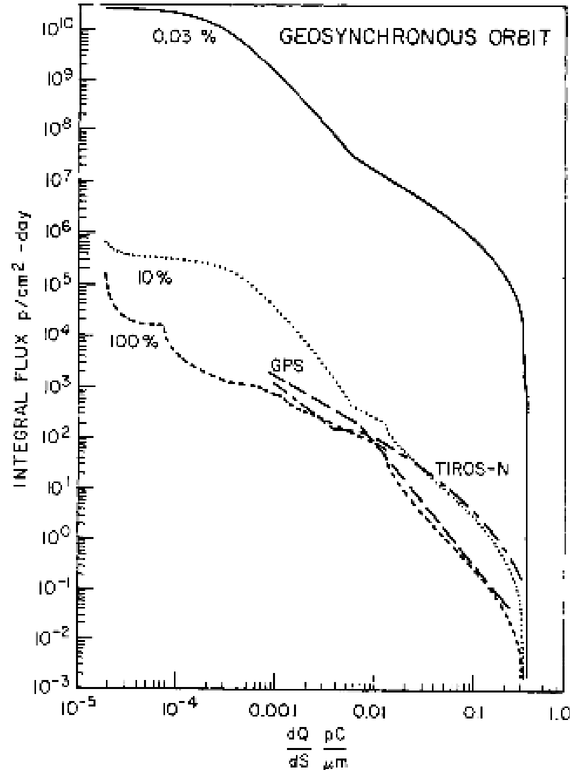

Figure 24. Integral energy loss spectrum at geosynchronous orbit from [62]

Protons are another radiation particle of concern in space [66]. Protons can interact with the semiconductor materials present on an IC and produce secondary ionizing particles. These secondary ionizing particles are ejected at angles within the IC and able to deposit charge near multiple transistors. At proton energies <2 MeV, direct ionization caused by protons can become a reliability issue [67]. The peak LET of low energy protons is 0.5 MeV-cm^2/mg and a result, only deep-sub-micron technology node designs are vulnerable to low energy protons.

Similarly, in the terrestrial environment, neutrons are able to cause secondary particles by interacting with the nucleus of IC materials. These neutrons are produced from radiation interactions with the earth's atmosphere, and the neutron flux decreases with decreasing altitude. Again, the generated neutron secondary ions can deposit charge over a large area causing charge sharing among multiple circuit nodes [37], [46], [68], [69].

Each time a neutron or proton interacts with the nucleus of an atom (referred to as an inelastic collision), secondary particles may unpredictably be ejected in all directions, illustrated in Figure 25 [70]. Many different particles, energies, and LET values can result from a neutron event with a silicon atom, shown in Figure 26 and Figure 27 [71]. Combining these results with the distances seen in Figure 28, it is easy to see that these generated secondary particles can deposit charge across a large area.

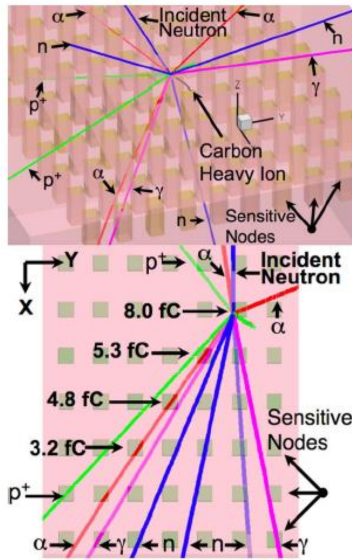

Figure 25. MRED generated nuclear event. The shaded volumes represent the sensitive nodes of the memory device. The incident neutron enters and induces a nuclear event. The shower of secondary products includes alpha particles, protons, neutrons, gamma rays, and a carbon heavy ion (n + Si → C + 3n + 2p + 3α). In the top–down view on bottom, the generated charges for sensitive nodes with more than 1 fC are labeled from [67]

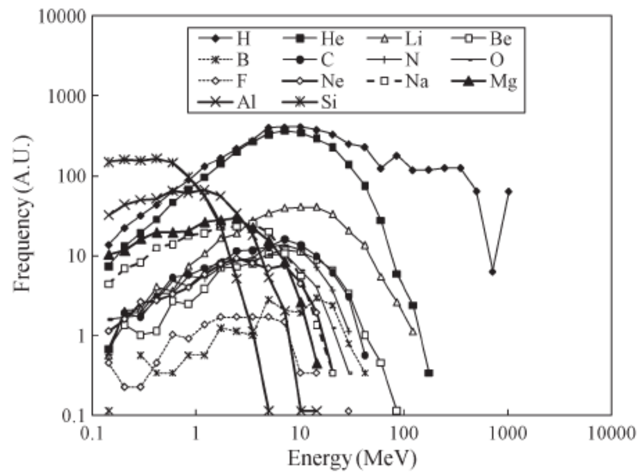

Figure 26. Relative frequency of secondaries produced from neutron-silicon collisions versus energy at sea level in New York City from [68]

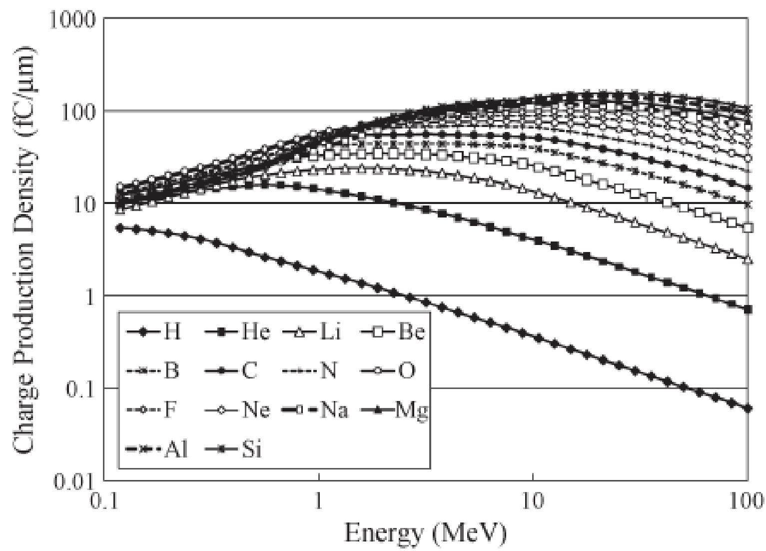

Figure 27. Density of electron-hole pairs generated in silicon [68]

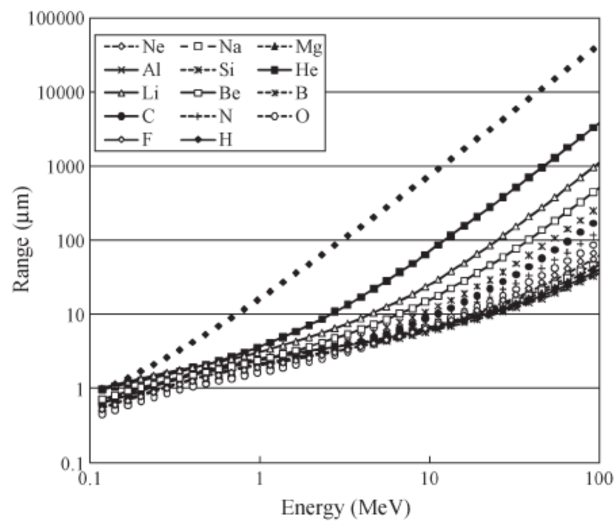

Figure 28. Neutron secondary particle distances in Si vs. energy [68]

Impurities in IC packaging and the silicon wafer itself can create alpha particles and are a concern for terrestrial applications [46]. These alpha particles can travel up 100 µm in silicon and have been shown to create multiple cell upsets in SRAM cells even though they have a very low LET [25].

All these results show a need for evaluating the trends for conventional and hardened flip-flop designs at advanced technology nodes. The availability of such trends will allow designers to anticipate error rates for their latest designs without having to get

actual experimental data. Since experimental data is available only after the technology has been in use, designers often do not have any knowledge of SER values for their designs until after they are fabricated. Analysis presented in this work will allow designers to assess the vulnerability of their designs to a first degree without requiring any experimental data. Since different flip-flops designs will have different response to single events, this thesis uses multiple non-hardened and hardened designs to evaluate the SER trends for technology scaling.

Section 1.3 Dissertation Overview

As mentioned in the introduction, this works aims to characterize the SEU cross sections of both DFFs and hardened FF designs experimentally and with TCAD simulations.

Chapter 2 covers the basic 90nm bulk CMOS TCAD structure and associated compact models used for simulations.

Chapter 3 focuses on the mechanisms that affect the SEU cross section of DFF designs across a broad LET spectrum and shows where future work may need to look to find the determining factor.

In Chapter 4, the experimental and TCAD simulation SEU cross section response of hardened FF designs are examined.

Chapter 5 DFF and hardened FF SEU cross sections are compared to show both trends as technology scaling continues.

CHAPTER II

MOSFET SIMULATION MODELS

Section 2.1 Overview

This chapter covers the basic MOSET models used in later 3D TCAD simulations. The MOSFET models are based on the IBM 9SF 90nm bulk CMOS technology node. The information presented here is thoroughly covered in [59], but are briefly repeated here for the reader.

Section 2.2 3D TCAD MOSFET models

Previously calibrated full 3D TCAD device models were used as baseline structures for all simulations. Calibration details are thoroughly covered in [59]. The well structure and STI depth are based on 130nm technology node, as these are expected to be similar. Model creation and heavy ion simulation are performed with Synopsys Sentaurus tools, specifically the models are built with Structure Editor and Mesh then bias and heavy ions simulations are performed by SDevice [60]. Simulations were performed on the ACCRE computing cluster at Vanderbilt University [61]. This section covers then current characteristics of the models and detailed structures of the transistors and wells.

The nFET size used in all simulations has an actual channel length of 80nm and width of 280nm. The current versus voltage curves are shown in Figure 29. In Figure 30, the basic nFET, p-well, p+ buried layer, and p-substrate are shown. All doping implants are created using Gaussian profiles shown in Figure 31.

The actual length used in pFET simulations is 80nm. Two pFET widths are used, 280nm and 840nm. Current versus voltage sweeps are for a pFET with 280nm width are shown in Figure 32. The basic pFET, n-well, p+ buried layer, and p-substrate are displayed in Figure 33. Gaussian doping profiles versus depth are contained in Figure 34.

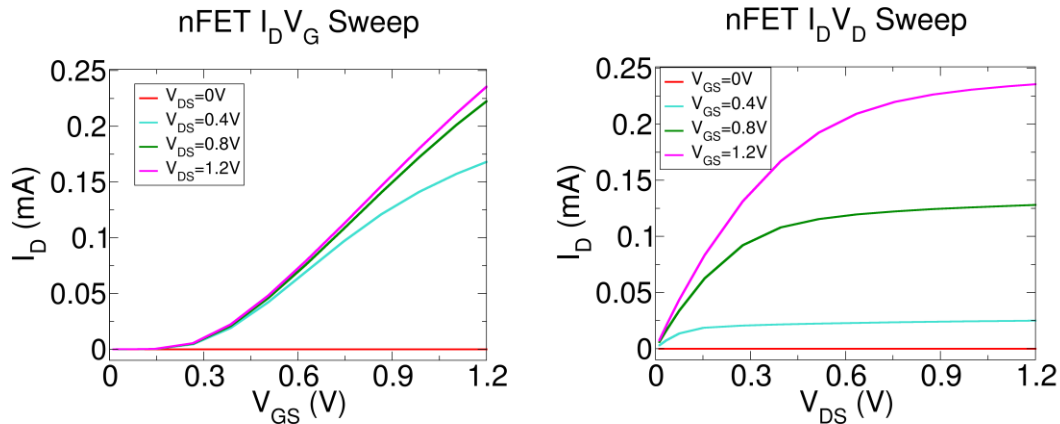

Figure 29. Current versus voltage sweeps for a nFET with L=80nm and W=280nm.

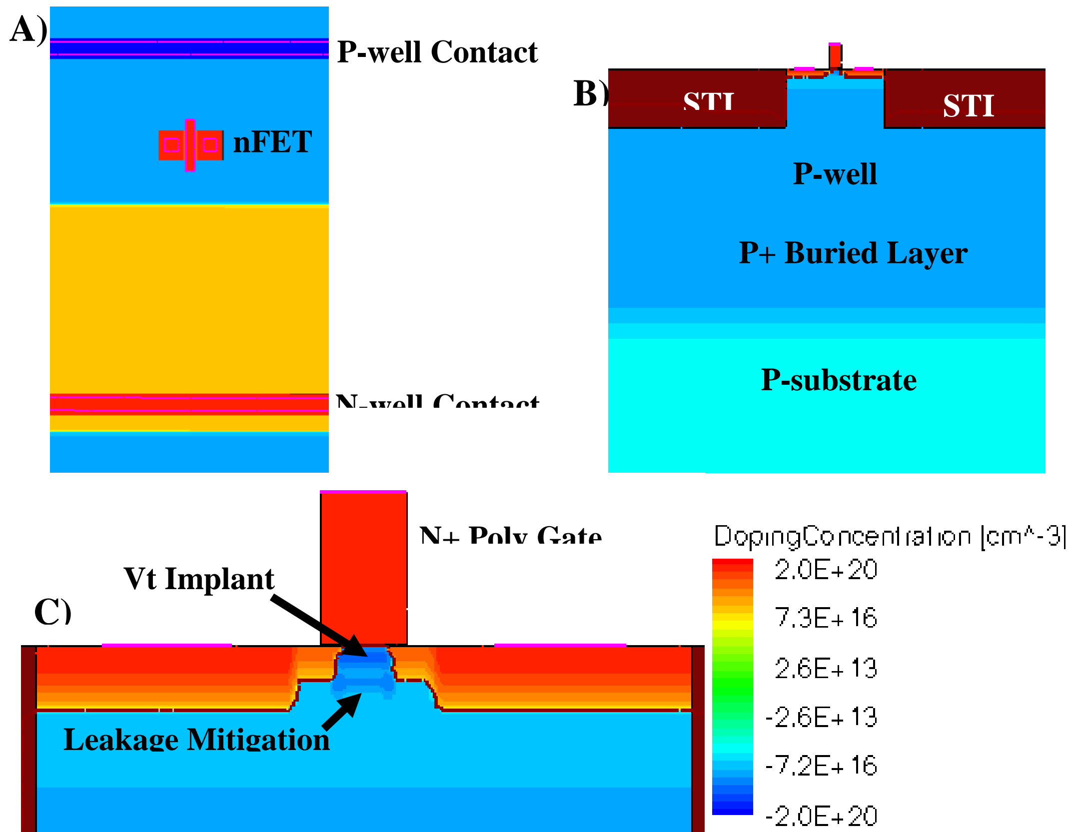

Figure 30. nFET 3D TCAD structure. A) overhead view of nFET and wells. B) Side view of nFET showing the P-well, P+ buried layer, and P-substrate. C) Close-up view of nFET.

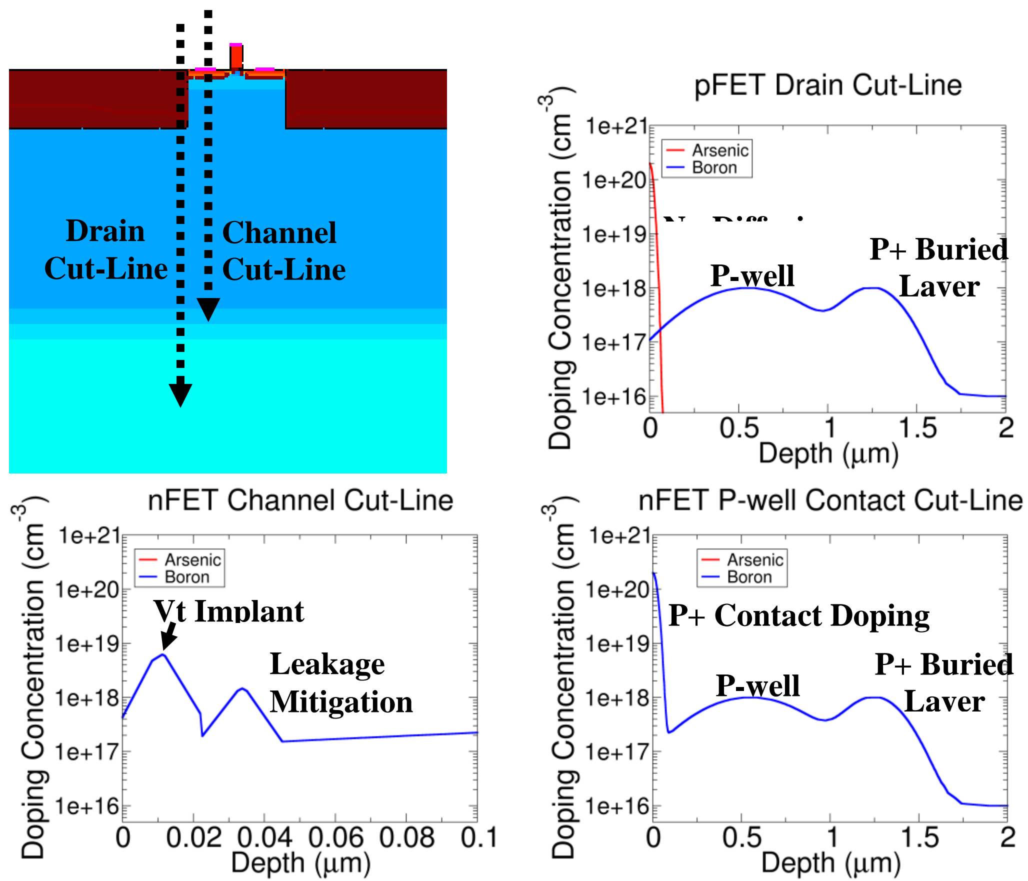

Figure 31. 1D cut-line showing the doping concentration versus depths at various locations of the nFET structure.

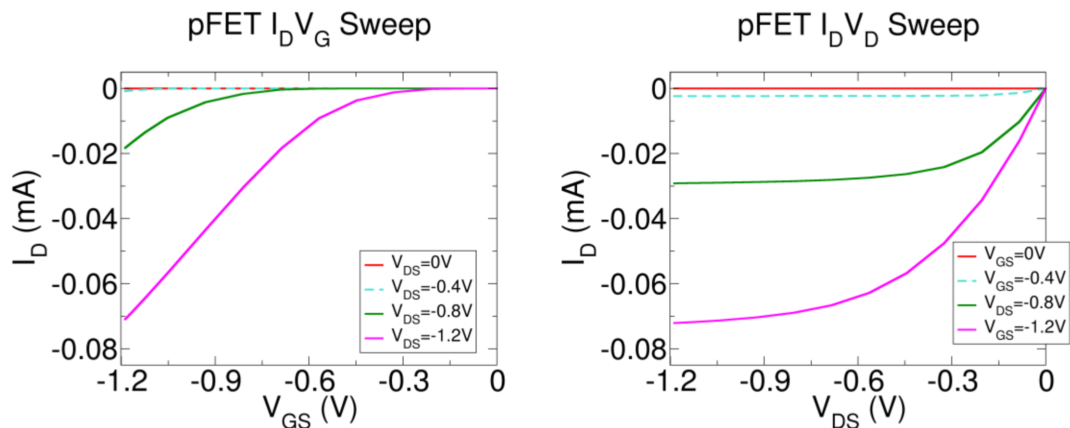

Figure 32. Current versus voltage sweeps for a pFET with L=80nm and W=280nm.

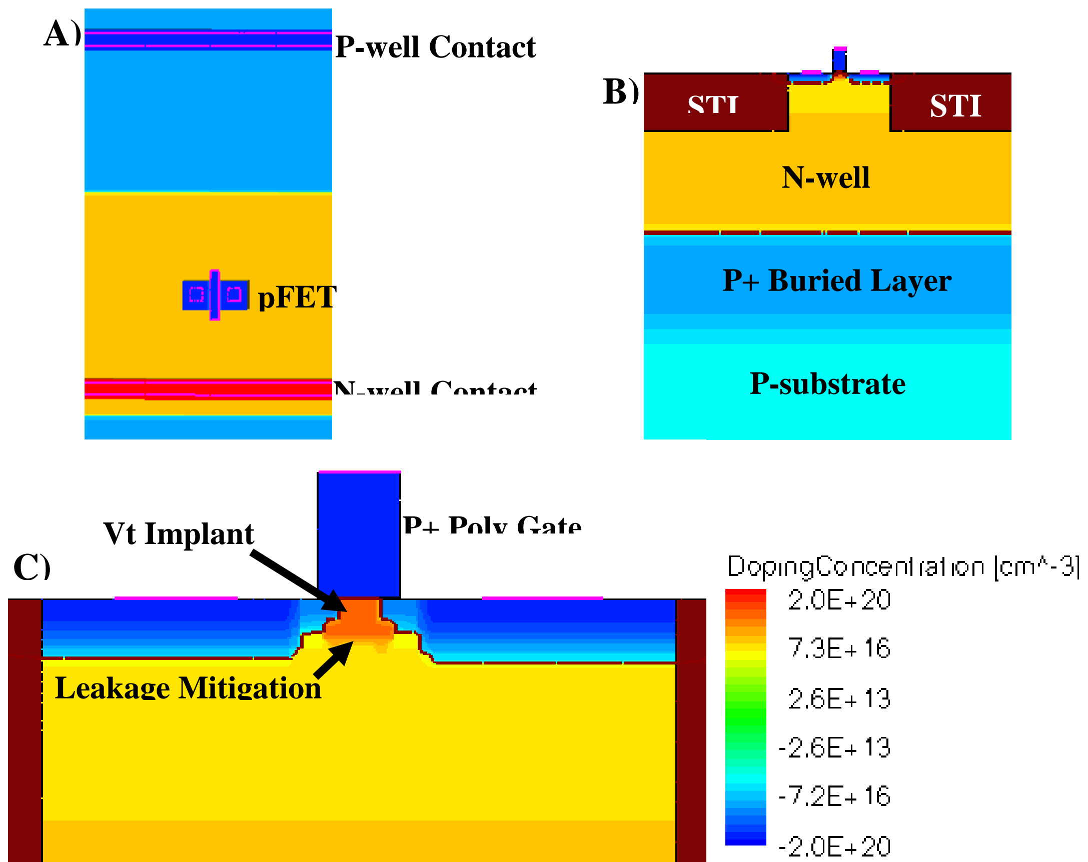

Figure 33. pFET 3D TCAD structure. A) overhead view of pFET and wells. B) Side view of pFET showing the N-well, P+ buried layer, and P-substrate. C) Close-up view of pFET.

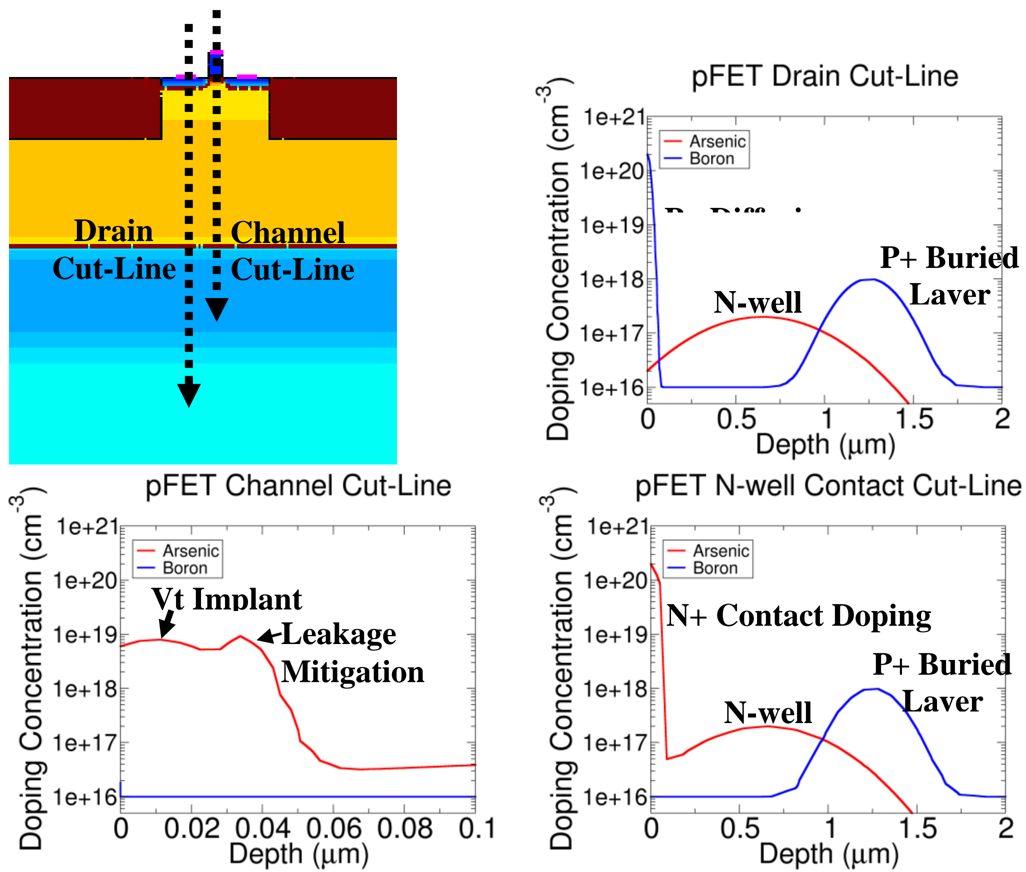

Figure 34. 1D cut-line showing the doping concentration versus depths at various locations of the pFET structure.

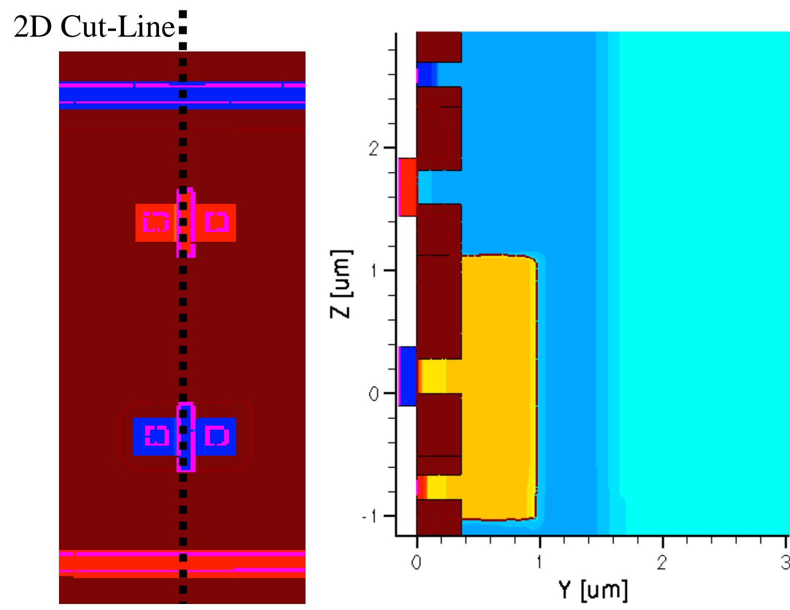

Fig. 1 2D Plot of the side of both nFET and pFET to show well dimensions.

CHAPTER III

COMPARISON OF NORMAL INCIDENCE HEAVY-ION DFF and HARD-FF SEU CROSS SECTIONS AND MECHANISMS

Section 3.1 Overview

In section 1.2, it was shown that different models predict different trends for DFF SEU cross sections as technologies scale. This chapter begins by exploring mechanisms that can change the SEU cross section of DFFs through TCAD simulations by varying common parameters that would change when technologies scale by applying them to the 90-nm TCAD models described in chapter 2. In these simulations, the extent from the vulnerable FET in a latch is analyzed versus changing technology process parameters in the well. Then, DFF and Hard-FF normal incidence heavy-ion experimental results are compared.

The process parameters that vary with process that are analyzed include: maximum transistor drive current, well doping, well depth, well width, well contact spacing, and upset reversal. These are all parameters that can have a major impact on the SET response of a circuit. Also, all these parameters can influence the effects of other parameters on SEU cross sections.

The chapter ends by comparing experimental results for DFF designs to narrow down which mechanisms may be dominating the SEU cross section response for various LET values.

Section 3.2 DFF and Hard-FF TCAD Simulation Setup

The 90-nm 3D TCAD models described in chapter are used for the following simulations. Mixed-mode simulations will be used where 1 or 2 FETs from the latch will be simulated in the physical portion of the simulation, while the remaining FETs in the latch will be simulated in SPICE. Multiple ion strikes with increasing distance from the edge of the drain for the vulnerable FET are simulated to find the greatest extent an ion strike will cause an upset for changes to a given process parameter, shown in Figure 35. Unless otherwise stated, all ion strikes have an LET 58 MeV-cm^2/mg (0.58 pC/μm). The process parameter will be varied in a way to mimic changes that would occur as technology feature sizes become smaller.

For simulations utilizing a single FET in the physical portion of the simulation of the latch, a 3D model is used. When 2 or more FETs are simulated in the physical portion of the simulation, 2D models are used to reduce simulation time and overcome any convergence issues. It is important to note that using the 2D simulations may enhance any charge sharing that may occur in the physical simulation, but will not affect the results as only 2D simulations will be not be compared to 3D simulations.

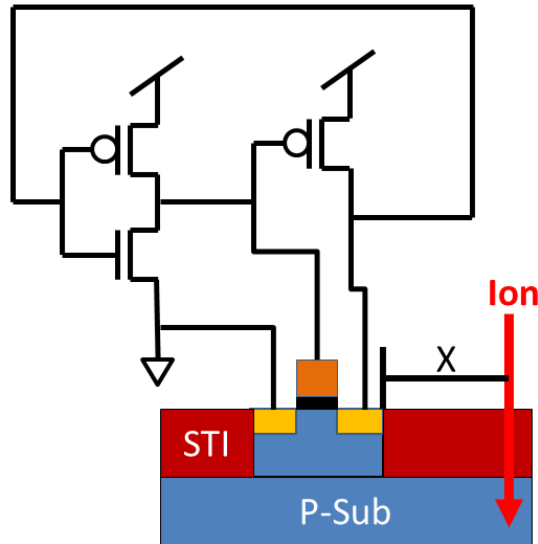

Figure 35. Illustration of the 3D TCAD simulation setup to strike a single nFET in a latch.

Section 3.3 Transistor Drive Current

One goal of technology is to reduce power consumption by decreasing transistor drive currents. By decreasing the transistor drive currents, the amount of charge needed to cause an upset becomes much smaller thus potentially increasing the SEU cross section of a FF [2].

To examine this effect in 3D TCAD simulations, the width of the transistors opposite of the transistor being struck in the physical simulation had the widths shrunk to mimic decreasing transistor current strengths with scaling. If the nFET is in the physical portion of the mixed-mode simulation, the pFETs in the latch that are in the circuit simulation portion had their widths changed, as illustrated in Figure 36. Table 3 shows the parameters that are kept constant in the simulation while the transistor width is changed.

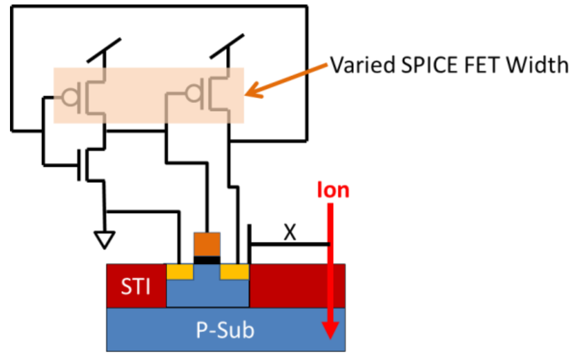

Figure 36. Illustration of a nFET being simulated in the physical portion of the simulation and the pFET widths are varied to emulate decreasing FET drive currents with scaling.

Table 3. Simulations parameters kept constant when changing the transistor width.

Sim Parameters	
P-well doping (cm^{-3})	1E+18
N-well doping (cm^{-3})	5E+17
Well Depth (um)	0.7
STI Depth (um)	0.33
Well Contact	Strip
Buried P+	Yes
$W_P = W_N$	

The simulation results are shown in Figure 37. As expected, as the transistor width decreases (transistor current decreases with scaling) the extent at which an ion strike can cause an SEU in the latch increases. There is a difference in the rate of increase of extent of SEU distance versus FET width is different for nFETs and pFETs. The nFET increase in extent of SEU distance increases linearly with decrease in transistor current, but the pFET increase is almost quadratic. The difference in the nFET and pFET trends is due to the WPM activating the pFET bipolar. As shown in [62], the WPM effect is negligible for strikes in p-wells compared to n-wells. In addition, these results indicate that the voltage at which the well potential must drop to cause an SEU in a latch will change based on the driving current of the restoring transistors connected to the vulnerable FETs. This is important because the WPM will play major role in the SEU cross section response for vulnerable pFETs compared to nFETs as technologies scale for dual well technologies.

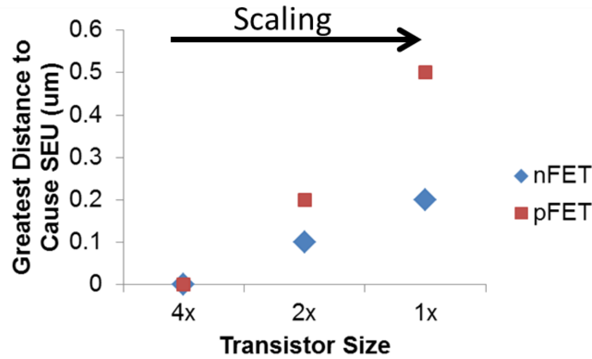

Figure 37. 3D TCAD simulations results showing the greatest extent from the drain an ion strike with a LET of 58 MeV-cm2/mg will cause an SEU in the latch vs. transistor width.

Section 3.4 Well Doping Concentration

Another parameter that changes as technologies scale is well doping concentration which helps reduce latchup and substrate noise issues. The well doping concentration is increased to improve the latchup immunity and substrate noise as technology feature sizes become smaller. As shown in [62] the well doping can be a major parameter determining the WPM response during an SE and decreases with higher well doping concentrations.

The 3D TCAD simulation used to explore this effect focused on changing the peak well doping concentration while forcing the doping concentration at depth to remain the same so transistor and well junction parameters remain unaffected.

Table 4 shows the parameters that were held constant when the peak well doping concentration was varied.

As the well doping concentration increases, the greatest distance from the center of the drain region from which an ion strike can cause an SEU decreases as shown in Figure 38. Strike distance from the drain in the n-well show a much larger decrease with increasing doping than the p-well; this follows the same trend as the decreasing WPM extent seen in [62]. Well doping concentration increases can decrease the SEU cross section of a DFF by decreasing WPM effects in the n-well by decreasing the well resistance to the well contacts.

Table 4. Common simulations parameters while peak well doping concentration was changed.

Sim Paramters	
Well Depth (um)	0.7
STI Depth (um)	0.33
Well Contact	Strip
Buried P+	Yes
$W_P = 2*W_N$	

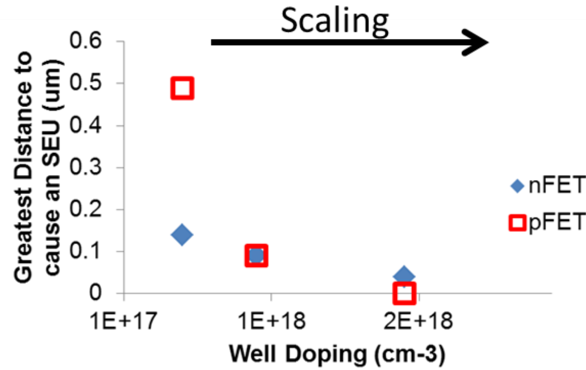

Figure 38. Greatest extent that can cause an SEU in a latch vs. well doping.

Section 3.5 Well Depth

To reduce latchup effects as technology feature sizes become smaller, well depths are decreased to reduce the gain of the n-well/p-well junction [62]. Decreasing the well depth reduces the area of the n-well/p-well junction reducing the current gain of the latchup structure. This will affect the WPM of the well by changing the resistance from ion strikes to well contacts and changing the bipolar response of multiple transistors.

In Figure 39, the nFET shows no change in SEU distance vs. well depth, but there is a change in the pFET distance; this is again due to the pFETs being located in a constrained n-well, unlike the nFETs in the p-well and p-substrate. Table 5 shows the parameters that remained constant while changing the well depth. Thus, as technologies scale, the well depth will decrease causing a wider WPM area in constrained n-wells and potentially increasing the SEU cross section of a DFF.

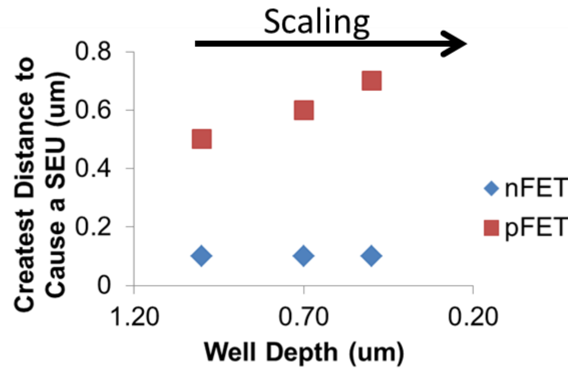

Figure 39. Greatest extent that can cause an SEU in a latch vs. well depth.

Table 5. Common simulations parameters while well depth was changed.

Sim Parameters	
P-well doping (cm^{-3})	1E+18
N-well doping (cm^{-3})	5E+17
STI Depth (um)	0.33
Well Contact	Strip
Buried P+	Yes
$W_P = 2*W_N$	

Section 3.6 Well Width

Ever improving ion implantation methods and reducing transistors sizes allows designers to reduce well sizes as technology feature sizes decrease. Changing the well width impacts the resistance from an ion strike to well contacts and affects the WPM response, which in turn affects the bipolar response of transistors.

In Figure 40, the nFET response to changing the p-well width does not affect the SEU response of the DFF, but the pFET response does show sensitivity to shrinking the well width. Table 6 shows the parameters that remained constant while the well width was changed. Again, decreasing the well conductivity to the well contacts causes an increase in the WPM area and increases the DFF cross section for constrained well structures. As technologies scale, shrinking the well width can cause a DFF SEU cross section to increase.

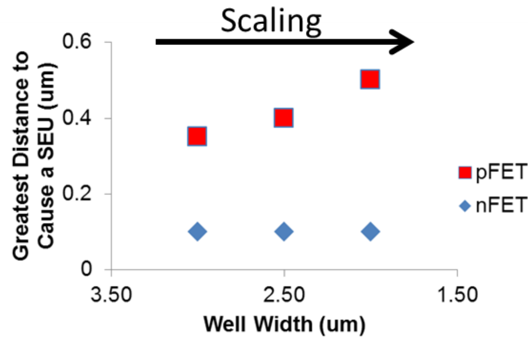

Figure 40. Greatest extent that can cause an SEU in a latch vs. well width.

Table 6. Common simulations parameters while well width was changed.

Sim Parameters	
P-well doping (cm^{-3})	1E+18
N-well doping (cm^{-3})	5E+17
STI Depth (um)	0.33
Well Contact	Strip
Buried P+	Yes
$W_P = 2*W_N$	

Section 3.7 Transistor Spacing from N-well/P-well Boundary

As technologies scale, it is possible for designers to decrease spacing between transistors and the n-well/-well boundary. Decreasing the distance between a transistor from the n-well/p-well boundary can reduce the amount of minority carrier current collected by a transistor [63].

In Figure 41, the pFET shows no change in the extent an SEU with decreasing distance to the n-well and p-well boundary, but the nFET simulations show a small decreasing trend in the extent to cause an SEU with decreasing distance between the n-well/p-well boundary. Table 7. Common simulations parameters while n-well/p-well boundary spacing was changed. Again, the WPM response plays a role in determining the SEU response of pFETs; the distance of a pFET will not have a significant change to the WPM response of an ion strike near the pFET and will collect the same amount of charge because the WPM response is not changed because the resistance to the well contacts remains the same. As technologies scale, the distance between nFETs and the n-well/p-well boundary will decrease and lead to small decreases in the SEU cross section of DFFs.

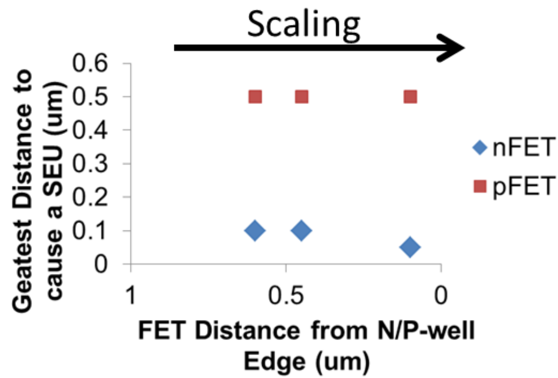

Figure 41. Greatest extent that can cause an SEU in a latch vs. spacing to n-well/p-well boundary.

Table 7. Common simulations parameters while n-well/p-well boundary spacing was changed.

Sim Parameters	
P-well doping (cm^{-3})	1E+18
N-well doping (cm^{-3})	5E+17
STI Depth (um)	0.33
Well Contact	Strip
Buried P+	Yes
$W_P = 2*W_N$	

Section 3.8 Well Contact Spacing

As technologies feature sizes decrease, spacing between well contacts can increase (or maximum distance from a well contact to a transistor can increase). This allows for higher transistor densities. To mitigate latchup issues, designers can chose to increase well contact density [62]. Changes to well contact spacing have a major impact on the WPM of a constrained well due to an ion strike.

In Figure 42, the nFET SEU response shows no sensitivity to the well contact spacing, but the pFET response shows a major change in the SEU response due to WPM. The nFETs are not affected by WPM because of the p-well being connected to the p-substrate, but the n-well in constrained and changing the well contact spacing can easily change the resistance to an ion strike from the well contcts affecting the restoring current to and WPM response. As technologies scale, the well contact spacing can increase causing the well resistivity from ion strike location to increase and potentially increase a DFF SEU cross section.

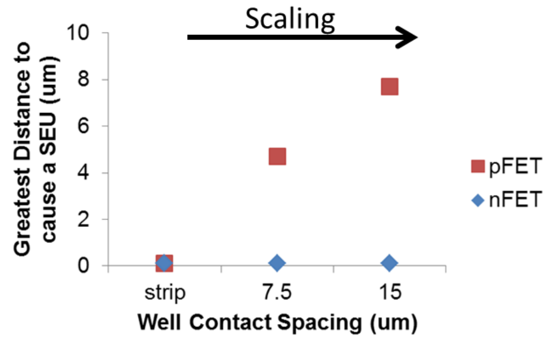

Figure 42. Greatest extent that can cause an SEU in a latch vs. spacing between contacts.

Table 8. Common simulations parameters while spacing between well contacts was changed.

P-well doping (cm^{-3})	1E+18
N-well doping (cm^{-3})	5E+17
Well Depth (um)	0.7
STI Depth (um)	0.33
Buried P+	Yes
$W_P = 2*W_N$	

Section 3.9 Normal Incidence Heavy-Ion Experimental Results of Flip-Flops in 40-nm, 28-nm, and 20-nm

To compare the effects of technology on a scaled flip-flop design, experiments were conducted on the 40-nm, 28-nm, and 20-nm test chips. Tests were conducted at nominal supply voltages (0.9 V for 40-nm, 0.85 V for 28-nm, and 0.9 V for 20-nm) at a clock frequency of 10 MHz and a constant data input stream of either all ones or all zeroes. The same relative transistor placement was used in all three test chips, but the design is shrunk with respect to technology parameters, for example transistor pitch, gate length, and transistor width are decreased. The schematic of the standard latch used in all three test chips to make a master-slave flip-flop is shown in Figure 43.

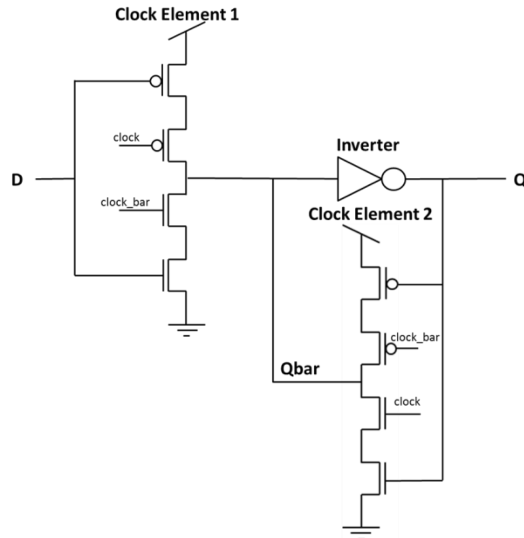

Figure 43. Schematic of the latch used to create the master/slave flip-flop on the three test chips.

Alpha experiments were conducted at Vanderbilt University using a 10 µCi 241Am source. The experiments were conducted in air at a distance of 5 mm from the top of the IC die surface. The chip was tested to a fluence of 3.8×10^9 alphas/cm^2 resulting in ~10,000 errors for each design. The alpha SEU cross section versus technology node is shown in Figure 44. A survey of various flip-flops designs shows a similar decreasing SEU cross section trend shown in Figure 45. The SEU cross section for this design is shown to decrease with scaling and decreases by an amount similar to the off-state drain area.

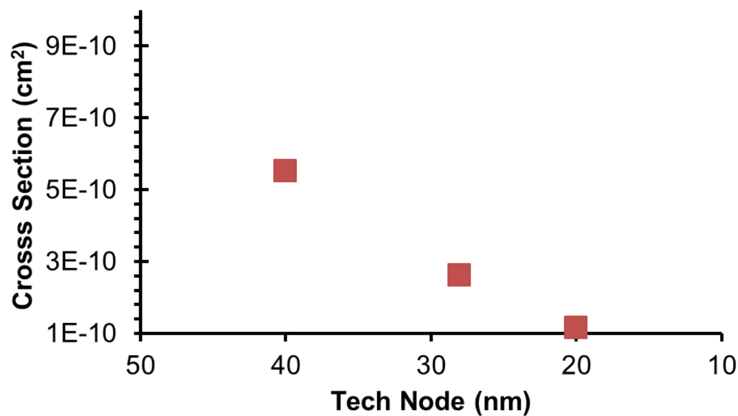

Figure 44. Alpha SEU cross section per FF vs. technology feature size for a DFF.

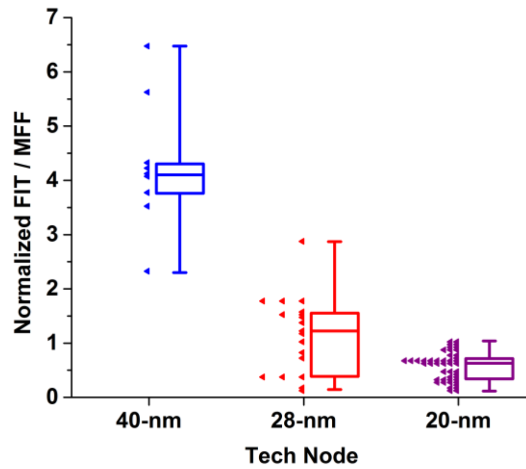

Figure 45. Normalized Alpha SEU cross sections of various flip-flops across three technologies.

Higher LET particle experiments were conducted at the Lawrence Berkeley National Laboratory (LBNL) at normal incidence in vacuum with the 10 MeV/u ion cocktail. The ions used with their associated LET values are shown in Table 9. Each ion species was tested to a fluence of $5x10^7$ ions/cm^2. The results in Figure 45 show the SEU cross section for DFF in the three technologies decreases across the LET spectrum.

Table 9. Ion Species and LET Values TEsted at LBNL

Ion	LET (MeV-cm^2/mg)
Br	0.9
O	2.2
Ne	3.5
Ar	9.7
V	14.6
Kr	30.2
Xe	58.8

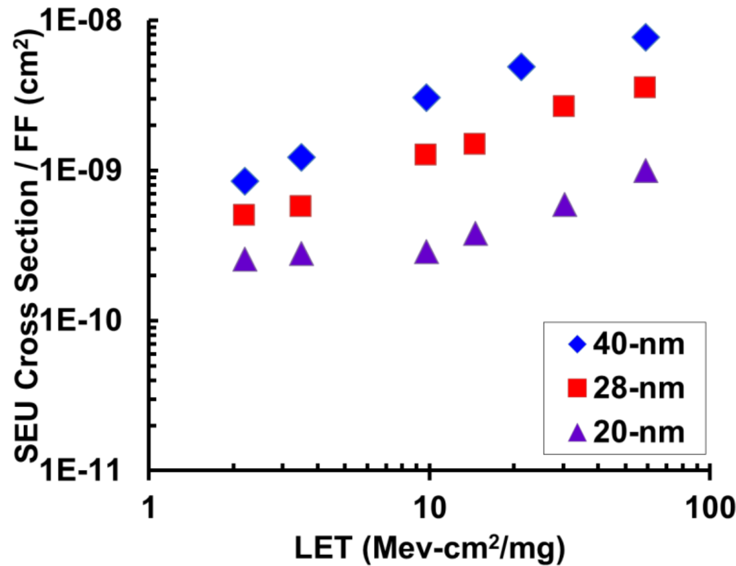

Figure 46. Heavy-ion SEU cross section vs. LET for the DFF.

Section 3.10 Summary of DFF Heavy-Ion Experiments vs. Simulations

The heavy-ion simulations show that many factors compete to decrease or increase the SEU cross section. Many parameters can influence the SEU cross section of a flip-flop as technologies scale and is dependent on how the parameters change with relation to each other. Experimental results for one commercial process from 40-nm, 28-nm, and 20-nm show the SEU cross section for the presented DFF decreases as feature size becomes smaller. This indicates for this commercial specific commercial process the technology scaling parameters that can decrease SEU cross sections can dominate resulting in an overall decrease in SEU cross section.

Section 3.11 Simulation of Hard-FF Normal Incidence Heavy-Ion SEU Cross Sections

To analyze charge sharing effects in hard-FFs vs. transistor drive current, 2D TCAD simulations were used to save simulation time. First, nFETs connected to X0 and X2 sensitive node pairs were placed 240 nm apart as illustrated in Figure 47. Ion strikes were simulated in 50 nm steps from source to source on both nFETs. These simulations showed no SEUs in the hard-FF due to charge sharing among the nFET sensitive pair for the 90-nm technology. To further check this result, the minimum pFET width was varied to mimic the current drive of the 65-nm and 45nm to see if sensitivity changed and still no SEUs were observed. Remember that 2D TCAD simulations show increase charge

sharing effects because charge cannot dissipate in the 3rd dimension. These results show that TCAD simulations nFETs in a hard-FF even at minimum node spacing may show no vulnerability to SEUs as technologies become decrease.

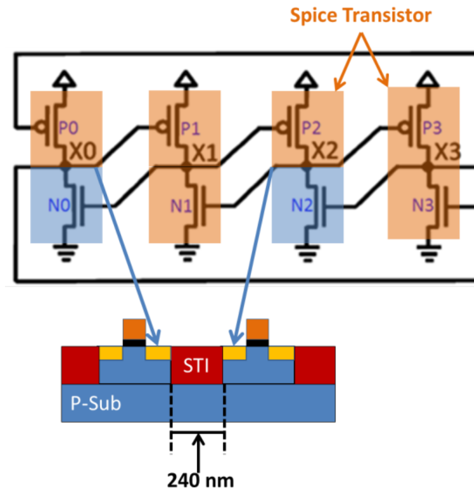

Figure 47. Illustration of 2D TCAD setup for a hard-FF. The X0 and X2 nFETs and implemented in the 2D model and the other transistors are implemented in spice.

Section 3.12 Traditional Hard-FF Normal Incidence Heavy-Ion SEU Cross Sections

Various heavy-ion results for different technologies are shown in Figure 47. The 90-nm and 130-nm results are from [46] and the 180-nm results are from [44]. The 40-nm, 28-nm, and 20-nm results were collected at the LBNL heavy-ion facility at normal incidence in air at a frequency of 10 MHz. The 10 MHz locking frequency reduces the chance of a SET being latched in the DICE circuit thus only showing SEUs due to charge sharing at two sensitive node pairs. The legend in Figure 48 shows the technology feature size on the left and the node spacing on the right, for example the 28-nm technology has a minimum sensitive node pair spacing of 700-nm. The results in Figure 48 show SEU cross section for these hard-FF design remains within an order of magnitude of each other across the LET range. This indicates that as technology scales, the SEU cross section of the hard-FF designs remains similar due to charge sharing physical mechanisms remaining similar. The 28-nm does show a SEU cross section at a LET of ~2 MeV-cm^2/mg while the other technologies do not; this is only one error at the LET ~2 MeV-cm^2/mg and zero errors at an LET of ~3 MeV-cm^2/mg indicating that the single upset is due to a randomly captured transient. Even down to the 28-nm technology node, hard-FFs show to be effective at reducing the SEU cross section for sensitive node pair

spacing of ~1 μm for LETs below 9 MeV-cm²/mg. For LET values above 9 MeV-cm²/mg, the SEU cross section does not increase and technology feature size decreases for normal incidence particles.

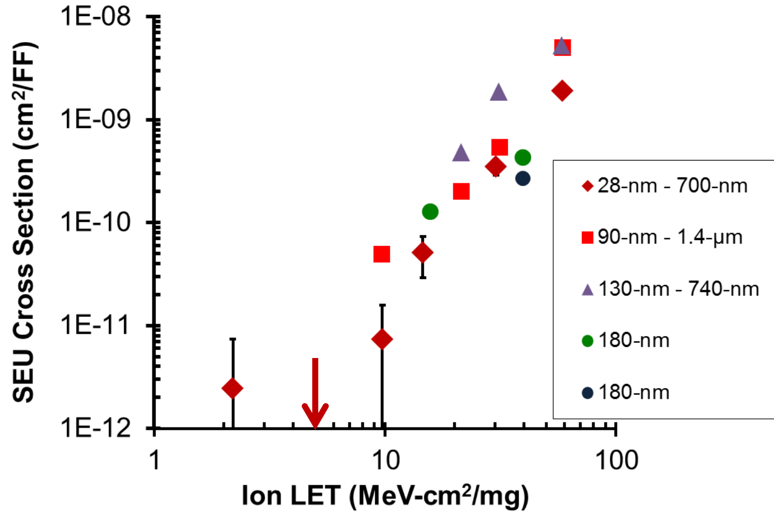

Figure 48. SEU Cross section vs. LET for hard-FF designs. The technology feature size is given on the left in the legend and the node spacing is given on the right.

Section 3.13 Comparison of Normal Incidence Heavy-Ion DFF and Traditional Hard-FF Results

For any technology node, a hard-FF design must provide sufficient SEU cross-section reduction compared to a DFF design to justify the performance penalties of using hard-FF designs. The ratio of hard-FF SEU cross section to DFF upset cross section for each technology node is plotted versus LET in Figure 49 to show the differences in their performance across technology nodes and LET range. For low LET particles (LET of less than 10 MeV-cm²/mg), redundant-FF upset cross section shows improvement of over 100X when compared to DFF cross section across the presented technologies. Above 10 MeV-cm²/mg, the decreasing DFF cross sections with technology begin to reduce the improvement gained by the hard-FF designs.

It is clear from above observations that sensitive-node spacing strongly affects the slope of the cross-section curve as a function of particle LET. Effects of sensitive-node spacing are more pronounced than those of scaling. With similar sensitive-node spacing, redundant-FF designs across all technologies show similar SEU cross-sections as a function of particle LET. DFF designs, on the other hand, show a very strong dependence of SEU cross-section on scaling and particle LET. These two different trends in different

operating environments must be evaluated carefully by designers to optimize SEU performance of a given design. Increased sensitive-node spacing provides the greatest benefits in hard-FF SEU cross sections at LET values below 10 MeV-cm^2/mg as technologies scale below 28-nm.

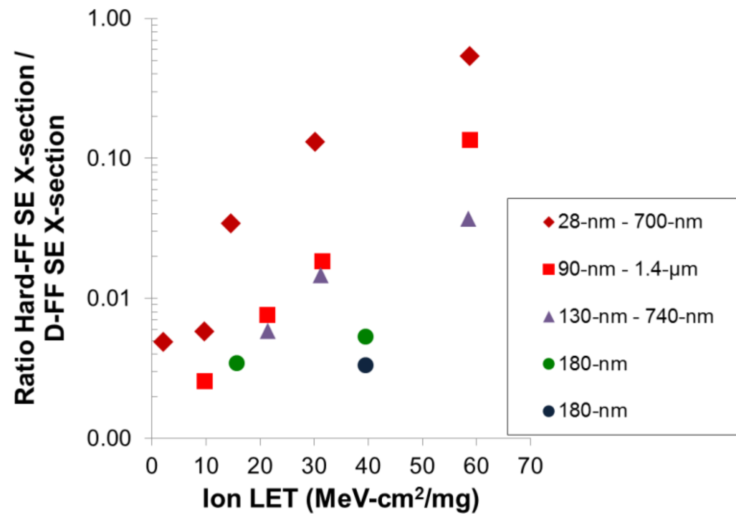

Figure 49. Ratio of hard-FF SEU cross section to DFF SEU cross section for each technology node vs. LET.

Section 3.14 Summary

The trend in SEU cross-section for a set of redundant-FF designs and DFF designs across multiple technology nodes is quantified through experimental results. DFF designs show a strong dependence of SEU cross-section on minimum feature size and particle LET. Redundant-FF design SEU cross-sections show a very strong dependence on sensitive-node distance due to the dominance of charge sharing mechanisms. Redundant-FF cross sections in this work show a weak dependence on scaling and particle LET > 20 MeV-cm^2/mg if the redundant node spacing is kept constant. The ratio of SEU cross section of redundant-FFs compared to DFFs decreases when technologies scale at high LET values; one factor that contributes to this trend is the DFF cross section approaches the redundant-FF cross section with decreasing feature size. In 28-nm technologies, if particles with LET values greater than 30 MeV-cm^2/mg are of concern, designers may need to find alternative schemes for significantly improving FF reliability versus performance penalties, such as applying LEAP principles to the layout or increasing the sensitive-node spacing greater than 1 μm.

CHAPTER IV

COMPARISON OF ANGLED INCIDENCE HEAVY-ION DFF AND HARD-FF SEU CROSS SECTIONS

Section 4.1 Overview

Chapter 3 showed that DFF SEU cross sections approach hard-FF SEU cross sections as technologies scale at normal incidence. As the angle of an incidence ion increases, the probability of charge collection at multiple nodes increases, which is not fully captured by normal incidence strikes. This chapter compares angled incident heavy-ion experimental results for 130-nm, 90-nm, 28-nm for both DFF and hard-FFs.

The 28-nm DFF and hard-FFs were implemented in a circuit for radiation effects self test (CREST) design [64] and fabricated in a commercial 28 nm bulk CMOS process. The designs are tested at a clock frequency of 10 MHz at nominal supply voltages and at room temperature. The 10 MHz clock frequency is chosen to lower the probability of SETs affecting the SEU cross section seen at higher frequencies. A constant input of one or zero was supplied to the CREST input; the constant data input avoids SETs generated in the clock tree from generating SEUs. The data is shifted out of the data counter serially, logged by an FPGA, and recorded on a laptop. The 28-nm DFF is a standard cross-coupled inverter design. The 28-nm hard-FF has 1-µm spacing between the sensitive storage node pairs.

Experimental measurements were taken at Lawrence Berkley National Laboratory (LBNL) using the 10 MeV ion cocktail in vacuum for the 28-nm designs. The ions used in the experiments were O, Ne, Ar, Cu, and Xe with LET values of 2.19, 3.49, 9.74, 21.17, and 58.78 MeV-cm2/mg, respectively. Angles of incidence include normal and 60° along the direction of the wells (parallel to power rails).

The 130-nm and 90-nm DFF and hard-FF experimental results were obtained from work done by Amusan et al. [5]. The hard-FF have 0.74-µm and 1.4 -µm sensitive storage node pairs for the 130-nm and 90-nm processes, respectively. Experimental data was collected in a similar manner as the 28-nm at normal incidence and 60° along the wells.

Section 4.2 Angled DFF Heavy Ion Experimental Results

Figure 50 shows the DFF experimental SE cross sections at normal and 60° for 130-nm, 90-nm, and 28-nm. Error bars for 28-nm results are smaller than the symbols. As expected, the nearly saturated cross section decreases with scaling. The nearly saturated cross section for incident angles of 0° and 60° across the particle LET range only changes by a factor of 2. This small increase for 60° incidence over normal incidence indicates the strong influence charge sharing has for preventing upsets in the DFF. These results clearly demonstrate that the increased angle of incidence does not necessarily result in a large increase in cross section for DFFs. As explained earlier, this is mainly caused by increased charge sharing strengthening the upset-reversal (or RCC) mechanism.

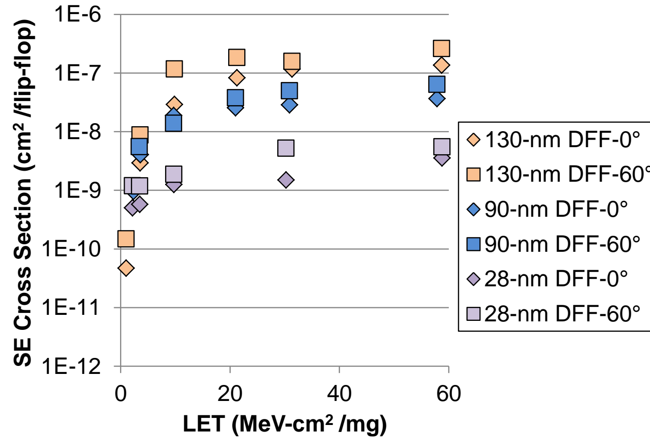

Figure 50. DFF SE cross section vs. LET for normal incidence and 60°. Error bars for 28-nm results with 95% confidence intervals smaller than symbols.

Section 4.3 Angled Hard-FF Heavy Ion Experimental Results

Figure 51 shows the SE cross sections of the hard-FF designs vs. LET at normal incidence and 60° incidence. Unlike DFF designs, the effects of scaling do not show a clear trend. The high LET cross section for all three technology nodes shows a much smaller difference than for DFF designs. This indicates that technology scaling has less of an effect on the SEU cross section of hard-FFs than DFFs, even for angled ion strikes. For all the hardened designs, it is seen that the SEU cross section for incident angles of 0° and 60° across the particle LET range increases by a factor greater than 2X. This indicates that charge sharing increases the hard-FF cross section at a faster rate than compared to DFF cross sections (where charge sharing actually helps to reduce cross section) as angle of incidence in increased. Also, the saturated cross section for DFF

reduces by more than order of magnitude between 130-nm and 28-nm nodes, but the same for hardened flip-flop design does not show any significant reduction.

It is important to note that the distance between sensitive storage nodes for 130-nm and 28-nm node hardened flip-flop designs was 0.74 µm and 1 µm, respectively, whereas the node spacing was 1.4 µm for the 90-nm design. These results clearly indicate that the dominating factor for hard-FF designs across technology nodes is the node spacing and not the changing process parameters.

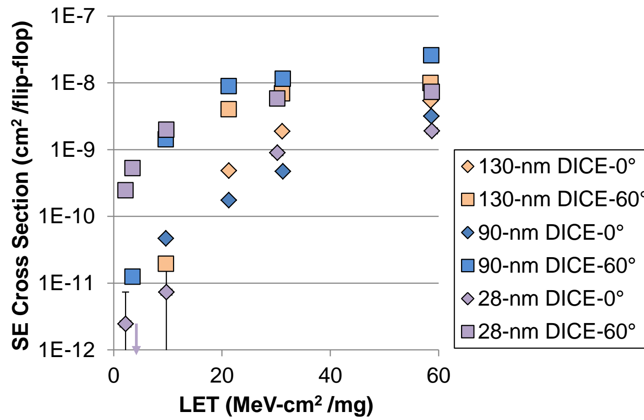

Figure 51. Hardened flip-flop SE cross section vs. LET for normal incidence and 60°. Error bars for 28-nm results with 95% confidence intervals shown.

Section 4.4 Comparison of DFF and Hard-FF Angled SEU Cross Sections

Designers are concerned with the amount of improvement in SEU cross section gained by using a hardened flip-flop compared to a DFF to justify performance and area penalties. To make this comparison, Figure 52 plots the ratio of the hard-FF cross section to DFF cross section across the LET range for each technology node. It is seen that the effectiveness of hard-FFs diminishes with technology scaling. This is due to the fact that DFF cross sections decrease with scaling, while hardened flip-flop cross sections remain similar across technology nodes (as seen in Figure 52). This shows care must be taken when moving to a smaller technology node because a hardened design may not yield the same improvement over the DFF design across technology generations.

The ratio of hardened flip-flop cross section to DFF cross section for 60° incidence compared with 0° incidence shows a large increase in cross section for all technology nodes. These data show that with scaling, this ratio is getting closer to one. In fact, for the 28-nm technology node, cross section for hard-FF is greater than that for DFF at 60° incidence for LET values above 10 MeV-cm^2/mg. This behavior has not been

seen previously for any other technology node. The combined effect of decreasing DFF cross section with scaling and sensitivity to angular strikes for hard-FF designs results in the reversal of what is generally observed. For heavy-ion environments, these findings are particularly troublesome since effectiveness of hard-FF approaches is not guaranteed in some space envirnemnts. It must be noted at this point that this ratio (DFF cross section to hard-FF cross section) is a strong function of layout.

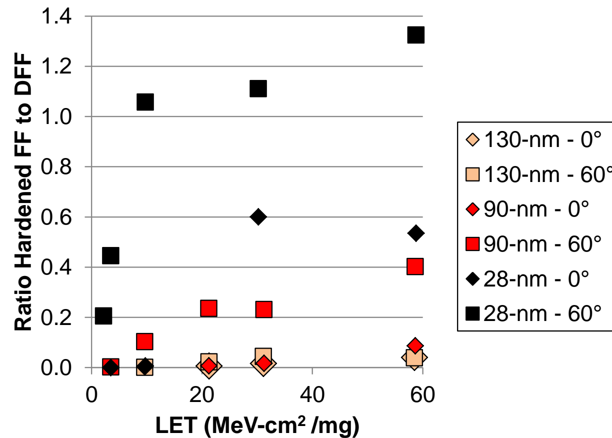

Figure 52. Ratio of hardened flip-flop (FF) cross section to DFF cross section vs. LET at normal incidence and 60°.

Section 4.5 Summary

The SEU sensitivity of unhardened and hard-FF cross sections for ion strikes incident at angles is studied for technologies ranging from 130-nm to 28-nm. Across the technologies investigated, the DFF cross section increased by ~2X when ion strikes angles are at 60° incidence compared to normal incidence across the LET range. The hard-FF cross section may increase as much as 200X across the same LET range as feature sizes decrease. At the 28-nm technology node, the hard-FF cross section becomes greater than the DFF cross section for LET values above 10 MeV-cm^2/mg for ions incident at 60°. This shows ions incident at angles will be a major reliability concern below 28-nm in a heavy-ion environment. These results show the importance of characterizing the SEU response of both hardened and unhardened flip-flops to ions incident at various angles at a given technology node to evaluate the effectiveness of hardening approaches.

CHAPTER V

NEUTRON AND HIGH ENERGY PROTON DFF and HARD-FF CROSS SECTIONS

Section 5.1 Overview

Soft-error rates due to neutrons are expected to dominate the FIT rates for integrated circuits (IC) fabricated at advanced technology nodes in the terrestrial environment. Chapters 3 and 4 focused on the effects of heavy ion particles on SEU cross sections in various flip-flops. Another reliability concern is from secondary particles produced by neutrons and high energy protons. Secondary particles can be emitted at angles leading to increases in SEU cross sections in flip-flops. This chapter focuses on using SRAM MCU cluster size data to help predict hard-FF SER for high energy protons and terrestrial neutrons.

Section 5.2 Background

Neutron collisions with atoms result in secondary ionizing particles that traverse the semiconductor material and deposit charges in their wake. One example of this is when a high-energy neutron interacts with the silicon nucleus and produces a magnesium ion [65]. In general, secondary particles can be ejected at any angle, can have LET values as high as 16 MeV-cm^2/mg (0.16 pC/μm), and travel 100's of microns in silicon [66]. These three factors make it difficult for designers to determine the amount of charge that may be deposited in a given region. Depending on the size of the deposition region and the amount of charge deposited, these charges may be collected by multiple transistors resulting in multi-cell upsets (MCU) in SRAMs or upsets in hardened FF designs.

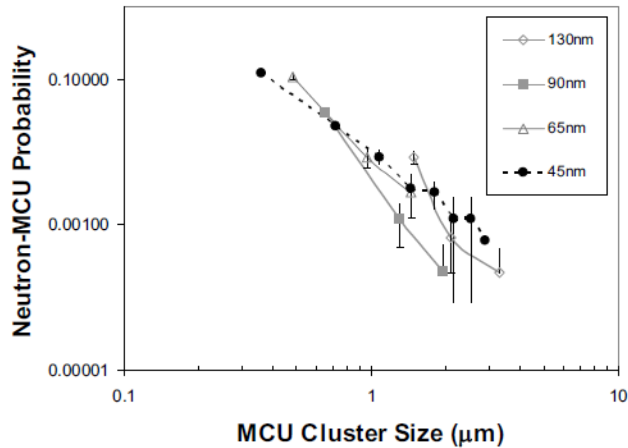

Figure 53. SRAM neutron MCU probability (ration of MCUs to single-cell upsets) versus cell cluster size along the bit line for various bulk CMOS technology nodes [40]

SRAM MCUs occur when a neutron secondary ionizing particle (or particles) deposit charge in the collection regions of vulnerable transistors across multiple SRAM cells. Knowing the SRAM structure/layout, it is possible to determine the distance within which a neutron secondary particle causes SEUs in multiple SRAM cells. Figure 53 shows the SRAM MCU probability versus cluster size for four different technology nodes [40]. The cluster size is calculated by measuring the distance of the outer-most SRAMs upset during a given time and area. The neutron-MCU probability is the ratio of number of MCU occurances, with a given cluster size, along the bit-line (parallel to the n-well/p-well) versus single bit upsets (SBU). This neutron-MCU probability versus cluster size curve can be interpreted as the probability that a neutron interaction will upset SRAM cells within a given distance. Results are similar for all these technology nodes because the underlying silicon lattice structure is identical, resulting in similar physical extent of charge deposition in the collection regions of SRAM sensitive transistors. Also, the critical charge (Qcrit) of the 90-nm and 65-nm SRAM cells has been calculated to be approximately equal (~1 fC), resulting in similar SRAM SER [67], [68]. Using neutron-MCU vs. cluster data, it is possible to probabilistically model the complex charge deposition caused by neutron secondary particles in collection regions of transistors as a function of distance from the neutron strike location.

The hardened flip-flop designs considered in this work employ redundant storage nodes in the design. These flip-flop designs consist of four or more data storage nodes in

each latch, unlike a D-latch that has only two storage nodes [47], [51], [54], [55]. To upset a redundant storage node flip-flop, charge must be collected on two or more nodes (referred to as sensitive node pairs). Proper placement of storage nodes in the layout is an important parameter to consider ensuring that SER robustness of a hardened flip-flop is maintained. The farther the storage nodes can be placed apart, the more robust the hardened flip-flop will be to SEUs.

Another factor to consider in SER reliability of a hardened flip-flop design is the amount of charge that needs to be collected at multiple storage nodes to cause an upset. Figure 54 shows the minimum charge that must collected on two storage nodes of a DICE design to cause an upset at various technology nodes [48]; if the collected charge at both nodes falls in the upper-right region above the curve an upset will occur. The plot shows that the minimum amount of dual node charge needed to cause an SEU decreases with technology. Also, it is seen that the amount of dual node charge to cause an upset in a hardened flip-flop is comparable to the critical charge of SRAM cells (~1 fC in 90-nm) in that technology.

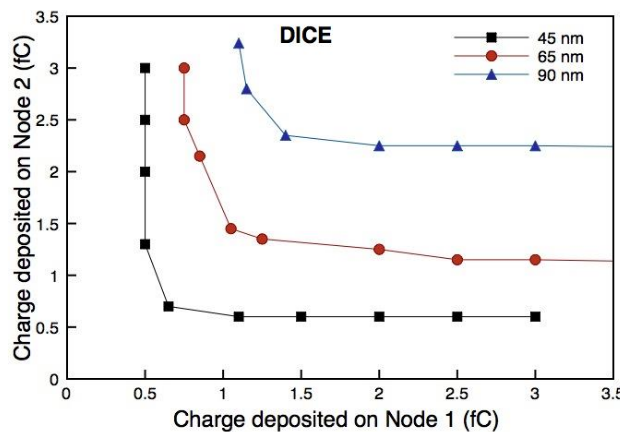

Figure 54. SMHOO plot showing minimum charge collected at two storage nodes in a DICE flip-flop to cause as upset for various technologies [48].

Section 5.3 Experimental Setup

The 40-nm and 28-nm hardened flip-flop designs were implemented in TSMC bulk processes. The flip-flops were configured in a circuit for radiation effects self test (CREST) design as 8 kb shift registers. The 40-nm experiment had seven integrated circuits (IC) tested simultaneously in the neutron beam, while 15 ICs were simultaneously tested for 28-nm technology. During the test, a field programmable gate

array (FPGA) polled each IC for data every minute and transmitted the error counts to a laptop. The designs are tested at a clock frequency of 10 MHz with a continuous data stream of 1 or 0 at nominal supply voltages. Neutron experimental data from various hardened flip-flops from cited works are compared in this paper: the 65-nm Soft error immune latch (SEILA) flip-flop [55], 65-nm Bistable Cross-coupled Dual-Modular Redundancy (BCDMR) flip-flop [54], 65-nm Quatro flip-flop [51], and 32-nm SEUT flip-flop [47].The experiments in the cited works are conducted in a similar fashion to the 28-nm and 40-nm tests.

Section 5.4 Hardened Flip-Flop and SRAM MCU Experimental Data

Figure 55 shows the SRAM and hardened FF vulnerability data for various technology nodes. For this figure, 45-nm SRAM MCU data from [seifert 2008] is combined with 28- and 40-nm DICE-based FF experimental results and various hardened designs in 32-nm ([seifert 2010]) and 65-nm ([Yamamoto 2011], [Rennie 2011], [Uemura 2011]) technology nodes from literature. The 28- and 40-nm design node distances were the smallest minimum sensitive-node-pair distances calculated from the layouts; the two 28- and 40-nm designs have been reported previously in [Lilja 2013], [Loveless 2011]. For the 32- and 65-nm designs, distances between sensitive nodes were reported in the corresponding works. All the hardened FF designs in Figure 55 are redundant storage node designs similar to DICE. The Y-axis values on the graph shows the ratio of hardened FF SER to D flip-flop (DFF) SER of the same technology process allowing designers to quickly view the overall improvement in SER.

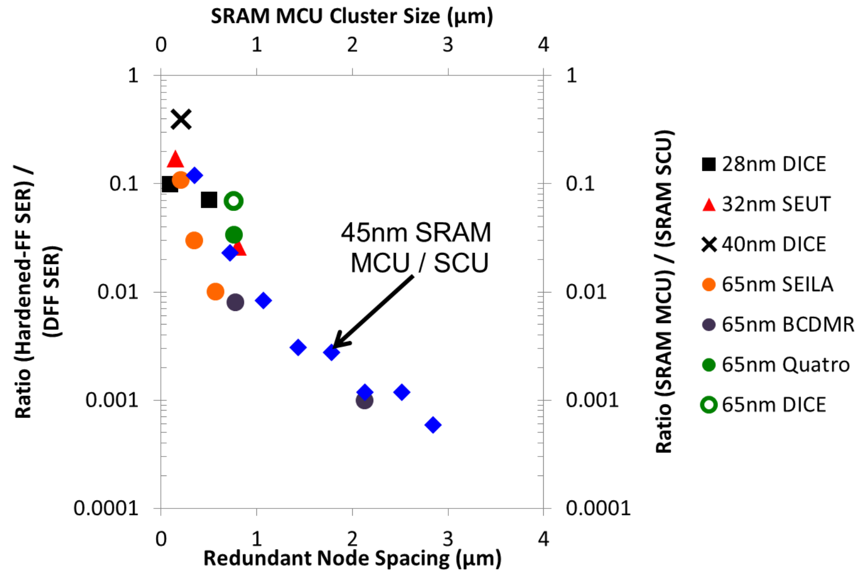

Figure 55. Ratio of hardened FF neutron SER to DFF SER neutron data from various designs overlaid onto 45-nm SRAM neutron MCU cluster size data.

The hardened flip-flop SER data is overlaid onto the 45-nm SRAM MCU cluster data from Figure 53in Figure 55. The hardened flip-flop neutron SER values show a similar trend to the 45-nm SRAM MCU cluster data with worst case deviation being less than a factor of 10. The correlation between the hardened flip-flop SER and SRAM MCU cluster size is hypothesized to be due to similarities in neutron charge deposition, multiple node charge collection, and the Qcrit for the circuits. Evidence of these factors influencing this correlation can also be seen in the SRAM MCU cluster size probability being similar across technology nodes in Figure 53. Comparing the hardened flip-flop SER to the 45-nm SRAM MCU cluster, the 45-nm SRAM MCU cluster data can provide a baseline with which to compare the hardened flip-flops and predict the SEU robustness of a design, even across technology node.

From Figure 55, it is seen that for technologies from 65-nm and below, the neutron SER of the hardened FF designs is dominated by the sensitive node spacing. This indicates the hardened flip-flop storage node spacing in the layout is an important parameter a designer must consider during SER optimization, even as technologies scale. Due to the exponential decrease in the neutron SER of the hardened flip-flops compared to node spacing, the minimum spaced sensitive nodes of the design will dominate the SER as compared to other storage nodes with larger node distances. The greatest reductions in SER are seen when sensitive node spacing is increased from minimum

transistor distance to 1 µm, resulting in a two order of magnitude improvement in SER. Minimum spacing may coincide with redundant storage nodes sharing the same drawn active area (shown in Figure 56), which is absolutely the worst case FF design for soft error reliability. The designs where storage nodes share drawn active areas are the 40-nm design with 200-nm redundant node spacing, one of the 28-nm designs has 100-nm node spacing, and one of the 65-nm SEILA designs has 320-nm node spacing; these designs are optimize for area and metal routing. Based on the 45-nm SRAM MCU data and BCDMR data points (Figure 55), we see little over one order of magnitude decrease in neutron SER when node spacing increases from 1 to 3 µm. Though data is not available for distance greater than 3 µm, the 45-nm SRAM MCU data as a hardened FF baseline suggests that potential reductions in the neutron SER will be smaller for any further increases in redundant node spacing.

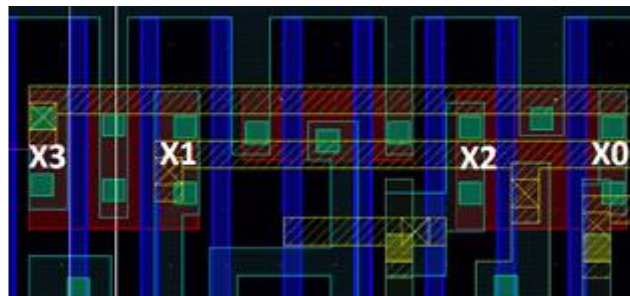

Figure 56. 28-nm layout of pFETs and corresponding storage nodes. Red is active and vertical dark blue is poly.

Using the 45-nm SRAM MCU data from [40], it may be possible to estimate the neutron SER of a hardened design within an order of magnitude by modeling the redundant storage nodes as SRAM cells. The designer needs to find the minimum redundant storage node spacing from the hardened flip-flop layout. With the minimum storage node spacing, the designer can use the SRAM MCU cluster data to estimate the fraction of the neutron events that upset the DICE vs. DFF and decide if hardened FF will meet design requirements. An example of this shown in Figure 57 plotting interconnect capacitance (calculated using [69]).on the left Y-axis, interconnect routing length between storage nodes on the right Y-axis versus the 45-nm SRAM MCU cluster data that is used as a baseline for reduction in hardened flip-flop neutron upsets vs. DFF. Figure 57 shows that the interconnect capacitance increases as the baseline neutron events for hardened flip-flop vs. DFF decreases, but to achieve a value below 0.01 for the hardened flip-flop vs. DFF ratio the interconnect capacitance increases almost

exponentially and would result is unacceptable speed and power penalties. This approach allows a designer to optimize the neutron upset ratio of a hardened flip-flop to DFF (through redundant node spacing) versus other requirements such as speed, and power early in the design process without costly simulations and experiments.

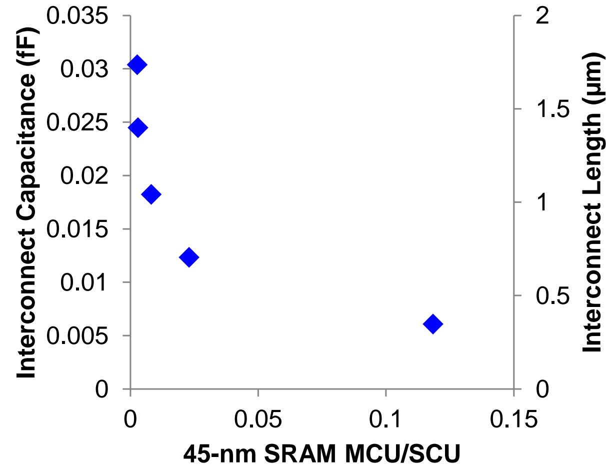

Figure 57. Interconnect capacitance and interconnect routing length between storage nodes versus 45-nm SRAM MCU/SCU. Interconnect capacitance values [69]

High-energy protons have been used previously as a substitute for neutron experiments [47]. Since proton experiments can be conducted relatively easily and quickly, the overall costs for the test campaign is lower. Proton experiments were performed on the 40- and 28-nm designs at Tri-University Meson Facility (TRIUMF) at the University of British Columbia in Vancouver. The test ICs were exposed to a 57 MeV proton beam with nominal VDD at a frequency of 10 MHz with a continuous data stream of 1 or 0. The 32-nm designs were tested with a 27.7 MeV proton beam [40]. Again, we see the hardened flip-flop proton SER results showing good correlation to the 45-nm neutron SRAM MCU data in Figure 58.

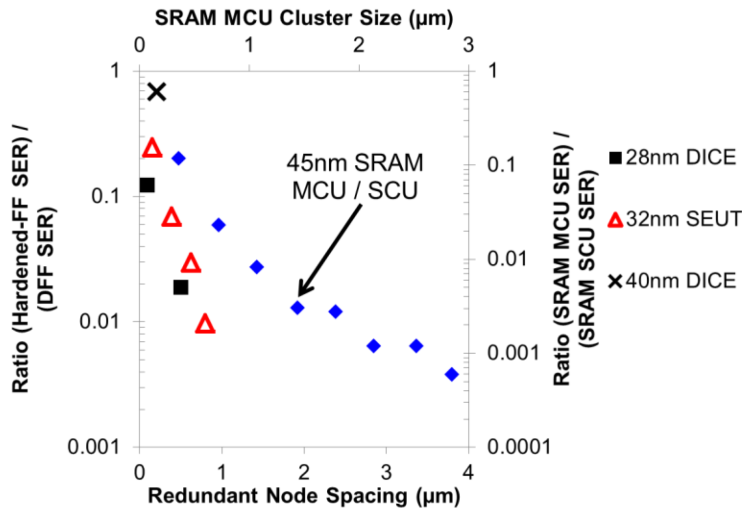

Figure 58. Ratio of hardened FF proton SER to DFF SER overlaid onto 45-nm SRAM neutron MCU data.

Section 5.5 Conclusion

The SER of any hardened design is strongly dependent of the distance between the redundant storage nodes. Even at technologies below 65-nm, redundant node spacing is still a viable option for reducing neutron SER. Again, these are local redundancy storage node designs, and hardened flip-flops that rely on temporal hardening schemes may not follow similar trends. A correlation study on the SER of hardened FF designs compared to DFF designs using neutron SRAM MCU cluster size data is developed. A 100x reduction in neutron SER for hardened flip-flops is possible when increasing node spacing from minimum transistor distance to 1 µm, but only reduction of ~10x is seen for node spacing increases from 1 to 3 µm. Without costly TCAD or experiments, it may be possible for designers to estimate a hardened FF neutron SER using published SRAM MCU data. Using SRAM MCU cluster size data as a baseline for hardened flip-flop SER, the designer can optimize the neutron and proton SER, area, speed, and power of a hardened flip-flop as a function of node spacing.

CHAPTER VI

DISCUSSION

The previous chapters showed results for DFF and hard-FF versus technology scaling. However, the simulations presented did not clearly show which mechanisms are affected by technology scaling dominate SEU cross sections. This chapter examines the results presented and shows what mechanisms could dominate the SEU cross section under different conditions with respect to dual-well bulk technologies unless otherwise noted.

To visualize how the SEU cross section corresponds to the physical area of the DFF, the cell area, and off-state vulnerable drain area are plotted along with LET 0.5, 3.5, and 58 MeV-cm^2/mg SEU cross sections versus technology nodes in Figure 59. For very low LET values near 0.5 MeV-cm^2/mg, such as alpha particles, the SEU cross section is similar to the off-state drain area of the transistors; this indicates that strikes outside of the drain areas do not lead to sufficient charge collection to create a SEU within the DFF. Therefore, for low LET ranges, the SEU cross section of DFF designs will be determined by the drawn dimensions of the DFF drain areas. Thus, with scaling, transistor areas decrease and force the SEU cross section of DFFs to decrease at very low LET values.

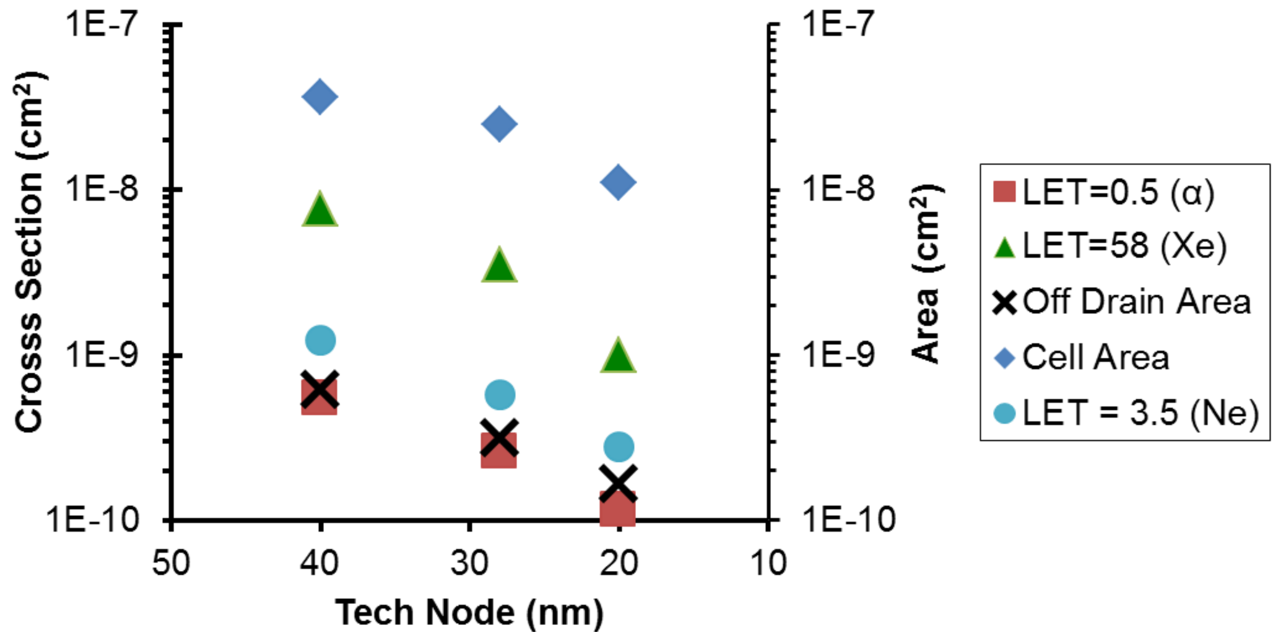

Figure 59. SEU Cross Section, Drain Area, and Cell Area vs. Technology Node.

At LET values above 0.5 MeV-cm^2/mg, sufficient charge is deposited by ions to cause SEUs for strikes outside of the vulnerable drain areas. For the LET range of 0.5 to ~3.5 MeV-cm^2/mg, DFF SEU cross sections increase exponentially, as can be seen in Figure 60 for technologies from 180-nm to 20-nm. However, it should be noted that the DFF designs in Figure 60 do not have the same schematic or layout for all technologies, (180-nm data are from [44] and 130-nm and 90-nm data are from [5]), which means that different DFF designs experience the similar trends in the 0.5 to 3.5 MeV-cm^2/mg LET range at different technology feature sizes. Mechanisms such as charge diffusion from the strike location (SEUs from nFETs) and WPM (SEUs from pFETs) begin to play a role in the SEU cross section of DFFs, leading to exponential-type increases of cross section in this LET range because of both mechanisms increasing the SEU cross section. On the other hand, charge sharing among transistors will be at a minimum in this LET range and thus upset reversal will not play a major role. Again, Figure 59 shows that for LETs up to ~3.5 MeV-cm^2/mg the SEU cross section follows the same trend as the off-state drain area vs. technology feature size, indicating that in this LET range the SEU cross section again is affected by the drawn transistors' dimensions which shrink with technology scaling.

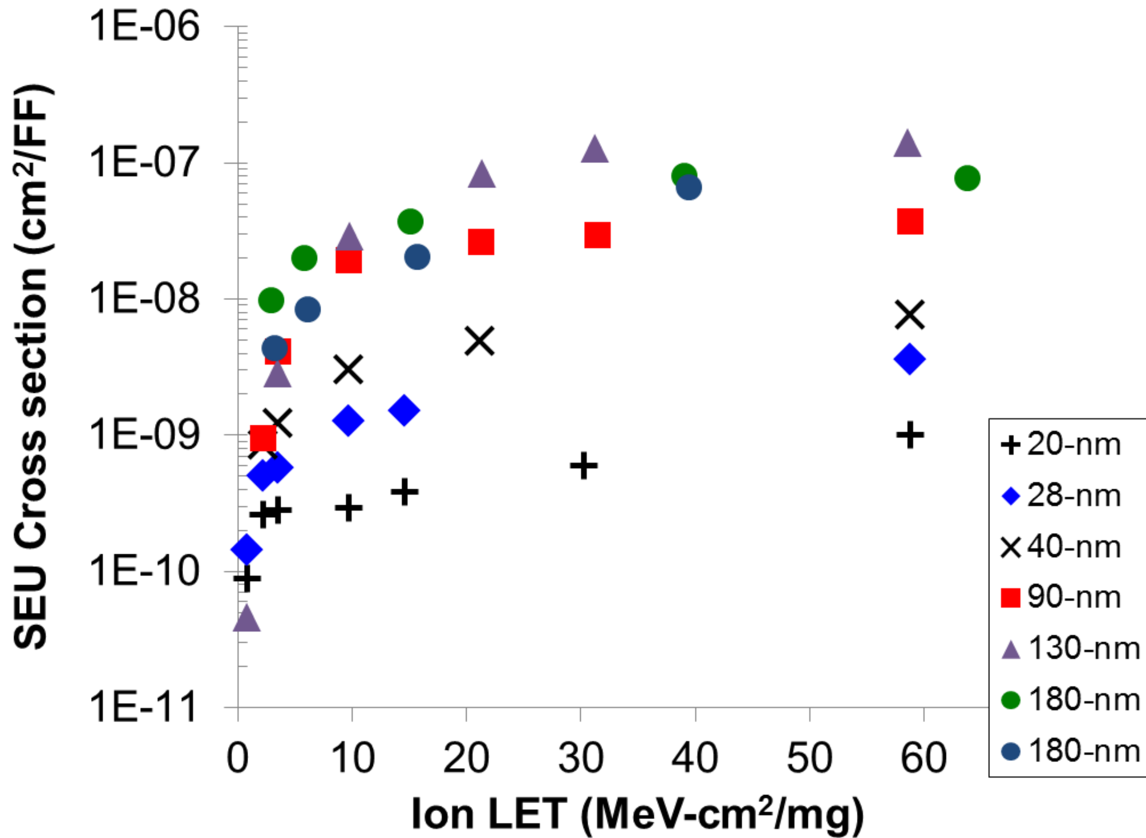

Figure 60. SEU Cross section vs. LET for DFFs from 180-nm to 20-nm

For LET values above ~3.5 MeV-cm^2/mg, the SEU cross sections of the various DFF designs stop increasing exponentially and enter a region of saturation (or near saturation with feature sizes below 90-nm), as seen in Figure 60. Above LET values of ~3.5 MeV-cm^2/mg, SE deposited charge and WPM mechanisms begin to encompass multiple transistors leading to multiple node charge collection and upset reversal. The probability of upset reversal can increase with technology scaling due decreased transistor pitch and higher LET ions creating larger charge clouds, but this does not completely cancel out the probability of increasing the SEU cross section. As transistor spacing decreases with technology scaling, it is possible for charge sharing to cause upsets as charge is shared across the n-well and p-well boundary in a DFF layout. Charge sharing across the n-well and p-well boundary is less effective than charge sharing in the same well, and consequently upset reversal will have a more prominent effect on the resulting SEU cross section for a DFF. This can be seen in the DFF angular results in

Section 4.2. Upset reversal probability increases with technology scaling due to decreasing distances between transistors in DFF designs and increasing LET.

In the LET range above ~3.5 MeV-cm^2/mg, WPM will play a major role in the SEU cross section and affect the upset reversal mechanism in DFF designs. One way circuit designers could change the DFF SEU cross section trends in this LET range is by altering the distance between well contacts (changing well contact density). By decreasing the well contact spacing (increasing well contact density), the WPM area and duration will be decreased; if sufficient well contacting is used, such as strip or stripe well contacts, the WPM area and duration become very small and WPM will not create significant charge sharing, thereby decreasing upset reversal. Thus, by decreasing the well contact spacing, designers could potentially reduce the impact of the WPM mechanism and upset reversal, causing an increase in the SEU cross section change versus LET compared to more sparse well contact spacing.

The simulations in this work show that WPM activating the parasitic bipolar of transistors is major factor in charge sharing that designers can influence through transistor placement, well taps, or well width unlike diffusion of charge. Designers can charge sharing by diffusion and WPM effects on upset reversal by changing the spacing between transistors that control data and data_bar in a DFF layout. If the transistors that control the complimentary data storage nodes are next to each other in the layout, the complimentary data pair transistors will collect similar amounts of charge due to a single ion strike through diffusion of charge or WPM. The more similar the amount of charge collected by the complimentary data pair transistors, the effect upset reversal is with preventing a SEU from occurring. The further apart the complimentary data pair transistors are placed, the larger difference in the amount of charge collected for the two transistors and leading to less effective upset reversal. For DFF designs, it is advantageous for designers to place the complimentary data pair transistors directly next to each other in the layout to encourage the upset reversal mechanism.

Placing all complimentary data pair transistors of a DFF design next to each other in the layout to take advantage of upset reversal is not always an option. For example, if a designer has access to a diffusion model, WPM model, and SE parasitic bipolar activation model, it is possible to optimize the complimentary data pair transistor spacing

along with placement and routing of other transistors while taking advantage of upset reversal; this would give the designer more options in routing/placement to meet area, speed, and power design metrics. If the SEU robustness of a DFF design is top priority and no upset reversal models are at hand, then a designer would want to try and make the complimentary data pair transistor spacing as small as possible in the layout to maximize the probability of upset reversal preventing SEUs.

By manipulating the well width and spacing between well contacts, designers can influence charge sharing through WPM effect on upset reversal in DFF designs. Decreasing the well width and/or increasing the well contact spacing leads to a decrease in the conductivity of the well to remove charge after an ion strike and increases the duration and the area covered by WPM thus activating the parasitic of bipolar of many transistors for longer time periods. Increasing the WPM duration and area causes an increase chance of upset reversal preventing a SEU by decreasing the well width, but the well width is limited by the overall layout strategy and designers may not have much leeway in changing this parameter. Another way to increase the probability of WPM and upset reversal is by changing the well contact spacing; increasing the well contact spacing increases the duration and area of WPM increasing the probability of upset reversal. To maximize upset reversal through WPM, a designer can use the maximum allowed well contact spacing around the DFF design.

There are two drawbacks of increasing the probability of upset reversal in DFFs through WPM by decreasing the conductivity to well contacts: increased SET pulse width and increased probability of latchup. Increasing the WPM duration and area can increase the number of SETs and SET pulse widths in logic and DFF designs. This increased number of SETs and SET pulse widths can increase the chance of upsets occurring in the combinational logic and is a factor of clock frequency. Latchup becomes a concern because the decreased well conductivity increases the resistance to the bases of the parasitic BJTS allowing lower LET particles to trigger the latchup condition. Thus, designers must take care when using well width and well contact spacing to maximize the upset reversal response through WPM because soft errors could increase due to SETs in combinational logic or lead to latchup reliability issues in a design.

Another factor that can affect SEUs in DFFs is the shrinking of the drawn transistor drains constricting the amount of charge from the substrate to the vulnerable drains. The opening to the substrate affects how quickly charge can be swept from the substrate to the drain junction; the smaller the drawn drain area, the slower the rate that charge can be collected, and changing the charge collection time profile. Thus, strikes away from the drain will collect less charge due to smaller openings as technologies scale and transistor areas decrease, ultimately adding to decreasing SEU cross sections for DFF designs. Designers should note, that there is a trade-off of using a smaller width transistor to try to take advantage of this effect in a given technology node; this leads to a smaller drive current and can lead to an increase in the SEU cross section.

DFF experimental results show that alphas, normal incidence heavy ions across the LET spectrum, neutrons, and high energy protons that the SEU cross section should decrease with technology scaling. If the same DFF design relative transistors sizes and transistor placement are used, then the SEU cross section will decrease with scaling unless there is a disruptive change in well parameters or transistor geometry, it is reasonable for a designer to assume the SEU cross section for a DFF design will decrease with technology scaling.

Hardened redundant storage node flip-flop designs are usually designed to meet a certain SEU cross section specification, unlike DFF designs that are optimized for area, speed, and power rather SEU robustness. The SEU response of a hard-FF design is determined by the distance between the redundant storage node pairs. The smaller the distance between the sensitive node pairs, the lower LET a particle must have to cause a SEU in a hard-FF. In traditional hard-FF designs, the redundant storage nodes were placed in the same wells, but this did not prove to be an issue until the 130-nm technology node [50].

In a rad-hard FF, TCAD simulations showed that WPM modulation in the n-well is a dominant factor in causing charge sharing among pFETs compared to charge sharing through diffusion in nFETs in a p-well implanted in a p-substrate (in dual-well technologies) in causing SEUs. Again, WPM in a p-well implanted in a p-substrate is shown to be negligible causing SEUs or upset reversal. If the spacing between the pFETs controlling redundant storage node pairs is large enough, low LET particles are not able

to induce a WPM area that can encompass multiple redundant storage node pFETs. As the LET of particles increases, the WPM area grows and can cause SEUs in a hard-FF by activating the parasitic bipolar of multiple pFETs. If the spacing is far enough apart that charge sharing due to diffusion of SE charge in the p-well between nFETs is small, then only WPM in the n-well causing charge sharing among pFETs will cause SEUs in the hard-FF which is usually the case for designs with proper node spacing; the hard-FF with larger than minimum transistor node spacing shows a different trend when only WPM causes SEUs, the SEU cross section of hard-FF designs versus increasing LET at a increases at a much slower amount than the DFF. If a triple well technology is used, WPM charge sharing among nFETs causing SEUs in a hard-FF can occur and will be a reliability concern. Thus, as technology scaling progresses, redundant storage node spacing will dominate the SEU cross section of hard-FF designs.

Simulations and measurements have demonstrated that regardless of the topology of the FF design, or the geometry of the layout, some common trends in cross section versus LET can be expected to continue as feature sizes shrink and LETs increase. If n-well parameters changed by a large amount with technology scaling, a different trend might be seen for hard-FF designs with similar redundant node pair spacing. The TCAD simulations show that the WPM response is strongly determined by n-well parameters and the hard-FF SEU response would be sensitive to this and would show in these data. One way designers can reduce the WPM effect on SEUs in a hard-FF is by decreasing well contact spacing (a common hardening technique for traditional hard-FFs), but at the cost of increased area and interconnect routing length, which translate to increases in power and delay.

The angular data shows that traditional hard-FFs may only provide small improvements over DFF designs in space applications, even though lower LET particles dominate the LET spectrum. Thus, for space applications, designers may need to implement techniques where the redundant storage node pair transistors are placed in separate wells, or well contact density is increased to reduce the probability of charge sharing causing SEUs [50], but at the obvious cost of increased area, increased power, or decreased speed.

Alpha and neutron experiments have shown that traditional redundant storage node layouts still provide adequate SEU robustness for terrestrial environments. Alpha particles do not impart enough charge to result in adequate WPM to cause a SEU in hard-FFs. Neutron experiments show that there increased probability secondary particles generated can impart sufficient charge to create SEUs in the hard-FF designs, but hard-FF still perform 100X to 1000X better depending on the redundant storage node spacing used even as technologies scale down to 28-nm. Again, the experimental data of various hard-FF designs across different technologies show the improvement over DFF designs is dominated by node spacing rather than technology parameters as technology feature sizes shrink.

CHAPTER VII

FUTURE WORK

To further this work, more accurate 3D TCAD models corresponding to commercial PDK doping parameters could be developed and integrated with spice models from the PDK. The same set of simulations could be conducted with the same flip-flop design with the commercial 3D TCAD models to examine what effects shown here dominate the SEU response of the flip-flop. Also, when calibrating the models, the TCAD models need to take into account well contact placement. Process variations may need to be taken into account when calibrating to heavy-ion data. This would require a large matrix of simulations and time to complete. One way of accomplishing this would be calibrating to 90-nm and older models which have less channel engineering and more readily available doping concentrations making it easier to calibrate TCAD models.

With further TCAD simulations calibrated to heavy-on data, it would be possible to create models related physical processes. Two important models would be related to diffusion and WPM. The simulations in this work show that diffusion plays a strong influence on nFET charge collection, especially in dual well processes. Well potential modulation dominates the charge collection process of pFETs and nFETs within a triple well implant. These models would benefit both D-FF designs and hardened designs.

A set of experiments that would help further calibrate TCAD models would involve a DICE design with the node spacing between sensitive node pairs are varied. This would help to calibrate the diffusion and WPM models from the D-FF designs. By varying the node spacing in the DICE design, the fidelity of charge sharing can be further calibrated.

In future technologies, charge sharing characteristics of FETs can change due to changing device geometries, such as FinFETs. Experiments with the same D-FF and hardened designs could be conducted to see how these geometry changes can affect the SEU cross section. These experiments with calibrated diffusion and WPM models could further explain the charge collection process of FETs as geometries change.

CHAPTER VIII

SUMMARY

For heavy-ion particles with LET below 58 MeV-cm2/mg, standard D-FF SEU cross sections decrease with decreasing feature sizes showing a dominance of cell area over other technology parameters that affect SEU mechanisms. TCAD simulations show that scaling well parameters can cause competing SEU cross section trends as technology feature sizes are reduced. Other competing mechanisms that affect SEU cross sections, such as SEU reversal and decreasing current drive, will continue as technology feature sizes decrease. Heavy-ion experiments of D-FF show that mechanisms decreasing SEU cross sections dominate over mechanisms that will cause increases in SEU cross sections with technology scaling.

Experiments conducted on various redundant storage node FF design in various technologies with heavy-ions, neutron, and protons show that redundant storage node spacing dominates over changes to the process. Hard-FFs with similar redundant storage node spacing across technologies show the similar SEU cross sections for heavy-ions. Neutron experiments of various hard-FF and D-FF designs show that the SEU improvement of a hard-FF to D-FF is strongly dependent on storage node spacing below 65-nm technology nodes.

With technology scaling, hardened flip-flop designs show that SEU cross sections are dominated by sensitive node pair spacing compared technology process parameters for both direct ionization of particles and indirect ionization from inelastic collisions. D-FF designs show a decrease in SEU cross section with technology scaling following a similar trend as area scaling. Neutron and protons experiments hard-FF designs shows it requires an exponential increase in area, speed, and power to obtain a linear decrease in SER by increasing spacing between storage nodes. Redundant flip-flops' ability to maintain the same SEU robustness with scaling to compete with decreasing cross sections of D-FF designs shows that aggressive design techniques are needed to keep SEU robustness, such as LEAP [51] or techniques created by Boeing [50].

APPENDIX

A. Test Chip Descriptions

The 40-nm, 28-nm, and 20-nm test chips were created in commercial bulk CMOS processes. Each test contained multiple different flip-flop designs that were both soft and hardened, shown in Table 10. The designs were created as 1X height cells or 2X height cells, as illustrated in Figure 61. Each flip-flop design was placed in an 8-kb serial shift register, similar to Figure 62. Data was input into the 8-kb shift registers with a constant 1 or 0 pattern at ~ 10 MHz clock frequency. Each chip was tested at the nominal supply voltage for the technology node. An error detection circuit was connected to the output of the 8-kb shift register to count errors at a ~10 MHz clock frequency. Each test included an on-chip phase lock loop (PLL) to generate a clock on chip. The clock source output was distributed to the 8-kb using a clock tree network. The data source was distributed to the input of all 8-kb shift registers with a buffer network. All 8-kb shift registers are exercised at the same time. A FPGA communicates with the chips to control data pattern, clock frequency, and monitor errors.

Table 10. Technology Node Summary of number of flip-flops and die.

Tech Node (nm)	# DFF Designs	# Unique Die
40	17	1
28	40	2
20	72	3

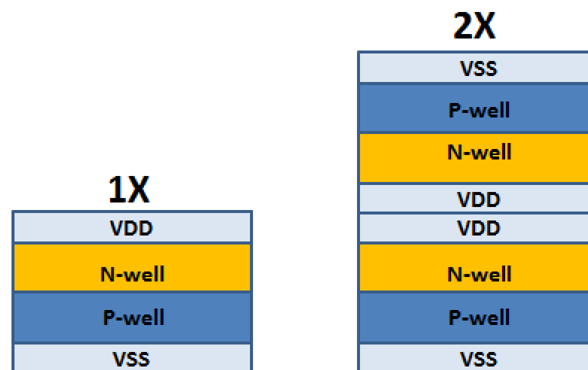

Figure 61. 1X and 2X height cell illustration.

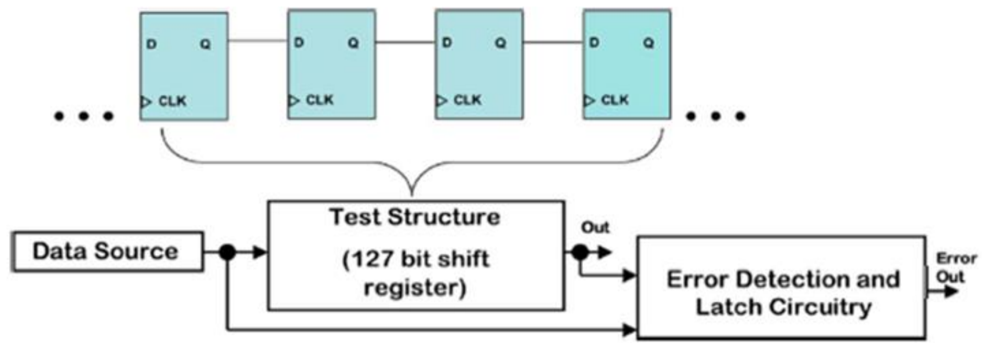

Figure 62. Illustration of the shift register design used in the test chips [70].

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