DEVELOPMENT OF VERTICAL NANODIAMOND VACUUM FIELD EMISSION MICROELECTRONIC INTEGRATED DEVICES

By

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To my dearest wife

And

To my beloved parents and brothers

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CHAPTER I

INTRODUCTION

1.1 Overview of the development of vacuum microelectronics

Conventional vacuum tubes played an important role in the development of electronic technology that led to the evolution of communication and audio industries, including radio broadcasting, radar, telephone networks, television, and sound reinforcement, etc [1]. The vacuum tube triode was the first electronic amplification device that could provide power gain at audio and radio frequencies, making it widely used in consumer electronics before 1940s. However, vacuum tube devices were soon become obsolete and overtaken by the solid-state microelectronic devices in 1950s due to the invention of solid-state transistors [2] and the subsequent development of low-cost, batch-fabricated integrated circuits (ICs) [3–5]. Compared to solid-state transistors, the conventional thermionic vacuum tubes were large, fragile, and inefficient. They required a vacuum to operate and used a cathode heated to over 1000 °C to generate the electrons and thereby had high power consumption. Consequently, vacuum tubes were replaced by solid-state transistors and ICs in most of modern microelectronics and computing applications.

Nevertheless, solid-state microelectronic devices have some disadvantages as well, such as limited operating speed due to the carrier saturation velocity in the solid and sensitivity to radiation and high temperature due to junction leakage and damage of the semiconductor crystal structure [6], restricting their utilization in some specific electronic applications. On the other hand, the emergence of vacuum devices in microelectronic forms, vacuum microelectronic devices (VMDs) [7–11], using micron-size cold cathodes has overcome the disadvantages of conventional vacuum tubes, generating renewed interests in the exploitation of VMDs for many new applications. The realization of VMDs based on miniaturization of vacuum devices to micro- and nano-scale dimensions, using novel field emission cathode materials, was enabled by the facilitation of advanced semiconductor micro/nanofabrication techniques. The VMDs principally employ "cold" cathodes based on electron field emission process [12], where electrons quantum-mechanically tunnel through the surface potential barrier of the material into vacuum by an externally applied electric field across the vacuum, in contrast to the conventional vacuum tubes that exclusively utilize thermionic "hot" cathodes [13] by increasing the thermal energy of electrons for emission. The replacement of thermionic cathodes with miniature field emission cathodes significantly improved the vacuum device performance and reduced the size and weight of these systems.

Vacuum micro- and nano-scaled field emission devices (VFEDs) have several advantages. First, they can operate at room temperature since the electron field emission is employed to generate charge carriers, eliminating the high thermal energy required to heat up the cathode for electron emission. Second, VFEDs possess high operation speed and low energy dissipation due to the superior ballistic transport of free electrons in vacuum, which is more efficient than the collision-dominated and mobility-limited carrier transport in solid-state devices. Third, the "junction-free" feature allows VFEDs to operate at extreme conditions, including high temperature and high radiation, with no performance degeneration, unlike solid-state devices that suffer performance degradations in harsh environments. These advantages of VFEDs are beneficial for many applications such as active elements in extreme microelectronic devices and integrated circuits, electron beam sources for lithography and microscopy, field emitter arrays for flat panel displays, high power microelectronics for amplification, high speed/frequency electronics for harsh environment applications (e.g. aviation and space-based communication systems), novel sensors, and X-ray generators for medical applications (e.g. computed tomography scanners) [8–11,14–17]. **Table 1.1** summarizes the device properties of vacuum micro/nanoelectronic devices and solid-state devices for promising applications [9].

The rebirth of vacuum tubes in micro- and nanoelectronic forms have led to the active pursuit of VFEDs with high and stable emission current at low operating voltage and their further implementation into vacuum integrated circuits (ICs) [18] for practical applications. Despite there having been conceptual and modeling proposals for vacuum ICs and logic gates [19,20], only few practical implementations of vacuum devices at the circuit level have been reported in the past. Improvement in VFE device efficiency and stability, particularly cold cathode reliability, is required for the realization of practical VFE microelectronic devices in ICs. Therefore, the core research of vacuum microelectronics for the last several decades has been focused on the development of useful cathode materials and structures with better and more reliable performance, including the employment of electric field enhancement on sharp micro/nanotips to assist electron quantum tunneling through the solid-vacuum potential barrier, the utilization of emitter materials with low work function, mechanical stability, and chemical inertness to enhance electron emission and reliability, and the fabrication of a large array of emitters to deliver high emission current.

Table 1.1 Comparison of vacuum microelectronics versus solid-state electronics

Property	**Solid-state devices**	**Vacuum micro/nano electronic devices**	**Advantage and disadvantages of VMDs**
Structure	Solid/solid interface	Solid/vacuum	Ballistic electron transport in vacuum
Size	Micron/nano-scale range	Micron/nano-scale range	Similar to solid-state devices
Current density	10^4-10^5 (A/cm^2)	10^4-10^5 (A/cm^2)	Same as solid-state devices
Voltage (V_{op})	> 0.1 V	> a few (V)	Higher operating voltage
Electron transport - medium - ballistic - coherence	Solid carrier mobility limited Length < 0.1 μm Time < 10^{-13} s at RT	Vacuum 100 % ballistic Length >> 0.1 μm Time >> 10^{-13} s	Better electron transport with less collision and less energy loss
Cutoff frequency	< 20 GHz (Si) < 100 GHz (GaAs)	< 100-1000 GHz	High frequency operation
Power	Small	Large	High power applications
Speed	Moderate	Very fast	High speed applications
Radiation hardness	Poor	Excellent	Harsh environment applications
Temperature sensitivity	-30 to +50 °C	< 500 °C	
Reliability	Fair	Good	Better reliability
Life time	Medium	Long	Longer life time
Technology	Very well established	Recently developing	Technology improvement need to be done

Metal emitters were first developed and employed in field emission diodes and triodes for VFEDs since 1960s [8,21–28]. Although the refractory metal emitters provided robust mechanical properties in high applied electric fields required for high electron current density, the drawbacks of high work functions and impurity adsorption on metal surfaces have restricted their potential applications. The high work functions of metals resulted in high threshold electric fields and thus required high turn-on voltages. In addition, metal emitters are very sensitive to impurity adsorption, which would results in unstable emission current, and therefore require extremely high vacuum conditions for a stable operation. Despite various methods such as thermal annealing [29] and co-adsorption of silicon (Si) and titanium (Ti) on tungsten (W) emitters [30] have been proposed to ameliorate the instability and poor emission characteristics of the metal cathodes, limited improvement was achieved.

The well-established silicon-based microfabrication technology was exploited for the development of silicon-based VFEDs in diode and triode configurations [31−43]. The microfabrication techniques facilitated the formation of arrays of silicon field emission sharp tips, making mass production of emitters possible. However, their field emission behavior is relatively poor because of the high work function, low thermal conductivity, and inadequate mechanical and chemical properties, restricting their practical applications. The poor thermal conductivity and low breakdown electric field of silicon, which lead to the instability of silicon emitters operating at high emission current and high field, prohibit their employment in high emission current and high power applications. The heat accumulation and atom migration on silicon tips operating at high field and high current have been found to cause emission current degradation with time and device failure [44,45]. Besides, the impurity adsorption problem of silicon emitters causes unstable emission current and thus ultra high vacuum is essential for stable operation. To improve the emission performance and stability of silicon emitters, variety of approaches have been developed, including silicidation by metal adsorption [46,47], coating of silicon emitters with different materials [48,49], utilization of advanced emitter structures such as p^{+}-n^{++} junction [50], MOSFET [51], MIS cathode [52], MOS cathode [53], porous silicon diodes [54], and hybrid integration of field emitter arrays with solid-state JFETs [55]. Nevertheless, these techniques lead to complicated fabrication processes with little improvement in field emission performance, giving limited success of silicon-based VFEDs.

Recent research and development of carbon-derived materials such as diamond and diamond-like-carbon (DLC) [56–71], carbon nanotubes (CNTs) [15–17,72–76] and graphene [77–79] has revealed their superior electron field emission characteristics. The emitters composed of these carbon-derived materials have emerged as appealing candidates for the new generation of VFEDs. Among them, chemical vapor deposited (CVD) diamond has been demonstrated to yield large emission currents at low electric fields relative to that of metals and narrow band-gap semiconductors [70]. CVD diamond possesses the unique properties of low electron affinity [58–60], good thermal stability [80–82], excellent chemical inertness, and extreme mechanical hardness [83], making it a robust cathode material for VFEDs. The low electron affinity translates to low threshold electric field needed to achieve electron emission, hence an anticipated small turn-on voltage as well as low operating voltages for diamond-based VFEDs. Additionally, the high thermal conductivity of diamond prevents over-heating of the emitters while operating at large current density. The superior mechanical and chemical properties make diamond immune to ion bombardment and impurity adsorption, allowing diamond emitters to operate with good stability in less stringent vacuum levels for more practical utilization. Furthermore, diamond has a strong crystal structure and thus a high electric breakdown field, along with the high thermal conductivity, making diamond VFEDs capable of operating at high current with long life time. **Table 1.2** compares the material properties of diamond with those of silicon and metal for field emission applications [81,84]. These advantageous features signify that diamond is a promising emitter material for VFEDs in the potential applications such as vacuum ICs, sensors, flat panel displays, intense electron sources, and other high-power high-frequency electronic devices.

Table 1.2 Comparison of diamond, silicon and metal for field emission applications

Property	**Diamond**	**Silicon**	**Metal**	**Advantages of diamond**
Electron affinity (eV)	Low EA and NEA on some facets	4.05	4–6	Low operating voltage
Electrical breakdown field (V/cm)	1 x 10^7	2.5 x 10^5	N/A	High power applications
Thermal conductivity (W/cm-K)	10–25	1.5	0.5–5	High emission current/current density
Carrier mobility (cm^2/V-s)	1.5 x 10^3	2.0 x 10^3	10^2-10^3	High carrier saturation velocity
Surface chemical stability	Relatively inert to adsorption	Very sensitive to adsorption	Quiet sensitive to adsorption	High stability, larger emitting area
Vacuum requirement (Torr)	Relatively low vacuum (10^{-5}-10^{-6})	Very high vacuum (10^{-10} – 10^{-11})	Very high vacuum (10^{-9}-10^{-11})	Practical vacuum environment
Process Technology	Recently developing	Well established	Well established, but with slow progress	Technology rapidly advancing

More recently, the emergence of nanocrystalline diamond has elevated the utility of diamond for vacuum micro/nanoelectronics further, providing a wider range of applicability over the conventional microcrystalline diamond [69–71,85−100]. Apart from the advantageous properties of microdiamond, nanodiamond possesses smaller grain size (1–100 nm), higher volume density of grain boundaries, and much smoother and more uniform surface morphology, offering wider latitude for integration with other materials in fabrication processes and the final device forms. Besides, n-type conductivity can be achieved by *in situ* nitrogen doping in CVD nanodiamond film, concomitantly providing a deliberate amount of sp^2 graphitic inclusion in the sp^3 diamond matrix with enhanced electron emission characteristics [87–93]. Chapter III will give more details and discussions of the nanodiamond film used for VFEDs studied in this research.

1.2 Motivation

This research is motivated by the apparent advantages of vacuum microelectronic devices over solid-state microelectronics and conventional vacuum thermionic devices [101] and inspired by the emerging VFEDs using superior nanodiamond emitters for vacuum microelectronic applications:

- Vacuum is a superior electron transport medium compared to solid for high-speed electronics with less energy consumption. The electron velocity in vacuum can approach the speed of light (~3 x 10^8 m/s), while that in solid-state medium is limited by the carrier saturation velocity of the solid (~10^5 m/s in silicon) due to optical and acoustic phonon scattering.
- VFEDs can in principle operate at high frequency for fast modulation and high power. The operating frequency of VFEDs can approach 100–500 GHz, limited only by the parasitic capacitance.

- The operational characteristics of VFEDs are essentially insensitive to high temperature and radiation damage owing to their junction-free feature; unlike most solid-state devices which suffer from performance degradation under high temperature and radiation due to the junction leakage and damage of semiconductor crystal structure.
- Superior properties of nanodiamond including low electron affinity, high thermal conductivity, excellent chemical inertness, good mechanical hardness, small grain size, smooth surface morphology, attainable n-type electrical conductivity and insertion of a deliberate amount of sp^2-carbon for enhancing field emission behavior, qualify it as an excellent emitter material for field emission.
- Large emission currents from CVD nanocrystalline diamond at low electric fields have been experimentally demonstrated.
- The pursuit of reliable diamond vacuum field emission devices and their further development into integrated devices at circuit levels for practical applications are of great interests to the researchers in this field.

1.3 Objective of the research

The scope of this research is focused on (i) the development of a reliable and consistent process technique to fabricate three-electrode nanocrystalline diamond vacuum field emission devices, (ii) the study of their electron field emission characteristics and device operating principles in transistor and triode configurations, and (iii) the implementation of a nanodiamond vacuum integrated differential amplifier to demonstrate the feasibility of vacuum ICs for practical applications. The main idea is to develop vacuum microelectronic devices with high emission current at low operating voltages for integrated-circuit compatible and harsh environment applications. The research includes:

- Development of a dual-mask well-controlled microfabrication process, involving a mold-transfer self-aligned gate-emitter technique in conjunction with nanodiamond deposition into the micropatterned molds for the formation of micropatterned nanodiamond pyramidal emitter tips integrated with a self-aligned silicon gate electrode for a wide range of applications.
- Electrical characterization of the fabricated three-electrode nanodiamond field emission device in transistor and triode configurations, analysis of the field emission behavior using the modified Fowler-Nordheim theory, and the devices *dc* operating principles.
- Design and fabrication of vacuum differential amplifier employing nanodiamond field emission transistors on a single chip, composed of common nanodiamond emitter arrays integrated with partition gates and split anodes.
- Implementation and characterization of the nanodiamond vacuum microelectronic integrated differential amplifier, and analysis of the differential-amplifier performance using equivalent circuit model.
- Study the *ac* signal amplification performance of the fabricated nanodiamond vacuum field emission devices, including transistors, triodes, and differential amplifier, and perform analysis based on *ac* models of these devices.

1.4 Organization of the dissertation

There are seven chapters in this study, organized in the following topics:

- *Chapter I* introduces the vacuum microelectronic and electron field emission devices. The development of vacuum microelectronic devices is presented, followed by the advantages of microcrystalline and nanocrystalline diamonds as field emission materials for vacuum devices. The motivation and objectives of this research are also outlined.
- *Chapter II* reviews the theoretical background of electron emission in vacuum and the operating principles of vacuum field emission devices. The electron field emission theory and some possible mechanisms responsible for diamond field emission are discussed. Additionally, the basic operating principles of vacuum field emission diodes, triodes, transistors, and differential amplifiers are described.
- *Chapter III* is dedicated to the underlying basic science and unique properties of the core emitter material used in this research, nanocrystalline diamond, with particular emphasis on the application to vacuum micro/nanoelectronics. Additionally, an extensive survey of recent research work on diamond and nanodiamond field emission is presented.
- *Chapter IV* explains the proposed research and the methodological approaches utilized to achieve the objectives of this research work.
- *Chapter V* discusses the details of experimentation. The fabrication processes of vertically-configured nanodiamond VFE transistors and triodes and their integration into a vacuum differential amplifier are described, followed by the

device structural and material characterization. In addition, the electrical characterization techniques are also described.

- *Chapter VI* presents the vacuum field emission electrical performance of the fabricated devices, followed by further analysis and discussion of the device field emission behaviors and operating principles.
- *Chapter VII* summarizes the accomplishments of this research and recommendations for future work.

CHAPTER II

ELECTRON EMISSION and OPERATING PRINCIPLES of VFE DEVICES

This chapter first reviews the basic concepts of electron emission from solid into vacuum and the fundamental theory of electron field emission. Several possible mechanisms responsible for the electron field emission from CVD diamond are then described in detail. In the end, the basic operating principles of vacuum field emission devices including diode, triode, transistor and differential amplifier, are discussed.

2.1 Basic concepts of electron emission from solid into vacuum

Electron emission is the process of emitting electrons from a solid surface into vacuum, usually induced by exerting external energies onto the solid. Based on the form of applied energy, the electron emission processes can be categorized in three categories: thermionic emission by heat, field emission by electric field, and thermionic-field emission by both heat and electric field energies. The mechanisms for these processes can be explained by considering the energy band diagram of a metal-vacuum system [102] as shown in **Figure 2.1**. Electron emission can also occur by other methods such as light excitation (photoelectric electron emission), external electron energy (secondary electron emission), and internal polarization switching (ferroelectric electron emission). These interesting electron emission phenomena are beyond the scope of this research.

For thermionic emission from metal, electrons emit into vacuum due to heat application normally at very high temperature of 1500-2500 °C. The temperature required for electron emission depends on the material work function (Φ). As temperature is absolute zero (0 K), all electrons in solid have energy below the Fermi level (E_F). Some electrons acquire kinetic energy and have total energy above the Fermi level when temperature increases. If the temperature is sufficiently high, some electrons can have total energy higher than the vacuum level (E_{vac}) and thus become ready to emit into vacuum under the condition of no applied potential, as shown in the case of (1) e^- in **Figure 2.1**.

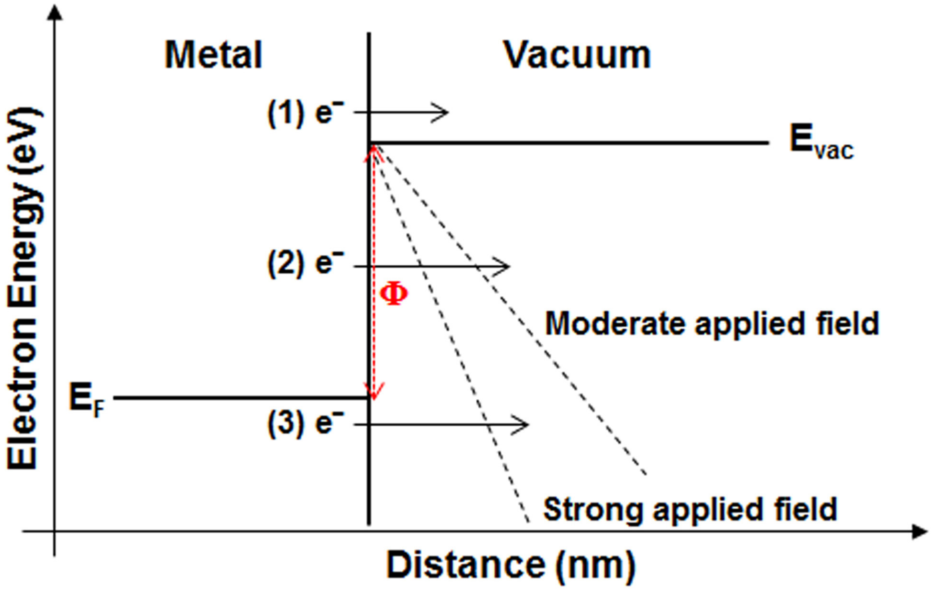


Figure 2.1 Mechanisms for (1) thermionic, (2) thermionic-field, and (3) field emissions.

As for thermionic-field emission, the metal is usually heated up to a moderate temperature, at which some electrons gain kinetic energy and have total energy above the Fermi level but still below the vacuum level, and thus no electron is readily emitted. Additional energies are required to thin down the potential barrier for these electrons to emit into vacuum. Therefore, a moderate electric field must be applied to thin down the potential barrier which can reduce the electron tunneling distance and thereby enhance the electron tunneling probability, as illustrated in the case of (2) e^- in **Figure 2.1**. This thermal-field activated emission process via quantum-mechanical tunneling is so called thermionic-field emission. Depending on the metal work function, thermionic-field emission from metal can be observed at moderate temperature of 700-1500 °C.

Different from the other two emission processes, electron field emission is a unique quantum-mechanical effect of electrons tunneling from a condensed matter (solid or liquid) into vacuum at low temperature. In this case, most of electrons have total energy below the Fermi level and require a very high energy to overcome the potential barrier at the solid/vacuum interface for emission. Therefore, a strong external electric field must be applied to thin down the potential barrier (width of ~ 1.5 nm), allowing electrons to quantum-mechanically tunnel into vacuum, as shown in the case of (3) e^- in **Figure 2.1**. This phenomenon is called field emission since electric field is the main energy source inducing the electron emission. The efficiency of the field emission process is tens of millions of times higher than that of other known emission processes. The field emission process exhibits extremely high current density with no energy consumption, providing exceptionally wide possibilities for practical application of this effect. In the following sections, the theoretical aspects of field-induced electron emission as the main topic of this research are discussed in detail.

2.2 Fowler-Nordheim theory of electron field emission

The complete electron field emission mechanism from a metal cathode can be illustrated by the corresponding energy band diagrams, as displayed in **Figure 2.2**. As an anode-cathode voltage is applied across the vacuum gap, a uniform electric field is created and the rectangular surface potential barrier is changed into a triangle barrier accordingly. If the applied voltage is sufficiently strong to reduce the width of surface potential barrier approaching ~ 1.5 nm, the low energy electrons can quantum-mechanically tunnel from the highest occupied energy states in the solid into vacuum and are subsequently accelerated to the positively biased anode [101].

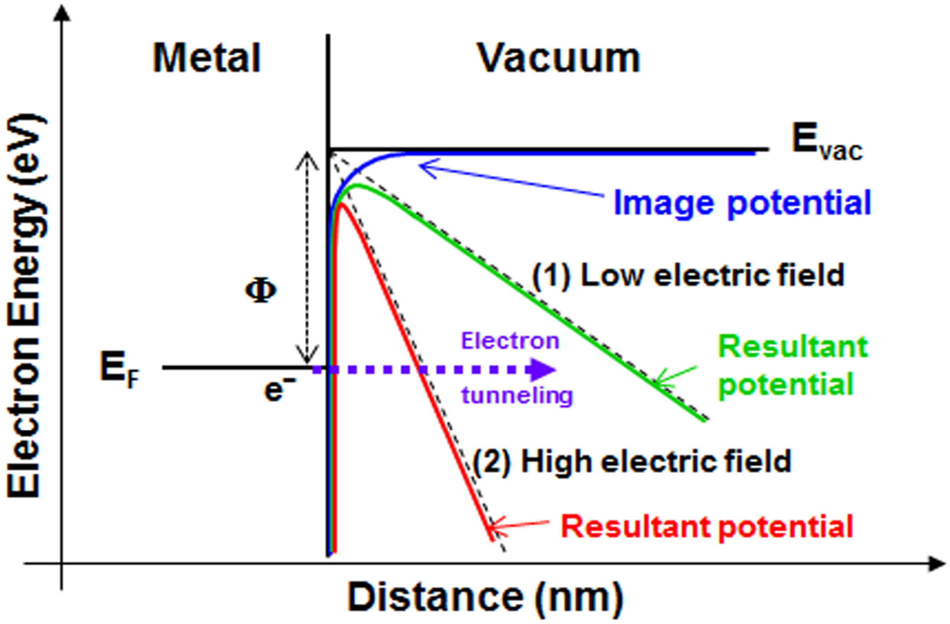


Figure 2.2 The energy band diagram of a metallic emitter for illustrating the electron field emission mechanism. The resultant surface potential barriers under low and high applied electric fields are shown, respectively.

The electron field emission theory for cold cathodes with flat surface was developed by Fowler and Nordheim in 1928 [103], describing the dependence of the emission current density J (A/cm^2) on the work function of the emitting surface Φ (eV) and the electrical field across the parallel plates E (V/cm) [103–105]. The J is equal to the total emission current I (A) divided by the emission area A (cm^2) whereas the E is equal to the applied anode-cathode voltage V (V) divided by the anode-cathode spacing d (cm). The Fowler-Nordheim (F-N) theory can be expressed as:

$$J = \frac{I}{A} = k_1 \frac{E^2}{\phi} \exp\left(-k_2 \frac{\phi^{1.5}}{E} \right) \tag{2.1}$$

where k_1 and k_2 are universal constants given by:

$$\begin{aligned} k_1 &= \frac{e^3}{8\pi h} = 1.54 \times 10^{-6} \left(AeV / V^2 \right) \\ k_2 &= \frac{4(2me)^{0.5}}{3e\hbar} = 6.83 \times 10^7 \left(V / eV^{1.5} cm \right) \end{aligned} \tag{2.2}$$

where e is the elementary positive charge, m_e is the electron mass, h is the Planck's constant and $\hbar = h/2\pi$. It should be noted that Eq. 2.1 was derived for a metal cathode with the following physical assumptions [12]:

- The metal cathode has a free-electron band structure.
- The electrons obey Fermi-Dirac statistics.
- It is at absolute zero degree (0 K).
- The cathode has a smooth flat surface.
- The work function is uniform across the emitting surface and independent of electric field.
- The electric field outside the metal surface is uniform.
- The effect of image field between the emitted electrons and the surface is neglected in a first approximation.

From the F-N equation, the emission characteristic is strongly influenced by the work function of the emitting material and is an exponential function of the applied electric field.

In 1956, Murphy and Good [13] presented a full mathematical analysis of the standard physical assumptions in F-N theory to consider the image field effect which is due to the interaction of electrons in vacuum and the metal cathode. The interaction modifies the triangle potential barrier as shown by the colored solid curves in **Figure 2.2**. The numerical result is the inclusion of two electric field dependent elliptical functions $v(y)$ and $t^2(y)$ into Eq. 2.1, where y is the image charge lowering contribution to Φ and defined as:

$$y = k_3 \frac{E^{0.5}}{\phi} \tag{2.3}$$

where k_3 is also an universal constant given by:

$$k_3 = \left(\frac{e^3}{4\pi\varepsilon_0} \right)^{0.5} = 3.79 \times 10^{-4} \left(eVcm^{0.5} / V^{0.5} \right) \tag{2.4}$$

where ε_0 is the permittivity of vacuum ($8.85\text{x}10^{-14}$ F/cm). The image-corrected F-N equation is expressed as:

$$J = \frac{I}{A} = k_1 \frac{E^2}{t^2(y)\phi} \exp\left(-k_2 \frac{v(y)\phi^{1.5}}{E} \right). \tag{2.5}$$

The sharp cone structure, which is generally referred as the "Spindt cathode", is usually employed on various types of emitting materials for enhancing emission performance due to the field enhancement at high curvature regions. Thus, it is important to take the non-uniform electric field distribution of the system into consideration in the F-N equation, Eq. 2.1, which is derived for planar cathode with the assumption of uniform electric field applied across the vacuum gap. The electric field is highest at the tip apex and rapidly decreases outward to the anode. The precise calculation of potential distribution, electric field, and emission current for a sharp microstructure involves numerical calculation of 3-dimensional Poisson equation and Schrodinger equation for electron emission [106–110]. Nevertheless, the emission current from a sharp microstructure can be obtained with a modification of F-N equation derived for a planar metal cathode simply by replacing the parallel electric field E in Eq. 2.1 with the electric field at the apex of the sharp tip E_{tip}, that is:

$$E_{tip} = \beta E = \beta \frac{V}{d} \tag{2.6}$$

where β is defined as the geometrical field enhancement factor. In other words, the electric field on the sharp tip is enhanced by a factor of β relative to that on planar structure owing to the sharp microstructure. Therefore, the revised F-N equation can be expressed as:

$$J = \frac{I}{A} = k_1 \frac{\beta^2 E^2}{t^2(y)\phi} \exp\left(-k_2 \frac{v(y)\phi^{1.5}}{\beta E} \right). \tag{2.7}$$

This simple approximation implies that, in order to extract the same emission current, it requires a much lower applied voltage for a sharp microstructure than that for a planar cathode with the same vacuum gap, thus enhancing the electron emission. It is in well agreement with experimental results because the electric field of a sharp tip is strongest at the apex and reduced rapidly for the region away from the apex. Therefore it can be assumed that most of emission current arises from electron tunneling within the vicinity of this highest electric field region. From Eq. 2.7, it is obvious that a large β is favorable for extracting high emission current. Generally, β is determined by the geometrical shape and surface condition of the emitter. In the following section, more details and discussions about β will be addressed.

By rearranging Eq. 2.7 and taking the natural logarithm, it can be further rewritten as:

$$\ln\left(\frac{I}{E^2} \right) = \ln\left(\frac{k_1 A \beta^2}{t^2(y)\phi} \right) - \left(\frac{k_2 v(y)\phi^{1.5}}{\beta} \right)\left(\frac{1}{E} \right). \tag{2.8}$$

Thus, by plotting the emission current in the form of $ln(I/E^2)$ versus $1/E$, the field emission mechanism can be verified by a straight line with a negative slope proportional to $\Phi^{1.5}/\beta$ and a y-intercept proportional to $A\beta^2/\Phi$. For simplified analysis of the F-N theory, $v(y)$ and $t^2(y)$ are often taken to be unity in the calculations and hence the exclusion of the image charge effects.

2.3 Electron field emission from diamond

Diamond is one of the main high-pressure crystalline allotropes of carbon. In diamond, each carbon atom is covalently bonded to four other carbon atoms in a tetrahedral geometry. Each carbon atom is sp^3-hybridized. Eight carbon atoms form a cubic unit cell [111] as shown in **Figure 2.3(a)**, and these unit cells extend and connect together, constructing a stable 3-dimensional network structure with sp^3 covalent bonds and thus strong diamond crystal, as shown in **Figure 2.3(b)**. Diamond, as mentioned in Chapter I, has been demonstrated as a superior emitter material with excellent field emission behavior and robust mechanical and chemical properties. The presence of low electron affinity on diamond surfaces [58−60], coupled with practical chemical vapor deposition (CVD) of diamond [111−114] as a thin film on a variety of substrates, has attracted more attention to diamond's promise as high performance field emitters. Although the electron field emission mechanisms of diamond-related materials have been discussed over the past decades, the mechanisms responsible for high electron emission at low applied electric field from diamond are not clearly understood. Hence, this section focuses on the discussion about possible mechanisms of electron field emission from CVD diamond.

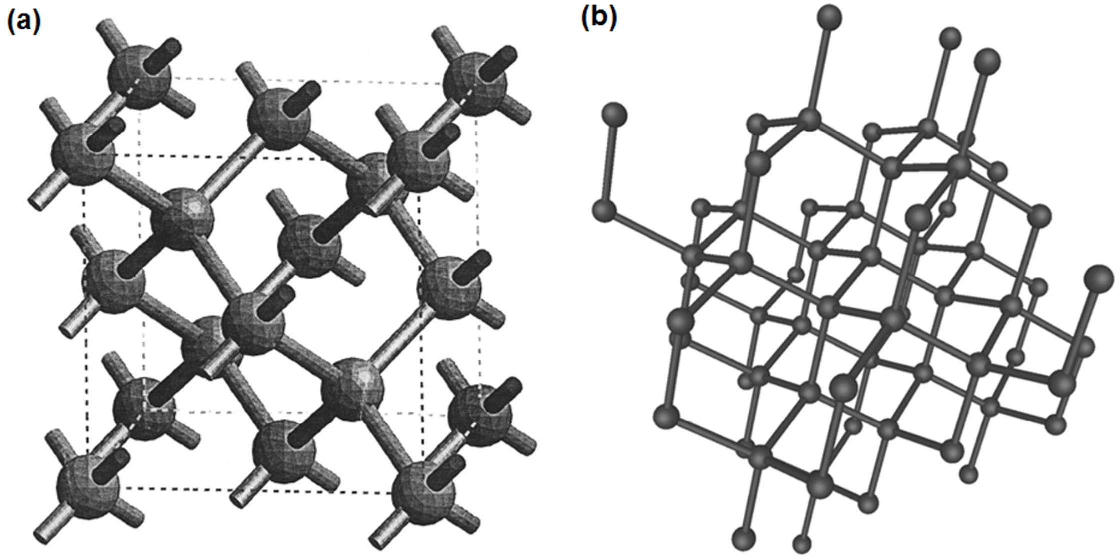


Figure 2.3 (a) The face-centered cubic structure of diamond crystal, and (b) 3-dimensional network of diamond crystals [111].

2.3.1 Energy band diagram of diamond

A complete knowledge on energy band diagram of diamond surface is key information to understand electron field emission from diamond. Diamond is an indirect wide band-gap material with $E_g = 5.45$ eV, thus having a relatively small energy barrier between conduction band and vacuum level, i.e. low electron affinity. Three distinct types of diamond surfaces have been widely studied [58–60,115−120]. **Figure 2.4(a)** schematically shows the hydrogen-free diamond surfaces with small and positive electron affinity, whereas **Figure 2.4(b)** illustrates the partially hydrogenated (111) and (100) diamond surfaces which have effective negative electron affinity (NEA), i.e. the vacuum energy level lies below the conduction band minimum. The adsorption of hydrogen forms a surface dipole layer, which lowers the diamond surface electron affinity. This reduction of electron affinity coupled with a short characteristic downward band bending results in the effective negative electron affinity. In addition, adsorption of a thin metallic layer such as Zirconium (Zr), Nickel (Ni), Cobalt (Co) and Copper (Cu) on the hydrogen-free diamond surface also results in the effective NEA property [121−124]. **Figure 2.4(c)** illustrates the energy band diagram of the true NEA. It is believed that completely hydrogenated diamond surfaces exhibit true NEA property [60,120,125].

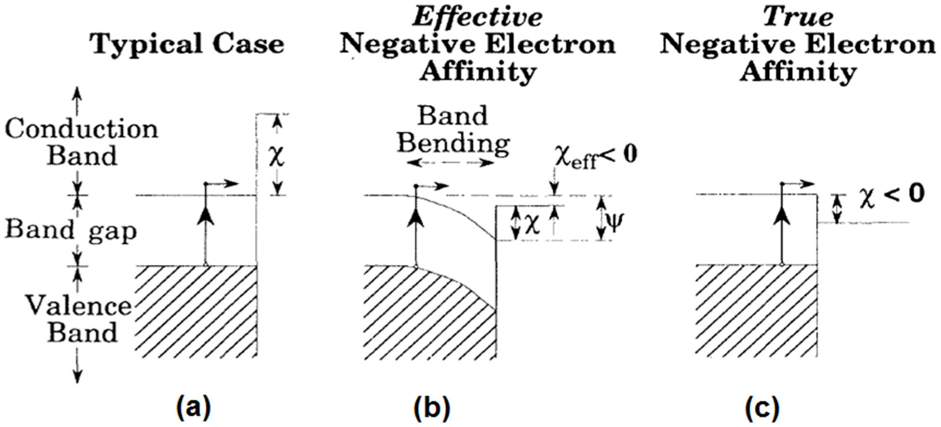


Figure 2.4 Energy band diagrams of diamonds with (a) positive electron affinity, (b) effective negative electron affinity, and (c) true negative electron affinity, respectively [60].

The occurrence of the true NEA has not been found for conventional semiconductor materials. Assuming an intrinsic diamond surface with small positive electron affinity, the corresponding energy band diagram for electron emission from the diamond surface can be drawn as displayed in **Figure 2.5** [102]. At thermal equilibrium, the conduction band minimum in diamond is below the vacuum level with a small surface potential barrier at diamond-vacuum interface, whereas the Fermi level in metal is very far away below the diamond conduction band minimum with a very high potential barrier at metal-diamond interface, as shown in **Figure 2.5(b)**. For electrons to emit into vacuum, they must be able to quantum-mechanically tunnel from metal into diamond, followed by drifting through the bulk diamond to reach to the diamond-vacuum interface and then tunneling into vacuum under an applied electric field, as shown in **Figure 2.5(c)**.

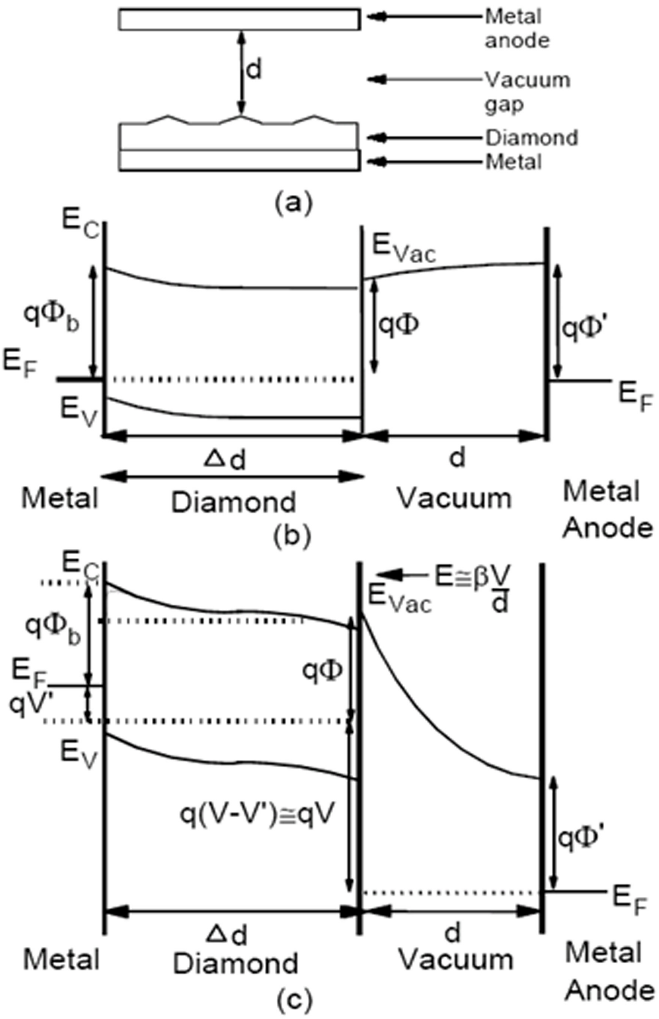


Figure 2.5 (a) Schematic diagram of a diode structure with diamond cathode and metal anode. (b) The corresponding energy band diagram at thermal equilibrium, and (c) the energy band diagram under forward bias [102].

It is believed that the small electron affinity of diamond is responsible for the observed high field emission current at low applied electric field because electrons from the conduction band of diamond can be easily emitted into vacuum under applied bias. However, the wide band gap nature of diamond limits the amount of electrons present in the conduction band, unless n-type doping is performed. In order to have emission happen, electrons must be injected from metal-contact into the conduction band of diamond. This requires a high electric field since the potential barrier at metal-diamond interface would be as high as the work function of silicon or metals, which is then contradictory to the fact of low field electron emission from diamond. Therefore, the basic energy band diagram as described is inadequate for the explanation of the observed low field emission from diamond.

The low electron affinity property of diamond surfaces is important and can make diamond an efficient emitter; nevertheless, it is insufficient by simply invoking this property to explain the corresponding good field emission behavior. The low electron affinity is advantageous in lowering the surface potential barrier for electron emission only when the energy levels of some occupied states or bands are positioned sufficiently close to the conduction band minimum in diamond. In order to make field emission occur and sustain, there must be a continuous supply of electrons and a sustainable electron transport mechanism through diamond-metal interface and the bulk diamond film to reach the emitting surface. Besides, the energy levels of these electrons relative to the vacuum level are critical in determining the threshold field required for emission. Thus, it requires a better comprehension of the carrier transport principles for electrons tunneling through diamond-metal interface and drifting in the bulk of diamond film to better explain the field emission mechanism from diamond. Moreover, a more complete energy band structure, which takes the effect of defects and grain boundaries in polycrystalline diamond into consideration, is also required to be understood. So far, many experimental and theoretical studies have been performed and proposed, discussing field emission mechanisms from diamond, carrier transport principles through the diamond bulk and field emission enhancement models for various types of diamond emitters. The following section summarizes some of the important proposed theories and models.

2.3.2 Electron field emission mechanisms

(i) Simple field enhancement model

Most arguments cite the classical field enhancement theory by considering local field enhancements on sharp morphological features protruding on the diamond surface, similar to what is mentioned in **Section 2.2** for the sharp cone structural “Spindt cathode”, attributing the enhanced emission performance to the field enhancement at high curvature regions. As the applied potential between anode and cathode is fixed, the electric field at the apex of micropatterned diamond microtips is enhanced due to sharp microstructure, resulting in the increase of electron tunneling probability [9,61,126]. Therefore, field emission from diamond microtip emitters exhibits significant enhancement both in total emission current and stability compared to planar diamond emitters. The enhancement can be described by a factor defined as the geometrical field enhancement factor β which depends only on the shape of the microstructure.

Figure 2.6 shows many different geometrical shapes of field emitters, ranging from rounded whisker to wide-angle pyramid. In order to compare field emission characteristics of these various emitters, the figure of merit (f) based on the concept of maximizing the emission current while minimizing the applied voltage and the dimension of an array of field emitters is defined as [9]:

$$f_i = \left(\frac{I_i}{I_o}\right) \cdot \left(\frac{V_i}{V_o}\right)^{-1} \cdot \left(\frac{L_i}{L_o}\right)^{-1} \tag{2.9}$$

where I_i, V_i and L_i are emission current, applied voltage, and linear device dimension of the ith field emitter, while I_o, V_o, L_o are the same parameters of an ideal field emitter, respectively. The f for various shapes have been estimated and shown in the figure. It can be primarily concluded that the rounded whisker shape is the closest form to the ideal field emitter, which is a floating sphere, whereas the wide-angle pyramidal shape is a poor field emitter even though its thermal and mechanical stability is excellent.

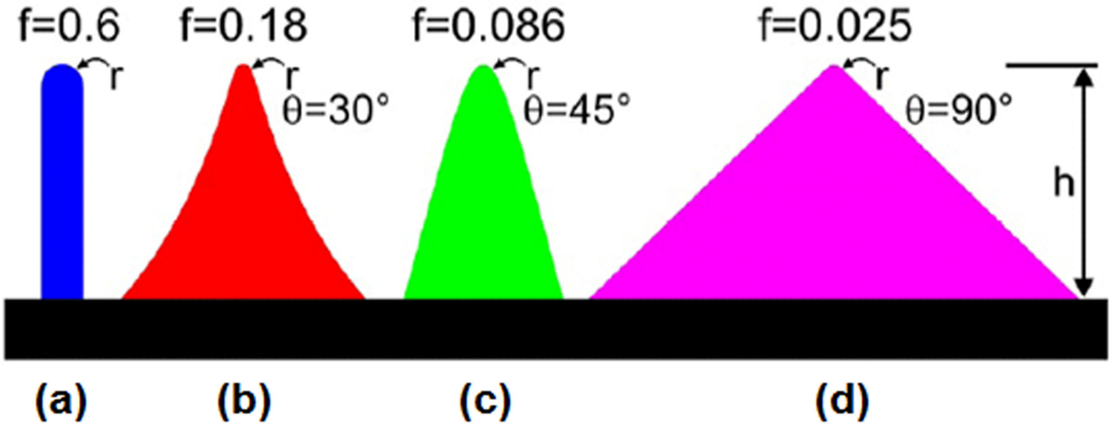


Figure 2.6 Various shapes of field emitters and their figures of merit: (a) rounded whisker, (b) sharpened pyramid, (c) hemi-spheroid, and (d) pyramid [9].

With an applied potential *V* across the vacuum gap *d* between top anode and ground, the electric field distribution at the surface of a sphere as shown in **Figrue 2.7(a)** can be calculated based on elementary electrostatic theory and expressed in closed form as a function of polar angle θ [9], described as:

$$E = \left(\frac{V}{d}\right)\left(\frac{h}{r} + 3\cos\theta\right) \tag{2.10}$$

$$\beta = \frac{h}{r} + 3\cos\theta \tag{2.11}$$

where *h* is the height of the sphere from the ground and *r* is the radius of the sphere. For $h >> r$, this gives $E \approx (h/r)(V/d)$ and $\beta \approx (h/r)$. It has been demonstrated that the electric field at the apex of a rounded whisker shape is approximately equal to that of a floating sphere [127], as shown in **Figure 2.7(b)**. Thus, ideally, the field at the apex of a rounded whisker shape is approximately equal to that of a floating sphere, given by $E = \beta(V/d)$ where $\beta = (h/r)$.

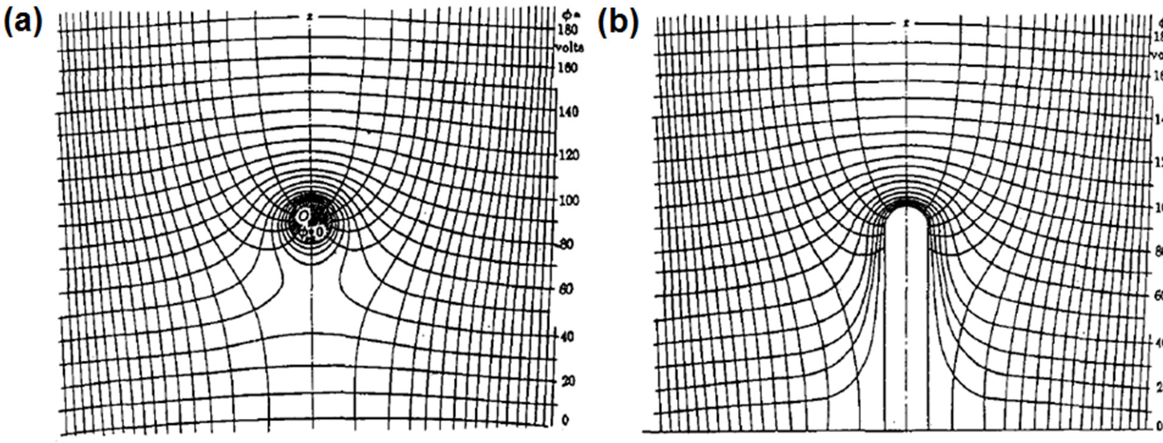


Figure 2.7 The electric field distribution at the surface of ideal shapes for field emitters. (a) floating sphere, and (b) rounded whisker [9].

(ii) Two step field enhancement (TSFE) model

In reality, on the surface of diamond, there are a number of small ultrasharp protrusions which act as tiny tips and should be taken into consideration for field emission. Hence, the simple field enhancement model is modified to account for the complicated morphology of diamond surface. The TSFE model was proposed to analyze the electron emission from diamond coated silicon field emitters, showing good agreement with experimental data [126]. Assuming the emitting tip with height h_1 and sharpness of radius r_1 possesses a number of tiny tips with height h_2 and radius of curvature r_2, as shown in **Figure 2.8**, the corresponding electric fields on the blunt tip (E_1) and at the apex of protrusions (E_2) are respectively expressed by the following equations:

$$E_1 = \left(\frac{h_1}{r_1}\right)\left(\frac{V}{d}\right) \tag{2.12}$$

$$E_2 = \left(\frac{h_2}{r_2}\right)E_1 = \left(\frac{h_1 h_2}{r_1 r_2}\right)\left(\frac{V}{d}\right). \tag{2.13}$$

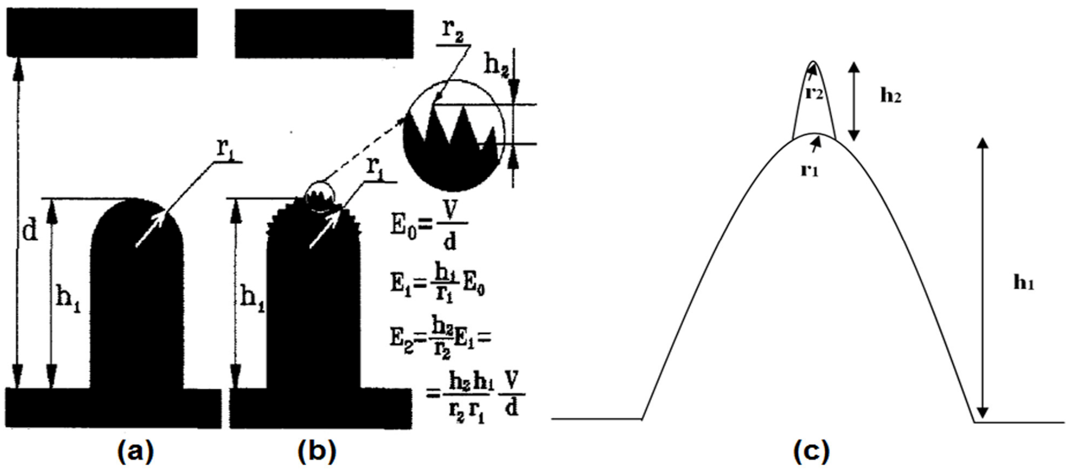


Figure 2.8 Geometry of emitters: (a) The simple field enhancement approach, (b) The TSFE approach [126], and (c) TSFE approach applied to the sharpened pyramidal diamond microtip [128].

This model has also been well applied to explain the increase in the geometrical field enhancement of the sharpened pyramidal diamond microtip [93,102,128], which consists of a large pyramid with an ultrasharpended tip sitting on its top, as shown in **Figure 2.8(c)**. The heights of the large pyramid and ultrasharpended tip are h_1 and h_2, while their corresponding tip radius of curvatures are r_1 and r_2. Based on the TSFE model, the electric field at the sharpened tip apex arises from the two-cascaded tip structure. The first step of field enhancement takes place near the apex of the large pyramid with an enhancement factor of h_1/r_1 from the planar base. The second step is the field enhancement at the apex of the ultrasharpended tip with an enhancement factor of h_2/r_2 from the top of the pyramid. The resultant geometrical field enhancement factor of the cascaded tip structure is then equal to:

$$\beta_g = \left(\frac{h_1}{r_1}\right)\left(\frac{h_2}{r_2}\right). \tag{2.14}$$

The estimated geometrical field enhancement factor using the TSFE model was found to be consistent with the result obtained from F-N analysis [93,126], suggesting this model can be used to explain the enhanced emission characteristics of diamond microtips. Nevertheless, the sustainable carrier transport mechanism for electrons to reach the emitting surface and the continuous supply of electrons in the wide-bandgap diamond material still needed to be addressed.

(iii) Surface work function lowering

It is believed that the work function of emitting surfaces can be reduced by surface coating with low work function materials, surface adsorption of atoms, or surface treatment. For example, Givargizov et al. reported a significant electron field emission enhancement from diamond coated silicon tips in 1995 [126], which could be attributed to the lowering of the surface work function by diamond. The calculated results from F-N plots using slope and intersection method showed well agreement with experimental data. But it is unclear how diamond could have sufficient amount of electrons in or near the conduction band to produce large emission currents without n-type doping and how the electrons could transport to the emitting surfaces. It was speculated that the emission might occur from surface states below the conduction band and the conduction channels might be formed through grain boundaries for providing sufficient electrons for emission [126,129,130]. These two mechanisms will be further discussed in the following subsections.

It has been found that the diamond surface work function can be lowered by coating with a low work function material such as Cesium (Cs) [60,131]. In addition, it has also been found that the lithium-doped and nitrogen-doped diamond exhibited enhanced electron field emission behavior after the surface treatment with O_2 plasma and

Cs deposition [59]. It has been suggested that this emission enhancement is attributed to the formation of a diamond-O-Cs surface, obtained by the reaction of Cs with oxygen-terminated diamond surface, which lowers the surface work function of diamond. The work function lowering of diamond surface by Cs was proposed to be attributed to the dipole formation due to electron rearrangement within the surface region [131]. However, since Cs is an expensive and reactive element, the work function lowering by Cs treatment for field emission enhancement is not a practical technique.

Hydrogen treatment on diamond surfaces was also found to improve field emission performance significantly [64,118]. It was believed that the work function lowering of diamond surfaces is the most presumable mechanism for the observed field emission enhancement. The hydrogen termination on diamond surface is known to form a positive surface dipole which could produce downward band bending and result in lowering of electron affinity and work function of diamond surfaces. Oxygen treatment, on the other hand, was found to degrade field emission characteristics, which was believed to be due to the increasing of surface work function of diamond [122,132]. The oxygen termination on diamond surfaces forms a negative surface dipole to produce upward band bending, thereby leading to increasing of electron affinity and work function of diamond surfaces.

(iv) Defect/impurity theory

It has been speculated that there exist defect/impurity states located within the energy band gap of diamond and the corresponding defect-induced energy bands are responsible for the enhanced field emission from diamond [59,129,133,134]. Defects in

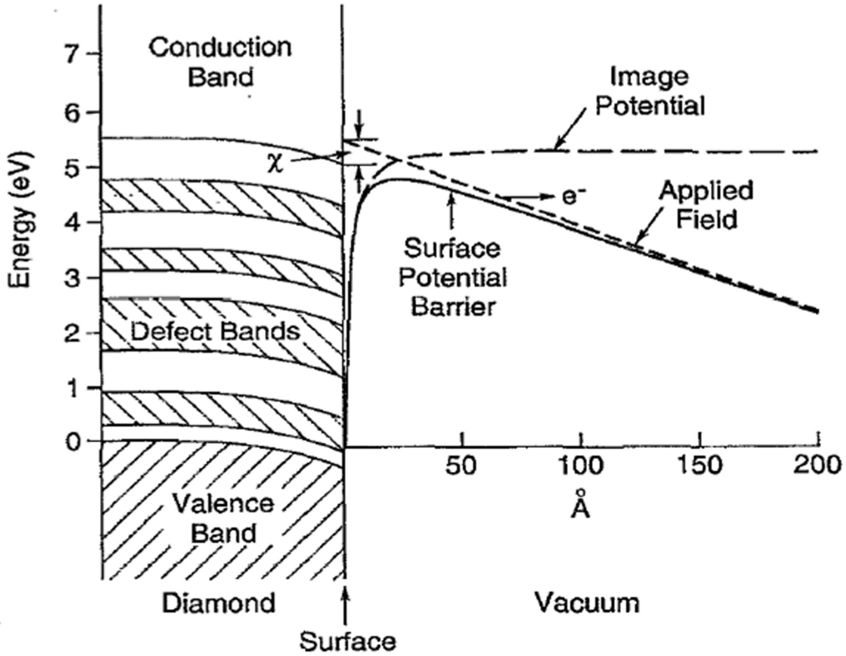


Figure 2.9 A schematic energy band diagram showing the presence of defect-induced energy bands within the band gap of diamond with a positive electron affinity under forward bias [133].

diamond such as vacancies, grain boundaries, dislocations and second phases such as graphite and amorphous carbon components, have been observed [134]. If the number of defects/impurities is significant, the electron states in these defects could interact and form energy bands in the bulk energy band gap as illustrated in **Figure 2.9** [133]. When these energy bands are wide enough or closely spaced, the electron hopping within the bands or excitation from the valence band could easily provide a steady flow of electrons to the emitting surface, sustaining stable emission of electrons into vacuum. The electrons from these defect-induced energy bands can either be excited into the conduction band or unoccupied surfaces states to emit, or tunnel directly into vacuum. The formation of these energy bands essentially raises the Fermi level up and provides energy states as donors in the diamond, and thereby reduces the efficient energy barrier that electrons must tunnel through. This theory is supported by overwhelming experimental data indicating that defective or lower quality diamonds have better emission properties. Additionally, it also appears to explain the enhanced emission performance from many "doped" diamond films, not necessarily because of the electrical doping effect, but rather by the creation of structural damages and defects during the doping process [134,135]. For example, it was found that the threshold electric field reduces rapidly as the implantation dose increases. And it was also found that the implantation of Si^+ ions causes more enhanced emission behavior than the implantation of C^+ ions since bigger Si atomic ions create more structural defects.

(v) Role of sp^2-carbon content in the diamond film

There have been a number of discussions in regard to the presence of graphite in the diamond matrix for electron emission enhancement. Robertson proposed that electrons would emit from the surface of sp^2 bonded grain boundaries where a strong downward band bending and high local field occur [66]. Silva et al. proposed that in a high sp^2 content diamond film, the localized field enhancement is resulted from the dielectric mismatch between the conductive sp^2 clusters and the insulating sp^3 matrix near the surface, the local arrangement of the sp^2 clusters and the ability of electrons to hop from one cluster to the next [68,136]. Athwal et al., and Xu and Latham suggested a field-induced hot electron emission process from isolated graphitic inclusions in diamond, citing an antenna effect that leads to field concentrations on a "floating" conductive graphite particle embedded in an insulative diamond matrix [137,138]. This model is based on the observation that active emission sites correspond to discrete location of defects or graphite inclusions on the diamond surface [56,139,140]. To sustain a continuous flow of emitting electrons, it has been assumed to be supplied to the emitting surface through conduction channels formed in diamond via an electroforming process at high electric fields [102,141,142]. Grain boundaries in diamond films [143] and hydrogenated diamond surfaces [144] have been suggested to function as conduction channels.

Wisitsorat-at proposed a complete diamond field emission mechanism for micro-patterned pyramidal diamond tips [65,67,102], describing the electrons transport from the back metal contact to the diamond-emitting surface. The model takes into consideration electrons tunneling through the potential barrier at the metal-diamond interface into diamond, the subsequent electron transport through the bulk diamond layer, and the final tunneling of electrons through a small potential barrier at the diamond-vacuum interface into vacuum. The detailed energy band diagram and electric field consideration of the proposed model were described with the inclusion of *sp*^{2} graphitic content in the *sp*^{3} diamond matrix that forms a series of cascaded *sp*^{2}-diamond-*sp*^{2} (metal-insulator-metal (MIM)) nanostructures that enhance a localized electric field around the *sp*^{2} particle induced by external applied voltage. This locally enhanced electric field distribution owing to the inclusion of isolated conducting *sp*^{2} nano-particles augments the electric field inside the diamond film and thereby increases the field enhancement factor. The image effect at the diamond-*sp*^{2} interface causes the energy band bending in the conduction band of diamond and thus reduces significantly the width of electron tunneling distance (W) at the metal-diamond interface, as illustrated in **Figure 2.10**. This increases the electron tunneling probability through the metal-diamond interface, facilitating the electrons tunneling into the conduction band of diamond. The electrons in the conduction band of diamond are then accelerated toward the next floating sp^2 particle under the locally induced electric field. As the sp^2 particle density is sufficiently high, the electrons would be able to transport through the bulk layer to reach the emitting surface via the conducting channel formed by the series of cascaded sp^2-diamond-sp^2 MIM nanostructures. Therefore, the inclusion of sp^2 graphitic content in the sp^3 diamond can facilitate electron tunneling through the potential barrier at metal-diamond interface and subsequent electron transport through the bulk diamond to emitting surface, enhancing diamond field emission.

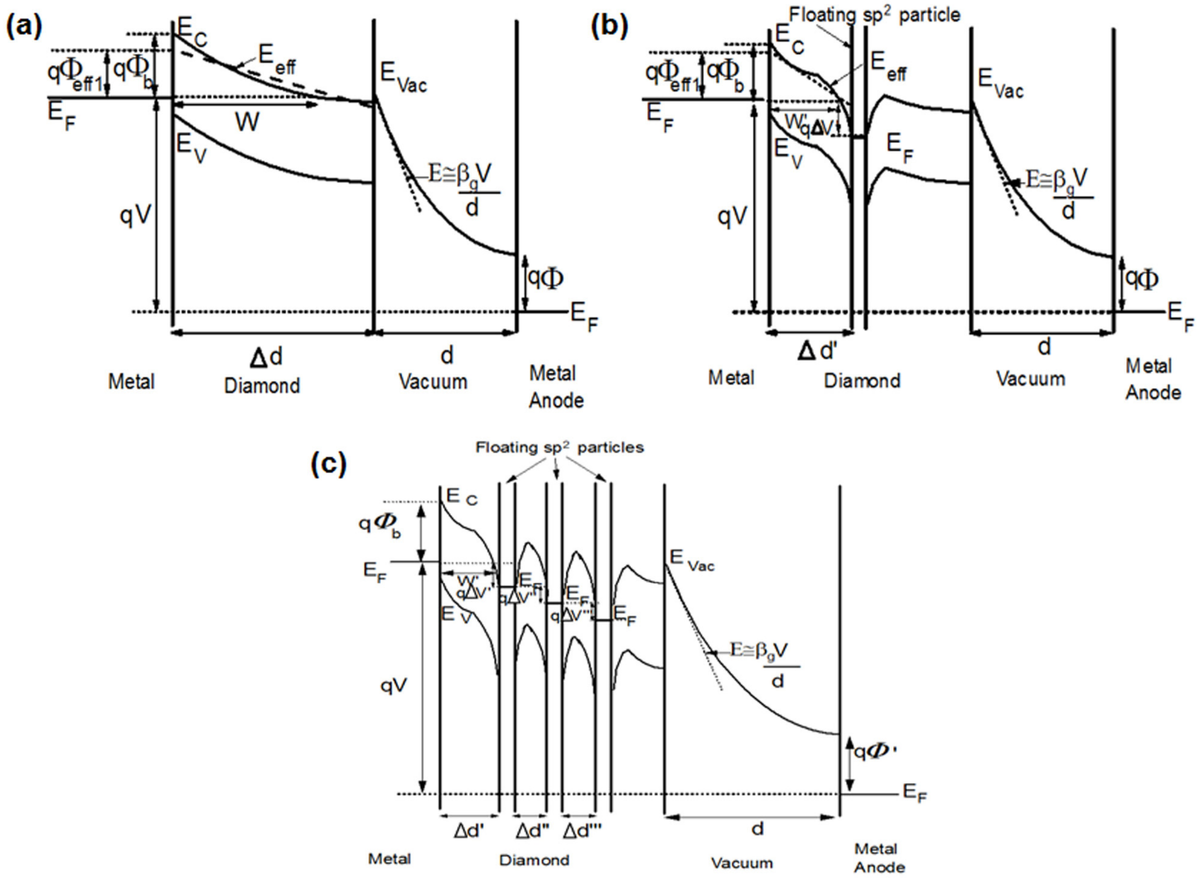


Figure 2.10 Energy band diagrams for MIM microstructure model: (a) electron transport through bulk diamond without sp^2-carbon, (b) field enhancement due to the presence of sp^2-carbon in diamond film, and (c) field enhancement via a series of sp^2-carbons embedded in diamond, providing an electron conduction channel [102].

Moreover, a systematic study to verify the enhanced field emission mechanisms responsible for the diamond emission was conducted. The analysis of the field emission data confirmed the usefulness of the model [67]. Similarly, Cui et al. concluded from their photoelectron sub-bandgap emission study that the diamond phases provide a thermally and mechanically stable matrix with a comparatively low work function, while graphitic phases provide the transport path for electrons to reach the surface and emit [125].

Recently, Ghosh proposed a modified electron transport mechanism for the n-type nanocrystalline diamond film [145] using the energy band diagram of cascaded MIM nanostructures in n-type nanodiamond with localized shallow trap level lying below the conduction band, as shown in **Figure 2.11**. For simplicity, the figure has been drawn under the assumption of (i) equal grain size throughout the film, (ii) uniform distribution of trap density (N_t) in the film and (iii) partially occupied trap levels under thermal equilibrium without external biasing or other forms of stimulation. At forward bias, the cascaded MIM structure forms a conduction channel consists of sp^2 floating particles allowing electrons to tunnel through sp^3-diamond, as shown in **Figure 2.11**. A voltage drop, ΔV appears across each grain or sp^3 particle. Since the amount of excess electron concentration in the conduction band is less, the trap level remains partially occupied which causes negligible effect on the tunneling electrons. Thus, the emission behavior obeys F-N theory with negative slope.

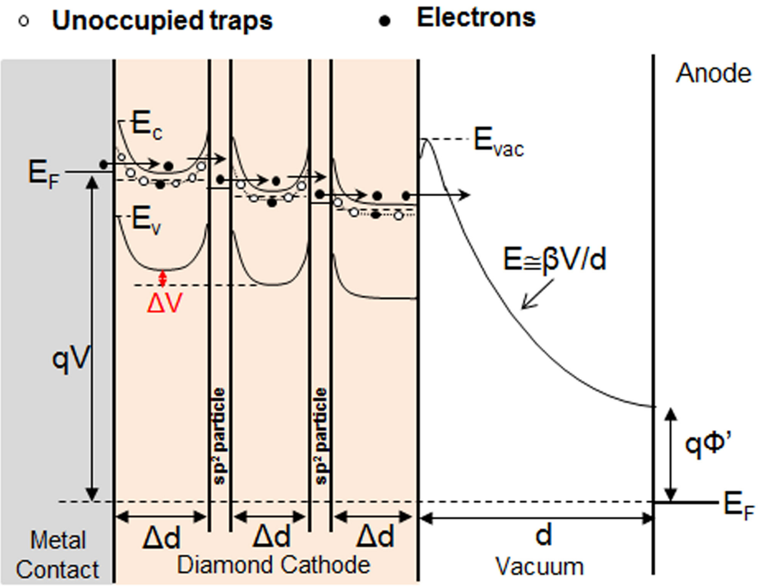


Figure 2.11 Energy band diagram of n-type nanocrystalline diamond film used to explain the electron transport via a series of *sp*^{2}-carbons embedded in diamond with localized shallow trap levels, providing an electron conduction channel [145].

(vi) Field emission enhancement via doping

The minimum electron energy in the conduction band of diamond is close to the minimum electron energy in vacuum, i.e. diamond possesses a low electron affinity. Electrons can be easily emitted into vacuum if they can reach the conduction band of emitting surfaces. However, because of the wide energy band gap property, unless there is a substantial electron source in the conduction band or in a sub-band within the energy band gap, the property of low electron affinity has no practical application. If the conduction band of diamond, with small electron affinity, can be directly populated with electrons via donors, a very small electric field is sufficient to induce electron emission.

Generally in practice, the carrier concentration of a semiconductor can be altered by dopants. Adding p-type acceptor impurities into diamond would increase the holes concentration in the valance and enhance the bulk electrical conductivity. On the other hand, the addition of n-type donor impurities into diamond would increase the electron concentration in the conduction band and improve electron emission. Even though introducing impurities especially donors into diamond is difficult since diamond is a wide band gap material with very tight lattice structure, diamond film doped with various n-type dopants such as phosphorous (P) and nitrogen (N) has been reported by direct ion implantation or *in situ* doping techniques [59,63,69,146–148]. Ion implantation is the first successful method to introduce n-type dopants into diamond [146]. Nitrogen and phosphorous have been successfully incorporated into CVD diamond films by the addition of various dopant gases such as nitrogen (N_2), ammonia (NH_3), urea ($(NH_3)_2CO$), and phosphine (PH_3) into CH_4/H_2 plasma [63,69,147,148]. It has been reported that nitrogen-incorporated nanocrystalline diamond film with high nitrogen concentration of $2x10^{20}$ atoms/cm^3 and high electrical conductivity of ~100 $\Omega^{-1}cm^{-1}$ was achieved using plasma-enhanced CVD technique by adding N_2 gas in CH_4/Ar gas mixture [87,149,150].

The high concentration of n-type donor impurities and their related defect energy bands, as illustrated in **Figure 2.12**, are beneficial for electron field emission. The energy levels associated with Li and P dopants are still unknown, but it has been found that the substitutional nitrogen forms a donor level ~ 1.7 eV below the conduction band [102]. Assuming an NEA property on the diamond surface, the minimum energy state in vacuum is lower than the minimum energy state in the conduction band by ~ 0.7 eV. Consequently, the energy barrier between the nitrogen donor level and the minimum of vacuum energy level is 1 eV, which means that the work function is approximately 1 eV. As a result of reducing the surface energy barrier by N-dopants, electrons from the nitrogen donor states can more easily tunnel into vacuum by the influence of a low electric field. The effect of n-type doping on electron emission enhancement has been independently confirmed by experiments using P and N as donors, showing better emission characteristics than p-type (boron-doped) diamond emitters [63,151]. Furthermore, the N-doped diamond film with a surface treatment of O_2 plasma and Cs deposition has shown emission at fields as low as 0.2 V/μm [59], the lowest reported value to date. In this study, n-type dopant (nitrogen) incorporated nanodiamond film developed by Vanderbilt [128] has been employed to achieve enhanced electron field emission.

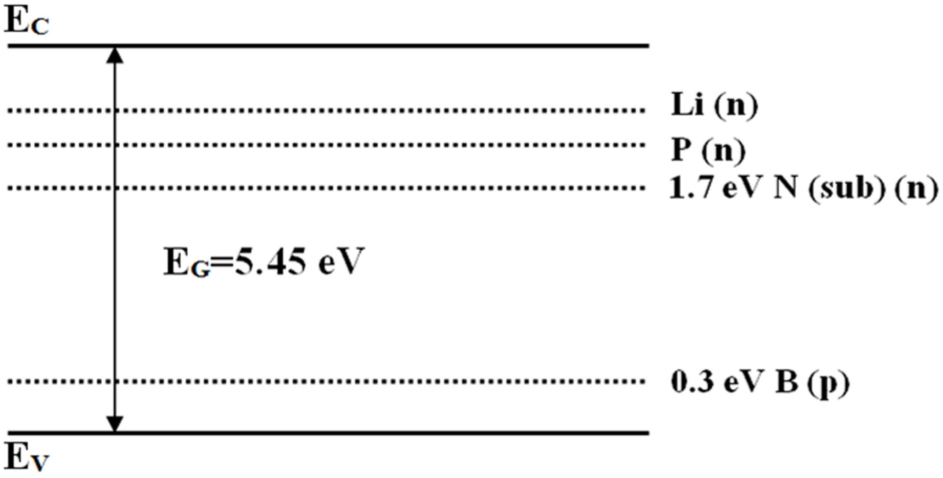


Figure 2.12 Energy band of diamond showing the energy levels of dopants Li, P, N and B [102].

(vii) Other interesting models

There are many other conduction models and mechanisms proposed for carrier transport through the diamond bulk, including electron injection over a Schottky barrier at the back-contact interface between a metallic substrate and diamond as the controlling mechanism [152], field concentrations induced by chemical inhomogeneity (such as hydrogen termination) on the surface [144], dielectric breakdown that provides conductive channels in diamond [142], surface arcing that causes surface roughness and thus provide additional geometric field enhancement [153], and space charge limited conduction current through the bulk of the diamond [154]. But neither of these mechanisms is necessarily mutually exclusive, because each discusses a particular part of an overall complex field emission process that includes the critical steps of supplying sufficient electrons to diamond, transporting them through the bulk of diamond to the emitting surface, and emitting them into vacuum.

2.4 Operation principles of VFE devices

2.4.1 Two-electrode VFE device and diode characteristics

The vacuum field emission diode is the most fundamental form of vacuum devices with a simple structure of two electrodes, anode and cathode, as shown in the schematic diagram of **Figure 2.13(a)** along with its circuit symbol in **Figure 2.13(b)**. The anode and cathode are separated by a vacuum gap as a medium for electron transport. Normally, the cathode is made of low work function materials and/or with sharp structures for electron emission at low electric field; while the anode is made of high work function material such as metal and silicon with planar structure, which prevents electron emission from anode to cathode under reverse bias.

In general, the electron emission from cathode is induced by the electric field resulted from the positive voltage applied to the anode with respect to the cathode. Under forward bias, as the anode voltage is sufficiently high to thin down the potential barrier at the interface between cathode and vacuum, electrons can emit into vacuum via quantum-mechanical tunneling through the potential barrier. The emitted electrons are then

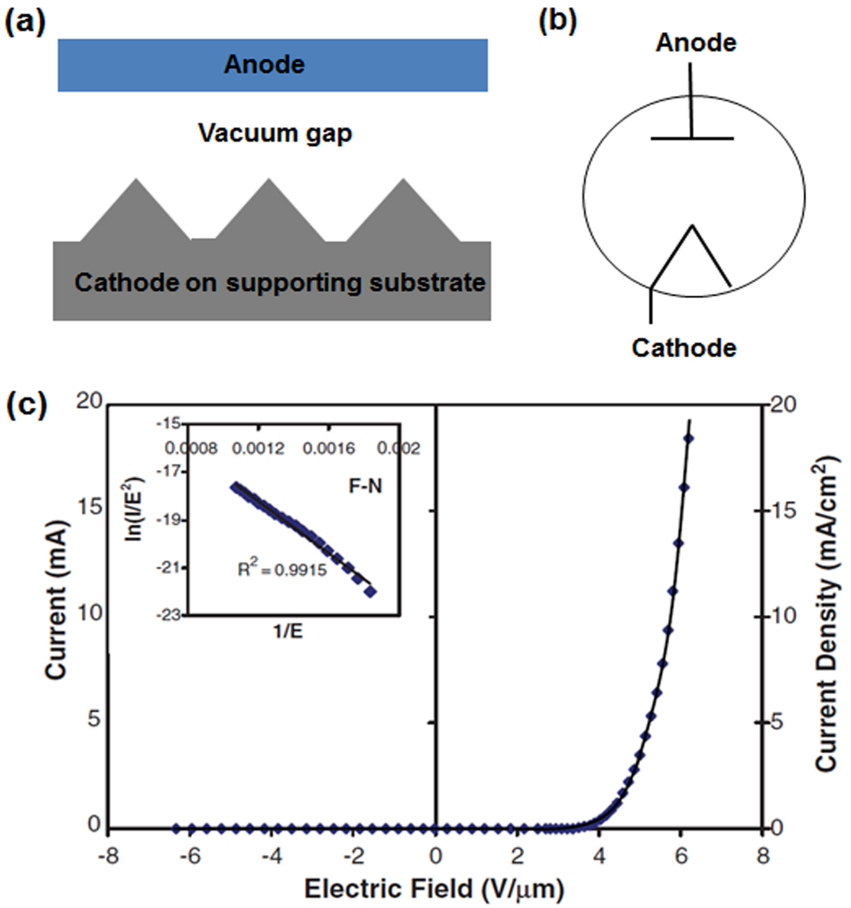


Figure 2.13 (a) Schematic diagram of a typical vacuum field emission diode, (b) circuit symbol of a VFE diode, and (c) typical VFE diode I-V characteristic with a rectifying feature [93].

accelerated by the positive anode potential and collected at the anode, forming the emission current flowing from cathode to anode. According to the Fowler-Nordhiem theory [103–105], the emission current increases exponentially with the applied anode voltage. Under reverse bias where a negative voltage is applied to the anode with respect to the cathode, electrons may emit from anode into vacuum but it requires a very high electric field due to high work function and planar anode structure. The reverse breakdown field and voltage depend on the anode-to-cathode spacing, type of anode, and condition of anode surface [155]. Thus, in normal operation, the current is zero at low electric field under reverse bias. Therefore, VFE diode has a rectifying current-voltage behavior [102], as shown in a typical I-V characteristic of a VFE diode in **Figure 2.13(c)**. Its corresponding F-N plot of Ln(I/V^2) versus 1/V as shown in the inset exhibits a linear feature with a negative slope, conforming to F-N theory.

2.4.2 Three-electrode VFE devices with transistor and triode characteristics

A three-electrode vacuum field emission device, which can be implemented in triode and transistor configulations, has a simple device structure consisted of cathode, anode, and gate as shown in the schematic diagram of **Figure 2.14(a)** along with its circuit symbol in **Figure 2.14(b)**. The cathode and anode have been described previously in the field emission diode, whereas the third electrode serving as the gate is placed in between the cathode and anode in the form of a suitable mesh, screen, or circular flat structure. The gate electrode is often referred as the control electrode. The emission current flowing from the cathode must pass through the gate opening to the anode. Since the gate normally lies closer to the electron-emitting cathode, a small potential applied to the gate is sufficient to produce a large electric field on the emitter and thereby efficiently control the emission current due to the proximity between gate and cathode. Therefore, the three-electrode VFE devices are useful for signal detection, amplification, processing and conditioning as well as for the generation of oscillations [102].

The electrical characteristics of a three-electrode VFE device conform to the Fowler-Nordheim theory which describes the relationship between the emission current and electric field as discussed in **Section 2.2**. In three-electrode configuration, the total electric field (E_t) at the cathode consists of two components. They are the electric field produced by the gate voltage (V_g) and the stray electric field acting through the gate opening by the anode voltage (V_a) [156]. Accordingly, the total electric field depends upon many factors such as gate-cathode spacing, anode-cathode spacing, and gate geometry. In general, the total resultant electric field on the cathode, as the combined effect of gate and anode potentials, can be expressed as:

$$E_t = \frac{\left(V_g + V_0 + \gamma V_a\right)}{d_g} \tag{2.15}$$

where d_g is the gate-cathode spacing, V_0 is the contact difference potential between gate and cathode, and γ is a coefficient transferring V_a to an equivalent stray potential γV_a associated with the screening of gate structure. The value of γ ranges from 0 to 1, and it can be calculated from the electrostatic theory for simple geometrical design by simulating the device structure. But in practice, it depends not only on the gate geometry but also on the gate and anode voltages because the potentials on gate and anode also affect the effectiveness of gate in shielding anode field, making the calculation based on electrostatic theory more complicated. Alternatively, the γ of a three-electrode VFE device can be determined from the device coefficient extracted from the measured electrical characteristics. Details of this will be addressed in Chapter VI.

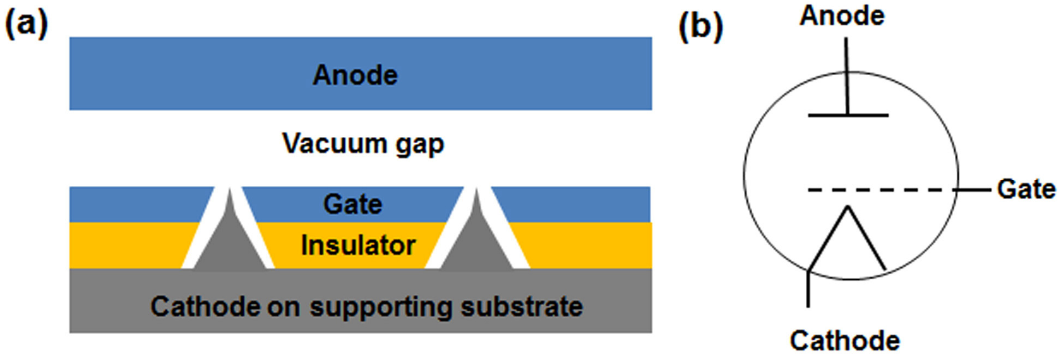


Figure 2.14 (a) Schematic diagram of a typical three-electrode vacuum field emission device, and (b) its corresponding circuit symbol.

According to F-N equation, **Eq. (2.7)**, the total emission current (I_t) for a three-electrode VFE device can be modified and described as:

$$I_t = k_1 \frac{A\beta^2 \left(V_g + V_0 + \gamma V_a\right)^2}{t^2(y)\phi d_g^2} \exp\left(-k_2 \frac{v(y)\phi^{1.5} d_g}{\beta\left(V_g + V_0 + \gamma V_a\right)}\right). \tag{2.16}$$

The I_t from the cathode would be split into two components, anode current (I_a) and gate current (I_g). A transport factor α is defined to describe the fraction of the anode current to the total emission current [156]. Then the I_a and I_g are given by:

$$I_a = \alpha I_t = k_1 \frac{\alpha A\beta^2 \left(V_g + V_0 + \gamma V_a\right)^2}{t^2(y)\phi d_g^2} \exp\left(-k_2 \frac{v(y)\phi^{1.5} d_g}{\beta\left(V_g + V_0 + \gamma V_a\right)}\right) \tag{2.17}$$

$$I_g = (1-\alpha) I_t = k_1 \frac{(1-\alpha) A\beta^2 \left(V_g + V_0 + \gamma V_a\right)^2}{t^2(y)\phi d_g^2} \exp\left(-k_2 \frac{v(y)\phi^{1.5} d_g}{\beta\left(V_g + V_0 + \gamma V_a\right)}\right). \tag{2.18}$$

The α factor is determined by several parameters including the relative value between anode and gate voltages and the gate-cathode and anode-cathode distances.

The electrical performance of a three-electrode VFE device can be determined by three important characteristic coefficients [32,102,156]: amplification factor (μ), gate-anode transconductance (g_m), and anode resistance (r_a). These coefficients are particularly useful for ac equivalent circuit modeling. First, μ is a measure of the effectiveness of gate voltage in controlling the anode current with respect to anode voltage, i.e. it is the ratio of the change in anode voltage due to a change in gate voltage at constant anode current. It determines the voltage gain of the device. Mathematically, it can be expressed as,

$$\mu = -\left.\frac{\partial V_a}{\partial V_g}\right|_{Ia=cons\tan t}. \tag{2.19}$$

Second, g_m characterizes the gate modulation on anode current at a selected operation condition. It is defined as the corresponding alternation of anode current due to a change of gate voltage at a given anode voltage. The g_m generally depends on the bias condition of gate and anode voltages. It determines the current driving capability, the voltage gain and frequency response of the device. Mathematically, g_m is defined as,

$$g_m = \left.\frac{\partial I_a}{\partial V_g}\right|_{Va=cons\tan t} . \tag{2.20}$$

Third, r_a describes the corresponding variance of anode voltage to the infinitesimal change of anode current at a selected operation condition. It is a measure of the effectiveness of anode voltage in controlling the anode current at a given gate voltage. It also generally depends on gate and anode voltages. Mathematically, r_a is defined as,

$$r_a = \left.\frac{\partial V_a}{\partial I_a}\right|_{Vg=cons\tan t} . \tag{2.21}$$

The values of these three coefficients μ, g_m and r_a vary with the operating conditions. According to their definition, a useful relation exists among these coefficients, which is,

$$g_m \cdot r_a = \mu \tag{2.22}$$

for a given set of bias conditions.

There are two operating configulations in a three-electrode VFE device's construct [157]. One is the anode-induced field emission triode, where the field emission is initiated by the anode voltages while the total emission current from the cathode is modulated by the gate biases. The other is the gate-induced field emission transistor, in which the electron emission is triggered by the nearby gate voltage and collected by the relatively remote anode with relatively small influence on the total field at the cathode. The respective operation mechanism for each configulation is discussed in detail in the following.

(i) Anode-induced field emission triode characteristics

In this configulation, the function of anode and cathode for a VFE triode are basically the same as that of a vacuum diode, whereas the function of gate is to control the emission current. The electron emission from cathode is induced by the anode voltage and modulated by the close-by gate voltage [34,36,43,96,158,159]. The positive anode voltage, relative to the emitter, thins down the potential barrier at the emitter-vacuum interface and extracts electrons emitted from the cathode to the anode, while the gate voltage modulates the net electric field on the cathode and modifies the corresponding equipotential distribution, and thereby controls the electron tunneling probability and total emission current from the cathode. If the gate is made slightly positive with respect to the cathode, the gate significantly increases the electric field at the cathode, thus permitting the anode to draw a larger emission current. On the other hand, if the gate is made negative with respect to the cathode, the negative electric field of the gate significantly reduces the electric field at the cathode, resulting in a smaller emission current.

The anode electrode in this configulation, usually placed close to the cathode, has a relatively larger influence on the field emission. Thus, the corresponding γ is non-negligible. For $V_g = 0$ V, the field emission behavior of a triode is the same as that of a diode. Upon emission occurs, as the anode voltage exceeds the threshold voltage, all the emitting electrons are collected by the anode, i.e. $\alpha = 1$, since the anode is positive biased while the gate is still grounded. In I_a-V_a characteristics, the anode current is an exponential function of anode voltage. For $V_g > 0$ V, more electrons are emitted from the cathode at a given anode voltage. In this case, α has a value between 0 and 1. In general,

V_g is much smaller than V_a in triode mode, and therefore most of the emitting electrons are still collected at the anode, i.e. $\alpha \approx 1$. The I_a-V_a characteristic at positive V_g bias would show similar exponential feature with reduced anode threshold voltage. If $V_g < 0$ V, the emission current decreases at a given anode voltage. In this case, α is clearly equal to unity. But the I_a-V_a characteristic at negative V_g bias would exhibit an increased anode threshold voltage. **Figure 2.15** shows the typical triode behavior of I_a-V_a-V_g characteristics from a silicon vacuum field emission device [36].

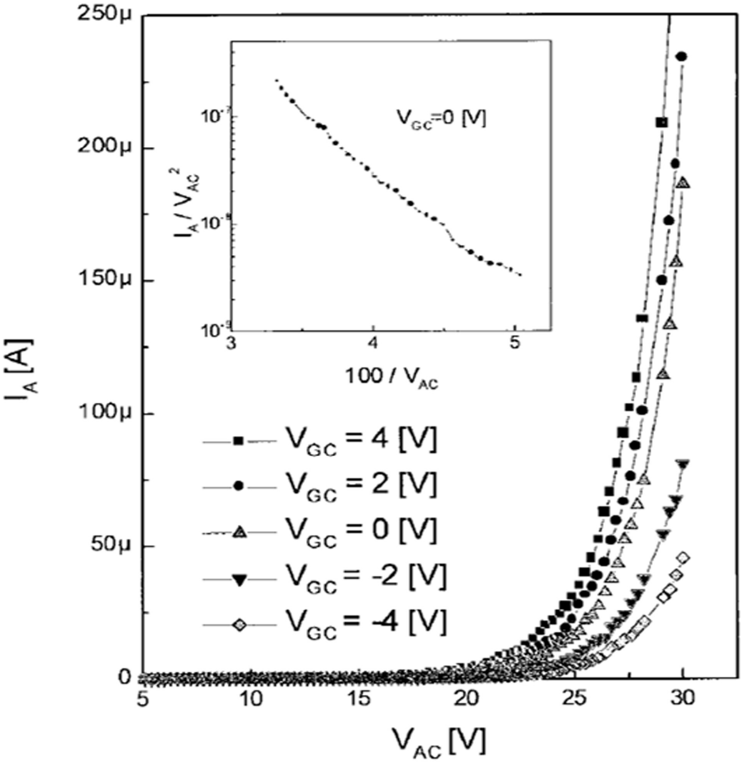


Figure 2.15 The I_a-V_a characteristics as a function of V_g and corresponding F-N plot at $V_g = 0$ V from a lateral silicon VFE device [36], illustrating the typical triode behavior of a three-electrode VFE device.

As operating in triode mode, the three-electrode VFE device generally possesses a modest voltage gain (low/medium μ) with low output resistance (low r_a). For signal amplification and processing, the triodes with these features can be suitable as buffer amplifiers in the output stage of electrical circuit blocks, providing low output impedance for avoiding signal distortion when connecting to a load [160,161], by isolating the input signal from the output signal without the need of feedback loops.

(ii) Gate-induced field emission transistor characteristics

In transistor configulation, the function of gate is to induce electron emission from the cathode and manipulate the total emission current, while the anode acts as a current collector [95,102,156,162,163]. The positive gate voltage, relative to the cathode, lowers the potential barrier between emitting surface and vacuum and extracts electrons emission into vacuum. The emitted electrons are then accelerated to move to the anode via a positive anode voltage with respect to the cathode. The anode is usually placed remotely from the cathode in this configulation, and thereby the anode voltage has a relatively small influence on the total electric field at the cathode. Consequently, the corresponding γ is close to zero and the contribution of V_a in the resultant electric field is negligible. On the other hand, the gate voltage has more effect on the total electric field due to its closer proximity to the cathode. Therefore, the emission current from the cathode depends mainly on the gate voltage but lesser on the anode voltage. If the gate voltage increases, the electric field at the cathode increases and thereby allows more electrons tunneling into vacuum, enhancing the emission current; and vice versa. But as the anode voltage increases, the total electric field at the cathode would scarcely raise and thereby the emission current would keep nearly invariant.

As the electron emission occurs, if V_a is much smaller than V_g, all emitting electrons are collected by the gate electrode and none of them reaches the anode, i.e. $\alpha =$

0. Since no anode current is detected, this stage is called the cutoff region. When V_a increases and becomes comparable to V_g, parts of the emitting electrons move to the anode and I_a starts to increase with V_a. At this stage, α has a value between 0 and 1, and the device is operating in the linear region. As V_a elevates further and becomes significantly higher than V_g, all of the emitting electrons from the cathode transit to the anode and I_a tends to saturate with V_a at a given V_g. In this case, $\alpha \approx 1$, and the device is operating in the saturation region where the anode current is mainly controlled by gate potential and nearly independent of anode potential. Therefore, three distinct regions (cutoff, linear, and saturation) will be observed in the I_a-V_a characteristics for a given family of gate voltages. **Figure 2.16** illustrates the typical transistor behavior of vacuum field emission devices, employing the I_a-V_a-V_g characteristics from a vertically configured carbon nanotube and a laterally configured nanodiamond emitter as examples [128,163].

When operating in transistor configulation, the three-electrode VFE device generally possesses a high voltage gain (high μ) and large output resistance (high r_a). The transistors with these features can be a favorable fundamental device providing high voltage gain for signal amplification in the electrical circuit blocks of signal processing [102,163]. Despite the large output impedance would limit the signal transfer to the load, it can be adjusted by connecting a buffer amplifier with low output impedance and modest voltage gain. The low/medium μ triode is a suitable buffer amplifier as described earlier. Therefore, the electronic circuits with desired voltage/power gain and minimal signal distortion can be achieved by using the high μ transistor for signal amplification and the low/medium μ triode as buffer amplifiers for better signal delivery with low noise.

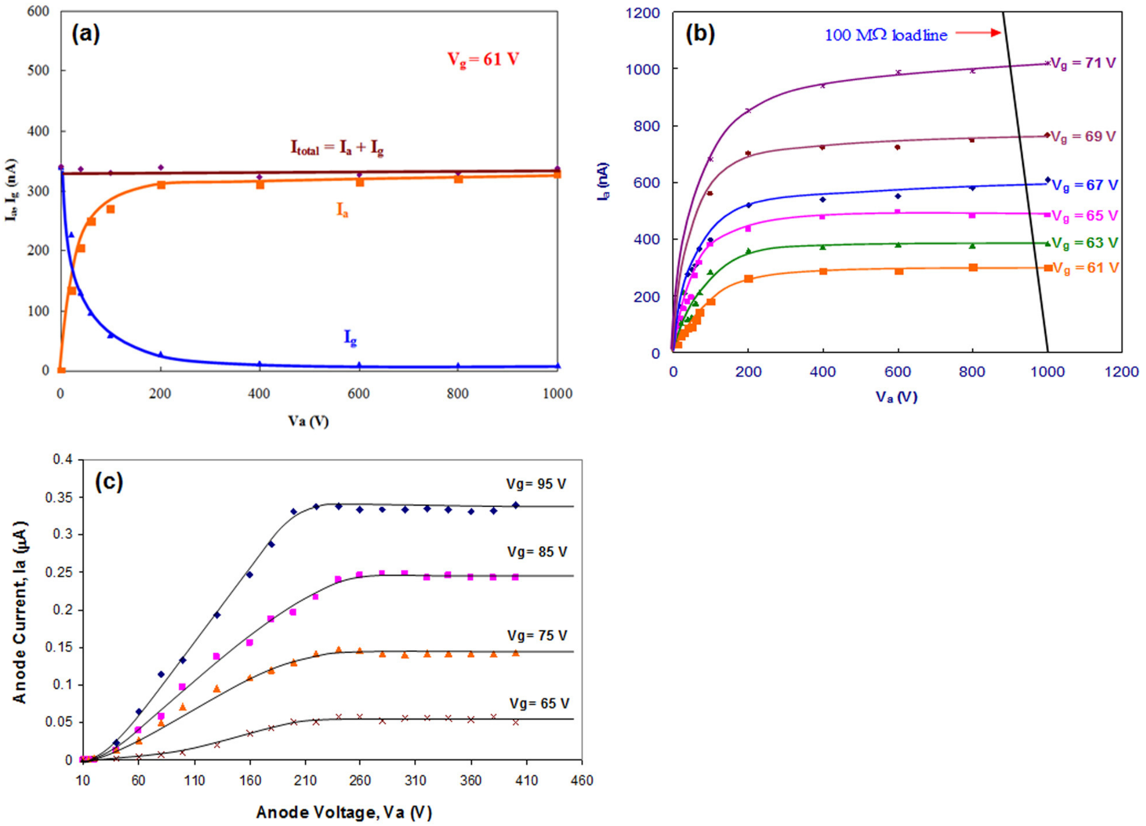


Figure 2.16 The I-V characteristics of VFE devices for demonstrating the typical transistor behavior. (a) I_a and I_g as a function of V_a at a given V_g and (b) the family plots of I_a-V_a at varied V_g biases obtained from a carbon nanotube VFE device [163]. (c) The I_a-V_a-V_g feature of a lateral nanodiamond VFE transistor [95].

2.4.3 VFE differential amplifier

In a single-ended amplifier, the bias point, voltage gain and impedance are sensitive to the interference resulting from power supply, capacitive coupling and ground noises. This would lead to signal distortion during signal transmission. In solid-state microelectronics, the differential amplifier (diff-amp) [161,164] has been developed in order to overcome these inherent drawbacks. It is known to be the most important circuit building block used in analog and mixed-signal integrated circuits (ICs). For instance, the input stage of an operational amplifier and the basic element of emitter-coupled high-speed logic [161,165] incorporate the diff-amp. A dual-triode configuration has also been developed in vacuum tube technology [163]. The device consists of an identical pair of triodes with well-matched electrical characteristics, sharing a common cathode with split gates and anodes, as illustrated in the schematic diagram of **Figure 2.17(a)** along with its circuit symbol in **Figure 2.17(b)**.

The diff-amp performance can be evaluated based on several figure of merits characterized by the common-mode voltage gain, differential-mode voltage gain and common-mode-rejection ratio (CMRR) [161,163,164]. The input and output small-signal voltages are defined to be v_{in1} and v_{out1} for transistor #1 and v_{in2} and v_{out2} for transistor #2. There are two modes for differential amplifier operation. First, in common-mode operation, the common-mode input voltage (v_{ic}) is the voltage applied to both input terminals of the diff-amp, namely,

$$v_{ic} = \frac{(v_{in1} + v_{in2})}{2}, \tag{2.23}$$

while the common-mode differential output voltage (v_{oc}) is defined as the voltage difference between two output terminals, that is,

$$v_{oc} = v_{out1} - v_{out2}. \tag{2.24}$$

The common-mode voltage gain (A_{cm}) is equal to v_{oc}/v_{ic}. Ideally, if the electrical characteristics of the triode pair are identical, then A_{cm} is zero. Second, in differential-mode operation, the differential-mode input voltage (v_{id}) is the voltage difference between the two input small-signal voltages, i.e.

$$v_{id} = v_{in1} - v_{in2}, \tag{2.25}$$

while the differential-mode output voltage (v_{od}), similar to common-mode, is the corresponding voltage difference between two output ends, expressed as

$$v_{od} = v_{out1} - v_{out2}\,. \tag{2.26}$$

The differential-mode voltage gain (A_{dm}) is defined as v_{od}/v_{id}. Ideally, a small differential input would result in a large differential output and thereby a large A_{dm}. Finally, the common-mode-rejection ratio, an important figure of merit for diff-amp, is determined by the absolute value of the ratio of differential-mode gain to common-mode gain, namely,

$$CMRR = \left| {}^{A_{dm}}\!/_{A_{cm}} \right|. \tag{2.27}$$

This value was utilized to evaluate the ability of a diff-amp in rejecting input noise common to both input terminals, particularly important when the signal of interest is contained in the voltage difference of inputs.

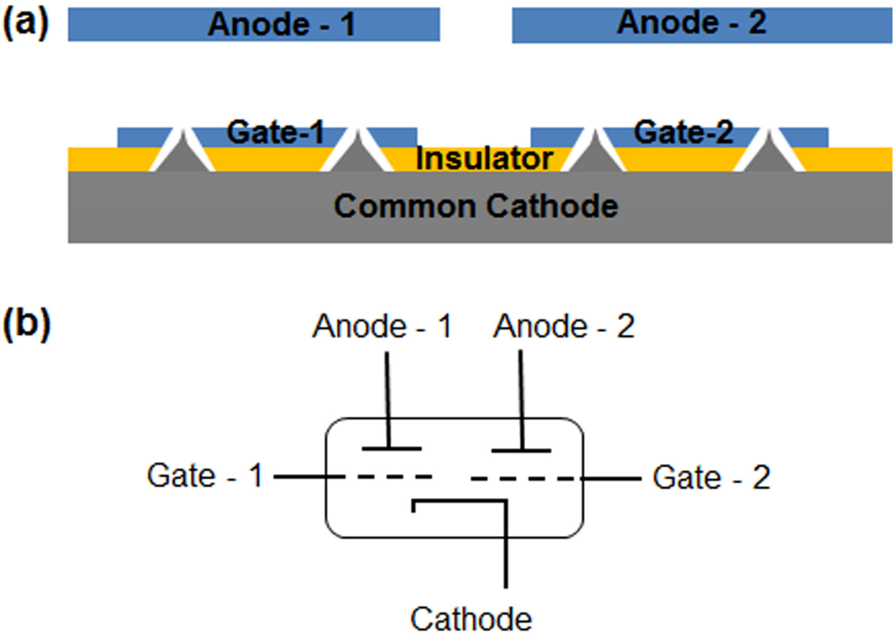


Figure 2.17 (a) Schematic diagram of a vacuum field emission differential amplifier, and (b) its corresponding circuit symbol.

Despite the concepts and modeling of vacuum ICs were proposed [18−20], only few practical implementations of VFE devices at the circuit level have been reported in the past due to the lack of reliable VFE devices, especially stable cathodes. It is until recently that Wong successfully developed a VFE diff-amp based on carbon nanotube emitters in 2006 [163], promoting VFE fundamental devices into vacuum ICs. One of the main objectives of this research is to develop a nanodiamond VFE integrated diff-amp employing the nitrogen-incorporated nanodiamond VFE transistors for better diff-amp behavior. The details of corresponding fabrication processes and electrical characteristics will be discussed in this dissertation.

CHAPTER III

NANOCRYSTALLINE DIAMOND

As this research oriented towards the development of promising VFE electronic devices utilizing CVD nanocrystalline diamond as the cold cathode material, it would be appropriate to dedicate a chapter to introduce the material. This chapter explains the underlying basic science and technology of CVD diamond and discusses the rapid advancements of CVD nanodiamond in a variety of micro/nanoelectronic applications owing to its unique features including small grain size, smooth surface morphology, sp^2-carbon inclusion within grain boundaries, high n-type conductivity, and capability of low temperature deposition. Following that, some of the recent developments and important results of diamond and nanodiamond field emission devices reported so far are presented.

3.1 Introduction of CVD diamond

Diamond is formed naturally when carbon atoms are arranged in the hybridized sp^3 tetrahedral structure under high temperature and high pressure conditions. Eight carbon atoms form a cubic unit cell as shown in **Figure 2.3(a)**. The lattice structure of diamond consists of two interpenetrating face centered cubic (fcc) lattices, displaced along the body diagonal of the cubic cell by one quarter the width of the unit cell in each dimension [111]. Diamond has the most extreme physical properties of any material, including the mechanical hardness, high thermal conductivity, low thermal expansion coefficient, optical transparency over a wide range of wavelength, good electrical insulation, biological compatibility and inertness to most chemical reagents [112]. Yet its scarcity and expense restrict the practical application of diamond in science and engineering.

The desire to exploit the superlative properties of diamond has led to the development of chemical vapor deposition techniques for depositing diamond thin films onto a variety of substrate materials [111−114]. **Figure 3.1** shows two of the common types of low pressure CVD reactors [111,166]. CVD involves a gas phase chemical reaction occurring above a solid surface, which causes deposition of a targeted material onto that surface. All CVD techniques for producing diamond films [112] require a means of activating gas phase carbon-containing (hydrocarbon) precursor molecules for diamond nucleation and further growth. The activation of hydrocarbon and hydrogen molecules is generally executed by thermal energy (hot filament CVD) or the electric discharge method (microwave plasma CVD). Methane (CH_4) diluted in excess of hydrogen, typically in a mixing volume ratio of 1% CH_4, is usually used for diamond growth. The mixed gaseous species gain energies via thermal decomposition in a hot filament system or via electron impact in plasma system, dissociating hydrogen and methane into atomic hydrogen and hydrocarbon radicals. The reactive radicals would adsorb on the substrate surface or diffuse around close to the surface until an appropriate active site is found, reacting with the substrate and forming nucleation sites on the surface for diamond growth. Carbon contained reactive radicals can collide and react with the nucleation or form other new nucleation sites, effectively adding carbon to the lattice. **Figure 3.2** illustrates the physical and chemical processes occurring during diamond CVD. Eventually, the nucleations collide and join together, forming a continuous film. When the growth conditions including the hydrocarbon and hydrogen gas ratio, substrate temperature, chamber pressure and activation energy, are appropriate, one possible outcome is diamond.

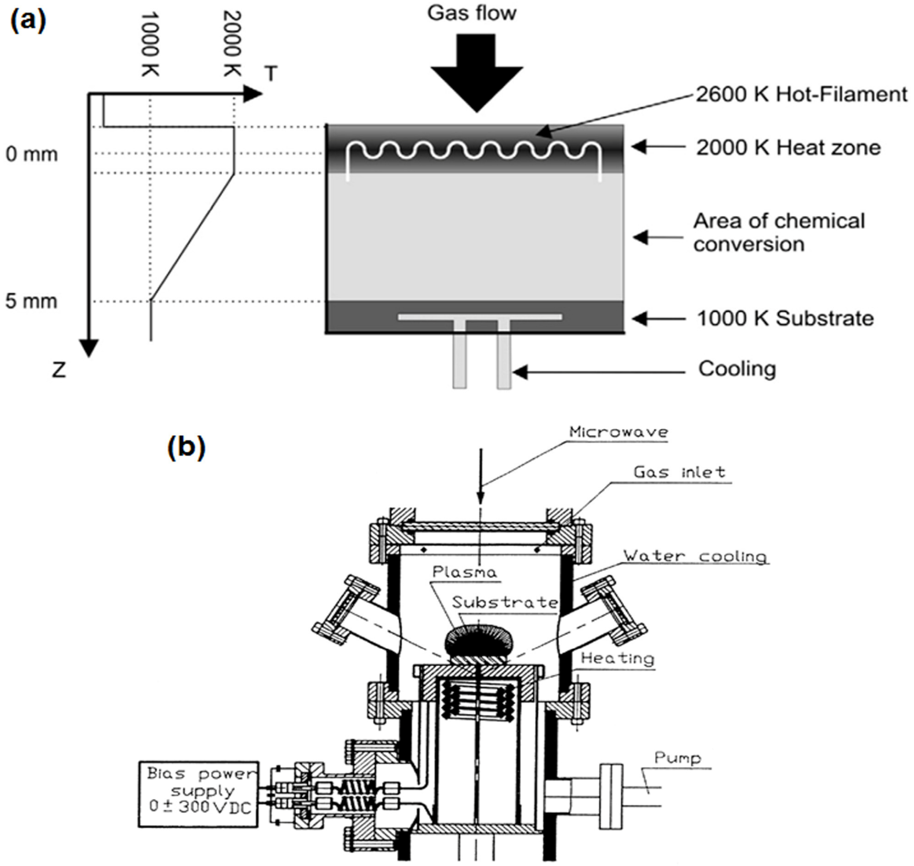


Figure 3.1 Schematic of (a) a hot filament CVD method [166] and (b) a microwave plasma-enhanced CVD reactor (ASTeX) [111].

It is believed that the atomic hydrogen plays an important role in the diamond growth process [111−114,166]. First, atomic hydrogen converts hydrocarbons into reactive radicals, a necessary precursor for diamond formation. Second, the presence of atomic hydrogen during the deposition process would lead to preferential etching of the amorphous carbon and graphite rather than diamond, reducing the impure mixed phases and improving the quality of diamond film. Third, atomic hydrogen stabilizes the diamond surface via termination of the surface dangling bonds by hydrogen and maintains the sp^3 hybridization configuration. Fourth, atomic hydrogen abstracts hydrogen from the hydrocarbons attached on the substrate surface and thereby creates active sites for adsorption of the diamond precursor.

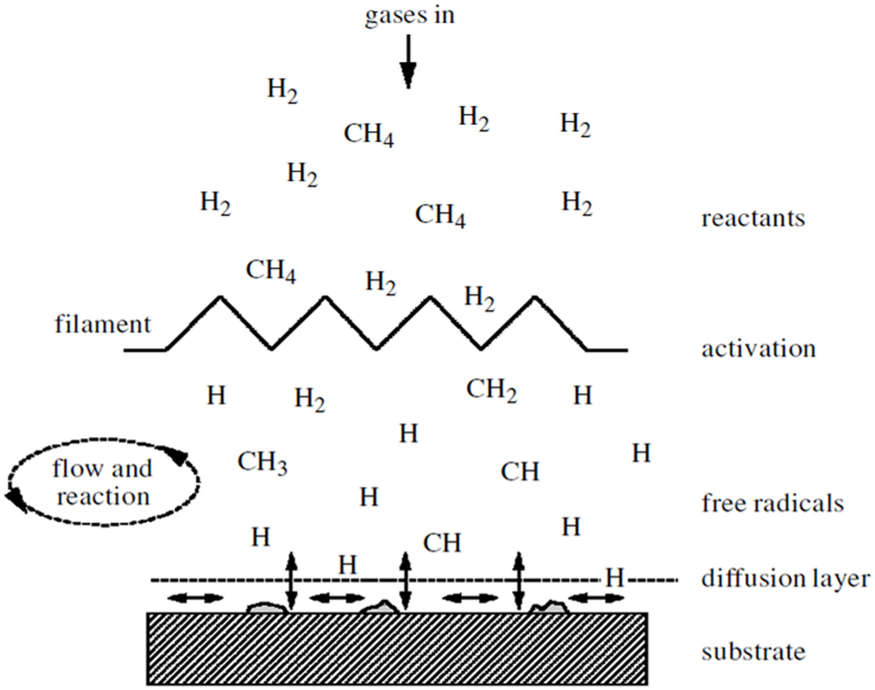


Figure 3.2 A schematic diagram illustrating the diamond chemical vapor deposition processes via the hot filament CVD method [112].

Nucleation is the first and critical step of CVD diamond growth [167,168]. If single crystal diamond is used as a substrate, the diamond lattice can be grown atom-by-atom with sp^3 tetrahedral bonds as deposition proceeds, leading to homoepitaxial diamond. But for non-diamond substrates, a surface pretreatment is often required for increasing the density of nucleation sites. A considerable amount of work has been performed to enhance the diamond nucleation for optimizing the diamond film properties such as grain size and film morphology. And a number of nucleation enhancement methods have been developed to enable the control of nucleation density over several orders of magnitude, including seeding, mechanical abrasion, ultrasonic scratching, and electrical biasing etc [167–173]. **Table 3.1** summarizes the surface nucleation densities of diamond after various surface pretreatments [167]. Substrate scratching, the most common method for achieving nucleation enhancement, is able to increase the nucleation density from <10^5 cm^{-2} on untreated substrates up to 10^{11} cm^{-2}. It is believed that such surface abrasion aids nucleation by either creating appropriate defects which act as growth templates, or embedding nanometer sized fragments of diamond which act as seed crystals, or a combination of both. These experimental investigations have provided the guideline for the optimum of surface pretreatment methods and deposition parameters for diamond CVD process, which might promote the utilization of diamond in electronic applications.

Table 3.1 Typical surface nucleation densities of diamond after various surface pretreatment methods [167].

Pretreatment method	Nucleation density (cm^{-2})
No pretreatment	10^3–10^5
Scratching	10^6–10^{10}
Ultrasonic scratching	10^7–10^{11}
Seeding	10^6–10^{10}
Biasing	10^8–10^{11}
Covering/Coating with	
Fe film	4.84×10^5
Graphite film	10^6
Graphite fiber	$>10^9$
a-C film (first scratched)	3×10^{10}
C_{70} clusters + biasing	= seeding effect
Y-ZrO_2, a-BN, cSiC layer	Enhancement
C^+ ion implantation on Cu	Enhancement
As^+ ion implantation on Si	10^5–10^6
Pulsed laser irradiation + coating a-C, WC, cBN layer	Enhancement
Carburization	Enhancement

The CVD diamond is a suitable material for applications ranging from electronics to tribology owing to its high thermal conductivity, low electron affinity, high chemical stability and high resistance to particle bombardment [174]. Although it has been practically utilized in the market for cutting tools, protective coatings and composite additives based on the hardness of diamond, the conventional CVD microcrystalline diamond is not widely used for applications in micro/nanoelectronic devices, optical devices and nanoelectromechanical systems (NEMS) mainly due to its large grain size and rough surface morphology. It is important to refine this material to suit with many applications for better exploiting its superior properties. To achieve this goal, the processing challenges and difficulties encountered in applying diamond to thin film and device forms can be minimized by the development of nanocrystalline diamond, often referred to as “nanodiamond”, which possesses a grain size in the nanometer scale between 1 nm and 100 nm. Apart from the substantial nature of the conventional CVD microcrystalline diamond, the nanodiamond, attributing to its material features of small grain size and massive network of grain boundaries, also has several unique properties including smooth and uniform surface morphology, n-type dopant incorporation, deliberate amount of sp^2-bonded carbon content in the sp^3 diamond matrix, lower internal stress, and large scope for materials processing and integration. The benefits of n-type dopant incorporation and sp^2 graphitic inclusion for enhancing field emission behavior have been discussed previously in **Section 2.3.2 (v)** and **(vi)**. In addition, the small grain size and smooth surface morphology of nanodiamond allow compatible process and integration with silicon microfabrication technology and thus further facilitate the development of diamond micro/nanoelectronic devices. Furthermore, these properties of nanodiamond are controllable, reproducible and tunable over a broad range, elevating the utility of nanodiamond in vacuum micro/nanoelectronics.

3.2 Morphology of nanodiamond

The main feature of nanodiamond is its small grain size which is generally below 100 nm and can typically be controlled to be as small as 2 nm. The diamond film with the smallest grain size is called ultrananocrystalline diamond (UNCD) [71,83,87−89,91], a term originating from Argonne National Laboratory. This film has grain size around 2 − 5 nm with a considerable amount of *sp*^{2}-carbon within grain boundaries [87]. **Figure 3.3** shows a high resolution transmission electron microscope (TEM) image of the UNCD where the lattice planes of diamond are clearly observed. All other typical nanodiamond films have cluster morphology with grain size of 15 – 20 nm, as shown in **Figure 3.4(a)** and **(b)** [128]. The change in morphology of the diamond film brings with it a large increase in the utility of the material.

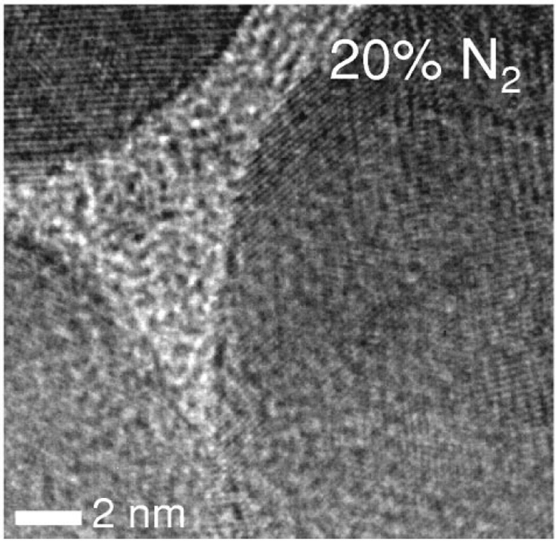


Figure 3.3 Plan-view TEM image of the UNCD film synthesized using 20% N_2 in CH_4/Ar plasma, showing 3−5 nm grain size with large fraction of sp^2-bonded atoms within the grain boundaries [87].

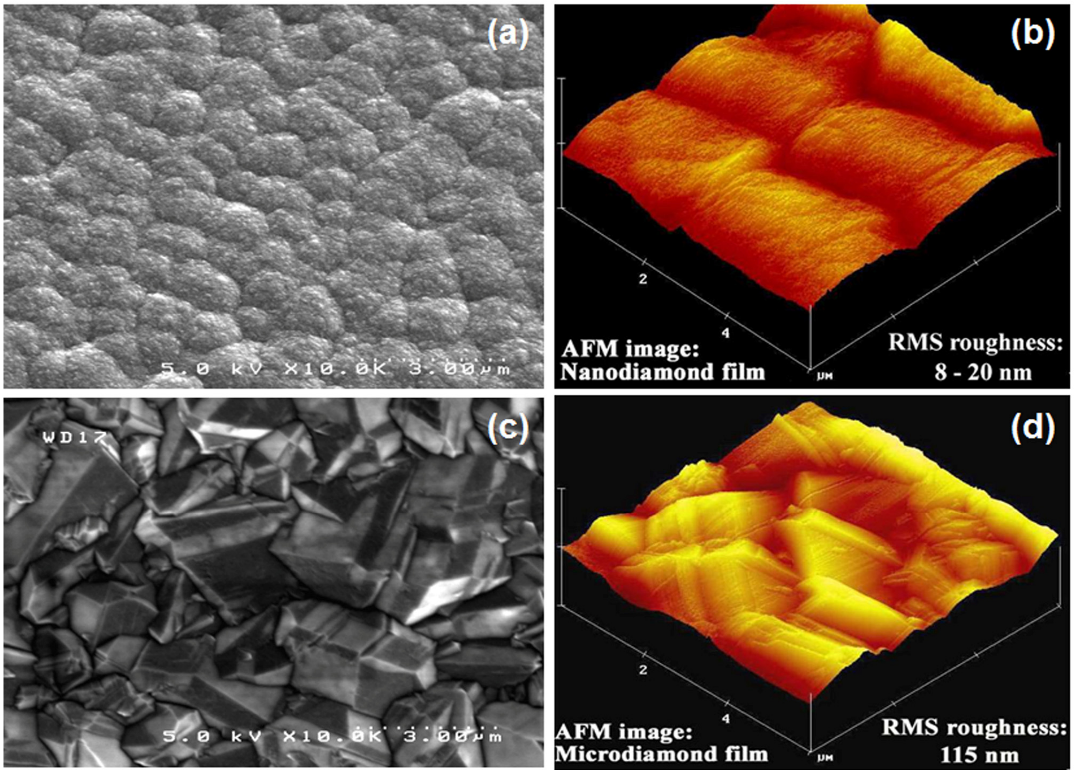


Figure 3.4 (a) Plan-view SEM and (b) AFM images of nanocrystalline MPCVD diamond films. (c) Plan-view SEM and (d) AFM images of microcrystalline MPCVD diamond films [128].

With regard to field emission, the nanometer-sized diamond grain allows the formation of an ultra-sharp emitter tip with small radius of curvature, which provides a high geometrical field enhancement factor [93]. Additionally, the increased grain boundary network acts as conduction channels in the bulk nanodiamond layer, facilitating the electron transport through the film and enhancing its electrical conductivity [87,91]. Furthermore, the smooth, dense and uniform surface morphology of nanodiamond offers a conformal diamond coating on a wide variety of materials with high aspect ratio structures, overcoming most of the drawbacks and difficulties of processing conventional microdiamond. As for the protective optical coating, the nanodiamond also provides a smooth and uniform film with a typical root mean squared surface roughness of ~ 20 nm and without compromising the diamond hardness and other useful properties, independent of the film thickness. This surmounts the problem of high surface roughness (100 – 400 nm) in the conventional microdiamond associated with the attenuation and scattering of transmitted signals, eliminating the requirement of using the expensive and time consuming post-polishing method. The smoothness of the thin film is directly related to its mechanical properties such as coefficient of friction relevant to NEMS, and is also a very critical factor in several cases including micropatterning of diamond films to realize useful structures, and integration of different materials with diamond.

Our research group has developed an effective and consistent microwave plasma enhanced CVD (MPECVD) technique for the deposition of nanodiamond and explored the effects of controlling the plasma chemistry and process parameters on the diamond film morphology [102,128]. The diamond grain size was significantly reduced to 5 – 15 nm, as shown in **Figure 3.4**, by decreasing the methane flow rate, reducing the microwave power and lowering the reactant pressure. The atomic force microscopy (AFM) of diamond image, shown in **Figure 3.4,** also confirmed that the nanodiamond film has a smoother surface morphology and wider latitude for materials processing and integration than the microdiamond film. Moreover, this nanodiamond film has been successfully integrated with silicon microfabrication technology and employed in the fabrication of monolithic lateral electron field emission devices via micropatterning coupled with the reactive ion etch technique [128,145], demonstrating the feasibility of using nanodiamond in realizing useful device structures. In this research, the smooth nanodiamond film will be applied to the fabrication of vertically-configured nanodiamond emitter tips in triodes and integrated structures, employing a mold transfer technique incorporated with the conformal nanodiamond deposition.

3.3 Raman spectroscopy and sp^2/sp^3 composition of nanodiamond

Raman spectroscopy is a non-destructive standard characterization technique for any carbon system, utilized to determine structure and composition of carbon films [175,176]. It relies on Raman scattering (inelastic scattering) of monochromatic light which is usually obtained from a laser with a wavelength ranging from near ultraviolet to near infrared. Raman scattering can be described as the phenomenon that the incident photons interact with the molecular vibrations, phonons, or other excitations in such a way that energy is either gained or lost so that the energy of scattered photons are shifted [177]. As the excitation photon impinges upon a molecule, it excites the molecule from the ground energy state to a virtual energy state. When the molecule relaxes and returns to a different rotational or vibrational state, it emits a photon which has a different energy from that of the initial state, resulting in a frequency shift between the scattered and incident photons. The scattered photon with changed wavelength is collected by a detector, giving information about the vibrational modes in the system.

Figure 3.5(a) exhibits a typical visible Raman spectrum of a nanodiamond film, featuring three typical bands at 1120, 1332, and 1560 cm^{-1}, in comparison with that of a conventional microdiamond film (grain size of 1 – 3 μm) as shown in **Figure 3.5(b)**, where a sharp peak at 1332 cm^{-1} and a insignificant peak at 1560 cm^{-1} are observed. The peak at ~ 1332 cm^{-1} is assigned to the first-order phonon mode for diamond, reflective of the sp^3-bonded diamond crystallites [176]. It is known that the intensity and broadening of Raman peaks are directly correlated with the crystallinity (crystal size) of films. The significantly broadened diamond peak for the nanocrystalline films results from the

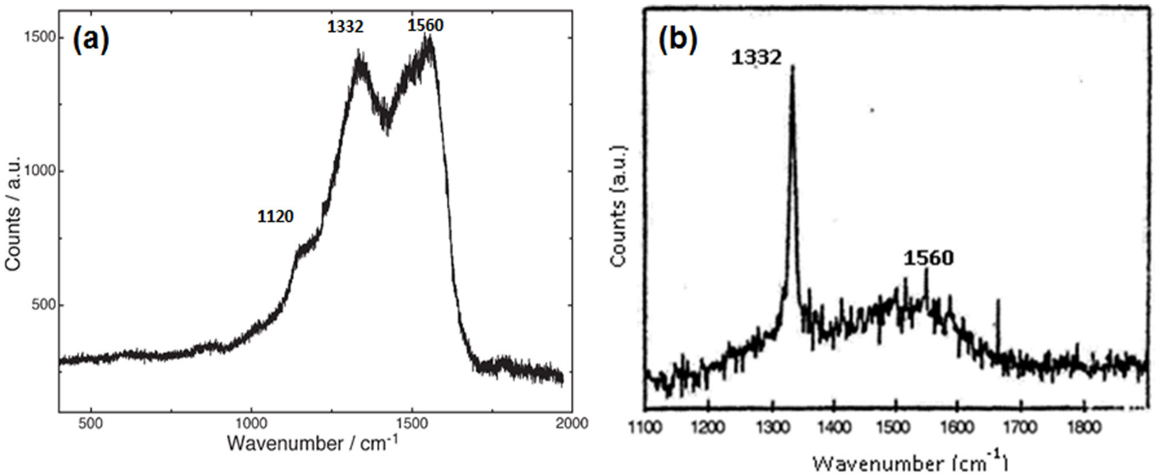


Figure 3.5 Typical visible Raman spectra of (a) a nanocrystalline diamond film and (b) a microcrystalline diamond film [128].

decreasing grain size to the nanometer scale. To a first approximation, the full width at half maximum (FWHM) of the peak is a measure of the phonon lifetime. Since the nanodiamond possesses more grain boundaries and dopant impurities (e.g. nitrogen) than microdiamond, the phonon lifetime is short and thereby the FWHM of diamond peak is broader [149]. The peak at ~ 1560 cm^{-1} is assigned to the sp^2-graphitic component, resulted from the bond stretching of all pairs of sp^2 atoms in both rings and chains. Except for UV excitation, the Raman spectra are dominated by the sp^2 sites because the excitation resonates with π-bonded carbon atoms [175]. Raman scattering in visible range is about 50 times more sensitive to the sp^2-bonded carbon than the sp^3-bonded carbon [149]. Also, the use of visible excitation often gives rise to an intense background photoluminescence that can mask the Raman line in nanodiamond, even in films with low amount of sp^2-bonded carbon. Therefore, a graphitic peak is observed in the visible Raman spectrum of a nanodiamond film owing to the low amount of sp^2-bonded carbon atoms existing in the grain boundaries. The position and intensity of this broad peak depends on the excitation wavelength, the relative amount of sp^2-bonded carbon phase, and how microstructurally ordered or disordered the phase is. The peak at 1120 cm^{-1} is observed in nanodiamond films in the vicinity of 1120 – 1190 cm^{-1} by different researchers [85,89,90,92,93,149]. The origin of this peak is still controversial, and definitive assignment of this peak has not yet been made. It is possible that the band arises from the effects of nanocrystallites or disorder in the tetrahedral carbon network of diamond.

Visible Raman spectroscopy is mainly suitable to monitor the sp^2-carbon behavior and follow the evolution of sp^2-carbon phase since the scattering cross-section of the sp^2 phase is much higher than that of sp^3 phase. UV–Raman spectroscopy, on the other hand, using more energetic photons (shorter wavelength) can characterize the nature of sp^3-bond in the films more clearly. The signal for diamond is expected to increase relative to that for amorphous or graphitic carbon as the excitation wavelength is shifted toward the UV due to an increase in the scattering cross section. The typical UV Raman spectrum of nanodiamond films taken with 325 nm excitation is shown in **Figure 3.6(a)** [176]. It is obvious that the diamond peak at 1332 cm^{-1} is of a high-resolution in the UV Raman spectrum, but not easily resolvable in visible Raman spectroscopy. **Figure 3.6(b)** displays UV Raman spectra of nanodiamond films deposited using different N_2 gas ratio in the source gas mixture [149]. It can be seen that the peak intensity ratio of the sp^3-bond to the sp^2-bond decreases with the increase of nitrogen in the reaction gas mixture. One of the theories suggests that the reduction of sp^3/sp^2 ratio with N_2 is owing to the decrease of the diamond grain size and the increase of the relative number of grain boundaries where the sp^2-bonded carbon atoms exist [87]. Overall, it is evident that nanodiamond films have a significant diamond crystal component with a deliberate amount of sp^2-bonded carbon inclusion.

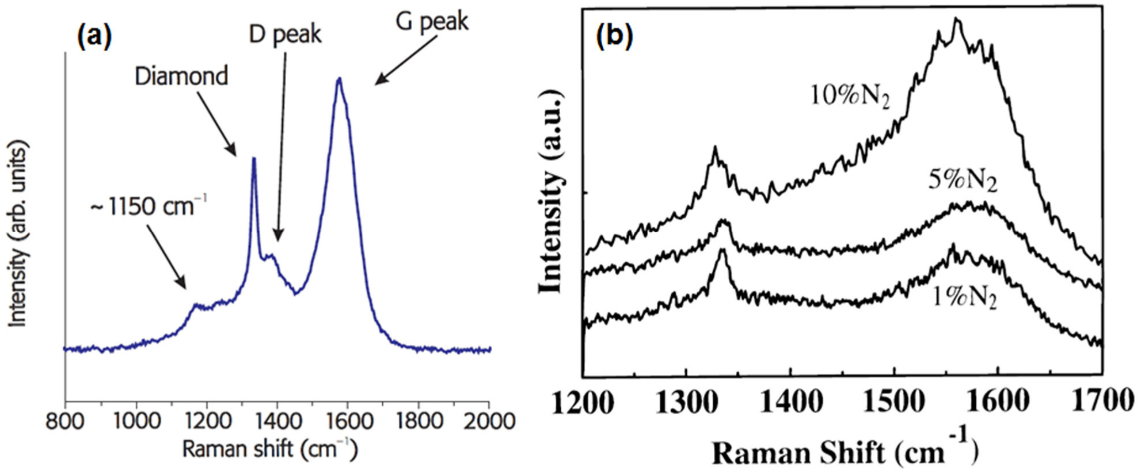


Figure 3.6 (a) A 325 nm Raman spectrum of a nanocrystalline diamond grown under typical conditions [176]. (b) UV Raman spectra of nanocrystalline diamond films deposited from 1, 5, and 10% N_2 in the CH_4/Ar plasma [149].

3.4 Nitrogen as an n-type dopant in nanodiamond

In practice, introducing impurities especially donors into diamond is difficult since diamond is a wide band gap material with very tight lattice structure. The success in fabricating diamond-based electronic devices has thereby been severely restricted due to the difficulty of producing n-type diamond thin films with sufficiently high conductivity at room temperature. For instance, in bulk diamond, nitrogen atoms at substitutional sites introduce a deep donor level at 1.7 eV below the conduction band minimum, and thus the nitrogen doping is not thermally activated at room temperature [92]. However, nitrogen doping in nanocrystalline diamond shows different characteristics. It has been demonstrated that nitrogen is among a few suitable dopants for nanodiamond. Nitrogen doped nanodiamond films with n-type conductivity have been achieved via the *in-situ* addition of N_2 gas to the reaction gas plasmas generated in CH_4/Ar and CH_4/H_2 mixtures, exhibiting significant enhancement of room temperature electrical conductivity [87–89,91–93].

Unlike single crystal diamond or microcrystalline diamond films, nanodiamond allows for easier incorporation of nitrogen impurities because of its small grain size and high density of grain boundaries. It has been shown that the nitrogen incorporation into the grain boundaries is preferred than into the bulk diamond owing to the lower substitution energy of nitrogen for the grain boundaries [87,150,178]. Nitrogen increases the amount of threefold-coordinated carbon atoms in the grain boundaries, resulting in an upward shift of the Fermi level toward the conduction band due to the additional electronic states associated with carbon π bonds and dangling bonds, providing a conduction channel through the grain boundaries. The role of sp^2-carbon content within the grain boundaries for enhancing the electron transport and thereby increasing the electrical conductivity has been explained in **Section 2.3.2-(v)**.

Researchers in Argonne National Laboratory have demonstrated the nitrogen incorporation into the ultrananocrystalline diamond films for enhancing the n-type conductivity by determining the nitrogen content and electrical conductivity of the film as a function of N_2 reaction gas percentage in CH_4/Ar plasma [87,91,149]. Their secondary ion mass spectroscopy (SIMS) analysis indicated that the nitrogen concentration in the film saturates at 2×10^{20} atoms/cm^3 (~ 0.2 % total nitrogen content in the film) when 5 % N_2 was added in the plasma, as shown in **Figure 3.7(a)**. The conductivity at room temperature increases dramatically with nitrogen concentration, from 0.016 (for 1 % N_2) to 143 $\Omega^{-1}cm^{-1}$ (for 20 % N_2), as shown in **Figure 3.7(b)**. Further, the nitrogen incorporation has been confirmed to be consistent through the depth of the film, shown by the profiles of the carbon and nitrogen concentrations as a function of depth for the nanodiamond film deposited using $CH_4/N_2/Ar$ mixture, as displayed in **Figure 3.7(c)**.

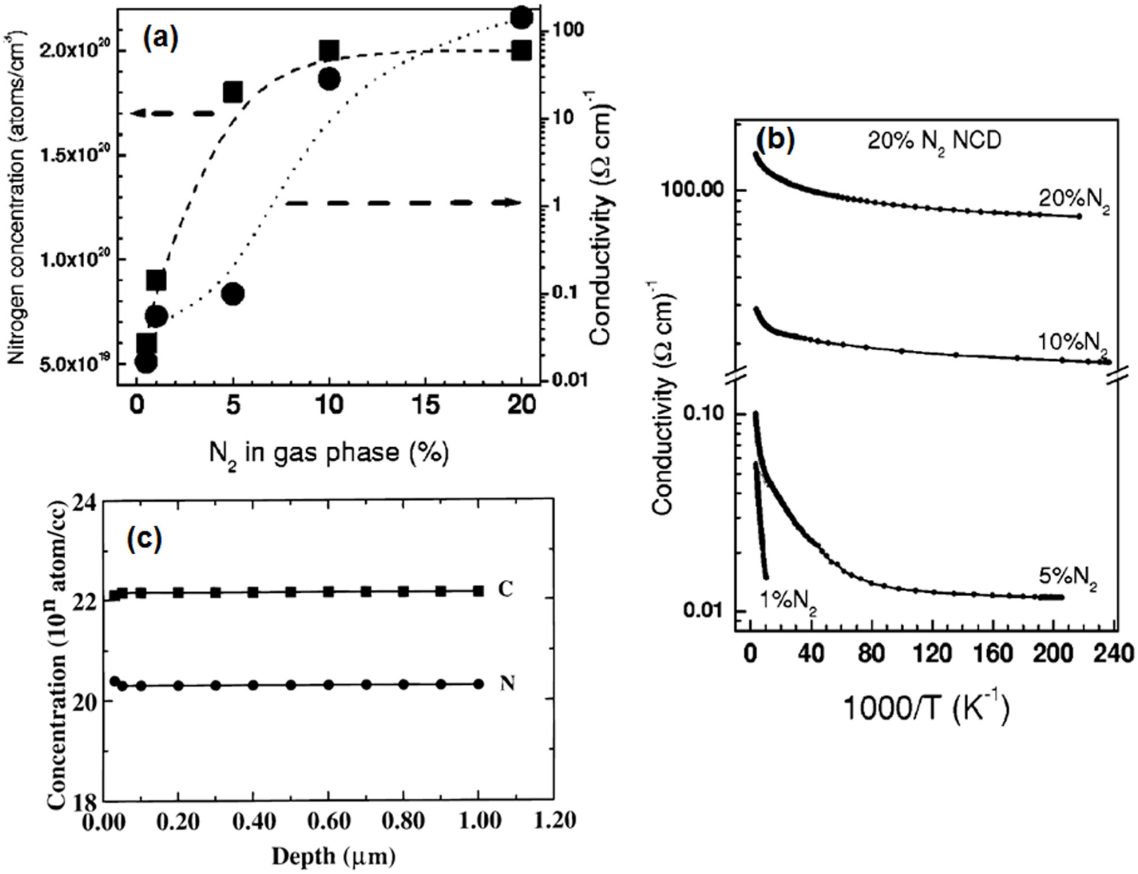


Figure 3.7 (a) Total nitrogen content and room-temperature conductivity of the nitrogen-incorporated UNCD films as a function of nitrogen in the plasma, and (b) the corresponding Arrhenius plot of conductivity data obtained in the temperature range of 300 – 4.2 K [87]. (c) Depth profiles for the atomic carbon and nitrogen concentrations in a nitrogen-containing nanodiamond film deposited using 5% N_2 in CH_4/Ar plasma [149].

Several research teams, including our group in Vanderbilt, have reported successful nitrogen incorporation and high electrical conductivity in nanodiamond films [93]. The composition analysis of the nanodiamond grown from $CH_4/H_2/N_2$ MPECVD has been conducted by employing energy dispersive X-ray spectrometry (EDS) and Rutherford backscattering spectrometry (RBS). **Figure 3.8(a)** shows the EDS

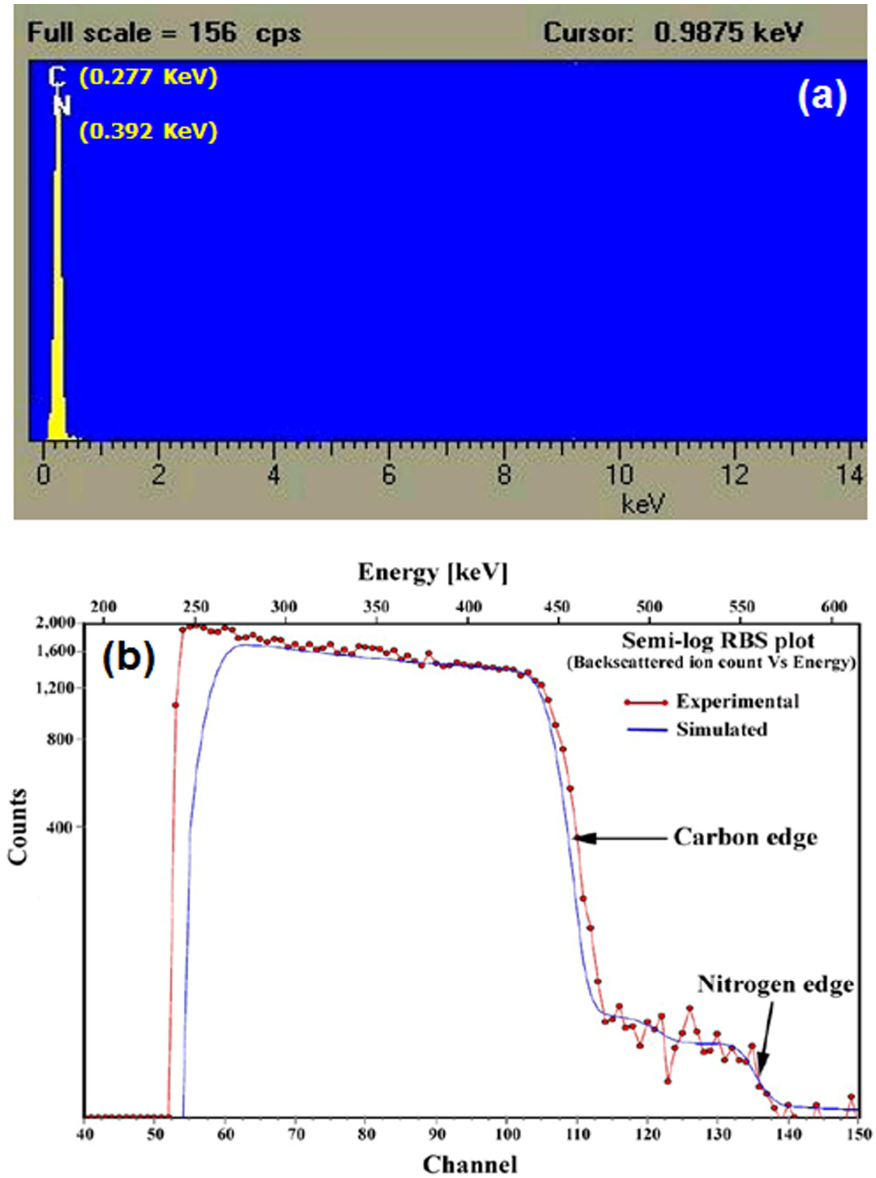


Figure 3.8 (a) EDS profile (X-ray count vs. energy) and (b) Semi-log RBS plot (backscattered ion count v.s. energy) obtained from the nanodiamond film deposited by $CH_4/H_2/N_2$ MPECVD [128].

microanalysis which displays a real time histogram of X-ray count per channel versus energy expressed in keV [128], indicating the incorporation of nitrogen in the diamond. The profile obtained from nanodiamond films exhibits the characteristic carbon and nitrogen elemental peaks at X-ray energies of 0.277 and 0.392 keV, respectively. The presence of nitrogen is also confirmed according to the semi-log RBS plot [93] which displays a distinct nitrogen edge, as shown in **Figure 3.8(b)**. Quantitatively, the nitrogen concentration is found to be ~ 4.5 x 10^{21} cm^{-3} in the near surface region (~ 50 Å) of the nanodiamond film. The actual percentage composition of nitrogen in the diamond is ~ 1.45 %. Although RBS is used to verify the composition in the near surface region, the nitrogen concentration should be uniform throughout the nanodiamond layer since the *in-situ* nitrogen incorporation technique is homogeneous during nanodiamond thin film deposition.

3.5 Growth temperature of nanodiamond

The substrate temperature for most CVD processes is usually required to be above 700 °C to grow high quality crystalline diamond films at reasonably high deposition rates. The nucleation and growth of diamond is not an easy task at lower substrate temperature (< 400 °C). This has limited the development of diamond-based microelectronics and its utilization in integrated circuits and other applications such as NEMS devices. Therefore, finding ways to grow diamond at a reduced substrate temperature without sacrificing the diamond quality is thus highly sought-after. So far, successful synthesis of nano/ultrananocrystalline diamond films grown with H_2/CH_4 and Ar/CH_4 plasma chemistries at temperatures as low as 400 °C has been reported [179–181], using an optimized seeding process with nanodiamond powder via ultrasonication. The heating of the substrate by the plasma is greatly reduced owing to the lower thermal conductivity of Ar than that of H_2 and the lower power levels needed for plasma formation [179]. Besides, the thermal activation energy for the UNCD thin film is lower than that for the conventional microcrystalline diamond. It has also been found that the

UNCD synthesized with Ar/CH_4 plasma chemistry exhibits less temperature dependence in the growth rate than the microcrystalline diamond prepared with H_2/CH_4 chemistry. **Figure 3.9(a)** and **(b)** display uniform and continuous UNCD films obtained at substrate temperatures of 800 and 400 ˚C, respectively. The *sp*^{3} component in the UNCD films deposited at different substrate temperatures has been confirmed by the observation of clear diamond peak at 1332 cm^{-1} in the UV Raman spectra, as shown in **Figure 3.10(a)**. Additionally, the low-temperature UNCD can be seen conformally deposited on the integrated structure of the device containing aluminum with low melting point (660 °C), as shown in **Figure 3.10(b)**. Deposition of diamond at low temperatures can facilitate the integration of diamond with other materials and promote its application in integrated circuits and other electronic applications.

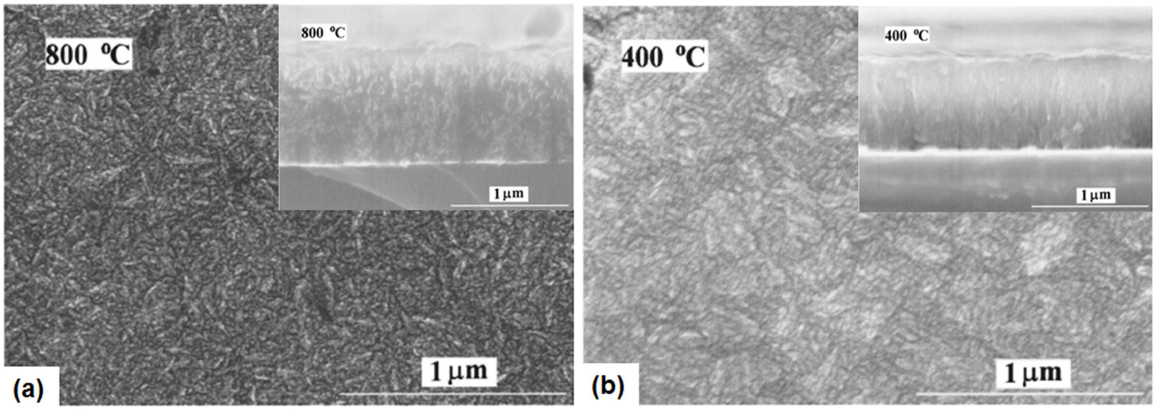


Figure 3.9 SEM pictures of surface morphologies of UNCD films deposited at (a) 800 °C and (b) 400 °C, respectively, along with their corresponding cross-section view images in the inset.

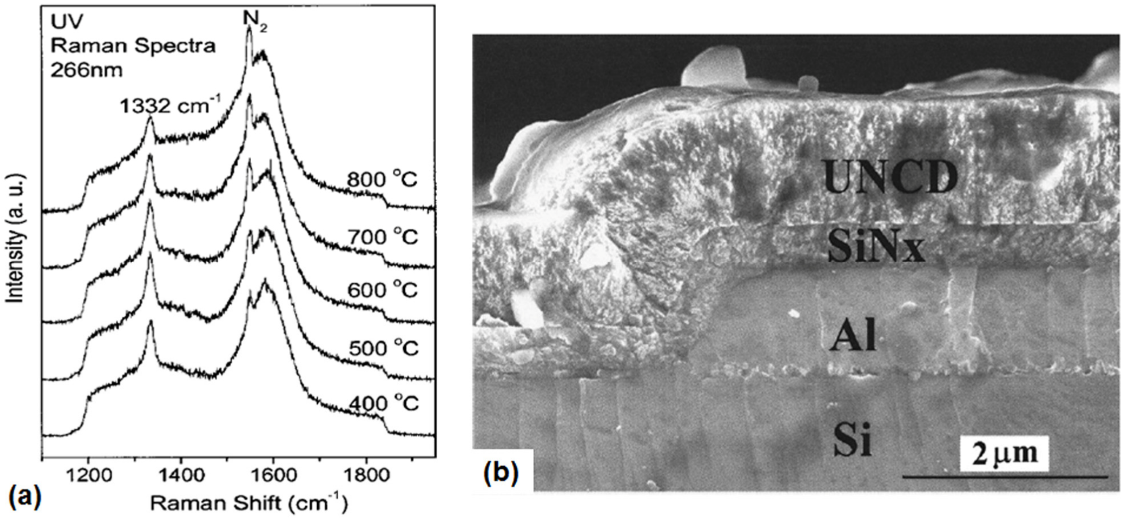


Figure 3.10 (a) UV Raman spectra of UNCD films deposited at various temperature. (b) SEM image of Low temperature UNCD deposition as hermetic protective coating for bioMEMS.

3.6 Reported field emission characteristics of nanodiamond

The first successful, reproducible low-pressure CVD for diamond synthesis over diamond substrate was achieved by Eversole in 1952 and presented in 1962 [182]. The negative electron affinity of diamond was reported by Himpsel et al. in 1979 [115]. Despite this early start, it was until the early 1990's that the investigations of field emission properties of diamond started significantly, generating a lot of scientific and economic interest. This was due to the increased availability of diamond coatings and depositions onto a variety of substrate materials using controlled quality low-pressure CVD techniques [113,114]. Since then, many researchers reported electron emission from different types of diamond emitters, demonstrating that diamond and diamond-like-carbon (DLC) materials possess superior field emission behaviors with low turn-on fields and useful emission current densities.

Diamond field emission was reported in the early 1990's. Wang et al. [56] presented the electron emission from an undoped thick polycrystalline diamond film grown by microwave plasma assisted CVD method, observing a current density of 10 mA/cm^2 at a low electric field of 3 V/μm. Geis et al. [57] also reported the electron emission from diamond cold cathodes in diode configuration formed by using carbon ion implantation into p-type diamond substrates. Djubua and Chubun [24] investigated the field emission properties of Spindt-type cathode arrays with molybdenum, hafnium and diamond-like-carbon materials, mentioning that although the DLC had the lowest operating voltage, high current density was not achieved with such cathodes because of low conductance in DLC material. Since then, tremendous amount of research have been conducted to enhance the diamond field emission, including surface treatment (with H_2, O_2 and Cs) [59], n-type (Li, P and N) and p-type (B) doping of the film [63,146–148], conformal coating on sharp Si tips [71,126], and formation of sharp diamond structures [61]. Most of these diamond-based cold cathodes are found to emit electrons efficiently under applied fields. In the late 1990's, the field emission characteristics of nanocrystalline diamond were studied. A good emission behavior with a low onset electric field of 3.2 V/μm (at emission current of 4 μA/cm^2) was observed from a nanodiamond thin film synthesized by microwave plasma enhanced CVD [69]. A superior emission performance from nanostructured diamond particles than most of the cathode materials including Mo tips, Si tips, CVD diamond, and Cs-coated diamond was also reported, showing a relative high emission current density of 10 mA/cm^2 at an applied field of 3 to 5 V/μm [70]. Since then, nanocrystalline diamond, as an emerging form of CVD diamond, has dominated the field of vacuum micro/nanoelectronics [85−100].

Over the last decade, the Vanderbilt Diamond Group has become one of the leading research teams in this area and has published many outstanding works on diamond vacuum field emission from various structures. A uniquely engineered mold transfer technique for creating micropatterned diamond pyramidal microtip emitters has been developed [102]. **Figure 3.11(a)** displays a typical high-density diamond pyramidal field emitter array microstructure fabricated using the mold transfer process. Various methods developed to enhance diamond field emission, including the incorporation of sp^2 content into diamond, vacuum-thermal-electric (VTE) treatment, p-type boron doping, and tip sharpening have been systematically studied based on the diamond pyramidal emitters in diode configurations. Improved emission behavior was clearly observed, as shown in **Figure 3.11(b)**. A high emission current of 22 mA at an electric field of 16 V/μm has been recorded from a diamond pyramidal emitter array (1.5 x 10^5 microtips) tested in diode configuration [183]. Additionally, transistor characteristics have also been studied based on the three-electrode field emission device employing both the undoped and boron-doped diamond pyramidal microtips as emitters, exhibiting a high anode current of ~ 230 μA from a 256 x 256 boron-doped diamond microtip array under the bias condition of V_a = 400 V and V_g = 32 V. **Figure 3.11(c) and (d)** show the fabricated diamond VFE transistor and its corresponding electrical behavior [102].

Recently, nitrogen-incorporated nanocrystalline diamond films with grain size as small as 5 nm have been grown by utilizing the $CH_4/H_2/N_2$ MPECVD technique at Vanderbilt [128]. Enhanced field emission diode behavior was observed from the pyramidal microtip array fabricated with $CH_4/H_2/N_2$ deposited nanodiamond [93], showing a very low threshold field of 1.6 V/μm and a high emission current of 19 mA at

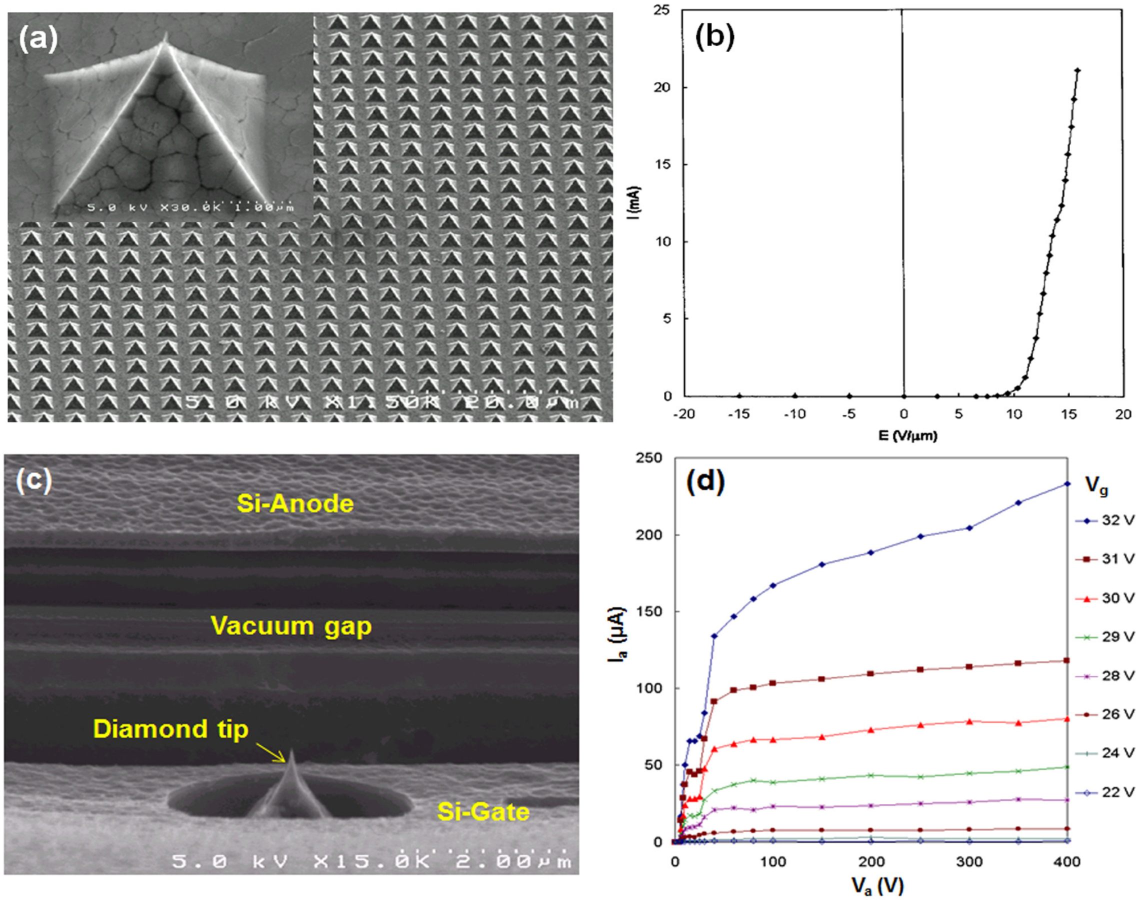


Figure 3.11 (a) SEM image of a high density diamond pyramidal sharp tips array, inset shows the high magnification image of a single tip. (b) The field emission I-V characteristics obtained from the diamond pyramidal emitter array. (c) SEM image of a diamond vertical transistor structure. (d) The corresponding I_a-V_a-V_g characteristics.

6 V/µm (2.5 x 10^5 microtips). The improvement can be attributed to the better geometrical enhancement factor, increased *sp*^{2}-carbon content and higher electrical conductivity. The nitrogen-incorporated nanodiamond has also been utilized for lateral field emission devices with finger-like emitter geometry and controllable interelectrode spacing [128,145]. The smooth surface morphology and uniformly controlled thickness properties of nanodiamond have overcome many lithography problems, facilitating the thin film micropatterning via nanodiamond reactive ion etch technique. Diode structures with different emitter-to-anode spacing ranging from few microns to 300 nm and with

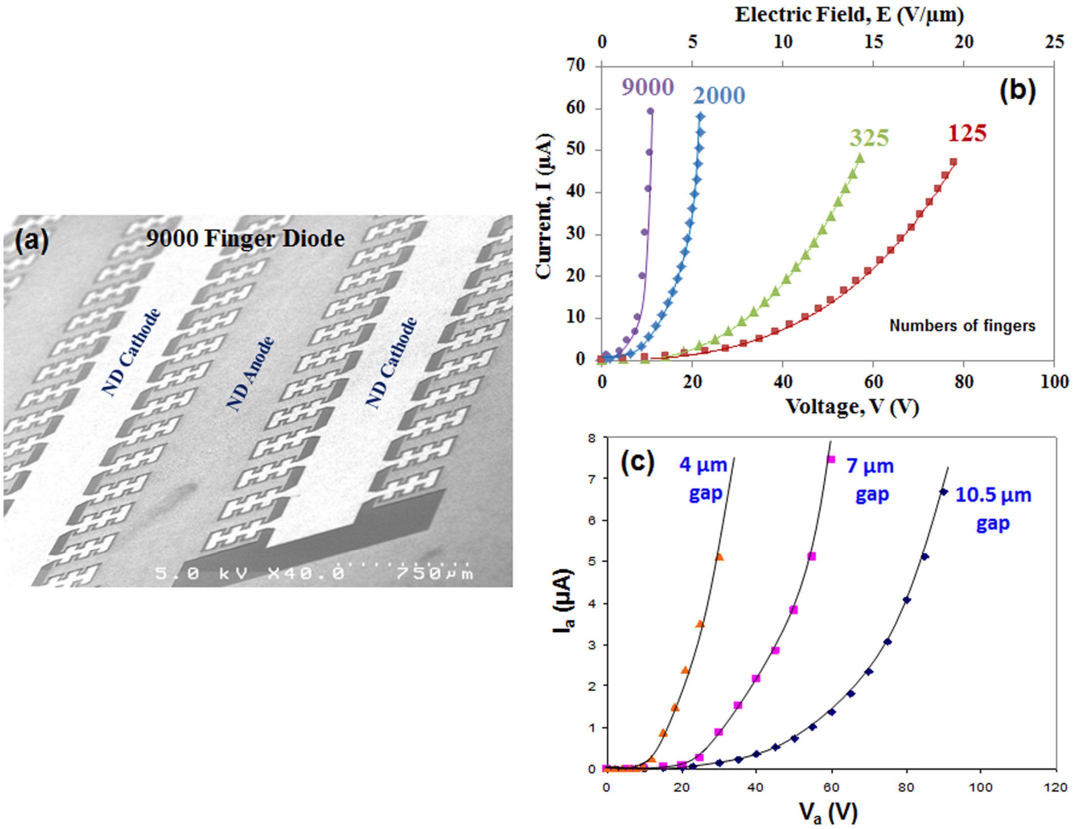


Figure 3.12 (a) SEM image of a lateral-configured 9000-fingered nanodiamond comb array device. (b) Field emission I-V characteristics of the nanodiamond lateral devices with various numbers of emitter fingers. (c) Field emission I-V characteristics of the nanodiamond lateral devices with different anode-to-emitter gaps.

different numbers of finger-like emitters from 6 fingers to 9000 fingers have been realized. The SEM images and corresponding emission characteristics are shown in **Figure 3.12**. It is observed that the threshold voltage lowering obtained by decreasing the emitter-to-anode gap whereas the emission current enhancement achieved by increasing the emitter area. Furthermore, the features of temperature tolerance and radiation hardness of the nanodiamond lateral vacuum field emission microelectronics technology have been manifested, exhibiting unaffected electrical performance at the temperature up to 400 °C and after the radiation exposure of 15 Mrad total doses and $4.4(10^{13})$ neutrons/cm^2 level [97−99]. Besides, three-electrode field emission devices with transistor and triode characteristics have also been successfully demonstrated in a completely integrated planar lateral emitter configuration, as shown in **Figure 3.13**. A high emission current of 40 μA from 140 nanodiamond emitter fingers at the bias condition of $V_a = 60$ V and $V_g = 10$ V was obtained from the triode structure employing a silicon bottom gate electrode lying underneath the nanodiamond emitter fingers.

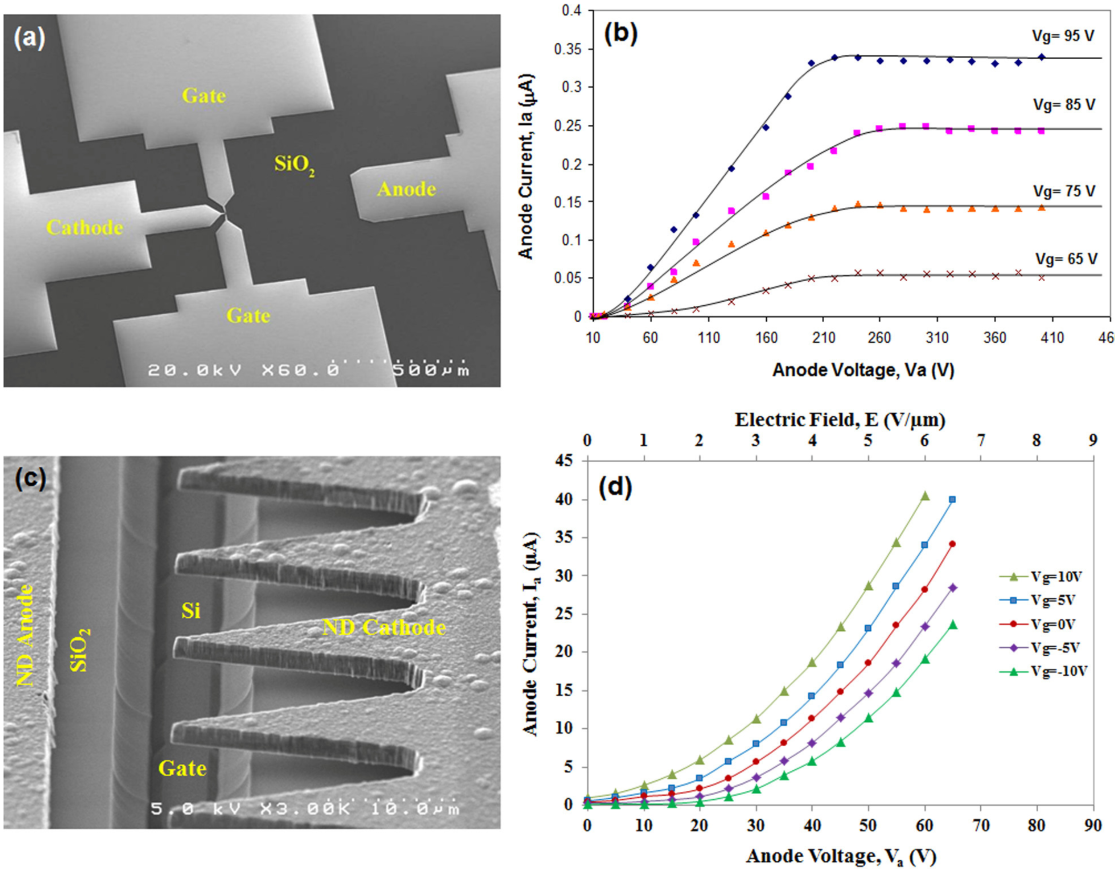


Figure 3.13 (a) SEM image of a completely integrated nanodiamond lateral field emission transistor with single finger. (b) The corresponding I_a-V_a-V_g characteristics. (c) SEM image of a lateral field emission triode with multiple nanodiamond emitting fingers. (d) The corresponding I_a-V_a-V_g characteristics.

Despite the excellent field emission performance of nanodiamond lateral field emission devices, few problems still limit their application into vacuum microelectronic circuits. The addition of more emitter fingers indeed enhances the emission current, but increases the total area footprint of the device and complicates the fabrication processes with lower yield. In addition, the anode currents of lateral vacuum triodes and transistors described above are relatively low compared to their solid state counterparts. Furthermore, since both of the anode and emitter in the lateral vacuum devices are made of nanodiamond, electron emission might occur under reverse bias, losing the rectifying behavior. On the other hand, the densely packed array of vertically-configured nanodiamond pyramidal microtips can be easily realized, providing higher current from a small area footprint. Also, higher emission current can be obtained from the vertical vacuum triodes and transistors employing the array of nanodiamond pyramidal microtip emitters because of the better gate control over emission current owing to the uniform gate-to-emitter spacing for each individual emitter tip. Moreover, high work function materials such as metal and silicon are usually utilized as the anode and gate electrodes in vertical diamond vacuum triodes and transistors, giving nearly no current under reverse bias and negligible emission current from the gate under forward bias.

In this research, various forms of three-electrode nanodiamond vacuum devices based on the superior nitrogen-incorporated nanodiamond pyramidal microtip emitter array are developed, employing an IC-compatible fabrication process which involves the mold transfer self-aligned gate-emitter technique and conformal CVD nanodiamond growth. The transistor and triode electrical characteristics of the device are studied. And the further implementation of vacuum differential amplifier using the vertically configured nanodiamond field emission transistor on a single chip is realized, demonstrating the feasibility of using vacuum integrated circuits for practical electronic applications.

CHAPTER IV

RESEACH APPROACH

4.1 Overview

The purpose of this research is to develop a reliable fabrication process for achieving efficient three-terminal nanodiamond field emission devices operable at low voltage and high emission current with low leakage current for vacuum micro/nanoelectronics and IC-compatible applications. This research is comprised of three main sections. The first part of the research is to develop the nanodiamond pyramidal sharp tip microstructures integrated and self-aligned with the silicon gate in the three-electrode configuration, employing a dual-mask microfabrication process which involves a silicon-on-insulator (SOI) mold transfer technique in collaboration with MPECVD nanodiamond deposition and silicon gate partitioning. This part includes the design, fabrication and electrical characterization of the vertically-configured nanodiamond field emitter microtip arrays in transistor and triode configurations. The aim is to develop well-controlled and reproducible processes for realizing useful nanodiamond VFE transistors/triodes with high anode current and low gate current at low operating voltage via optimizing the geometric structure of gate electrode. The second part of this research focuses on the development of nanodiamond VFE transistor and triode signal amplifiers using the anode-to-emitter spacing as the device design parameter. The target is to achieve functional microelectronic devices with good values of small-signal device coefficients including μ, g_m and r_a for providing distinct functions in electronic circuit applications. The final part of the research is the implementation of an integrated differential amplifier employing the developed nanodiamond VFE transistors on a single chip, demonstrating a viable approach to vacuum-based IC technology. The specific device design, fabrication details, characterization techniques, device behaviors and experimental results achieved are presented and discussed in chapter V and VI. This chapter summarizes the significance of this research approach.

4.2 Development of vertically-configured nanodiamond VFE transistor and triode

An efficient three-terminal vacuum field emission device should comprise an efficient emitter with a large field enhancement factor and a closely built gate electrode with optimum geometry for effective modulation of emission current at low operating voltage and low gate current. Nitrogen-incorporated nanodiamond has been demonstrated to be a promising material for electron emission. It possesses several unique features including low electron affinity, n-type conductivity, and sp^2-carbon inclusion in diamond matrix, which are beneficial for electron emission as discussed in previous chapters. As for producing a large field enhancement factor, an emitter with a sharp tip is usually utilized to create a high geometric aspect ratio and thereby an enhanced electric field at the apex of the tip. The diamond pyramidal microtips with sharp apexes have been successfully achieved via the silicon molding technique [184], which involves formation of inverted pyramidal silicon molds by silicon anisotropic etching and MPECVD diamond deposition into the molds. This process can produce well-controlled micropatterned diamond emitters with uniformity over a large area that cannot be achieved by other techniques.

In this study, the nitrogen-incorporated nanodiamond pyramidal microtips are integrated with a self-aligned silicon gate and a planar suspended silicon anode as illustrated in **Figure 4.1**, accomplishing a three-terminal vacuum field emission device. The key device parameter for vacuum transistor (triode) design is the gate turn-on voltage (gate-controlled current modulation). For most practical applications, the turn-on voltage (modulating voltage) is desired to be as small as possible. Since the operating voltage depends upon the emitter field emission property and the gate-to-emitter distance, it is desired to fabricate the emitters with low turn-on electric field and the gate electrode with small gate-to-emitter spacing. In addition to the low operating voltage, vacuum transistors (triodes) also require low gate current for practical utilization. The gate current is consisted of two components: the leakage current through the dielectric isolation layer and the gate intercept current due to the emitting electrons captured by the gate electrode. For minimizing the gate leakage current, a thick dielectric layer with low defect and high dielectric strength between gate and emitter substrate is utilized. As for diminishing the gate intercept current without sacrificing the efficiency of gate control over emission current, a gate electrode with optimum geometric structure and position relative to emitter tip is needed. Therefore, we have developed a well-controlled and reproducible dual-mask microfabrication process, involving a SOI mold transfer technique in conjunction with MPECVD nanodiamond deposition and self-aligned silicon gate optimization, to fabricate a vertically-configured nanodiamond emitter microtip array in transistor and triode configurations operable at low voltage with high anode current and low gate current. The detailed fabrication methodology of nanodiamond vacuum field emission transistors and triodes will be addressed in next chapter.

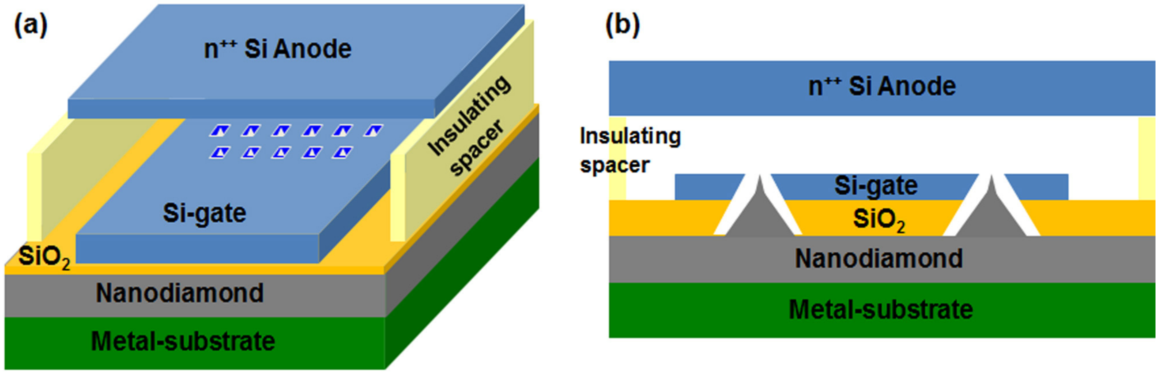


Figure 4.1 The schematic diagrams of basic design of a vertically-configured nanodiamond field emission transistor and triode in (a) inclined view and (b) side view.

4.3 Development of nanodiamond VFE transistor and triode signal amplifiers

A small variation of the gate potential can modulate the total amount of emitted electrons from the emitter and thereby a change in the anode current. This physical mechanism of gate modulation on emission current makes the vacuum field emission transistor and triode ideal for signal amplification, as shown schematically in **Figure 4.2**. The amplification performance of a VFE device is usually determined by three important small-signal device coefficients: amplification factor μ, transconductance g_m, and anode resistance r_a, as described in **Section 2.4.2**. The transistors/triodes with different amplification factor and anode resistance have distinct functions in electronic circuits. The high μ transistors which usually possess larger output resistance r_a provide high voltage gain for signal amplification. The low/medium μ triodes, which generally have modest voltage gain offer a low output impedance r_a, are used to avoid signal distortion when connecting to the load by isolating the input signal from the output signal without the need of feedback loops. The electronic circuits with desired voltage/power gain and minimal noise are programmable by using the former for signal amplification along with the latter as buffer amplifiers.

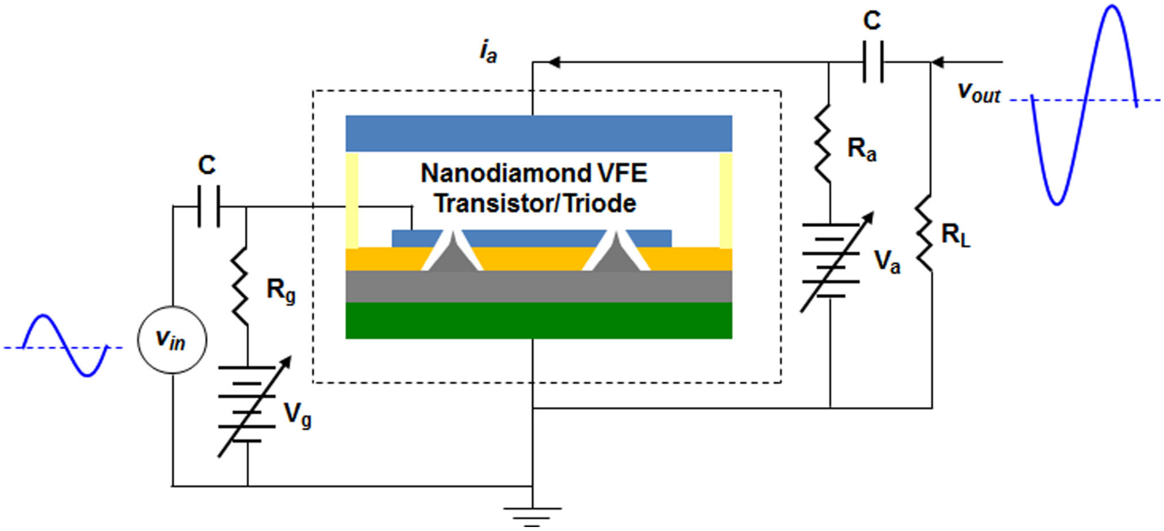


Figure 4.2 The schematic diagram illustrating a vacuum field emission transistor/triode operates as signal amplifier.

These coefficients of μ, g_m, and r_a depend on the geometric structure of gate electrode, the placement of anode electrode, and the applied gate and anode voltages. In this research, the dependency of device coefficients on the anode-to-emitter spacing and the applied gate and anode voltages are qualitatively explained by the underlying device operational principles and quantitatively extracted from the experimentally measured I-V characteristics. The nanodiamond VFE transistor and triode signal amplifiers are achieved via adjusting the anode-to-emitter spacing by the placement of the silicon anode electrode on different spacers with varied thickness. And their corresponding field emission characteristics and signal amplification behaviors are measured, followed by a systematic analysis using a modified Fowler-Nordheim theory and small signal circuit modeling. This study demonstrates that the voltage gain and output resistance of VFE transistors/triodes are programmable by designing and engineering the device geometric structures, providing a diversity of functional devices for vacuum-based electronic circuit applications.

4.4 Development of nanodiamond VFE integrated differential amplifier

The diff-amp has been developed to reduce the noise interference in single-ended amplifiers, as shown schematically in **Figure 4.3**. The sensitive signal is distributed as two equal signals with opposite phases and fed into the two input terminals of the dual-transistor, respectively. By taking the differential output, the input signals with opposite phases are amplified, while the noise common to both signals are offset owing to the symmetry of electrical characteristics of the two transistors. Therefore, the dual-transistor device can operate as a differential amplifier for amplifying the difference between input signals and rejecting the noises common to both signals.

The implementation of a vacuum-based diff-amp has been considered by the deployment of nanodiamond VFE transistors on a chip. To realize a useful vacuum-based nanodiamond diff-amp for practical application, an identical VFE transistor/triode pair with nearly the same electrical characteristics should be achieved. The nanodiamond VFE transistor pair should possess a well-matched turn-on voltage, identical emission current and similar amplification behavior at the same operating voltage. Therefore, the transistor pair with separated gate contact pads and split anode electrodes should have identical device geometric structures, including the same gate-to-emitter distance, the same anode-to-emitter gap, and exactly the same amount of nanodiamond emitter microtips with uniform tip sharpness.

The developed dual-mask microfabrication process for constructing nanodiamond emitter microtip array in transistor/triode configuration, as described in **Section 4.2**, have been employed to build a single-chip nanodiamond VFE integrated diff-amp. The SOI molding technique is able to produce uniformly micropatterned nanodiamond emitter microtips over a large area as well as well-controlled self-aligned silicon gate for each microtip. In addition, the silicon gate partitioning process, which involves photolithography to define silicon gate pads and a silicon reactive ion etch to isolate the gate electrode for individual transistors, allowing the deployment of VFE transistors for vacuum diff-amp. These fabrication methods enable the formation of identical nanodiamond VFE transistors with the same geometric structures on a single chip, offering a viable approach for future vacuum-based IC technology.

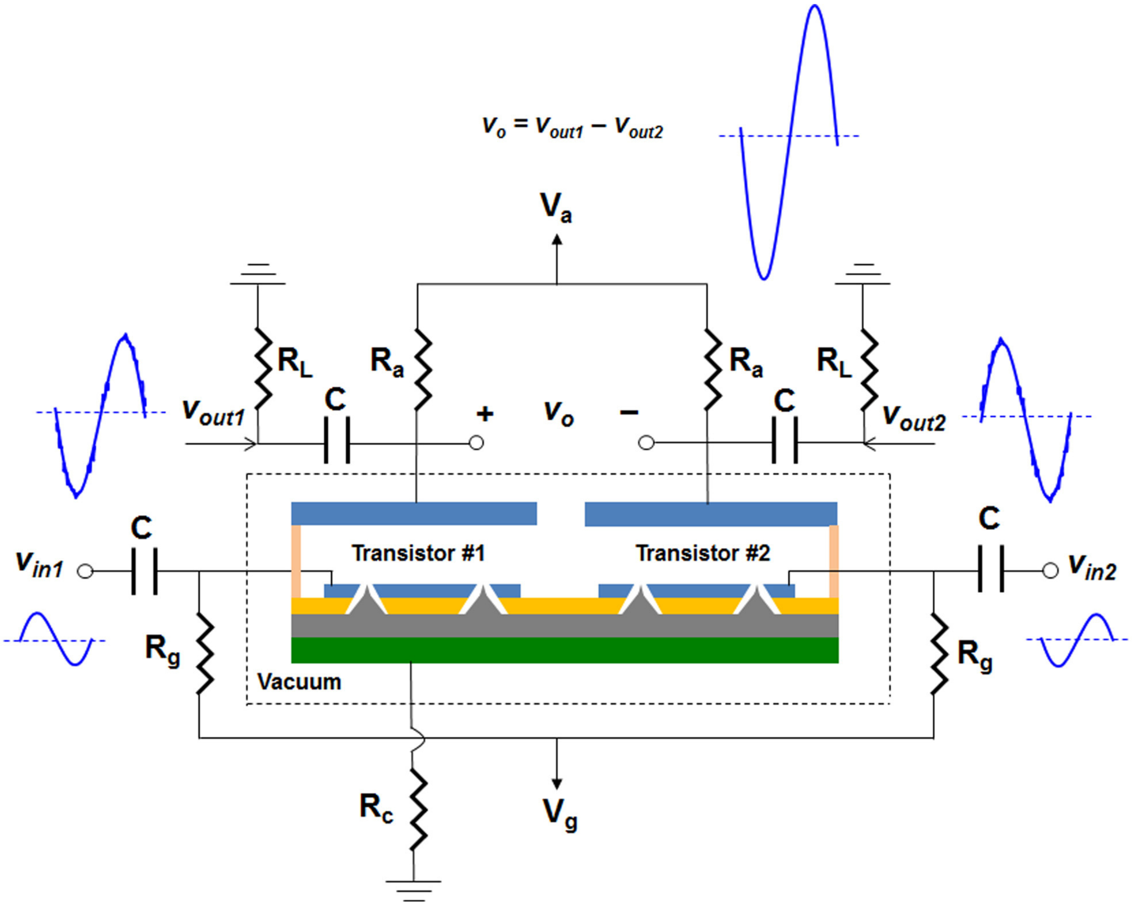


Figure 4.3 The schematic diagram illustrating a vacuum field emission diff-amp is able to reject the noises common to both transistors by taking the differential output signal between two transistors, giving a less noisy output signal with high voltage gain.

CHAPTER V

DEVICE DESIGN, FABRICATION and EXPERIMENTATION

VFE triodes and transistors are fundamental devices needed for implementation of vacuum integrated circuits. The three-electrode nanodiamond VFE device employing densely packed nanodiamond pyramidal microtips in vertical configuration can provide not only high emission current at low operating voltage from a small area footprint but also efficient gate control over emission current for signal processing, conditioning, and amplification. This chapter presents fabrication techniques developed for realization of the nitrogen-incorporated nanodiamond vacuum field emission devices in the three-terminal configuration, and their implementation into a vacuum integrated differential amplifier. The devices are fabricated by using a dual-mask microfabrication process which involves a mold-transfer self-aligned gate-emitter technique in conjunction with nanodiamond deposition into the micropatterned molds on the active layer of a silicon-on-insulator (SOI) substrate followed by silicon gate partitioning. The details of the process techniques, fabrication schemes and results are described in the following.

5.1 Fabrication of three-terminal nanocrystalline diamond VFE devices

The Vanderbilt Diamond group had previously created a mold transfer technique [184] to construct micropatterned diamond in 2000, and the physical and electrical characteristics of the diamond microtips were well explored by Wisitsora-at [102] in 2002. Following that development, nitrogen-incorporated nanodiamond films were investigated in the fabrication of pyramidal nanodiamond microtips via the mold transfer technique by Subramanian [128] at Vanderbilt in 2008, exhibiting a significant enhancement in field emission diode behavior over undoped nanodiamond microtip emitters. More recently, nanocrystalline diamond films with very small grain size of 5 – 10 nm, smooth surface morphology and high electrical conductivity were formed by optimizing the growth temperature and pressure by Ghosh [174]. In this research, the optimized nanodiamond film is utilized to form pyramidal microtip emitters in a three-terminal configuration, employing a dual-mask microfabrication process which involves a SOI mold-transfer technique in conjunction with nanodiamond deposition into the micropatterned molds followed by silicon gate partitioning.

5.1.1 Layout design of nanodiamond emitter microtip array

This research focuses on the development of three-terminal VFE devices employing nanodiamond pyramidal emitter microtip arrays in vertical configuration. The purpose of using an emitter of an array of microtips is to achieve high emission current from a small area. Thus, the array usually possesses densely packed emitter microtips. In this study, the base width of pyramidal microtip was designed to be 2 μm x 2 μm with a spacing of 8 μm between microtips. Five nanodiamond VFE devices with different emitter array sizes were fabricated on a 1 cm x 1 cm single chip to investigate the field emission transistor characteristics of the devices. The array sizes were designed to be 5x5, 20x20, 50x50, 100x100, and 100x200 microtips. For the single-chip VFE integrated diff-amp study, a 1 cm x 1 cm chip consisting of eight separate nanodiamond VFE transistors with individual anode electrode and gate contact pad were designed. The emitter array size for each transistor was designed to be 80 x 80 with the same microtip pitch. Each transistor is capable of being operated independently, and can also be integrated with other transistors as diff-amp pairs, giving the possibility of four dual-transistor diff-amps on this chip.

5.1.2 Mold-transfer self-aligned gate-emitter technique

Figure 5.1 shows the schematic layout and fabrication scheme of the nanodiamond VFE devices. First, a thermal oxidation was performed to form a 0.3 μm-thick SiO_2 layer on the 2.5 μm-thick n^{++} active (100) silicon layer of the SOI wafer. The highly conductive active silicon layer of the SOI was initially utilized as the mold and finally as the gate layer. The thickness of the active silicon layer must be properly designed to match the base width of pyramid microtip. The thermal-SiO_2 thickness of 0.3 μm was chosen for two reasons, (i) a thin SiO_2 is required in order to minimize the lateral etching and better control the microtip size and (ii) a sufficiently thick SiO_2 is needed as a hard mask during the anisotropic etching of silicon with potassium hydroxide (KOH) solution. The etching selectivity of silicon over SiO_2 by KOH is normally around 10 to 100 depending on KOH concentration and temperature. For a 2-μm based pyramidal cavity used in this research, the cavity depth is ~ 1.5 μm. Assuming a minimum etching selectivity of 10, the minimum thermal-SiO_2 thickness required is ~ 0.15 μm. Hence conservatively, a 0.3 μm-thick SiO_2 layer was used.

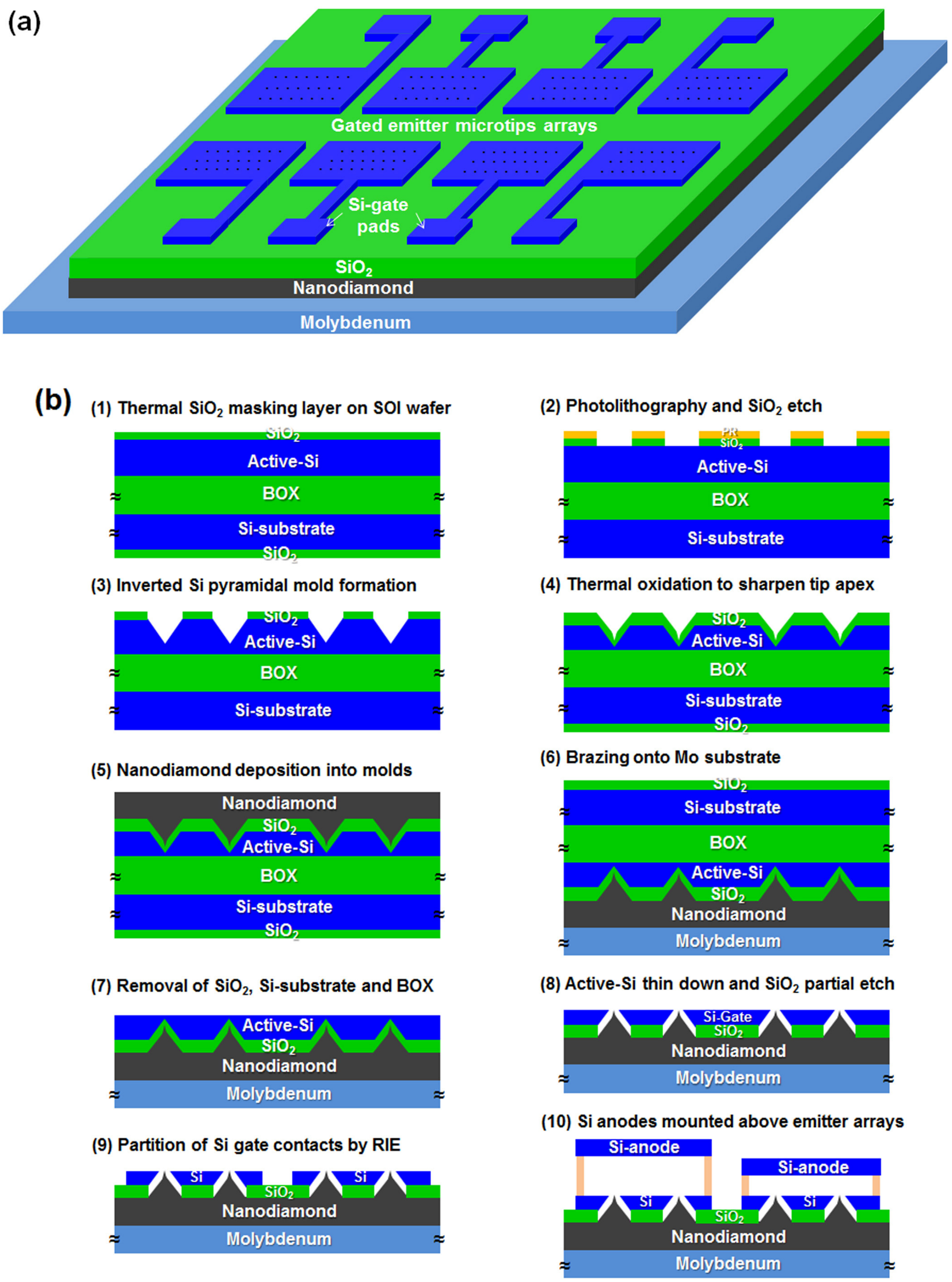


Figure 5.1 (a) Schematic diagram of the gated nanodiamond emitter arrays with separate silicon gate contact pads, constructed on a chip brazed onto a Mo substrate. (b) Fabrication flowchart of the three-terminal nanodiamond VFE devices.

Conventional photolithography micropatterning was then used to define an array of square pattern with base width of 2 μm x 2 μm for the nanodiamond pyramidal microtips. The 0.3 μm-thick thermal-SiO_2 in the patterned area was then etched away by buffered oxide etching (BOE) solution, followed by removal of the photoresist. Subsequently, the revealed active silicon surface in the patterned area was anisotropically etched using potassium hydroxide solution diluted in deionized water (volume ratio of 1:1) at 60 ˚C to form an inverted pyramidal cavity as the remaining 0.3 μm-thick thermal-SiO_2 acted as hard mask. This anisotropic silicon etching step is an etch-stopped process owing to the higher etching rate of KOH solution on silicon (100) plane than on (111) plane, and thereby forming an inverted pyramidal structure which consists of four (111) planes with side edges at a 54.7 degree angle from the surface. The remaining thermal-SiO_2 layer was then completely removed by BOE solution.

Based on structural geometry, the relationship between the base width (W) and the height (H) of the inverted pyramidal cavity can be determined and expressed by:

$$H = \frac{W}{\sqrt{2}}. \tag{5.1}$$

As the base width of the pyramidal mold was defined to be 2.48 μm, the corresponding height was approximately 1.75 μm, as shown in the SEM micrograph in **Figure 5.2**. It is observed that a silicon undercut of ~ 0.19 μm was formed, indicating the width of square micropattern was defined to be 2.1 μm in photolithography and the base width of pyramidal cavity increased to be 2.48 μm during the anisotropic silicon etching. This increase of base width resulted in a taller pyramidal cavity by 0.27 μm which is acceptable since a 2.5 μm-thick active silicon layer is selected.

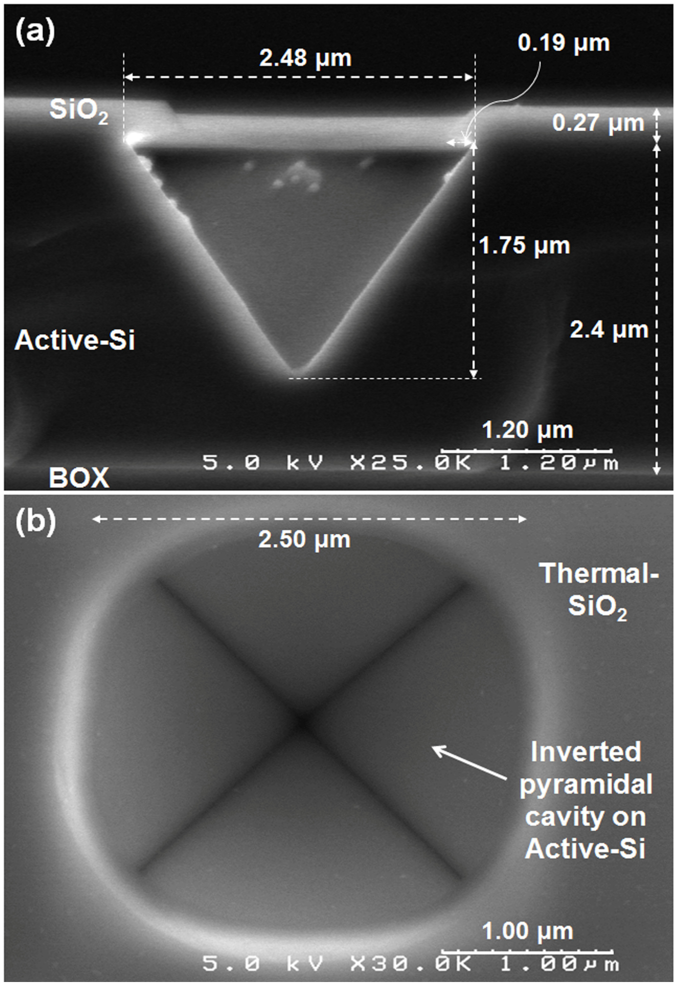


Figure 5.2 SEM micrographs showing (a) the cross-sectional view and (b) the top view of an inverted silicon pyramidal cavity fabricated on the active silicon layer of a SOI substrate.

Next, a second thermal oxidation was carried out at 1100 ˚C on the inverted pyramidal silicon mold cavities to grow a ~ 1 µm-thick SiO_2 layer, which serves as the gate-to-emitter dielectric isolation layer and simultaneously produces ultrasharp apexes at the tips of the inverted pyramidal mold. The thermal oxidation process comprised of three steps including a dry oxidation of 18 hours, followed by a wet oxidation of 1.5 hour and another dry oxidation of 1 hour. The ultrasharp apex occurred due to the higher oxidation rate on (111) than on (100) silicon planes and the limited oxidation reaction and smaller

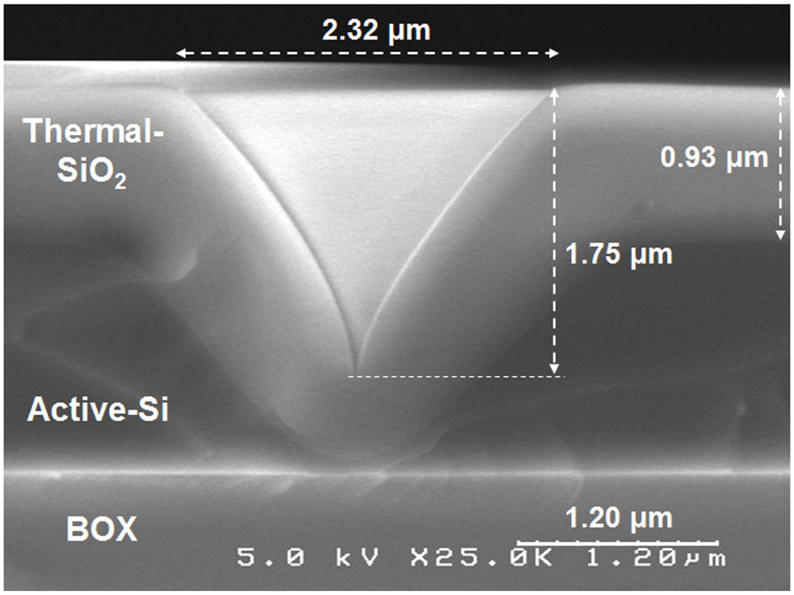


Figure 5.3 A cross-sectional viewed SEM micrograph of an inverted SiO_2 pyramidal mold with ultra-sharp apex formed by thermal oxidation.

oxidation rate in the confined region, the apex of pyramidal mold. It has been found that increasing the SiO_2 thickness would improve the sharpness of the inverted mold apex, and thereby enhance the geometric field enhancement factor of the emitter tip. Nevertheless, a thicker SiO_2 would increase the gate-to-emitter distance, leading to a higher threshold gate voltage. Besides, it is unpractical to grow dry SiO_2 layer thicker than 1 μm since it requires ~ 48 hours at the standard growth temperature of 1100 ˚C. Therefore, the thermal-SiO_2 thickness of 1 μm was chosen for optimum tip sharpness and moderate gate-to-emitter spacing. **Figure 5.3** displays the cross-sectional SEM micrograph of an inverted pyramidal mold with an ultrasharp apex formed by thermal oxidation process. Then, nanodiamond is deposited into the mold to form the ultrasharp nanodiamond emitter tip, which is self-aligned to the active silicon layer that acts as the gate electrode. Thus, this fabrication process is so called the mold-transfer self-aligned gate-emitter technique. This sharpened apex with small radius of curvature creates a high aspect ratio, assisting the formation of concentrating equipotentials on top of the tip and thereby enhancing the electric field and facilitating the electron field emission from the tips.

5.1.3 Deposition of nanocrystalline diamond into the molds

The nanocrystalline diamond films were deposited into the molds in an ASTeX® microwave plasma enhanced CVD system with a 1.5 kW generator operating at 2.45 GHz. **Figure 5.4(a)** shows the schematic of a typical MPECVD system. The substrate temperature was set by an induction heater independent of the plasma, and the reaction chamber was coupled with a controlled gas handling system which allows precise control of the process gas flow rates. This MPECVD system is employed in this study for the fabrication of a nanodiamond pyramidal emitter microtip array.

The as-prepared inverted pyramidal mold cavities were pretreated by surface polishing, using ultrasonication in nano-scaled (5 – 20 nm) diamond powder suspension in acetone solution, to enhance diamond nucleation sites. The mold substrate was then cleaned and rinsed with acetone followed by methanol and DI-water, and subsequently transferred into the MPECVD chamber which was evacuated to a base pressure of 10^{-2} Torr. A two-step synthesis process, including nucleation and growth stages, was performed to achieve a conformal deposition of the nitrogen-incorporated nanodiamond into the mold substrate. The chamber was first purged and filled with hydrogen while the substrate heater was heated up to 800 ˚C. The H_2-rich plasma was then initiated with a microwave power of 550 W at a reactant pressure of 13 Torr, followed by introducing the precursor gases of methane and nitrogen. This low-pressure low-power process, called

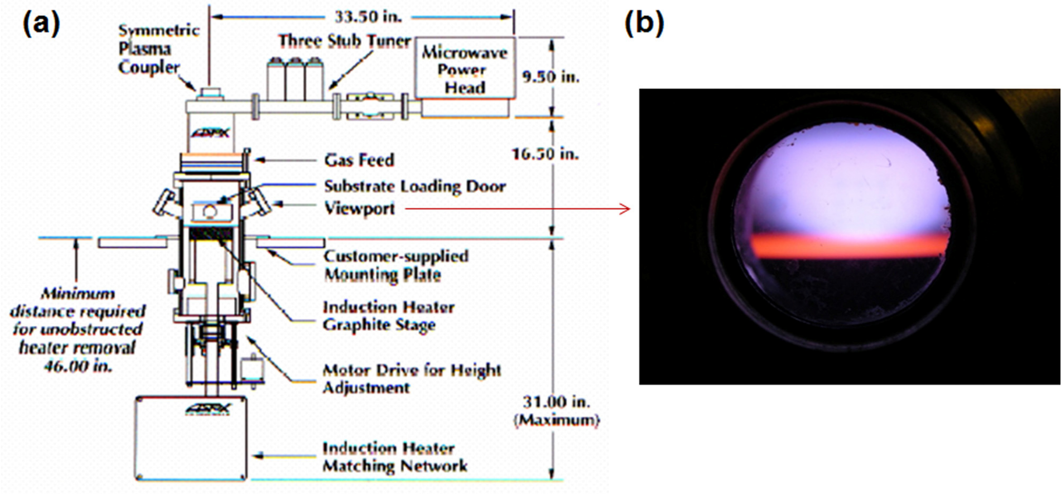


Figure 5.4 (a) Schematic diagram of a typical ASTeX® MPECVD system [145]. (b) Snapshot of the $CH_4/N_2/H_2$ plasma during nanodiamond deposition.

the nucleation stage, was continued for 2 hours. It has been experimentally demonstrated that an effective method to grow nanocrystalline diamond is to increase the nucleation rate and decrease the growth rate by adjusting the microwave power and reactant pressure. During diamond growth, diminishing the microwave power would reduce the plasma energy and decreasing the reactant pressure would spread out the microwave plasma in the chamber. Thus, under the low-pressure and low-power condition where the reaction is starved, the nucleation density would increase and the grain size would reduce [128,174]. This produces a high density of nano-sized and fine diamond grains aggregating on the mold substrate to initiate the nanodiamond film growth, facilitating the synthesis of a thin, continuous and smooth layer of CVD nanodiamond.

After the 2–hour nucleation stage, the microwave power and reactant pressure were increased to 1000 W and 28 Torr, respectively, while the substrate temperature and gas flow rates were kept the same. This process with higher microwave power and higher pressure, called the growth stage, was continued for another 10 hours. The resultant CVD nanodiamond film grown on the mold substrate was examined using an SEM, revealing that the conformal deposition of nanodiamond films has completely filled the inverted pyramidal mold cavity, as shown in **Figure 5.5**. In addition, it was clearly observed that the two-step growth process produces a continuous and smooth nanodiamond thin film with very small grain size of 5 – 10 nm, as shown in **Figure 5.6**. The small grain size and conformal deposition of nanodiamond film are very important for filling the ultrasharp apex of the inverted pyramidal mold with nanodiamond, constructing the nanodiamond microtip with ultrasharp apex. The electrical resistance measurements of the nanodiamond film using a multimeter probing on the gold electrodes placed on the nanodiamond surface revealed a resistance of 1 – 10 kΩ. This relatively higher electrical conductivity of nanodiamond synthesized by $CH_4/N_2/H_2$ MPECVD, compared to that of undoped microdiamond, can be attributed to the incorporation of nitrogen in the synthesized nanodiamond film. To enhance the conductivity and support, a thick boron-doped diamond film was then grown on the nanodiamond film using a $CH_4/H_2/C_3H_9B$ gas mixture under 130 Torr with 5 kW microwave power at a growth temperature of 800 °C to provide a highly conductive (~ 10 **Ω**) support layer. The diamond-filled mold was then coated with a composite layer of sputtered titanium and nickel to form the back metal contact and brazed onto a molybdenum handling substrate using a titanium-copper-silver (ticusil) brazing alloy, with the diamond/metal side facing the brazing material. The Ti/Ni bilayer provided strong metallurgical adhesion with diamond and facilitated the brazing of diamond onto the Mo substrate, while the ticusil layer provided good metal contact between diamond and Mo substrate after being melted at 900 °C in vacuum of 10^{-7} Torr and solidified upon cooling.

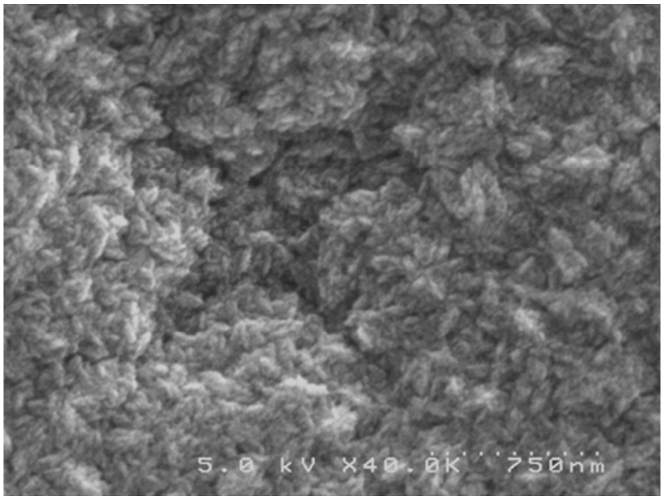


Figure 5.5 A top-viewed SEM image of a nanodiamond filled inverted pyramidal mold cavity.

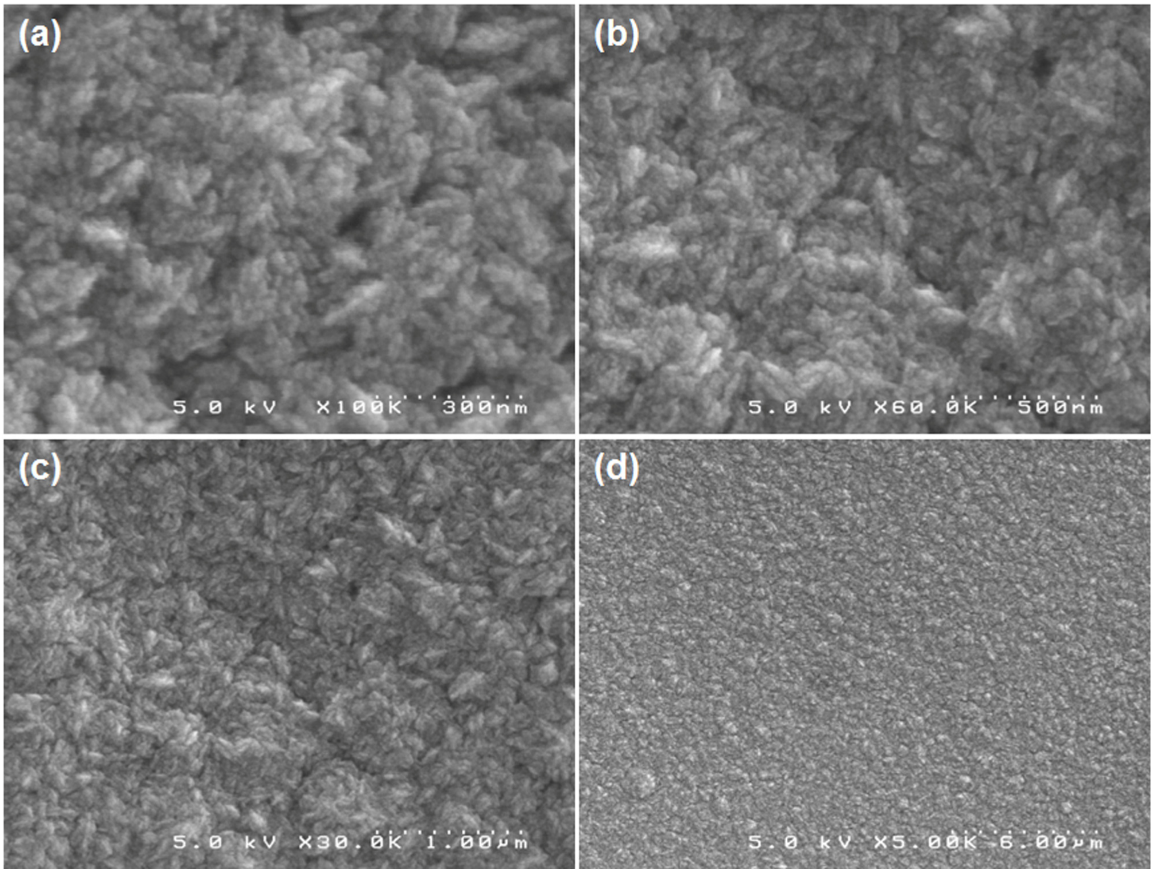


Figure 5.6 SEM micrographs of the as-deposited nanocrystalline diamond film on the mold substrate with average grain size of 5 – 10 nm grown by the $CH_4/N_2/H_2$ MPECVD process at different magnifications: (a) 100 kX, (b) 60 kX, (c) 30 kX, and (d) 5 kX.

5.1.4 Realization of nanodiamond VFE transistors and triodes

The schematic of the nanodiamond filled pyramidal mold mounted on the Mo substrate is shown in step (6) of device fabrication scheme, **Figure 5.1**. The top of nanodiamond microtips were covered with the handling silicon substrate and buried oxide (BOX) of the SOI wafer where the inverted pyramidal molds were initially built on. Therefore, a series of wet etching was performed to remove these layers in order to reveal the nanodiamond microtips as well as the active silicon layer. The 525 µm-thick handling silicon substrate was etched away using KOH solution diluted in DI-water (volume ratio of 1:1) at 70 ˚C. Subsequently, the 4 µm-thick BOX layer was completely etched with a controlled etch rate by using BOE solution, a mixture of hydrofluoric acid (HF) and ammonium fluoride (NH_4F). The NH_4F containing etch gives a smoother silicon surface than HF. Next, the active silicon layer was thinned down from a thickness of 1.4 µm as shown in **Figure 5.3** to ~ 0.8 µm by the hydrofluoric acid and nitric acid (volume ratio of 1:30) mixture with an etching rate of ~ 0.013 µm/s. This silicon thin down process was well controlled, providing uniform silicon gate openings and an optimized proximity of gate to emitter tips by self-alignment. The protruded thermal-SiO_2 dielectric layer around the tip region was then etched away using a BOE solution diluted in DI-water to reveal the sharpened nanodiamond pyramidal tip, forming the structure of nanodiamond tips surrounded by self-aligned silicon gate with a radial free-spacing of ~ 0.9 µm in-between. This accomplished several arrays of nanodiamond emitters integrated with a common silicon self-aligned gate on a single chip.

In order to construct individual nanodiamond VFE devices from the fabricated emitter array, a second photolithography micropatterning along with silicon reactive ion etching (RIE) was executed to partition the silicon gate into individual gate electrodes and contact pads. The silicon partitioning was performed with a dry-etched RIE process using a gas mixture of sulfur hexafluoride (SF_6) and oxygen (O_2) at 150 mTorr with RIE power of 200 W, pre-patterned with photoresist. The silicon RIE step partitioned the silicon gate and formed individual nanodiamond VFE devices with separate contact pads on a single chip, enabling further implementation of the devices into the vacuum-based circuit building blocks, as shown by step (9) of device fabrication scheme in **Figure 5.1**. The SEM micrograph of gated nanodiamond emitter arrays with separated gate and electrical contact pads is shown in **Figure 5.7**. In addition, this process step reduced the device effective area and the overlapping area between gate to emitter, thereby minimizing the gate-emitter capacitance and enhancing high frequency response. Finally, highly conductive silicon anodes were separately mounted above each VFE device with various anode-to-emitter distances, accomplishing nanodiamond VFE transistors and triodes on a single chip. The variation of anode-to-emitter spacing was realized by using different thicknesses of insulating spacers.

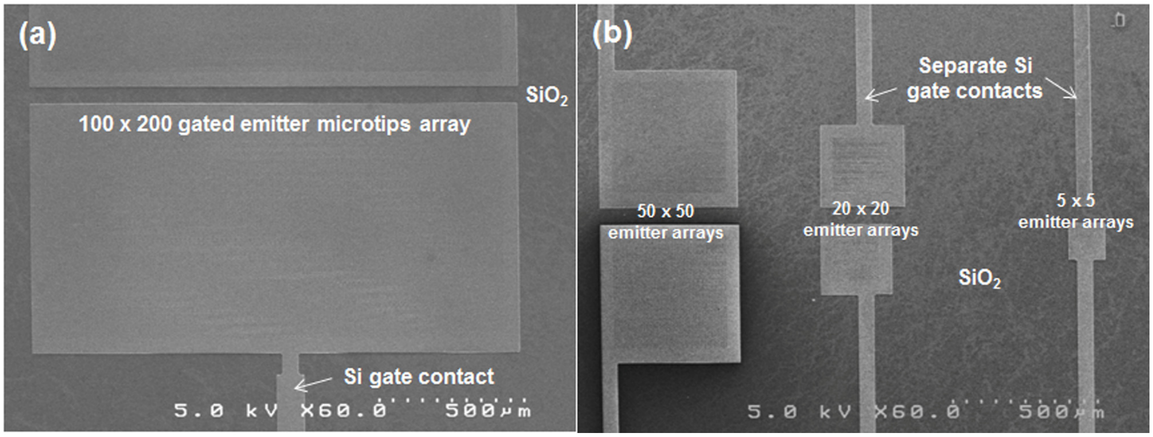


Figure 5.7 SEM micrographs of gated nanodiamond emitter arrays with different array size ranging from (a) 100 x 200, (b) 50 x 50, 20 x 20, and 5 x 5. Each has individual gate contact pad.

5.1.5 Implementation of nanodiamond VFE integrated differential amplifier

The practical implementation of vacuum ICs has been considered by the deployment of nanodiamond VFE transistors on a chip. The vacuum-based diff-amp is composed of two identical nanodiamond emitter arrays integrated with partitioned silicon gates and split silicon anodes. The layout of the vacuum-based diff-amp chip in this study was designed to have eight identical VFE transistors on a 1 cm x 1 cm chip, each has 80 x 80 nanodiamond emitter microtips with individual gate and anode contacts, as shown schematically in **Figure 5.8**. The layout of eight 80 x 80 emitter arrays was chosen in order to be able to easily place multiple metal probes on the diff-amp in our current characterization probe station and also to have appropriate emission current from the emitter array. The nanodiamond VFE transistors with the same emitter array size and device structural geometry were constructed using a well-controlled dual-mask microfabrication process, similar to the process flow of nanodiamond VFE transistors as described earlier. The anode-to-emitter distance in every transistor was determined by the thickness of alumina spacers where the silicon anode was placed on, which is 600 μm. Since these eight nanodiamond VFE transistors are geometrically identical, any two of them can be utilized for diff-amp characterization.

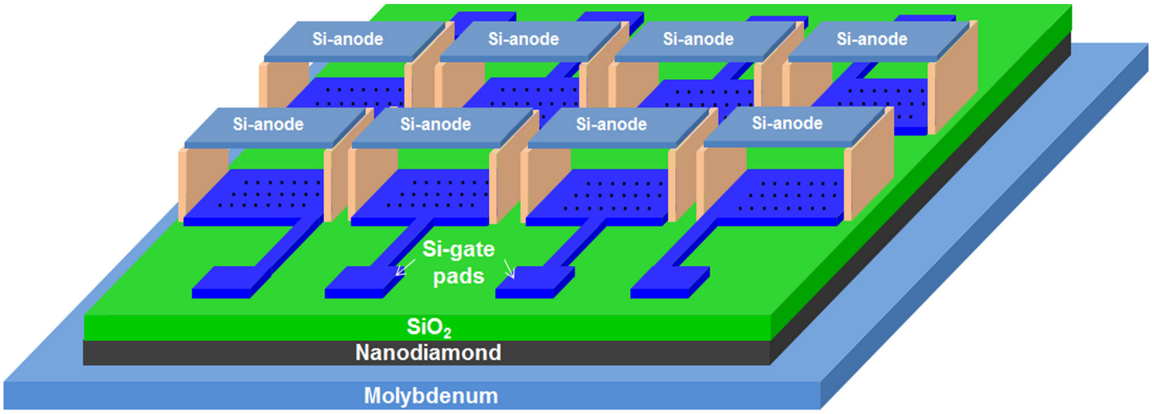


Figure 5.8 Schematic diagram of a vacuum-based differential amplifier chip, possessing multiple VFE transistors with separate gate and anode contacts.

5.2 Structural and Material characterization

The SEM examination of the fabricated device revealed the formation of uniform gate openings over the whole emitter array, as shown in **Figures 5.9** and **5.10**, and the ultrasharp pyramidal nanodiamond tip apex was found to be well-aligned to the integrated silicon gate, as shown in **Figure 5.9(d)**. The gate opening was determined not only by the thermal-SiO_2 thickness but also by the silicon thinning down process. If the active silicon layer is thinned down insufficiently, the silicon gate opening would be smaller and its surface would be at a higher elevation than the emitter tip, which might lead to the electron collection at the gate during electron emission and thereby a gate interception current. On the other hand, if the active silicon layer is thinned down more than enough, the silicon gate opening would be larger and its surface would be at a lower elevation than the emitter tip, which might result in the inefficient gate control over electron emission due to the large distance between gate and emitter tip. Therefore, in this research, an optimized silicon gate position with the close proximity to the nanodiamond emitter tip was achieved by the well controlled silicon thin down process in order to have efficient gate modulation on electron emission and negligible gate intercept current. **Figure 5.11** displays the tilted-view SEM micrographs of part of the fabricated nanodiamond emitter microtip array with self-aligned silicon gate, and a high magnification of a gated emitter. It can be clearly observed that the silicon gate surface is at the same level as the apex of emitter tip with an optimum proximity of silicon gate edge to emitter tip. This is important for having efficient gate manipulation over electron emission from nanodiamond emitter tips and for minimizing gate-intercepted current.

The fabricated adjacent nanodiamond VFE transistor pair for the diff-amp was examined under SEM, as shown in **Figure 5.12(a)**. The transistor pair has separated silicon gate contacts sitting on the SiO_2 isolation layer. **Figure 5.12(b)–(d)** shows part of the nanodiamond emitter microtip array and the corresponding high magnification of the transistor. Under high magnification, the transistor pair clearly exhibited identical gate-to-emitter spacing of ~ 1 μm and uniform nanodiamond tip sharpness, with more than 90% yield. The uniform gate-to-emitter spacing with well-formed nanodiamond emitters is crucial to acquiring an identical transistor pair with well-matched electrical characteristics for practical diff-amp implementation.

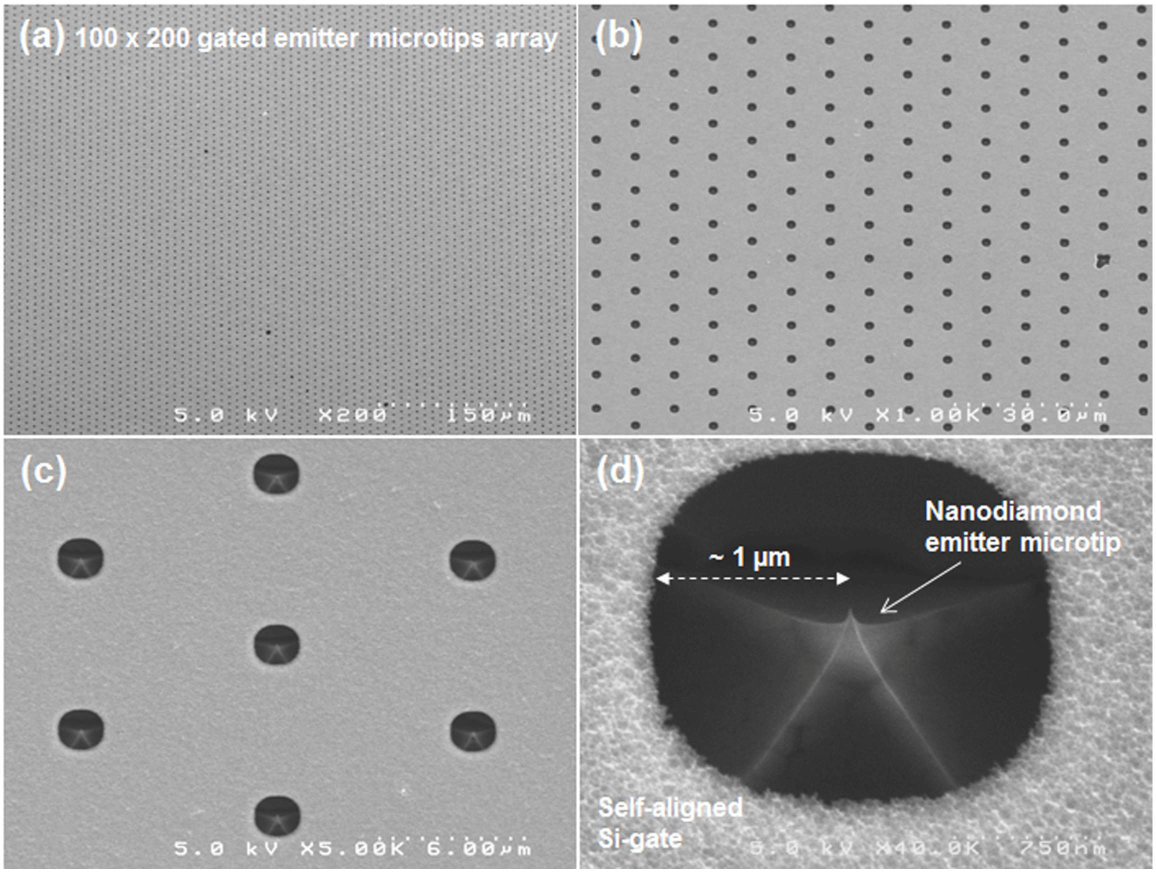


Figure 5.9 Top-viewed SEM micrographs of a 100 x 200 gated nanodiamond emitter microtips array taken at different magnifications: (a) 200 X, (b) 1 kX, (c) 5 kX, and (d) 45 kX.

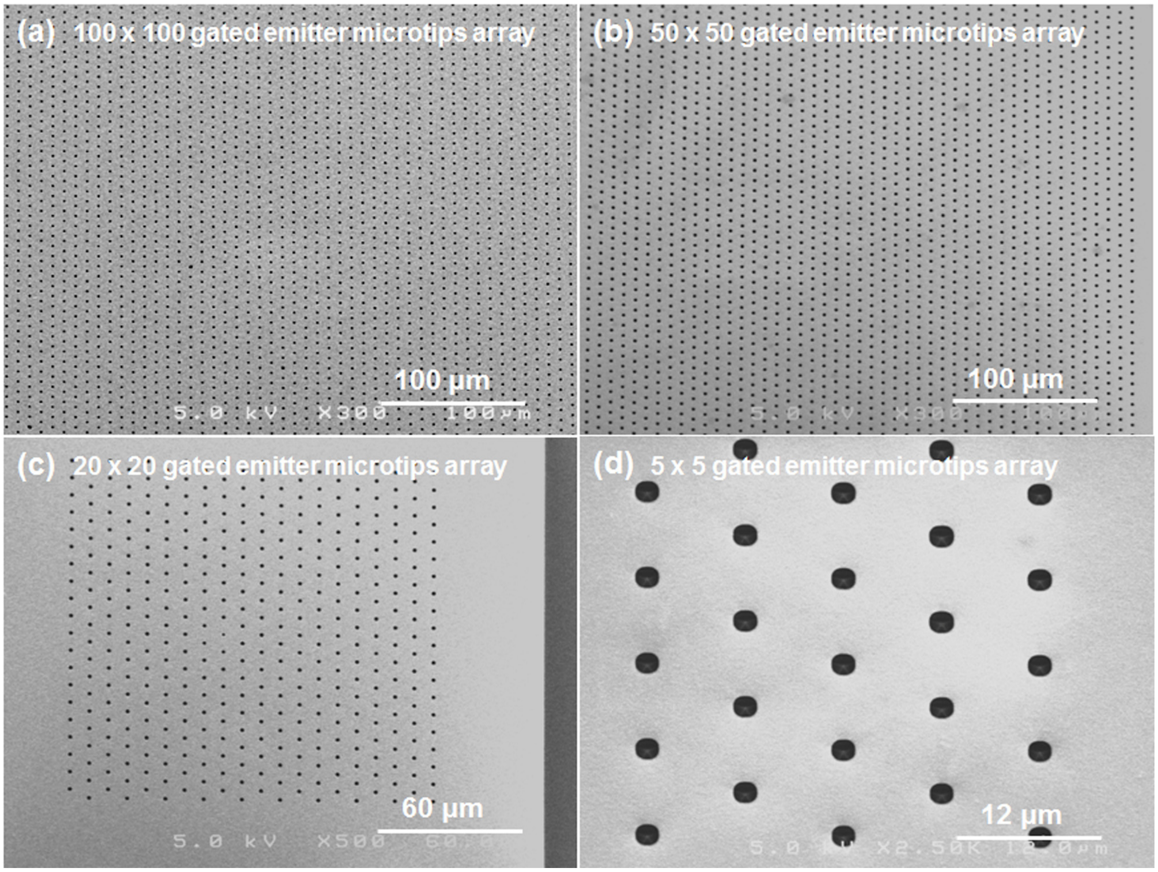


Figure 5.10 Top-viewed SEM micrographs of gated nanodiamond emitter microtips arrays with different array size of (a) 100 x 100, (b) 50 x 50, (c) 20 x 20, and (d) 5 x 5.

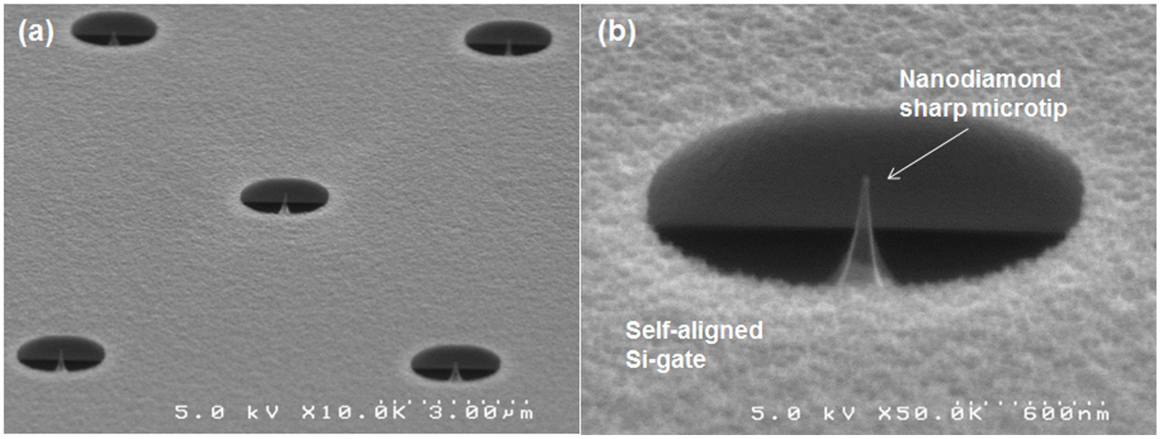


Figure 5.11 (a) Tilted-viewed SEM micrograph of part of the nanodiamond emitter microtip array with self-aligned silicon gate. (b) A high magnification image of a single nanodiamond microtip, showing the close proximity of silicon gate to emitter tip.

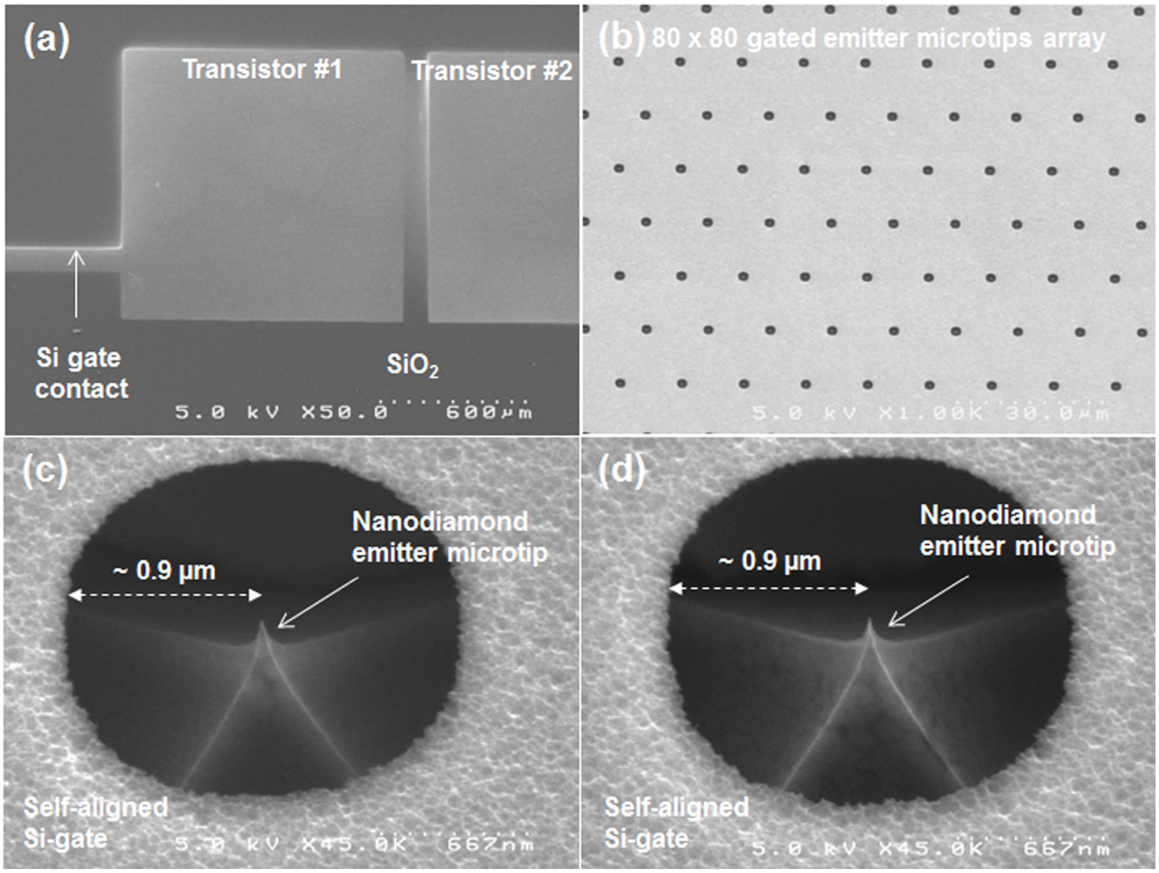


Figure 5.12 Top-viewed SEM micrographs of (a) a pair of nanodiamond VFE transistors for diff-amp and (b) part of the nanodiamond VFE transistor. (c) and (d) display a single nanodiamond emitter with self aligned silicon gate from transistor #1 and #2, respectively, showing well-matched microtip structure and similar gate opening.

The elemental composition of the nitrogen-incorporated nanodiamond emitter surface was analyzed by Raman spectroscopy, a non-destructive diagnostic tool widely used for evaluation of CVD diamond films. The visible Raman spectrum of the nanodiamond emitters was taken utilizing a Thermo Scientific DXR Raman microscope with an excitation wavelength of 532 nm and an excitation power of 2 mW, while the UV Raman spectrum was taken using an excitation wavelength of 325 nm with an excitation power of 6 mW. In order to perform Raman study on the nanodiamond emitter, the silicon gate and SiO_2 isolation layer of the VFE transistor were wet-etched away using

KOH and BOE solutions, respectively, followed by a RCA cleaning procedure to remove any contaminants present on the emitter surface during the wet etching. The bare nanodiamond emitter microtip array is displayed in **Figure 5.13** with a high magnification micrograph of a single emitter tip shown in the inset, revealing the well-controlled CVD nanocrystalline diamond deposition into the inverted pyramidal molds and formation of the nanodiamond pyramidal microtips. The visible and UV Raman examinations were then performed on the nanodiamond pyramidal emitter surface. Both spectra, as shown in **Figure 5.14** and **Figure 5.15**, exhibited the sp^3 diamond peak at 1332 cm^{-1} and the sp^2 graphitic peak at 1550 – 1580 cm^{-1}, demonstrating the existence of sp^2 and sp^3 hybridized carbons in the nanodiamond emitter tips. The broad feature detected at ~ 1140 cm^{-1} in visible Raman spectrum and the small peak at ~ 1160 cm^{-1} in UV Raman spectrum indicated the nanocrystalline phase existing in the emitter tips, possibly attributive of the disordered sp^3-bonded carbon distributed in the nano-dimensioned grain boundaries. These Raman spectra displayed the typical characteristics of a nitrogen-incorporated nanocrystalline diamond film with a broad sp^3-diamond peak and a higher sp^2-shoulder [149], as discussed in **Section 3.3**. The sp^3/sp^2 peak intensity ratio was found to be ~ 0.86 in visible Raman spectrum. Although having a large sp^2-bonded carbon peak, the nanodiamond emitter tip still retains a highly sp^3-bonded diamond structure because the sp^2-bonding has almost 50 times larger Raman scattering cross section and thus higher scattering efficiency than sp^3-bonding in visible excitation wavelength [149]. Our UV Raman spectrum is consistent with other researchers' results that an intense sp^2-graphite peak along with a moderate sp^3-diamond peak was obtained in UV Raman spectrum recorded from a nanodiamond film grown with 1% CH_4 / 10% N_2

/ 89% Ar [149]. It has also been observed that the sp^3/sp^2 peak intensity ratio in UV Raman spectrum decreases as more N_2 is added in the precursor gas mixture. Besides, it has been demonstrated that the degree of sp^2-carbon content in the diamond film depends upon the grain size and the plasma chemistry [128]: the sp^2-carbon content increases as the grain size decreases and as the nitrogen was added in the plasma chemistry. This phenomenon can be attributed to that nitrogen preferentially enters the network of grain boundaries and promotes new electronic states associated with sp^2-bonds in the neighboring carbon atoms [87,128,178]. The fabricated nanodiamond emitter tips consist of a high degree of sp^3-bonded carbons with deliberate inclusion of sp^2-carbon, which has been demonstrated to enhance the electron transport and electron field emission as explained in **Section 2.3.2**.

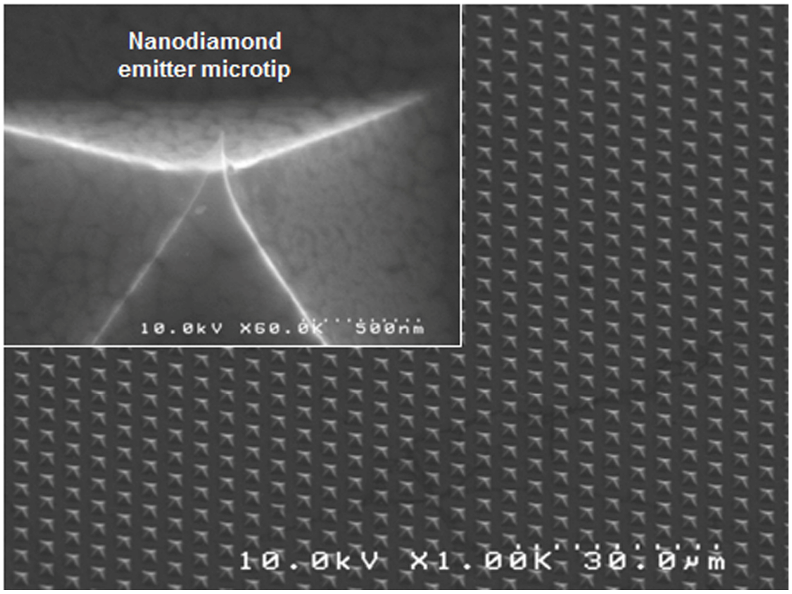


Figure 5.13 Top-viewed SEM micrographs of an array of nanodiamond emitter microtips after the removal of silicon gate and thermal-SiO_2 layer for Raman test. Inset shows one of the nanodiamond microtip with sharp apex.

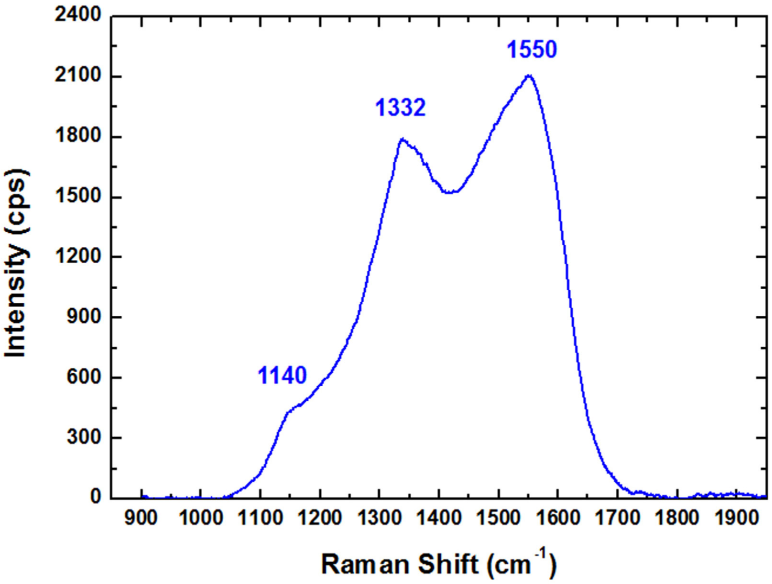


Figure 5.14 Visible Raman spectrum (532 nm) obtained from the surface of a nitrogen-incorporated nanodiamond pyramidal emitter microtip.

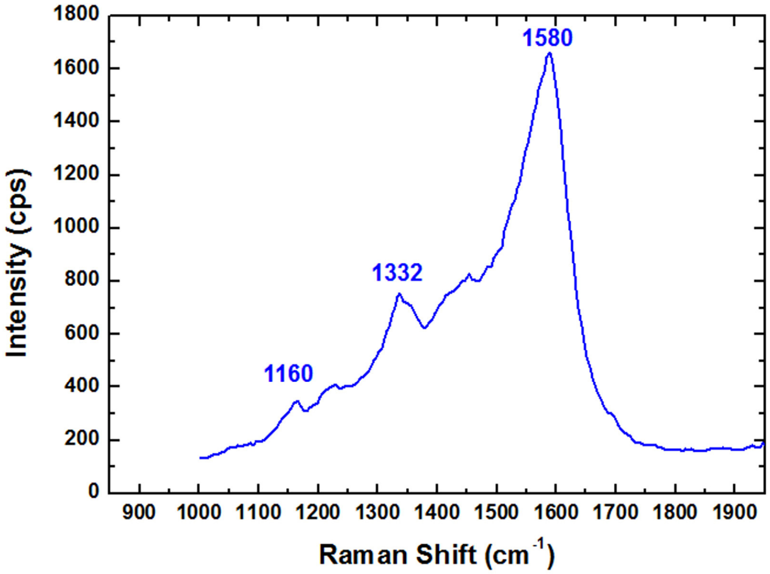


Figure 5.15 UV Raman spectrum (325 nm) obtained from the surface of a nitrogen-incorporated nanodiamond pyramidal emitter microtip.

5.3 Device characterization techniques

5.3.1 Electrical characterization of nanodiamond VFE transistors and triodes

The field emission characterization of the fabricated nanodiamond VFE transistors and triodes was performed in a vacuum of ~ 10^{-7} Torr at room temperature. The testing circuit for *dc* electrical characteristics of the device in a common emitter configuration is shown in **Figure 5.16**. A resistor R_a was used as a *dc* load in the anode circuit, while a resistor R_g was used to limit the gate leakage current in case of short circuit in the gate circuit. All of the anode, cathode and gate electrodes were electrically connected to the circuit via metal probes in the vacuum system. Prior to emission characterization, the nanodiamond VFE device was subjected to a series of in-situ vacuum tip conditioning by means of vacuum-thermal-electric (VTE) treatment to remove water vapor or other residual adsorbates which accumulated on the device surface during the terminus of device processing or by exposure to ambient. The device was first thermal treated by slowly heating up and maintaining at 500 °C for several hours using a button heater stage, followed by cooling down slowly to room temperatue. Subsequently, the device was heated up to 300 °C while the anode and gate voltages were applied to obtain an emission current of ~ 10 μA from the nanodiamond emitter tips. The emission current was kept at ~ 10 μA by adjusting the applied gate voltage as temperature was slowly increased and maintained at 500 °C. The VTE treatment was usually continuous for an hour or more to execute more localized cleaning of the nanodiamond emitter microtips. The tip conditioning treatment was terminated when a stable current was obtained for a period of time. After the emitter conditioning, the device was then cooled down and tested at room temperature.

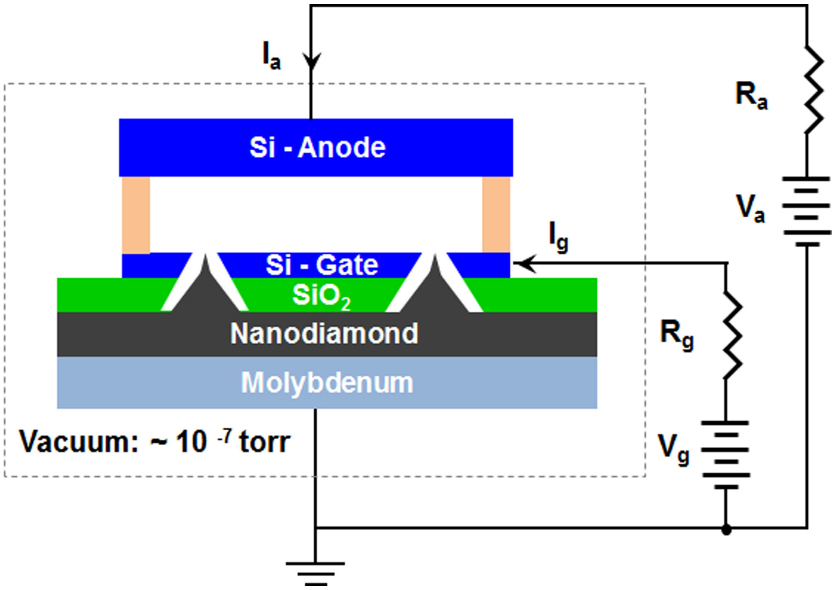


Figure 5.16 Schematic diagram of the *dc* field emission test circuitry for the nanodiamond VFE transistor and triode in a vacuum system.

The emission current collected by the anode (I_a) and by the gate (I_g) were measured as a function of the anode voltage (V_a) and gate voltage (V_g) utilizing a downward sweep method with an integration interval of 30 seconds for each bias condition by a computerized data acquisition system. The testing procedures varied depending on the operation mode. In transistor operation, the electron emission is triggered by the nearby gate voltage and collected by the relatively far away high anode voltage. Thus, as the device operated in transistor mode, a moderate V_a was first applied without inducing the electron emission from the emitters. Then, the V_g was slowly increased to extract electrons from the nanodiamond emitter microtips. Upon the emission induced by V_g, the electrons were accelerated to the anode as the V_a was usually set to be higher than V_g. As the emission current stabilized, the current recording was performed. For each set of I_a and I_g, the V_a was scanned manually while keeping V_g constant. The same measurement was repeated for every V_g value to attain a complete set of data. On the other hand, in triode operation, the electron emission from the nanodiamond emitter is induced by the anode voltage located in close proximity to the emitter and modulated by gate voltage. Hence, as the device operated in triode mode, the positive V_a relative to the emitter was first applied and increased to extract electrons from the emitter. As a significant anode current was perceived, the V_g was altered from positive to negative biases and the corresponding anode current modulation was measured. For each set of emission current, the V_g was scanned manually while V_a was kept constant. The same measurement was repeated for every V_a value to attain a complete set of data. The emission characteristics of transistors and triodes were obtained by plotting the anode current as a function of gate and anode voltages.

Thereafter, the *ac* performance of the device was characterized utilizing the test setup as shown in **Figure 5.17** with preselected V_a and V_g for *dc* biasing the device. The two high-voltage capacitors (C_1 and C_2) were used for *dc* blocking and *ac* signal coupling. An *ac* sinusoidal signal input voltage (v_{in}) from a function waveform generator was superimposed on *dc* gate voltage, while the corresponding *ac* output voltage (v_{out}) was measured across a load resistor (R_L). The input and output signals were recorded simultaneously by a dual-channel digital oscilloscope. The *ac* small signal voltage gains of the transistor and triode were then determined by the ratio of v_{out} to v_{in} at a chosen operating condition.

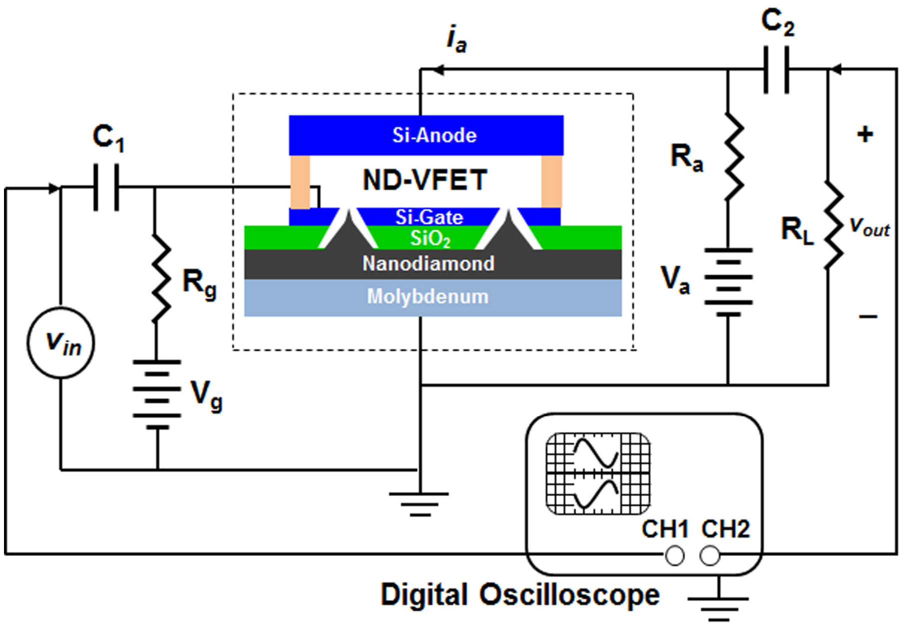


Figure 5.17 Schematic diagram of the *ac* signal amplification test circuitry for the nanodiamond VFE transistor and triode in a vacuum system.

5.3.2 Electrical characterization of nanodiamond VFE differential amplifier

The schematic testing circuit for characterizing the nanodiamond VFE diff-amp is shown in **Figure 5.18**. The two VFE transistors on the chip were first tested separately for *dc* field emission characteristics in a common emitter configuration as described earlier, in order to evaluate the matching transistor pair's electrical behavior. The matching in the device characteristics would determine the usefulness of the transistor pair being employed as a diff-amp. The *ac* signal amplification of the VFE diff-amp was subsequently examined by feeding input signals to the gate electrodes of the transistor pair and recording the output signals at the anode electrodes of the transistor pair. Both transistors were *dc* biased at a predetermined operating point in the saturation region. We defined the *ac* input and output voltages to be v_{in1} and v_{out1} for transistor #1, and v_{in2} and v_{out2} for transistor #2.

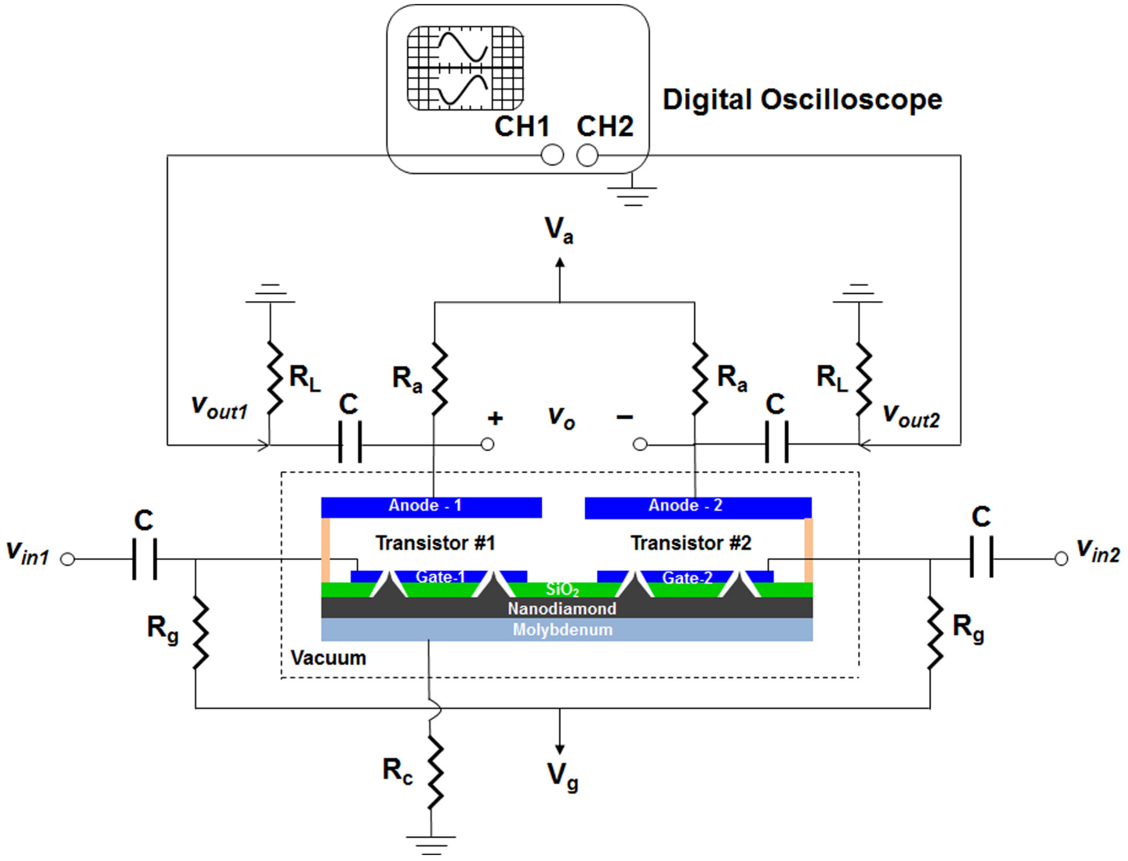


Figure 5.18 Schematic diagram of the testing circuitry for the nanodiamond VFE diff-amp in common-emitter configuration. *DC* bias voltages were applied to operate the pair of transistors in saturation mode. *AC* input small signals were applied through coupling capacitors to gate electrodes, while output voltages were collected at anode electrodes.

In the common-mode test, an *ac* sinusoidal small signal was applied to both gate electrodes, namely, $v_{in1} = v_{in2} = V_p \sin(2\pi ft)$ V, where V_p and f are the amplitude and frequency of the input signal. Based on **Eq. (2.23)**, the common-mode input voltage v_{ic} is equal to v_{in1} and v_{in2}. The corresponding output voltages, v_{out1} and v_{out2}, were then measured across the load resistors R_L and recorded by a dual-channel digital oscilloscope. According to **Eq. (2.24)**, the common-mode differential output voltage v_{oc} is equal to $v_{out1} - v_{out2}$ which was also measured by the oscilloscope utilizing the built-in math function. The common-mode voltage gain A_{cm} of the diff-amp was then determined by v_{oc}/v_{ic}.

Next, for differential-mode operation, the diff-amp was tested utilizing a half-circuit method. The sinusoidal small signal was first applied only to the gate electrode of transistor #1, while no signal was fed to the gate terminal of transistor #2 to achieve a half-circuit differential input, namely, $v_{in1} = \mathrm{V_p} \sin(2\pi ft)$ V and $v_{in2} = 0$ V. The corresponding output signals, v_{out1} and v_{out2}, were also recorded using the oscilloscope. The differential-mode input and output voltages v_{id} and v_{od} are equal to v_{in1} and v_{out1}, respectively, since there is no signal amplified by transistor #2, based on **Eq. (2.25) and (2.26)**. Thus, the half-circuit differential-mode voltage gain $\mathrm{A_{dm1}}$ of the diff-amp was determined by v_{od}/v_{id} which is equal to the voltage gain v_{out1}/v_{in1} of transistor #1. The same procedures were employed on transistor #2 with no signal applied on transistor #1 to acquire a similar half-circuit differential-mode voltage gain $\mathrm{A_{dm2}}$ of the diff-amp, but with 180° out of phase. Finally, the value of common-mode-rejection ratio CMRR was determined by its definition, $|\mathrm{A_{dm}}/\mathrm{A_{cm}}|$, given in **Eq. (2.27)**.

CHAPTER VI

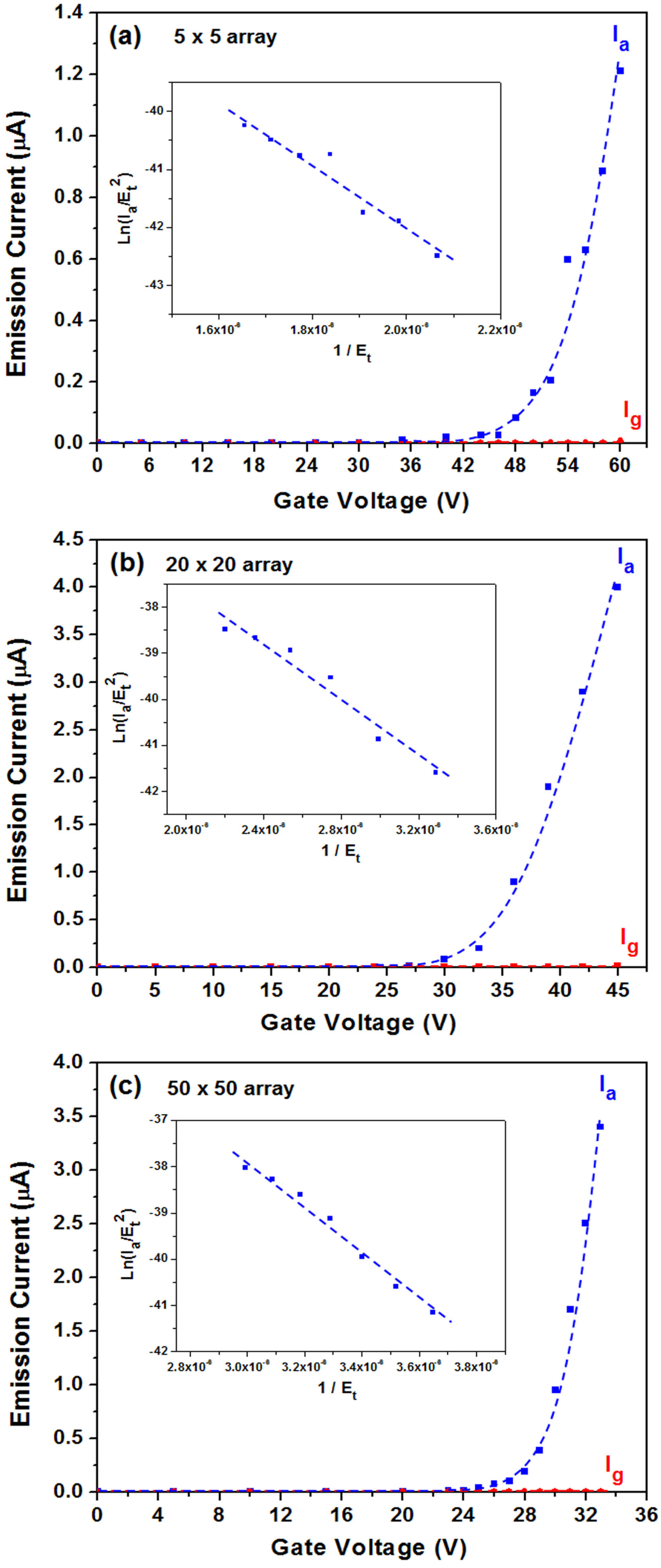
DEVICE CHARACTERIZATION RESULTS and DISCUSSIONS

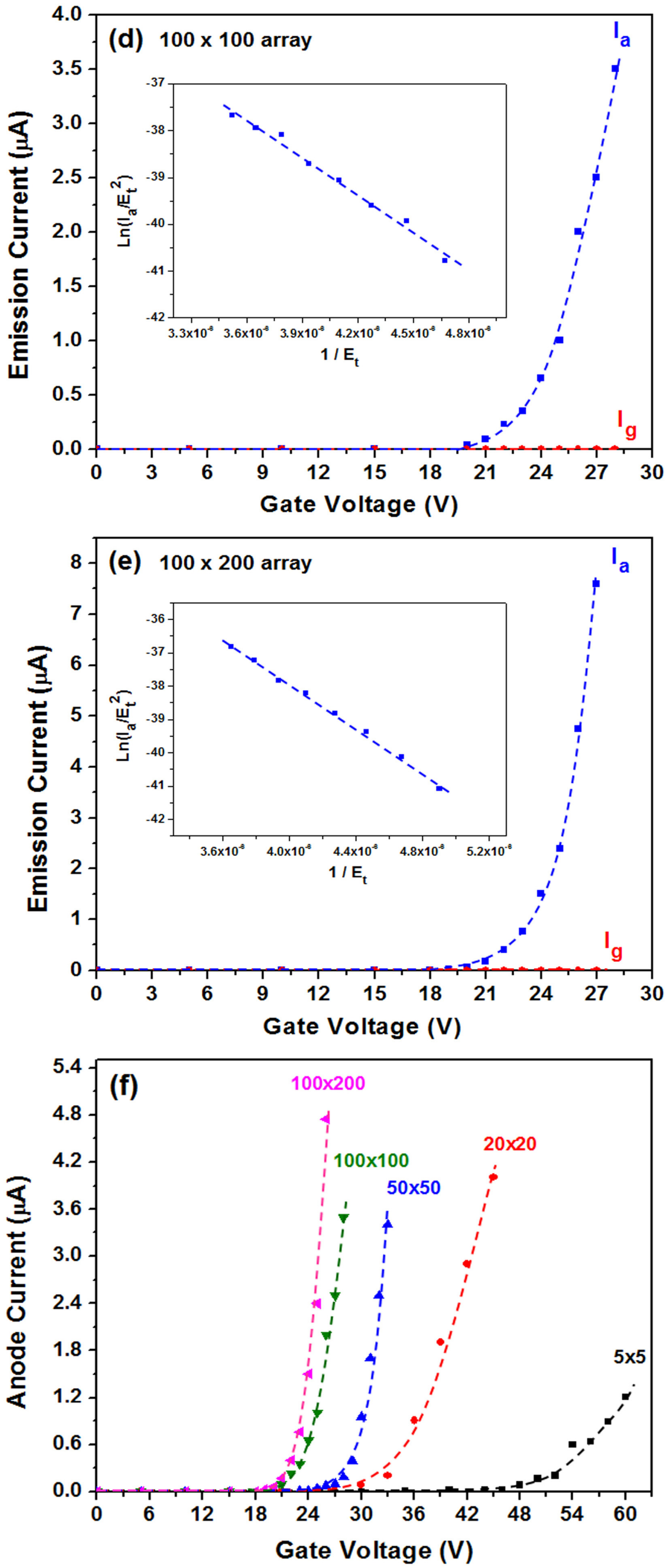
This chapter presents the electrical performance of the fabricated nanodiamond vacuum field emission transistors, triodes, and differential amplifiers, along with the analysis of their electrical characteristics based on modified Fowler-Nordheim theory.

6.1 VFE transistors with different nanodiamond emitter array sizes

The vertically-configured nanodiamond VFE transistors with different emitter array sizes of 5 x 5, 20 x 20, 50 x 50, 100 x 100, and 100 x 200 were tested individually in vacuum by means of the characterization techniques described in **Section 5.3.1**. The anode electrode of each transistor was mounted above the emitters with a 600–μm spacer and the anode voltage was kept at 400 V. Their corresponding current versus voltage (I–V) characteristics, as shown in **Figures 6.1(a)–(f)**, were compared. The gate threshold voltage of the transistor is defined as the voltage required to obtain 10 nA of anode current. The 5 x 5 transistor array exhibited the highest gate threshold voltage of ~ 40 V and an emission current of ~ 1.2 μA at a high gate voltage of ~ 60 V. The 20 x 20 transistor array showed a gate threshold voltage of ~ 29 V and it can deliver an emission current of 3.5 μA by a gate voltage of ~ 43 V. As the emitter array size was increased to 50 x 50, the gate threshold voltage was decreased to ~ 25 V and a lower gate voltage of ~ 33 V was able to draw the same emission current of 3.5 μA. As the 100 x 100 emitter array was utilized in the transistor, a further reduced gate threshold voltage of ~ 20 V was observed and it only required a gate voltage of ~ 28 V to obtain 3.5 μA emission current. The device with the largest array of 100 x 200 exhibited the lowest gate threshold voltage of ~ 19 V and delivered a much higher emission current of ~ 7.6 μA at the gate voltage of 27 V. All of these transistors possessed undetectable gate currents during the test, suggesting that the 1–μm thick thermal SiO_2 between gate and emitter can sustain a high voltage up to 60 V and the gate electrode can efficiently manipulate the electron emission from the emitter tips with no gate intercepted currents. The anode current versus gate voltage characteristics of these five different devices were plotted together in **Figure 6.1(f)**, clearly displaying both the reduction of gate threshold voltage and the increase of emission current with the increase of total amount of emitter microtips in the transistor.

The field emission tunneling mechanism was confirmed for all the transistors from their linear Fowler-Nordheim plots of $\mathrm{Ln}(I_a/E_t^2)$ versus $1/E_t$, as shown in the insets of **Figures 6.1(a)–(e)**, where E_t is determined by the electric fields produced by gate and anode voltages based on **Eq. (2.15)**. The F-N plots of these five transistors have equal slopes, approximately -4×10^6 V/cm, as shown in **Figure 6.1(g)**. Based on the natural logarithm of F-N equation, the negative slope of the F-N plot is proportional to $\Phi^{1.5}/\beta$ as described by **Eq. (2.8)**. Therefore, the almost identical slopes of these F-N plots indicate that the nanodiamond emitters in these five transistors possess essentially the same work function Φ and field enhancement factor β, demonstrating the well-controlled fabrication processes for making identical and reproducible nanodiamond emitter microtips in a variety of emitter arrays on a single chip.


(a) 5 x 5 array
(b) 20 x 20 array
(c) 50 x 50 array
I_a
I_g
Emission Current (μA)
Gate Voltage (V)
$Ln(I_a/E_t^2)$
$1 / E_t$
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
0
6
12
18
24
30
36
42
48
54
60
-40
-41
-42
-43
1.6x10^{-8}
1.8x10^{-8}
2.0x10^{-8}
2.2x10^{-8}
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
0
5
10
15
20
25
30
35
40
45
-38
-39
-40
-41
-42
2.0x10^{-8}
2.4x10^{-8}
2.8x10^{-8}
3.2x10^{-8}
3.6x10^{-8}
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
0
4
8
12
16
20
24
28
32
36
-37
-38
-39
-40
-41
-42
2.8x10^{-8}
3.0x10^{-8}
3.2x10^{-8}
3.4x10^{-8}
3.6x10^{-8}
3.8x10^{-8}


(d) 100 x 100 array
I_a
I_g
Emission Current (µA)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
3
6
9
12
15
18
21
24
27
30
Gate Voltage (V)
$Ln(I_a/E_t^2)$
-37
-38
-39
-40
-41
-42
3.3x10^-8
3.6x10^-8
3.9x10^-8
4.2x10^-8
4.5x10^-8
4.8x10^-8
$1 / E_t$
(e) 100 x 200 array
I_a
I_g
Emission Current (µA)
8
7
6
5
4
3
2
1
0
0
3
6
9
12
15
18
21
24
27
30
Gate Voltage (V)
$Ln(I_a/E_t^2)$
-36
-37
-38
-39
-40
-41
-42
3.6x10^-8
4.0x10^-8
4.4x10^-8
4.8x10^-8
5.2x10^-8
$1 / E_t$
(f)
100x200
100x100
50x50
20x20
5x5
Anode Current (µA)
5.4
4.8
4.2
3.6
3.0
2.4
1.8
1.2
0.6
0.0
0
6
12
18
24
30
36
42
48
54
60
Gate Voltage (V)

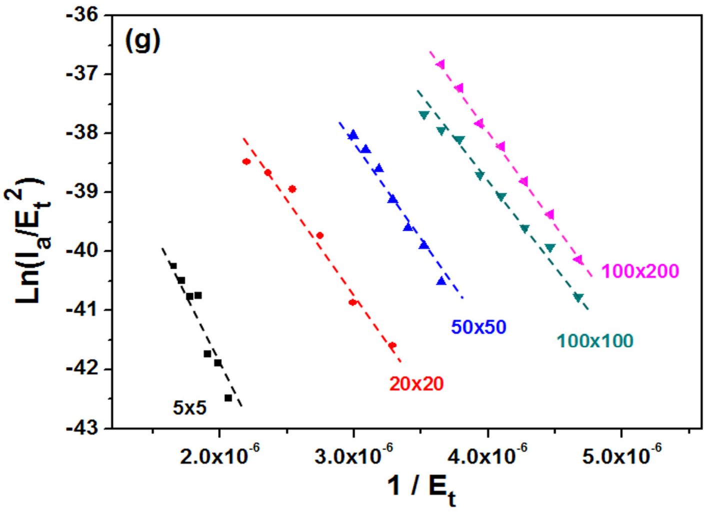


Figure 6.1 Plots of I_a-V_g and I_g-V_g characteristics of the fabricated nanodiamond VFE transistors with the emitter array size of (a) 5 x 5, (b) 20 x 20, (c) 50 x 50, (d) 100 x 100, and (e) 100 x 200. Insets show their corresponding Fowler-Nordheim plots. (f) and (g) display the comparison of I_a-V_g curves and F-N plots, respectively.

6.2 Nanodiamond vacuum field emission transistor characterization

6.2.1 Transistor field emission characteristics

The fabricated nanodiamond VFE transistor with the emitter array size of 100 x 200 was further tested for its electrical characteristics. The anode to emitter spacing was kept at 600 μm. The transistor characterization technique described in **Section 5.3.1** was utilized to measure the emission current as a function of anode and gate voltages and to generate a family I-V curves of the device. **Figure 6.2** shows the plots of anode current and gate current versus gate voltage (I_a-I_g-V_g) at various anode bias conditions. A low gate turn-on voltage, defined as the voltage required to obtain 1 μA of anode current, was observed to be ~ 25 V. The I_a increased exponentially with V_g, which follows the Fowler-Nordheim theory as depicted in **Eq. (2.7)** and demonstrates the gate manipulated electron field emission behavior. The I_a kept invariant with V_a, revealing that the electron emission from the cathode is induced by the gate electrode while the anode performs as a current collector. A high anode current of ~ 160 μA was achieved at $V_g = 34$ V with negligible gate intercepted current which was less than 2% of the anode current at high gate voltages. The efficient gate control over emission current with low gate intercepted current can be attributed to the formation of a well-structured self-aligned silicon gate electrode with optimum gate to emitter distance. In addition, this negligible gate intercepted current guarantees better endurance with practical applications of the nanodiamond VFE transistor.

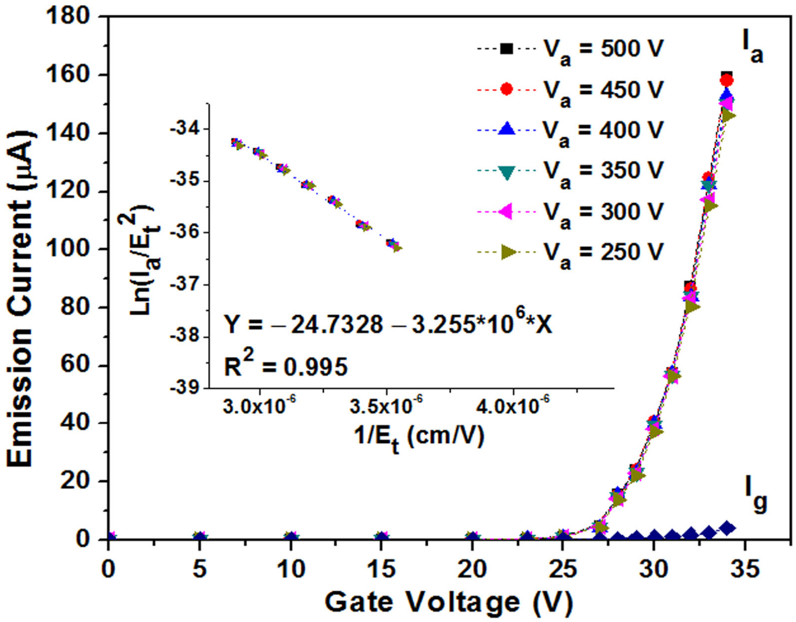


Figure 6.2 Plots of I_a-V_g and I_g-V_g of the nanodiamond VFE transistor with 100 x 200 emitter microtips at various V_a bias voltages. Inset shows the Fowler-Nordheim plots of the corresponding I_a-E_t.

In order to analyze the transistor field emission characteristics based on the Fowler-Nordheim equation, it is important to determine the total electric field applied on the emitters, $E_t = (V_g + V_0 + \gamma V_a) / d_g$, as mentioned earlier in **Section 2.4.2**, and which requires a value for γ. Instead of calculating the value of γ using electrostatic theory by simulating the device structure for simple geometrical design, the γ of the three-electrode

VFE device can be determined from the amplification factor μ of the device, extracted from the measured I-V characteristics. The relationship between γ and μ can be deduced from the F-N equation. Taking the partial derivative of the F-N equation, **Eq. (2.17)**, with respect to V_g, we get

$$\frac{\partial I_a}{\partial V_g} = \left(\frac{\alpha k_1 A \beta^2}{\phi d_g^2}\right)\left[\left(\gamma \frac{\partial V_a}{\partial V_g} + 1\right)\left(2\gamma V_a + 2V_g + \frac{k_2 \phi^{1.5} d_g}{\beta}\right)\right]\exp\left(-k_2 \frac{\phi^{1.5} d_g}{\beta\left(V_g + \gamma V_a\right)}\right). \quad (6.1)$$

Substituting **Eq. (2.19)** into **Eq. (6.1)**, we obtain

$$\frac{\partial I_a}{\partial V_g} = \left(\frac{\alpha k_1 A \beta^2}{\phi d_g^2}\right)\left[\left(-\gamma\mu + 1\right)\left(2\gamma V_a + 2V_g + \frac{k_2 \phi^{1.5} d_g}{\beta}\right)\right]\exp\left(-k_2 \frac{\phi^{1.5} d_g}{\beta\left(V_g + \gamma V_a\right)}\right). \quad (6.2)$$

It should be noted that the two elliptical functions of *v(y)* and $t^2(y)$ defined previously are taken to be unity in the calculations for simplified analysis and the V_0 is taken to be zero since the cathode is grounded. The left hand side of **Eq. (6.2)** is equal to zero because I_a is constant by the definition of μ. Since a non-zero emission current was measured at the anode, this gave α ≠ 0, hence the middle term of the right hand side of **Eq. (6.2)** must be zero to have **Eq. (6.2)** stands. Thus, γ can be either

$$\gamma = \frac{1}{\mu} \quad (6.3)$$

or

$$\gamma = -\left(\frac{V_g}{V_a} + \frac{k_2 \phi^{1.5} d_g}{2\beta V_a}\right). \quad (6.4)$$

However, **Eq. (6.4)** is invalid since a negative resultant electric field is generated by placing **Eq. (6.4)** into **Eq. (2.15)**, namely $E_t = - k_2\Phi^{1.5}/2\beta$, which is contradictory to the fact that a positive electric field is required to induce electron emission from the cathode. Therefore, only **Eq. (6.3)** is valid and the γ of the device can be determined from μ which can be extracted from the I_a-V_a-V_g characteristics according to its definition as depicted by **Eq. (2.19)**. From **Figure 6.2**, it can be clearly observed that a small variation of V_g corresponds to a large change in V_a at a given I_a, suggesting a high amplification factor. The nanodiamond VFE transistor exhibited a high μ of ~ 1400. The γ was then determined based on **Eq. (6.3)** to be ~ 0.0007, and thereby the corresponding resultant electric field was dominated by V_g.

The measured anode currents were further analyzed by extracting the corresponding F-N plots of $Ln(I_a/E_t^2)$ versus $1/E_t$, as shown in the inset of **Figure 6.2**, which exhibited a linear feature with the slope and y-intercept value of – 3.26 x 10^6 V/cm and – 24.73, respectively. This linear feature agrees with the field emission theory and confirms that the observed anode current is due to the electron field emission from the nanodiamond emitters induced by the gate voltages. As discussed in **Section 2.2**, the field enhancement factor β and total emission area A can be deduced from the slope and y-intercept value of the F-N plots. The work function of the nitrogen-incorporated nanodiamond film, synthesized with the same reactant gas mixture ratio, temperature, and microwave power as utilized here was found to be 1.39 eV according to our previous analysis using the thermionic electron emission method [185]. Based on this value, the β and A were calculated to be ~ 35 and ~ 1.34 μm^2. The low β might resulte from the smaller field enhancement attributed by lesser electric field lines imposed by the gate electrode onto the emitter tips. The calculated emission area closely matched with the total area of emitter tips, using a nominal tip curvature of 5 nm, suggests that the electron emission indeed occurred at the tip region and a uniform emission was obtained.

6.2.2 Transistor behavior

The transistor characteristics of the device were clearly demonstrated by the family plots of anode current versus anode voltage at different gate voltages (I_a-V_a-V_g), as shown in **Figure 6.3(a)**. Distinct cutoff, linear, and saturation regions were observed in the measured I_a-V_a-V_g plots of the fabricated device. The I_a increased with V_a for V_a<<V_g and saturated for V_a>>V_g for a given V_g. This feature is consistent with the electron transport mechanism discussed in **Section 2.4.2–(ii)**. As the transistor is turned on (V_g > 25 V), and if V_a is zero, all the electrons emitted from the nanodiamond emitters would be collected by the gate electrode and I_a would be zero. If V_a is increased but still less than V_g, parts of the emitting electrons move to the anode and thus I_a starts to increase linearly and I_g decreases correspondingly. When V_a is further elevated to a higher value than V_g, all of the emitted electrons transit to the anode and thereby I_a tends to saturate at a given V_g and I_g decreases to zero. This electron transport mechanism with regard to V_a at fixed V_g can be observed clearly from the I_a-I_g-V_a characteristics as shown in **Figure 6.3(b)**. The device exhibited a current density of 12.5 mA/cm^2, considering the area of whole array including the spacing between emitter tips. This current density can be enhanced to 200 mA/cm^2 if only the area of 100 x 200 pyramidal emitter array is considered, i.e. for the case of a densely packed emitter array.

The electrical performance of the fabricated VFE transistor was further evaluated to determine their small-signal parameters: amplification factor μ, gate-anode transconductance g_m, and anode resistance r_a as described earlier in **Section 2.4.2**. These three coefficients can be determined from the measured I-V characteristics based on their corresponding definition as expressed in **Eq. (2.19) – (2.21)**, respectively. First, the

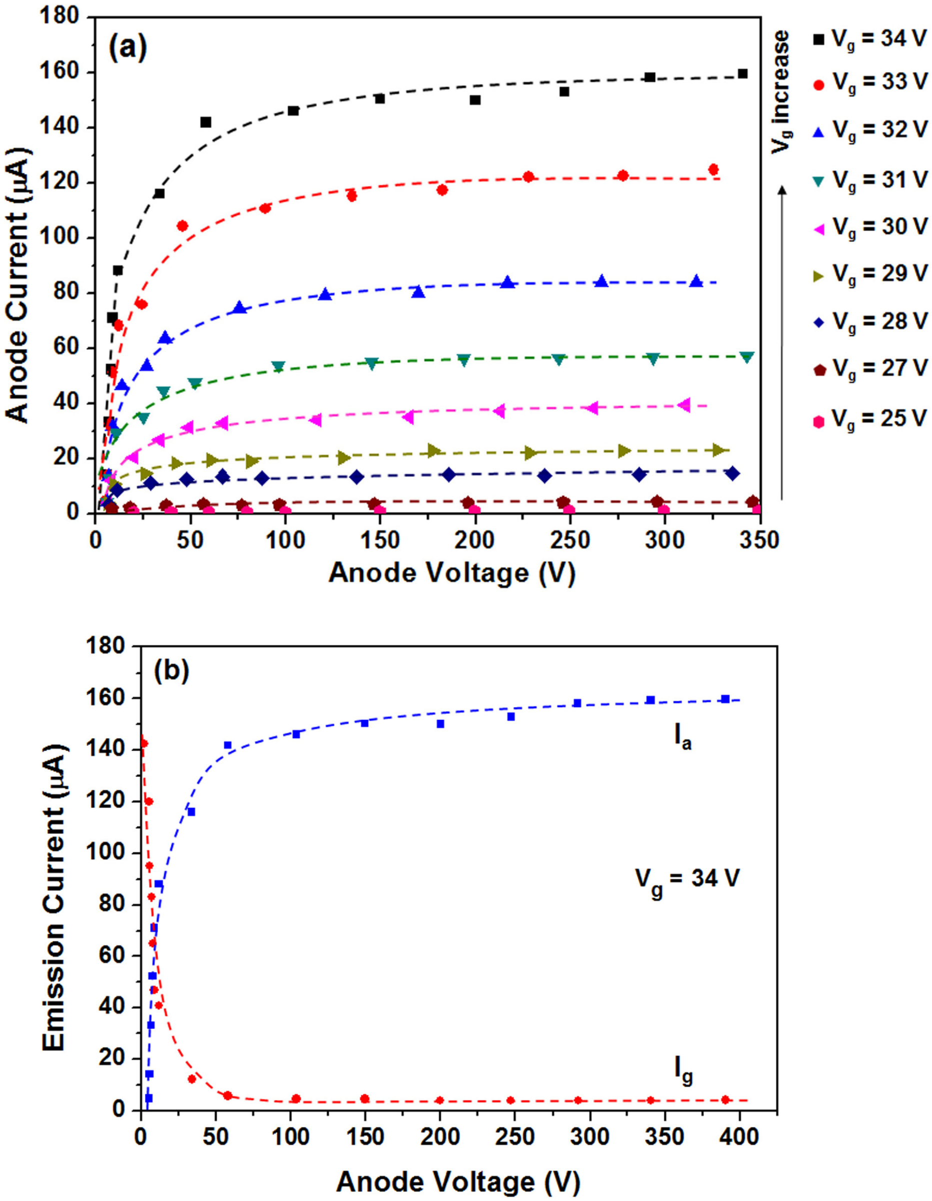


Figure 6.3 (a) Plots of I_a-V_a of the nanodiamond VFE transistor with 100 x 200 emitter microtips for different V_g bias voltages, exhibiting transistor characteristics. (b) Plots of I_a-V_a and I_g-V_a of the device at V_g = 34 V, illustrating the electron transport mechanism with respect to V_a.

amplification factor signifies the ratio of the variation in anode voltage to the change in gate voltage at a constant anode current. The fabricated nanodiamond VFE transistor showed a high μ of ~ 1400 at a constant I_a of 100 μA, suggesting a high *dc* voltage gain for signal amplification applications. Second, the device transconductance g_m which characterizes the driving capability of gate voltage on anode current, defined in **Eq. (2.20)**, can be found by taking the partial derivative of **Eq. (2.17)** with respect to V_g, evaluated at a constant V_a. Hence, g_m can be expressed as an exponential function of V_a and V_g, namely,

$$g_m = \frac{\alpha k_1 A\beta}{\phi d_g}\left[\frac{2\beta}{d_g}\left(V_g + \gamma V_a\right) + k_2\phi^{1.5}\right]\exp\left(-k_2\frac{\phi^{1.5} d_g}{\beta\left(V_g + \gamma V_a\right)}\right) \tag{6.5}$$

This equation indicates that transconductance increases exponentially with total electric field. It also confirms that the emission current is strongly affected by the total electric field applied onto the emitters. The g_m of the fabricated transistor was calculated at a given V_a of 300 V and plotted as a function of V_g, **Figure 6.4**, showing an exponential increase with V_g, as supported by **Eq. (6.5)** that g_m is an exponential function of V_g. This further verifies that the measured emission current obeys the F-N theory and is mainly extracted by the gate voltage. Third, the anode resistance r_a determines the controlling capability of anode voltage over the anode current. For transistor application, the device is usually operated in the saturation region where the anode current is kept nearly invariant with the increase of anode voltage, resulting in a large anode resistance. The r_a of the fabricated transistor was computed to be ~ 40 MΩ at V_g = 32 V in the saturation region.

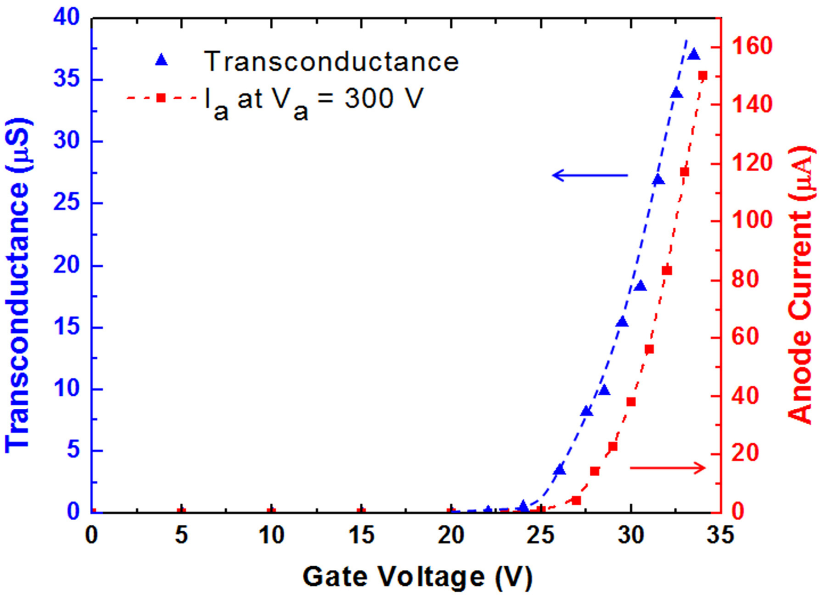


Figure 6.4 Plots of g_m-V_g and I_a-V_g of the fabricated nanodiamond VFE transistor at an applied $V_a = 300$ V.

6.2.3 Small signal amplification application

A small variation of the gate potential can modulate the amount of emitted electrons from the emitter and thus a change in the anode current. This physical mechanism of gate modulation on emission current makes the VFE transistor a suitable active device for signal amplification.

(i) Modeling

A modified small signal circuit model was proposed and used to analyze the amplification behavior of the nanodiamond VFE transistor. The simplified *ac* equivalent circuit of the VFE transistor is shown in **Figure 6.5**, where the circuit nodes labeled as A, E, and G represent the anode, emitter, and gate electrodes, respectively. The g_m and r_a, two small signal parameters commonly used to determine the transistor performance, are employed in the circuit model. Their values vary with the operation conditions and can be

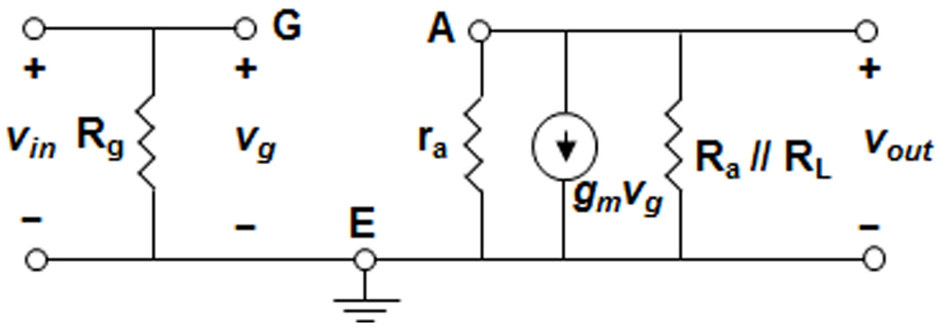


Figure 6.5 Schematic diagram of the simplified small signal equivalent circuit used for the nanodiamond VFE transistor.

determined from *dc* field emission characteristics. We assume the source resistance of the input signal to be relatively small compared to the gate resistor R_g which is selected to be 10 MΩ so that the *ac* voltage at the gate v_g is equal to the *ac* voltage from the function generator v_{in}. The *ac* output voltage v_{out} is the voltage dropped across the equivalent output resistance attributed to the parallel combination of anode resistor R_a, load resistor R_L and r_a in the transistor circuit. Consequently, the output voltage is equal to the multiplication of output current at anode and the equivalent output resistance, that is,

$$v_{out} = -g_m v_g \left(R_a // R_L // r_a \right). \tag{6.6}$$

This gives the theoretical small signal voltage gain A_v of the transistor to be

$$A_v \equiv \frac{v_{out}}{v_{in}} = -g_m \left(R_a // R_L // r_a \right). \tag{6.7}$$

This equation is utilized to estimate and verify the *ac* voltage amplification characteristics of the nanodiamond VFE transistor. When the device is operated at V_a = 300 V and V_g = 32 V, the g_m and r_a are ~ 25 μS and ~ 40 MΩ, respectively. The theoretical A_v of the fabricated nanodiamond VFE transistor is estimated to be ~ 111 (41 dB) according to **Eq. (6.7)** with R_a and R_L both equal to 10 MΩ. A higher *ac* voltage gain is achievable if the device is operated at a higher operation voltage and current, which would give a larger g_m value.

(ii) Experimental performance

The *ac* signal amplification performance of the fabricated nanodiamond VFE transistor with the emitter array size of 100 x 200 was experimentally measured by the characterization technique as described in **Section 5.3.1**, utilizing the test setup as shown in the schematic of **Figure 5.17**. The device was *dc* biased at a predetermined operation point, $V_a = 300$ V and $V_g = 32$ V, in the saturation region. An *ac* input signal v_{in} with an peak-to-peak amplitude of 0.89 V and a frequency of 100 Hz was applied from a function generator to the gate electrode of the transistor. The corresponding *ac* output signal v_{out} was measured across the anode resistor R_a of 10 MΩ and a load resistor R_L of 10 MΩ, which were connected in parallel. The recorded output signal displays a 44.5 V peak-to-peak value and a phase shift of 178.2°. Both input and output small signals were recorded by the digital oscilloscope, as shown in **Figure 6.6**. This nearly 180° phase shift is in good agreement with the theoretical prediction as given by **Eq. (6.7)**.

However, the experimental *ac* voltage gain of the device was found to be ~ 50 (34 dB) which is inconsistent with the theoretically calculated value mentioned earlier. The discrepancy is caused by the three parasitic capacitances residing in the test setup circuitry, namely the parasitic capacitances between gate-to-emitter, gate-to-anode, and emitter-to-anode attributable to the testing facility. These parasitic capacitances were measured to be ~ 150 pF, so they need to be considered in a more accurate small signal equivalent circuit model, as shown in **Figure 6.7(a)**. According to the Miller's Theorem

[186], the gate-to-anode parasitic capacitance C_{ga} can be replaced by two capacitances, i.e., the input capacitance C_1 between gate-to-ground and output capacitance C_2 between anode-to-ground, as shown in **Figure 6.7(b)**. The reactance of these capacitors can be determined from C_{ga} and included in the revised voltage gain equation as

$$A_v = -g_m\left(R_a // R_L // r_a // Rc_{ea} // Rc_2\right), \tag{6.8}$$

where R_{Cea} is the reactance of the emitter-to-anode parasitic capacitance C_{ea} and R_{C2} is the reactance of C_2. The theoretical *ac* voltage gain is then calculated to be ~ 60 (35.6 dB) which is in close agreement with the experimental result. Although the ac performance of the device was restricted by the parasitic capacitances in the test setup, the voltage amplification was realized, measured, and verified by the modified small signal equivalent circuit model, achieving a consistent method for analyzing the performance characteristics of the nanodiamond VFE transistor.

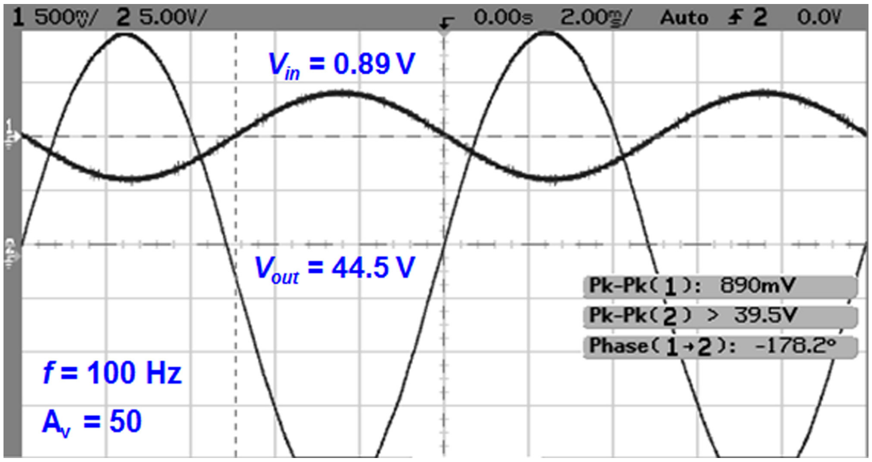


Figure 6.6 Plots of *ac* input and output voltage signals of the nanodiamond VFE transistor at frequency of 100 Hz, showing a voltage gain of 50 with a phase shift of 178.2°.

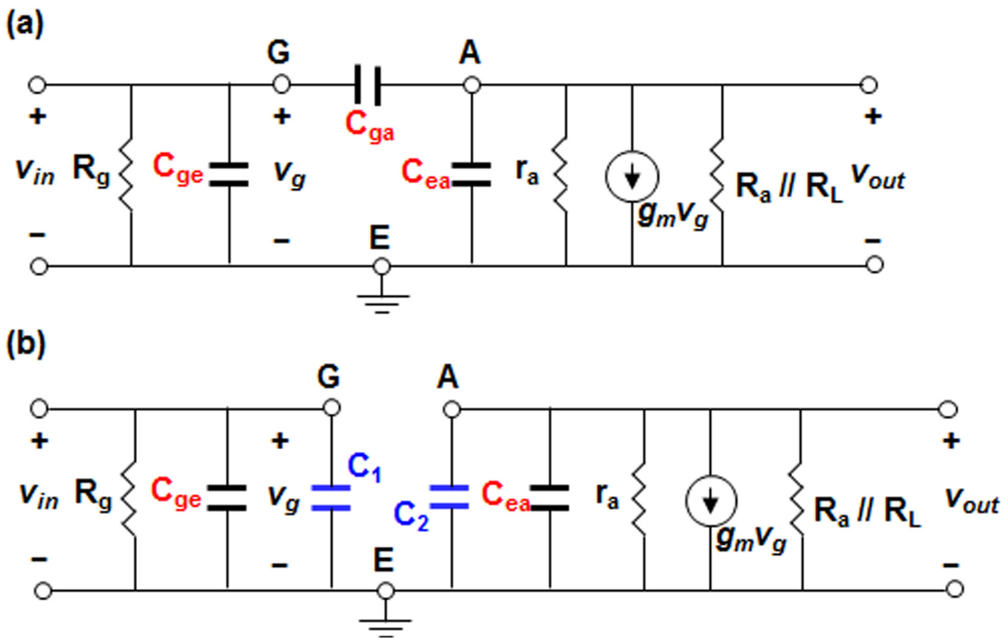


Figure 6.7 Schematic diagrams of the modified small signal equivalent circuit in which (a) the three parasitic capacitances associated with the test setup are included, and (b) the gate-to-anode parasitic capacitance is replaced by two capacitances at the input and output terminals.

6.3 Nanodiamond vacuum field emission triode characterization

The three-terminal nanodiamond vacuum field emission device can be operated in "transistor" and "triode" modes depending on the anode-to-emitter spacing. In the previous section, the electrical characteristics of the nanodiamond VFE transistor with a 600−μm anode-to-emitter spacing were discussed. Different from the transistor operation, the electron emission of a triode is induced by the electric field from the anode (with closer proximity to the emitters) and modulated by the gate voltage. Thus, in this section, the electron field emission behavior of the nanodiamond VFE triodes with varied anode-to-emitter gaps (25 and 4 μm) and a systematic analysis of their corresponding electrical characteristics are reported.

6.3.1 Field emission triode characteristics

The triode characterization technique described in **Section 5.3.1** was utilized to measure the emission current as a function of anode and gate voltages and to generate the I-V curves of the device. The nanodiamond VFE triode with the emitter array size of 80 x 80 and a 25−μm anode-to-emitter spacing was first tested. **Figure 6.8(a)** exhibited its corresponding anode current versus anode voltage plots at various gate bias conditions (I_a-V_a-V_g). As the gate electrode was grounded, the I_a increased exponentially with V_a, indicating the anode-induced field emission behavior of the device. The device possessed an anode turn-on voltage, defined as the anode voltage required to obtain 1 μA of anode current, of ~ 200 V which gives an anode turn-on electric field of ~ 8 V/μm. This turn-on field is slightly higher than that of a similar nanodiamond pyramidal tip array without the silicon gate [93] due to the screening effect of gate structure that partially blocks the emitter from the anode electric field. Similar behavior was also observed in the nanodiamond VFE triode with a 4−μm anode-to-emitter spacing, described later. The gate-controlled current modulation was then clearly observed by applying positive and negative gate voltages. The gate voltage was found to be able to symmetrically enhance and suppress the emission current induced by a given anode voltage, agreeing with the triode operation mechanism that the gate voltage modulates the total electric field on the emitter and thus the electron tunneling probability, as described in **Section 2.4.2–(i)**. The anode current changed by an order of magnitude with a ± 4 V alternation in the gate bias, as shown in **Figure 6.8(a)**, revealing the efficient gate control over emission current which can be attributed to the close proximity of silicon gate to emitters. This device exhibited a relatively low emission current because of the shielding effect of the gate structure which leads to a significant decrease in the geometrical field enhancement factor. Nevertheless, it can be improved by applying higher anode and gate voltages or by reducing the distance between the anode and emitter electrodes.

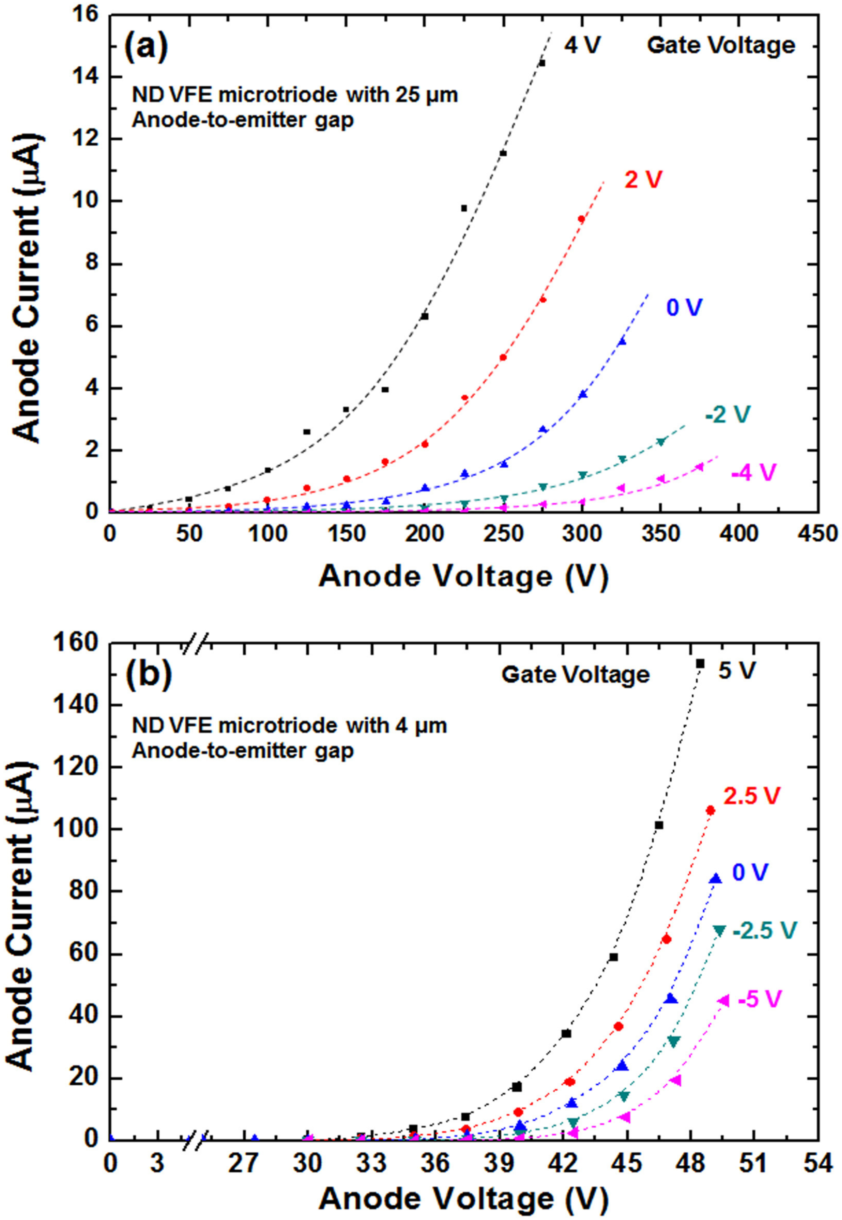


Figure 6.8 Plots of measured I_a-V_a characteristics of the fabricated nanodiamond VFE triodes with (a) 25−µm and (b) 4−µm anode-to-emitter gap at various V_g bias voltages, displaying clear triode behavior with anode-induced field emission and gate-controlled emission current modulation.

The field emission characteristics of the nanodiamond VFE triode with the emitter array size of 80 x 80 and a 4−μm anode-to-emitter spacing were then measured using the same method, and the results are shown in the family plots of I_a-V_a-V_g in **Figure 6.8(b)**. The anode current increased exponentially with the anode voltage and varied symmetrically with the gate biasing voltages, conforming to F-N theory of **Eq. (2.17)**, clearly demonstrating the triode behaviors whereby electron emission from the emitter is induced by the anode voltage and modulated by the gate bias, verifying the triode operation mechanism. The device exhibited a small anode turn-on voltage of ~ 30 V which corresponds to an anode turn-on electric field of ~ 7.5 V/μm. A high emission current of ~ 85 μA was obtained at V_a of 49 V and $V_g = 0$ V. This significantly enhanced emission performance with a smaller anode operating voltage and higher emission current can be attributed to the more effective anode electric field in extracting the electron emission owing to the reduced anode-to-emitter distance, i.e. larger γ. In addition, the device showed efficient gate-controlled current modulation with an order of magnitude variation in emission current by ± 5 V change in the gate bias. This behavior is similar to that of the device with 25−μm anode-to-emitter spacing fabricated on the same chip because the same aperture of gate opening was constructed, verifying the satisfactory formation of a self-aligned silicon gate with small and uniform gate-to-emitter distance. A high emission current of ~ 155 μA was achieved at the bias condition of $V_a = 48.5$ V and $V_g = 5$ V. The corresponding current density was 24.2 mA/cm^2, taking the area of the whole array including the spacing between emitter tips into consideration. The current density can be enhanced to be 605 mA/cm^2 if counting only the area of 80 x 80 pyramidal emitters, i.e. in the case of a densely packed emitter array.

The low applied voltages required to initiate and modulate the electron emission with high emission current are attributed to the geometry of the triode constructed and the excellent material properties of nitrogen-incorporated nanodiamond emitter tips for electron emission.

The field emission tunneling mechanism of measured I-V characteristics was verified based on the modified F-N equation depicted in **Eq. (2.17)**. Similar to the field emission analysis of VFE transistor as described in Section 6.2.1, it is also important to calculate the geometric coefficient γ of the VFE triode in order to determine the total electric field $E_t = (V_g + V_0 + \gamma V_a) / d_g$ applied on the emitters. The γ can be determined from the amplification factor μ according to **Eq. (6.3)**. The μ extraction for both nanodiamond VFE triodes with 25−μm and 4−μm anode-to-emitter spacing will be discussed in detail in next section. Based on the calculated μ, the γ for each bias condition was determined accordingly and employed for the calculation of the corresponding total electric field. **Figure 6.9(a)** and **(b)** present the generated F-N plots of $\mathrm{Ln}(I_a/E_t^2)$ versus $1/E_t$ at various V_g for the emission current measured from the nanodiamond VFE triodes with 25−μm and 4−μm anode-to-emitter spacing, respectively. Linearity features of F-N plots were observed, agreeing with the field emission theory and demonstrating that the measured anode currents are due to a field emission mechanism. For each triode, the linear F-N curves possess a nearly identical slope (-3.8×10^6 and -4×10^6 V/cm for 25–μm and 4–μm microtriodes, respectively) with changed y-intercept values as V_g varied. The invariant F-N slope with the change of V_g indicates that the field enhancement factor β was constant during the gate modulation, which agrees with that β is independent of V_g and is determined by the triode structure and the geometry and *sp*^{2}-graphite content of the

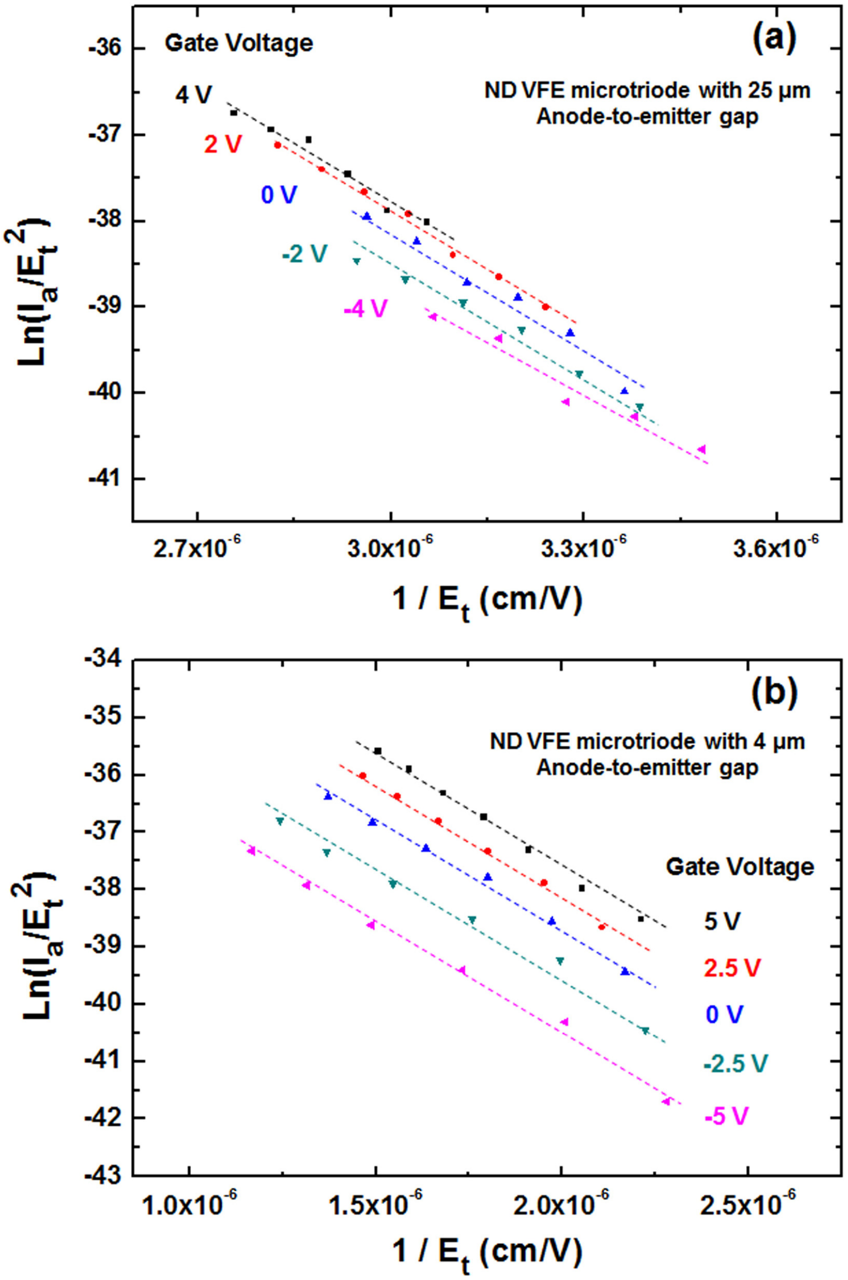


Figure 6.9 The Fowler-Nordheim plots of the nanodiamond VFE triodes with (a) 25−µm and (b) 4−µm anode-to-emitter spacing, $\mathrm{Ln}(I_a/E_t^2)$ versus $1/E_t$ at various V_g bias voltages, showing parallel straight lines with nearly the same slope and increased y-intercept value as V_g increases.

nanodiamond emitters. The changes in the y-intercept value with V_g indicates that the emission area was enlarged or reduced as V_g increased or decreased, respectively, which is consistent with the triode operation mechanism that a higher or lower total composite electric field modulated by the gate voltage can increase or decrease the electron tunneling probability and thereby affecting the total amount of emitting electrons from an effective emitting area. This confirms that the enhancement and suppression of emission current results from the electric field modulation by the gate voltage. Based on the work function of the nitrogen-incorporated nanodiamond film (1.39 eV), the corresponding β was calculated to be ~ 29.5 and 28 for the nanodiamond VFE triodes with 25−μm and 4−μm anode-to-emitter spacing, respectively, from the slope of the F-N plots. These values are similar to that extracted from the nanodiamond VFE transistor discussed in **Section 6.2**. The relatively low β is due to the field screening effect by the gate structure that partially blocks the emitter substrate from the anode electric field. The extracted emission areas were found to be ~ 0.01 μm^2 at $V_g = 4$ V for the triode with 25–μm anode-to-emitter spacing and ~ 0.06 μm^2 at $V_g = 5$ V for the device with 4–μm anode-to-emitter spacing. These results confirmed the field emission mechanism of the measured I-V characteristics and demonstrated the gate-controlled emission current modulation of the fabricated nanodiamond VFE triodes.

6.3.2 Triode parameters extraction

The amplification factor μ, transconductance g_m, and anode resistance r_a of the fabricated triodes were extracted from the measured I-V data per their definitions. First, the μ of the nanodiamond VFE triodes with 25–μm and 4–μm anode-to-emitter spacing was separately determined from their I_a-V_a-V_g characteristics and plotted as a function of V_a and V_g, as shown in **Figure 6.10**. The μ was found to linearly decrease with V_a and linearly increase with V_g for both triodes, demonstrating that the screening coefficient γ depends on the gate and anode voltages. This dependency of μ on V_a can be qualitatively explained by considering the relative values of gate and anode voltages, described as the following. Under a certain V_g bias, as V_a decreases, the anode electric field has less influence on the electron emission due to the gate shielding effect. Thereby a larger V_a variation is required for responding to a given V_g change in overcoming the gate shielding effect in order to maintain a constant emission current, thus resulting in a higher μ. In this case, the γ is smaller owing to the enhanced shielding effect of the higher gate voltage. On the other hand, at a higher V_a bias condition, a smaller change in V_a is sufficient to compensate for the same V_g alteration in keeping emission current unvaried, thereby giving a lower μ. The γ in this case is larger due to the stronger anode field trying to overcome the gate shielding effect. Similar explanation can be made for the dependence of μ and γ on V_g. This experimental observation is consistent with the simulation results reported by Orvis et al. who calculated the μ from F-N equation based on the electrostatic field modeling of a field emission triode using a two-dimensional static field code and metallic boundaries [32]. In addition, the μ was observed to decrease by nearly an order of magnitude with the reduction of the anode-to-emitter distance from 25-μm to 4-μm, as similar anode and gate electric fields were applied. This is attributed to the relatively stronger influence of the anode electric field on the emission as the anode approaches the emitter, resulting in the increase of γ and decrease of μ. This result is also consistent with the very high μ of ~ 1400 obtained from the nanodiamond VFE transistor which possesses an anode-to-emitter distance of 600 μm. This variable *dc* gain can be obtained by simply engineering the triode structure, providing a simple method for designing functional devices with a diversity of functionality in electronic circuits.

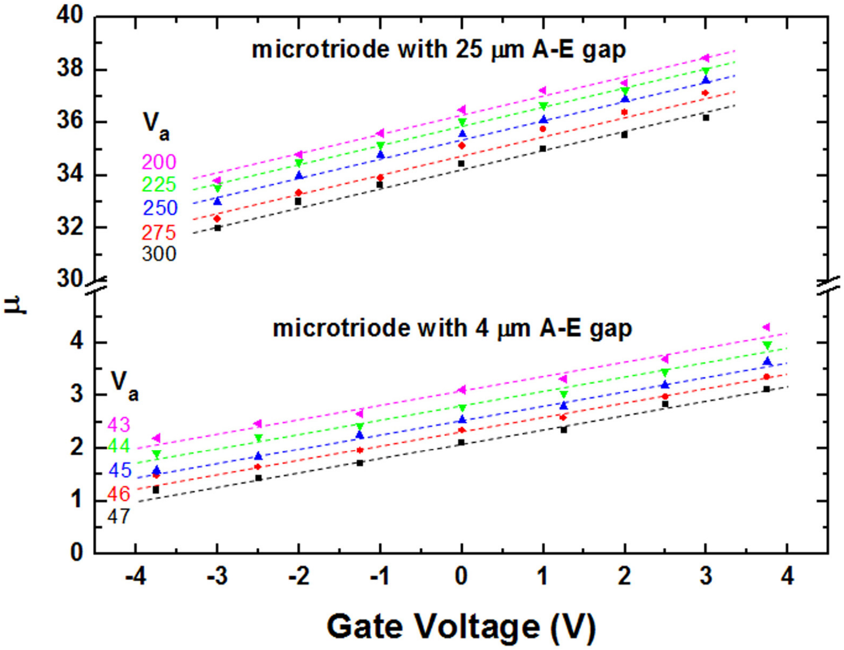


Figure 6.10 The amplification factor (*dc* voltage gain) of the fabricated nanodiamond VFE triodes with 25−μm and 4−μm anode-to-emitter gap plotted as a function of V_a and V_g, showing linear dependence of μ upon both V_a and V_g.

Second, the g_m for both nanodiamond VFE triodes with 25–μm and 4–μm anode-to-emitter spacing was also computed from the I_a-V_a-V_g characteristics to generate the g_m-V_a plots at various V_g biases, as shown in **Figure 6.11(a)** and **(b)**, respectively. The g_m obviously increased exponentially with anode voltage V_a at a fixed gate voltage V_g, in accordance with **Eq. (6.5)** and further verifying that the measured emission current obeys the F-N theory. Moreover, a high g_m of ~ 5.9 μS was obtained from the device with 25−μm anode-to-emitter spacing at the bias condition of V_a = 300 V and V_g = 3 V. It was further enhanced to ~ 22 μS at similar applied anode and gate electric fields as the anode-to-emitter vacuum gap was reduced to 4 μm. This can be attributed to the higher emission current obtained from the device with 4−μm anode-to-emitter gap due to the stronger influence of the anode electric field on emission. This value can be further improved by applying higher electric fields and/or employing a larger nanodiamond pyramidal tip array as the emitter.

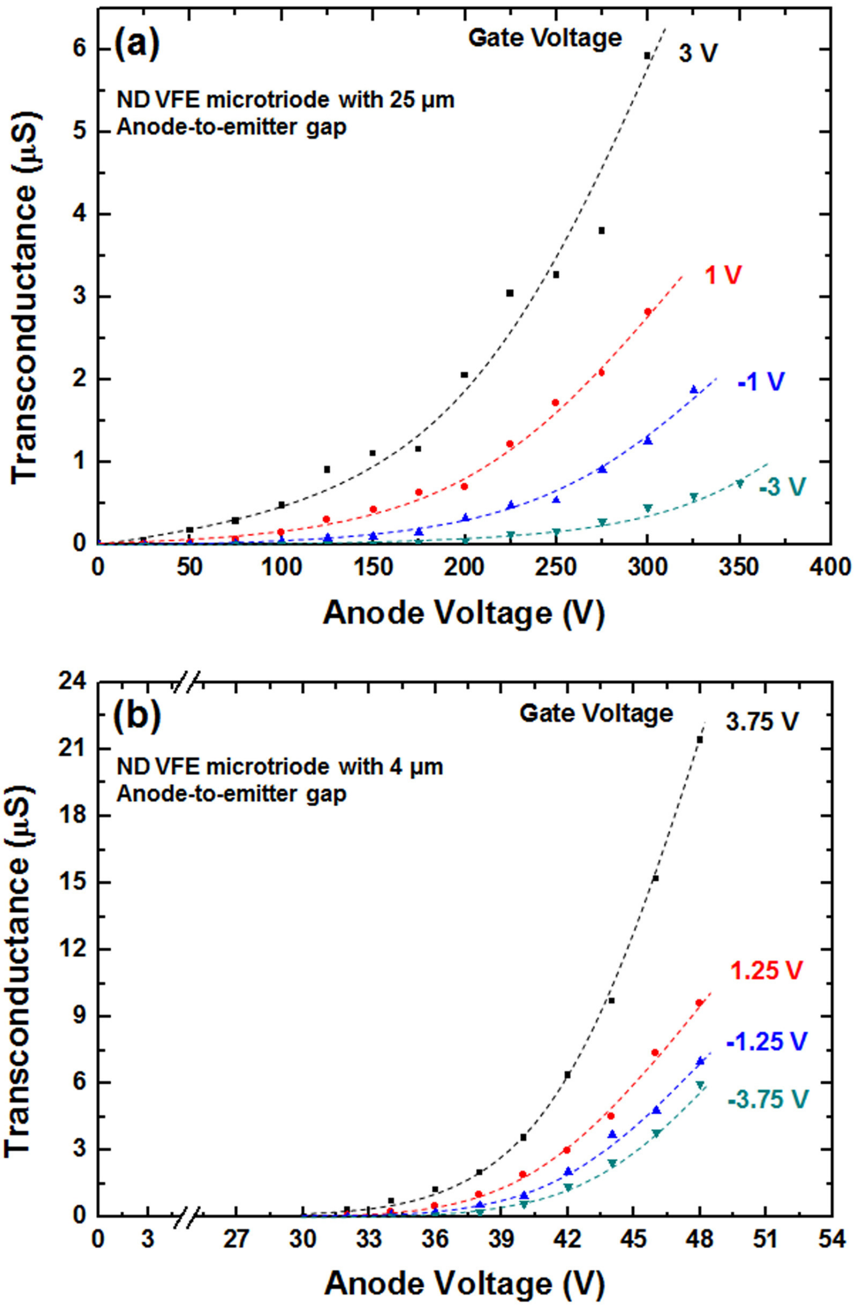


Figure 6.11 The transconductance plotted as a function of V_a at various V_g for the nanodiamond VFE triodes with (a) 25−μm and (b) 4−μm anode-to-emitter spacing, respectively. Exponentially increasing trend was observed, agreeing with the derivation of F-N equation.

Third, the r_a for both microtriodes was calculated from the measured I_a-V_a-V_g data and plotted as a function of V_a at various V_g biases. Based on the partial derivation of the F-N equation, **Eq. (2.17)**, with respect to V_a evaluated at a constant V_g, r_a is found to be the reciprocal of an exponential function of V_a and V_g, as expressed by

$$r_a = \frac{\phi d_g}{\alpha k_1 A \beta \gamma}\left[\frac{2\beta}{d_g}\left(V_g + \gamma V_a\right) + k_2 \phi^{1.5}\right]^{-1} \exp\left(\frac{k_2 \phi^{1.5} d_g}{\beta\left(V_g + \gamma V_a\right)}\right). \tag{6.9}$$

This equation indicates that the anode resistance would decrease exponentially as the total electric field increases. And both fabricated triodes indeed experimentally exhibited the feature of exponential decrease of r_a with the increase of V_a and V_g, as shown in **Figure 6.12**, conforming to the governing formula of **Eq. (6.9)** and confirming again the field emission mechanism. The r_a dropped by nearly 3 orders of magnitude as the anode-to-emitter distance reduced from 25 μm to 4 μm at the anode electric field of 12 V/μm and $V_g = 0$ V. This reduction of r_a is because the closer anode electrode is able to control the electron emission more efficiently, thereby giving a smaller r_a. Overall, the three small-signal coefficients of the triode were quantitatively extracted from the experimentally measured I-V characteristics and qualitatively analyzed to explore their dependency on the applied voltages and the anode-to-emitter distance, providing a good understanding of the VFE triode operation mechanism and a useful tool for designing functional devices with desired properties for application in vacuum integrated microelectronic devices and circuits.

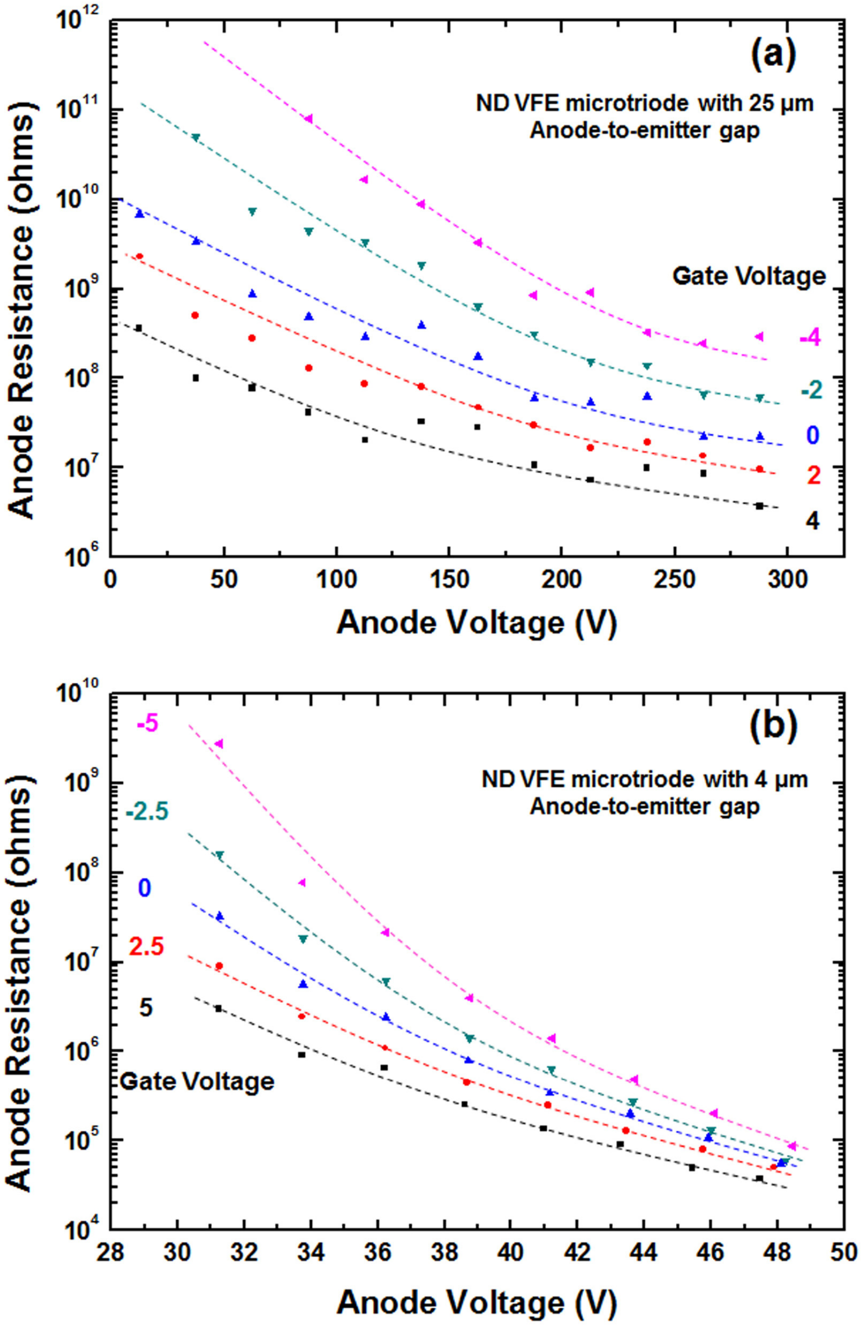


Figure 6.12 Plots of the anode resistance versus V_a at various V_g for the nanodiamond VFE triodes with (a) 25−µm and (b) 4−µm anode-to-emitter spacing, respectively. Both plots exhibited exponential decreasing of r_a with the increase of V_a and V_g, agreeing with the derivation of F-N equation.

6.3.3 Small signal amplification application

The nanodiamond VFE three-terminal devices, such as a transistor and a triode, are functional electronic devices suitable for signal amplification applications by reason of the physical mechanism that a small voltage variation on the gate modulates the electron emission and thus the anode current. The VFE transistors and triodes with different amplification factor values have distinct functions in electronic circuits. The high μ transistors, which usually possess larger output resistance, provide high voltage gain for signal amplification. Whereas, the low/medium μ triodes, which generally have modest voltage gain, offer low output impedance in the output stage to avoid signal distortion when connecting to the load, thereby isolating the input signal from the output signal without the need of feedback loops. The electronic circuits with desired voltage/power gain and minimal noise are programmable by using the former for signal amplification along with the latter as buffer amplifiers. The nanodiamond VFE transistor which possesses a larger anode-to-emitter spacing and a high μ of ~ 1400 has been tested to exhibit a good *ac* voltage gain of 34 dB as mentioned in **Section 6.2.3**. Here, the *ac* response of the nanodiamond VFE triodes with low/medium μ was presented.

The *ac* signal amplification characteristics of the VFE triodes were analyzed with a small signal equivalent circuit model, as shown schematically in **Figure 6.13(a)**. The input signal v_{in} fed to the gate electrode is amplified to be μv_{in} at the anode, and the corresponding output voltage $v_{out} = -\mu v_{in}(R_a//R_L)/[r_a+(R_a//R_L)]$ is collected across the load. The A_v is therefore equal to

$$A_v = -\frac{\mu(R_a // R_L)}{r_a + (R_a // R_L)}. \tag{6.10}$$

And by considering the parasitic capacitances residing in the test setup circuitry as discussed in **Section 6.2.3**, the A$_v$ can be modified to be

$$A_v = -\frac{\mu\left(R_a // R_L // R_{Cea} // R_{C2}\right)}{r_a + \left(R_a // R_L // R_{Cea} // R_{C2}\right)}, \tag{6.11}$$

as shown in **Figure 6.13(b)**. This equation is utilized to estimate and verify the *ac* voltage amplification performance of the fabricated nanodiamond VFE triodes.

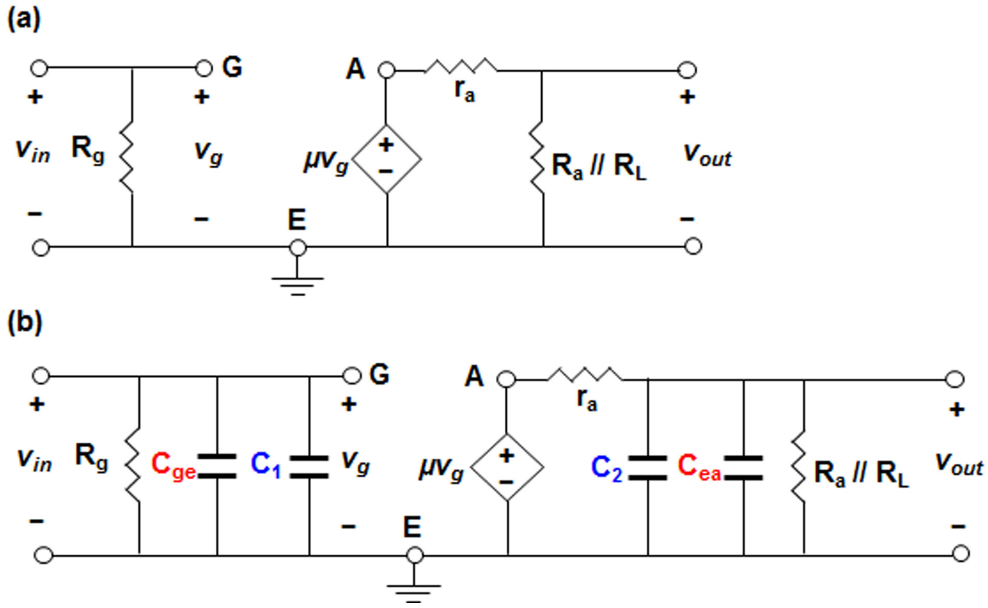


Figure 6.13 Schematic diagrams of (a) the simplified small signal equivalent circuit used for the nanodiamond VFE triode, and (b) the modified equivalent circuit in which the parasitic capacitances associated with the test setup are included.

The fabricated devices were then experimentally examined for their *ac* response by the characterization technique as described in **Section 5.3.1**, utilizing the test setup as shown in the schematic of **Figure 5.17**. The triode with 25−μm anode-to-emitter spacing was first *dc* biased at V$_a$ = 275 V and V$_g$ = 4 V with anode and load resistors of 2 MΩ connected in parallel. The *ac* sinusoidal input signal with a peak-to-peak amplitude of 2.13 V at 100 Hz applied to the gate electrode of the device was amplified to 8.1 V with a phase shift of 166.7°, as shown in **Figure 6.14(a)**, giving a modest A_v of ~ 3.8 (11.6 dB). This experimental *ac* voltage gain agrees with the theoretical value which is ~ 3.7 calculated according to the modified small signal equivalent circuit model depicted in **Eq. (6.11)**, using the corresponding triode coefficients μ of ~ 38 and r_a of ~ 8 MΩ. Furthermore, a higher A_v of ~ 16.4 dB was obtained at elevated V_g = 8 V with an increased I_a of 50 μA, as shown in **Figure 6.14(b)**, demonstrating that enhanced voltage gain is achievable at higher operating voltage and current. The *ac* response of the triode with 4−μm anode-to-emitter spacing was also evaluated by the same method at a *dc* bias condition of V_a = 48 V and V_g = 5 V. The μ and r_a under this bias condition were found to be ~ 3 and ~ 50 kΩ, respectively. It exhibited a nearly unity gain of ~ 1.84, when an input signal with a peak-to-peak amplitude of 3.13 V was superimposed on V_g and its corresponding output signal with 5.75 V amplitude and 166.8° out of phase was recorded across $R_a//R_L$ = 100 kΩ, as shown in **Figure 6.15**. This experimental A_v of 1.84 is also consistent with the theoretic value of ~ 1.99 calculated based on **Eq. (6.11)**, confirming the validation of the proposed small signal equivalent circuit model. Since the I_g was negligible, both devices have high input resistance.

These results suggested that the device can be used as buffer amplifier, and the voltage gain and output resistance of the nanodiamond VFE triodes are programmable by designing and engineering the device's geometric structures, thereby providing a diversity of functional devices for electrical circuit building blocks. The integration of high μ transistors and low/medium μ triodes can establish the vacuum microelectronic circuits possessing useful signal amplification performance and better signal delivery with low distortion. This would be a potentially suitable device for high fidelity applications with the requirements of minimal noise and accurate frequency response for temperature- and radiation-hardness space electronics.

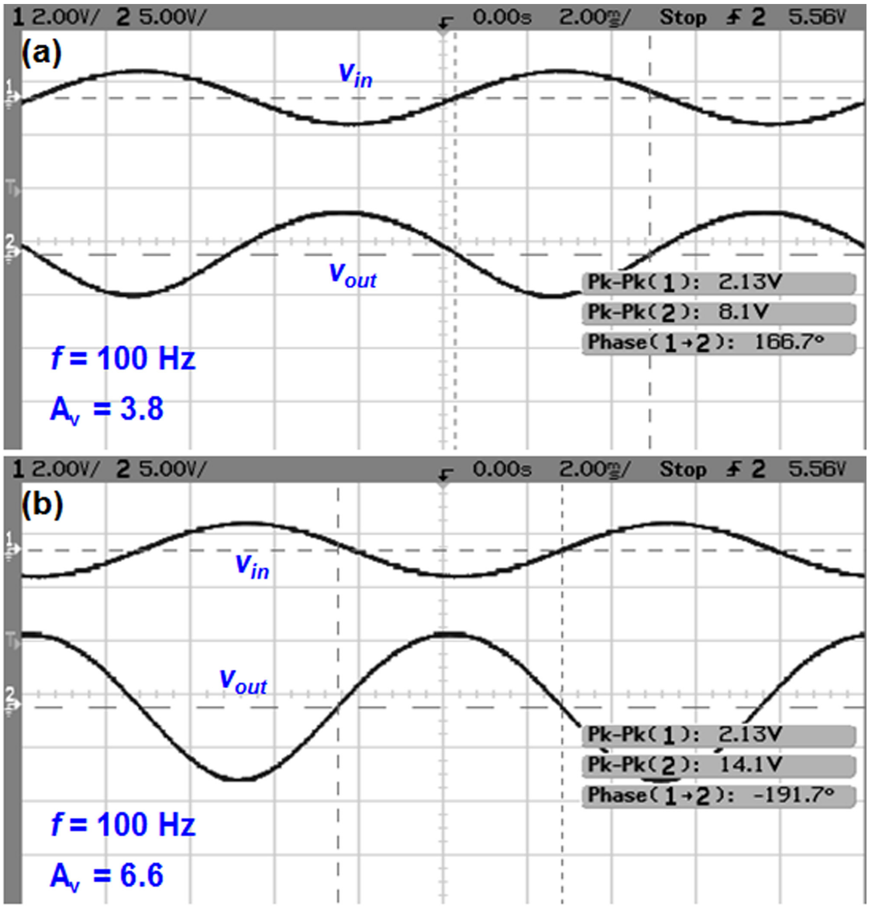


Figure 6.14 The *ac* small signal amplification performance of the nanodiamond VFE triode with 25−μm anode-to-emitter spacing, *dc* biased at (a) V_a = 275 V and V_g = 4 V; and (b) V_a = 275 V and V_g = 8 V, respectively.

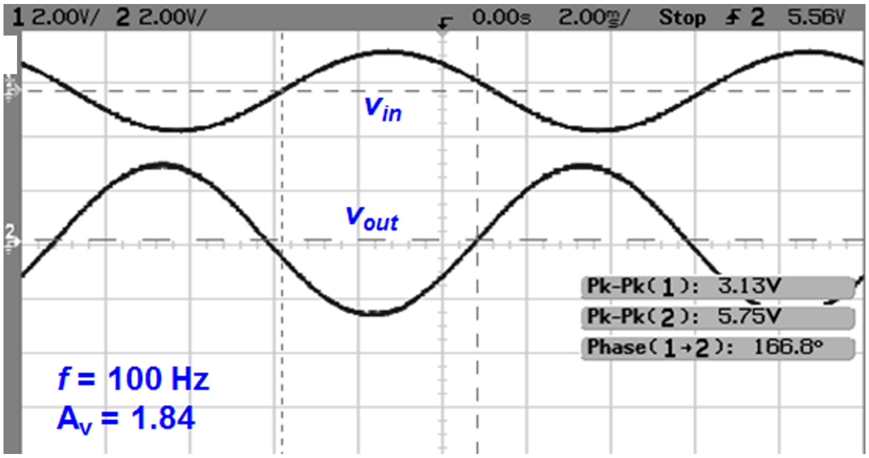


Figure 6.15 Plots of *ac* input and output voltage signals of the nanodiamond VFE triode with 4−μm anode-to-emitter spacing, *dc* biased at V_a = 48 V and V_g = 5 V, displaying a nearly unity gain.

6.4 Nanodiamond vacuum field emission integrated differential amplifier

The fabricated nanodiamond VFE transistors have been demonstrated to exhibit low turn-on voltage, stable emission current, and high voltage gain, allowing further implementation of the transistors into vacuum ICs. In order to demonstrate the vacuum IC capability, we have considered their deployment and implementation into a differential amplifier in this study. The vacuum-based diff-amp chip which consists of eight VFE transistors, each has 80 x 80 nanodiamond emitter microtip array with individually separated gate and anode contacts, has been fabricated as described in Chapter V. For each transistor, positive gate voltage was applied at a given anode voltage such that electrons induced from emitters by V_g were gathered by anode electrode. The anode and gate currents were measured as a function of V_g to characterize each transistor pair in the saturation mode. Two nanodiamond VFE transistors with identical field emission device features were then utilized for diff-amp *ac* testing.

6.4.1 Field emission characteristics of VFE transistor pair

A family plot of I_a-V_a-V_g transistor characteristics of one of the devices is shown in **Figure 6.16**, where distinct cutoff, linear, and saturation regions are observed. The I_a increased with V_a when $V_a << V_g$ and saturated when $V_a >> V_g$ for a fixed gate bias. This feature is consistent with the electron transport mechanism discussed previously. In order to perform as a signal amplifier, the transistor is operated in the saturation region by applying a constant V_a of 350 V. **Figure 6.17** displays the I_a-V_g curves of the selected nanodiamond VFE transistor pair, operated in the saturation region, along with their corresponding gate currents. The exponential increase features of I_a with V_g are indicative of gate-induced field emission, obeying the F-N theory. In addition, the linearly negative slope of $\ln(I_a/E_t^2)$ versus $1/E_t$ plots extracted from the recorded I_a-V_g data, as shown in the inset, is consistent with the F-N formula, further confirming that the measured anode currents are due to the field-induced emission behavior. These two nanodiamond VFE transistor possessed well-matched emission anode currents up to ~ 28 μA at $V_g = 42$ V with a mismatch of 1.2% and fairly low gate turn-on voltages of ~ 29 V. Such nearly identical characteristics of the transistor pair would provide useful common-mode-rejection performance in the diff-amp. The VFE transistors also exhibited negligible gate intercepted currents, ~ 3.5% of I_a, suggesting the long-term operation capability and stability of the diff-amp.

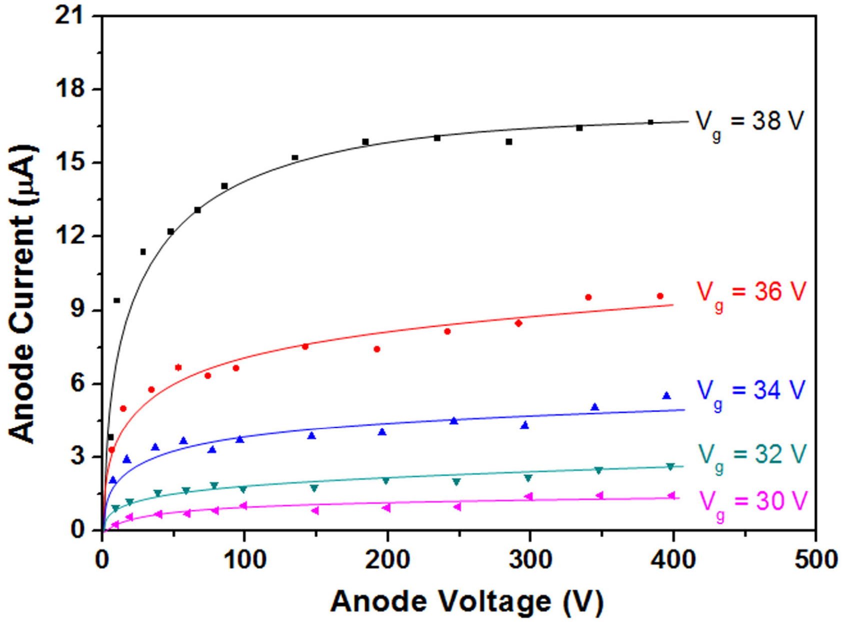


Figure 6.16 Plots of the anode current versus anode voltage of one of the fabricated nanodiamond VFE transistor at various gate voltages, showing clear transistor characteristics with distinct cutoff, linear, and saturation regions.

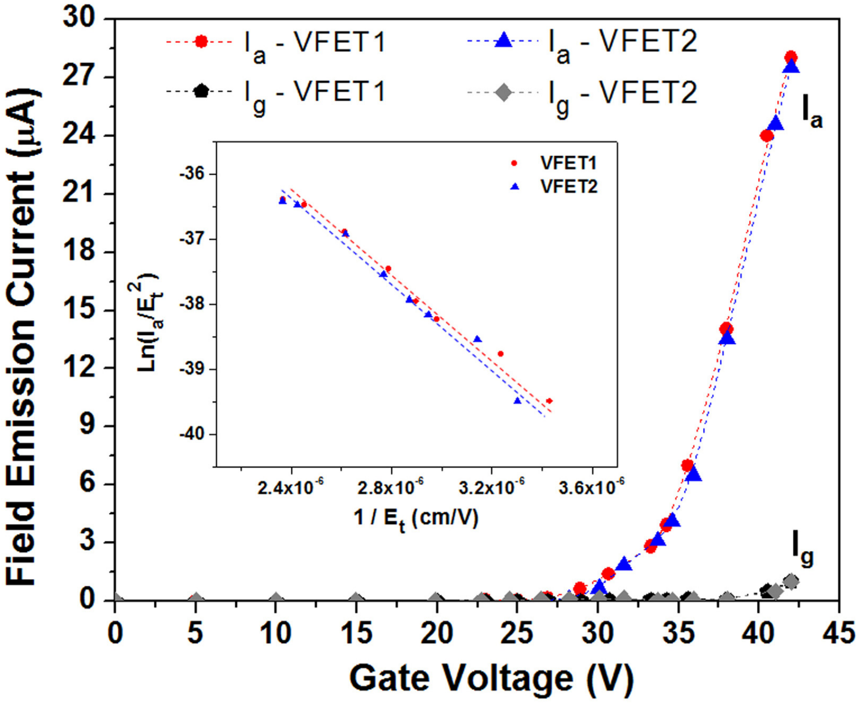


Figure 6.17 *DC* field emission characteristics of a nanodiamond VFE transistor pair utilized for diff-amp biased at fixed V_a of 350 V, exhibiting well-matched anode currents as a function of gate voltage with negligible gate currents. Inset shows F-N plots of the corresponding I_a-V_g data.

6.4.2 Small signal amplification performance of VFE diff-amp

(i) Modeling

According to its definition, the common-mode voltage gain A_{cm} is equal to v_{oc}/v_{ic}. Using the equivalent circuit analysis of the diff-amp [186], the v_{oc} is equal to voltage difference recorded across the anode and load resistances (R_a and R_L), while the v_{ic} is the voltage applied to gate terminals. Consequently, the A_{cm} can be expressed as

$$A_{cm} \equiv \frac{v_{oc}}{v_{ic}} = \frac{\left(I_{a1} - I_{a2}\right) \times \left(R_a // R_L\right)}{V_{ic}} = \frac{\Delta I_a}{V_{ic}} \times \left(R_a // R_L\right) \tag{6.12}$$

where ΔI_a is the mismatch value of anode emission currents. On the other hand, the half-circuit differential-mode voltage gain A_{dm} is equal to v_{od}/v_{id}. The half-circuit v_{od} is the output voltage recorded from a single-ended transistor, that is the voltage across the $R_a//R_L$; while the v_{id} is the input voltage of the single-ended transistor. Therefore, the A_{dm} can be described as

$$A_{dm} \equiv \frac{v_{od}}{v_{id}} = \frac{v_{out1}}{v_{in1}} = \frac{I_{a1} \times \left(R_a // R_L\right)}{V_{in1}} = g_{m1} \times \left(R_a // R_L\right). \tag{6.13}$$

where g_{m1} is the transconductance of the single-ended transistor #1. In this analysis, the internal parasitic capacitances were ignored since we examine low-frequency response to demonstrate the operation of nanodiamond VFE diff-amp, and the coupling capacitors were chosen to be at the microfarad level such that the reactance was negligible. Consequently, the value of CMRR was determined by

$$CMRR = \left| {}^{A_{dm}}\!\!\diagup\!{}_{A_{cm}} \right| = \frac{V_{ic} g_{m1}}{\Delta I_a}. \tag{6.14}$$

The CMRR of a diff-amp can be enhanced by increasing the transistor transconductance and reducing the anode emission current mismatch. The CMRR is independent of load and output resistances.

(ii) Experimental performance

The *ac* response of the fabricated nanodiamond VFE diff-amp was evaluated using the characterization technique described in **Section 5.3.2**. After acquiring *dc* characteristics, the *ac* signal amplification performance of the diff-amp was measured at a predetermined operation point of V_a = 350 V with V_g varied from 33 to 42 V. An *ac* sinusoidal input signal with a peak-to-peak amplitude of 1 V at 100 Hz was superimposed on V_g = 42 V at the gate terminals, and the amplified output signals were recorded across the load resistors $R_a//R_L$ (10 MΩ each) at the anode electrodes by a digital oscilloscope. In the common-mode test, the same small signals as shown in **Figure 6.18(a)** were applied to both of the inputs. The signals were amplified to be 15.0 and 15.2 V at outputs #1 and #2 by transistors #1 and #2, respectively, as shown in **Figure 6.18(b)**. This resulted in a small peak-to-peak common-mode output voltage v_{oc} of ~ 1.1 V and the common-mode voltage gain A_{cm} was calculated to be ~ 0.0256.

As for the differential-mode test, the small signal was first fed to the first input of the diff-amp, while no signal was applied to the other input, i.e., $v_{in1} = 0.5 \sin(2\pi ft)$ V and $v_{in2} = 0 \sin(2\pi ft)$ V. **Figure 6.19(a)** shows the corresponding output waveforms recorded at outputs #1 and #2 along with a differential output voltage v_{od1} of ~ 13.8 V, giving a proper voltage gain at the operating current of 28 μA. Similarly, by alternating the input sequence, the output waveform of transistor #2 v_{out2} and the corresponding differential output signal v_{od2} with a ~ 13.8 V peak-to-peak value and an 180˚ phase shift are shown in **Figure 6.19(b)**, as the input signal amplified only by the second transistor. The differential-mode voltage gain A_{dm} was computed to be ~ 13.8 which is equivalent to the voltage gain of a single-ended transistor amplifier.

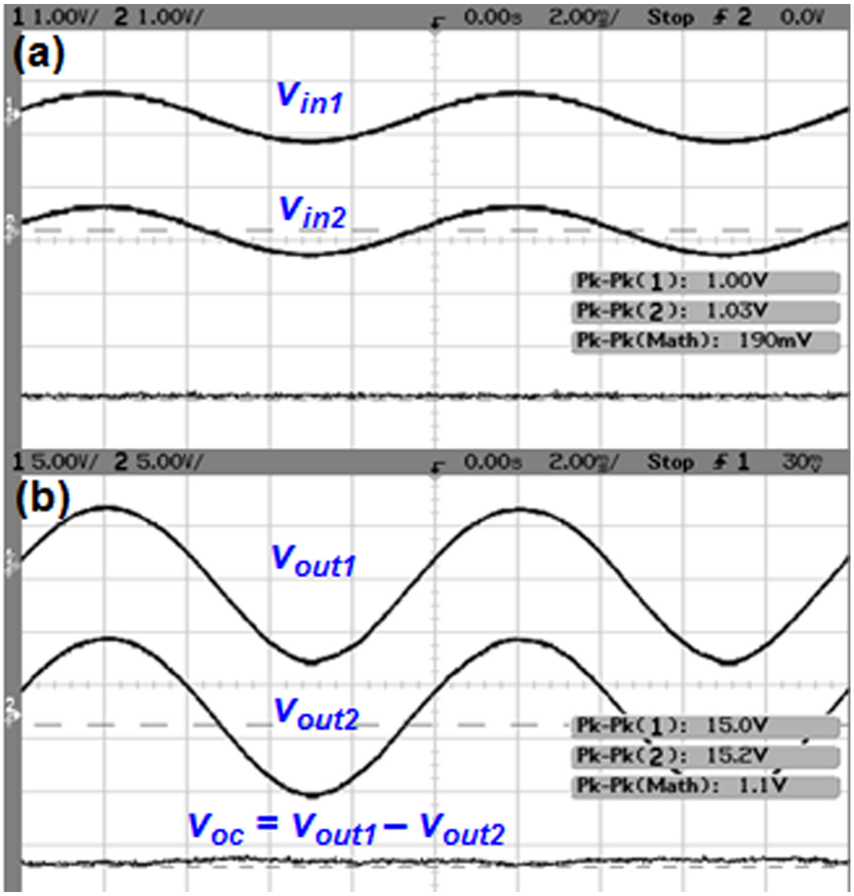


Figure 6.18 *AC* characteristics of the single-chip nanodiamond VFE diff-amp: (a) input signals applied to both gate terminals in common mode; and (b) common-mode output signals recorded at both anode electrodes, along with the corresponding v_{oc}.

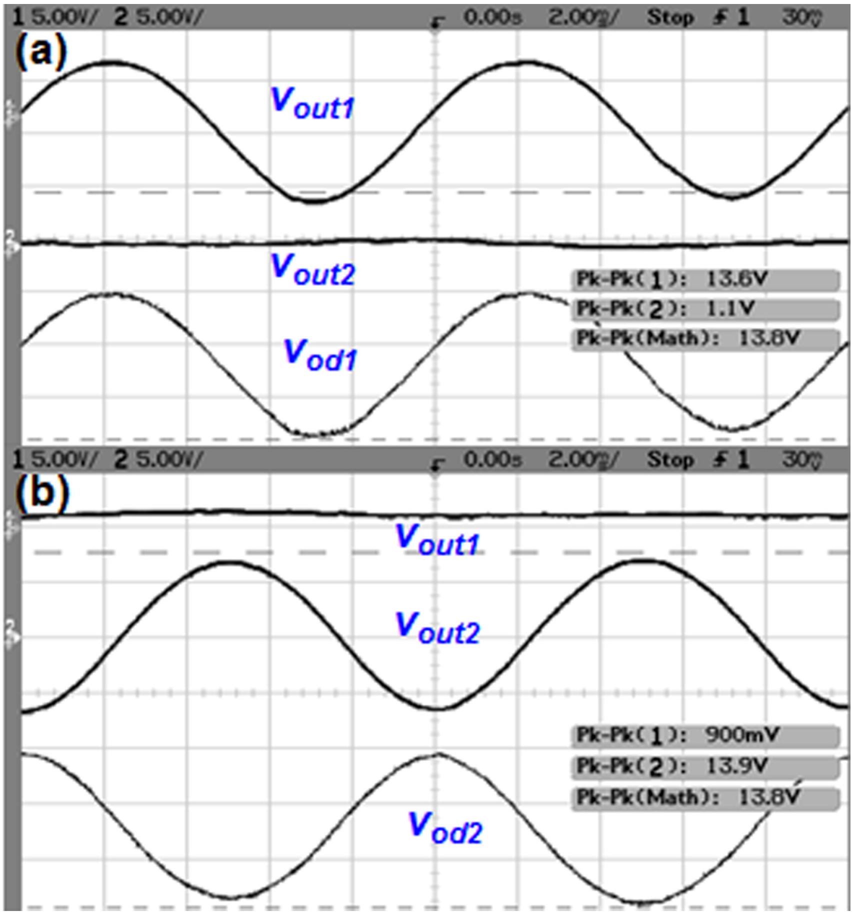


Figure 6.19 *AC* characteristics of the single-chip nanodiamond VFE diff-amp: (a) first differential-mode output waveforms recorded at both anode electrodes along with the corresponding v_{od1}; and (b) second differential-mode output waveforms and the corresponding v_{od2} with 180° phase shift.

Then, the common-mode-rejection ratio of the nanodiamond VFE diff-amp was determined to be ~ 540 (54.6 dB), demonstrating the feasibility for vacuum IC implementation. Relatively less noise was observed on v_{od1} and v_{od2} waveforms compared to v_{oc}, implying that the noise common to both input terminals was offset in the differential-mode outputs, a basic and required feature of a diff-amp. Note that a doubled CMRR of ~ 1080 (60.7 dB) can be obtained under the condition of fully differential signals applied to the input terminals. This value is comparable to that of the commercially available solid-state diff-amps [187] which are well known to have limited operating temperature range. Therefore, the fabricated nanodiamond VFE diff-amp can be an alternative IC building block providing good common-mode-rejection performance with capability for harsh environment operation.

Eq. (6.12) and **(6.13)** were utilized to estimate the common-mode and differential-mode voltage gains of the diff-amp. In this experiment, the diff-amp was operated at V_g = 42 V with an *ac* input voltage amplitude of 0.5 V for R_a and R_L of 10 MΩ each. The A_{cm} and A_{dm} were calculated to be 0.039 and 20, respectively, giving an estimated CMRR of 513 (54.2 dB) which is consistent with the experimentally measured result. The slight overestimations of both A_{cm} and A_{dm} in the analysis model were observed, which are probably due to the neglect of the noninfinite output resistance looking into the anode. Nevertheless, the estimation of CMRR is reliable since the CMRR is independent of load and output resistances, providing a simple method to evaluate the common-mode-rejection performance of the VFE diff-amp.

The *ac* measurement procedures were then repeated on the nanodiamond VFE diff-amp for variant operation points, and the corresponding CMRR was plotted as a function of V_g, as shown in **Figure 6.20**. The enhancement of CMRR with V_g from ~ 37.9 dB at 33.5 V to ~ 54.6 dB at 42 V was observed, which is attributed to the increase of the g_m and transistor voltage gain, agreeing with the prediction of equivalent circuit analysis where CMRR is proportional to g_m as depicted in **Eq. (6.14)**. The CMRR in decibels increased linearly with the gate voltage because g_m is an exponential function of V_g as indicated in **Eq. (6.5)**. The further improvement of common-mode rejection is potentially achievable by the improvement of the transconductance of the transistor pair and/or by minimizing the anode current mismatch. The high-frequency response of the nanodiamond VFE diff-amp will be explored in the future with optimized device structure and better test setup.

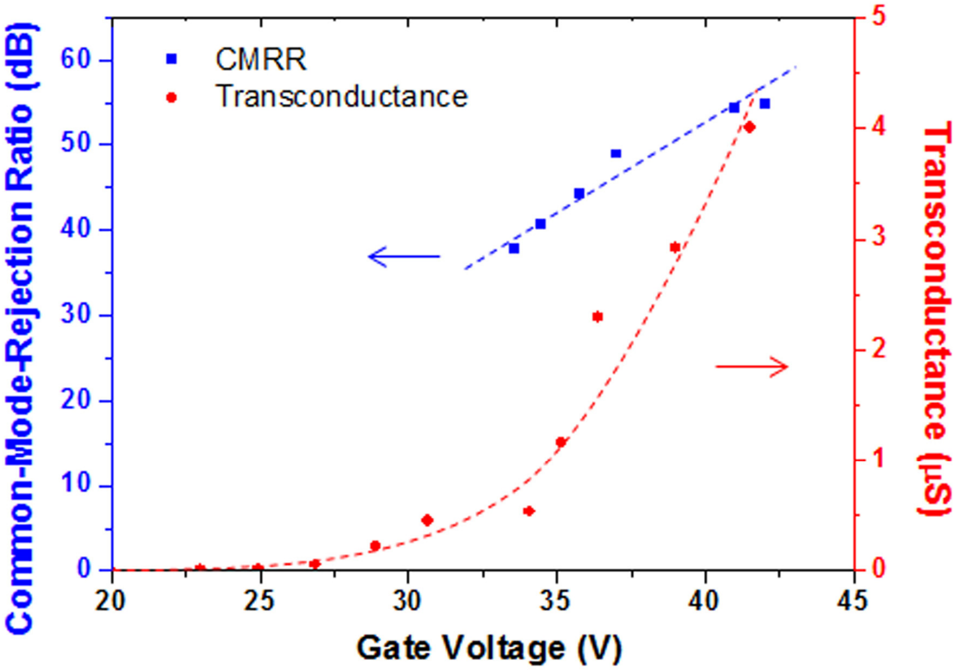


Figure 6.20 Plots of the transconductance and measured CMRR versus the gate voltage of the fabricated nanodiamond VFE diff-amp at a given anode voltage of 350 V.

CHAPTER VII

CONCLUSIONS and RECOMMENDATIONS

In this dissertation, the nanodiamond vacuum field emission microelectronic devices including transistors, triodes, and integrated differential amplifiers have been developed and systematically studied. The important findings from the research are summarized in this chapter, followed by recommendations for future studies on the VFE device technology.

7.1 Conclusions

7.1.1 Three-terminal nanodiamond VFE device fabrication

A consistent and IC-compatible dual-mask microfabrication process, involving the mold-transfer self-aligned gate-emitter technique coupled with conformal CVD nanodiamond deposition into the micropatterned pyramidal molds, has been developed to form the vertically configured three-terminal nanodiamond VFE devices. An advanced nanodiamond deposition method was developed to fill the inverted pyramidal molds with nanodiamond by $CH_4/H_2/N_2$ MPECVD, producing the nitrogen-incorporated nanodiamond microtips with ultrasharp apexes. The well-structured nanodiamond emitter microtip arrays were batch-fabricated and self-aligned with the silicon gate by employing the mold-transfer technique on a SOI wafer. An optimized silicon gate positioned at close proximity to the emitter tip with uniform gate opening was achieved by well-controlled silicon thin down process, allowing efficient gate modulation of the emission current with minimum gate intercept current. The silicon gate partitioning was realized with a second mask and silicon RIE process, forming individual array of nanodiamond VFE devices isolated by the dielectric SiO_2 layer with separate gate electrodes and contact pads on a single chip, enabling further implementation of the integrated devices into vacuum-based integrated circuits. The gate-to-emitter spacing of 1 μm was realized and it can be further reduced simply by decreasing the thickness of thermal SiO_2 between them, allowing further lowering of the gate operating voltage. In addition, an anode-to-emitter distance down to 4 μm has been achieved by utilizing a thinner dielectric spacer, providing the capability of low anode voltage operation for triode devices.

7.1.2 Nanodiamond VFE transistor and triode characteristics

The three-terminal VFE devices, transistors and triodes, can be realized with the fabrication method developed in this thesis by proper placement of the electrodes. In the transistor configuration, electron emission is triggered by the nearby gate voltage and collected by the relatively far away anode electrode that acts as a current collector. The fabricated nanodiamond VFE transistors comprised of various emitter array sizes and a 600–μm anode-to-emitter gap have been characterized, showing both the reduction of gate threshold voltage and the increase of emission current with the number of emitter microtips in the transistor array. The VFE transistor with 100 x 200 nanodiamond emitter microtip array exhibited a low gate turn-on voltage of 25 V, a high anode current of 160 μA at a low gate bias of 34 V, and negligible gate current, suggesting the potential for practical applications of the nanodiamond VFE transistors. The transistor characteristics with distinct cutoff, linear, and saturation regions were obtained, agreeing with the transistor operating principle.

In the triode configuration, the anode electrode is located at much closer proximity to the emitter than that in the transistor case. The electron emission is induced by the voltage applied on the anode electrode, and modulated by the gate voltage. The triode characteristics were demonstrated, displaying anode-induced electron emission along with excellent gate-controlled emission current modulation that led to current enhancement or suppression depending on the gate biasing voltages. The VFE triode with 80 x 80 nanodiamond emitter microtips and a 4–μm anode-to-emitter spacing exhibited a low anode turn-on voltage of 30 V and a high anode current of 155 μA at very low operating voltages of V_a = 48.5 V and V_g = 5 V, demonstrating that the three-terminal VFE functional device is operable at low voltages and high emission current.

A systematic analysis of the field emission characteristics for the three-terminal VFE transistors and triodes based on the modified Fowler-Nordheim theory have been established and performed, confirming the electron field emission mechanism and operation principle of the devices. The device small signal coefficients, including amplification factor μ, transconductance g_m and anode resistance r_a, were extracted from the measured I-V data and studied as a function of bias conditions and anode-to-emitter distances, showing consistency with the modeling results based on electrostatic theory. The analysis of device coefficients provides a viable approach to understand the field emission mechanism of the transistor and triode and for further design of the device structure with desired performance for vacuum electronics and integrated circuits.

7.1.3 Small signal amplification applications

The practical application of the fabricated nanodiamond VFE transistors and triodes for signal processing and amplification has been discussed and evaluated experimentally. The voltage amplification performance was realized, measured, and verified by the proposed modified small signal equivalent circuit model, achieving a consistent method for analyzing the *ac* performance of VFE devices. The transistors with larger anode-to-emitter distance generally produce higher μ and hence higher voltage gain for signal amplification. The fabricated transistor with a 600–μm anode-to-emitter gap was found to have μ of 1400 experimentally, exhibiting an *ac* voltage gain of 50 (34 dB) at the bias condition of $V_a = 300$ V, $V_g = 32$ V and $g_m = 25$ μS, demonstrating a VFE voltage amplifier.

On the other hand, the triode which has small anode-to-emitter distance produces a low/medium μ, and can offer low output impedance in output stage as buffer amplifiers for avoiding signal distortion when connecting to the load. A r_a of 50 kΩ with a nearly unity gain of 1.84 was realized from the fabricated triode with a 4–μm anode-to-emitter gap and μ of 3 at the bias condition of $V_a = 48$ V and $V_g = 5$ V, demonstrating a buffer amplifier with unity gain and low output resistance.

The modified small signal circuit model was utilized to analyze the *ac* voltage amplification performance of the VFE triodes and transistors. The modeling results showed good consistency with the experimentally measured data, providing a useful method for predetermination of the device signal amplification behavior. These results also suggested a systematic method in designing VFE functional devices by engineering device geometry with variable transistor and triode coefficients for desired voltage gain and output resistance. Coupling with the capability into circuits, it can promote the development of vacuum ICs in critical components for advanced vacuum microelectronics.

7.1.4 Nanodiamond VFE integrated differential amplifier

A basic circuit building block of nanodiamond VFE integrated differential amplifier for vacuum IC has been developed and implemented. The well-controlled dual-mask microfabrication process involving the mold-transfer self-aligned gate-emitter technique coupled with nanodiamond deposition and gate partitioning enables the fabrication of the identical nanodiamond VFE transistor pairs on a chip. The fabricated VFE transistor pair showed well-matched field emission characteristics with low gate turn-on voltage and negligible gate intercept current, suggesting good common-mode-rejection performance and long-term operation capability of the diff-amp. A large CMRR of 540 (54.6 dB), which is consistent with the estimated value in the analysis model, was realized at an operating gate voltage of 42 V with a transconductance of 4 μS. And a CMRR of 60.7 dB, which is comparable with that of commercially available solid-state diff-amps, can be obtained by applying fully differential signals to the diff-amp. The enhancement of CMRR with increasing gate voltage as well as transconductance was observed, agreeing with the equivalent circuit analysis and suggesting that higher CMRR is achievable at higher operation voltage. The successful implementation of this basic circuit building block, consisting of an integrated VFE transistor diff-amp, demonstrates the feasibility of using vacuum-based ICs for practical applications, including high-speed and temperature- and radiation-hardened electronics.

7.2 Recommendations for future work

The future work on the nanodiamond VFE devices can be summarized as follows:

(i) Design and fabricate three-electrode nanodiamond VFE devices with optimized structures in terms of the microtip emitter array size, microtip emitter spacing, and reduce redundant device area for high frequency operation.

(ii) Develop a nanodiamond tip on pole structure with thicker SiO_2 dielectric layer between self-aligned gate and emitter substrate for high frequency operation.

(iii) Develop a microfabrication process utilizing the silicon substrate of SOI wafer as an integrated anode, instead of using electrostatic bonding anode, for realization of monolithic nanodiamond VFE triode in vertical configuration.

(iv) Develop nanodiamond VFE transistors and triodes with submicron/nano-scaled gate-to-emitter gap by reducing the thermal-SiO_2 thickness for ultra-low voltage device turn-on and operation.

(v) Apply the nanodiamond VFE integrated devices in other configurations of vacuum ICs, digital logic gates and complex electronic systems.

(vi) Develop packaging for the vertically-configured nanodiamond VFE devices .

(vii) Expand the basic VFE diff-amp building block to more complicated IC integration.

LIST of PUBLICATIONS

Research works related to this dissertation have been published in or submitted to the following peer-reviewed journals and conferences as listed below.

Journal papers:

1. **S. H. Hsu**, W. P. Kang, S. Raina, M. Howell, and J. H. Huang, “Nanodiamond vacuum field emission triode,” *IEEE Trans. Electron Devices*, 2014 (submitted).
2. **S. H. Hsu**, W. P. Kang, S. Raina, and J. H. Huang, “Nanodiamond vacuum field emission device with gate modulated triode characteristics,” *Appl. Phys. Lett.*, vol. **102**, p. 203105, 2013.
3. **S. H. Hsu**, W. P. Kang, J. L. Davidson, J. H. Huang, and D. V. Kerns, Jr., “Nanodiamond vacuum field emission integrated differential amplifier,” *IEEE Trans. Electron Devices*, vol. **60**, p. 487, 2013.
4. **S. H. Hsu**, W. P. Kang, J. L. Davidson, J. H. Huang, and D. V. Kerns, “Vacuum microelectronic integrated differential amplifier,” *Electronics Lett.*, vol. **48**, p. 1219, 2012.
5. **S. H. Hsu**, W. P. Kang, J. L. Davidson, J. H. Huang, and D. V. Kerns, “Performance characteristics of nanocrystalline diamond vacuum field emission transistor array,” *J. Appl. Phys.*, vol. **111**, p. 114502, 2012.
6. **S. H. Hsu**, W. P. Kang, A. Wisitsora-at, and J. L. Davidson, “Nitrogen-incorporated nanodiamond vacuum field emission transistor with vertically configured self-aligning gate,” *Diamond Relat. Mater.*, vol. **22**, p. 142, 2012.
7. A. Wisitsora-at, **S. H. Hsu**, W. P. Kang, J. L. Davidson, and A. Tuantranont, “Advanced nanodiamond emitter with pyramidal tip-on-pole structure for emission self-regulation,” *J. Vac. Sci. Technol. B*, vol. **30**, p. 022204, 2012.
8. **S. H. Hsu**, W. P. Kang, J. L. Davidson, and J. H. Huang, “Vertically configured nanodiamond vacuum field emission transistor arrays,” *ECS Trans.*, vol. **35**, p. 191, 2011.
9. **S. H. Hsu**, W. P. Kang, S. Raina, and J. H. Huang, “Triode characteristics analysis of nanodiamond vacuum field emission device,” *J. Appl. Phys.* (to be submitted).

Conference papers:

1. W. P. Kang, N. Ghosh, **S. H. Hsu**, S. Raina, and J. H. Huang, “Monolithically integrated nanodiamond vacuum lateral microtriode operable at low voltages,” IEEE Nanotechnology Materials and Devices Conference, Tainan, Taiwan, Oct. 2013.

2. N. Ghosh, W. P. Kang, **S. H. Hsu**, and S. Raina, “A monolithic multi-finger nanodiamond lateral vacuum microtriode,” 26th International Vacuum Nanoelectronics Conference, Roanoke, Virginia, Jul. 2013.

3. **(Best Paper Award)**
   S. H. Hsu, W. P. Kang, S. Raina, and J. L. Davidson, “Nanodiamond vacuum field emission triode signal amplifier,” 25th International Vacuum Nanoelectronics Conference, Jeju, Korea, Jul. 2012.

4. **S. H. Hsu**, W. P. Kang, S. Raina, and J. L. Davidson, “Vacuum field emission integrated differential amplifier,” 25th International Vacuum Nanoelectronics Conference, Jeju, Korea, Jul. 2012.

5. W. P. Kang, **S. H. Hsu**, N. Ghosh, J. L. Davidson, J. H. Huang, and D. V. Kerns, “Nanodiamond vacuum field emission integrated devices,” 25th International Vacuum Nanoelectronics Conference, Jeju, Korea, Jul. 2012.

6. A. Wisitsora-at, **S. H. Hsu**, W. P. Kang, and J. L. Davidson, “Advanced nanodiamond emitter using pyramidal tip on pole structure for emission self-regulation to improve performance,” 21st European Conference on Diamond, Diamond-like Materials, Carbon Nanotubes, and Nitrides, Budapest, Hungary, Sep. 2010.

7. **S. H. Hsu**, W. P. Kang, and J. L. Davidson, “Nanodiamond vacuum field emission transistor arrays,” 23rd International Vacuum Nanoelectronics Conference, Palo Alto, CA, Jul. 2010.

8. W. P. Kang, J. L. Davidson, K. Subramanian, Y. M. Wong, **S. H. Hsu**, N. Ghosh, and S. Raina, “Carbon-derived cold cathodes for vacuum electronic applications,” Nanotech 2010 Conference and Expo, Anaheim, CA, Jun. 2010.

9. **S. H. Hsu**, W. P. Kang, A. Wisitsora-at, and J. L. Davidson, “Nitrogen-incorporated nanodiamond field emission transistor with vertically configured self-aligning gate,” 4th International Conference on New Diamond and Nano Carbons, Suzhou, China, May 2010.

Additional publications on other research topics (supercapacitor, lithium-ion batteries, and dye-sensitized solar cells) conducted at Vanderbilt University:

1. S. Raina, **S. H. Hsu**, S. Akbulut, M. Yilmaz, W. P. Kang, J. H. Huang, and M. Howell, "Design and development of 3D nanostructured MnO_2/CNT electrodes for supercapacitor applications," 225th meeting of Electrochemical Society, Orlando, Florida, May 2014.

2. J. B. Kang, S. Raina, **S. H. Hsu**, S. Akbulut, and M. Yilmaz, "Advanced, flexible ultracapacitor electrodes on carbon fiber cloth using nano-architectured MnO_2/CNT," 225th meeting of Electrochemical Society, Orlando, Florida, May 2014.

3. S. Raina, Y. Zhang, **S. H. Hsu**, J. Chen, S. Z. Deng, N. S. Xu, J. H. Huang, and W. P. Kang, "A novel hybrid supercapacitor electrode utilizing vertically oriented grapheme nanosheets coated with conformal layer of pseudocapacitive MnO_2 nanoparticles," 225th meeting of Electrochemical Society, Orlando, Florida, May 2014.

4. S. Raina, **S. H. Hsu**, M. Yilmaz, S. Akbulut, W. P. Kang, and J. H. Huang, "$Li_2Fe_xMn_yCo_zSiO4$ nanoparticles incorporated CNTs as a novel high capacity cathode for lithium ion batteries," 224th meeting of Electrochemical Society, San Francisco, California, Oct. 2013.

5. S. Raina, **S. H. Hsu**, S. Akbulut, M. Yilmaz, W. P. Kang, and J. H. Huang, "Advanced MnO_2/CNT ultracapacitors – transition from planar to micropatterned array electrodes," 224th meeting of Electrochemical Society, San Francisco, California, Oct. 2013.

6. W. P. Kang, **S. H. Hsu**, S. Raina, S. Akbulut, M. Yilmaz, and J. H. Huang, "Micropatterned MnO_2/CNT ultracapacitor array with high volumetric capacitance," IEEE Nanotechnology Materials and Devices Conference, Tainan, Taiwan, Oct. 2013.

7. W. P. Kang, S. Raina, Y. Zhang, **S. H. Hsu**, J. Chen, S. Z. Deng, J. H. Huang, and N. S. Xu, "Vertically aligned graphene/MnO_2 nanosheets for ultracapacitor applications," 223rd meeting of Electrochemical Society, Toronto, ON, Canada, May 2013.

8. W. P. Kang, S. Raina, **S. H. Hsu**, M. Yilmaz, J. H. Huang, and A. Serkan, "A novel nano-structured ternary orthosilicate on carbon nanotube as lithium-ion battery cathode," 223rd meeting of Electrochemical Society, Toronto, ON, Canada, May 2013.

9. S. Raina, **<u>S. H. Hsu</u>**, W. P. Kang, and J. H. Huang, "Micropatterned MnO_2/CNT MEA ultracapacitors," 222nd meeting of Electrochemical Society, Honolulu, Hawaii, Oct. 2012.

10. S. Raina, **<u>S. H. Hsu</u>**, W. P. Kang, J. H. Huang, and M. Yilmaz, "In-situ electrochemical deposition of MnO_2 on CNTs for ultracapacitor applications," 222nd meeting of Electrochemical Society, Honolulu, Hawaii, Oct. 2012.

11. **<u>S. H. Hsu</u>**, M. Howell, and W. P. Kang, "Dye-sensitized solar cells with multiwalled carbon nanotubes and MnO_2-coated MWCNTs counter electrodes," 220th meeting of Electrochemical Society, Boston, Massachusetts, Oct. 2011.

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