EFFECTS OF SINGLE-EVENT-INDUCED CHARGE SHARING IN SUB-100 NM BULK CMOS TECHNOLOGIES

By

Oluwole Ayodele Amusan

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Approved:

Professor Lloyd W. Massengill

Professor Bharat L. Bhuva

Professor Arthur F. Witulski

Professor Michael L. Alles

Professor Mark N. Ellingham

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LIST OF ACRONYMS

ASET........ Analog Single Event Transient

CME........ Coronal Mass Ejection

CMOS........ Complementary Metal Oxide Semiconductor

DD........ Displacement Damage

DICE Latch........ Dual Interlocked Cell

DRAM........ Dynamic Random Access Memory

DSET........ Digital Single Event Transient

DUT........ Device Under Test

FWHR........ Full-Width, Half-Rail

GCR........ Galactic Cosmic Ray

IC........ Integrated Circuit

LET........ Linear Energy Transfer

N-S........ North-to-South

NIR........ Near-Infrared

MBU........ Multiple Bit Upset

RHBD........ Radiation Hardened By Design

SCR........ Solar Cosmic Rays

SE........ Single Event

SEB........ Single Event Burnout

SEE........ Single Event Effect

SEGR........ Single Event Gate Rupture

SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SOHO	Solar and Heliospheric Observatory
STI	Shallow Trench Isolation
TCAD	Technology Computer-Aided Design
TCR	Terrestial Cosmic Rays
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TPA	Two-Photon Absorption
TRIBICC	Time-Resolved Ion Beam Induced Charge Collection
W-E	West-to-East
WGR	With Guard-Ring
WOGR	With-Out Guard-Ring

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CHAPTER I

INTRODUCTION

Sub-100 nm technologies are more vulnerable than older technologies to Single Event Effects (SEE) due to the Complementary Metal Oxide Semiconductor (CMOS) scaling trend [Sei00], [Har01], [Bau02]. The increased SEE vulnerability can be attributed to several factors such as a decrease in the amount of charge required to represent a HIGH node voltage, reduced nodal separation, and reduced nodal capacitance [Joh98]. The CMOS scaling trend is due to the constant race for integration and higher packing densities to increase Integrated Circuit (IC) functionality. An adverse effect of this higher packing density, for the radiation community, is the increased probability of multiple nodes collecting charge from a single ion-strike (i.e., charge sharing) [Amu06a].

Charge sharing is a significant SEE issue because it can circumvent circuit-level hardening techniques [Amu07], an issue first discussed by Oshida *et al.* [Osh93] in 1993. Oshida *et al*. examined the effects of charge sharing in Dynamic Random Access Memory (DRAMs) and found that charge collection at the struck cell was lower in 256-Mbit DRAMs than in 64-Mbit DRAMS because of charge sharing at surrounding nodes. Conventional SEE Radiation Hardened By Design (RHBD) approaches such as Dual Interlocked Cell (DICE latch) [Cal96], Triple Modular Redundancy (TMR) [Pet80], or temporal latch [Mav00] provide excellent protection against Single Event Upsets (SEU) because they are based on the assumption that charge collection occurs on a single node after an ion strike. The single node charge collection assumption made RHBD designs

Single Event (SE) tolerant for older technologies, which had comparative larger nodal separation. However, for Sub-100 nm technologies, the nodal separation between devices is significantly smaller, and previous work [Amu07] has shown that charge sharing can result in multiple circuit nodes collecting charge from a single ion-strike, thereby increasing the SEE susceptibility of the RHBD designs. As CMOS processes continue to scale down, there is a continued decrease in the device nodal separation of each successive technology, but no change in the ionization radius of the heavy-ion striking the sensitive drains. Hence, charge sharing can be expected to become an increasingly prevalent SE issue for Sub-100 nm bulk processes.

This dissertation uses both Technology Computer-Aided Design (TCAD) and circuit simulations to analyze the effects of Single-Event-Induced charge sharing in Sub-100 nm Bulk CMOS technologies with the results verified through laser and heavy-ion experimental data. Chapter I introduces the motivation for this work. Chapter II presents background information on SEEs including an introduction to the space environment and to the various sources of radiation. Also covered in this chapter are the effects of irradiation on microelectronic circuits, including charge generation and charge collection mechanisms. The last section of Chapter II introduces the modeling and simulation techniques used for analyzing SEEs. Chapter III examines the basic difference in charge collection mechanisms for NMOS and PMOS devices, and proposes optimized transistor sizing to reduce SE pulse-widths based on this difference. Chapter III also provides laser data verifying the existence of the parasitic bipolar amplification effect in PMOS devices. Chapter IV introduces the charge sharing effect and discusses some of the previous charge sharing research efforts and provides the first experimental data verifying the charge sharing effect. This chapter also details the quantification of normal vs. angular effects of charge sharing. In addition it provides heavy-ion data that verifies and demonstrates the significance of considering charge sharing angular effects during circuit

characterization. Chapter V examines the effectiveness of different charge sharing mitigation techniques, including layout techniques. This chapter also provides heavy-ion data that verifies the effectiveness of the different charge sharing mitigation techniques.

The work presented in this dissertation directly impacts the SEE circuit qualification techniques used in the radiation community by showing how underestimation of SE cross-section and Linear Energy Transfer (LET) threshold could occur as a result of charge sharing in the Sub-100 nm technologies. The layout mitigation techniques proposed and verified through heavy-ion experiments are also very useful for improving the radiation hardness of the Sub-100 nm technologies and provides designers with layout guidelines for use in space-borne applications.

CHAPTER II

SINGLE EVENT EFFECTS - BACKGROUND

Introduction

For microelectronic circuits, irradiation can cause device damage through effects such as Total Ionizing Dose (TID), Displacement Damage (DD), and SEE. This work is focused on SEE; hence TID and DD effects will be omitted. Reference materials providing detailed discussions of both TID effects [Emi96], [Ale96], [Ler99], [Sch02], [Old03a], [Ale03], [Bar05] and DD effects [Sro88a], [Sro88b], [Sum92], [Bra94], [Mar99], [Sro03] are listed for the interested reader.

SEE effects in microelectronics is of major concern because SEEs are caused by a wide range of energetic particles such as protons, neutrons, alpha particles, and heavy-ions that strike sensitive regions (i.e., reverse-biased junctions) of the microelectronic circuit, thereby causing temporary or permanent errors. SEEs were first theorized by Walmark *et al.* [Wal62] in 1962 to cause significant damage to circuits and Binder *et al.* [Bin75] made the first observation of upsets due to cosmic-rays in 1975.

The rest of this chapter will discuss: CMOS scaling and the implications for SEEs, different radiation environments, fundamental charge generation and collection mechanisms, charge collection effects on microelectronics, the types of manifestations that can occur in microelectronics due to SEEs, and the modeling and simulation techniques used to investigate and analyze SEEs.

CMOS Scaling

One of the significant technological advancements over the last 40 years is the scaling of CMOS ICs [Tho05]. Figure 1 [Tho05] shows the history of transistors, starting with the initial concept of the field-effect transistor in 1933, the first bipolar junction transistor that was successfully produced in 1947 by Bardeen, Shockley and Brattain with a gate length of approximately 100 μm [Bar48], [Sho51], and a state-of-the art transistor with a gate length of 37 nm [Tho05]. CMOS scaling has directly affected technological advancement, from computer technology to the increased use of portable devices. The CMOS scaling trend has followed Moore's Law as shown in Fig. 2 [Moo98], which was originally proposed in 1965, and states that: The number of transistors on a chip would double every two years for the next ten years. To achieve Moore's Law, significant inroads have been made by the semiconductor industries in terms of reducing device parameters such as device dimensions, operating voltage, gate oxide thickness, gate length, nodal separation of the devices, nodal capacitance, etc. This has lead to improvements such as: significant increase in performance and speed, decrease in IC cost, and smaller chips with greater functionality for CMOS technology.

However, for the radiation community, these so-called "improvements" have had a negative impact and CMOS scaling trends have exacerbated SEEs [Old03b]. The reduction in gate oxide thickness and nodal capacitance makes it easier to cause an upset [Joh98], the reduced gate length increases the parasitic bipolar effect [Dod96], and the decrease in the nodal separation and desire for higher packing density increases the probability of charge sharing during an ion-strike [Amu06b]. Two of the SEE effects directly related to CMOS scaling trends, parasitic bipolar amplification and charge

sharing will be discussed extensively in this chapter. Reference materials providing detailed discussions of CMOS process and material scaling trends and effects on SEEs [Dod96], [Joh98], [Old03b] are listed for the interested reader.

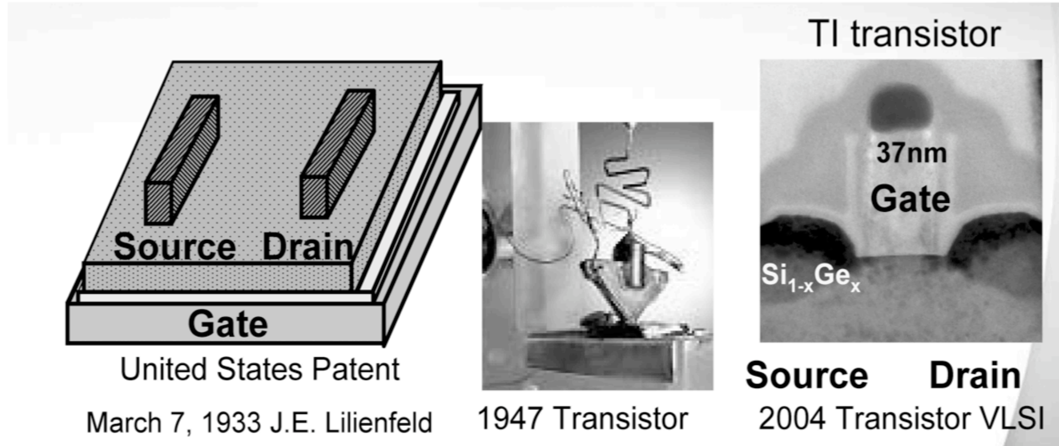


Fig. 1. History of Transistors [Tho05].

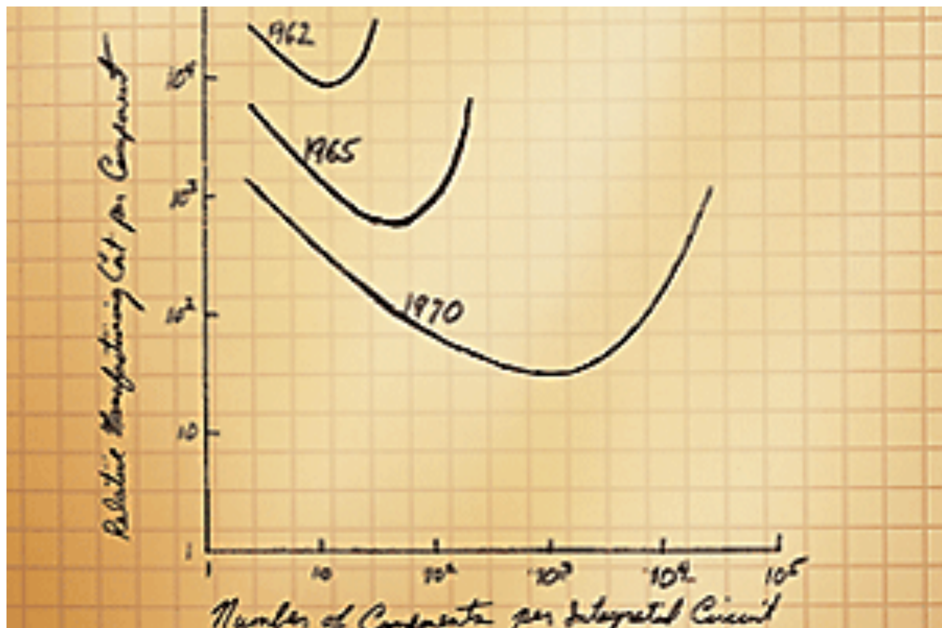


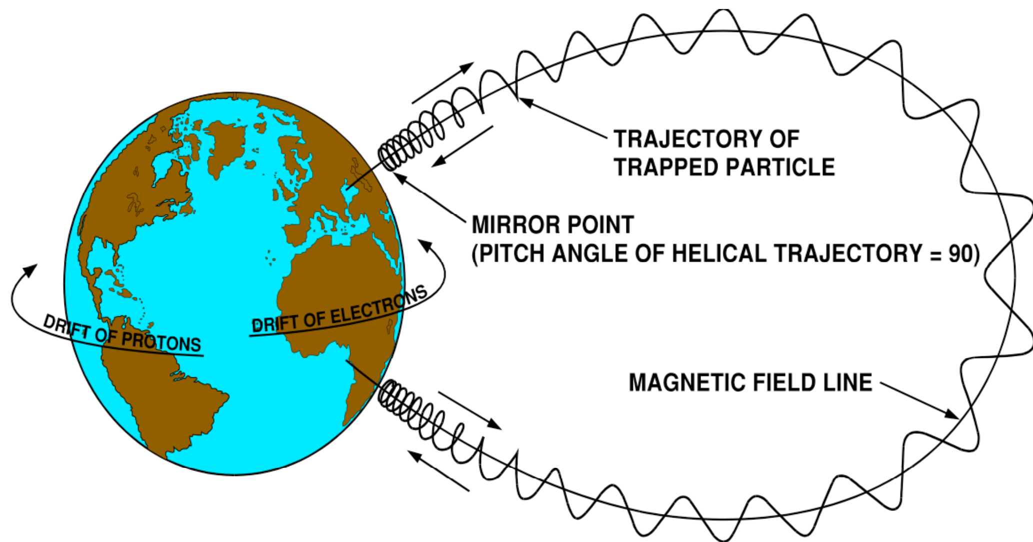
Fig. 2. Moore's original graph predicting the scaling trend [Moo98].

Radiation Environment

One of the many considerations for designing space-bound microelectronics is exposure to space radiation environment. The effects of the space radiation environment on these microelectronics is of major concern for a number of reasons including the cost of developing space-bound electronics, the unavailability of replacements or repair in the event of a failure, and the harsh temperatures to which they are exposed. Hence, studies on the space environment provide a means for designing reliable space-borne electronics with longevity. The main contributors to the high-space radiation environments are cosmic rays, solar flares, and trapped radiation [Sta88]. Each represents various levels of radiation in space that can have adverse effects on microelectronics and are discussed in detail below.

Trapped Radiation Environment

The Earth's magnetic field can affect the trajectory of charged particles evolving in the near-Earth space. Some charged particles become trapped in the geomagnetic field lines and follow relatively reliable and stable trajectories as shown in Fig. 3 [Sta88]. The Earth's trapping phenomenon leads to an accumulation of particles in specific areas of the magnetosphere called the Van Allen Belts discovered by Van Allen [Van59]. Research has shown that there are two permanent belts; the inner belt and the outer belt as illustrated in Fig. 4 [Bar03]. The inner belt extends 2.5 Earth radii, where one Earth radius is 6380 km, and consists of energetic protons up to 600 MeV in combination with electrons up to several MeV, as shown in Fig. 5 [Sta88]. The outer belt is also shown in Fig. 5 [Sta88] extending to 10 Earth radii and consisting mainly of electrons. Occasionally, temporary radiation belts may appear due to intense solar activity.



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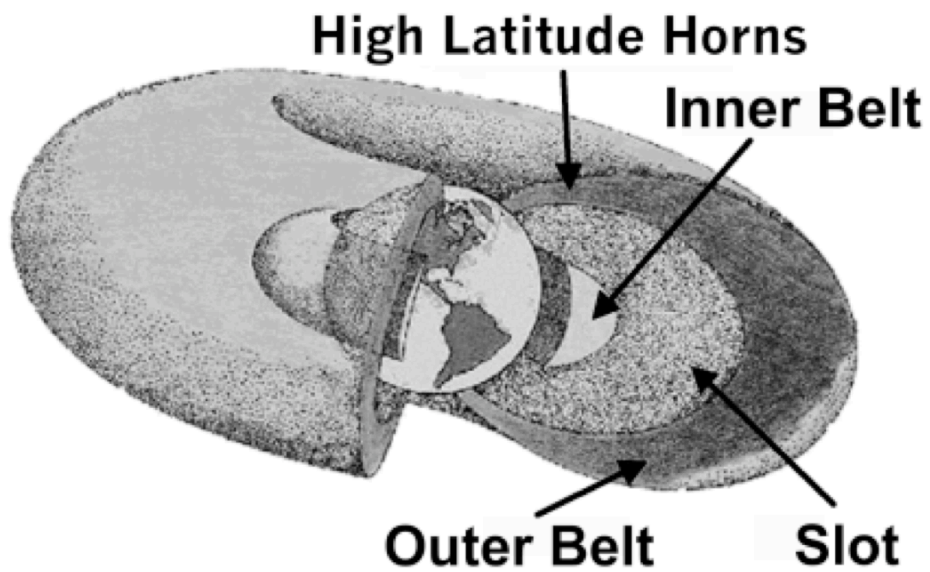


Fig. 4. Artist's drawing of the Earth's Van Allen radiation belts [Bar03].

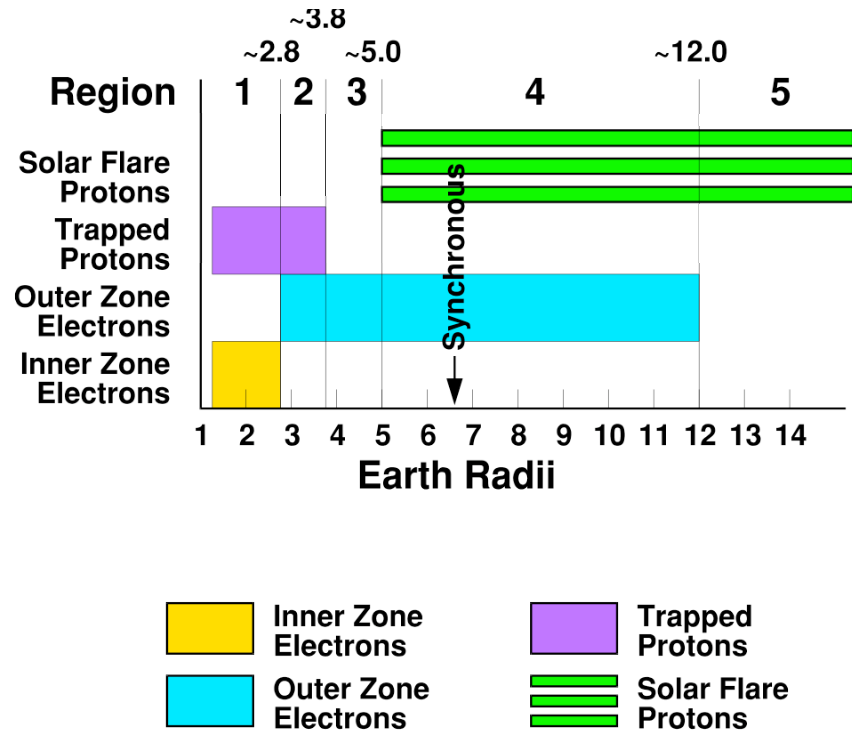


Fig. 5. Boundaries of the domain of Van Allen radiation belts [Sta88].

The origins of trapped particles are not yet completely understood. However, the contributing sources to the formation of the radiation belts are believed to be solar flares, cosmic ray particles from interplanetary space, reaction products from Galactic Cosmic Ray (GCR) collision with nuclei atoms present in the Earth's upper atmosphere (O and N), and exo-atmospheric nuclear explosions [Sta88].

The proton belt is a prominent source of SEE for spacecrafts as protons are capable of penetrating spacecrafts and prolonged exposure to the energetic protons, can damage instruments or be hazardous to astronauts. Associated with the proton belt is a singular anomaly called the South Atlantic Anomaly. The anomaly is located off the coast of South America and displays a large increase in proton flux at altitudes less than 1000 – 2000 km as shown in Fig. 6 [Bar97]. The anomaly results because of the tilt of the

Earth's magnetic pole from the geographic pole and the displacement of the magnetic field from the center, causing a dip in the Earth's magnetic field over the South Atlantic Ocean. This dip results in a bulge at the underside of the inner belt [Bar03], thereby allowing cosmic rays and other charged particles to reach lower into the atmosphere. The large increase in proton flux (> 30 MeV) can cause significant SEs for satellites, aircrafts, and space shuttles operating in the region.

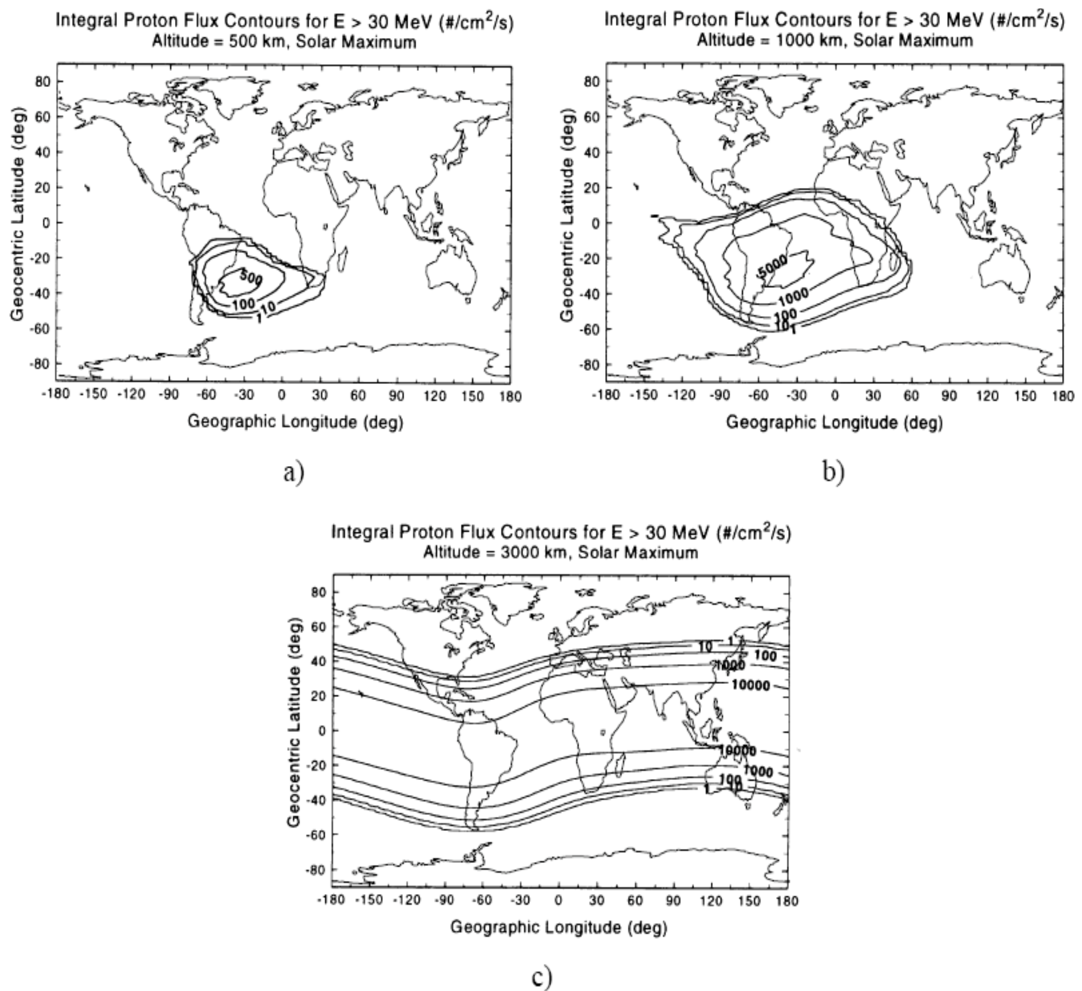


Fig. 6. The South Atlantic Anomaly is the principal geographic feature of low altitude proton belts. Integral proton flux contours as a function of latitude and longitude. Altitudes are a) 500 km, b) 1000 km, and c) 3000 km. Note the South Atlantic Anomaly, which is visible at lower altitudes but disappears by 3000 km [Bar97].

Cosmic Rays

There are three main sources of cosmic rays: Galactic Cosmic Rays (GCR), Solar Cosmic Rays (SCR), and Terrestial Cosmic Rays (TCR). GCR represent the 'primary' high-energy charge particles. While the source of GCRs is still unknown, they are believed to have originated somewhere outside the solar system and are assumed to be remnants from nova and supernova explosions. The spectrum of ions represented in GCRs spans across most of the elements in the periodic table as shown in Fig. 7 [Mey74]. The major constituents of GCRs are Protons (H^+) and Alpha Particles (He^{2+}), which represent 83% and 13% of the spectrum, respectively. The remaining particles are high-energy electrons (3%) and ions with $Z > 2$ (1%). While the heavy-ions represent a small portion of GCRs, they are highly energetic particles that cannot be stopped by spacecraft shielding and can interact with on-board electronics. SCRs consist mainly of protons but also include helium, heavier elements, and electrons. SCRs originate from tremendous explosions at the surface of the Sun (i.e., solar flares). TCRs originate from the Earth's atmosphere and can contribute to SEs. TCRs are the result of a shower of daughter particles that can be sensed at ground level and consist mostly of proton, neutrons, pions, muons, electrons, and photons (see Fig. 8 [Zie98]) and can cause significant software failures in electronics.

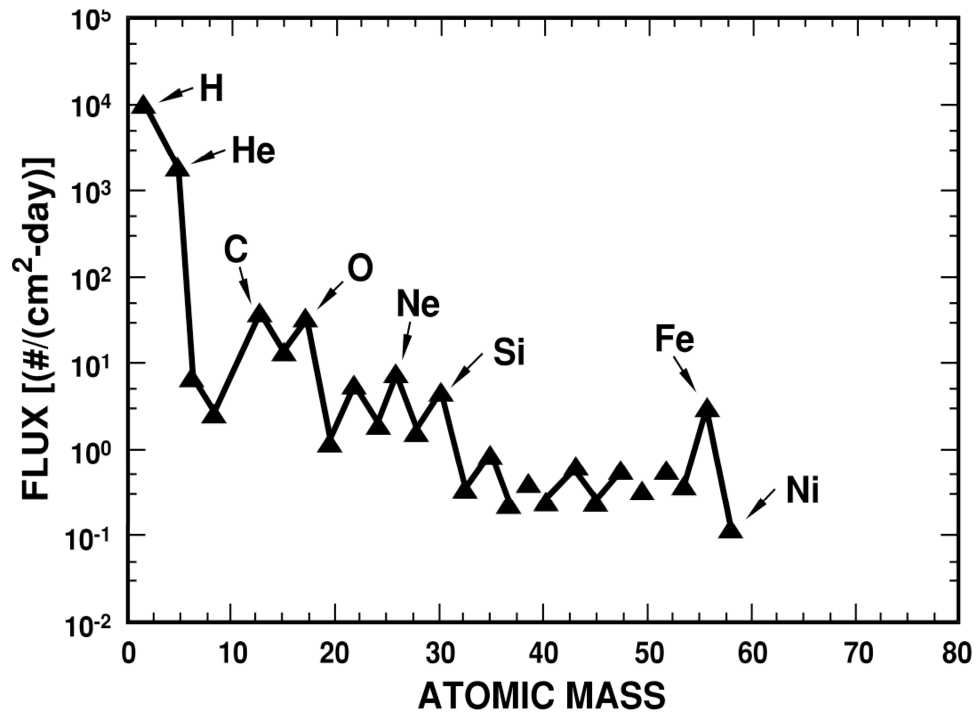


Fig. 7. Galactic cosmic ray particle spectrum as a function of atomic mass [Mey74].

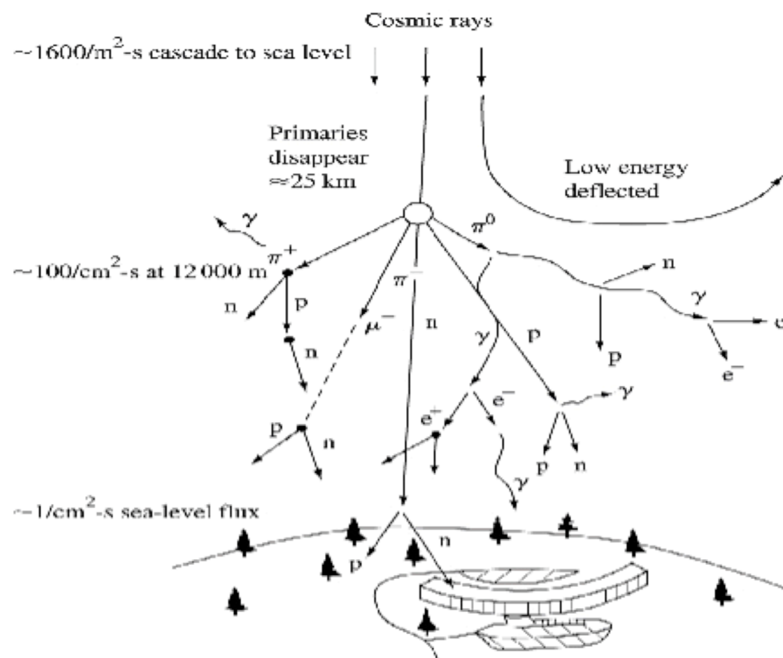


Fig. 8. Schematic of how cosmic rays cascade into a shower of secondary particles interacting with the Earth's atmosphere [Zie98].

Solar Flares

Solar flares have been discussed as part of the SCR section. Fig. 9 [NAS01] shows the largest solar flare on record. The Solar and Heliospheric Observatory (SOHO) satellite captured this flare on the 2nd of April, 2001. The Sun's solar cycle averages a span of 11 years with 7 years of high activity and 4 years of relative inactivity. Another form of emission from the Sun is Coronal Mass Ejection (CME), which is the discharge of huge bubbles of gas. The CME can release 10^{17} grams of plasma and is rich in protons. CME tends to disrupt the solar wind and can produce disturbances that strike the Earth, causing significant damage to microelectronic.

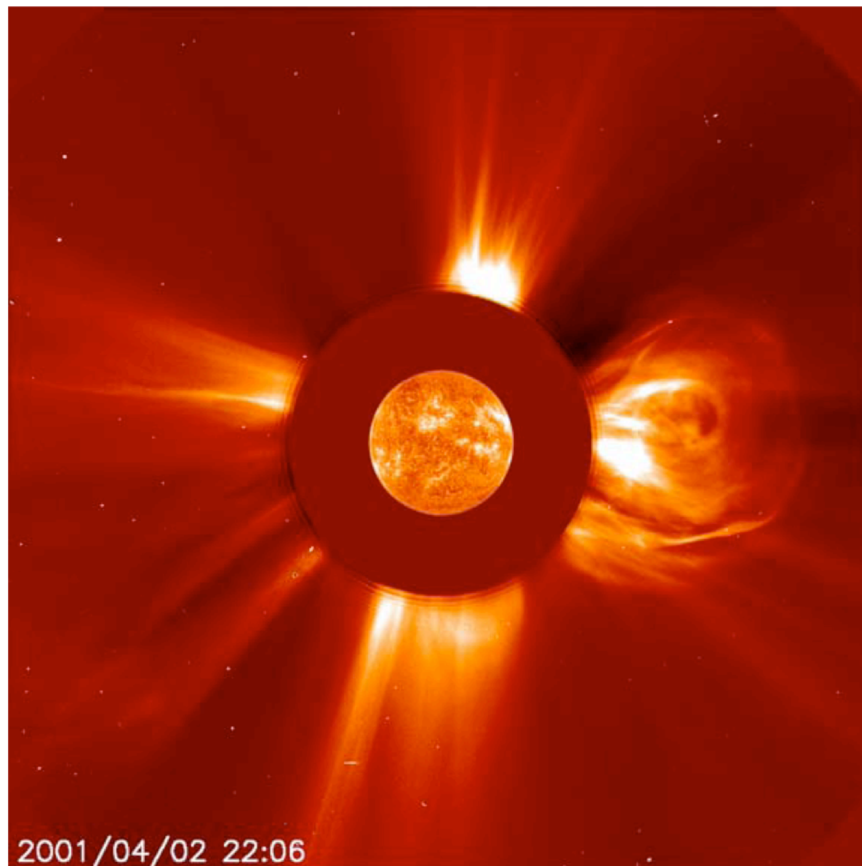


Fig. 9. The largest solar flare ever recorded unleashed as observed by the SOHO satellite, on Monday, April 2, 2001 [NAS01].

Basic Single Event Mechanisms

Charge Generation

Ionizing radiation generates charge in a semiconductor device through two primary mechanisms, which can cause significant damage to microelectronic circuits. The first method (indirect ionization) is a result of the nuclear interaction between an energetic particle and a struck device, which results in ionization by secondary particles. The second method is through direct ionization by energetic particles. Both mechanisms are discussed in detail below.

Indirect Ionization: As mentioned above, indirect ionization is a result of the nuclear interaction between an energetic particle and a struck device, thereby resulting in ionization by secondary particles. The energetic particle in this case refers to lighter particles such as protons and/or neutrons, which can produce significant upset rates due to indirect mechanisms by undergoing elastic collisions with a target nucleus [Pet81], [Wro00]. Examples of nuclear reactions than can occur due to the interaction between lighter particles and struck devices include: 1) elastic collisions producing Si recoils; 2) Alpha/Gamma particle emission and the recoil of a daughter nucleus (e.g., Si emits alpha-particle and a recoiling daughter Mg nucleus), and 3) spallation reactions (target nucleus is broken into two fragments (e.g., Si breaking into C and O ions), all of which can independently recoil [Dod99]. Any of these nuclear reactions can produce particles heavier than the original proton/neutron (i.e., the same as a heavy-ion particle), thereby resulting in direct ionization that can cause upsets. Typically, inelastic collision products have fairly low energy and do not travel far from the particle impact site. The secondary particles also tend to scatter forward in

the direction of the original lighter particles; hence a significant angular dependence on SEU sensitivity in microelectronic circuits [Ree94], [Ree02], and [Tip06].

Direct Ionization: For heavy-ion upsets, where a heavy-ion is defined as any ion with an atomic number greater than or equal to two (i.e., particles other than protons, electrons, neutrons, or pions), the primary charge deposition mechanism is direct ionization. Direct ionization occurs when an energetically charged particle passes through a semiconductor material and frees electron-hole pairs along its path as it loses energy. The total path length traveled by the energetic particle before coming to rest in the semiconductor is referred to as the particle *range*. The term *linear energy transfer* (LET) is typically used to describe the energy loss per unit length of a particle as it passes through a material [Mas93]. LET is measured as MeV·cm^2/mg, and represents the energy loss per unit path length (in MeV/cm) normalized by the density of the target material (in mg/cm^3), so that the LET is roughly independent of the target. In silicon, the average energy required to produce these electron-hole pairs is 3.6 eV, and silicon has a density of 2328 mg/cm^3 [Sze81], hence an LET of 97 MeV·cm^2/mg corresponds to a charge deposition of 1 pC/µm. This conversion factor of ~100 provides an approximate means for going back and forth between energy loss (LET) and charge deposition.

Charge Collection and Transport

The previous section described the charge generation process from irradiation, while this section focuses on charge collection and transport of the charge generated from the ion-strike. The three main mechanisms governing the charge collection process are: 1)

Drift (charge can transport in response to applied or built-in fields in the device), 2) Diffusion (charge can transport due to carrier concentration gradients within the device), or 3) Recombination (two carriers of opposite charge (an electron and a hole) can be annihilated by recombining with each other) [Pie89]. The charge collection and conduction process occur through depletion region drift collection, field-assisted funneling collection and diffusion collection. Figure 10 [Bau05] depicts the charge collected as a function of the various mechanisms involved. The final consequence of these free carrier generation and collection processes is the creation of a photocurrent at the terminals of the struck device [Mes82].

Depletion region drift occurs due to the high electric field present in a reverse-biased junction depletion region. The reverse-biased p-n junction represents the most sensitive region during charge collection and can efficiently collect the particle-induced charge through drift processes. Depletion region drift collection can result in a transient current at the junction contact. The time period typically associated with drift collection is extremely small as the saturation velocity of carriers limits the drift. For electrons in Si, saturation velocity is 1×10^{7} cm/sec [Mul03].

Another collection process is known as the field funneling collection process, which was discovered by IBM researchers in 1981[Hsi81], [Hsi83]. The “field funnel” is due to a transient disturbance of the junction electrostatic potential. The high charge density connects the deposited charge with the depletion region. Hence, the high field region is extended. The collapsed junction is due to the highly conductive nature of the charge track and the separation of the charge by the depletion region field. This collapse can lead to a situation where charges that were not initially exposed (outside the depletion

junction) to the electric field assisted drift are pushed to the junction contacts due to the "funneling" action. The overall result is an increase in the charge collected by the drift process, thereby helping to initiate the node voltage flip.

The last collection process is the diffusion collection process, which is the diffusion of charge to the contact. The main factor that determines the charge diffusion collection process is the diffusion junction length. It should be noted that the diffusion collection process is a much slower process in comparison to the drift collection process. While charge collection amplification effects such as parasitic bipolar amplification and charge sharing are not discussed in this section, they will be covered extensively in succeeding chapters.

A consequence of the charge generation and charge collection process is the radiation-induced photocurrents at the device terminals. The shape of the current pulse can be related to the dynamics of charge collection and current can be expressed as $I=dQ/dt$ (where I is the current, Q is the charge, and t is the time). As the collection process is dependent on the drift and diffusion collection processes, the initial spike in the current pulse shape as seen in Fig. 11 [Nas93] represents the drift component of the collection process, and the slow long tail decrease in the current pulse shape represents the diffusion collection process. The photocurrent pulse represents the bridge between the microscopic world of nuclear reactions, molecular interaction of coulomb forces, and the macroscopic world of solid state devices and integrated circuits. The circuit response to irradiation is dependent on the photocurrent and the different effects of irradiation on circuit response are discussed in the next section.

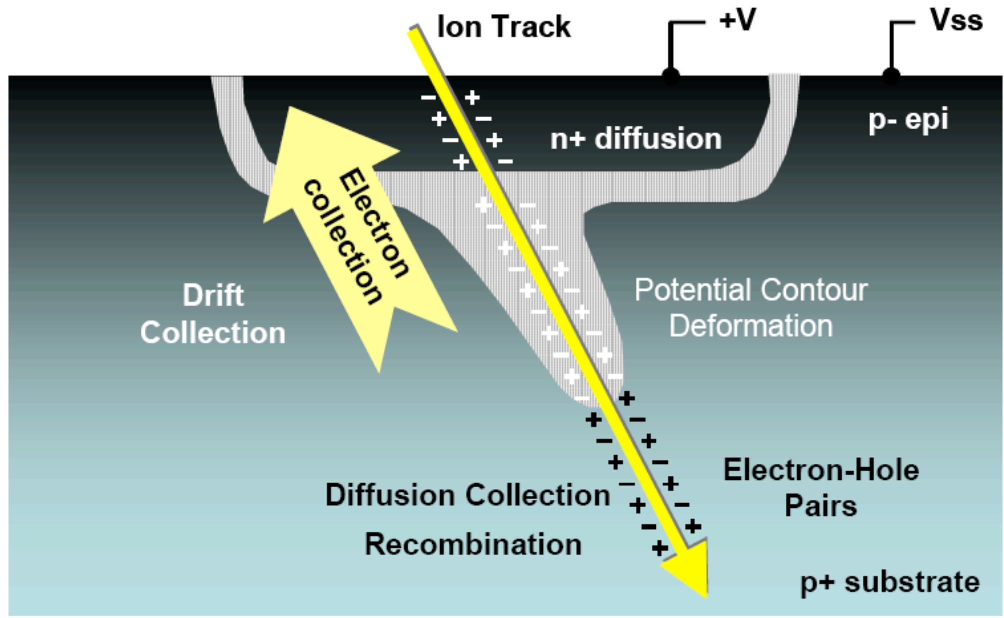


Fig. 10. Illustration of an ion strike on a p/n junction showing the drift, diffusion, recombination, and field funneling collection processes [Bau05].

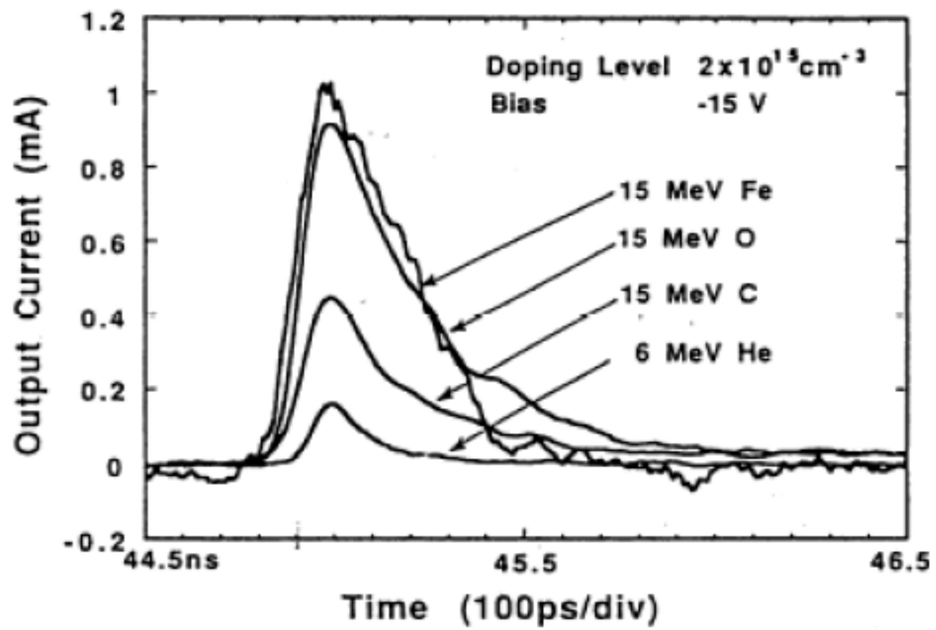


Fig. 11. Current transients as a function of time for a series of ions with different energies. The spike is due to the drift collection process and the gradual decay is due to the diffusion collection process [Nas93].

Circuit Response

As previously stated, irradiation can result in device damage due to the generation of charge and collection of the generated charge. The circuit response from the irradiation can be a destructive effect (i.e., hard error) or a temporary effect (i.e., soft error). This section will discuss a variety of more common destructive and temporary SEE failure modes.

Permanent Errors

Permanent errors imply destructive, irreversible damage to the circuit functionality, typically involving physical damage to the device. Three main types of destructive SEEs are: Single Event Burnout (SEB), Single Event Gate Rupture (SEGR), and Single Event Latchup (SEL).

An SEB is typically observed in power bipolar and MOSFET transistors. SEB is a destructive failure mechanism that depends on the currents generated by the ion strike. The current generation turns on either the parasitic or active bipolar device, and triggers a regenerative feedback mechanism, secondary breakdown, or snap-back [Gal96]. If the high current is not limited and a permanent short occurs between the source and drain, it will eventually lead to the burning out of the device or metallization [Was86].

An SEGR is a failure in the insulating material separating the gate and channel region due to the electric field across the insulating material exceeding a threshold value. This effect can also occur in concurrence with SEB [Dod99]. An SEGR occurs when an ion strikes the gate oxide and charge is transported near the $Si/Si0_2$ interface. The accumulation of the ion-strike charge underneath the gate region (and depending on the

gate bias) results in an increase in the electric field of the insulator, thereby causing a localized dielectric failure.

An SEL is an effect common to CMOS devices due to the presence of the n-p-n-p junction in the process. The parasitic latchup structure inherent to bulk CMOS structure is shown in Fig. 12 [Joh96]. An SEL can be initiated by ionizing radiation when the ion-strike causes a current to flow from within the well/substrate junction, thereby causing a voltage drop in the well. The voltage drop leads to the forward biasing of the vertical device, which in turn leads to an increased current in the substrate. The increase in substrate current causes a voltage drop in the substrate, which turns on the lateral device. The resulting effect is an increase in the current flow at the base of the vertical device, initiating the positive feedback loop. Once the latchup is triggered, the sustained high current can destroy the device due to the thermal runaway or failure of metallization [Joh96]. A reduction in power or removing power from the device in the latched state can help return the device to normal operation, thereby preventing destructive failure.

Temporary Errors

Temporary errors can occur as a spurious signal (i.e., Single Event Transient - SET) or a latched spurious signal (i.e., Single Event Upset) as a result of an ion-strike. An SET is a voltage glitch in the normal circuit operation due to a SE, where the SE is the interaction of a single ionized particle with a semiconductor. The SETs can occur in digital circuits as Digital Single Event Transient (DSET) or in analog circuits as Analog Single Event Transient (ASET). An SEU is a bit flip or change of state induced in a device by an SE. The change of state or upset can become an error if the signal is latched or misinterpreted as valid data by other circuitry. For this work, SETs and SEUs are

major discussion points since charge sharing and parasitic bipolar amplification of SE currents can create temporary errors. Multiple Bit Upset (MBU) is another kind of temporary error wherein multiple circuits are affected from one event spreading to multiple sensitive nodes spaced close together.

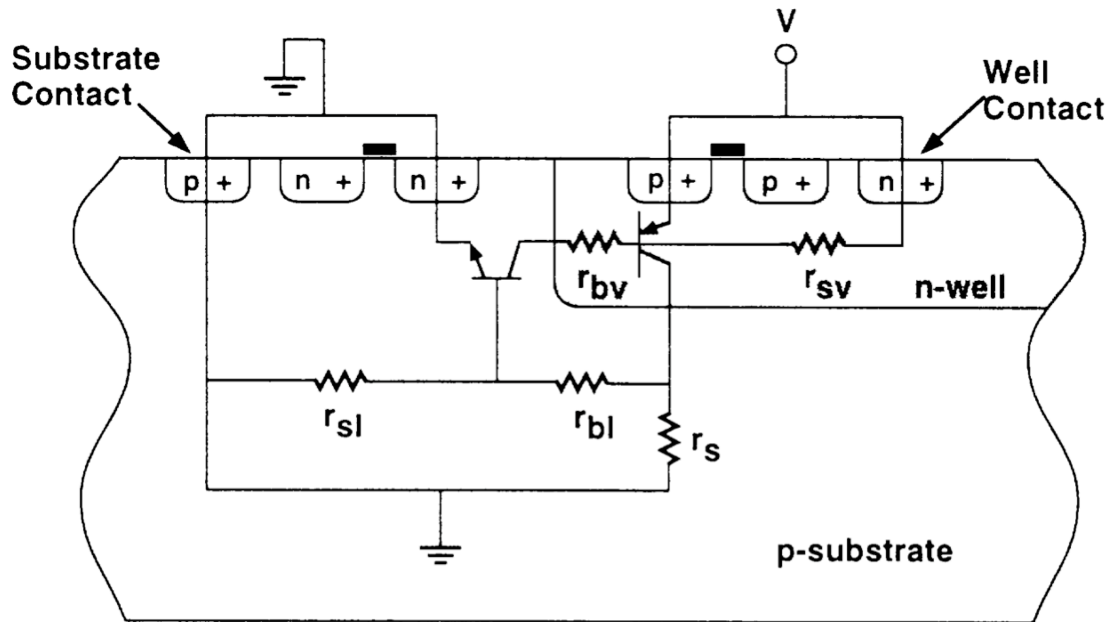


Fig. 12. Illustration of the parasitic latchup structure inherent to bulk CMOS technologies [Joh96].

Single Event Effects Modeling and Simulation

The modeling and simulation of SEEs provides insight into the effects of irradiation on microelectronic devices. The modeling and simulation tools for predicting and analyzing the effects of irradiation include: circuit simulators for modeling the circuit response to a single event, device simulators for predicting the physical interaction between the charge generation and device reaction, and codes that can help predict error

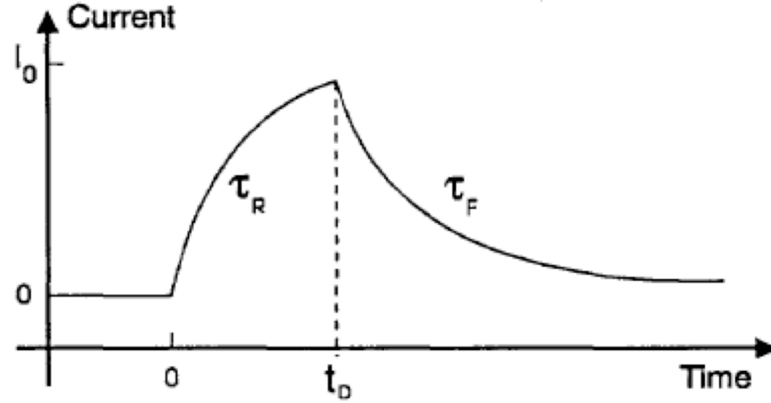
rates for a particular orbit. As this works makes use of circuit simulation and device simulators, the importance of the two simulators are discussed below.

Device simulators

Examples of device simulators include: Stanford's PISCES, Silvaco's Atlas and Athena, GENESIS, PADRE, DaVinci, MEDICI, and Synopsis's Structure Editor. Device simulators use the information such as the doping prolife to determine the interaction of the device with the ion strike. Device simulators provide a cost effective means for analyzing different effects of device irradiation. The generated currents at the device terminals can be used in circuit simulators to determine the effects of the irradiation on circuit functionality.

Circuit simulators

Examples of circuit simulators include: Berkeley's SPICE, Silvaco's SmartSpice, Mentor's AccuSim, Synopsis HSPICE, and Cadence Virtuoso Spectre. Circuit simulators can be used for simulating complex circuit designs from a macro-model view of the devices. As the models are typically generated by extensive measurement of a given technology, circuit simulations tend to represent realistic circuit performance and provide a cost effective way for analyzing the radiation performance of a circuit design. While it is true that circuit simulators sacrifice accuracy in device modeling, they make up for it with vastly increased computational throughput. For SE circuit simulations, a typical practice is to use a double-exponential current pulse to represent the ion-strike photocurrent as shown in Fig. 13 [Mas93].



$$I(t) = \begin{cases} I_o\left(1 - e^{-t/\tau_R}\right) & ; \ t < t_D \\ I_o\left(1 - e^{-t_D/\tau_R}\right) e^{-(t-t_D)/\tau_F} & ; \ t > t_D \end{cases}$$

$$Q = I_o\left[t_D + \tau_F - \tau_R - (\tau_F - \tau_R)e^{-t_D/\tau_R}\right]$$

Fig. 13. The double exponential pulse used for circuit simulations and the equations defining it are represented above. The total charge (Q) delivered by the current pulse is obtained by the integral over time of I(t) [Mas93].

As seen in Fig. 13 [Mas93], the double exponential current pulse has a rise time in the order of tens of picoseconds (ps) and a fall time on the order of 200 ps to 300 ps. However, due to scaling trends, recent results by Mavis *et al.* [Mav06] and DasGupta *et al.* [Das07a] has shown that the double exponential current pulse might not accurately predict the SE current pulse generated from the ion-strike for Sub-100 nm processes. To navigate around this issue, simulators that incorporate both device and circuit simulations, called mixed-mode simulators, can be used. Most of the current device simulators also function as mixed-mode simulators. Mixed-mode simulations allow for

device-level ion interaction while factoring in the circuit level effects. The use of mixed-mode simulators also allows for a more realistic current pulse shape that is dependent on the ion-strike energy, strike location, and circuit state. Different physics models can be implemented during mixed-mode SE simulations and a detailed discussion on specific considerations of models for SE simulations is provided by [Law06]. Device, circuit, and mixed-mode simulations have all been used to determine and analyze the mechanisms and effects of parasitic bipolar amplification and charge sharing in Sub-100 nm technologies and will be discussed in the following chapters.

CHAPTER III

SINGLE DEVICE CHARGE COLLECTION EFFECTS ON SINGLE EVENT TRANSIENTS

Introduction

This chapter focuses on the effects of an ion strike on a single device. It provides an understanding of the charge collection process differences between NMOS and PMOS devices, and explains the basic charge collection mechanisms in Sub-100 nm twin-well bulk CMOS technologies. It also presents laser data verifying the parasitic bipolar effect in PMOS devices. This chapter also introduces the charge collection process that occurs when multiple devices collect charge from a single ion strike (i.e., charge sharing). The ion-strike effects on the voltage transient are used to provide an optimum transistor sizing for designers.

The voltage pulse duration at the affected node [Baz97] (or at any of the subsequent nodes through which a SET propagates) is one measure of the severity of a SET pulse in combinational logic. SET pulse width indicates the amount of charge collected at the hit node, the rate at which the charge accumulates at the node, and the rate of charge removal from the node. Several popular SE hardening schemes utilize temporal filtering to eliminate SET pulses below a pre-determined threshold pulse width [Nic99], [Mav02], [Bal05], [Shu06]. Either reducing the amount and rate of charge collected, or increasing the rate at which the collected charge is removed, reduces the SET pulse width (and reduces the vulnerability of the hit node). This dichotomy offers the opportunity to

exploit design tradeoffs in optimizing area, power, speed, and SEE-tolerance in RHBD approaches.

In Sub-100 nm twin-well bulk CMOS technologies with p-substrate, parasitic elements in the CMOS structure lead to significantly different PMOS and NMOS device charge collection characteristics, especially the temporal nature of the currents related to charge collection. This chapter provides analysis and quantification of the differences in SET pulse widths for NMOS ion-strikes (i.e., n-hit) and PMOS ion-strikes (i.e., p-hit). This chapter also includes analysis of the effect of n-well contact distance to the device and n-well area on SET pulse widths. This study allows quantification of the effectiveness of RHBD design techniques in both (1) reducing the collected charge and (2) increasing the rate of charge removal. These results of RHBD design reduce the average SET pulse width generated at a combinational logic node for enhanced SE mitigation. These metrics form a basis for the development of RHBD design rules governing device sizing. This chapter shows that device-sizing design rules can incorporate optimized area, power, speed, and single-event radiation tolerance.

Single Device Charge Collection

The charge collected at a hit node for a given deposited charge (i.e., Linear Energy Transfer - LET) equals the sum of drift, diffusion, and parasitic bipolar amplification of the SE-related currents [Mas93]. Figure 14 shows a 2D cross-section view, which includes: the n-well, p-well, p^+ deep well, p-substrate, Shallow Trench Isolation (STI), and the parasitic bipolar device for NMOS and PMOS devices. The amount of charge collected due to an ion hit depends on all three mechanisms and can vary between NMOS

and PMOS devices of a given technology.

To examine the single device charge collection and pulse widths, 3-D TCAD mixed-mode simulations were conducted on calibrated device models from a commercial 90 nm bulk CMOS, twin-well process available through the MOSIS foundry-access system. The 3-D TCAD structures were developed with Synopsis Structure Editor and Sdevice simulator and calibrated to match DC and AC electrical characteristics (e.g., I_d-V_d and I_d-V_g curves) obtained from the standard compact models for this technology [Das07b].

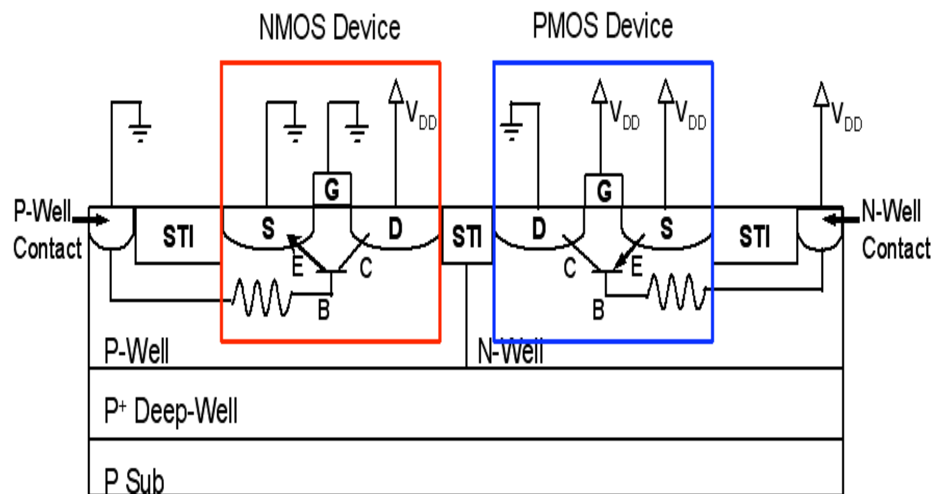


Fig. 14. CMOS cross section view showing parasitic elements. The NMOS device has a lateral parasitic npn bipolar transistor and the PMOS device has a lateral parasitic pnp bipolar transistor.

For these simulations, examination of the charge collection and pulse width generated from an ion hit employed a 5-stage minimum-sized matched-current-drive inverter chain with the 3-D TCAD (i.e., struck NMOS and PMOS device) structure in the 3rd stage. The IBM 90 nm bulk CMOS compact models were used for the simulations. The PMOS W/L size was 480 nm / 80 nm and the NMOS W/L size was 200 nm / 80 nm. All simulations were conducted using the Vanderbilt ACCRE computing cluster [ACC94]. In all

simulation results, charge collected was determined after saturation occurs for the integrated SE generated current pulse, and the pulse width reported was measured from half-rail to half-rail (i.e., from half-V_{DD} of SE pulse onset to half-V_{DD} of SE pulse ending, Full-Width, Half-Rail - FWHR).

LETs in all simulations ranged from 5 - 40 MeV·cm^2/mg, with an ion-track radius of 50 nm and ion-strike length of 5 μm. The 3-D TCAD structures had dimensions of 20 μm × 20 μm × 5 μm. The 3-D TCAD mixed-mode simulation results (Figs. 15 and 16) show higher charge collection and longer pulse width for hits to the PMOS device than the hit to the matched-current-drive NMOS device. Parasitic bipolar amplification causes increased PMOS charge collection [Sun78], [Fu85], [Woo93], [Dod96], [Ols05], [Ibe06], [Amu06a]. A PMOS device in n-well with p-substrate produces more pronounced parasitic bipolar amplification for a bulk, twin-well CMOS process [Amu06a].

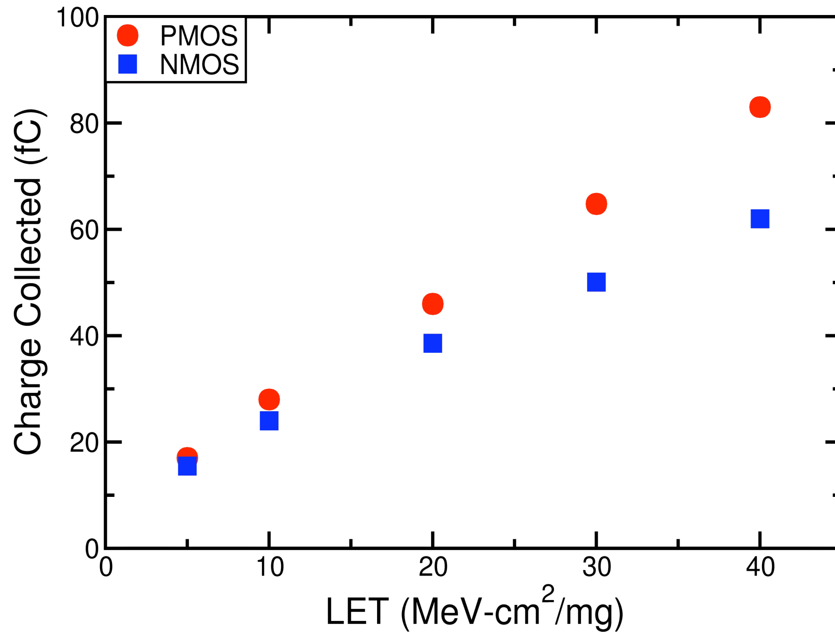


Fig. 15. Charge collected with varying LET in 90 nm NMOS and PMOS devices. Parasitic bipolar amplification causes a significant increase in charge collected with increasing LET for the PMOS device.

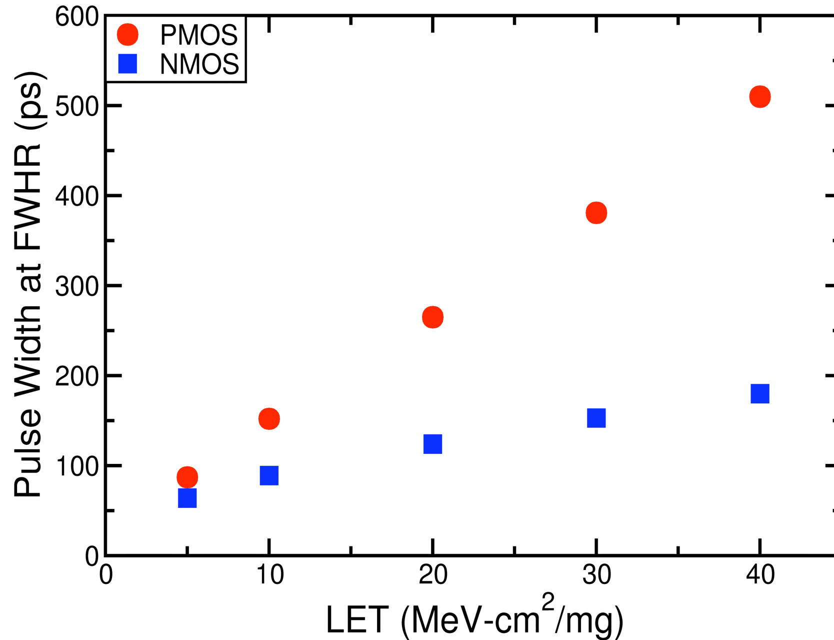


Fig. 16. FWHR voltage pulse widths at the output of the 5th stage of the inverter chain with varying LET for both 90 nm NMOS and PMOS devices.

Charge Collection Circuit

Laser experiments allowed further exploration of the parasitic bipolar amplification effect on PMOS devices. The laser experiment required development of an on-chip charge collection measurement circuit. Although existing charge-collection measurement techniques such as the Time-Resolved Ion Beam Induced Charge Collection (TRIBICC) [Bre07] have proven effective in measuring charge collection on individual devices, they may require considerable expense to implement and require large transistors for viable current measurements. In advanced technologies, the circuit and layout parameters at the hit node, such as restoring device characteristics [Das07b] and the presence of multiple devices within a certain distance, affects the collected charge [Amu06a]. Hence, charge-collection measurements must use devices of the relevant size contained within their intended circuit environment (e.g., active area, device spacing, and contact location). The

pico-second range timescale of the charge-collection process necessitates an on-chip measurement system. The on-chip measurement circuit must measure charge collected by the circuit node without affecting the circuit operation. The charge measurement circuit must also be able to perform the following: measure charge within a very short time, measure a wide range of collected charge, distinguish effects of parasitic bipolar transistors [Ols07], and measure the effects of charge sharing (i. e., charge collected from an ion hit slightly away from the device [Amu06a]).

The speed of operation matters most for the measurement circuit design. As the speed of the charge-collection process is of the same order as the switching speeds of the transistors, the measurement circuit must operate at high speeds. As most techniques cannot directly measure charge in the pico-second range, the described laser experiments required a novel measurement technique employing indirect measurement of the collected charge. The charge collected at a node directly relates to the voltage at that node, provided only capacitive loading occurs:

$$Q = C \times V$$

Where Q is the charge, C is the nodal capacitance and V is the nodal voltage. Changes in voltage also reflect any change in charge, assuming that capacitance does not change. The design of the test circuit employs this principle. *A priori* knowledge of the nodal capacitance at the hit node and the measured change in voltage across the capacitor allows estimation of the charge collected by the capacitor. This equation reduces the problem to measuring the capacitor voltage.

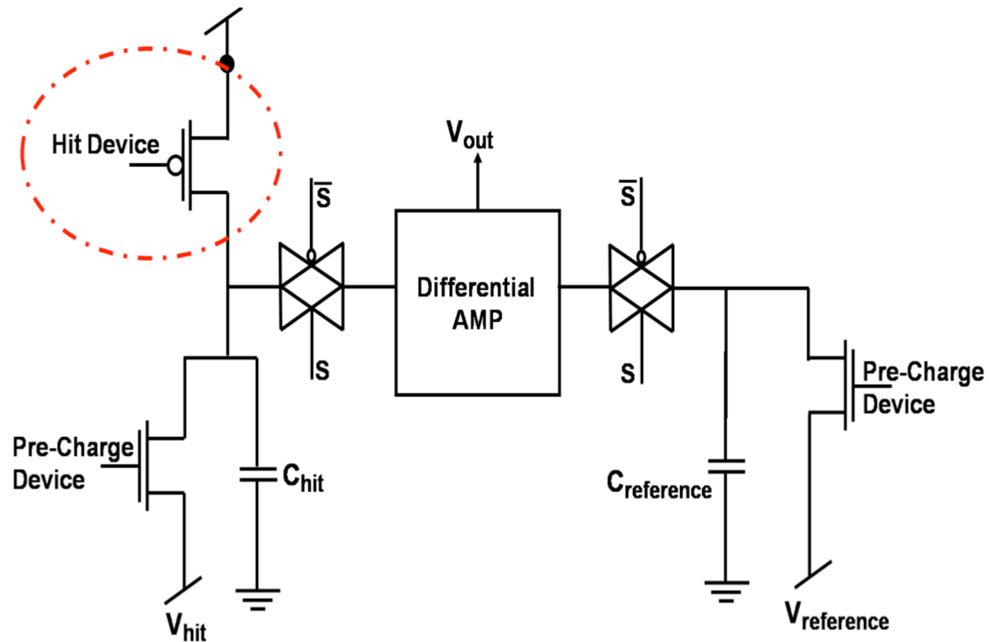


Fig. 17. Laser measurement circuit for the PMOS device determines the amount of charge collected.

The idea of the measurement circuit is similar to DRAM circuits which are essentially capacitor voltage measurement circuits. In DRAM circuits, the sense amplifier measures the voltage on the memory capacitor by comparing it to the voltage on the dummy capacitor. A similar technique to that of DRAM circuits involves using a dummy capacitor with known voltage to compare (and measure) the voltage on the hit node capacitor. Fig. 17 shows the basic test circuit based on this technique. After charging the capacitor associated with the hit device (C_{hit}) to a known voltage value, the capacitor and the hit device are disconnected from the rest of the circuit and a hit takes place at the hit node. The charge collected due to the hit alters the voltage across the capacitor C_{hit}. Following the closing of the pass gates connecting the hit node to the differential amplifiers, the capacitor voltage is compared to the reference voltage, $V_{reference}$. If the voltage on the hit capacitor exceeds the voltage on the reference capacitor, the differential

amplifier changes state. Measurement repeats with different reference voltages until determination of the exact value of the voltage on the hit capacitor. The difference in value of the voltage across C_{hit} yields the collected charge:

$$\Delta Q = C_{reference} \times \Delta V$$

The values of the capacitors C_{hit} and $C_{reference}$ must be decided so as to account for the range of the charge collected and the supply voltage used. C_{hit} and $C_{reference}$ must also include all parasitic capacitances for accurate measurements. Using a MOSFET-Capacitor (MOS-CAP) for C_{hit} and $C_{reference}$ improves representation of the voltage dependent nature of nodal capacitance values in real circuits. The MOS-CAP helps capture the nodal capacitances using an integrated average over possible voltage swings provided process and layout parameters are known. Uyemura [Uye99a] and Sze [Sze81] provide in-depth discussions of how to calculate the nodal capacitance of a MOS-CAP.

Bipolar Amplification Laser Experiment Details

Design and fabrication of the on-chip charge-collection measurement circuit employed the IBM 130 nm CMSF8RF bulk CMOS technology node. The twin-well bulk CMOS process used in this work has a p^+ deep well and a p^+ substrate. Two test structures with 500 fF capacitor size were designed for the parasitic bipolar study:

1. p^+ diode (p^+ active in n-well)
2. PMOS device

In the first case, a reverse-biased p^+ diode (Fig. 18), the charge collected yield data for a p-hit. Results from the PMOS device (Fig. 19) include effects of parasitic bipolar transistor [Sun78] on the charge collected at the hit node. As the laser strike measures

approximately 1 μm in diameter, each structure implemented a 1 μm^2 drain area (Figs. 18 and 19). The W/L for the PMOS device is 2.85 μm/ 0.12 μm. Figs. 18 and 19 show a simplified circuit (representative of the circled region in Fig. 17). For the PMOS transistor in Fig. 19, the red region represents the gate and the green regions represent the drain/source area. For the p^+ diode in Figs. 18, the green region represents the drain area.

The laser experiments were conducted at the Naval Research Laboratory. Two-Photon Absorption (TPA) allowed injection of laser-induced carriers through the wafer using high peak femto-second pulses at sub-bandgap optical wavelengths as demonstrated in [McM00], [McM02], [McM03]. Unlike other approaches, TPA interrogates SEE phenomena [Bal08] and circuit vulnerability [Lov07] through the wafer using backside irradiation [Bal08]; thereby eliminating the metallization layer stacks interference inherent in these technologies. All experiments were performed at room temperature.

Imaging of the Device Under Test (DUT) through the wafer, using Near-Infrared (NIR) imaging optics with an InGaAs focal plane array (Indigo Alpha NIR), permits determination of the center of the drain strike. Sweeping the laser across the sensitive node in an iterative fashion determines the center of the active area by measuring maximum charge collection. Both a strike at the center of the drain and another strike location 2 μm from the center of the drain device were examined (Figs. 18 and 19).

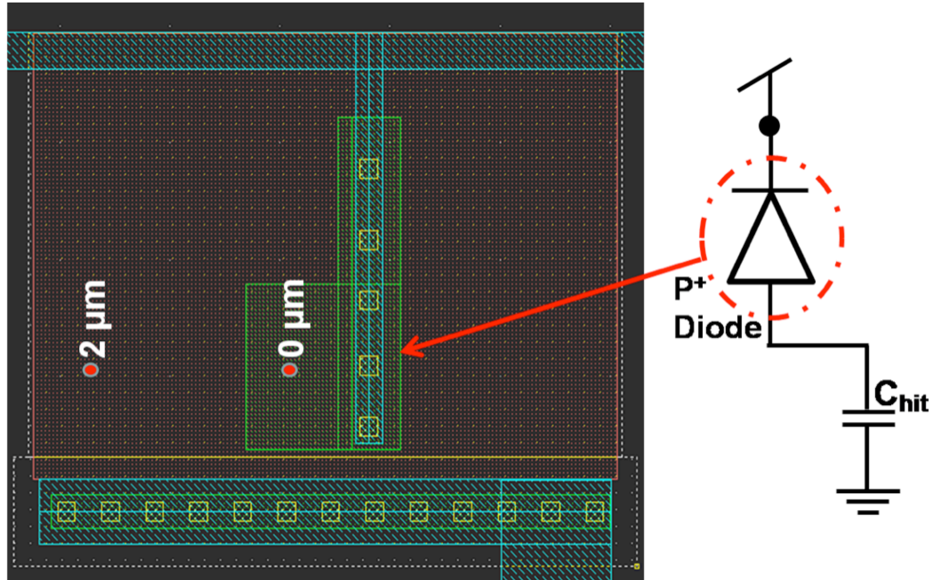


Fig. 18. Simplified p^+ diode circuit and diagram showing strike locations.

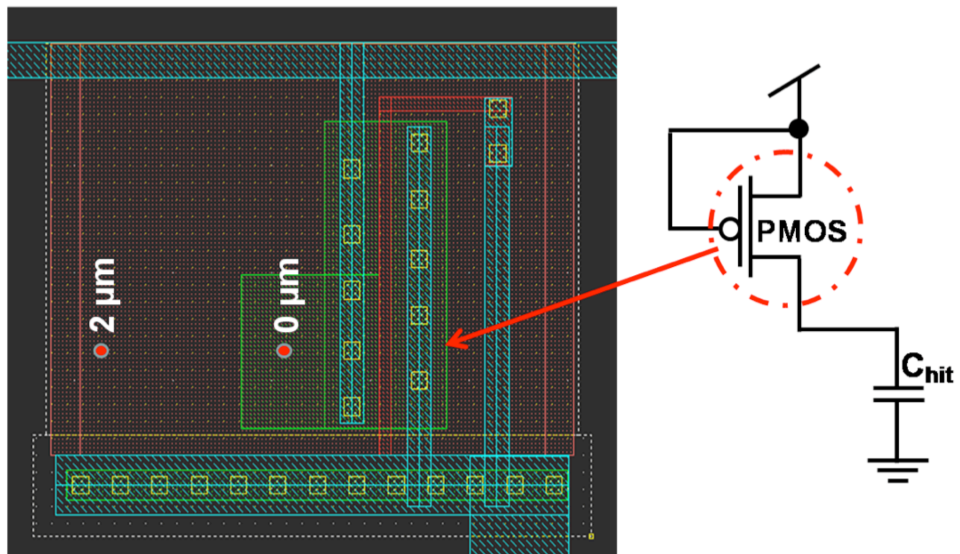


Fig. 19. Simplified PMOS circuit and layout diagram showing strike locations. Device width is 2.85 μm.

Bipolar Amplification Laser Experiment Results

Olson *et. al.* [Ols07] discusses the parasitic pnp bipolar transistor in detail. The parasitic pnp bipolar transistor amplification study compares the p^+ diode and PMOS device. The p^+ diode and the PMOS device differ only in the presence or absence of the gate and source (Fig. 20). This allows examination of the parasitic bipolar amplification effect which is due to the change in the n-well potential, which leads to a forward-biased source/body junction and possibly a parasitic pnp bipolar transistor turn-on [Amu06a], [Law06], [Sun78], [Fu85], [Woo93], [Ols07]. Comparing charge collected with the source (i.e., PMOS device) to without the source (i.e., p^+ diode) determines the effect of the parasitic pnp bipolar transistor on the charge collection process.

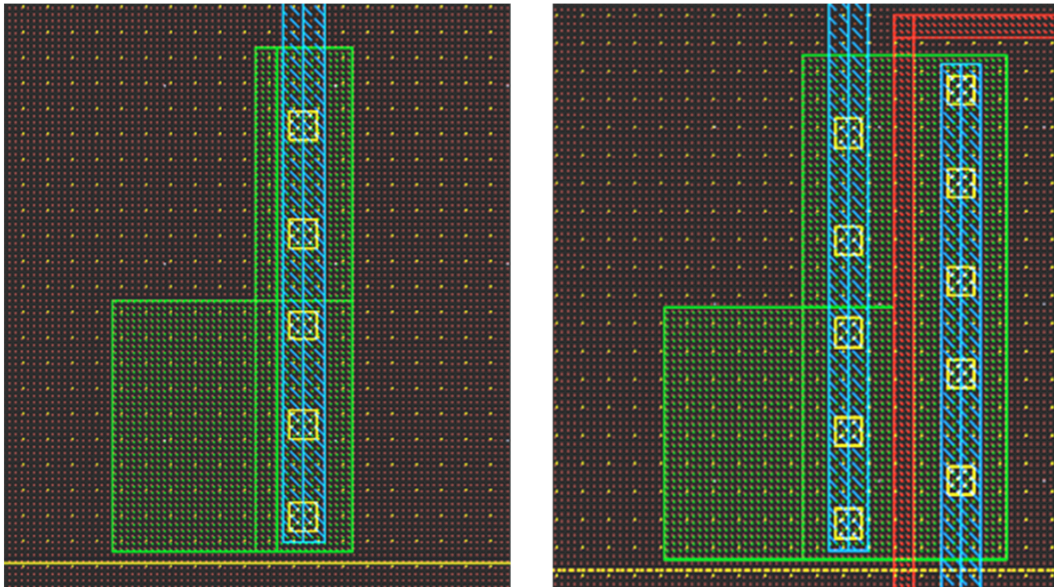


Fig. 20. p^+ diode layout (left) and PMOS device layout is (right). The PMOS device contains a source/gate, while the p^+ diode does not.

The p^+ diode/PMOS device results indicate a noticeable increase in charge collection for the PMOS device compared to the p^+ diode, attributable to parasitic bipolar amplification of SE related currents for the PMOS device (Fig. 21). Fig. 21 shows that the parasitic bipolar amplification depends on the strike location (i.e., 0 µm vs. 2 µm). Strikes on the drain (0 µm) yield greater parasitic bipolar amplification, while strikes farther away from the drain (2 µm) yield no parasitic bipolar effect

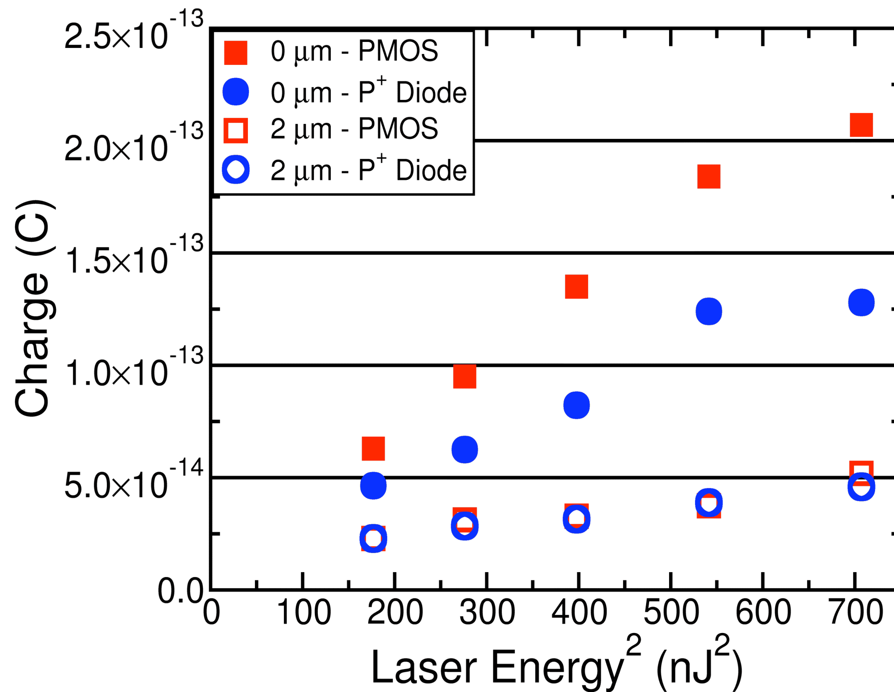


Fig. 21. PMOS device collects more charge than the p^+ diode for 0 µm hits; PMOS device and p^+ diode charge collection is comparable for 2 µm hits.

The main reason for this enhanced collection via parasitic amplification in the PMOS transistor is the collection of electrons in the n-well from deposited charge, which in turn reduces the n-well potential. The drop in n-well potential, along with additional carriers present in the substrate due to the hit, turns on the PMOS parasitic pnp bipolar transistor, resulting in higher charge collection and longer SET pulse widths. Conversely, the

absence of any regions for carrier confinement makes drift and diffusion currents from deposited charge in the p-well, not parasitic bipolar action, the dominant charge collection mechanism for the NMOS device [Amu06a].

As a result, the SET pulse widths for PMOS device hits exceed those from an NMOS device for high LET particles by more than 50% (Fig. 16). Thus, reducing the SET pulse widths from PMOS device hits significantly improves the SE performance of a circuit in reducing the overall error rate.

SE Pulse Width Reduction through Reduced Charge Collection

Parasitic bipolar amplification exacerbates p-hit pulse widths causing a difference in the p-hit pulse widths from the n-hits pulse widths, techniques to reduce the parasitic bipolar effects should result in shorter SET pulses for p-hits. The parasitic bipolar amplification depends on the collapse and the re-establishment of the electric field in the n-well [Ols07]. The ion-strike creates electrons collected by the n-well contact; this in turn leads to a reduction in the n-well electric field, resulting in a potential gradient in the n-well. This localized potential drop occurs in the channel regions of the PMOS transistor (Fig. 14) and forward biases the source-body junction leading to the parasitic bipolar transistor activation. Maintaining the n-well potential relatively constant throughout an SE hit mitigates the parasitic bipolar transistor effects.

N-well vertical resistance ($R_{vertical}$) and the resistance between the channel and n-well contact/contacts (R_{well}) determine the voltage drop in the n-well assuming the carrier density is below the doping level and thus greatly affect parasitic bipolar amplification (Fig. 22) [Ols07], [Sun78]. N-well contact area determines the resistance $R_{vertical}$; larger

n-well contacts yield lower $R_{vertical}$, requiring higher currents to turn on the parasitic bipolar transistor. R_{well} directly relates to the distance between the n-well contact and the transistor. Close spacing of the contact and device reduces the effect of the parasitic bipolar amplification.

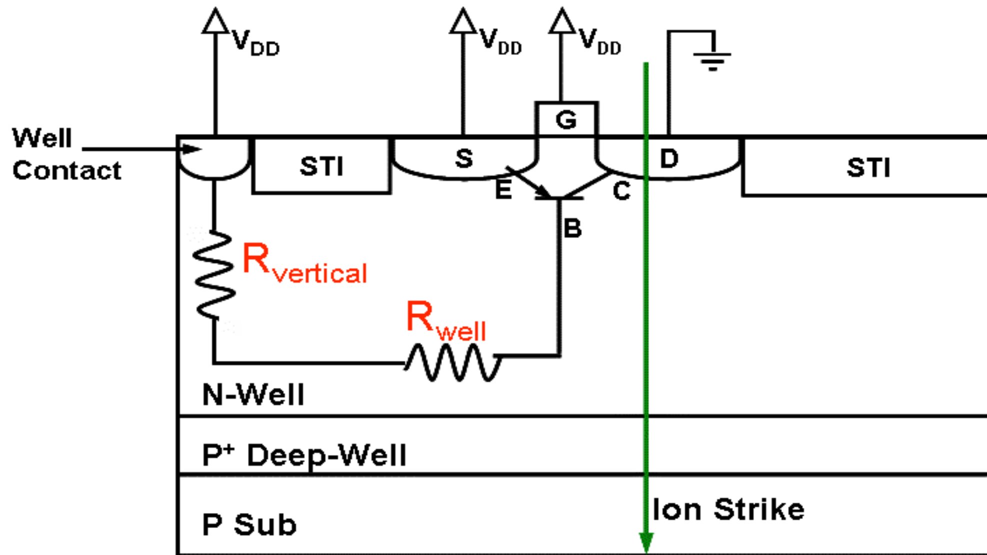


Fig. 22. Illustration of the vertical resistance ($R_{vertical}$) associated with the n-well contact area and the well resistance (R_{well}) associated with the n-well contact distance from the device.

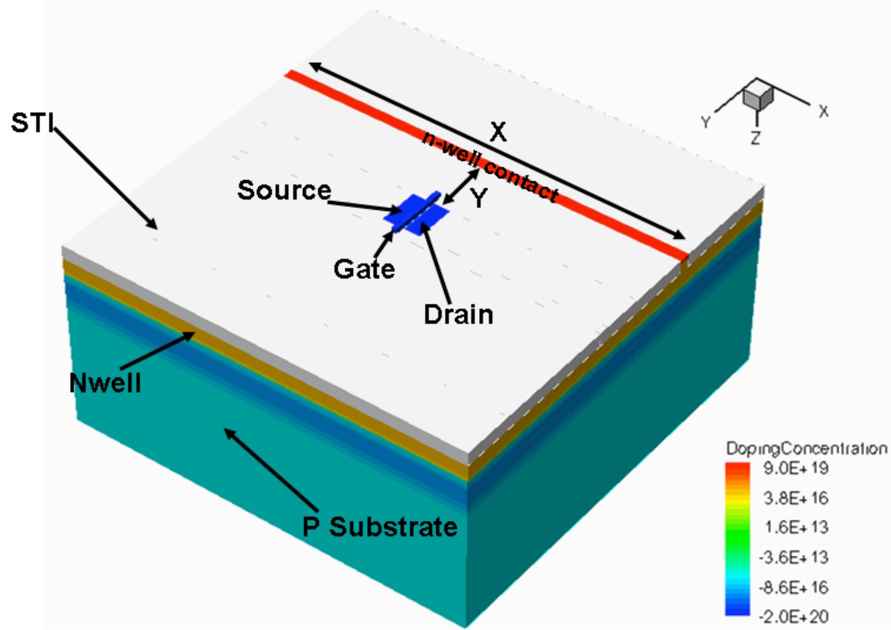


Fig. 23. 3-D TCAD PMOS device shows the variation of the n-well distance (i.e., R_{well}) and n-well contact area (i.e., $R_{vertical}$). *Y* represents the distance change of the drain to the well contact and is from 500 nm to 9 µm. *X* represents the area change from 200 nm × 200 nm to 200 nm × 10 µm.

N-Well Contact Distance (R_{well})

Varying distance from 300 nm to 9 µm (*Y* in Fig. 23) allowed examination of the effects of the distance between n-well contact and the PMOS device. The 5-stage minimum-sized matched-current-drive inverter chain included the 3-D TCAD PMOS structure in the 3rd stage. All simulations used a fixed n-well contact size of 200 nm × 10 µm and an LET of 40 MeV·cm²/mg. The simulation results in Fig. 24 show the effect of the contact distance *Y* on the generated pulse width. The reduction in the generated pulse width with reduced distance to n-well contact distance is due to the reduced R_{well}. The reduced R_{well} associated with the closely located n-well contact also helps reduce the potential collapse in the n-well. It should be noted that process design rules dictate the minimum spacing between the n-well contact and PMOS device.

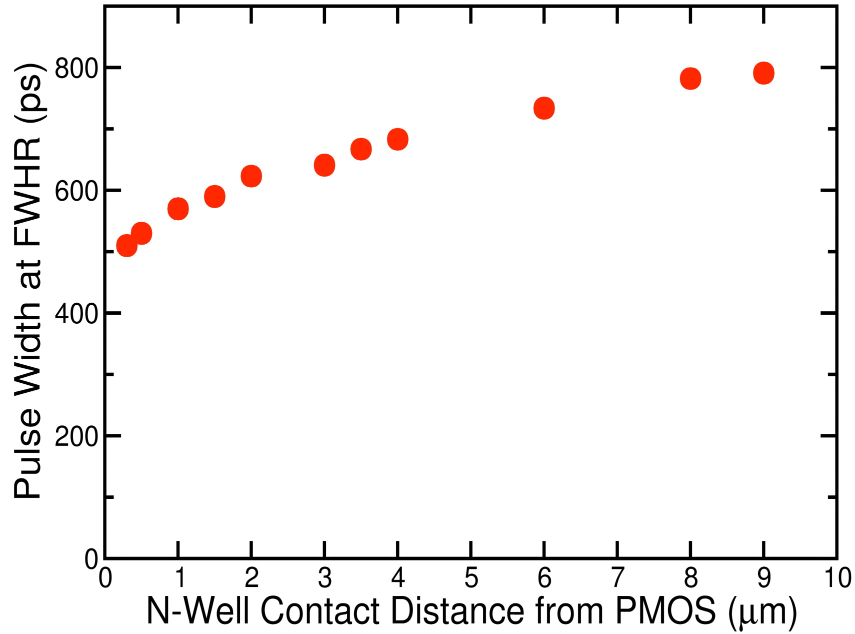


Fig. 24. FWHR voltage pulse widths for varying n-well contact distance (*Y* in Fig. 23) from 300 nm to 9 µm. The decrease in the PMOS pulse width (from 791 ps to 511 ps) with reduced contact distance is due to reduced R_{well}.

N-Well Contact Area ($R_{vertical}$)

Simulations for contact sizes ranging from 200 nm × 200 nm to 200 nm × 10 µm (*X* in Fig. 23) and LET of 40 MeV·cm^2/mg allowed investigation of the effects of the n-well contact area (i.e., $R_{vertical}$) on the generated pulse width. The n-well contact remained 300 nm away from the PMOS device for all simulations. The results illustrate the dependence of the pulse width on the n-well contact area (Fig. 25). The reduction in the pulse width is due to the reduced $R_{vertical}$. The increased contact area also helps mitigate the parasitic bipolar amplification effect by requiring greater potential drop in the n-well to activate the parasitic bipolar transistor and creating a larger collection area for the electrons generated from the ion strike, resulting in the reduced pulse width.

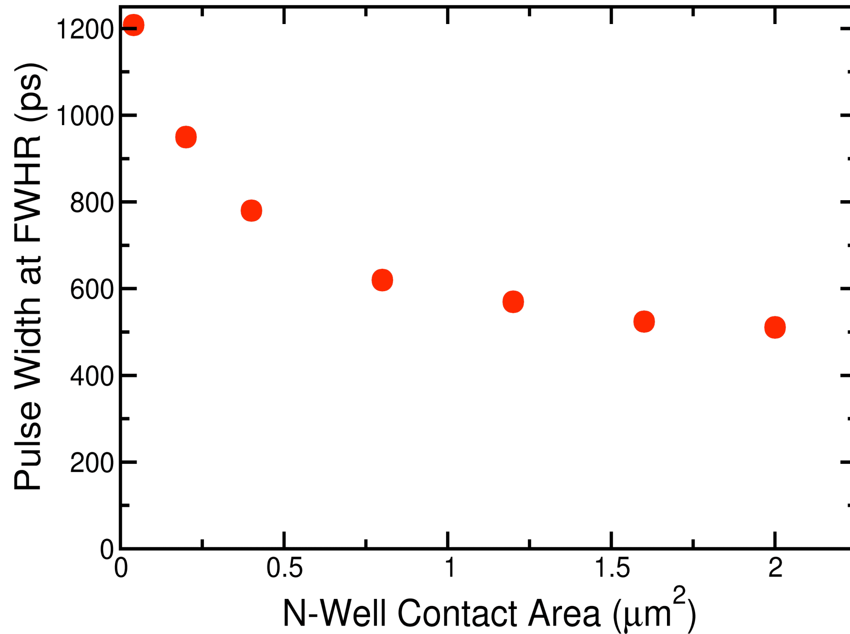


Fig. 25. FWHR voltage pulse widths for varying n-well contact area from 200 nm × 200 nm to 200 nm × 10 μm. The decrease in the PMOS pulse width (from 1208 ps to 511 ps) with increased contact area is due to reduced $R_{vertical}$.

To further investigate the effect of n-well contact area ($R_{vertical}$) on the parasitic bipolar turn-on, two simulations were conducted in which the n-well contact area ($R_{vertical}$) was kept at a constant area 200 nm × 1 μm at distance of 300 nm. The contact was placed parallel to the gate width and orthogonal to the gate width as shown in Figs. 26 and 27. For both the cases, the voltage pulses generated on the PMOS drain was equal demonstrating that the n-well contact area ($R_{vertical}$) is a main component of the parasitic bipolar turn-on. Thus, a combination of n-well area and contact distance can be used to mitigate the longer pulse widths generated in the PMOS devices.

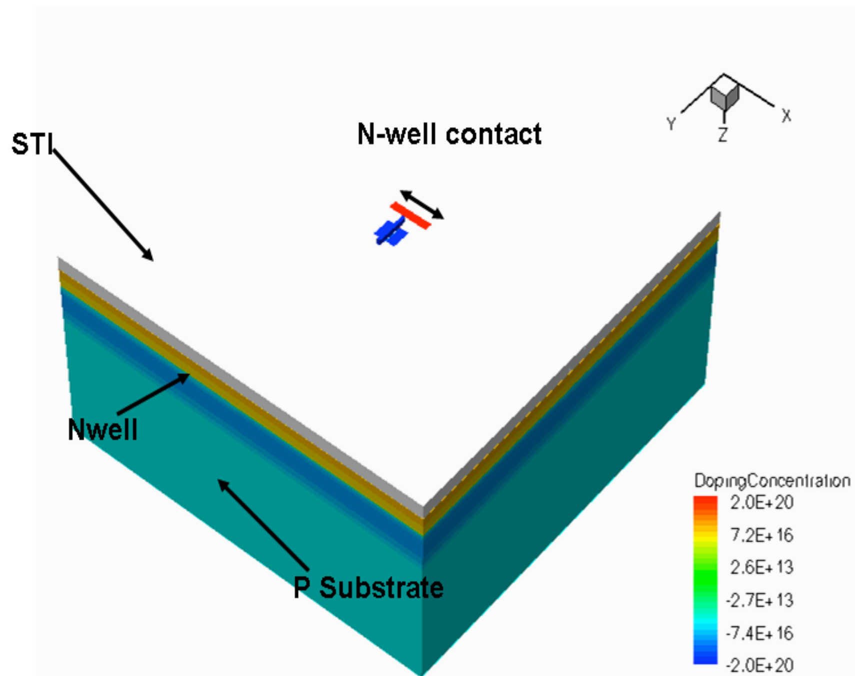


Fig. 26. N-well contact is 300 nm from the PMOS device; the n-well contact area is 200 nm × 1 µm.

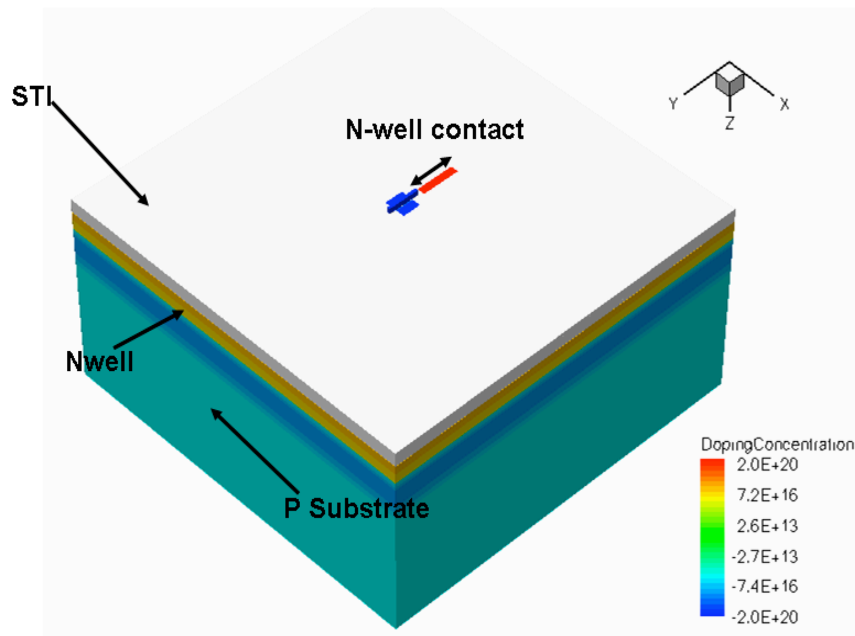


Fig. 27. N-well contact is 300 nm from the PMOS device; the n-well contact area is 1 µm × 200 nm.

SE Pulse Width Reduction through Increased Rate of Charge Removal

Increasing the rate of charge removal also reduces SET pulse widths. The current carrying capability of the restoring transistor determines the rate of charge removal [Buc01]. Increasing the size (i.e., transistor width) of the transistors associated with vulnerable nodes remains a popular technique for reducing pulse widths. However, increasing the transistor width also creates an area and power penalty. A better option is to only harden those nodes that are most vulnerable. Srinivasan *et al.* [Sri05] have proposed an algorithm for determining the vulnerability of each node and the contribution of each node towards overall vulnerability of a circuit. Increasing the width of the restoring transistors associated with the node decreases their vulnerability.

Assuming the type of hit transistor does not affect the amount of charge collected, approaches such as those of [Buc01], [Sri05], and [Zho04] increase the transistor sizes uniformly (i.e., current drive increases proportionally with both NMOS and PMOS widths , $I_{nsat} = I_{psat}$, also an increase in gate capacitance). A 2X uniform transistor width increase on the n-hit response is shown in Fig 28. The slightly reduced pulse widths is due to the increased rate of charge removal associated with the increased PMOS restoring current drive and is consistent with older technologies in which drift and diffusion account for charge collection mechanisms.

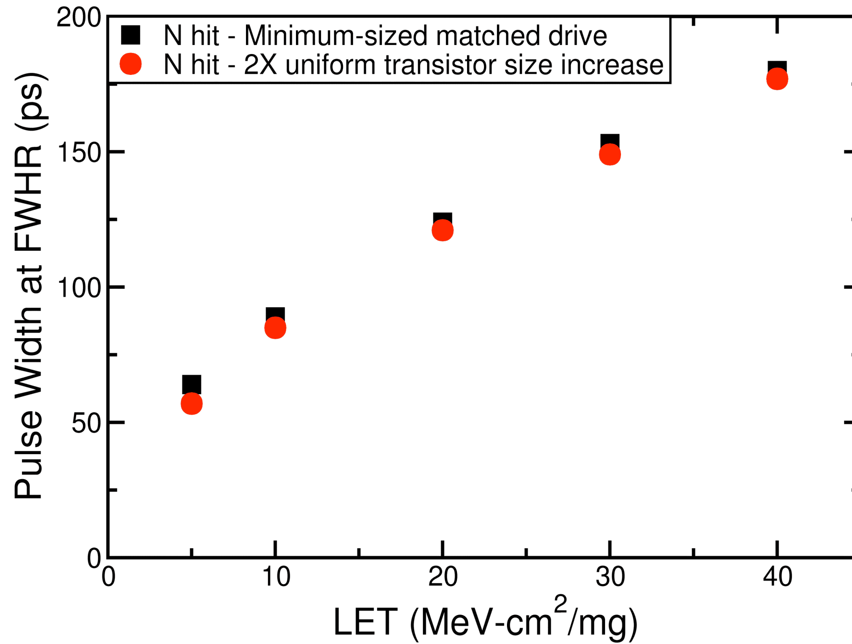


Fig. 28. FWHR voltage pulse widths for n-hit minimum sized matched drive vs. 2X uniform increase in transistor widths. Increased rate of charge removal with increased transistor widths causes a slight reduction in the voltage pulse width.

However, our results reveal that at the Sub-100 nm technology node examined, NMOS devices collect significantly less charge than PMOS devices due to parasitic bipolar amplification on the PMOS devices. As the n-hit results in shorter SET pulse width and PMOS devices provide the restoring current, the increase in size of the PMOS device need not mimic that for NMOS device. A uniform transistor width increase (i.e., both NMOS and PMOS widths increase by 2X and maintain matched current drive, $I_{nsat} = I_{psat}$) results in unnecessary increases in power dissipation and area requirements. Also, the 2X uniform transistor width increase of the PMOS device leads to an increase in the area associated with the parasitic bipolar transistor (i.e., emitter of the pnp transistor) and thus charge collection, thereby increasing the SET pulse width (Fig. 29). This p-hit pulse width increase requires an increase in the pre-determined threshold pulse width

associated with implementing temporal pulse width filtering, adversely affecting temporal techniques.

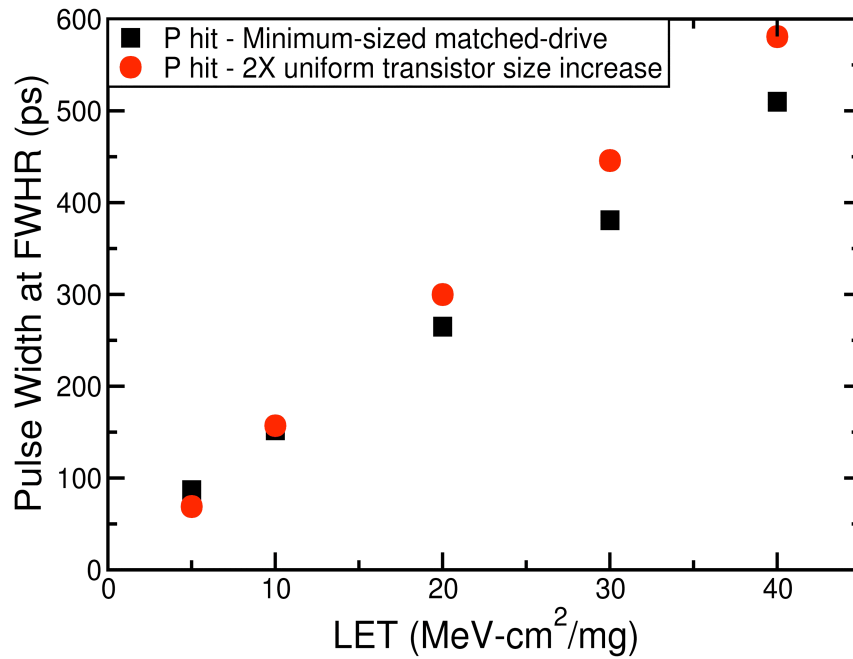


Fig. 29. FWHR voltage pulse widths for p-hit minimum sized matched drive vs. 2X uniform transistor width increase. Increasing the current drive does not improve SE pulse widths because increasing PMOS width increases parasitic bipolar amplification.

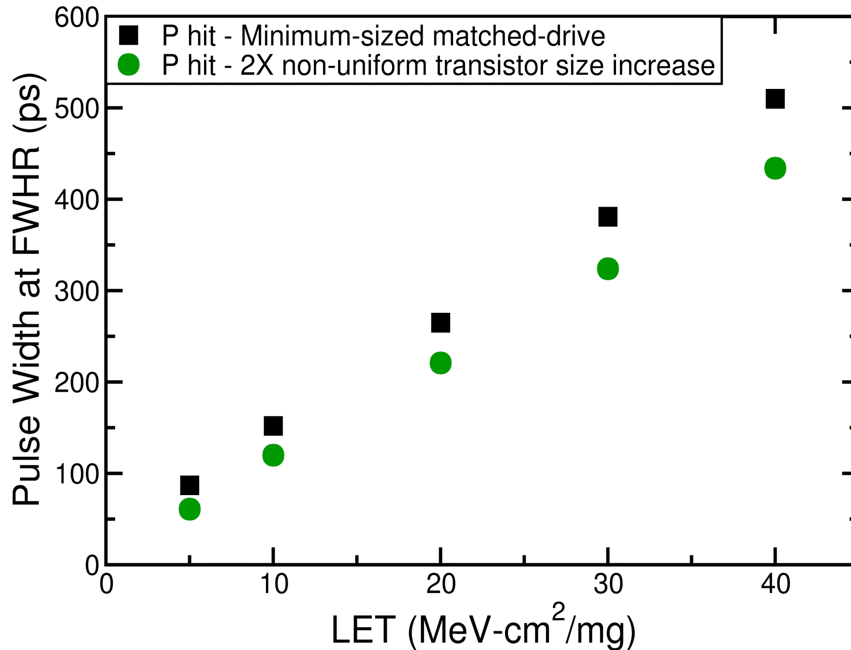


Fig. 30. FWHR voltage pulse widths for p-hit minimum sized matched drive vs. 2X non-uniform transistor width increase. Increasing the current drive improves SE pulse-widths because this approach keeps the PMOS transistor size at a minimum, thereby minimizing parasitic bipolar amplification.

Using the SET pulse width difference between n-hit and p-hit allows better transistor sizing. A non-uniform transistor increase, in which the NMOS transistor width is increased by 2X and the PMOS width is kept at the minimum size (i.e., $I_{nsat} > I_{psat}$), helps reduce the p-hit pulse width by 30% in comparison to a uniform transistor increase (Fig. 30). The non-uniform transistor increase reduces p-hit pulse width by 15% compared to minimum transistor sizing. Increased NMOS restoring current drive associated with the p-hit node and the resulting increased rate of charge removal causes this reduced pulse width, while keeping the parasitic bipolar transistor area at a minimum.

This improved and optimized transistor sizing approach creates a decreased SET pulse width for the longest pulses, thereby helping reduce the pre-determined threshold pulse width required for temporal filtering techniques. This does adversely affect rise

time and fall time for an individual logic gate, making them non-uniform, but over a chain of logic gates, the ratioless design of CMOS logic gates minimizes this difference [Wes94]. Also, the non-uniform 2X increase causes a negligible shift (i.e., 30 mV decrease) in the midpoint voltage [Uye99b]; hence, the non-uniform 2X increase has no significant effect on Noise Margin. Non-uniform sizing also creates an area and power advantage over a uniform increase in transistor sizing (Table 1). The results in Table 1 were obtained using a commercial 90 nm bulk CMOS process for a 5-stage inverter chain. The layout was designed with regard for all design rules. The speed penalties were minimal for both hardening approaches.

Table 1: Percentage change with respect to a 5-Stage-Inverter-Chain (minimum sized, matched-current-drive) using a commercial 90 nm process. All design rules followed, speed penalties minimal for both hardening approaches.

	Area	Power	SET Pulse Width
2X uniform transistor width increase	+23.7%	+100%	+15%
2X Non-uniform transistor width increase	+12.6%	+30.5%	-15%

Conclusions

Analysis of single device 90 nm CMOS SET response quantifies the interaction between charge collection and charge redistribution in a matched-current-drive inverter chain. The varying charge collection mechanism affects the total amount of charge collected for p-hit and n-hit. The potential change in the n-well and the resulting parasitic bipolar amplification on the PMOS device cause the charge collection and SET pulse width differences between n-hits and p-hits. Laser testing confirms the parasitic bipolar

amplification effect in PMOS devices. Hence, p-hits are more damaging for temporal filtering techniques than n-hits, and p-hit mechanisms must be mitigated.

Either reducing total collected charge or increasing the charge removal rate from the hit node allows reduction of SET pulse widths. RHBD approaches for increasing n-well contact area (reduced $R_{vertical}$) and decreasing distance between n-well contact and devices (reduced R_{well}) reduce SET pulse widths by mitigating parasitic bipolar transistors and are quantified here for a commercial 90 nm technology. Unequal SET pulse widths for n- and p-hits also allow non-uniform transistor size increases for quicker charge removal from the hit node, resulting in improved SET response, area, power, and speed trade-offs.

This chapter has focused solely on the effects of an ion-strike on a single device and discussed the difference in the charge collection process and resulting SE transients for NMOS and PMOS devices. The next chapter delves into the effects of charge collection by multiple devices from a single ion-strike. The difference in charge sharing mechanisms for NMOS and PMOS devices is based on the difference in the charge collection mechanisms discussed in this chapter.

CHAPTER IV

DIRECTIONAL SENSITIVITY OF SINGLE EVENT UPSETS IN 90 NM CMOS DUE TO CHARGE SHARING

Introduction

This chapter discusses charge sharing (i.e., multiple node charge collection from a single ion-strike) in detail, provides the first experimental data verifying the charge sharing effect, and examines the difference in charge sharing for a normal and angled hit. The simulation results were verified through heavy-ion experiments and show the significance of considering charge sharing effects during SEE circuit characterization.

When a SE hit results in charge collection at only one node for larger CMOS technologies, conventional RHBD approaches, such as DICE latch shown in Fig. 31 [Cal96], TMR [Pet80], or temporal latch [Mav00], provide excellent protection against SEUs. With decreasing technology feature size, the close proximity of devices can result in charge collection at multiple nodes due to a single incident ion (i.e., charge sharing [Amu06a], [Ols05], [Vel96], [Ben05], [Bla05]). For example, at 130 nm technology, a DICE latch was shown to be susceptible to ions at low LET values as shown in Fig. 32 [Baz06] due to charge collection at multiple nodes from a single hit [Amu07], [Mas06].

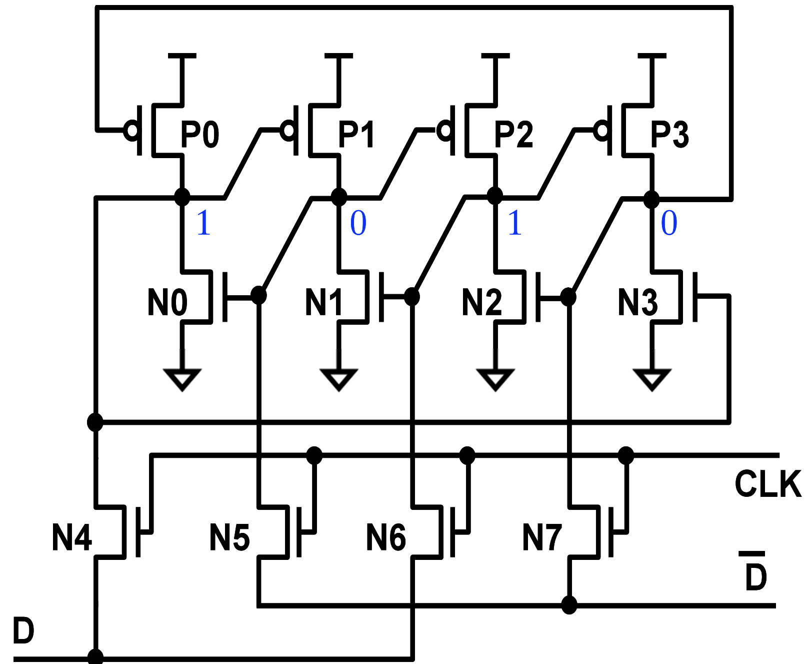


Fig. 31. DICE Latch circuit: interlocked design and use of redundant information storage makes it hardened to single node charge collection upsets [Cal96]. Charge sharing between transistors can upset the DICE [Vel96], [Baz06], [Mas06].

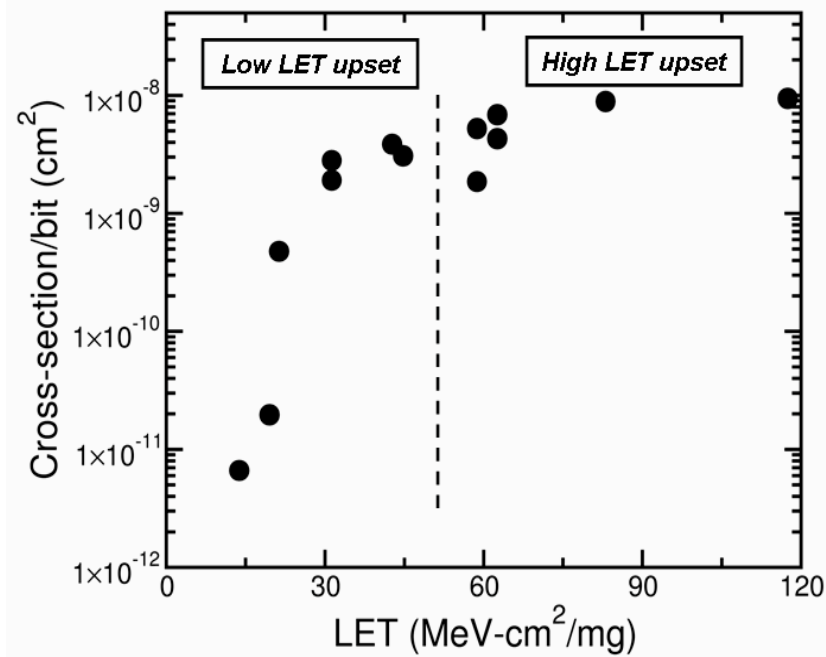


Fig. 32. Experimental heavy-ion data showing the upset cross-section for a DICE latch in a commercial 130 nm technology [Baz06]. Low LET upsets are due to charge sharing [Amu07], [Mas06].

Charge sharing is a major SE issue for deep-submicron technologies due to reduced nodal charge, higher packing densities, and reduced spacing between devices [Amu06a]. Due to the mechanisms (e.g., drift, diffusion, and parasitic bipolar amplification of SE related currents [Dod03]) involved in charge collection, angular SE strikes result in exacerbated charge sharing effects as compared to normal incidence SE strikes for advanced technologies as shown in this chapter. Hence, directional dependence of charge sharing should be taken into consideration during SEE circuit characterization.

This chapter also presents heavy-ion test data measured on a RHBD latch fabricated in a 90 nm bulk CMOS process showing a high degree of directional sensitivity in the SE response. A DICE latch design is considered immune to charge collection on a single node, and the SE vulnerability of DICE topologies due to charge sharing has been investigated previously [Amu07]. However, when a 90 nm RHBD Integrated Circuit (IC) was exposed to angular strikes with various orientations relative to the layout channels, we found an SE error cross-section variability of two orders of magnitude.

Previous work done in the studying the charge sharing effect was done through indirect summation. This chapter presents the first laser test data directly verifying the charge sharing effect in a Sub-100 nm bulk CMOS process. The laser data shows the effect of nodal spacing on charge sharing and dependence of charge sharing on charge deposition.

In this chapter, Spice and 3-D TCAD simulations were used to explain the mechanisms responsible for this directional dependence. Charge sharing on multiple devices and n-well potential collapse leading to parasitic bipolar effects were found to heavily influence the SE response of the RHBD design.

The heavy-ion results demonstrate the importance of considering the impact of multiple devices, including physical proximity in all directions of circuit layouts in determining the SE response of advanced CMOS technologies. Such effects have significant implications for SEE circuit testing and for calculation of error rates in advanced CMOS circuits.

Charge Sharing Laser Experiment Details

Previous work on the DICE latch deduced through indirect methods that charge sharing effect was the cause for unexpected upsets. The goal in this dissertation was to verify, through direct measurement, the charge sharing effect. The on-chip charge collection measurement circuit discussed in Chapter III was used for the charge sharing verification experiment. The on-chip charge collection was modified for NMOS charge collection as shown in Fig. 33 and the variation for NMOS charge sharing collection is shown in Fig. 34. It should be noted that the active NMOS device (i.e., hit NMOS device) is the same in both circuits and has a 500 fF capacitor connected to the drain. For the charge sharing measurement, the passive NMOS device has a 100 fF capacitor connected to the drain. Design and fabrication of the on-chip charge-collection measurement circuits employed the IBM 90 nm CMS9FLP bulk CMOS technology node. Three test structures were designed for the charge sharing verification:

1. NMOS device – measures charge collection for the active NMOS device
2. Passive Device, 0.14 µm – measures the charge collection for passive NMOS device located 140 nm from the active NMOS device

3. Passive Device, 0.70 μm – measures the charge collection for passive NMOS device located 700 nm from the active NMOS device

As the laser strike measures approximately 1 μm in diameter, each structure implemented a 1 μm^2 drain area for the active NMOS device (Figs. 35, 36 and 37). The W/L for the NMOS active and passive devices is 1 μm/ 0.1 μm. Fig. 35 shows a simplified circuit (representative of the circled region in Fig. 33) and Figs. 36 and 37 show simplified circuits (representative of the circled region in Fig. 34). For all NMOS transistors, the red region represents the gate and the green regions represent the drain/source area.

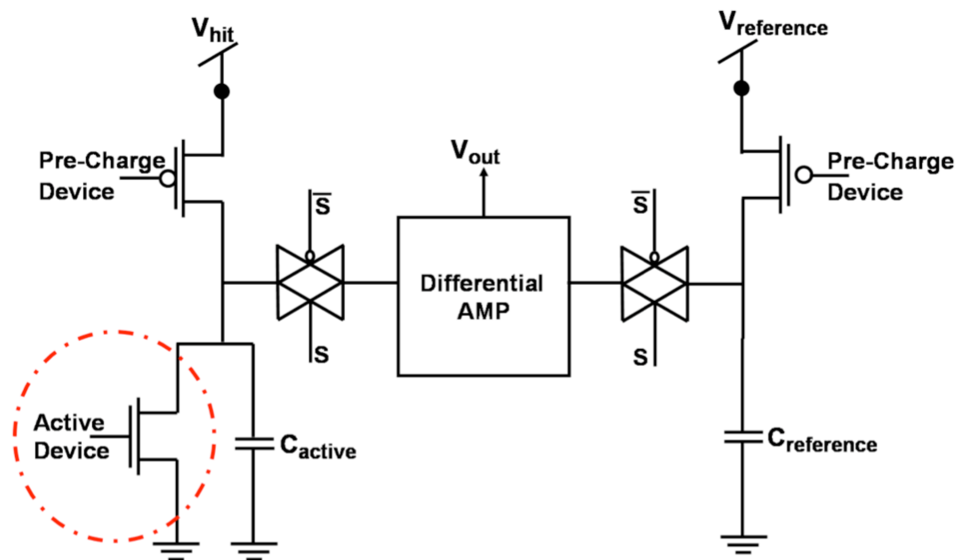


Fig. 33. Laser measurement circuit for the active NMOS device to determine the amount of charge collected.

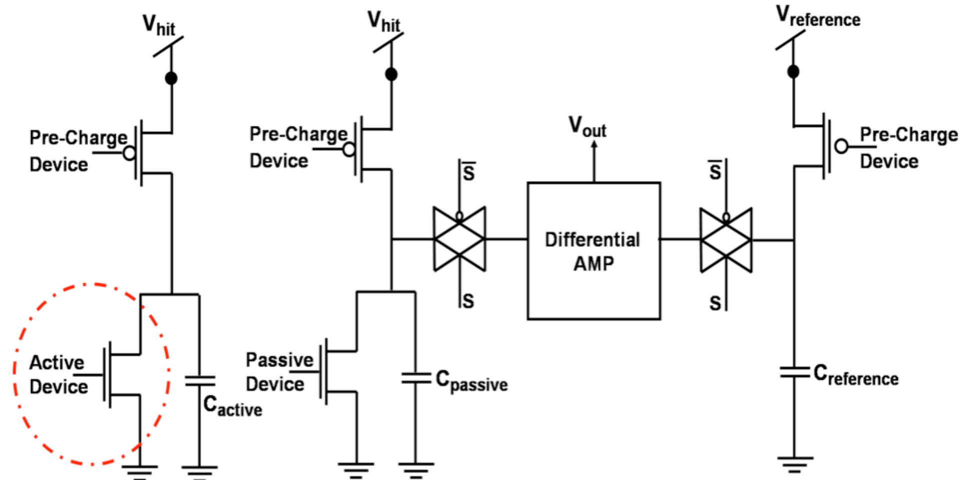


Fig. 34. Laser measurement circuit for NMOS charge sharing, this circuit determines the amount of charge collected on passive NMOS device for strikes on the active NMOS device.

The laser experiments were conducted at the Naval Research Laboratory. Two-Photon Absorption (TPA) allowed injection of laser-induced carriers through the wafer using high peak femto-second pulses at sub-bandgap optical wavelengths as demonstrated in [McM00], [McM02], [McM03]. Unlike other approaches, TPA interrogates SEE phenomena [Bal08] and circuit vulnerability [Lov07] through the wafer using backside irradiation [Bal08]; thereby eliminating the metallization layer stacks interference inherent in these technologies. All experiments were performed at room temperature.

Imaging of the DUT through the wafer, using Near-Infrared (NIR) imaging optics with an InGaAs focal plane array (Indigo Alpha NIR) permits determination of the center of the drain strike. Sweeping the laser across the sensitive node in an iterative fashion determines the centers of the active NMOS drain area and the laser strike was at the center of the drain for the three different setups (Figs. 35, 36, and 37).

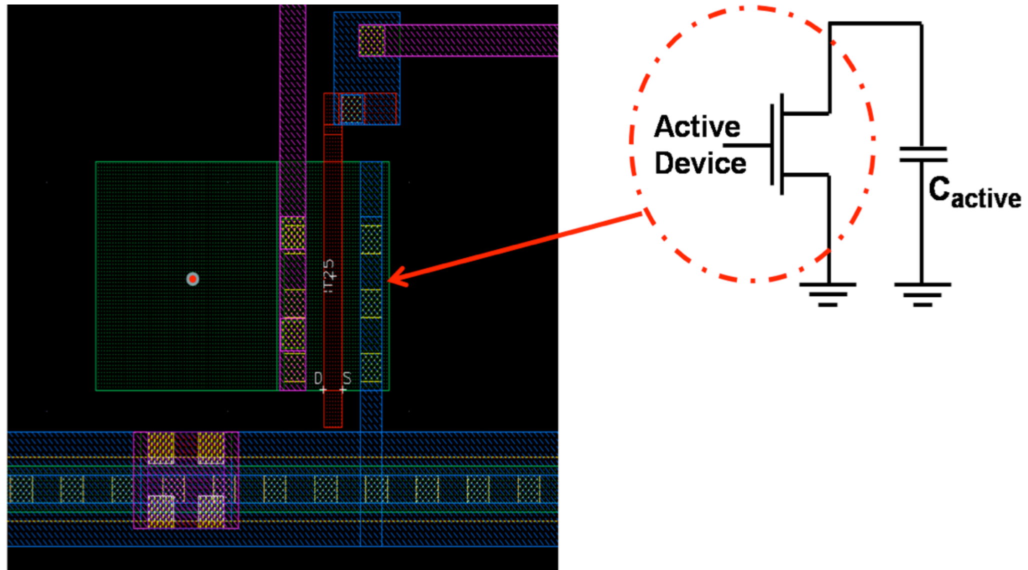


Fig. 35. Simplified active NMOS circuit and diagram showing strike location.

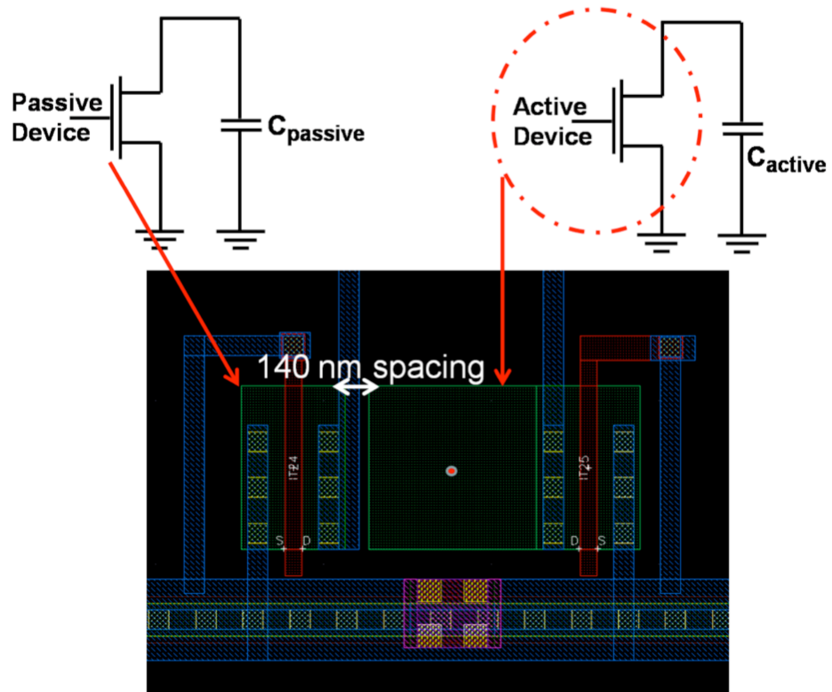


Fig. 36. Simplified passive NMOS circuit and layout diagram showing strike location. This layout is for the 140 nm spacing between the active and passive NMOS devices.

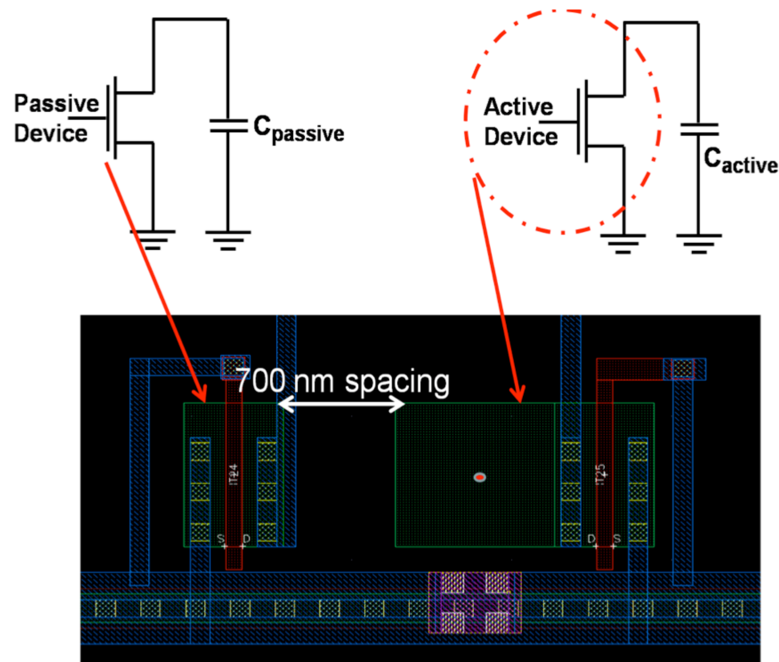


Fig. 37. Simplified passive NMOS circuit and layout diagram showing strike location. This layout is for the 700 nm spacing between the active and passive NMOS devices.

Charge Sharing Laser Experiment Results

The amount of charge collected for the active NMOS and passive NMOS devices is shown in Fig. 38. The result in Fig. 38 shows an increase in active NMOS charge collection with increasing laser energy and helps confirm the functionality of the on-chip charge collection circuit. This result also shows charge collection on the active and passive NMOS devices with increased laser energy. The result in Fig. 39 is a zoomed in view of Fig. 38 and focuses on the passive NMOS devices. Fig. 39 provides the first experimental verification of charge sharing in Sub-100 nm technologies. Fig. 39 also shows the dependence of charge sharing on the location of the passive device. The closely located passive NMOS device (i.e., located 140 nm from the active NMOS device) collects more charge compared to the further located passive NMOS device (i.e., located 700 nm from the active NMOS device). The result also shows the dependence of

charge sharing on laser energy, as an increase in laser energy increases the charge sharing effect. The nodal spacing dependence shown in this result will be explored in the next chapter as a charge sharing mitigation technique.

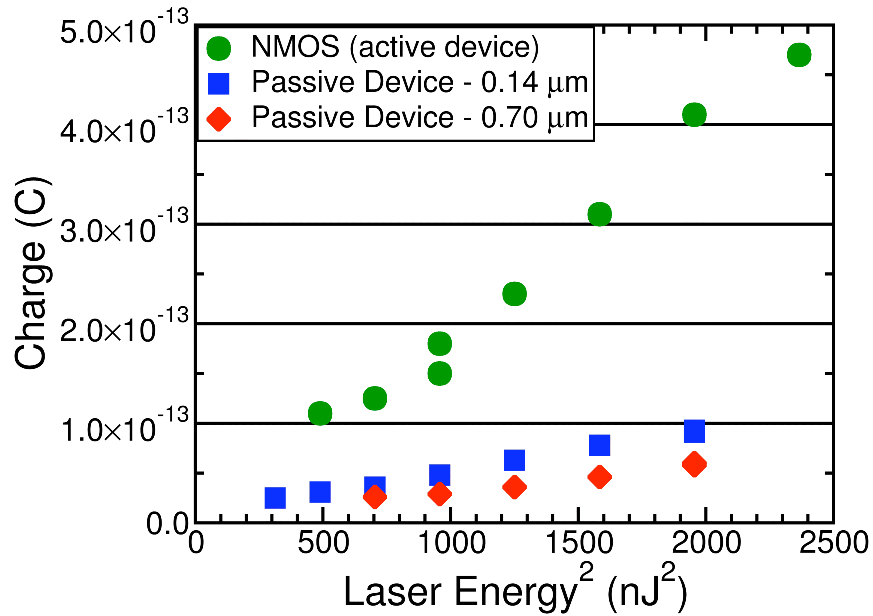


Fig. 38. Active NMOS device shows a charge collection trend dependent on the laser energy and confirms the functionality of the circuit. This result also shows the charge collection comparison for the active and passive NMOS devices.

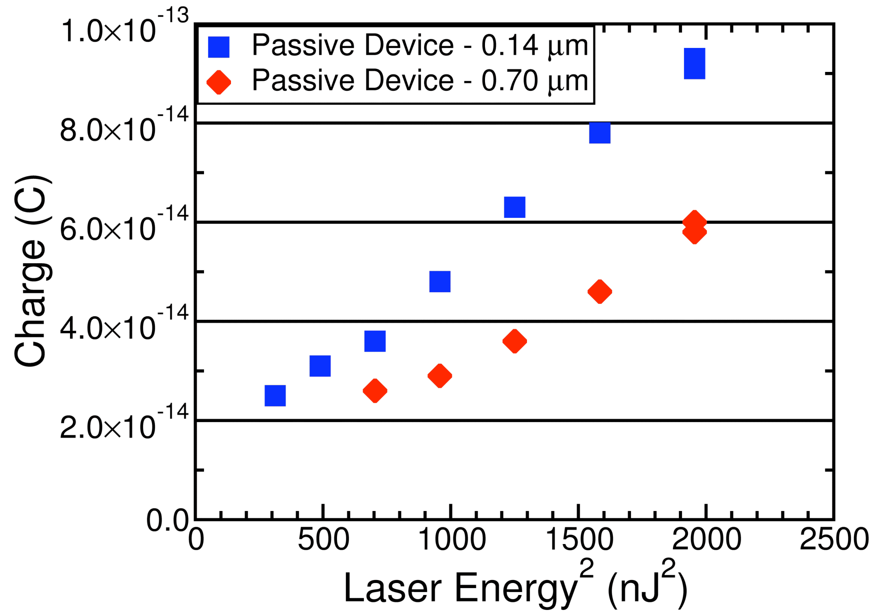


Fig. 39. Laser results for passive NMOS devices helps verify the charge sharing effect and show a nodal spacing dependence for the passive device charge collection.

3-D TCAD Simulation of Normal vs. Angled Hits

The first set of simulations aimed to examine the difference in charge sharing for normal and angled hits. The simulations were conducted for both NMOS and PMOS pairs with the struck device defined as the *active* device and the adjacent device in proximity defined as the *passive* device. The charge sharing devices were implemented in 3-D TCAD with the rest of the circuit in 90 nm compact models. The devices were calibrated to match the AC and DC characteristics of a commercial 90 nm bulk CMOS process [Das07a]. Both active and passive devices were simulated in the OFF state and each device was included in matched current drive inverter chains. The size of NMOS active and passive devices were 200 nm / 90 nm whereas PMOS active and passive devices were 480 nm / 90 nm with a nodal separation of 140 nm between the devices. The ion-strikes were simulated at two angles, a normal hit (0°) and a 60° angled hit

towards the passive device as shown in Fig. 40. The center of the drain of the active device was the struck node and charge collected results were reported after saturation occurred on both active and passive drains nodes in all simulations.

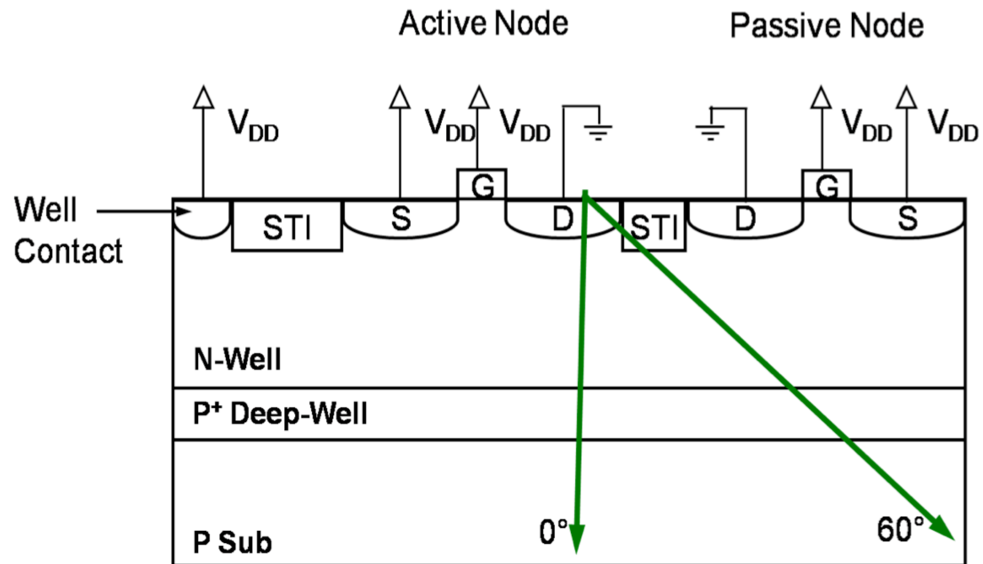


Fig. 40. Illustration of normal (0°) and angled (60°) hits for the PMOS charge sharing setup.

Fig. 41 shows there is a significant increase in the passive device charge collection for the 60° angled hit. The ion track traversing directly underneath the passive NMOS device increases the charge collection due to charge diffusion, resulting in the increase in charge collection on the passive NMOS device.

Fig. 42 shows a similar trend. There is a significant increase in charge collection on the passive PMOS device for the angled hit (60°) in comparison to the normal (0°) hit. The ion-track traversing underneath the passive PMOS device triggers the parasitic bipolar amplification on the passive PMOS device, causing the increase.

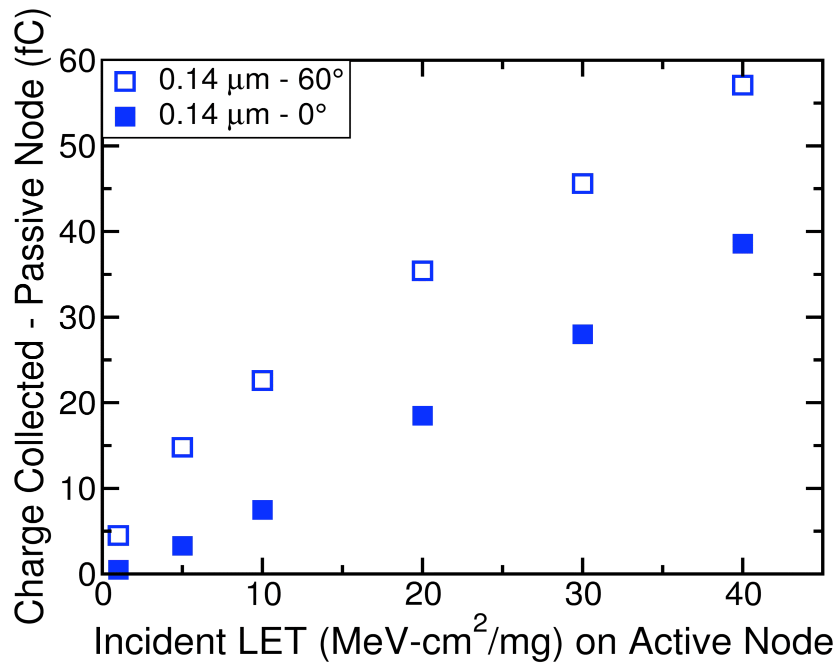


Fig. 41. Passive NMOS device charge collection for normal (0°) and angled (60°) hit.

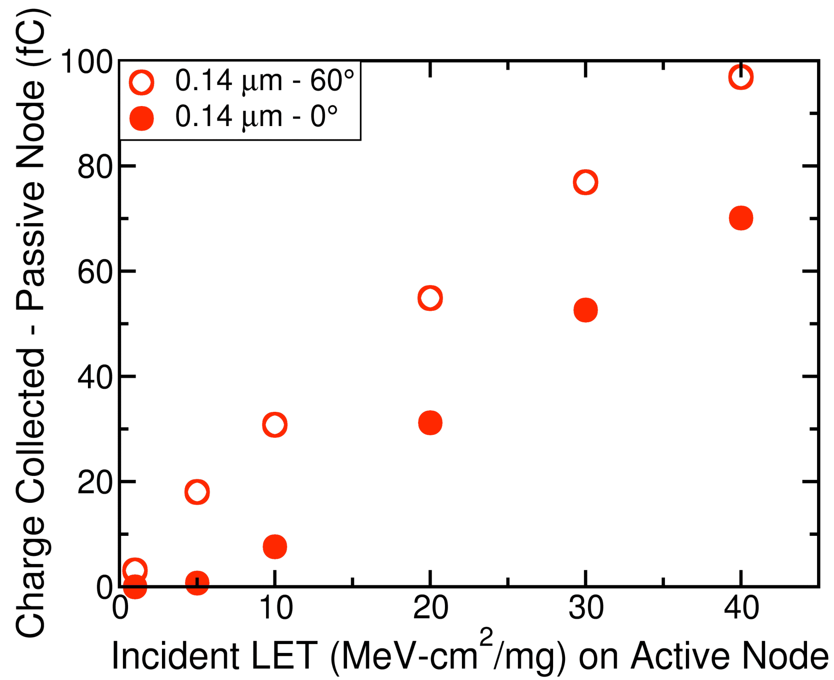


Fig. 42. Passive PMOS device charge collection for normal (0°) and angled (60°) hit.

Directional Dependence Heavy-Ion Experiment Details

The characterization of directional dependence was carried out on a test chip fabricated in a commercial 90 nm bulk CMOS technology, containing an array of DICE latches (Fig. 43) in a shift register arrangement. Multiple shift registers were placed in parallel to isolate clock hits from individual node hits in the DICE shift register (clock line hits result in upsets for all shift registers, individual hits result in upsets in a single shift register). Heavy-ion experiments were conducted at the Lawrence Berkeley National Laboratory. The ions used were argon, copper, xenon, neon, oxygen, boron and krypton with LET ranging from 3.45 to 62.6 MeV·cm^2/mg. The angles used for exposure were 0° and 60° from normal. The directional vector of the angled incident ions (i.e., 60°) was varied from *orthogonal* to the power rail (i.e., *North-to-South*) to *parallel* to the power rail (i.e., *West-to-East*). Therefore the roll, as opposed to the normal tilt, of the test fixture was varied. Multiple input data patterns were used for each ion exposure

Heavy-Ion Results for Normal and Angled Hits

The normal incidence exposure (0° incidence) data in Fig. 44 shows results comparable to previously presented data (Fig. 32 after [Baze06]). The upset cross-section shows vulnerability at low LET particles for DICE latch due to charge sharing [Amu07], [Mas06]. The dependence on input pattern is easily explained by the different set of vulnerable transistors or sensitive pairs prone to charge sharing with varying inputs as discussed in [Amu07]. Sensitive pairs are defined as two transistors that cause the DICE latch to upset upon simultaneous charge collection.

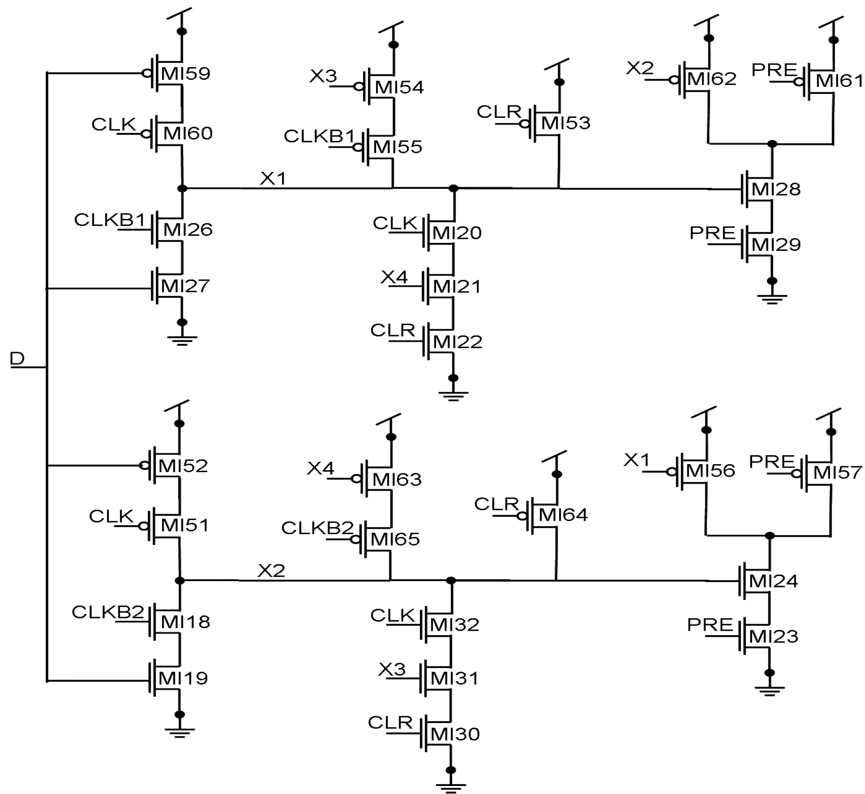


Fig. 43. Master stage of NAND-based DICE Cell.

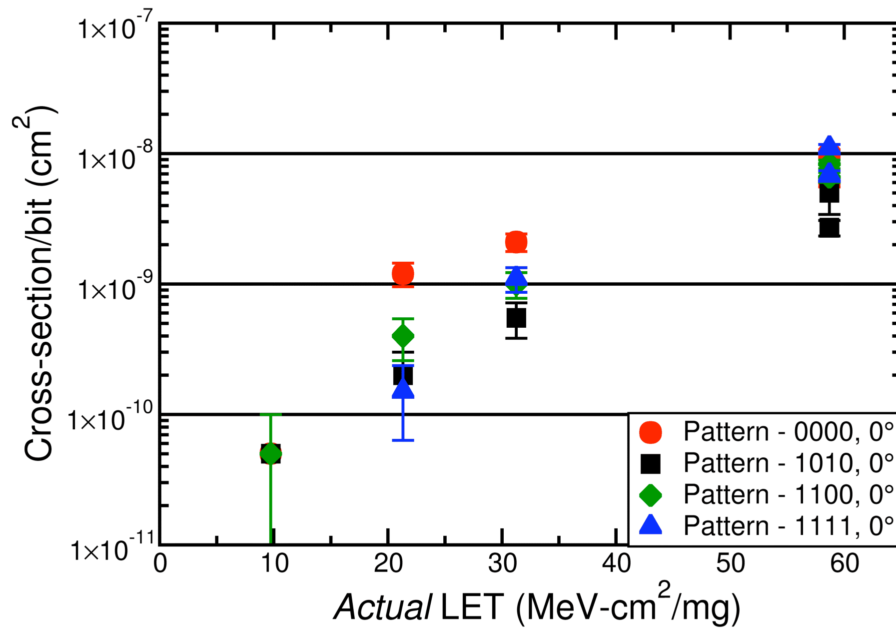


Fig. 44. Normal (0°) hit with varying input patterns for 90 nm DICE latch.

The angled (60°) hits were incident on the IC from different directions with respect to the actual layout of the transistors as shown in Fig. 45. The *North-to-South* (*N-S*) vectors traverse *orthogonal* to the power rails, and the *West-to-East* (*W-E*) vectors traverse *parallel* to the power rails, where the n-well and p-well contacts represent the power rails. Fig. 46 shows a significant directional dependency for angular strikes. The LET used in the figure is the *actual* incident LET - due to the directional dependence seen in the angular strikes. The results show that the DICE latches are more sensitive to W-E angular single-event strikes compared to the Normal and N-S SE strikes. The W-E data shows 2 distinct differences in comparison to the Normal and N-S SE strikes, (1) two orders of magnitude increase in cross-section and (2) decrease in LET threshold, whereas the N-S data shows a cross-section and LET threshold comparable to a Normal hit. The two data point for N-S SE strikes at LET of 10 MeV·cm^2/mg do show an order of magnitude difference. This difference can be attributed to testing statistics (i.e., low error counts, error counts of 2 and 9) during heavy-ion testing. These heavy-ion results clearly show the effect of directionality on angular SEE circuit characterization and the possible underestimation in LET threshold and cross-section that could occur as a result of untested directionality.

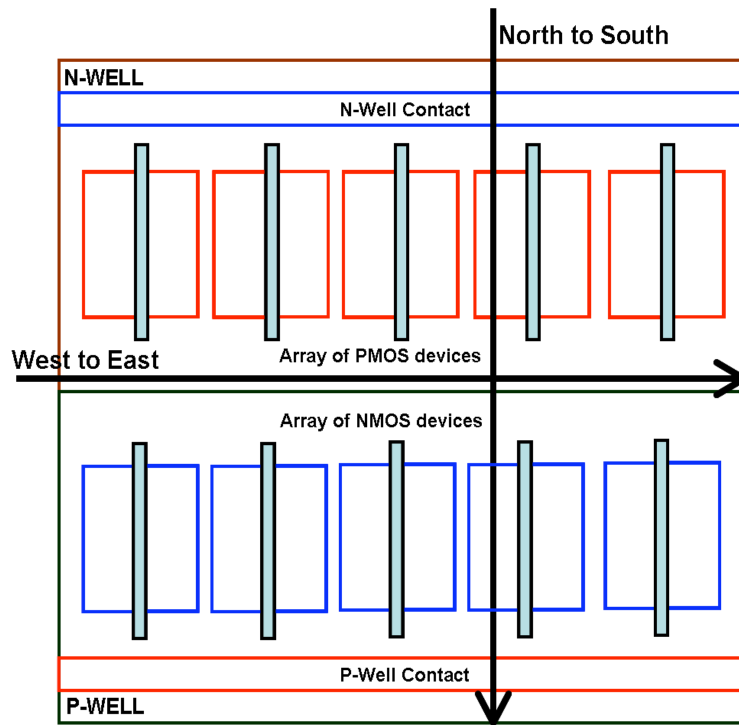


Fig. 45. *North-to-South* (*N-S*) vectors traverse *orthogonal* to power rails, *West-to-East* (*W-E*) vectors traverse *parallel* to the power rails.

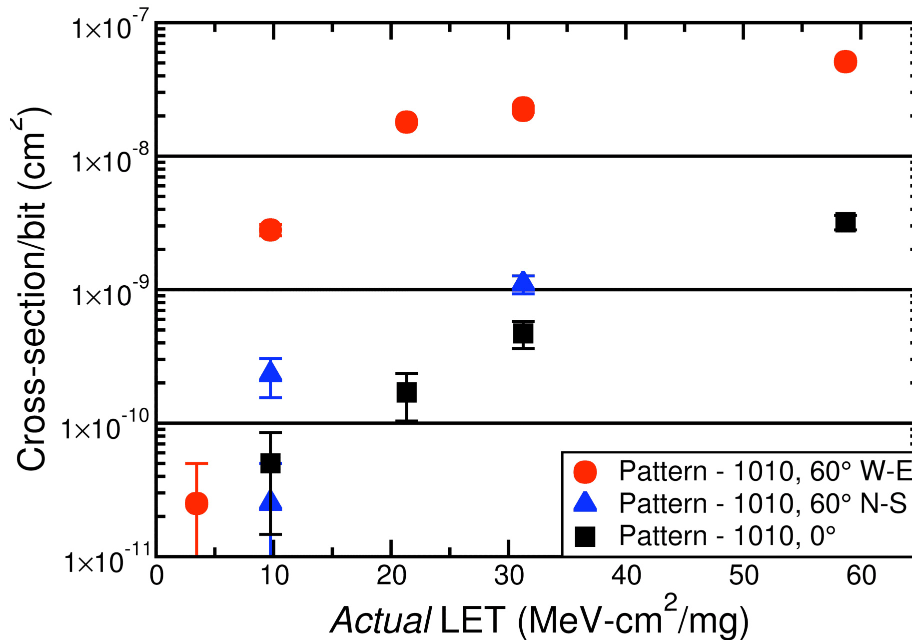


Fig. 46. Normal versus directional angled hits for 90 nm DICE latch. Directionality dependency is seen in the two orders of magnitude increase in cross-section and decrease in LET threshold for W-E angled strikes.

Spice and 3-D Mixed-Mode TCAD Analysis

It has been shown that charge sharing is more prevalent for transistors in the same well [Amu07], [Amu06a], [Ols05] than across well boundaries and as discussed in the previous chapter, there is a significant parasitic bipolar PNP turn-on in PMOS transistor [Ols07] for deep-submicron twin-well bulk CMOS processes. Therefore, the following discussion focuses on PMOS devices, but similar analysis can be carried out for NMOS devices.

SPICE analyses were carried out to identify upset-sensitive pairs of PMOS devices in the Boeing DICE latch, from which pairs in close physical proximity were determined from the layout. Using SE current pulses extracted from 3-D TCAD mixed-mode simulations, an exhaustive set of SE multiple-node-hit circuit simulations was used to generate SHMOO plots as shown in Fig. 47; where the *active* device is the hit node, and the *passive* device is the adjacent device in close proximity. The SHMOO plot in Fig. 47 is for the identified sensitive pair used in the LET threshold 3-D TCAD simulation, as discussed below. The charge contour in Fig. 47 shows an upset region with the amount of charge required on each transistor to cause an upset in the DICE latch. Similar contours were obtained for all sensitive pairs for the circuit.

LET threshold

The decrease in LET threshold for W-E strikes vs. Normal and N-S strikes (Fig. 46) implies an upset mechanism present only for W-E directionality. DICE latch upset at low LET requires charge collection by multiple devices, indicating the presence of adjacent sensitive pairs which collect enough charge for upsets only for W-E strike. Our simulations show this is the case, where two sensitive transistors, contained within a

single n-well, are proximal along the W-E direction as shown in Fig. 48(a). The nodal separation between PMOS A and PMOS B is 0.2 μm. The active and passive PMOS devices were calibrated to match the electrical characteristics of the transistors fabricated in a commercial 90 nm CMOS technology. The simulations were conducted in a mixed-mode environment with the charge sharing devices in 3-D TCAD and the DICE sub-circuit in the 90 nm compact models. The bias conditions of these transistors were identical to those for the actual DICE design (i.e., simulated PMOS transistors are in the OFF state – required for upset to occur). An n-well contact stripe was placed above the transistors as shown in Fig. 48 to match the Boeing DICE latch layout.

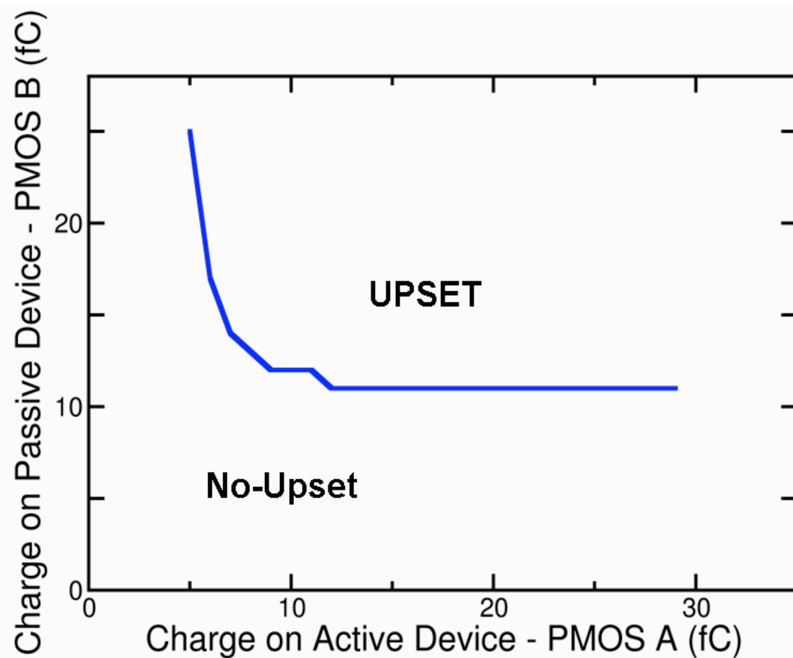


Fig. 47. Upset/No-Upset SHMOO plot for sensitive PMOS A - PMOS B pair quantifies the charge sharing necessary for upset.

For simulations, three different angles for ion strikes were used: normal incidence (0°), 60° incidence from N-S, and 60° incidence from W-E. A LET of 3.45 MeV·cm^2/mg was used in the LET threshold simulations. The LET was selected based on the decrease in LET threshold for W-E strikes vs. Normal and N-S strikes (Fig. 46). Ion strikes were incident on and around the drain area of PMOS A as shown in Fig. 48(a). The cross-section views in Fig. 48(b) and 48(c) show the simulated trajectories of the incident ion with respect to the 3-D TCAD devices.

Table 2 shows the simulation results for the charge collected at the drain node of each of the transistors for normal and angled hits. The hit device (PMOS A) shows a significant amount of charge collection regardless of the hit location or the angle orientation. Charge collection for PMOS B is strongly dependent on the orientation of the hit. The charge collected for normal and N-S strikes are comparable and will not result in an upset. However the W-E strike creates an ion-track that is located directly underneath PMOS B as illustrated in Fig. 48(c) and this leads to charge sharing and significant charge collection. The charge collection on PMOS A and PMOS B for W-E strike presented in Table 2 results in an upset of the DICE latch as indicated in the SHMOO plot of Fig. 47. Hence, the W-E strike results are representative of the reduced LET threshold seen in the heavy-ion data.

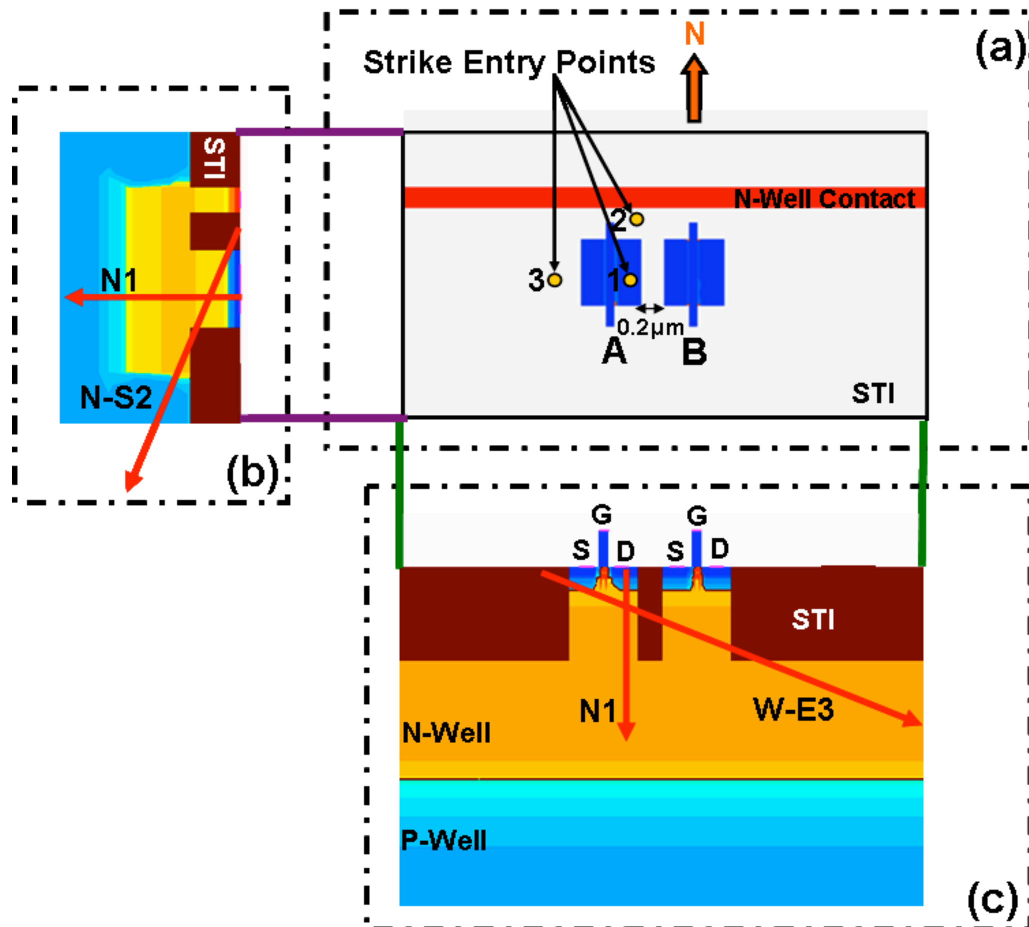


Fig. 48. Strike locations and directionality of the ion-strikes for LET threshold 3-D TCAD structure. 1, 2, and 3 in (a) represent the exact point of incidence for the ion. Letters preceding 1, 2, or 3 indicate whether the hit was Normal (N), North-to-South (N-S), or West-to-East (W-E). (b) and (c) show the trajectory of the ion on cross-section views.

Table 2: Charge Collected (fC) for Normal and Angled Hits on PMOS devices for LET threshold Study.

	N1	N-S2	W-E3
PMOS A	17	21	18
PMOS B	4	1	15

Cross-section

The observed cross-section for W-E strikes is increased as compared to Normal and N-S strikes (Fig. 46). This implies an increase in a sensitive area corresponding to the W-E directionality. This indicates the presence of sensitive pairs that cause an upset only for W-E strike and not for Normal or N-S strikes. Our circuit simulations show two sensitive transistors, contained within a single n-well, proximal along the W-E direction. From the list of such sensitive pairs, two sensitive transistors - which are separated by other, interleaved transistors (i.e., interleaved transistors are transistors present between the two sensitive transistors in the circuit layout but they do not contribute to an upset in the DICE latch) - were selected for simulation. Using the SHMOO plot in Fig. 49, the identified sensitive pair can be used in the cross-section 3-D simulation discussed below. The charge contour in Fig. 49 shows an upset region with the amount of charge required on each transistor to cause an upset in the DICE latch.

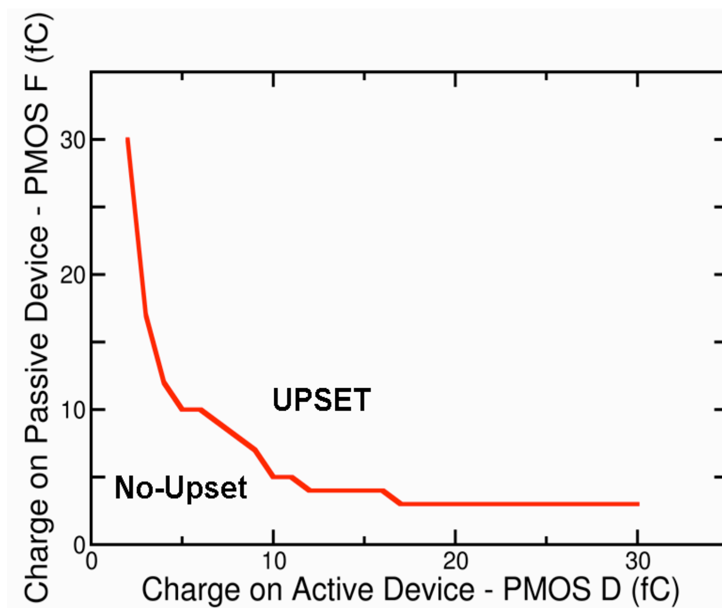


Fig. 49. Upset/No-Upset SHMOO plot for sensitive PMOS D - PMOS F pair quantifies the charge sharing necessary for upset.

The 3-D TCAD simulations were conducted in a mixed-mode environment with the charge sharing devices in 3-D TCAD and the DICE sub-circuit in 90 nm compact models. The bias conditions of these transistors were identical to those for the actual DICE design (i.e., simulated PMOS transistors are in the OFF state – required for upset to occur). Fig. 50 (a), (b), and (c) shows the hit locations and directionality of the ion-strikes. The nodal separation between PMOS D and PMOS F is 1.43 µm. An n-well contact stripe was placed above the transistors as shown.

For simulations, three different ion strike angles were used: normal incidence (0°), 60° incidence from N-S, and 60° incidence from W-E. A LET of 21 MeV·cm^2/mg was used in the cross-section simulations. The LET was selected based on the variability in cross-section for W-E strikes vs. Normal and N-S strikes (Fig. 46). Ion strikes were incident on and around the drain area of PMOS D as shown in Fig. 50(a). The cross-section views in Fig. 50(b) and 50(c) show the simulated trajectories of the incident ion with respect to the 3-D TCAD devices. It should be noted that the sensitive pair in this case are PMOS D and PMOS F, PMOS E represents a transistor present between PMOS D and PMOS F on the layout. PMOS E does not affect the upset mechanism after a strike.

Table 3 shows the simulation results for the charge collected at the drain node of each of the transistors for normal and angled hits. The angled hits show a strong dependence on the orientation (i.e., W-E versus N-S). The hit device (PMOS D) shows a significant amount of charge collection regardless of the hit location or the angle orientation. However, it should be noted that there is a difference between the amount of charge

collected for hits on and near the drain due the effects of the ion-track location and parasitic bipolar turn on.

Charge collection for PMOS E is significant across the different strike locations, although the significant difference between the amounts of charge collected for N-S hit versus W-E hit is notable. However, any charge collected by PMOS E does not affect the upset mechanism for the DICE latch.

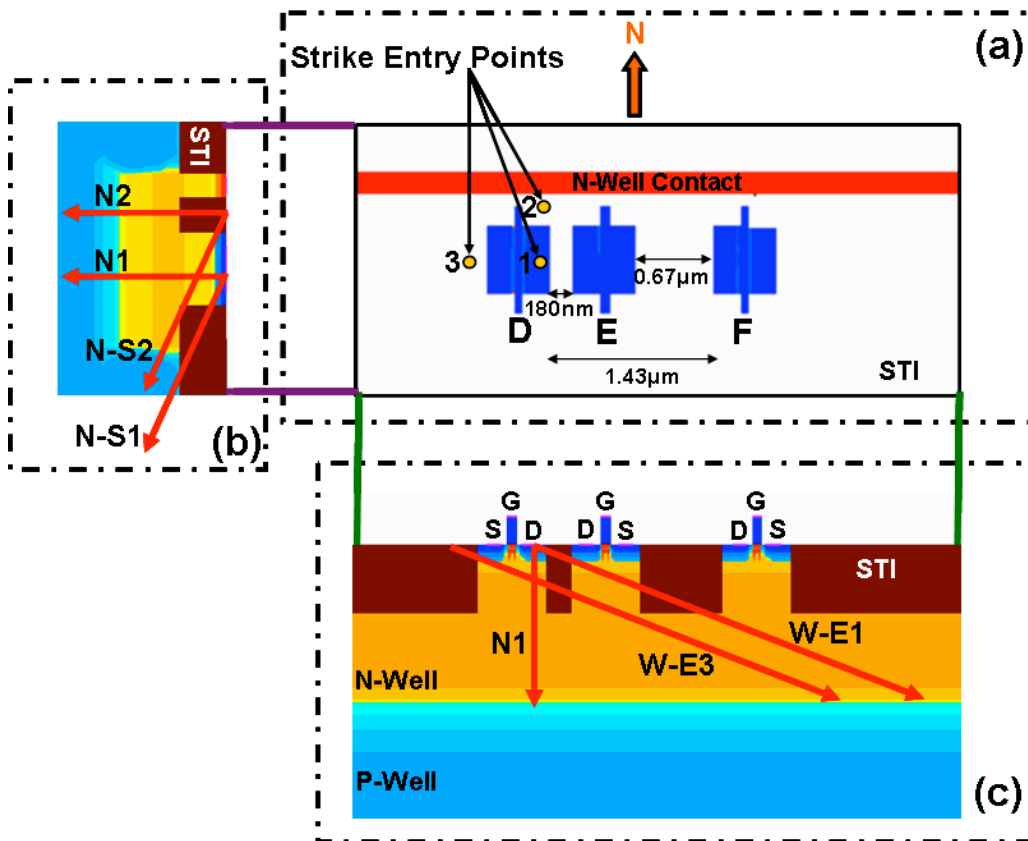


Fig. 50. Strike locations and directionality of the ion-strikes for 3-D TCAD structure. 1, 2, and 3 in (a) represent the exact point of incidence for the ion. Letters preceding 1, 2, or 3 indicate whether the hit was Normal (N), North-to-South (N-S), or West-to-East (W-E). (b) and (c) shows the trajectory of the ion on cross-section views.

Table 3: Charge Collected (fC) for Normal and Angled Hits on PMOS Devices for Cross-section Study.

	N1	N2	N-S1	N-S2	W-E1	W-E3
PMOS D	68	50	63	82	30	72
PMOS E	37	24	18	47	88	95
PMOS F	0	0	0	0	108	87

PMOS F showed a strong dependence only for the W-E hit because the normal and N-S hits did not create an n-well collapse extending to the location of PMOS F. The W-E strike created an ion-track that is located directly underneath PMOS F and this in turn leads to a parasitic pnp bipolar turn-on for PMOS F. The charge collection on PMOS D and PMOS F for W-E strikes presented in Table 3 results in an upset of the DICE latch as indicated in the SHMOO plot of Fig. 49. The W-E strike results were representative of a significant increase in SE sensitive area associated with the increased cross-section seen in the heavy-ion data.

To further illustrate the W-E charge sharing effect, a simulation was conducted to determine the extent of the n-well potential collapse that leads to the parasitic pnp bipolar turn on. Results presented in Fig. 51 show that the n-well collapse from a W-E strike for LET of 21 MeV·cm^2/mg at an angle of 60° can be between 4.5 μm to 5 μm from the strike location, implying that any hardened circuit that has sensitive PMOS pairs located within 5 μm of the hit location can display increased charge sharing effects due to parasitic bipolar amplification in this technology. This is even more remarkable considering that the n-well is densely contacted with the n-well contact strip (Fig. 50(a)) running just behind the slice shown in Fig. 51. Conventional wisdom might assume that such a densely-contacted n-well would ensure an effectively-pinned n-well potential,

thereby reducing parasitic bipolar conduction. However, these results clearly indicate a substantial n-well collapse and the possibility for parasitic bipolar turn-on as described in [Ols07] and the previous chapter.

These results indicate that angled strikes can have a significant effect on the sensitive area of devices and the directionality of the angled strike can have a significant impact on the SE cross-section for a circuit as seen in the heavy-ion data.

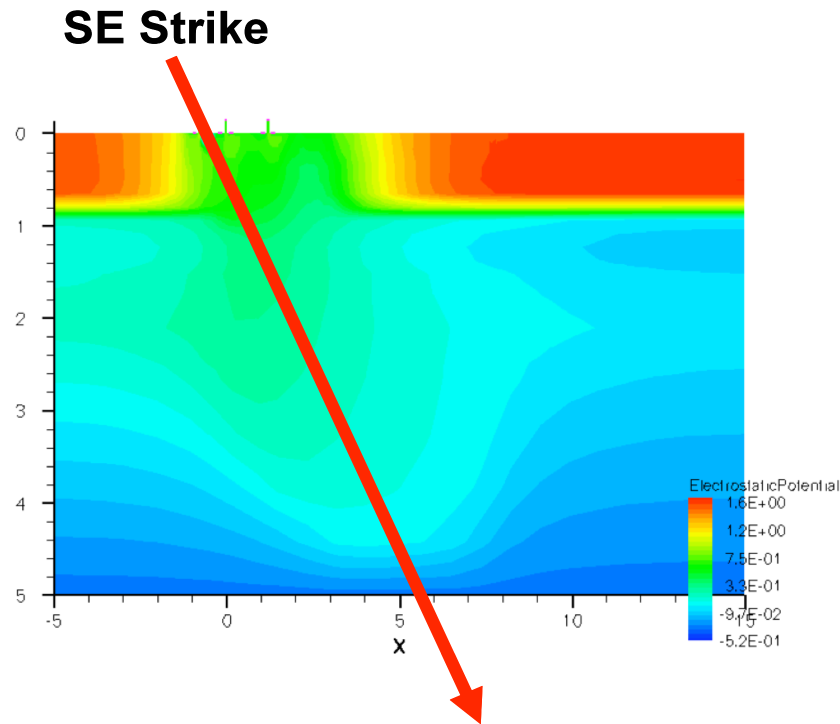


Fig. 51. N-well potential collapse of 4.5 µm - 5 µm from penetration point due to the W-E angled strike.

Conclusion

Heavy-ion data showing a significant dependence of upset cross-sections and LET thresholds on the orientation or directionality of the impinging ion vectors for a 90 nm

DICE latch was presented in this chapter. Conventional error-estimation techniques overlook this directional dependence, resulting in potential underestimation of error rates for deep-submicron technologies.

Using 3-D TCAD simulations, this chapter has described that the charge collection and charge sharing processes have a strong dependence on orientation of the angled strike (N-S vs. W-E). The directionality difference between N-S and W-E can be explained by two charge collection mechanisms exacerbated by W-E single-event strikes: the multi-node PMOS charge sharing between device nodes (affects the LET threshold) and the n-well collapse triggering parasitic conduction (affects the cross-section). The next chapter examines and analyzes charge sharing mitigation techniques to limit the directional dependence of charge sharing seen in this chapter.

CHAPTER V

MITIGATION TECHNIQUES FOR SINGLE-EVENT INDUCED CHARGE SHARING IN A 90 NM BULK CMOS PROCESS

Introduction

The previous chapter has shown a significant dependence of upset cross-sections and LET thresholds on the directionality of the impinging ion vectors due to charge sharing among circuit nodes. In this chapter, mitigation techniques to reduce the increased SEU cross-section associated with charge sharing in a 90 nm DICE latch are proposed. 3-D TCAD is used to analyze different layout mitigation techniques. Also, a RHBD latch array with different implementations of mitigation techniques has been fabricated in a commercial 90 nm bulk CMOS process and the resulting reduced error cross-sections due to heavy-ion exposure are presented. The results quantify the effectiveness of layout mitigation schemes in decreasing the hardened latch susceptibility to charge sharing resulting from angular strikes in deep-submicron technologies.

3-D TCAD Analysis

Using 3-D TCAD models calibrated to match the electrical characteristics of the commercial 90 nm process, charge sharing simulations were conducted to examine the effects of layout mitigation techniques, such as nodal separation, interleaving, guard-diodes and guard-rings on reducing the angular effects of charge sharing. The mitigation techniques examined are based on charge sharing mechanisms. The main mechanism for

PMOS to PMOS charge sharing is parasitic bipolar amplification; for NMOS to NMOS charge sharing, the main mechanism is charge diffusion [Amu06a].

Nodal Spacing

The 1st set of 3-D TCAD mixed-mode simulations was to examine the effect of nodal spacing on charge sharing. Simulations were conducted for two NMOS devices simulated in the OFF state (i.e., Gate LOW, Source LOW, Drain HIGH) and two PMOS devices in which both devices were simulated in the OFF state (i.e., Gate High, Source High, Drain LOW - PMOS devices) as illustrated in Fig. 52. The devices were included in a 5-string inverter chain with the rest of the circuit in compact models of the commercial 90 nm process. The struck device is defined as the *active* device and the charge sharing device in proximity to the struck device is defined as the *passive* device. Nodal spacing from 140 nm to 2 μm as illustrated in Fig. 52 was simulated and simulations were conducted for normal hit on the drain of the active device.

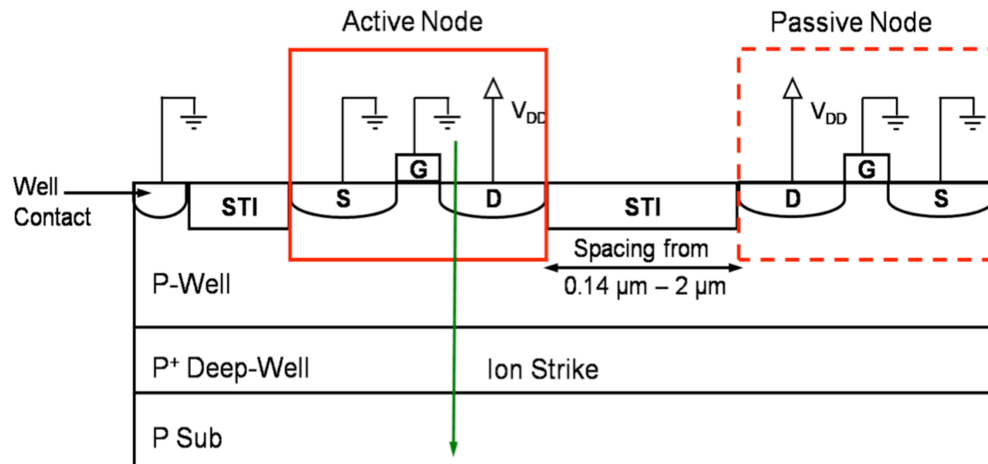


Fig. 52. Illustration of the nodal spacing between the active and passive NMOS devices.

Results in Figs. 53 and 54 show the diminished charge sharing effect with increased nodal spacing. It should be noted that the passive PMOS device results in Fig. 53 show increased charge collection in comparison to the passive NMOS device results in Fig. 54 for nodal spacing less than 1 µm. For nodal spacing greater than 0.70 µm, the passive NMOS device shows increased charge collection in comparison to the passive PMOS device results. The difference in the nodal spacing effect for passive NMOS and passive PMOS charge collection is due to the difference in the charge collection mechanisms. For passive PMOS, the main mechanism is bipolar amplification and with increased distance, the n-well potential collapse does not extend to the passive PMOS device. The main mechanism for passive NMOS is charge diffusion. For the active devices, the location of the passive device has no noticeable effect on the amount of charge collected on the active device as seen in Figs. 55 and 56.

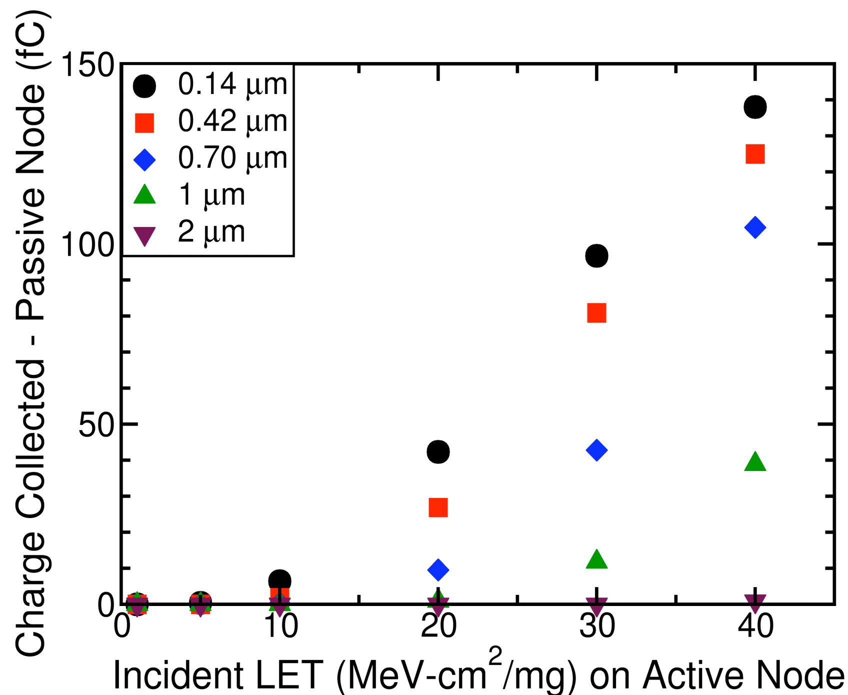


Fig. 53. Passive PMOS device charge collection shows a significant decrease with increased nodal spacing between the active and passive PMOS devices for a normal hit.

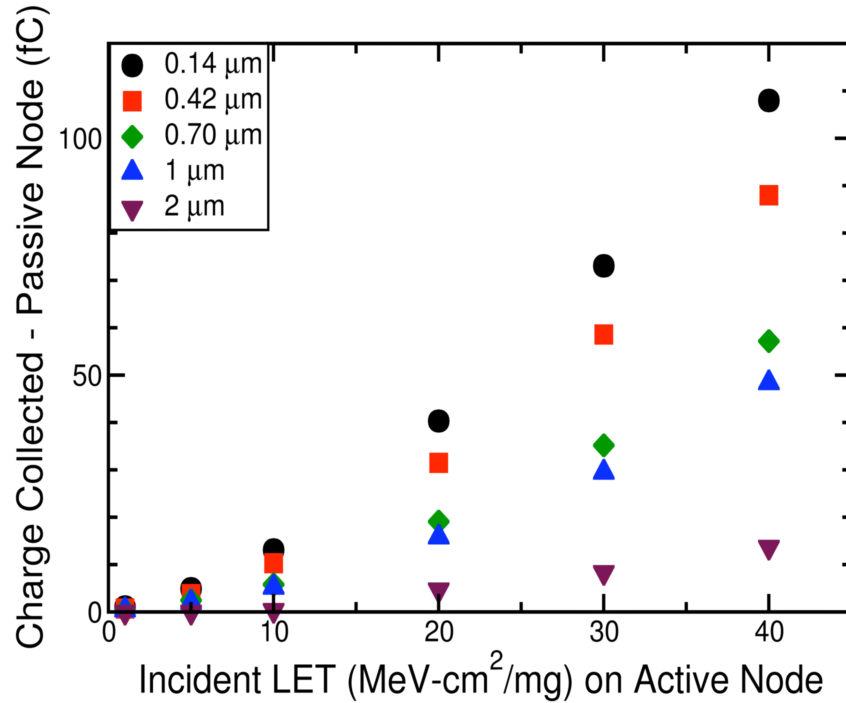


Fig. 54. Passive NMOS device charge collection shows a significant decrease with increased nodal spacing between the active and passive NMOS devices for a normal hit.

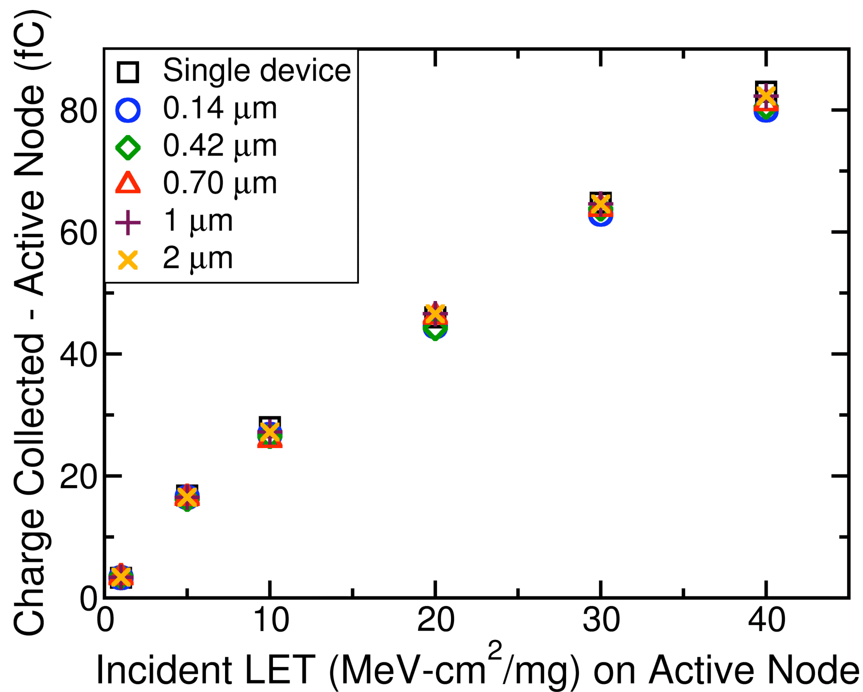


Fig. 55. Active PMOS device charge collection shows no dependence on the nodal spacing between the active and passive PMOS devices.

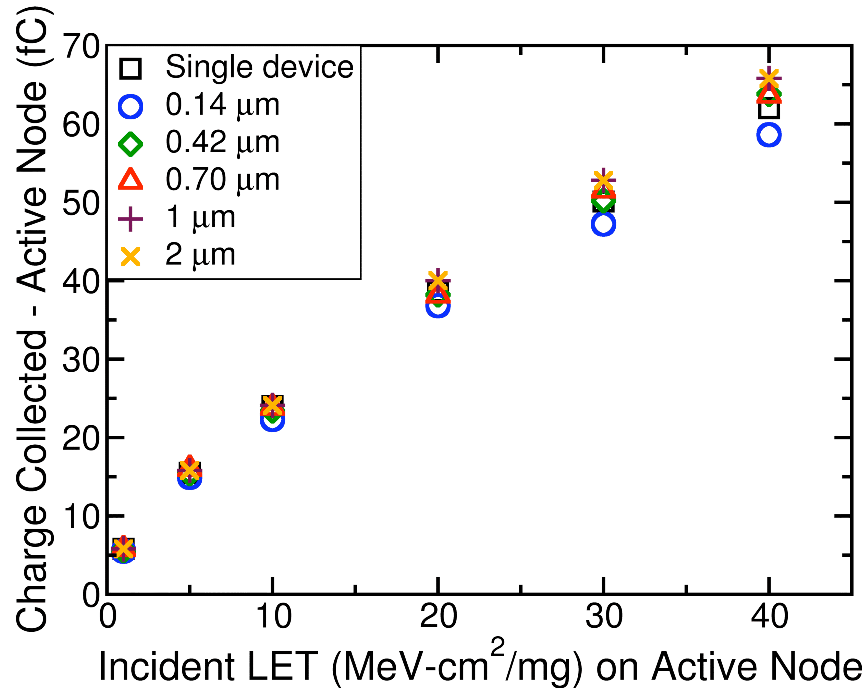


Fig. 56. Active NMOS device charge collection shows no significant dependence on the nodal spacing between the active and passive NMOS devices.

Interleaving

Since layout area is of concern with any circuit design, use of interleaving as discussed by [Bla05], [Amu06b] is recommended versus simple nodal spacing. Interleaving involves the placement of non-sensitive transistors between two critical nodes in the circuit layout as illustrated in Fig. 57. For example, in the DICE latch, simultaneous charge collection on two sensitive circuit nodes will result in an upset. Placement of non-sensitive transistors between the two critical nodes during the circuit layout process will help conserve area, leads to charge collection on the non-sensitive transistors, and also results in the nodal separation.

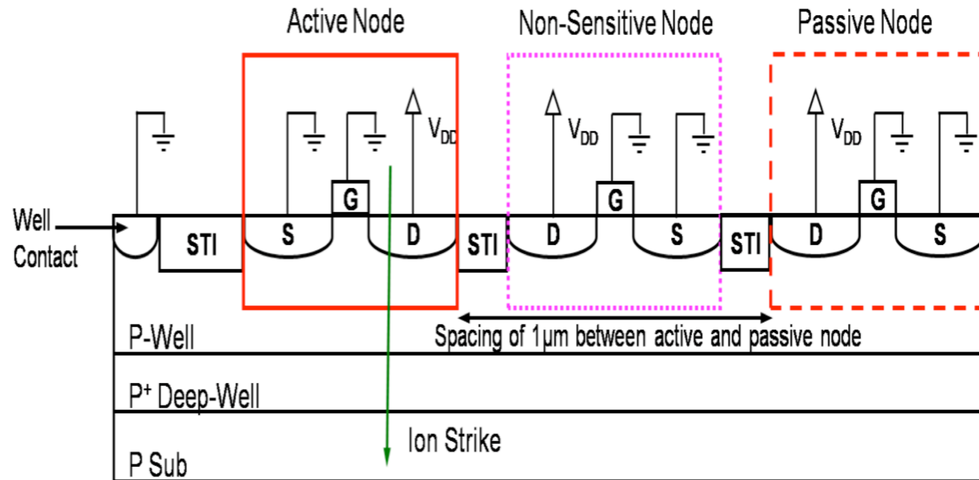


Fig. 57. Illustration of the NMOS interleaving setup. The non-sensitive node (i.e., in-between transistor) helps fill up the space, thereby conserving area.

The results in Figs. 58 and 59 show that for normal and 60° angled hits, the use of interleaving is just as effective as 1 µm nodal spacing. There is a slight decrease in the amount of charge collected for the passive NMOS device (Fig. 59) due to the charge collection process of diffusion, whereas there is no difference in the passive PMOS device (Fig. 58) as the non-sensitive device plays no role in mitigating the parasitic bipolar effect. It should be noted that the non-sensitive device does collect charge as shown in Figs. 60 and 61 but the collected charge is of no interest for redundancy-based circuit level hardening techniques.

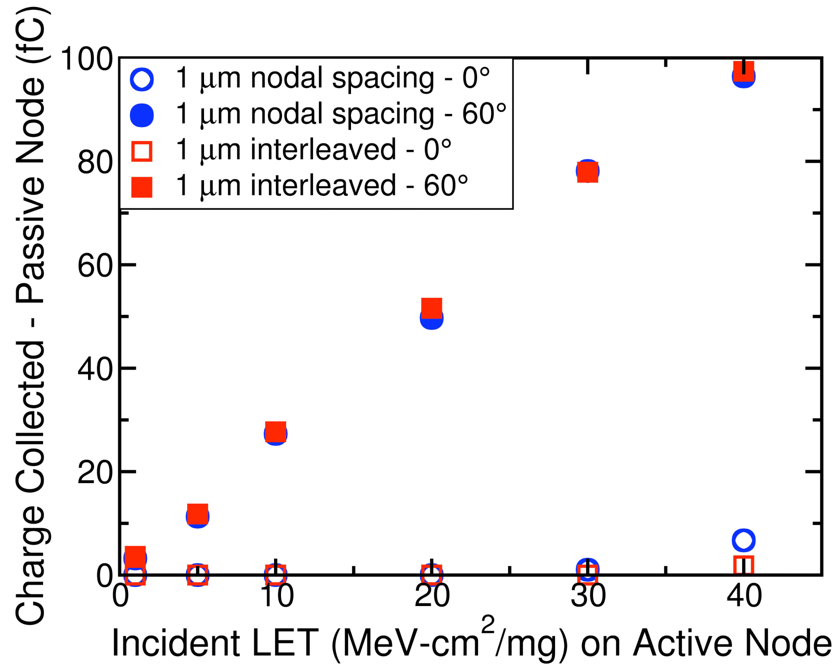


Fig. 58. For normal and angled hit, the interleaving technique is just as effective as the 1 µm nodal spacing technique in mitigating the charge sharing effect for the PMOS passive device.

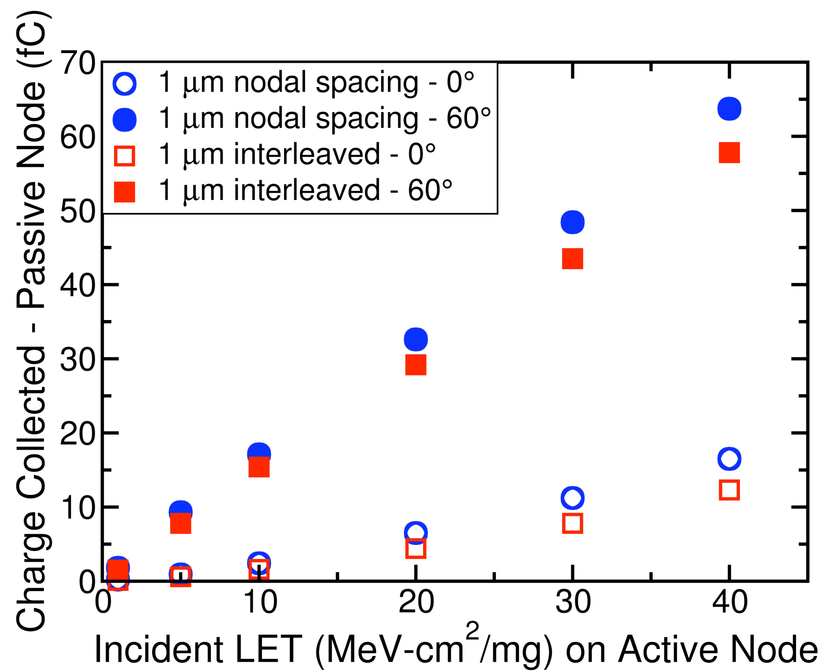


Fig. 59. For normal and angled hit, the interleaving technique shows a slight improvement in comparison to the 1 µm nodal spacing technique in mitigating the charge sharing effect for the NMOS passive device.

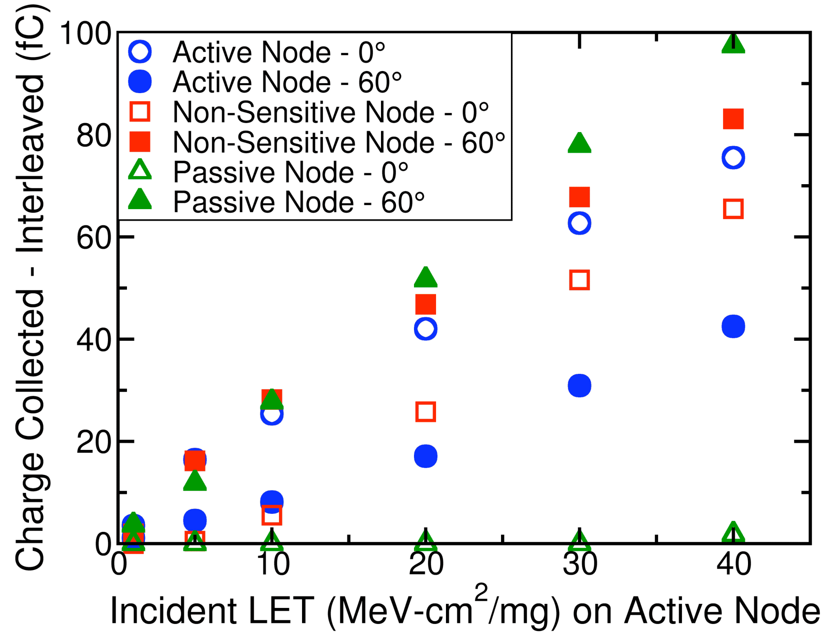


Fig. 60. This plot shows the amount of charge collected for the active, non-sensitive, and passive device for the PMOS setup. Charge collection on the non-sensitive device is significant for normal and angled hits, but of no concern as the device is considered to be non-sensitive for redundancy based circuit level hardening techniques.

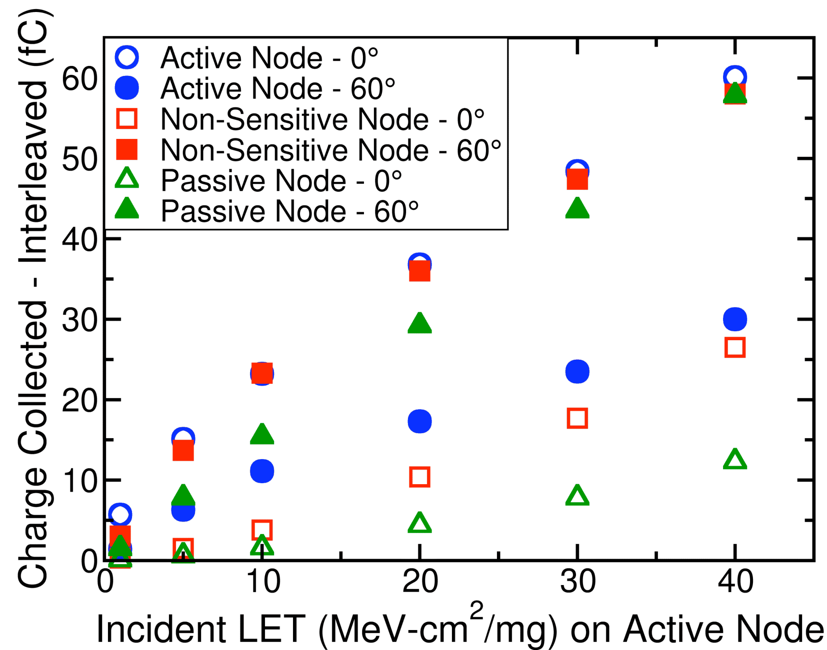


Fig. 61. This plot shows the amount of charge collected for the active, non-sensitive, and passive device for the NMOS setup. Charge collection on the non-sensitive device is significant for normal and angled hits, but of no concern as the device is considered to be non-sensitive for redundancy based circuit level hardening techniques.

Guard-ring and Guard-diode

The next set of simulations was to examine the use of guard-rings and guard-diodes in mitigating the charge sharing effect. Guard-rings are used as a SE mitigation technique, as they provide additional well-taps to help reduce the well potential collapse required to turn on the parasitic bipolar transistor [Bla05], [Ols07] using same doping as well type. Guard-diodes present additional reverse-biased junctions besides the drain terminal to help siphon the deposited charge. The illustration in Fig. 62 shows the placement of the guard-ring around the passive PMOS device and the guard-diode around the passive PMOS device. The illustration in Fig. 63 shows the guard-ring and guard-diode setup for the passive NMOS device.

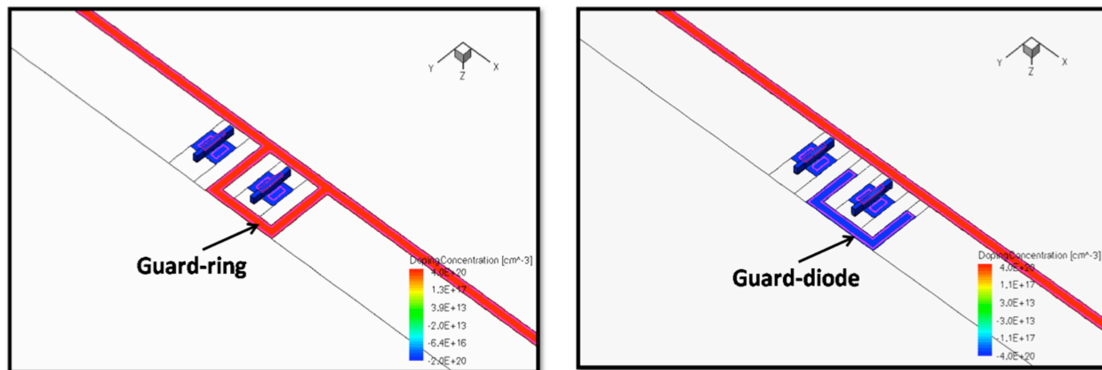


Fig. 62. The left figure shows a top-view of the guard-ring around the passive PMOS device. On the right, a top-view of the guard-diode around the passive PMOS device is shown.

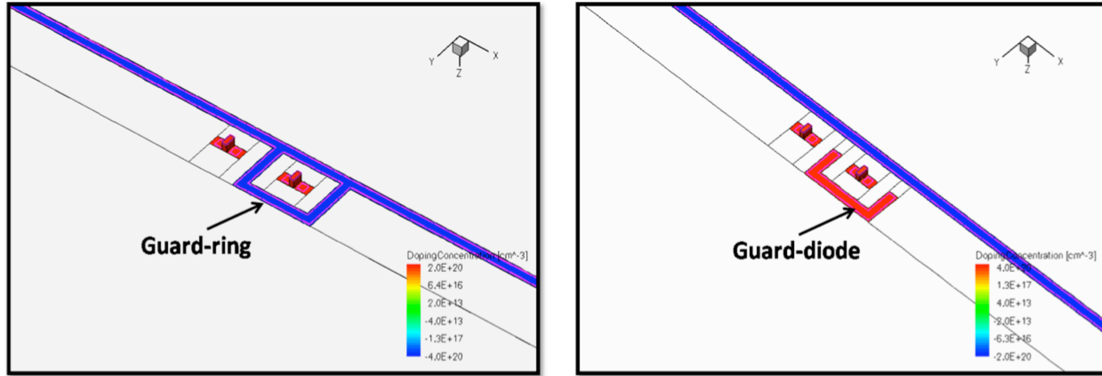


Fig. 63. The left figure shows a top-view of the guard-ring around the passive NMOS device. On the right, a top-view of the guard-diode around the passive NMOS device is shown.

The result in Fig. 64 shows the effectiveness of the guard-ring in reducing the amount of charge collected for the passive PMOS device for both a normal and 60° angled hit. The guard-ring helps maintain the n-well potential around the passive PMOS device, thereby limiting the parasitic bipolar amplification of SE related currents. However, the guard-ring does not eliminate charge collection for the passive PMOS device, especially for angled strikes as seen in Fig. 64. The guard-diode has no effect in reducing the charge collected for the passive PMOS device as seen in Fig. 64; this is due to the fact that the guard-diode does not help mitigate the parasitic bipolar effect because it has no effect on maintaining the well potential. For the passive NMOS device, Fig. 65 shows the effectiveness of the guard-diode in reducing the amount of charge collected for the passive NMOS device for both a normal and 60° angled hit. The guard-diode is effective in mitigating the charge collection on the passive NMOS device by siphoning deposited charge through the diffusion collection mechanism, thereby reducing the amount of charge collected on the Drain terminal of the passive NMOS device. The guard-ring has no significant effect in reducing the passive NMOS device charge collection. The main

reason for this is that the main charge collection for NMOS charge sharing is by charge diffusion [Amu06a].

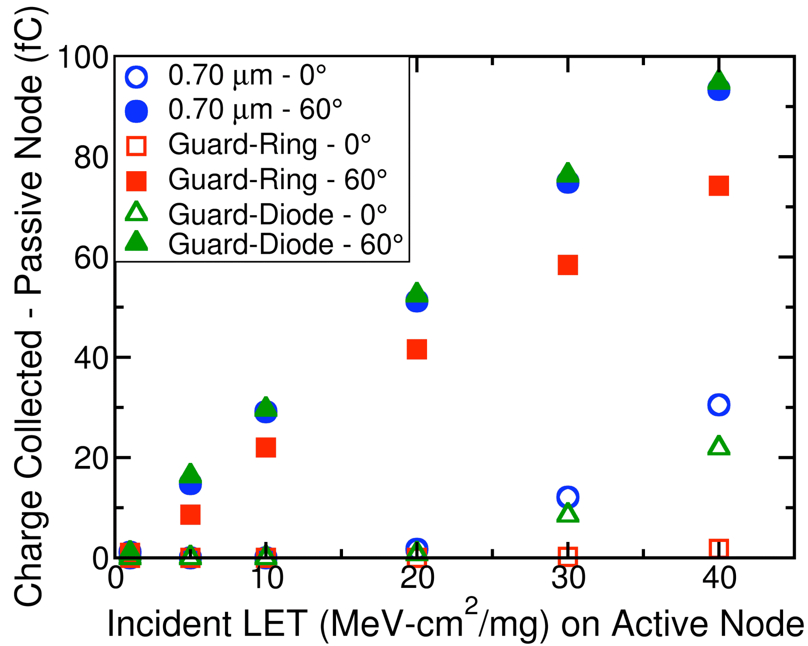


Fig. 64. The use of guard-ring reduces the passive PMOS device charge collection for both normal and 60° angled hit. However, the amount of charge collected is still significant and can cause an upset in deep-submicron technologies. The guard-diode has no effect in reducing the charge collection for the passive PMOS device.

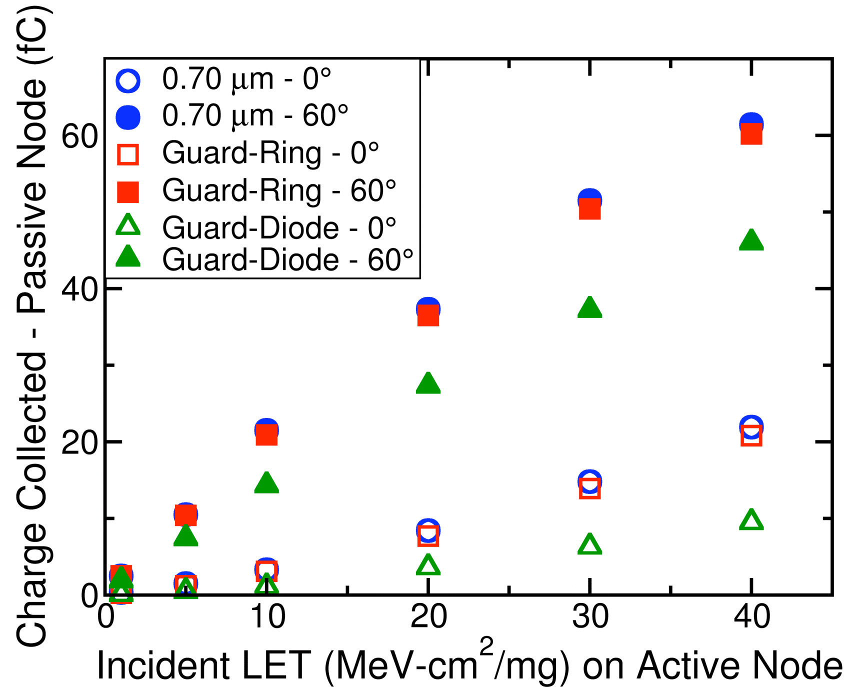


Fig. 65. The use of guard-diode reduces the passive NMOS device charge collection for both normal and 60° angled hit. However, the amount of charge collected is still significant and can cause an upset in deep-submicron technologies. The guard-ring has no effect in reducing the charge collection for the passive NMOS device.

Heavy-Ion Experiment Details

Heavy-ion experiments were conducted at the Lawrence Berkeley National Laboratory on a soft-error-hardened DICE latch. The DICE latch design is an interlocked latch using two storage nodes for each bit to provide information redundancy [Cal96]. As a result, it is considered virtually immune to an upset when a single storage node is perturbed. However, the DICE latch does possess identifiable sensitive node pairs that can cause an upset with simultaneous perturbations on two storage nodes [Vel96], [Amu07]. Mitigation of simultaneous charge collection between sensitive node pairs increases tolerance to single-event soft errors.

Three different DICE layout topologies were considered in the study of Sub-100 nm charge sharing induced soft error effects:

1) Layout design without any mitigation technique (i.e., no regard to the location of the sensitive pairs) – NORMAL.
2) Mitigation through layout spacing with a minimum 2 μm nodal separation of all sensitive pairs - WOGR (With-Out Guard-Ring).
3) Mitigation through layout spacing with 2 μm nodal separation of the sensitive pairs and in addition placement of guard-bands (i.e., contacted well region on all four sides of the transistor) around one of the devices (NMOS and PMOS) that make up a sensitive pair - WGR (With Guard-Ring).

The 2 μm nodal separation was chosen based on 3-D TCAD simulation results presented in the above section which show that charge sharing between devices is significantly reduced for a nodal separation of 2 μm (Figs. 53 and 54). These topologies were designed to investigate directional sensitivity and examine the effectiveness of layout mitigation techniques. The DICE latches were implemented in a shift register fashion with 511 stages and fabricated in a commercial 90 nm bulk CMOS technology.

The ions used were Argon, Copper, Krypton, and Xenon with LET ranging from 9.74 to 58.6 MeV·cm^2/mg. The lower LET range tested represents energies typical of neutron-generated particles [Haz04]. The angles used for exposure were 0° and 60° from normal. The direction of the angled incident ions (i.e., 60°) was varied from *orthogonal* to the power rail (i.e., *North-to-South*) to *parallel* to the power rail (i.e., *West-to-East*) as indicated in Fig. 45 in the previous chapter. Multiple input data patterns were tested at each ion exposure.

Heavy-Ion Results

The data in Fig. 66 show results comparable to previously presented data (Fig. 46 in the previous chapter) when no mitigation scheme is employed. Results show that DICE latches are more sensitive to W-E angular single-event strikes compared to the Normal and N-S angular SE strikes as discussed in the previous chapter. The increase in upset cross-section can be attributed to an increase in multiple node charge collection for sensitive pairs in the same well [Amu06a] (i.e., PMOS transistors in n-well and NMOS transistors in p-well) as the strike vectors traverse parallel to the power rails (Fig. 45) affecting multiple sensitive nodes.

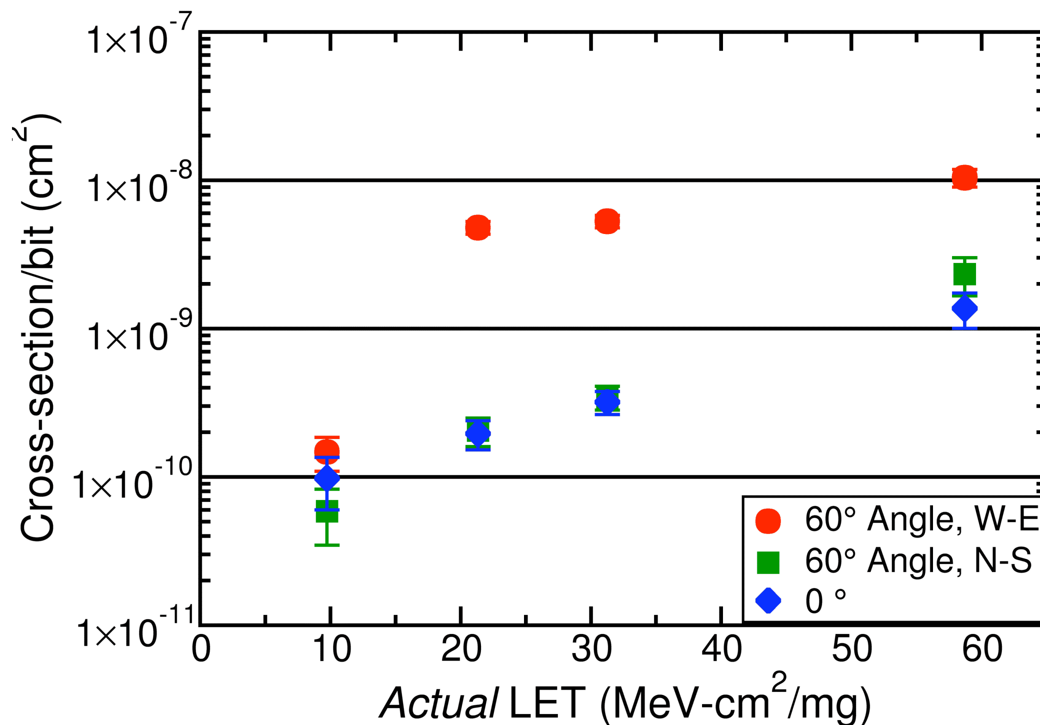


Fig.66. Heavy-ion data for the NORMAL layout shows an order of magnitude increase in upset cross-section for the 60° W-E strikes in comparison to the 60° N-S and 0° strikes.

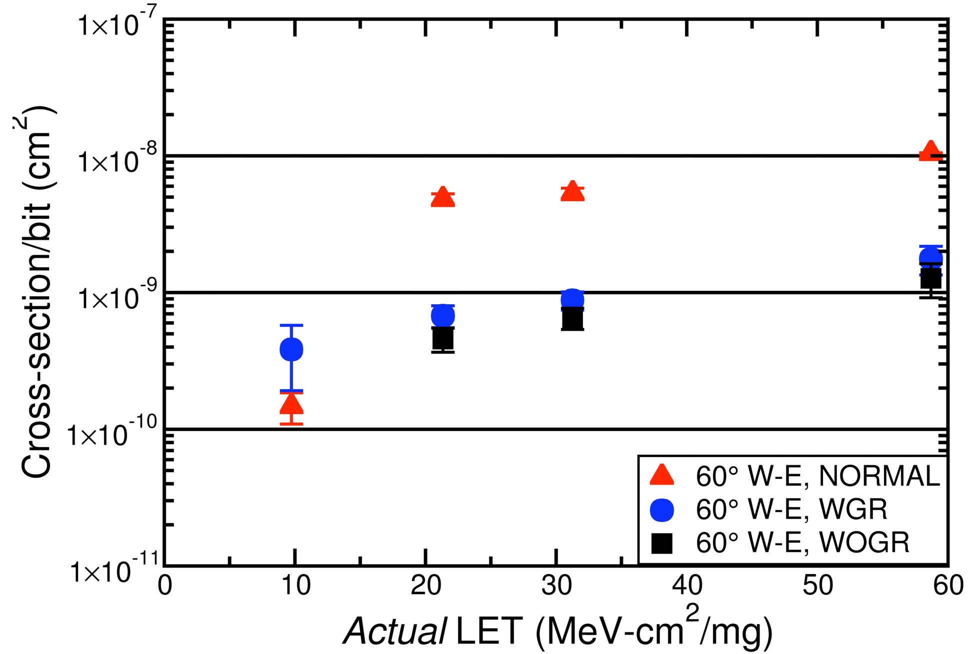


Fig. 67. Evaluation of the 60° W-E data for the three different layout topologies shows an order of magnitude decrease in upset cross-section for the WGR and WOGR layouts in comparison to the NORMAL layout.

The data in Fig. 67 shows a comparison of the three different layout topologies and the effectiveness of the layout mitigation techniques in reducing the order of magnitude increase in upset cross-section from that seen in Fig. 46 and Fig. 66 for 60° W-E angular strikes. The results show that nodal separation of the sensitive pairs (WOGR layout) is an effective measure in mitigating the directional sensitivity. However, as seen from the simulation results in Figs. 53 and 54, although 2 μm nodal spacing decreases the total charge collected at the passive node, enough charge can be collected to cause an upset or a transient at the passive node. The resulting cross-section from the 3rd layout topology (WGR layout), which included nodal separation and guard-rings around one of the sensitive pairs, is comparable to the WOGR layout as seen in Fig. 67. This shows that the guard-ring does not add any appreciable hardness improvement to the DICE circuit. This is due to the fact that the guard-ring is ineffective for passive NMOS device charge

collection as shown in Fig 65. Furthermore, the guard-ring does not eliminate charge collection for passive PMOS devices, as shown in Fig. 64, hence, the insignificance in reducing the upset cross-section (i.e., comparison between WGR vs. WOGR) as seen in Fig. 67.

Conclusion

This chapter has examined and quantified the effectiveness of different mitigation techniques in reducing the charge sharing effects for Sub-100 nm bulk CMOS technologies. The use of nodal spacing is an effective technique but area intensive; hence, interleaving is a better technique. Interleaving is comparable to nodal spacing and has the additional benefit of helping conserve area. The use of guard-rings is an effective mitigation technique for charge reduction on the passive PMOS device, but results show that the guard-rings have no effect on passive NMOS devices. In contrast, guard-diodes are effective in reducing the charge collection on passive NMOS device but have no effect on passive PMOS device.

This chapter has also demonstrated the effectiveness of layout mitigating techniques in reducing the soft-error cross-section (due to charge sharing) in the presence of directional sensitivity in a hardened latch design. The increased charge sharing for transistors in the same well for angular ion strikes depends on the directionality of the strike. Mitigation schemes proposed show that the DICE latch and other redundancy based designs can achieve improved SE hardness by physically separating the sensitive pairs in the layout of the circuit. Another common hardening technique (use of guard-rings) that was used for this design shows no noticeable improvement, due to its inability

to overcome parasitic bipolar amplification for PMOS transistors and its ineffectiveness in reducing the charge collection on NMOS transistors.

CHAPTER VI

CONCLUSION

An interesting phenomenon, "charge sharing", capable of increasing the SE vulnerability of hardened circuit designs has been investigated in this work. Charge sharing is a significant SE effect in Sub-100 nm technology and has been shown through 3-D TCAD mixed-mode simulations and heavy-ion data to create significant reliability issues. The angular effects of charge sharing have been simulated and experimentally verified through heavy-ion testing.

The research presented in this dissertation has achieved the following:

1) Presentation of the first experimental data verifying the parasitic bipolar amplification effect in PMOS devices and identification of layout techniques to minimize the parasitic bipolar amplification of SE currents
2) Development of optimum transistor sizing to reduce SE pulse-widths for Sub-100 nm technologies.
3) Presentation of the first experimental data verifying the charge sharing effect in a Sub-100 nm bulk CMOS process.
4) Examination of the charge sharing effect in the IBM 90 nm CMOS9SF Bulk CMOS process.
5) Quantification of the significance of charge sharing angular effects through detailed 3-D TCAD mixed-mode simulations.

6) Verification of the directional charge sharing effects through heavy-ion testing.
7) Examination of different layout charge sharing mitigation techniques through 3- TCAD simulations to curb the directional dependence of charge sharing.
8) Verification of the proposed layout mitigation techniques through heavy-ion experiments.

This research effort will significantly impact the radiation effects community by:

a) Providing design guidelines for optimum transistor sizing to reduce SE pulse-width.
b) Proposing a viable charge collection test circuit for use in investigating Sub-100 nm SE phenomena.
c) Determining the angular effects of charge sharing in Sub-100 nm hardened circuits and showing possible underestimation of SE cross-section and LET threshold that could occur as a result of charge sharing in the Sub-100 nm technologies.
d) Analyzing and presenting experimentally verified layout mitigation techniques for improved radiation hardness of the Sub-100 nm technologies.
e) And ultimately, demonstrating the importance of considering the impact of charge sharing in determining the SE response of Sub-100 nm technologies.

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