ENHANCED CHARGE COLLECTION IN SILICON CARBIDE POWER MOSFETS DEMONSTRATED BY PULSED-LASER TWO-PHOTON ABSORPTION SEE EXPERIMENTS

By

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1 INTRODUCTION

There is a strong incentive for designers of any satellite, spacecraft, or rocket with high power requirements to increase the operating voltage of its power supplies [1]. For constant power consumption, a higher operating voltage will result in less current draw, allowing for thinner and therefore lighter cabling throughout the satellite. This will let designers put more experimental or commercial load on their device, making every mission more productive than formerly possible. Silicon carbide has the capability to offer superior performance to even the theoretical limits of silicon in power electronics. SiC has a higher electric field breakdown and thermal breakdown, and these both allow for smaller devices for a needed voltage and current-handling capability, resulting usually in a lower capacitance and on resistance relative to a silicon device rated to meet the same specifications. More importantly, SiC can be used to handle voltage rails that are at least 1000V in standard power electronic packaging while maintaining these observed benefits over silicon. However, there are three failure mechanisms due to radiation that have been observed in SiC power devices, single event gate rupture (SEGR), single event burnout (SEB) and single-event-induced drain to source leakage current degradation. All three of these can occur in environments that are seen by electronics at various locations in space, and due to this make SiC power devices currently unsuitable for most missions. These failures have been recreated in controlled experiments and simulations with the intent of better understanding the physical mechanisms responsible for them, and the design and conclusions of these experiments will be summarized in this paper.

1.1 Experimental Techniques Available

The goal of every experimental technique mentioned in this paper is to replicate the effects of a single particle passing through a device and causing some response in the electric properties of the device. In the case of SEGR, SEB, and leakage current degradation, the response is permanent in most real-world settings, though this issue can be negated using various experimental designs. The following tests include heavy ion, proton, and neutron testing, TCAD simulation, and two photon laser testing, and are listed in the order of their contributions so far to the explanation of the previously mentioned single event effects in silicon carbide power MOSFETs.

1.1.1 Heavy Ion, Proton, and Neutron Testing

Heavy ion, proton, and neutron testing utilize a beam of radioactive particles of a consistent energy that is directed at the test devices. For a given semiconductor material there is a linear energy transfer, or LET, of each particle into the device, which determines how many charge carriers are generated for a particle hit. Particle testing has been experimentally successful in producing SEGR, SEB, and leakage current degradation in both silicon and silicon carbide power MOSFETs [2]–[6]. This testing is an exact representation of the effects specific examples of particles seen in space would have on a device, though for experimental convenience usually at much higher fluxes. In most single-event effects, a particle with a certain LET must travel along a specific path or set of paths within a device, an idea that is experimentally supported for both SEGR and SEB. With a high flux relative to most expected real-world radiation environments in space, single event effects, should they be possible to produce for a given set of circuit conditions, can occur in minutes rather than days or even years.

In testing, SEGR can be distinguished from SEB by monitoring the drain and gate currents, as shown in Fig. 1, from Akturk *et al.*[3]. In a SEGR, the damage to the gate results in a permanent current increase through the gate, whereas a SEB may result in a capacitive spike in gate current but no sustained effect. In both cases the destructive nature is due to the allowance of a sustained negative drain current large enough to cause damaging power dissipation.

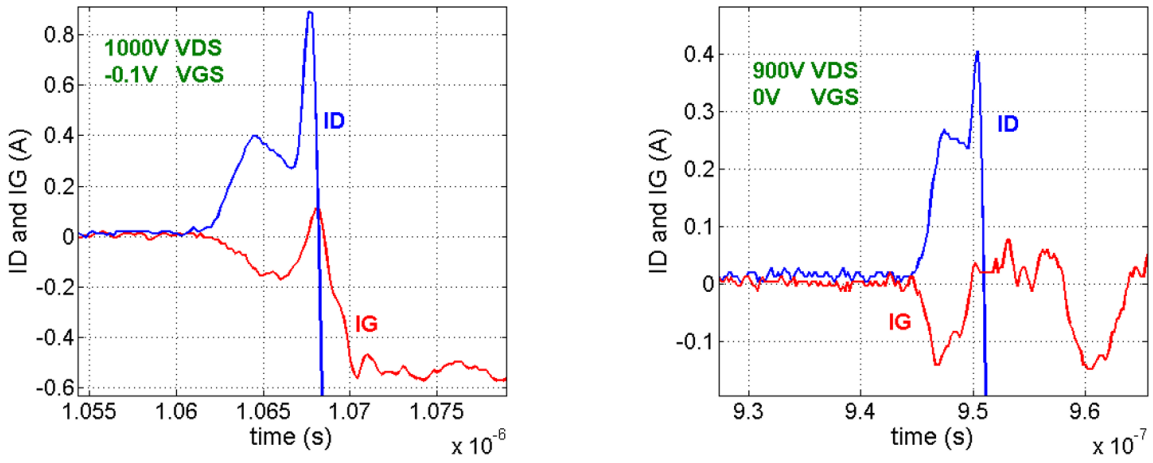


Fig. 1. Experimental drain and gate currents for single event gate rupture and single event burnout respectively, as observed and processed by Akturk e*t al.* [3]**.**

1.1.2 TCAD Simulation

TCAD simulation is the use of mathematical models to represent an ion strike or any number of radiation-like events, both physically possible and not. Simulation, when treated as an extension of heavy ion testing rather than a supplement to it, can provide insightful results that are otherwise not possible to acquire. Individual physics models can be turned off once a device is accurately modeled in simulation to determine which physical mechanism is essential for producing the result observed in both simulation and in physical experiments. As in particle testing, both the generation of charge carriers and the direction and velocity of a particle can be

chosen1. Additionally, simulations incur a significantly smaller financial cost to run than particle tests, and can yield results more quickly in certain cases.

1.1.3 Two-photon Laser Testing

Two-photon laser testing generates a localized collection of charger carriers at a focused point within a semiconductor. Charge carrier generation test locations within a device can be highly controlled in depth and within the plane of the device, allowing for tests to find specific regions of higher charge carrier generation sensitivity. Laser testing has produced both SEGR and SEB in devices using frontside tests [7], [8] and SEB in devices using backside tests [9], [10]. In addition, experimental designs have been constructed that limit current in the event of a SEB to take advantage of the localized nature of laser testing for generating maps of the sensitive volumes [8]–[10]. These volumes are locations in which a large enough charge carrier generation will reliably result in the tested single event effect, whether SEB or SEGR, or leakage current degradation. While there have been TPA testing used on SiC diodes to study SEB [10], no work has been done to compare SiC diodes and MOSFETs using this technique.

1.2 Observed Results

Utilizing heavy ions of various LETs on silicon devices, Allenspach *et al.* [4] identified three regions of operation for silicon power MOSFETs, differentiating between SEB and SEGR as the dominant cause of single event destructive failure. As shown in Fig. 2, from Wheatley *et al.* [11], the three regions are dispersed based on V_{GS}, V_{DS}, and the LET of the ionizing particles. At high LET values and high magnitude negative V_{GS}, SEGR dominates, causing failure at low critical Vds values relative to breakdown. At LET values below 20 MeV-cm^2/mg SEB is most

common independent of the gate to source voltage for the specific device tested, and at these values the critical Vds was observed to be within 60% of breakdown. For moderate LET values and low magnitude negative Vgs values there is a mix of SEB and SEGR failures.

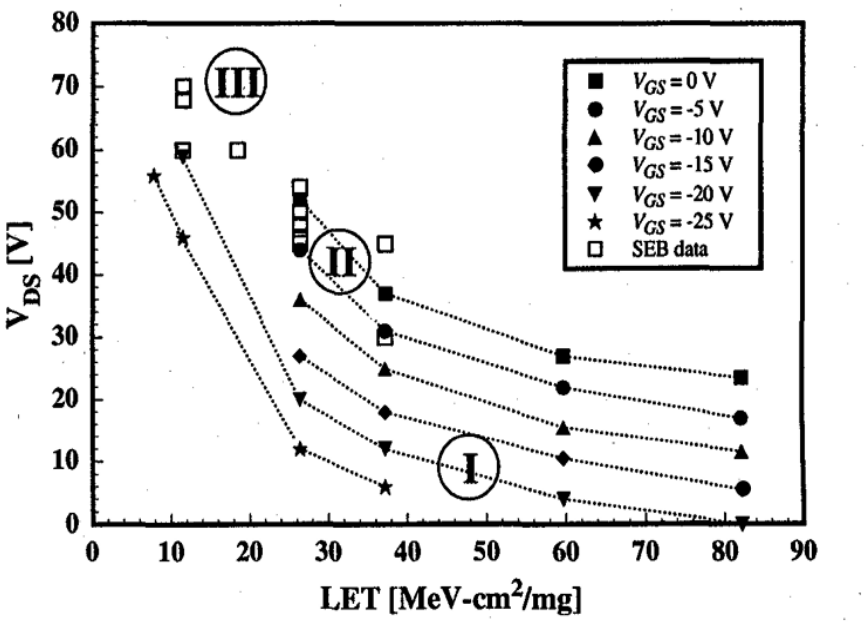


Fig. 2. Relative location of predominately SEGR failures (I), SEB failures (III), and possibility of either type of failure (II). Wheatley *et al.* [11].

This general distribution is found for silicon carbide power MOSFETSs as well, though a newer generation of Wolfspeed parts was found to have increased resistance to SEGR versus SEB relative to the generation prior [5]. This is despite the thinner oxide of the newer generation of tested parts, which intuitively would imply a more susceptible gate oxide. However, these parts are still susceptible to latent damage to the gate oxide after radiation, which presents itself as destructive gate failure in post-irradiation gate stress (PIGS) tests [12].

Heavy ion and neutron testing on both silicon and silicon carbide MOSFETs has also verified three distinct regions of operation for a constant gate to source voltage of zero with varying LET values and drain to source voltages. As shown by Fig. 3, from Mizuta *et al.* [2], for a given LET

value there exists a region of bias voltage from drain to source where there is only charge collection. Beyond a certain threshold however, there is leakage current induced in the device by radioactive particle fluence. Further increases in bias voltage increase the leakage, and eventually another threshold is crossed, at which point particles are capable of generating a destructive SEB.

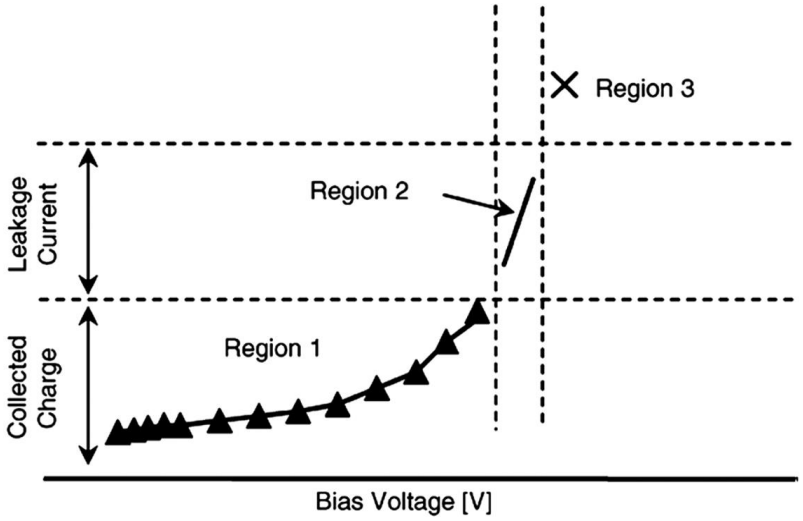


Fig. 3. Relative location of the three regions of operation of a power MOSFET in sufficiently high LET radiation to induce increased drain to source leakage current and also SEB. Mizuta *et al.* [2]**.**

Figure 4, from Witulski et al. [6], which contains additional data from Mizuta et al. [2] and Lauenstein et al. [13], displays observed and simulated observations representing the second threshold in figure 3 as a plot against threshold voltage and LET. The devices tested are all rated to support a drain to source voltage of 1200V, yet depending on the LET value fail anywhere from 1100V to 500V. The breakdown threshold appears to follow decay in critical bias voltage relative to LET, holding at roughly 500V at a LET of 20 or greater. This indicates that as the LET increases the circuit needs to generate a lesser electric field in the device to cause a SEB.

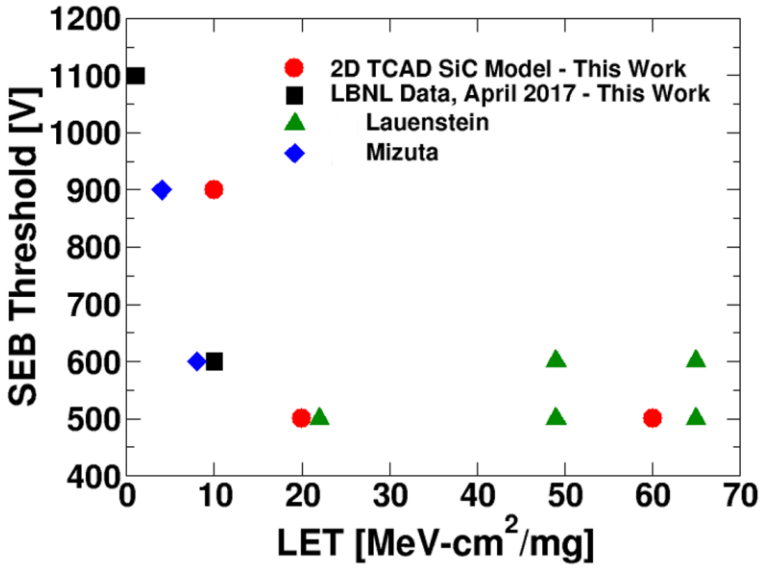


Fig. 4. Observed and simulated results characterizing the threshold voltage versus LET necessary to induce SEB in a silicon carbide power MOSFET with a breakdown voltage of 1200V. Witulski *et al.* [6]**.**

Radiation-induced leakage current has been shown to increase both with respect to LET and total fluence, with some saturation occurring relative to both of these variables. Since radiation-induced leakage current degradation, SEB, and SEGR are all destructive events, developing a non-destructive alternative for experimentation is desireable. Current silicon carbide MOSFET testing has not yet successfully utilized current limiting to operate devices in regions that induce SEB in a non-destructive manner, though simple current limiting through the use of a resistor has been unsuccessfully attempted [2]. Due to this, it is not yet verified whether or not the mechanisms that induce reverse-biased leakage continue to operate into the region where SEB occurs, continuing to increase in leakage current magnitude as LET and bias voltage increase, though there is no evidence to suggest this is not the case.

Further detail of the physical mechanism at play during a SEB has come from TCAD simulation [6]. A 1200V 4H-SiC power MOSFET was modeled using Synopsys Sentaurus. The device was then hit with a simulated heavy ion of a varying LET from 1 to 60 MeV-cm^2/mg

and a varying drain to source bias voltage from 400V to 1600V. With the Sentaurus model for impact ionization off, no SEB occurs at a bias of 900V and an LET of 10, yet with impact ionization turned on in the simulation a SEB does occur in the same testing environment. Without the impact ionization models, an ionizing particle does not generate charge carriers in the simulation calculations.

1.3 Summary

Silicon carbide power MOSFETs experience single event effects also observed in silicon devices. However, a key electrical property of SiC over silicon is an increased electric field breakdown, resulting in more efficient devices than theoretically possible with silicon [14]. As such, these issues, which all are more likely with increased drain to source bias voltage, are directly in conflict with observing a functional benefit to using SiC devices in high-radiation environments, specifically ones with high-energy particles. Heavy ion, proton, and neutron beam testing offers a faster and more controlled set of observations for the specific thresholds of single event gate rupture, single event burnout, and single event induced drain to source leakage current in regards to both LET and bias voltage. TCAD simulations verify these results for SEB. Furthermore, there exist laser-based testing methods that have successfully generated SEB and SEGR in silicon devices that should be able to produce the same in SiC devices. Of special interest is the current-limiting design multiple experiments have used to observe non-destructive SEBs in power devices. Repeating these experiments for silicon carbide could potentially provide detail into the characteristics of leakage in regions dominated by SEBs, as well as verify the nature of sensitive volumes observed for SEB in silicon.

2 Two-Photon Absorption in Silicon Carbide Power Devices

Silicon carbide (SiC) is an excellent material for power devices. It boasts a higher breakdown field and thermal conductivity than silicon, which permits devices with equivalent breakdown voltages, current ratings, and on-state resistances to be made smaller in SiC than in silicon [14]. This benefit is of importance both for terrestrial and space power systems.

Silicon power metal oxide field effect transistors (MOSFETs) are susceptible to catastrophic failure through both single-event gate rupture (SEGR) and single-event burnout (SEB), induced by protons, heavy ions, or neutrons. The mechanisms responsible for these events in silicon devices are well understood [4], [11], [15]. Specifically, for SEBs in silicon, the failures are linked to a parasitic bipolar junction transistor (BJT) inherent in the structure of conventional vertical double-diffused metal oxide semiconductor (VDMOS) power FETs, as shown in Fig. 5. Further information on the structure and function of VDMOSFETs can be found in "Advanced Power MOSFET Concepts" by B. J. Baliga [16]. Evidence indicating the influence of the parasitic BJT on SEB in silicon has been reinforced using pulsed-laser two-photon absorption backside testing with burnout protection circuits to map the regions where failure is most likely to occur [8], [9].

Silicon carbide power MOSFETs are also susceptible to both SEGR and SEB when exposed to energetic particles [5], and SEB has been examined for protons [5], heavy ions [2], [12], [17], and neutrons [18], [19]. Heavy ion-induced charge-collection measurements on MOSFETs are presented in Mizuta *et al.* [2]. The charge-collection distributions isolate two separate mechanisms, one that results in proportionate charge collection with bias and one with increasing charge amplification with bias. The latter is hypothesized in the work to be the parasitic bipolar amplification associated with SEB in silicon power MOSFETs and inherent in the vertical

MOSFET structure. In Witulski *et al.* [20], technology computer-aided design (TCAD) simulations show that a parasitic bipolar effect can be an element of the SEB process in SiC MOSFETs using structures modeled after the device used in this work.

Single-event effects can be created using pulsed-laser two-photon absorption (TPA) techniques [21]. It has been shown that SEB can be induced in SiC power diodes using TPA, and that the ability to induce SEB using TPA is dependent on diode reverse bias voltage and laser focus location within a device under test (DUT) [10].

In this work we investigate charge collection induced in SiC MOSFETs and SiC power diodes in an effort to explain similarities in their SEB response with respect to ion LET and bias voltage. Test are completed utilizing the two-photon laser technique through the backside of 1200 V devices SiC power MOSFETs to produce non-catastrophic transients. As a method of comparison, 1200 V SiC power diodes from the same manufacturer and technology are also tested. The similarity of the diodes to the MOSFETs permits isolation of MOSFET-specific mechanisms from the results. Using TPA, positional dependence of these MOSFET-specific mechanisms is found. An explanation of the results is provided, as well as a discussion comparing these results with the simulated and experimental results of prior works utilizing other radiation sources.

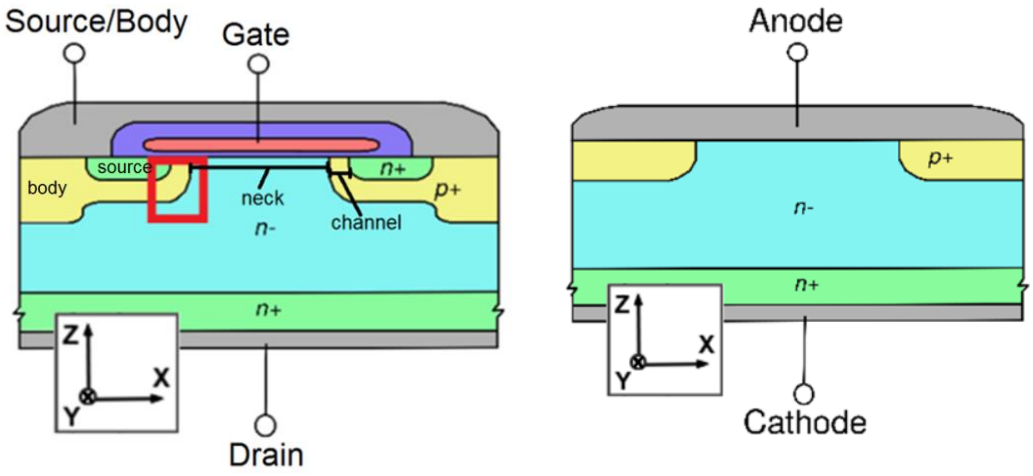
2.1 Experimental Conditions

2.1.1 Sample Devices

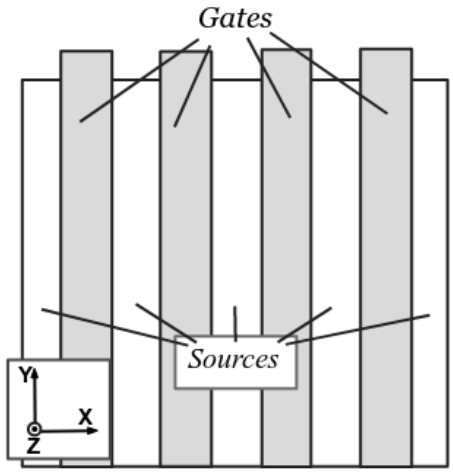
The SiC power MOSFETs used in this experiment were CPM2-1200-0080B bare die from Wolfspeed, a CREE company [22]. The MOSFETs' specifications are 1200 V, 80 mΩ, and 36 A for the blocking voltage, drain to source on resistance, and maximum drain to source current,

respectively. The devices are vertical enhancement-mode MOSFETS. The devices are fabricated on 4H SiC and consist of vertical MOSFETs symmetric along one axis while repeating along another, as shown in Figs. 1a and 1c. The stripes are repeated with a pitch of approximately 10 μm, determined by optical examination of the metal layers. The channel width is known to be approximately 1 μm.

The SiC junction barrier Schottky (JBS) power diodes tested are CPW4-1200-S020B spec sheet bare die also from Wolfspeed [23]. The device specifications are 1200 V, and 20 A for the blocking voltage and maximum current, respectively. The diodes are made of 4H SiC and have similar doping densities and structure sizes to the MOSFETs. The primary differences between the two are the lack of the gate and source structures within the diode and a hexagonal repeating geometry in the diode compared to the striped geometry in the MOSFET. Other device characteristics, including the dimensions of the hexagonal repeating geometry and overlayer composition, are not available from the manufacturer, and are not discernable optically due to the uniform topside metal layer.



(a) (b)



(c)

Fig. 5. Depiction of the vertical power MOSFET and diode structure for the devices used. Fig. 5a is a cross section through the XZ plane of a MOSFET, Fig. 5b is a cross section through the XZ plane of a diode, and Fig 5c is a top-down view of the MOSFET below the metalization. The highlighted region of the cross section covers one of the parasitic bipolar transistors inherent in the device structure, and known to play a fundamental role in SEB occurrence in Si and SiC vertical power MOSFETs.

2.1.2 Device Preparation

Each die was polished until the backside metalization was completely removed, minimizing the reduction in SiC die thickness while still exposing bare SiC. All dies were mounted using

silver epoxy into modified high-speed ceramic DIP40 packages with a hole drilled in to the package to expose a portion of the SiC for backside laser testing. The hole is sized to expose approximately 30% of the backside, which results in insignificant modification to the electric fields with bias compared to an unaltered die [9]. Gold bond wires connect the gate and source/body contacts to package pins, and the exposed die and bond wires were then coated in HumiSeal 1A33 and allowed to cure to ensure safe operation of the device at biases over 100 V [24]. The drain contact is on the backside of the device and is attached directly to a package contact using silver epoxy, effectively re-metalizing a portion of the drain. Each device underwent both forward and reverse biased current-voltage (IV) sweeps after packaging to verify normal operation.

2.1.3 Two-Photon Absorption Technique for SiC Devices

Pulsed-laser TPA testing was conducted using Vanderbilt's tunable wavelength focused laser facility. For 4H SiC, which has a larger bandgap than Si (3.2-3.3 eV), the maximum wavelengths able to generate electron-hole pairs from single-photon and double-photon absorption are 375 nm and 650 nm, respectively. The laser was tuned to a wavelength of 481 nm, which equates to a photon energy of 2.58 eV. This wavelength has been used to generate SEB in 4H SiC diodes in prior testing [10].

2.1.4 Printed Circuit

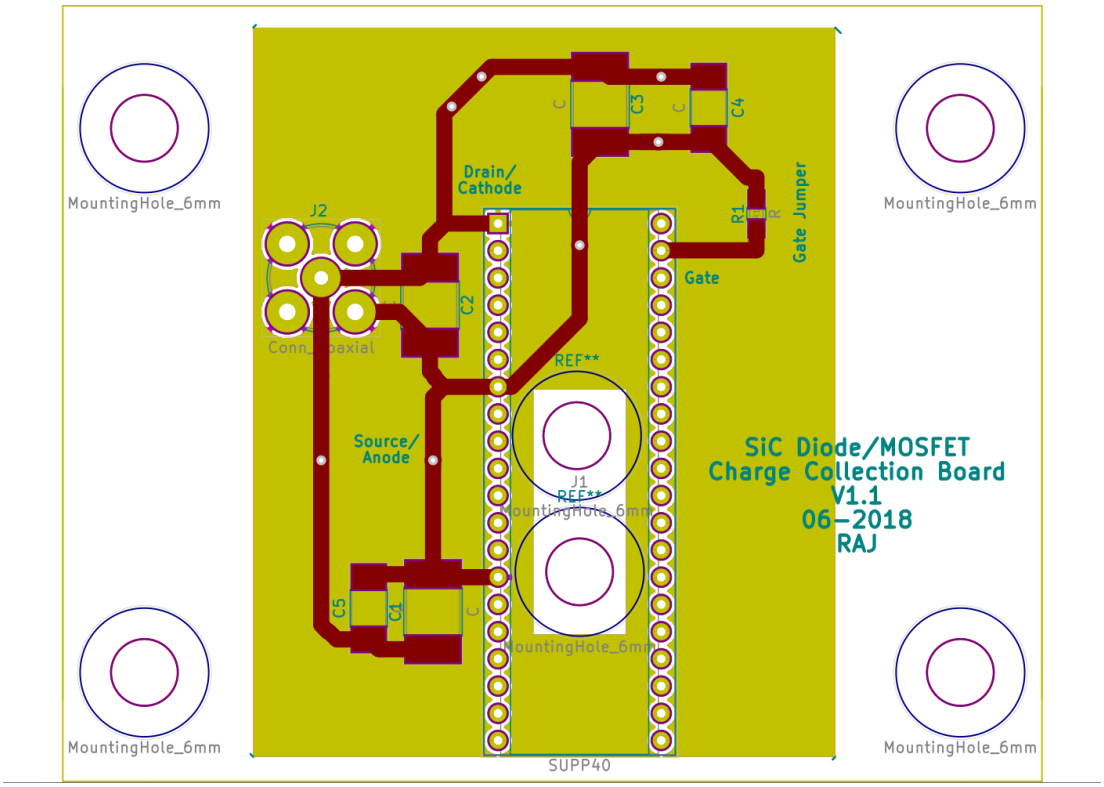
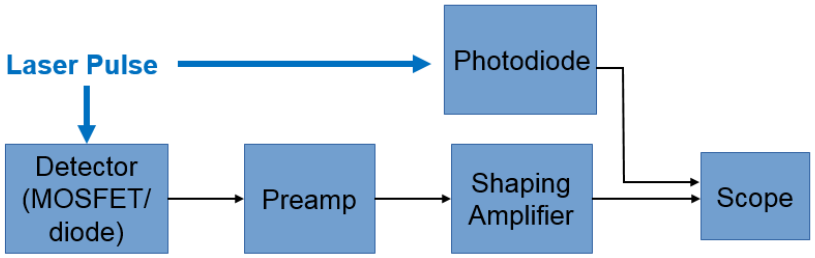
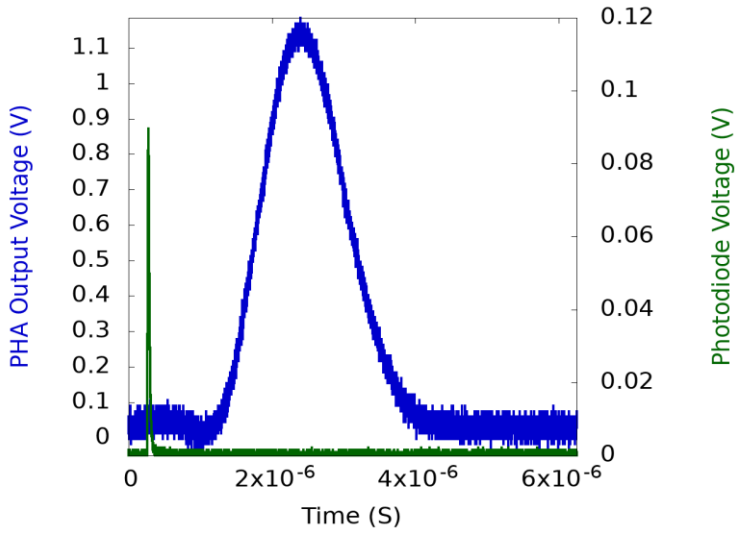


Fig. 6. PCB design for the test setup.

The board used for all tests is shown in Fig. 6. Initial charge collection measurement efforts utilizing bias tees and a CT-2 current probe to observe device waveforms were unable to produce sufficient signal over environmental and device noise at biases below 200 V, and above 200 V both MOSFETs and diodes exhibited laser-pulse induced leakage current degradation. Due to these factors, pulse height analysis was used to complete charge collection measurements.



(a)



(b)

Fig. 7. Fig. 7a provides a chart detailing the basic experimental setup and Fig. 7b. provides an example oscilloscope output.

Figure 7a shows a block diagram of the experimental setup used for charge collection measurements. This technique, known as pulse height analysis (PHA), is a well-established characterization method in nuclear spectroscopy and has been used for many years to measure charge-collection spectra from ionizing radiation events [25]. A device is exposed to a pulsed ionizing radiation source while biased and the resulting charge transient from a heavy ion or laser pulse is integrated by a FET amplifier within the preamplifier. This output pulse has an amplitude proportional to the charge collected by the biased device. The shaping amplifier provides additional signal processing to aid in isolating transient peaks. The output of the

shaping amplifier is then sent to an oscilloscope where it can be captured. The peak heights were converted to collected charge using the technique described in Reed, Mcnulty, and Beauvak *et al.* [25] and McNulty, Beauvais, and Roth *et al.* [26].

The photodiode is used to measure the pulse-to-pulse variation of the laser energy using the same oscilloscope as the output of the amplifier. The voltage generated by the photodiode has not been mapped quantitatively to energy values at the laser wavelength used, but the pulse energy is estimated to be on the order of nanojoules based on the efficiency of the photodiode. This measurement therefore is used exclusively for verifying consistency of laser pulse energies during each run as well as providing a relative measure of deposited energy per pulse between runs. Within individual test runs energy values remained fairly uniform, but drift in energy throughout test days varied by as much as 50%. Pulses were produced at a frequency of 1 kilohertz, yielding a total power dissipation of only microwatts in each sample due to the laser. Transients caused by laser pulses are isolated from noise by triggering the oscilloscope on pulses of the photodiode signal, which is shown in Fig. 7b.

The MOSFETs are biased with the gate and source attached to ground, and the diodes are reverse biased for all tests. The response to pulsed TPA was studied as a function of bias and position of the laser spot. The location of the laser focus is recorded for each laser pulse and resulting oscilloscope output trace. During voltage sweeps, a Keithley 2410 Source Measure Unit (SMU) provides bias and this bias is also recorded on each pulse [27]. The axis location of Z=0 was set to the SiC-metal interface of each device by finding the laser focus depth with the most concentrated reflections off of the metal as viewed through a backside camera. This method produced results within a few microns of the actual SiC-metal interface, an error which does present itself when comparing the results of multiple devices as discussed later. While able to

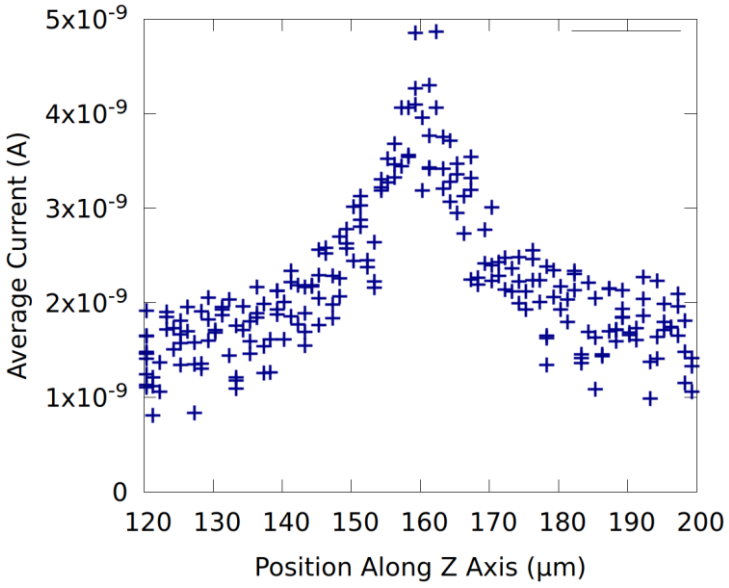
identify the striped structure of the MOSFET using both a frontside and backside camera, determining which stripes were associated with gate structures and which the spaces in between gate structures was not possible, necessitating later optical simulation to verify, as presented in section IV. Initial tests were performed to determine the locations of maximum charge collection in both the diode and MOSFET. Once these charge-collection maxima locations were found the voltage sweeps were run at these locations for each device.

2.2 Experimental Results

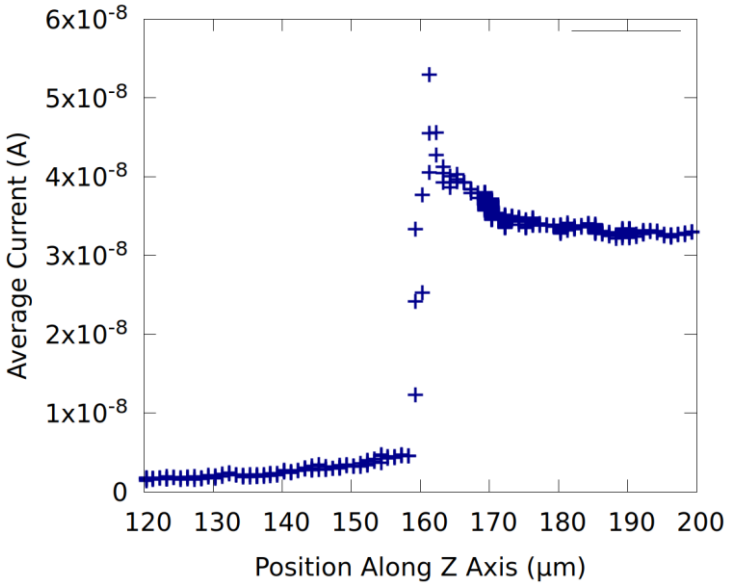
Devices were first tested with the leakage current measured directly, monitoring the current provided by the Keithley SMU. During these tests, both the diode and MOSFET demonstrated a maximum of current when sweeping vertically through the device, as shown in Fig. 8a, with a diode reverse biased at 200 V. If the laser was pulsed while a device was under sufficiently high bias, permanent leakage current degradation would occur, as shown in Fig. 8b, with the same diode reverse biased at 250 V. This degradation would partially anneal within a few minutes of developing, but never fully disappear. Due to this permanent effect, pulse-height analysis results are used for the remainder of the paper, as that method better isolates collected charge pulses from sustained increases in leakage current.

Lateral sweeps (x-axis in Fig. 5c) of laser focus through the diode yielded insignificant variation in collected charge at a constant reverse bias and laser energy, as shown in Fig. 9. Figure 10 presents a similar sweep in the MOSFET, where there is a periodic response with position. The period of the output is approximately 10 μm, which is consistent with the pitch of the gates within the MOSFET. These data suggest that the variation in structure in the MOSFET causes spatial variability in charge collection, but it was not possible to correlate the details of

the device structure with peaks and troughs. We accomplish this by comparing the response of the diode to the MOSFET (described next).



(a)



(b)

Fig. 8. Average current during a laser pulses while sweeping across a diode. At a 200 V bias (a) no leakage current degradation occurs, however when increasing the bias to 250 V (b) there is a step increase in leakage current that the device does not entirely recover from. The z axis is defined in Fig. 5c.

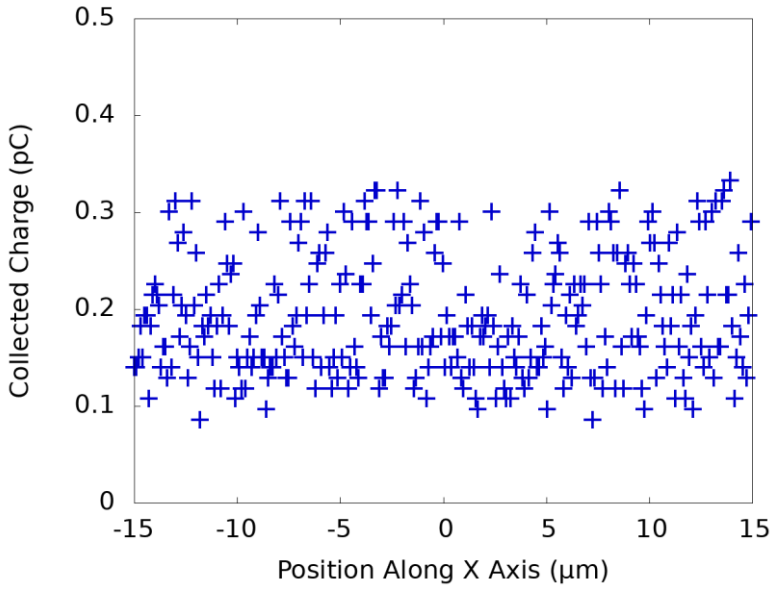


Fig. 9. Collected charge with a sweep of laser focus along the X axis in the diode. The diode was reverse biased at 50V.

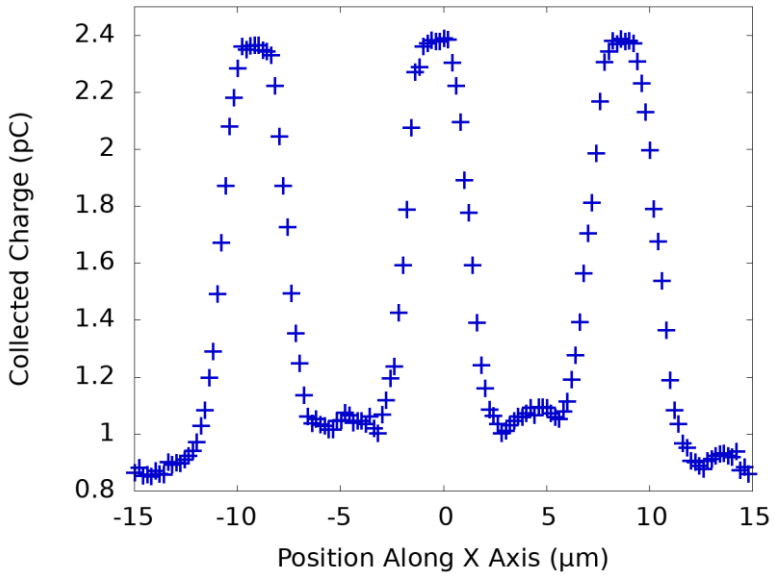
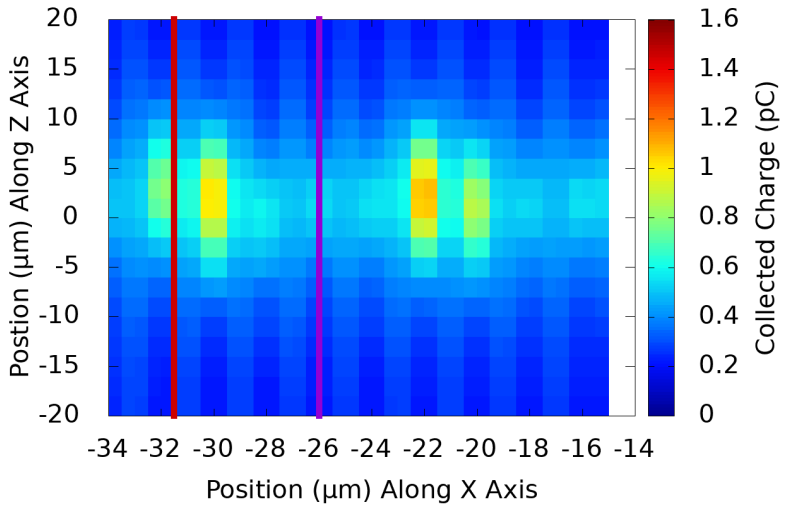
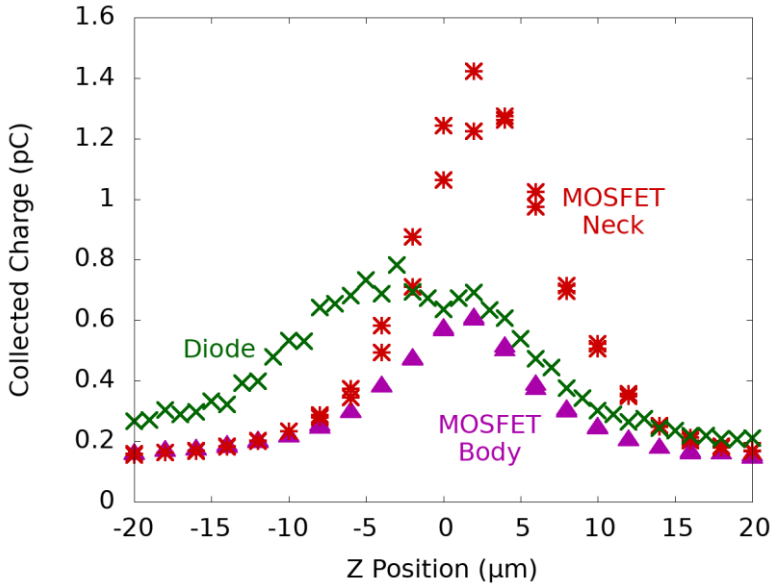


Fig. 10. Collected charge with a sweep of laser focus along X axis (across structures) in the MOSFET. Periodicity is the same as the observed pitch of device structures. The MOSFET was reverse-biased at 50V with the gate and source contacts grounded.



(a)



(b)

Fig. 11. Fig 11a shows collected charge with a cross section sweep of laser focus along X and Z axes (across device structures and vertically) in the MOSFET. Fig. 11b shows stripes in the Z axis taken from the data in Fig. 11a at peaks and troughs along the X axis, as well as a sweep of the diode along the Z axis. The lines shown in Fig. 5a are where the data stripes in Fig. 11b are taken. Data was acquired with the MOSFET and diode reverse-biased at 50V.

The diode structure (including the metal) is most similar to the region of the MOSFET

underneath the source/metal contact (e.g., compare the left most region in Fig. 1a to that in Fig. 1b), and consequently the charge-collection response to a laser sweep perpendicular to the top surface of the die (z-direction as shown in Fig 1c) will be similar for the two devices in this region, enabling correlation of the peaks and troughs in Fig. 10 to physical structures of the MOSFET.

Figure 11a shows a mapping of the collected charge for the MOSFET over two directions; the x-axis is perpendicular to the metal strips and z-axis is perpendicular to the top surface of the device; there are two device structures shown in this figure. Next, these data are sampled at two locations: x = -32 μm and x = -26 μm, indicated by the vertical lines in Fig. 11a and plotted in Fig. 5b. A vertical sweep in the diode is also plotted in Fig 11b. The distribution and amplitude of collected charge in the diode is very similar to that of the trough of the MOSFET in both distribution and amplitude. There is greater similarity in distribution between the two measurements within the MOSFET, however this is due to the limited accuracy of the method for setting z = 0, which only presents itself when comparing test results from multiple devices rather than within a device. From this data we conclude that the troughs occur under the shared source and body contacts of the MOSFET and the peaks occur under the gate-neck region.

Figure 12 contains a plot of charge collection as a function of reverse bias voltage for both the MOSFET and diode focused at respective positional charge maxima; the MOSFET data are collected with the laser is focused at the gate-neck region, i.e., the location where charge amplification is expected. In order to prevent saturation of the PHA system when operating up to 300 V, the laser energy was reduced below the energy of the pulses for positional sweeps at a 50 V bias. The diode's response appears to follow a square root rule, which is expected. The MOSFET's response tracks the diode's response from 0 V up to 30 V, then appears to maintain a

roughly linear relation. We will discuss this result in more detail in the discussion section.

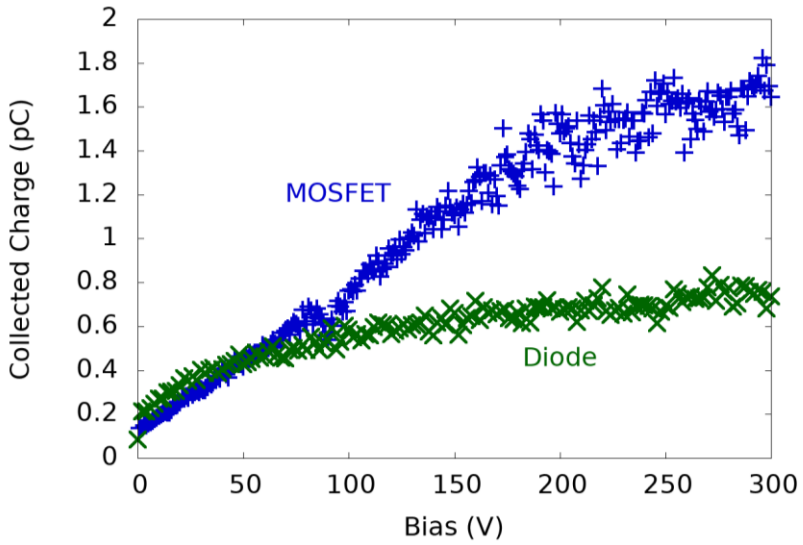


Fig. 12. Diode and MOSFET collected charge at reverse-biases between 0 and 300V. Due to variations in laser pulse energy throughout the day the diode received pulses with a similar distribution but 20% greater than the MOSFET, explaining the region between 0-60V where the diode collected charge is greater than the MOSFET.

3 Optical Simulations of Two Photon Absorption in SiC

As discussed previously, charge collection in the MOSFET structure was considered in two regions: underneath the source and underneath the gate. Nominally, these structures are differentiated by the location of the metal contact relative to the SiC bulk, with the source region being a SiC/metal contact interface and the gate region having a polysilicon layer between the SiC and metal contact (see Fig. 5). In order to better elucidate the charge-collection mechanisms of the device, the role of material interfaces and reflections on the optical generation of carriers should be considered when comparing charge collection from the two regions.

Optical simulations were performed by Ryder *et al.* [28] using Lumerical FDTD Solutions, a 3-D commercial nanophotonic software package [29], to calculate the optically generated carrier

distribution from a laser pulse. Two structures were simulated for evaluation of interfacial reflections and the implication for charge generation: a bulk SiC layer with a metal interface, similar to a VDMOS source structure, and a bulk SiC layer with a polysilicon layer between the metal contact, similar to a VDMOS gate structure. The laser was focused at the interface of the SiC and the adjacent material, corresponding to a Z position of zero in the experimental results. Simulations were conducted with an operating wavelength of 481 nm. For an overfilled objective at this wavelength, Lumerical calculates a spot size with a full width half max diameter of 494 nm [30], [31]. Values for the complex refractive index of polysilicon ($n_{Poly\text{-}Si}$ = 4.42+.086i), the complex refractive index of SiC (n_{SiC} = 2.69), and the TPA coefficient of SiC (β_{SiC} = 10cm/GW) were taken from [26], [30], [31].

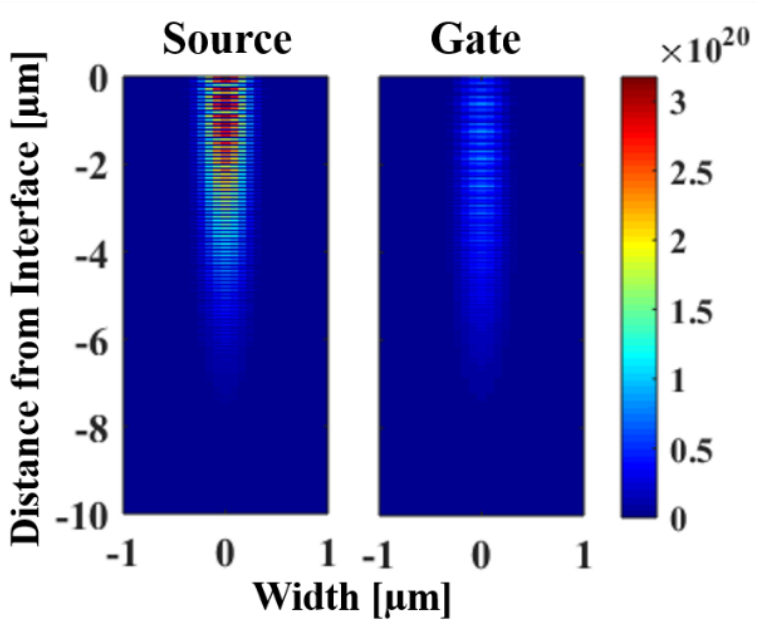


Fig. 13. Cross-section of optically generated carriers in SiC for bulk SiC with a metal contact (Source/Body) and bulk SiC with a polysilicon layer and metal contact (Gate) regions. In both simulations the interface between SiC and adjacent materials is defined at the zero line. The laser pulse propagates from the bottom and is focused at the interface.

For the stated refractive index values, the Fresnel reflection coefficient for the SiC/polysilicon interface indicates that <6% of the light incident on the interface is reflected back into the SiC. Due to significant absorption of light in the polysilicon, <1% of the light transmitted through the SiC/polysilicon interface will return to the SiC region after reflection from the metal contact. Hence, light that is not initially reflected at the SiC/polysilicon interface is almost completely absorbed by the polysilicon and does not significantly contribute to optical charge generation in the SiC. Accordingly, because the intensity of light reflected from the SiC/polysilicon interface is much lower than that reflected from the SiC/metal contact interface, there will be less optically generated charge in the SiC/polysilicon/metal contact structure (gate) than in the SiC/metal contact structure (source). The simulated spatial distribution of optically generated carriers in the SiC layer is shown in Fig. 13 for the source and gate regions under the same illumination conditions. Consistent with the aforementioned discussion, the optical carrier generation in the source region is larger than in the gate region. Furthermore, the spatial distribution shape affirms that reflections from the metal contact and etalon effects from the polysilicon layer in the gate structure are suppressed by absorption in the polysilicon. The full width half max diameter of the generated charge distribution is 355 nm.

The optical simulation results depicted in Fig. 13 are important for understanding the charge-collection mechanisms of the device by clarifying the impact of the material system on the optically generated charge. As seen most clearly in Fig. 5b, charge collection in the neck region below the gate is more than double the charge collection in the source and body at the SiC-metal interface. While not directly integrated with the TCAD simulations, the optical simulations demonstrate that the enhanced charge collection in the neck region is not due to enhanced optical generation from interfacial reflections.

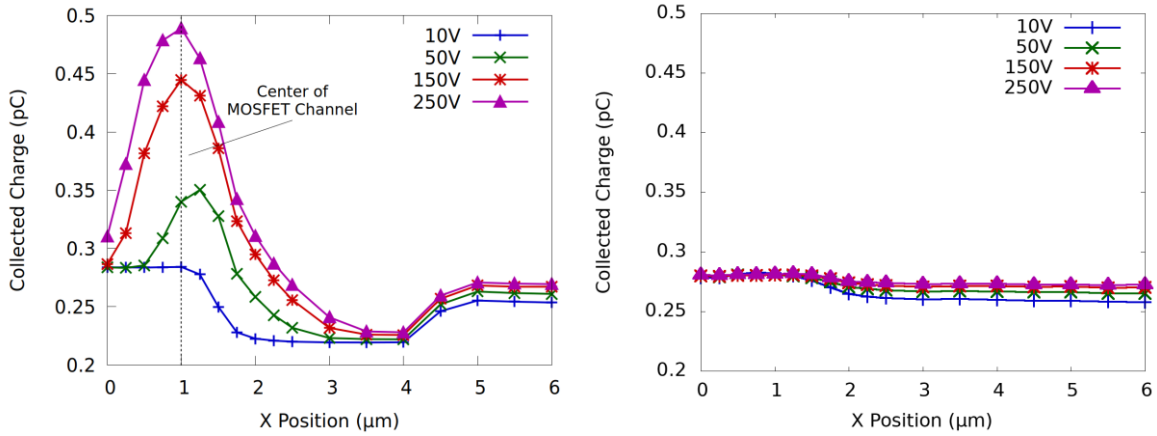
4 TCAD Simulations and Discussion of Results

Previous TCAD simulations of the MOSFET used in this study have shown a position dependence on the collected charge with ion strikes at bias voltages high enough to induce SEB in hardware testing [20]. If there are sufficient carriers generated in the body to forward-bias the body/source junction, holes begin to flow into the source, forming a base current for the BJT. Simulations were only able to produce runaway associated with SEB if impact ionization was implemented in the MOSFET, indicating two complimentary charge amplification mechanisms. However, impact ionization was only seen in significant amounts at biases above 450V. At lower biases, changes in depletion region depth present in both the diode and MOSFET explain the variation in charge collection with bias in the diode (green curve), as seen in Fig. 12.

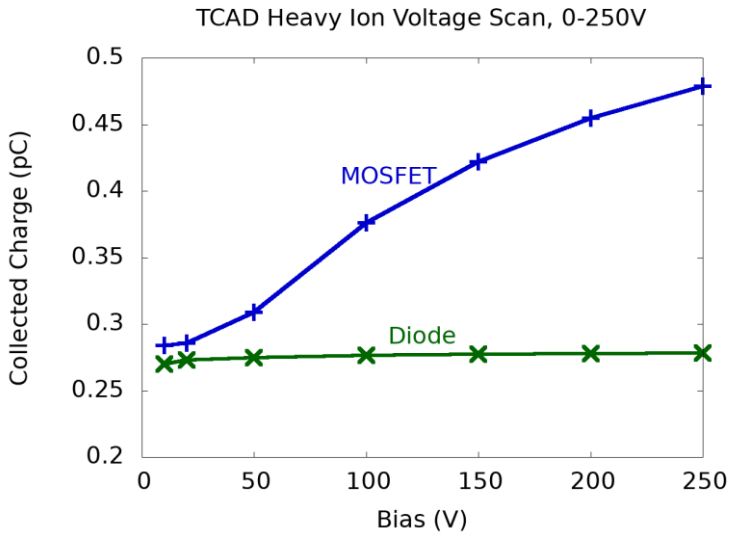
Given the similarity in structure, breakdown voltage, and doping of the diodes and MOSFETs tested, the effects of depletion depth variation on the charge collection from the laser events are expected to be similar for both device types and have little or no measurable positional dependence in either device. The amount of charge collected in the diode defines the portion of charge collected in the MOSFET due to carrier generation in the body-epi depletion region. If the BJT plays a significant role in charge collection for SiC MOSFETs, there should be evidence of charge amplification at bias voltages sufficiently large to activate the BJT during a laser strike for specific strike locations. Specifically, amplification should occur when carriers are generated in a MOSFET channel.

Figure 9 suggests this, but has limited detail due to the full width half max charge distribution diameter of 355 nm, which is approximately a third of the channel width of 1 µm. Rather than a peak charge collection centered in each channel with a slight dip in charge collection in the center of the neck between channels, the distributions around both channels are unavoidably

blurred across the neck, showing a single peak centered in each neck of each device stripe.



(a) (b)



(c)

Fig. 14. TCAD simulations of collected charge in a MOSFET for a constant amount of deposited charge but varying location and bias are shown in Fig. 14a. Fig. 14b shows TCAD simulations of collected charge in a diode for a constant amount of deposited charge but varying location and bias. For Figs. 14a and 14b, a strike location of 0 is at the center of the epitaxial region near the surface between two p-doped regions. Fig. 14c shows TCAD simulations of collected charge in a MOSFET and diode for a constant amount of deposited charge and constant location but varying bias.

Figure 14a shows 2D TCAD simulations using Synopsys Sentaurus [22] of collected charge

versus position and bias where x = 0 is centered in the MOSFET neck and also the MOSFET, x = 1 μm occurs in the channel, and x = 6 μm is in the body directly between two device gate stripes. These simulations used a deposited charge Gaussian diameter of 100 nm, or 28.2% of the TPA beam waist diameter and an ion LET of 10 MeV/cm. The charge is deposited in approximately the top micron of the device. Additionally, these simulations do not attempt to match the quantity of deposited charge using the laser but instead a reasonable approximation while also using a vastly smaller spot size and charge deposition depth in an effort to improve resolution of the results. Fig. 14b shows similar simulation results for the diode.

As shown in Fig. 14c, which uses data taken from Figs. 14a and 14b, the diode and MOSFET collect similar amounts of charge at biases below 20 V. Below 20 V there are insufficient injected charge carriers to produce a sufficient base emitter voltage in the parasitic bipolar transistor to saturate it. At higher biases, the bipolar transistor is turned on by the collected-charge induced voltage in the channel. In the experimental data shown in Fig. 12, the MOSFET and diode collected charge quantities start to differentiate at 60 V, never fully intersecting again with increased bias. Since the MOSFET tests are run with the laser focused just before the beam enters the gate polysilicon, compared to the diode tests, which are focused just before a relatively more reflective metal interface, the turn on for the bipolar turn-on occurs no higher than 60 V, where the collected charge is equal. Since the charge is all deposited closer to the surface of the device in TCAD simulations, there is minimal influence of bias on collected charge in the diode. This is due to the majority of the deposited charge fitting within the depletion region even at low biases, which is not the case for the experimental data. Positionally, bipolar gain results in a peak in charge collection when the charge generated in the channel is maximized for the MOSFET, while the diode has fairly constant charge collection at any carrier deposition location. It is more

likely that the critical concentration of charge carriers will be generated in the channel the closer the laser pulse focus is to the channel. However, once this critical concentration is reached, additional charge carriers are less significant for increased amplification than bias. This is seen in Fig. 14a with the widening of the peak with bias. With greater bias, more charge generation locations are able to produce approximately the same amount of collected charge.

As a final demonstration of parasitic bipolar amplification, we review similar charge collection measurements on the same MOSFET presented by Mizuta *et al*. [2]. The resulting charge collection distributions contain two primary maxima, indicating an additional charge collection mechanism on top of simple charge deposition by the ion track for this device. Fig. 15 replots the maximum collected charge values data from that paper as a function of bias for three different ion linear energy transfers (LET). (We note that the lower mode in the charge collection distribution did not depend on bias.) The horizontal lines represent the amount of charge generated in the epitaxial region for each ion LET. The maximum charge collected increases with bias for all three ion species used in that work, also the higher bias experiments show that more charge is collected than deposited. These effects were enhanced with increasing LET and increasing bias voltage.

As shown in Fig. 9, the diodes tested exhibited behavior consistent with the absence of charge carrier amplification dependent on position parallel to the SiC-metal interface of the device. However, MOSFETs demonstrated amplification dependent on laser focus position, seen in Fig. 10. For ion strikes of a constant LET, the only variable in strike conditions is the location of the strikes. Ions should all generate approximately the same charge in a device independent of strike location. If the resulting distribution of collected charge for all ion strikes contains multiple local maxima, there must be additional mechanisms that are only relevant for certain strike locations.

Therefore results of Fig. 15, imply a positionally dependent mechanism in the MOSFET during heavy ion testing, as the data contains two primary local maxima at every ion species and bias. Considering the similarity between the heavy ion data shown in [2], the TPA data shown in this work, and the TCAD simulation presented here and in [20], there is significant evidence that there are two charge collection mechanisms for these devices and that the experimental data are consistent with deposited carrier collection in the depletion region and amplification, as predicted by TCAD.

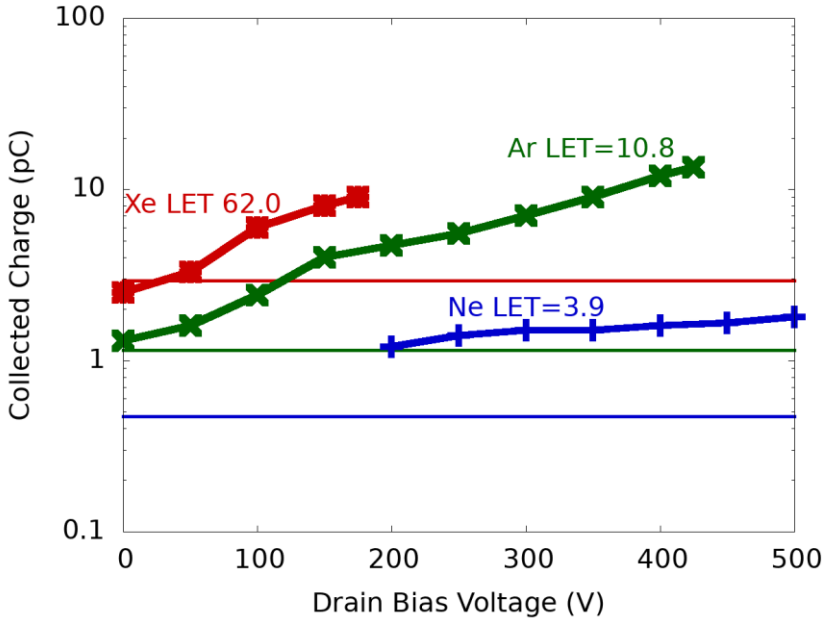


Fig. 15. Second peaks of collected charge as a function of the drain bias voltage below the bias voltage threshold for SEB [2] **as well as horizontal lines showing the calculated deposited charge for each ion using an epitaxial depth of 10 µm. A distribution of charge collection values was collected for each bias and ion species, and the points shown are the higher of the two most frequent collected charge bins in each distribution.**

5 SUMMARY

Two-photon backside laser testing has been used to identify the source of bias-dependent charge collection amplification with localized ionization in SiC power MOSFETs and SiC power diodes. Peaks in charge collection were seen with movement of the laser focus between power

MOSFET cells at a fixed depth. These peaks are not observed in similar measurements on SiC power diodes. Comparing the different responses of the diode and MOSFET, it is observed that when the laser is focused on the neck region of a MOSFET cell the greatest charge collection occurs. This agrees with prior simulated results [10]. The charge collection increases as the bias voltage increases, supporting results seen in earlier work using heavy ions [2]. We conclude that the parasitic bipolar amplification inherent in the vertical SiC power MOSFET structure is the cause of these phenomena and requires consideration when examining the mechanisms involved in the SEB in these devices.

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