Bias Instability, Radiation Effects, and Low-Frequency Noise in Semiconductor Devices

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CHAPTER 1 Introduction

For the past few decades, the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) has increased greatly after tremendously and aggressively scaling down the size. With the scaling, the transistor structures evolve from planar architecture to non-planar architecture, like fin field-effect transistors (FinFETs) [1]. FinFETs are compatible to the conventional planar CMOS process [2] and can suppress short channel effects [3, 4]. Fig. 1. 1 shows the development history of and new trends in MOSFETs with differing transistor structures and scaling stages [5].

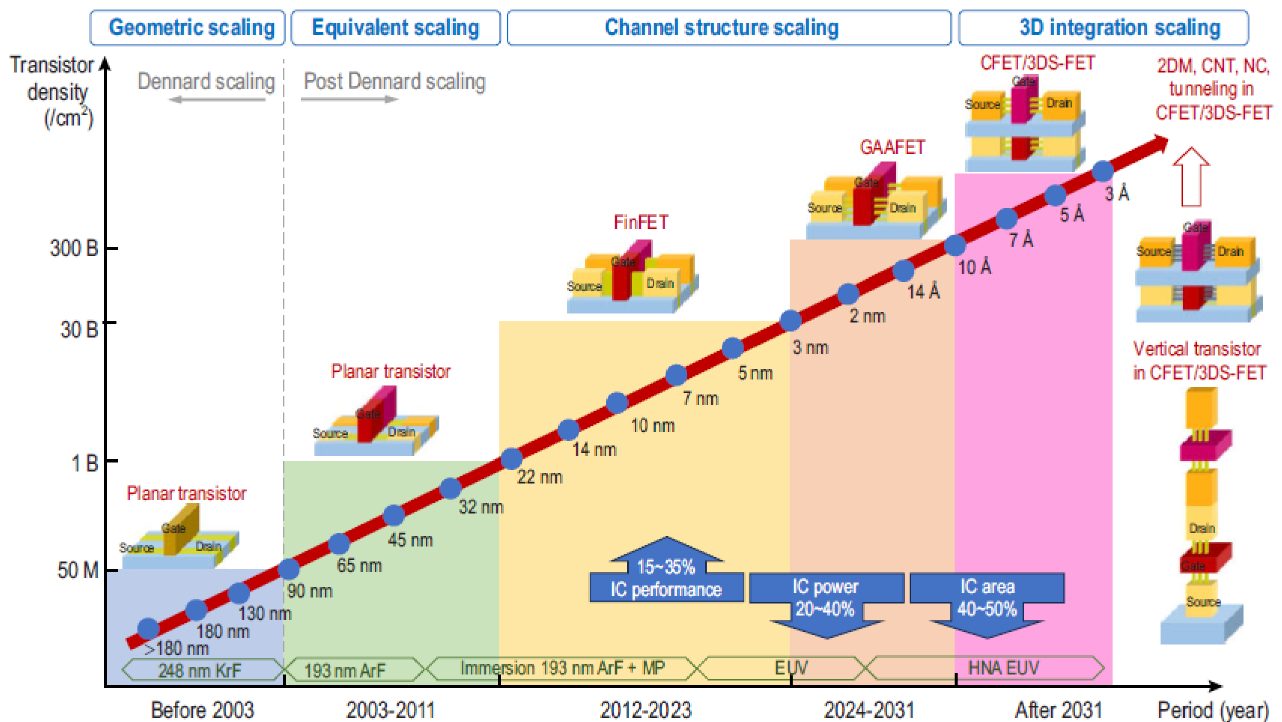

Fig. 1. 1 Development history of and new trends in MOSFETs with differing transistor structures and scaling stages. (After [5].)

As the scaling of silicon-based transistors has approached its physical limit, intensive efforts in finding alternative structures and channel materials have been made. For future logic devices beyond 10 nm node, the main effort is focused on Ge and III-V materials because of their superior carrier mobility [6]. The gate-all-around (GAA) nanowire structures [7] and novel two-dimensional

materials like graphene or transition metal dichalcogenides have also been considered [8].

As these devices have become more integrated and compact over time, ensuring their reliability has become a critical challenge. In modern CMOS technology, time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), and bias temperature instability (BTI) are three major reliability issues. BTI is largely caused by trapping and defect generation in the gate oxide [9-12]. It has been shown to adversely impact key device operating characteristics such as threshold voltage, drain current, and transconductance. BTI increases sharply with electric field and temperature, thus a primary reason for BTI concern is self-heating of modern MOS transistors during operation. For highly scaled *p*MOSFETs, negative BTI (NBTI) has been a more serious concern than positive BTI (PBTI) [9].

In microwave communications and radar systems, high-electron-mobility transistors (HEMTs) are widely used due to their efficiency and high-speed operation [13-15]. As HEMTs typically work under high voltage, hot electrons may be formed by the electric field between gate and drain contact. If the field is high enough, some hot electrons can overcome the conduction band discontinuity or, even cause impact ionization if their kinetic energy surpasses the bandgap. This effect will result in a degradation in gain and increase the ON resistance (R_{ON}), as well as cause a shift in threshold voltage [16-19]. The gain degradation and the increase of R_{ON} are due to the generation of surface traps in the SiN passivation layer between gate and drain. Thus, hot carrier effects are crucial for evaluating the reliability of HEMTs.

Radiation also poses a significant threat to the reliability and functionality of semiconductor devices, particularly in environments such as space or nuclear applications. The natural space

radiation environment originating from galactic cosmic rays (GCR), solar events, and particles trapped in the Earth's radiation belts can temporarily or permanently degrade the performance of electronic devices, circuits, and systems [20, 21].

Given the important concerns mentioned above, this dissertation investigates reliability issues in various semiconductor devices, including Ge *p*MOS FinFETs, GaAs pseudomorphic high-electron-mobility transistors (PHEMTs), and Si bipolar junction transistors (BJTs), with a focus on the effects of radiation and electrical stress. It aims to elucidate the underlying mechanisms of performance degradation and defect generation through low-frequency $1/f$ noise measurements. A more detailed introduction of this technique will be included in Chapter 2. This dissertation is organized as follows:

Chapter 2 gives a brief introduction of Ge-based FinFETs, HEMTs/PHEMTs, negative bias temperature instability, low-frequency noise and radiation effects in semiconductor devices. It is worth noting that the origin of low-frequency $1/f$ noise and its temperature dependence are discussed with an emphasis of the Dutta-Horn model, which enables the estimations of effective defect energy distributions.

Chapter 3 describes the negative bias temperature instabilities (NBTI) and low-frequency $1/f$ noise in strained Ge *p*MOS FinFETs. Ge *p*MOS FinFETs demonstrate negative bias temperature stress (NBTS)-induced interface-trap formation with activation energies lower than those typically seen in Si *p*MOSFETs. Low-frequency noise measurements above ~230 K detected newly created and/or activated border traps linked to oxygen vacancies and hydrogen, supporting earlier SiGe *p*MOS FinFET findings. The gate-voltage dependence of $1/f$ noise shows defect energy distributions

increasing toward midgap, contrasting with the trends towards the valence-band edge in previous *p*MOSFETs.

Chapter 4 evaluates the effects of electrical stress for industrial-quality AlGaAs/InGaAs/GaAs PHEMTs as a function of gate bias and temperature. A small positive shift of the threshold voltage V_{th} and negligible degradation in peak transconductance G_M were observed after the ON-state bias stressing, emphasizing the stability of these devices. Oxygen-related defects, isolated AsGa antisites and dopant-based DX centers may contribute significantly to the low-frequency 1/*f* noise in AlGaAs/InGaAs/GaAs PHEMTs.

Chapter 5 investigates the types of defects and resulting defect energy distributions before and after 17 MeV Si ion irradiation in 2N2222A *n-p-n* Si BJTs, through deep level transient spectroscopy (DLTS) and 1/*f* noise measurements. DLTS measurements identify three prominent classic defect levels in the bulk Si that are introduced by irradiation in the base-collector junction of these transistors. Temperature-dependent 1/*f* noise measurements identify at least two defect levels, one of which appears to be similar to levels identified via DLTS, and the other that is likely associated with oxygen vacancies and hydrogen complexes in the interfacial oxide layer that overlies the emitter-base (EB) junction.

Chapter 6 summarizes the conclusions of the dissertation.

CHAPTER 2 Background

2.1 Ge-based fin field-effect transistors

Germanium transistors exhibit several intrinsic properties that make them attractive for use in high-speed and low-power applications. The higher carrier mobility in germanium allows for faster switching times and better conductivity [22]. This is particularly advantageous for PMOS transistors, where the mobility of holes is a limiting factor in silicon devices. Despite their advantages, the integration of germanium into mainstream semiconductor manufacturing presents significant challenges. One of the primary issues is the formation of a high-quality, thermally stable gate oxide layer on germanium. Unlike silicon, germanium's natural oxide is volatile and water-soluble, which complicates the fabrication process [23, 24]. Furthermore, the integration of germanium with other materials commonly used in semiconductor manufacturing, such as silicon, can lead to defects due to lattice mismatch. Recent techniques such as surface passivation, high-k dielectric integration, and advanced gate stack engineering have shown promising results in improving the stability and performance of Ge FinFETs [25, 26]. Additionally, novel architectures like the Ge-on-insulator (GOI) platform are being explored to harness the benefits of germanium while mitigating the issues related to substrate interactions [27].

In 2013, imec reported the first functional strained germanium (sGe) quantum-well channel *p*MOS FinFETs, fabricated with a Si fin replacement process on 300 mm Si wafers [28]. It has already been proven to boost the channel mobility, and is also known for its excellent scalability potential, which is a possible evolution of the FinFET/trigate architecture for 7 nm and 5 nm CMOS technologies. The growth of compressively strained Ge channels on relaxed SiGe buffer and the use

of fin replacement process to fabricate the strained Ge channel devices make it especially attractive for co-integration with other devices on a common Si substrate.

2.2 High-electron-mobility transistors (HEMTs) and pseudomorphic HEMTs

Modulation doped AlGaAs/GaAs heterostructure was first reported by Bell Labs in 1978 [29]. By placing dopants in the middle of the AlGaAs layer, which reduces ionized impurity scattering, unprecedented mobilities were observed in the heterostructure [29]. At Fujistu, Mimura soon came up with the idea of using a single doped AlGaAs and undoped GaAs heterojunction to achieve field effect control of electron accumulation at the interface, and first released the high-electron-mobility transistors (HEMTs) in 1980 [30]. Since 1980, HEMTs have pushed the development of data communications by allowing the production of reliable high frequency, low noise amplifiers. GaN material system and oxide deposition techniques expanded the application of HEMTs into the high temperature and high power forefront of semiconductor technology [31].

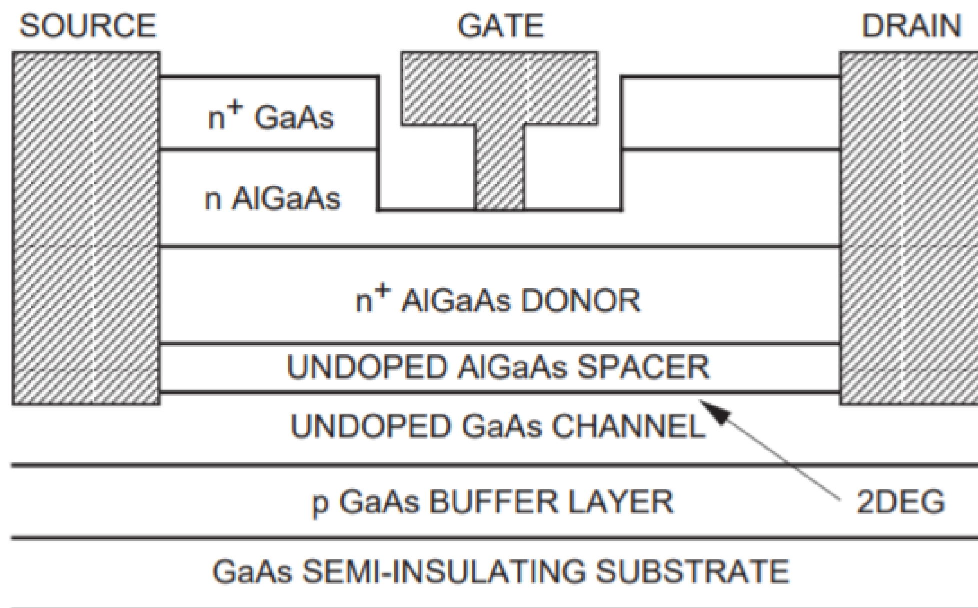

Fig. 2. 1 Epitaxial structure of a basic AlGaAs/GaAs HEMT. (After [32].)

HEMTs have been demonstrated in several material systems in the AlGaAs/GaAs and

AlGaN/GaN systems [33, 34]. The epitaxial structure of a AlGaAs/GaAs HEMT device is shown in Fig. 2. 1 [32]. The bandgap difference between $Al_xGa_{1-x}As$ and GaAs results in the formation of conduction and valence band discontinuities at the layer interface or heterojunction creating a quantum well in the conduction band. The wider band gap semiconductor ($Al_xGa_{1-x}As$), which has a band gap ranging from 1.42 eV to 2.16 eV, is doped with donors while the smaller band gap material (GaAs) is left undoped.

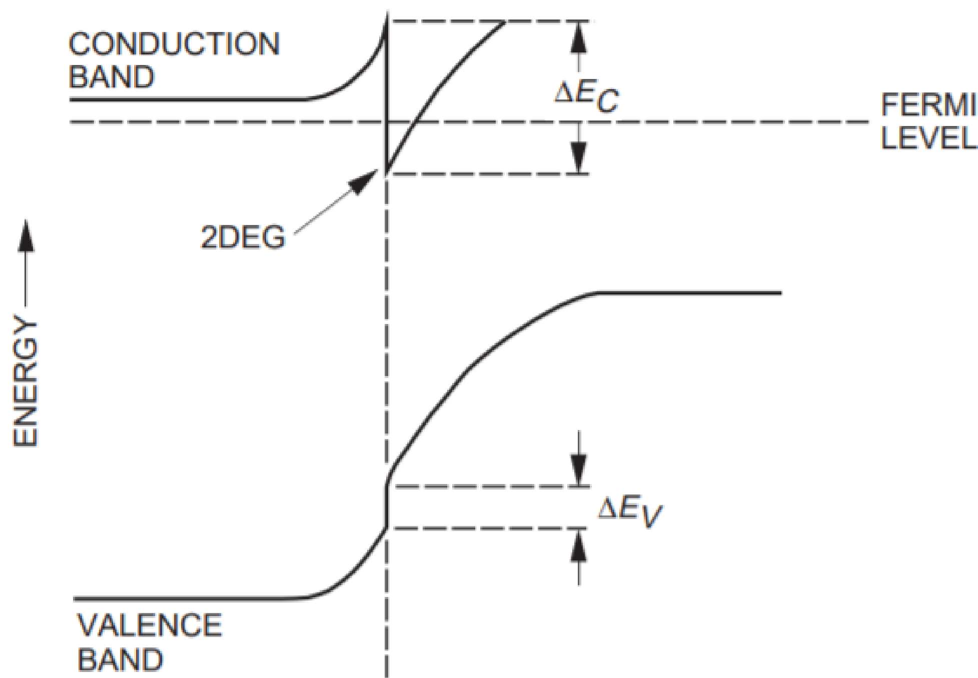

Fig. 2. 2 Band diagram of a basic AlGaAs/GaAs HEMT. (After [29].)

Illustrated in Fig. 2. 2 is the band diagram of a generic AlGaAs/GaAs HEMT showing the two-dimensional electron gas (2DEG) formed by the different band gaps. The conduction band electrons move from the higher band gap material ($Al_xGa_{1-x}As$) to the lower band gap material (GaAs) forming a 2DEG along the heterojunction. The band gap discontinuities are energy barriers spatially confining the electrons. In contrast to the MESFET, which has a doped channel and consequently lots of ionized donors, the 2DEG has significantly less Coulomb scattering, resulting in a very high

mobility device structure.

However, in the $Al_xGa_{1-x}As/GaAs$ system, conduction band discontinuity is limited by Al composition x to avoid DX center formation [35]. InGaAs has a lower band gap. Hence AlGaAs/InGaAs heterojunction can be used to achieve higher ΔE_C, 2DEG sheet density and modulation efficiency. Although InGaAs has a larger lattice constant than AlGaAs and GaAs, it can be grown "pseudomorphically" on a GaAs substrate without misfit dislocations as long as its thickness is less than a certain critical thickness, and this gave rise to pseudomorphic HEMTs (PHEMTs) [36]. Indium-rich materials also have higher intrinsic electron mobility and dominate high speed applications [13]. A GaAs PHEMT structure is shown in Fig. 2. 3 along with the associated band diagram. The conducting channel forms a 2DEG in the strained-layer InGaAs quantum well.

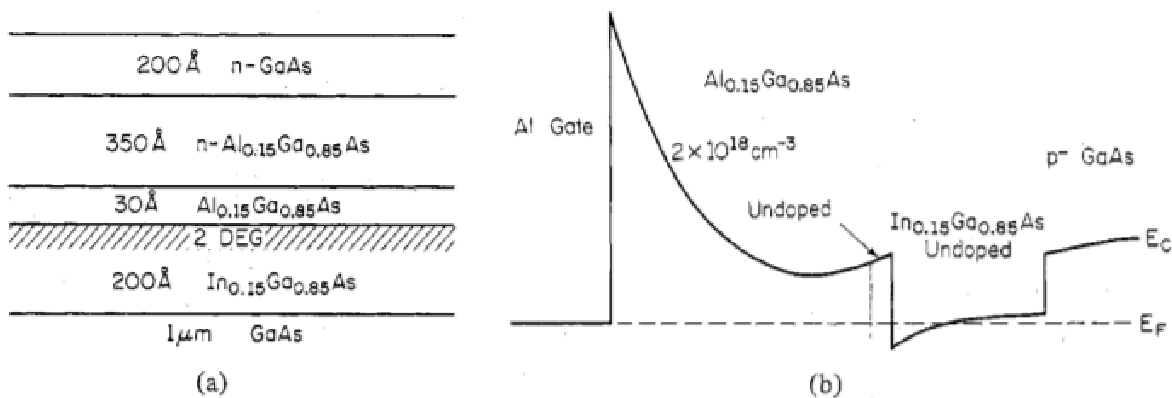

Fig. 2. 3 (a) and (b) Structure for a GaAs PHEMT and the associated conduction band diagram. (After [36].)

2.3 Negative bias temperature instability

Bias temperature instability (BTI) is a degradation phenomenon affecting mainly MOSFETs. The highest impact is observed in p-channel MOSFETs which are stressed with negative gate voltages at elevated temperatures. The stress conditions for this negative bias temperature instability

(NBTI) typically lie below 6MV/cm for the gate oxide electric field and temperatures ranging between 100 – 250℃ [37].

Although NBTI has been known for more than 50 years, the mechanism for NBTI is still under debate. NBTI has often been interpreted by some forms of reaction-diffusion (RD) model, as originally proposed in 1977 [38]. The RD model is diffusion controlled and assumes that Si-H bonds at the semiconductor/oxide interface are broken at higher temperatures and electric fields, causing some hydrogen species to be released from previously passivated interface defects and then dispersively diffuse into the oxide. However, some studies of NBTI [39, 40] find that interface-trap creation is not the sole source of degradation but a major hole trapping effect also occurs, especially when electric fields during NBTI stress approaches or exceeds ~ 10 MV/cm. Additionally, a large number of detailed recovery studies published in the last decade cannot be fully accounted for by the reaction-diffusion mechanism [40, 41]. In 2009 Grasser et al. developed a comprehensive quantitative two-stage model able to capture features [12], suggesting the degradation is due to interface trap generation and/or oxide charge buildup. The degradation is assumed to proceed in two coupled stages. For the first stage, the NBTI degradation process is initiated (state 1) when inversion layer hole capture occurs at an E' precursor site, e.g., a neutral oxygen vacancy. The hole capture leads to positively charged E' centers (paramagnetic defects observable with ESR) in the oxide, thereby creating a switching trap, as illustrated in Fig. 2. 4. Upon hole capture, the Si–Si bond breaks and a positively charged E'_{γ} center is created (state 2). Hole emission (electron capture) neutralizes the E'_{γ} center (state 3). Being in state 3, two options exist: a hole can be captured again, causing a transition to state 2, or the structure can relax back to its equilibrium configuration

(state 1). For the second stage, oxide silicon dangling bonds (E' centers) created in the stage one process trigger the creation of P_b centers via hydrogen exchange with a P_b center at the interface. ESR measurements further confirmed that E' centers are generated during NBTI stress and very quickly recover upon removal of the stress [39]. The E' defect density does not change during zero oxide bias at elevated temperature or negative oxide bias at room temperature. These observations support hole capture at an E' precursor site and the creation of interface traps.

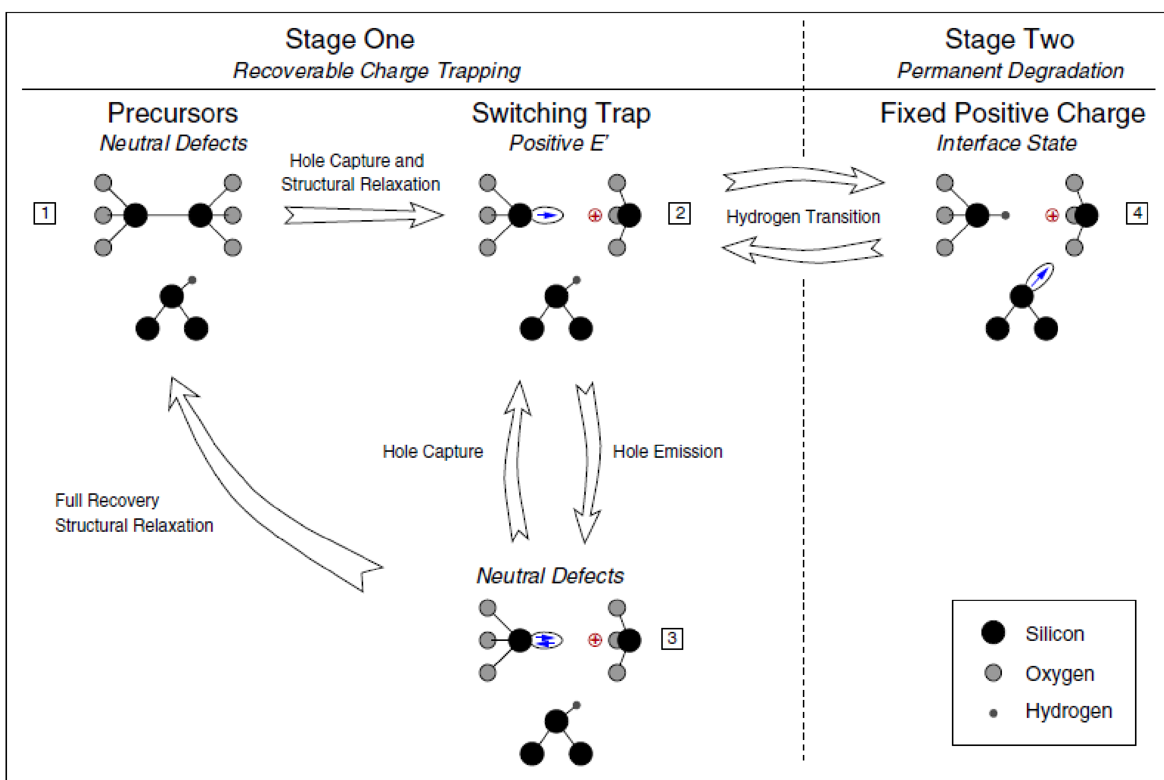

Fig. 2. 4 A two-stage model for negative bias temperature instability. (After [39].)

Recently Grasser et al. [42-44] have also included hydrogen related centers associated with NBTI. Complexes incorporating oxygen and hydrogen (e.g., the hydrogen bridge, which is a hydrogen atom at a dimer O vacancy in SiO_2) may also affect NBTI.

2.4 Low-frequency noise theory

Many physical systems exhibit fluctuations with spectral densities that vary approximately as low frequency (1/*f*) over a large range of frequencies. Several mechanisms generate noise in semiconductors leading to a unique spectral power distribution in the frequency domain. Of these sources, the noise behavior of bulk CMOS devices is dominated primarily by two noise sources: thermal noise [45, 46], low-frequency noise (1/*f* noise). Other sources present in the noise spectrum include shot noise [47, 48], generation/recombination (G-R) noise [49] and random telegraph noise (RTN) [50]. The noise magnitude of 1/*f* noise typically is found to be proportional to $1/f^{\alpha}$ (with α in the range of 0.7~1.3). Fig. 2. 5 shows a representative low-frequency noise in a Ge *p*MOS FinFET with high-K gate dielectric stack.

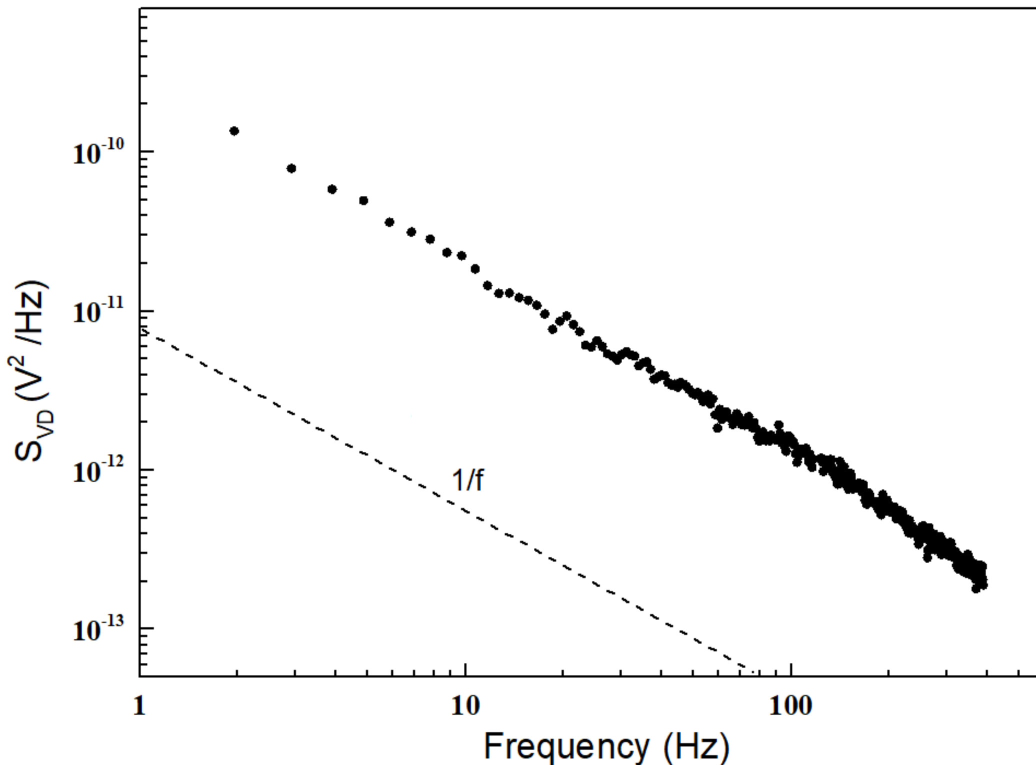

Fig. 2. 5 Excess voltage noise power spectral density S_{VD} (corrected for background noise) as a function of frequency for a Ge *p*MOS FinFET with high-K gate dielectric stack at room temperature. $V_{GS} - V_{th} = -0.4$ V, and $V_{DS} = -50$ mV.

In the past forty years, lots of work has been done to understand the links between low-frequency noise and defects in microelectronic materials and devices [49, 51-53]. The level of 1/*f* noise is a very useful parameter to evaluate the quality and reliability of devices. Although this noise is a nearly universal phenomenon in active devices, a variety of models have been proposed to explain 1/*f* noise in MOSFETs. Two popular models have appeared in the literature to explain the occurrence of flicker noise in MOSFETs: the McWhorter number fluctuation theory [54] and the Hooge mobility fluctuation theory [55].

It is generally accepted that the low-frequency noise in microelectronic material is caused by the fluctuation of carrier numbers resulted from the charge exchange between channel and defects, usually at or near semiconductor/insulator interface instead of mobility fluctuation [49]. The simplest version of this model assumes that trap centers are uniformly distributed near the channel, and that time constants increase with the distance from the channel. According to this model, if a MOS device is operated in its linear region at constant drain current and gate bias, the 1/*f* noise can be described approximately by [49]:

$$S_{Vd} = \frac{q^2}{C_{ox}^2}\frac{V_d^2}{(V_g-V_{th})^2}\frac{k_B T D_t(E_f)}{LWln(\tau_1/\tau_2)}\frac{1}{f} \tag{2.1}$$

where S_{Vd} is the excess drain-voltage noise power spectral density, V_{th}, V_g, and V_d are the threshold, gate, and drain voltages, f is the frequency, $-q$ is the electron charge, C_{ox} is the gate-oxide capacitance per unit area, L and W are the transistor channel length and width, k_B is the Boltzmann constant, T is the absolute temperature, $D_t(E_f)$ is the number of traps per unit energy per unit area at the Fermi level E_f, and τ_1 and τ_2 are the minimum and maximum tunneling times, respectively [56].

Dutta and Horn [57] proposed that the nearly 1/*f* spectrum in metals was due to a broad

distribution of activation energies. This theory was initially used to analyze the low frequency noise in thin metal film, and then extended well the responses of a wide variety of materials and several different types of semiconductor devices. They also demonstrated that, if the noise is the result of thermally activated processes involving two energy levels separated by an energy barrier of E_0 that the system must overcome for the system to move from one configurational state to another [51, 57], as shown in Fig. 2. 6. A single two-state system can be characterized by two energies: the energy difference between the states, ΔE, and the thermal activation energy for making the transition, E_0 or $E^{\pm}$, which is inferred from the temperature dependence of the noise.

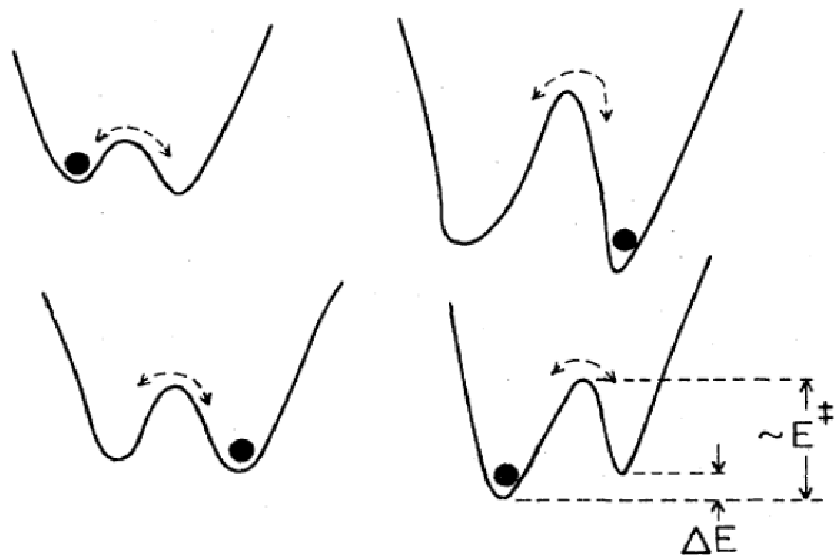

Fig. 2. 6 The distinction between the two energies: the energy difference between the states (ΔE) and thermal activation energy ($E^{\pm}$) for a two-level system in the classical regime. (After [51].)

They also have shown that, if the noise is caused by a random thermal-activated process that exhibits a broad distribution of energies $D(E_0)$ relative to kT, where k is the Boltzmann constant and T is the temperature, the frequency exponent shows a temperature dependence described by [49, 51, 57]:

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S_V(T)}{\partial \ln \mathrm{T}} - 1\right) \quad (2.2)$$

Here $\omega = 2\pi f$ and τ_0 is the characteristic time of the process leading to the noise. From measurements of the temperature dependence of S_V, we estimate the defect-energy distributions $D(E_0)$ [57], via

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T) . \tag{2.3}$$

Here the defect energy E_0 is given by [25], [26]:

$$E_0 \approx -kT \ln(\omega\tau_0) \tag{2.4}$$

In this work, the excess noise (corrected for background noise) in Ge FinFETs and GaAs PHEMTs was measured over a frequency span of 3 Hz to 390 Hz at a constant drain voltage supplied by a HP 4140B voltage supply with substrate and source grounded. The drain current was derived from a constant voltage source in series with a large resistor. Fluctuations in the drain to source voltage were measured with a low noise pre-amplifier SR 560 and SR 760 FFT spectrum analyzer. The electrical connection for low-frequency noise measurement is illustrated in Fig. 2. 7.

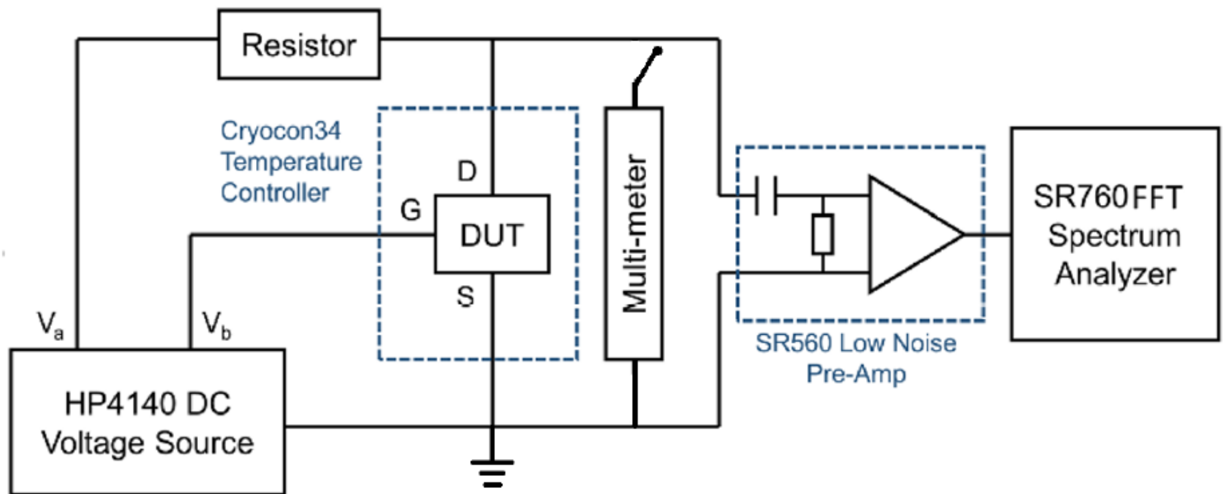

Fig. 2. 7 A typical low-frequency 1/*f* noise measurement system for MOSFETs. (After [58].)

The low-frequency 1/f noise in BJTs was measured using the experimental system shown in Fig. 2. 8. The devices under test (DUTs) were biased in a common-emitter configuration [59]. HP 4156A/B supplied the base current biasing. A low-noise metal film resistor R_L (typically several kΩ) was placed in series with the collector. The collector bias was chosen to operate the device in the active region, approximating realistic circuit operating conditions, and was supplied by a HP 4140B primarily for its convenience in control with our existing setup. The noise signal of the voltage power spectral density S_{VC} from the collector biasing resistance R_L was amplified by a SR560 operated in the differential mode, and then measured with a SR760 FFT spectrum analyzer at a constant I_B at frequencies from 3 Hz to 390 Hz. Base current fluctuations S_{IB} led to voltage noise S_{VC}; these were extracted via the relation $S_{IB} = \frac{S_{VC}}{R_L^2\beta^2}$, where β is the current gain [59-64].

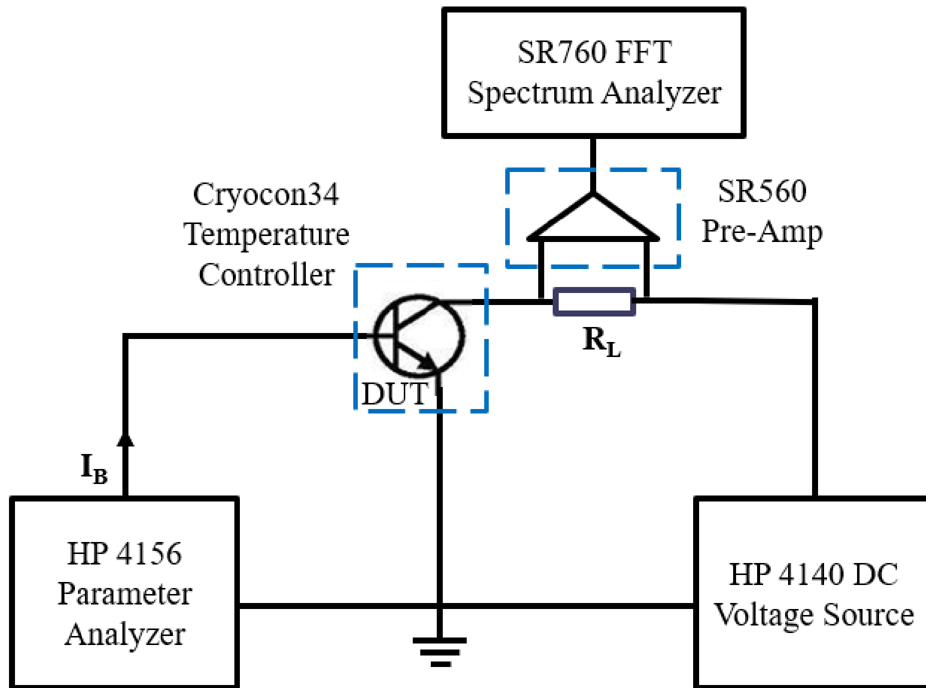

Fig. 2. 8 A typical low-frequency 1/f noise measurement system for BJTs.

There is very little dependency of the noise spectra on the collector voltage when the device was operated in the active region. Fig. 2. 9 shows the current-noise power spectral density, S_{IB} vs. f

at $I_B = 1$ μA for a typical 2N2222A *n-p-n* Si BJT, with the collector bias set at 1 V and 3 V. β of the DUT in the common-emitter mode was 172 and R_L was 1 kΩ. Therefore, the noise measurements were not sensitive to the collector bias we chose, when the device was operated in the active region.

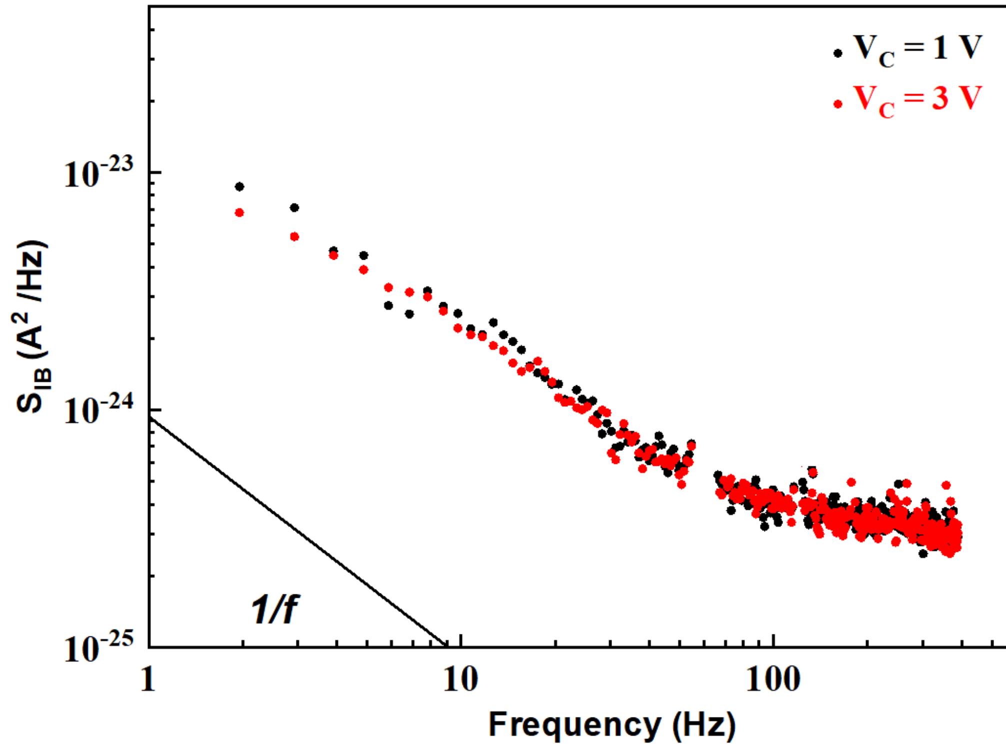

Fig. 2. 9 The comparison of current-noise power spectral density, S_{IB} vs. f at $I_B = 1$ μA for a typical 2N2222A *n-p-n* Si BJT, with the collector bias set at 1 V and 3 V. Unwanted spikes from 60-Hz pickup and harmonics are removed.

2.5 Radiation effects

Radiation-induced effects in electronics can be generally grouped into three types: Single Event Effects (SEEs), Total-ionizing-Dose (TID) effects, and Displacement Damage (DD) [65]. SEEs occur when high energy particles pass through the sensitive regions in semiconductor devices, and the energy would be lost to create electron-hole pairs through Coulomb scattering. The TID effect is the cumulative damage caused by ionizing radiation over the exposure time. It can cause long-term degradation in the gate/field oxides due to the formation of oxide/interface charge near the active region of the electronic devices [65, 66]. DD results from the non-ionizing process when energetic

particles, such as protons, electrons, neutrons and heavy ions, incident on the semiconductor, displace atoms from their original lattice sites, creating vacancies and interstitials [67]. The combination of a vacancy and an adjacent interstitial is known as a close pair or a Frenkel pair. Fig. 2. 8 shows the spatial distribution of the initial vacancy-interstitial pairs for the example of proton irradiated Si [67, 68].

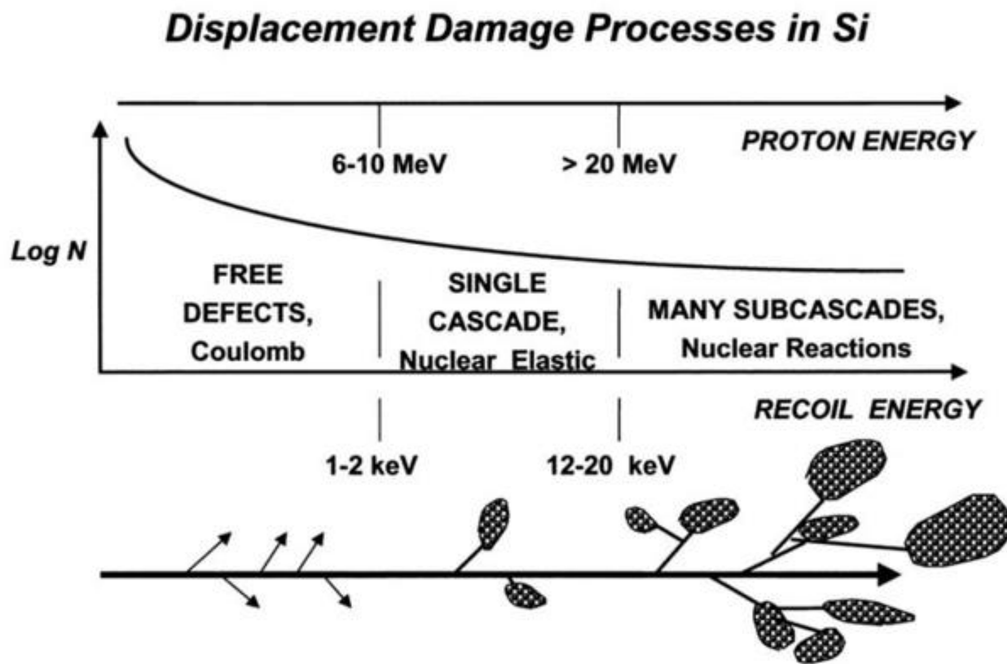

Fig. 2. 10 Spatial distribution of the initial defect configuration to the primary knock-on atom energy in Si material. (After [68].)

The vacancies and interstitials introduce allowable energy states in the band gap of a semiconductor material. For example, in bipolar transistors, DD creates bulk traps in the material. These traps increase carrier recombination in a forward biased junction (e.g. the base-emitter junction in active operation), which increases base current and may lead to a current gain reduction.

CHAPTER 3 Negative Bias-Temperature Instabilities and Low-Frequency Noise in Ge FinFETs

This chapter is adapted from "Negative Bias-Temperature Instabilities and Low-Frequency Noise in Ge FinFETs" published in IEEE Transactions on Device and Materials Reliability, and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Peng Fei Wang, Kan Li, Dimitri Linten, Jerome Mitard, Robert A. Reed, Daniel M. Fleetwood, and Ronald D. Schrimpf.

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3.1 Introduction

FinFETs are commonly used in highly scaled integrated circuits (ICs) due to enhanced electrostatic control compared to planar devices [4, 69, 70]. Further transistor scaling may replace silicon (Si) with higher mobility channel materials, including germanium (Ge) for p-type channels and III–V compounds for n-type channels [71, 72]. The higher carrier mobility offered by materials such as SiGe/Ge [73-75] can provide higher drive current than similar Si devices, enhancing the performance of future devices [73-76].

Negative-bias-temperature instability (NBTI) degradation has emerged as one of the most serious reliability issues for *p*MOSFETs with technology scaling [11, 28, 77]. Incorporating Ge into the channel can improve NBTI reliability [78-80]. This improvement has been found to be a process and architecture-independent property of Ge channel devices [81]. The NBTI reduction has been ascribed primarily to a favorable alignment shift of the Fermi level in the Ge-based channel with respect to defect energy levels in dielectric layers, which can reduce carrier-defect interactions [81]. The NBTI responses of SiGe planar and FinFETs and Ge gate-all-around (GAA) nanowire *p*FETs

also have been evaluated in several studies [82-87]. For SiGe FinFETs, a broad study of NBTI has been reported that focuses on the impact of Ge concentration, fin width, and orientation, and interface passivation by high pressure annealing [84].

In this work, we explore the NBTI response of strained Ge *p*MOS FinFETs. The Ge *p*MOS FinFET NBTI response varies less with temperature (corresponding to a smaller activation energy) than that of Si *p*MOS FinFETs [86]. $1/f$ noise measurements are utilized to provide insight into the density and energy distributions of defects [49, 57, 88-90]. We employ gate–voltage dependence and temperature dependence measurements of the $1/f$ noise to identify prominent traps before and after negative-bias-temperature stress. These defects are most likely oxygen vacancies and hydrogen-related defects in the SiO_2 and HfO_2 layers.

3.2 Experimental Details

The Ge *p*MOS FinFETs evaluated in this work were fabricated at imec on 300 mm bulk Si (100) wafers [25, 28]. The original n-type Si fin was replaced by a $Si_{0.25}Ge_{0.75}$ buffer. Strained Ge-channels were grown on relaxed $Si_{0.25}Ge_{0.75}$. A thin Si cap was partially oxidized, yielding an unconsumed thin Si buffer layer to passivate the Ge surface and improve the interface quality. On top of the SiO_2 interfacial layer (IL), a ~1.5 nm HfO_2 layer and TiN metal gate were deposited. The effective oxide thickness (EOT) of the gate dielectric stack is ~1.9 nm [91]. Fig. 3.1 shows a scanning transmission electron microscope (STEM) image of the device. All tested devices have 4 fins with gate length of 66 nm, fin width of 30 nm, and fin height of 15 nm.

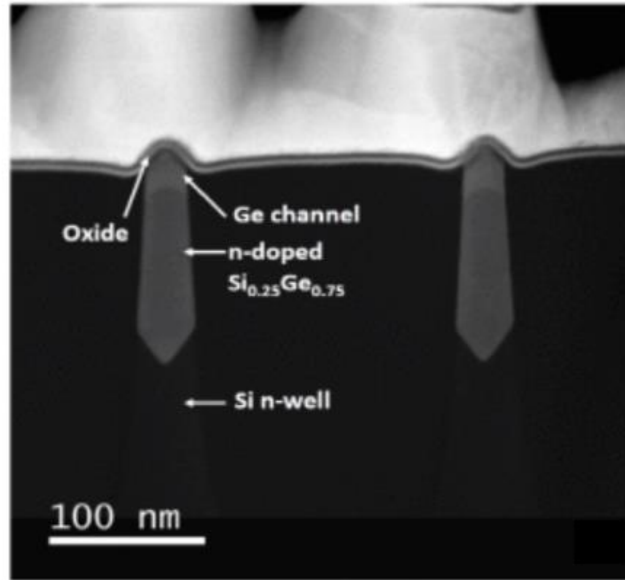

Fig. 3. 1 STEM cross-section of a Ge *p*MOS FinFET. The gate stack consists of a Si buffer layer, SiO_2/HfO_2 dielectric, and TiN gate. (After [92].)

I_D-V_G transfer characteristics were measured with an Agilent 4156A/B semiconductor parameter analyzer at $V_{DS} = -50$ mV, using medium integration time. The threshold voltage V_{th} is extracted by calculating the x-intercept of the linear extrapolation of the I_D-V_G curve at its maximum first derivative and subtracting $V_{DS}/2$ [93]. The room temperature noise power spectral density S_{Vd} was measured for a frequency range from 2 Hz to 390 Hz with correction for background noise [49]. The drain voltage was −50 mV with the source and substrate grounded. The gate voltage varied from 0.2 V to 0.5 V below V_{th}.

3.3 Experimental Results

3.3.1 Current-voltage measurements

Fig. 3. 2 shows typical I_D-V_G characteristics for Ge *p*MOS FinFETs after different stress durations up to 3840 s at room temperature under gate biases $V_G = -1.5$ V, $V_G = -2$ V, and $V_G = -2.5$ V. I_G–V_G characteristics (not shown) were monitored at regular intervals to confirm that the high gate voltages did not compromise the integrity of the gate oxides. There is minimal stress-

induced degradation in Fig. 3. 2(a) at $V_G = -1.5$ V. The degradation is larger and builds up more quickly at higher gate voltages in Figs. 3. 2(b) and 3. 2(c). The negative shift in $V_{\rm th}$ is due primarily to hole trapping; the increase in subthreshold stretchout is due to the buildup of interface and/or border traps [52, 83, 94, 95].

Fig. 3. 3(a) plots absolute values of threshold voltage shifts for the data of Fig. 3. 2 as functions of stress time for gate voltages of −2 V and −2.5 V. These shifts are comparable in magnitude to those reported for SiGe FinFETs in [95]. Stress-induced transconductance (G_M) degradation is shown in Fig. 3. 3(b). The worst-case peak G_M degradation occurs at $V_G = -2.5$ V; the peak G_M decreases by ~28% after 64-min stress. This is consistent with the large shift in subthreshold swing SS (~60 mV/dec) in Fig. 3. 3(c). These changes in response are primarily due to scattering of channel carriers due to interface-trap generation [77, 94, 96]. This interface-trap formation occurs as result of hydrogen release, transport, and reactions at the Si/SiO_2 interface [44, 77, 97], as discussed in Section 3.4.

Contributions of interface traps and oxide trapped charge to the V_{th} shift can be separated via the subthreshold swing technique [98]; results are plotted in Fig. 3. 4(a) as a function of stress time at $V_G = -2.5$ V. The V_{th} shift is due mainly to interface traps (ΔN_{it}), with a small contribution from oxide trapped charge (ΔN_{ot}), similar to previous results in Ge GAA devices [87]. The time evolution of $|\Delta V_{th}|$ in Fig. 3. 3 can be described by power-law dependencies of $\sim t^{0.23}$ for $V_G = -2$ V and $\sim t^{0.21}$ for $V_G = -2.5$ V, as illustrated in Fig. 3. 4(b). Similar power-law dependences are often observed in previous studies of stress-induced defect generation in Si, SiGe, and Ge MOS devices [44, 76, 83, 87].

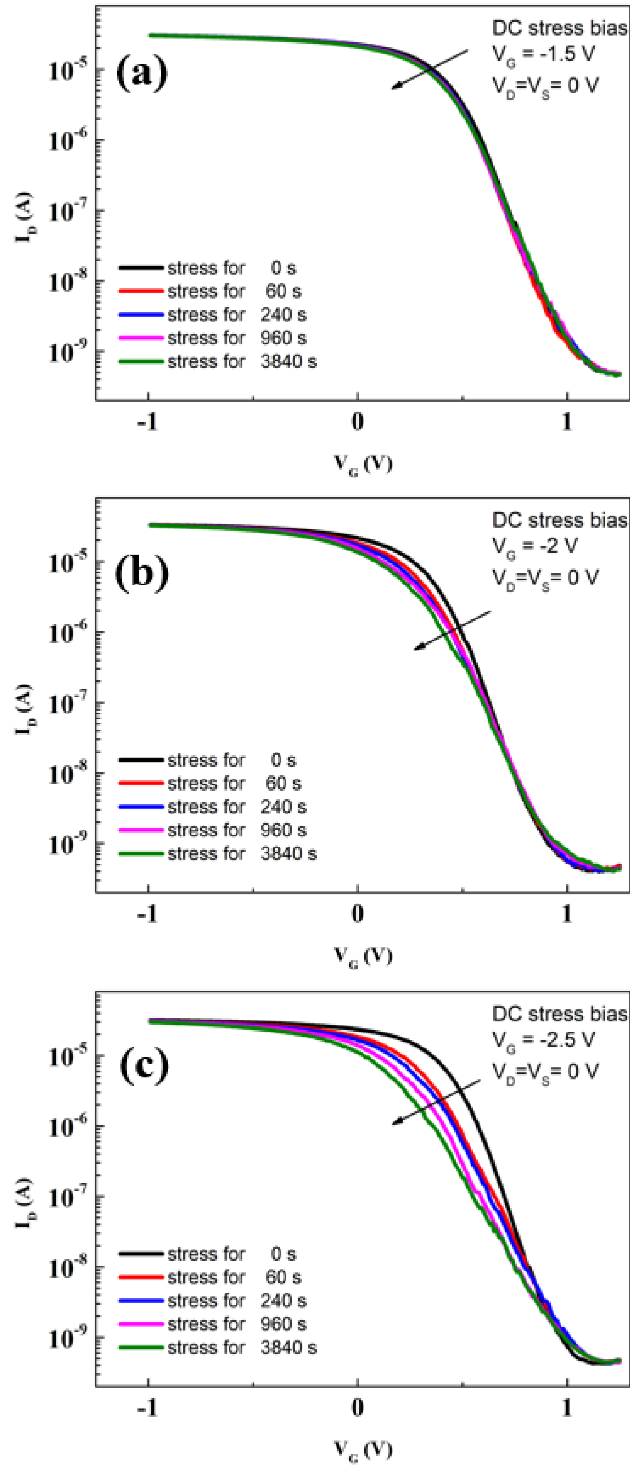

Fig. 3. 2 I_D-V_G characteristics measured at $V_{DS} = -50$ mV at different stress times. Devices with gate length of 66 nm, fin width of 30 nm, and fin height of 15 nm were stressed at (a) $V_G = -1.5$ V, (b) $V_G = -2$ V and (c) $V_G = -2.5$ V to capture representative NBTS degradation in drain current as a function of stress time. The drain, source and substrate were grounded when devices were stressed. The stress time is up to 3840 s (64 min). The small, abrupt changes in the slopes of curve result from charge-exchange with border traps and/or post-stress defect annealing. Similar steps in I_D-V_G curves of stressed devices measurements using medium or long integration time. (After [99].)

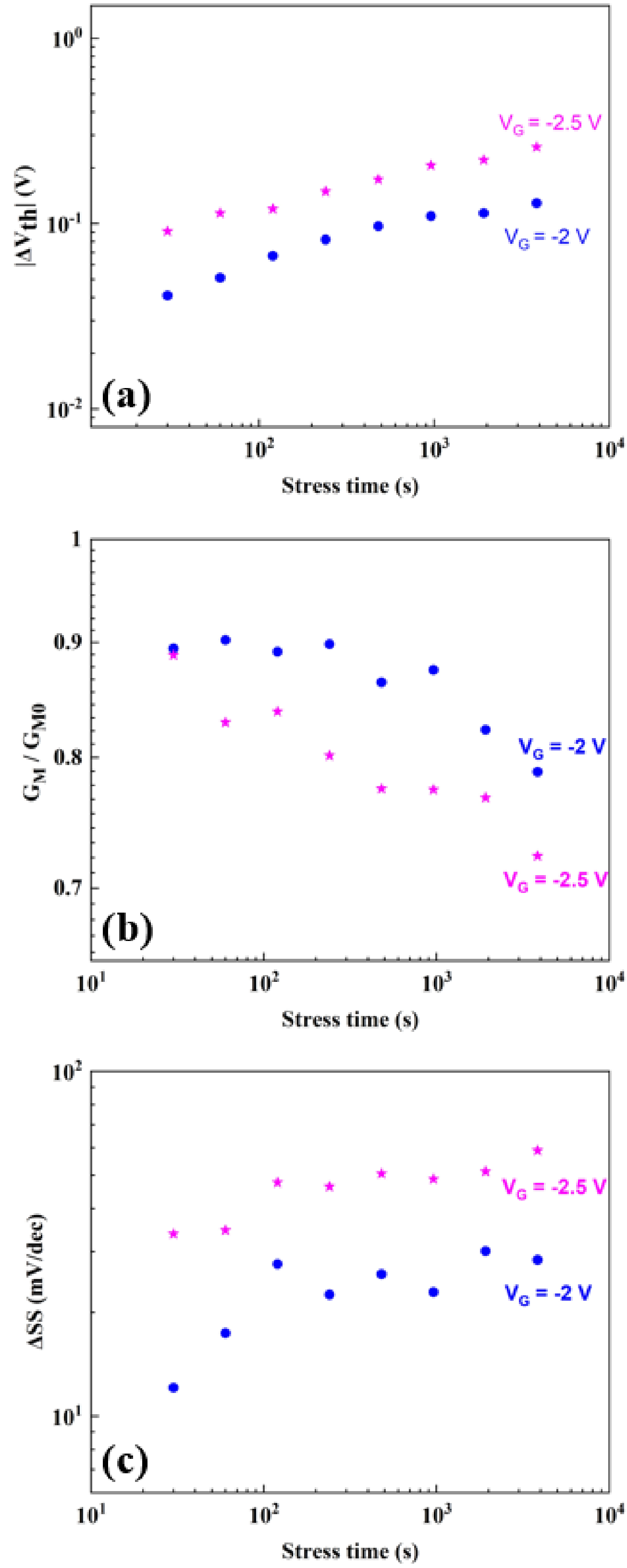

Fig. 3. 3 Logarithm of (a) absolute value of threshold-voltage shifts $|\Delta V_{th}|$, (b) normalized peak transconductance G_M variation and (c) subthreshold swing (*SS*) shifts for Ge *p*MOS FinFETs as functions of stress time and stress bias. G_{M0} represents the peak G_M before stress. (After [99].)

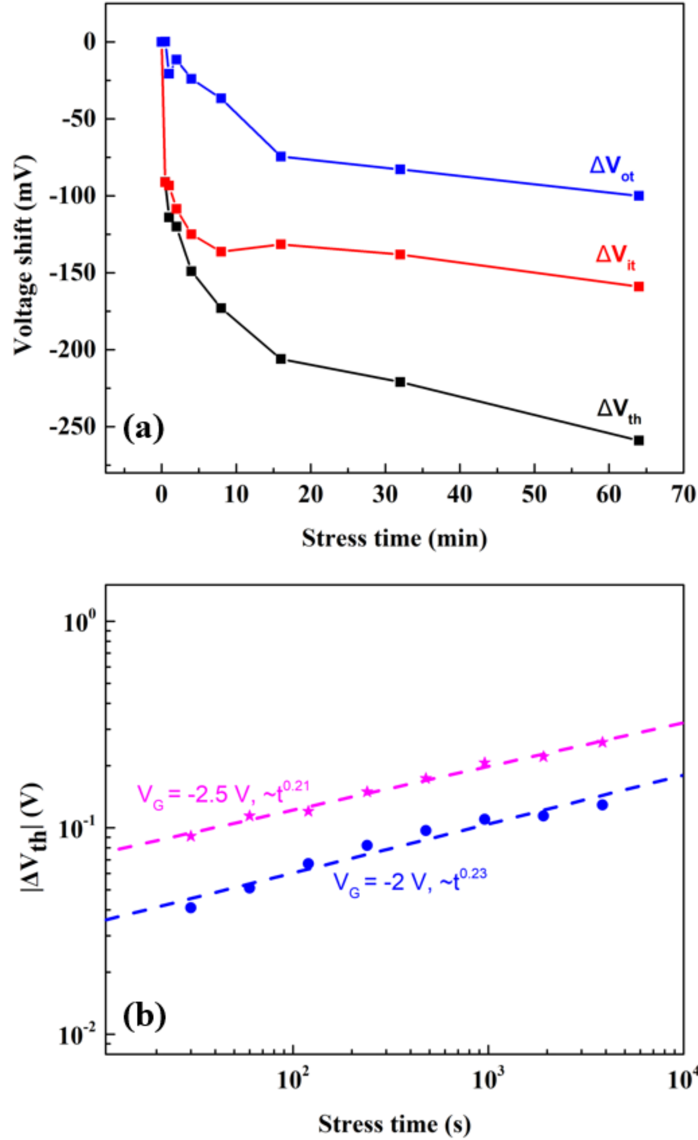

Fig. 3. 4 (a) Contributions of oxide traps (ΔV_{ot}) and interface traps (ΔV_{it}) to the total V_{th} shifts, as functions of stress time at V_G = -2.5 V and (b) power-law time dependence of NBTS-induced threshold-voltage shift $|\Delta V_{th}|$ for Ge *p*MOS FinFETs at different stress bias conditions. (After [99].)

To estimate effective activation energies, negative-bias-temperature stress (NBTS) was performed at different temperatures of 100 ℃, 150 ℃, and 200 ℃ at a stress voltage of $V_G = -1.6$ V. Source and drain terminals were grounded during NBTS. Four devices were tested at each temperature. Spot-I_d sense measurements were conducted to reduce measurement delays and times during the intermittent characterization step [10]. We extract the activation energy from the

temperature induced change in stress time t needed to achieve the fixed threshold voltage shift. Fig. 3. 5 shows the corresponding Arrhenius plot for various threshold voltage shifts from ΔV_{th} = 30 mV to ΔV_{th} = 70 mV. The slope of this Arrhenius plot is identified as an effective activation energy E_a. The extracted values of E_a range from 0.32 eV to 0.61 eV as the target value of ΔV_{th} increases, as often observed in previous studies of NBTI in Si MOS [100]. These values are smaller than the value of ~0.8 eV observed in Si *p*MOS devices at similar stress conditions [86, 100].

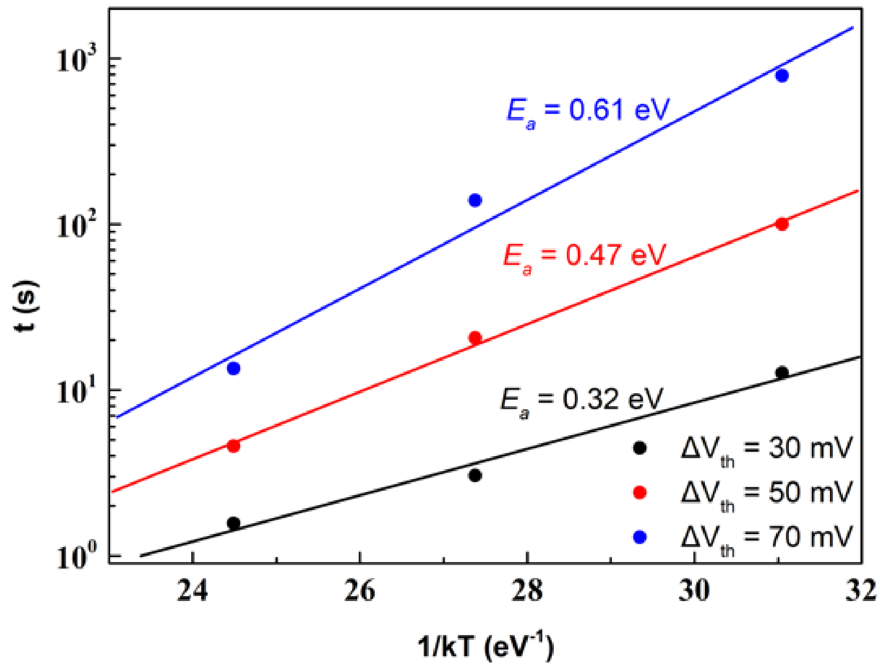

Fig. 3. 5 Arrhenius plot for the extraction of effective activation energy at various ΔV_{th} at temperatures of 100 °C, 150 °C, and 200 °C at a stress voltage of V_G = −1.6 V. The extracted activation energy E_a increases from 0.32 eV to 0.61 eV as the target V_{th} value increases from 30 mV to 70 mV.

3.3.2 Low-frequency noise measurements

Fig. 3. 6 shows excess voltage-noise power spectral densities, S_{Vd}, for Ge *p*MOS FinFETs for values of $V_{gt} = V_G - V_{th}$ ranging from −0.2 V to −0.4 V (a) before and (b) after NBTS for 64 min at V_G = −2 V. The $1/f$ noise was measured in the linear mode of device operation at V_{DS} = −50 mV with source and body contacts grounded. The spectra exhibit $1/f^{\alpha}$ frequency dependences for most frequencies and values of V_{gt};

$\alpha = \partial \ln S_{Vd}/\partial \ln f$. Deviations from $\alpha = 1$ can be caused by nonuniform defect-energy distributions in energy and/or space [49, 56, 101]. The frequency dependence of the noise changes significantly after NBTS. Notable increases are observed in post-stress low-frequency noise, especially in the higher range of frequencies. Multivalued frequency slopes α are due to prominent individual defects and/or highly nonuniform defect-energy distributions [49], as we demonstrate below.

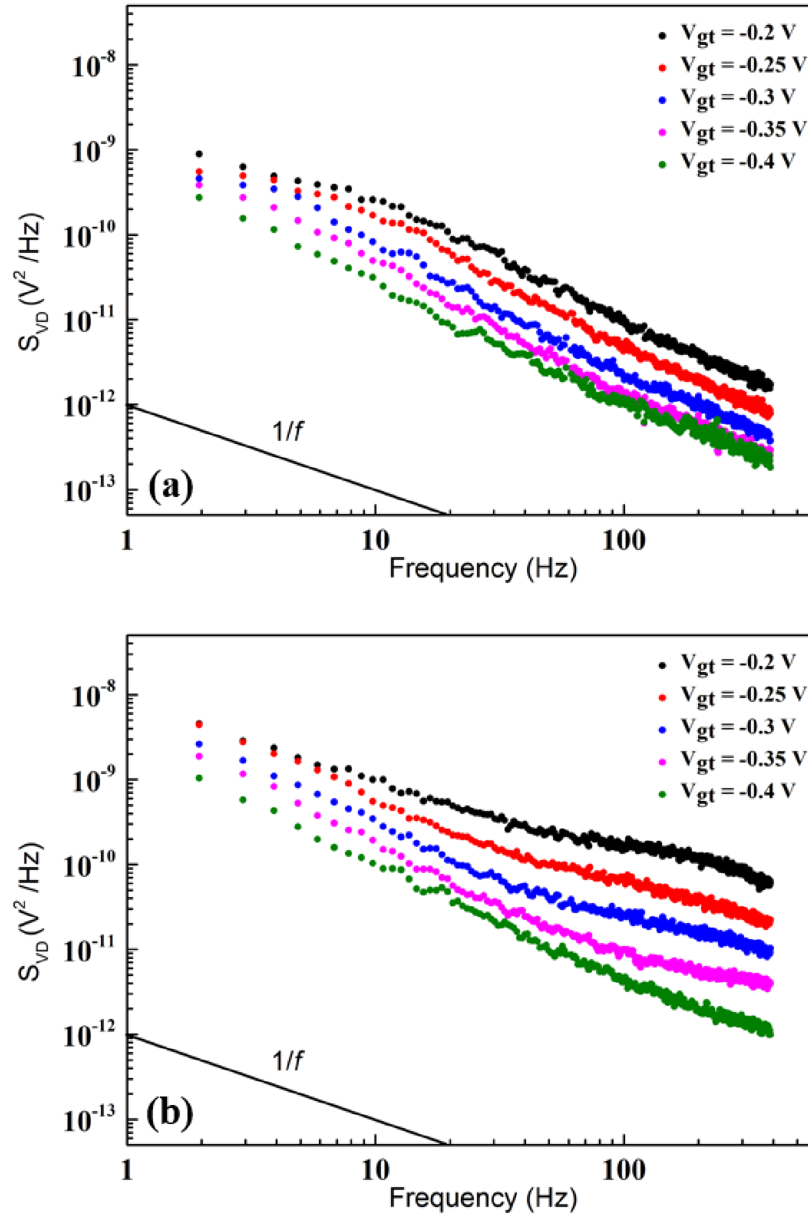

Fig. 3. 6 Excess voltage-noise power spectral density, S_{Vd}, vs. f at several values of $V_{gt} = V_G - V_{th}$ for Ge *p*MOS FinFETs (a) pre-stress, and (b) post-stress in linear operation. (After [99].)

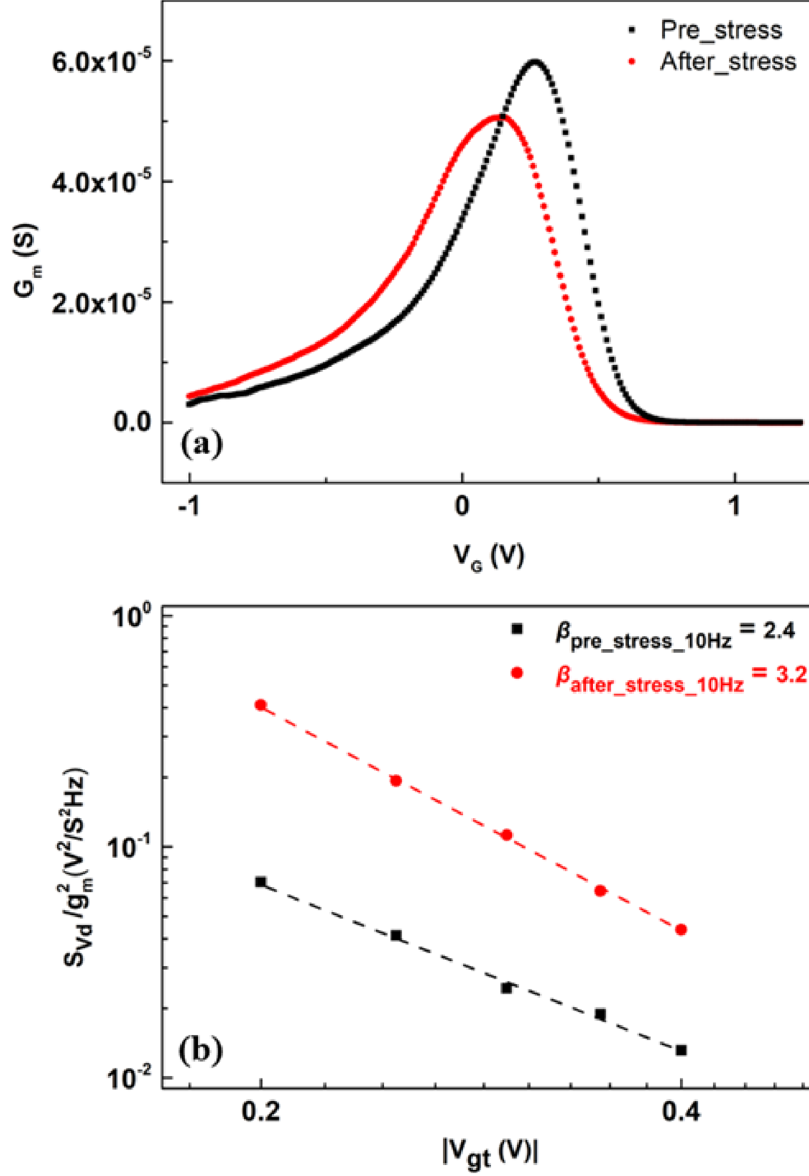

Fig. 3. 7 (a) Transconductance G_m characterization as a function of V_G and (b) S_{Vd}/g_m^2 at f = 10 Hz as function of V_{gt} for Ge *p*MOS FinFET devices before and after NBTS at −2 V. (After [99].)

For noise due to number fluctuations, if the defect-energy distribution is relatively uniform, $S_{Vd}/V_d^2 = S_{Id}/I^2$ is proportional to $(G_m/I_d)^2$ [56, 101-103]. Since $g_d^2 \sim V_{gt}^2$, the gate–voltage dependence $\beta = \frac{\partial ln(S_{Vd}/G_m^2)}{\partial \ln|V_{gt}|} \approx 2$ corresponds to an approximately uniform distribution of effective border-trap energies throughout the bandgap. Fig. 3. 7(a) shows the transconductance G_m characterization as a function of V_G before and after NBTS for 64 min at –2 V. Fig. 3. 7(b) shows the gate–voltage

dependence at f= 10 Hz of the low-frequency noise with G_m normalization for the devices of Fig. 3. 6. That $\beta \approx 2.4$ shows that the defect energy distribution is slightly nonuniform and increasing toward midgap surface potential [49, 101, 104]. After stress the noise magnitude increases significantly, indicating the generation of new border traps during NBTS [101, 104], and β increases to 3.2, consistent with a defect-energy distribution that is more strongly increasing toward midgap after stress than before.

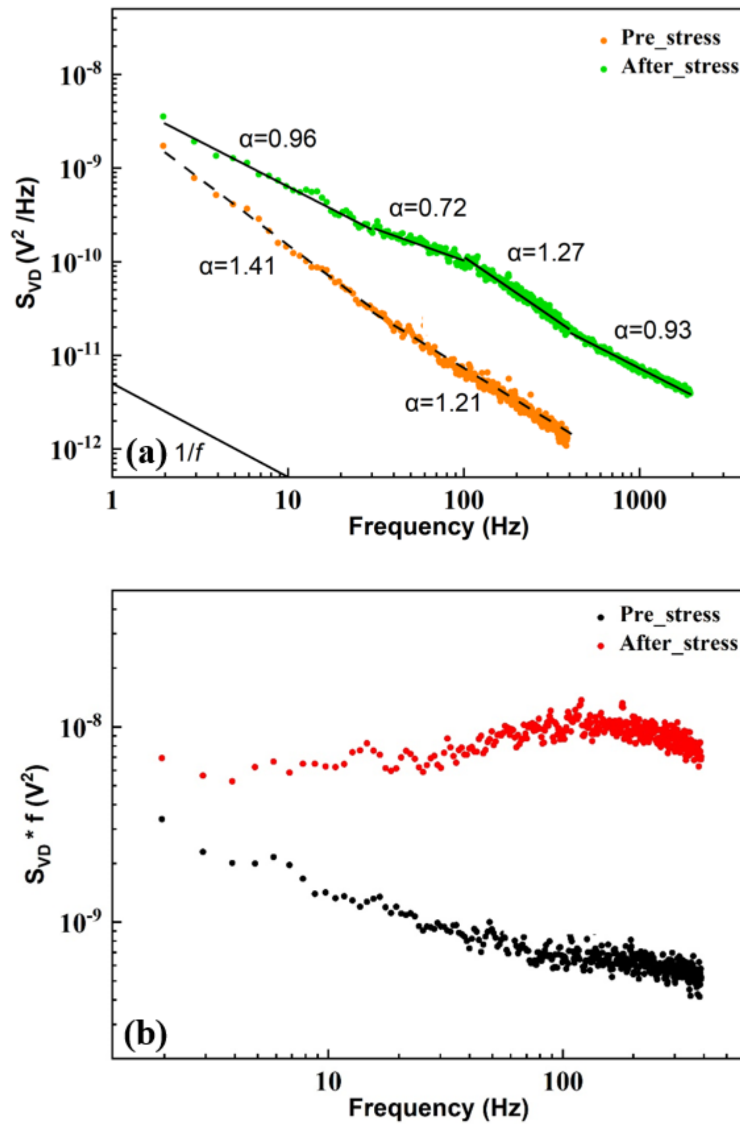

Fig. 3. 8 (a) Frequency dependence of S_{Vd} before and after NBTS, and (b) frequency-normalized noise, $S_{Vd}f$ vs. f. Noise measurements were performed at $V_{gt} = -0.35$ V and $V_{DS} = -50$ mV for Ge pMOS FinFETs. (After [99].)

To determine the relative influences of 1/*f* noise and potential generation-recombination (G-R) noise from localized, individual point defects [49], Fig. 3. 8(a) shows noise spectra before and after NBTS for a device with the same geometry as in Fig. 3. 6(b). Before stress, the slope of the frequency dependence α ranges from ~1.2 at higher frequencies to ~1.4 at lower frequencies. After NBTS, α ranges from ~0.7 to ~1.3 over the full frequency range. All of these values of α are consistent with "generic" 1/*f* noise [49, 51, 57]. In contrast, G-R noise leads to peak values of α greater than 1.5 [49, 105, 106]. To further assist in visualization of the variations in frequency dependence of the noise, Fig. 3. 8(b) shows $S_{Vd}f$ versus *f* before and after NBTS [51]. "Pure" 1/*f* noise will appear flat in this kind of chart; G-R noise will show a sharp peak. The broad peak observed at ~100 Hz in the stressed device is again consistent with 1/*f* noise due to a non-uniform defect distribution [49, 51], and not to G-R noise [49, 105, 106].

As we have discussed in Chapter 2, if the noise is caused by a random thermal-activated process that exhibits a broad distribution of energies $D(E_0)$ relative to kT, the frequency exponent shows a temperature dependence described by Eq. 2.2, thus enabling one to estimate the defect energy distribution through the temperature dependent noise data. In Eq. 2.2, τ_0 is set to 1.8×10^{-15} s based on experimental studies of the charge trapping and emission kinetics of oxide and border traps near the Si/SiO_2 interface [49, 89, 102, 107, 108]. From measurements of the temperature dependence of S_V, we estimate the defect-energy distributions $D(E_0)$ [57], via Eq. 2.4.

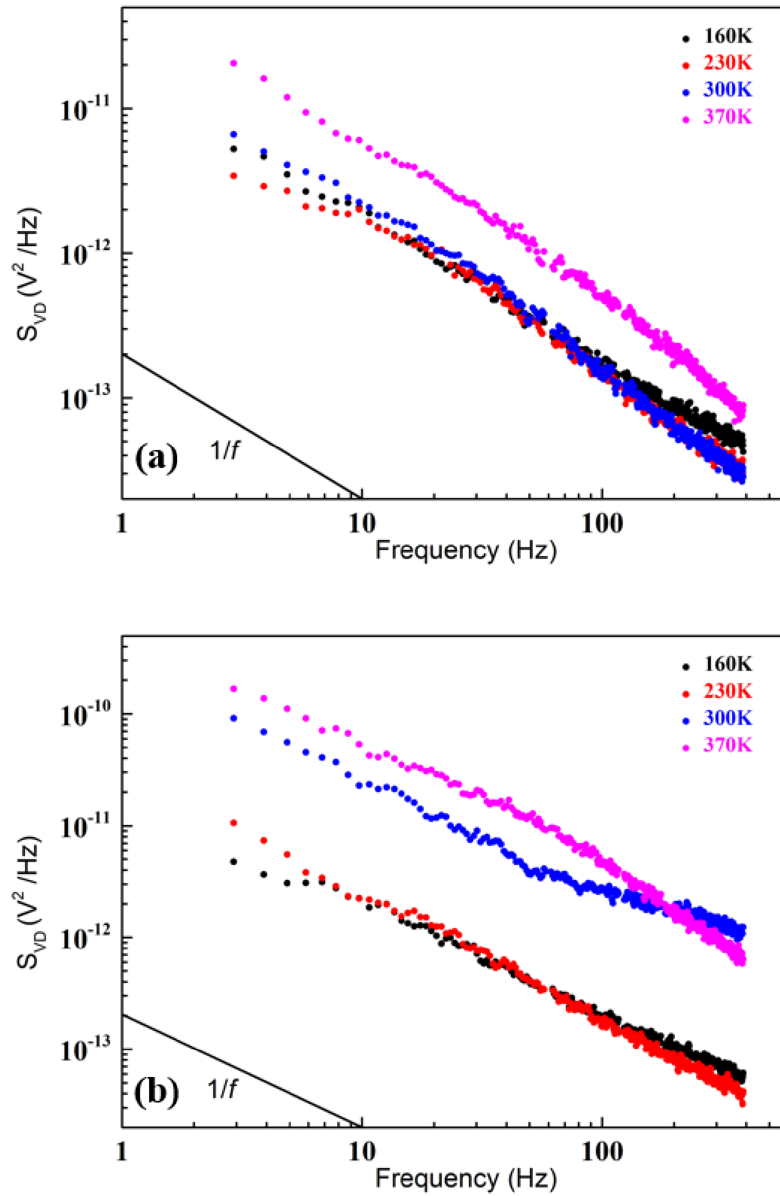

Fig. 3. 9 Excess voltage-noise power spectral density, S_{Vd}, vs. f at four temperatures for Ge *p*MOS FinFETs (a) with 0 V stress and (b) with NBTS during heating: $V_{gt} = -0.5$ V and $V_d = -50$ mV. (After [99].)

1/*f* noise measurements for an unstressed device were performed from 100 K to 380 K in steps of 10 K [109]. The threshold voltage V_{th} was extracted from the I_D-V_G curve at each temperature to ensure that V_{gt} was held constant for all noise measurements. During noise measurements, the device was biased at $V_D = -50$ mV and $V_{gt} = -0.5$ V. The unstressed device was held with all pins grounded for 10 minutes at each temperature step to serve as a control for a second series of

measurement that include NBTS. For this second run, the device was held at a constant gate bias of −2 V for ~10 min between successive noise measurements as the device during an otherwise similar series of noise measurements [109].

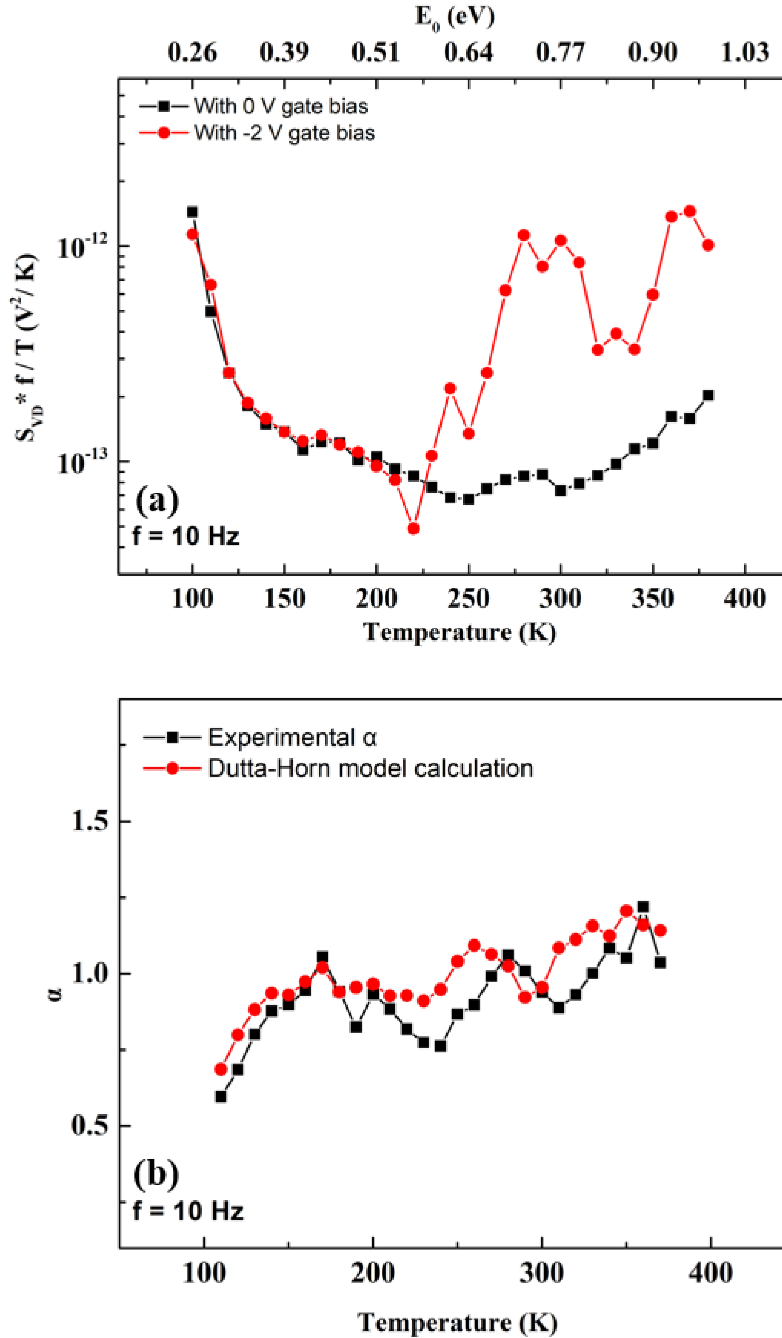

Fig. 3. 10 (a) Normalized 1/*f* noise as a function of temperature from 100 K to 380 K at f = 10 Hz. V_{gt} = −0.5 V and V_d = −50 mV for the Ge *p*MOS FinFETs before and after NBTS. (b) Experimental and calculated (from Eq. 2.2) frequency exponents α for unstressed device with S_{Vd} at 10 Hz and spectral slope α at 10 Hz. (After [99].)

Fig. 3. 9(a) shows noise spectra in a Ge *p*MOS FinFET at selected temperatures before NBTS. S_{Vd} was of the "generic" $1/f^{\alpha}$ type [49, 57]; the extracted frequency exponent α varies between 0.8 and 1.1. As shown in Figs. 3. 9(a) and 3. 9(b), the magnitudes of noise in stressed and unstressed devices are similar at lower temperatures, e.g., ~ 160 K and ~ 230 K, but noise magnitudes are much higher for stressed devices than unstressed device at higher temperatures, e.g., ~300 K and ~370 K. The increased noise in the stressed device primarily originates from defects activated and/or created by NBTS. These results are similar to those observed in work on SiGe *p*MOSFETs with high-K gate dielectrics [109].

Fig. 3. 10(a) shows the normalized noise magnitude $S_{Vd}*f/T$ at f = 10 Hz as a function of temperature from 100 K to 380 K. Noise levels in these devices at temperatures above ~230 K are affected significantly by NBTS. The energy scales on the upper *x*-axis in Fig. 3. 9(a) are derived from the Dutta–Horn model via Eq. 2.2. The applicability and validity of this relation to the devices of this work is validated by the results of Fig. 3. 10(b), which shows that the measured values of frequency exponent α from the noise data for unstressed devices agree well with Eq. 2.2 [49, 57, 109, 110].

The magnitudes of normalized noise for the stressed device increase significantly for 230 K < T < 380 K due to NBTS-induced trapped charge. Peaks in noise magnitude are observed at ~290 K and ~360 K, indicating accelerated rates of trap creation and/or activation at these temperature and energies. Previous experimental and computational studies strongly suggest that the noise in as-processed and stressed devices at relatively higher temperatures (> 200 K) is due most likely to O vacancies and hydrogen-related defects in SiO_2 and/or HfO_2 [49, 90, 102, 109, 111, 112]. The noise

at relatively lower temperatures (< 200 K) may result from interactions in the Ge layer [109], as discussed in Section 3.4.

3.4 Discussion

NBTI is often interpreted by a reaction-diffusion model [9]. This model typically assumes that inversion layer holes and oxide electric field assist in the breaking of H passivated defects at the Si/SiO_2 interface during stress, releasing H from previously passivated interface defects. The released hydrogen diffuses into the oxide, leading to an increase of Si dangling bonds and time-dependent buildup of oxide- and interface-trap charge [9]. Density functional calculations show that it is energetically much more favorable for Si–H bonds to be broken through reactions with protons that are released from dopants in the semiconductor and drift under negative bias toward the semiconductor-dielectric interface than by direct interactions with holes [77].

In contrast, defect-centric models are reaction-limited and consider trapping and trap transformation to be first-order processes [80, 113, 114]. Recent data on highly-scaled devices operating at higher electric fields generally are more consistent with this model than with reaction-diffusion models that include second-order processes as rate-limiting steps [114, 115]. The defects that are created and/or activated by NBTS are broadly distributed in space and energy [114-116]. Effective activation energies (AE) for defect formation often differ for recoverable components due to charge trapping and annealing and quasi-permanent components due to more stable charge trapping and interface-trap generation [42, 43, 80, 100, 114-116].

We now consider results of the measurements summarized in Fig. 3. 5. Effective activation energies in these devices increase from ~0.3 eV to ~0.6 eV as target values of V_{th} shift from 30 mV

to 70 mV. Higher target V_{th} shifts result from longer stress times, which are affected more strongly by the permanent component of NBTI [100], which in these devices (Figs. 3. 3 and 3. 4) include significant contributions from interface-trap formation. Reduced activation energies for interface-trap formation in SiGe and/or Ge devices than in Si MOS devices have been attributed to a reduced barrier for hydrogen release from Si dangling bonds in the presence of Ge atoms at the interface [83]. The relatively rapid buildup of interface traps in Fig. 3. 4 and corresponding degradation of G_M and *SS* in Fig. 3. 3(b) and 3. 3(c) most likely occur because applied negative electric fields in these cases significantly exceed the ~1.2 eV threshold that leads to proton release from hydrogen-passivated phosphorus dopant atoms [77, 117, 118]. The rate of interface-trap formation is reduced as the concentrations of hydrogen-passivated dopant atoms and/or passivated dangling bonds at the interface are reduced. Protons that surmount the barrier between the Si and SiO_2 without reaction may contribute to the net positive trapped oxide charge [77, 118].

Increases in effective border-trap energies E_o from 0.6 eV to 1 eV are inferred from the temperature-dependent low-frequency noise measurements of stressed devices in Fig. 3. 9. These border traps have been shown in previous work to be related to oxygen vacancies and their complexes with hydrogen in the near-interfacial SiO_2 and HfO_2 dielectric layers via low-frequency noise and random-telegraph-noise measurements [42, 43, 111, 112, 116, 119]. The results of Fig. 3. 7 show that the effective densities of the border traps in these Ge *p*MOS devices increase as the surface potential approaches midgap, consistent with results by Li *et al.* on bulk-Si *n*MOS FinFETs fabricated by imec with similar SiO_2/HfO_2 gate dielectrics [120]. In contrast, *p*MOS FinFETs in the work of Li *et al.* and elsewhere in the literature typically show effective defect-

energy distributions increasing toward the valence-band edge [56, 89, 101-104, 120]. These variations in defect-energy distribution certainly warrant follow-up studies. The NBTI response and low-frequency noise of strained Ge *p*MOS FinFETs have been evaluated.

3.5 Summary and Conclusions

The NBTI response and low-frequency noise of strained Ge *p*MOS FinFETs have been evaluated. Ge *p*MOS FinFETs show NBTS-induced interface-trap creation with activation energies of ~0.3 eV to ~0.6 eV. These energies are lower than the value of ~0.8 eV often observed for Si *p*MOSFETs [86, 100]. Newly created and/or activated border traps related to oxygen vacancies and their complexes with hydrogen are detected via low-frequency noise measurements above ~230 K, reinforcing the results and conclusions of previous studies on earlier generation SiGe *p*MOS FinFETs [109]. The gate–voltage dependence of the 1/*f* noise indicates that the defect energy distributions before and after NBTS are increasing toward midgap in these devices, in contrast with previous results that tend to show *p*MOS defect-energy distributions increasing toward the valence-band edge [49, 56, 101-104]. These results illustrate the sensitivity of border-trap spatial and energy distributions to detailed processing condition, reinforcing the utility of low-frequency noise measurement to aid the understanding of MOS defect densities and energy distributions.

CHAPTER 4 Low-Frequency Noise and Defects in AlGaAs/InGaAs/GaAs Pseudomorphic High-Electron-Mobility Transistors

This chapter is adapted from "Low-Frequency Noise and Defects in AlGaAs/InGaAs/GaAs Pseudomorphic High-Electron-Mobility Transistors" published in Journal of Applied Physics, and has been reproduced with the permission of the publisher and my co-authors Andrew O'Hara, Xun Li, Peng Fei Wang, En Xia Zhang, Ronald D. Schrimpf, Sokrates T. Pantelides, and Daniel M. Fleetwood.

- X. Luo et al., "Low-Frequency Noise and Defects in AlGaAs/InGaAs/GaAs Pseudomorphic High-Electron-Mobility Transistors," *Journal of Applied Physics*, vol. 135, no. 2, Jan. 2024, Art. no. 025702.

4.1 Introduction

AlGaAs/InGaAs/GaAs pseudomorphic high-electron-mobility transistors (PHEMTs) are widely used in microwave communications, radar systems, and other aerospace and defense systems [13-15]. Defects in as-processed devices are a concern for device yield and performance, while voltage- and/or temperature-stress induced defects are a potential concern for device reliability. A significant reliability concern is generation of hot electrons in the channel at high electric fields[16-18]. Effects of hot-electron stress in GaAs-based devices have generally been attributed to the activation of pre-existing defects and/or charge accumulation under the gate or at the interface between the semiconductor and passivation layers in the gate-drain region [16-18, 121, 122]. These defects can cause a reduction in drain current and transconductance, as well as shifts in threshold voltage, resulting in degraded DC and RF performance [16-19, 123-126].

In this work, effects of electrical stress at temperatures up to 105 ºC are evaluated for commercially available AlGaAs/InGaAs/GaAs PHEMTs biased in OFF (very low current, high

electric field), Semi-ON (medium current, relatively high electric field), and ON (high current, relatively low electric field) states. A small positive shift of threshold voltage and negligible degradation in peak transconductance are observed under ON-state bias conditions at elevated temperature, showing that minimal electron trapping (activation of acceptor defects) occurs. Low-frequency $1/f$ noise measurements [49, 57, 88], density functional theory (DFT) calculations, and literature analysis are combined to obtain insights into the energy distribution and possible microstructures of the defects in these devices.

4.2 Experimental Details

AlGaAs/InGaAs/GaAs PHEMTs were obtained from a commercial GaAs foundry. The rated device operating voltage is 3 V. A typical cross section of the epitaxial layer structures is shown in Fig. 4. 1 [127, 128]. The structure consists of a semi-insulating GaAs substrate, a GaAs buffer layer, an InGaAs channel layer, an AlGaAs spacer layer, an n-doped AlGaAs supply layer, and a heavily n-doped GaAs cap layer. The introduction of indium increases the electron mobility and thus the switching speed [13].

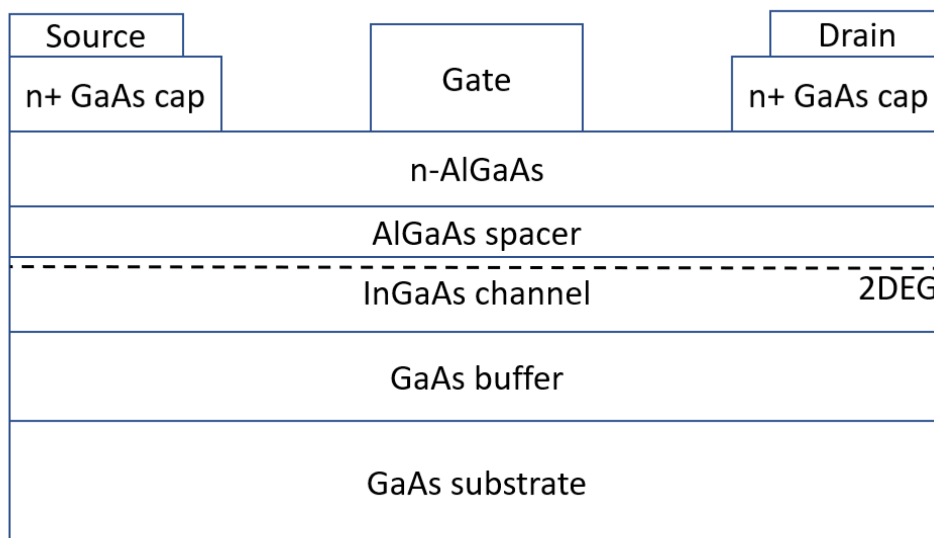

Fig. 4. 1 Schematic diagram of AlGaAs/InGaAs/GaAs PHEMT structures. (After [129].)

Direct current (DC) measurements and stresses were performed using an Agilent B1505A parametric analyzer (PA). Devices were stressed in a Test Equity Model 140 Temperature Chamber at elevated temperatures and cooled for ~30 minutes before measuring I_D-V_G characteristics. Threshold voltage V_{th} was extracted from the I_D-V_G curve in the linear range of transistor operation with $V_{\mathrm{DS}} = 50$ mV. The initial values of V_{th} were approximately −0.55 V for these devices. Low frequency 1/*f* noise measurements were performed from 80 K to 320 K using a Stanford Research SR 760 FFT spectrum analyzer in a cryostat-based system [49]. At least three devices were tested; representative results are shown below.

4.3 Experimental Results

4.3.1 Current-voltage measurements

Fig. 4. 2 shows (a) ΔV_{th}, and (b) normalized peak transconductance G_{M} as functions of time for a typical AlGaAs/InGaAs/GaAs PHEMT stressed under a fixed drain bias (5 V) for a series of gate biases increasing from −1 V (OFF state) to 0.4 V (ON state) at temperatures up to 105 °C. The V_{th} shifts in Fig. 4. 2(a) were nearly unchanged during both "OFF" state and "Semi-ON" state stresses. In the ON state, positive V_{th} shifts of ~12 mV were observed after a stress of 102 h at 80 °C and approached ~30 mV after a 66-h stress at 105 °C. The probability of significant gate-metal diffusion is minimal in this study, given that the temperature during stress is well below the threshold of ~200 °C for the onset of this process in GaAs MESFETs and PHEMTs [130-132]. The increase in V_{th} suggests activation of modest densities of acceptor-like defects and/or passivation of donor-like defects via electron capture at positively charged centers under ON-state bias conditions at elevated temperatures [19]. No significant change in peak transconductance G_{M} was observed during the

stress sequence, indicating that the charged defects responsible for the V_{th} shifts evidently are not located close enough to the two-dimensional electron gas (2DEG) to scatter carriers strongly. The nature of these defects is discussed in Section 4.4.

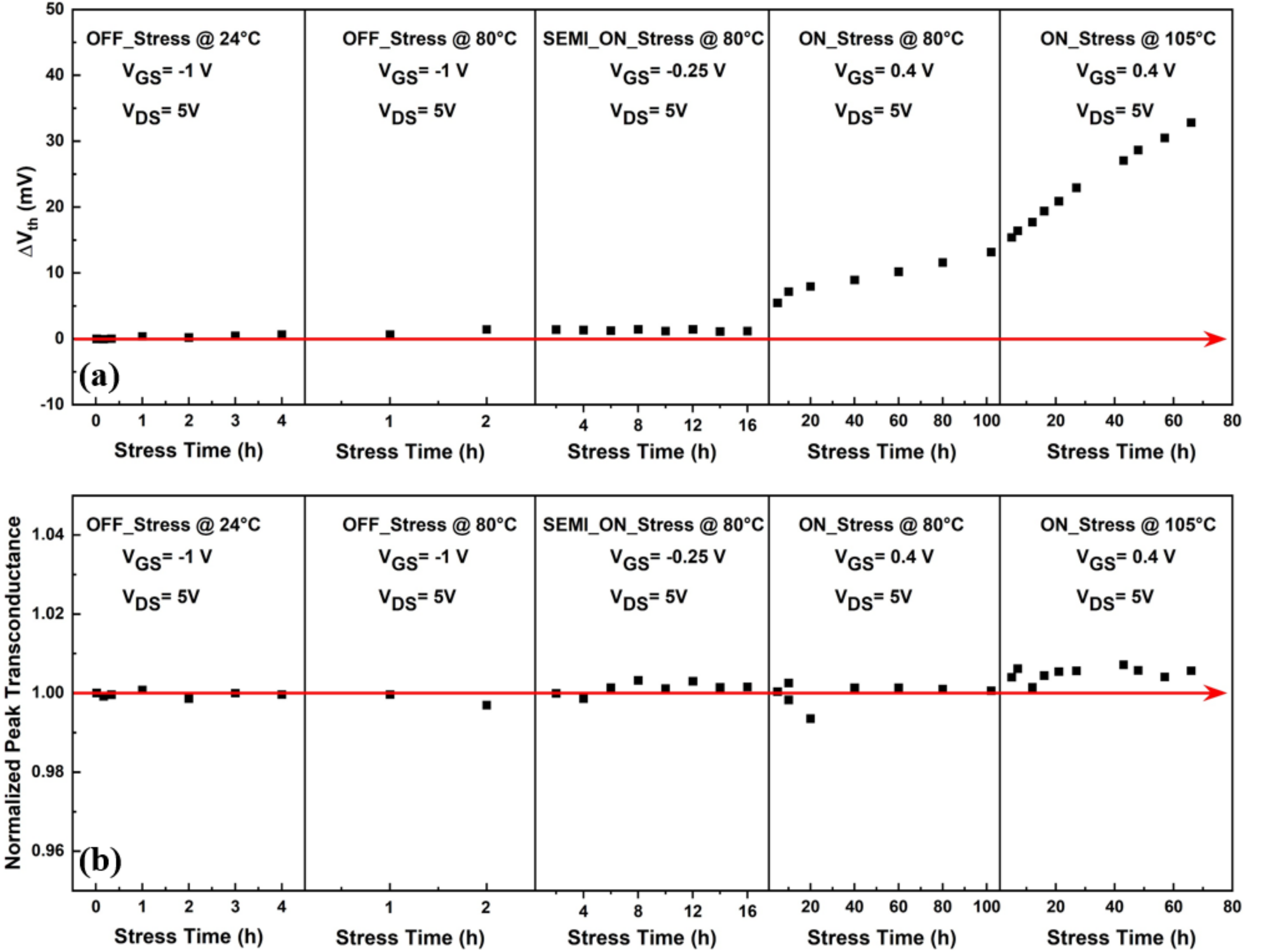

Fig. 4. 2 (a) Threshold voltage V_{th} shifts and (b) normalized peak transconductance G_M as functions of time for a typical GaAs PHEMT device stressed under various bias stress conditions at temperatures up to 105 °C. V_G = 0.4 V and V_{DS} = 5 V. DC measurements are performed at room temperature after devices are cooled for ~30 min. (After [129].)

Fig. 4. 3 shows (a) I_D-V_G and (b) I_G-V_G characteristics for the device before and after ON-state bias stress (V_G = 0.4 V; V_{DS} = 5 V) at elevated temperatures. The similar levels of the gate and OFF-state drain leakages suggest that the gate leakage current is the main contributor to the observed leakage from the drain terminal. The gate leakage under OFF-state operating voltage increases

significantly after ON-state bias stress. Little change in forward gate current is observed, consistent with the lack of change in G_M. This result verifies that the Schottky barrier height of the gate contact does not degrade significantly during the stressing conditions of this study.

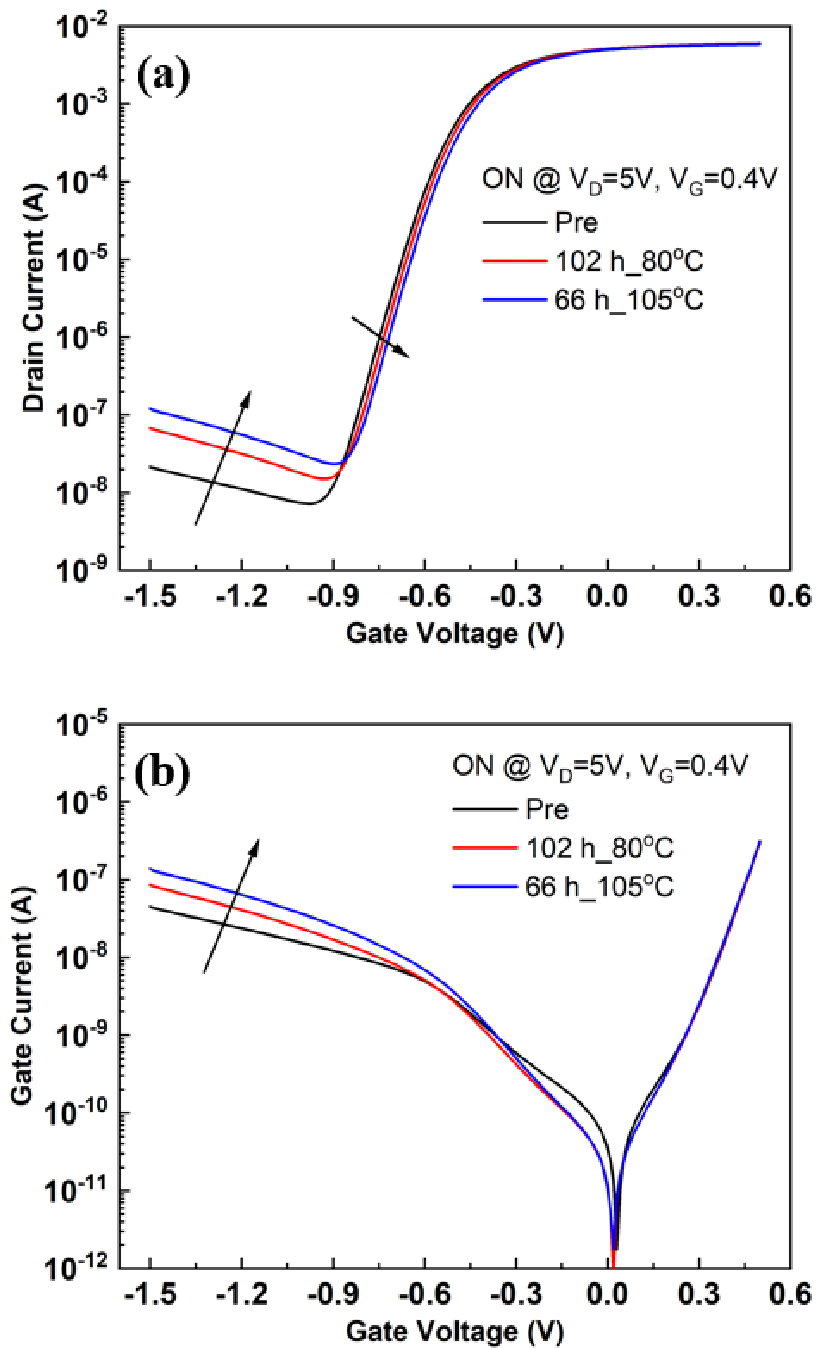

Fig. 4. 3 (a) I_D-V_G and (b) I_G-V_G characteristics measured at V_{DS} = 50 mV before and after ON-state bias stressing sequences at 80 °C and 105 °C. DC measurements are performed at room temperature after devices are cooled for ~30 min. (After [129].)

4.3.2 Low-frequency noise measurements

Fig. 4(a) shows excess voltage-noise power spectral densities, S_{Vd}, for as-processed devices at values of $V_{gt} = V_G - V_{th}$ ranging from 0.1 V to 0.55 V as a function of frequency at room temperature. The low-frequency (LF) noise was measured at V_{DS} = 50 mV with source and body contacts grounded. The bias voltages are chosen to ensure that the noise originates from the gated portion of the channel, with an approximately constant channel resistance [133]. The spectra exhibit a mixture of $1/f$ noise and generation-recombination noise at many frequencies and values of V_{gt}; $\alpha = -\partial \ln S_{Vd}/\partial \ln f$ [49]. For the noise spectrum measured at V_{gt} = 0.25 V and V_{DS} = 50 mV in Fig. 4. 4(a), the value of $\alpha = 0.7$ for 2 Hz $< f <$ 60 Hz and $\alpha = 1.2$ for 60 Hz $< f <$ 390 Hz. Deviations from $\alpha = 1$ are consistent with LF noise due to significantly non-uniform defect-energy distributions [49, 104]. Fig. 4. 4(b) shows the gate–voltage dependence of the low-frequency noise of GaAs PHEMTs before and after stress. Gate–voltage dependences $\beta = -\partial \ln S_{Vd}/\partial \ln |V_{gt}|$ were calculated at 10 Hz. The $\beta \approx 3.6$ value for high-voltage regions is typical for HEMTs [133]. Minimal changes are observed in β before and after stress.

Measurements of LF noise as a function of temperature can provide significant insight into distributions of energies for the responsible defects and impurity centers [49, 51, 57, 104, 134]. Accordingly, we have measured the excess drain-voltage-noise power spectral density S_{Vd} of GaAs PHEMT devices as a function of frequency f at temperatures from 80 K to 320 K before and after temperature-voltage stress. Fig. 4. 5 shows (a) V_{th} and (b) peak G_M as a function of measuring temperature for GaAs PHEMTs before and after 66 h ON-state stress at 105 °C. As the temperature increases from ~80 K to ~320 K, V_{th} decreases by ~180 mV (~0.75 mV/K) for both stressed and

unstressed devices; values of peak transconductance decrease by ~24% for each device type in Fig. 4. 5(b). These changes of V_{th} and peak G_M with temperature are comparable to those of Schottky gate GaN-based HEMTs [19, 126, 135].

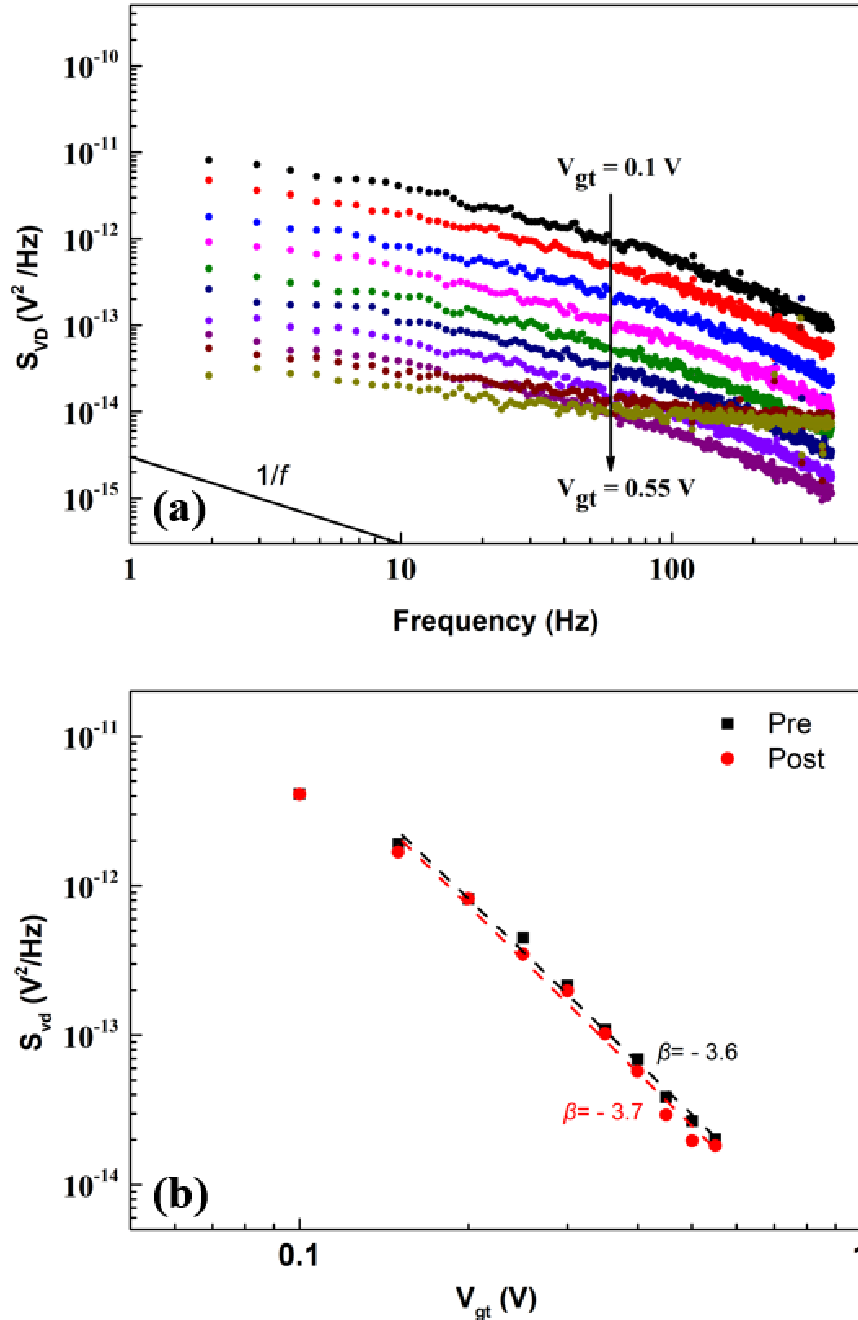

Fig. 4. 4 (a) Excess voltage-noise power spectral density, S_{Vd}, vs. f at several values of $V_{gt} = V_G - V_{th}$ for GaAs PHEMTs before stress, and (b) noise magnitude at $f = 10$ Hz as a function of V_{gt} for GaAs PHEMTs before and after stress. Unwanted spikes from 60-Hz pickup and harmonics have been removed. (After [129].)

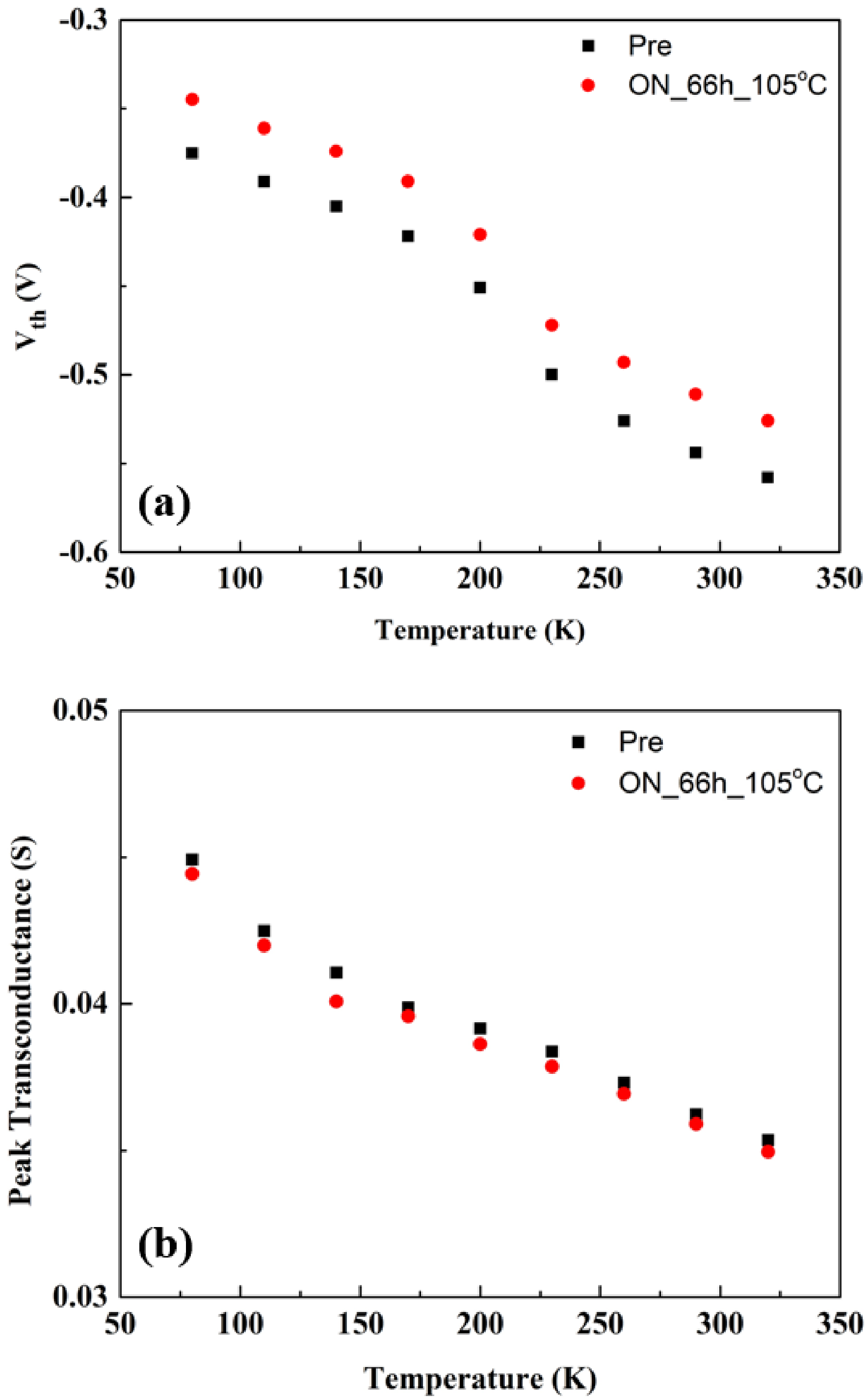

Fig. 4. 5 Temperature dependence of (a) V_{th}, and (b) G_M for AlGaAs/InGaAs/GaAs PHEMTs before and after ON-state bias stress. (After [129].)

Fig. 4. 6 shows frequency and temperature dependences of S_{Vd} for GaAs PHEMTs before stress. During noise measurements, the device was biased at V_{DS} = 50 mV and V_{gt} = 0.25 V. As the temperature increases from 80 to 320 K, S_{Vd} shows contributions from both Lorentzian (prominent

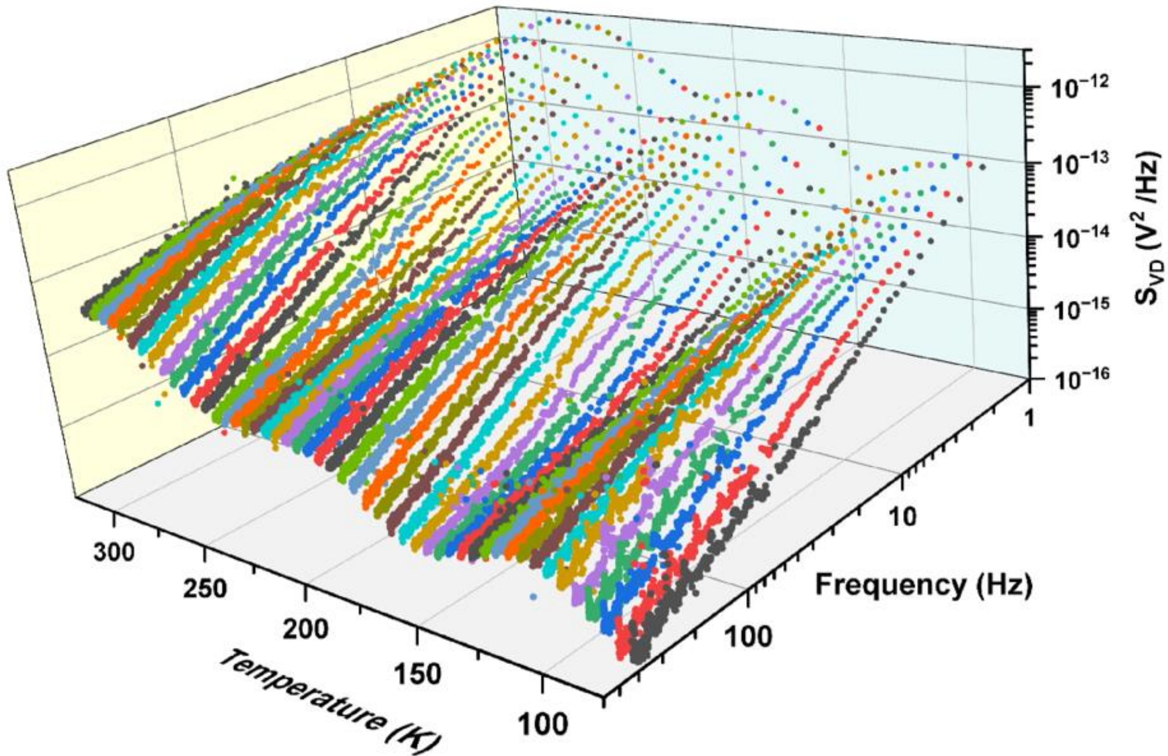

Fig. 4. 6 Frequency and temperature dependences of S_{VD} in the ranges f = 2-390 Hz and T = 80-320 K for GaAs PHEMTs before stress. Here V_{gt} = 0.25 V and V_{DS} = 50 mV. Unwanted spikes from 60-Hz pickup and harmonics are removed. (After [129].)

defect active at a given temperature and frequency) and 1/f (broad distribution with no prominent defect) noise sources [49, 57, 105]. Individual spectra from 100 K to 200 K and 250 K to 300 K before and after stress are shown in Fig. 4. 7(a) and Fig. 4. 7(b), respectively. Values of the frequency slope, α, are shown in the legend; these range from 0.6 to 1.6. Frequency slopes α that deviate significantly from 1.0 are due to generation-recombination (G-R) noise caused by prominent individual defects and/or highly non-uniform defect-energy distributions [49, 99, 105]. The G-R noise with Lorentzian spectra is superposed on background 1/f noise arising from a broad distribution of less prominent defects with ranges of characteristic times that vary slowly with respect to kT, where k is Boltzmann constant and T is the absolute temperature [49, 51, 57, 126].

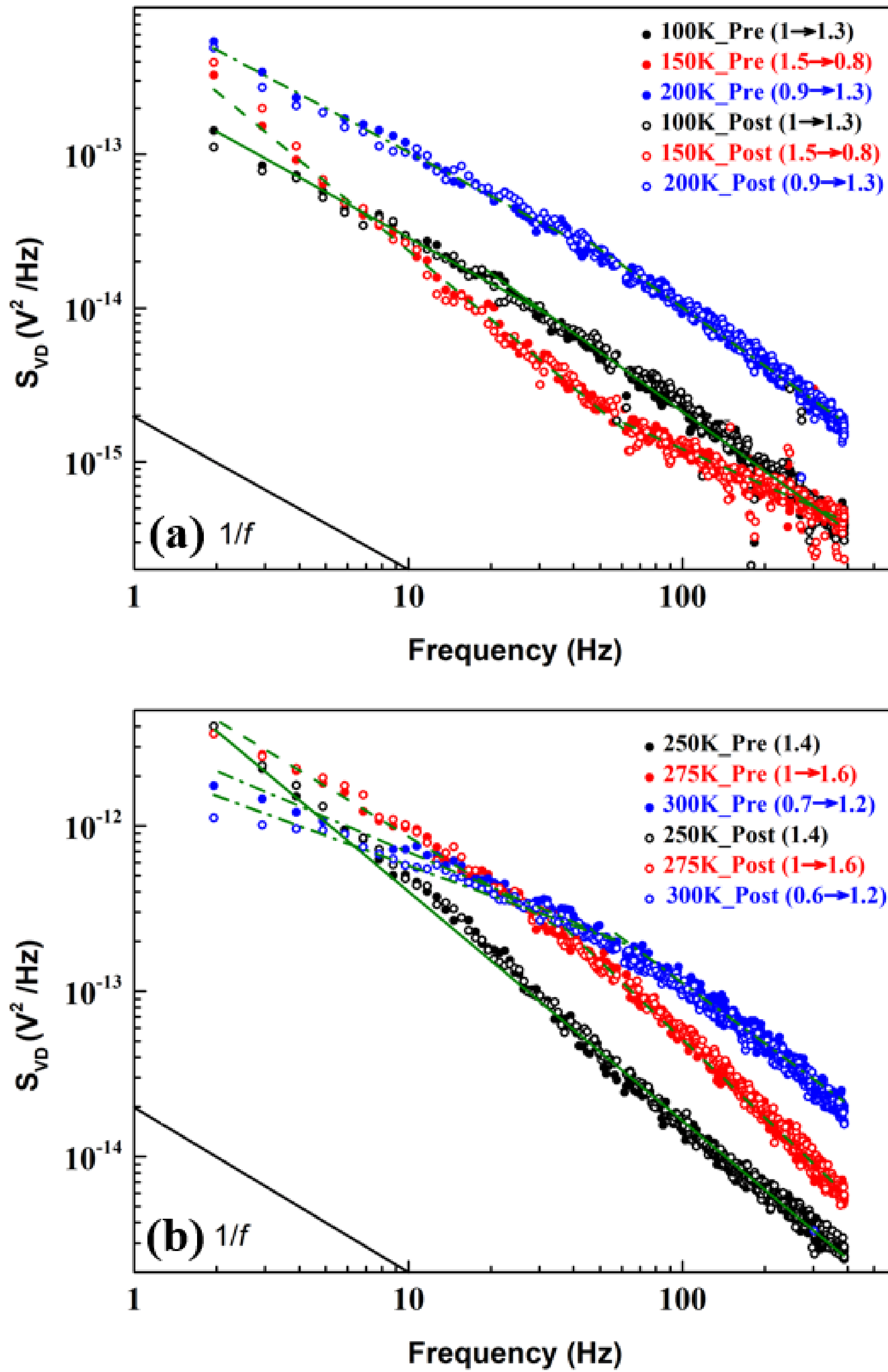

Fig. 4. 7 Excess voltage-noise power spectral density, S_{Vd}, vs. f for GaAs PHEMTs before and after stress from (a) 100 K to 200 K and (b) 250 K to 300 K. Here V_{gt} = 0.25 V and V_{DS} = 50 mV. Unwanted spikes from 60-Hz pickup and harmonics are removed. Values of slope, α, are shown in the legend. (After [129].)

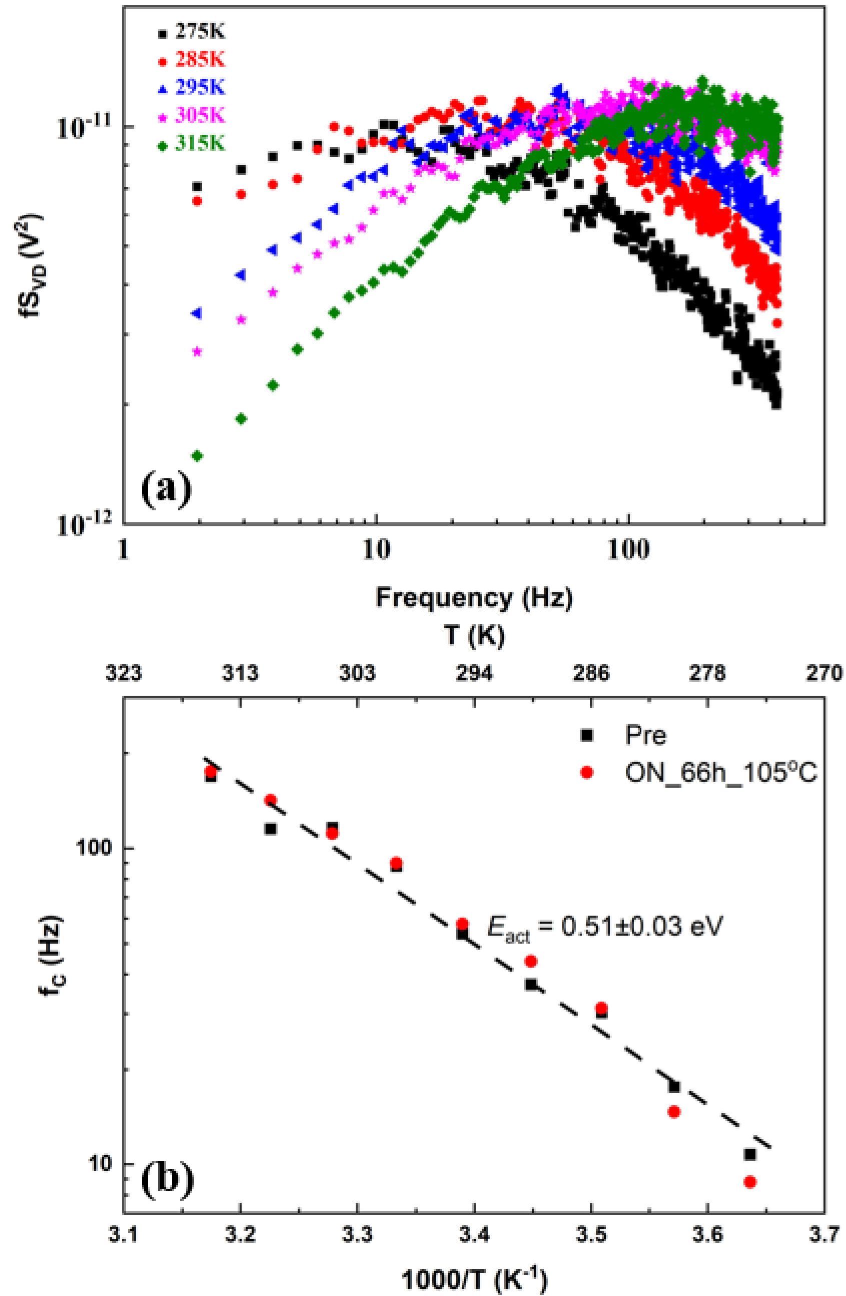

Fig. 4. 8 (a) fS_{Vd} vs. f for the as-processed GaAs PHEMTs at temperatures from 275 K to 315 K. (b) Arrhenius plot calculated at 5 K intervals of corner (peak) frequencies f_C vs. inverse temperature for the as-processed and stressed devices of Fig. 4. 7. (After [129].)

When prominent G-R peaks are observed, spectral analysis is facilitated by replotting data as fS_{Vd} vs. f [57]. Such a plot is shown in Fig. 4. 8(a) for the as-processed devices of Fig. 4. 7. The value of corner (peak) frequency f_C increases from ~10 Hz to ~170 Hz as the temperature increases from 275 K to 315 K. Activation energies for processes leading to low-frequency noise can be

estimated to first order via an equation of the Arrhenius form:

$$E_{\mathrm{act}} \approx -kT\ln(f/f_0) \quad (4.1)$$

Here f_o is a characteristic frequency of the underlying fluctuation process [49, 51, 57]. Fig. 4. 8(b) is an Arrhenius plot of extracted f_C as a function of inverse temperature. Applying Eq. (4.1) to the full set of results for devices of Fig. 4. 7, before and after temperature-voltage stress, the derived E_{act} is 0.51 ± 0.03 eV; the corresponding value of f_0 in Eq. (4.1) is 2×10^{10} Hz.

Dutta and Horn have shown that, if the noise is caused by a random thermally-activated process that exhibits a broad distribution of energies $D(E_{\mathrm{act}})$ relative to kT, the shape of effective defect-energy distribution $D(E_o)$ can be estimated from low-frequency noise measurements versus temperature via [49, 51, 57]:

$$D(E_0) \propto \frac{f}{kT} S_{Vd} \quad (4.2)$$

Fig. 4. 9 shows the normalized excess drain-voltage noise power spectral density $S_{VD}f/T$ at f = 20 Hz as a function of temperature, before and after devices were stressed under ON bias (0.4 V) conditions. A strongly nonuniform defect-energy dependence is observed, consistent with studies of the low-frequency noise of GaN/AlGaN HEMTs [49, 126, 135, 136]. In practice, these effective energies include transitions between a trap and the proximal energy band, or the energy required to reconfigure a defect between charge states on opposite sides of the Fermi energy [49, 89, 90, 107, 136]. The most prominent peak in Fig. 4. 9 is located at ~290 K with $E_o \approx E_{\mathrm{act}} \approx 0.51$ eV. The value of $\tau_o = 1/f_o = 5 \times 10^{-11}$ s derived by applying Eq. (4.1) to the data of Fig. 4. 8 is used to set the effective energy scale on the upper x-axis in Fig. 4. 9. This value of τ_o is similar to that found for GaN-based HEMTs [137, 138], and much lower than that used in previous studies on Si MOSFETs

[49].

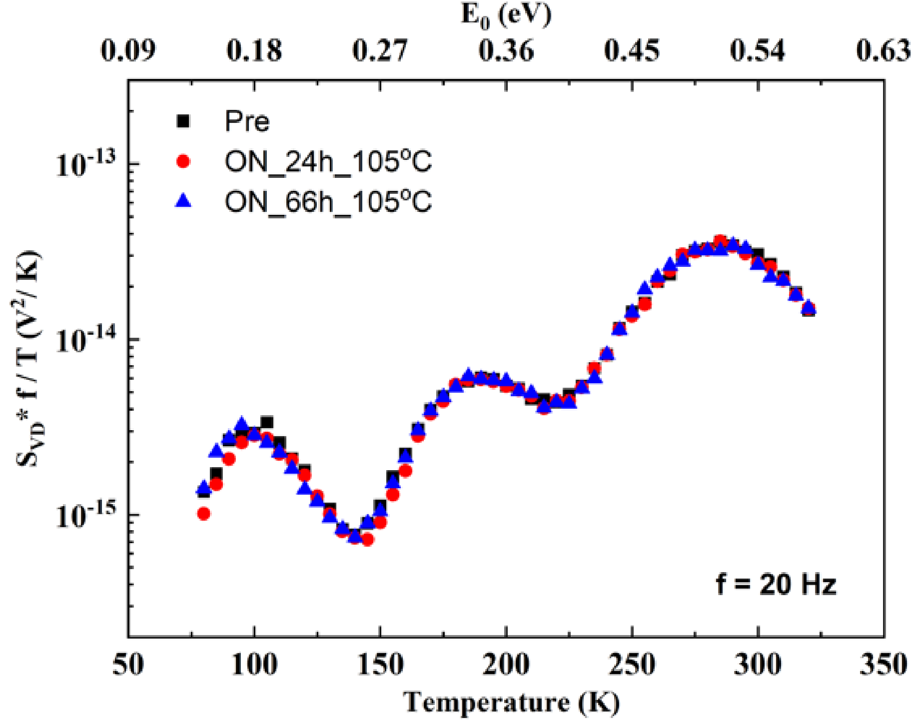

Fig. 4. 9 Normalized 1/*f* noise as a function of temperature from 80 K to 320 K at f = 20 Hz for GaAs PHEMTs before and after stress. Here V_{gt} = 0.25 V and V_{DS} = 50 mV. The energy scale on the upper *x*-axis is derived from the Dutta–Horn model via Eq. (4.3). The stress bias condition is ON state (0.4 V) at 105 °C. (After [129].)

When the assumptions that underlie (4.1) and (4.2) are satisfied, the frequency exponent shows a temperature dependence described by [49, 57]:

$$\alpha(f,T) \;=\; 1-\frac{1}{\ln(f\tau_0)}\left(\frac{\partial\,\ln S_V(T)}{\partial\ln \mathrm{T}}-1\right) \tag{4.3}$$

The self-consistency of Eq. (4.3) for these data is validated by the results of Fig. 4. 10, which shows that the values of the frequency-exponent α extracted from the noise data for both unstressed and stressed devices agree well with the calculated values using Eq. (4.3) and $\tau_0 = 5 \times 10^{-11}$ s, justifying the use of the Dutta-Horn model of LF noise to estimate effective defect-energy distributions [49, 57]. Stressing the device with V_{DS} = 5 V under the ON state does not change the noise magnitude. Three peaks in noise magnitude vs. temperature curves are observed in Fig. 4. 9 at ~100 K

(0.18 eV), ~190 K (0.34 eV), and ~290 K (0.51 eV). Potential defect identifications are discussed in Section 4.4.

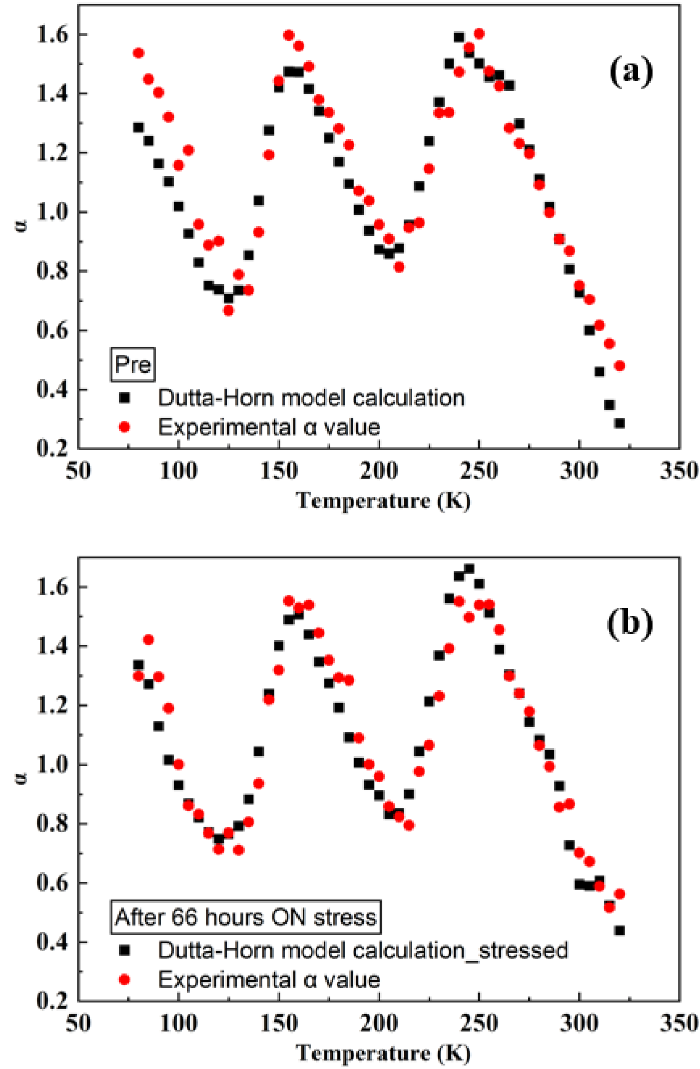

Fig. 4. 10 Experimental and calculated (from Eq. (4.3)) frequency exponents α for (a) unstressed devices and (b) devices stressed under ON-state conditions. (After [129].)

4.4 Discussion

Defects in both the AlGaAs spacer and GaAs buffer may contribute to the LF noise of these devices. Fig. 4. 11 shows a schematic band diagram appropriate for the tested AlGaAs/InGaAs/GaAs PHEMTs at room temperature. Experimental band gaps and electron affinities were self-consistently defined for each layer of the tested devices [139]. For

InGaAs/GaAs, the valence- and conduction-band offsets are 0.2 eV and 0.36 eV, respectively. For the devices under test, the expected valence- and conduction-band offsets between AlGaAs and InGaAs are 0.24 eV and 0.62 eV, respectively, as indicated in Fig. 4. 11. While strain in the InGaAs layer should lead to a small upward shift of both the valence and conduction bands, with a slight narrowing of the gap [140, 141], the band offset between the InGaAs channel and GaAs buffer in Fig. 4. 11 remains consistent with measured values [140-143].

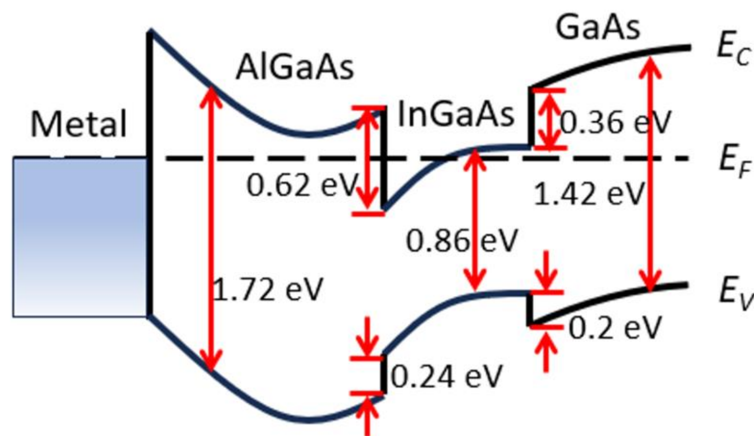

Fig. 4. 11 Band diagram at room temperature for the commercially available AlGaAs/InGaAs/GaAs PHEMTs tested in this work. Band gaps appropriate for tested devices and electron affinities are from Ref. 139. (After [129].)

We note first that the antisite-complex EL2 defect is commonly observed in GaAs, but its energy level is ~0.75 eV from the GaAs conduction band edge, which is too deep to be of relevance to the LF noise measurements of this study [144-160]. However, DFT calculations indicate that isolated tetrahedrally symmetric AsGa has a +/0 charge transition level that is ~0.5 eV below the GaAs conduction band [159], which makes the As_{Ga} a plausible candidate for the large magnitude, wide peak at ~0.5 eV in Fig. 4. 9. Oxygen is a common impurity in GaAs grown through a variety of methods [146, 152-154, 157, 160], including molecular beam epitaxy (MBE) and metal-organic chemical-vapor-deposition (MOCVD). Recently, the O_{As} defect was proposed [136] as a possible

contaminant-related defect in GaAs based on reanalysis of thermal generation rate studies on p-i-n-i-p GaAs structures grown by molecular beam epitaxy [155, 156]. In Ref. 136, these levels were calculated to be 0.62 eV and 0.49 eV below the GaAs conduction band for +/0 and 0/– transitions, respectively. Thus, charge exchange between these defects and the GaAs conduction band also may contribute to the broad noise peak around ~0.5 eV in Fig. 4. 9.

DLTS measurements on AlGaAs samples with similar molar composition to the devices of this work have identified peaks that are ~0.25 eV to ~0.35 eV below the conduction-band edge, attributed to dopant-based DX centers [145, 161-164]. These DX centers in AlGaAs may potentially contribute to the ~0.34 eV noise peak in Fig. 4. 9. In addition, calculations by Colleoni and Pasquarello show that complexes of arsenic antisites (As_{Ga}) with O_{As} impurity centers are more thermodynamically stable in GaAs if allowed to bind; these defects may contribute to Fermi-level pinning in GaAs [160]. Their calculation places the +/- defect level 1.17 eV above the GaAs valence band. Thus, ionization of the defect to the GaAs conduction band occurs at ~0.3 eV, which is also consistent with the middle noise peak in Fig. 4. 9.

We now extend the work of Ref. 136 to consider the possibility that As_{Ga}-O_{As} complexes may occur in the AlGaAs. The relevant density-functional-theory calculations utilize the same base parameters as in Ref. 136. For AlGaAs, a quarter of the Ga atoms were substituted with Al in a checkboard pattern at a lattice constant of 5.65 Å. The HSE06 functional mixing parameter of α = 0.27 provides a theoretical band gap of 1.83 eV, which lies between measured high-temperature [139] and low-temperature values [165]. Results are shown in Fig. 4. 12.

Structurally, O_{As} behaves similarly in AlGaAs and GaAs, with an approximately T_d-symmetric

structure in the positive charge state, as depicted in Fig. 4. 12(a). The oxygen sinks into the backbone in the negative charge state, for which there are two symmetrically distinct distortions. The O_{As} impurity center is amphoteric with charge transition levels of $\varepsilon(+/-) = 0.96$ eV and $\varepsilon(+/-) = 0.94$ eV, respectively. These levels are too deep, relative to the AlGaAs conduction band, to contribute to the low-frequency noise. However, if activated during stress, these levels could potentially contribute to the small V_{th} shifts in Fig. 4. 2.

For antisite-O_{As} complex, depicted in Fig. 4. 12(b), if the antisite occurs at one of the three neighboring Ga sites, a charge transition level is introduced at $\varepsilon(+/-) = 1.31$ eV, relative to the valence band (~0.52 eV below the calculated conduction band). Therefore, it is possible that As_{Ga}-O_{As} defects may contribute to the fairly large, broad peak at ~0.51 eV in LF noise observed in Fig.4. 9. Calculations were also performed on the defects similar to the $2As_{Ga}$-O_{As} defect considered in Ref. 154, as shown in Fig. 4. 12(c). This complex is found to have a level consistent with the As_{Ga}-O_{As} complex. We note that energy levels in the 0.45 eV to 0.49 eV range have been observed via DLTS [145, 166, 167] and temperature-dependent Hall measurements [168] of similar-stoichiometric AlGaAs samples known to contain oxygen impurities, supporting this possibility.

When in the negative charge state, the O_{As} defect breaks the tetrahedral T_d symmetry and relaxes into the lattice backbone, as noted in Ref. 136, and as shown on the left side of Fig. 4. 12(d). Accounting for degeneracy for this relaxation, the defect may distort in one of six different directions. The symmetric T_d structure (right side of Fig. 4. 12(d)) is metastable and 0.08 eV higher in energy. When accounting for the degeneracy of the distortion and energy difference via Boltzmann statistics, the vast majority of O_{As} defects will be in the distorted structure.

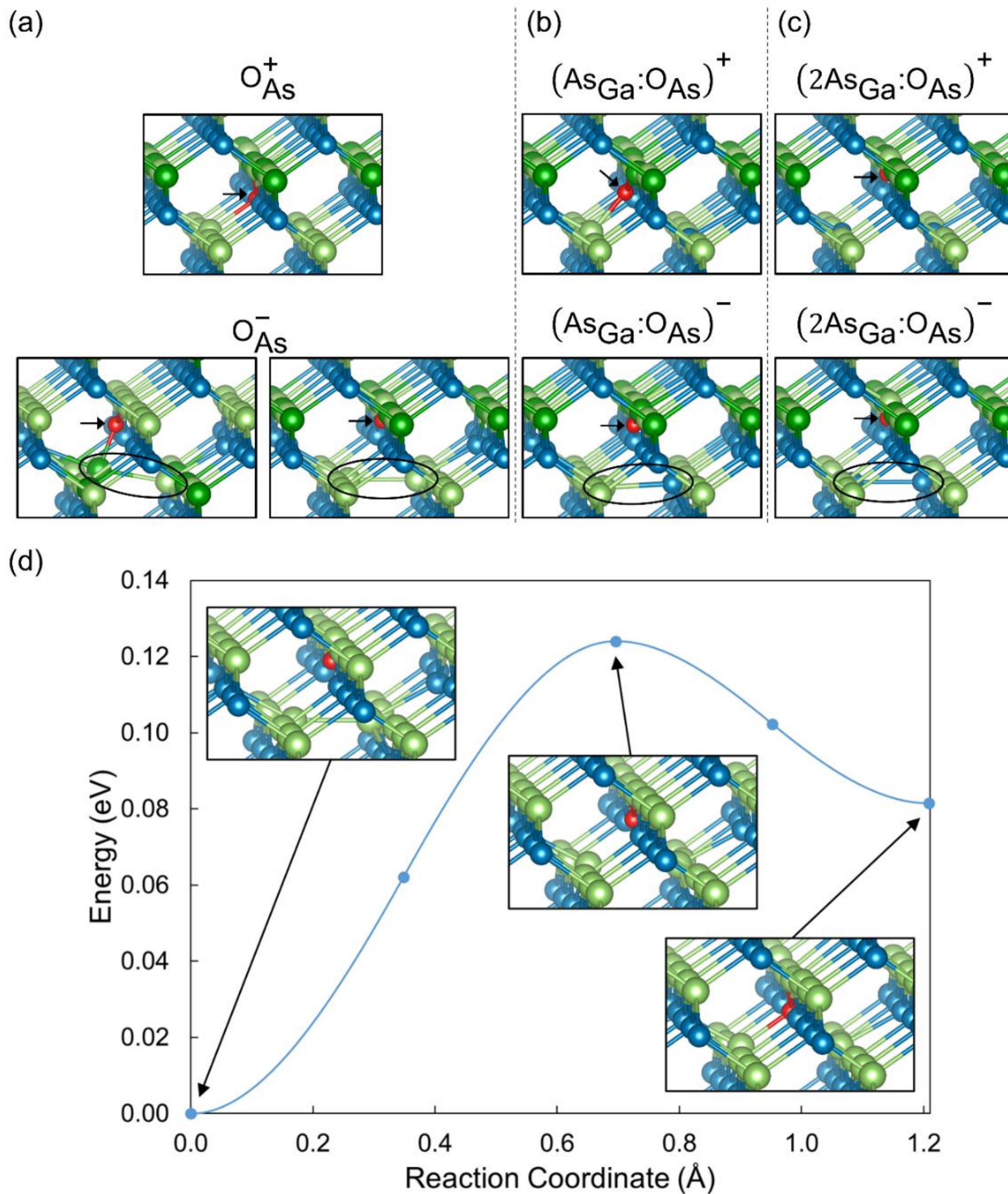

Fig. 4. 12 (a)-(c) Atomistic structures for oxygen-related defects in AlGaAs. Ga is light green, Al is dark green, As is blue, and O is red. (a) O_{As} defect in the positive state (top) with approximate T_d symmetry and two variants of the negative state (bottom) where the oxygen sinks into the backbone (arrow) allowing for cation-cation bonding (circled). (b) As_{Ga}-O_{As} defect in the positive state (top) where the oxygen pushes away from the antisite (C_{3v} symmetry), and negative charge state (bottom) where the oxygen sinks into the backbone and the remaining cation and antisite bond (circled). (c) $2As_{Ga}$-O_{As} defect where the oxygen sinks into the backbone in both charge states (top, bottom), but the antisites bond in the negative charge state (circled). (d) Energy barrier calculation for reconfiguration of the distorted O^-_{As} defect passing through the T_d symmetry structure. The reaction coordinate is an effect coordinate mapping all atomic shifts to a single coordinate along the minimum energy pathway. (After [129].)

The calculated energy barrier to switch from the distorted symmetry to the T_d symmetry (and likewise to over switch from one distorted direction to another) is 0.124 eV, as shown by the peak in Fig. 4. 12(d). Within the accuracy of such calculations, this provides a plausible assignment of the ~0.18 eV peak in Fig. 4. 9 as an O_{As} defect reconfiguration. We note that a similar "DX-like" relaxation of O_N-related impurity centers in AlGaN is inferred to contribute significantly to LF noise in the same energy region for AlGaN/GaN HEMTs [19, 58, 126, 135, 157, 169].

4.5 Summary and Conclusions

In summary, we have investigated the gate bias dependence of hot carrier effects in industrial-quality AlGaAs/InGaAs/GaAs PHEMTs at fixed drain bias (5 V) at temperatures up to 105 °C. A small positive shift of the threshold voltage V_{th} and negligible degradation in peak transconductance G_M were observed after the ON-state bias stressing, emphasizing the stability of these devices. The gate-voltage dependence of the low-frequency $1/f$ noise indicates that the defect-energy distribution of the devices varies strongly with energy. Temperature dependent $1/f$ noise measurements identify prominent traps at ~0.51 eV, ~0.34 eV, and ~0.18 eV. The noise magnitude is not significantly affected by stress.

Literature studies and our calculations provide strong evidence that the three observed noise peaks originate primarily from As antisite defects and various configurations of substitutional oxygen impurity centers in the GaAs buffer and AlGaAs barrier layers. The ~0.51 eV peak likely includes contributions from isolated As_{Ga} antisites in GaAs, along with potential contributions from O_{As} impurity centers in GaAs and As_{Ga}-O_{As} impurity complexes in AlGaAs. The ~0.34 eV peak is likely to include contributions from dopant-based DX centers in AlGaAs and/or substitutional As_{Ga}-

O_{As} complexes in GaAs. A plausible origin for the ~0.18 eV noise peak is structural reconfiguration of the O_{As} impurity center in GaAs or AlGaAs, akin to the DX relaxation of the O_N impurity center in AlGaN.

CHAPTER 5 Low-Frequency Noise and Deep Level Transient Spectroscopy in *n-p-n* Si Bipolar Junction Transistors Irradiated with Si Ions

This chapter is adapted from "Low-Frequency Noise and Deep Level Transient Spectroscopy in n-p-n Si Bipolar Junction Transistors Irradiated with Si Ions" published in IEEE Transactions on Nuclear Science, and has been reproduced with the permission of the publisher and my co-authors Jossue Montes, Sabina D. Koukourinkova, Bastiaan L. Vaandrager, Edward S. Bielejec, Gyorgy Vizkelethy, Ronald D. Schrimpf, Daniel M. Fleetwood, and En Xia Zhang.

- X. Luo et al., "Low-Frequency Noise and Deep Level Transient Spectroscopy in *n-p-n* Si Bipolar Junction Transistors Irradiated with Si Ions," *IEEE Transactions on Nuclear Science*, vol. 71, no. 4, pp. 591-598, Apr. 2024.

5.1 Introduction

Bipolar junction transistors (BJTs) are widely used in many electronic systems due to their high driving capability, linearity, and speed advantages [170, 171]. The reliability of BJTs in space systems and their radiation responses have been extensively studied since the 1950s [171-173]. Heavy ion-induced degradation has been studied via deep level transient spectroscopy (DLTS). Several defects that are important to the BJT radiation response have been identified [174-178]. In addition, Li et al. have employed DLTS measurements to investigate synergistic effects of ionization and displacement defects *in n-p-n* BJTs irradiated by heavy ions [179, 180].

Low-frequency (LF) noise measurements can also provide insight into the density and energy distributions of defects in microelectronic devices and materials [49, 57, 88]. Numerous studies of as-processed and irradiated devices have shown that the LF noise is more strongly affected by defects at the interface of the oxide that overlies the emitter-base (EB) junction than by bulk defects within the junctions [59-64, 181].

In this work, we perform DLTS and LF noise measurements to evaluate the types of defects and resulting defect energy distributions before and after 17 MeV Si ion irradiation of 2N2222A *n-p-n* Si BJTs. DLTS measurements identify four prominent defect levels in the bulk Si that are introduced by irradiation in the base-collector junction of these transistors. Temperature-dependent $1/f$ noise measurements identify at least two defect levels, one of which appears to be similar to levels identified via DLTS, and the other that is likely associated with oxygen vacancies and hydrogen complexes in the interfacial oxide layer that overlies the EB junction. These results demonstrate that DLTS and LF noise methods provide complementary information about defects in linear bipolar devices.

5.2 Experimental Details

Devices under test (DUTs) were Central Semiconductor 2N2222A *n-p-n* Si BJTs, which is a general purpose, low power planar epitaxial transistor commonly used in space and defense systems. See Fig. 5. 1(a) for a schematic diagram [182]. The base doping and collector doping of the DUT are ~3.4×10^{16} cm^{-3} and ~4×10^{14} cm^{-3}, respectively. 17 MeV Si ions are chosen to create end-of-range defects, mimicking neutron cluster damage primarily caused by silicon recoils [68, 178, 183]. SRIM simulation in Fig. 5. 1(b) shows that the range of the 17-MeV Si ions in silicon is 6.44 μm, consistent with the collector depth. Ion irradiations were performed at the Ion Beam Laboratory at Sandia National Laboratories up to a fluence of 10^{10}/cm^2. The beam was focused to a size somewhat larger than the transistor die (~0.5×0.5 mm^2). All device terminals were grounded during irradiation.

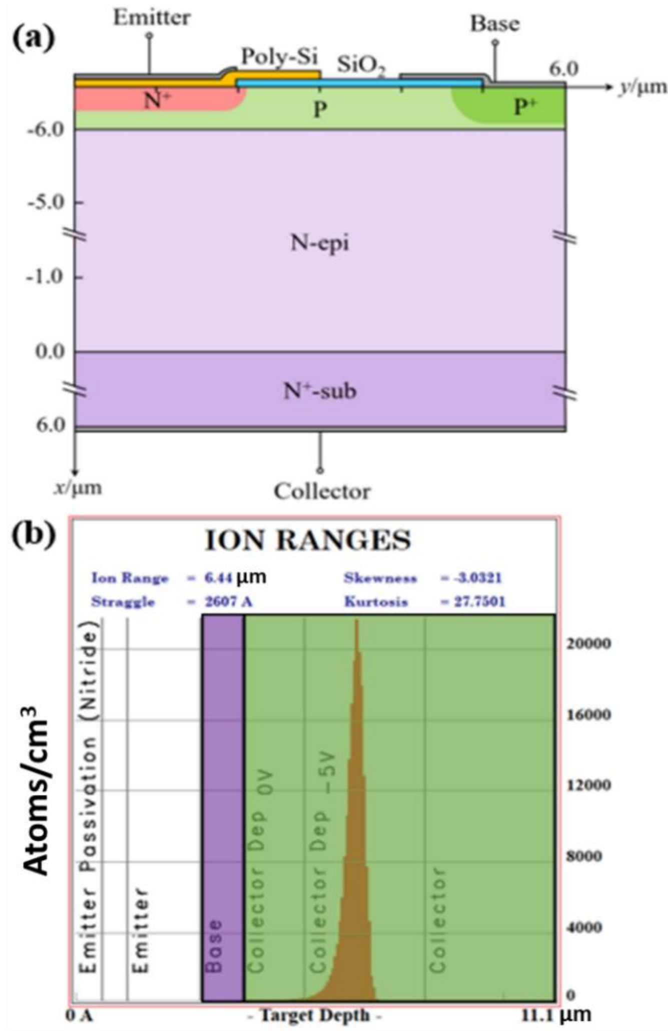

Fig. 5. 1 (a) Schematic cross section of a 2N2222A *n-p-n* Si BJT. (After [182]). (b) The number of vacancies as a function of depth in *n-p-n* BJTs induced by a single 17 MeV Si ion impact (simulated by SRIM). (After [184].)

Defects at the base-collector depletion zone in the collector of these devices are most efficiently probed via DLTS measurements [174, 175, 177, 178] because of the relatively low doping and large depletion width of the N-epi layer [174]. Thus, DLTS measurements were performed after ion irradiation with the base-emitter junction shorted using a filling pulse amplitude of 5 V, a quiescent reverse bias of −5 V, a 1 ms fill pulse, and 100 ms transient length. Changes in capacitance were measured during temperature scans from 60 K and 325 K and the measurements were analyzed using standard techniques [175, 185].

The Forward Gummel characteristics of the samples were measured with a HP4156 semiconductor parameter analyzer before and after Si ion irradiation at fluences from 10^6/cm^2 to 10^{10}/cm^2 in a common-emitter configuration. The base-emitter junction bias V_{BE} of the samples was swept from 0 V to 1 V at V_{CE} = 1 V during measurement [186, 187]. Ten devices were tested from the same diffusion lot. To within ± 3% experimental uncertainty, as-processed devices exhibited identical *I-V* and *C-V* characteristics (not shown). Typical results are reported in this work.

LF noise measurements were performed as a function of base current and temperature with BJTs biased in a common-emitter configuration [59]. The measurement system was shown in Fig. 2. 8. To measure the current noise of the BJT, a low-noise metal film resistor R_L (typically ~1 kΩ) was placed in series with the collector. The collector bias was chosen to operate the device in the active region. The noise signal of the voltage power spectral density S_{VC} from the collector biasing resistance R_L was measured at a constant I_B at frequencies from 3 Hz to 390 Hz. Base current fluctuations S_{IB} were extracted via the relation $S_{IB} = \frac{S_{VC}}{R_L^2 \beta^2}$, where β is the current gain [59-64].

5.3 Experimental Results and Discussion

5.3.1 Electrical Characteristics

The room-temperature forward Gummel characteristics are shown in Figs. 5. 2(a) and 2(b) before and after irradiation with different ion fluences. The base current I_B gradually increases with Si ion fluence and is more sensitive to the radiation damage than I_C [186, 187]. Si ions induce ionization and displacement damage in BJTs leading to an increase in carrier recombination and degradation in β [186]. The recombination current in the emitter-base junction varies as

exp (V_{BE}/nV_T), where V_{BE} is the bias voltage across the emitter-base junction, n is the ideality factor and V_T is the thermal voltage [186, 187]. The ideality factor n for I_B increases with increasing fluence from 1.02 to 1.36 in Fig. 5. 2(b). In BJTs, recombination in the neutral base exhibits an ideality factor n = 1; an ideality factor n = 2 is associated with recombination in the emitter-base depletion region [170, 186, 187]. Hence, for these devices the percentage of emitter-base depletion recombination current increases with ion exposure [186-188].

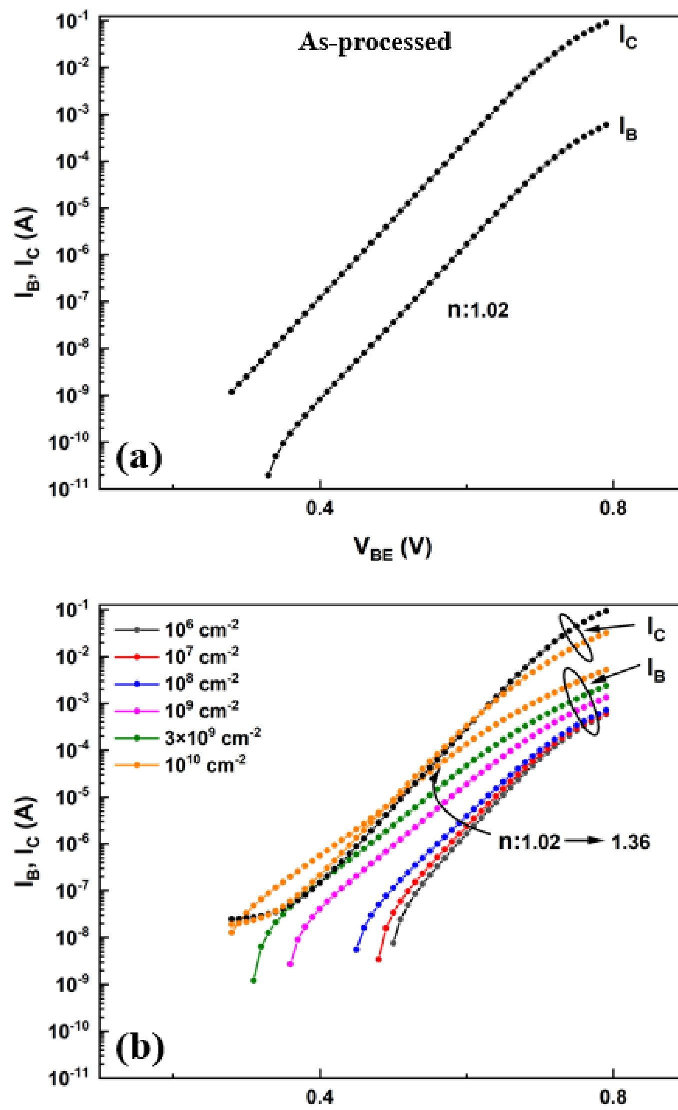

Fig. 5. 2 Room-temperature forward Gummel plots for 2N2222A n-p-n Si BJTs at V_{CE} = 1 V (a) before and (b) after 17 MeV Si ion irradiation up to a fluence of 10^{10}/ cm^2. The extracted ideality factor n is shown in (b). (After [184].)

The change in the reciprocal of the gain variation ($\Delta(1/\beta)$) is defined as the value after irradiation minus the initial gain, $\Delta(1/\beta) = 1/\beta - 1/\beta_{\text{As-processed}}$. Fig. 5. 3 shows $\Delta(1/\beta)$ at $V_{BE} = 0.65$ V as a function of fluence for 17 MeV Si ion irradiation of the *n-p-n* Si BJT devices. The values of $\Delta(1/\beta)$ increase linearly with ion fluence, and are suitably characterized by the Messenger–Spratt equation [178, 189]:

$$\Delta(1/\beta) = K\Phi. \tag{5.1}$$

Here, K is the damage factor and Φ is the incident particle fluence.

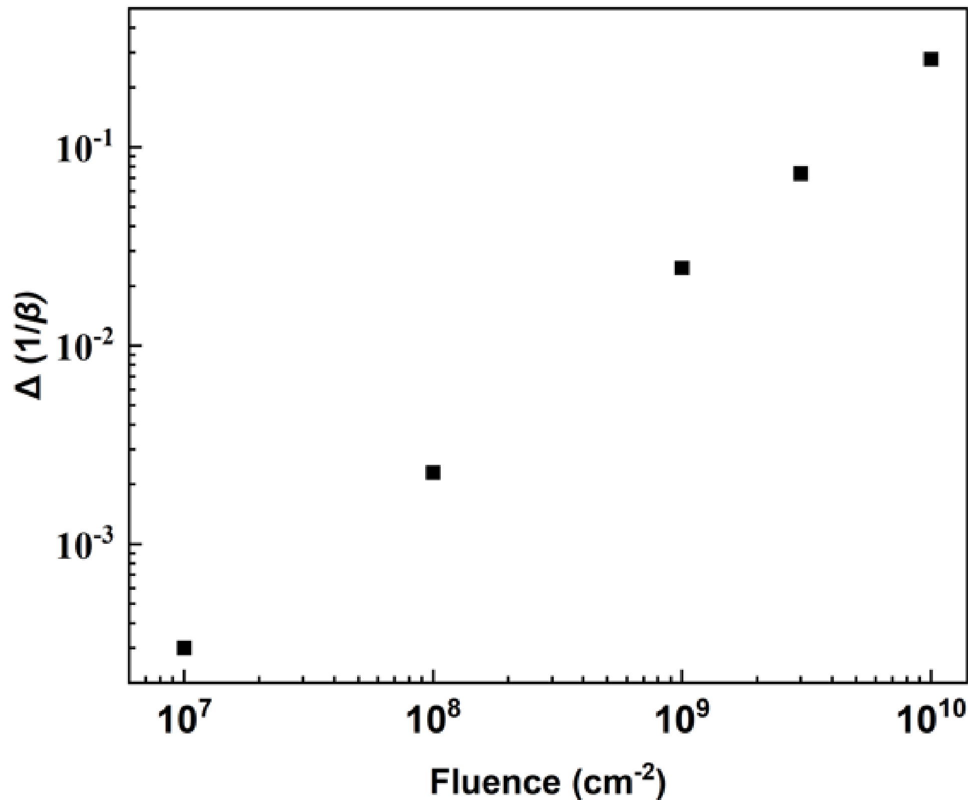

Fig. 5. 3 Changes in the reciprocal of current gain ($\Delta(1/\beta)$) as a function of fluence for *n-p-n* Si BJTs irradicated by 17 MeV Si ions ($V_{BE} = 0.65$ V). (After [184].)

5.3.2 DLTS measurements

Fig. 5. 4(a) shows DLTS spectra of the base-collector junction of the *n-p-n* Si BJT devices at a Si ion fluence of 10^9/cm^2 at four rate windows ranging from 4.3 ms to 43 ms. Four major peaks are

observed in the spectra; the corresponding Arrhenius plots associated with these peaks are shown in Fig. 5. 4(b). Vacancies, interstitials, and point defect/impurity complexes lead to various defect levels in the Si band gap, resulting in the degradation of current gain of BJTs [68, 183]. Three of four peaks in Fig. 5. 4 (a) correspond to classic defects in Si [178, 190-193]. The vacancy-oxygen (VO) trap produces a level at ~0.17 eV below E_C and a DLTS peak at ~90 K [175-178, 190-192]. The shallow divacancy in Si (V_2 (=/−)) has a level at ~0.24 eV below EC corresponding to ~140 K [190-193]. The peak at ~230 K ($E_C - 0.43$ eV) is composed of the vacancy phosphorous (VP), the divacancy (V_2 (−/0)) and other complex defects such as E5 centers [175, 177, 178, 190-193]. The defect level at ~280 K (~0.53 eV) appears to be unique to these Central Semiconductor *n-p-n* Si BJTs; this trap evidently is purposefully created to reduce carrier lifetimes in the as-processed devices.

Fig. 5. 4(c) shows DLTS spectra at the rate window of 4.3 ms as a function of fluence. In the DLTS spectra, the peak height is proportional to the trap concentration [185]. Increasing fluence yields higher defect amplitudes in the DLTS spectra at ~230 K. Thus, deeper levels, such as V_2 (−/0) and E5 centers are the critical defects that degrade the current gain in these devices [175, 177]. In contrast, a decrease in the peak at ~280 K is observed, suggesting passivation of the defects at the ~0.53 eV energy level in the as-processed devices via ion exposure. The densities of VO and V_2 (=/−) increase at fluences up to 10^9/cm^2 and then decrease at higher fluences. This is because the defects at ~230 K cause band bending and those shallow levels are no longer filled at higher ion fluences [177].

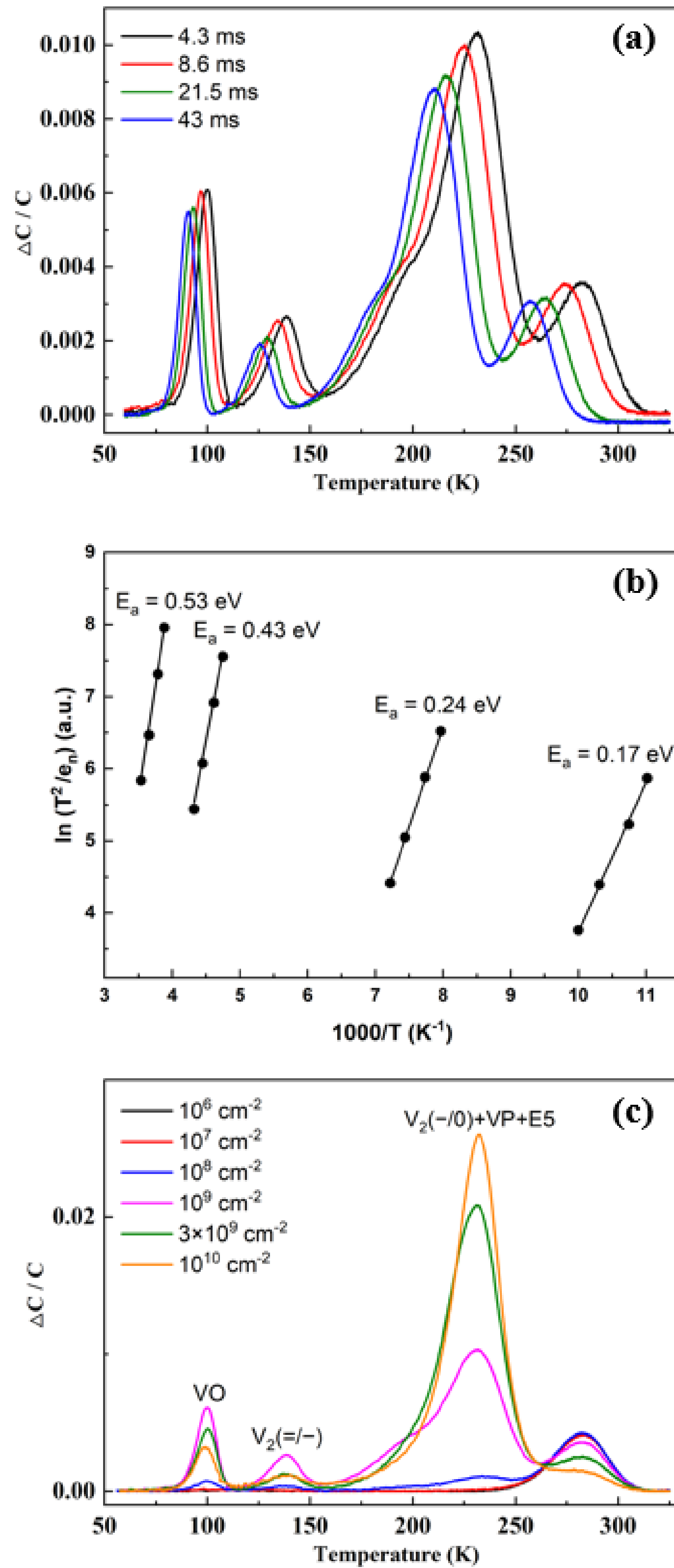

Fig. 5. 4 (a) Normalized DLTS spectra at different rate windows of the base-collector junction in the *n-p-n* Si BJT devices at a Si ion fluence of 10^9/cm^2 and (b) the Arrhenius plots corresponding to the four DLTS peaks. (c) Normalized DLTS spectra at the rate window of 4.3 ms vs. fluence for Si ion irradiations up to a fluence of 10^{10}/cm^2. (After [184].)

5.3.3 Low-frequency noise measurements

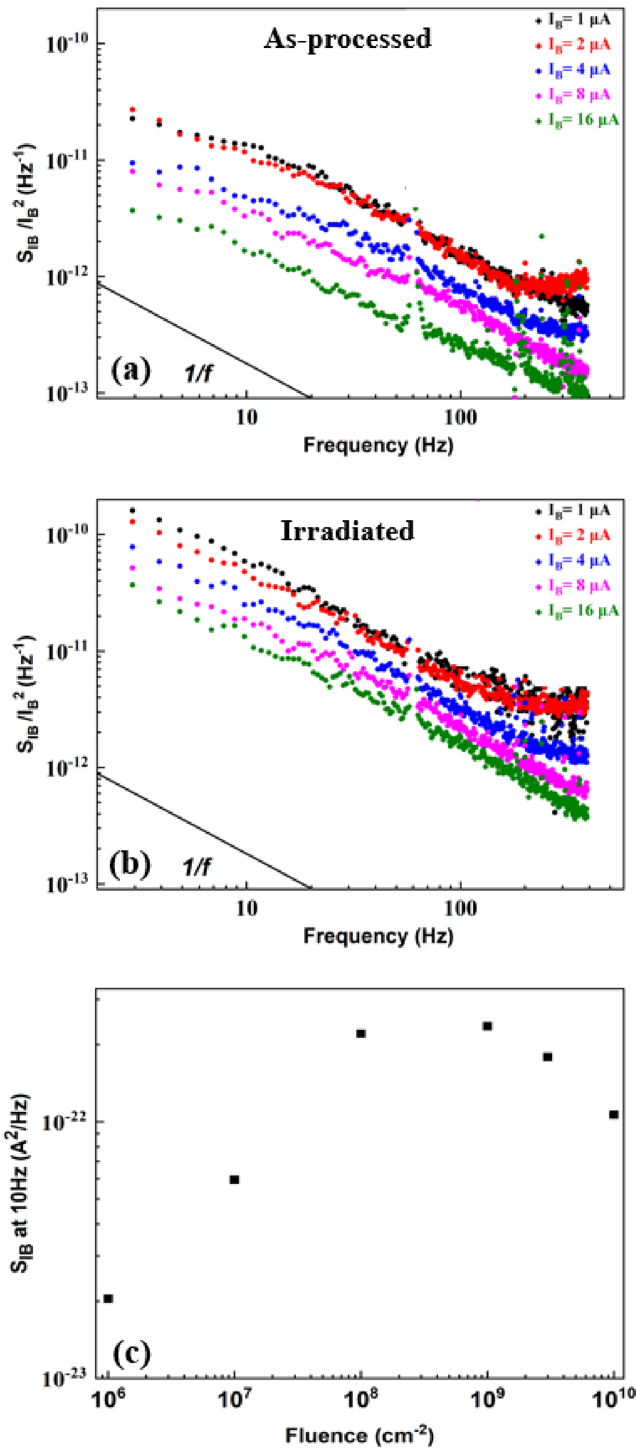

Fig. 5. 5 Normalized current-noise power spectral density, S_{IB}/I_B^2, vs. f at various I_B for *n-p-n* Si BJTs (a) as-processed, and (b) post-irradiation. (c) Effects of irradiation on the fluence dependence of the noise at 10 Hz with I_B = 2 μA. Devices were operated in the active region. Unwanted spikes from 60-Hz pickup and harmonics are removed. (After [184]).

Fig. 5. 5 shows extracted base noise current power spectra density S_{IB} normalized by I_B^2 with I_B

varying from 1 μA to 16 μA for (a) an as-processed device and (b) an irradiated device at the Si ion fluence of 10^{10}/cm^2. The noise magnitude increases significantly after irradiation. The spectra exhibit $1/f^{\alpha}$ frequency dependences for most frequencies and values of I_B, and are generally similar in shape to those observed in other Si BJTs [59-64]. The fluence dependence of S_{IB} at 10 Hz and I_B = 2 μA is shown in Fig. 5. 5(c). The noise level increases to fluences up to 10^9/cm^2 and then decreases slightly at higher fluences. This trend is similar to that of the densities of VO and V_2 defects (=/−) in DLTS, for example.

As we have discussed in Chapter 2, if the noise is caused by a random thermal-activated process that exhibits a broad distribution of energies $D(E_0)$ relative to kT, the frequency exponent shows a temperature dependence described by Eq. 2.2, thus enabling one to estimate the defect energy distribution through the temperature dependent noise data. In Eq. 2.2, τ_0 is set to 1.8×10^{-15} s based on experimental studies of the charge trapping and emission kinetics of oxide and border traps near the Si/SiO_2 interface. From measurements of the temperature dependence of S_V, we estimate the defect-energy distributions $D(E_0)$ [57], via Eq. 2.4. We note that Dutta-Horn analysis has been shown to be applicable to noise due to both carrier-number and carrier-mobility fluctuations [49, 51, 89, 102, 194]. Fluctuations in both carrier number and mobility likely occur in these devices [59-64, 181].

Temperature-dependent *1/f* noise measurements were performed from 80 K to 380 K in steps of 10 K. During noise measurements, the device was biased at I_B = 2 μA and operated in the active mode. In the literature, it is unusual to find temperature-dependent noise measurements for linear bipolar transistors. Understanding their capabilities and potential limitations is, therefore, important

not only to this study but to future work on defect characterization.

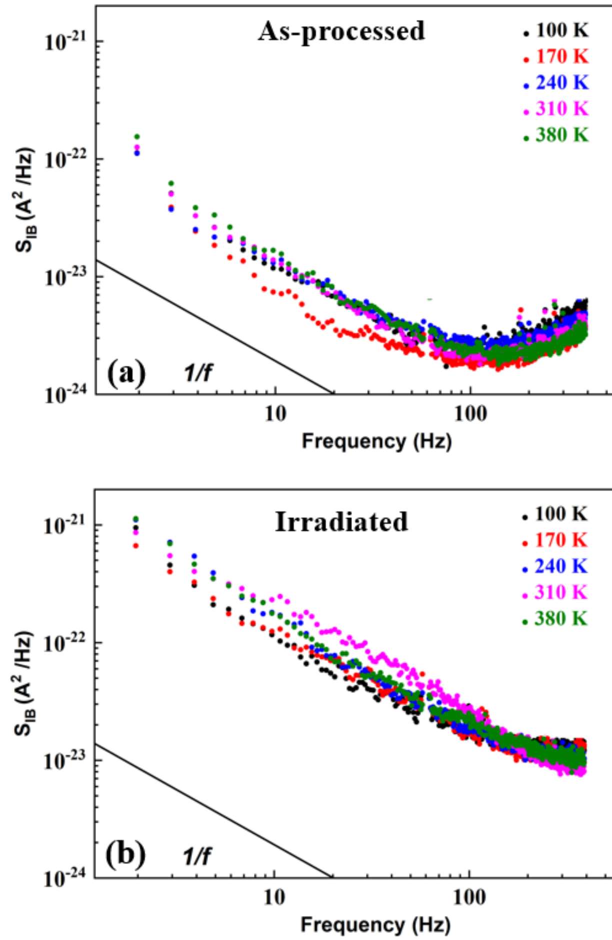

Fig. 5. 6 Current-noise power spectral density, S_{IB}, vs. f at various temperatures for *n-p-n* Si BJTs (a) before and (b) after a fluence of 10^{10}/ cm^2 17 MeV Si ion irradiation. Unwanted spikes from 60-Hz pickup and harmonics are removed. (After [184].)

Fig. 5. 6 shows noise spectra in the 2N2222A *n-p-n* Si BJTs at selected temperatures before and after Si ion irradiation. For the as-processed device, $1/f$ noise dominates over S_{IB} for the lower-frequency range, $f < 100$ Hz. S_{IB} is of the "generic" $1/f^{\alpha}$ type in irradiated devices [49, 57]; the extracted frequency exponent α varies between 0.9 and 1.1. As shown in Figs. 5. 6(a) and (b), the noise magnitudes are much higher for the irradiated devices than the as-processed devices owing to ion-induced defect creation. The upturn in noise at frequencies above ~ 100 Hz is attributed to diffusion noise caused by fluctuations in carrier density and mobility in the base [59-64]. This noise

is significant to the performance and reliability of linear *n-p-n* transistors but does not scale with fluence or effective defect density in the same way as the lower-frequency noise which behaves more similarly to the noise in MOS devices [49, 57]. This suggests that the noise below ~100 Hz may have a surface origin, e.g., resulting from fluctuations in the carrier density due to charge trapping and emission at the upper surface between the base-emitter junction and the base oxide (Fig. 5. 1) [49, 57, 89, 102, 186, 194].

Fig. 5. 7 shows the normalized low-frequency noise $S_{IB}*f/T$ as a function of temperature at f = 20 Hz and I_B = 2 μA for the devices before and after Si ion irradiation. After irradiation, the noise magnitude increases significantly with increasing fluence. The energy scales on the upper *x*-axis in Fig. 5. 7 are derived from the Dutta–Horn model via Eq. 2.4. These scales are sensitive to the chosen value of τ_0 in Eq. 2.2 and Eq. 2.4. Due to the logarithms in these expressions the energy scale only changes by 10-15 % when τ_0 is varied by several orders of magnitude [57, 102].

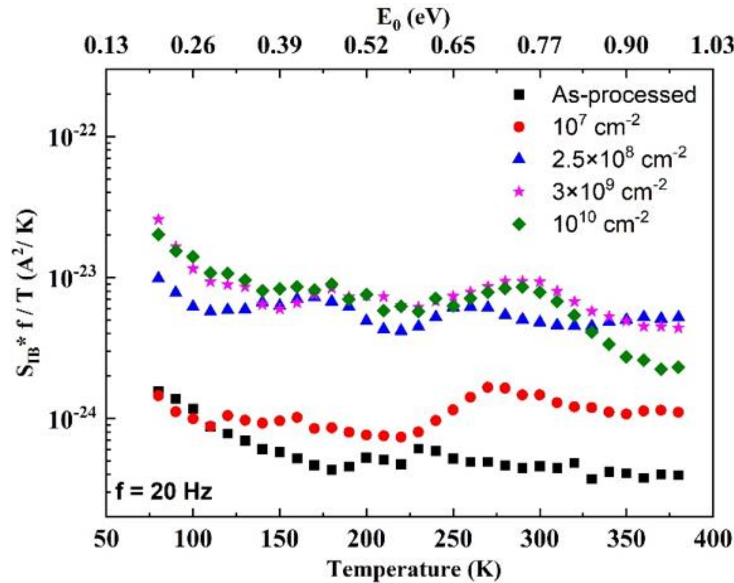

Fig. 5. 7 Normalized 1/*f* noise for *n-p-n* Si BJTs as a function of temperature from 80 K to 380 K at f = 20 Hz and I_B = 2 μA. (After [184].)

The applicability and validity of the Dutta-Horn model of 1/*f* noise to the devices of this work

is demonstrated by the results of Fig. 5. 8. The measured values of the frequency exponent α from noise data for the devices before and after a fluence of 10^{10}/cm^2 Si irradiation agree well with Eq. 2.4 [57]. The applicability of the Dutta-Horn analysis confirms that the noise in Si BJTs is caused by thermally activated processes. The energy scale in Fig. 5. 7 differs from that in Fig. 5. 4 by 15-20% due to the small differences in the rate windows, the uncertainties in the values of τ_o, and the differences in the approximations made in the treatments of the Arrhenius prefactors in the DLTS analysis [185] and Dutta-Horn theory [57]. Similar offsets can be observed between the energy scales for 1/*f* noise and thermally stimulated current measurements [89]. The resulting differences are within the combined uncertainties of the respective methods [57, 89, 185]. In Section 5.3.4, we focus primarily on comparisons between the temperatures of observed peaks in Figs. 5. 4 and 5. 7 to avoid uncertainties in the respective energy scales.

After irradiation of the devices to a fluence of 10^7/cm^2, a noise peak is observed at ~270 K. After further irradiation of the devices to 10^{10}/cm^2, broad peaks centered at ~180 K and ~290 K are observed. In MOS devices, these border traps leading to 1/*f* noise are often associated with a distribution of defects, including oxygen vacancies and hydrogen complexes [49, 89, 102]. Recently, contributions to 1/*f* noise that result from the sequential, reversible activation and passivation of interface traps have also been identified [194]. Such defects may well contribute to the noise in these devices if located at the interface of the base oxide and the base-emitter junction, for example [186]. However, bulk defects are also likely to contribute to the observed noise in linear bipolar transistors [59-64, 194].

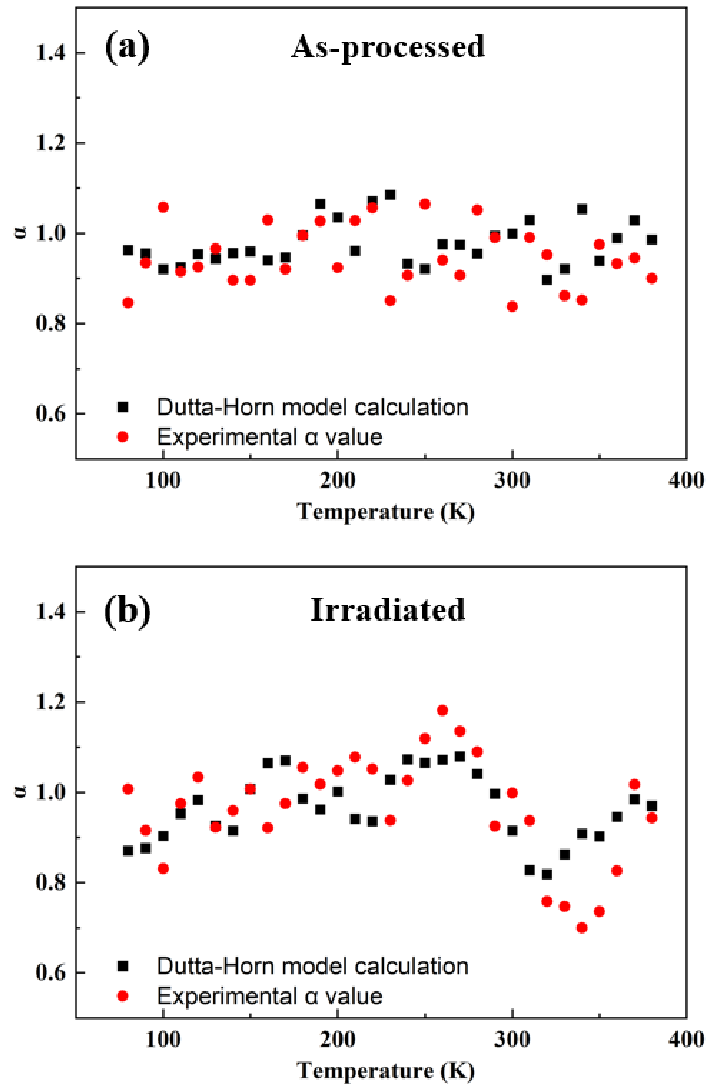

Fig. 5. 8 Experimental and calculated (from Eq. 2.4) frequency exponents α for device (a) before and (b) after a fluence of $10^{10}/cm^2$ Si irradiation with S_{IB} at 20 Hz. (After [184].)

5.3.4 Comparison of DLTS and 1/*f* noise

While DLTS primarily senses defects at the base-collector junction of the BJT and the 1/*f* noise appears to be more sensitive to defects at the base-emitter junction with the base oxide (Fig. 5. 1), it is still interesting to see how the effective defect energy distributions may compare for the two techniques. As in earlier comparisons of 1/*f* noise and thermally stimulated current measurements in MOS devices [89], these results illustrate how each method may reinforce and/or complement results of the other.

Comparing Figs. 5. 4 and 5. 7, VO defects are clearly visible at ~100 K in the DLTS spectrum, and there is an upturn in noise magnitude at temperatures below 100 K that could be associated with the same defect. However, neutral hydrogen diffusion occurs with similar energy levels [195, 196], so hydrogen-induced trap activation and passivation may also play a role in the $1/f$ noise at these temperatures [194]. The small V_2 peak at ~140 K in the DLTS spectrum in Fig. 4 is matched by a small upturn in noise magnitude in Fig. 5. 7 at similar temperatures. However, H_2 diffusion and reactions with charged defects also occur with similar activation energies near Si/SiO_2 interfaces [197-199], providing an alternative explanation for the noise results [200, 201].

The large peak at ~240 K in DLTS in Fig. 5. 4 is entirely missing from the $1/f$ noise measurements. Hence, the defects in this case are clearly affecting primarily the base/collector interface upon which the DLTS measurements are focused [174-178]. The absence of this peak in the noise measurements shows its insensitivity to defects at this junction for these devices. Interestingly, at 280 K both DLTS and $1/f$ noise show prominent defects. However, inferred concentrations of these decrease with fluence during DLTS measurements and increase with fluence during noise measurements, suggesting that the two defects most likely differ in microstructure and/or location. The peak in noise measurements at these energies has been associated with H^+ motion and reactions at or near Si/SiO_2 interfaces [194, 195, 202, 203].

Taken together, the differences in the temperature and fluence dependences of the DLTS and low-frequency noise defect energy distributions in Figs. 5. 4 and 5. 7 show that each method is indeed primarily probing a different region of the linear bipolar transistor. Hence, the two methods provide complementary and not duplicative information about defects in the transistor structure. For

DLTS, primarily bulk defects are observed at the base-collector junction. For low-frequency noise, traps at the junction of the base, emitter, and base oxide evidently play a more significant role. We note that this result contrasts with recent DLTS and low-frequency noise measurements in GaN-based HEMTs in which similar defects are observed via temperature-dependent noise and DLTS measurements [58, 126, 137, 204-206]. The similarity of the results in these cases is most likely because defects and impurities in the GaN buffer layer (e.g., nitrogen vacancies and substitutional iron, Fe_{Ga}) are sensed in both noise and DLTS measurements of GaN-based HEMTs [58, 126, 137, 204-206]. One should not expect such similarity to always occur in other devices, e.g., these linear bipolar transistors.

5.4 Summary and Conclusions

DLTS and low-frequency 1/*f* noise measurements are compared for *n-p-n* Si BJTs as a function of fluence for 17-MeV Si ion irradiation. The base current I_B increases with increasing fluence, and thus the gain degrades. DLTS spectra show that the oxygen vacancy (VO), the shallow divacancy (V_2 (=/−)), and a composition of the vacancy phosphorous (VP), divacancy (V_2 (−/0)) and other complexes such as E5 centers are generated in the base-collector junction of the transistor after irradiation. The underlying mechanisms for the decrease in amplitude of the unique peak at ~280 K with increasing fluence remain under investigation.

The 1/*f* noise magnitude for these devices increases significantly after ion irradiation. A combination of contributions from oxygen vacancies and hydrogen complexes in the oxide that overlies the base-emitter junction is inferred from measurements of the temperature dependence of the noise below 100 Hz, although contributions from bulk defects is also possible. The diffusion

noise at higher frequencies is dominated by fluctuations in carrier number and mobility for transiting carriers in the base. A detailed comparison of the effective energy distributions and magnitudes of the defects identified via DLTS and $1/f$ noise measurements show that these techniques provide complementary information about the performance, fluctuation phenomena, and radiation response of linear bipolar transistors. This contrasts with recent work that shows that DLTS and LF noise measurements sense similar defects in GaN-based HEMTs, for example, reinforcing the benefits of using multiple techniques to characterize defects in semiconductor materials and devices.

CHAPTER 6 Conclusions

This dissertation extensively investigates the reliability and performance degradation mechanisms in different semiconductor devices, with a focus on the effects of electrical stress and radiation.

First, we assessed the stability and reliability of Ge *p*MOS FinFETs, particularly under negative bias temperature stress (NBTS). These advanced Ge-based FinFET devices are fabricated by imec on 300 mm bulk Si (100) wafers with high-k gate stacks. The experimental results and comprehensive analysis reveal that the NBTS-induced degradation Ge FinFETs mainly originates from interface-trap generation, and the activation energies for interface-trap formation are significantly lower than those in comparable Si devices. Reduced activation energies for interface-trap formation in SiGe and/or Ge devices than in Si MOS devices have been attributed to a reduced barrier for hydrogen release from Si dangling bonds in the presence of Ge atoms at the interface. Newly created and/or activated border traps after NBTS related to oxygen vacancies and their complexes with hydrogen are detected via low-frequency $1/f$ noise measurements above ~230 K. The gate–voltage dependence of the $1/f$ noise indicates that the defect energy distributions before and after NBTS are increasing toward midgap in these devices, in contrast with previous results that tend to show *p*MOS defect-energy distributions increasing toward the valence-band edge.

Then we studied the gate bias dependence of hot carrier effects in industrial-quality AlGaAs/InGaAs/GaAs PHEMTs at fixed drain bias (5 V) at temperatures up to 105 °C. A small positive shift of the threshold voltage V_{th} and negligible degradation in peak transconductance G_M were observed after the ON-state bias stressing, emphasizing robust device performance under

typical operational stresses. The gate-voltage dependence of the low-frequency $1/f$ noise indicates that the defect-energy distribution of the devices varies strongly with energy. Temperature dependent $1/f$ noise measurements identify prominent traps at ~0.51 eV, ~0.34 eV, and ~0.18 eV. Literature studies and our calculations provide strong evidence that the three observed noise peaks originate primarily from As antisite defects and various configurations of substitutional oxygen impurity centers in the GaAs buffer and AlGaAs barrier layers.

Finally, we evaluated the degradation and the nature of radiation-induced defects before and after 17 MeV Si ion irradiation of *n-p-n* Si BJTs through DLTS and low-frequency $1/f$ noise measurements. The base current I_B increases with increasing fluence, and thus the current gain degrades. DLTS measurements identify three prominent classic defect levels in the bulk Si that are introduced by irradiation in the base-collector junction of these transistors. A combination of contributions from oxygen vacancies and hydrogen complexes in the oxide that overlies the base-emitter junction is inferred from measurements of the temperature dependence of the $1/f$ noise below 100 Hz, although contributions from bulk defects is also possible. The diffusion noise at higher frequencies is dominated by fluctuations in carrier number and mobility for transiting carriers in the base. A detailed comparison of the effective energy distributions and magnitudes of the defects identified via DLTS and $1/f$ noise measurements show that these techniques provide complementary information about the performance, fluctuation phenomena, and radiation response of linear bipolar transistors.

To summarize, these studies contribute to a broader understanding of the degradation mechanisms and reliability issues in semiconductor devices across different materials and device

architectures. For future research, low-frequency $1/f$ noise measurement remains a valuable tool for enhancing our understanding of defect densities and energy distributions in microelectronic devices.

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