LASER-INDUCED SINGLE EVENT EFFECTS, TOTAL-IONIZING- DOSE EFFECTS, AND LOW-FREQUENCY NOISE IN ADVANCED FINFETS

By

KAN LI

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Approved:

Ronald D. Schrimpf, Ph.D.

Daniel M. Fleetwood, Ph.D.

Robert A. Reed, Ph.D.

Enxia Zhang, Ph.D.

Sokrates T. Pantelides, Ph.D.

Greg Walker, Ph.D

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CHAPTER 1

Introduction

With the goal of lower cost, better performance and higher efficiency, the integrated circuit (IC) industry has made incredible progress following Moore's Law in the past few decades, which states that the number of transistors in a dense integrated circuit doubles roughly every eighteen months [19–22]. Therefore, the key to sustain Moore's Law is the scaling of single transistors, which involves several significant innovations in materials and architecture of MOSFETs. Specifically, strain engineering was introduced in 90 nm technologies to increase the electron and hole mobility [23], Metal-gate/high-k gate stacks were brought in the 45 nm node to reduce the gate leakage and eliminate poly-silicon depletion [24], [25]. As the requirement of channel length scaling entered the sub-30 nm regime, the outstanding electrostatic control of multi-gate device structures makes them preferable for the following generations of CMOS technology nodes.

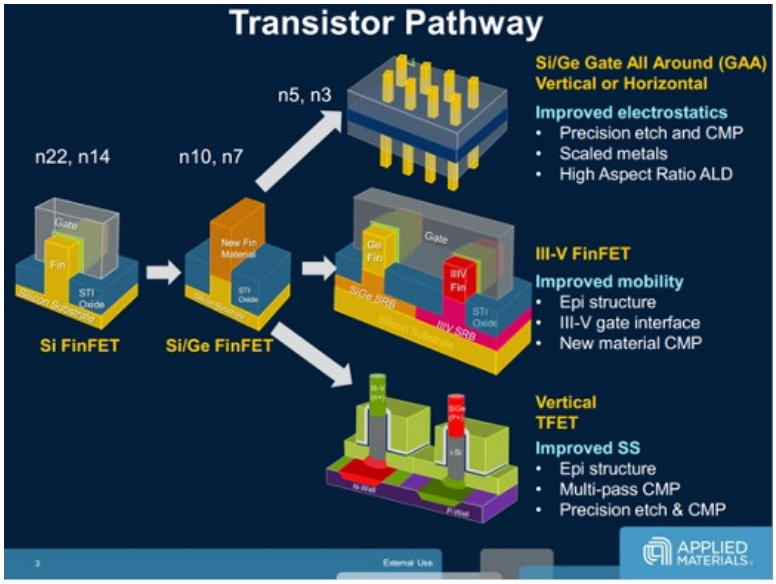


Figure 1.1: Non-planar transistor pathway and illustration of the development in architecture, channel materials and the corresponding fabrication technologies (Source: Ars Technica UK, July, 2016)

Among the multi-gate architectures, FinFETs are highly promising due to their self-aligned multi-gate structure, better compatibility to the conventional planar CMOS process [26], suppression of short channel effects [27–29], and wider application than gate-all-around (GAA) FETs with

current manufacturing technologies. Fig.1.1 shows the ongoing transistor pathway of the non-planar topologies, indicating that advanced FinFETs featuring highly scaled dimensions and/or promising alternative channel materials to silicon maybe be used.

Applying the electronics with these advanced FinFETs in space or other high-radiation environments has been an very important topic as well as a significant concern for human beings. The natural space radiation environment originating from galactic cosmic rays (GCR), solar events, and particles trapped in the Earth's radiation belts can temporarily or permanently degrade the performance of electronic devices, circuits, and systems [30], [31]. These radiation-induced effects in the electronics can be generally grouped into three types: Single Event Effects (SEEs), Total-ionizing-Dose (TID) effects, and Displacement Damage (DD). SEEs occur when high energy particles pass through the sensitive regions in semiconductor devices, and the energy would be lost to create electron-hole pairs through Coulomb scattering. The TID effect is the cumulative damage caused by ionizing radiation over the exposure time. It can cause long-term degradation in the gate/field oxides due to the formation of oxide/interface charge near the active region of the electronic devices [8], [32]. DD results from the non-ionizing process when energetic particles incident on the semiconductor, displace atoms from their original lattice sites, creating vacancies and interstitials [33].

Another big concern along with the evolution and development of electronic devices and ICs is the defect generation in dielectrics and at channel-dielectric interface, as it can limit their electrical performance, reliability and radiation hardness [8], [34], [35]. Over the past 30 years, plenty of evidence has shown that the most important cause of low-frequency noise (1/*f* noise) in electronic devices is the thermally activated interaction of carriers with the defects in the dielectrics [13], [36], [37]. Therefore, low-frequency noise measurements are usually applied to provide deep insights into the defect densities, energy-distributions, and microstructures in various semiconductor devices [17], [18], [37–41]. For example, as defects responsible for low-frequency noise in MOS devices vary with frequency, temperature, and voltage, the frequency and temperature dependence of 1/*f* noise are often correlated via the Dutta-Horn model to estimate the defects' energies [38], [39], and the gate-voltage dependence of 1/f noise can help to evaluate the defects' densities in different region of the semiconductor and/or insulator band gaps [42–44]. A typical low-frequency noise spectrum in electronic devices shows the noise magnitude inversely proportional to its frequency

($\sim$0.01 Hz - $\sim$10 kHz). However, a single prominent defect in the dielectrics of the device can perturb this shape and manifests through the Lorentzian shape of noise spectra in the frequency domain and abrupt switching events between two or more current levels in the time domain. This type of noise response is called Random Telegraph Noise (RTN) [45].

Given the important concerns mentioned above in the development of the electronic devices, the objective of this work is to investigate two broad categories of radiation effects: single event effects and total-ionizing-dose effects, in advanced FinFETs with highly scaled fin widths (sub-10 nm), which either have alternative channel materials with enhanced electrical properties or are integrated with an innovative structure for improved performance. In addition to that, low-frequency noise is also explored in part of this work to provide a deeper understanding of defects in the corresponding dielectric.

The first type of advanced FinFETs of interest in this dissertation is InGaAs FinFETs with sub-10 nm fin widths. As MOSFETs scale down, they are increasingly limited by the power constraints since the power density dissipated by logic chips has reached about 100 W/cm^2 [46]. Therefore, the increase of power density goes hand in hand with substantial packaging and cooling costs, which makes these chips impractical for most applications. On the other hand, the reduction of operating voltage along with the scaling may compromise the switching speed [1]. The III-V compound semiconductors with outstanding electron transport properties provide a promising solution to the continued scaling, such as GaAs, InGaAs, InAs. Fig. 1.2 (a) and (b) show the low field carrier mobility and electron injection velocity of different III-V compound semiconductors [1]. The electron mobility of InGaAs is more than 10 times higher than that of silicon at a comparable sheet charge density. Besides, its injection velocity is also more than twice that of comparable silicon MOSFET at less than half of voltage. The injection velocity plays an important role in an *n*MOS transistor in saturation, as I_{ON} is determined by the product of the sheet electron concentration and the electron injection velocity. In addition, for sub-10 nm technology, transistors operate in the quasi-ballistic region, where very few scattering events occur when the electrons travel from source to drain [47]. The drive current I_{ON} can be described as [48]:

$$I_{on} \propto v_{inj} Q_i \approx v_{inj} C_i (V_{gs} - V_t) \tag{1.1}$$

Where Q_i denotes the inversion layer charge, C_i is the capacitance of the gate dielectrics, and $V_{gs} - V_t$ is the gate overdrive voltage. Therefore, these properties make InGaAs a promising *n*MOS channel material for future CMOS technology generation, and InGaAs FinFETs are important as they also incorporate the advantages of FinFETs over planar architecture mentioned above. In general, InGaAs FinFETs are constructed either on III-V substrates, such as InP, to reduce the lattice mismatch [49], [50], or on Si to be compatible with current CMOS technology [51].

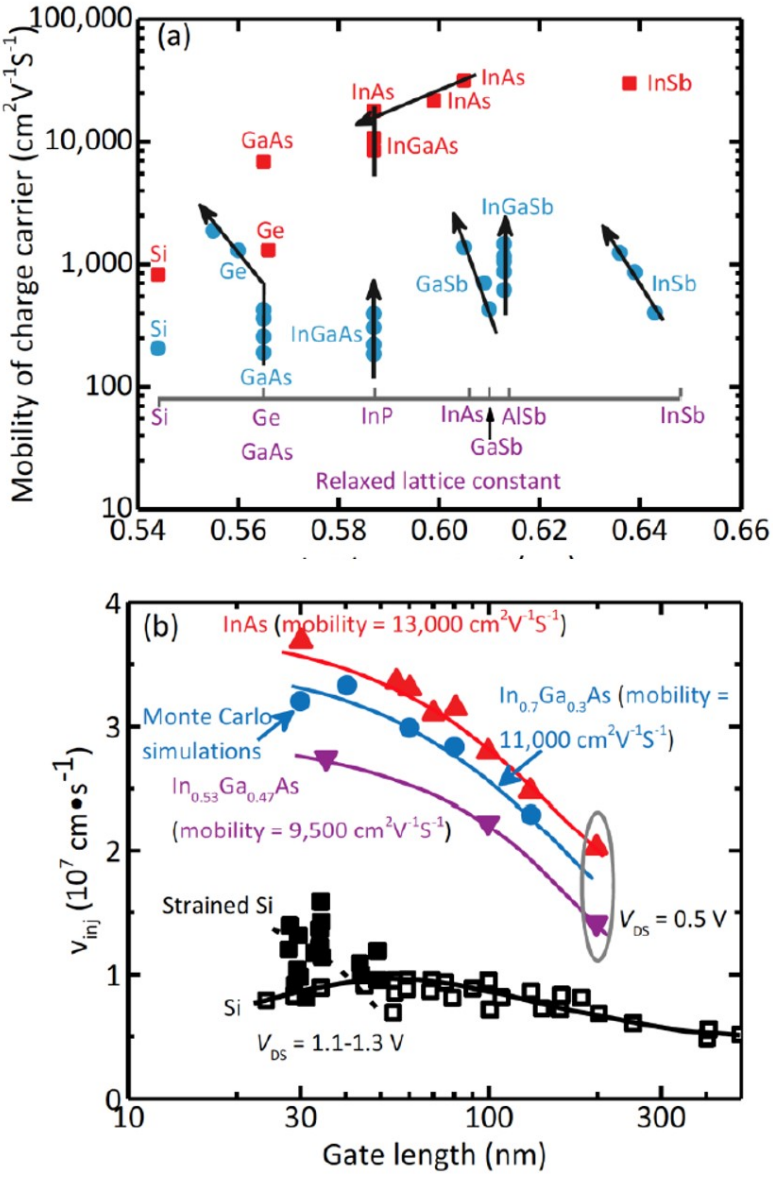


Figure 1.2: (a) Electron and hole mobility of group III-V compound semiconductors. Electron mobility is marked red and hole mobility is in blue. The arrow indicates the increase of biaxial compressive strain. (b) Electron injection velocity in III-V compound semiconductors [1]

The second type of advanced FinFETs explored in this work is bulk Si FinFETs integrated with through silicon vias (TSVs) near the active region. Although novel channel materials and exceptional device architectures are introduced to extend Moore's law in pushing the physical limits of the oxide thickness, junction depth, and depletion width, the key challenge for these cutting-edge integration and device options is the growing obstacles in their fabrication and the incompatibility of various designs with planar structures [52]. Besides, the ever-expending and demanding electronic market is highlighting the limitations of conventional two-dimensional (2D) ICs as they not only have limited floorplanning choices, but also lack suitability for the integration of disparate signals (digital, analog, and rf) and technologies like SOI, SiGe, heterojunction bipolar transistors, GaAs, etc [53]. 3D IC technology is currently one promising solution to these problems, even in the absence of continued scaling, which enables each transistor to access a greater number of neighbor ones and increases the bandwidth of each circuit functional block. It is reported that compared to its 2D counterparts, 3D ICs have shown improved wire efficiency ($\sim$15%), significantly reduced total active power (more than 10%) [54], decreased noise, enhanced signal integrity, and increased transistor packing density [55].

There are several different types of 3D packaging according to the stacking method, including on-chip 3D integration where the functional layers within a chip are built layer-by-layer; die-to-die or package-to-package stacking; and TSV integration technology incorporated 3D ICs. Despite the great maturity and excellent characterization, the traditional wire bonding technologies face their limitation when it comes to 3D chip interconnection: long connections between the peripheries of the devices restrict I/O density by the resolution of the wire bonders requiring increased volumes to accommodate the wire bonds both vertically and horizontally [56]. However, TSVs, on the other hand, can provide much shorter interconnection length, which are directly between different chips and minimize the need for wire bonding, substantially reducing the distance of information flow on a chip by up to 1000 times. It features higher density and higher aspect ratio connections, making it possible for the integration of multi-chip systems entirely within the silicon and massive additional pathways and channels other than wire bonding [56].

Based on the application, the vertical TSV integration technology can be classified into two types: via-first and via-last TSVs, shown in Fig. 1.3. The former type typically has the diameter ranging from 1 to 5 μm, while the diameter of the later type ranges from 5 to 20 μm [2].

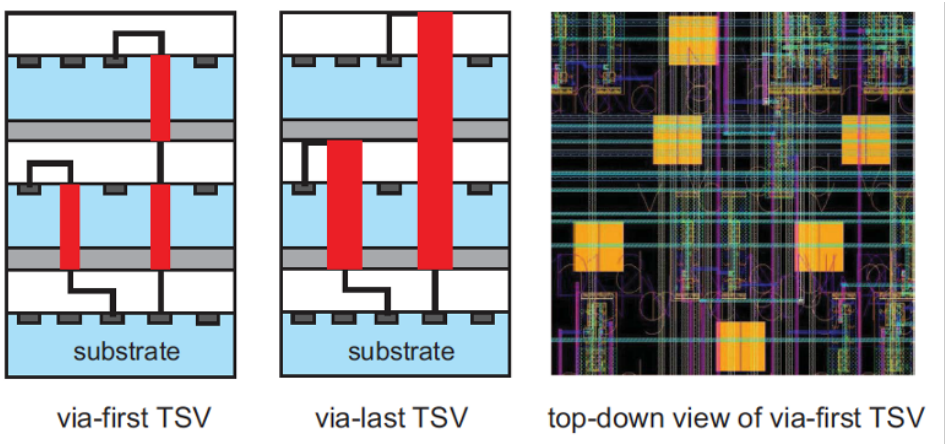


Figure 1.3: Via-first and Via-last TSVs with face-to-back bonding [2]

This work is organized as follows. Chapter II gives a brief background information on relevant topics including single event effects, total-ionizing dose effects, and low frequency noise. The basic charge collection mechanisms of SEE are discussed together with two main effects observed in the experiments, the shunt effects and parasitic bipolar effects. Pulsed-lased induced SEE is particularly illustrated with a concise explanation of single-photon absorption (SPA) and two-photon absorption (TPA). The physical process of the TID effects is reviewed in detail which involves the formation and effects of oxide and interface traps. Moreover, the origin of $1/f$ noise and its temperature dependence are discussed with an emphasis of the Dutta-Horn model, which correlates the frequency and temperature dependence of $1/f$ noise and enables the estimates of effective defect energy distributions.

Chapter III investigates the single-event transient (SET) response and charge collection mechanisms for advanced InGaAs FinFETs on InP substrates with sub-10 nm fin widths through pulsed-laser irradiation. The SET dependence on irradiation position, fin-width, V_{ds}, and V_{gs} are examined. Quantum-well structures confine the charge collection in the InGaAs channel layer both in longitudinal and transverse directions. Consistent with the conclusion in the previous research of InGaAs FinFETs [15], higher peak current and more collected charge are observed in the devices with wider fins. TCAD simulation is also implemented to explain this phenomenon. Besides, due to the mobility difference of electrons and holes in the substrate layers, the holes left in the substrate can modulate the channel potential and lead to the parasitic bipolar effect, which enhances the charge collection in these devices. This effect is also illustrated by TCAD simulation for devices with

different fin widths.

Chapter IV describes the impacts of TSV integration on TID effects and low-frequency noise at room temperature in advanced bulk *n*MOS and *p*MOS Si FinFETs with SiO_2/HfO_2 gate dielectrics. TSV integration has negligible impacts on threshold shifts and degradation of subthreshold swing and I_{on}/I_{off} ratios. The off-state leakage currents increase with the TID due to the radiation-induced traps in the field oxide, the extent of which is affected by electric field in the corresponding oxide region. Similar low-frequency noise magnitudes and frequency dependences are observed before and after TID irradiation for each device type, indicating the insignificant influence of TSV integration on $1/f$ noise.

Chapter V explores the defect densities, energies, and microstructures one step further in the SiO_2/HfO_2 dielectrics of the bulk Si FinFETs for both *n*MOS and *p*MOS devices on the same chips, through the measurements of temperature and gate-voltage dependencies of the $1/f$ noise, which in previous work showed general opposite trends for the effective border-trap densities from the midgap to the relavent band (conduction band for *n*MOS and valence band for *p*MOS) [17]. Within the temperature range we measured (80K-330K), the overall normalized noise decreases dramatically for *n*MOS and increases slowly for *p*MOS transistors as the temperature increases. By examining the gate-voltage dependences of $1/f$ noise at particular temperatures extracted from temperature dependence measurements, the correlation of temperature and gate-voltage dependencies is qualitatively explained in terms of the energy-dependent trap density for both types devices, consistent with the conclusion of large planar MOS devices [57]. The similar temperature dependence results of $1/f$ noise before and after irradiation in both types devices affirm the excellent radiation hardness of the devices in [17].

Chapter-VI summarizes the conclusions of the dissertation.

CHAPTER 2

Background

2.1 Single Event Effects

2.1.1 Charge deposition

When high energy particles (protons, neutrons, electrons, heavy ions, etc.) pass through the sensitive regions in semiconductor devices, the energy they lose creates electron-hole pairs through Coulomb scattering. The resulting effects on the devices are referred as single event effects (SEEs). The energy loss per unit path for a particle is described by linear energy transfer (LET) [58]:

$$LET = -\frac{1}{\rho}\frac{dE}{dx} \qquad MeV \cdot cm^2/mg \tag{2.1}$$

Where ρ is the density of the target material. In silicon, a LET of 97 $MeV \cdot cm^2/mg$ corresponds to charge deposition of $1pC/\mu m$. The average LET always increases initially and then decreases as the incident particle's energy decreases, where the peak of the LET is called the Bragg peak [59]. The location and magnitude of the Bragg peak are different for various materials in different materials. Typically, for two ions with atomic number $Z_1 > Z_2$, incident on the same materials with the same energy, the LET for Z_1 will be greater than than for Z_2. The distance that an incident particle travels in the target material is defined as the particle range. Obviously, the average range in the target material decreases as the particle's energy decreases. In general, the particles with energies near the Bragg peak have limited range [60].

Apart from Coulomb scattering, photon absorption is another efficient way to induce extra charge in semiconductor materials. Specifically, lasers with different wavelengths are typically used to irradiate the sensitive area of the semiconductor devices, in which the photons can give their energies to the electrons in the valence band of the material and excite them to the conduction band, forming electron-hole pairs. Based on the excitation mechanisms, this approach can be classified into single-photon absorption (SPA) or two-photon absorption (TPA). Fig. 2.1 (a) and (b) depict the SPA and TPA processes of exciting an electron from the valence band to the conduction band.

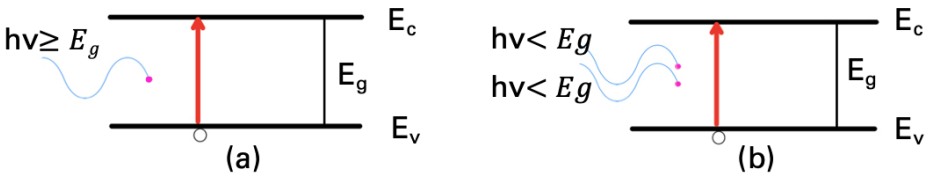


Figure 2.1: Energy band diagram for illustrating the process of (a) SPA, and (b) TPA. hν is the energy of the incident photon.

SPA occurs when the photon energy is greater than the band gap, and each photon absorbed can create one electron-hole pair. This process is governed by Beer's law [61], which claims the intensity of light traveling through a material decreases exponentially with distance into the material at a rate determined by the linear absorption coefficient, α:

$$I(z) = I_0 exp(-\alpha z) \tag{2.2}$$

where I_0 is the intensity of the incident beam, and z is the laser penetration depth. Fig. 2.2 shows this absorption coefficient as a function of wave length for silicon [3]. One thing to note here is that, unlike heavy ions, laser light cannot pass through metals, and that's why semiconductor devices are usually irradiated from the backside to avoid the reflections from metal contacts on the top.

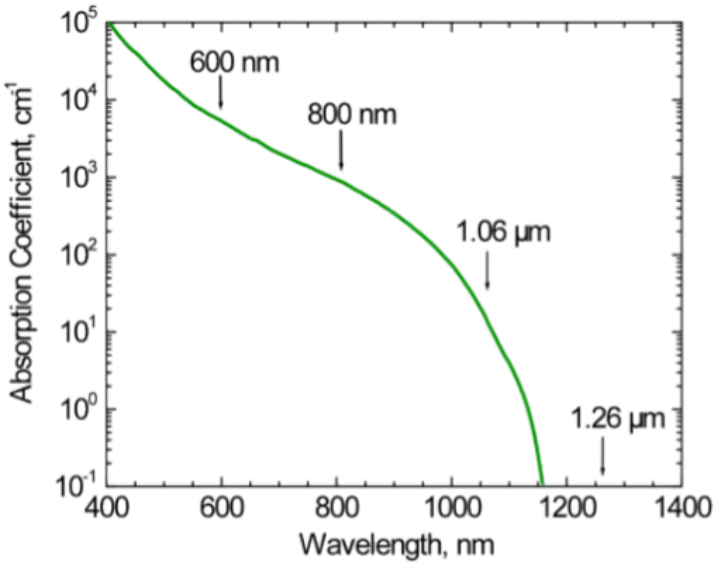


Figure 2.2: Room temperature absorption spectrum of silicon in the visible and near-infrared region of the spectrum illustrating the common laser wavelengths used for above-bandgap single-event effects measurements and also that for the subbandgap experiment [3]

On the other hand, TPA occurs when two photons with energies less than the band gap are simultaneously absorbed and create an electron-hole pair [3]. Therefore, TPA is highly dependent on the incident laser intensity and only the region in focus can generate extra carriers, which makes the spatial profiling of SEEs possible. Given these two types of photon generation methods, the light propagation and charge deposition in a semiconductor material can be described as the following equations [62], [63]:

$$\frac{dI(r,z)}{dz} = -\alpha I(r,z) - \beta_2 I^2(r,z) - \sigma_{ex} N I(r,z) \tag{2.3}$$

$$\frac{d\Phi(r,z)}{dz} = \beta_1 I(r,z) - \gamma_1 N(r,z) \tag{2.4}$$

$$\frac{dN(r,z)}{dz} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \tag{2.5}$$

where I is the laser intensity, N is the density of free carriers, α is the single-photon absorption coefficient, β_2 is the two-photon absorption coefficient, σ_{ex} is the absorptivity of generated free carriers, Φ is the phase, γ_1 describes the refraction due to free carriers, and z is the depth in the material.

Here in this work, we applied the pulsed-laser method to investigate the SEEs in the InGaAs FinFETs instead of using heavy ions, because compared to the heavy ion SEE test, pulsed-laser sources are easily accessible, inexpensive, non-destructive, and can provide the temporal and spatial information which is very helpful to understand the mechanisms responsible for SEEs.

2.1.2 Charge collection mechanism

In terms of the failure types in devices, SEEs can be classified as destructive effects and non-destructive effects. The former ones include single event latchup (SEL) where parasitic pnpn junctions are triggered and a low resistance path between the power supply and ground is formed; single event burnout (SEB) in which a single energetic-particle strike induces a localized high-current state in a device that results in catastrophic failure; and single event gate rupture (SEGR) where a conducting path is created in the gate oxide [64]. Non-destructive SEE, also known as soft error,

includes single event upset (SEU) in a memory cell where the memory cell flips, which is recoverable compared to the first failure type. The fundamental reason for all of these failures is the generation of single event transients (SET) that exceed the critical value that devices can tolerate. The most sensitive regions in an electronic device are reverse-biased p-n junctions where a high electric field exists in the depletion region. Fig. 2.3 illustrates an SET induced by an energetic ion and the subsequent charge collection by drift and diffusion in a reverse biased p-n junction [4].

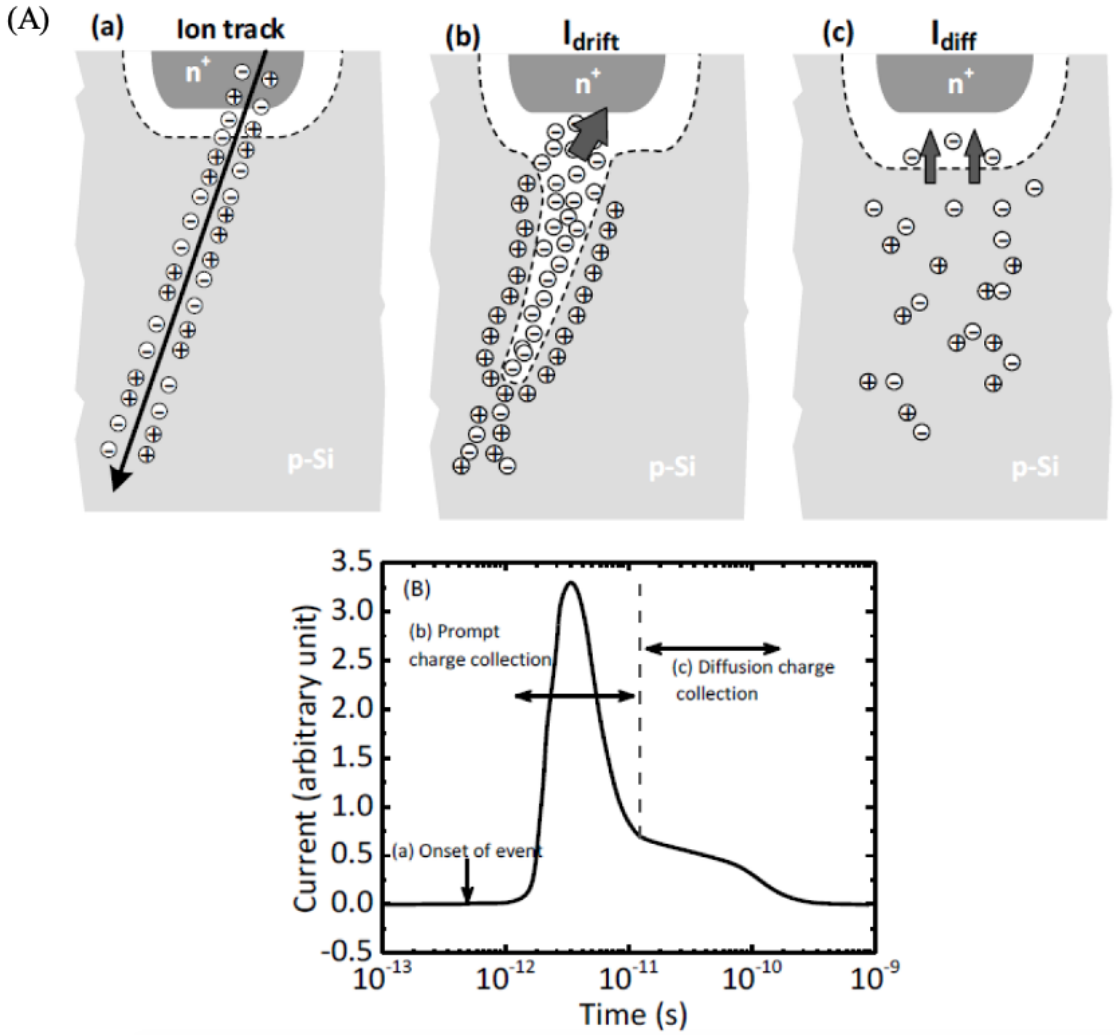


Figure 2.3: (A)Charge generation and collection processes in a reverse biased pn junction and (B) the resultant current transient caused by the passage of a high-energy ion [4]

Electron-hole pairs are initially generated along the energetic ion path (a). Then, due to the high electric field, the carriers in the depletion region are quickly collected through drift, creating a large current transient I_{drift} with a duration up to picoseconds. It is noticeable that there is a distortion of

the depletion potential, which is a function of substrate concentration, bias voltage, and the particle energy (b) [65]. After the drift collection, diffusion of the carriers in the vicinity of the depletion region dominates the carriers' collection process (c) with a relatively long time (up to hundreds of nanoseconds). Generally, the farther the event occurs away from the depletion region, the less charge will be collected. Fig. 2.3 (B) shows a representative current transient pulse, exhibiting a prompt drift and a slow diffusion component.

2.1.3 Shunt effects

Along with Moore's law, the electronic devices have been scaled down to a point that multiple junctions in a device can be affected by one single ion track or laser beam. Then, the charge collection of each junction cannot be treated individually. A transient conductive path would be formed between these junctions as a result of the high density of generated carriers. This phenomenon is called a "shunt effect" [5]. Fig. 2.4 shows an ion track passing through a N^+-P-N-N^+ structure. A highly conductive ohmic-like region due to impact ionization connects the two heavily doped N^+ layers. In nowadays advanced semiconductor devices, the shunt effects are more likely to take place because of the shrunk dimensions. For example, the source-channel junction and drain-channel junction can be easily connected as the channel length is getting smaller and smaller, forming the source-drain transient currents [15], [14, 66–71].

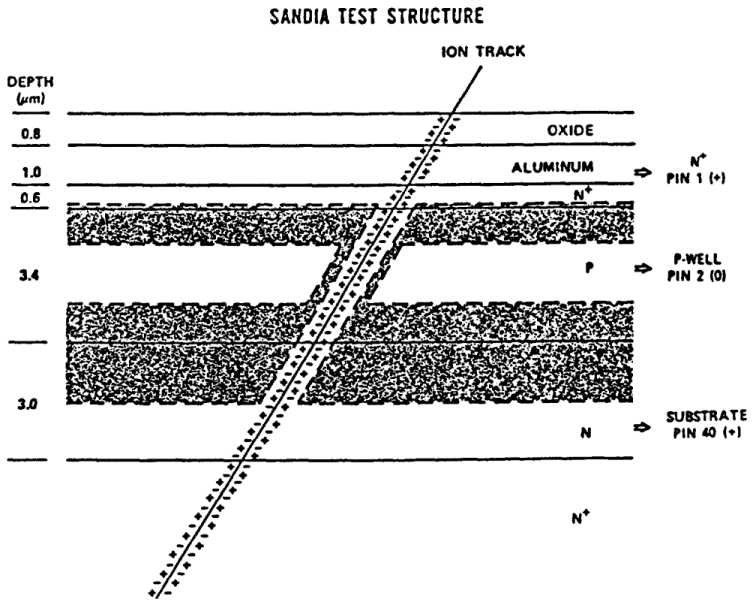


Figure 2.4: Illustration of ion track shunt effect in two-junction experimental structure [5]

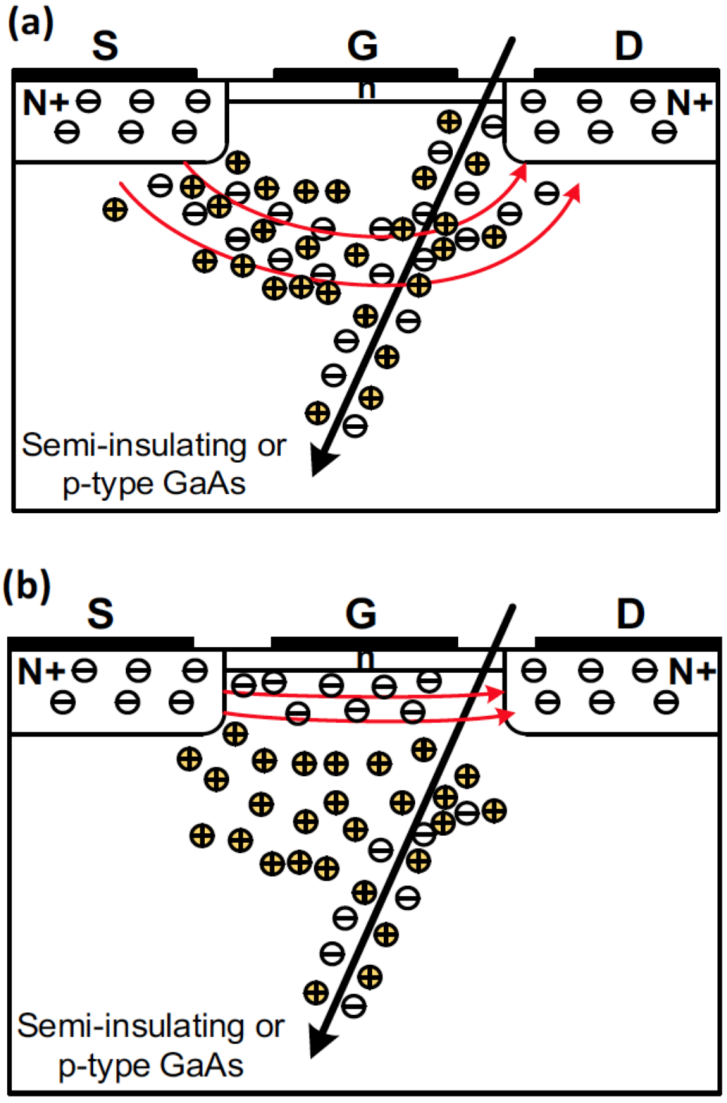


Figure 2.5: Schematic diagram illustrating (a) the bipolar gain and (b) channel-modulation charge enhancement mechanisms that contribute to the charge collection processes of GaAs FETs [6].

2.1.4 Bipolar amplification effect

Bipolar amplification of the SEE charge collection in semiconductor devices has been reported in a significant number of studies [6], [15], [70, 72–78]. Fig. 2.5 illustrates the mechanism of this effect in a GaAs FET [6]. A high density of electron-hole pairs is generated along the ion track when the device is irradiated by a heavy ion strike. Due to the much higher mobility, electrons are collected very quickly, while a large amount of holes remain in the channel layer or the substrate underneath the channel because of their much lower mobility. As a result, the holes accumulated

near the source region can reduce the source-channel barrier and facilitate the electron injection from the source to channel, which are then collected by the drain terminal. This mechanism is similar to a bipolar transistor operating at forward active condition, and is called the bipolar amplification effect. More charges would be collected than were generated because of this effect.

2.2 Total Ionizing Dose (TID) Effects

2.2.1 Charge trapping and mechanism overview

Besides the semiconductor materials, oxides and insulators are also key components in electronic devices. Total ionizing dose (TID) effects usually occur in these regions where the ionizing radiation can induce significant charge buildup, leading to parametric degradation and functional failure [8]. In the radiation environments like space and nuclear power plants, TID effects can severely impair system lifetime when exposed to high fluxes of electrons and protons. Take MOSFET for example. Fig. 2.6 illustrates an MOS band diagram for a p-substrate capacitor with a positive gate bias. When this MOS transistor is irradiated under high-energy ionizing incident, a large amount of electron-hole pairs are generated in the gate oxide immediately (within picoseconds). Due to the electric field, electrons will be swept toward the gate and holes will drift toward the Si/SiO_2 interface. During this process, part of the electrons will combine with holes before they leave the oxide. This is called initial recombination, and the fraction of electron-hole pairs that avoid recombination is referred to as charge yield. The charge yield is highly dependent on the energy and type of incident particle, and the electric field in the oxide, shown in Fig. 2.7. For all sorts of particles, the probability of recombination between holes and electrons decreases as the electric field increases. Therefore, the charge yield increases.

The holes that survive initial recombination will hop through localized states in the oxide on their way to the Si/SiO_2 interface. Due to their low mobility, some of the holes will be trapped by the microstructural defects and pre-existing traps, forming a positive oxide-trap charge. During the ”hopping” and ”trapping” processes, hydrogen ions (protons) are possibly released, which can also drift to the Si/SiO_2 under the effect of electric field to form interface traps [7]. In *n*MOSFETs, the interface traps are usually negatively charged, while in *p*MOSFETs, they are charged positively. Detailed explanations will be given later.

Apart from the charge buildup in oxide traps and interface traps, TID effects will also take place

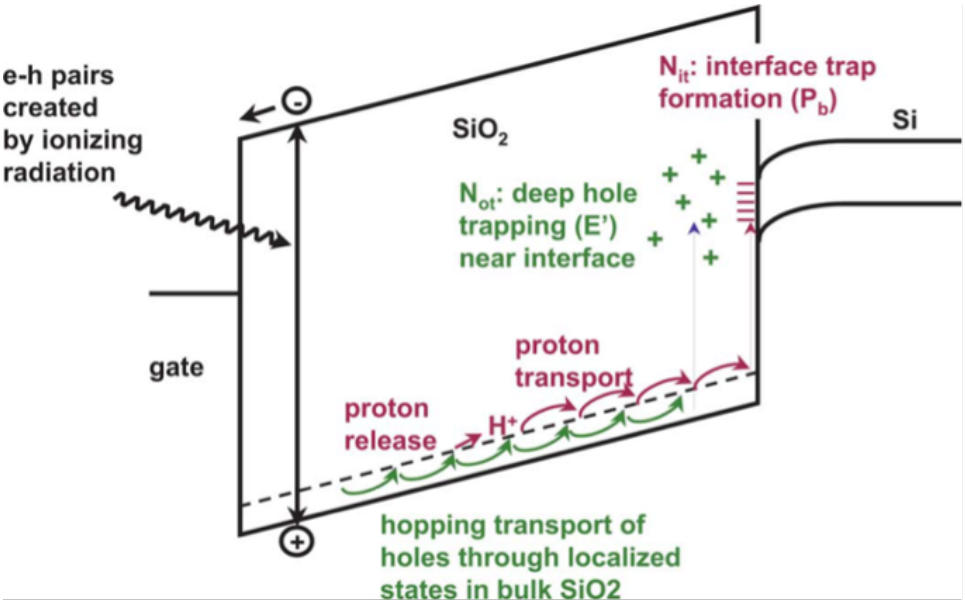


Figure 2.6: Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation. After [7]

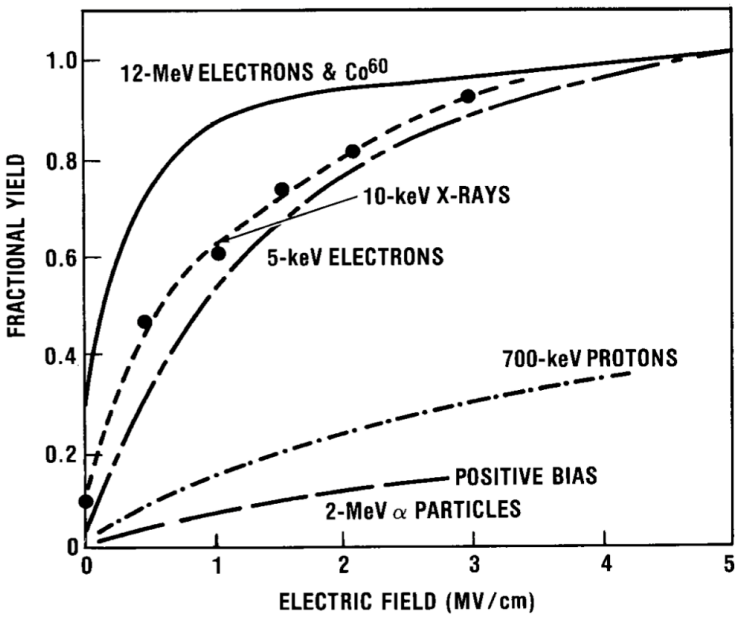


Figure 2.7: Experimentally measured fraction hole yield as a function of applied field, for a number of incident particles. After [8].

in the field oxides. In the region near the channel, holes generated by the high-energy ionizing incident are also likely captured by the defects in the field oxides, and this positive charge buildup can cause parasitic leakage current to flow in the off state condition, which would increase the static

power in ICs. This phenomenon in field oxides is actually becoming the dominant radiation-induced degradation in modern advanced electronics as the gate dielectrics are scaled to a high level (several nm) with very limited pre-existing defects.

2.2.2 Oxide traps

As holes generated by irradiation move through the gate oxide (e.g. SiO_2), the local potential field of the SiO_2 lattice is distorted, which increases the trap depth at the local site, and in turn confines the holes to its immediate vicinity [7]. This combination of a hole and its distorted field is referred to as a polaron [79]. The mobility of the holes is decreased as their effective mass is increased by the polaron, which is why the hole transport can occur over many decades in time after the radiation [80], [81]. As holes drift to the Si/SiO_2 interface under a positive gate bias, some of them will be trapped by the oxygen vacancies near the interface, which are formed due to the out-diffusion of oxygen in the oxide [82] and lattice mismatch at the interface. The number of trapped holes is determined by the capture cross-section near the interface, which is a function of the electric field and also affected by the device fabrication. Since the oxide traps are positively charged, in both *n*MOS and *p*MOS devices, the threshold voltage would be shifted negatively. Fig. 2.8 shows the threshold voltage shift due to oxide-trap charge as a function of electric field in gate oxide [9]. The measured data adjusted for charge yield exhibits approximately an $E^{-1/2}$ electric field dependence.

The oxide-trapped charge also undergoes neutralization as soon as they are formed, mostly through: 1) the electron tunneling from the channel to either oxide traps [83–85] or electron traps associated with trapped holes [86]; (2) the thermal emission of electrons from the oxide valence band to oxide trap [84], [87], which will not remove the trapped hole. Typically, tunneling is the dominant mechanism at or near room temperature, while thermal excitation will become the main factor when the temperature is raised enough. The rate of charge neutralization is highly related to the spatial and energy distributions of the oxide traps. Oxide traps physically closer to the Si/SiO_2 interface are easier to neutralize through tunneling, and thermal excitation is more likely to happen if the energy levels of the oxide traps are close to the oxide valence band. In addition, the gate bias can also play a big role in the neutralization process, which usually manifests itself in the annealing process after a TID test. For example, in the previous case, applying a negative gate bias can help electrons tunnel back to the channel and partially restore the oxide-trapped charge.

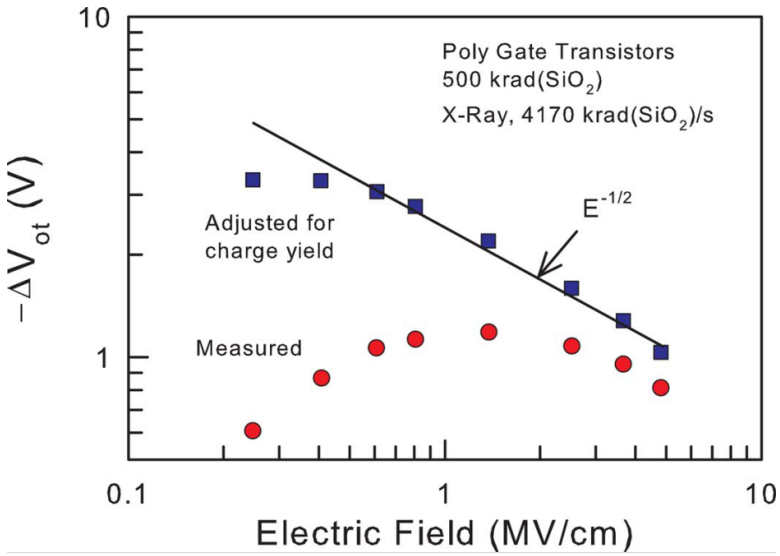
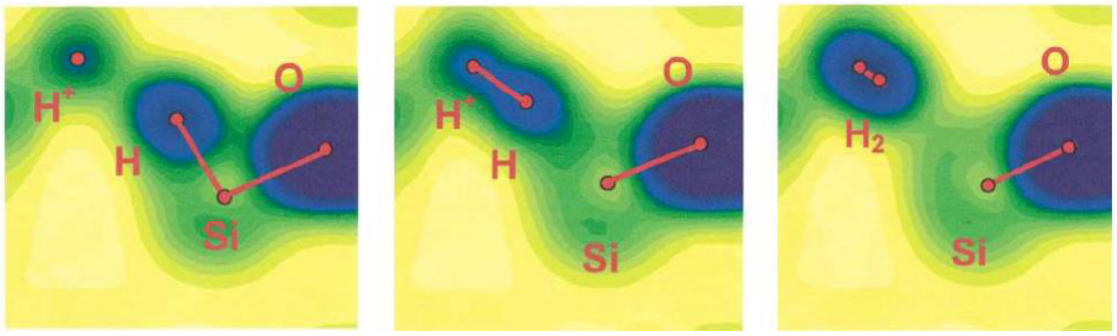


Figure 2.8: Threshold voltage shift as a function of electric field. Shown are the measured data (circles) and the measured data corrected for charge yield (squares). After [9]

2.2.3 Interface traps

In addition to oxide traps, TID effects will also cause the formation of interface traps at the channel-oxide interface. Although the detailed creation steps of interface traps are still under debate by different models, a reasonable consensus has been reached about the general procedure. The precursor of the radiation-induced interface trap is believed to be a Si atom bonded to a hydrogen atom and three other Si atoms on the channel side or O atoms on the SiO_2 side along the interface. Under the effect of H induced by irradiation, the Si-H bond dissociates, forming H_2, and a Si unpassivated dangling bond as an electrically active defect, also known as a P_b center or interface trap. Rashkeev et al. [88] proposed that the H^+ is the only stable charge state at the Si/SiO_2 interface and depassivates the Si-H bonds directly instead of the neutral H through the reaction: Si-H + $H^+ \rightarrow$ $D^+ + H_2$, where D^+ is a dangling bond. Fig. 2.9 shows the depassivation process. When the proton gets close to the Si-H bond, the bond length increases and a "bridge" between Si-H and H^+ gradually forms. Then both electrons from the Si-H bond flee and create a neutral hydrogen molecule. Once the dangling bond is formed, it can exchange charge with the silicon substrate freely and that's why the charge of an interface trap can be changed easily by the external bias.

Based on the energy levels within the Si band gap, interface traps can be positive, negative, or neutral. Traps in the upper portion of the band gap are mostly acceptor-like, while traps in the



(a) (b) (c)

Figure 2.9: Electronic density at different stages of the reaction between H^+ and a Si-H bond: (a) a proton approaches a Si-H bond; (b) an Si-H-H^+ bridge is created; (c) an H_2 molecule and a D^+ defect are formed. After [5]

lower portion of the band gap are primarily donor-like. For example, an n-channel transistor at threshold is affected predominantly by the interface traps in the upper portion of the band gap, in which case the Fermi level is usually above the trap energy levels. Therefore, these traps tend to accept electrons from the silicon and are charged negatively, leading to a positive shift of threshold voltage. In contrast, for a p-channel transistor, the interface traps mostly in the lower portion of the band gap would affect the device at threshold. As the Fermi level is typically below the energy levels of the traps, these interface traps are likely to donate electrons to the silicon and are charged positively. Thus, interface traps in p-channel devices are usually positive, causing negative V_{th} shifts. At midgap, interface traps are approximately neutral. Since oxide-trap charge is positive for both *n*MOS and *p*MOS transistors, interface-trap charge and oxide-trap charge add to each other for *p*MOSFETs and compensate each other in *n*MOSFETs.

2.2.4 Border traps

Apart from the oxide trap and interface trap charge, there is a layer of near-interfacial traps that physically reside in the oxide, but electrically behave as interface traps communicating with the channel. These traps are named ”border traps” by Fleetwood [89], which has been widely accepted by the community as it resolves a lot of confusion especially in the study of 1/*f* noise. Fig. 2.10 illustrate the physical locations of the three types of traps, in which border traps lie within $\sim$ 3 nm of the interface. Compared to the faster interaction between interface traps and Si, the slower

defect with a smaller capture cross section could well be a border trap [90]. The effective border trap densities can usually be obtained by low-frequency measurements, which will be explained in detail later in this section.

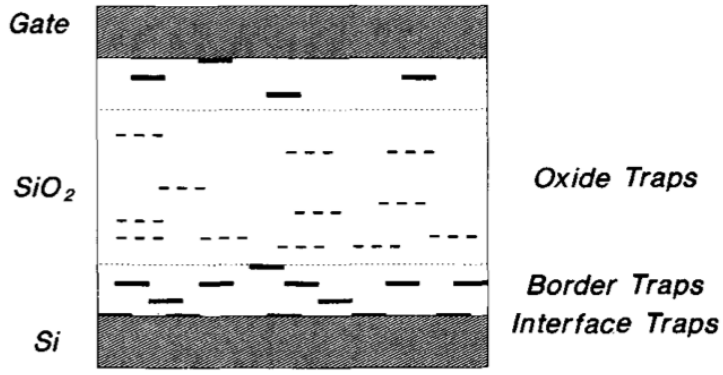


Figure 2.10: Schematic diagram of oxide traps, border traps, and interface traps in MOS structure [5].

2.3 Low-frequency Noise in MOS Device

2.3.1 Origin of low-frequency noise in MOS devices

Noise is a spontaneous fluctuation in current or in voltage that exists in all semiconductor devices. When current is passed through a resistor, three types of noise are normally observed: 1) thermal noise, which is present regardless of whether current flows [91]; 2) shot noise, detected whenever carriers are emitted from a cathode or cross a potential barrier [92]; and 3) low frequency noise (or 1/*f* noise), predominantly caused by carrier number fluctuations due to charge trapping in MOS devices. Specifically, it is the thermally activated interaction between carriers and border traps located near the channel/oxide interface that causes the fluctuations in the surface potential and inversion charge density, which in turn leads to the noise in the drain current. The characteristic times of the border traps include times to capture and emit the carrier, whose distribution forms the noise process in a distinct range of frequencies. As mentioned above, border traps have the spatial distribution near the interface and the energy distribution within the band gap of the channel material. Therefore, the effective border density obtained by low-frequency noise measurements is dependent on the time scale and voltage bias conditions, and it is known that the ability of a border trap to communicate with the underlying Si decreases exponentially with its distance from the

Si/SiO_2 interface [90].

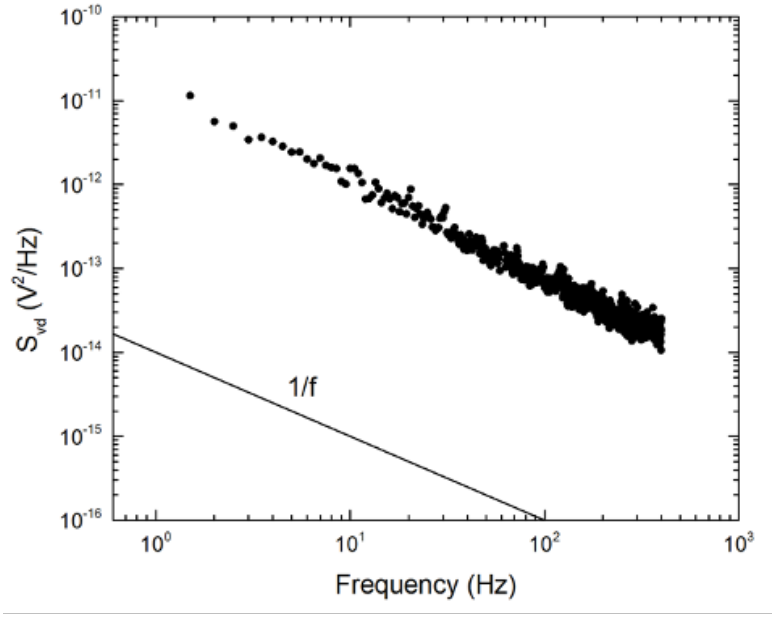


Figure 2.11: Excess voltage noise power spectral density S_{vd} (corrected for background noise) as a function of frequency for bulk Si FinFET with 220 fins at room temperature.

Low frequency noise is typically found to be proportional to $1/f^{\alpha}$ (with α in the range 0.7 $\sim$ 1.3). Fig. 2.11 shows a representative low frequency noise in bulk Si FinFET with 220 fins. As the dimension of transistors is scaled down, low frequency noise is increasingly important to the performance of semiconductor devices, such as mixers and oscillators. Its magnitude is also regarded as a diagnostic parameter to evaluate the quality and reliability of electronic devices [93]. For example, when electrons are captured by the border traps, the net voltage drop between gate and substrate decreases, which therefore reduces the effective gate voltage as well as the drain current. In reverse, emitting electrons from the charged border traps would increases the effective gate voltage and the drain current. This random fluctuations component in currents can be included in the equation of drain current as:

$$I(t) = \bar{I} + i_n(t) \tag{2.6}$$

where $\bar{I}$ is the average current, and $i_n(t)$ is a randomly fluctuating current [10], which typically shows in form like Fig. 2.12 (a). Fig. 2.12 (b) illustrates the noise in the MOS device when the fluctuating component is converted by Fourier transformation: at high frequencies, the thermal and

shot noise dominates, while in the low frequency region, the noise spectrum exhibits the 1/*f* form as shown in Fig. 2.11.

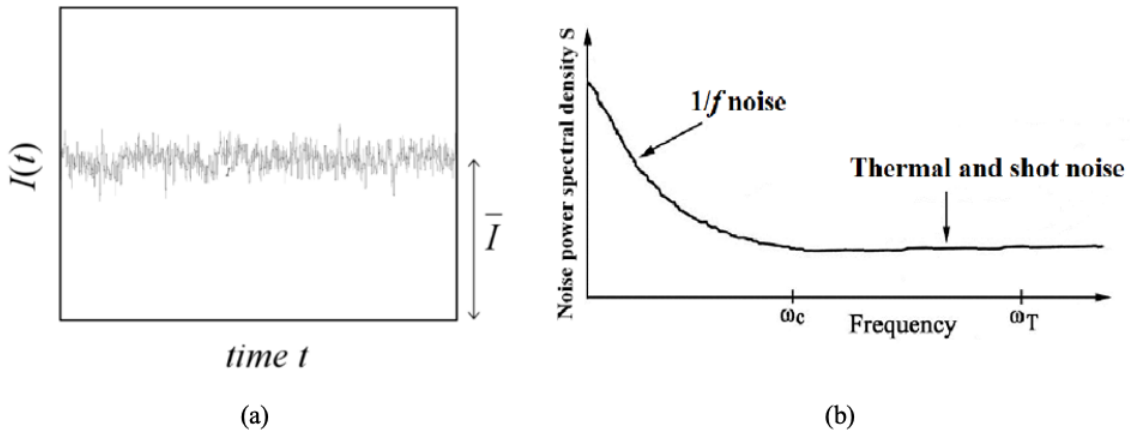


Figure 2.12: (a) A typical noise waveform in the time domain (After [10]); (b) the schematic illustration of noise power spectral density in the frequency domain (After [11]).

2.3.2 Voltage dependence of low-frequency noise in MOS devices

According to the McWhorter model, a number of researchers have been able to obtain first-order estimates of effective trap densities in MOS devices by noise measurements at room temperature, for defects with energy level that within a few kT of the Fermi level, which means we can sense defects close to the conduction band for *n*MOS transistors and valence band for *p*MOS transistors, and its simplest form attributes the noise to tunnel-assisted charge exchange between the Si channel and defects in the near-interfacial SiO_2 [39], [94]. Under constant drain current and gate bias condition, in the linear region of MOS operation, the transistor with an evenly distributed border traps in space and energy can be essentially regarded as a gated resistor, and the the excess drain voltage noise power spectral density, S_{V_d}, is described as [39]:

$$S_{V_d} = \frac{q^2}{C_{OX}^2} \frac{V_d^2}{(V_g - V_{th})^2} \frac{k_B T D_t(E_f)}{LW ln(\tau_1/\tau_0)} \frac{1}{f} \tag{2.7}$$

Here C_{OX} is the gate oxide capacitance per unit area V_{th}, V_d, and V_g are the threshold, drain, and gate voltages, L and W are the transistor channel length and width, $D_t(E_f)$ is the number of traps per unit energy per unit area at the Fermi level E_f, T is the temperature in Kelvin, k is the Boltzmann constant, f is the frequency, and τ_0, τ_1 are minimum and maximum tunneling times, respec-

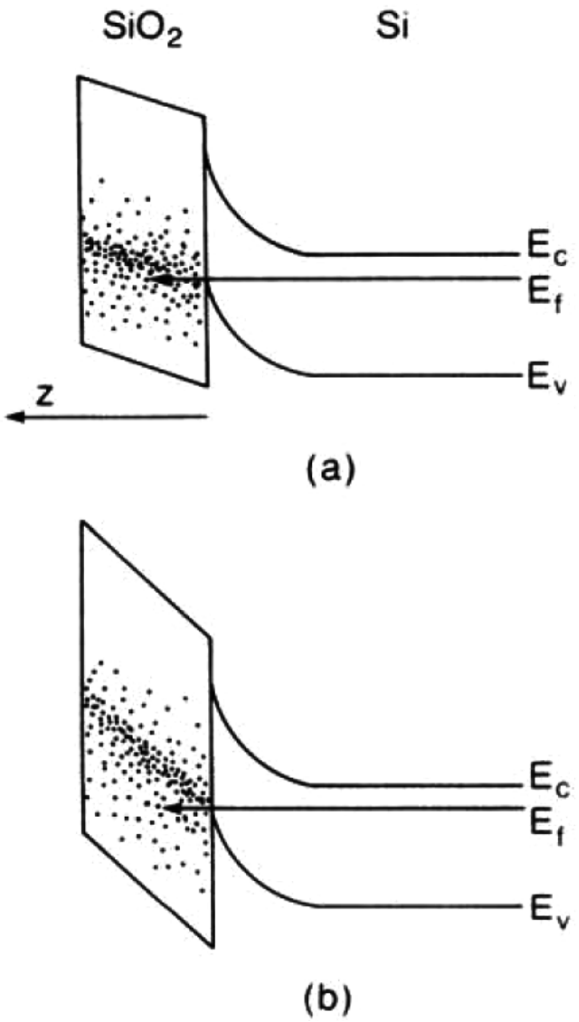


Figure 2.13: Energy bands for a *p*MOS Si/SiO_2 transistor for (a) lower and (b) higher applied electric field. The dots are a notional representation of trapping sites in the SiO_2. The $1/f$ noise of a MOS transistor is sensitive to defects within a few kT of the Fermi level, which means that changing the bias enables one to probe a different range of defect energy levels in the near-interfacial SiO_2. (After Surya and Hsiang [12]).

tively [94–97]. Therefore, for a device with a uniform defect-energy distribution, the gate-voltage dependence of noise $\beta = \partial \ln S_{V_d} / \partial \ln |V_g - V_{th}|$, is supposed to be ~ 2 [39], [41]. However, in reality, defects responsible for low-frequency noise in MOS devices are not usually distributed evenly in space or energy. Instead, they often change with frequency, voltage, and temperature. It has been reported that varying the gate bias can help to probe different regions of the semiconductor and/or insulator band gaps, even at room temperature [39], [41]. β values higher than 2 indicate that the effective border-trap energy distribution increases as it moves away from the conduction

band edge for *n*MOS devices (or the valence band edge for *p*MOS); while values of β less than 2 imply the opposite trends [39], [42], [57]. Fig. 2.13 illustrates the band bending of SiO_2 insulator as the gate voltage is altered [12]. Although the spatial distribution of the defects is not easy to obtain, changing the gate bias can still serve as useful and complementary information to changing the temperature [12], [57], [98].

Dutta and Horn [38] demonstrated that the low-frequency noise in a metal film is strongly temperature dependent, resulting from a random thermally-activated process with a broad distribution of energy relative to kT. This theory was initially used to analyze the low frequency noise in thin metal film, and then extended to semiconductor devices with different gate oxides. Based on the Dutta-Horn model, the measurements of temperature dependence of $1/f$ noise are often used to obtain insights into the defects' energy and microstructure [39], [18], [99], [100]. Dutta and Horn have shown that if the low-frequency noise is caused by a random thermally activated process having a broad distribution of energies relative to kT, the frequency and temperature dependences of the noise are related by:

$$\alpha(\omega, T) = 1 - \frac{1}{\ln \omega \tau_0}\left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1\right) \tag{2.8}$$

Here S_V is the excess voltage-noise power spectral density after the thermal noise is subtracted, τ_0 is the characteristic time of the process leading to the noise, which is usually chosen as 1.81×10^{-15}s to be consistent with MOS studies [39], [18], and $\omega = 2\pi f$. For noise described by Eq. (2.8), the shape of the defect-energy distribution $D(E_0)$ can be described via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T) \tag{2.9}$$

Where the defect energy can be expressed by the temperature and frequency via [38], [39]:

$$E_0 \approx -kT \ln(\omega \tau_0) \tag{2.10}$$

If the noise is the result of thermally activated processes involving two energy levels, then E_0 is the energy barrier that the system must overcome to move from one configurational state to the other state [38], [39], [97], as shown schematically in Fig. 2.14.

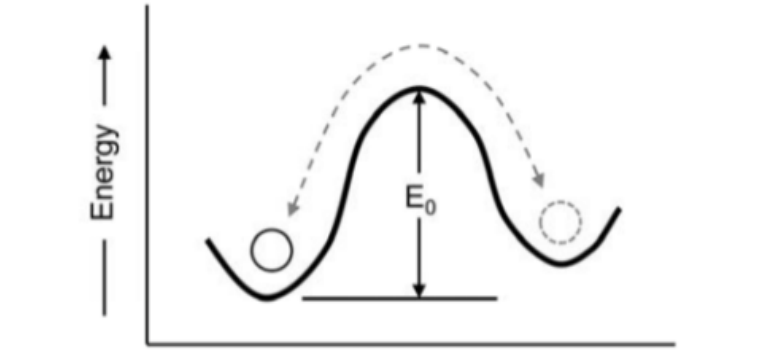


Figure 2.14: Schematic illustration of a system with two configurations with different energy levels, charge states, and/or carrier scattering rates. E_0 is the energy barrier for the system to move reversibly from one configurational state to another. (After [13]).

2.4 Previous Work on The Radiation Effects on These Advanced FinFETs

There has been much effort in investigating the SEE particularly in InGaAs FinFETs due to their very promising application in space [15], [70], [71]. These devices were built either on InP semi-insulating substrates with an InAlAs buffer layer or on Si substrates with a GaAs buffer layer. Both heavy ions and pulsed-laser measurements have been used to generate the single event transients in the devices. InGaAs FinFETs with an InP substrate show a long SET tail current due to the charge collection from the semi-insulating substrate, while a Si-based InGaAs FinFET exhibits a very quick SET similar to other silicon substrate technologies [101] due to the conductivity of the substrate. TCAD simulations also confirm that a large amount of holes pile up underneath the channel layer in InP-based devices, which induces the bipolar amplification effect and enhance the SET charge collection, but this effect is eliminated in the Si-based InGaAs FinFETs due to extraction of holes through the substrate contact, reducing their SEE sensitivity. The shunt effect is also observed in both types of devices, which contributes to the peak current as the incident particles cover the whole channel, connecting the source and drain terminals. In addition, SETs in these devices increase with the drain voltage (source grounded) because a higher electric field will provide an enhanced charge collection. In contrast, the gate-voltage dependence of SETs in these InGaAs FinFETs is not as obvious as that in InGaAs planar MOSFETs [77]. Moreover, wider-fin devices generally are able to collect more charge in terms of SETs. However, in an even more highly scaled device in fin width (sub-10 nm), the SEE responses have not been studied. On the other hand, radiation effects and 1/*f* noise of advanced FinFETs with TSV integrated near the channel have not been revealed as well.

CHAPTER 3

Pulsed-Laser Induced Single-Event Transients in Advanced InGaAs FinFETs

This chapter is adapted from "Pulsed Laser-Induced Single-Event Transients in InGaAs FinFETs with sub-10-nm Fin Widths" published in 2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS), and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Stefano Bonaldo, Andrew L Sternberg, John A Kozub, Andrew M Tonigan, Mahmud Reaz, Landen D Ryder, Kaitlyn L Ryder, Huiqi Gong, Sharon M Weiss, Robert A Weller, Alon Vardi, Jesús A del Alamo, Robert A Reed, Daniel M Fleetwood, Ronald D Schrimpf.

- K. Li *et al.*, "Pulsed Laser-Induced Single-Event Transients in InGaAs FinFETs with sub-10-nm Fin Widths," *2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2019, pp. 1-5.

3.1 Introduction

The outstanding electron transport properties of InGaAs make it a promising nMOS channel material for future CMOS technology generations in both planar and FinFET configurations [1], [49], [102], [103]. In general, InGaAs MOSFETs are constructed either on III-V substrates, such as InP, to reduce the lattice mismatch [49], [50], [104], or on Si to be compatible with current CMOS technology [51], [105]. For space applications, researchers have evaluated single-event effects (SEE) in InGaAs FinFETs on both substrate types [15], [70], [71]. The single-event transient (SET) response has been found to depend on gate length, drain to source voltage (V_{DS}), gate to source voltage (V_{GS}), and fin width, as well as substrate material. However, all devices that have been evaluated to date have fin widths of tens of nanometers or greater. As InGaAs FinFET technology is extended to sub-7 nm nodes, fin widths are narrower than 10 nm, [49], [50], [104]. It is therefore important to understand the effects of further size scaling and technology evolution of the SET response of InGaAs FinFETs.

Photons and energetic particles both generate electron-hole pairs, but laser irradiation offers control over the time and location at which the carriers are generated. Consequently, pulsed laser ir-

radiation is a convenient, lower-cost (than ion testing), and non-destructive approach to assist in the evaluation of single event effects in semiconductor devices [61], [106]. Photon absorption by semiconductors occurs primarily via single-photon absorption (SPA) when the photon energy is greater than the band gap, or by two-photon absorption (TPA) when the photon energy is less than the band gap. In this work [107], we investigate the SET response of InGaAs nFinFETs on InP substrates with fin widths less than 10 nm via pulsed-laser irradiation. By examining different fin widths, bias conditions, and irradiation locations, we evaluate the impact of each factor on the SET response and examine charge generation and collection mechanisms. Higher peak currents and greater charge collection are observed in wider fin devices as a result of larger active volumes, consistent with trends observed in previous work on larger devices. The amplitudes of the SETs and the collected charge also increase with V_{ds} due to the enhancement of the electric field along the channel; the transient tail increases as the overdrive voltage increases. Charge collection is influenced strongly by the shunt effect from source-to-drain when the laser spot covers the channel region, and by the parasitic bipolar effect caused by the accumulation of holes underneath the channel. In general, the sub-10 nm fin-width devices show response trends that are generally consistent with those of wider-fin devices [15], [70], [71]. In addition, we perform device simulations that provide insight into parasitic-bipolar charge enhancement in narrow fin devices.

3.2 Experimental Details

3.2.1 Device structure

The devices under test (DUTs) are double-gate nMOS InGaAs FinFETs fabricated at MIT [50]; there are no p-channel devices in the technology examined here as InGaAs only shows exceptional electron transport properties for potential applications. Schematic cross-sectional and side-view diagrams of a single fin are shown in Figs. 3.1(a) and (b), respectively; layers are not drawn to scale. Devices are constructed on a standard 4-inch semi-insulating InP wafer (with thickness $\sim$ 625 m). A 50 nm thick $In_{0.53}Ga_{0.47}As$ channel layer is grown on a 40 nm thick InP layer and a 300-nm thick $In_{0.52}Al_{0.48}As$ buffer layer. The fin height is approximately 200 nm. On top of the fin, there are 1 nm HfO_2 and 90 nm hydrogen silsesquioxane (HSQ) layers. There are 34 fins in parallel for each device with a spacing of 0.2 μm between each fin. Fig. 3.2 shows the device layout. The middle metal pad is connected to the gate terminal, and the pads on two side are symmetrical, which

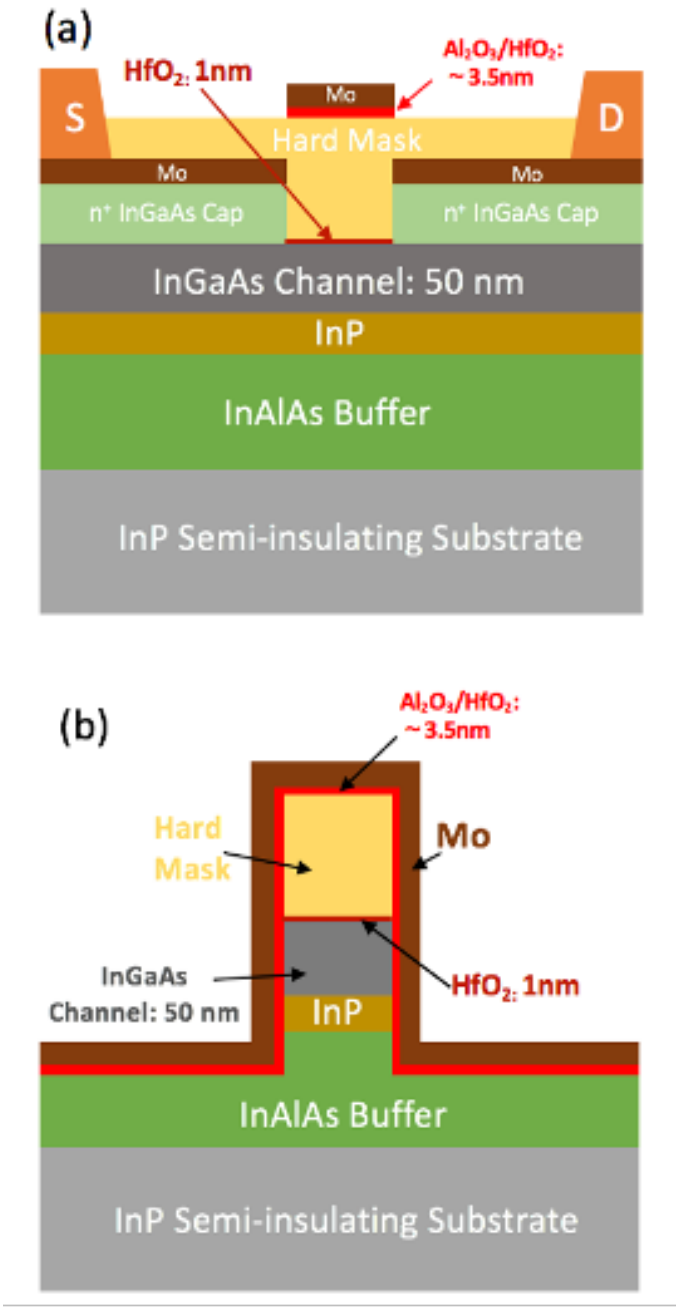


Figure 3.1: (a) Schematic cross section and (b) side-view of InGaAs double-gate FinFET (not drawn to scale).

are connected to source and drain terminals. Detailed fabrication information is given in [50].

The FinFETs of Fig. 3.1 operate as double-gate MOSFETs with the channel controlled by the side gates, but not the top gate due to the isolation by the HSQ hard mask. The gate dielectric materials, one monolayer of Al_2O_3 and 3 nm of HfO_2 (EOT $\sim$ 0.8 nm), are deposited by atomic

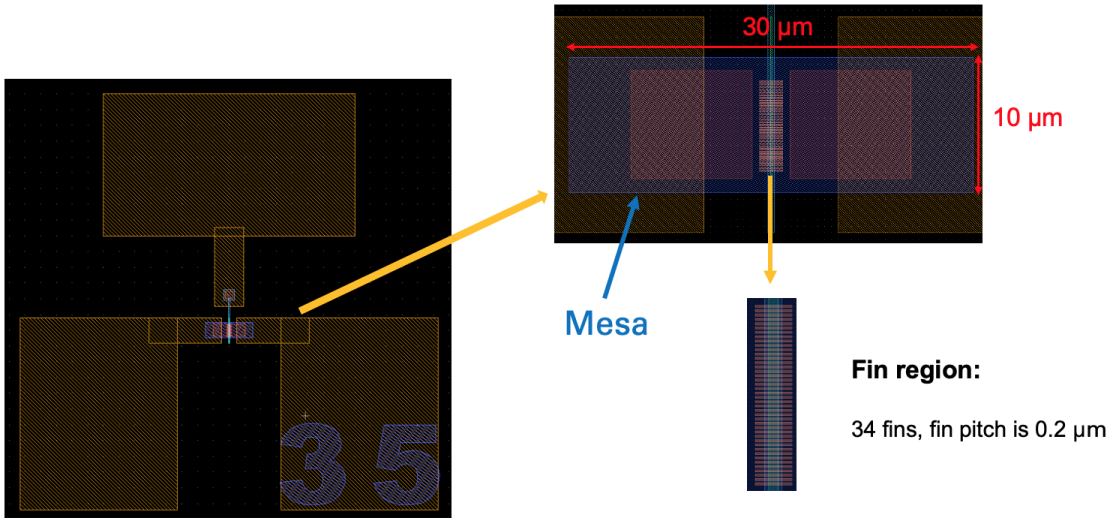


Figure 3.2: InGaAs FinFETs layout with 34 fins; The middle pad is connected to the gate terminal, source and drain terminals are symmetrical.

layer deposition (ALD). The fin pitch is 0.2 μm. The fin widths of the devices used in this study are 5 nm, 7 nm, and 9 nm; gate lengths are 80-100 nm. There are 34 fins in these devices. As these are double-gate FinFETs, the channel width W is twice the channel height ($\sim$ 50 nm) multiplied by the fin number, which is approximately 3.4 μm.

$I_D - V_{GS}$ characteristics are monitored before and after each set of transients to make sure the DUTs are in good condition before and after testing. Fig. 3.3 shows the transfer characteristics of the DUTs with 80-nm gate lengths and different fin widths under 50 mV drain bias (source grounded), which conforms with the proportional relationship between the on-state drive current with the channel width. All exhibit typical nMOSFET characteristics with high on/off current ratios. In the off-state region, it is found that the leakage currents increase as V_{GS} is getting more negative. This is a typical behavior in $I_D - V_{GS}$ curves due to the gate-induced drain leakage (GIDL). It occurs in the region where the gate overlaps the drain junction. As the gate is set more negative, the depletion region forms in the n-type drain and the band bending occurs in the interfacial region. When the band bending is more than the band gap, electrons in the conduction band are easily tunnel through the band gap to the conduction band, creating electron-hole pairs, which are then collected by the drain terminal as GIDL.

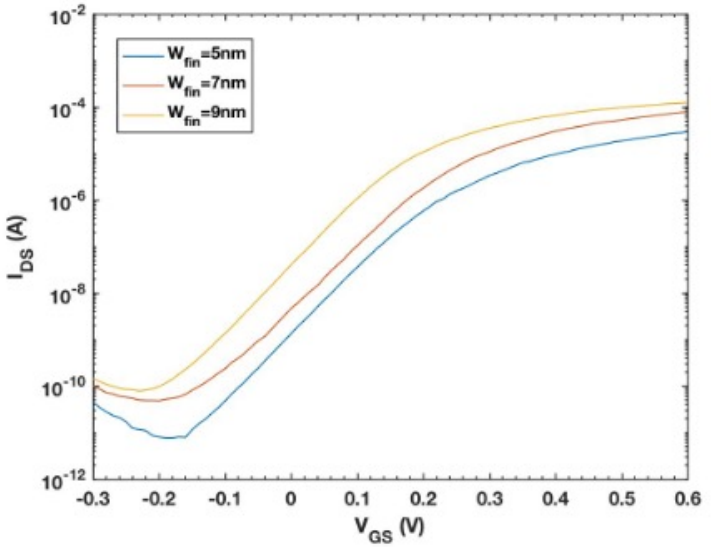


Figure 3.3: $I_{DS} - V_{GS}$ characteristics for devices with different fin widths. The gate lengths are all 80 nm. V_{ds} = 50 mV.

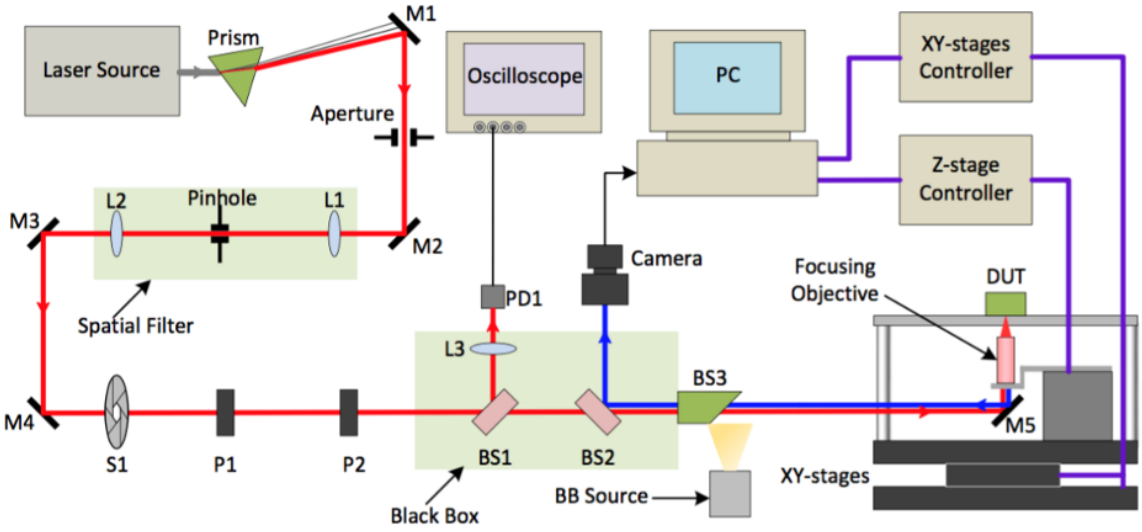


Figure 3.4: A simplified block diagram of TPA test setup. In the figure, 'L' stands for lens, 'M' stands for mirror, 'S' stands for shutter, 'P' stands for polarizer, 'BS' stands for beam splitter, 'PD' stands for photodiode, and "BB" represents the broadband light source. The red line indicates the optical path traveled by the laser beam. The blue line indicates the reflected light that is imaged by the near infrared camera

3.2.2 Experimental setup

Pulsed-laser testing experiments were performed at Vanderbilt University using the system shown in Fig. 3.4 [70], which generates 150 fs pulses with 1 kHz repetition rate. This tunable

wavelength laser system can be optimized both for the two-photon (TPA) and single-photon (SPA) absorption tests. The laser applied in the experiment has a wavelength of 1260 nm (energy of ∼0.98 eV) and spot size of ∼1.2 μm [3]. The sensitive region of the device is the InGaAs channel layer.

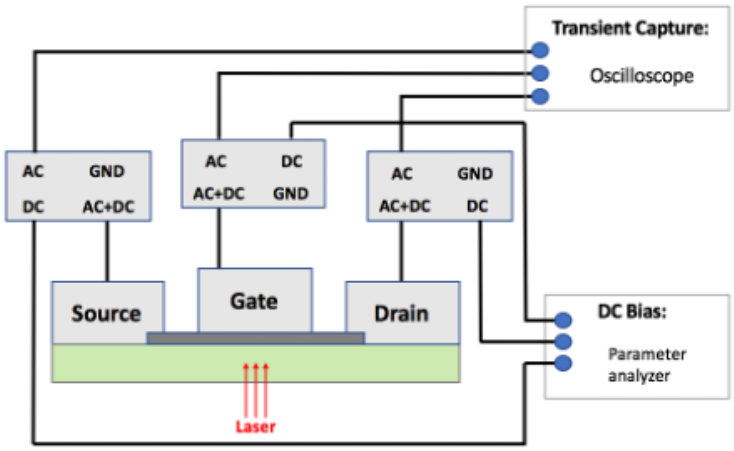


Figure 3.5: Schematic experimental setup of pulsed-laser-induced SET testing.

Figure 3.6: High-speed package for SET capture [14]

For pulsed-laser tests, DC bias are supplied by a semiconductor parameter analyzer (HP 4156A) through bias tees with 50-GHz bandwidth for the $I_D - V_{GS}$ measurements during the tests to make sure the devices were not damaged, as well as contributing to the tests of drain or gate bias dependences. A Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36-GHz front-end bandwidth and 80 GS/s sampling rate is used to capture the transients at each terminal. The schematic experimental connection is shown in Fig. 3.5. Devices under test are mounted in a custom-milled

high-speed brass package [108], shown in Fig. 3.6 [14]. Three terminals of the devices are wire-bonded to impedance-matched strip lines and terminated with SMA- or K- connectors. A hole is drilled in the center of the package and the devices are irradiated from the backside to avoid gate metal effects. The best focus is determined by both metal-reflected and transmitted illumination sources, confirmed by minimum laser spot size observed in the optical microscope image [3]. For each location at which the laser is focused, 100 transients are recorded and averaged.

3.3 Experimental Results and Analysis

3.3.1 Representative laser-induced SET pulse

Relevant band gaps and corresponding charge generation mechanisms are summarized in Table 3.1. Since the photon energy of the pulsed-laser is 0.98 eV (= 1260 nm), the charge is generated in the InGaAs channel primarily via single-photon absorption (SPA) as the photon energy is above the band gap, and from the InP and InAlAs layers via TPA as the photon energy is below its band gap [61], [106]. Hence, more of the incident laser energy is absorbed in the channel layer than in the InP or $In_{0.52}Al_{0.48}As$ layers due to the higher density of carrier generation induced by SPA over TPA.

Table 3.1: Charge generation mechanism for 1260-nm laser

Material	Band gap (eV)	Photon absorption mechanism
$In_{0.53}Ga_{0.47}As$	0.75	SPA/TPA
InP	1.35	TPA
$In_{0.52}Al_{0.48}As$	1.46	TPA

Fig. 3.7 shows a representative transient when the pulsed-laser is focused on the center of a device with 7 nm fin width under a bias condition of V_D = 0.5 V, V_S = 0 V, and $V_G = V_{th}$, where V_{th} is the threshold voltage and the initial values for all the devices are in the range of +0.35 $\pm$ 0.1 V. The gate voltage is set at V_{th} here and in the following experiments because it (1) corresponds to the maximum SET response in InGaAs planar devices [16], and (2) facilitates comparison with the wider fin devices in [15] at the same gate bias. The spot size is approximately 1.2 μm, as determined by a typical knife-edge optical spot size measurement at the beam waist [109], [110], and optical pulses were focused onto the DUT using a 100 $\times$ (NA 0.45) microscope objective. The maximum

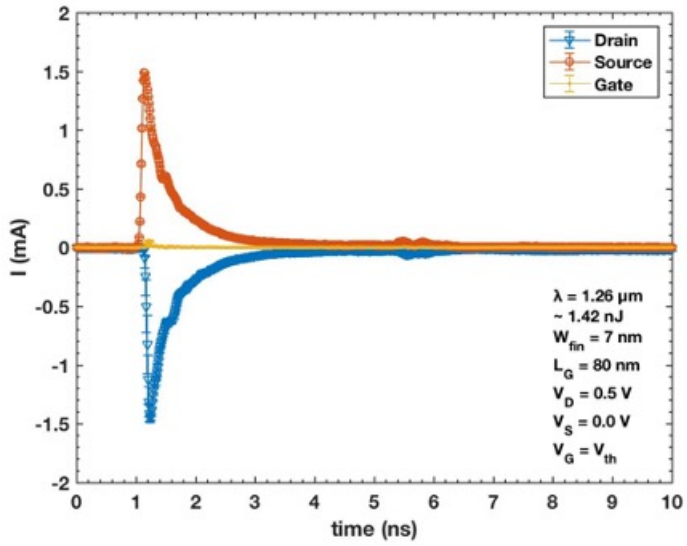


Figure 3.7: Representative SET signal of an InGaAs FinFET on semi-insulating InP with 7-nm fin width, L_G = 80 nm, V_{DS} = 0.5V, V_G - V_{th} = 0 V.

peak currents are observed when the center of the laser spot is located on the fin. Because the fin pitch is 0.2 μm, 6 of 34 fins are irradiated by each laser pulse.

The gate transient is almost negligible compared to those of the source and drain. This is due to the potential wells that define the channel both in the fin width and fin height directions, as shown in Fig. 3.8 (a) and (b), respectively. These wells effectively confine the carriers in the channel region with minimal carriers tunneling to the gate oxide and being collected by gate terminal, making the channel layer critical to the charge collection, similar to the behavior observed in the wider devices [15]. The nearly symmetric source and drain signals also suggest that the collected current is mainly from the channel. The quick rise and prompt peak of the current result from carrier drift in the channel, while the tail of the transient is mainly due to the diffusion of carriers from the substrate, and the deeper in substrate the charge is generated and collected, the longer the tail of the transient would be, which is consistent with previous work on the InP-based FinFETs [15], [70], [77], but differs significantly from the Si-based FinFETs with no tail currents observed in the SETs [67], [71] due to the substrate contact collection through the conductive substrate. The total collected charge for each SET is obtained by the integration of current vs. time beginning and ending at 10% of the peak current.

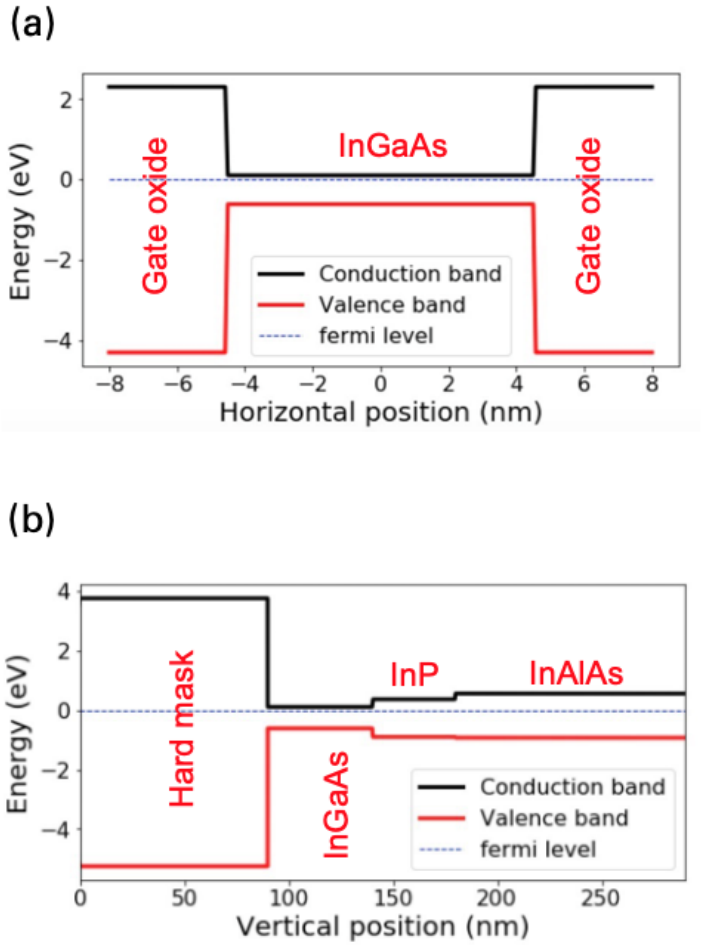


Figure 3.8: Band diagrams (a) across the fin width direction and (b) along the fin height direction.

3.3.2 Fin-width-dependence of pulsed-laser-induced SET

Figs. 3.9 (a) and (b) show changes of peak drain current and drain-collected charge along a line scan of the laser spot from source to drain for devices with different sub-10 nm fin widths (5nm, 7nm, 9nm). The center of the gate metal is defined as x = 0 μm; the gate length of all DUTs is 80 nm. The energy of a laser pulse at the die surface is approximately 1.4 nJ, extracted according to the calibrated energy peak relationship [111]. Devices are biased with V_D = 0.5 V, V_S = 0 V, and V_G - V_{th} = 0 V. The maximum SET responses are observed when the laser is focused in the channel region of these devices (x = 0 μm). The laser spot size is larger than the distance between the source and drain, so the laser-induced carriers shunt the channel [70], [69]. The response is small when the laser is focused on the source and drain because the semi-insulating InP substrate limits the

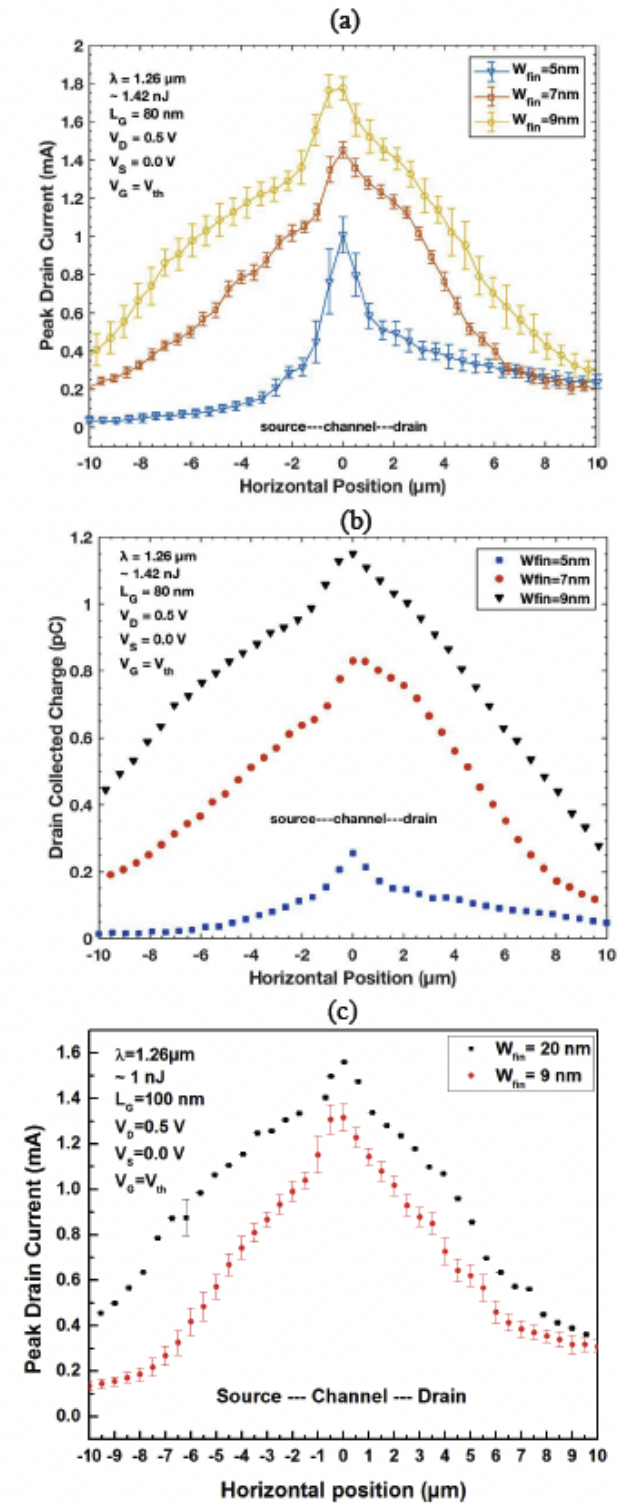


Figure 3.9: (a) Peak drain current and (b) drain collected charge change along a line scan of laser spot for InGaAs FinFETs with 5, 7, 9-nm fin widths. (c) Peak drain current of InGaAs FinFETs with 20-nm fin width from [15] with InGaAs FinFETs with 9-nm fin width.

collection volume [15]. The peak drain current shows some spatial asymmetry where it's higher in the drain side. This is because the drain side has a higher electric field. In addition, the peak drain current increases approximately linearly with fin width from 5 nm to 9 nm when the laser is focused on the channel, and the collected charge decreases when the fin width decreases, consistent with trends observed for devices with 20 nm and 30 nm fin width in [15]. In contrast to the peak drain current, the collected charge is not directly proportional to the fin width when the laser is focused on the channel, since the integral of the transient current with respect to time also includes carriers generated outside the fin and collected via diffusion. A possible reason for this scaling trend in SET response is that the charge generation by the laser pulse is nearly uniform over the small channel volume. As the laser spot has a waist of 1.2 μm and a Rayleigh length of about 15 μm [70], [112], the 50-nm thick InGaAs decreases the incident intensity less than 10% according to a Beer's law calculation [113]. Therefore, the laser intensity in the channel layer can be taken approximately evenly distributed, and the sensitive region for charge collection is proportional to fin volume. This scaling trend may also be related to the changes of the recovery time for source-channel barrier lowering and the area of the source-channel depletion region.

Consistent with this interpretation, Fig. 3.9 (c) shows that for comparable photon energies and the same gate length, the peak drain current of the device with 9 nm fin width (red dots) in this study is smaller than that of the device with 20 nm fin width (black dots) in [15]. Moreover, the fin pitch in [15] is 0.8 μm, while in this study, it is 0.2 μm. Since the radius of the laser spot is $\sim$0.6 μm, only one fin is irradiated in [15], but several fins are covered by the laser spot in this study. Hence, the SET response of a single fin for the device with 9 nm fin width is even smaller than it appears in Fig. 3.9 (c), compared to the device with 20-nm fin width in [15]. A direct comparison of SET response in the range of 5 nm to 30 nm is provided later in the discussion subsection.

3.3.3 Bias-dependence of pulsed-laser-induced SET

Fig. 3.10 (a) and (b) show changes of peak drain current and drain collected charge along a line scan from source to drain for a device with Wfin = 9 nm under different drain biases with $V_G = V_{th}$. For $V_S = V_D = 0$ V, the transients are mainly from the junctions, since there is no electric field along the channel, and transients are much smaller than when bias is applied between source and drain. Therefore, when $V_D \ \ V_S$, the transients are mainly from charge collection in the channel. The

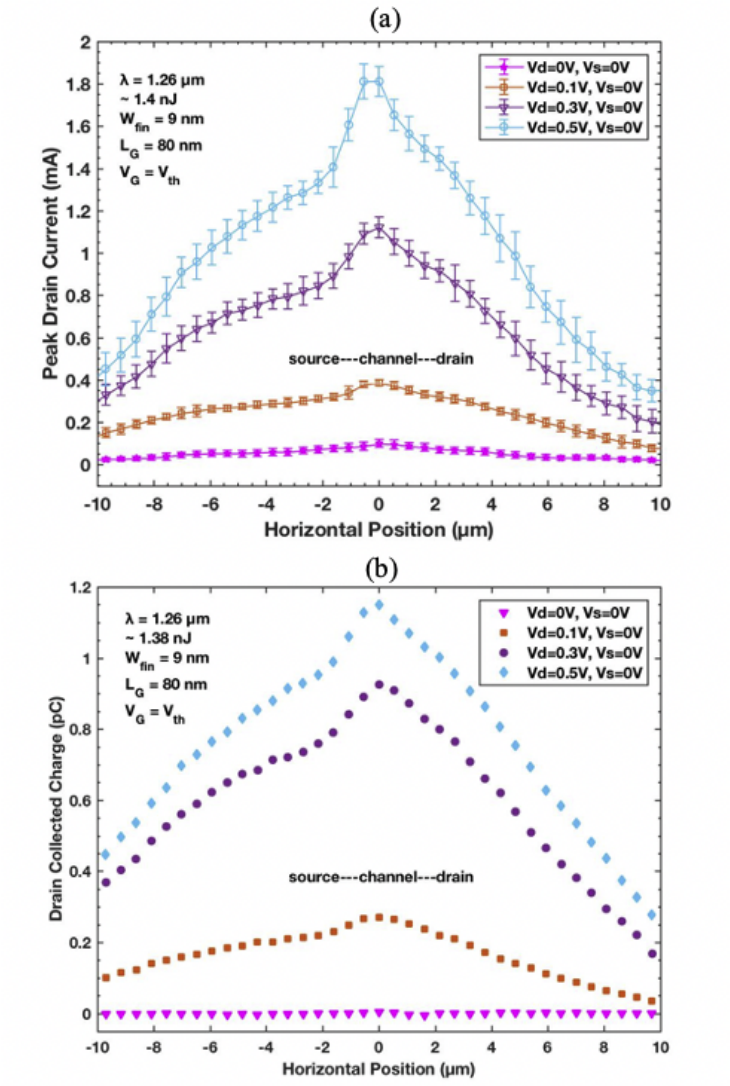


Figure 3.10: (a) Peak drain current and (b) drain collected charge change along a line scan under different source and drain biases.

peak drain current and collected charge increase with drain bias, because higher electric field along the channel promotes enhanced charge-collection efficiency. This phenomenon is also observed in devices with wider fin widths [15], [70], [71]. The transients are collected mainly because of the laser-shunt and parasitic bipolar mechanisms discussed in [70]. Since the gate length is only 80 nm, while the diameter of the laser spot is about 1.2 μm, the shunt effect plays a role when the laser spot covers the channel, during which the photoexcited carriers short the source and drain, resulting in a large prompt current [70], [69]. The parasitic bipolar effect also plays an important role when

laser-induced holes accumulate under the channel due to their low mobility. This decreases the source-channel barrier and induces a source-to-drain current pathway [70]. Consequently, when the laser spot is away from the channel, for example, x = $\pm$ 4 m, significant transients are still observed, which are much higher than those produced when the laser strikes the source or drain junctions with $V_S = V_D = 0$. This phenomenon is also significantly different from what is observed in Si-based InGaAs FinFETs [71], or Si and SiGe FinFETs [67], [69], [101], for which a large amount of charge is collected when source and drain terminals are tied together, indicating that the junction plays a big role in charge collection as there is no electric field along the channel.

Fig. 3.11 shows drain current transients for the device with Wfin = 7 nm at different gate biases when the device is biased on. The laser spot was centered on the channel. V_DS was fixed at 0.5 V. Here, the overdrive voltage $V_{OV} = V_{GS}$-V_{th}. The peak drain current does not change significantly with the overdrive voltage, in contrast to planar III-V MOSFETs [77]. The small bump at $\sim$ 1.5 ns is due to reflection of the signal from one of the components in the signal path between the DUT and the oscilloscope.

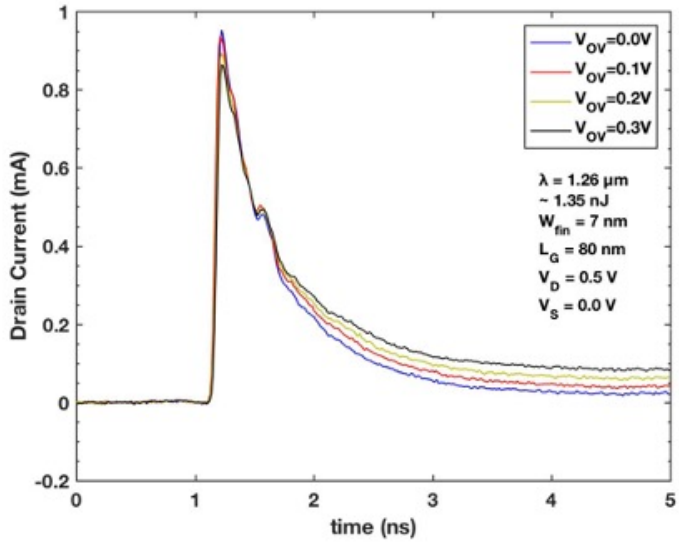


Figure 3.11: Drain current transients for InGaAs FinFETs with W_{fin}=7 nm at several gate bias conditions.

This occurs because the device is controlled by the two side gates and they have limited effect on the substrate below the fin. However, in planar III-V MOSFETs [77], the excess electron density, which is the absolute electron density difference between the post-strike and pre-strike condition,

decreases substantially in inversion. That is because the post-strike electron densities are almost same for different gate voltage due to a very large number of carriers generated during irradiation, while the pre-strike electron density increases with the overdrive voltage in the planar devices. In addition, the tail current is higher when the overdrive voltage is larger, similar to the responses of wider fin devices in [70] and GaAs MESFETs in [75].

3.3.4 Energy-dependence of pulsed-laser-induced SET

Fig. 3.12 shows the peak drain current (left axis) and drain collected charge (right) dependences on the pulsed-laser energy for the device with W_{fin}=5 nm. The bias condition was fixed at V_{GS}=V_{th} and V_{DS} = 0.5 V. As energy increases, more carriers are generated, resulting the increases of peak current and collected charge. The sublinear relationship shows that under the laser irradiation of = 1260 nm, both single-photon absorption and two-photon absorption take place during the carrier generation process.

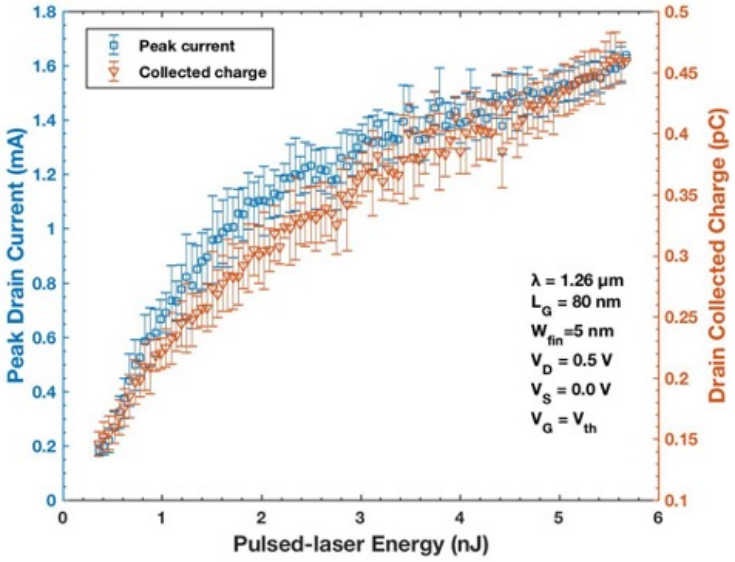


Figure 3.12: Peak drain current (left) and drain collected charge (right) change with the pulsed-laser energy.

3.4 TCAD Simulation

To further understand the charge collection mechanisms, 3-D technology computer-aided design (TCAD) simulations were performed. All the key parameters of the simulated devices including

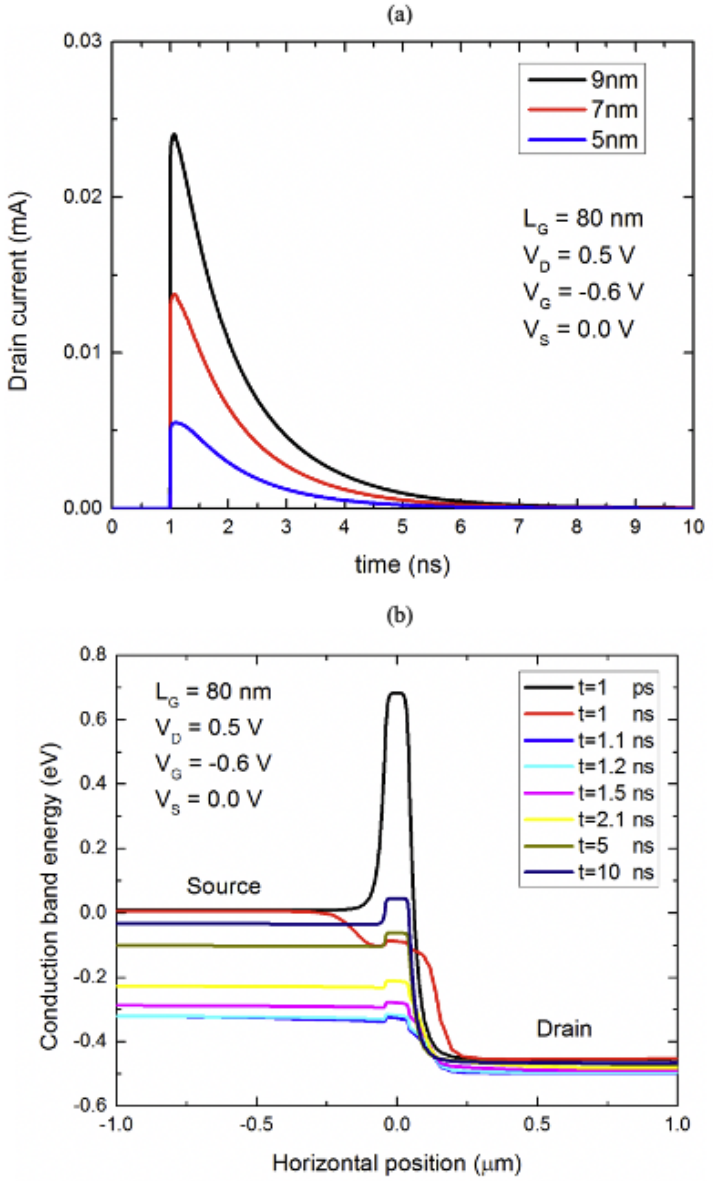


Figure 3.13: (a) Drain current transients for InGaAs FinFETs with sub-10-nm fin widths in TCAD simulations. (b) Evolution of conduction band energy along the channel. Charge was injected at 1 ns.

gate length, fin width and thickness of different layers are the same as the tested devices, except for the thickness of the InP semi-insulating substrate which is truncated to 20 μm for efficiency. The simulation structure included one fin; additional parallel fins exhibit the same trends and mechanisms. The SETs were simulated by injecting charge with a Gaussian distribution in both time and space. The characteristic width of the Gaussian distribution is 50 nm and the strike is centered at

1 ns with a characteristic time of 2 ps. The amount of the deposited charge is 76 fC/μm along 8 μm vertically from the top of the gate to the substrate, centered at the middle of the channel. The parameters used in the TCAD simulations are the same as those used in the previous work for wider fin devices [70], [15], which allows us to establish consistency with the fin width dependence of the SETs that was reported previously for the larger devices.

Fig. 3.13 (a) shows the simulated drain current as a function of time for devices with three different fin widths (all less than 10 nm). The quick rise of the current, followed by a relatively long tail is consistent with the experimental results shown in Fig. 3.7. Moreover, devices with wider fins exhibit higher current peaks as well as more charge collection, which also agrees with the experimental data shown in Figs. 3.9 (a) and (b). Fig. 3.13 (b) shows the time evolution of the conduction band energy for the device with W_{fin} = 9 nm along the channel from source to drain,before and after the charge injection. The source-channel barrier drops quickly when the charge is deposited and recovers to about 0.1 eV at 10 ns. This barrier-lowering phenomenon, as a result of the accumulated holes under the channel layer, demonstrates the parasitic bipolar effect in the charge collection. These simulation results for devices with sub-10-nm fin widths are consistent with those of wider fin devices [70], [15].

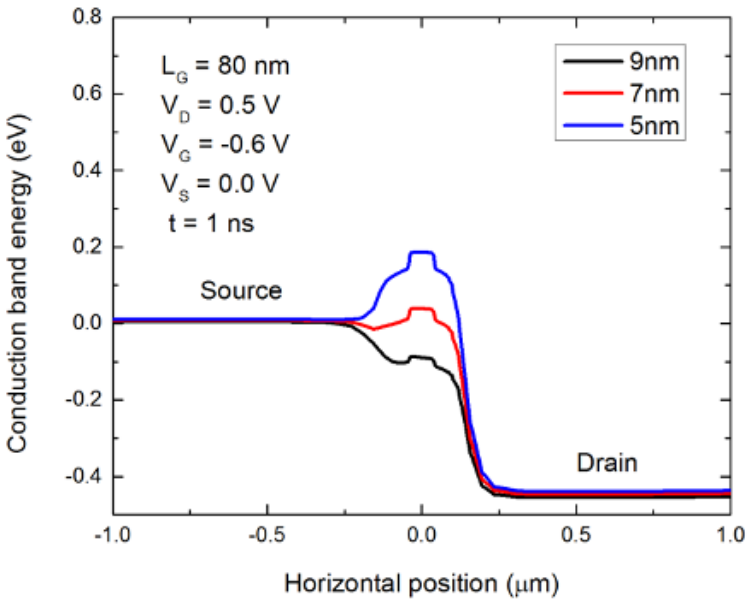


Figure 3.14: Conduction band energy along the channel layer for the devices with different fin widths in the sub-10-nm region, at 1 ns (peak of the charge deposition).

To extend the understanding of parasitic bipolar effects in previous work in [70], [15], [75], [114] to smaller fins, Fig. 3.14 illustrates the conduction band energy along the channel for devices with different fin widths in the sub-10-nm region. The time corresponds to the peak charge deposition. Lower source-channel barriers are observed in devices with wider fins, indicating a stronger parasitic bipolar effect and more charge collection.

3.5 Discussion

To facilitate comparison to the wider-fin devices in [15] and illustrate scaling effects, the SET response of the devices with sub-10-nm fin widths in Fig. 3.9 (a) is scaled empirically to account for the laser energy, the gate length, and fin number to compare the two sets of devices more directly. Scaling the results by the ratio of peak drain currents at x = 0 for the devices with W_{fin} = 9 nm in Figs. 3.9 (a) and Fig. 3.9 (c) leads to excellent agreement of the curves.

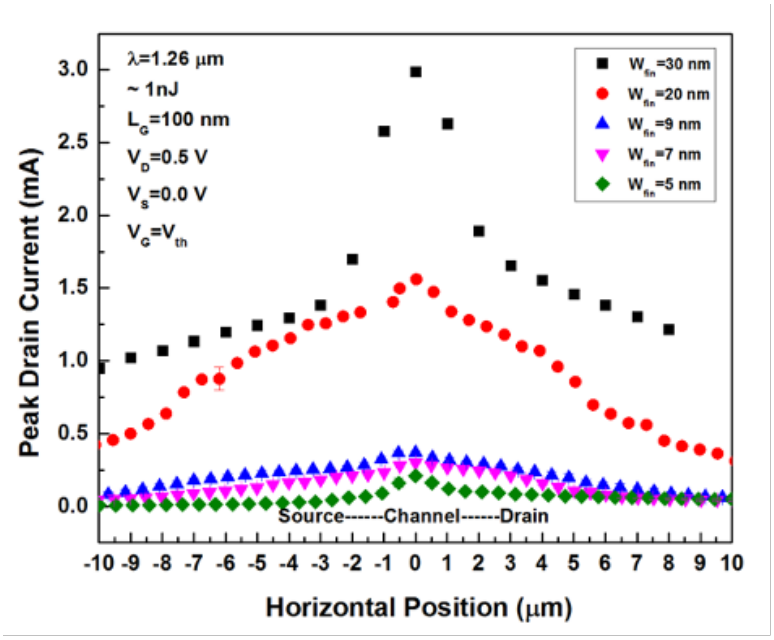


Figure 3.15: Peak drain current along a line scan for InGaAs FinFETs with W_{fin} = 20, 30 nm from [15] and scaled response of devices with Wfin = 5, 7, 9 nm in this work.

Fig. 3.15 shows the peak drain current along a line scan for the devices with fin widths from 5 nm to 30 nm incorporating the previous data in [15] and the scaled data in this study. Fig. 3.16 illustrates the scaled drain peak current for a single fin under irradiated at channel region x = 0 μm as a function of fin width. The SET response varies directly with the fin width for the entire range of the

devices tested in the two studies. This is a qualitative comparison to evaluate whether previously observed trends in wider devices also occur in devices with narrower (and more technologically relevant) fins. However, the two sets of devices were fabricated with different layouts on different process runs. Testing conditions and laser calibrations were not exactly identical. To obtain an accurate quantitative relation between fin width and SET response over the full range of widths would require testing the same types of devices from the same test chip under identical experimental conditions.

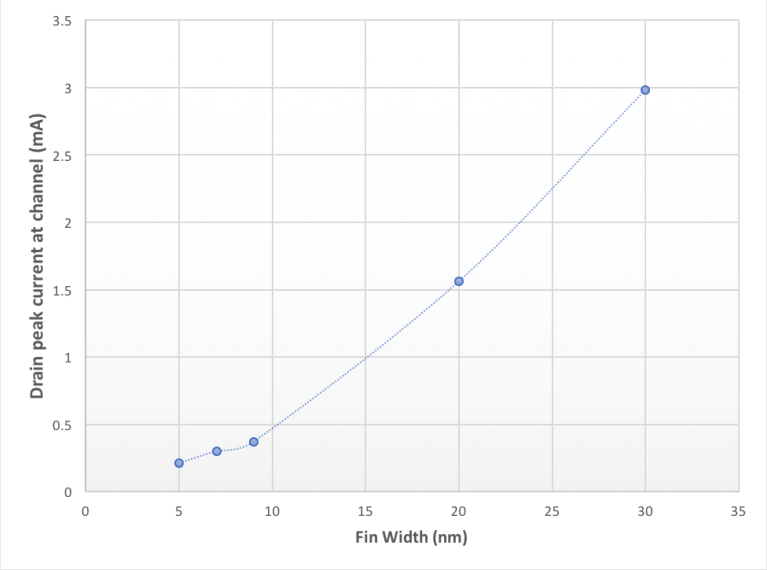


Figure 3.16: Scaled peak drain current for a single fin under irradiated at channel region x = 0 μm as a function of fin width from 5 nm to 30 nm.

3.6 Summary and Conclusion

The laser-induced SET response is investigated for InGaAs FinFETs on InP with sub-10-nm fin widths. Consistent with results of devices with 20 and 30 nm fin widths, more charge and higher peak currents are obtained in wider fin devices, which is likely due to an increase of sensitive volume for charge collection. This scaling trend may also be related to the changes of the recovery time for source-channel barrier lowering and the area of the source-channel depletion region. The collected charge is mostly from the channel, when the source or drain is biased, with negligible contributions from junction depletion-region charge collection. Higher drain-to-source bias produces higher electric fields along the channel, creating larger peak currents and enhanced charge collec-

tion. Larger overdrive voltage does not change the peak current in the channel a lot but increases the tail current from the substrate. Charge collection is influenced strongly by the laser-shunt when the laser spot is on the channel, and by parasitic bipolar effects caused by accumulated holes underneath the channel. The TCAD simulations agree with the fin-width dependence of SETs observed in the experiments and demonstrate that the parasitic bipolar effect is stronger in wider-fin devices. These results significantly extend the range of scaling trends observed in wider-fin devices, and reinforce the potential utility of highly scaled InGaAs FinFETs in space electronics.

CHAPTER 4

Impacts of Through-Silicon Vias on Total-Ionizing-Dose Effects and Low-Frequency Noise in Advanced FinFETs

This chapter is adapted from "Impacts of Through-Silicon Vias on Total-Ionizing-Dose Effects and Low-Frequency Noise in FinFETs" published in IEEE Transactions on Nuclear Science, and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Mariia Gorchichko, Peng Fei Wang, Mahmud Reaz, Simeng E Zhao, Gaspard Hiblot, Stefaan Van Huylenbroeck, Anne Jourdain, Michael L Alles, Robert A Reed, Daniel M Fleetwood, Ronald D Schrimpf.

- K. Li *et al.*, "Impacts of Through-Silicon Vias on Total-Ionizing-Dose Effects and Low-Frequency Noise in FinFETs," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 740-747, May 2021.

4.1 Introduction

As scaling has pushed gate-dielectric and junction technologies closer to physical limits, three-dimensional (3D) integrated circuits (ICs) have drawn much attention due to enhancement of chip performance, functionality, and device packing density [55]. In 3D-IC technology, multiple layers of chips are stacked vertically and electrically connected by through-Si vias (TSVs) and microbumps. These provide shorter total interconnection length compared with 2D-ICs [2]. The reduced interconnection length can improve the wiring efficiency ($\sim$15%), decrease the total active power (more than 10%), and reduce fabrication cost [54]. However, the manufacturing process of TSVs may also modify charge trapping properties of gate and field oxides. For example, local mechanical stress and defects may be induced in the field oxide during thermal cycling and wafer thinning [115]; plasma-induced charging during TSV etching could lead to enhanced trap generation in gate or isolation oxides [16, 116, 117]; or dose enhancement effects [32], [118] around the TSV filling metal could increase doses in nearby oxides. Therefore, it is important to evaluate the impact of TSV integration on the total-ionizing-dose (TID) response and low-frequency noise of these devices in advance of potential use in high-radiation environments, such as space systems or particle accelerators [32], [35].

In this work [17], Total-ionizing-dose (TID) effects and low-frequency noise are evaluated in advanced bulk nMOS and pMOS FinFETs with SiO_2/HfO_2 gate dielectrics. Otherwise identical devices built with and without through-silicon via (TSV) integration exhibit threshold voltage shifts of less than 25 mV and changes in maximum transconductance of less than 1% up to 2 Mrad(SiO_2). TSV integration negligibly impacts threshold shifts and degradation of subthreshold swing and I_{on}/I_{off} ratios. Similar low-frequency noise magnitudes and frequency dependences are observed before and after TID irradiation for each device type. Effective densities of the near-interfacial electron traps responsible for the noise in the *n*MOS devices increase as the surface potential moves toward midgap, while effective densities of the hole traps that cause the noise in the *p*MOS devices increase as the surface potential moves toward the valence band edge.

4.2 Device and Experiments

Bulk FinFETs with/without TSV via-last integration near the transistor channel ($\sim$1 μm) were fabricated by imec [16]. The TSV has a diameter of 1 μm and a depth of 5 μm, isolated by a 100 nm thick SiO_2 liner, and filled with Cu. The FinFET features a replacement metal gate, in-situ doped epitaxial junctions, and has 2-levels of Damascene tungsten local interconnects. Fig. 4.1 (a) shows the cross-section of the technology [16]. There are 220 fins in the FinFETs with height = 26 nm, width = 7 nm, and pitch = 45 nm. The gate length is 1 μm; the gate dielectric consists of a 0.5 nm thick SiO_x interfacial layer and a 2 nm thick HfO_2 layer; the effective oxide thickness (EOT) is 0.9 nm. The gate metal is tungsten with a thin layer of work-function metal close to the gate oxide. Fig. 4.1 (b) shows the side-view schematic diagram of an individual fin.

Devices were irradiated at room temperature at Vanderbilt University using an ARACOR Model 4100 X-ray irradiator with peak energy deposition at $\sim$10 keV [32]. The dose rate was 30.3 krad(SiO_2)/min. All devices were irradiated in steps to a cumulative dose of 2 Mrad(SiO_2), followed by annealing for 60 min at room temperature (RT). Ionizing doses and dose rates are referred to equilibrium dose in SiO_2 to be consistent in calibration and facilitate comparison with other work [32]. During irradiation and annealing, devices are biased under conditions similar to those of typical device operation: "+1 V" (V_{gs} = +1 V, V_{ds} = 0 V), "0 V" (V_{gs} = 0 V, V_{ds} = 0 V), and "-1 V" (V_{gs} = -1 V, V_{ds} = 0 V). Source, drain, and body contacts were grounded during irradiation.

$I_d - V_g$ transfer characteristics were measured at V_d = 0.05 V with an Agilent 4156B semicon-

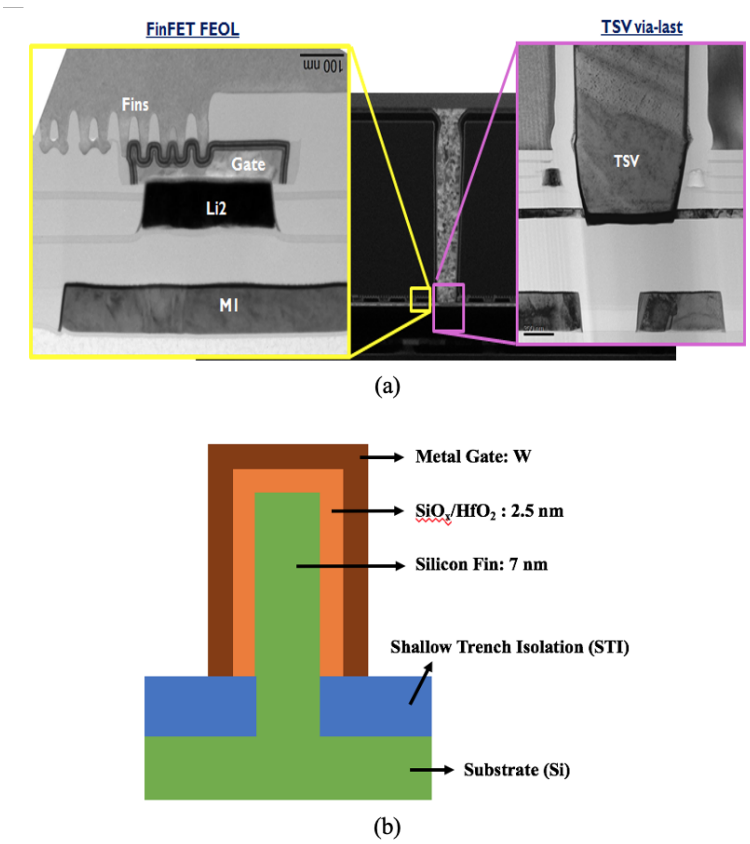


Figure 4.1: (a) Cross-sectional diagram of a bulk FinFET with 1×5 μm TSV via-last integration [16]. (b) Side-view schematic diagram of an individual fin

ductor parameter analyzer. For each device, the IV curves were measured before irradiation, after a accumulative dose of 30 Krad, 100 Krad, 200 Krad, 300 Krad, 500 Krad, 1 Mrad, 2 Mrad(SiO_2), and after annealing of 5, 15, 30, 60 minutes, respectively. The threshold voltage V_{th} is estimated by calculating the x-intercept of the linear extrapolation of the $I_d - V_g$ curve at its maximum first derivative and subtracting $V_d/2$ [119]. More than 24 devices were tested in this work. At least 12 included TSV-last integration; at least 12 were nominally equivalent but without TSV integrated. At least two devices of each type were measured for all results reported here. For each condition, device-to-device variation in radiation response is less than 10%; error bars denote ranges of device responses.

The noise power spectral density S_{V_d} was measured at room temperature for a frequency range from 2 Hz to 400 Hz with correction for background noise [39]. The drain voltage was 0.05 V. The gate voltage varied from 0.1 V to 0.45 V above V_{th} for nMOS, and varied from -0.1 V to -0.45 V

below V_{th} for *p*MOS; the source, body, and substrate were all grounded.

4.3 Experimental Results and Discussion

4.3.1 Impact of TSV via-last integration on TID effects

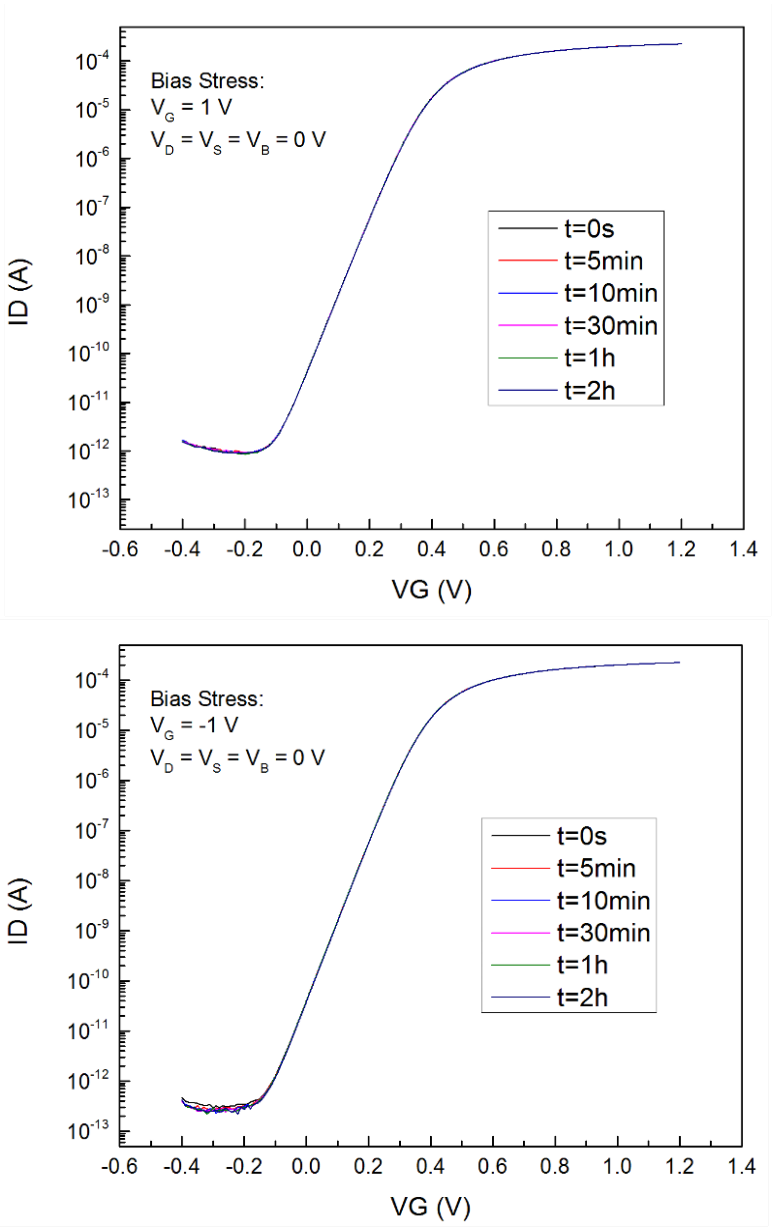


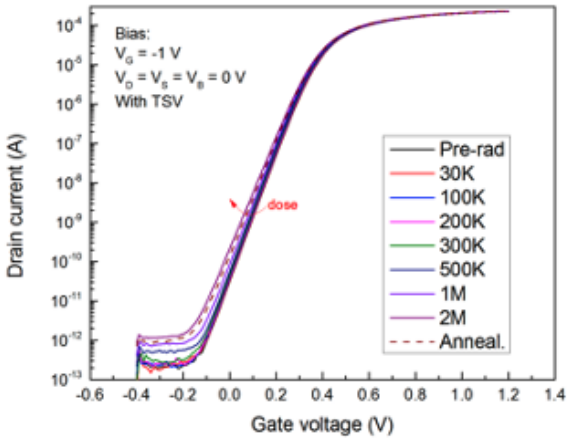
Figure 4.2: $I_d - V_g$ transfer characteristics at $V_d = 0.05$ V for an *n*MOS FinFET with TSV integration at "+1 V", "-1 V" biasing condition, for a duration (2h) comparable to that applied during TID irradiation and annealing processes. All curves lie on top of one another.

That unirradiated devices biased with times and voltages similar to those applied during TID irradiation and annealing is typically carried out to examine the stability of the devices and separate

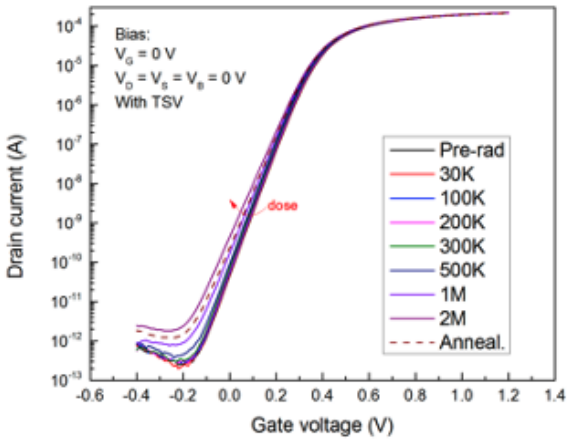
the effects of TID irradiation from the applied bias through the shifts in the IV curves [120]. For example, Fig. 4.2 shows $I_d - V_g$ transfer characteristics at V_d = 0.05 V for an *n*MOS FinFET with TSV integration at "+1 V" and "-1 V" biasing condition, respectively, for a duration (2h) comparable to that applied during TID irradiation and annealing processes. All curves lie on top of one another, demonstrating the excellent stability of unirradiated devices with TSV integration under different bias conditions. V_{th} shifts less than 2 mV, and the on-state current changes less than 5%. Same outstanding stability is also observed in *p*MOS and the devices without TSV integration under all different bias conditions.

Fig. 4.3 shows $I_d - V_g$ curves at Vd = 0.05 V for *n*MOS FinFETs with TSV integration irradiated up to 2 Mrad(SiO_2) and annealed for 60 min at room temperature under "-1 V", "0 V" and "+1 V" bias conditions. Devices irradiated under the "-1 V" bias condition showed shifts comparable to or smaller than those of the devices irradiated under the "0 V" bias condition, and devices irradiated under "+1 V" bias condition exhibit the largest changes. Fig. 4.4 shows similar results for *n*MOS FinFETs without TSV integration. For both device types at all bias conditions, off-state leakage currents increase with the total dose. This is due to the increase of radiation-induced trapped charge in the shallow trench isolation (STI) of the sub-fin region shown in Fig. 4.1 (b). As the devices were under irradiation, the incident high-energy particles will also generate a large number of electron-hole pairs in the STI oxide region, in which electrons can easily be swept out due to there high mobility, while holes are likely to be trapped by the defects as they move very slow in the oxides. Therefore, these trapped positive charges can invert the p-type silicon near the STI edge and create a parasitic leakage path from drain to source [121–123]. Among these bias conditions, the leakage currents increase most for the "+1 V" condition, indicating that the trapped-charge density in the STI is highest for irradiation under this bias condition.

For each case, the off-state leakage current increases with the total ionizing dose, since the more incident particles come into the STI region, the more electron-hole pairs are generated, thus forming more positively charged traps. The 1-hour annealing after 2 Mrad(SiO_2) under each condition facilitates the positively charged traps to recover due to the neutralization of electrons, and that's why the dash lines (device after annealing) in all bias conditions show less leakage currents than those in irradiated device after a total dose of 2 Mrad(SiO_2). The changes of key parameters before and after irradiation will be discussed and analyzed later.



(a)



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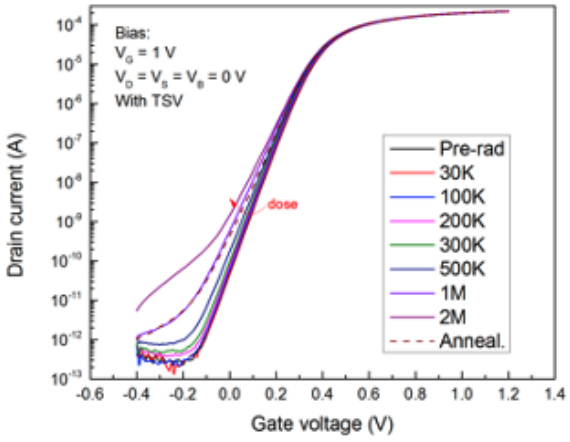
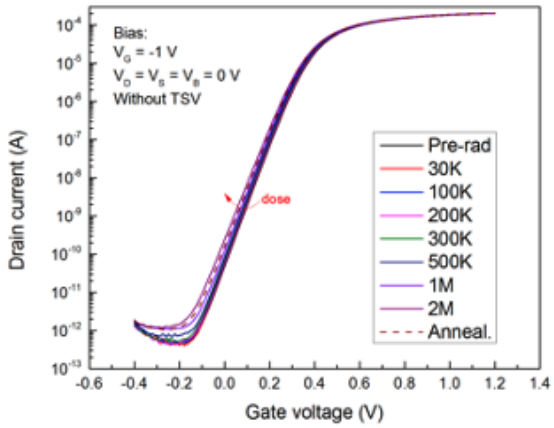
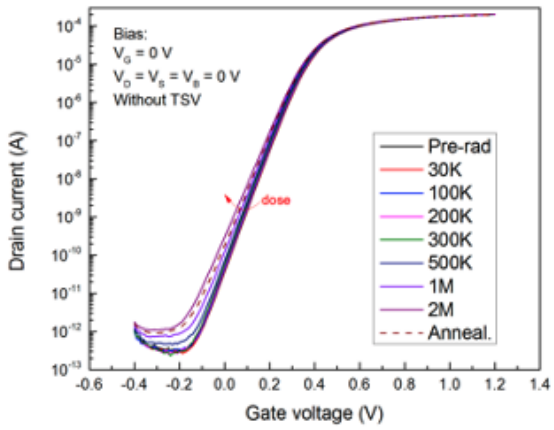


(c)

Figure 4.3: $I_d - V_g$ curves at Vd = 0.05 V for *n*MOS FinFETs with TSV integration near the channel as functions of dose up to 2 Mrad(SiO_2) and annealing at RT for 1 hour for the (a) "-1 V", (b) "0 V", and (c) "+1 V" bias conditions.



(a)



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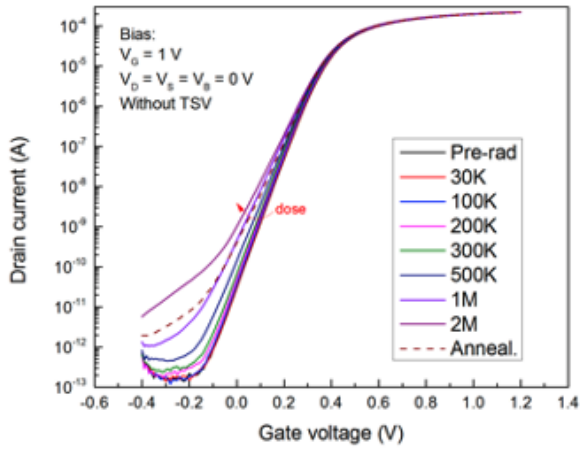
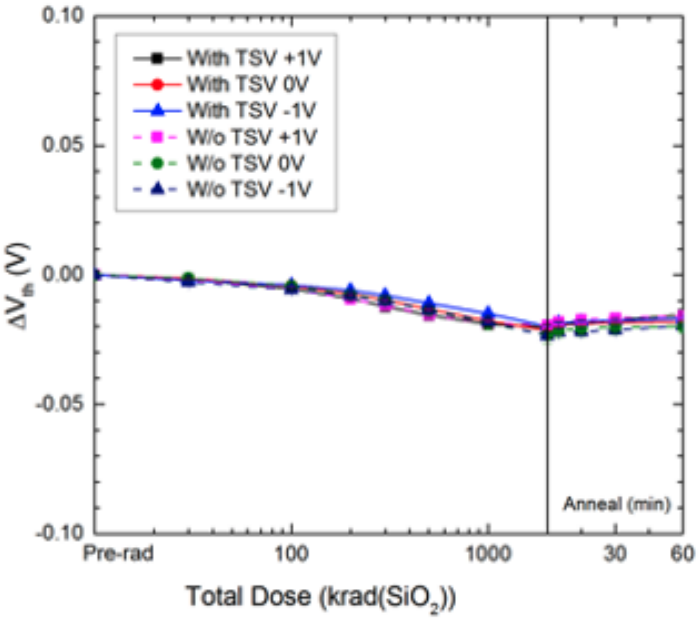
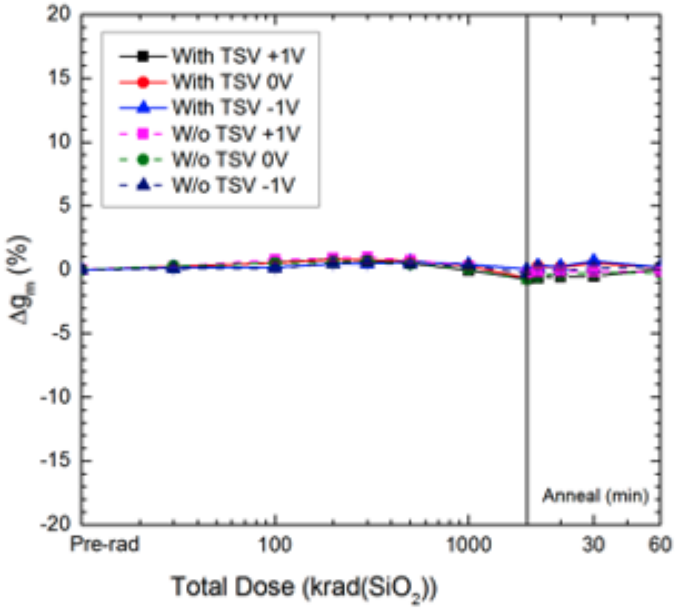


(c)

Figure 4.4: $I_d - V_g$ curves at Vd = 0.05 V for *n*MOS FinFETs without TSV integration near the channel as functions of dose up to 2 Mrad(SiO_2) and annealing at RT for 1 hour for the (a) "-1 V", (b) "0 V", and (c) "+1 V" bias conditions.



(a)



(b)

Figure 4.5: (a) V_{th} shifts and (b) normalized maximum transconductance variations for *n*MOS bulk FinFETs with TSV integration (solid lines) and without TSV integration (dash lines) irradiated and annealed at RT in the "-1 V", "0 V", and "+1 V" bias conditions. Error bars denote the ranges of device responses.

From the IV curves in Fig. 4.3 and Fig. 4.4, several key electric parameters of the devices such as threshold voltage, maximum transconductance, substhreshold swing and I_{on}/I_{off} ratio can

be extracted to evaluate the property change of gate or field oxide during the irradiation. Fig. 4.5 shows (a) V_{th} shifts and (b) changes in maximum transconductance for the devices of Figs. 4.3 and 4.4 for all three irradiation bias con-ditions; Fig. 4.6 shows (a) degradation of subthreshold swing and (b) changes in I_{on}/I_{off} ratios. The parameters of devices with TSV integration are shown in solid lines; dashed lines represent those without TSV integration. V_{th} shifts of less than 0.025 V are found in all cases, and less than 10% variation in response is observed for device types irradiated under similar bias conditions. Given that the gate voltage sweep step is 10 mV, a 25 mV of change in threshold voltage is almost negligible under TID irradiation. This excellent TID response is consistent with a low density of net radiation-induced trapped positive charge in the gate dielectric layers and outstanding gate electrostatic control because of the FinFET structure [122–125].

In a typical *n*MOSFET, the drive current can be described as:

$$I_D = \frac{\bar{\mu_n} W C_i}{L}[(V_G - V_T)V_D - \frac{1}{2}V_D^2] \tag{4.1}$$

Where $\bar{\mu_n}$ is the surface electron mobility (not the same as the mobility in the bulk material), W and L are the width and length of the channel respectively, C_i is the capacitance of the insulator. Obviously, $\frac{\bar{\mu_n} Z C_i}{L} = k_N$ is proportional to the transconductance of the n-channel MOSFET, and this also applies to FinFETs in general.

Therefore, for a given FinFET with fixed channel length, width and gate dielectric, the change in transconductance can be the indicator of the variation in surface electron mobility, which can be affected by the interface trap generation during the TID irradiation. From Fig. 4.5 (b), changes in maximum transconductance are less than 1% for all devices and bias conditions. This also demonstrates that the TID effects on the gate oxide for both types of devices are minimal. In addition, considering the similarly small shifts in V_{th} and G_m change, the whole result shows that the impact of TSV via-last integration on TID effects in the gate oxide is negligible.

The degradation of the subthreshold swing and I_{on}/I_{off} ratios (here defined as I_{on} at V_g = 1 V and I_{off} at V_g = –0.2 V) in both devices result from off-state sub-fin leakage [121–123]; less than 3% decreases are observed in on-state currents in all cases. Fig. 4.6 confirms that the worst-case degradation of subthreshold characteristics and off-state leakage current occur for "+1 V" bias condition, with the "0 V" case showing the next highest, and the "- 1 V" case the least. These

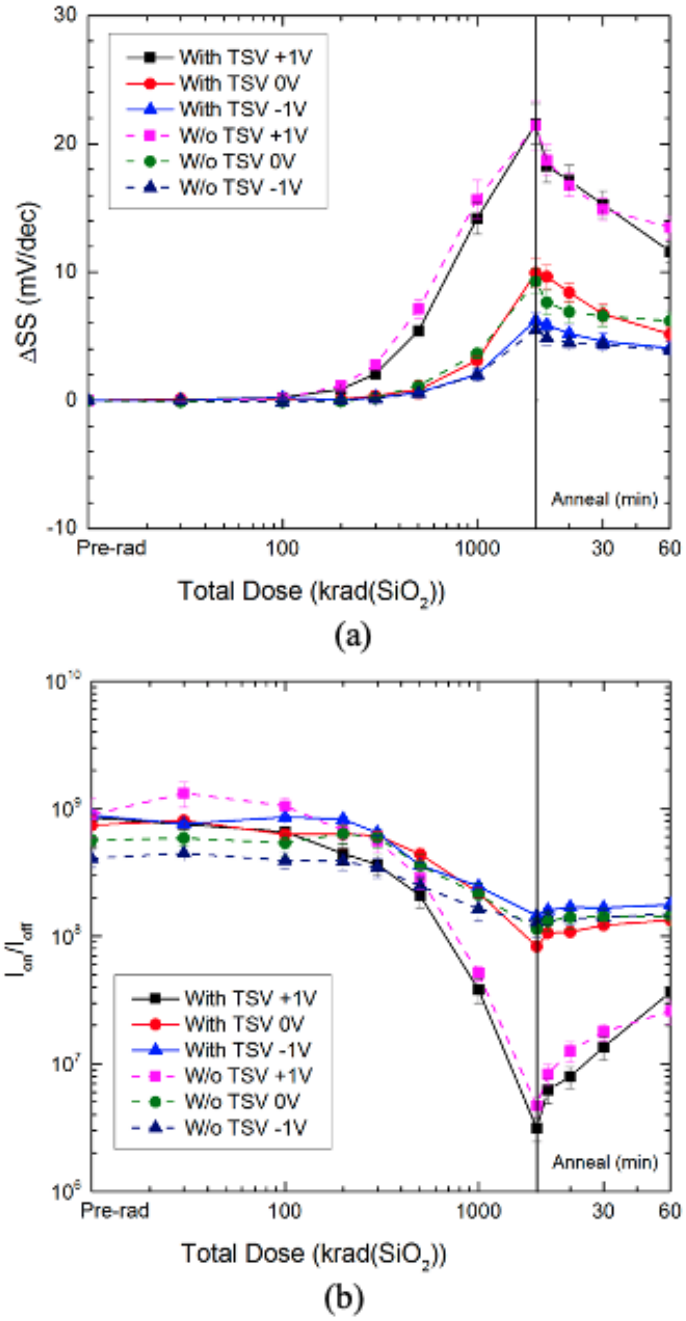


Figure 4.6: Changes in (a) subthreshold swing degradation and (b) I_{on}/I_{off} ratios as functions of dose and RT annealing for the nMOS devices and experimental conditions of Fig. 4.5. Error bars denote the ranges of device responses.

trends in subthreshold response with bias evidently are observed because, when the work function difference Φ_{ms} of $\sim$ 0.6 eV is taken into account for the calculation of gate-oxide electric field, the "+1 V" case has the highest electric field (6.4 MV/cm), the "0 V" case has the next highest

electric field (2.4 MV/cm), and the "-1 V" case has the lowest electric field (1.6 MV/cm). Trends in electric field magnitude and direction in the STI regions in closest proximity to the channel that determine the level of the observed subthreshold leakage scale similarly [121], [124], [125]. Hence, the highest charge yield and densities of trapped-oxide charge in the STI are found for the "+1 V" case, and reduced yields and charge trapping densities are observed in the "0 V" and "-1 V" cases [32], [41], [122], [123] [125–128]. Positive gate bias also enhances the density of trapped positive charge at the interface of the STI and channel, relative to the "0 V" and "-1 V" cases [32], [129]. Hence, the leakage path under the fins is affected the most in the "+1 V" case, with the "0 V" case the next, and the "-1 V" case the least. Incorporating with the $I_d - V_g$ curves shown in Fig. F.3 and Fig. 4.4, it can be inferred that the degradation in subthreshold swing and I_{on}/I_{off} ratio is the result of the increase of the leakage current in the off-state region. Therefore, the changes of these two parameters can reflect the modification of field oxide (STI in the sub-fin region) charge-trapping properties. The similar variations for both device types under the three bias conditions shown in Fig. 4.6 demonstrate that the impact of TSV via-last integration on TID effects in the field oxide is also minimal.

Similar as Fig.4.3 and Fig. 4.4, $I_d - V_g$ curves at Vd = 0.05 V for *p*MOS FinFETs with and without TSV integration near the channel as functions of dose up to 2 Mrad(SiO_2) and annealing at RT for 1 hour for the (a) "-1 V", (b) "0 V", and (c) "+1 V" bias conditions are shown in Fig. 4.7 and Fig. 4.8, respectively. As seen with the *n*MOS device, similar TID responses are observed with and without TSV integration. For both types of *p*MOS FinFETs, the threshold voltage shifts by less than 6 mV, maximum transconductance changes less than 10%, and subthreshold swing changes less than 10% before and after irradiation. These similar results observed for *p*MOS devices irradiated under all three bias conditions again show that the impact of TSV integration on TID effects is negligible in these devices. However, compared to the *n*MOS devices, the *p*MOS devices exhibit very limited increase in leakage currents, regardless of different bias conditions they are applied with. This is because, to form a leakage path in a *p*MOS device, the polarity of carriers in *n*-type substrate surface have to be inverted to holes, which requires the trapped charge in the STI to be negative. However, the positively charged traps are the dominant traps in the sub-fin STI as mentioned before as a result of mobility difference of electrons and holes. Therefore, the leakage current does not change with TID irradiation dose too much in *p*MOS devices, no matter what bias conditions are applied.

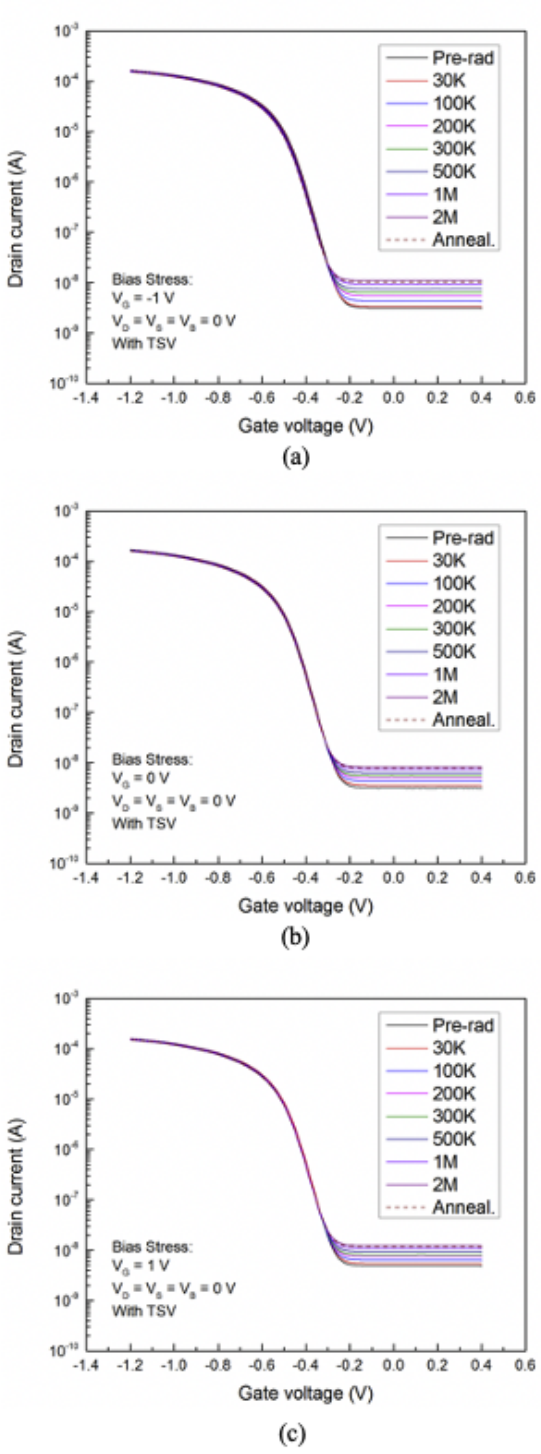


Figure 4.7: $I_d - V_g$ curves at Vd = 0.05 V for *p*MOS FinFETs with TSV integration near the channel as functions of dose up to 2 Mrad(SiO_2) and annealing at RT for 1 hour for the (a) "-1 V", (b) "0 V", and (c) "+1 V" bias conditions.

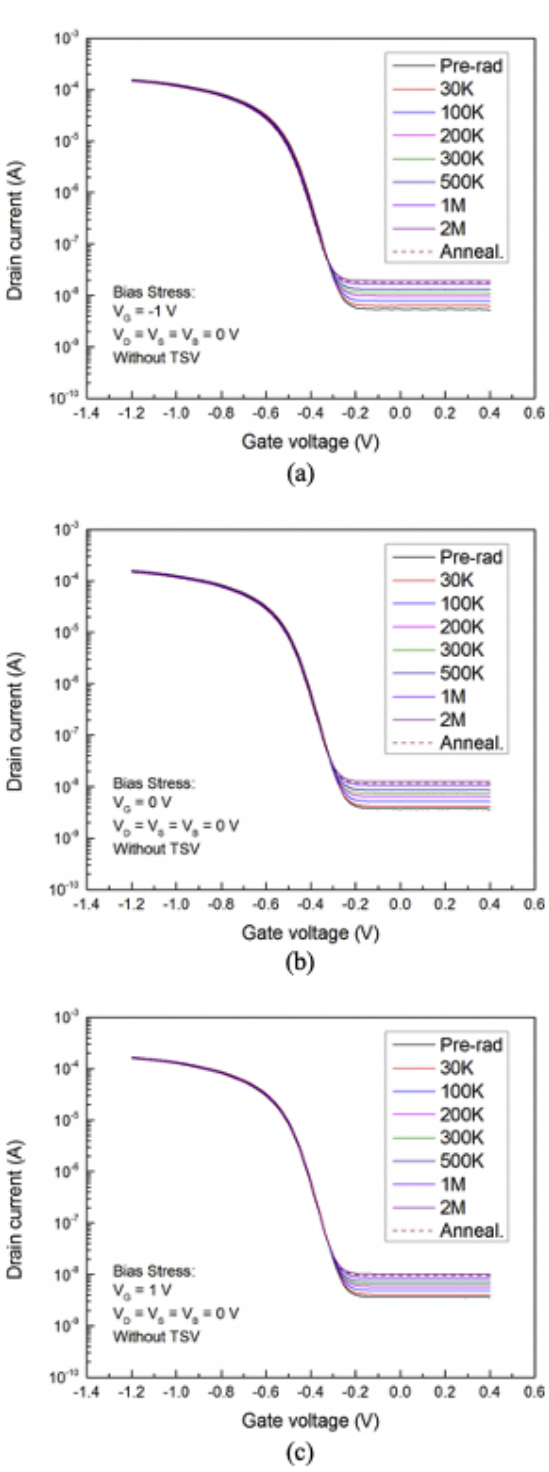


Figure 4.8: $I_d - V_g$ curves at Vd = 0.05 V for *p*MOS FinFETs without TSV integration near the channel as functions of dose up to 2 Mrad(SiO_2) and annealing at RT for 1 hour for the (a) "-1 V", (b) "0 V", and (c) "+1 V" bias conditions.

4.3.2 Impact of TSV via-last integration on 1/*f* noise

Because the physical thickness of the gate dielectric is ~2.5 nm with an EOT of 0.9 nm, defects in the gate oxide and/or near-gate STI introduced by TSV integration may also potentially cause differences in 1/*f* noise before and after irradiation [90], [119], [125], [130]. Therefore, it is useful to evaluate the impact of TSV via-last integration on low-frequency noise.

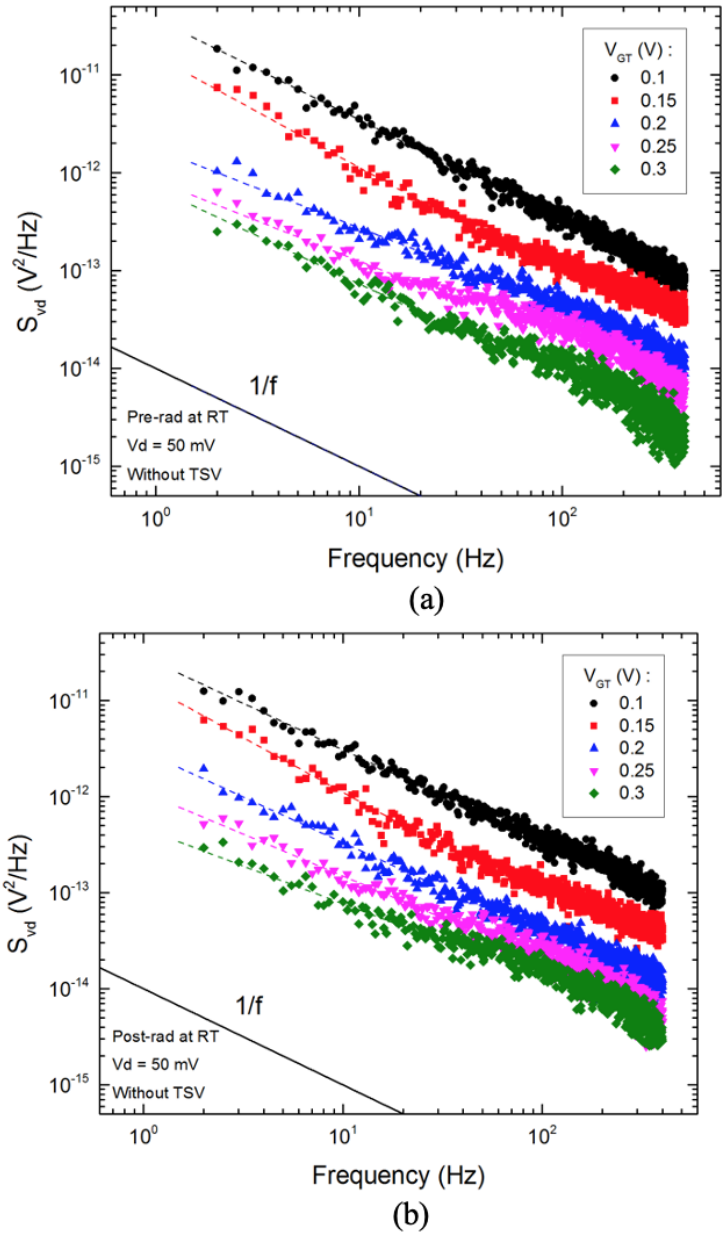


Figure 4.9: Excess voltage-noise power spectral density, S_{V_d}, vs. f at several values of $V_{gt} = V_{gs} - V_{th}$ for *n*MOS FinFETs without TSV integration (a) pre-irradiation, with slope $\alpha = 0.98 \pm 0.09$, and (b) post-irradiation, with slope $\alpha = 0.96 \pm 0.08$. Error bars denote the ranges of device responses.

Fig. 4.9 shows the excess voltage-noise power spectral density, S_{V_d}, for nMOS bulk FinFETs without TSV integration for values of V_{gt} = V_{gs} - V_{th} ranging from 0.1 V to 0.3 V, (a) before and (b) after 2 Mrad(SiO_2) irradiation in the worst case "+1 V" bias condition. The $1/f$ noise was measured at V_{ds} = 0.05 V with source and body contacts grounded. The spectra exhibit $1/f^{\alpha}$ frequency dependences for most frequencies and values of V_{gt}. Deviations from a simple $\sim 1/f$ frequency dependence result from border traps with non-uniform energy distributions [38], [39], [41], [57], [100]. The frequency dependence α is estimated for the data of Fig. 4.9 by fitting the noise spectra from 3 to 30 Hz; values of α typically change less than 5% after irradiation.

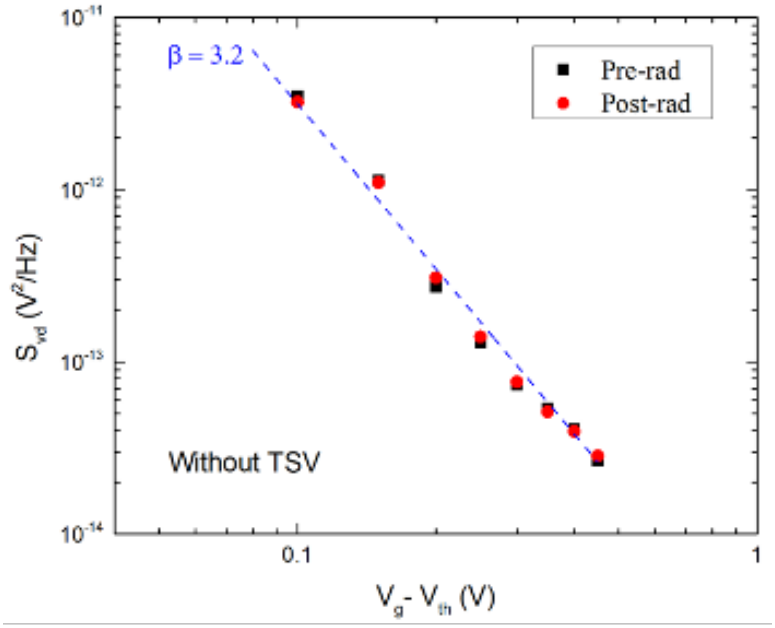


Figure 4.10: Noise magnitude at f = 10 Hz as function of V_{gt} for nMOS devices without TSV integration at pre-irradiation and post-irradiation. β = 3.2 $\pm$ 0.1. Error bars denote the ranges of device responses.

Fig. 4.10 shows noise magnitudes at f = 10 Hz for the data of Figs. 4.9(a) and 4.9(b) as functions of V_{gt}; values of S_{V_d} differ by less than 10% in each case. For noise due to number fluctuations with a uniform defect-energy distribution, the slope of the voltage dependence of the noise, β, is expected to be $\sim$ 2 [39], [41]. However, in Fig. 4.10, β = 3.2 $\pm$ 0.1, with a change less than 10% after irradiation. The significant deviation of β from 2 in Fig. 4.10 suggests that the border traps responsible for the noise in these devices have a non-uniform defect-energy distribution [39], [41], [42], [57]. That values of β are significantly greater than 2 is consistent with an effective border-trap energy distribution increases as it moves away from the conduction band edge [39], [42] [57].

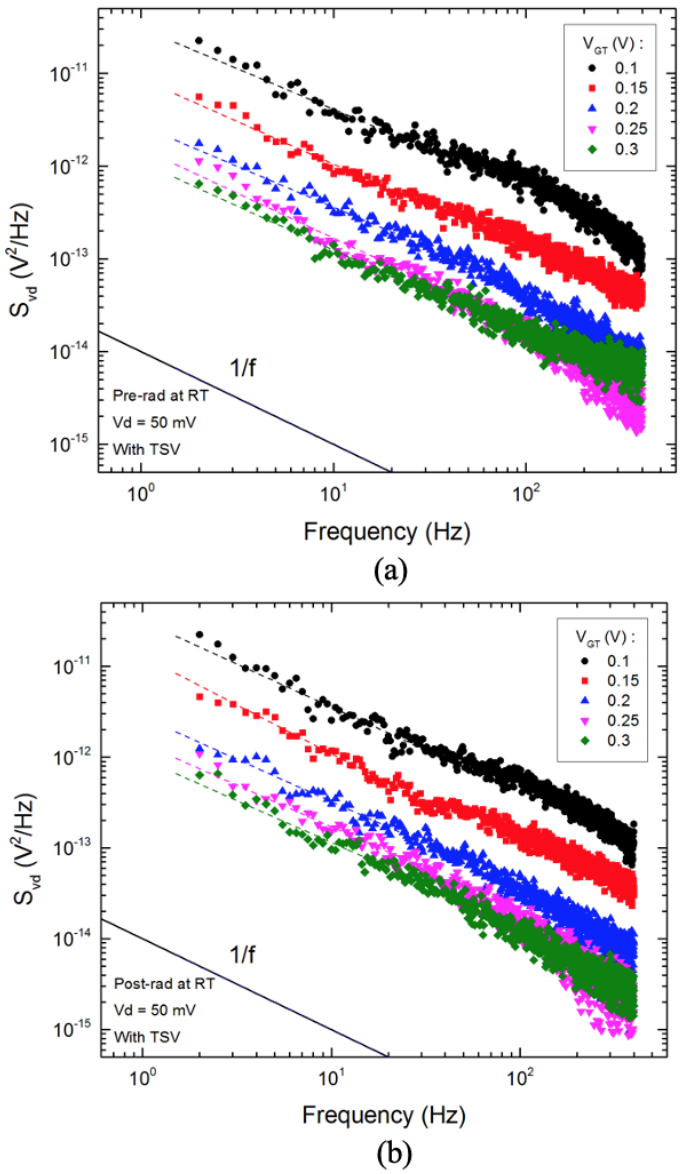


Figure 4.11: Excess voltage-noise power spectral density, S_{V_d}, vs. f at several values of $V_{gt} = V_{gs}$ - V_{th} for *n*MOS FinFETs with TSV integration (a) pre-irradiation, with slope $\alpha = 0.95 \pm 0.07$, and (b) post-irradiation, with slope $\alpha = 0.99 \pm 0.08$.

Noise magnitudes and voltage dependencies in these devices are similar to those observed in work on early generations of bulk and SOI FinFETs with high-K gate dielectrics reported by Gorchichko et al. [131].

Plots similar to those of Figs. 4.9 and 4.10 are shown for *n*MOS devices with TSV integration in Figs. 4. 11 and 4.12. Values of α vary by less than ~5% and values of S_{V_d} and β vary by less

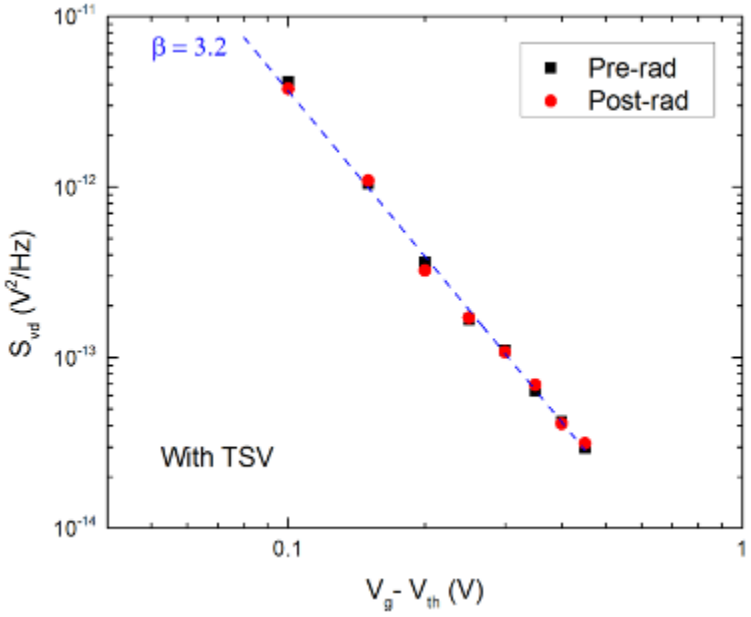


Figure 4.12: Noise magnitude at f = 10 Hz as function of V_{gt} for nMOS devices with TSV integration at pre-irradiation and post-irradiation. $\beta = 3.2 \pm 0.1$.

than ∼10% for irradiated and unirradiated devices. Hence, the results of Figs. 4.9-4.12 show that TSV via-last integration does not have a significant impact on the low-frequency noise, implying that the border-trap densities of the two types of devices are also similar [39], [90], [97], [132].

Plots similar to those of Figs. 4.9-4.12 are shown for pMOS devices with and without TSV integration in Figs. 4.13-4.16, irradiated to 2 Mrad(SiO_2) in the "+1 V" bias condition. Again, values of α vary by less than ∼5% and values of S_{V_d} and β vary by less than ∼10% for irradiated and unirradiated devices. Hence, similar to what is observed for nMOS devices, neither the radiation response nor the effective border-trap densities in pMOS devices is affected by TSV via-last integration. In contrast to the nMOS devices, values of β are less than 2 in Figs. 4.14 and 4.16. This is consistent with an effective border-trap energy distribution in these pMOS devices that increases as it moves away from the midgap [39], [42] [57].

We now apply a first-order number fluctuation model to provide estimates of the effective border-trap densities and energy distributions for the nMOS and pMOS devices of Figs. 4.9-4.16 [39], [41], [131], [132]:

$$D_t(E_f) = \frac{LW}{q^2 k_B T} \frac{C_{OX}^2 S_{V_d} f (V_g - V_{th})^2}{V_d^2} ln(\tau_1/\tau_0) \tag{4.2}$$

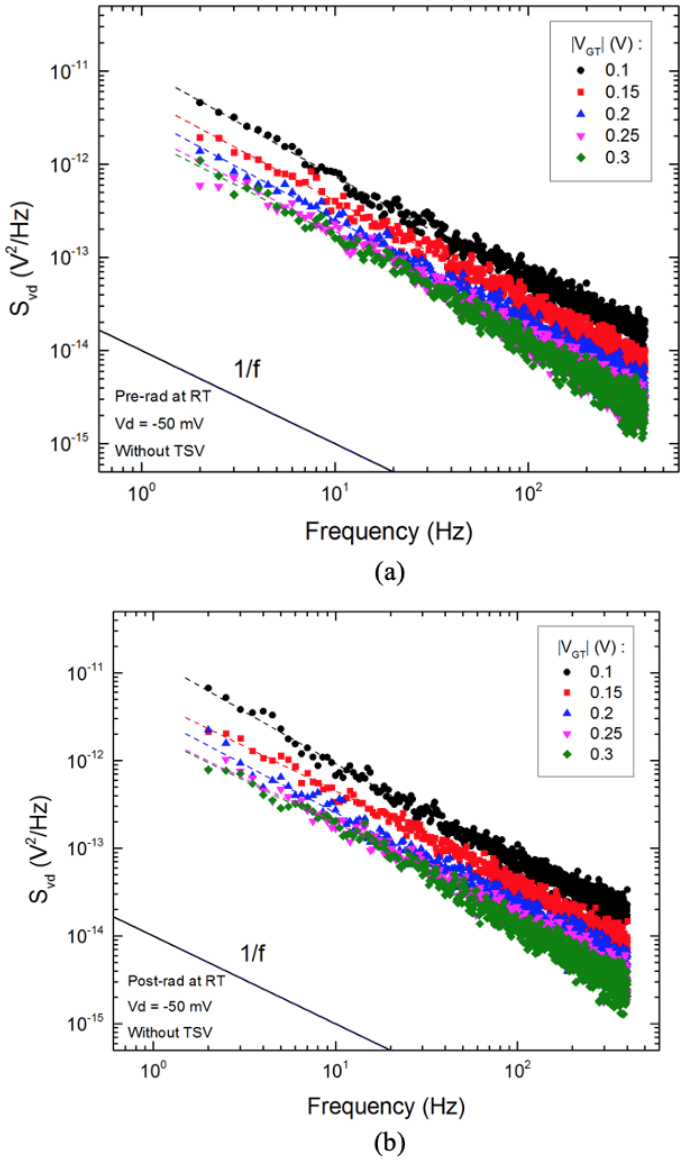
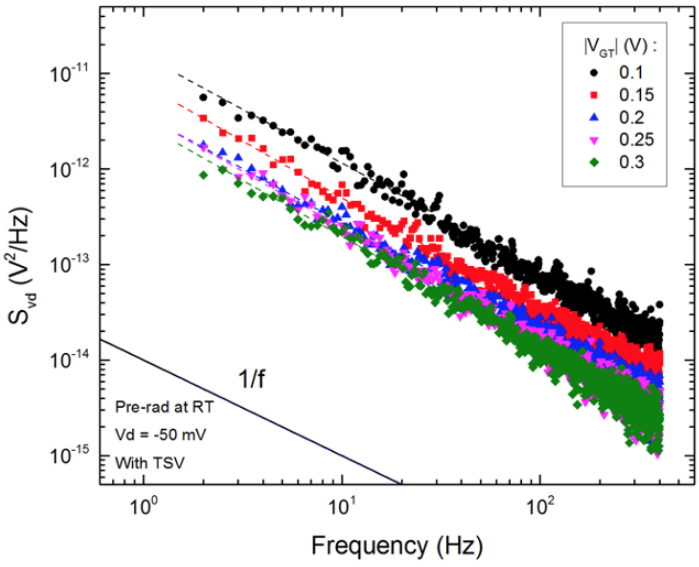
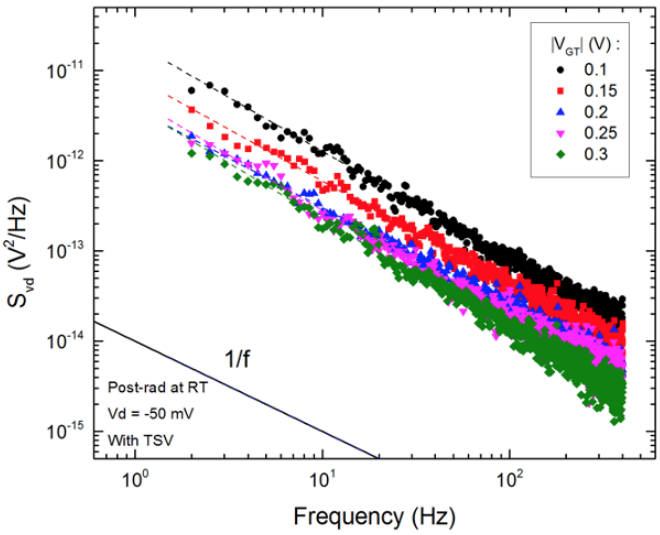


Figure 4.13: S_{V_d}, vs. f at several values of $|V_{gt}| = |V_{gs} - V_{th}|$ for pMOS FinFETs without TSV integration (a) pre-irradiation, with slope $\alpha = 1.10 \pm 0.05$, and (b) post-irradiation, with slope $\alpha = 1.10 \pm 0.09$. Error bars denote the ranges of device responses.

Here $D_t(E_f)$ is the number of traps per unit energy per unit area available to contribute to the noise process at a given gate bias and Fermi level, L and W are the transistor channel length and effective width, q is the magnitude of the electron charge, k_B is the Boltzmann constant, T is the absolute temperature, C_{OX} is the gate-oxide capacitance per unit area, S_{V_d} is the excess drain-voltage noise power spectral density, corrected for background noise, f is the frequency, V_{th}, V_g, V_d are the threshold, gate, drain voltages, and τ_0 and τ_1 are the minimum and maximum tunneling times,



(a)



(b)

Figure 4.14: S_{V_d}, vs. f at several values of $|V_{gt}| = |V_{gs} - V_{th}|$ for pMOS FinFETs with TSV integration (a) pre-irradiation, with slope $\alpha = 1.17 \pm 0.05$, and (b) post-irradiation, with slope $\alpha = 1.16 \pm 0.07$. Error bars denote the ranges of device responses.

respectively [42]. For tri-gate FinFETs with 220 fins, $W \approx 220(FW + 2FH)$, where FW is the fin width and FH is the fin height [41], [120], [122–124], [131]. We estimate the ratio $\tau_1/\tau_0 \approx 10^{12}$ to be consistent with previous work [39], [90], [97], [132], [133].

Fig. 4.17 shows $D_t(E_f)$ at f = 10 Hz as a function of V_{gt} for devices (a) without and (b) with TSV integration. Consistent with trends in the voltage dependence of the noise of nMOS

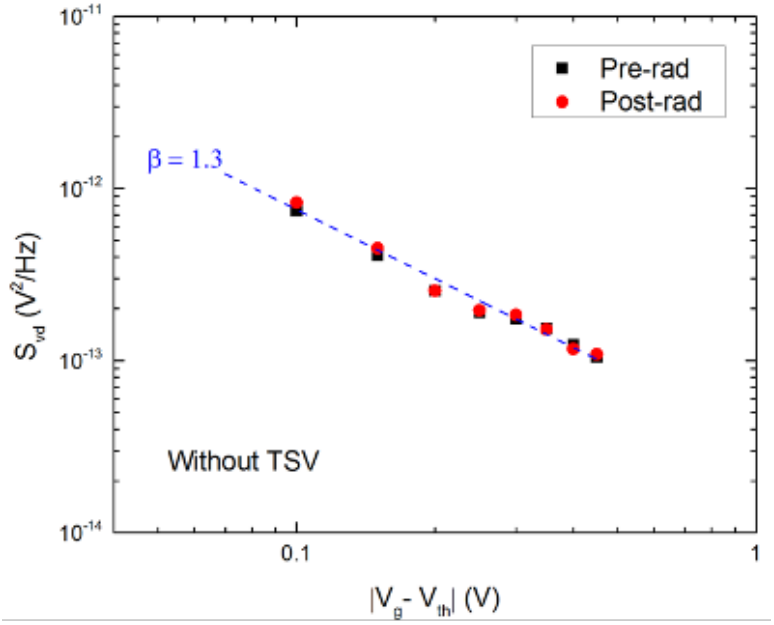


Figure 4.15: Noise magnitude at f = 10 Hz as function of $|V_{gt}|$ for pMOS devices with TSV integration at pre-irradiation and post-irradiation. $\beta = 1.4 \pm 0.1$. Error bars denote the ranges of device responses.

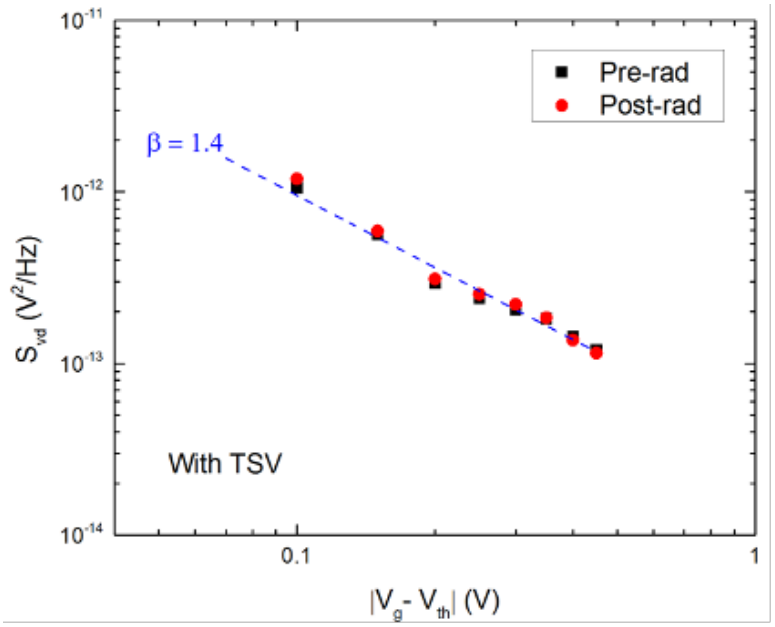


Figure 4.16: Noise magnitude at f = 10 Hz as function of $|V_{gt}|$ for pMOS devices without TSV integration at pre-irradiation and post-irradiation. $\beta = 1.3 \pm 0.1$. Error bars denote the ranges of device responses.

devices in Figs. 4.10 and 4.12, the effective density of electron traps increases strongly as the applied voltage is reduced in magnitude, corresponding to defect energies closer to midgap surface

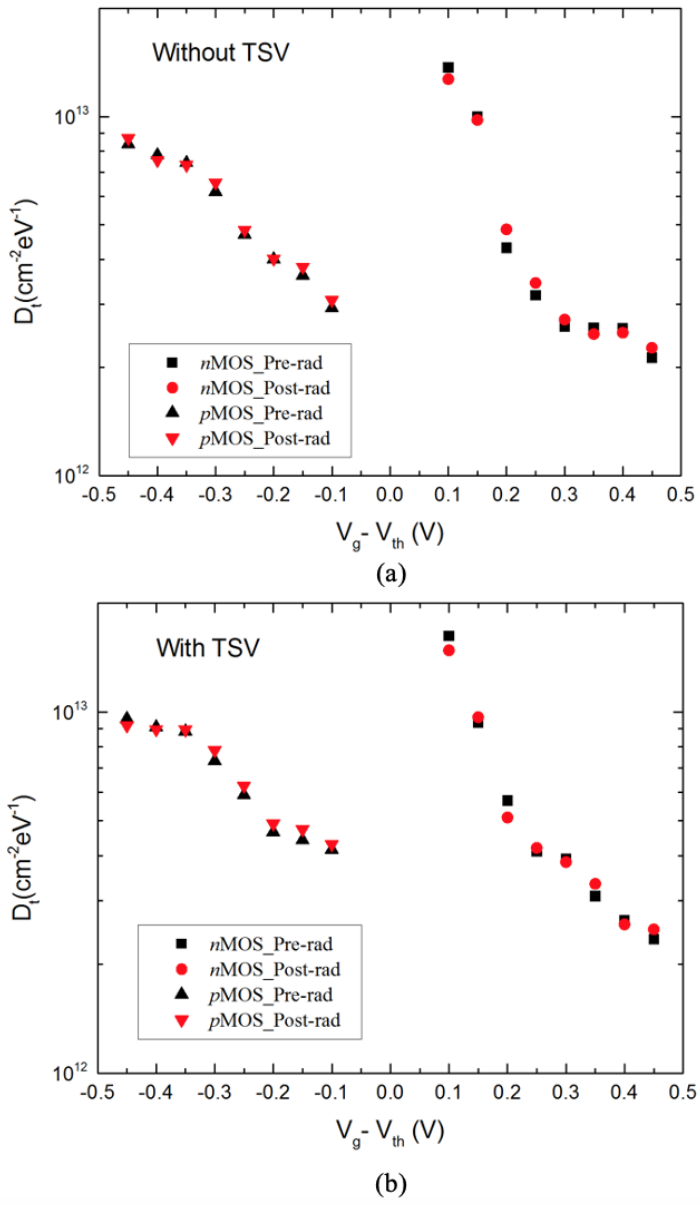


Figure 4.17: Effective border-trap energy distribution at f = 10 Hz as a function of V_{gt} for nMOS and pMOS devices (a) without TSV integration and (b) with TSV integration, before and after 2 Mrad(SiO_2) total dose irradiation.

potential [39], [42] [57]. Similarly consistent with trends in the voltage dependence of the noise of pMOS devices in Figs. 4.14 and 4.16, the effective density of hole traps increases strongly as the applied voltage is increased in magnitude, corresponding to defect energies closer to the valence band edge [39], [42] [57]. For nMOS devices, effective border-trap densities range from a high of $\sim$1.3 $\times 10^{13}$ $cm^{-2}eV^{-1}$ when V_g - V_{th} = 0.1 V to a low of $\sim$2 $\times 10^{12}$ $cm^{-2}eV^{-1}$ when

V_g - V_{th} = 0.45 V. For pMOS devices, effective border-trap densities range from a high of ∼9 $\times 10^{12}$ cm^{-2}eV^{-1} when V_g - V_{th} = 0.45 V to a low of ∼3 $\times 10^{12}$ cm^{-2}eV^{-1} when V_g - V_{th} = 0.1 V. These trap densities are typical of those observed in devices with high-K dielectrics in other studies [39], [41], [100], [131].

Because the near-interfacial SiO_2 layer in the devices of this study is only ∼0.5 nm thick, it is unlikely that the majority of the electron and hole traps responsible for the low frequency noise are located in the SiO_2 layer. Charge exchange with traps in SiO_2 so close to the interface occurs far too rapidly to con-tribute to noise in the frequency range employed in this study [39], [41], [90], [132]. Hence, it is likely that the defects re-sponsible for the observed noise in the devices are located within the bulk HfO_2 or at the SiO_2/HfO_2 dielectric/dielectric interface [39], [131], [134–138]. Oxygen vacancies in HfO_2 are known to have both electron and hole trap levels that may well be responsible for the observed noise in these devices, and are often complexed with hydrogen [39], [41], [134–140].

4.4 Summary and Discussion

The total-ionizing-dose response is reported for advanced FinFETs with and without TSV via-last integration near the channel. The worst-case TID response in nMOS devices is the "+1 V" bias condition, for which the highest electric field, highest charge yield, and thus the largest hole trapping is observed in the STI. These charged traps in the STI degrade the subthreshold swing and I_{on}/I_{off} ratio. Off-state currents increase modestly with increasing TID. The shifts of the threshold voltage in both devices are small because of the relatively few charged traps in the thin gate oxide and the excellent electrostatic gate control of the FinFET structure. No significant changes in low-frequency noise magnitude are observed during device irradiation, consistent with the small V_{th} shifts.

The effective border-trap densities responsible for the noise in the nMOS devices increase as the surface potential moves away from the conduction band edge, consistent with the response of older-generation FinFETs with SiO_2/HfO_2-based FinFETs. This similarity suggests that the $1/f$ noise in nMOS devices with SiO_2/HfO_2-based gate dielectrics is due most likely to electron traps in the bulk HfO_2 or at the SiO_2/HfO_2 interface. The effective border-trap densities responsible for the noise in the pMOS devices decrease as the surface potential moves away from the valence band edge. These defects also have been identified in previous studies as oxygen vacancies, and are known to be often

complexed with hydrogen. Reducing the densities of these near-interfacial defects will therefore improve the performance, reliability, and radiation response of integrated circuits built in this and other technologies with HfO_2-based gate stacks.

Finally, TSV integration does not significantly affect threshold shifts, maximum transconductance variation, degradation of subthreshold swing, low-frequency noise, or I_{on}/I_{off} ratio in both *p*MOS and *n*MOS devices, indicating that trapping properties of the gate oxide and STI are relatively unaffected by TSV integration. If single-event effects are similarly unaffected (or perhaps improved [141]), technologies that in-corporate TSVs will be highly promising for use in space and other high-radiation environments due to their enhanced chip functionality without degradation in radiation hardness.

CHAPTER 5

Low-Frequency Noise and Border Traps in Irradiated nMOS and pMOS Bulk Si FinFETs with SiO_2/HfO_2 Gate Dielectrics

This chapter is adapted from "Low-Frequency Noise and Border Traps in Irradiated nMOS and pMOS Bulk Si FinFETs with SiO_2/HfO_2 Gate Dielectrics" submitted to 2022 IEEE Nuclear and Space Radiation Effects Conference, and has been reproduced with the permission of the publisher and my co-authors Xuyi Luo, Rony W Mohammed, Mariia Gorchichko, Gaspard Hiblot, Stefaan Van Huylenbroeck, Anne Jourdain, Michael L Alles, Robert A Reed, En Xia Zhang, Daniel M Fleetwood, Ronald D Schrimpf.

- K. Li *et al.*, "Low-Frequency Noise and Border Traps in Irradiated nMOS and pMOS Bulk Si FinFETs with SiO_2/HfO_2 Gate Dielectrics," *submitted to 2022 IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, July, 2022.

5.1 Introduction

As electronic devices and integrated circuits (ICs) have evolved, defect generation and charge trapping in dielectrics and at channel-dielectric interfaces are among the most important concerns that limit their performance, reliability, and radiation response [8], [34], [35] [142]. The most important cause of low-frequency noise in electronic devices is the thermally activated interaction of carriers with defects in dielectrics; low-frequency noise measurements can provide significant insights into defect densities, effective energy distributions, and microstructures in semiconductor devices [18], [37–39], [99], [100]. Measurements of the frequency and temperature dependence of $1/f$ noise enable estimates of effective defect energy distributions via the theory of Dutta and Horn [38], [39]. Estimates of effective defect densities and energy dependence may also be derived from the number fluctuation model of low-frequency noise of MOS devices, within the limited range of surface potentials accessible at a fixed temperature [42–44], [57].

In previous work, effective border-trap densities were evaluated for as-processed and irradiated bulk Si *n*MOS and *p*MOS FinFETs built in the same process technology via gate-dependence measurements of low-frequency noise per-formed (only) at room temperature [17]. For *n*MOS devices,

the effective density of border traps was found to increase toward midgap. For *p*MOS devices, effective border-trap densities were found to increase toward the valence band. Here we perform a detailed comparison of the low-frequency noise of these devices at temperatures from 80 K to 320 K. The gate-voltage dependence of the $1/f$ noise is investigated in both device types at several temperatures after irradiation and annealing, with results similar to [17] in all cases. The *n*MOS noise generally decreases with increasing temperature, with three prominent individual defect-related peaks in plots of noise magnitude vs. temperature identified at $\sim$ 95 K, 155 K, and 215 K. In strong contrast, the *p*MOS noise magnitude generally increases with increasing temperature with no prominent individual defect-related peaks in noise magnitude vs. temperature. The noise and effective energy distributions are only affected modestly when devices are subjected to bias-stress at $80^{\circ}C$ (353 K) and/or irradiated up to 2 Mrad(SiO_2). The applicability of Dutta-Horn analysis is demonstrated in all cases, demonstrating that the noise is caused by thermally-activated processes with energy distributions that vary slowly relative to kT, where k is Boltzmann's constant and T is the absolute temperature. Trends in energy distributions inferred from Dutta-Horn analysis of the temperature dependence of the noise and from gate-voltage measurements of noise are qualitatively consistent for both types of FinFETs.

5.2 Experimental Details

5.2.1 Device structure

Bulk Si FinFETs were fabricated by imec with 220 fins, fin height = 26 nm, fin width = 7 nm, and fin pitch = 45 nm [16]. The gate length is 1 μm and the gate dielectric consists of a 0.5 nm SiO_x interfacial layer and 2 nm HfO_2 layer, which provides an EOT of 0.9 nm. The gate metal is tungsten with a thin layer of work-function metal between the W layer and the gate oxide. Fig. 1 shows a side-view schematic diagram of an individual fin [17], [16].

5.2.2 Experimental setup

Drain current vs. gate voltage ($I_d - V_g$) characteristics were measured with an Agilent 4156A/B semiconductor parameter analyzer at V_{ds} = $\pm$ 0.05 V for *n*MOS/*p*MOS devices. The threshold voltage V_{th} is extracted by calculating the x-intercept of the linear extrapolation of the $I_d - V_g$ curve

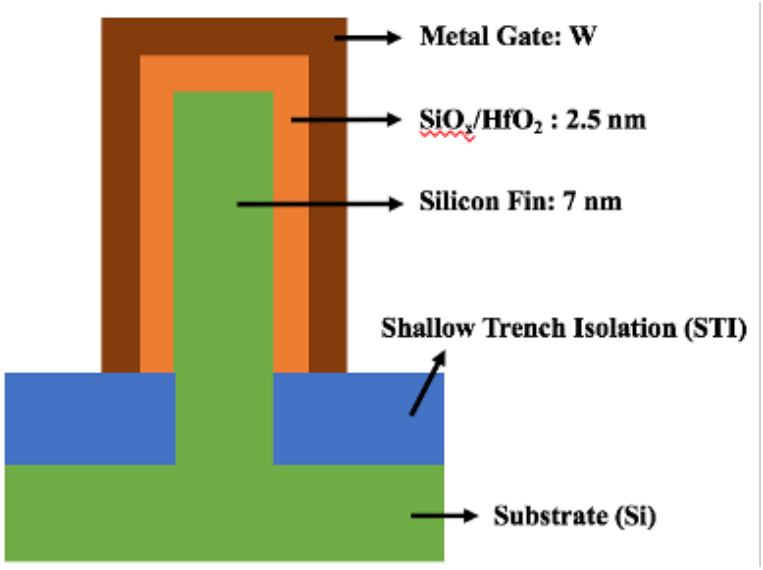


Figure 5.1: Side-view schematic diagram of an individual fin [17].

at its maximum first derivative and subtracting $V_ds/2$ [119]. The low-frequency noise power spectral density S_{vd} was measured with correction for background noise; V_d was at 0.05 V for *n*MOSFETs and 0.05 V for *p*MOSFETs, with source, body, and substrate grounded [39]. Temperatures ranged from 80 to 320 K and frequencies ranged from 2 Hz to 400 Hz. The gate voltage varied from 0.1 V to 0.6 V above V_{th} for *n*MOS devices and 0.1 V to 0.5 V below V_{th} for *p*MOS devices. After initial noise measurements were performed on as-processed devices, bias-temperature stresses were performed at $80°C$ (353 K) at $V_g = \pm$ 0.8 V for each device to check for stability [100], [143]. The electrical connection for low-frequency noise measurement is illustrated in Fig. 5.2 [18].

TID irradiation was performed at room temperature at Vanderbilt University using an ARACOR Model 4100 X-ray irradiator with peak energy deposition at 10 keV [35] at a dose rate of 30.3 krad(SiO_2)/min. All devices were irradiated in steps to a total dose of 2 Mrad(SiO_2), followed by annealing for 60 min at room temperature. Ionizing dose and dose rate are referred to equilibrium dose in SiO_2 for consistency in calibration and to facilitate comparison with other work [35]. Devices are biased under the worst-case "+1 V" condition (V_{gs} = +1 V, V_{ds} = 0 V) during irradiation and annealing [17], with source, drain, and body contacts grounded. At least three devices were measured for each device type, with typical device-to-device variations in response less than 10%.

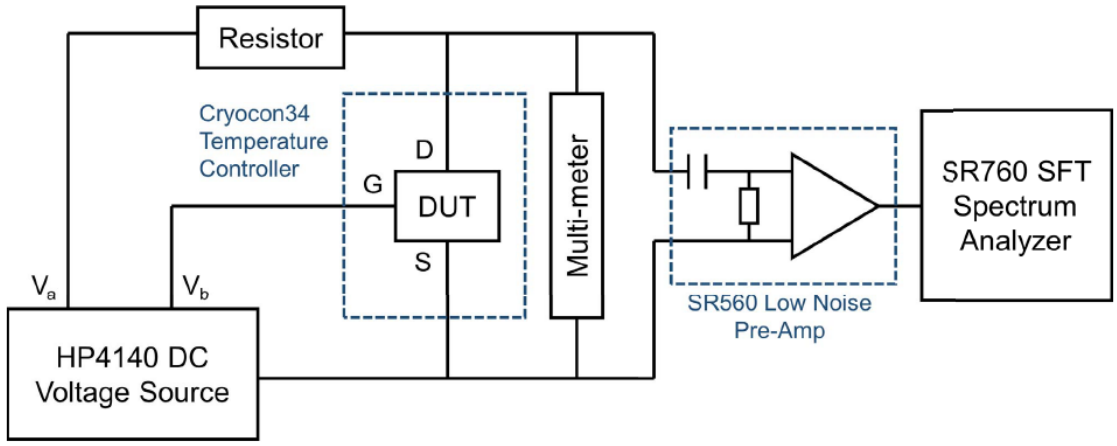


Figure 5.2: Low-frequency noise measuring system (after [18]).

5.3 Experimental Results and Discussion

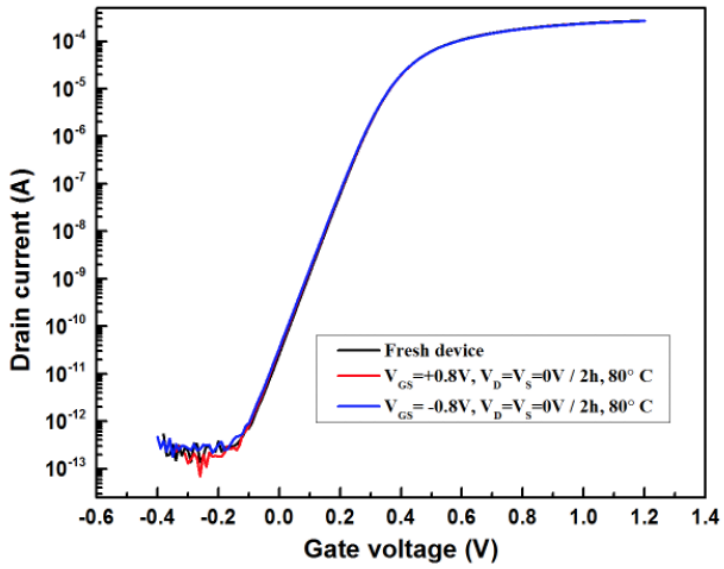
5.3.1 1/f noise and border traps in irradiated nMOS FinFETs

Fig. 5.3 shows $I_d - V_g$ characteristics for nMOS devices that were (a) biased at V_{gs} = $\pm$0.8 V for 2 h at 80°C and (b) irradiated in steps up to 2 Mrad(SiO_2) and annealed at room temperature for 1 h. In Fig. 5.3(a) V_{th} shifts less than 3 mV and the on-state current changes less than 5% during bias stress, indicating high stability. Values of V_{th} shift less than 0.02 V and gm changes less than 1% [17]. In Fig. 5.3(b), off-state leakage currents increase with dose due to radiation-induced trapped charge in the shallow trench isolation (STI) of the sub-fin region (Fig. 5.1). Trapped positive charges can invert the p-type silicon near the STI edge and create a parasitic leakage path from drain to source [121], [122], [124].

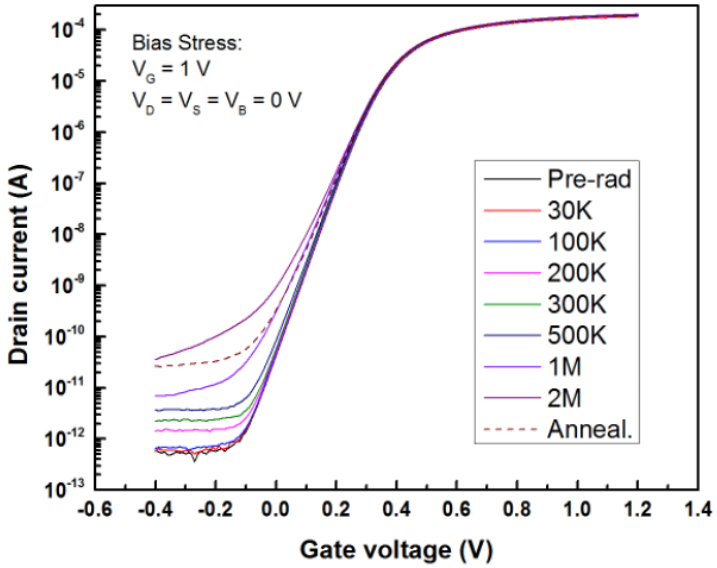
For semiconductor devices, low-frequency noise is primarily caused by random thermally activated processes having a broad distribution of energies relative to kT. Dutta and Horn showed that the frequency and temperature dependences of 1/f noise that results from such processes are correlated via:

$$\alpha(\omega,T) = 1 - \frac{1}{ln(\omega\tau_0)}\left(\frac{\partial S_V(T)}{\partial lnT} - 1\right) \tag{5.1}$$

Here S_V is the excess voltage–noise power spectral density after the thermal noise is subtracted, $\alpha = -\partial S_V/\partial f$, $\tau_0 = 1/f_0$ is the characteristic time of the process leading to the noise, and $\omega = 2\pi f$.



(a)



(b)

Figure 5.3: $I_d - V_g$ transfer characteristics for nMOS FinFETs at V_{ds} = 0.05 V (a) for unirradiated devices, before and after devices were stressed at V_{gs} = $\pm$0.8 V for 2 h at 80°C, and then (b) as functions of dose up to 2 Mrad(SiO_2) and annealing at room temperature (RT) for 1 hour for the "+1 V" bias conditions.

A value of $\tau_0 = 1.81 \times 10^{-15}$ s is chosen here to be consistent with previous MOS studies [18], [39], [100], [144], [145]. For noise described by Eq. (5.1), the defect-energy distribution $D(E_0)$ can be inferred from measurement of S_V by the relation:

$$D(E_0) \propto 1 - \frac{\omega}{kT} S_V(\omega, T) \tag{5.2}$$

where the defect energy is related to temperature and frequency by the expression [18], [38], [39]:

$$E_0 \approx -kT\,ln(\omega\tau_0) \tag{5.3}$$

If the noise results from thermally activated processes involving two energy levels, E_0 is the energy barrier that the system must overcome to move from one configurational state to another with a different charge state and/or different carrier scattering probability [13], [38], [39], as shown in Fig. 5.4.

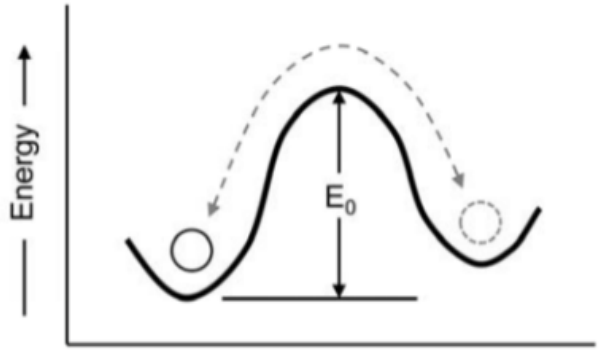


Figure 5.4: Schematic illustration of a system with two configurations with different energy levels, charge states, and/or carrier scattering rates. E_0 is the energy barrier for the system to move reversibly from one configurational state to another. (After [13]).

Fig. 5.5 shows the evolution of the normalized low-frequency noise $S_{Vd}f/T$ (left y-axis) and corresponding effective border-trap energy distribution $D_t(E_f)$ (right y-axis) for nMOS devices before and after the stability tests and irradiation/annealing tests of Fig. 5.3; here f = 10 Hz, $V_g - V_{th} \equiv V_{gt}$ = 0.3 V, and V_d = 0.05 V. The noise magnitude generally decreases with increasing temperature in all cases. Minimal changes are observed in $S_{Vd}f/T$ at a given value of T with bias-stress and/or irradiation to 2 Mrad(SiO_2), affirming the excellent stability and radiation tolerance of these devices. The effective border-trap density and energy distribution $D_t(E_f)$ is estimated via a first-order number fluctuation model [39], [41], [97], [131]:

$$D_t(E_f) = \frac{LW}{q^2 k_B T} \frac{C_{OX}^2 S_{V_d} f (V_g - V_{th})^2}{V_d^2} ln(\tau_1/\tau_0) \tag{5.4}$$

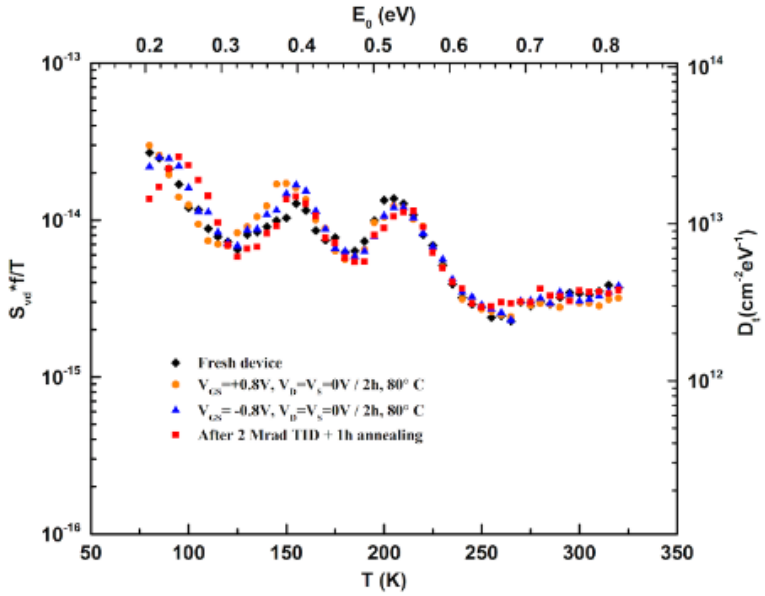


Figure 5.5: Normalized $1/f$ noise (left hand scale) and effective border-trap energy distribution (right hand scale) as a function of temperature from 80 K to 320 K at f = 10 Hz and $V_g - V_{th}$ = 0.3 V and V_d = 0.05 V for the *n*MOS bulk Si FinFETs of Fig. 5.3 before and after bias-temperature stress and subsequent TID irradiation and annealing. Three devices were measured with similar responses; the results of a typical device are shown here.

Here L and W are the transistor channel length and effective width. For these tri-gate FinFETs with 220 fins, $W \approx 220(FW + 2FH)$, where FW is the fin width and FH is the fin height [41], [120], [122–124], [131]. τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [11]. We estimate the ratio $\tau_1/\tau_0 \approx 10^{12}$ to be consistent with previous work [17], [39], [90], [97], [132], [133]. Effective border-trap densities for *n*MOS devices range from $\sim 2 \times 10^{12}$ cm^{-2}eV^{-1} to $\sim 3 \times 10^{13}$ cm^{-2}eV^{-1}.

Fig. 5.6 evaluates the degree to which the temperature- and frequency-dependences of the noise are correlated via Eq. (5.1), which provides a test of the ability of the Dutta-Horn model to describe the noise kinetics of these devices [38], [39], [100], [146], [147]. The consistency of the trends in experimental and predicted values of α justify the use of Eq. (5.3) to estimate the effective border-trap densities in Fig. 5.5 (upper x-axis) [38], [39].

Three peaks in noise magnitude vs. temperature curves are observed in Fig. 5.5 at $\sim$ 95 K (0.25 eV), $\sim$ 155 K (0.40 eV), and $\sim$ 215 K (0.55 eV), indicating three prominent defects. Fig. 5.7 shows the frequency dependence of S_{Vd} for the irradiated and annealed devices at room temperature (295

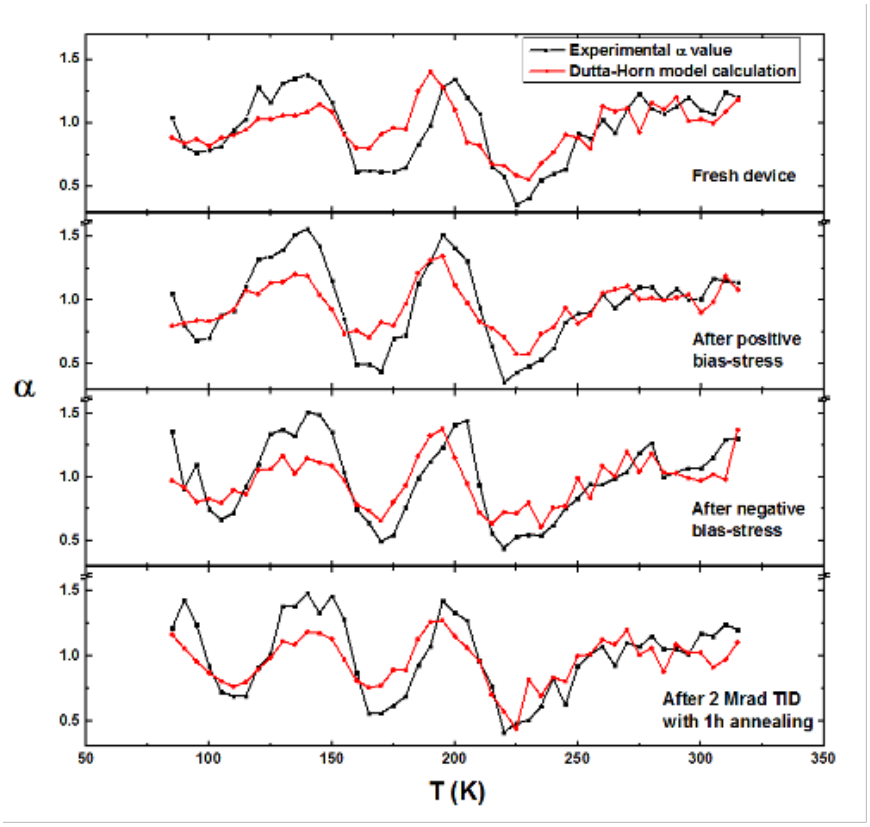


Figure 5.6: Comparison of experimental values of the frequency dependence of the noise, $\alpha = -\partial S_{Vd}/\partial f$, estimated in the frequency range 5-20 Hz, for temperatures from 80 K to 320 K. Predicted values are extracted from the data of Fig. 5.5 using Eq. (5.1) of the text.

K) and the temperatures of prominent peaks and troughs in Fig. 5.5. At 125 K, 185 K, and 295 K (troughs in the distributions), S_{Vd} exhibits a $\sim 1/f$ power law, while at 95 K, 155 K, and 215 K (peaks in the distributions), deviations from the power law dependence are consistent with a single, dominant defect that is active at $\sim$ 10 Hz in each case [39]. The 0.4 eV defect in SiO_2 has been identified with hydrogen shuttling near the interface [100], [148]; active defects at $\sim$ 0.25 eV and $\sim$ 0.55 eV are most likely O vacancies in the HfO_2 [39], [41], [99], [149].

Gate-voltage dependence measurements of low-frequency noise can be used to obtain the energy and/or space distribution of the effective border trap densities [17], [18], [39], [42], [150]. The excess drain-voltage noise power spectral density S_{Vd} can be expressed via [7-9]:

$$S_{Vd}(f, V_{ds}, V_{gs}) = K V_{ds}^2 f^{-\alpha} (V_{gs} - V_{th})^{-\beta} \tag{5.5}$$

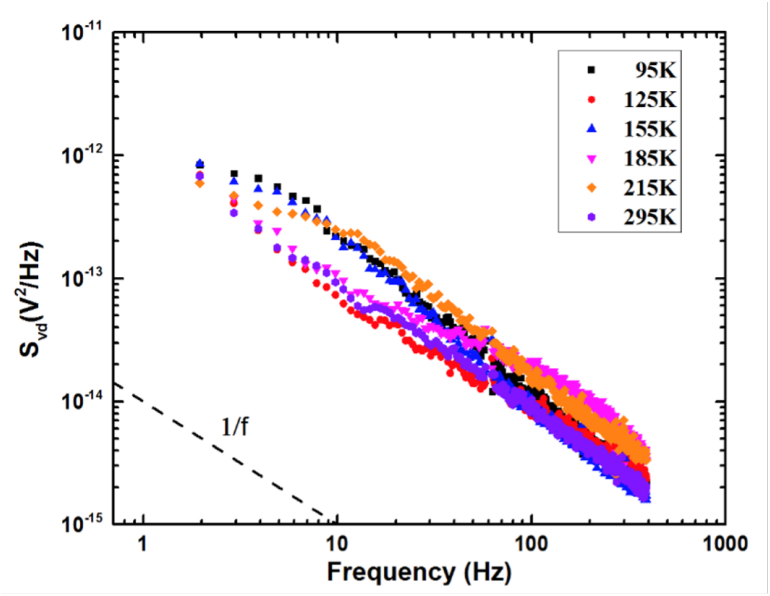


Figure 5.7: Frequency dependence of S_{Vd} at temperatures corresponding to the peaks and troughs of the noise magnitude vs. temperature plots in Fig. 5.5 for devices that completed the full bias-stress and irradiation/annealing sequence.

Here K is the normalized noise magnitude. For noise due to number fluctuations with a uniform defect-energy distribution, the slope of the voltage dependence of the noise, β, is expected to be $\sim$ 2 [18], [39]. The values of β are larger than 2 when the defect energy distribution increases toward midgap. Values of β are less than 2 if the defect energy distribution increases toward the conduction band for *n*MOS devices or the valence band for *p*MOS devices [17], [18], [39], [42], [99].

Fig. 5.8 shows noise magnitudes at f = 10 Hz as a function of $V_{gt} = V_{gs}$-V_{th} from 0.1 V to 0.6 V at room temperature and the three temperatures at which peaks occur for the irradiated and annealed devices of Fig. 5.5: 95 K, 155 K, and 215 K. In all four cases, the values of β for the full range of V_{gt} fall within a band of $\beta = 3.3 \pm 0.5$. That these values are significantly greater than 2 confirms that, over the full range of temperatures investigated, the effective border-trap energy distribution increases as energies approach midgap and decreases as the energy moves away from the conduction band [39], [42], [57]. This is consistent with the overall decrease of the noise magnitude with increasing temperature in Fig. 5.5, since increasing temperature probes defects that are closer in energy to the corresponding band (conduction band for *n*MOS devices and valence band for *p*MOS devices) [57].

As shown by the dashed lines in Fig. 5.8, values of β are close to 2 at higher and lower voltages,

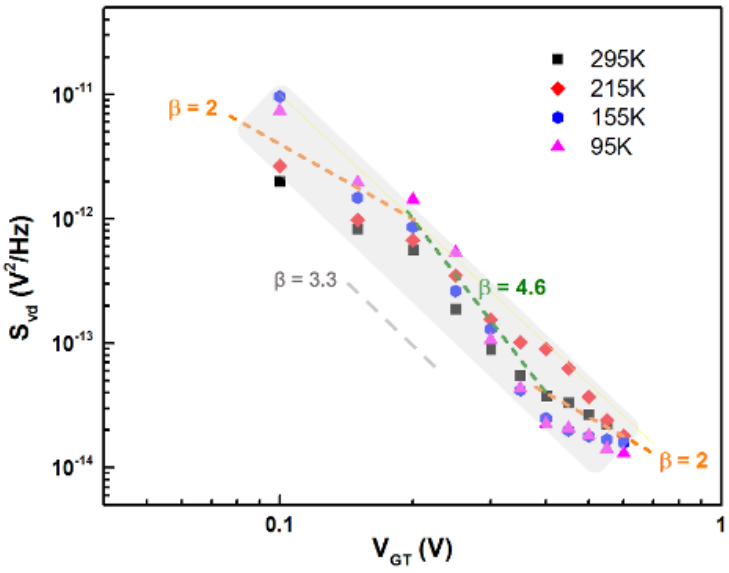


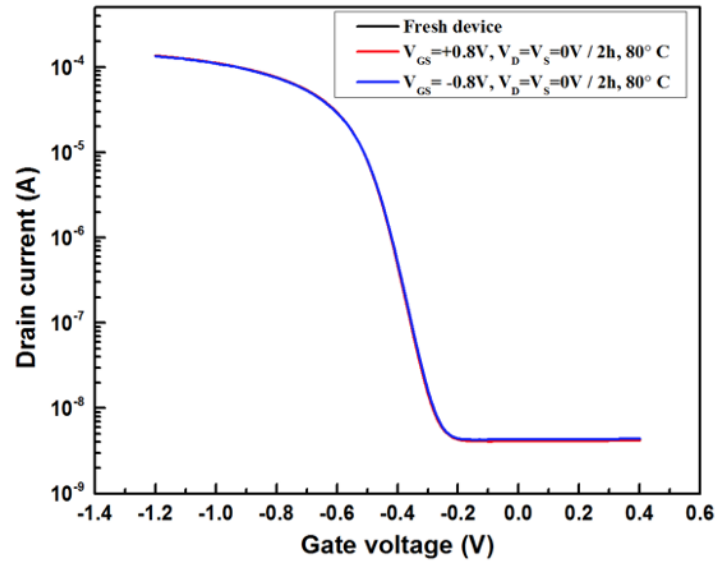
Figure 5.8: Noise magnitude at f = 10 Hz as a function of Vgt from 0.1 V to 0.6 V for the devices of Fig. 5.7.

with higher values of β at mid-range voltages. Scofield et al. have shown that variations in voltage dependence in noise magnitude in large planar MOS devices with thick SiO_2 gate dielectrics can be attributed to prominent individual defect-related peaks that are also evident in plots of noise vs. temperature [57], as seen in Figs. 5.5 and 5.8.

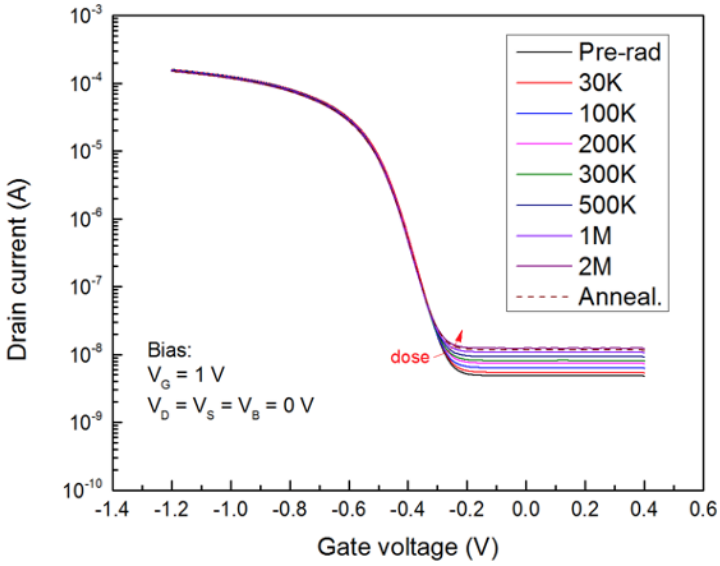
5.3.2 1/f noise and border traps in irradiated pMOS FinFETs

Similar to nMOS FinFETs, pMOS devices also exhibit excellent stability after being biased at V_{gs} = $\pm$0.8 V for 2 h at 80°C prior to TID irradiation, as shown in Fig. 5.9(a). V_{th} shifts less than 2 mV, and the on-state current changes less than 5%. Fig. 5.9(b) shows $I_d - V_g$ curves at V_{ds} = -0.05 V during irradiation and annealing at the "+1 V" (V_{gs} = +1 V, V_{ds} = 0 V) bias condition. Changes in threshold voltage of less than 15 mV and maximum transconductance of less than 1% are observed in these pMOS devices, similar to the responses of nMOS devices to bias-temperature stress and TID exposure in Fig. 5.3.

Fig. 5.10 shows the normalized low-frequency noise and corresponding effective border-trap energy distribution $D_t(E_f)$ as a function of the temperature at f = 10 Hz and V_{gs} = 0.3 V for pMOS devices before and after bias-temperature stress and 2 Mrad(SiO_2) TID irradiation and 1 h annealing. Minimal changes in noise are observed at a given value of T with bias-stress or irradiation. The



(a)



(b)

Figure 5.9: $I_d - V_g$ transfer characteristics for *p*MOS FinFETs at V_{ds} = -0.05 V (a) for unirradiated devices, before and after devices were stressed at V_{gs} = $\pm$0.8 V for 2 h at 80°C, and then (b) as functions of dose up to 2 Mrad(SiO_2) and annealing at room temperature (RT) for 1 hour for the "+1 V" bias conditions.

inset shows agreement between the measured frequency dependences of the noise and calculated values based on Dutta-Horn model. Unlike the *n*MOS devices, there are no obvious individual defect-related peaks in the *p*MOS devices. This is due to the differences in the energy dependences of near-interfacial electron and hole traps in SiO_2/HfO_2 gate dielectrics. The effective border-trap

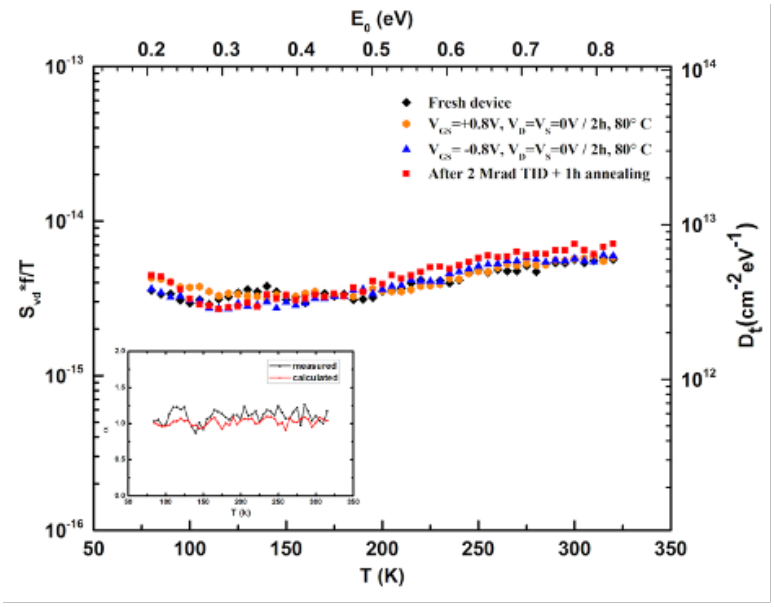


Figure 5.10: Normalized $1/f$ noise (left hand scale) and effective border-trap energy distribution (right hand scale) as a function of temperature from 80 K to 320 K at f = 10 Hz and $V_g - V_{th}$ = -0.3 V and V_d = -0.05 V for the pMOS bulk Si FinFETs of Fig. 5.9 before and after bias-temperature stress and subsequent TID irradiation and annealing. Inset: experimental values of α compared with the values derived from Dutta-Horn model. Three devices were measured with similar responses; the results of a typical device are shown here.

densities for pMOS devices range from $\sim 3 \times 10^{12}$ cm^{-2}eV^{-1} to $\sim 9 \times 10^{12}$ cm^{-2}eV^{-1}, consistent with previous work [17].

Fig. 5.11 shows the noise magnitude at f = 10 Hz as a function of V_{gt} from 0.1 V to 0.5 V at the same four temperatures as in Fig. 5.8 for the irradiated and annealed pMOS devices of Fig. 5.10. In all cases, hole trap distributions increase toward the valence band edge [57], [100], in contrast to electron trap distributions, which increase strongly toward midgap in Fig. 5.8 [17], [100]. This distribution is similar to that observed in NBTI studies of hole trapping in the near-interfacial SiO_2, in which a broad, relatively uniform distribution is observed of O vacancies complexed with hydrogen near the Si/SiO_2 interface and extending into the HfO_2 [41], [139], [140], [151]. Note that, under the conditions of the measurements shown, the normalized noise magnitudes are similar near room temperature for the nMOS devices in Fig. 5.5 and the pMOS devices in Fig. 5.10. In this region, prominent individual defects do not contribute as significantly to the nMOS noise as at lower temperatures.

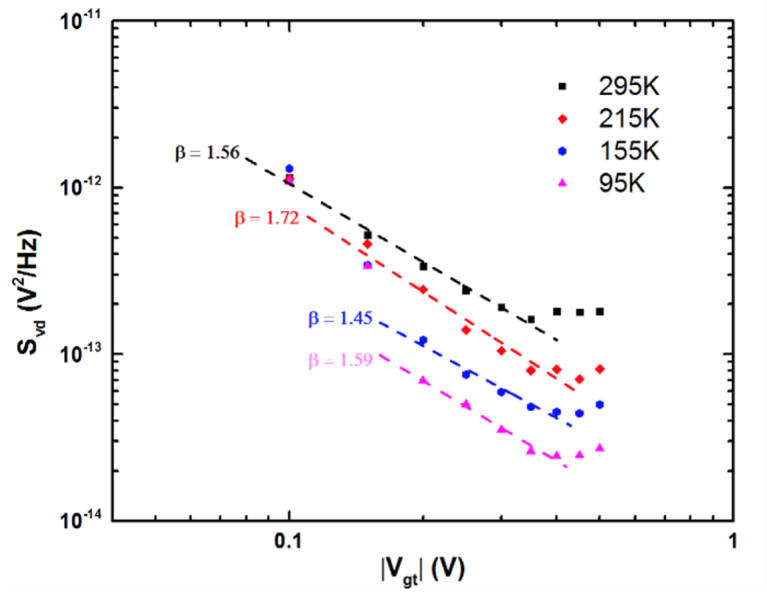


Figure 5.11: The noise magnitude at f = 10 Hz as function of V_{gt} from -0.1 V to -0.5 V at the same four temperatures as in Fig. 5.8 for the irradiated and annealed *p*MOS devices of Fig. 5.10.

5.4 Summary and Conclusions

The temperature and gate-voltage dependences of the $1/f$ noise are investigated for complementary bulk Si FinFETs. Noise magnitudes and frequency dependence are not significantly affected by bias-temperature stress or TID exposure to 2 Mrad(SiO_2), emphasizing the stability and radiation tolerance of these devices. Three prominent, individual electron traps contribute significantly to the low-temperature noise of the *n*MOS devices. In contrast, no prominent defects are identified in the *p*MOS noise measurements. These differences in response are strong evidence of differences in the effective energy distributions of near-interfacial electron and hole traps in SiO_2/HfO_2 gate dielectrics. The noise in *n*MOS devices is affected strongly by non-uniformities in the effective border-trap defect-energy distribution associated with prominent individual defects in these devices. These results provide significant insight into the reasons for which *n*MOS and *p*MOS transistors often show significantly different noise magnitudes and gate-voltage dependence, and reinforce the significant role that prominent, individual defects can play in these comparisons and in performance, reliability, and radiation response.

CHAPTER 6

Conclusions

This dissertation investigates the radiation effects and low-frequency noise in advanced FinFETs. The first type of advanced FinFETs explored are the devices with the promising InGaAs channel material and highly-scaled fin widths. Single-event effects are studied in these devices through the pulsed laser method. The *n*MOS InGaAs FinFETs are fabricated by MIT with the fin-widths less than 10 nm. A 50 nm thick $In_{0.53}Ga_{0.47}As$ channel layer is grown on a 40 nm thick InP layer and a 300-nm thick $In_{0.52}Al_{0.48}As$ buffer layer. The FinFETs operate as double-gate MOSFETs with the channel controlled by the side gates, gate length L_G = 80, 100 nm, fin widths W_F= 5 nm, 7 nm, 9 nm, fin height H_F = 200 nm, fin number N_F = 34 and fin pitch of 0.2 μm. The gate dielectrics consist of one monolayer of Al_2O_3 and 3 nm of HfO_2 (EOT$\sim$ 0.8nm). Pulsed laser measurements are applied in the single event transient (SET) tests due to their nondestructive, easy-accessible and low-cost properties. Using a laser with 1260 nm wavelength ($\sim$0.98 eV), charge is generated from the InGaAs channel layer primarily via single-photon absorption (SPA), and from the InP and InAlAs layers via two-photon absorption (TPA). The bias dependences of SET are examined through the line scans of the pulsed laser from source to drain direction with different drain biases or gate biases. Devices with different fin widths within 10 nm were irradiated with the pulsed laser to extend the study of the fin-width dependence of SETs from wider fin to sub-10 nm region. 3-D TCAD simulations of single event transients were performed by using the heavy-ion model in Sentaurus TCAD to provide a further understanding of the charge collection mechanism.

The experimental results show that for InGaAs FinFETs on InP with sub-10-nm fin widths, more charge and higher peak currents are obtained in wider fin devices, which is likely due to an increase of sensitive volume for charge collection, consistent with results of devices with 20 and 30 nm fin widths. The amplitudes of the SETs and the collected charge increase with V_{ds} due to the enhancement of the electric field along the channel, while the peak drain current of SET does not change significantly with the gate voltage. This is because the fins are thin and fully depleted, and the two side gates have limited effect on the channel materials below the fins. Similar to the response of planar III-V MOSFETs, the tail current of SET increases as gate voltage increases.

Charge collection is influenced strongly by the shunt effect from source-to-drain when the laser spot covers the channel region, and by the parasitic bipolar effect caused by the accumulation of holes underneath the channel. The TCAD simulations demonstrate the dependence of the parasitic bipolar effect on fin width via the source-channel barrier lowering.

The second type of advanced FinFETs studied are bulk Si FinFETs with through-silicon vias (TSVs) near the active region, and highly-scaled fin width as well. The devices were fabricated by imec with ate length L_G = 1 μm, fin widths W_F= 7 nm, fin height H_F = 200 nm, fin number N_F = 220. The TSV was integrated $\sim$1 μm away from the channel with a diameter of 1 μm and a depth of 5 μm. Total-ionizing-dose effects and low-frequency noise at room temperature are evaluated in both *n*MOS and *p*MOS FinFETs with SiO_2/HfO_2 gate dielectrics. Otherwise identical devices built with and without through-silicon via (TSV) integration exhibit threshold voltage shifts of less than 25 mV and changes in maximum transconductance of less than 1% up to 2 Mrad(SiO_2). TSV integration negligibly impacts threshold shifts and degradation of subthreshold swing and I_{ON}/I_{OFF} ratios. Similar low-frequency noise magnitudes and frequency dependencies are observed before and after TID irradiation for each device type. Effective densities of the near-interfacial electron traps responsible for the noise in the *n*MOS devices increase as the surface potential moves toward midgap, while effective densities of the hole traps that cause the noise in the *p*MOS devices increase as the surface potential moves toward the valence band edge.

The opposite border-trap energy distribution trends in *n*MOS and *p*MOS devices inspired a further detailed investigation of the defects near the interface. The temperature dependence of low-frequency noise from 80 K to 320 K is explored for these *n*MOS and *p*MOS bulk Si FinFETs with SiO_2/HfO_2 gate dielectrics. The *n*MOSFET $1/f$ noise generally decreases as temperature increases, with three prominent individual defect-related peaks detected. These peaks in the noise magnitude as a function of temperature are most likely due to hydrogen shuttling near the interface and/or O vacancies in HfO_2. In contrast, the $1/f$ noise in the *p*MOSFETs generally increases with increasing temperature without any prominent peaks in the noise magnitude as a function of temperature. The gate-voltage dependence of low-frequency noise is evaluated at different temperatures for both device types, showing the trends in border-trap densities that are qualitatively consistent with those inferred from Dutta-Horn analysis of the temperature dependence of the noise.

References

[1] J. A. Del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, 2011.

[2] D. H. Kim, K. Athikulwongse, and S. K. Lim, "Study of through-silicon-via impact on the 3-D stacked IC layout," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 5, pp. 862–874, 2012.

[3] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: Carrier generation via two-photon absorption," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3002–3008, 2002.

[4] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transactions on Device and materials reliability*, vol. 5, no. 3, pp. 305–316, 2005.

[5] J. R. Hauser, S. E. Diehl-Nagle, A. R. Knudson, A. B. Campbell, W. J. Stapor, and P. Shapiro, "Ion track shunt effects in multi-junction structures," *IEEE Transactions on Nuclear Science*, vol. 32, no. 6, pp. 4115–4121, 1985.

[6] D. McMorrow, T. R. Weatherford, S. Buchner, A. R. Knudson, J. S. Melinger, L. H. Tran, and A. B. Campbell, "Single-event phenomena in GaAs devices and circuits," *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 628–644, 1996.

[7] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in MOS oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[8] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 483–499, 2003.

[9] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, K. L. Hughes, and F. W. Sexton, "Field dependence of interface-trap buildup in polysilicon and metal gate MOS devices," *IEEE Transactions on Nuclear Science*, vol. 37, no. 6, pp. 1632–1640, 1990.

[10] M. Haartman and M. Östling, *Low-frequency noise in advanced MOS devices*. Springer Science & Business Media, 2007.

[11] H. D. Xiong, *Low frequency noise and charge trapping in MOSFETs*. Vanderbilt University, 2004.

[12] C. Surya and T. Y. Hsiang, "Theory and experiment on the $1/f^{\gamma}$ noise in p-channel metal-oxide-semiconductor field-effect transistors at low drain bias," *Physical Review B*, vol. 33, no. 7, p. 4898, 1986.

[13] M. B. Weissman, "$1/f$ noise and other slow, nonexponential kinetics in condensed matter," *Reviews of Modern Physics*, vol. 60, no. 2, p. 537, 1988.

[14] C. Liang, R. Ma, K. Li, Y. Su, H. Gong, K. L. Ryder, P. Wang, A. L. Sternberg, E. X. Zhang, M. L. Alles *et al.*, "Laser-induced single-event transients in black phosphorus MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 384–388, 2018.

[15] H. Gong, K. Ni, E. X. Zhang, A. L. Sternberg, J. A. Kozub, K. L. Ryder, R. F. Keller, L. D. Ryder, S. M. Weiss, R. A. Weller *et al.*, "Scaling effects on single-event transients in InGaAs FinFETs," *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 296–303, 2017.

[16] G. Hiblot, S. Van Huylenbroeck, G. Van der Plas, B. De Wachter, A. V. Chasin, B. Kaczer, T. Chiarella, J. Mitard, S. De Muynck, G. Beyer *et al.*, "Impact of 1μ m TSV via-last integration on electrical performance of advanced FinFET devices," in *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*. IEEE, 2018, pp. 122–124.

[17] K. Li, E. X. Zhang, M. Gorchichko, P. F. Wang, M. Reaz, S. E. Zhao, G. Hiblot, S. Van Huylenbroeck, A. Jourdain, M. L. Alles *et al.*, "Impacts of Through-Silicon Vias on Total-Ionizing-Dose Effects and Low-Frequency Noise in FinFETs," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 740–747, 2021.

[18] D. M. Fleetwood, H. D. Xiong, Z. Y. Lu, C. J. Nicklaw, J. A. Felix, R. D. Schrimpf, and S. T. Pantelides, "Unified model of hole trapping, $1/f$ noise, and thermally stimulated current in MOS devices," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 2674–2683, 2002.

[19] G. E. Moore, "Cramming more components onto integrated circuits (reprinted from electronics, pp. 114-117, Apr. 19, 1965)," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[20] C. A. Mack, "Fifty years of Moore's law," *IEEE Transactions on Semiconductor Manufacturing*, vol. 24, no. 2, pp. 202–207, 2011.

[21] E. Mollick, "Establishing Moore's law," *IEEE Annals of the History of Computing*, vol. 28, no. 3, pp. 62–75, 2006.

[22] R. R. Schaller, "Moore's law: past, present and future," *IEEE Spectrum*, vol. 34, no. 6, pp. 52–59, 1997.

[23] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus *et al.*, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," *IEEE International Electron Devices Meeting*, pp. 978–980, 2003.

[24] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-*k*/metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Letters,*, vol. 25, no. 6, pp. 408–410, 2004.

[25] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau *et al.*, "A 45nm logic technology with high-*k*+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging," *IEEE International Electron Devices Meeting*, pp. 247–250, 2007.

[26] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, T.-J. King, J. Bokor, and C. Hu, "Sub-60-nm quasi-planar FinFETs fabricated using a simplified process," *IEEE Electron Device Letters,*, vol. 22, no. 10, pp. 487–489, 2001.

[27] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Device Letters*, vol. 24, no. 4, pp. 263–265, 2003.

[28] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman *et al.*, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *2012 Symposium on VLSI Technology (VLSIT)*. IEEE, 2012, pp. 131–132.

[29] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu *et al.*, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm 2 SRAM cell size," in *2014 IEEE International Electron Devices Meeting*. IEEE, 2014, pp. 3–7.

[30] J. L. Barth, C. S. Dyer, and E. G. Stassinopoulos, "Space, atmospheric, and terrestrial radiation environments," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 466–482, 2003.

[31] E. G. Stassinopoulos and J. P. Raymond, "The space radiation environment for electronics," *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1423–1442, 1988.

[32] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706–1730, 2013.

[33] J. R. Srour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653–670, 2003.

[34] H. J. Barnaby, "Total-ionizing-dose effects in modern CMOS technologies," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103–3121, 2006.

[35] D. M. Fleetwood, "Evolution of total ionizing dose effects in MOS devices with Moore's law scaling," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1465–1481, 2017.

[36] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise," *Advances in Physics*, vol. 38, no. 4, pp. 367–468, 1989.

[37] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, "1/f noise and radiation effects in MOS devices," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1953–1964, 1994.

[38] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: 1/f noise," *Reviews of Modern Physics*, vol. 53, no. 3, p. 497, 1981.

[39] D. M. Fleetwood, "1/f noise and defects in microelectronic materials and devices," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1462–1486, 2015.

[40] T. L. Meisenheimer and D. M. Fleetwood, "Effect of radiation-induced charge on 1/f noise in MOS devices," *IEEE Transactions on Nuclear Science*, vol. 37, no. 6, pp. 1696–1702, 1990.

[41] D. M. Fleetwood, "Total-ionizing-dose effects, border traps, and 1/f noise in emerging MOS technologies," *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, pp. 1216–1240, 2020.

[42] S. A. Francis, A. Dasgupta, and D. M. Fleetwood, "Effects of Total Dose Irradiation on the Gate-Voltage Dependence of the 1/f Noise of nMOS and pMOS Transistors," *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 503–510, 2009.

[43] J. Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1965–1971, 1994.

[44] C. Jakobson, I. Bloom, and Y. Nemirovsky, "$1/f$ noise in CMOS transistors for analog applications from subthreshold to saturation," *Solid-State Electronics*, vol. 42, no. 10, pp. 1807–1817, 1998.

[45] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: Individual interface traps and low-frequency ($1/f$) noise," *Physical Review Letters*, vol. 52, no. 3, p. 228, 1984.

[46] D. J. Frank, "Power-constrained CMOS scaling limits," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 235–244, 2002.

[47] J. Wang and M. Lundstrom, "Ballistic transport in high electron mobility transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 7, pp. 1604–1609, 2003.

[48] A. Rahman and M. S. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 481–489, 2002.

[49] A. Vardi, X. Zhao, and J. A. del Alamo, "Quantum-size effects in sub 10-nm fin width InGaAs FinFETs," in *2015 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2015, pp. 31–3.

[50] A. Vardi, L. Kong, W. Lu, X. Cai, X. Zhao, J. Grajal, and J. A. del Alamo, "Self-aligned InGaAs FinFETs with 5-nm fin-width and 5-nm gate-contact separation," in *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017, pp. 17–6.

[51] N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar, D. Tsvetanova, F. Sebaai, D. Van Dorp, A. Milenin *et al.*, "An InGaAs/InP quantum well FinFet using the replacement Fin process integrated in an RMG flow on 300 mm Si substrates," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*. IEEE, 2014, pp. 1–2.

[52] K. W. Guarini and H.-S. Wong, "Wafer bonding for high-performance logic applications," in *Wafer Bonding*. Springer, 2004, pp. 157–191.

[53] S. Oktyabrsky, J. Castracane, and A. E. Kaloyeros, "Materials, Components and Integration Technologies for Optical Interconnects," in *Proc. SPIE*, vol. 4652, no. 213, 2002.

[54] S. F. Al-Sarawi, D. Abbott, and P. D. Franzon, "A review of 3-D packaging technology," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 21, no. 1, pp. 2–14, 1998.

[55] A. W. Topol, D. La Tulipe, L. Shi, D. J. Frank, K. Bernstein, S. E. Steen, A. Kumar, G. U. Singco, A. M. Young, K. W. Guarini *et al.*, "Three-dimensional integrated circuits," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 491–506, 2006.

[56] R. Beica, C. Sharbono, and T. Ritzdorf, "Through silicon via copper electrodeposition for 3D integration," in *2008 58th Electronic Components and Technology Conference*. IEEE, 2008, pp. 577–583.

[57] J. H. Scofield, N. Borland, and D. M. Fleetwood, "Reconciliation of different gate-voltage dependencies of $1/f$ noise in n-MOS and p-MOS transistors," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1946–1952, 1994.

[58] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583–602, 2003.

[59] S. Buchner, N. Kanyogoro, D. McMorrow, C. C. Foster, P. M. O'Neill, and K. V. Nguyen, "Variable depth Bragg peak method for single event effects testing," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2976–2982, 2011.

[60] R. A. Reed, "Fundamental mechanisms for single particle-induced soft errors," in *IEEE NSREC Short Course*, 2008.

[61] J. S. Melinger, S. Buchner, D. McMorrow, W. J. Stapor, T. R. Weatherford, A. B. Campbell, and H. Eisen, "Critical evaluation of the pulsed laser method for single event effects testing and fundamental studies," *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, pp. 2574–2584, 1994.

[62] E. W. Van Stryland, H. Vanherzeele, M. A. Woodall, M. J. Soileau, A. L. Smirl, S. Guha, and T. F. Boggess, "Two photon absorption, nonlinear refraction, and optical limiting in semiconductors," *Optical Engineering*, vol. 24, no. 4, p. 244613, 1985.

[63] T. Boggess, K. Bohnert, K. Mansour, S. Moss, I. Boyd, and A. Smirl, "Simultaneous measurement of the two-photon coefficient and free-carrier cross section above the bandgap of crystalline silicon," *IEEE Journal of Quantum Electronics*, vol. 22, no. 2, pp. 360–368, 1986.

[64] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 603–621, 2003.

[65] C. M. Hsieh, P. C. Murley, and R. R. O'brien, "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices," *IEEE Electron Device Letters,*, vol. 2, no. 4, pp. 103–105, 1981.

[66] M. Gaillardin, P. Paillet, V. Ferlet-Cavrois, J. Baggio, D. McMorrow, O. Faynot, C. Jahan, L. Tosti, and S. Cristoloveanu, "Transient radiation response of single-and multiple-gate FD SOI transistors," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2355–2362, 2007.

[67] F. El-Mamouni, E. X. Zhang, N. D. Pate, N. Hooten, R. D. Schrimpf, R. A. Reed, K. F. Galloway, D. McMorrow, J. Warner, E. Simoen *et al.*, "Laser-and heavy ion-induced charge collection in bulk FinFETs," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2563–2569, 2011.

[68] F. El-Mamouni, E. X. Zhang, R. D. Schrimpf, R. A. Reed, K. F. Galloway, D. McMorrow, E. Simoen, C. Claeys, S. Cristoloveanu, and W. Xiong, "Pulsed laser-induced transient currents in bulk and silicon-on-insulator FinFETs," *International Reliability Physics Symposium*, pp. 882–885, 2011.

[69] F. El-Mamouni, E. X. Zhang, D. R. Ball, B. Sierawski, M. P. King, R. D. Schrimpf, R. A. Reed, M. L. Alles, D. M. Fleetwood, D. Linten *et al.*, "Heavy-ion-induced current transients in bulk and SOI FinFETs," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 2674–2681, 2012.

[70] K. Ni, A. L. Sternberg, E. X. Zhang, J. A. Kozub, R. Jiang, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, M. L. Alles, D. McMorrow *et al.*, "Understanding charge collection mechanisms in InGaAs FinFETs using high-speed pulsed-laser transient testing with tunable wavelength," *IEEE Transactions on Nuclear Science*, vol. 64, no. 8, pp. 2069–2078, 2017.

[71] H. Gong, K. Ni, E. X. Zhang, A. L. Sternberg, J. A. Kozub, M. L. Alles, R. A. Reed, D. M. Fleetwood, R. D. Schrimpf, N. Waldron *et al.*, "Pulsed-laser induced single-event transients in InGaAs FinFETs on bulk silicon substrates," *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 376–383, 2018.

[72] T. R. Weatherford and W. T. Anderson, "Historical perspective on radiation effects in III-V devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 704–710, 2003.

[73] J. M. Borrego, R. J. Gutmann, S. B. Moghe, and M. J. Chudzicki, "Radiation effects on GaAs MESFETs," *IEEE Transactions on Nuclear Science*, vol. 25, no. 6, pp. 1436–1443, 1978.

[74] I. K. Samsel, E. X. Zhang, N. C. Hooten, E. D. Funkhouser, W. G. Bennett, R. A. Reed, R. D. Schrimpf, M. W. McCurdy, D. M. Fleetwood, R. A. Weller *et al.*, "Charge collection mechanisms in AlGaN/GaN MOS high electron mobility transistors," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4439–4445, 2013.

[75] D. McMorrow, J. B. Boos, A. R. Knudson, W. T. Lotshaw, D. Park, J. S. Melinger, B. R. Bennett, A. Torres, V. Ferlet-Cavrois, J.-E. Sauvestre *et al.*, "Transient response of III-V field-effect transistors to heavy-ion irradiation," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3324–3331, 2004.

[76] S. DasGupta, D. McMorrow, R. A. Reed, R. D. Schrimpf, and J. B. Boos, "Gate bias dependence of single event charge collection in AlSb/InAs HEMTs," *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 1856–1860, 2010.

[77] K. Ni, E. X. Zhang, N. C. Hooten, W. G. Bennett, M. W. McCurdy, A. L. Sternberg, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, M. L. Alles *et al.*, "Single-event transient response of InGaAs MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3550–3556, 2014.

[78] K. Ni, E. X. Zhang, I. K. Samsel, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, A. L. Sternberg, M. W. McCurdy, S. Ren, T.-P. Ma *et al.*, "Charge collection mechanisms in GaAs MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2752–2759, 2015.

[79] C. Kittel, "Introduction to solid state physics," *American Journal of Physics*, vol. 35, no. 6, pp. 547–548, 1967.

[80] F. B. McLean, H. E. Boesch Jr, and T. R. Oldham, "Electron-hole generation, transport and trapping in SiO_2," in *Ionizing Radiation Effects in MOS Devices and Circuits*, 1989.

[81] F. B. McLean and G. A. Ausman Jr, "Simple approximate solutions to continuous-time random-walk transport," *Physical Review B*, vol. 15, no. 2, p. 1052, 1977.

[82] W. L. Warren, M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, P. S. Winokur, and R. Devine, "Microscopic nature of border traps in MOS oxides," *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, pp. 1817–1827, 1994.

[83] T. R. Oldham, A. J. Lelis, and F. B. McLean, "Spatial dependence of trapped holes determined from tunneling analysis and measured annealing," *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1203–1209, 1986.

[84] P. J. McWhorter, S. L. Miller, and W. M. Miller, "Modeling the anneal of radiation-induced trapped holes in a varying thermal environment," *IEEE Transactions on Nuclear Science*, vol. 37, no. 6, pp. 1682–1689, 1990.

[85] M. Schmidt and H. Köster Jr, "Hole trap analysis in SiO_2/Si structures by electron tunneling," *Physica Status Solidi (b)*, vol. 174, no. 1, pp. 53–66, 1992.

[86] A. J. Lelis, T. R. Oldham, H. E. Boesch, and F. B. McLean, "The nature of the trapped hole annealing process," *IEEE Transactions on Nuclear Science*, vol. 36, no. 6, pp. 1808–1815, 1989.

[87] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, "Physical mechanisms contributing to device "rebound"," *IEEE Transactions on Nuclear Science*, vol. 31, no. 6, pp. 1434–1438, 1984.

[88] S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Defect generation by hydrogen at the Si-SiO_2 interface," *Physical Review Letters*, vol. 87, no. 16, p. 165506, 2001.

[89] D. M. Fleetwood, "Border traps in MOS devices," *IEEE Transactions on Nuclear Science*, vol. 39, no. 2, pp. 269–271, 1992.

[90] D. M. Fleetwood, P. S. Winokur, R. A. Reber Jr, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, "Effects of oxide traps, interface traps, and "border traps" on metal-oxide-semiconductor devices," *Journal of Applied Physics*, vol. 73, no. 10, pp. 5058–5074, 1993.

[91] H. Nyquist, "Thermal agitation of electric charge in conductors," *Physical Review*, vol. 32, no. 1, p. 110, 1928.

[92] A. Van der Ziel, "Flicker noise in electronic devices," in *Advances in Electronics and Electron Physics*. Elsevier, 1979, vol. 49, pp. 225–297.

[93] L. K. J. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 2176–2187, 1994.

[94] A. L. McWorther, "$1/f$ noise and germanium surface properties," *Semiconductor Surface Physics*, vol. 207, 1957.

[95] S. Christensson, I. Lundström, and C. Svensson, "Low frequency noise in MOS transistors—I theory," *Solid-State Electronics*, vol. 11, no. 9, pp. 797–812, 1968.

[96] H. Mikoshiba, "$1/f$ noise in n-channel silicon-gate MOS transistors," *IEEE Transactions on Electron Devices*, vol. 29, no. 6, pp. 965–970, 1982.

[97] J. H. Scofield and D. M. Fleetwood, "Physical basis for nondestructive tests of MOS radiation hardness," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1567–1577, 1991.

[98] C. Surya and T. Y. Hsiang, "A thermal activation model for $1/f^{\gamma}$ noise in Si-MOSFETs," *Solid-state Electronics*, vol. 31, no. 5, pp. 959–964, 1988.

[99] S. Bonaldo, S. E. Zhao, A. O'Hara, M. Gorchichko, E. X. Zhang, S. Gerardin, A. Paccagnella, N. Waldron, N. Collaert, V. Putcha *et al.*, "Total-ionizing-dose effects and low-frequency noise in 16-nm InGaAs FinFETs with HfO_2/Al_2O_3 dielectrics," *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 210–220, 2019.

[100] C. Liang, R. Ma, Y. Su, A. O'Hara, E. Zhang, M. Alles, P. Wang, S. Zhao, S. Pantelides, S. J. Koester *et al.*, "Defects and low-frequency noise in irradiated black phosphorus MOSFETs with HfO_2 gate dielectrics," *IEEE Transactions on Nuclear Science*, vol. 65, no. 6, pp. 1227–1238, 2018.

[101] E. X. Zhang, I. K. Samsel, N. C. Hooten, W. G. Bennett, E. D. Funkhouser, K. Ni, D. R. Ball, M. W. McCurdy, D. M. Fleetwood, R. A. Reed *et al.*, "Heavy-Ion and Laser Induced Charge Collection in SiGe Channel pMOSFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3187–3192, 2014.

[102] H. Riel, L.-E. Wernersson, M. Hong, and J. A. Del Alamo, "III–V compound semiconductor transistors—from planar to nanowire structures," *Mrs Bulletin*, vol. 39, no. 8, pp. 668–677, 2014.

[103] J. A. Del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, "Nanometer-Scale III-V MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 5, pp. 205–214, 2016.

[104] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 294–296, 2008.

[105] L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell, R. Erni, and J. Fompeyrine, "Confined epitaxial lateral overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates," in *2015 Symposium on VLSI Technology (VLSI Technology)*. IEEE, 2015, pp. T172–T173.

[106] S. P. Buchner, F. Miller, V. Pouget, and D. P. McMorrow, "Pulsed-laser testing for single-event effects investigations," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1852–1875, 2013.

[107] K. Li, E. X. Zhang, S. Bonaldo, A. L. Sternberg, J. A. Kozub, A. M. Tonigan, M. Reaz, L. D. Ryder, K. L. Ryder, H. Gong *et al.*, "Pulsed Laser-Induced Single-Event Transients in InGaAs FinFETs with sub-10-nm Fin Widths," in *2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*. IEEE, 2019, pp. 1–5.

[108] E. X. Zhang, D. M. Fleetwood, N. D. Pate, R. A. Reed, A. F. Witulski, and R. D. Schrimpf, "Time-domain reflectometry measurements of total-ionizing-dose degradation of *n*MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4470–4475, 2013.

[109] A. H. Firester, M. E. Heller, and P. Sheng, "Knife-edge scanning measurements of subwavelength focused light beams," *Applied Optics*, vol. 16, no. 7, pp. 1971–1974, 1977.

[110] N. C. Hooten, W. G. Bennett, L. D. Edmonds, J. A. Kozub, R. A. Reed, R. D. Schrimpf, and R. A. Weller, "The impact of depletion region potential modulation on ion-induced current transient response," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4150–4158, 2013.

[111] N. C. Hooten, *Charge collection mechanisms in silicon devices during high-level carrier generation events*. Vanderbilt University, 2014.

[112] J. N. Damask, *Polarization optics in telecommunications*. Springer Science & Business Media, 2004, vol. 101.

[113] D. A. Humphreys, R. J. King, D. Jenkins, and A. J. Moseley, "Measurement of absorption coefficients of $Ga_{0.47}In_{0.53}As$ over the wavelength range 1.0-1.7 μm," *Electronics Letters*, vol. 21, no. 25, pp. 1187–1189, 1985.

[114] D. McMorrow, J. S. Melinger, N. Thantu, A. B. Campbell, T. R. Weatherford, A. R. Knudson, L. H. Tran, and A. Peczalski, "Charge-collection mechanisms of heterostructure FETs," *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, pp. 2055–2062, 1994.

[115] M. Murugesan, J. C. Bea, H. Kino, Y. Ohara, T. Kojima, A. Noriki, K. W. Lee, K. Kiyoyama, T. Fukushima, H. Nohira *et al.*, "Impact of remnant stress/strain and metal contamination in 3D-LSIs with through-Si vias fabricated by wafer thinning and bonding," in *2009 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2009, pp. 1–4.

[116] Y. Sugawara, H. Hashiguchi, S. Tanikawa, H. Kino, K.-W. Lee, T. Fukusima, M. Koyanagi, and T. Tanaka, "Impact of deep-via plasma etching process on transistor performance in 3D-IC with via-last backside TSV," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*. IEEE, 2015, pp. 822–827.

[117] A. Martin, "Review on the reliability characterization of plasma-induced damage," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 27, no. 1, pp. 426–434, 2009.

[118] R. A. Reed, R. A. Weller, M. H. Mendenhall, D. M. Fleetwood, K. M. Warren, B. D. Sierawski, M. P. King, R. D. Schrimpf, and E. C. Auden, "Physical processes and applications of the Monte Carlo radiative energy deposition (MRED) code," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1441–1461, 2015.

[119] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. T. Barrios, J. J. Liou, and C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 53, no. 1, pp. 90–104, 2013.

[120] G. X. Duan, C. X. Zhang, E. X. Zhang, J. Hachtel, D. M. Fleetwood, R. D. Schrimpf, R. A. Reed, M. L. Alles, S. T. Pantelides, G. Bersuker *et al.*, "Bias dependence of total ionizing dose effects in SiGe-MOS FinFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 2834–2838, 2014.

[121] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2584–2592, 1998.

[122] I. Chatterjee, E. X. Zhang, B. L. Bhuva, M. A. Alles, R. D. Schrimpf, D. M. Fleetwood, Y. P. Fang, and A. Oates, "Bias dependence of total-dose effects in bulk FinFETs," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4476–4482, 2013.

[123] I. Chatterjee, E. X. Zhang, B. L. Bhuva, R. A. Reed, M. L. Alles, N. N. Mahatme, D. R. Ball, R. D. Schrimpf, D. M. Fleetwood, D. Linten *et al.*, "Geometry dependence of total-dose effects in bulk FinFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 2951–2958, 2014.

[124] M. P. King, X. Wu, M. Eller, S. Samavedam, M. R. Shaneyfelt, A. I. Silva, B. L. Draper, W. C. Rice, T. L. Meisenheimer, J. A. Felix *et al.*, "Analysis of TID process, geometry, and bias condition dependence in 14-nm FinFETs and implications for RF and SRAM performance," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 285–292, 2016.

[125] C.-M. Zhang, F. Jazaeri, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz, "Characterization and modeling of Gigarad-TID-induced drain leakage current of 28-nm bulk MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 38–47, 2018.

[126] H. E. Boesch and J. M. Bendetto, "The relationship between Co-60 and 10-keV x-ray damage in MOS devices," *IEEE Transactions on Nuclear Science*, vol. 33, pp. 1318–1323, 1986.

[127] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for cobalt-60 and 10-keV X-ray irradiations of MOS devices," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1187–1194, 1991.

[128] P. Paillet, J. R. Schwank, M. R. Shaneyfelt, V. Ferlet-Cavrois, R. L. Jones, O. Flarrient, and E. W. Blackmore, "Comparison of charge yield in MOS devices for different radiation sources," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 2656–2661, 2002.

[129] M. Turowski, A. Raman, and R. D. Schrimpf, "Nonuniform total-dose-induced charge distribution in shallow-trench isolation oxides," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3166–3171, 2004.

[130] V. Re, L. Gaioni, M. Manghisoni, L. Ratti, and G. Traversi, "Comprehensive study of total ionizing dose damage mechanisms and their effects on noise sources in a 90 nm CMOS technology," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3272–3279, 2008.

[131] M. Gorchichko, Y. Cao, E. X. Zhang, D. Yan, H. Gong, S. E. Zhao, P. Wang, R. Jiang, C. Liang, D. M. Fleetwood *et al.*, "Total-ionizing-dose effects and low-frequency noise in 30-nm gate-length bulk and SOI FinFETs with SiO_2/HfO_2 gate dielectrics," *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 245–252, 2019.

[132] D. M. Fleetwood, M. R. Shaneyfelt, and J. R. Schwank, "Estimating oxide-trap, interface-trap, and border-trap charge densities in metal-oxide-semiconductor transistors," *Applied Physics Letters*, vol. 64, no. 15, pp. 1965–1967, 1994.

[133] X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, F. Faccio, and L. Gonella, "Radiation effects on the $1/f$ noise of field-oxide field effect transistors," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 2975–2980, 2008.

[134] E. Simoen, A. Mercha, L. Pantisano, C. Claeys, and E. Young, "Low-frequency noise behavior of SiO_2-HfO_2 dual-layer gate dielectric nMOSFETs with different interfacial oxide thickness," *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 780–784, 2004.

[135] B. Min, S. P. Devireddy, Z. Celik-Butler, A. Shanware, K. Green, J. J. Chambers, M. V. Visokay, and L. Colombo, "Low-frequency noise characteristics of HfSiON gate-dielectric

metal-oxide-semiconductor-field-effect transistors," *Applied Physics Letters*, vol. 86, no. 8, p. 082102, 2005.

[136] G. Giusi, F. Crupi, C. Pace, C. Ciofi, and G. Groeseneken, "Comparative study of drain and gate low-frequency noise in nMOSFETs with hafnium-based gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 823–828, 2006.

[137] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, "Origin of the threshold voltage instability in SiO_2/HfO_2 dual layer gate dielectrics," *IEEE Electron Device Letters*, vol. 24, no. 2, pp. 87–89, 2003.

[138] K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, "Defect energy levels in HfO_2 high-dielectric-constant gate oxide," *Applied Physics Letters*, vol. 87, no. 18, p. 183505, 2005.

[139] T. Grasser, W. Goes, Y. Wimmer, F. Schanovsky, G. Rzepa, M. Waltl, K. Rott, H. Reisinger, V. Afanas' ev, A. Stesmans *et al.*, "On the microscopic structure of hole traps in pMOSFETs," *IEEE International Electron Devices Meeting*, pp. 530–533, 2014.

[140] W. Goes, Y. Wimmer, A.-M. El-Sayed, G. Rzepa, M. Jech, A. L. Shluger, and T. Grasser, "Identification of oxide defects in semiconductor devices: A systematic approach linking DFT to rate equations and experimental evidence," *Microelectronics Reliability*, vol. 87, pp. 286–320, 2018.

[141] W. Tian, T. Ma, and X. Liu, "TSV Technology and high-energy heavy ions radiation impact review," *Electronics*, vol. 7, no. 7, p. 112, 2018.

[142] H. L. Hughes and J. M. Benedetto, "Radiation effects and hardening of MOS technology: Devices and circuits," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 500–521, 2003.

[143] G. X. Duan, J. A. Hachtel, E. X. Zhang, C. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, R. A. Reed, J. Mitard, D. Linten, L. Witters *et al.*, "Effects of Negative-Bias-Temperature-Instability on Low-Frequency Noise in SiGe *p*MOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 4, pp. 541–548, 2016.

[144] D. M. Fleetwood, P. S. Winokur, M. R. Shaneyfelt, L. C. Riewe, O. Flament, P. Paillet, and J. L. Leray, "Effects of isochronal annealing and irradiation temperature on radiation-induced trapped charge," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2366–2374, 1998.

[145] J. H. Scofield, N. Borland, and D. M. Fleetwood, "Temperature-independent switching rates for a random telegraph signal in a silicon metal–oxide–semiconductor field-effect transistor at low temperatures," *Applied Physics Letters*, vol. 76, no. 22, pp. 3248–3250, 2000.

[146] D. M. Fleetwood, T. Postel, and N. Giordano, "Temperature dependence of the $1/f$ noise of carbon resistors," *Journal of Applied Physics*, vol. 56, no. 11, pp. 3256–3260, 1984.

[147] D. M. Fleetwood and N. Giordano, "Direct link between $1/f$ noise and defects in metal films," *Physical Review B*, vol. 31, no. 2, p. 1157, 1985.

[148] A. G. Marinopoulos, I. Batyrev, X. J. Zhou, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Hydrogen shuttling near Hf-defect complexes in SiO_2/HfO_2 structures," *Applied Physics Letters*, vol. 91, no. 23, p. 233503, 2007.

[149] M. Gorchichko, E. X. Zhang, P. Wang, S. Bonaldo, R. D. Schrimpf, R. A. Reed, D. Linten, J. Mitard, and D. M. Fleetwood, "Total-ionizing-dose response of highly scaled gate-all-around Si nanowire CMOS transistors," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 687–696, 2021.

[150] P. Wang, R. Jiang, J. Chen, E. X. Zhang, M. W. McCurdy, R. D. Schrimpf, and D. M. Fleetwood, "1/f noise in as-processed and proton-irradiated AlGaN/GaN HEMTs due to carrier number fluctuations," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 181–189, 2016.

[151] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectronics Reliability*, vol. 52, no. 1, pp. 39–70, 2012.