Total-Ionizing-Dose Effects, Low-Frequency Noise, and Random Telegraph Noise of MOSFETs with Advanced Architectures

By

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Every time when you try to measure noise, you succeed. It is just that you don't always know where this noise comes from.

—Dr. Daniel Fleetwood

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AIC	Akaike Information Criterion
BIC	Bayesian Information Criterion
BOX	Buried Oxide
BTI	Bias Temperature Instability
CMOS	Complementary Metal Oxide Semiconductor
CTT	Charge Trap Transistor
DC	Direct Current
DD	Displacement Damage
DFT	Density Functional Theory
EOT	Effective Oxide Thickness
FinFET	Fin Field Effects Transistors
GAA	Gate-All-Around
GR	Generation-Recombination
HMM	Hidden Markov Model
LFN	Low Frequency Noise
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NW	Nanowire
P/E	Programming/Erasing
PLL	Phase-Locked Loop
PSD	Power Spectral Density
RF	Radio Frequency
RTN	Random Telegraph Noise
S/D	Source/Drain
SEE	Single Event Effects
SILC	Stress-Induced Leakage Current
STAR	Self-heating Temperature Assisted eRase
STI	Shallow Trench Isolation
SOI	Silicon-On-Insulator
SS	Subthreshold Slope
TID	Total Ionization Dose

CHAPTER I

INTRODUCTION

Space exploration has been both a source of inspiration and one of the greatest technological challenges for humankind. In order to operate in space, electronic systems must have high reliability and radiation tolerance, in addition to an ever-increasing demand for speed, performance, and memory size. Thus, the mitigation of space-radiation-induced effects has been a significant concern for space exploration [1], [2]. Galactic cosmic rays, solar particle events, and Van Allen radiation belts all contribute to a space radiation environment that can temporarily or permanently degrade the performance of electronic components, circuits, and systems [3], [4]. Based on their underlying mechanisms, radiation-induced effects are classified as Total-Ionizing-Dose (TID) effects, Single Event Effects (SEEs), and Displacement Damage (DD). SEEs are instantaneous and caused by a single particle strike, ionizing a sensitive volume of semiconductor material in an electronic component. SEEs impact can significantly vary from the recoverable loss of information to permanent damage and functional interruptions [5]. Both TID and DD are cumulative effects that occur through the interaction of an electronic device with a large number of particles. TID causes long-term degradation via ionization of a dielectric material and the formation of a radiation-induced trapped charge close to the active area of an electronic device [6], [7]. On the other hand, DD causes non-ionizing long-term damage arising from the displacement of atoms from the semiconductor lattice [8].

In order to mitigate radiation-induced effects, a deeper investigation of the radiation degradation mechanisms is needed. It has been found that low-frequency noise can provide insight into border-trap densities, defect energy distributions, and defect microstructures in metal-oxide-semiconductor (MOS) devices, including TID-induced defects [9]–[19]. Low-frequency noise (LFN, $1/f$ noise, flicker noise, pink noise) is a form of noise in electronic devices that dominates at low frequencies with a magnitude inversely proportional to its frequency. There is no single mechanism responsible for $1/f$ noise in all electronic devices. Instead, for example, in metal films, low-frequency noise is attributed to carrier mobility fluctuations due to scattering on defects and impurities [15], [20]. In the majority of MOS devices, the most important source of $1/f$ noise is carrier number fluctuations associated with the trapping on and detrapping from defects and impurities [15], [21]–[23]. The origin of $1/f$ noise in many devices with advanced materials is yet to be determined [24].

Understanding 1/*f* noise is also critical because of its role in analog and radio-frequency (RF) circuits. The increase of low-frequency noise in nanoscale devices due to the degradation of signal-to-noise ratio and highly-scaled gate areas has recently captured a lot of attention. High LFN negatively affects the performance of analog and radio-frequency (RF) electronic devices fabricated in low-voltage CMOS technology. More specifically, 1/*f* noise affects the input voltage of operational amplifiers, the most commonly used element of analog and mixed-signal circuits [25]. Furthermore, the noise decreases the stability of virtual ground and requires the implementation of specific 1/*f* noise reduction techniques [25], [26]. Additionally, 1/*f* noise upconverts into close-in phase noise of a voltage-controlled oscillator, an integral part of a phase-locked loop (PLL), and degrades its performance [27], [28]. While the effects of 1/*f* noise on circuit performance are not discussed in this dissertation in detail, the obtained results could be of interest for designers of analog, mixed-signal, and RF circuits for space and terrestrial applications.

Due to a small number of defects active in modern highly-scaled devices, the pure 1/*f* law can be disturbed when the impact on a single prominent defect dominates the noise response of the device. This type of noise response is called Random Telegraph Noise (RTN) [29]. It manifests through the Lorentzian shape of noise spectra in the frequency domain and abrupt switching events between two or more current levels in the time domain. RTN can significantly affect characteristics of the transistor, for example, by shifting threshold voltage and increasing leakage [30]–[32]. Thus, in recent years, RTN has become a significant concern for memory devices [33]–[35]. In addition, irradiation can contribute to the activation/passivation of prominent defects, leading to RTN in highly-scaled devices.

This work is focused on investigating total-ionizing-dose effects in nanoscale silicon Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with advanced architectures, e.g., Gate-All-Around (GAA) FETs and Charge-Trapping Transistor (CTT) FinFETs using low-frequency and random telegraph noise.

The first part of this dissertation is focused on GAA FETs. GAA transistors enable the best of all possible electrostatic configurations in FETs with the elimination of short-channel effects. Various technological advancements over the last ten years, e.g., vertical stacking [36], [37] and nanosheet structures [38] for increased drive current, dual work-function metal gate stacks for optimized control of threshold voltages [39], and improvements in the integration of high-k dielectrics with reduced interface-trap densities [40]–[42] enable GAA devices to become a promising candidate for sub-7-nm technological nodes. From their first

demonstrations more than 30 years ago, GAA devices have shown improved total-ionizing-dose (TID) response in comparison with planar SOI MOSFETs [43]–[45] due to edge leakage suppression. Despite a long history of development, only a few attempts to characterize the radiation response of GAA devices have been made. Recent studies have pointed out the potentially high TID tolerance of Si- and III-V semiconductor-based GAA devices due to decreased radiation-induced charge buildup and the elimination of parasitic conduction channels [46], [47]. In [48], the authors investigate the role of gate spacers and overlap between S/D and the gate edge for radiation tolerance of sub-100 nm GAA devices. Several works have explored the potential of GAA structure for radiation-tolerant memories [49], [50]. Simulations suggest that GAA Si transistors with high-k gate stack can outperform their FinFET counterparts in terms of radiation tolerance due to improved gate control [51].

The second part of this work is focused on CTTs. These memory devices can be built as standard logic transistors and programmed and erased via high-field charge injection [52]–[54]. CTTs can achieve large electrically programmable threshold voltages through the population of existing traps in the bulk of the high-k dielectrics and at the interface between the high-k dielectric and the interfacial thermal oxide, as well as through the creation of additional traps during the Programming/Erasing (P/E) operations [52]–[55]. Brewer and co-workers performed an initial evaluation of the TID response of CTTs [55], who found that 14-nm bulk FinFETs are affected less by TID irradiation than 22-nm planar silicon-on-insulator devices as trapping in the BOX dominates [55].

This work is structured as follows. Chapter II discusses gives the background information of low-frequency noise, random telegraph noise, and total-ionizing effects. Chapter III presents DC response of GAA FETs to ionizing irradiation. *n*FETs and *p*FETs show similar TID responses, making the GAA NW technology an excellent candidate for CMOS IC applications in high-radiation environments. In Chapter IV low-frequency noise and random telegraph noise responses provide insight into defects in GAA devices. Prominent traps in the SiO_2 and HfO_2 dielectrics are observed before and after irradiation; they are most likely due to oxygen vacancies and/or hydrogen complexes. Chapter V provides the evaluation of TID results for as-processed, irradiated, programmed, and erased CTTs. Significant random telegraph noise (RTN) is observed in as-processed 2-fin devices. TID increases the uniformity of effective border-trap energy distributions. Programming/erasing leads to activation/deactivation of prominent individual traps, but underlying, featureless $1/f$ noise magnitudes are not affected significantly. Finally, Chapter VI provides a summary of the work.

CHAPTER II

BACKGROUND

2.1 Fundamental Noise Sources

There are a few primary noise sources in electronic devices and materials: thermal noise (Nyquist, Johnson noise), shot (Poisson) noise, and generation-recombination noise.

Thermal noise is caused by the thermal motion of electrons in materials. When an electron is scattered, the velocity of this electron is randomized; thus, the average net current of all carriers over a long time is zero. Thermal noise in a resistor is independent of electrical current flowing through the device and for frequencies $f < 10^{12}$ Hz and temperatures $T > 10$ K is independent of frequency, i.e., "white" noise, with the voltage noise power spectral density (PSD) S_V:

$$S_V = 4kTR, \qquad \text{II-1}$$

where k is the Boltzmann constant, T is the absolute temperature, and R is resistance.

Shot noise stems from the discrete nature of the electric charge. The current flow in an electronic device consists of discrete charge carriers: electrons emitted from a cathode or crossed a potential barrier at random times. A Poisson distribution of the waiting times/frequencies before emission/crossing of a barrier leads to shot noise. This noise is also "white" over a wide range of frequencies for $f < \sim 10^{12}$ Hz. Contrary to the thermal noise, shot noise is dependent on electric current flowing through the device and is independent of the temperature of the system and can be expressed as:

$$S_I = 2qI, \qquad \text{II-2}$$

where S_I is the current noise power spectral density, q is the electronic charge, and I is the current flowing through the device.

Generation-recombination (GR) noise originates from fluctuations in the number of free carriers in a semiconductor due to random transitions of carriers between states in different energy bands, primarily due to transitions between (1) localized levels in the bandgap, i.e., traps, and conduction band, (2) conduction and valence bands [15], [56], [57]. The trapping/detrapping process caused by a single trap will have a power spectral density in the form of:

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+\omega^2\tau^2}, \qquad \text{II-3}$$

where $\overline{\Delta N^2}$ is the variance of number fluctuations and τ is a time constant for charge fluctuations in this trap [56]. Eq. II-3 produces a noise spectrum with a Lorentzian shape, where the noise PSD is constant for low frequencies and decreases as $1/f^2$ after reaching the cut-off frequency. A special case of generation-recombination noise is RTN, which is discussed in section 2.2.

Low-frequency noise with the magnitude inversely proportional to the frequency is usually observed for $f < 10^3$ Hz - 10^4 Hz. For the majority of MOS devices, $1/f$ noise originates from the superposition of generation-recombination noise, so the carrier mobility fluctuations and Hooge model is not discussed in this work [58].

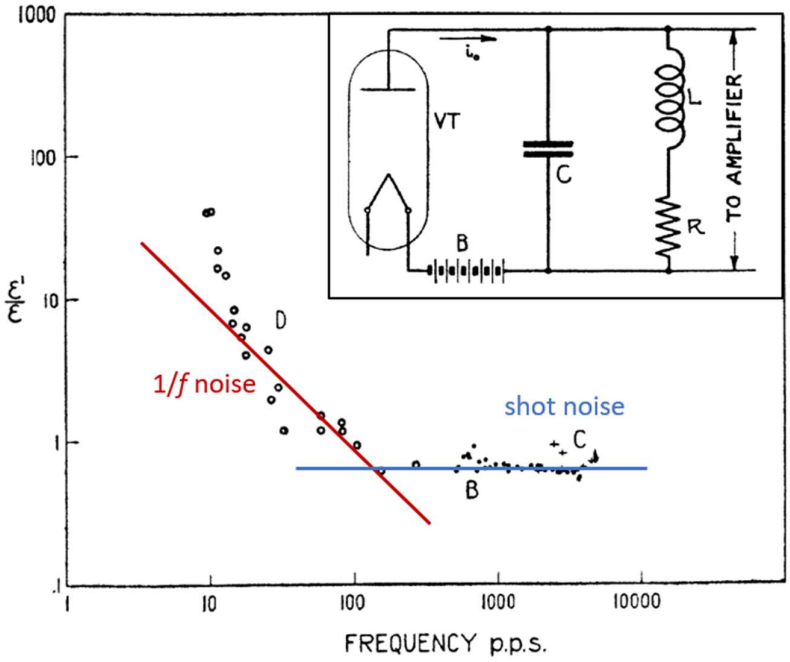


Fig. II-1. Relative voltage fluctuations in tungsten filament following $1/f$ dependence were found for low frequencies from ~10 Hz to ~100 Hz (B, C, D – different inductances L). Inset: The experimental circuit with a vacuum tube. (After [59].)

2.2 Low-Frequency Noise in MOS Devices

Processes of fluctuating physical variables $V(t)$, exhibiting power-spectrum behavior $S(f)$, inversely proportional to the process frequency f, are widespread in the world. They can be observed from voltage fluctuations of electrical impulses in nerve membranes [60] to the brightness of quasars and undersea ocean current velocities [61]. The phenomenon of low-

frequency noise in electronic devices significantly influences the performance of microelectronic systems and has been intensively studied for almost a hundred years.

The voltage fluctuations, inversely proportional to frequency, in microelectronic devices were initially found in vacuum tubes. The first observation of 1/*f* noise occurred in 1925 by J.B. Johnson during his studies on shot noise [59], discovered by W. Schottky in filaments of vacuum tubes a few years before that [62]. The voltage fluctuations across the experimental circuit consisting of a vacuum tube and a resonant RLC circuit were found to be dependent on the frequency at low frequencies. Noise, observed by J.B. Johnson in tungsten and oxide coated filaments, was much larger at low frequencies than it was predicted for shot noise. The observed results and the experimental circuit are shown in Fig. II-1. These results allowed the researcher to suppose that the observed effect has a different nature than a pure probabilistic emission of electrons (as in the shot noise), that the process leading to this effect happens at different rates, and is greatly dependent on the surface of the filament, but no coherent theory was yet proposed.

According to [15], further investigation of 1/*f* noise in MOS devices was related to the following significant achievements. Firstly, it was established in 1937 that 1/*f* noise is a thermally-activated random process with a uniform distribution of energies. Secondly, McWhorter's model allowed first-order estimates of effective trap densities in MOS transistors in 1957 [63], attributing the noise to carrier number fluctuations caused by tunnel-assisted trapping and detrapping electrons from the Si channel on near-interfacial SiO_2. Finally, the development of the Dutta-Horn model [64] allowed one to infer defect energy distributions from the temperature dependence of *1/f* noise, which was proved to apply to Si- and compound-semiconductor-based microelectronic devices.

With the recent advances in material science and the plethora of new materials and devices with new materials applications developed recently, the specific mechanisms of low-frequency noise in the advanced materials still require thorough investigation, for example, in charge-density-wave materials [24], [65].

2.2.1 Origin of 1/*f* Noise in MOS Devices

1/*f* noise in semiconductor devices is a process caused by the thermally activated interaction of carriers with border traps located close to a channel/oxide interface. These traps has specific characteristic times: time to capture a carrier and time to emit the carrier; the distribution of characteristic times forms the noise process with a specific range of frequencies.

Each trap has its characteristic time τ_i with which the trap can exchange charge or "switch" (trap and release an electron) with the channel by a tunneling process, which causes time constant dispersion [66]. Traps are distributed in physical space and energy space, so the effective density of border traps obtained through *1/f* noise measurements depends on the time scale and voltage bias conditions during the measurements [67]. The probability of an oxide defect to capture an electron decreases exponentially as the distance from the interface to the trap increases [23], [66], [68]. The McWhorter model suggests that with *1/f* noise measurements, it is easier to access traps in SiO_2 with the energy level in the vicinity of the Fermi level, usually within a few *kT* [15], which means that we are able to sense defects close to the conduction band for *n*MOS transistors and to the valence band in the *p*MOS transistors. Fig. II-2 shows a schematic illustration of the process leading to *1/f* noise. An electron traveling from the source to the drain through the inversion layer of Si substrate can be trapped by defects in the gate oxide located close to the semiconductor-dielectric interface (border traps). These traps that can exchange charges with the channel in the time frame of the measurements are called border traps [67], [69], [70]. Usually, they are located within 1-3 nm from the channel/oxide interface.

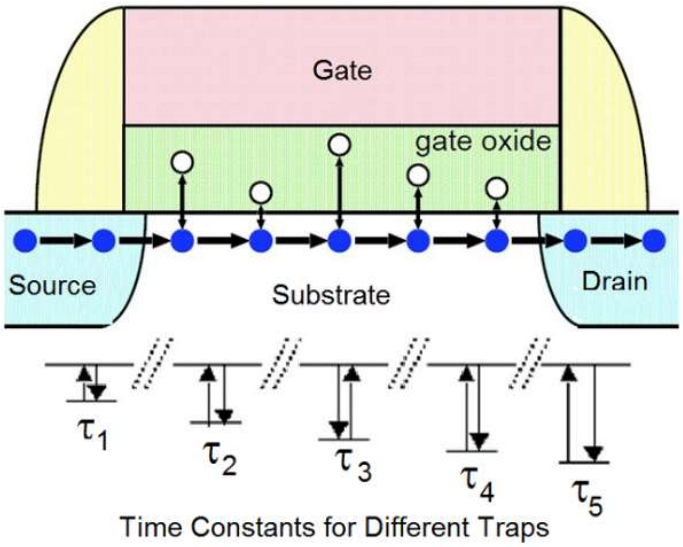


Fig. II-2. The schematic illustration of *1/f* noise origin in MOSFET due to gate oxide traps with different time constraints. (After [71].)

Electrons, trapped in the gate oxide, decrease the net voltage drop between the positively biased gate terminal and grounded substrate, which decreases the effective gate

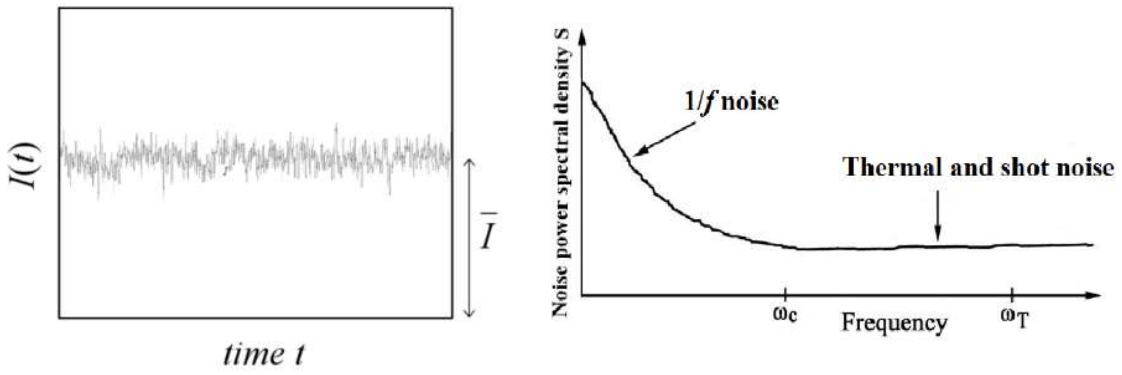
voltage and subsequently decreases the drain current. Conversely, releasing the electron to the channel and leaving an empty border trap behind increases the effective gate voltage and the drain current. Since the trapping/detrapping process is stochastic and the number of carriers in the channel is large, it can significantly affect the device's performance. The diagram of the process is shown in Fig. II-3.

Fig. II-3. A diagram of the impact of charge trapping on device parameters.

Accounting for the random fluctuations component, the drain current can be written as:

$$I(t) = \bar{I} + i_n(t), \qquad \text{II-4}$$

where $\bar{I}$ is the average bias current, and $i_n(t)$ is a randomly fluctuating current [56], which is illustrated in Fig. II-4(a). When converted with Fourier transformation noise in the MOS device will look like Fig. II-4(b): at low frequencies, the noise spectrum in form of power spectral density (PSD) is proportional to $1/f^{\alpha}$ with $\alpha \approx 1$ and at high frequencies where thermal and shot noise components are dominant the noise is approximately constant.



(a) (b)

Fig. II-4. (a) A typical noise waveform in the time domain (After [56]); (b) the schematic illustration of noise power spectral density in the frequency domain (After [72].)

In the majority of MOS devices, *1/f* noise is caused by fluctuations in the number of carriers, i.e., a stochastic process of capturing and emitting carriers as discussed above. For example, in Fig. II-5, *1/f* noise spectrum is a superposition of 11 prominent traps spectra with

different characteristic times and, subsequently, different corner frequencies. *1/f* noise is formed by a plurality of the switching events and if the distribution of the time constants of traps follows the rule $D(\tau) \sim 1/\tau$ for $\tau_1<\tau<\tau_2$, so the shape of the *1/f* noise is proportional to *1/f* for $1/\tau_2<f<1/\tau_1$ [15] and results in a similar spectrum shown in Fig. II-5.

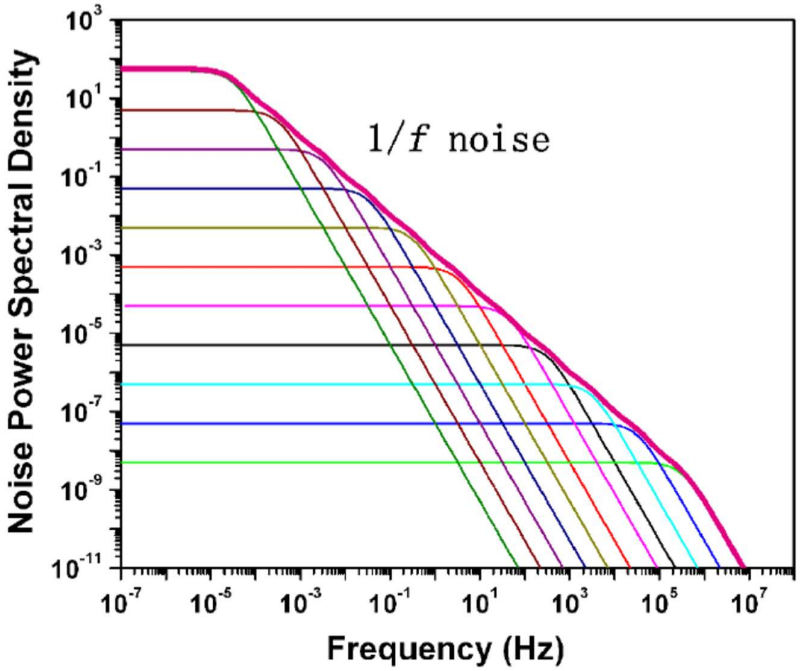


Fig. II-5. The schematic illustration of *1/f* noise power spectral density as a superposition of Lorentzian spectra of generation-recombination noise with different corner frequencies. (After [72].)

To first order, the low-frequency noise of MOS devices can be described via a simple number-fluctuation model that assumes tunnel-assisted charge exchange between the channel Si and defects in the near-interfacial gate oxide [10], [15], [18], [21], [22], [63], [73]. Within the framework of this model, the excess drain-voltage noise power spectral density, S_{Vd}, is described via:

$$S_{V_d} = \frac{q^2}{C_{ox}^2} \frac{V_d^2}{\left(V_g - V_{th}\right)^2} \frac{kTD_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f}, \qquad \text{II-5}$$

Here V_{th}, V_g, and V_d are the threshold, gate, and drain voltages, C_{ox} is the gate oxide capacitance per unit area, L and W are the transistor channel length and width, $D_t(E_f)$ is the number of traps per unit area at the Fermi level E_f, T is the absolute temperature, k is the Boltzmann constant, f is the frequency and τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [15],

[21], [22], [63], [73], [74]. The gate-voltage dependence $\beta = \partial \ln S_{Vd}/\partial \ln |V_g\text{-}V_{th}|$ of the noise is an indicator of the degree of uniformity of $D_t(E_f)$ [15], [21], [22], [63], [73], [74]. The value of $\beta \approx 2$ corresponds to an approximately uniform distribution of effective border-trap energies throughout the Si bandgap [15], [21], [74]. Values of $\beta < 2$ denote an energy distribution increasing toward the conduction (valence) band edge for *n*MOS (*p*MOS) transistors, and values of $\beta > 2$ denote a distribution increasing toward midgap [15], [18], [21], [74]. Consequently, the border-trap density D_{bt} in the gate oxide was extracted from 1/*f* noise measurements via

$$D_{bt} = \frac{A\, C_{ox}^2}{q^2 k_B T} ln \frac{\tau_1}{\tau_0} \frac{(V_g - V_t)^2}{V_d^2} S_{V_d} f. \quad \text{II-6}$$

2.2.2 Temperature Dependence of *1/f* Noise

Dutta and Horn have shown that if (1) the noise is caused by a random thermally activated process having a broad distribution of energies *D(E)* relative to *kT*, where *k* is the Boltzmann constant and *T* is the temperature, (2) the fluctuation process is characterized by an attempt frequency f_0 much higher than the measuring frequency, and (3) the coupling constants between the random processes responsible for the noise and the total integrated noise magnitude are independent of frequency [14], [15], [64], [75], the frequency and temperature dependences of the noise are related via

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega \tau_0)} \left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1 \right). \quad \text{II-7}$$

Here S_V is the excess voltage-noise power spectral density after the thermal noise is subtracted, $\tau_0 = 1/f_0$ is the characteristic attempt time of the process leading to the noise and the frequency $\omega = 2\pi f$. A value of $\tau_0 = 1.81 \times 10^{-15}$ s is chosen here to be consistent with previous MOS studies[14], [15], [17]. For noise described by Eq. II-7, the shape of the defect-energy distribution $D(E_0)$ can be described via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T), \quad \text{II-8}$$

where the defect energy [15], [76]:

$$E_0 \approx -kT \ln(\omega\, \tau_0). \quad \text{II-9}$$

If the noise is the result of thermally activated processes involving two energy levels, for example, E_0 is the barrier that the system must overcome to move from one configurational state to the other [10], [15], [64]. A schematic illustration of the transition process in a system with two energy levels is shown in Fig. II-6.

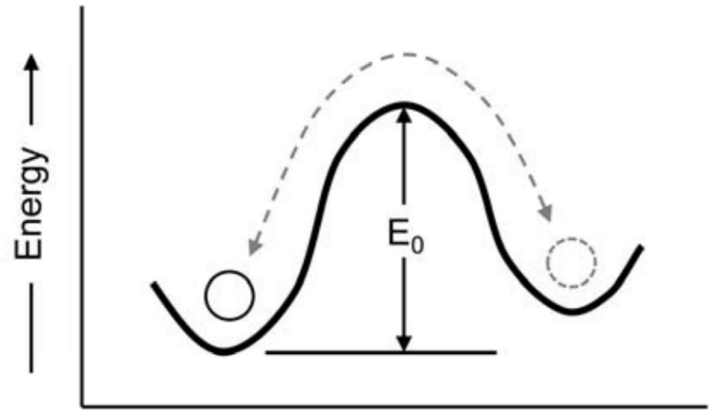


Fig. II-6. Schematic illustration of a system with two configurations with different energy levels, charge states, and/or carrier scattering rates. E_0 is the energy barrier for the system to move reversibly from one configurational state to another. (After [18].)

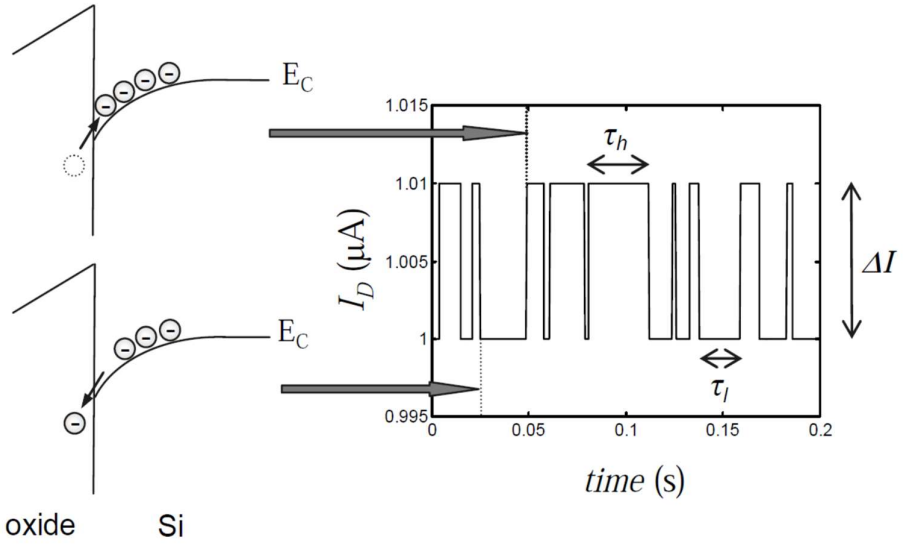


Fig. II-7. Schematic description of RTS noise, exemplified for a MOSFET. The drain current switches between two discrete levels when a channel electron moves in and out of a trap in the gate oxide. (After [56].)

2.3 Random Telegraph Noise

2.3.1 Origin of Random Telegraph Noise

Noise that represents itself in the time domain as a series of random discrete switching events is called random telegraph noise (RTN). In its simplest forms, the current (resistance) switches between two levels: “high” and “low” and can be characterized by the amplitude

ΔI (ΔR), as shown in Fig. II-7. RTN was reported in MOSFETs in 1984 and attributed to random trapping and detrapping of carries by a trap located near the Si/SiO_2 interface [29].

For a symmetric capture-emission process with a single characteristic time constant $\tau = \tau_e = \tau_c$, where τ_e and τ_c are emission and capture times, RTN fluctuations exhibit a Lorentzian power spectral density [23], [31], [77]:

$$S_{V_d}(f) = \frac{2(\Delta V_d)^2 \tau}{4 + (2\pi f \tau)^2}, \qquad \text{II-10}$$

where ΔV_d is the fluctuation in drain voltage caused by trapping/detrapping. At low frequencies, i.e., $2\pi f < 1/\tau$, the noise magnitude of a device with noise dominated by RTN due to a single prominent fluctuator is relatively independent of frequency, consistent with the results shown below. At high frequencies, i.e., $2\pi f > 1/\tau$, the noise magnitude falls off as $\sim 1/f^2$. The characteristic frequency f_c, corresponding to the point at which S_{Vd} decreases to half its plateau amplitude, is given by [31]:

$$2\pi f_c = \frac{1}{\tau}. \qquad \text{II-11}$$

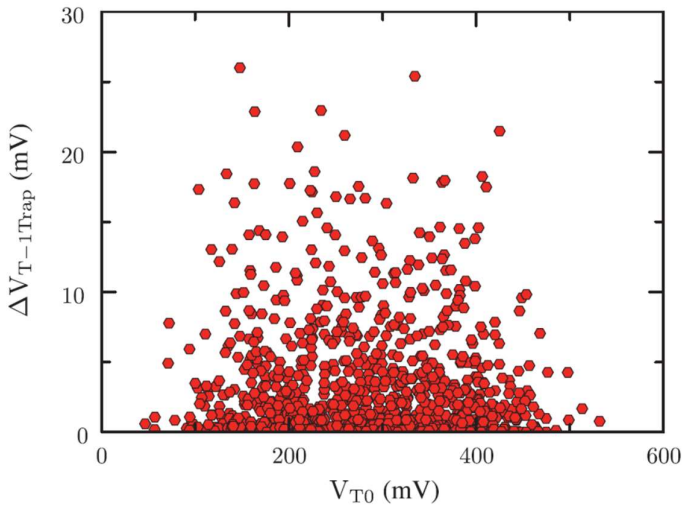


Fig. II-8. Single trap induced threshold voltage shift ΔV_t as a function of initial V_t for 1000 devices suffering from combined statistical variability. (After [78].)

It is widely accepted that $1/f$ noise observed in large-area MOSFETs is a superposition of individual Lorentzians, as shown in Fig. II-5 [23], [31], [63]. However, in modern technologies with small-area devices, noise response is usually dominated by RTN, which causes significant concerns in terms of device-to-device variability and circuit performance [78], [79]. As an example of the possible severity of RTN in modern transistors, Fig. II-8 shows

simulated threshold voltage shifts up to 25 mV due to activation of one trap in devices simulated with several sources of statistical variability.

2.3.2 Analysis of Random Telegraph Noise

A variety of different methods was developed for RTN characterization. RTN could be measured on different timescales: starting from microseconds to tenths and hundreds of seconds, often determined by equipment resolution, and providing different analysis depth.

2.3.2.1 Conventional methods

One of the easiest and widely used methods is weighted time lag plots [80]. It consists of mapping the current levels for two consecutive time moments, $t = t_i$ and $t = t_{i+1}$, against each other on perpendicular scales, as shown in Fig. II-9. Here, three stable current levels are located on the diagonal of the plot, denoted by stars for clarity. These current levels are produced by trapping/detrapping on two "large" traps. This method gives a clear picture of the distribution of the device's current levels and "switching" between them.

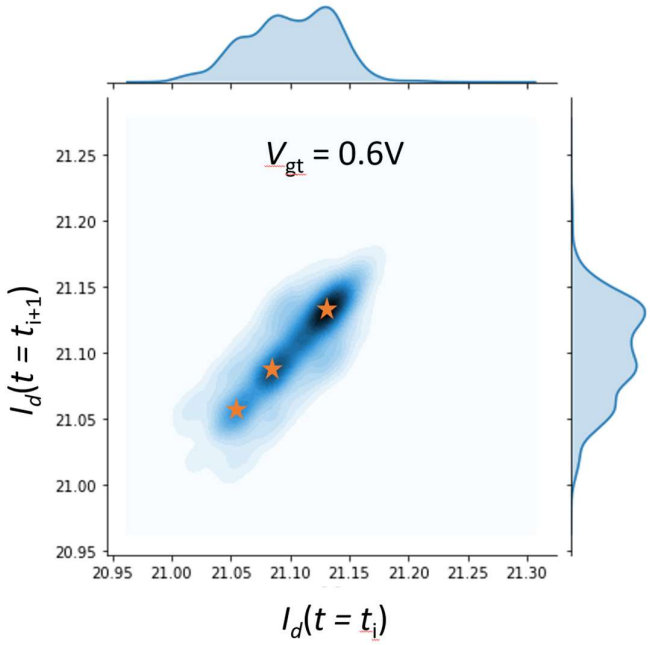


Fig. II-9. Weighted time lag plot showing stable current states on the diagonals and amplitude histograms (top, right) derived from time-domain signals for V_{GT} = 0.6 V. At least two "large" traps are present, producing three stable current levels denoted by stars.

Thus, weighted time lag plots are an excellent tool to evaluate the presence of RTN caused by "large" traps active in the device – traps characterized by a significant difference in

current levels and high probability of the device to be in one of the trap's states. Unfortunately, it does not give insight into small traps: more subtle or less common traps are also active simultaneously. Often the skewness of the distribution of occurrence of specific current levels vs. current levels can prompt the presence of small traps (Fig. II-10(b)) and the need for additional analysis methods. In contrast, symmetrical distribution with a single peak signifies the noise formed by defects, uniformly distributed in energy, and will show 1/*f*-like behavior in the frequency domain (Fig. II-10(a)).

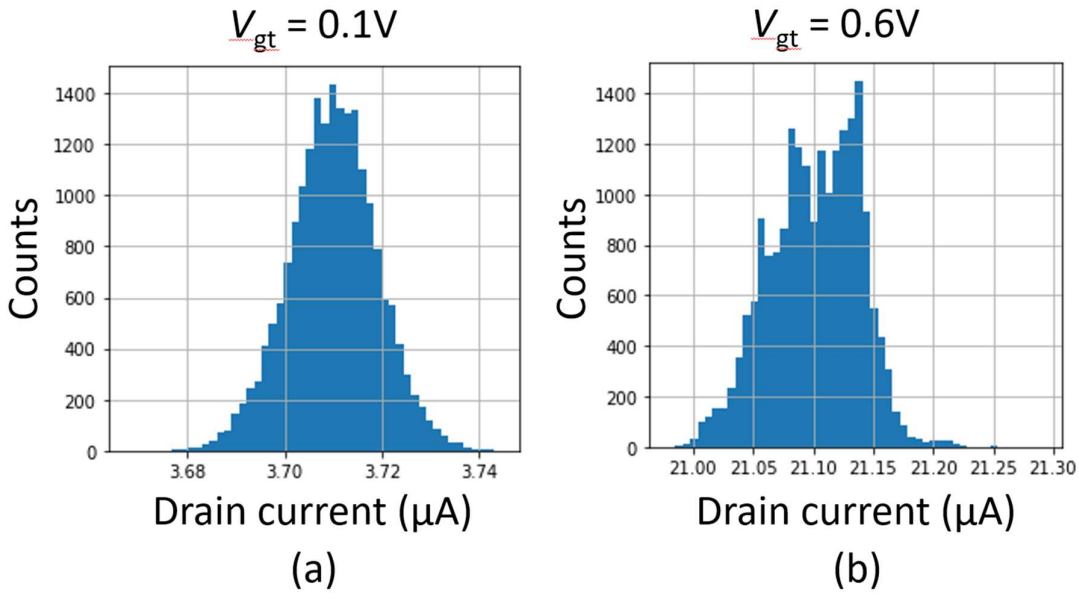


Fig. II-10. (a) Relatively symmetrical distribution of drain current with a single peak, which represents 1/*f* noise behavior and absence of RTN; (b) "Skewed" distribution with at least three peaks, which requires further analysis of small traps active in the device but not clearly visible on the weighted time lag plot on Fig. II-9.

2.3.2.2 Hidden Markov Models

One of the ways how small traps could be analyzed is by applying Hidden Markov Model (HMM) to RTN data. Application of HMM to the identification of traps in gate-all-around transistors is discussed in section 4.3. HMM is a statistical model commonly used for time series data analysis in various applications. It is based on the Markov chain or Markov process – a random sequence of states (events), where the probability of the following state depends only on the present state, i.e., the future state is independent of the past states, given the present. The simple structure of HMM for drain fluctuation is shown in Fig. II-11. Here,

the observations are the sequence of drain current values, which is governed by the trapping and detrapping of carriers on two defects in the gate dielectric. The defects here are denoted as hidden states A and B, which we cannot observe directly, but they affect the drain current output. The system is described by state transition probabilities p_{AB}, p_{BA} - transitions from the state of one trap dominating current response and by output probabilities φ_{A1}, φ_{A2}, φ_{B2}, φ_{B3} – the likelihood that a specific trap, being active, will lead to a specific current level. The goal of applying HMM to RTN analysis is given the observations I_d, characterize active defects in the device (hidden states) in terms of time to emission τ_e and time to capture τ_c. This information can be further used to determine the location of the defect with respect to the channel, as described in section 4.3.

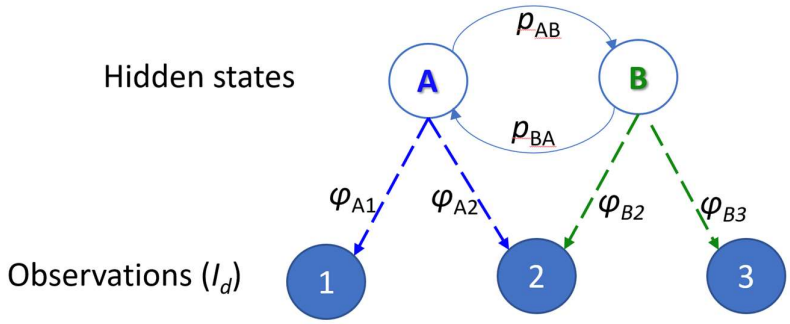


Fig. II-11. The basic structure of HMM, where A, B are hidden states; 1, 2, 3 are observations, in our case drain current fluctuations I_d; p_{AB}, p_{BA} – state transition probabilities; φ_{A1}, φ_{A2}, φ_{B2}, φ_{B3} – output probabilities.

A simplified example of RTN parameter extraction using HMM with two hidden states is shown in Fig. II-12. Here, the top trace shows the experimental results (noisy blue data on the back); on top of it is the extracted via HMM resulting RTN. Two bottom traces show the contribution of each trap to the resulting RTN. So, in this simplified example, trap A is empty for the majority of the time (high current level prevails). In contrast, trap B is occupied most of the time (low current level means that there are fewer carriers in the channel, so the carrier was trapped on a defect). By dividing the high current level for one trap over the low current level for the same trap, one will estimate the τ_e/τ_c ratio of the trap.

While solving the problem of identifying defects using HMM, it is up to the researcher to guess how many hidden states (traps) use in the model. It could be challenging to determine by eye how many traps are active in the device and if the particular “trained” HMM is the best

possible fit for the given current data. Choosing a large number of hidden states will improve the likelihood function of the model but likely cause overfitting. There are two common approaches used to weight different HMMs against each other and select the best model while preventing overfitting, are Bayesian Information Criterion (BIC) and Akaike Information Criterion (AIC) via:

$$BIC = -2 \cdot LL + p \cdot \ln N, \quad \text{II-12}$$

$$AIC = -2 \cdot LL + 2p, \quad \text{II-13}$$

where N is the length of the observation, LL is the logarithmic likelihood of the model, p denotes the number of independent parameters of the model and can be calculated as follows:

$$p = m^2 + km - 1. \quad \text{II-14}$$

Here m is the number of states in the Markov chain of the model, and k is a single numeric value representing the number of parameters of the underlying distribution of the observation process (e.g., k=2 for the normal distribution (mean and standard deviation)) [81]. Fig. II-13 shows a dependence of BIC and AIC as a function of the number of traps m. The optimal number of traps is six because it is the first local minimum of the BIC (and AIC). Thus, further increase in the number of traps will not add significant improvement in the accuracy of the model.

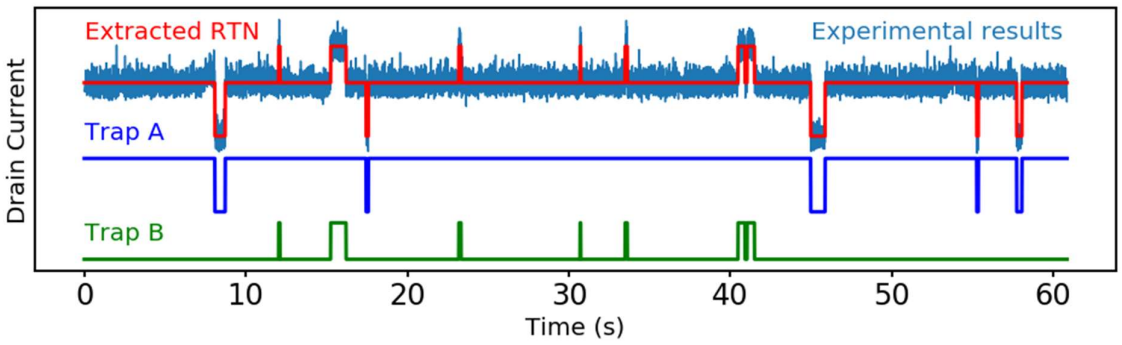


Fig. II-12. Simplified example of RTN extraction using HMM, shown in Fig. II-11.

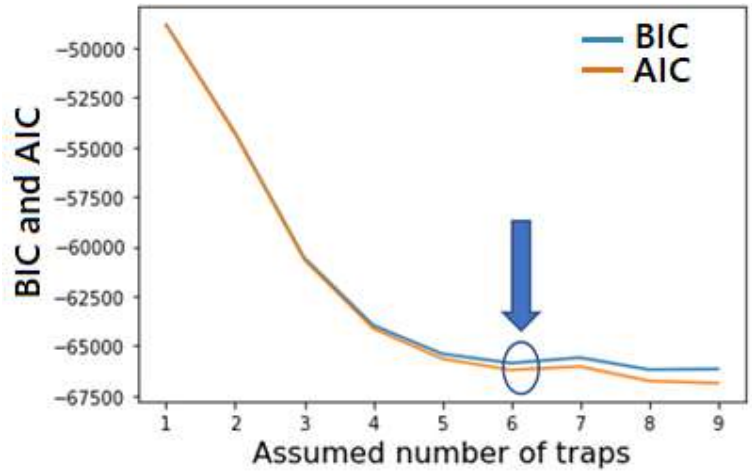


Fig. II-13. Dependence of BIC and AIC on the number of traps in HMM with the optimum number of traps denoted by the arrow.

2.4 Total Ionizing Dose Effects in MOS Devices

2.4.1 Mechanism

TID irradiation creates electron-hole pairs in dielectrics and contributes to charge trapping, which affects the performance of the device. The classical mechanism of this process is explained in Fig. II-14. This is a band diagram of a biased device under ionizing irradiation. (1) The electron-hole pairs created during irradiation transport in different directions under applied electric field: unrecombined electrons - towards the positively charged gate, unrecombined holes - to the oxide-semiconductor interface. Since the mobility of holes is significantly lower than the mobility of electrons, (2) they slowly travel towards the Si-SiO_2 interface through localized states in SiO_2 along with protons. When they reach the interface, (3) the pre-existing oxygen vacancies capture holes and form oxide and border traps, and (4) free protons contribute to interface-trap buildup [6], [82]–[86]. Nowadays, for highly-scaled devices, radiation-induced charge trapping in the STI for bulk devices and in BOX for SOI devices became a primary radiation-tolerance concern since gate stack oxides have been replaced by thin layers of high-k materials [85].

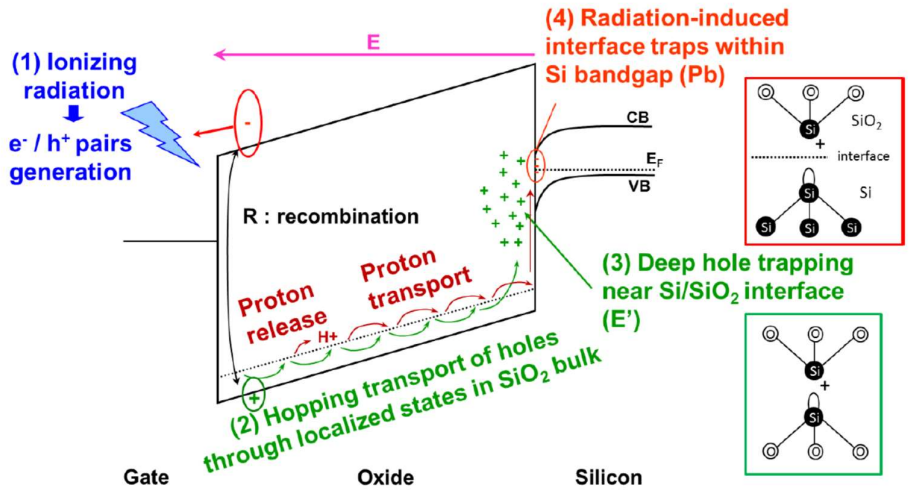


Fig. II-14. Process of radiation-induced interface and oxide traps formation described in the band diagram of a biased metal-oxide-semiconductor structure [84].

2.4.2 Influence of Irradiation on DC Characteristics

TID irradiation contributes to the formation of interface traps and oxide traps in a microelectronic device. Oxide traps are positively charged in SiO_2, while interface traps can change their electrical states due to surface potential.

Fig. II-15 indicates the contribution of radiation-induced oxide and interface traps buildup to the DC characteristics of *n*MOS and *p*MOS devices. Oxide traps are charged positively in SiO_2 both in *p*MOS and *n*MOS, i.e., they decrease the threshold voltage and shift IV curves negatively, which is shown with dashed green lines in Fig. II-15. *p*MOS transistors at threshold are affected mainly by positively charged interface traps located in the lower part of the Si bandgap (empty donor-like traps). Consequently, the effects of positive interface traps and positive oxide traps add up for *p*MOS devices, increasing the absolute value of the negative threshold voltage and shifting the IV curve negatively during TID exposure (i.e., the increase of the radiation-induced threshold voltage shift) [84], [86]. On the other hand, *n*MOS devices at threshold are affected mainly by negatively charged traps located in the upper part of the Si bandgap (filled acceptor-like traps). So, for *n*MOS devices, the effect of negatively charged interface traps compensates the negative radiation-induced threshold voltage shift due to always positive oxide traps.

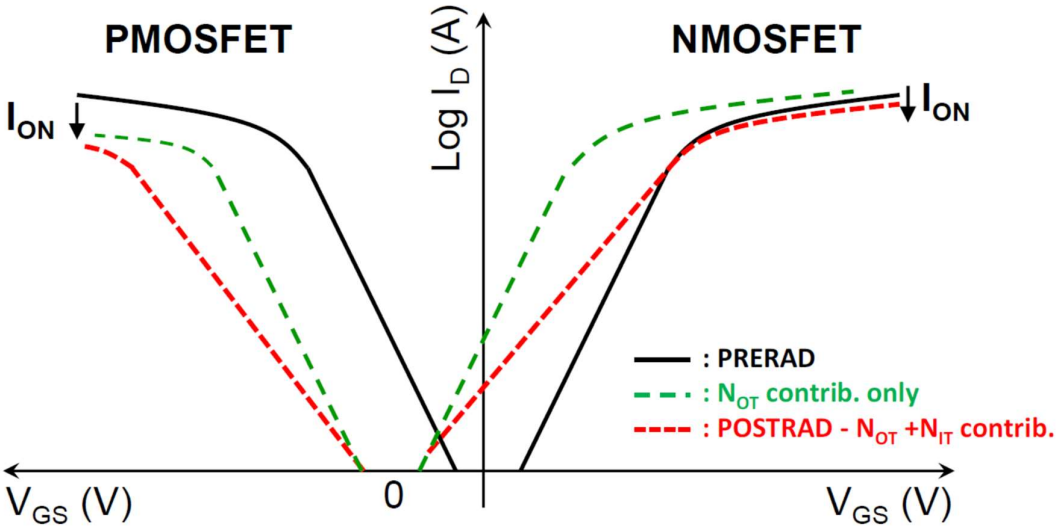


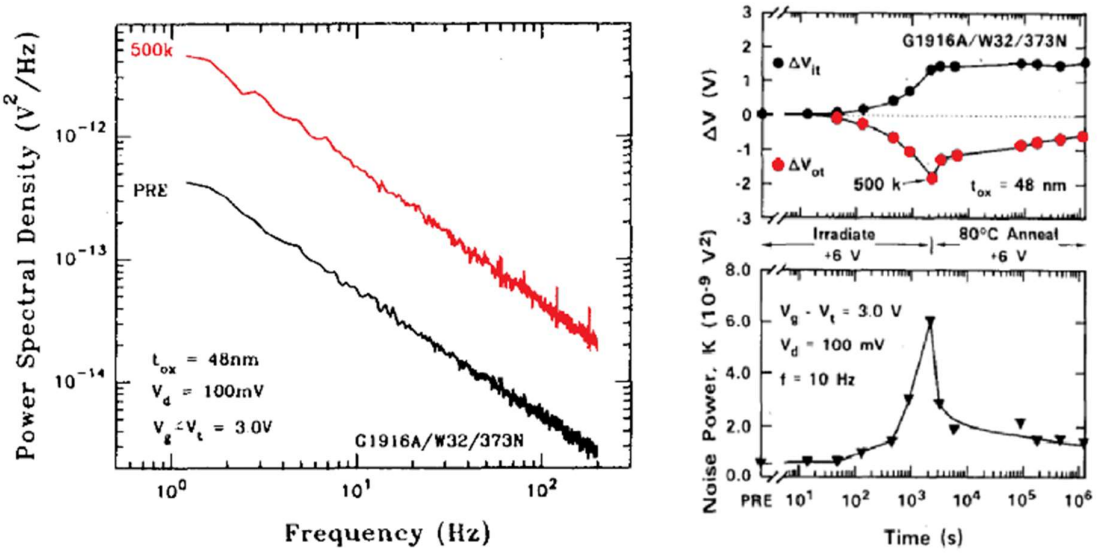
Fig. II-15. Radiation-induced oxide trapped charge (green dashes) and interface traps (short red dashes) contributions on I-V curves in *p*MOSFET and *n*MOSFETs [84].

2.4.3 Influence of Irradiation on *1/f* Noise and RTN

Due to the activation of border traps during TID irradiation low-frequency noise of irradiated devices is higher than the low-frequency noise of as-processed devices fabricated in older technologies [13]–[15], [87]–[89]. Fig. II-16(a) shows typical results for a micron-sized MOSFET before and after irradiation with a significant uniform increase in the post-irradiation noise spectrum over the whole range of measured frequencies.

It has been found that the pre-irradiation *1/f* noise level in MOS devices strongly correlates with post-irradiation threshold voltage shift due to border traps buildup [68], [90]. Further evidence of the correlation between *1/f* noise and threshold voltage shift due to oxide traps was observed in [11], demonstrating that *1/f* noise in the studied transistors increased with increasing the amount of the oxide traps during irradiation and decreasing during annealing with decreasing of the oxide traps. In contrast, the number of interface traps was almost constant during annealing [13], shown in Fig. II-16(b).

The combination of density functional theory (DFT) calculations and low-frequency noise measurements as a function of temperature and irradiation is a powerful tool for determining reliability-limiting defects in microelectronic materials and devices and processes occurring during irradiation [15]. One of the examples [17], [75], [87], [91], [92] is shown in Fig. II-17, where defects in graphene transistors activated during irradiation were passivated during high-temperature annealing and were attributed to the influence of hydrogen- and oxygen-related defects.



(a) (b)

Fig. II-16. (a) Pre- and post-irradiation *1/f* noise spectra for MOSFET L_{CH} = 7.5 μm, W_{CH} = 50 μm (after [11]); (b) Top: threshold voltage shift due to interface-trap charge ΔV_{it} and oxide trap charge ΔV_{ot} as a function of irradiation and annealing. Bottom: normalized noise power through the same irradiation and annealing processes. (After [13].)

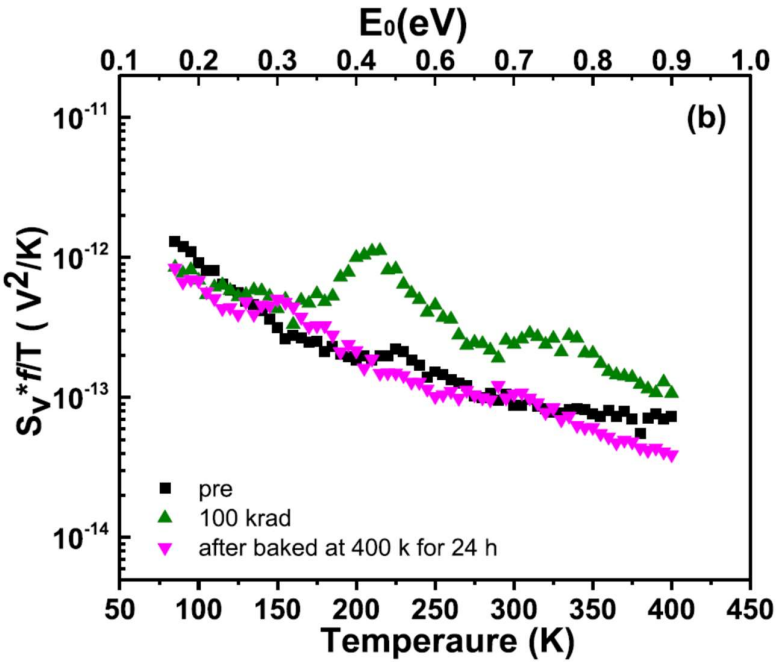


Fig. II-17. 1/*f* noise vs temperature before and after irradiation and after high-temperature annealing of graphene transistors from [93].

For highly-scaled devices, instead of a uniform increase of low-frequency noise, as shown in Fig. II-16, activation of prominent defects leads to disturbed 1/*f* noise behavior [18]. In Fig. II-18, deviations from pure 1/*f* law are observed for as processed and irradiated bulk FinFET. Initially, a "fast" prominent defect was active at low frequencies, with corner frequency ~ 4 Hz. After irradiation, this defect was passivated, but two other defects were activated: the "fast" defect outside of the measured frequencies, with a part of a Lorentzian spectrum visible from 1 Hz to 3 Hz, and the "slow" defect, with the plateau visible from ~4 Hz to ~300 Hz. This behavior shows that the distribution of defects active in this device was significantly altered due to irradiation. Thus, the noise response is governed by individual defects, implying a non-uniform defect energy distribution. These results indicate the importance of joint analysis of 1/*f* noise and RTN to provide insight into the properties of radiation-induced individual defects in highly-scaled devices.

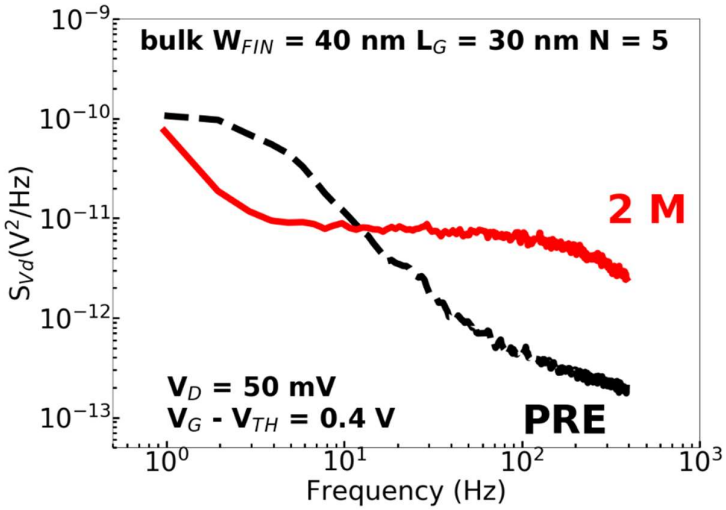


Fig. II-18. S_{Vd} as a function of *f* for representative SOI and bulk FinFETs fabricated by imec before and after irradiation with ~10-keV X-rays to 2 Mrad(SiO_2) under ON-state bias. The dielectric is 2.3 nm HfO_2 over 1 nm interfacial oxide; the effective oxide thickness is 1.5 nm. Tested devices had 5 fins, channel length of 30 nm, and fin widths of 40 nm. For noise measurements, V_d = 50 mV and $V_g - V_{th}$ = 0.4 V. (Data for this plot is taken from [19]).

CHAPTER III

TOTAL-IONIZING-DOSE RESPONSE OF GATE-ALL-AROUND DEVICES

This chapter is adapted from "Total-Ionizing-Dose Response of Highly-Scaled Gate-All-Around Si Nanowire CMOS Transistors" published in IEEE Transactions on Nuclear Science and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Pan Wang, Stefano Bonaldo, Ronald D. Schrimpf, Robert A. Reed, Dimitri Linten, Jerome Mitard, and Daniel M. Fleetwood.
Reference:

- M. Gorchichko *et al.*, "Total-ionizing-dose response of highly scaled gate-all-around Si nanowire CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 687–696, May 2021.

Gate-all-around (GAA) transistors enable the best of all possible electrostatic configurations in FETs with the elimination of short-channel effects. Various technological advancements over the last ten years, e.g., vertical stacking [36], [37] and nanosheet structures [38] for increased drive current, dual work-function metal gate stacks for optimized control of threshold voltages [39], and improvements in the integration of high-k dielectrics with reduced interface-trap densities [40]–[42] enable GAA devices to become a promising candidate for sub-7-nm technological nodes. From their first demonstrations more than 30 years ago, GAA devices have shown improved total-ionizing-dose (TID) response in comparison with planar SOI MOSFETs [43]–[45] due to edge leakage suppression.

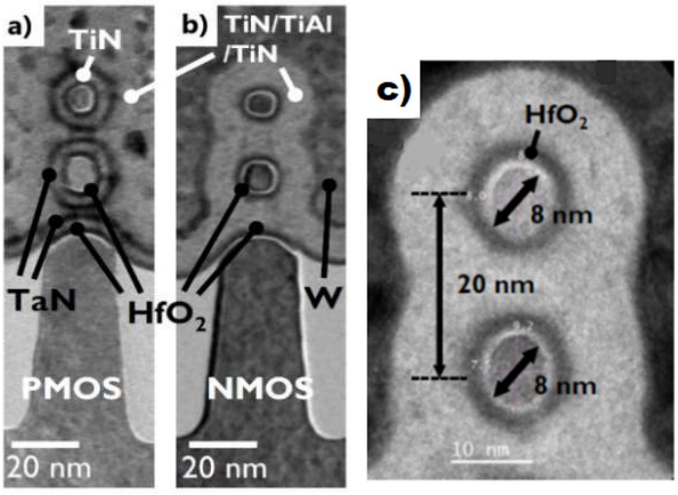


Fig. III-1. Cross-sectional TEM images of a) pMOS and b) nMOS transistors at the end of the fabrication process; c) enlarged image of NW. (After [94].)

Despite a long history of development, only a few attempts to characterize the radiation response of GAA devices have been made. Recent studies have pointed out the potentially high TID tolerance of Si- and III-V semiconductor-based GAA devices due to decreased radiation-induced charge buildup and the elimination of parasitic conduction channels [46], [47]. In [48], authors investigate the role of gate spacers and overlap between S/D and the gate edge for radiation tolerance of sub-100 nm GAA devices. Several works have explored the potential of GAA structure for radiation-tolerant memories [49], [50]. Simulations suggest that GAA Si transistors with high-k gate stack can outperform their FinFET counterparts in terms of radiation tolerance due to improved gate control [51].

In Chapter III, we investigate the basic mechanisms of the TID response of highly-scaled bulk GAA Si nanowire (NW) CMOS transistors. *n*FETs and *p*FETs show comparable TID sensitivities. DC measurements demonstrate outstanding ionizing radiation tolerance due to enhanced electrostatic gate control and suppression of parasitic leakage current. Minimal changes are observed in threshold voltage, peak transconductance, and subthreshold slope (SS).

3.1 Studied Devices

Four-terminal GAA transistors with horizontal silicon NWs were fabricated by imec [95], [96]. *n*FETs in this chapter have gate length L_g = 24-26 nm, and *p*FETs have L_g = 24-34 nm. Fig. III-1 shows cross-sectional images of the GAA NW FETs under test. The gate stack features 1.8 nm of HfO_2 over a thin layer of interfacial SiO_2. Threshold-voltage matching of *n*FETs and *p*FETs is obtained via dual-work-function metal integration [96]. Each transistor has four fins; each fin contains two vertically stacked horizontal Si NWs with a diameter of 8 nm (circumference ~ 25 nm).

TABLE III-1
IRRADIATION AND ANNEALING CONDITIONS FOR GAA NW FETS

nFET				
Bias condition	V_g (V)	V_d (V)	V_S (V)	V_B (V)
Positive gate bias	0.5	0	0	0
Positive drain bias	0	0.5	0	0
Negative gate bias	-0.5	0	0	0
*p*FET				
Bias condition	V_g (V)	V_d (V)	V_S (V)	V_B (V)
Negative gate bias	-0.5	0	0	0
Negative drain bias	0	-0.5	0	0
Positive gate bias	0.5	0	0	0

3.2 Experimental Setup

3.2.1 Irradiation

Devices were irradiated at room temperature with ~10-keV X-rays [6] at a dose rate of 30.3 krad(SiO_2)/min up to 1 Mrad(SiO_2) (unless otherwise stated) with ARACOR Model 4100 Semiconductor Irradiation Test Source. Devices were tested with wafer probes positioned to prevent shadowing of X-rays. IV characteristics were obtained at V_d = 0.05 V with an Agilent 4156A/4156B semiconductor parameter analyzer. Biases applied during irradiation and room-temperature annealing are listed in Table III-1.

3.3 Experimental Results

3.3.1 Impact of Irradiation on DC Characteristics

To distinguish electrical-stress-related degradation from radiation-induced degradation, bias conditions of Table III-1 were applied for the same times as it takes for devices to be irradiated up to 1 Mrad(SiO_2), ~32 min. Both types of GAA NW FETs show excellent stability, with threshold voltage shifts ΔV_{th} less than 2 mV for each examined bias condition. As one example, positive (negative) gate-bias stress results for a typical *n*FET (*p*FET) are shown in Fig. III-2. Devices show negligible stress-induced degradation for this bias and time.

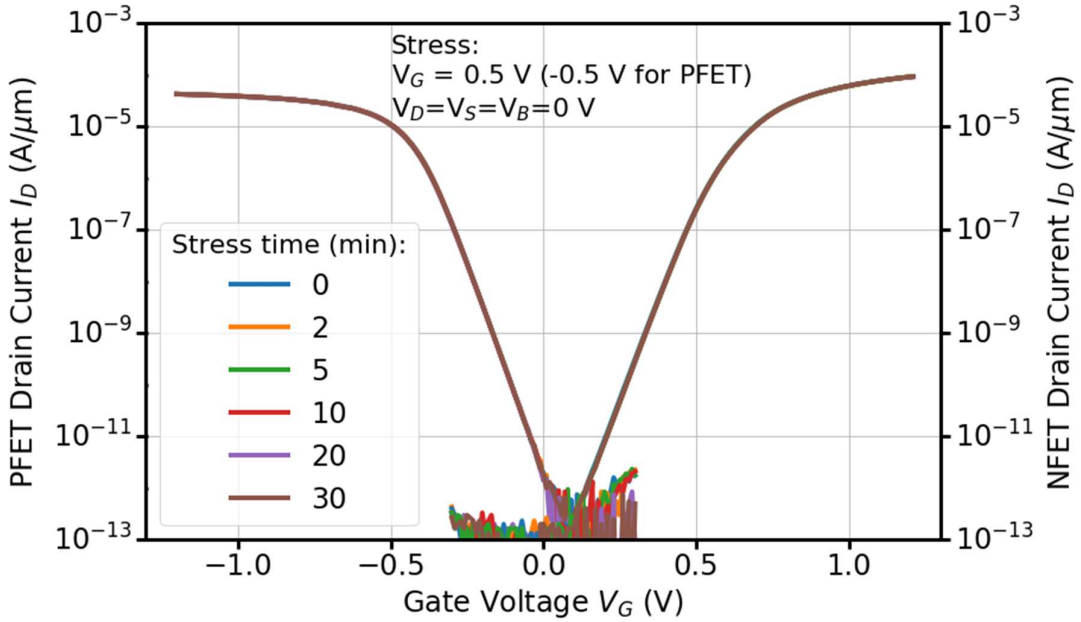
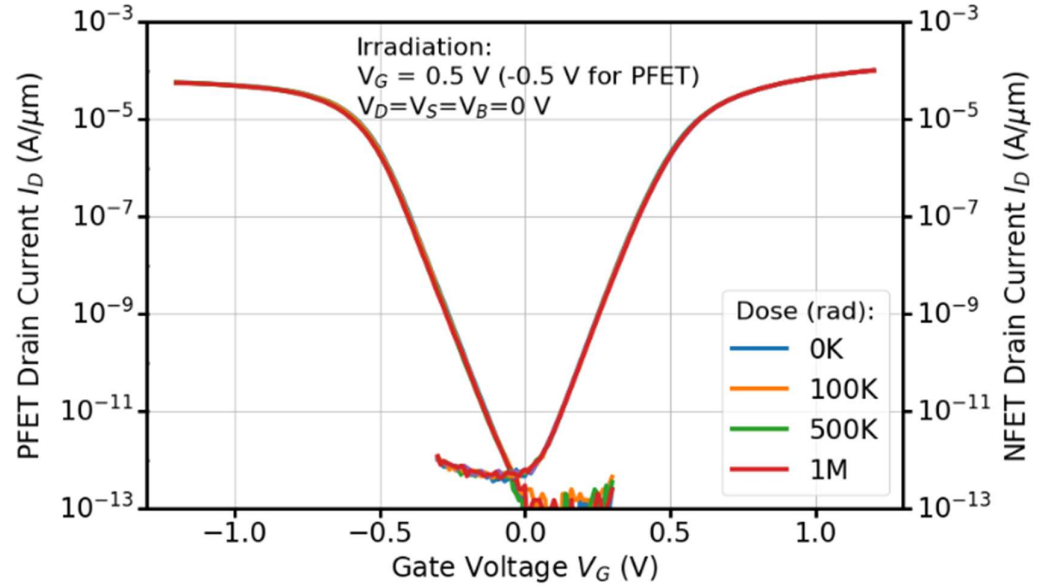
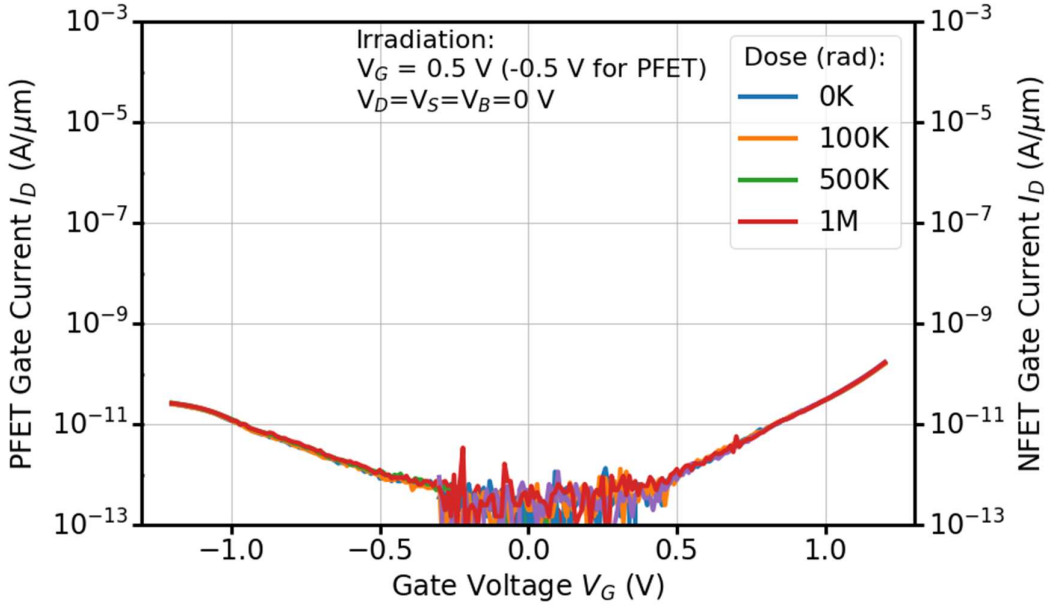


Fig. III-2. *n*FET and *p*FET I_d−V_g characteristics, normalized by NW circumference and the number of NWs, under stresses of $|V_g|$ = 0.5 V applied for biasing times comparable to those required for irradiation. (After [94].)



(a)



(b)

Fig. III-3. (a) Normalized I_d–V_g curves at |Vd|= 50 mV and (b) Ig-Vg curves as functions of dose for nFETs and pFETs irradiated with Vg = +0.5 V up to 1 Mrad(SiO_2). (After [94].)

Fig. III-3 shows the I_d-V_g and I_g-V_g characteristics of GAA NW FETs irradiated with V_g = +0.5 V bias. The drain and gate currents are normalized by the NW circumference and the number of NWs. Only small changes are observed after irradiation and annealing, with insignificant increases in off-state leakage and gate leakage.

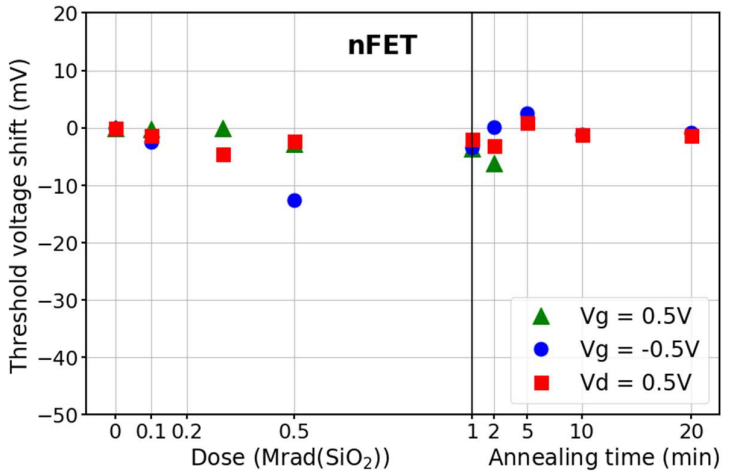
These results demonstrate that the performance of the studied GAA transistors generally is not affected by an increase in subthreshold leakage due to radiation-induced trapped charge in the shallow trench isolation (STI), which is one of the primary causes of degradation in other technologies, i.e., highly-scaled planar MOSFETs and FinFETs [97]–[100]. The remarkable TID tolerance of these devices is most likely associated with the extremely thin gate dielectrics and superior electrostatic gate control over the channel. These factors combine to attenuate TID-induced parametric shifts related to charge buildup in gate oxide and STI, and to suppress potential leakage paths in the Si under the NW [96].

Figs. Fig. III-4 and Fig. III-5 show threshold voltage shifts ΔV_{th}, normalized peak transconductance $g_{m\text{-}max}$, and shifts in subthreshold slope *SS* as functions of total dose and annealing time under three bias conditions for GAA NW *n*FETs and *p*FETs, respectively.

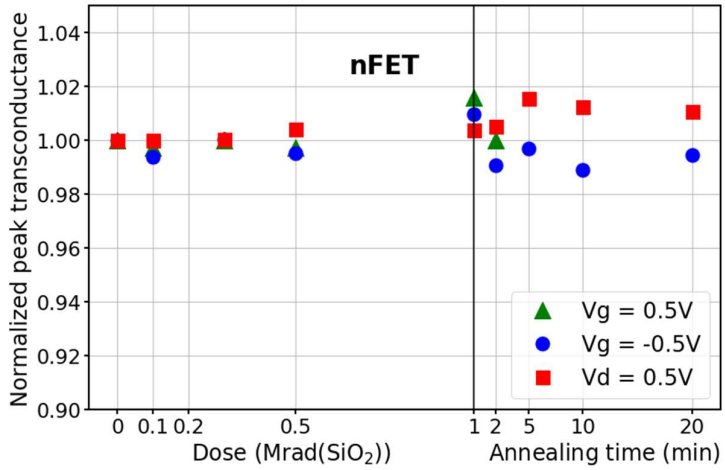
Devices were irradiated up to 1 Mrad(SiO_2) and annealed at room temperature for 20 min. Both *n*- and *p*-channel FETs exhibit V_{th} shifts less than 20 mV for all tested bias conditions (see Figs. Fig. III-4(a) and Fig. III-5(a)). The TID-induced degradation for different bias conditions is comparable, in contrast to some previous work showing significant bias-dependent differences in results for devices with HfO_2-based dielectrics [18], [70], [101], [102]. This difference in response is due most likely to the thinner dielectric layers, differences in device geometries, and/or modest range of biases employed in this work, ± 0.5 V, compared with many previous studies [18], [70], [101], [102]. The variation of the normalized peak transconductance is ±2% for *n*FETs and ±4% for *p*FETs, as shown in Figs. Fig. III-4(b) and Fig. III-5(b). The slight changes in g_{m_max} and the similarly small changes in *SS* in Figs. Fig. III-4(c) and Fig. III-5(c) also suggest minimal buildup of radiation-induced interface and border traps [6], [70], [97], [102] due to: (1) high quality interfaces in as-processed devices [95], (2) strong electrostatic control over the channel provided by the GAA structure, and (3) the extremely thin gate oxides.

3.4 Conclusions

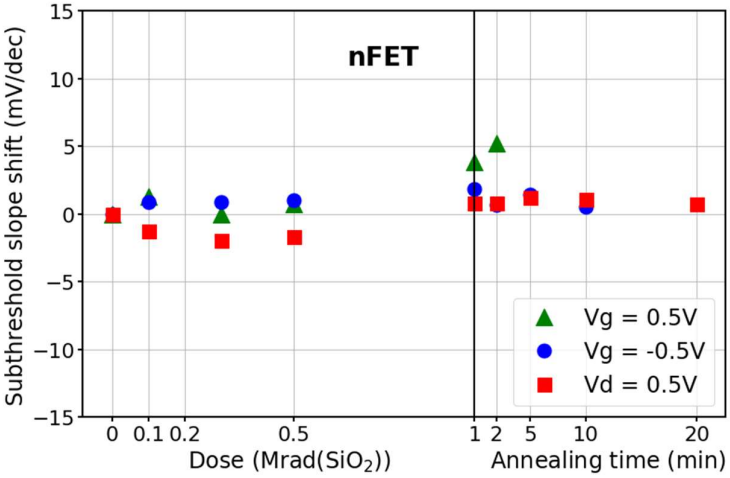
Vertically stacked bulk GAA Si-NW *n*-channel and *p*-channel FETs show outstanding radiation tolerance relative to that of other highly scaled devices [46], [97], [102]–[104]. Irradiated GAA transistors show low sensitivity to TID due to the excellent electrostatic gate control over the channel and the effective suppression of the radiation-induced drain-to-source leakage path.



(a)

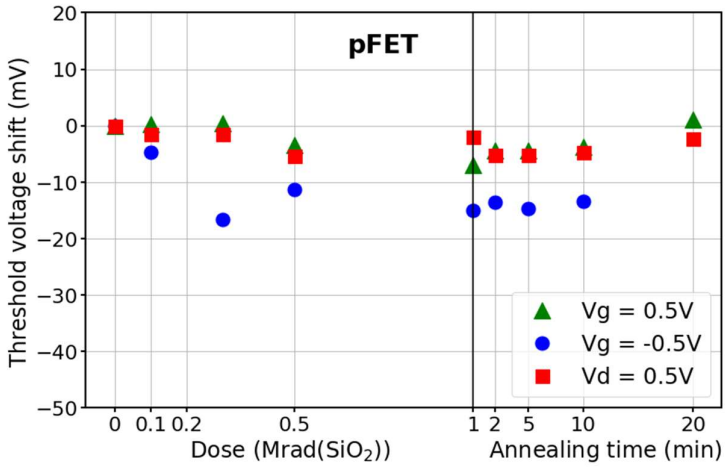


(b)

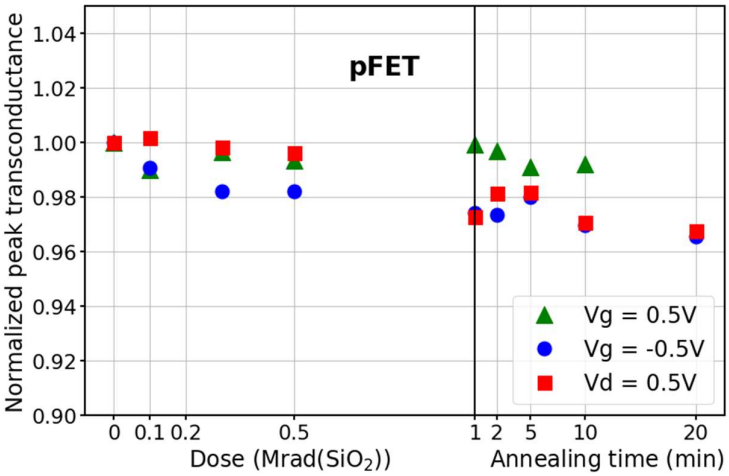


(c)

Fig. III-4. Radiation-induced (a) V_{th} shifts, (b) normalized peak transconductance, and (c) change in subthreshold slope as functions of total dose for different bias conditions during irradiation of GAA NW *n*FETs. The vertical lines indicate the beginning of the annealing test. (After [94].)



(a)



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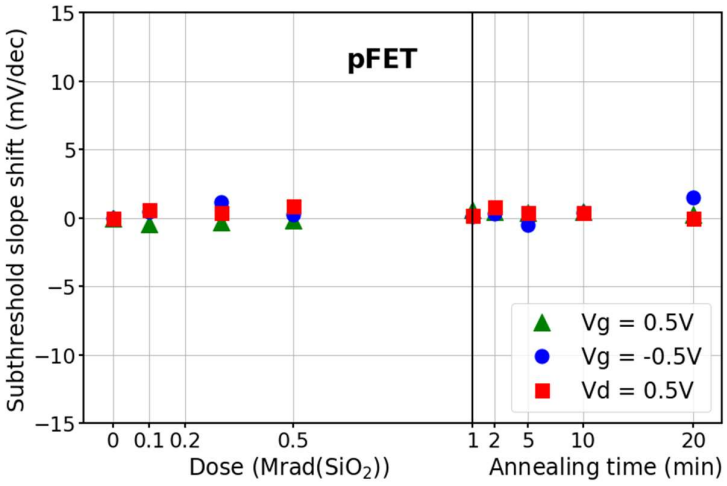


(c)

Fig. III-5. Radiation-induced (a) V_{th} shifts and (b) normalized peak transconductance, and (c) changes in subthreshold slope as functions of total dose for different bias conditions during irradiation of GAA NW *p*FETs. The bold vertical lines indicate the beginning of the annealing test. (After [94].)

One of the significant advantages of the studied GAA devices is that *p*-channel transistors demonstrate comparable TID response to *n*-channel counterparts over the range of examined doses and bias conditions. The similarity in responses enables simplified integrated circuit design, and the overall excellent radiation tolerance of *n*MOS and *p*MOS devices makes the GAA NW FETs promising candidates for future CMOS applications in space electronics requiring high radiation tolerance together with high performance.

CHAPTER IV

1/*f* NOISE AND RANDOM TELEGRAPH NOISE IN GATE ALL-AROUND DEVICES

This chapter is adapted from "Total-Ionizing-Dose Response of Highly-Scaled Gate-All-Around Si Nanowire CMOS Transistors" published in IEEE Transactions on Nuclear Science and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Pan Wang, Stefano Bonaldo, Ronald D. Schrimpf, Fellow, IEEE, Robert A. Reed, Dimitri Linten, Jerome Mitard, and Daniel M. Fleetwood.
Reference:

- M. Gorchichko *et al.*, "Total-ionizing-dose response of highly scaled gate-all-around Si nanowire CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 687–696, May 2021.

Low-frequency noise in GAA FETs has been a topic of great interest in recent years since nanowire transistors became known as the best possible candidate for highly-scaled CMOS technologies [105]. However, a scarce amount of research focused on the effects of TID irradiation on 1/*f* noise in GAA FETs [106]. In Chapter IV, we present low-frequency noise and random telegraph noise results for GAA FETs to provide insight into defects in these devices. Prominent traps are observed before and after irradiation; these are most likely due to oxygen vacancies and/or hydrogen complexes. The RTN is due to traps located in both the SiO_2 and HfO_2 dielectrics, with significant variations in capture and emission times over the range of voltages explored. These results confirm the increasing importance of RTN for highly-scaled nanowire devices.

4.1 Experimental Setup

4.1.1 Low-Frequency Noise and Random Telegraph Noise Measurements

The noise power spectral density S_{Vd}, with correction for background noise, was measured at ~ 295 K over a frequency f range from 1 Hz to 390 Hz unless otherwise stated. During noise measurements, the drain voltage V_d was held at 0.05 V with a source and substrate grounded. The gate-to-threshold voltage V_{gt} was varied from 0.2 V to 0.6 V. Temperature dependence of low-frequency noise was measured in the temperature range from 80K to 320K. For the low-frequency noise testing in a wide temperature range, a mounted device was placed into Janis VPF-100 Cryostat in a low-pressure environment. The schematic diagram of the low-frequency noise setup is shown in Fig. II-4. Random telegraph noise (RTN) measurements

were performed at room temperature with Keithley 4200-SCS Parameter Analyzer at the same bias conditions as *1/f* noise measurements.

4.2 Experimental Results

4.2.1 Low-Frequency Noise at Room-Temperature

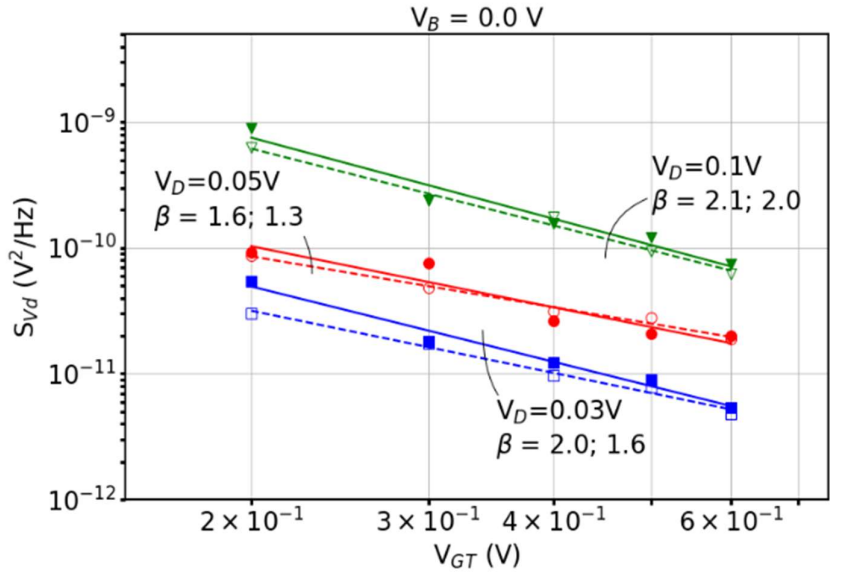
Low-frequency noise analysis is a well-known method to characterize the densities and energy distributions of border traps in semiconductor devices [10], [15], [18], [64], [71], [107], [108]. It has been found to be helpful in providing insight into process- and radiation-induced defects [10], [17], [45], [74]. To first order, the low-frequency noise of MOS devices can be described via a simple number-fluctuation model that assumes tunnel-assisted charge exchange between the channel Si and defects in the near-interfacial gate oxide [10], [15], [18], [21], [22], [63], [73]. Within the framework of this model, the excess drain-voltage noise power spectral density, S_{Vd}, is described via:

$$S_{V_d} = \frac{q^2}{C_{ox}^2} \frac{V_d^2}{(V_g - V_{th})^2} \frac{kTD_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f}. \quad \text{IV-1}$$

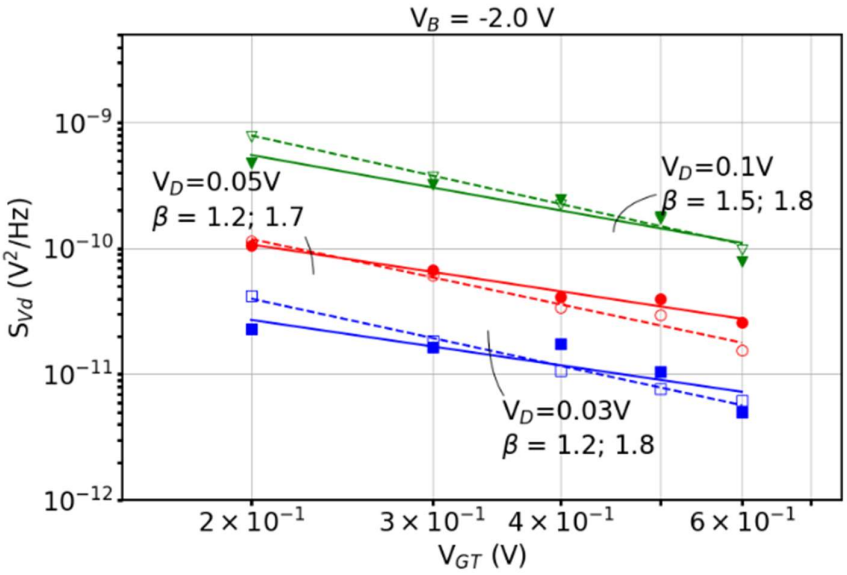
Here V_{th}, V_g, and V_d are the threshold, gate, and drain voltages, C_{ox} is the gate oxide capacitance per unit area, L and W are the transistor channel length and width, $D_t(E_f)$ is the number of traps per unit area at the Fermi level E_f, T is the absolute temperature, k is the Boltzmann constant, f is the frequency and τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [15], [21], [22], [63], [73], [74]. The gate-voltage dependence $\beta = \partial \ln S_{Vd}/\partial \ln |V_g\text{-}V_{th}|$ of the noise is an indicator of the degree of uniformity of $D_t(E_f)$ [15], [21], [22], [63], [73], [74]. Value of $\beta \approx 2$ correspond to an approximately uniform distribution of effective border-trap energies throughout the Si bandgap [15], [21], [74]. Values of $\beta < 2$ denote an energy distribution increasing toward the conduction (valence) band edge for *n*MOS (*p*MOS) transistors, and values of $\beta > 2$ denote a distribution increasing toward midgap [15], [18], [21], [74].

Fig. IV-1 shows the gate-to-threshold voltage dependence $V_{gt} = |V_g\text{-}V_{th}|$ of S_{Vd} for as-processed and irradiated GAA NW *n*FETs at $f = 10$ Hz and $V_d = 30$ mV, 50 mV, and 100 mV. Noise measurements were performed at room temperature with (a) the body terminal grounded and (b) an applied body potential $V_b = -2$ V. At fixed gate-to-threshold voltage the ratio S_{Vd}/V_d^2 is generally constant, consistent with expectations for noise due to number fluctuations [10], [15], [22], [63], [73]. Dashed lines and open symbols denote devices irradiated to 1 Mrad(SiO_2) and annealed for 20 min with $V_g = +0.5$ V. Values of gate-voltage dependence

$\beta = \partial \ln S_{Vd}/\partial \ln |V_g\text{-}V_{th}|$ are shown for each value of V_d. The first values are for as-processed devices, and the second values are for irradiated devices. Results show that the magnitude of the room-temperature low-frequency noise is affected minimally by irradiation and/or applied body potential during measurement.

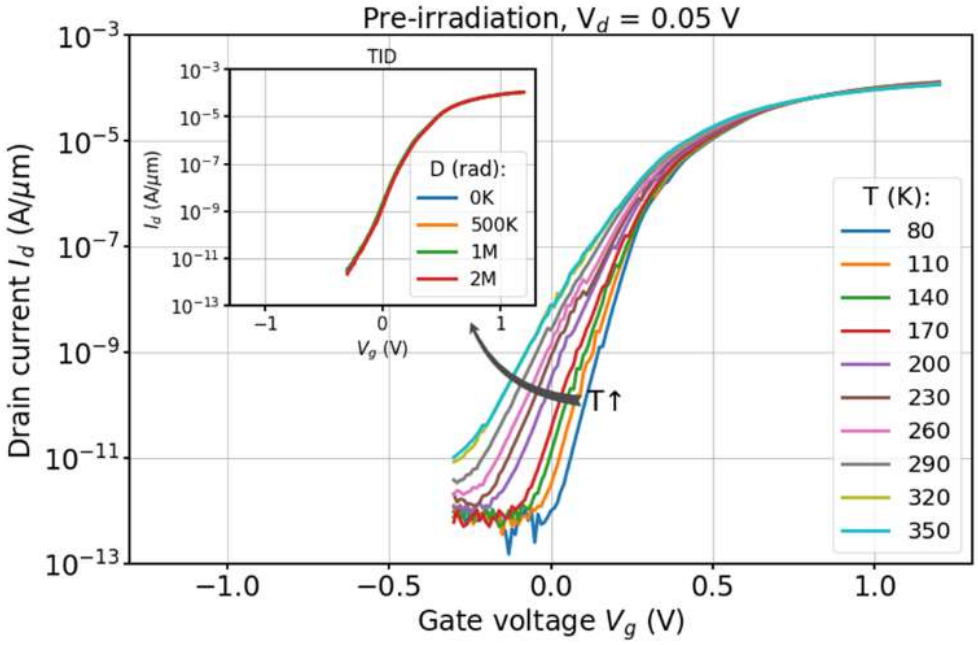


(a)

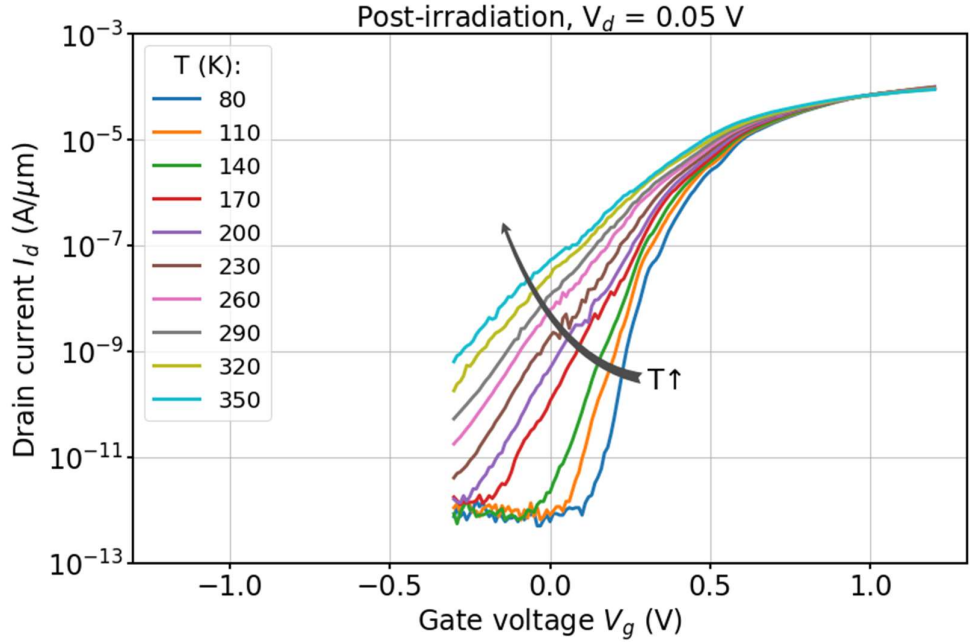


(b)

Fig. IV-1. Gate-voltage dependence of S_{Vd} at V_d = 30 mV (blue), 50 mV (red), and 100 mV (green) for as-processed (closed symbols, solid lines) and irradiated (open symbols, dashed lines) GAA NW *n*FETs. The device was irradiated to 1 Mrad(SiO_2) at V_g = +0.5 V. The body terminals during the noise measurements were biased at (a) V_b = 0 V and (b) V_b = -2 V. (After [94].)



(a)



(b)

Fig. IV-2. I_d−V_g curves vs. temperature (a) before and (b) after irradiation in the range T = 80-350 K. The device was irradiated to 2 Mrad(SiO_2) at V_g = +0.5 V and annealed for 1 h under the same bias condition. Inset: I_d−V_g curves show relative stability during. (After [94].)

In Fig. IV-1(a), values of β are close to 2 for as-processed devices with V_b = 0 V. The noise in this case may include effects of defects in the sub-channel region (Fig. III-1). The potential impact of traps in the sub-channel region is decreased when negative bias is applied

to body terminal, as shown in Fig. IV-1(b). For this case, noise magnitudes are similar but values of β are generally less than 2 for as-processed devices. This reduction in β reflects an effective defect-energy distribution that is increasing towards the conduction band edge [15], [21], [74]. Variations in β with applied drain bias, e.g., for V_d = 50 mV in Fig. II-6(a), are due primarily to the presence of random telegraph noise [15], [18], as discussed in detail below.

4.2.2 Low-Frequency Noise and RTN vs. Temperature

Fig. IV-2 depicts I_d–V_g curves versus temperature (a) before exposure and (b) after irradiation to 2 Mrad(SiO_2). Devices were annealed for 1 h at room temperature at V_g = +0.5 V. Irradiated devices exhibit more significant stretch-out for temperatures higher than 140 K due to the activation of radiation-induced interface [109] and border traps [15], [70]. The device in Fig. IV-2 is affected significantly by random telegraph noise (RTN), as evidenced by changes in V_{th}, changes in slopes of the subthreshold I_d-V_g curves, and changes in frequency dependence of S_{Vd} [23], [31], [77]–[79], each of which is discussed in detail below.

Fig. IV-3 shows V_{th} as a function of temperature for the as-processed and irradiated devices of Fig. IV-2. The significant differences in values of V_{th} before and after irradiation and noise measurement are caused by random activation and passivation of individual, prominent defects during the experimental sequence. These defects are more stable than those leading to RTN and low-frequency noise in these devices [23], [31], [78], [79]. The inset of Fig. IV-3 shows that the as-processed device exhibited a relatively low defect density. During or after room-temperature noise measurement, a prominent defect was activated, leading to a subthreshold "bump" in the voltage range V_g = 0.2 V-0.4 V (Fig. IV-3, orange dashed curve, inset) and a ~8 mV decrease in V_{th}. During the temperature-dependent noise measurements of Fig. IV-2(a), a second individual fluctuator became activated, leading to an additional increase in subthreshold leakage in the range V_g = 0.0 V-0.3 V (Fig. IV-3, green dotted curve, inset), and a similar increase in gate leakage (not shown). This second defect was evidently passivated after the noise measurement of Fig. IV-2(a) and before the irradiation test (Fig. IV-3, red dash-dot curve, inset, and Fig. IV-4).

Minimal changes are observed in the I_d-V_g curves that were measured during and after irradiation and annealing for these devices (insets of Fig. IV-2(a) and Fig. IV-3). However, another prominent defect was activated before post-irradiation temperature-dependent noise measurement, which increased the subthreshold leakage significantly in the range V_g = 0.0 V-0.3 V, increased the gate leakage similarly (not shown), and increased V_{th} by

~ 20 mV (brown dash-dot curve, Fig. IV-3, inset). Hence, the combined effects of these relatively stable individual fluctuators account for the majority of the differences in subthreshold stretchout and values of V_{th} for the pre- and post-irradiation curves in Fig. IV-2 and Fig. IV-3. The relative stability of these defects is similar to that observed for the defects leading to stress-induced leakage current (SILC) in MOS devices, which have been linked to similar changes in subthreshold leakage current and V_{th} in previous studies, e.g., O vacancies and their complexes with hydrogen [14], [15], [18], [110]–[113].

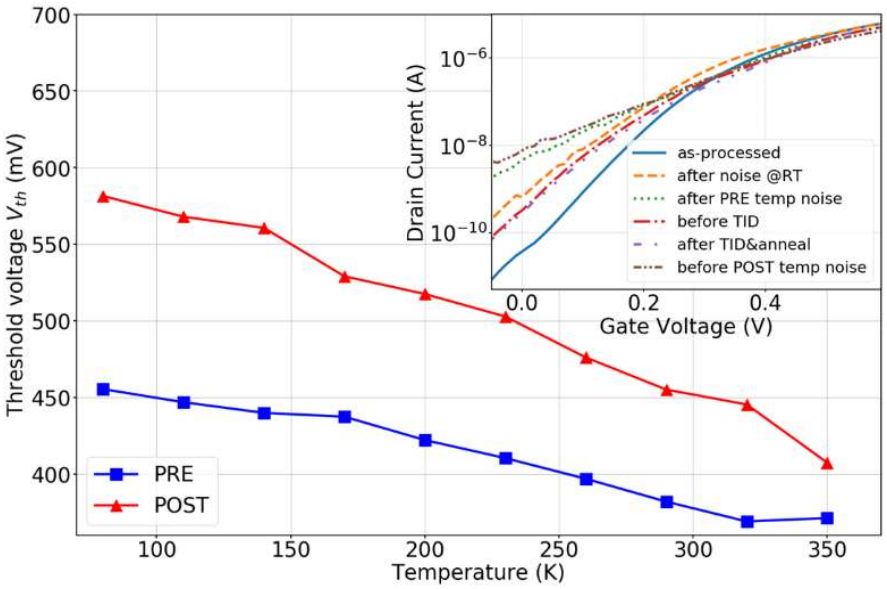
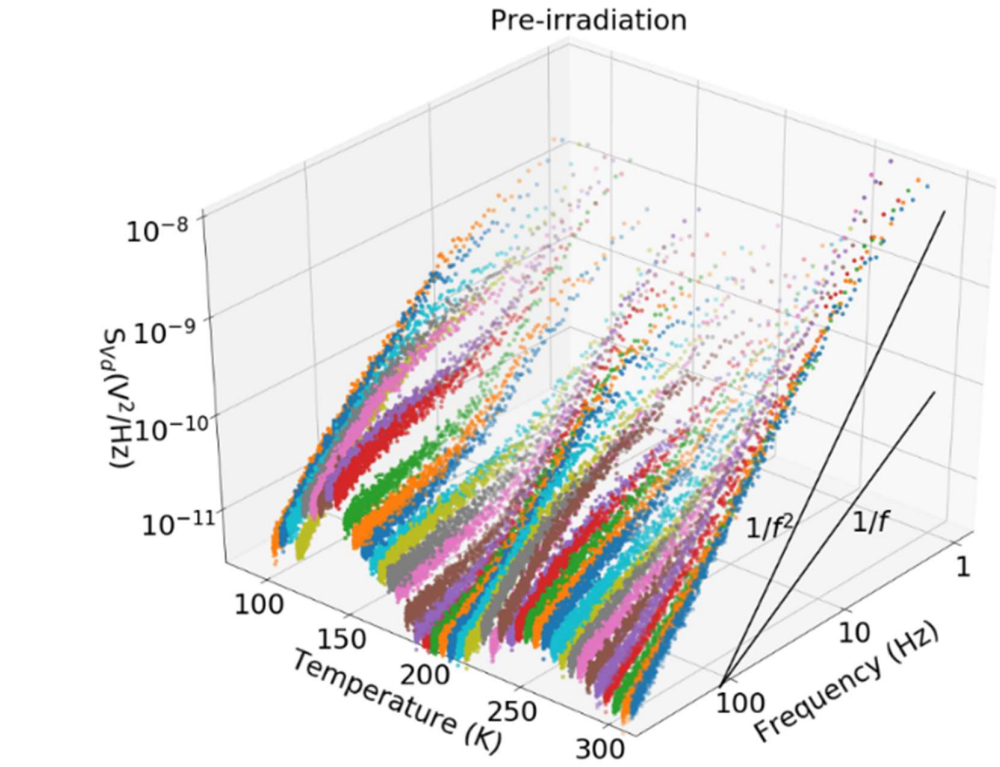


Fig. IV-3. V_{th} vs. T for nFETs before and after irradiation for the device of Fig. IV-2. Inset: I_d-V_g curves during the experimental sequence, showing the longer-term effects of prominent charged defects on V_{th} for the post-irradiation devices. (After [94].)

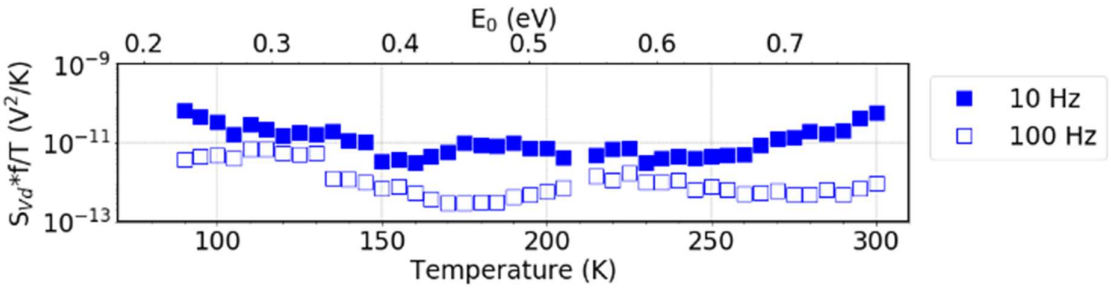
To obtain additional information about the defects in these devices, Fig. IV-4 Fig. IV-6 show S_{Vd} for the as-processed and irradiated GAA NW nFETs of Fig. IV-2 and Fig. IV-3, respectively. Consider first the as-processed devices in Fig. IV-4(a). As the temperature increases from 80 K to 300 K, S_{Vd} switches between primarily Lorentzian and 1/f shapes. Zoomed-in values for individual spectra at 90 K, 250 K, and 300 K are shown in Fig. IV-6(a). Several prominent individual fluctuators can be identified in Fig. IV-4(a) and Fig. IV-6(a) for the as-processed device. The first defect is active at temperatures below ~165 K (e.g., blue circles in Fig. IV-6(a)). The value of f_c for this defect ranges from ~20 Hz at ~90 K to above 400 Hz at ~165 K. This is consistent with more rapid changes in defect charge state as the device is heated [23], [31]. The effects of this defect on values of S_{Vd} are shown clearly at

f = 10 Hz and f = 100 Hz in Fig. IV-4(b). A second prominent fluctuator becomes active with f_c ~4 Hz at ~175 K. Again, the value of f_c increases with increasing temperature, reaching ~400 Hz at ~240 K. A third defect appears above ~265 K in Fig. IV-4(a) and Fig. IV-6(a), switching at rates less than a few Hz.

The energy scales on the upper x-axis in Fig. IV-4(b) and Fig. IV-5(b) are derived from the Dutta-Horn model of 1/f noise, shown to be consistent with the kinetics of a broad range of defect phenomena in microelectronic materials and devices [14], [15], [22], [64].



(a)



(b)

Fig. IV-4. (a) Frequency and temperature dependences of S_{Vd} in the ranges f = 1 Hz to 400 Hz and T = 90 K to 300 K, and (b) temperature dependence of normalized S_{Vd} at f = 10 Hz and f = 100 Hz of as-processed GAA NW nFETs. Noise measurements were performed at V_{gt} = 0.4 V and V_d = 50 mV. (After [94].)

Fig. IV-5(a) shows frequency and temperature dependences of S_{Vd} for GAA NW *n*FETs irradiated to 2 Mrad(SiO_2) and annealed for 1 h at V_g = +0.5 V. Zoomed-in values for individual spectra at 90 K, 250 K, and 300 K are shown in Fig. IV-6(b). At temperatures 80 K - 120 K, effects of a prominent fluctuator are observed intermittently (e.g., blue dots in Fig. IV-5(b)). At 120 K this defect becomes more predictably active, with a characteristic frequency that increases from ~5 Hz at 120 K to ~400 Hz at 200 K. No prominent individual

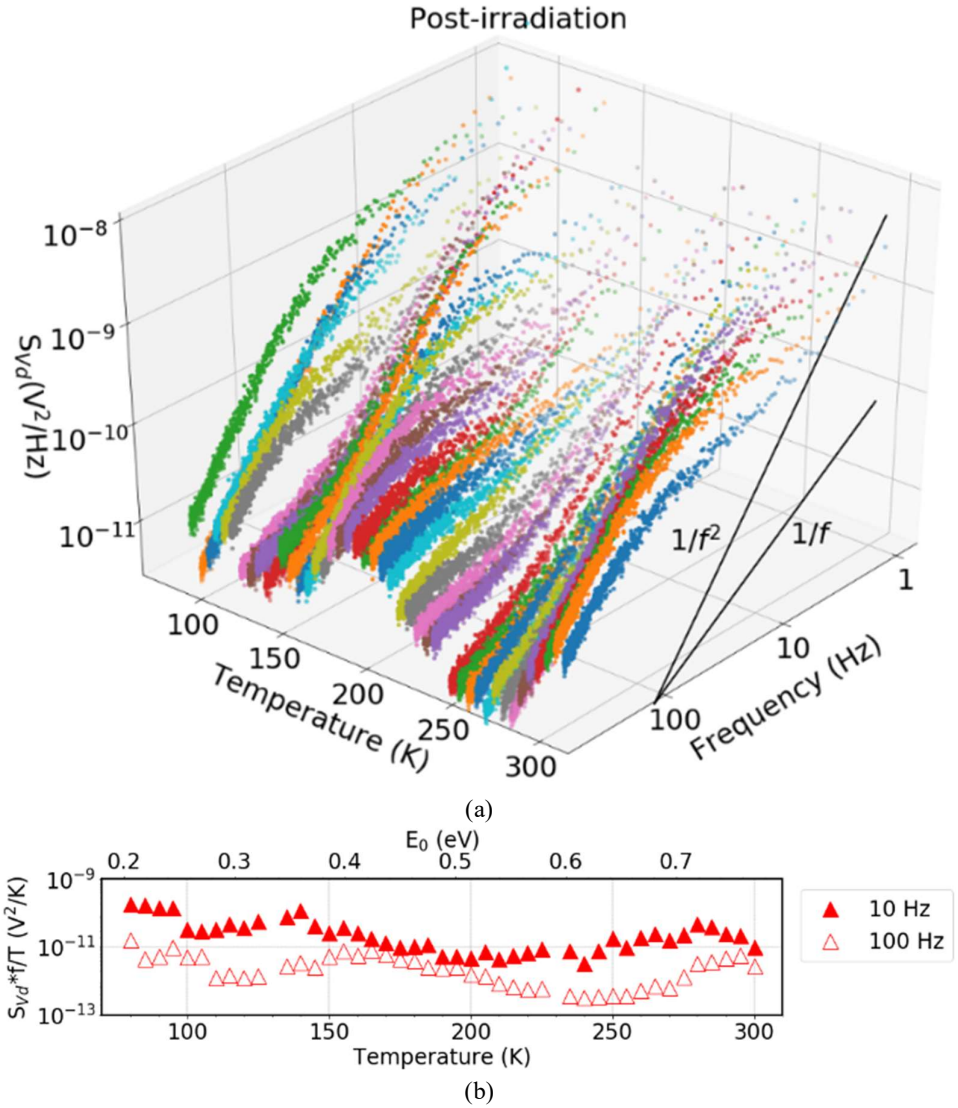
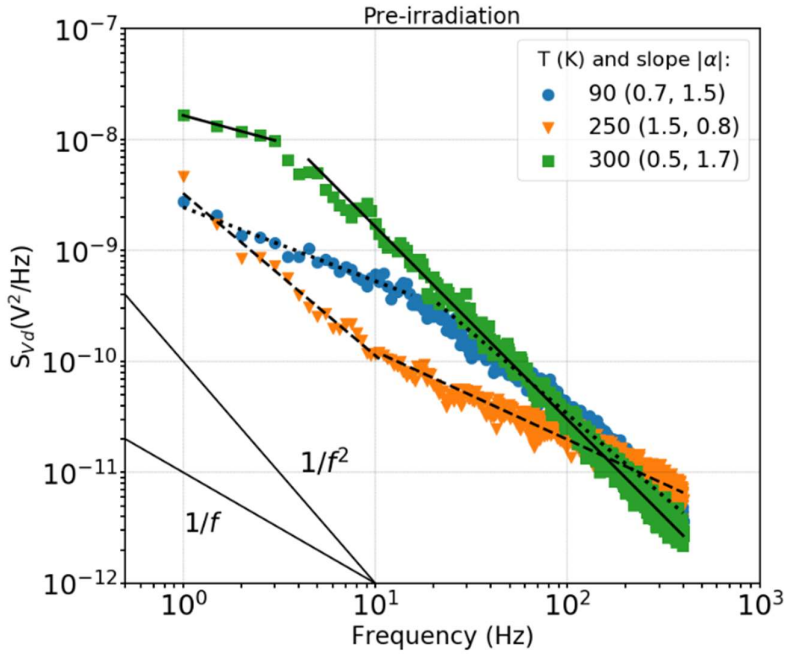
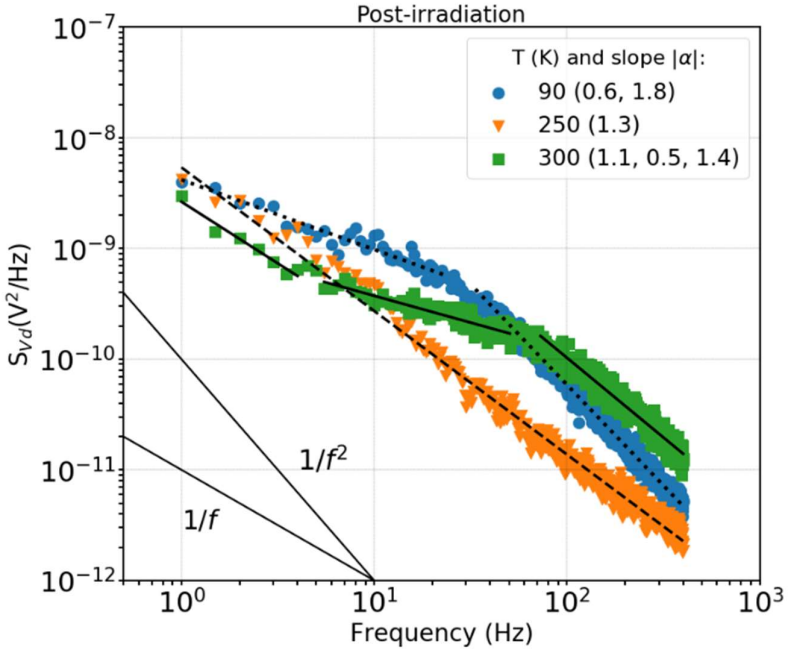


Fig. IV-5. (a) Frequency and temperature dependences of S_{Vd} in the ranges f = 1 Hz to 400 Hz and T = 80 K to 300 K and (b) temperature dependence of normalized S_{Vd} at f = 10 Hz and f = 100 Hz for GAA NW *n*FETs irradiated to 2 Mrad(SiO_2) and annealed for 1 h at V_g = +0.5 V. Noise measurements were performed at V_{gt} = 0.4 V and V_d = 50 mV. (After [94].)



(a)



(b)

Fig. IV-6. Selected temperature dependences of S_{Vd} (a) before and (b) after irradiation of the device of Fig. IV-4 Fig. IV-5. Noise measurements were performed at $V_{gt} = 0.4$ V and $V_d = 50$ mV. Values of slope, α, are shown in the legend. (After [94].)

fluctators are observed between 200 K and 255 K. Another prominent fluctuator becomes active with $f_c \sim 9$ Hz at ~260 K (e.g., green squares in Fig. IV-6(b)), increasing to ~100 Hz

at 300 K. Comparing Fig. IV-4(b) and Fig. IV-5(b), noise magnitudes are generally similar in magnitude, but the defect-energy distribution is perturbed significantly by irradiation and/or temperature cycling. While these types of changes are not unusual for irradiated MOS devices [14], [15], [87], their impacts are greatly magnified in devices with nanoscale dimensions [14], [23], [31], [75], [78], [79], [111]–[113]. The width and broadening of the noise peaks observed in Fig. IV-4(b) and Fig. IV-5(b) suggest that these traps are associated with a distribution of defects, again most likely oxygen vacancies and/or hydrogen complexes, demonstrated to be significant issues for the reliability and radiation response of $Si/SiO_2/HfO_2$ systems [15], [18], [70], [100], [17], [21], [76], [114]–[120].

4.3 RTN Analysis of As-Processed Devices

Fig. IV-7 and Fig. IV-8 provide further insight into the defects causing RTN in as-processed devices. The gate-to-threshold voltage dependence of the drain current is shown in the time domain in Fig. IV-7. Prominent individual defects are observed in all cases, with especially large numbers of switching events observed for V_{gt} = 0.2 V and 0.3 V.

Fig. IV-8 shows weighted time lag plots [80], [121] for the current traces of Fig. IV-7. The histograms on the tops and right-hand sides of the plots show relative distributions of I_d values. The diagonals of the time lag plots represent stable current states, and off-diagonal values represent charge trapping and emission events.

Weighted lag plots provide a convenient visualization of the effects of prominent defects on channel conduction [80]. Fig. IV-8(a) shows symmetric distributions that are fairly typical of classical 1/*f* noise [22], [80], [121]. The multiple stable current states in Fig. IV-8(b), (d), and (f) indicate the presence of prominent individual fluctuators [80], [121], [122]. In Fig. IV-8(c) and (e), prominent individual trap levels are not readily apparent, but the deviations from Gaussian shapes of the histograms indicate the presence of less prominent traps with more closely located I_d levels than those active in Fig. IV-8(b), (d) and (f).

To further investigate RTN, time-domain data were analyzed using a hidden Markov model (HMM) [80], [121], [123]–[125]. The Baum-Welch algorithm [126] was used to optimize model parameters. The Viterbi algorithm [127] was used to obtain the most likely trap states [121], [125]. The optimum number of traps was estimated using Bayesian information criteria [128]. The location of the identified traps, relative to the channel, was attained using the following relationship, based on a simple tunneling model of the noise [129]:

$$\frac{x}{T_{ox}} = -\frac{kT}{q}\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_G}. \qquad \text{IV-2}$$

Here x is the distance between the trap location and the Si/SiO_2 interface, and T_{ox} is the oxide thickness. The channel in these GAA NW FETs is surrounded by ~1 nm interfacial SiO_2, upon which a 1.8 nm HfO_2 layer is deposited.

Fig. IV-9 shows τ_e/τ_c ratios for clusters of traps estimated by HMM over the range of values of V_{gt}. At least four prominent traps (labeled 1-4) are active fluctuators at multiple voltages. The distance from the channel calculated using Eq. IV-2 is noted for each of the four

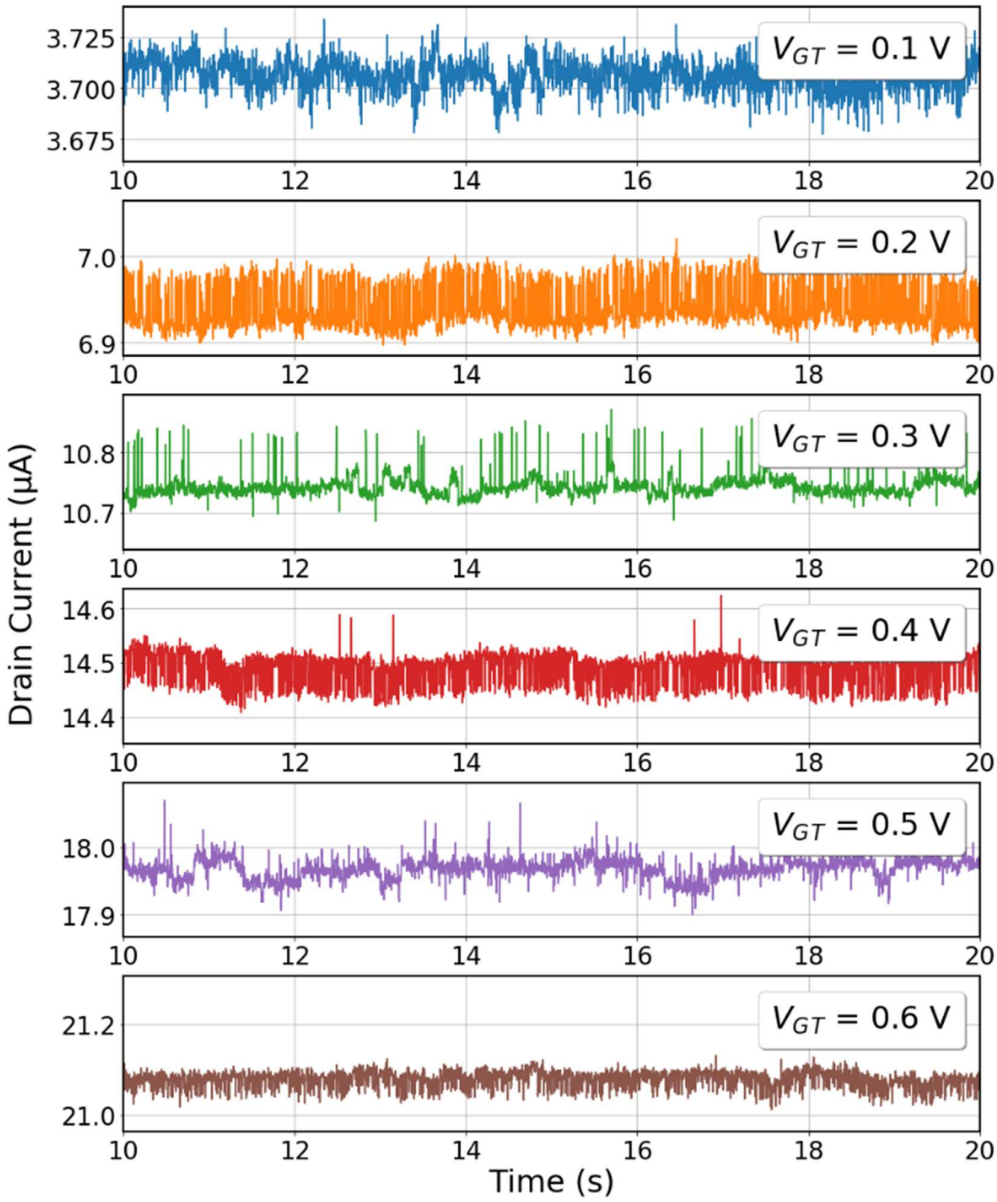


Fig. IV-7. Examples of gate-to-threshold voltage dependence of drain current I_d of a GAA NW *n*FET. Measurements were performed at V_d = 50 mV. (After [94].)

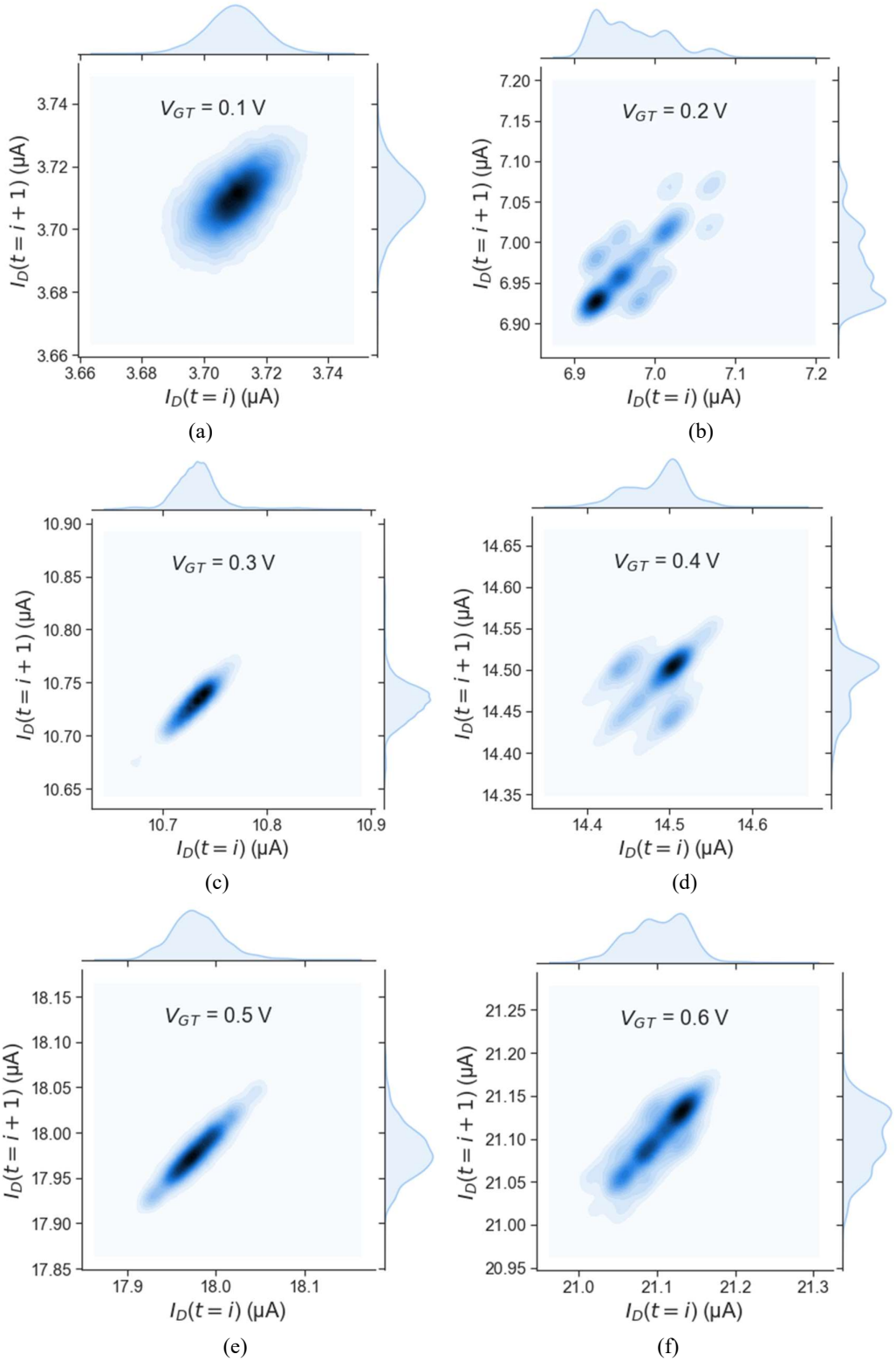


Fig. IV-8. Weighted time lag plots showing stable current states on the diagonals and amplitude histograms (top, right) derived from time-domain signals for un-irradiated devices with values of V_{gt} ranging from 0.1 V to 0.6 V. (After [94].)

traps. Two of the four identified traps are inferred to be border traps in the interfacial SiO_2. The other two are relatively deep traps near the SiO_2/HfO_2 interface or in the HfO_2 layer. For a number of traps (circles), we were unable to obtain similar information due to time and voltage resolution limitations of the experiments. Again, these defects are most likely associated with O vacancies and their complexes with hydrogen [15], [18], [14], [110]–[113], [114]–[120].

4.4 Summary and Conclusions

Prominent defects that are most likely associated with oxygen vacancies and/or hydrogen complexes are observed via low-frequency noise measurements of irradiated devices. The observed RTN is due to traps located in both the SiO_2 and HfO_2 dielectrics, with significant variations in capture and emission times over the range of voltages explored. These results indicate that defects in these devices are distributed non-uniformly in energy and space and confirm the increasing importance of RTN for highly-scaled devices. These defects can strongly affect device performance and reliability [31], [70], [78], [130], [131], which can be manifested on a circuit level by RTN-induced cell leakage and logic delay fluctuations in

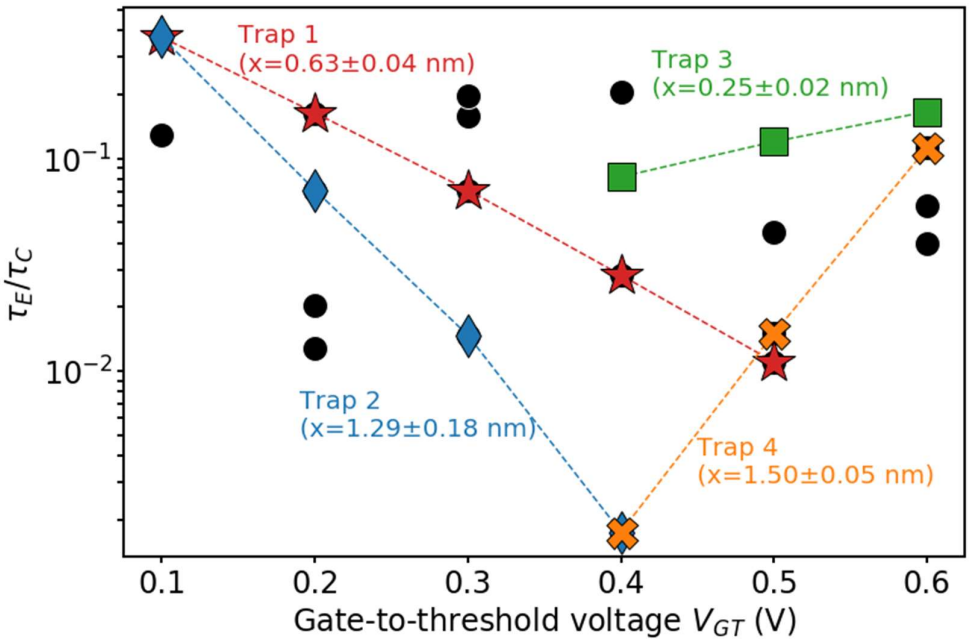


Fig. IV-9. Extracted ratios between emission time and capture time as a function of gate-to-threshold voltage V_{gt} = from 0.1 V to 0.6 V. Four individual traps (1-4) were identified, and positions x in the gate stack measured with respect to Si/SiO_2 interface were estimated during Eq. IV-2 of the text. (After [94].)

digital logic cells, jitter in memory cells, and frequency variability, e.g. in ring oscillators, especially under low voltage operation [132]–[134]. The devices likely would benefit from reduction of interface and border-trap densities by optimizing processing steps for the high-k gate stack, e.g., mitigating fin oxidation by reducing the STI thermal budget [39].

CHAPTER V

CHARGE TRAP TRANSISTORS

This chapter is adapted from "Low-Frequency and Random Telegraph Noise in 14-nm Bulk Si Charge-Trap Transistors" submitted to IEEE Transactions on Electron Devices and has been reproduced with the permission of the publisher and my co-authors En Xia Zhang, Mahmud Reaz, Kan Li, Peng Fei Wang, Jingchen Cao, Rachel M. Brewer, Ronald D. Schrimpf, Robert A. Reed, Brian D. Sierawski, Michael L. Alles, Jonathan Cox, Steven L. Moran, Subramanian S. Iyer, and Daniel M. Fleetwood.
Reference:

- M. Gorchichko *et al.*, "Low-frequency and random telegraph noise in 14-nm bulk Si charge-trap transistors," s*ubmitted to T-ED*, 2021.

5.1 Introduction

Ever-increasing memory demands require new technological solutions. Compact, dense, and reliable memory devices can greatly enhance the performance of electronic systems in space applications. Fabrication costs and system complexity can be reduced by seamlessly integrating memory and logic devices. Charge Trap Transistor (CTT) memories facilitate this objective. CTT can be built as standard logic transistors and programmed and erased via high-field charge injection [52]–[54]. CTTs can achieve large electrically programmable threshold voltages through the population of existing traps in the bulk of the high-k dielectrics and at the interface between the high-k dielectric and the interfacial thermal oxide, as well as through the creation of additional traps during the P/E operations [52]–[55]. An initial evaluation of the TID response of CTTs was performed by Brewer, et al. [55], who found that 14-nm bulk FinFETs are affected less by TID irradiation than 22-nm planar silicon-on-insulator devices [55].

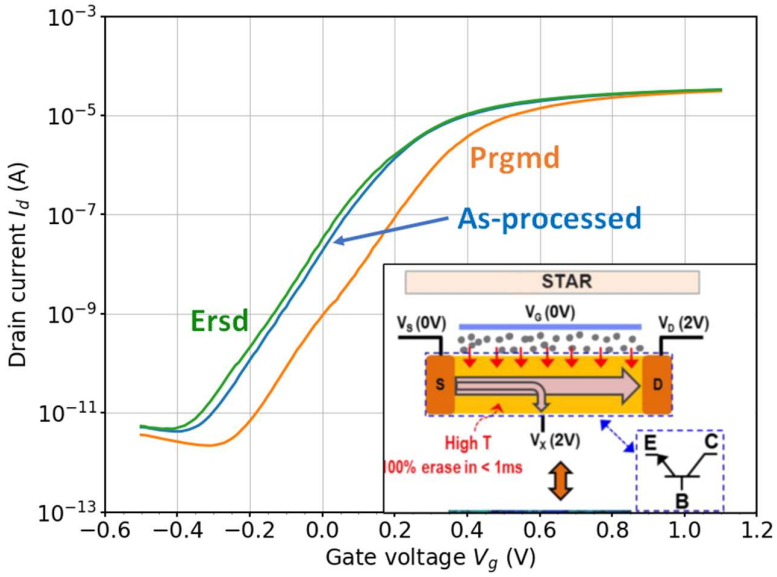
LFN and RTN are practical concerns for scaled multi-level nonvolatile memory devices [135]–[137], and are also useful for investigating the charge trapping properties of microelectronic devices and materials [15], [18], [108]. In this chapter, we present the evaluation the LFN and RTN of as-processed, irradiated, programmed, and erased 14-nm bulk-CMOS CTT FinFETs. Significant RTN is observed in as-processed 2-fin devices, as illustrated via weighted time lag plots as functions of gate voltage. Programming/erasing (P/E) leads to activation/deactivation of prominent individual traps, but underlying, featureless $1/f$ noise magnitudes are not affected significantly. TID increases the uniformity of effective border-trap energy distributions.

5.2 Devices and Methods

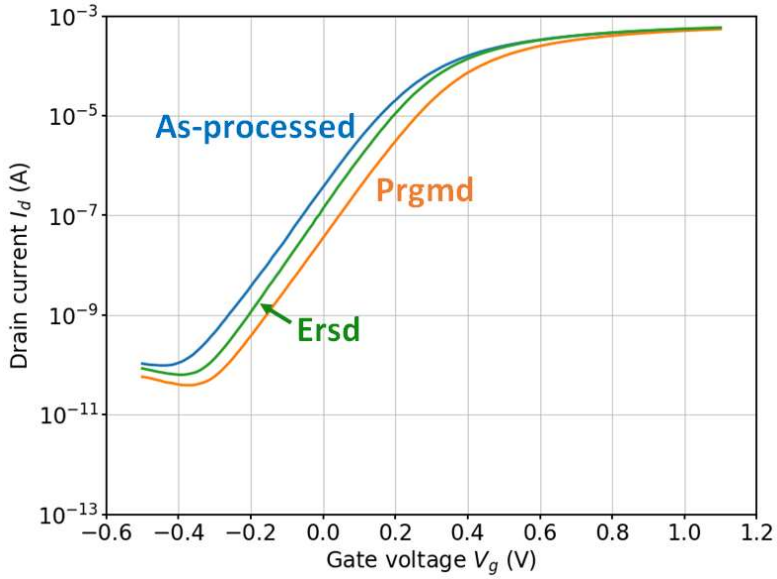
The 14-nm bulk FinFETs in this study were fabricated by GLOBALFOUNDRIES [138]. Applications of these devices as Charge-Trap Transistors (CTT) for multi-programmable non-volatile memory technologies are discussed extensively in [52]–[54], [139], [140]. We have studied devices with 2 and 40 fins with effective widths of 150 nm and 3 μm, respectively. The gate stack consists of (1) high-k gate oxide HfO_2 (EOT ~ 1.3 nm), which serves as charge trapping layer and modulates V_{th} during P/E cycling, (2) barrier work-function metal, and (3) tungsten fill [138].

Devices were mounted in custom high-speed packages [141] and programmed using a Keithley 4200A-SCS Parameter Analyzer by applying a series of 22 total pulses to the gate, ranging from 1.6 V to 2.2 V in increments of 0.2 V, and constant, overlapping 1.2 V pulses to the drain. Each pulse duration is 10 ms. For sensing pulses, following programming or erasing, V_g is 0.6 V and V_d is 0.1 V. The sensing time is 50 ms per cycle [52], [55]. In contrast to [55], where a traditional erase technique with high negative gate bias pulsing was used, devices in this work were erased via the Self-heating Temperature Assisted eRase (STAR) technique [54] (Fig. 1(a), inset); 22 pulses were applied to the bulk terminal, starting at $V_b = 1.6$ V and increasing in magnitude until $V_b = 2.2$ V, and constant, synchronized 1.2 V pulses to the drain.

Devices were irradiated at room temperature with ~ 10-keV X-rays [6] at a rate of 30.3 krad(SiO_2)/min to 500 krad(SiO_2) at $V_g = +0.5$ V, with other terminals grounded, and then annealed at the same bias for 30 min at room temperature. DC characteristics were measured at $|V_d| = 50$ mV with an Agilent 4156A/B semiconductor parameter analyzer (PA) at ~295 K. V_{th} was extracted using linear extrapolation; $V_{th} + V_d/2$ is defined as the x-intercept of the linear extrapolation of the $I_d - V_g$ curve at the point of maximum transconductance $g_{m\text{-}max}$ with the V_g-axis [142]. At least two devices of each type were tested under the same conditions; TID responses varied by less than ±10%. The low-frequency noise-power spectral density, S_{Vd}, was measured for packaged devices using the methods and apparatus described in [15], [143] at ~295 K at frequencies from $f = 1$ Hz to 390 Hz, with correction for background noise. Random telegraph noise was measured using a HP4156A PA using a time step of ~ 3 ms. During low-frequency and random telegraph noise measurements, the drain was biased at 50 mV with source and substrate terminals grounded; the gate voltage V_G was varied from 0.1 V to 0.6 V above V_{th}. At least two devices with similar noise responses were at each test condition; representative results are shown below.



(a)



(b)

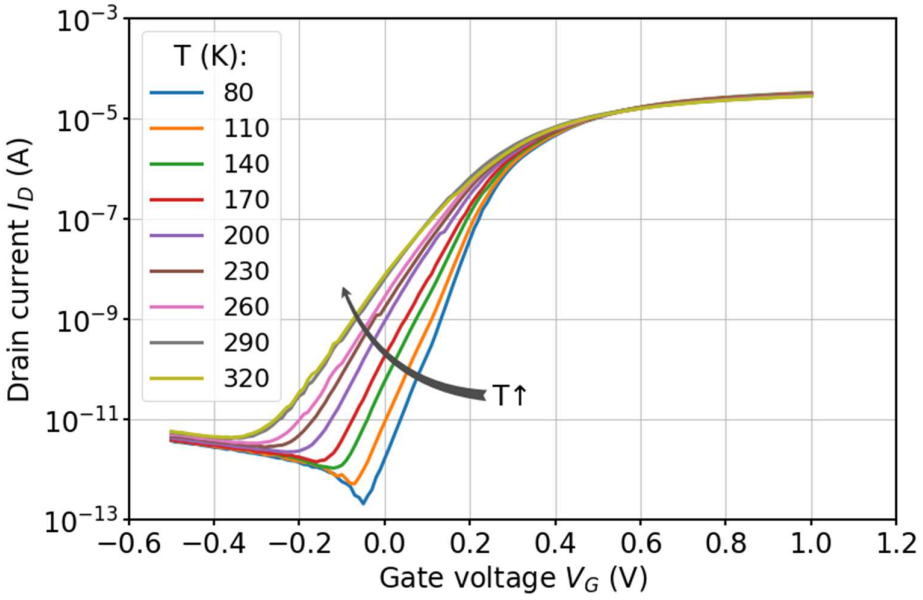
Fig. V-1. I_d–V_g characteristics at $|V_d|$= 50 mV for (a) 2-fin and (b) 40-fin devices as-processed, programmed, and erased using the STAR technique. A schematic illustration of the STAR technique is shown as an inset in (a). (After [144].)

5.3 Results and Discussion

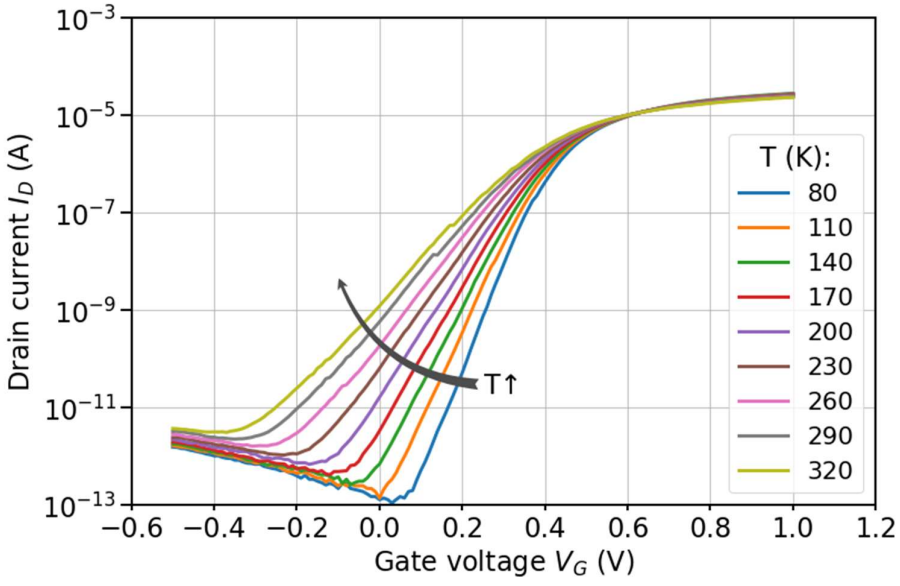
5.3.1 DC response

Fig. V-1 shows typical transfer characteristics of a CTT before and after programming and after erasing for (a) 2-fin and (b) 40-fin devices. V_{th} shifts are caused primarily by electron

trapping [6], [52], [139], [145]. The over-erasure for the 2-fin device most likely results from hole injection via band-to-band tunneling [53], [54], [146]. The 40-fin device shows a smaller memory window (ΔV_{th} = ~100 mV) than the 2-fin device (ΔV_{th} = ~130 mV), likely due to the non-uniform response of fins to programming/erasing [97], [147].

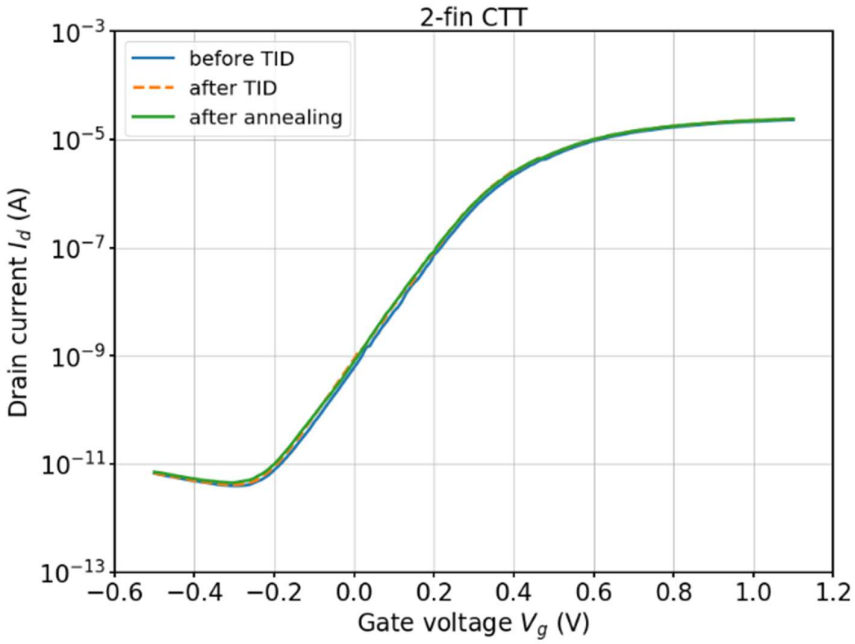


(a)

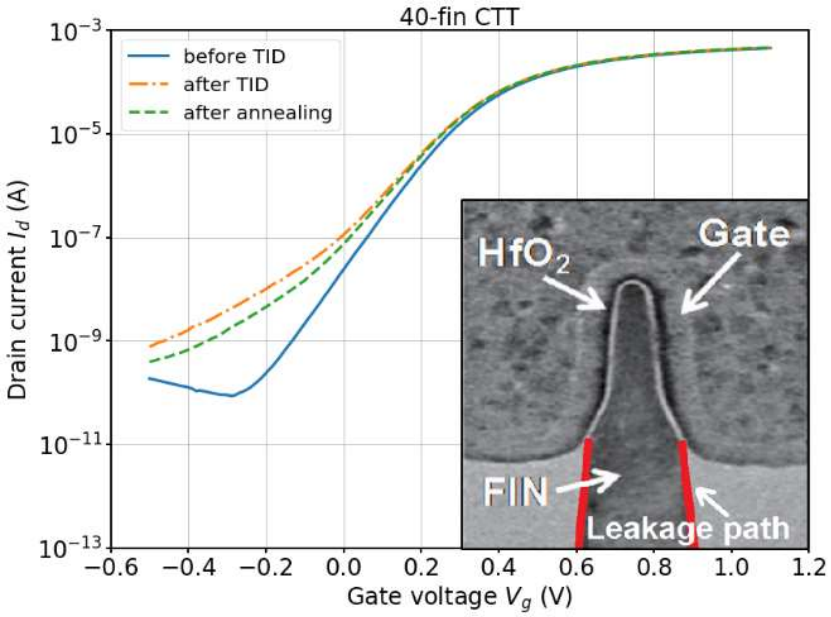


(b)

Fig. V-2. I_d–V_g characteristics vs. temperature (a) before and (b) after programming in the range T = 80-320 K. (After [144].)



(a)



(b)

Fig. V-3. Typical I_d–V_g characteristics at $|V_d|$= 50 mV before irradiation, after irradiation with V_g = +0.5 V up to 500 krad(SiO_2), and after annealing under the same bias for 30 min for (a) 2-fin CTT and (b) 40-fin CTT. Inset: TEM cross-section of 14 nm FinFET CTT perpendicular to the fin direction with denoted location of parasitic leakage paths (adapted from [54]). (After [144].)

Fig. V-2 shows the temperature dependence of I_d–V_g curves for (a) as-processed and (b) programmed 2-fin devices. The stretch-out in the subthreshold region is significantly more

pronounced in the programmed device than in the as-processed device due to activation of a large number of interface traps during programming, consistent with and extending the room-temperature results of Brewer et al. [55].

Fig. V-3 shows $I_d - V_g$ characteristics of programmed (a) 2-fin and (b) 40-fin CTTs before irradiation, after irradiation with V_g = +0.5 V up to 500 krad(SiO_2), and after annealing under the same bias for 30 min. 2-fin CTTs show very small changes due to irradiation, demonstrating an excellent total-ionizing-dose (TID) tolerance. 40-fin CTTs, on the other hand, show a relatively large increase in leakage and stretch-out in the subthreshold region, consistent with the results shown in [55]. This increase in leakage is due to the parasitic radiation-induced leakage path along the Si/SiO_2 interface in the sub-fin region, as shown in the inset of Fig. V-3(b) [19], [97], [147].

5.3.2 Low-Frequency Noise

Low-frequency noise measurements can be used to assess trap distributions and evaluate material/interface characteristics [10], [15], [18], [64], [71], [107], [108]. In semiconductor devices with uniform defect-energy distributions, the excess drain low-frequency noise exhibits an inverse dependence on frequency ($S_{Vd} \sim 1/f$) [15]. This dependence results from the convolution of the individual noise spectra of several traps, where each single trap has a Lorentzian noise spectrum [29], [63]. The Lorentzian shape is identified by a plateau (S_{Vd} = const) at frequencies lower than the characteristic frequency f_c, specific for each trap, and a $1/f^2$ dependence at frequencies higher than f_c [15], [31], [63], [108]. When there are only a few active defects in the accessible frequency range, e.g., at low temperature or in highly-scaled devices, the noise spectra deviate from a $1/f$ dependence and show a Lorentzian form, denoting prominent single defects [19], [29], [94], [148]. In the time domain the resulting current is dominated by random telegraph noise (RTN), distinct switching between two or more current states that correspond to the trapping and detrapping of carriers by a single defect [23], [29], [31], [77]–[79]. The gate-to-threshold ("overdrive") voltage dependence of low-frequency noise can provide significant insight into defect energy distributions [15], [18], [21], [74].

Low-frequency noise was measured for as-processed and irradiated devices before programming, after programming, and after erasing CTTs. Fig. V-4 summarizes the mean border-trap densities at f = 10 Hz for as-processed and programmed devices CTTs [138]. To

first order, the effective border-trap density D_{bt} in the gate oxide can be estimated from $1/f$ noise measurements using a number-fluctuation model [15], [18], [70], [149]:

$$D_{bt} = \frac{A\, C_{ox}^2}{q^2 k_B T} ln \frac{\tau_1}{\tau_0} \frac{(V_g - V_t)^2}{V_d^2} S_{V_d} f. \qquad \text{V-1}$$

Here S_{Vd} is the excess drain-voltage noise power spectral density, V_t, V_g, and V_d are the threshold, gate, and drain voltages, f is the frequency, q is the electron charge, C_{ox} is the gate-oxide capacitance per unit area, A is the transistor channel area, k_B is the Boltzmann constant, T is the absolute temperature, and τ_0 and τ_1 are minimum and maximum tunneling times [15], [18]. Pronounced RTN was excluded from this analysis. Border-trap densities are higher for as-processed 40-fin CTTs than 2-fin CTTs due most likely to an increasing probability of process-induced defects and/or fin-to-fin variations in conductivity in multi-fin devices. Effective border-trap densities increase by ~1.5–5 times as a result of programming; more significant increases observed for the 2-fin devices. Low-threshold-voltage *n*FETs (lvtnfet) exhibit smaller border-trap densities and smaller increase in D_{bt} with programming than high-threshold-voltage *n*FETs (hvtnfet) due to processing differences in the gate stack [138]. The inferred trap densities for as-processed CTTs are similar to those of MOS devices with high-k gate dielectrics in the literature [15], [18], [19], [94], [113], [120].

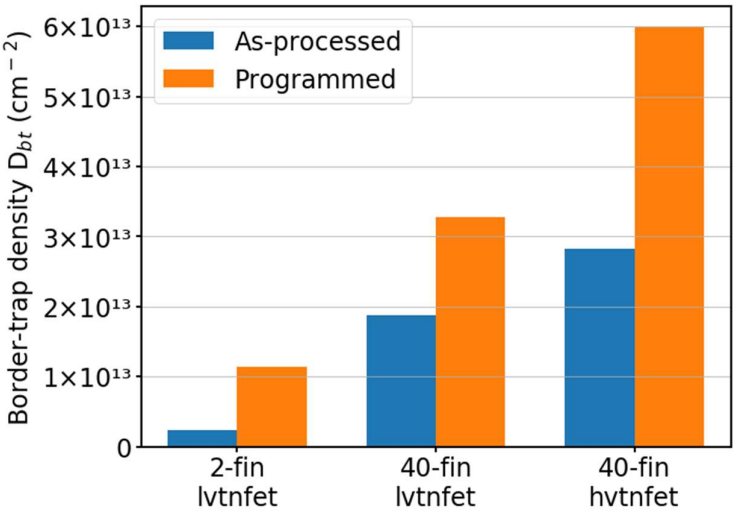


Fig. V-4. Border-trap densities estimated via low-frequency noise measurements for as-processed and programmed 2-fin and 40-fin CTTs. (After [144].)

Illustrative noise spectra are shown in Fig. V-5 for a 2-fin device irradiated to 500 krad(SiO_2) four weeks before programming and erasing. Similar results are observed for

devices measured soon after irradiation, as long as sufficient time has elapsed so that short-term trapped-charge annealing does not lead to threshold-voltage drift during noise measurement [6], [18], [55]. For these devices and irradiation conditions, repeatable noise measurements are usually obtained within 2.5 h to 8 h after irradiation and annealing.

Fig. V-5(a) shows the frequency dependence of the excess drain voltage noise power spectral density S_{Vd} in as-processed 2-fin CTT devices for gate-to-threshold voltages V_{gt} = 0.1 V to 0.6 V. Numbers in parentheses in the legend denote the slope of the frequency dependence. Changes in slopes of noise spectra are indicated where applicable. Values of $\alpha \approx 1$ correspond to a uniform defect energy distribution [15]. The as-processed device generally shows 1/*f*-like behavior, with a prominent defect active at V_{gt} = 0.6 V. In Fig. V-5(b) prominent radiation-induced defects lead to a steeper-than-1/*f* slope at low frequencies and low voltages and a higher-frequency noise plateau at V_{gt} = 0.3 V to 0.4 V. This defect evidently is passivated during programming, as shown in Fig. V-5(c). The resulting spectra in Fig. V-5(c) are similar in magnitude to Fig. V-5(b) and in general scale more closely to 1/*f*. Comparing Fig. V-5(c) and Fig. V-5(d), erasing the devices leads to small changes and less variability in the frequency dependence of the noise spectra. These results suggest that irradiation and programming CTTs do not change overall low-frequency noise magnitudes significantly, but significant differences in response may occur due to the activation or passivation of prominent, individual defects, especially in 2-fin devices. The low-frequency noise of 40-fin CTTs exhibits less radiation-induced variability than 2-fin devices.

Insets in Fig. V-5 show $\beta = -\partial \log S_{vd} / \partial \log \left| V_{gs} - V_{th} \right|$, the gate-to-threshold voltage dependence, for the spectra of Fig. 5. Values of β are calculated for f = 10 Hz and f = 100 Hz after excluding contributions from RTN (Fig. V-8). Values of $\beta \approx 2$ correspond to uniform distribution of border-trap energies in the Si bandgap [15], [21], [74]. Most of the plots show $\beta > 2$, which signifies a defect energy distribution increasing towards midgap; i.e., increasing trap densities as the voltage approaches V_{th}.

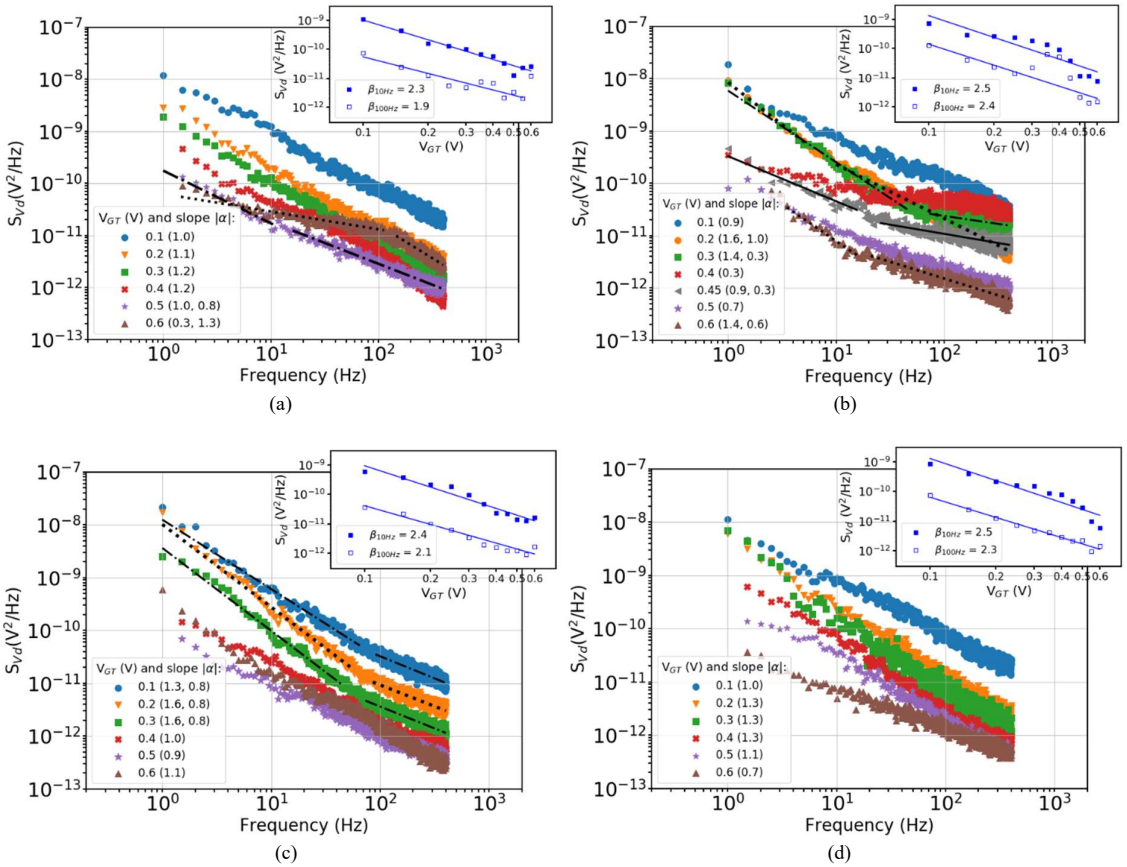


Fig. V-5. Frequency dependences of S_{Vd} for 2-fin CTT: (a) as-processed, (b) irradiated and annealed with V_g = +0.5 V and other terminals grounded at room temperature, (c) programmed after irradiation, and (d) erased using the STAR technique. Insets (a)-(d): Gate-to-threshold voltage dependences of S_{Vd} for f = 10 Hz and f = 100 Hz. Effects of a prominent defect that leads to a high-frequency plateau in the noise spectra in (a) at voltages V_{gt} from 0.3 V to 0.4 V (green squares, red crosses, and grey tilted triangles) is removed during the programming sequence performed before the spectra of (c). (After [144].)

Fig. V-6 shows a three-dimensional visualization of the effects of the prominent defect that is activated during irradiation for the device of Fig. V-5. As-processed frequency spectra are generally proportional to 1/*f*. After irradiation, the spectra became Lorentzian in form, with a clearly observable plateau representing a one order of magnitude increase in noise at higher frequencies for f > 100 Hz. This individual-defect-related plateau remains visible in the next two sets of results, obtained two and four weeks after irradiation. After programming, the noise spectra change shape to become 1/*f*-like and the plateau disappears. The last set of noise

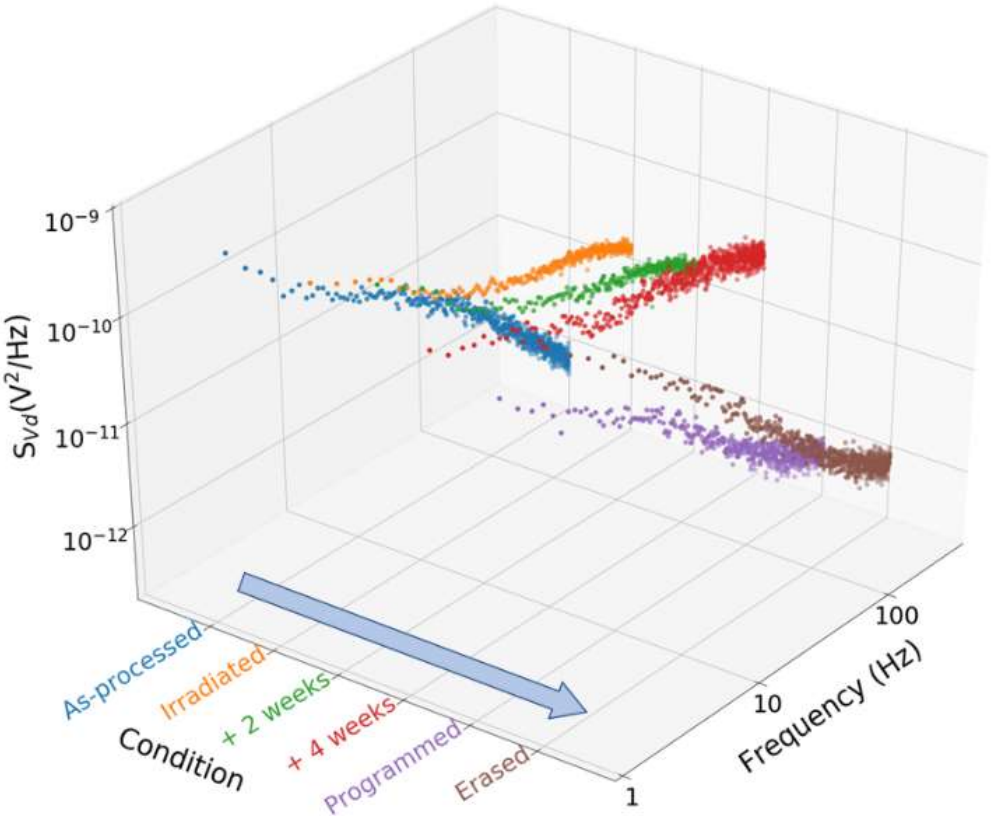


Fig. V-6. Three-dimensional visualization of the frequency dependence of S_{Vd} at V_{gt} = +0.4 V and V_d= 50 mV for the devices and conditions of Fig. V-5. (After [144].)

measurements on the erased device also shows an approximate 1/*f*-dependence, with a slight increase in slope. Thus, the results of Fig. V-5 and V-6 illustrate that TID irradiation can have a significant and lasting effect on the trap distribution of 2-fin CTTs by activating prominent defects. Programming the devices under the conditions of this study activates additional defects, leading once more to featureless 1/*f* noise at V_{gt} = 0.4 V.

5.3.3 Random Telegraph Noise

RTN measurements also were performed on the devices of Fig. V-5 andFig. V-6 at values of V_{gt} from 0.1 V to 0.6 V. Fig. V-7(a), V-7(b), and Fig. V-8(c) show characteristic RTN traces at V_{gt} = 0.2 V for irradiated, programmed, and erased devices, respectively. Fig. V-8 illustrates the full evolution of RTN response. The variations of up to $\Delta I_d \sim 1$ μA in average drain current in Figs. V-7 and Fig. V-8 at similar applied V_{gt} are due to (1) small changes in V_{th} during RTN measurements, (2) the relatively steep slopes of the *IV* curves in this region, and

limitations of the V_{th} determination algorithm employed in this work. These variations do not significantly affect the results or conclusions of the study.

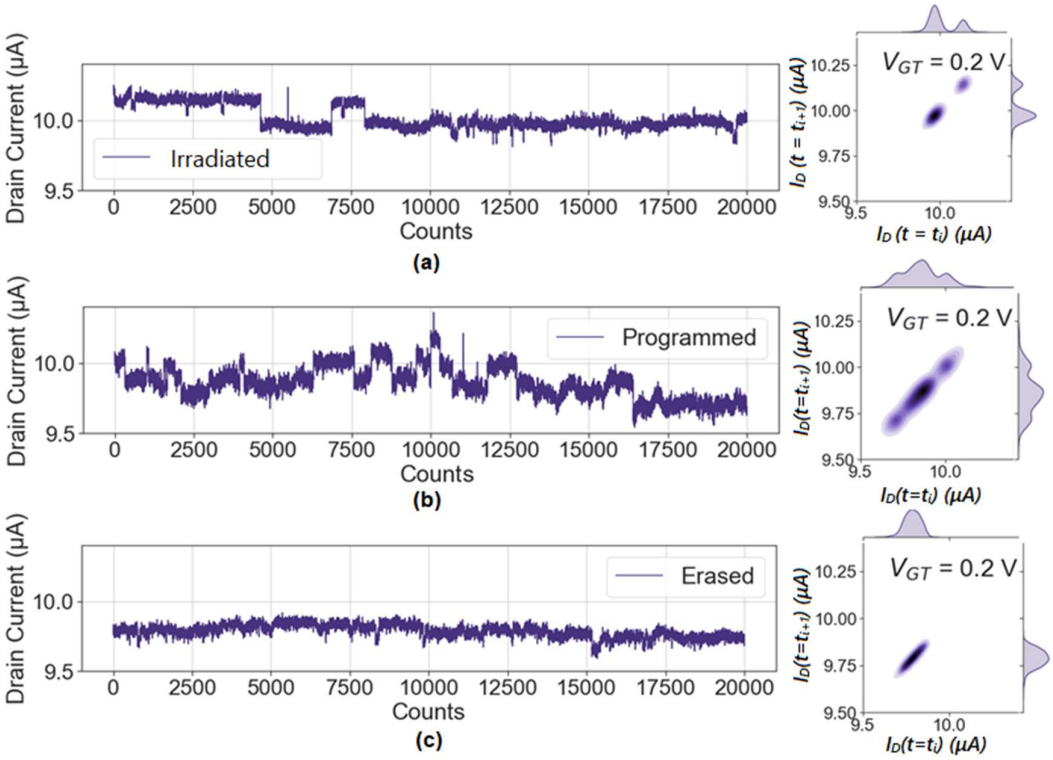


Fig. V-7. Drain current traces at V_{gt}= 0.2 V for 2-fin devices that were (a) irradiated and annealed with V_g = +0.5 V and other terminals grounded at room temperature, (b) programmed, and (c) erased. Weighted time lag plots show stable current states on the diagonals and amplitude histograms (top, right) for each of the conditions. (d) Weighted time lag plots are shown for all measured gate-to threshold voltages for irradiated and annealed, programmed, and erased devices. (After [144].)

In Fig. V-7(a) two distinct current levels are evident in the weighted time lag plot, which signifies the presence of a prominent trap. After programming, at least two distinct traps contribute to RTN; these are easily visible in the weighted time lag plot in Fig. V-7(b). Each of these trends in RTN is consistent with the large increases in slope of the corresponding noise spectra (yellow triangles) in Fig. V-5(b) and V-5(c) at low frequencies. After erasing, the spectra in Fig. V-7(c) show no prominent RTN, consistent with the more uniform 1/*f*-noise-like behavior in Fig. V-5(d) at V_{gt} = 0.2 V. Fig. V-8 shows that, after the device is erased, the majority of RTN-producing defects are passivated, and noise spectra show less variation in response.

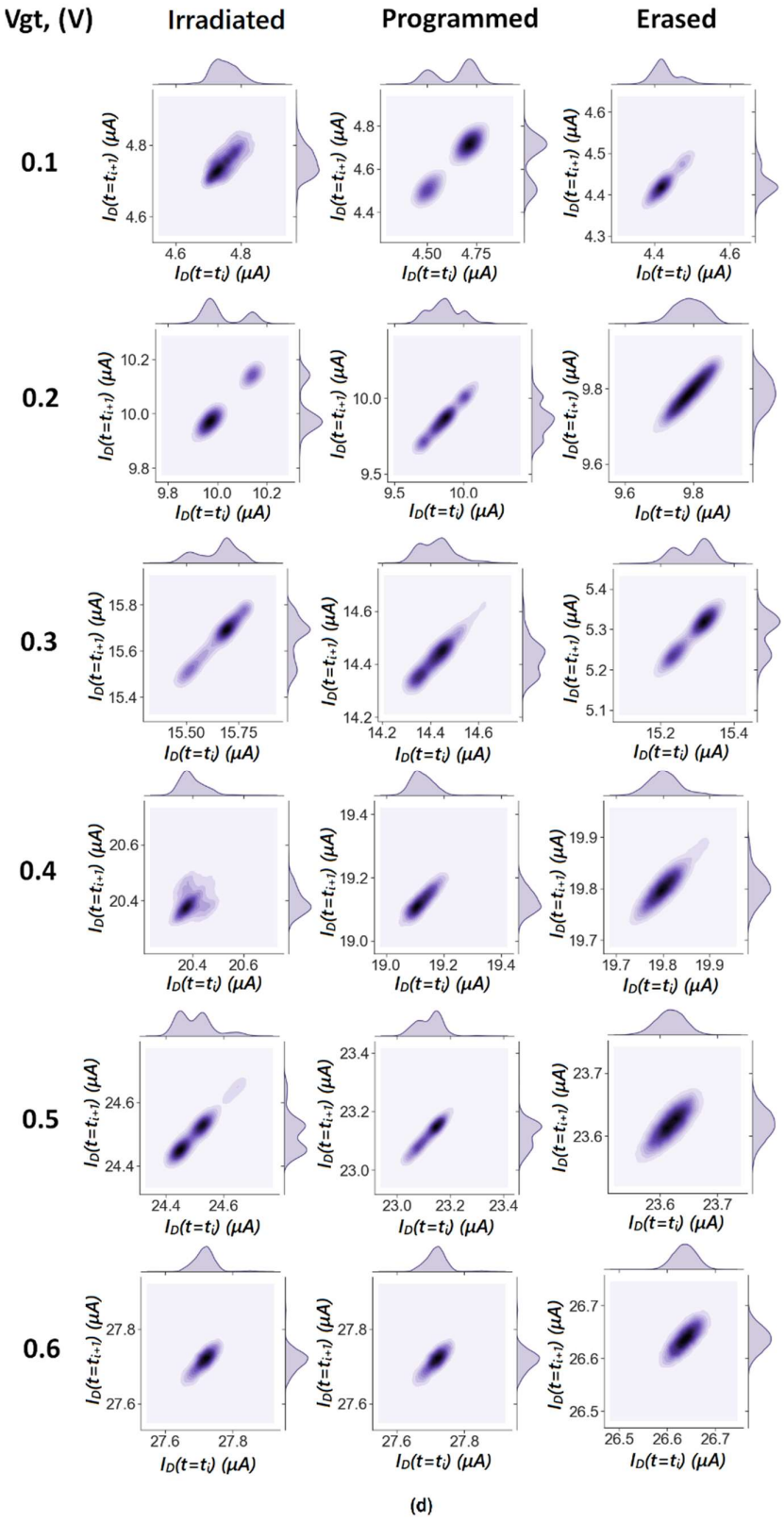


Fig. V-8. Weighted time lag plots are shown for all measured gate-to threshold voltages for irradiated and annealed, programmed, and erased devices. (After [144].)

Along with the prominent, individual defects observed in Fig. V-8, there is an underlying 1/*f* noise spectrum, due most likely to a broad distribution of defects in the near-interfacial regions of the as-processed devices [15], [18]. Consequently, it is not possible to use the hidden Markov model and/or other advanced RTN-related analyses [94], [121], [123]–[125], [150]–[153], to identify the relative positions of the most prominent traps in the insulating layers or with response to the source of drain junctions. However, previous work on similar SiO_2/HfO_2 dielectrics strongly suggests that the defects responsible for RTN in devices with SiO_2/HfO_2 dielectrics are associated with O vacancies in the near-interfacial HfO_2 and/or hydrogen shuttling between dangling Si bonds at the Si/SiO_2 interface and defects at the SiO_2/HfO_2 interface [17], [18], [70], [114].

RTN must be considered in memory applications using CTTs. It has been known that fluctuations in threshold voltage V_{th} caused by presence of RTN can lead to read failures in flash memories after P/E cycling [34]. These results show that RTN may be a similarly significant issue for CTTs. RTN may lead to instabilities in analog memory devices for neural network applications, since device-to-device variation in responses can degrade the precision of neural network training and operation of these devices [140].

5.4 Conclusions

LFN and RTN were evaluated in as-processed, irradiated, programmed, and erased CTTs fabricated in a 14-nm bulk CMOS technology as a function of gate-to-threshold voltage. TID irradiation increases the uniformity of effective border-trap energy distributions due to activation of stable radiation-induced traps. Programming moderately increases the low-frequency noise and border-trap densities and activates a number of prominent individual defects. These lead to deviations from 1/*f* frequency dependence in noise spectra and RTN in the time domain, likely associated with trapping at O vacancies in the near-interfacial HfO_2 and/or hydrogen shuttling between dangling Si bonds at the Si/SiO_2 interface and defects at the SiO_2/HfO_2 interface. Erasing devices passivates the active defects leading to RTN, resulting in a more uniform defect-energy distribution. We conclude that the noise of CTTs is generally similar to that of other devices that incorporate SiO_2/HfO_2 gate dielectrics. These results are encouraging for the future use of 14-nm bulk CMOS CTTs as non-volatile memory elements in a space environment. However, the presence of RTN in CTT-based analog memory devices will require special attention during the neural network training and operation of these devices.

CHAPTER VI

CONCLUSIONS

The introduction of new architectural approaches and advanced materials in microelectronic device fabrication raises the need for a deeper investigation of the radiation response of these nanoscale devices. In this work, we have studied the total-ionizing-dose effects in nanoscale silicon MOSFETs with advanced architectures using low-frequency and random telegraph noise. The devices were irradiated with 10 keV X-rays up to 0.5 Mrad(SiO_2) – 2 Mrad(SiO_2) and then annealed at room temperatures. The collected results help to gain insights into the TID response of advanced devices and obtain a better understanding of the physical mechanisms underlying radiation degradation.

Extensive analysis of TID-induced degradation was performed for 30-nm Gate-All-Around FETs. Vertically stacked bulk GAA Si-NW *n*-channel and *p*-channel FETs show outstanding radiation tolerance relative to that of other highly scaled devices [46], [97], [102]–[104]. Specifically, irradiated GAA transistors show low sensitivity to TID due to the excellent electrostatic gate control over the channel and the effective suppression of the radiation-induced drain-to-source leakage path. These results confirm the great promise for the use of GAA NW devices in CMOS circuits for applications in high-radiation environments.

Analysis of TID-induced low-frequency noise response was performed on highly-scaled GAA devices. High-degree of RTN was observed in low-frequency noise response measured from 80 K to 300 K. The evolution of traps with temperature shows the presence of stable prominent defects. They are most likely associated with oxygen vacancies and/or hydrogen complexes. The observed RTN is due to traps located in both the SiO_2 and HfO_2 dielectrics, with significant variations in capture and emission times over the range of voltages explored. These results indicate that defects in these devices are distributed non-uniformly in energy and space and confirm the increasing importance of RTN for highly scaled devices. These defects can strongly affect device performance and reliability [31], [70], [78], [130], [131], which can be manifested on a circuit level by RTN-induced cell leakage and logic delay fluctuations in digital logic cells, jitter in memory cells, and frequency variability, e.g. in ring oscillators, especially under low voltage operation [132]–[134]. This RTN-caused device-to-device variability will likely govern the noise response of a circuit built with GAA devices. The devices likely would benefit from the reduction of interface and border-trap densities by

optimizing processing steps for the high-k gate stack, e.g., mitigating fin oxidation by reducing the STI thermal budget [39].

In-depth analysis of LFN and RTN was performed in as-processed, irradiated, programmed, and erased CTTs fabricated in a 14-nm bulk CMOS technology as a function of gate-to-threshold voltage. TID irradiation increases the uniformity of effective border-trap energy distributions due to activation of stable radiation-induced traps. Programming moderately increases the low-frequency noise and border-trap densities and activates several prominent individual defects. These lead to deviations from 1/*f* frequency dependence in noise spectra and RTN in the time domain, likely associated with trapping on O vacancies in the near-interfacial HfO_2 and/or hydrogen shuttling between dangling Si bonds at the Si/SiO_2 interface and defects at the SiO_2/HfO_2 interface. Erasing passivates the active defects leading to RTN, resulting in a more uniform defect-energy distribution. We conclude that the noise of CTTs is generally similar to that of other devices that incorporate SiO_2/HfO_2 gate dielectrics. These results are encouraging for the future use of 14-nm bulk CMOS CTTs as non-volatile memory elements in a space environment. However, the presence of RTN in CTT-based analog memory devices will require special attention during the neural network training and operation of these devices.

In conclusion, miniaturization of electronic devices, switching to thin high-quality oxides, and the use of advanced device architectures, such as FinFETs and GAAs, have reduced the severity of TID effects in highly-scaled devices in terms of DC response. However, these technologies have brought about a new issue of non-uniform TID response due to device-to-device variability and prominent defects. Therefore, investigation of LFN and RTN can help to thoroughly assess the TID response and provide insight into the basic radiation degradation mechanisms and reliability-limiting defects in highly-scaled MOSFET devices.

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