High-Current State Triggered in the Bulk FinFET Technology

By

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CHAPTER I

Background

1. Background

The electronics industry has made significant advances with the development of integrated circuits (IC). As with any technology, semiconductor technologies have experienced a myriad of failure mechanisms. Multiple failure modes have been extensively researched to increase the reliability of the ICs and decrease the probability of a failure [1, 2]. One of the most significant failures affecting the opertation of an IC is the high-current state. High-current state is defined as significantly increased supply current under normal operating conditions. High-current state of a circuit can be attributed to multiple mechanisms. These mechanisms may be triggered by either external (operational environment related) or internal (operational variables). An example of an external factor is radiation-induced latch-up leading to a short circuit between supply voltage and ground potential for CMOS ICs. An example of an internal factor is an overshoot at output pad on an IC leading to a latch-up condition. In this thesis the high-current state caused by radiation-induced latch-up or by changes in the operating frequency will be investigated.

For the environment in which most of the commercial ICs operate, both man-made and natural radiation are present. [3]. Cosmic rays are most likely to affect circuit operation on the ground other than nuclear facilities. Part of the radiation on the ground is generated from the products of sixth and seventh generation of galactic cosmic rays (GCR) and solar particles in the atmosphere, as is seen in Fig. 1-1. The radiation effects on circuits in the nuclear facilities also need to be considered [3]. The parasitic silicon-controlled rectifiers (SCR) could be triggered in the circuits

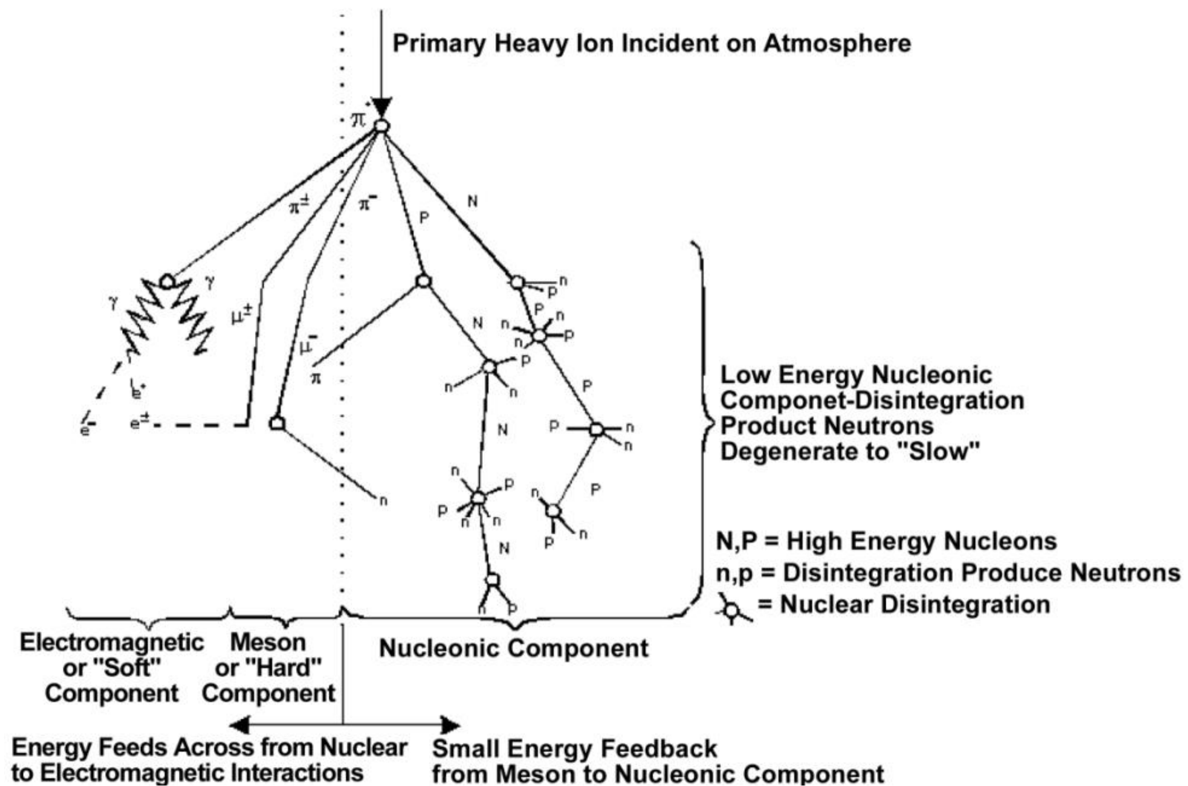


Fig. 1-1 Cosmic rays hit the top of the atmosphere and disintegrate into neutrons, pions, muons, etc [3].

operating in these environments due to the radiation. Such an undesirable operational mode has been termed as latch-up. Under latch-up, operating current will increase significantly. This kind of high-current states must be addressed and mitigated before it influences the operating behavior of the IC. The exact mechanism for latch-up will be introduced in the following sections.

In addition to the influence of the radiation effects, the high-current state could also be triggered due to the change of the operational settings of the circuits. The change of the operating-frequency in the circuits may also trigger the high-current state. This kind of high-current may lead to the thermal runaway, which may damage the IC. The temperature of a die and the supply current usually form a positive feedback loop – an increase in temperature will increase the supply current, and the increased supply current will increase the die temperature [4-7]. If the heat removal rate is

smaller than the heat generation rate, a thermal runaway event may be triggered. This thesis shows how a change in operating frequency may lead to a high-current state (similar to latch-up) which may be responsible for thermal runaway.

This thesis will be organized as following sections:

1. Chapter 1 illustrates the general introduction of the background information about the high-current state triggered in the digital ICs, and listed two basic mechanisms that will be introduced in the thesis. Latch-up, especially the single-event latch-up triggered by the radiation exposures is one of the factors that will lead to the high-current state. Another novel mechanism that is related to operating-frequency change will also be introduced in the thesis.
2. Chapter 2 presents the experimental details of the single-event latch-up tests and the tests of high-current state triggered by operating-frequency change. The basic design of the test chips will be discussed along with the test setup for the radiation exposures. Fast neutrons and alpha particles are used in the radiation tests. For the operating-frequency-change tests, the steps of frequency changes and the test setup are also discussed in the thesis. Factors affecting the failure probabilities, such as supply voltage and temperature are characterized in these tests.
3. Chapter 3 presents experimental results. The test results of both single-event latch-up tests and the tests of high-current state triggered by operating-frequency change are discussed in this chapter. The supply current behavior and the latch-up failure in time (FIT) rate are included in the thesis. The behavior of frequency-induced high-current state is also demonstrated. The temperature effects of high-current state triggered by latch-up and change of operating-frequency are also discussed in the thesis.

4. Chapter 4 illustrate the analysis of the high-current states observed that are triggered under two different situations and give the conclusions and the future directions of this topic.

2. ***Introduction of the Latch-up***

Latch-up in CMOS devices and integrated circuits (IC) is one of the most important issues of reliability, especially for the electronic systems implemented in the field of automobile and space system [8, 9, 10]. Latch-up is defined as a high-current state in which an electrical conducting path connecting the supply voltage and ground is generated. H.N. Becker, et. al. showed that the latch-up event could lead to the structural changes in interconnects that appears to be due to electromigration in the ICs due to the large amount of heat generated and the resulting melting [11]. Latch-up can often be sustained for a relatively long period of time. In such a case, the current increases to a relatively high level and may remain stable for very long time periods. The non-destructive latch-up event will not do severe damage to the circuits but may degrade the performance of the devices and ICs. It is then imperative for designers and users to understand factors initiating and affecting latch-up. As presented in this thesis, change of the circuit operating condition or a particle strike may generate the necessary transient current to initiate a latch-up state. Peng Wang, et. al. measured two-photon absorption-induced latch-up for the specially designed p-n-p-n cell arrays and characterized the onset region in which the probability of latch-up triggering has a transition between 0 and 1 as the energy of the laser pulse increases [12]. James Karp, et. al. have shown that the 64 MeV proton beam could trigger the latch-up state and sudden increases in supply current of more than 100 mA was observed [13]. Chien-Yao Huang, et. al. also observed and characterized how the existence of deep-n-well (DNW) will increase the latch-up sensitivity [14].

In the process of manufacturing CMOS ICs, it is inevitable that the parasitic p-n-p-n structures (also known as the basic structures of silicon-controlled rectifiers (SCR) or thyristors), will exist. The parasitic pnp BJT transistors are usually formed by p+ source/n-well/p-substrate, and parasitic npn BJT transistors are usually formed by n+ source/p-substrate/n-well, as it is shown in Fig. 1-2 (planar technology) [15], and Fig. 1-3 (bulk FinFET technology). In the equivalent circuits that represents the parasitic latch-up structure, as shown in Fig. 1-4 [16], the base junction of the npn BJT transistor is connected to the collector junction of the pnp transistor. The p-substrate region functions as both the base region of the parasitic npn transistor and the collector region of the parasitic pnp transistor. Similarly, the base junction of the pnp BJT transistor is connected to the collector junction of the npn transistor. The n-well region functions as both the base region of the parasitic pnp transistor and the collector region of the npn transistor. The parasitic npn and pnp

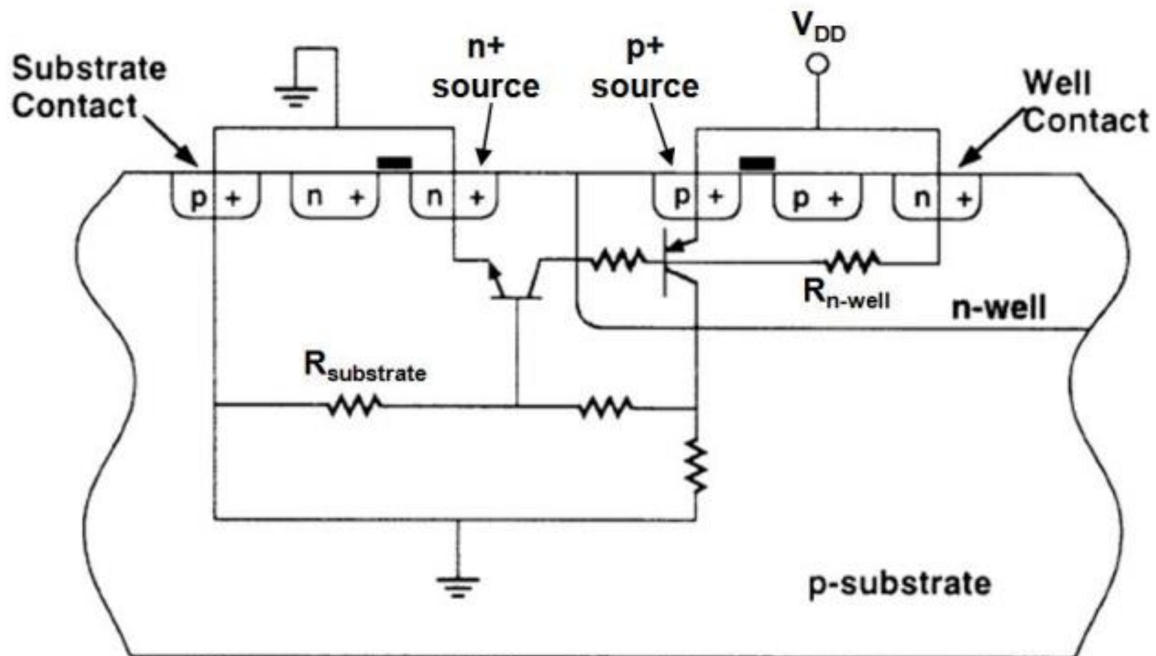


Fig. 1-2 Parasitic transistors and resistors in the CMOS [15]

transistors then form a positive feedback loop together. The base-collector junctions of both npn and pnp BJT transistors are reversed biased under normal non-latch-up operation. Transient current generated due to a particle strike may increase the voltage of base/emitter junctions of those BJT transistors. If a transient current is generated in the circuits and then one of the transistors is turned on. The base/emitter junction of one of the BJT transistors is forward-biased, then the base current will be amplified. The other BJT transistor will be turned on, then the positive feedback loop and latch-up state is established. The resulting high-current state is the latch-up state. The related event is viewed as single-event latch-up (SEL). The common-emitter current gains, βpnp and βnpn, are among the most important factors of the latch-up. Results show that the product of the common-emitter current gains is required to be larger than 1 in order to trigger the positive feedback loop. The supply voltage also needs to be greater than triggering threshold value to meet latch-up criteria

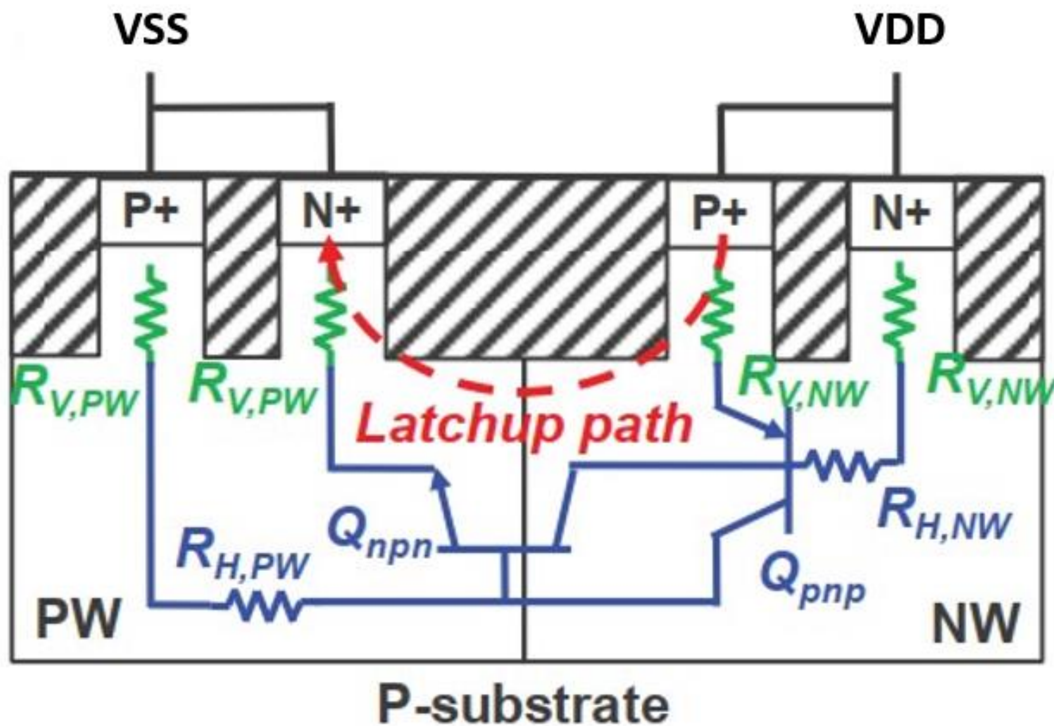


Fig. 1-3 The cross-sectional view of the latch-up path in the bulk FinFET technology ([after 22])

[17, 18, 19, 20]. Fig. 1-5 shows the typical curve of I-V characteristics of a parasitic SCR. The

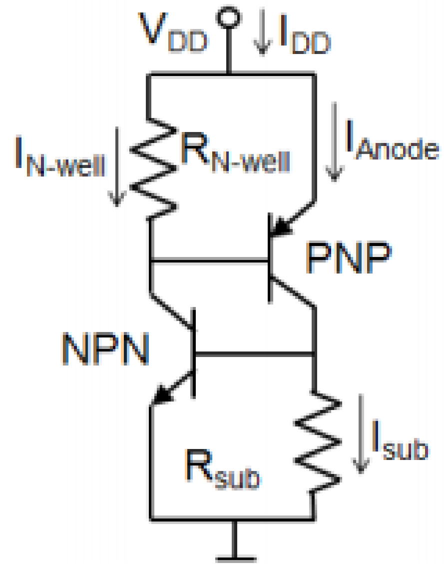


Fig. 1-4 The equivalent circuits of a typical latch-up structure [16]

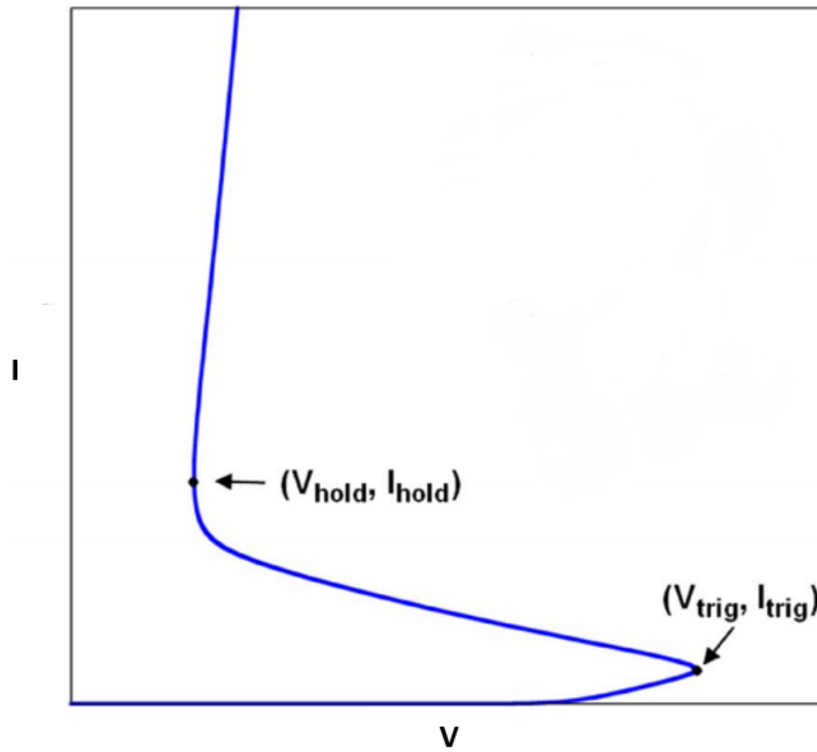


Fig.1-5 I-V characteristics of a typical p-n-p-n structure (after [16])

triggering point is V_{trig}. Once the latch-up is triggered, the p-n-p-n structure will then remain in the high-current state unless the voltage is reduced to the level that is below a critical value which is V_{hold}. If supply voltage is lower than the holding voltage, then the latch-up could not be sustained [16].

3. ***High-Current State Triggered by Frequency-Change***

Thermal runaway process may start with a sudden increase in supply current, resulting in an increase in the local die temperature. The temperature of a die and the supply current usually form a positive feedback loop [4-7], and if the heat removal rate is smaller than the heat generation rate, a thermal runaway event may be triggered. Since thermal runaway is a destructive event, reliability engineers have made characterization of all factors responsible for thermal runaway a high priority issue. The number of variables that can initiate thermal runaway events include supply voltage variations or frequency variations. Supply-voltage spikes causing latch-up, which may increase the local die temperature and subsequently lead to the thermal runaway, are well known and have been evaluated and characterized previously [20, 22], and will also be introduced in the thesis. Through a test IC, this work shows how a change in operating frequency will lead to a high-current state (similar to latch-up) which may also be responsible for thermal runaway.

CHAPTER II

Experimental Details

7-nm bulk FinFET technology is used in the experiments to characterize the high-current state. 7-nm is widely used in the digital circuits, such as personal computer, mobile phone, etc. As it has been shown in the previous sections, high-current state of the circuits triggered by latch-up and operating-frequency change are included in this thesis. This chapter will introduce the basic structure and elements of the test chips, and the related settings of the experiments.

1. Information of Test Chips

Test chips were fabricated in a commercial 7-nm bulk FinFET technology. Shift registers with different flip-flop (FF) designs of varying radiation hardness were implemented in Circuit for Radiation Effects Self-Test (CREST) configuration [23], as shown in Fig. 2-1. The number of

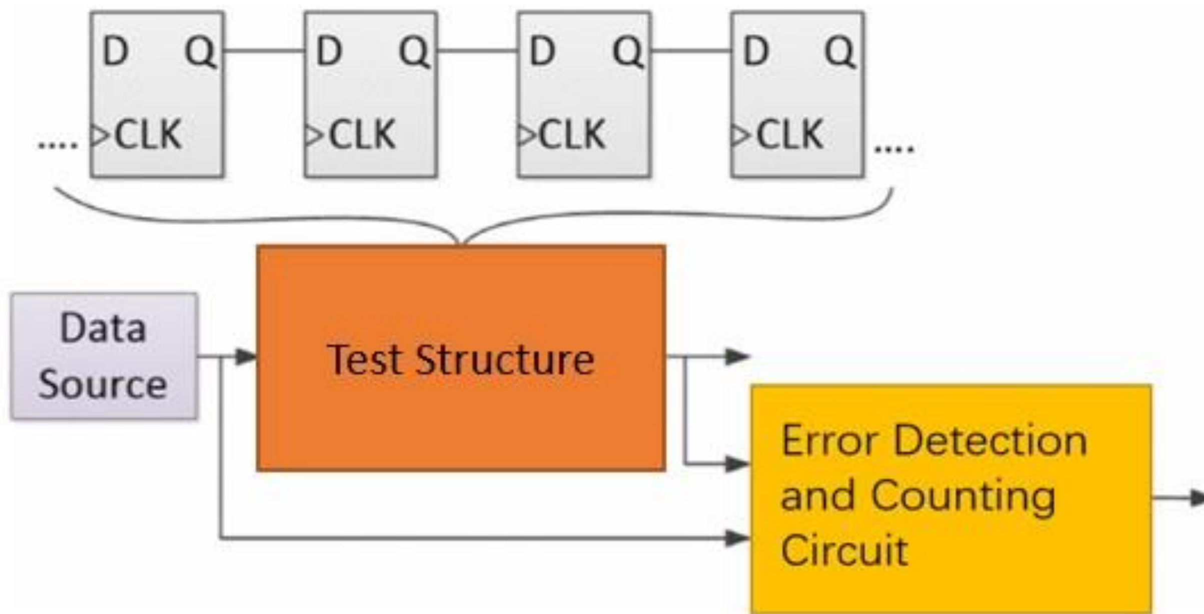


Fig. 2-1 CREST block level design used for evaluating SEU response of FF cells [after 24]

stages in the shift register varied from 8K to 32K depending on the FF design. The size of the test IC was 2 mm × 1 mm. The circuit board is shown as the Fig. 2-2.

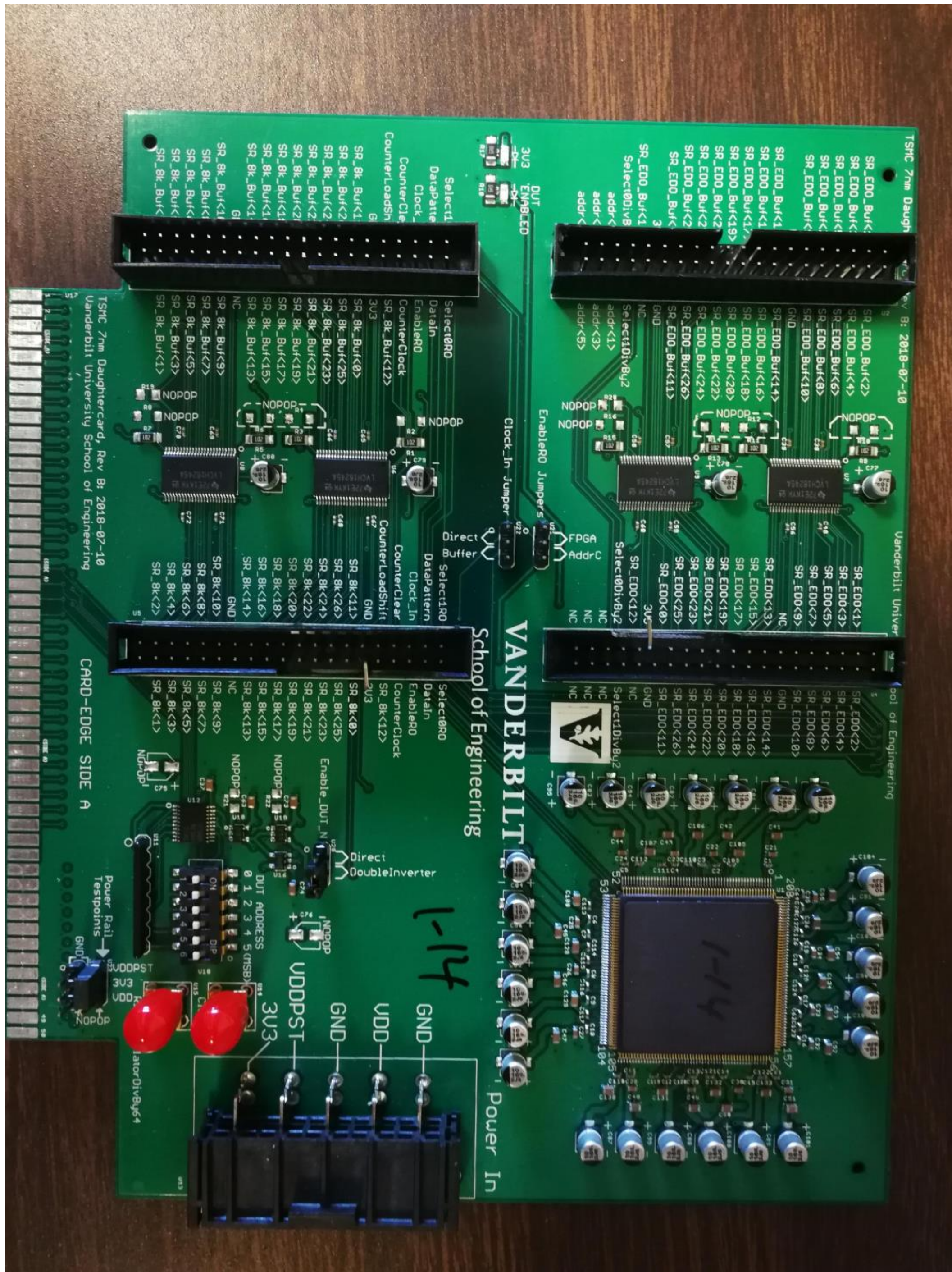


Fig. 2-2 Typical circuit board used in the experiments

2. *Setup of the Latch-up Tests*

Fast neutrons and alpha particles are used in the experiments to test if the latch-up could be triggered in the ICs. Fast neutrons experiments were conducted at ChipIr facility at Appleton-Rutherford Laboratory in Didcot, UK. The flux of fast neutron beam is ~6×10^{6} neutron/cm^2/s. Alpha experiments were conducted at Vanderbilt University using Americium-240 foil source. This source (1 cm × 1 cm size) was placed right above the circuit. The alpha emissivity was 1000 alpha/mm^2/sec. The distance between the die and the alpha source was less than 1 mm. The LET value of alpha particles is less than 1 MeV-cm2/mg. The typical experiment setups are shown in the Fig. 2-3 and Fig. 2-4.

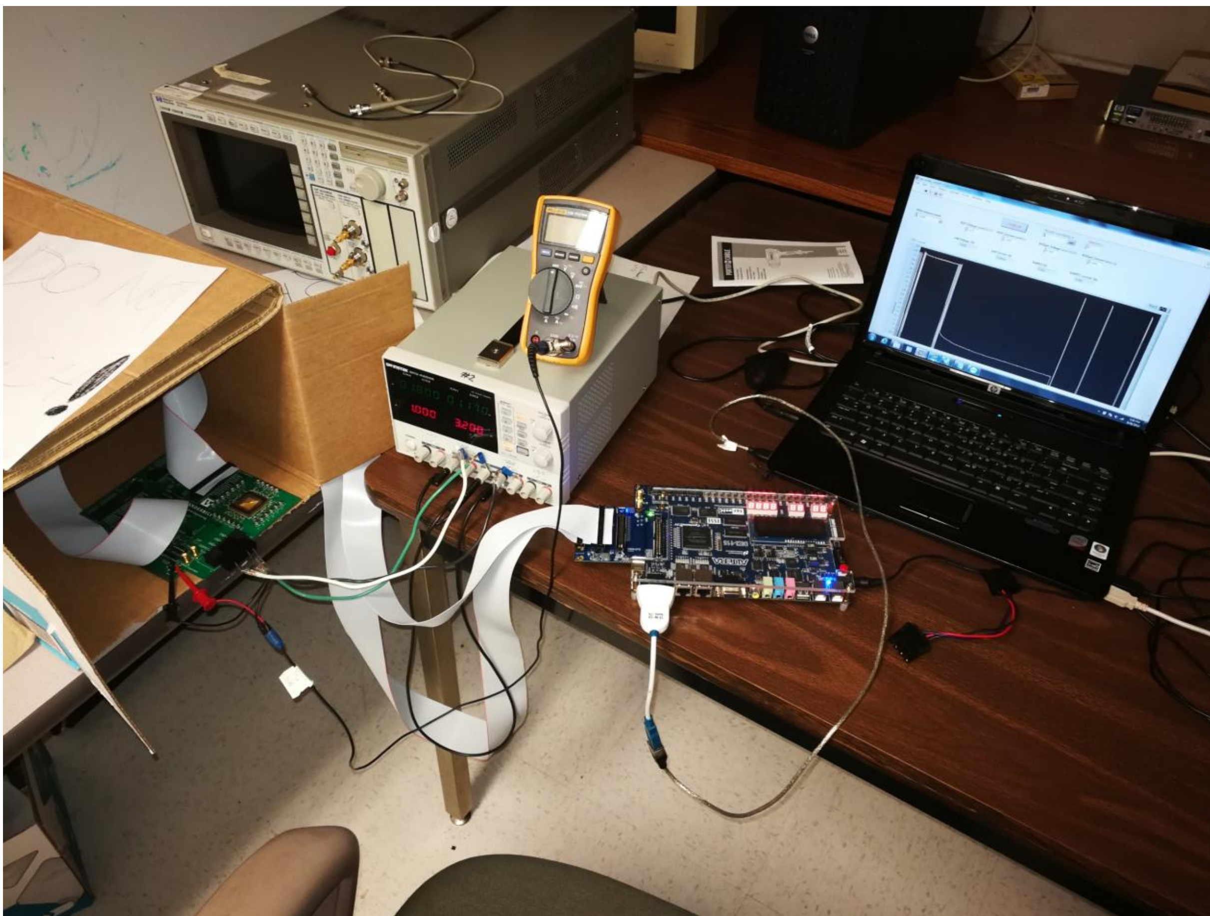


Fig. 2-3 Typical test setup of the alpha tests

Effects of temperature on FIT rates for latch-up due to neutron and alpha particles were also evaluated in the tests. A heat gun was used to heat the board during the operation of the ICs. Temperature was measured by an infrared thermometer. The operating temperature was slowly controlled such that the temperature of IC does not fluctuate significantly. The temperature of the test chip ranges from ~25 ^{o}C to ~125 ^{o}C. The operating frequency during the test was provided by the FPGA and is ~2.5 MHz. In order to monitor the supply current and plot the curve of supply current versus time, the LabVIEW program was used to communicate with the DC power supply and control the supply voltage and monitor the supply current. The LabVIEW program could be organized as various sub-models. The sub-models could be modified and be implemented into other test programs. Python, C, etc. could also be used to communicate with the power supply and extract the voltage-current data.

Fig. 2-4 Typical test setup of the neutron tests

3. ***Setup of the Tests of Frequency Change-Triggered High-Current State***

The test circuits used in the experiments containing shift registers with different flip-flop (FF) designs capable of operating up to 6 GHz was fabricated at the 7-nm node. Ring Oscillators were used to generate on-chip high-frequency (up to 6 GHz) clock signals. Low frequency clock (less than 100 MHz) signals were provided from external sources. FPGAs were used to control/exercise the test IC and provide the signals for selecting desired operating frequency. The low frequency clock (2.5 MHz) is provided by the FPGA, and on-chip high frequencies used for the experiment were ~700 MHz, ~1100 MHz and ~1500 MHz. These frequencies were measured at nominal supply voltage. The actual value of these frequencies will vary under different supply voltages used in the experiments. The exact values of different operating frequencies were measured with high-resolution oscilloscope. Tests were conducted at room temperature and elevated temperatures. A heat gun was used to increase the operating temperature of the die. The temperature of the die during experiment was varied from 25 ^{o}C to 115 ^{o}C. The input to the shift register was held at logic 0 for all experiments (meaning, change in frequency affected only the clock network and not the rest of the circuit). A LabVIEW program, shown in Appendix A, was used to communicate with the DC power supply and monitor the supply current. To evaluate the effects of operating frequency changes, the operating frequency settings was changed in multiple ways as shown in Table 2.1. These frequencies were generated using different on-chip ring oscillators. As the frequency of ring oscillators are a strong function of supply voltage, any changes in supply voltage will change these frequencies. It should be noted that the actual frequency value is different for different test conditions due to different supply voltages used. It must also be noted that operating temperature will also affect ring oscillator frequencies. The actual frequency value will be mentioned in the following chapter as appropriate. These changes in frequencies were carried out for a wide range of supply voltages, ranging from 0.75 V (nominal)

to 1.3 V. Elevated supply voltages were used to initiate the failure mode quickly – similar to how it is done for latch-up and aging tests.

TABLE 2.1. Representative Sequences of Frequency Settings Used During Tests (frequency values shown are for nominal supply voltage. Depending on the supply voltage used, these frequencies will change.)

Steps	#1	#2	#3
Test #1	2.5 MHz	700 MHz	2.5 MHz
Test #2	2.5 MHz	1.1 GHz	2.5 MHz
Test #3	2.5 MHz	1.5 GHz	2.5 MHz
Test #4	700 MHz	2.5 MHz	
Test #5	1.1 GHz	2.5 MHz	
Test #6	1.5 GHz	2.5 MHz	

CHAPTER III

Experiment Results

Single-Event latch-up (SEL) event and operating frequency-triggered high-current state have been characterized in these experiments. Both set of experiments demonstrate similar high-current behavior. This chapter will introduce the experiment results of the SEL experiments and operating-frequency change-triggered high-current tests.

1. Experiment Results of the SEL Tests.

For neutron tests, the current limit on the power supply was set to 1.0 A to avoid damaging the test IC. The nominal operating current was in 10's of mA range at 2.5 MHz frequency. Latch-up events were not observed when the supply voltage was lower than 1.1 V for the total fluence of more than $\sim 1\times 10^{10}$ neutron/cm^2. For the tests at room temperature, single-event latch-up was observed when the supply voltage was increased to 1.4 V. For alpha tests, the latch-up occurred when the supply voltage was increased beyond 1.4 V. Fig. 3-1 shows the results of supply current versus time of a typical latch-up event at VDD = 1.6 V for alpha tests. The results show that multiple step increases (termed as micro latch-up events) occurred before the current limit was reached, suggesting that micro latch-ups occurred in the IC. Fig. 3-2 shows the SEL FIT rate (or cross-section, C.S.) for alpha and neutron tests at different supply voltage for room temperature and elevated temperatures. Results show that the SEL FIT rate increases as supply voltage increases. At elevated temperature (~100 ºC for fast neutron tests and ~75 ºC for alpha tests), the SEL FIT rate is significantly larger than that at room temperature.

I-V properties are also characterized for the latch-up current state. After the supply current reaches the current limit value, the radiation source was removed, and the supply voltage was reduced and the current was monitored in this process. Fig. 3-3 shows a typical curve of I-V characteristics of the latch-up state after being triggered by the alpha source. When the supply voltage was reduced, the supply current decreased linearly first and then several step decreases occurred, which may be related to the removal of the micro latch-up in multiple locations. When the supply voltage is ~1.14 V, the current drops back to the initial value where latch-up does not exist. The current will never change back to the high-current latch-up state. In this case, ~1.14 V could be viewed as the 'holding voltage' of the latch-up state. Fig. 3-4 shows the results of holding

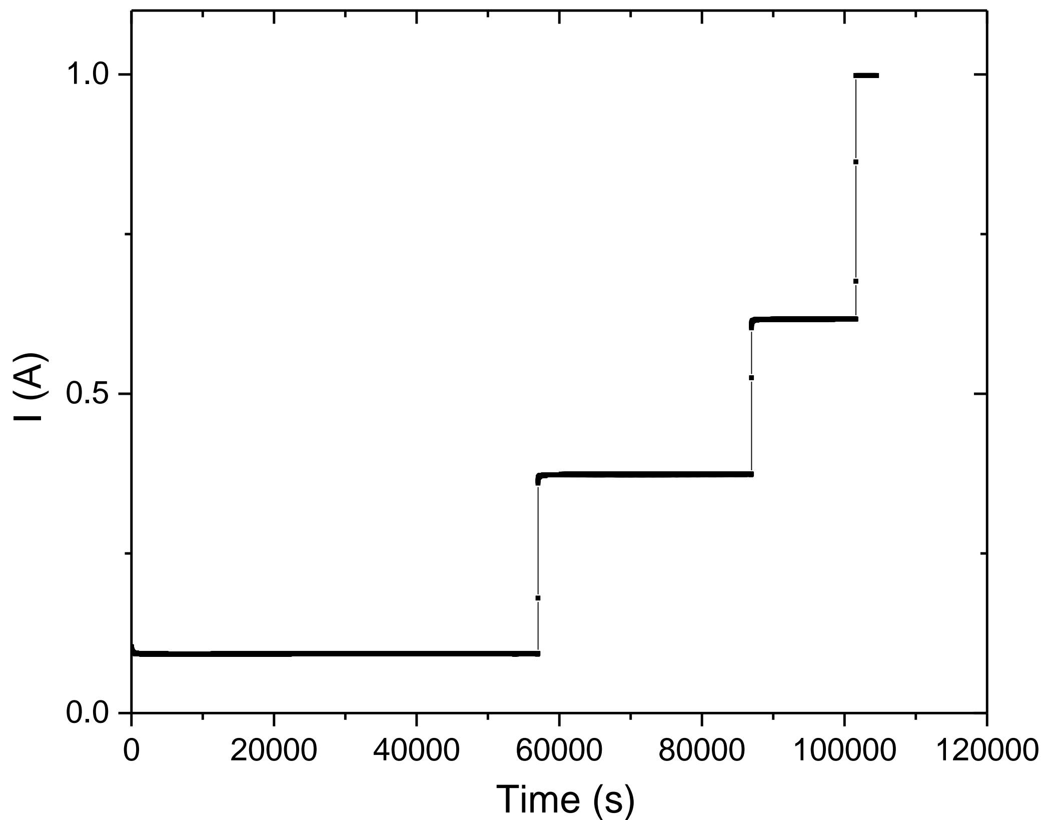
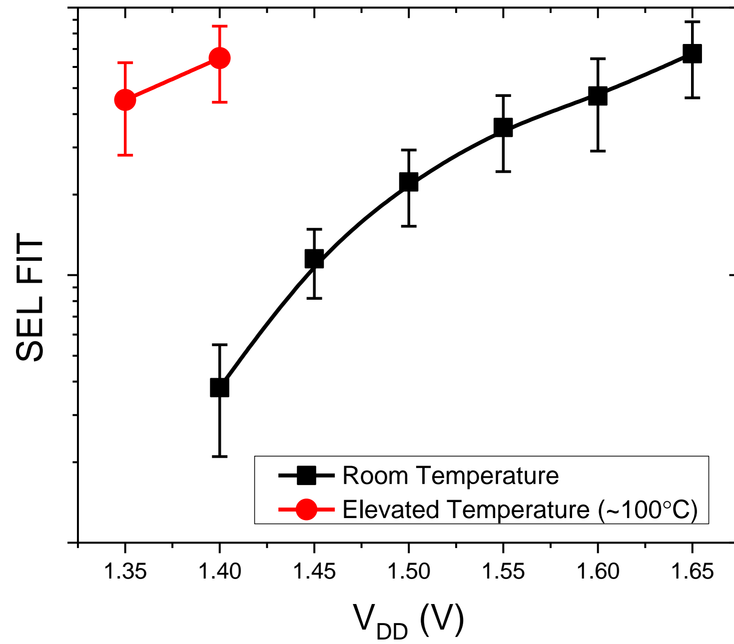
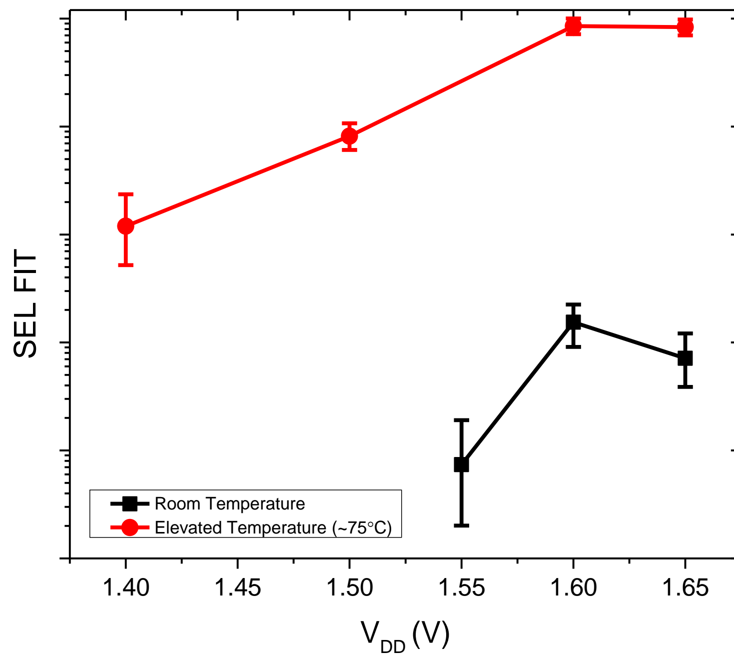


Fig. 3-1 The VDD current versus time observed at VDD = 1.6V



(a)



(b)

Fig. 3-2 SEL FIT rate for (a) fast neutron and (b) alpha tests at different V_{DD}

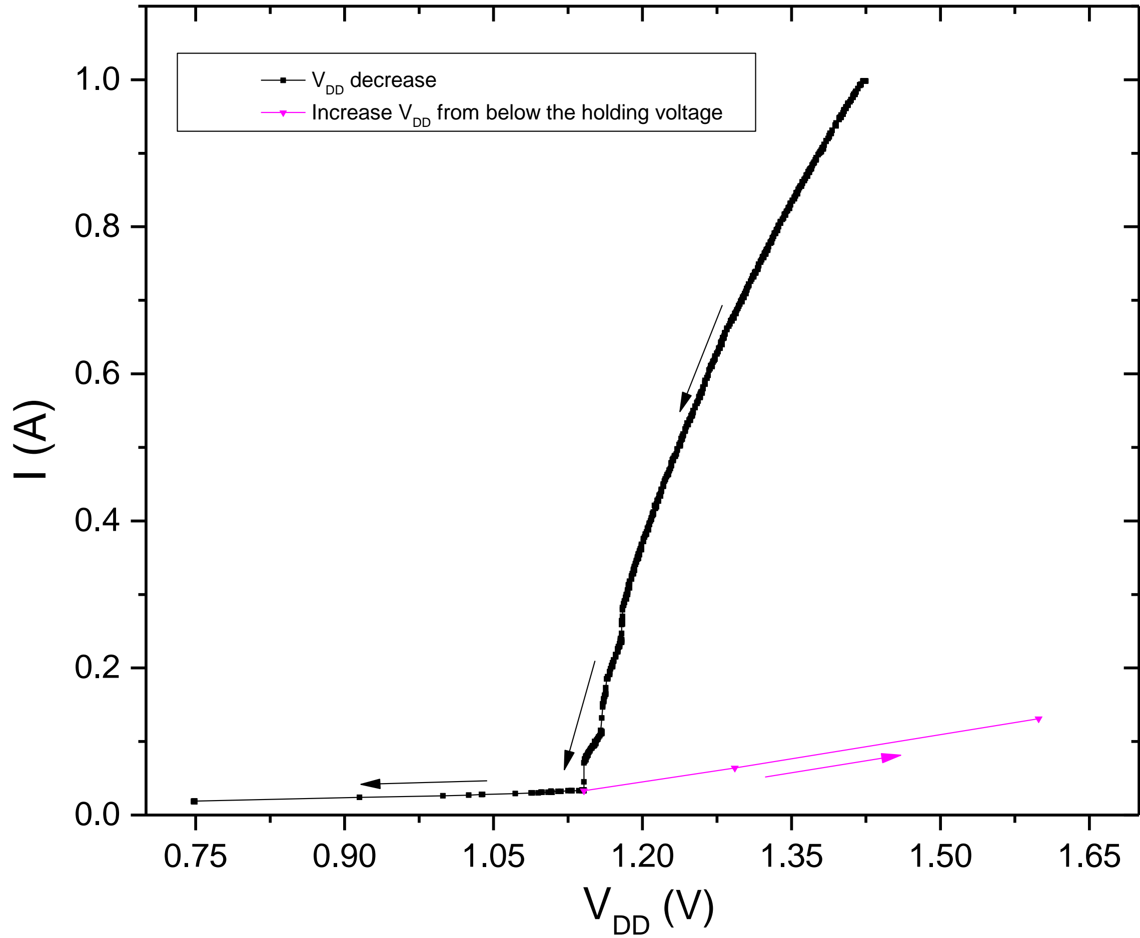


Fig. 3-3 I-V characteristics of the latch-up state after being triggered by the alpha source

voltage for different supply voltages. The holding voltage decreases linearly when the temperature increases from room temperature (~25 ºC) to 125 ºC, which indicates the increasing single-event latch-up vulnerability with increasing operating temperature.

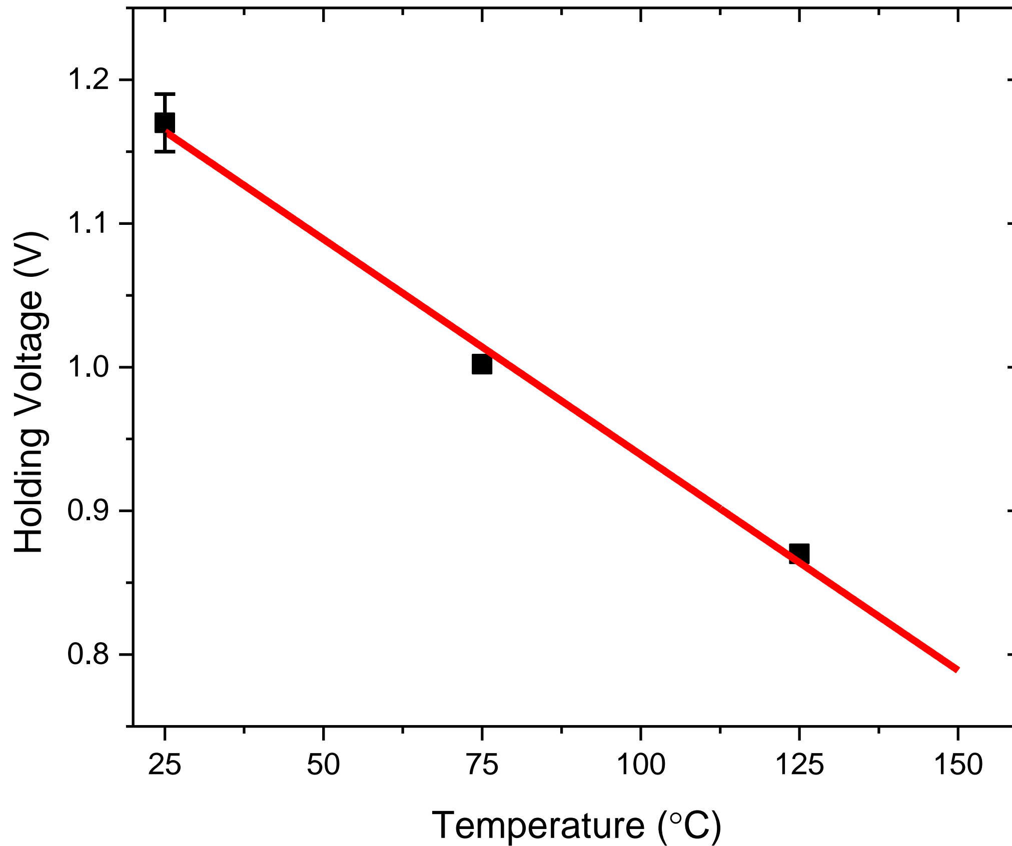


Fig. 3-4 The holding voltage for different temperatures

2. ***Experiment Results of the Tests of Frequency Change-Triggered High-Current State***

The initial test consisted of changing operating frequency from a low value (2.5 MHz) to a high value (above 500 MHz) while keeping the supply voltage below 1.15 V. Increasing frequency increased the IC current due to increased dynamic current. When the operating frequency was lowered to 2.5 MHz, the current value decreased to original value as seen in Fig. 3-5. In Fig. 3-5, the current was ~40 mA at 2.5 MHz and ~1.5 A at ~800 MHz. This is the expected behavior for a circuit operating normally. These frequency values are for nominal supply voltage. As mentioned

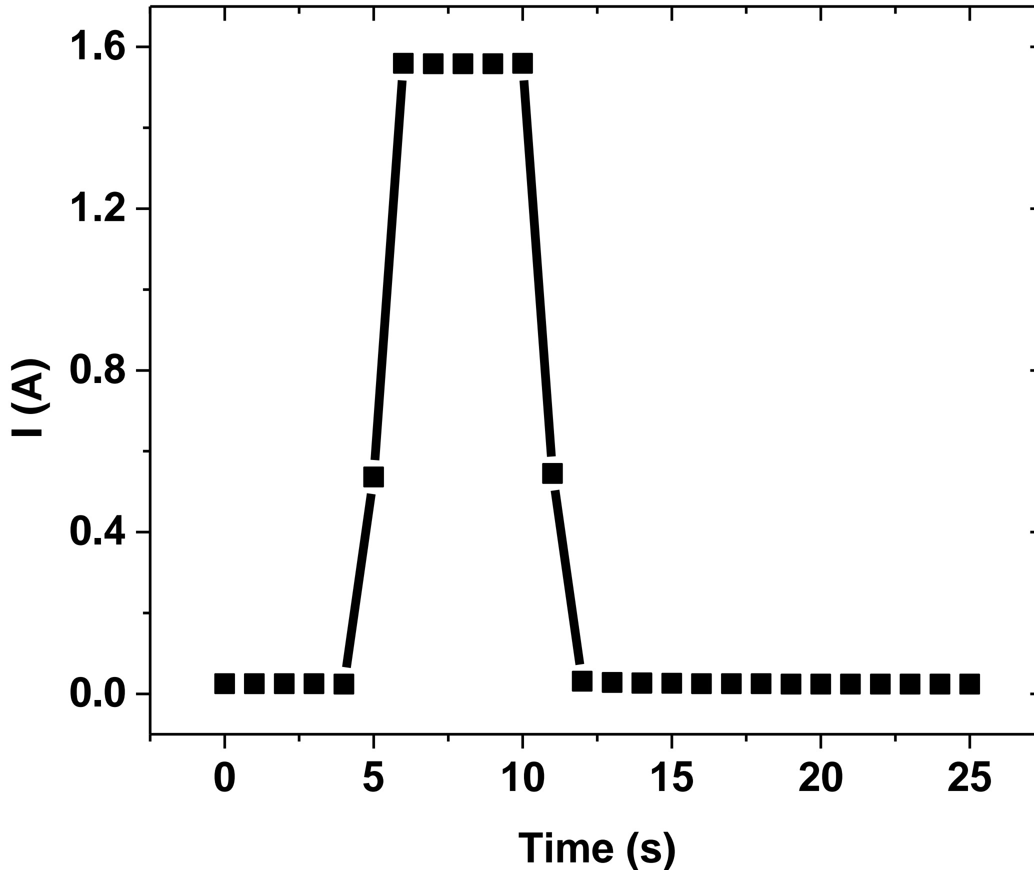


Fig. 3-5. The current behavior related to the change of operating frequency at V_{DD} = 1 V. The frequency was increased from 2.5 MHz to 700MHz at time ~ 5 s and then was reduced to 2.5 MHz at time ~ 11 s.

earlier, different supply voltages will yield different frequencies. Irrespective of the operating frequencies, the behavior of the failure mode described here does not change.

When the supply voltage was increased beyond 1.15 V, the latch-up like failure mechanism was observed. When the frequency was increased from 2.5 MHz to ~834 MHz (actual frequency measured at this supply voltage) with elevated supply voltage, the current increased as expected due to increased dynamic current requirements of the circuit. But when the operating frequency was changed back to 2.5 MHz, the current didn't decrease back to a value that was observed for 2.5 MHz frequency, as shown in Fig. 3-6. It must be noted that this latch-up like high-current state

was not observed every time this change in frequency was carried out. For these experiments, if the high-current state was not observed after the process (changing frequencies as shown in Table 2.1) was repeated 20 times, it was assumed that the high-current state will never occur under that specific conditions. The supply voltage was gradually increased (while keeping the temperature and the frequency settings unchanged) to test the critical voltage point when the high-current state occurred. This behavior was observed for all supply voltage values above 1.15 V and all frequency values higher than ~834 MHz (actual frequency measured at this supply voltage) at room temperature. The threshold frequency value for ~1.15 V at room temperature is ~ 834 MHz.

Once high-current state was achieved, the supply voltage was gradually reduced to determine if there is a holding voltage (similar to what is seen for latch-up events) beyond which the supply current value returns to normal values for circuit operation. Fig. 3-7 shows the supply current as a function of supply voltage after high-current was achieved. Current-voltage characteristics were very similar to what is observed for latch-up. In the beginning range (1.12 V ~ 1.2 V) of the supply voltage, the current gradually reduced with decreasing supply voltage. The current will go back to the elevated value if the supply voltage was increased again (similar to what is observed for latch-up events). The current will start to reduce significantly if the supply voltage was reduced close to holding voltage. Results in Fig. 3-7 (for room temperature) indicate the holding voltage for this high-current state is approximately 1.08 V. After the high-current state was removed, the current was measured with increasing supply voltage (while keeping operating frequency at 2.5 MHz), as it is shown in the red curve of the Fig. 3-7. It is clear that the current value will not go back to the elevated value related to the high-current state, indicating the disappear of this high-current state below the holding voltage. The holding voltage of 1.08 V is similar to the holding voltage for latch-up that was observed for this technology.

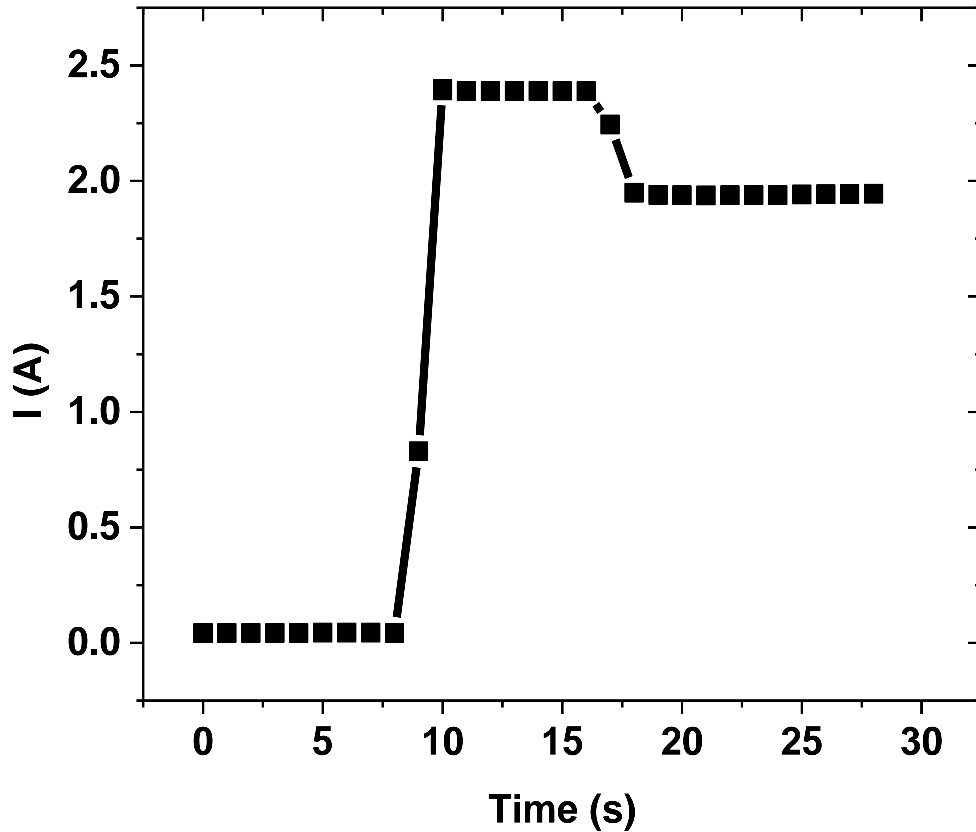


Fig. 3-6. The current behavior related to the change of operating frequency at V_{DD} = 1.3 V. The frequency was increased from 2.5 MHz to 700 MHz at time ~ 8 s and then was reduced to 2.5 MHz at time ~ 15 s

The effect of temperature is also worth noting on the holding voltage. Previous results have shown that the latch-up sensitivity is strongly dependent on temperature [25, 26, 27, 28]. The threshold LET values for latch-up to occur for radiation environments were reduced by about a factor of 2.5 at 125 ºC relative to room temperature. The results also show that the latch-up cross-section increases with increasing operating temperature. It is expected that the temperature will also affect this latch-up like high-current state. Changing the temperature of the 7-nm die during the test, showed a decreasing trend for the trigger voltage, as seen in Fig. 3-8. The slope of the

curve was dependent on the value of the high-frequency used during the test (low frequency was always kept at 2.5 MHz). As the frequency increased, the trigger voltage showed a decreasing trend. For the highest temperature and frequency tested, the trigger voltage reduced to ~0.97 V.

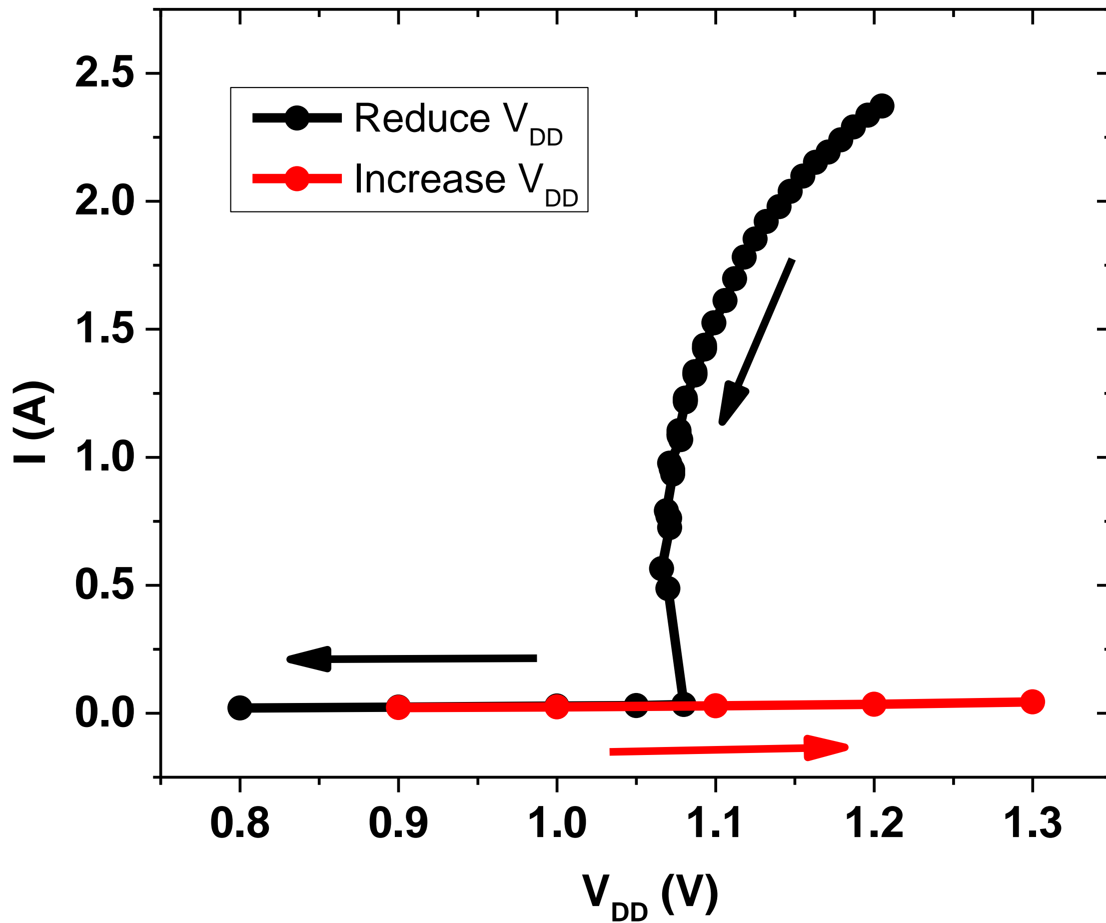
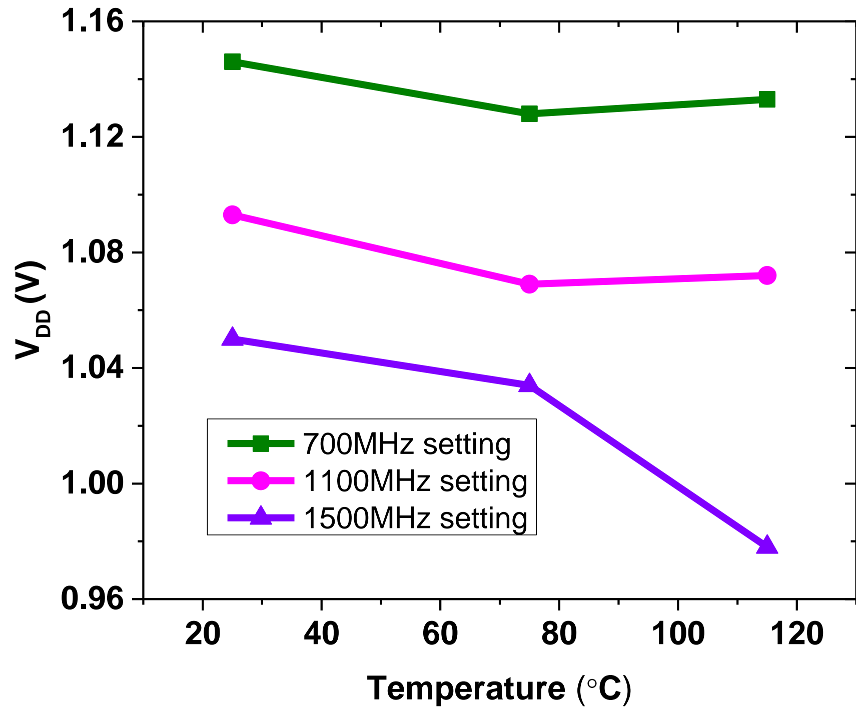


Fig. 3-7. The current versus V_{DD} behavior after high-current state was achieved. Black arrows indicate the direction of change in V_{DD} after the high-current state was observed. Red arrow indicates the direction of V_{DD} after the high-current state was removed.



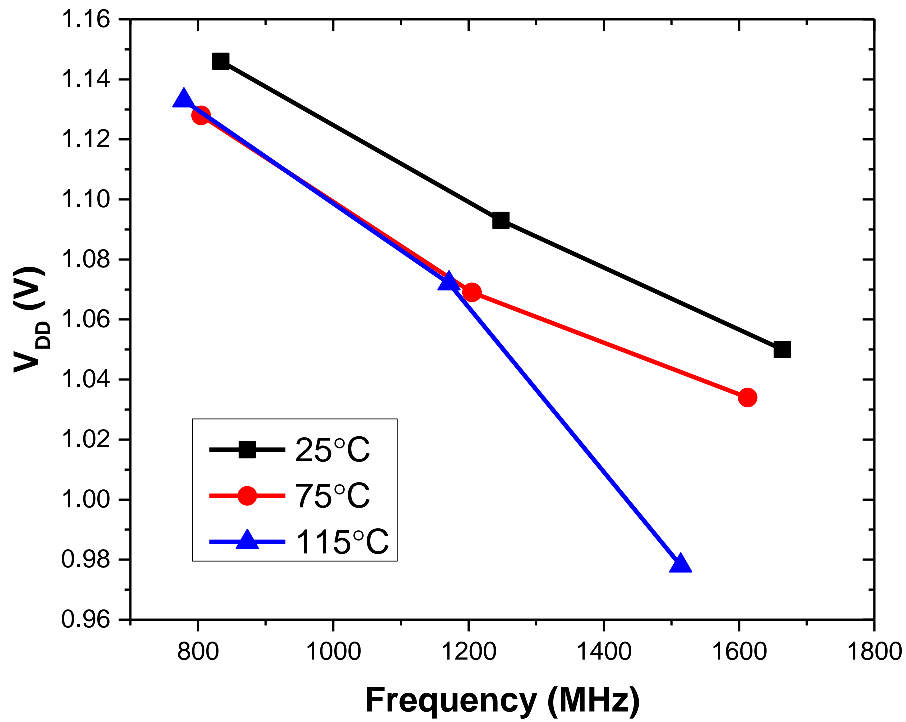


Fig. 3-8. The trigger V_{DD} for a given frequency at different temperatures.

CHAPTER IV

Analysis and Conclusions

The objective of the work illustrated in this thesis was to provide an initial analysis for the behavior and mechanisms of the phenomena of the high-current state triggered in ICs fabricated at the 7-nm node. The performance of the high-current state, either through SEL event or operating-frequency change, have been introduced in previous chapters. Experimental results show that the SEL can be triggered at the 7-nm bulk FinFET node with some operating conditions. The SEL FIT rate increases when the supply voltage increases. The SEL FIT rate also increases significantly when temperature increases. The results also show that the holding voltage is strongly dependent on temperature.

SEL FIT rate was characterized for various supply voltage and operating temperatures. The nominal voltage for the IC is ~ 0.75 V. When the supply voltage is lower than 1.4 V, whether the SEL event will still occur remains an issue since the time for an event to be triggered will increase significantly for lower supply voltage. However, this does not mean that the SEL event will not happen at lower supply voltage. SEL FIT rate at lower supply voltage can be obtained by extrapolating the curve. If a specific supply voltage value is defined as the critical value at which the SEL event 'will never happen', then the related supply voltage is viewed as the threshold value of a SEL event. It is clear that the increasing temperature will lead to reducing value of the threshold triggering supply voltage. For elevated temperature, the threshold value may reach near the nominal voltage. It will be an important information for the designers and users that will implement this technology.

Initial observation indicates that frequency-induced high-current event is similar to a latch-up event. Sudden supply current increases are observed in both latch-up event and frequency-induced high-current event. Both show similar trigger voltage and holding voltage values. In FinFET technology, the doping levels are relatively low, which leads to the relatively high resistivity of substrate and well. When the frequency is increased to the GHz level, the voltage-drop on the parasitic well- and substrate-resistors will increase due to the increase of the substrate-injection current, as it could be shown in the Fig. 4-1. The common-emitter current gains for npn and pnp transistors (respectively βnpn and βpnp) are higher than that in planar technology [13, 22]. It is postulated that all these factors combined may be sufficient to forward bias base-emitter junction of a parasitic bipolar transistor to initiate a latch-up, which may be responsible for initiating a frequency-induced high-current state. This novel failure mechanism has been characterized by

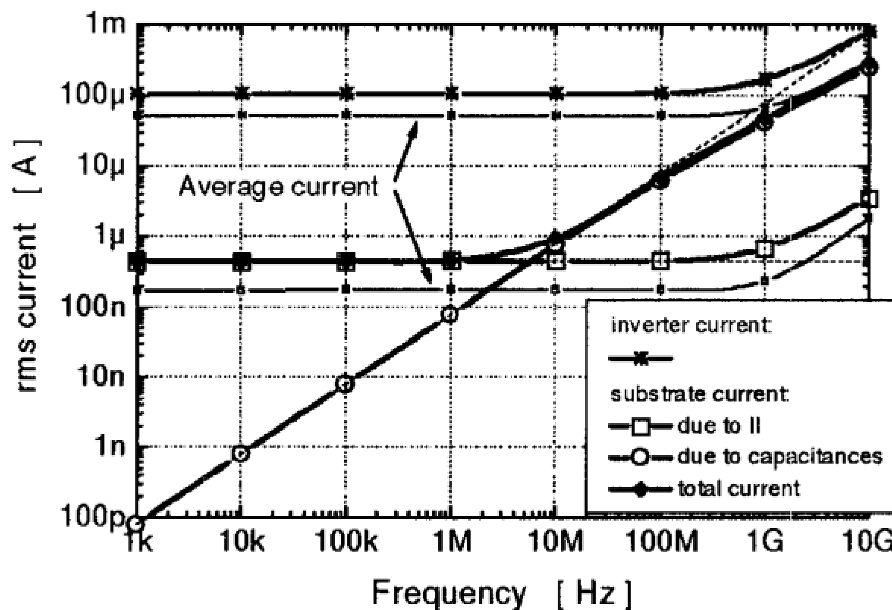


Fig. 4-1 The simulated substrate and inverter currents in a single inverter, as a function of input frequency. The substrate current, including impact ionization current, capacitive coupling, etc., begins to increase with increasing frequency when the operating frequency reaches ~100 MHz [29].

varying temperature and frequency along with supply voltage. Such a failure event poses a serious reliability threat for ICs operating at GHz range of frequencies.

High-current states triggered in the circuits, including single-event latch-up state and operating frequency-triggered high-current state, have been discussed in this thesis. Both phenomena have similar latch-up like behavior. In both cases, the current stays at relatively high level and demonstrate similar current behavior when the voltage is being reduced from relatively high voltage. Both types of high-current state are tightly connected, which provide valuable information in the field of the reliability of the digital circuits for researchers and engineers.

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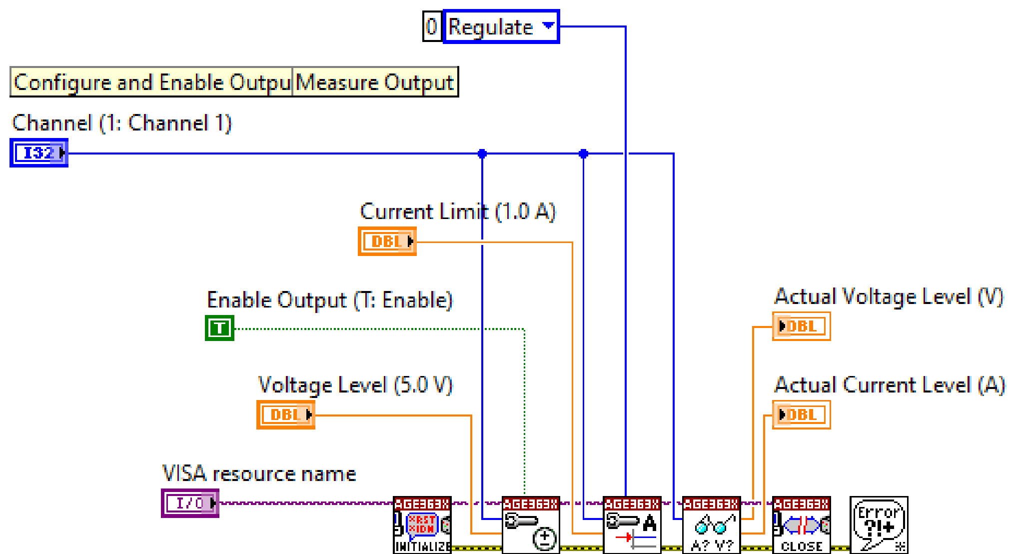
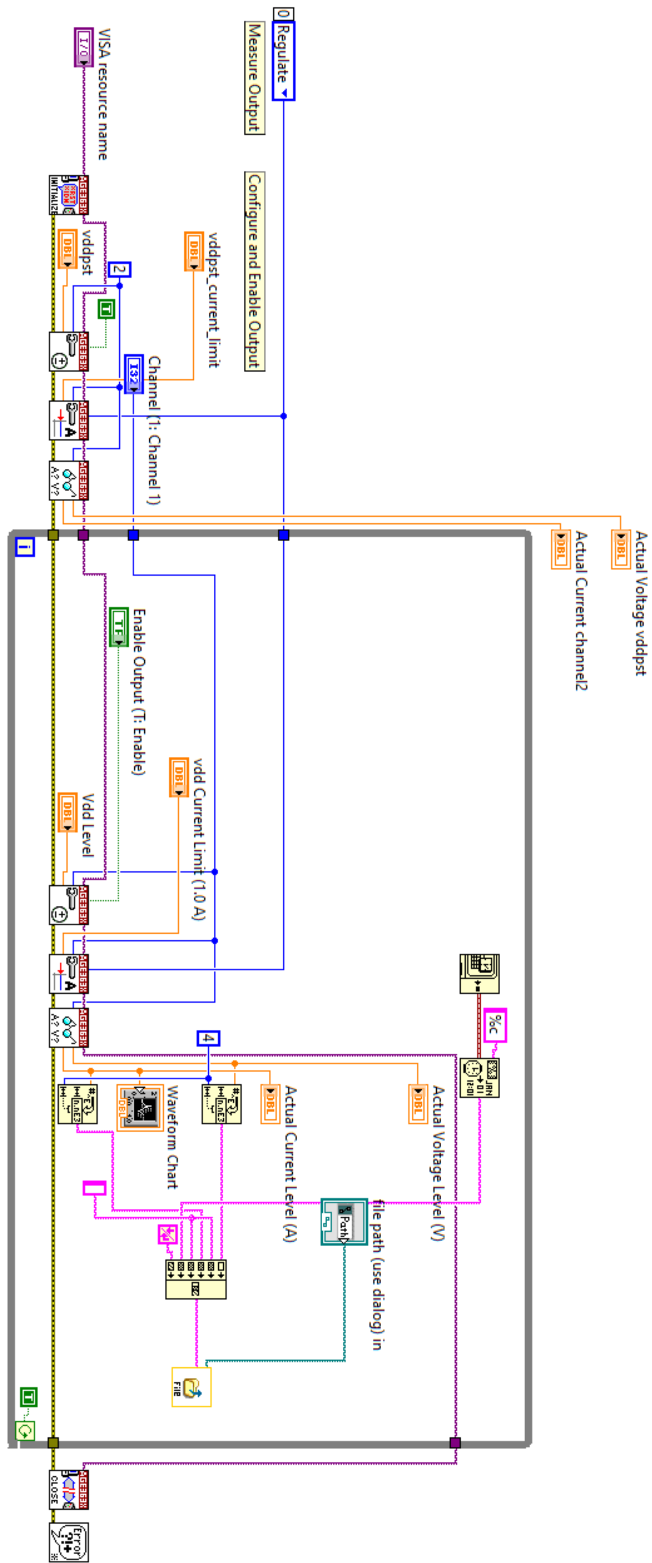
APPENDIX A

LabVIEW Program Used in Current Behavior Measurements

The LabVIEW program used for measuring current behavior is created and modified based on the official LabVIEW Instrument Driver for Agilent E363X Series Power Supply. The related website for downloading the driver and the official documents is: http://www.ni.com/downloads/instrument-drivers/. The original modules and the program with modification used in the experiments are shown as following.



The original module used to generate the program for measuring the current behavior



The LabVIEW program used for monitoring the current-time behavior