TOTAL IONIZING DOSE EFFECTS IN ADVANCED CMOS TECHNOLOGIES

By

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CHAPTER I

INTRODUCTION

A. Overview

As complementary metal–oxide–semiconductor (CMOS) technology has scaled, the device aspect dominating the total-ionizing dose (TID) response has changed. Local oxidation of silicon (LOCOS) isolation has been used for many years, but all commercial IC suppliers have replaced LOCOS isolation with shallow-trench isolation (STI) for advanced submicron technologies due to superior scalability, plus electrostatic effects in the bird's beak regions. For sub-100 nm technologies the scaling of SiO_2 gate oxides in bulk CMOS devices to thinner dimensions has reduced, almost to elimination, the significance of threshold-voltage shifts due to TID radiation-induced charge buildup in ultrathin SiO_2 gate oxides [1]. As a result, the dominant TID effect in most bulk CMOS technologies is now charge buildup in the STI [2]. Charge trapped in the isolation dielectric, particularly at the Si/SiO_2 interface along the sidewalls of the trench oxide, creates a leakage path that becomes the dominant contributor to off-state drain-to-source leakage current in n-channel MOSFETs [3]. This effect is illustrated schematically in Fig. 1.1, which shows (a) the edge leakage path from drain-to-source on the planar view of the nMOSFET and (b) the device cross-section with the oxide trapped charge buildup in the STI, which induces the leakage path.

Also, scaling is making the use of some radiation hardened by design (RHBD) structures, namely edgeless devices, prohibitive due to design rules for manufacturability and lithography limitations. Wider devices are often laid out with fingers, creating multiple active/STI edges.

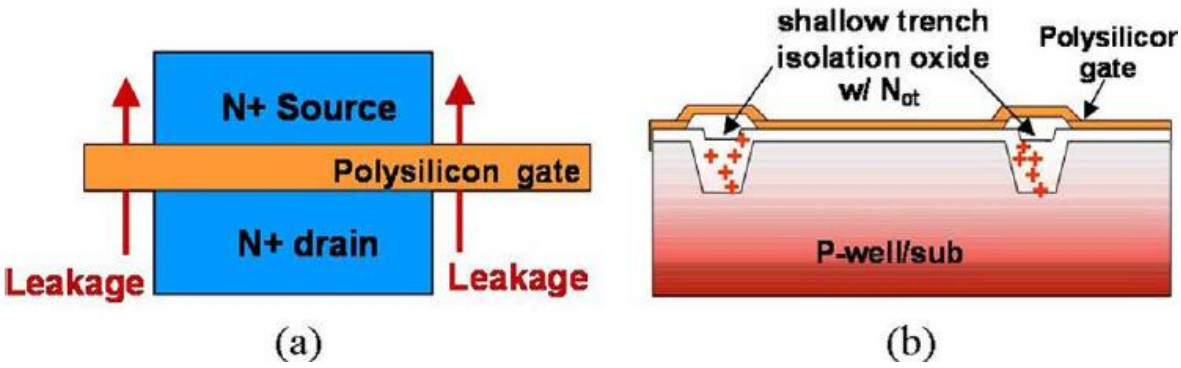


Fig. 1.1. (a) Illustration of drain-source leakage path in an nMOSFET and (b) its cause: positive oxide trapped charge buildup in the isolation oxide [3].

Understanding factors that determine the edge-related leakage current, and possible variability in it, is important since characterization of a process for TID response often involves measurement on a relatively small number of devices.

Silicon dioxide has been the primary gate insulator since MOS ICs were first developed. To achieve the drive currents required by advances in IC technology, gate dielectrics are becoming extremely thin. They have reached the point where electron tunneling can cause prohibitively large increases in power consumption. To circumvent this problem, alternate gate dielectrics with high dielectric constants (also referred to as "high-k" dielectrics) have been introduced. By using a high-dielectric-constant gate material, a thicker dielectric can be used to obtain the equivalent capacitance of thinner dielectrics. For these thicker high dielectric constant insulators, electron tunneling is reduced. However replacing SiO_2 with high-k materials leads to two problems, threshold voltage pinning and phonon scattering, both limiting the transistor's switching speed. The solution is to use metal gates, using different metals for the NMOS and PMOS transistors. In selecting the gate metal material, the work function of the metal gate should be given the most consideration, since it determines the threshold voltage (V_t) of the MOSFET.

Silicon-on-insulator (SOI) technology is a very promising candidate for extending the limits

of silicon technology as we approach the end of the International Technology Roadmap for Semiconductors (ITRS). Among its advantages over bulk silicon devices, one could highlight the immunity to short channel effects (SCE), the reduction in parasitic junction capacitance and the lower sensitivity to process variability. However in addition to charge buildup in the STI, charge trapping in SOI buried oxides also affects the TID sensitivity; therefore, it is important to understand the sensitivity of SOI devices to charge trapping in the STI as well as the buried oxide. The 32 nm IBM PDSOI technology uses a high-k dielectric and metal gates; since the doping profiles depend on the gate work function it is important to understand the effect of doping changes associated with the metal gate work function on the TID response.

This work examines key aspects of TID response of advanced CMOS technologies using experiments (ARACOR X-ray) and TCAD simulations. Understanding the key aspect of the TID response of scaled down technologies will give insight into understanding the implication for future emerging technologies. The TID sensitivity of edge-related leakage current in CMOS bulk and SOI devices to key parameters: STI process variations, combined with sidewall doping variations as well as layout related stress effects are being studied.

Process variations (namely the STI process, sidewall doping and mechanical stress) are being investigated to account for the radiation response and variability in scaled down technology nodes. These characteristics may in part account for observed differences among supposedly identically processed devices, between devices from various vendors at the same technology node, and between low power and high performance process variants. Implications for characterizing variations in TID sensitivity due to processing are noted.

The experiment and simulation details are covered in chapter II. The STI-stress effect on TID-induced leakage current is examined using experimental results, which will be covered in

chapter III of this thesis. The physical mechanisms that affect the TID sensitivity are considered, particularly changes in the doping profile of the channel edges and at the STI sidewall, due to STI stress.

Space applications using advanced CMOS technologies require accurate evaluation of the variability of total-ionizing dose (TID) response and its dependence on individual device layout. Device-to-device variability between nominally identical devices and systematic variability that depends on the local structure can affect circuit-level TID response. In this work the variability in sub-100 nm technologies is examined; device-to-device variability is compared for two bulk technologies (65 and 90 nm) and three process variants (low, standard, and high threshold voltage). These results illustrate the effects of process-induced variability (including stress) on the radiation response of MOS devices and integrated circuits and are presented in chapter IV.

Finally SOI technologies are considered, and the results are presented in chapter V. As CMOS has scaled to sub-100 nm dimensions, the silicon has also scaled to sub-100 nm thickness, and the body doping has increased (similar to channel doping in bulk devices). In this work, the sensitivity of device I-V characteristics to charge trapped in the sidewall oxides and BOX for fully depleted and partially depleted SOI devices in both 90 nm and 45 nm technologies are investigated. Moreover 32 nm PDSOI devices using high-k gate metal are examined; the sensitivity of device I-V characteristics to gate work function and to charge trapped in the sidewall oxides and BOX are investigated.

Chapter VI concludes the dissertation, outlining the original contributions of this work to the existing literature.

B. CMOS scaling and isolation techniques

The evolution of IC density requires that device geometries scale proportionately; technology scaling involves a decrease of the channel length, width and gate oxide thickness, with an increase of the doping concentration. Therefore, as transistors get smaller, the voltage and the current are reduced and thus the transistor can switch faster and use less power. Not only is the geometry changing from one device generation to the next, but also the processing techniques, materials, and processing tools are changing. Commercial requirements (transistor density) have driven the basic isolation methods, impacting MOS radiation hardness. Therefore, in some cases it has been necessary to develop methods to improve the radiation tolerance of the corresponding approaches.

To meet increasing demand for hardened ICs of greater device density, a hardened field oxide structure smaller than the direct-moat type (which is a type of radiation-hard field oxide developed by Sandia National Laboratories) was necessary [4]. The semiconductor industry pursued various new lateral oxide isolation approaches, such as local oxidation of silicon (LOCOS), poly-buffered LOCOS, and selected poly-Si oxidation (SEPOX), each having hardening advantages and disadvantages. Of major concern to the IC builder is the extent of oxide encroachment, such as the LOCOS "bird's beak," which reduces active device area and causes increased radiation sensitivity due to the mechanical stress in the oxide. To meet the scaling requirements, STI approaches, with no bird's beak encroachment, are commonly used. Fig. 1.2 shows a comparison of LOCOS and STI structures, showing how the effective channel width (W_{eff}) is reduced by the "bird's beak" inherent to LOCOS. As seen from Fig. 1.3, due to yield problems, LOCOS lateral isolation was abandoned for technology generations below 0.4 μm [5].

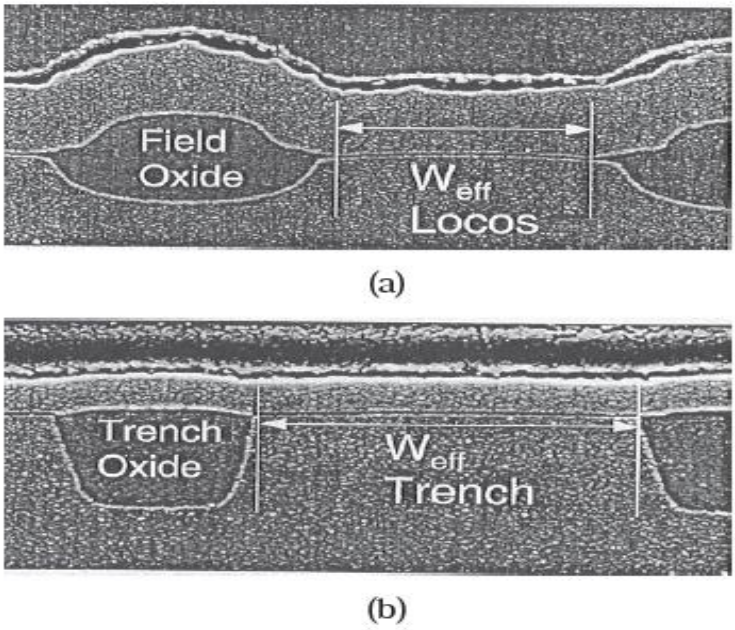


Fig. 1.2. Transmission electron micrograph (TEM) images of (a) LOCOS and (b) trench regions (STI), showing less encroachment on the channel width (W_{eff}) for trench than LOCOS [4].

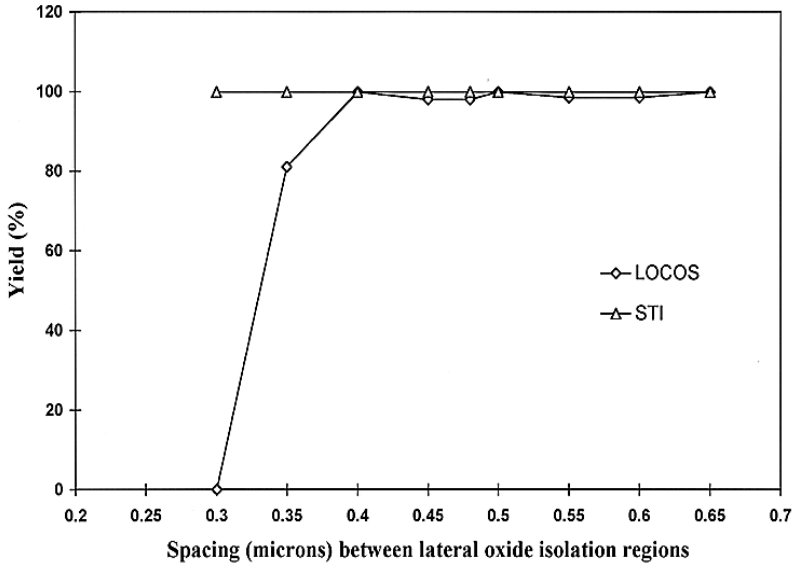


Fig. 1.3. Yield versus scaling size for LOCOS versus trench, showing reduced yield for LOCOS for channel scaling below 0.4 µm [4].

However, there is a wide variation in the radiation hardness of STI. In some cases, TID

failure levels for STI were observed at less than 10 krad(SiO_2) [2], while in other cases radiation hardness levels of greater than 100 krad(SiO_2) were measured on commercial technologies. It is understood that the hardness of the STI region depends on a number of features, including geometry and type of trench refill oxide.

C. Shallow trench isolation

a. STI variability

One of the motivating factors in this research was the observation that different fabrication lots with supposedly identical processing, and nearly identical pre-irradiation leakage currents, could exhibit vastly different TID response with one lot showing a minimal increase in leakage and the other a dramatic increase as shown in Fig. 1.4 [6]. This difference was hypothesized to be related to differences in the STI.

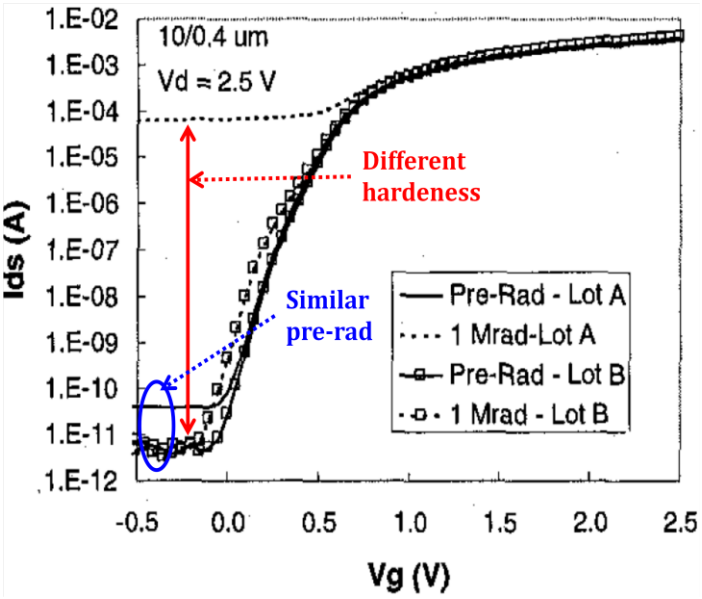


Fig. 1.4. Potential variability in the total dose hardness of two identically processed lots (without hardening) [6].

Key parameters that may affect edge leakage, as well as TID response, are the shape of the transition from the active to the isolation region and the doping of the active silicon region along the sidewall [2], [3], [8].

b. TID response variation

i. Foundry-to-foundry variation

In [2] it was demonstrated that recessed STI fill could exacerbate the TID response in a 0.5 μm CMOS technology. The concept of recessed fill is discussed in detail below. More recently it was demonstrated that radiation-induced leakage current and threshold-voltage shifts in narrow transistors may depend strongly on the details of edge effects [9], and that significant differences in degradation of NMOS transistor characteristics can be observed at the 130 nm technology node from different manufacturers, as shown in Fig. 1.5 [10].

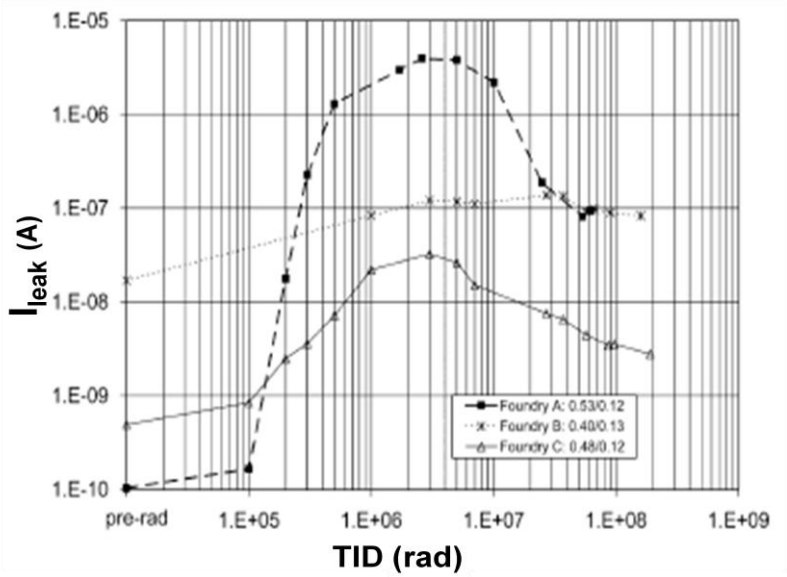


Fig. 1.5. Leakage current evolution with TID of NMOS core transistors from different foundries [10].

This large foundry-to-foundry variation may be attributed to differences in the fabrication processes, namely in the STI oxide growth/deposition process and planarity, and/or in the doping profiles of the devices [10]. Further, within a given manufacturer's process, it is possible that the degree of recess may vary across a wafer depending on device widths and inter-device spacing (process loading) for a specific design, or from lot to lot or fabrication location. Such subtle variations may not affect standard electrical monitor measurements or be important for normal electrical operation, but may have implications for the TID response of a large circuit. Finally, a single manufacturer may have variations in nominal processes to target high performance vs. low power applications, typically including differences in doping to adjust leakage and threshold voltages; such doping differences may have implications for the TID response.

ii. Sample to sample variation

In [6], it was demonstrated that different fabrication lots with supposedly identical processing, and nearly identical pre-irradiation leakage currents, could exhibit vastly different TID response, with one lot showing a minimal increase in leakage and the other a dramatic increase. STI processing and substrate doping profile also play important roles in the TID response variability. In fact, not only devices fabricated in different foundries but also those manufactured in the same foundry, even on one wafer, have variations in physical and electrical characteristics [12]. The samples located at different wafer locations have different TID responses, as represented in Fig. 1.6, which shows the off state leakage current distribution of twenty-seven I/O NMOS transistors after 100 krad(SiO_2) irradiation. The distribution map indicates that the leakage current at the left part of the wafer seems to be smaller than that at the right part. As we know, this leakage current is related to the STI. So the STI quality plays a

crucial role in determining this leakage. In fact, the STI process is very complicated and many process steps can impact its profile, which will be discussed in detail below. Different STI profiles may lead to different amounts of charge trapping, thus showing different degrees of leakage current degradation. Another important factor is the sidewall doping concentration.

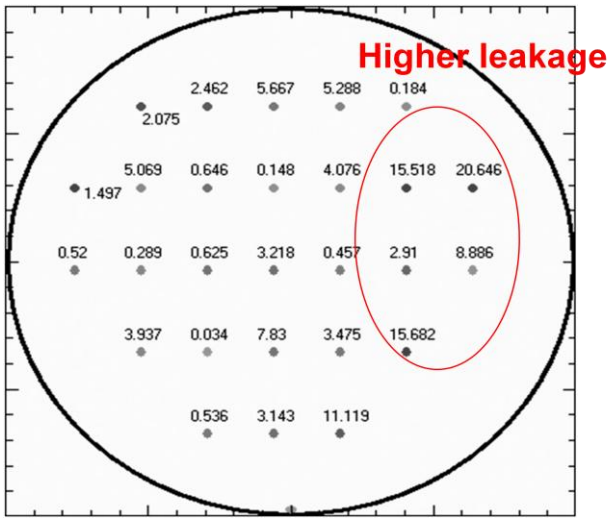


Fig. 1.6. Off-state leakage current distribution on the wafer map at a dose level of 100 krad(SiO_2) with units of 10^{-9} A (nA) [12].

Another example of sample-to-sample or device-to-device variability is represented in Fig. 1.7, which shows the off-state leakage current evolution with TID of 90 nm NMOS core transistors from different dies (from the same wafer). The same NMOS device was measured in three different dies (all three dies are from the same wafer). The results show similar pre-irradiation off state leakage current (I_{off}), but very different post-irradiation I_{off}.

Once again, key parameters that may affect pre-irradiation edge leakage, as well as TID response, are the shape of the transition from the active to the isolation region, the doping of the active silicon region along the sidewall [2], [3], [8], and finally layout related stress effects that will be discussed in more detail later in this paper.

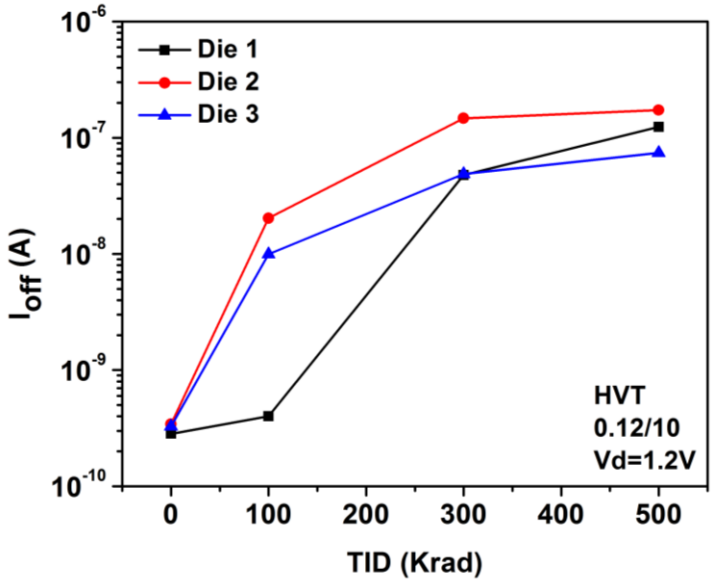


Fig. 1.7. Off-state leakage current evolution with TID of a 90 nm NMOS core transistors from different dies [13].

c. STI edge topology

During the fabrication process it is challenging to control planarity precisely, and trench fill can be recessed intentionally or unintentionally. If the trench oxide becomes recessed below the silicon active region the gate oxide will wrap around the silicon corner as illustrated in Fig. 1.8.

An example of variation in amount of trench recess for two STI regions with different amounts of recess is shown in Fig. 1.9. The recess depth of STI-B is 2X that of STI-A, leading to a corresponding increase in sidewall gate [11]. The peak electric fields at the trench corner region are further enhanced if the trench fill is recessed below the trench corner, and high electric fields in the trench corner region have been shown to create anomalous humps in the current-voltage characteristics, even for un-irradiated devices [2].

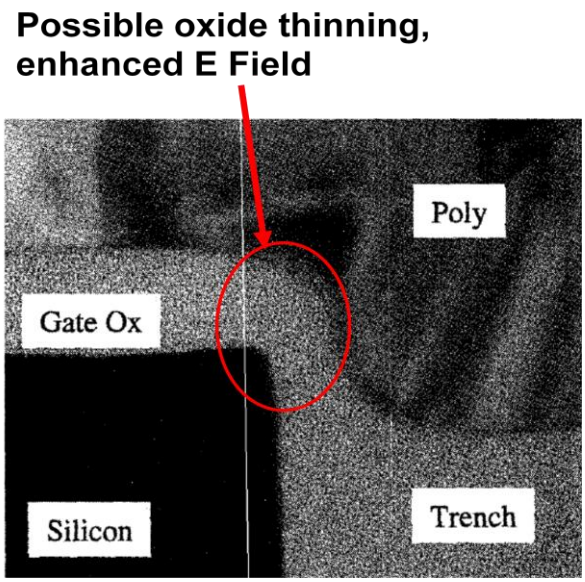


Fig. 1.8. TEM of shallow trench isolation that is recessed below the silicon active region and the trench corner shows the gate oxide and gate electrode wrapping around the corner [2].

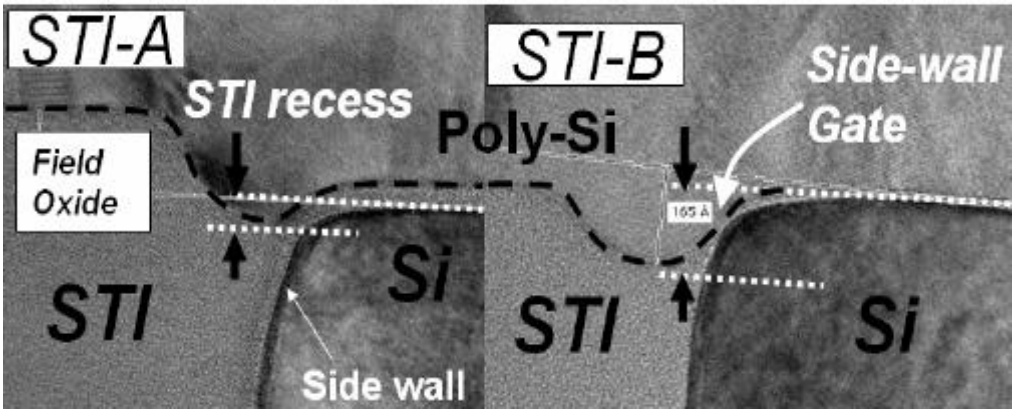


Fig. 1.9. TEM cross-section at the active-to-field oxide region highlighting the differences in STI recess for two isolation processes [11].

Fig. 1.10 shows the subthreshold I-V characteristics of three different trench profiles: planar, recessed and overfilled. The results show a large hump for the recessed trench; for a

planar trench the hump is significantly reduced and no hump exists for an overfilled trench.

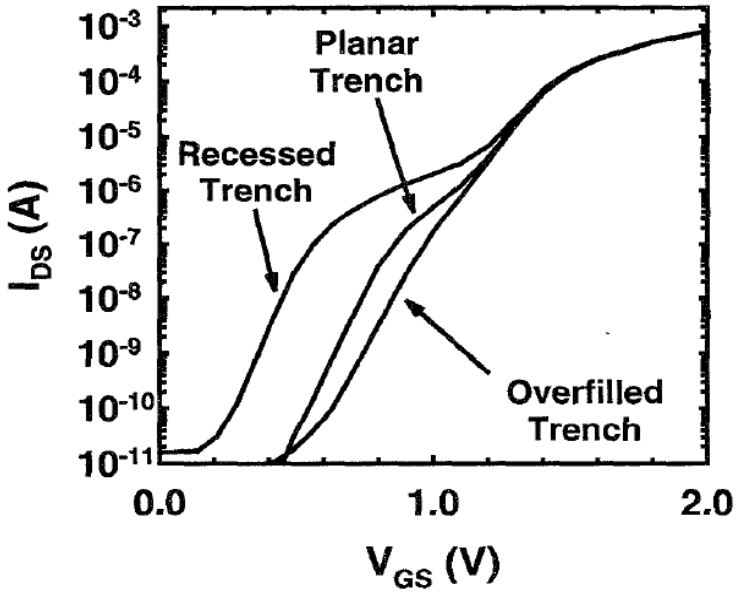


Fig 1.10. Simulated I-V characteristics for three different trench profiles. For the overfilled trench profile, the trench insulator extends 100 nm above the trench corner [2].

The effects of polishing time are explicitly shown in Figs. 1.11(a) and 1.11(b), which show the pre- and post-radiation I-V curves for devices from lots with two amounts of polishing time. These two devices are from the same lot, with a processing split at STI polish representing the expected polishing time process window. The device with the longer STI polish has two orders of magnitude greater leakage at 100 krad(SiO_2) than the device with reduced polish time. The reduced amount of trench recess for reduced polish times translates into less radiation-induced edge leakage. However, there is a process trade-off, since the shorter polish may leave trench fill oxide over the pad nitride. This oxide will prevent the nitride from being stripped off, resulting in non-functional devices in those areas [6]. The change in polish time also affects the variability of the total dose response for unhardened STI.

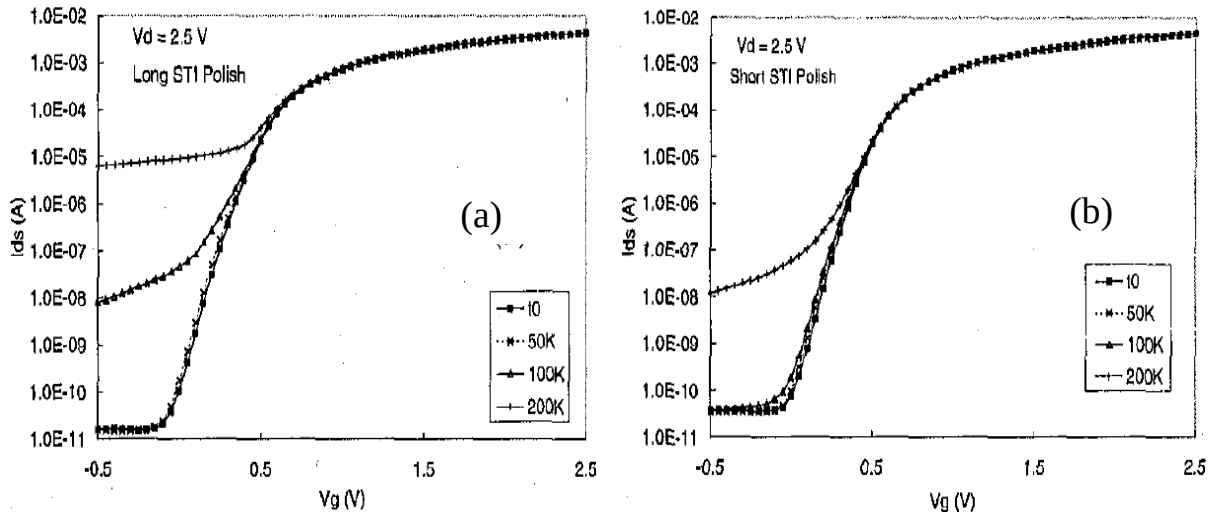


Fig. 1.11. I-V curves, pre- and post-radiation, for unhardened devices, with either (a) long STI polish time, or (b) short STI polish time. Device size is 10/0.4 um [6].

d. Sidewall doping

The primary causes for radiation-induced off-state drain-to-source leakage in bulk MOSFETs are:

- The reduction in the threshold voltage or
- The increase in current for the parasitic n-channel MOSFET associated with the edges of the "as drawn" device shown in Fig. 1.12(a).

Prior to radiation exposure, the leakage current of the parasitic devices is low due to the relatively large effective gate oxide thickness (high threshold voltage of the parasitic devices) relative to the "as drawn" structure and small effective width. After irradiation, the threshold voltage shift in the parasitic edge transistors ultimately leads to an increase in the off-state leakage current.

In addition to negative voltage shifts, the drive current of the parasitic nFET also increases significantly as shown in Fig. 1.12 (b).

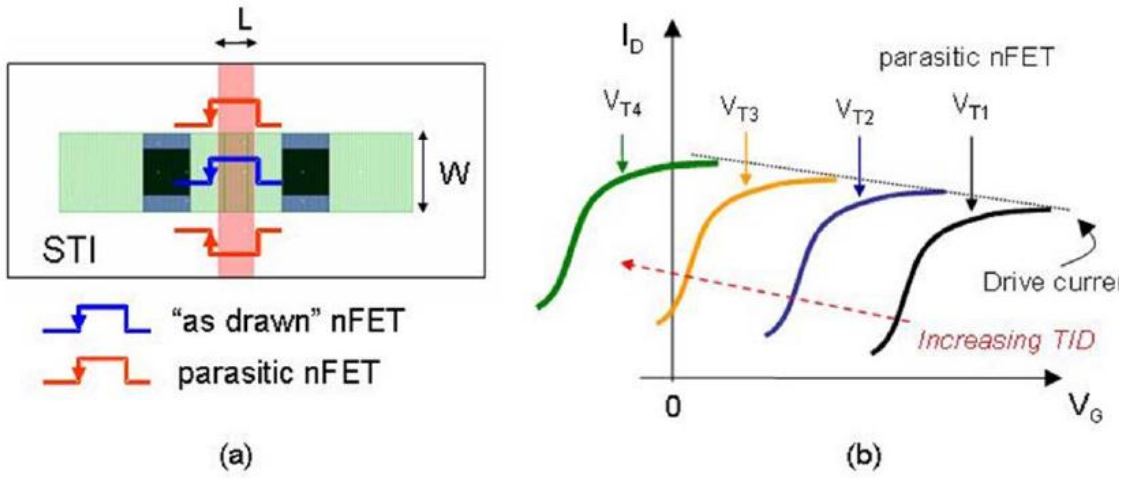


Fig. 1.12. (a) Illustration of the circuit-level models associated with the n-channel MOSFET with parasitic nFETs, and (b) the effects of increasing TID radiation exposure on the threshold voltage and drive current of the parasitic nFET [3].

This occurs because the effective width of the parasitic transistor, to which drive current is proportional, increases as surface along the STI sidewall inverts in response to positive oxide charge buildup [3]. The degree to which oxide charge can invert this surface is also inversely proportional to the doping concentration along the sidewall [3]. Thus, a higher doping concentration in the p-type body will typically mitigate the effects of fixed oxide trapped charge in the STI.

Fig. 1.13 illustrates the impact of using enhanced sidewall doping and n+ pullbacks on the simulated *I-V* characteristics of both the active transistor and the parallel parasitic sidewall transistors. The simulations were performed by physically splitting the gate contact at the trench corner to separate the contributions due to active and parasitic transistors [2]. Also shown are the simulated parasitic sidewall I-V curves with enhanced sidewall doping, and with combined sidewall implants and a 0.3 μm n+ pullback. Increased sidewall doping alone increases the parasitic threshold voltage above the active gate threshold and thus no noticeable hump is observed in the pre-irradiation *I-V* curve.

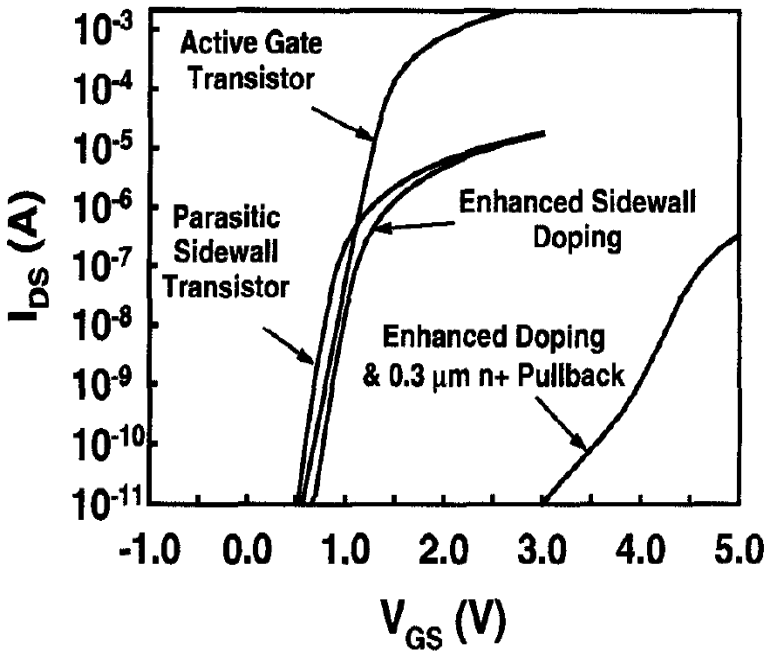


Fig. 1.13. Simulated subthreshold I-V characteristics of both the active transistor and the parasitic sidewall transistors. The impact of using enhanced sidewall doping and n+ pullback on the parasitic sidewall transistors is shown [2].

e. STI process variations affecting TID response and variability

As mentioned previously, the STI profile plays an important role in the leakage degradation [1]-[11], where different process variations may impact the radiation response. Before going into the STI process variations that affect the TID sensitivity it is important to review the STI process flow, for which a typical process is described here:

(1) Pad oxide growth and silicon nitride deposition:

A thin (100-Å) layer of silicon oxide is grown using high temperature dry oxidation, followed by the deposition of a 1500-Å layer of silicon nitride using chemical vapor deposition (CVD). The silicon nitride acts as a hard mask for the trench etch steps as shown in Fig. 1.14 (1).

(2) Trench etch:

A nitride dry-etch step is followed by a silicon etch step to create deep (0.36 to 0.5 μm) trenches as shown in Fig. 1.14 (2).

(3) Liner oxide:

A thin thermal oxide layer (~15 nm) called liner oxide is grown on the trench walls as shown in Fig. 1.14 (3).

(4) Trench fill:

STI gap filling utilize high density plasma (HDP) deposition technique to produce high-quality oxide filler as shown in Fig. 1.14 (4).

(5) CMP oxide removal:

Chemical mechanical polishing (CMP) removes the oxide and stops after all oxide above the nitride has been removed as shown in Fig. 1.14 (5).

(6) Nitride and pad oxide strip:

The nitride is removed, leaving the trenches filled with oxide. When the nitride is removed, the STI oxide is also removed a little. The result is that the divot is generated at the STI top corner as shown in Fig. 1.14 (6).

During the STI processing the trench walls should have a small slope, to avoid leaving voids, and the top and bottom corners of the trenches need to be slightly rounded.

After reviewing the STI flow process, we can now look at the possible STI process variations that may affect the TID response [12]:

1) Variations in the STI width and depth:

Within a wafer the STI width is not exactly the same. This factor itself has negligible impact on the TID effects, but it will influence the following STI HDP step. Different STI width will induce different STI trench oxide height, the oxide thickness (height) in the trench is determined

by not only the amount of the HDP oxide but also the STI width. A narrower STI will lead to a thicker STI trench oxide [12]. The STI depth is different in different samples. It also impacts the final trench oxide thickness as a shallower STI leads to a higher STI oxide [12]. In a shallower and narrower STI the effect of stress is stronger which may affect the amount of charge trapping.

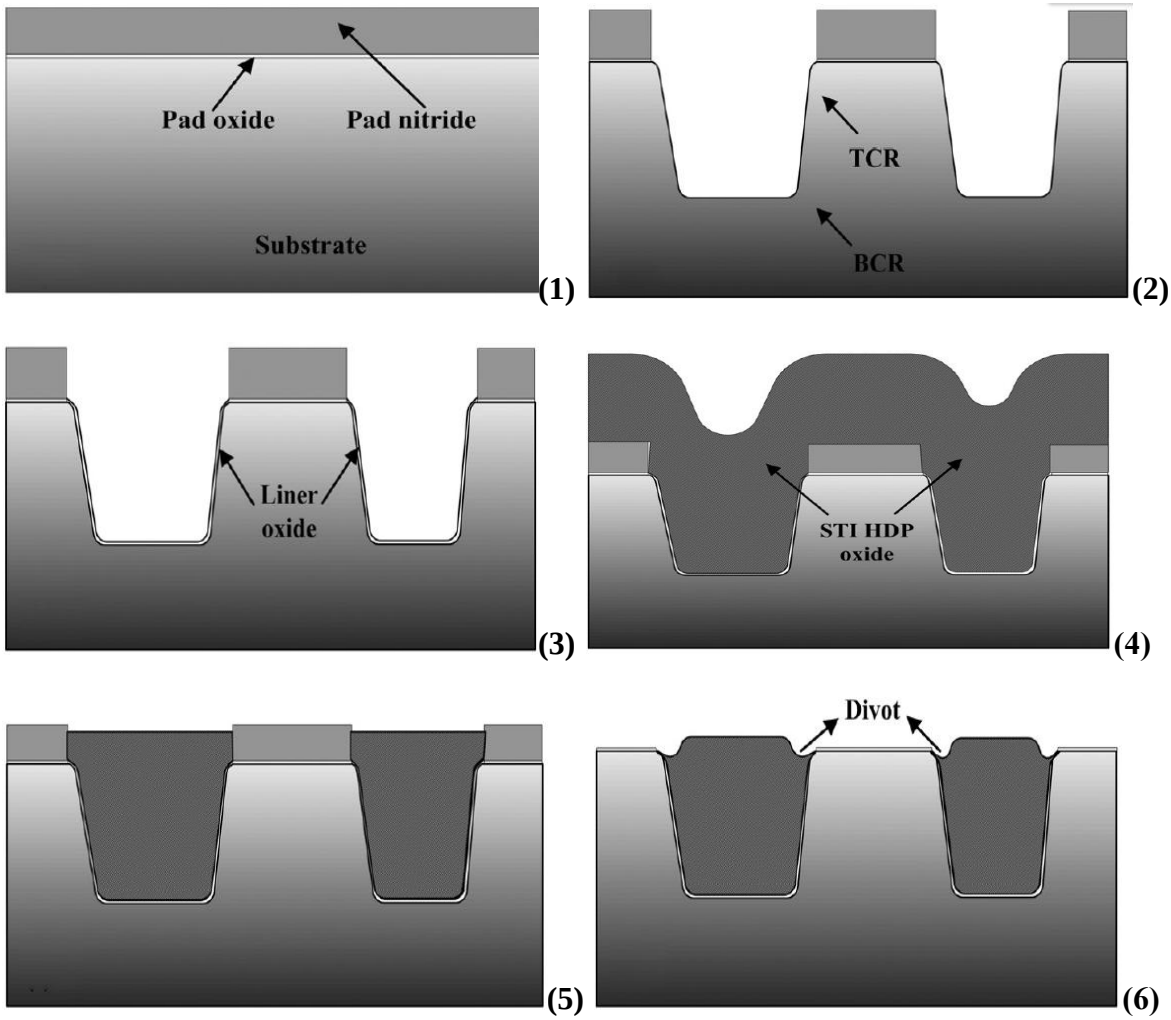


Fig. 1.14. STI process flow [12].

2) Variations in the STI angle:

This factor influences the electric field in the STI oxide during irradiation, and also impacts the

effective channel width of the parasitic transistor [3].

3) Variations in the top corner rounding (TCR) profile:

A more rounded corner can decrease the electric field at the corner, which will affect the electron-hole pair recombination.

4) STI liner oxide thickness variations:

The thickness of the STI liner oxide is not exactly the same on the whole wafer. This oxide formed by dry method at high temperature has a higher quality than the following high density plasma (HDP) oxide. In other words, the liner oxide has less initial trapping centers than the HDP oxide. The total STI oxide is composed of liner oxide and HDP oxide. Assuming a constant STI oxide thickness, a thicker liner oxide will lead to a thinner HDP oxide, hence less charge trapped in the whole STI oxide. As the liner oxide directly contact with the sidewalls, the charge trapped in it plays a very important role.

Finally the CMP polishing rate also may vary in different wafer areas, producing variation in the final STI oxide thickness; thus the TID response varies from sample to sample, and we have seen in [6] that shorter STI CMP (overfilled trench) reduces the radiation induced leakage current. The well implant is also different in different wafer locations, depending on the energy and implanter current in different sites of the wafer. As a result doping profile variations in different samples may occur, which leads to variation in the TID response [8], [13].

f. Dependence of channel stress on layout

Mechanical stress plays an important role in determining the electrical characteristics of advanced technologies. It influences the structural integrity of devices, the yield depends on stress, and the carrier mobility depends on stress [14]. In addition, leakage currents are also a

function of the stress in the system. Shallow trench isolation (STI)-induced mechanical stress increases with reduction of the device active area. Many processing steps individually or collectively contribute to the development of STI stress [15], such as liner oxidation, high density-plasma oxide deposition, and thermal oxidation processes after STI formation. Corner rounding effects in the STI also cause mechanical stress, where the top corner rounding occurs during the trench etch. The different coefficients of thermal expansion of silicon and oxide cause compressive lateral stress from the oxide to the silicon (active area of the transistor) [16]. STI stress results in a strained region in the active area, thus affecting the silicon band-gap, the diffusivity of impurities in silicon, and the mobilities of both electrons and holes [2]. As a result, MOSFET characteristics become more sensitive to the device layout [17]. The threshold voltage, saturation drain current, and off-state leakage current are affected by the layout. Higher integration requires more compact STI structures, and thus induces higher stress. Mechanical stress affects many device characteristics such as carrier mobility and dopant diffusion [18]. The mechanical stress that exists during the fabrication process can enhance or retard dopant diffusion, thereby influencing the final doping of the device [19]. STI stress and size (width and depth) may change the doping profile of the devices, leading to threshold-voltage shifts for gate and isolation oxides, as well as affecting other processes, such as drain-induced barrier lowering and the body effect [20].

The amount of stress in the channel depends strongly on layout, specifically on the gate-to-active area spacing, as shown in Fig. 1.15. A larger active area means that the STI is farther away from the channel, which lowers its effect on the total channel stress. Stress in the channel region decreases monotonically as the distance from the gate to the STI increases. Therefore, the drive current and leakage current of a transistor depend not only on the gate length and width,

but also on the specific layout of the individual transistor. The performance of two transistors with comparable gate lengths and widths can differ significantly, depending on other features of their layouts, including the geometry of the source and drain regions [21].

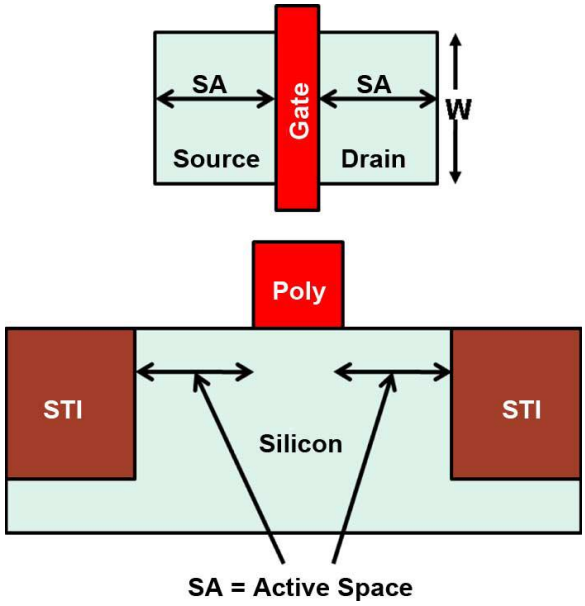


Fig. 1.15. Typical MOS layout top view and cross section showing the SA (active space) distance.

CHAPTER II

DEVICES, EXPERIMENTS AND SIMULATIONS

A. Overview

In this chapter, the different devices and structures used in this work are presented and described. Experiment setup and simulation details are also presented.

B. Experimental details

a. Test structure

In this work TID effects are investigated in both bulk and SOI technologies. The bulk devices are fabricated in 90 nm and 65 nm commercial CMOS processes. The gate oxide thickness is 2.2 nm and the STI depth is 360 nm for both technologies; the nominal supply voltage is 1.2 V and 1 V for the 90 nm and 65 nm technologies, respectively. The test structures used in this study consist of nMOS transistors with different channel widths (0.12 µm, 0.9 µm, 1 µm, and 10 µm), different active space distance (SA = 0.24 µm, 0.48 µm, 0.72 µm, and 2 µm), and three different threshold voltage options (the standard V_t (AVT), high V_t (HVT) , and low V_t (LVT)). SA is the distance from the gate poly to the STI edge (edge of the active region) on each side; varying SA changes the STI stress. Fig. 1.15 represents a typical MOSFET layout view and cross section, showing the SA distance.

For each technology all the devices considered are from the same wafer and are all processed in the same way, and any device-to-device variations are primarily due to natural process variations, such as random dopant fluctuations, STI topology (planarity), and mechanical stress.

For the variability study, measurements on 8 transistors are performed for the 90 nm technology and for the 65 nm technology measurements on 7 transistors are performed.

The SOI devices are fabricated in 45 nm (both partially depleted and fully depleted) and 32 nm partially depleted commercial CMOS technologies. The nominal supply voltage is 0.9 V for both the 45 nm and 32 nm technologies. The 45 nm SOI test structures used in this study consist of nMOS transistors with different channel widths (1007 nm and 152 nm), two different threshold voltage options (AVT, and RVT) and finally core vs. IO devices.

The 32 nm PDSOI devices include both low and high V_t devices for fixed channel width and length. The 32 nm PDSOI ring oscillator consists of a 201 stage and the layout is shown in Fig. 2.1. V_{dd} and V_{ss} are 0.9 V and 0 V, respectively, and DV_{DD} is 1.8 V for the I/O. The signal "Enable", allows the output of the ring oscillator to oscillate when biased at 1.8 V.

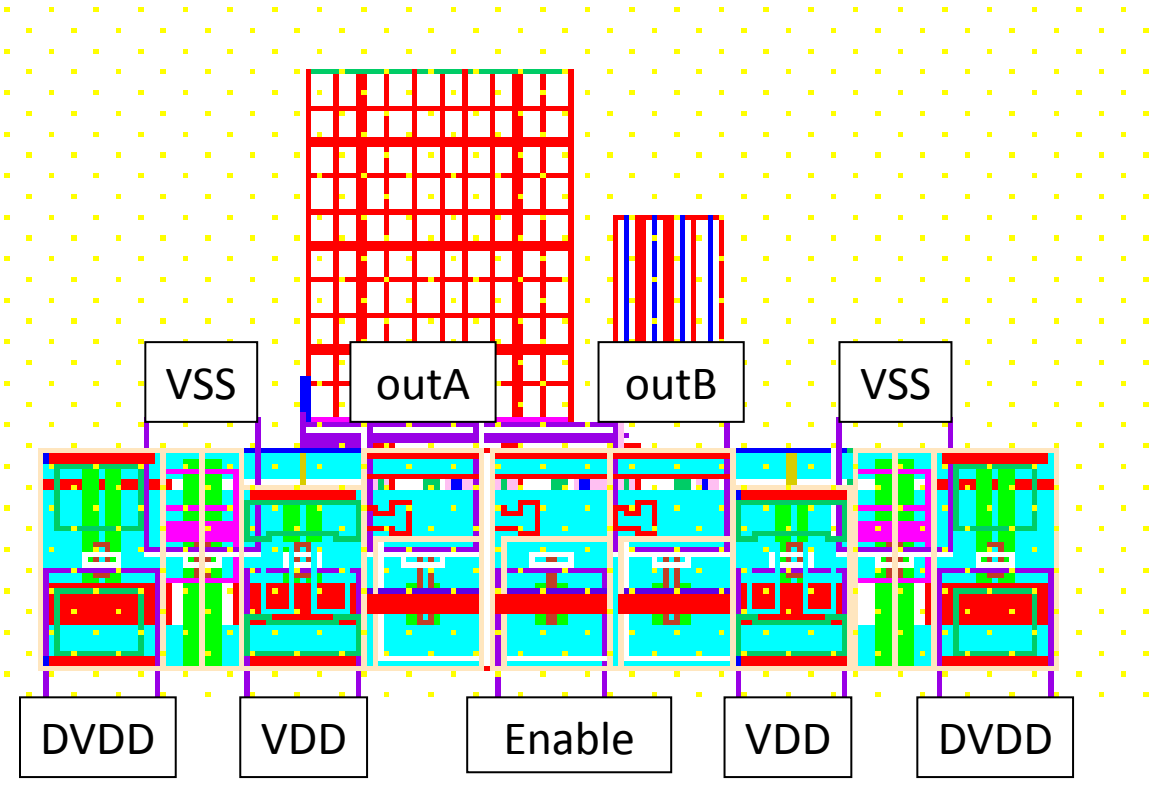


Fig. 2.1. Layout view of the 32 nm PDSOI ring oscillator from the VU test chip.

b.Test setup

Each measurement is performed using the following equipment:

- An ARACOR 10-keV X-ray radiation source,
- A custom-developed probe card with 24 probe tips (2 × 12 arrays, to match the size and pitch of the pads), was used for characterizing both 90 nm and 65 nm bulk technologies. The test structures are arranged into tiles of 2 ×12 pad arrays for probing. Structures are routed to pads that are sized 100 μm × 63 μm. Pad spacing is 5 μm in the *x*-direction and 100 μm in the *y*-direction, as shown in Fig. 2.2.

This combination of a 2 × 12 pad array and its related structure set is called a "**TILE"**. Fig. 2.3 shows an example of the tile arrangement for a SPICE model tile. The probe card is installed inside the X-ray irradiation cabinet, where the X-ray tube and a microscope can be moved manually. This allows the operator to either obtain a view of the chip under test to correctly position the probe tips of the probe card on the pads, or to position the X-ray tube over the chip to perform the irradiation.

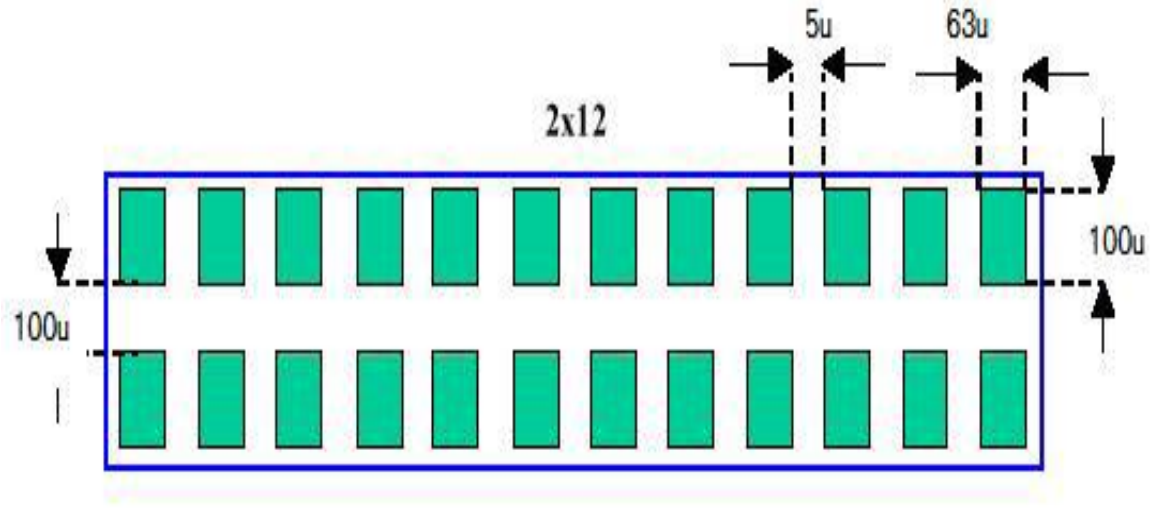


Fig. 2.2. 2 × 12 Pad Arrangement.

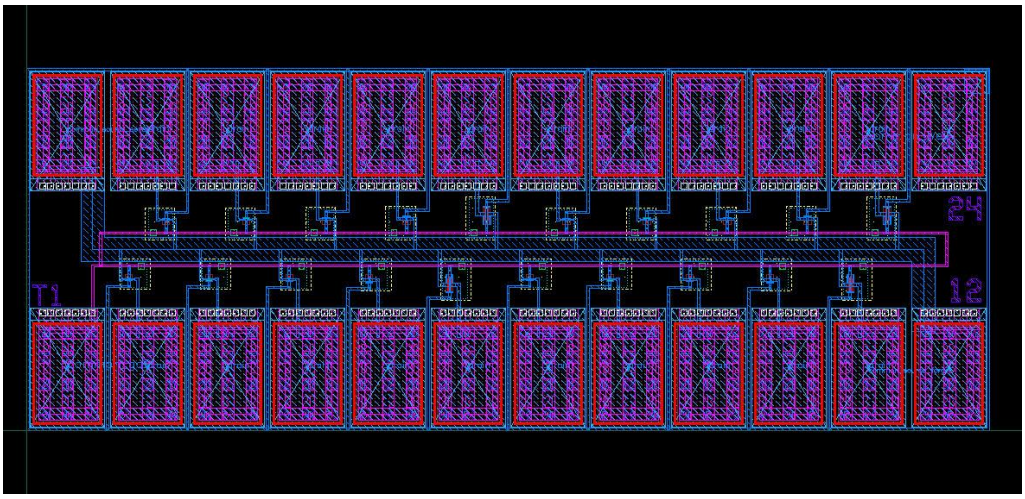


Fig. 2.3. Tile arrangement example.

- A semiconductor parameter analyzer (HP4156A), which is used to perform the static transistor measurements; (typically, I_d is measured as a function of V_{gs} and V_{ds});
- A Keithley 3706 switching matrix, which is used to connect the measuring channels of the HP4156A to the appropriate pads;
- A computer that controls the measurement of up to 20 transistors sequentially and automatically using a Python program.

A picture of the test setup is shown in Fig. 2.4, which shows the ARACOR X-ray irradiator and the parameter analyzer. This test setup enables all the characterization to be performed on an individual chip without the need for any manipulation, reducing the risk of damage to the gate oxide of the transistors due to packaging or other handling. During the measurements, the drain is biased at the nominal supply voltage. Irradiation is performed at room temperature up to a TID of 1 Mrad(SiO_2), at a dose rate of 31.5 krad(SiO_2)/min. The measurements are repeated ~20 minutes after irradiation on multiple parts, and the measurements are stable, indicating that there is no annealing on the time scale of the

experiments.

Recent work [8] has shown that X-ray irradiation may underestimate the radiation level at which inversion first occurs in devices with STI, as compared to Co-60, and therefore may overestimate the hardness level of CMOS STI. This is a result of the enhanced recombination effects in 10-keV X-ray irradiation, relative to Co-60 irradiation [9]. When comparing the two sources, a difference in the total dose at which a particular level of degradation occurs is expected due to differences in electron-hole recombination and dose enhancement [10], which can change the effective dose and charge yield [11]. The results presented here are useful for characterizing the variability in radiation response, although Co-60 irradiation may lead to more degradation at a given dose [8], [9]. The choice of radiation source does not otherwise affect the trends in results shown here.

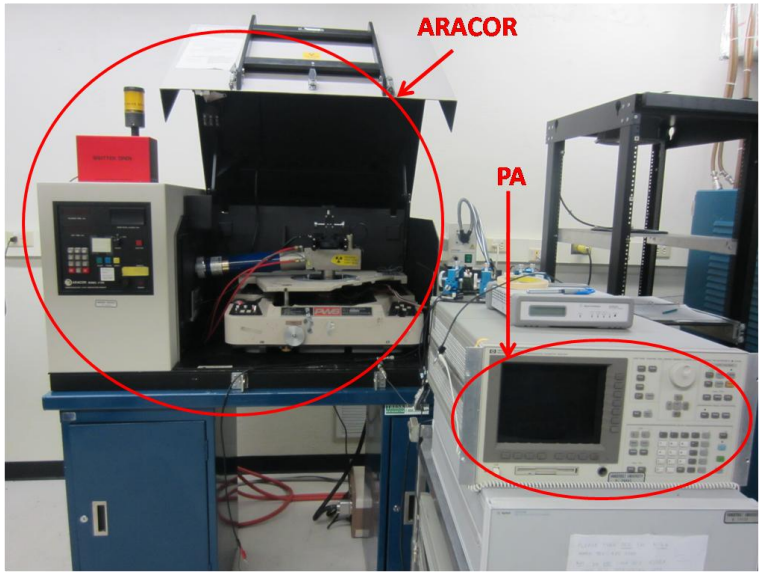


Fig. 2.4. Experimental setup showing the 10-keV X-ray source and semiconductor parametric analyzer used in this work [22].

The devices are irradiated with all terminals of the transistors grounded, except the gates,

which are kept at V_{dd} (again, 1.2 V and 1 V), which is the worst case bias condition for off-state leakage current for bulk technologies [3], [5], since larger potentials applied to the gate lead to an increase of the electric field across the gate oxide and the STI.

For SOI devices all the 45 nm devices from the VU test chip are packaged and the 32 nm SOI devices are characterized using individual probes. For most of the measured SOI devices during irradiation the drain and source are kept at V_{dd} (i.e., 0.9 V) and the rest of the terminals were grounded. The VU 32 nm ring oscillator is also packaged and both the output frequency and power supply leakage current are measured up to a TID of 5 Mrad(SiO_2), at a dose rate of 31.5 krad(SiO_2)/min.

C. Simulation approach

In this work, 3D technology computer aided design (TCAD) simulations were applied to examine the sensitivity of device I-V characteristics to gate work function change and to charge trapped in the sidewall oxides and BOX interfaces with the active silicon regions. The choice of gate-metal work function determines the doping profile required to get the desired threshold voltage and leakage current. Three technology nodes are examined: 90 nm, 45 nm and 32 nm partially depleted SOI.

In order to provide a baseline comparison with simulation studies that were previously conducted on 90 nm bulk CMOS technology (details can be found in [23]), a generic 90 nm partially-depleted NMOS SOI device was constructed in 3D Synopsys Dessis. The simulated device structure used a 150 nm BOX and an 80 nm silicon layer. Fig. 2.5 shows a comparison of the bulk and SOI devices that were simulated. While the specific doping profiles of particular vendor technologies are difficult to ascertain, it is possible to estimate appropriate doping

profiles for an SOI technology by starting with the assumption of uniform body doping. Fig. 2.6 shows I_d-V_g curves for a set of constant body doping values. It is clear that a value on the order of 10^{18}-10^{19} cm^{-3} is required to achieve acceptable characteristics. This value is consistent with the channel doping used in bulk CMOS devices. A non-uniform body profile spanning the noted range, shown in Fig, 2.7, was then used. This is more representative of a typical implanted doping profile (neglecting non-ideal effects such as pileup or dopant depletion at interfaces). The I_d-V_g curves shown in Fig. 2.8 were calibrated to published experimental data [24].

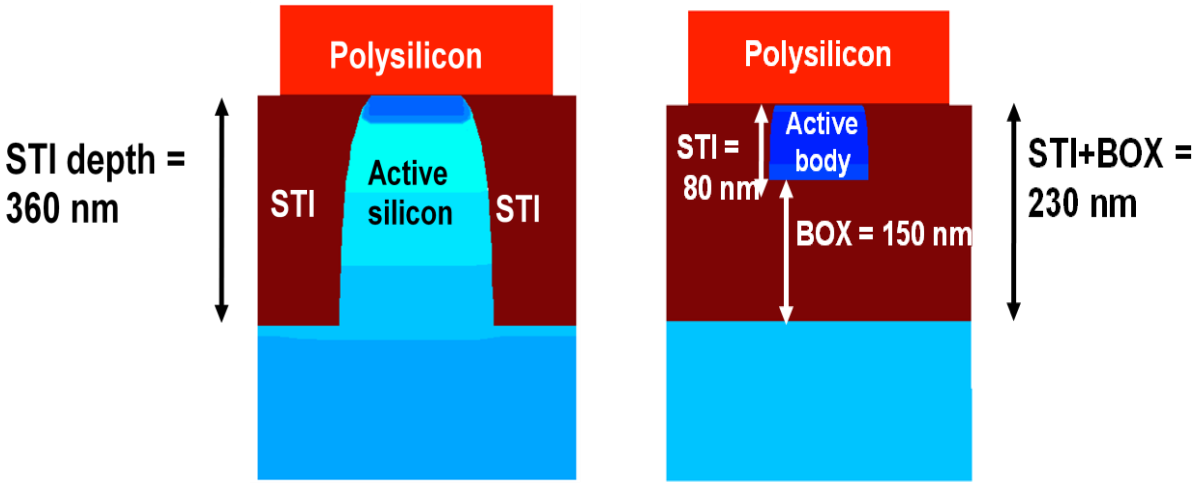


Fig. 2.5. Comparison of Bulk vs. SOI

For the 45 nm partially depleted SOI technology, the structures were constructed in 3D using Synopsys Dessis and were calibrated to the 45 nm PDSOI IBM process design kit (PDK), where a non-uniform doping profile (shown in Fig. 2.9 (a)) was used to match the PDK curve. A standard V_t device was used for calibration; the doping profile magnitude was ~ 1-3 × 10^{18} cm^{-3}, with two peaks corresponding to the threshold adjust implant near the surface and the halo implant located deeper in the body. The gate work function used is 4.2 eV, which is a typical value for NMOS poly [26]. Fig. 2.9 (b) shows very good agreement between the TCAD model and the PDK.

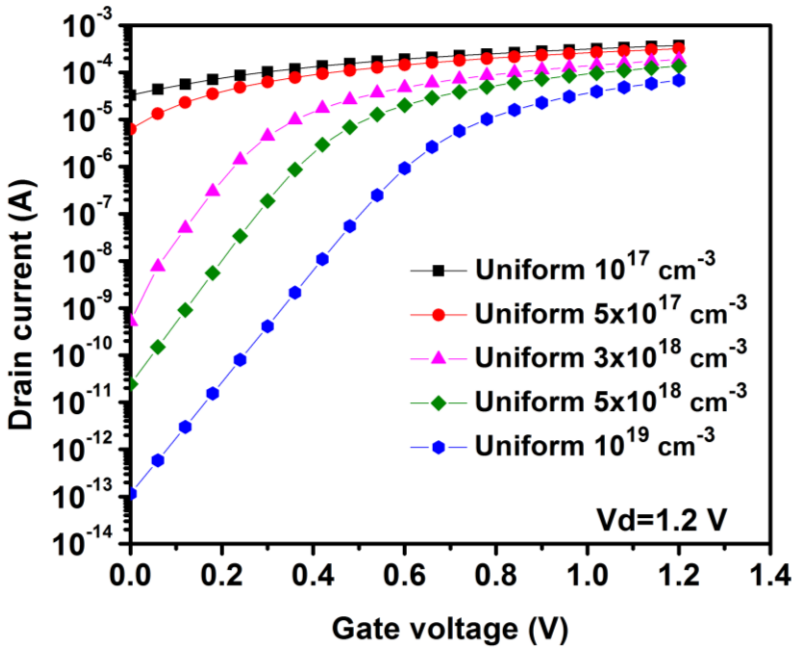


Fig. 2.6. I_d-V_g curves for a set of constant body values [25].

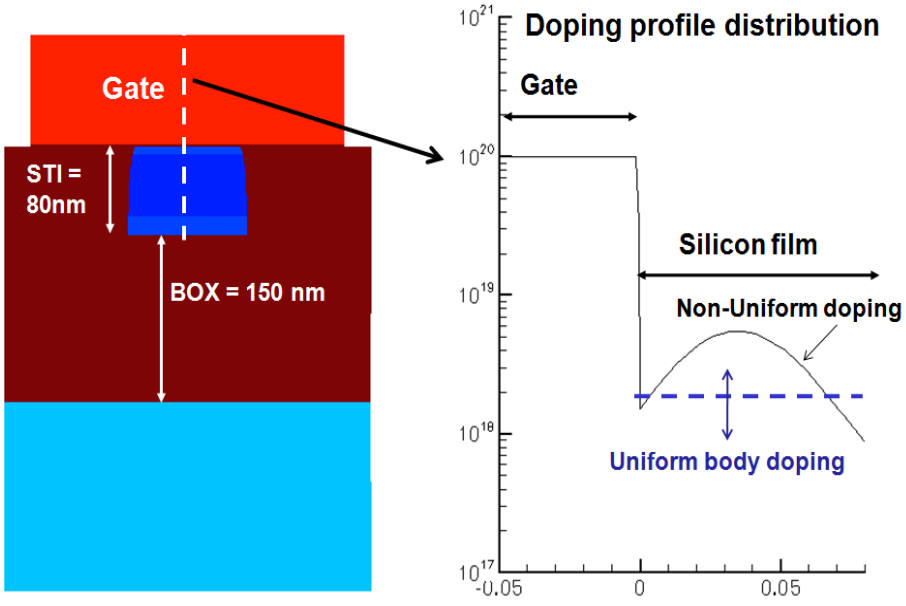


Fig. 2.7. Non uniform body doping profile distribution [25].

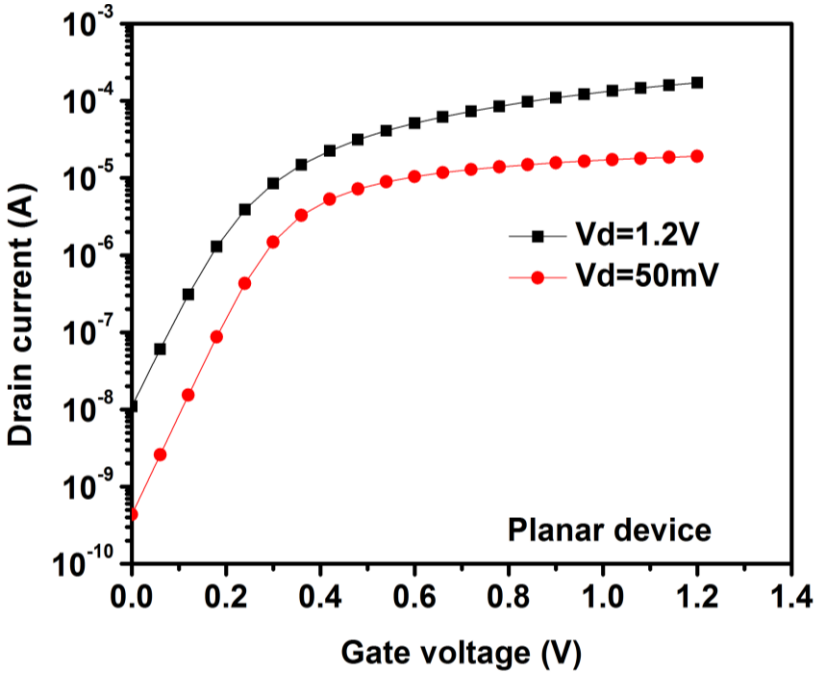


Fig. 2.8. Drain current vs. gate voltage for two drain bias conditions (50 mV and 1.2V) for 90 nm SOI device (using the non-uniform body doping shown in Fig. 2.7 [25].

A similar approach was used to construct and calibrate the 32 nm PDSOI structure to the 32 nm PDSOI IBM PDK. The doping profile shown in Fig. 2.10 (a) was used to match the PDK I-V curves. A standard V_t device was used for calibration; the doping profile magnitude was ~ 1-3 × 10^{18} cm^{-3}, again with two peaks corresponding to the threshold adjusted implant near the surface and the halo implant located deeper in the body. The metal gate has a work function of 4.2 eV. Fig. 2.10 (b) shows very good agreement between the TCAD model and the PDK.

Radiation-induced charge was simulated by varying the positive charge density uniformly at the silicon/STI interface (N_{ot}) along both sidewalls and back interface as shown in Fig. 2.11, for uniform sheet charge concentrations of 5 × 10^{11} cm^{-2}, 10^{12} , 2 × 10^{12} and 1 × 10^{13} cm^{-2}.

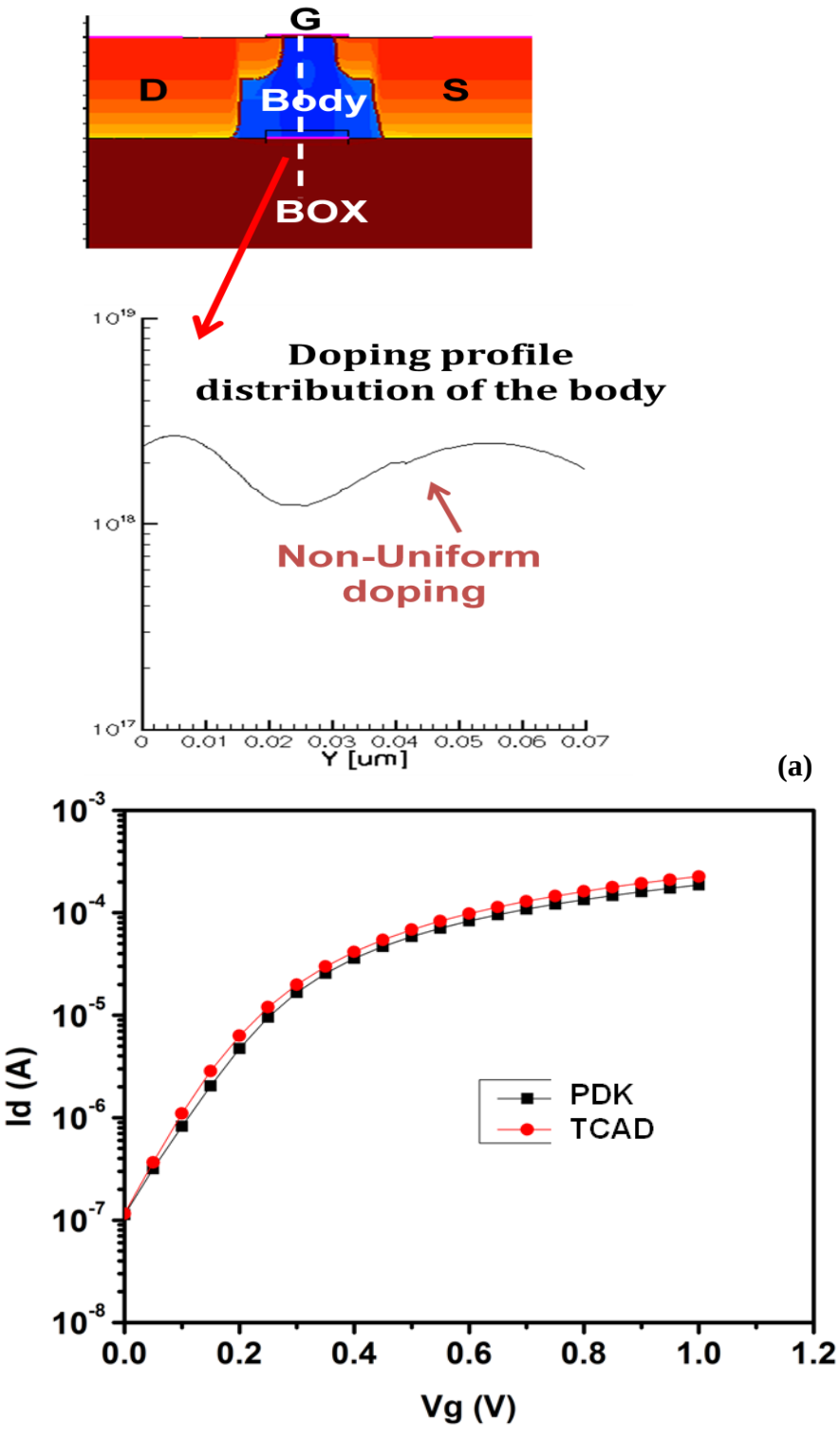


Fig . 2.9 (a) Non uniform body doping profile distribution (45 nm PDSOI). (b) I_d-V_g curve from TCAD modeling matching the PDK curve (using the non-uniform body doping shown in (a)).

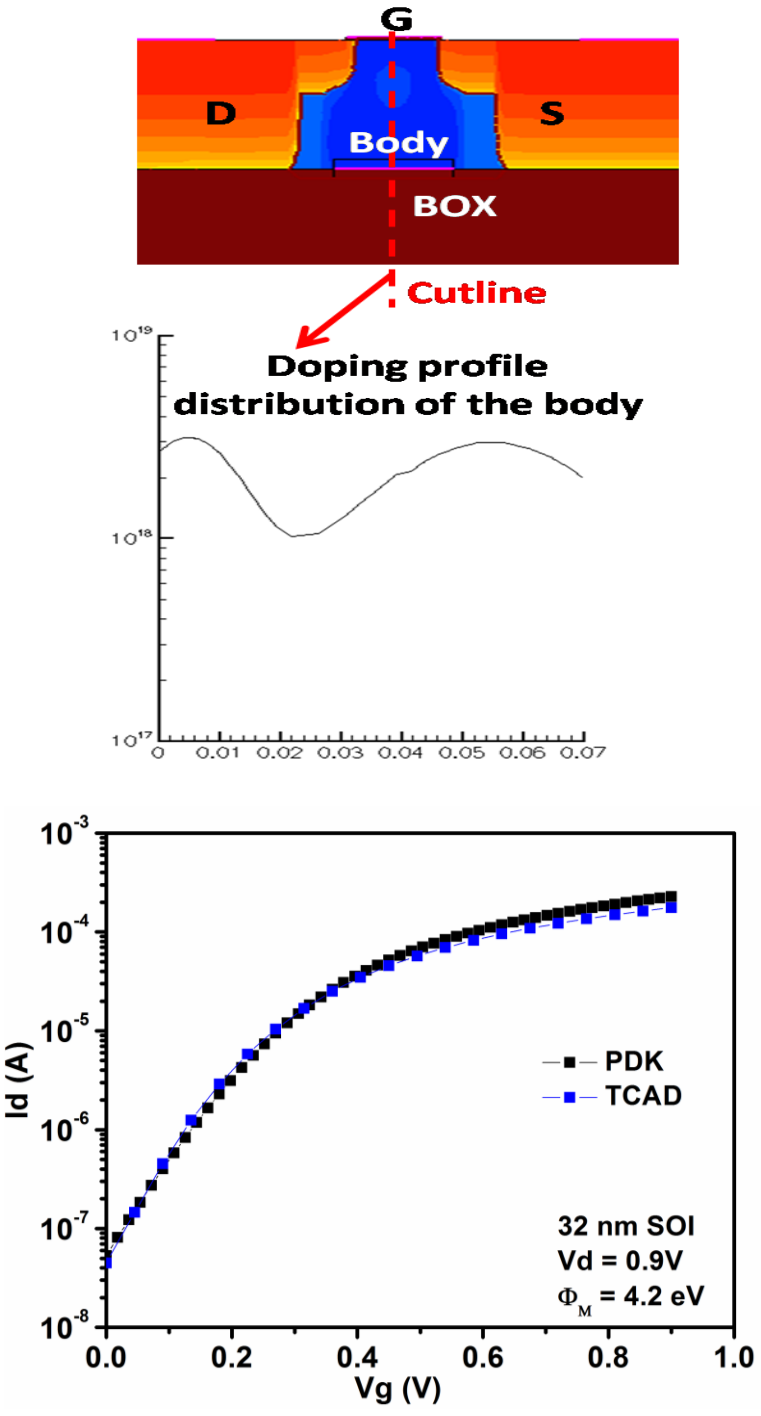


Fig. 2.10 (a). Non-uniform body doping profile distribution (32 nm PDSOI). (b) I_d-V_g curve from TCAD modeling matching the PDK curve (using the non-uniform body doping shown in (a)) [27].

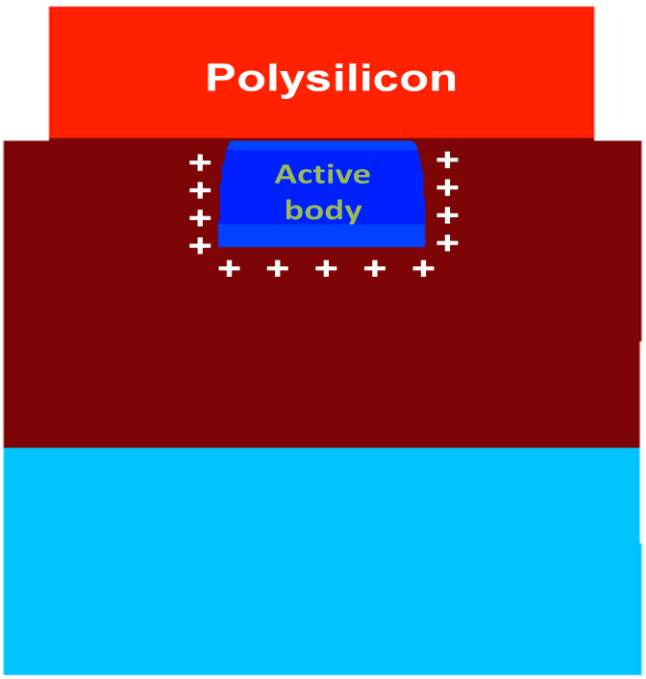


Fig. 2.11. Uniform sheet charge simulated at the silicon/STI interface (N_{ot}) along both sidewalls and back interface.

CHAPTER III

LAYOUT RELATED STRESS EFFECTS ON RADIATION INDUCED LEAKAGE CURRENT

A. Overview

In this chapter, the effects of shallow-trench-isolation-induced mechanical stress on radiation-induced off-state leakage current are reported in 90 nm NMOS bulk devices. The radiation-induced leakage current increases with increasing active device-to-isolation spacing. The leakage current also depends on channel width; narrow devices exhibit less leakage before irradiation, but more after irradiation. These geometrical factors affect the mechanical stress in the device, which impact the dopant diffusion and activation, and the charge trapping in the STI oxide. The combined effects of these layout-related phenomena affect the sensitivity to radiation-induced charge. The physical mechanisms that affect the TID sensitivity are considered, particularly changes in the doping profile of the channel edges and at the STI sidewall. The results are consistent with estimates of mechanical stress inferred from the measured subthreshold current ($I_{d\,(sub)}$).

B. Experimental details

All devices were fabricated in a commercial 90 nm bulk CMOS technology that uses STI. The operating voltage is 1.2 V, the gate oxide thickness is 2.2 nm, and *W/L* is 0.2 μm/0.08 μm. The test structures used in this experiment consist of symmetric nMOS transistors with different active space distance (SA) = 0.24 μm, 0.48 μm, 0.72 μm, and 2 μm. The stress in the active region is compressive due to the lower thermal expansion coefficient of the STI oxide compared to silicon. The effects of channel width on leakage are also investigated; devices with widths of

0.12 μm, 0.9 μm, and 10 μm were measured. During the electrical characterization the drain was biased at 1.2 V. Irradiation was performed at room temperature up to 500 krad(SiO_2), at a dose rate of 31.5 krad(SiO_2)/min, using an ARACOR 10-keV X-ray irradiation source. The devices were irradiated with all terminals of the transistors grounded, except the gates, which were biased at V_{dd} (i.e., 1.2 V); more details about the experiment setup can be found in chapter II.

C. Active space distance effects on TID induced leakage current

Figs. 3.1 and 3.2 show the pre-irradiation threshold voltage (V_{th}) and off-state leakage current (I_{off}) versus SA. Each data point is an average of five measured devices; the error bars in Fig. 3.2 represent the standard deviation. The threshold voltage increases with decreasing SA, and I_{off} decreases with decreasing SA. These results are consistent with previously published data illustrating the effects of layout on pre-irradiation edge leakage [28], [29]. The mechanical stress from the STI edge may affect impurity diffusion in the channel region [17], [28], [30]. It has been suggested that boron and phosphorus diffusion may be retarded by compressive stress [31]. Stress also affects other parameters, such as inversion-layer mobility, the activation of boron dopant atoms, and the resistance, which also affect the electrical characteristics of the device. The effect of stress associated with the trench on the active device is complicated and not always well characterized.

The compressive stress in the STI is created as the device cools down following the trench fill process. The different coefficients of thermal expansion (CTE) of silicon and oxide cause a compressive lateral stress from the oxide in the silicon (active area of the transistor) [16].

As the SA decreases, the STI approaches the channel region of the MOSFET and increases the magnitude of the compressive stress [31].

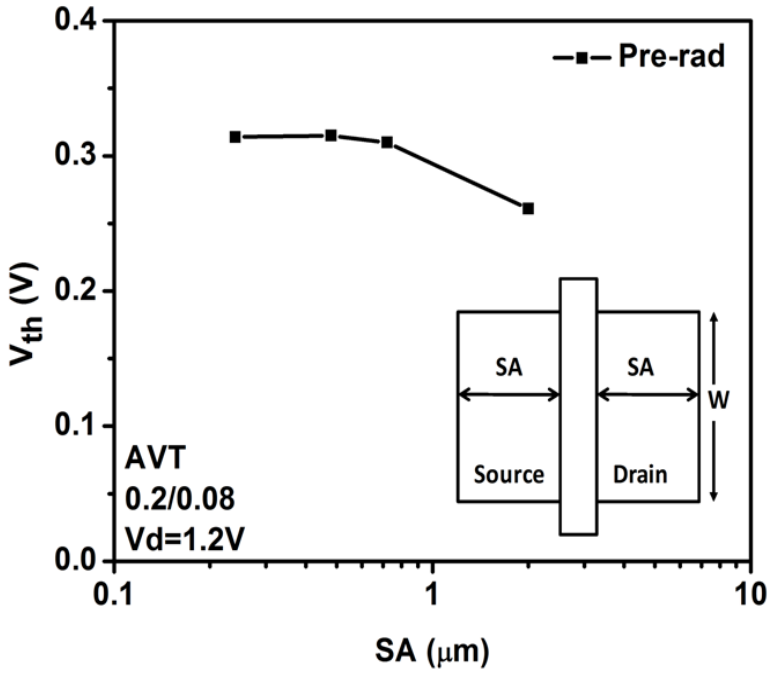


Fig. 3.1. Pre-irradiation threshold voltage versus the active space distance (SA) [32].

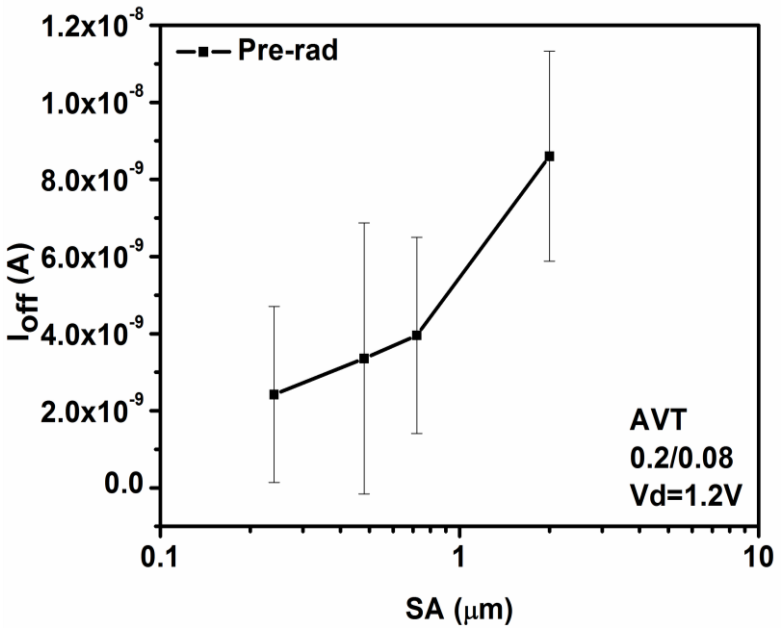


Fig. 3.2. Pre-irradiation drain to source leakage current evolution with active space distance (SA) [32].

The compressive stress originating in the STI edge [17], [30], [31] may reduce the diffusion of the pocket (or halo) implant (boron), increasing the doping concentration at the edge of the channel and increasing the threshold voltage (as shown in Fig. 3.3 (b), obtained along "Cutline X" shown in Fig. 3.3 (a)).

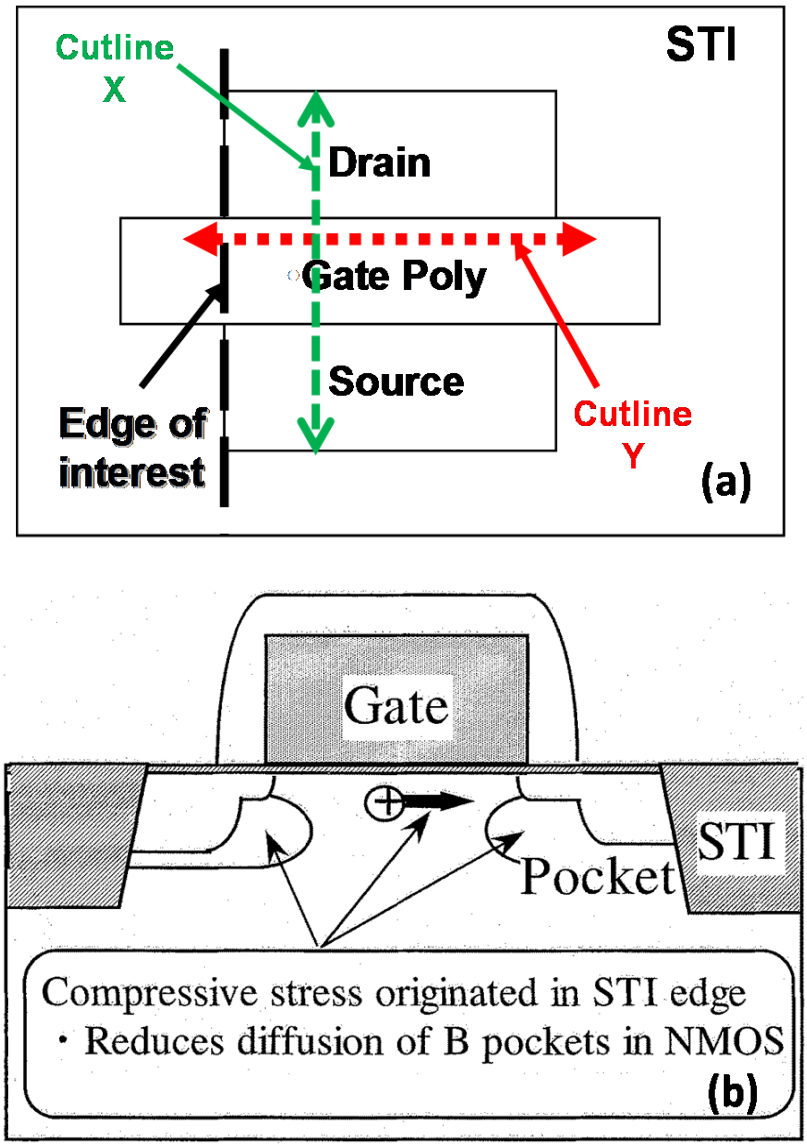


Fig. 3.3. (a) Top view of nMOS device showing two different cutlines, where "Cutline X" gives the 2D view shown on the bottom, and "Cutline Y" gives a 2D view showing the leakage path (edge of interest) along the STI sidewall. (b) Schematic mechanism of increasing V_{th} in nMOS [16].

The doping concentration may also become higher at the STI sidewall (along "Cutline Y"), which explains the decrease of the off-state leakage current with smaller SA, since higher doping at the STI sidewall reduces the off-state leakage current. Fig. 3.4 shows the post-irradiation leakage current variation with SA, showing that TID-induced leakage current increases with increasing SA. The TID-induced current is smaller for smaller SA, since the effective sidewall doping concentration is higher compared to devices with larger SA, probably due to the combined effects of changes in boron activation and impurity diffusion in the channel region and at the STI sidewall.

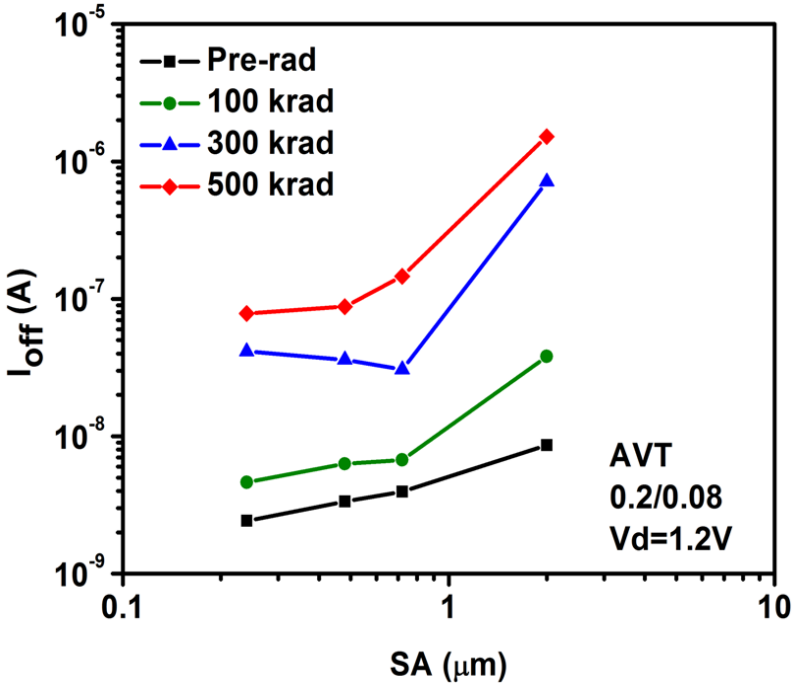


Fig. 3.4. Pre-irradiation and post-irradiation leakage current evolution with active space distance (SA) [32].

D. Channel width effect on TID induced leakage current

Fig. 3.5 shows the dependence of TID-induced current on channel width, with the narrow

devices exhibiting less leakage pre-irradiation, but more leakage post-irradiation. Again each data point represents an average of 5 measured devices. Fig. 3.6 shows the pre- and post-irradiation drain current versus gate voltage for three different channel widths. The on-state current does not change after irradiation; only the off-state current changes. For the wider device (W = 10 μm), no significant shift of the post-irradiation off-state leakage current (solid blue line curve located below the blue symbol curve) is observed.

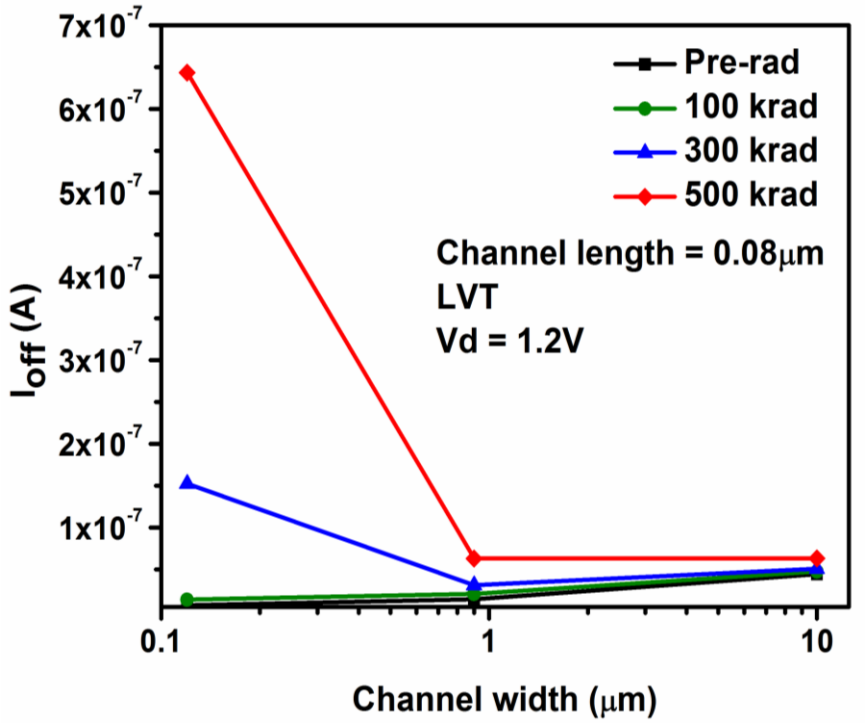


Fig. 3.5. Pre-irradiation and post-irradiation leakage current evolution with channel width [32].

In a symmetric layout, the stresses from adjacent STI edges (STI space) are added to the original STI stress [17]. For narrow devices where the STI spacing is smaller, there is more compressive stress, which may increase the doping concentration at the STI sidewall, reducing the off-state leakage current.

The amount of radiation-induced positive charge trapped in oxides has been shown to depend

on the stress in the oxide for irradiated gate oxides [33], [34]. The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge. However, the thin gate oxides, which trapped less charge when they were irradiated under stress, may behave qualitatively differently from STI oxides, which are of lower quality [2]. STI oxides are generally much thicker (by more than two orders of magnitude), than the gate oxide, and therefore are more sensitive to TID. Moreover, the fringing fields may be higher at the STI edge for narrower width devices [35], depending on the details of the device structure, which can also increase the radiation-induced charge trapping.

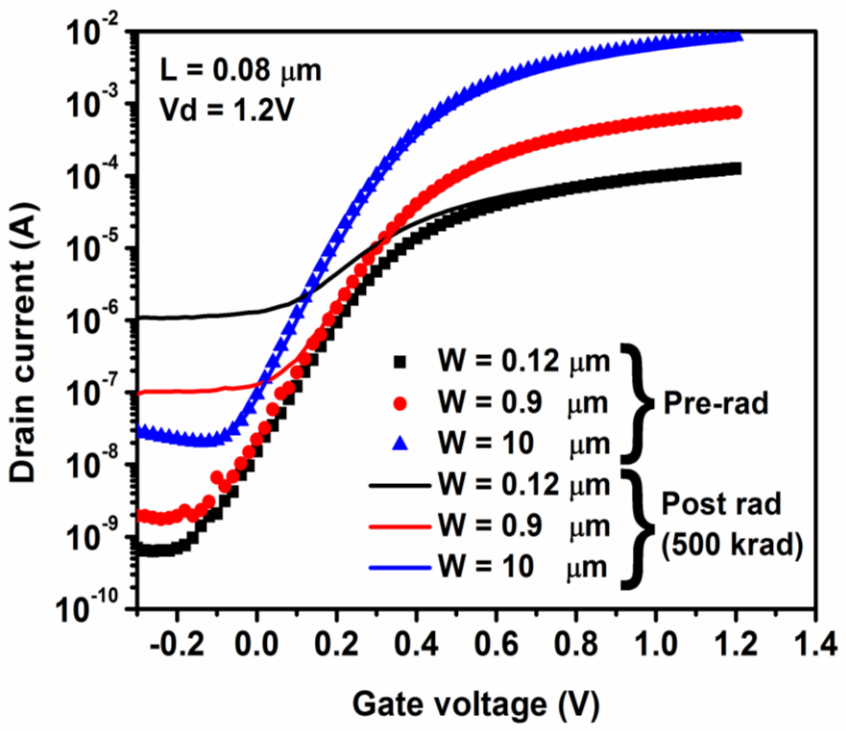


Fig. 3.6. I_d-V_g pre-irradiation and post-irradiation (solid lines) curves for three different widths [32].

E. Estimating stress using measured $I_{D(SUB)}$

The mechanical stress generated in MOSFETs can change the band gap E_g, electron and hole effective masses, diffusion coefficients of dopants, and scattering rates [336]. The mechanical

stress can be estimated using the measured $I_{d(sub)}$, because E_g depends on stress [36].

From deformation potential theory [36], [37], [38], [39], [40], the changes in the silicon conduction band ΔE_C and valence band ΔE_V due to strain can be expressed as functions of stress (σ) [17], as shown in Eqs. (1) and (2).

$$\Delta E_C = \left[\Xi_d (S_{11} + 2S_{12}) + \Xi_u S_{12}\right]\sigma \tag{1}$$

$$\Delta E_V = \left[a(S_{11} + 2S_{12}) + \frac{\sqrt{b^2 (S_{11} - S_{12})^2 + (d/2)^2 S_{44}^2}}{2} \right]\sigma \tag{2}$$

Here S_{11}, S_{12} and S_{14} are the elastic compliance constants given in [21], and Ξ_d , Ξ_u , and a, b, d are the deformation potential constants given in [20].

The change in band gap ΔE_g is the difference between ΔE_C and ΔE_V. Therefore, using Eqs. (1) and (2), ΔE_g varies with stress as:

$$\Delta E_g = \Delta E_c - \Delta E_V = -4.39 \times 10^{-11} \times \sigma \tag{3}$$

Hsieh and Chen [19] estimated the relative amplitude of mechanical stress from the measured $I_{d(sub)}$ of MOSFETs using Eq. (3) and:

$$I_{d(sub)} \propto n_i^2 \propto \exp\left(\frac{-E_g}{kT}\right) \tag{4}$$

where k is Boltzmann's constant and T is the absolute temperature. Since the mobility in the subthreshold region ($V_G < V_{\text{th}}$) is primarily determined by Coulomb scattering rather than phonon scattering, and hence is independent of stress, the subthreshold current is proportional to n_i^2 [19], where n_i is the intrinsic carrier concentration. As a result, the change of the subthreshold current can be transformed into the band gap change ΔE_g. Using Eqs. (3) and (4), the average

stress can be estimated as:

$$\sigma = \frac{\ln\left(\frac{I_{d(sub)}}{I_{d(sub)}(SA = 2\mu m)}\right) \times kT}{4.39 \times 10^{-11}} \quad (5)$$

where the current ratio is based on the measured subthreshold current ratio with respect to a reference device, in this case, the largest devices with SA = 2 μm. Fig. 3.7 shows the calculated mechanical stress versus SA. The estimated stress is large for smaller SA (750 MPa for devices with SA = 0.24 μm) compared to larger SA. The stress at SA = 2 μm is reported as zero, for convenience, since this device, as the largest one available, has the smallest stress and is chosen as the reference. In [17], the authors estimated the dependence of compressive stress on SA at the center of the channel region. Devices with SA = 0.3 μm have compressive stress of 750 MPa, which is about 550 MPa higher than that of devices with SA = 2 μm, which is comparable to the mechanical stress estimated using the measured subthreshold current. The high mechanical stress in devices with smaller SA results in a higher doping concentration at the STI sidewall, as described above. The increased doping concentration reduces the radiation-induced leakage current for devices with smaller SA, as shown in Fig. 3.8, which plots the post-irradiation off-state leakage current versus the mechanical stress for different active space distance.

$$\sigma = \frac{\ln\left(\frac{I_{d(sub)}}{I_{d(sub)}(W = 10\mu m)}\right) \times kT}{4.39 \times 10^{-11}} \quad (6)$$

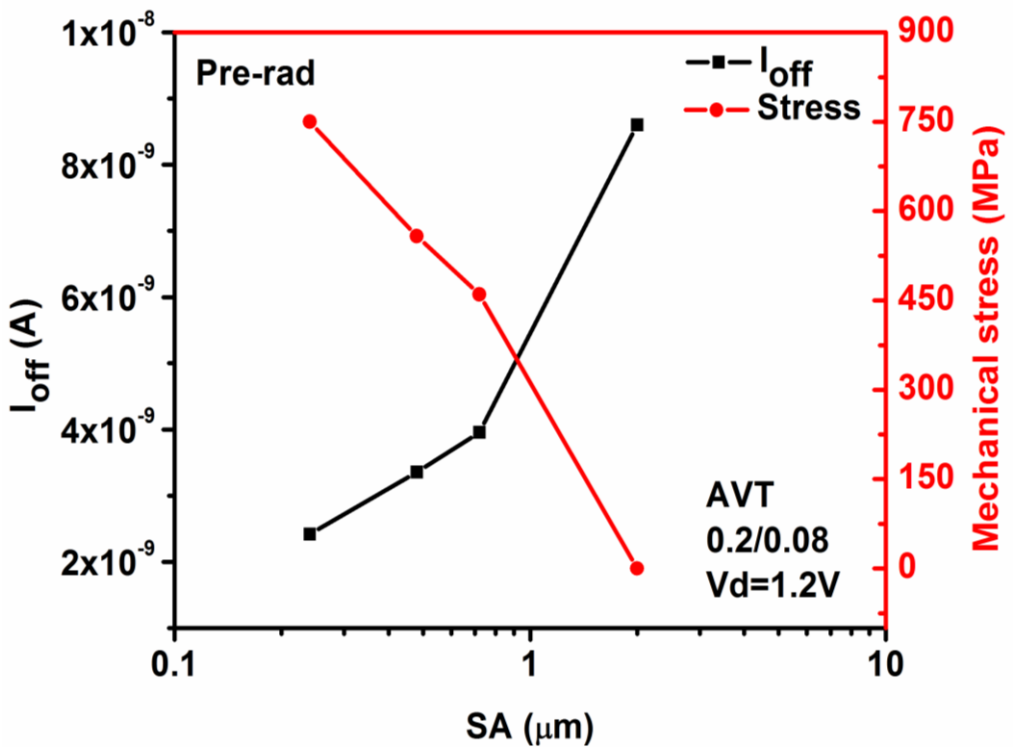


Fig. 3.7. Subthreshold current and estimated mechanical stress versus active space distance SA [32].

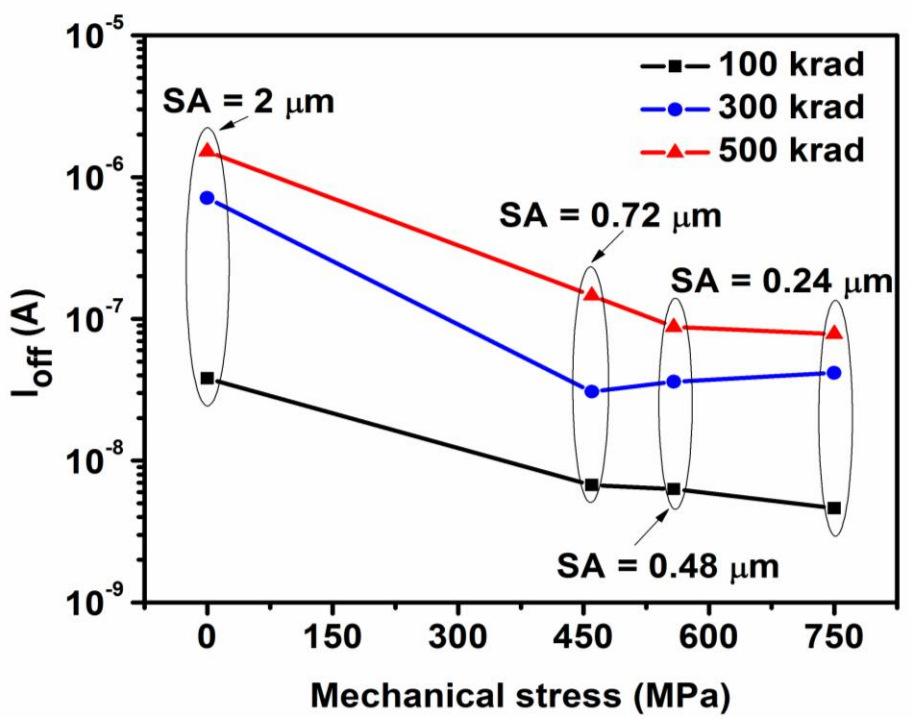


Fig. 3.8. Post-irradiation leakage current versus mechanical stress for different active space distance (SA) [32].

Fig. 3.9 shows the estimated mechanical stress versus channel width, confirming that the stress increases for small channel widths. In this case, the reference current corresponds to a device with W = 10 μm, as shown in Eq. (6). The very large mechanical stress estimated for narrow width devices (~ 1000 MPa) may have a strong influence on the amount of radiation-induced positive trapped charge in the STI oxide, and therefore enhance the radiation sensitivity of narrow width devices, as shown in Fig. 3.10. This figure plots the post-irradiation off-state current versus mechanical stress for different channel widths.

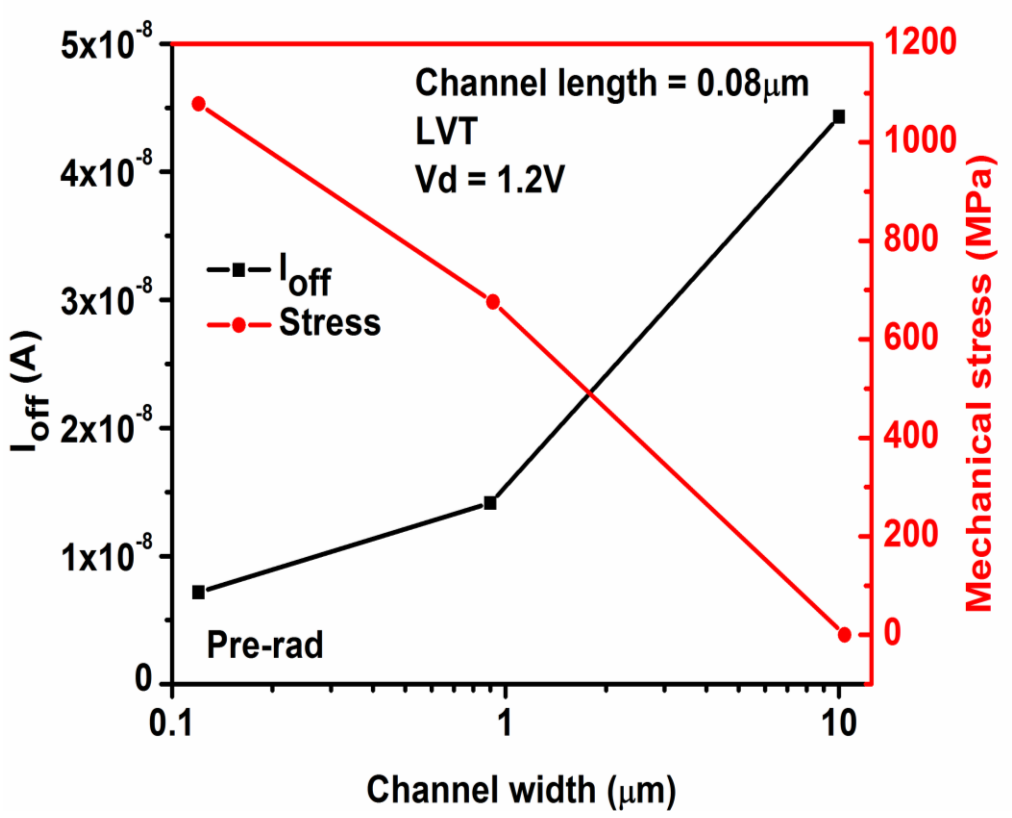


Fig. 3.9. Subthreshold current and estimated mechanical stress versus channel width [32].

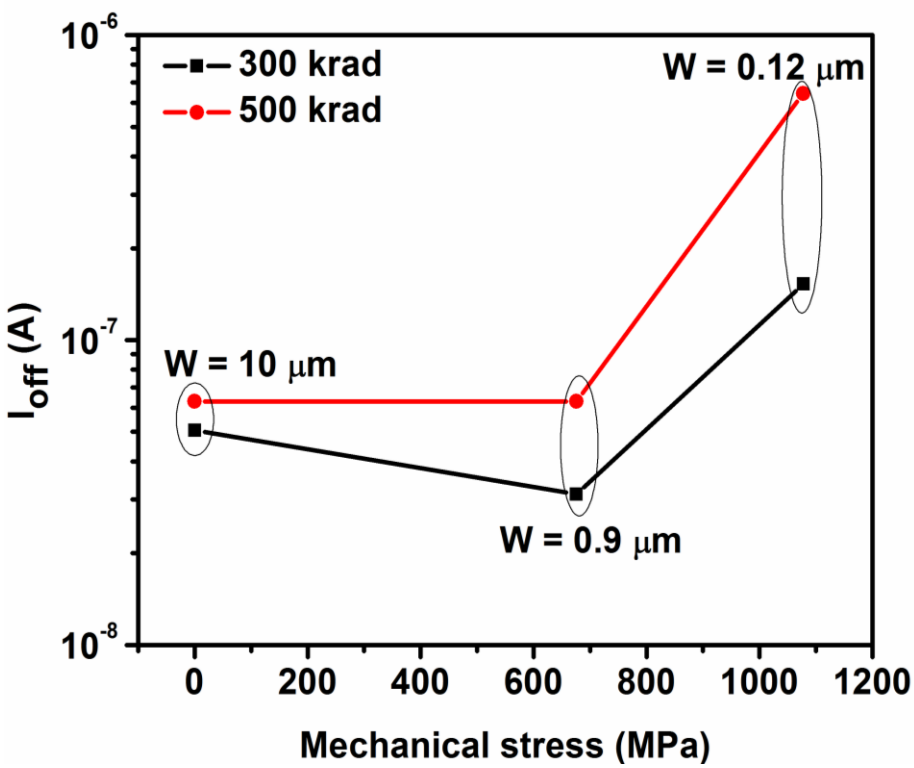


Fig. 3.10. Post-irradiation leakage current versus mechanical stress for different channel widths [32].

F. Conclusions

The TID-induced leakage current of submicron MOSFETs increases with increasing gate-to-isolation spacing. Mechanical stress may affect the TID sensitivity through changes in dopant diffusion, boron activation, or charge trapping in the oxide. There also is a strong dependence of TID-induced current on channel width, with the narrow devices exhibiting less leakage pre-irradiation, but more leakage post-irradiation. The compressive stress dependence on the space between adjacent STI edges and doping-profile differences at the device edges affects the pre-irradiation leakage current. The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge. Finally, mechanical stress was extracted using the measured subthreshold current characteristics.

As technology scales down, stress can strongly affect radiation-induced leakage currents in ways that are difficult to predict in advance of detailed characterization and modeling of the responses of devices across a range of representative geometries. These results are useful when designing devices for radiation environments. For the technology considered here, devices with smaller SA are less sensitive to TID; therefore designers should consider devices with minimum SA distance. Also, wider devices are less sensitive to TID compared to narrow devices.

CHAPTER IV

THE VARIABILITY OF POST-IRRADIATION LEAKAGE CURRENT RESULTING FROM PROCESS VARIATIONS (INCLUDING STRESS) IN 90 AND 65 NM CMOS TECHNOLOGIES

A. Overview

In this chapter, the impact of device width on the variability of radiation-induced leakage currents in 90 nm and 65 nm CMOS bulk technologies is investigated. The off-state leakage current variability increases with decreasing channel width for both technologies, and with increasing total ionizing dose for three different process variants from the 90 nm technology. More variability is observed for narrow width devices compared to wider devices before and after irradiation. Device-to-device variability is compared for two technologies (65 and 90 nm) and three process variants (low, standard, and high threshold voltage). These results illustrate the importance of process-induced variability on the radiation response of MOS devices and integrated circuits.

B. Experimental Details

The devices are fabricated in 90 nm and 65 nm commercial bulk CMOS technologies. The gate oxide thickness is 2.2 nm and the STI depth is 360 nm for both technologies; the nominal supply voltage is 1.2 V and 1 V for the 90 nm and 65 nm technologies, respectively. The test structures used in this study consist of nMOS transistors with different channel widths (0.12 µm, 0.9 µm, 1 µm, and 10 µm), and three different threshold voltage options (AVT, HVT, and LVT). For each technology all the devices considered are from the same wafer and are all

processed in the same way, and any device-to-device variations are primarily due to natural process variations, such as random dopant fluctuations, STI topology (planarity), and mechanical stress. Details about the experiment setup can be found in chapter II.

All the measured data points are included in the following figures, as well as the relative standard deviation (RSD), which represents the ratio of the standard deviation to the mean, where high RSD indicates more variability. For the 90 nm technology, measurements on 8 transistors are performed and for the 65 nm technology measurements on 7 transistors are performed. These sample sizes are relatively small for estimating the quantitative variability of the population, but the overall trends illustrated in the data are clear. The standard error of the mean is SE = $\sigma/\sqrt{N}$, where σ represents the standard deviation and N corresponds to the sample size. For a sample size of 8, $1/\sqrt{N} \approx 0.35$.

C. Effects of scaling on off-state current mechanisms

Fig. 4.1 shows the drain current vs. gate voltage of the two technologies (65 nm and 90 nm) at different TID levels. The off-state current of the 90 nm technology increases with TID, whereas the change in the *I-V* curves of the 65 nm technology is very small for the range of doses examined. The pre-irradiation off-state current (defined at V_g = 0) of both technologies is determined by the threshold voltage and subthreshold slope (not by sidewall or junction leakage current). The post-irradiation off-state current can increase due to one of two effects: (1) an increase in the isolation-related sidewall leakage, manifested as an increase in the off-state plateau at low and negative gate voltage (from −0.3 V to 0 V as shown in the bottom part of Fig. 4.1), or (2) translation of the subthreshold current to the left (since nMOS devices were measured), resulting from charge trapping in the gate oxide. The gate oxide thickness in

technologies of 90 nm and below typically is so thin that charge trapping is negligible and leakage current associated with the STI dominates the TID response.

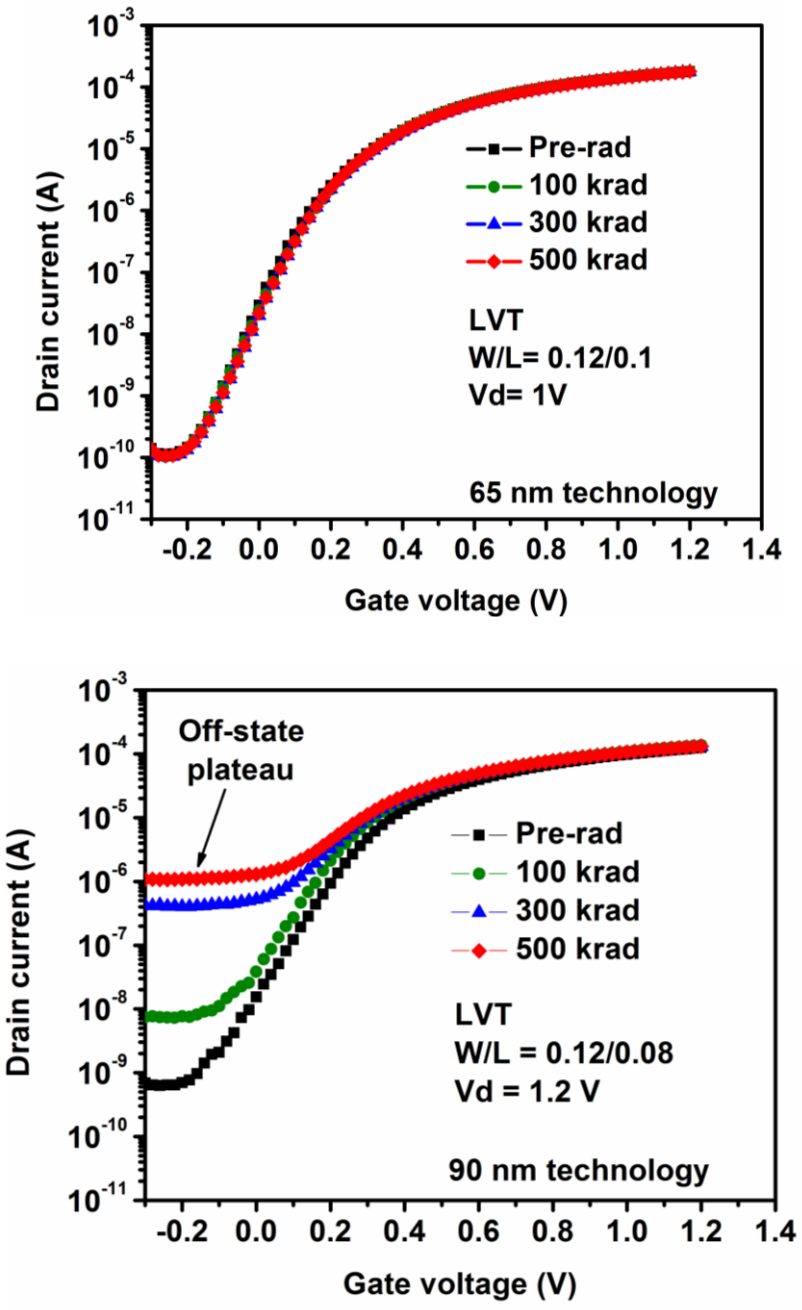


Fig. 4.1. I_d-V_g pre-irradiation and post-irradiation curves for two technologies, illustrating the effects of scaling on off-state current mechanisms [22].

For the 90-nm technology, the off-state current increases with TID because of charge trapping at the STI sidewall and a reduction in V_t. For the 65-nm technology neither of these effects appears to be significant since the off-state current is virtually unchanged with TID, presumably due to the higher body/channel doping compared to the 90 nm devices.

D. Comparison of off-state leakage current variations for different process options and technologies

The device-to-device variability of the off-state current before and after irradiation is investigated; Fig. 4.2 shows the off-state current vs. dose for a HVT device from the 90 nm technology. More variability is observed after irradiation compared to pre-irradiation for doses greater than 300 krad(SiO_2). This can be seen from the range of the data at a given dose, as well as the relative standard deviation (RSD). Variations in quantities such as doping concentration, transistor width, STI topology (planarity), and STI stress resulting from the contributions of process steps such as liner oxidation, high density-plasma oxide deposition, thermal oxidation processes after STI formation, and corner rounding effects in the STI [4], [10], [41]-[43], [2], [9], [13], [17], [32], may contribute to the device-to-device variability as the dose increases.

Small variations in the amount of trench recess may lead to relatively small variations of the pre-irradiation leakage current, while still resulting in considerable variations in the post-irradiation leakage current (orders of magnitude difference), especially if the sidewall doping level is low [13]. Variations in the sidewall doping level may be produced by process variability, including effects related to boron segregation and the effects of mechanical stress on dopant diffusion. Finally, mechanical stress also may affect the amount of charge trapping in the STI.

The variability of the off-state leakage current is compared for the three different threshold-

voltage variants in both technology nodes.

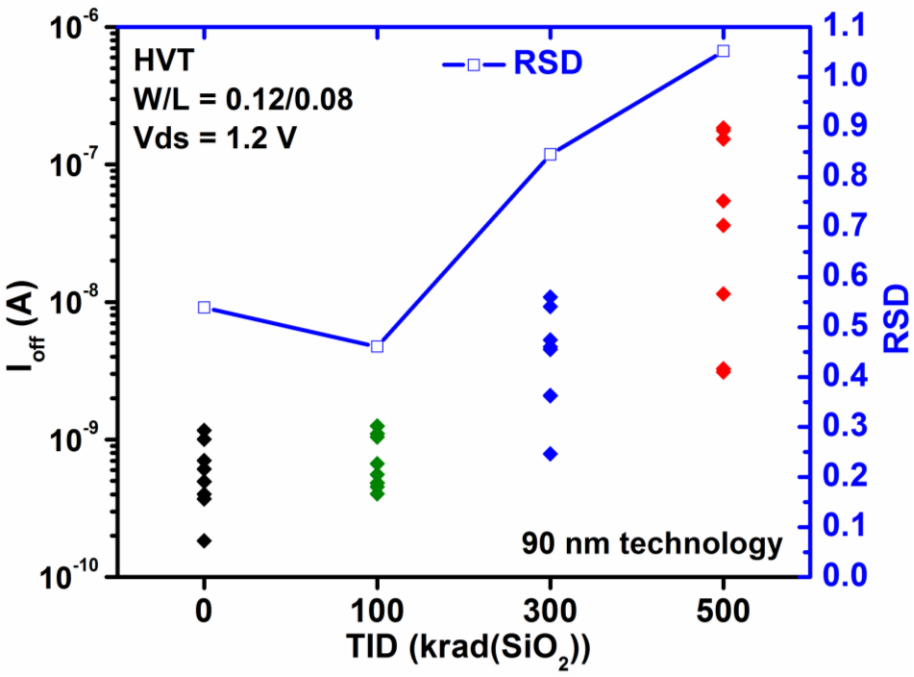


Fig. 4.2. Off-state current evolution with TID [22].

The off-state current for the three variants behaves as expected; for both technologies, LVT (low V_t) devices exhibit higher off-state current compared to AVT and HVT devices (as shown in Fig. 4). For the 90 nm technology, the narrow devices in all three threshold-voltage variants exhibit less off-state current pre-irradiation, but more leakage post-irradiation compared to wider devices, as shown in Figs. 4.3 and 4.4. These results are consistent with previously published results [32], conducted on only one process variant (LVT). In [32],[17] the results are attributed to the mechanical stress from adjacent STI edges, which may affect the doping concentration at the STI sidewall, as well as the amount of charge trapping.

The variability of off-state leakage current in 90 nm devices increases due to irradiation, especially in the narrow devices in all V_t variants (as shown in Fig. 4.4). Notably, the standard

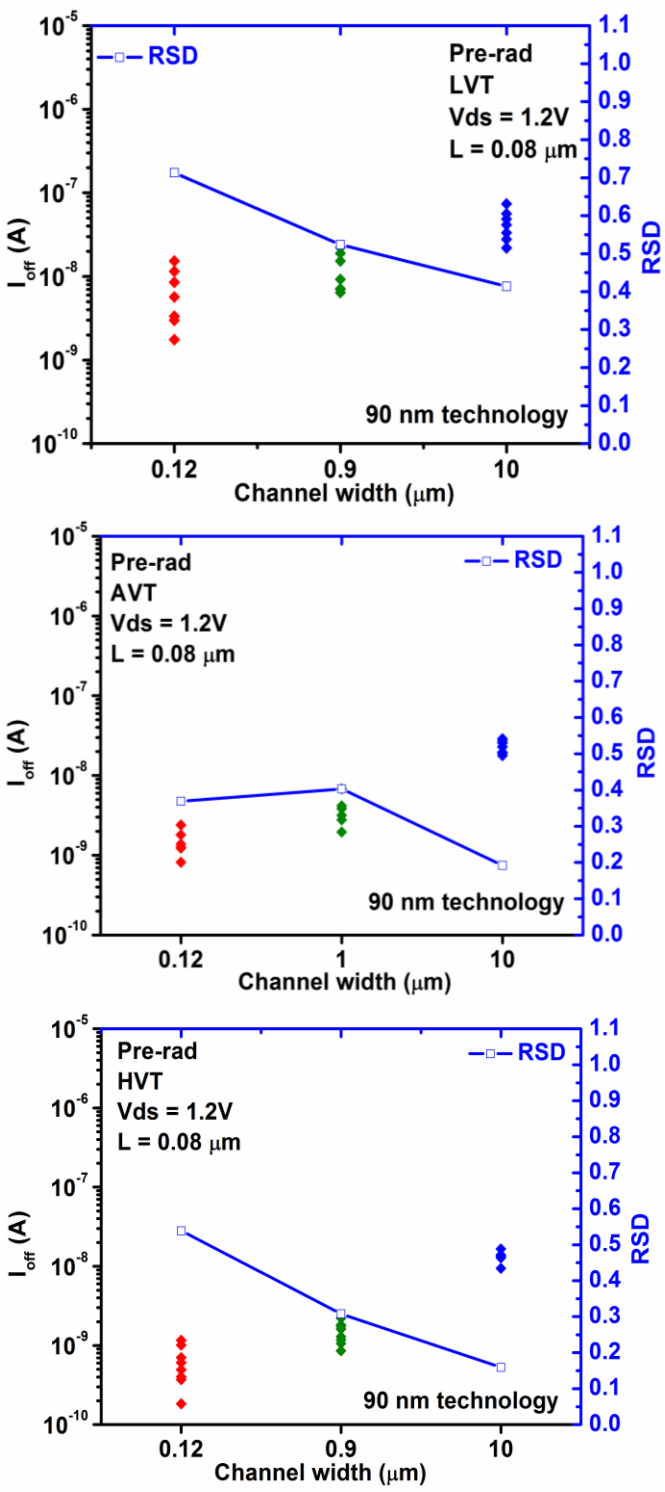


Fig. 4.3. Pre-irradiation off-state current variation with channel width for LVT, AVT, and HVT process variants; devices are from a 90 nm CMOS technology [22].

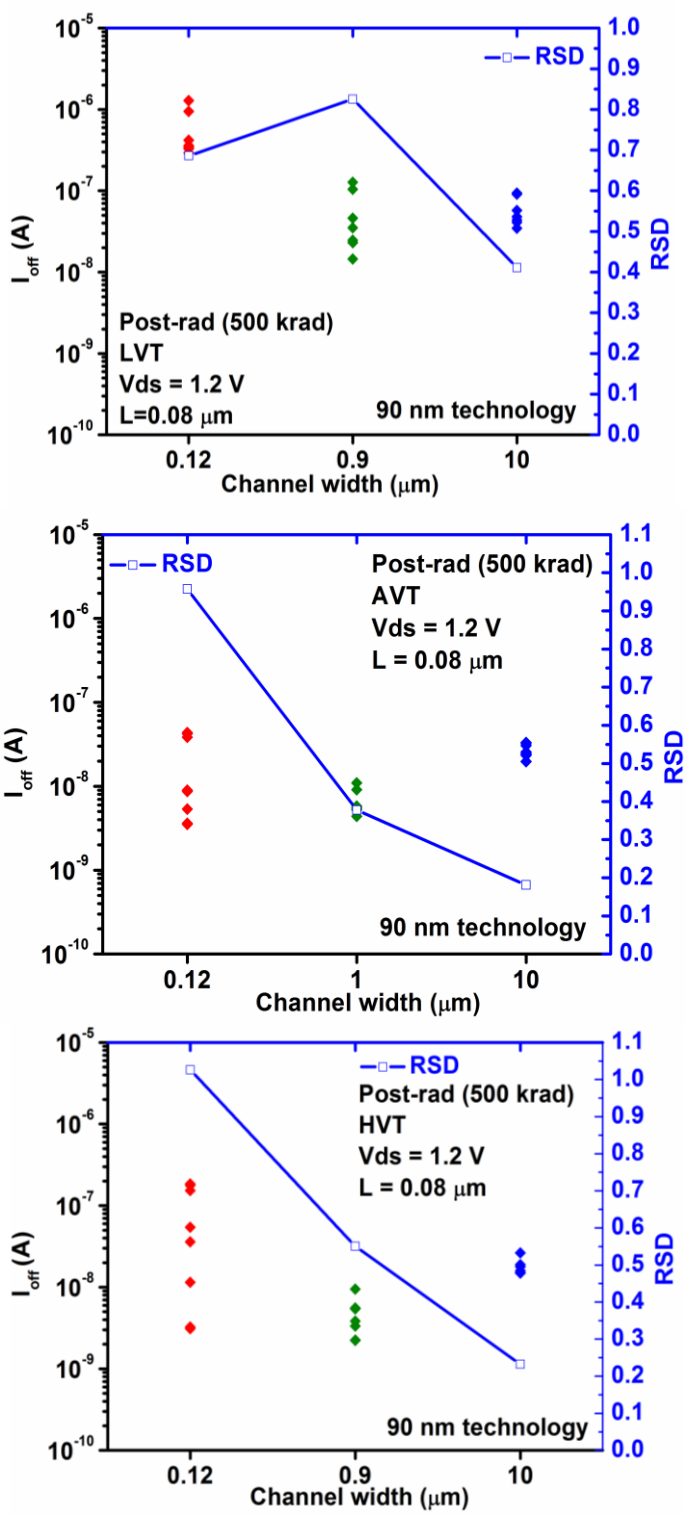


Fig. 4.4. Post-irradiation (500 krad(SiO_2)) off-state current evolution with channel width for LVT, AVT and HVT processes; devices are from a 90 nm CMOS technology [22].

and high threshold voltage devices show greater increases in post-irradiation variability (more than an order of magnitude in measured range).

The increased variability in narrow width devices may occur as a result of the contribution of stress/strain engineering in scaled-down technology nodes [44]. In particular, it has been shown that in a symmetric layout, the stresses from adjacent STI edges (STI space) are added to the original STI stress [32], [17]. For narrow devices where the STI spacing is smaller, there is more compressive stress, which results in variations in both doping concentration and amount of charge trapping [33], [34]. In addition, random dopant fluctuations that result from variations in the implanted impurity concentration can also lead to variability in the as-processed device leakage [45]-[48]. Variability decreases with increasing channel width since the total number of impurities in the channel volume increases; thus, the parameter fluctuations increase in narrow width devices [45].

Random doping fluctuations include the variation in the number of dopants and the shift in the positions of dopant atoms in the channel in extremely small MOSFETs [46], [47], [48]. These fluctuations can lead to variability of threshold voltages, where the standard deviation of V_t ($\sigma(V_t)$) due to dopant fluctuations can be modeled as [49]:

$$\sigma(V_t) = \frac{q}{C_{inv}} \frac{N_{sub} W_{dep}}{3LW} \quad (1)$$

where C_{inv} is the inversion layer capacitance, N_{sub} is the substrate concentration, W_{dep} is the depletion region width, W is the channel width and L is the channel length. The approximate number of dopant atoms in the channel region for a transistor with $W = 0.12$ μm and $L = 0.08$ μm is ~5000 and $\sigma(V_t) = 0.025$ V, whereas for a device with $W = 10$ μm the number of dopant atoms is ~4×10^5 and $\sigma(V_t) = 0.019$ V. While fluctuations in the number of dopant atoms for the narrow device lead to more variation in V_t than they do in the wide device, it is clear from these

calculations that random dopant fluctuations are not as significant as stress in causing device to device variations in the devices investigated in this work. Finally in [32] mechanical stress versus channel width has been estimated, confirming that the stress increases for small channel widths. The very large mechanical stress estimated for narrow width devices (~1000 Mpa) may have a strong influence on the amount of radiation-induced positive trapped charge in the STI oxide, and therefore enhance the radiation sensitivity of narrow width devices, as well as the observed variability of off-state leakage current.

For the 65 nm technology, there is negligible TID-induced increase in off-state current (as shown in Fig. 4.5(b)), due to the high body/channel doping compared to the 90 nm technology. According to the ITRS roadmap, the body doping levels are approximately 1.5×10^{18} cm^{-3} for the 90 nm technology, and approximately 5.0×10^{18} cm^{-3} for the 65 nm technology [50]. However, the pre-irradiation current still depends on the channel width (as shown in Fig. 4.5(a)), with the narrower devices showing less pre-irradiation off-state leakage current than the wider devices, especially for the devices with the three larger channel widths. This occurs because the devices are narrower, since the off-state current normalized to the width is higher in the narrower devices as shown in Fig 4.5(b), and because both the sidewall current and the doping variations resulting from mechanical stress [32] have a proportionally greater contribution in the narrow devices. Fig. 4.5(c) shows the drain current divided by the channel width as a function of gate voltage. For the two wider device types, the normalized off-state leakage current is the same, indicating that edge effects in these wider devices are negligible. For the 0.12 μm devices, however, the normalized off-state current is greater.

Fig. 4.6 shows the pre and post-irradiation (500 krad(SiO_2)) off-state current evolution with channel width for 65 nm technologies (LVT devices). The 65 nm technology shows higher

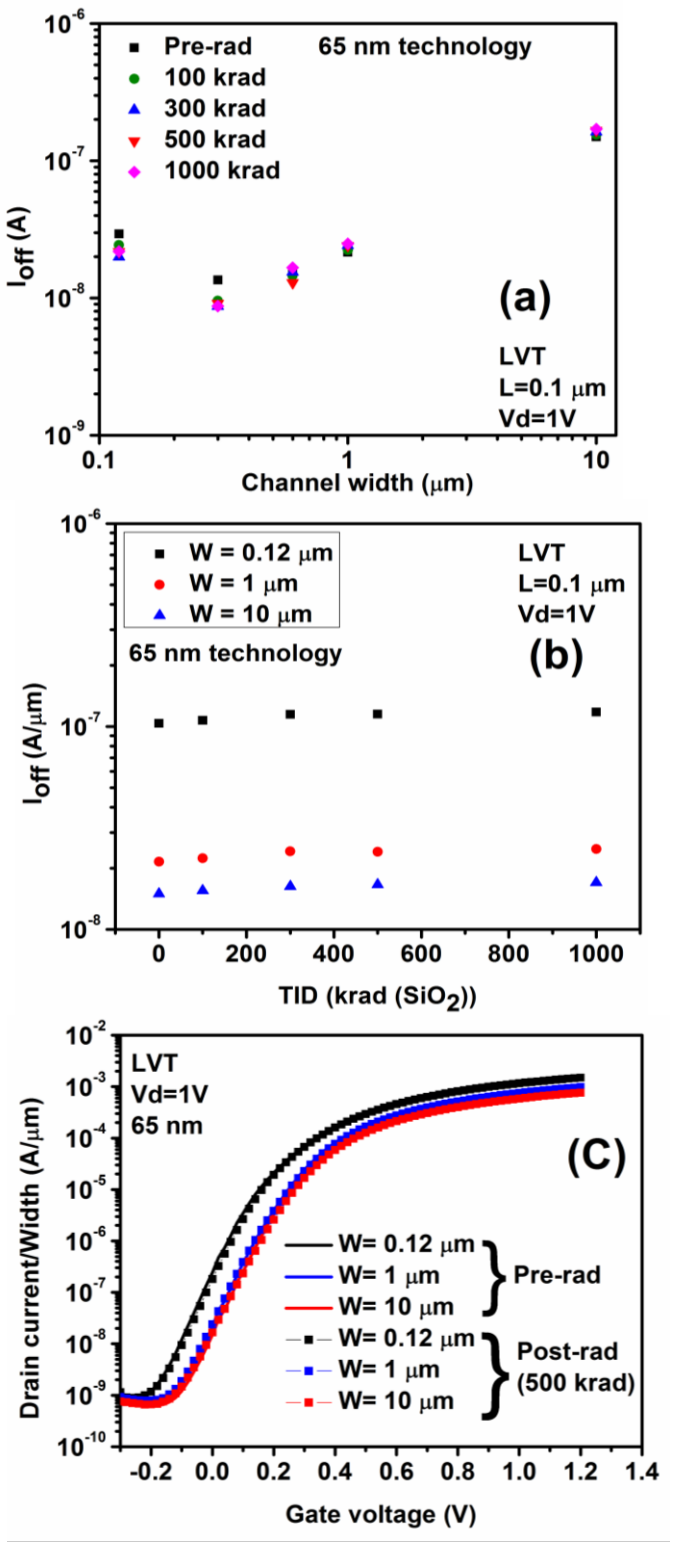


Fig. 4.5. (a) Off-state current vs. channel width; (b) normalized off-state current to channel width vs. TID; (c) normalized drain current to channel width versus gate voltage; devices are from a 65 nm CMOS technology [22].

pre-irradiation off-state leakage current, and less variability (RSD) both pre- and post-irradiation compared to the 90 nm technology (shown in top part of Figs. 4.3 and 4.4) for all channel widths. The variability and the sensitivity to TID are reduced for the 65 nm technology and are independent of the channel width, whereas narrow width devices from the 90 nm technology exhibit more variability compared to wider devices.

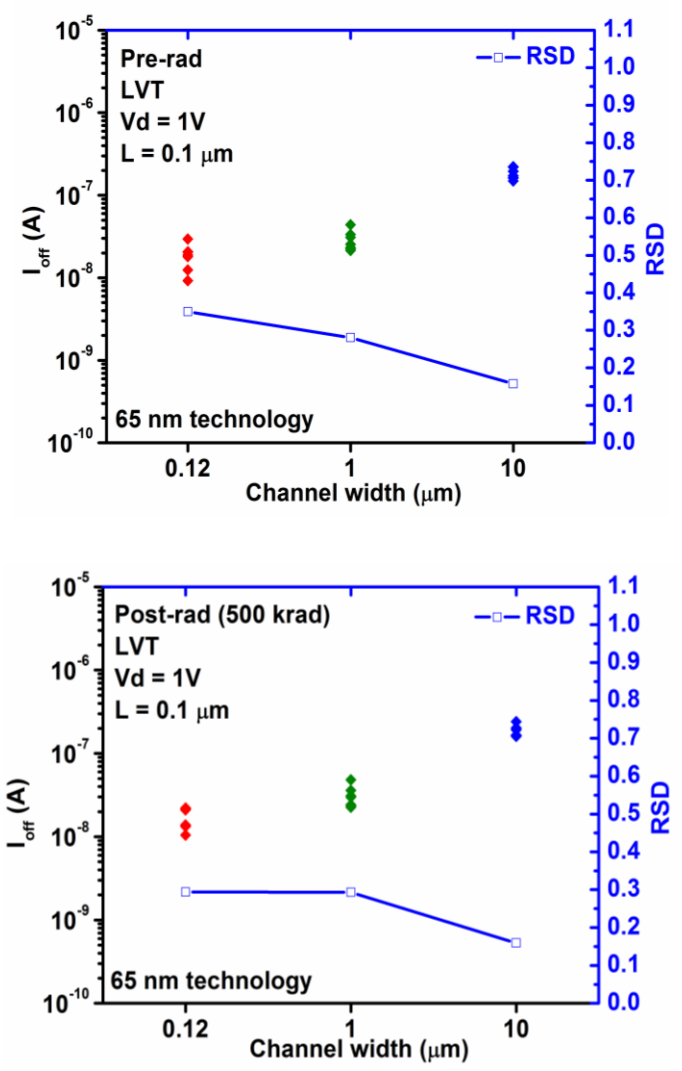


Fig. 4.6. Pre and post-irradiation (500 krad(SiO_2)) off-state current evolution with channel width for 65 nm technologies (LVT devices) [22].

E. Comparison of off-state leakage current for the same technology and different vendors

Fig. 4.7 shows the subthreshold *I-V* characteristics for two devices with similar *W/L* ratios, from the same technology node (65-nm) and two different vendors (A and B) that likely have used different processes, (*W/L* = 1/0.24 for vendor A and *W/L* = 1/0.2 for vendor B). Although the leakage current is not significant for the second process, there are likely to be significant differences between processes at the same technology node, as reported previously [10]. The differences are likely to be due to differences in the doping profile along the sidewall, the trapping quality of the STI oxide, the STI planarity, and/or the amount of stress. Therefore, both the radiation hardness and the variability of a given technology are usually process dependent, and general conclusions about the radiation hardness of a particular technology node cannot be drawn from the results of a single study on one particular process type.

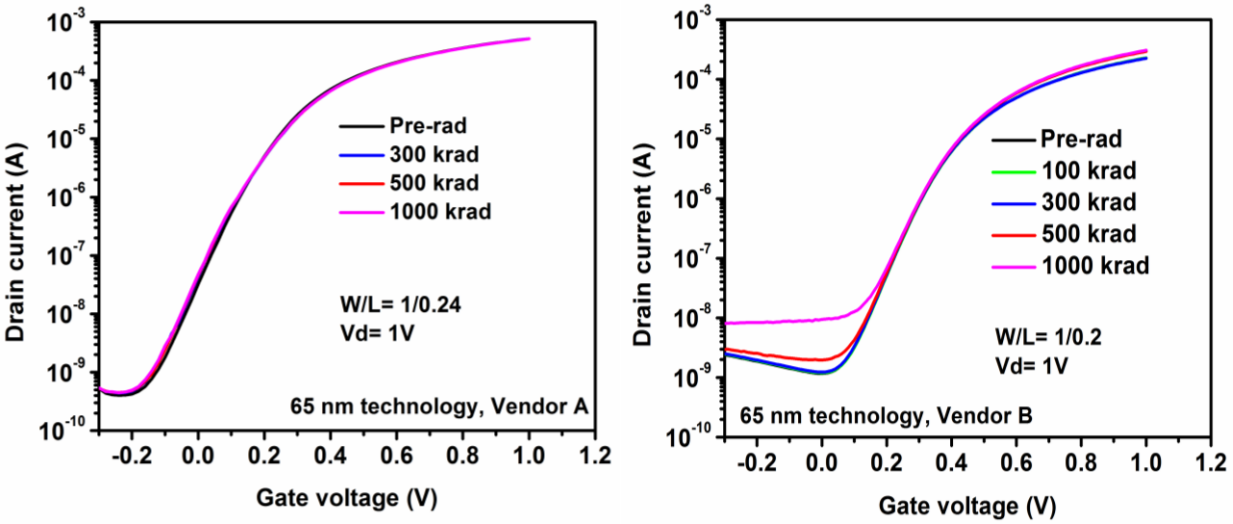


Fig. 4.7. Comparison of off-state leakage current for two vendors (same technology node (65 nm)) [22].

F. Conclusions

Quantifying the variability in parameters, in this case the pre- and post-irradiation off-

state current, and the dependence on design parameters (device size, layout, etc.) is essential to determine the significance of variability in the circuit design and lot-acceptance processes. TID variability has been found to be most pronounced in narrow devices. In the devices investigated, the effects of stress are more significant than are random dopant fluctuations. Random dopant fluctuations may contribute more significantly to variations of the threshold voltage in smaller geometries. For parasitic leakage current due to charge trapping in STI oxides, a small variation in threshold voltage that results from stress-induced changes in radiation response or random doping fluctuation can lead to a large increase in off-state leakage current.

Doping generally increases as devices become smaller for planar CMOS devices. This increase in doping decreases the sensitivity of the devices to these sources of variability in TID response of the STI. In addition, the higher sidewall doping expected in the 65 nm technology leads to less threshold voltage shift during irradiation than observed in the 90 nm technology. Thus, technology scaling trends for TID appear to be favorable going forward, at least until device dimensions become so small that random doping fluctuations begin to dominate the variability in response.

CHAPTER V

TOTAL-IONIZING-DOSE RADIATION RESPONSE OF SUB-100 NM PARTIALLY AND FULLY DEPLETED SOI DEVICES

A. Introduction

Silicon-on-insulator (SOI) devices are known to provide inherent advantages for single event and transient radiation effects. However, the buried oxide (BOX) provides an additional region for charge trapping due to total ionizing dose (TID) radiation compared to bulk devices. In scaled CMOS technologies, the gate insulators have become so thin that threshold voltage shifts due to TID have become negligible. In bulk CMOS technologies, sidewall leakage due to charge trapping in the STI is the dominant TID effect. Sidewall doping profiles and gate topology (and variation in these parameters) determine the sensitivity to TID effects in bulk technologies. In SOI, fully-depleted devices employ light body doping and charge trapped in sidewall oxides and the BOX may lead to increased leakage and front gate threshold-voltage shifts. In partially depleted devices, however, the channel doping levels tend to be comparable to those in bulk devices ($> 10^{18}$ cm^{-3} [51]) in order to provide reasonable threshold voltages and I_{on}/I_{off} values. In partially-depleted SOI having somewhat thicker silicon layers, it is possible that junction engineering and channel implants may not dope the back channel, and charge trapped in the BOX could induce a parasitic leakage path in the absence of any specific back channel doping. As CMOS has scaled to sub-100 nm dimensions, the silicon has also scaled to sub-100 nm thickness in SOI technologies, and the body doping has increased (similar to channel doping in bulk devices). In this work, 3D technology computer aided design (TCAD) simulations were used to examine the sensitivity of device I-V characteristics to charge trapped in the sidewall

oxides and BOX interfaces with the active silicon regions. Results indicate that the high body doping tends to mitigate the sensitivity to TID in SOI, providing the body doping reaches the BOX and sidewalls, which is probable given the sub-100 nm thickness of the silicon. Experimental TID measurements of partially-depleted 45 nm floating body NMOS SOI devices show no notable changes at doses up to 1 Mrad, supporting the simulation results.

B. TID response of PD and FD SOI devices

a. Pre-irradiation results: Trench recess variation (90 nm PDSOI)

In order to provide a baseline comparison with simulation studies that were previously conducted on 90 nm bulk CMOS technology, a generic 90 nm partially-depleted NMOS SOI device was constructed in 3D Synopsys Dessis (details can be found in chapter II).

Previous work on 90 nm bulk technology showed that the amount of trench recess may exacerbate the off state leakage current before and after irradiation [13]; therefore, the effect of varying the trench recess on the off state leakage current for 90 nm SOI devices has been investigated. The amount of trench recess was varied; a range with a maximum of 20% recess of the nominal trench depth is considered. Structures in which the trench fill is recessed below the surface by 10.8, 18, 36, 54 and 72 nm, corresponding to 3, 5, 10, 15 and 20% of the nominal trench depth, respectively were simulated. Fig. 5.1 shows the pre-irradiation off-state leakage current versus trench recess depth, for planar devices (amount of recess, X = 0 nm), as well as those in which the top of the fill is recessed by X = 10.8, 18, 36, 54 and 72 nm. The results show that the trench recess has little effect on the pre-irradiation off-state current of these SOI devices due to the high doping of the active body.

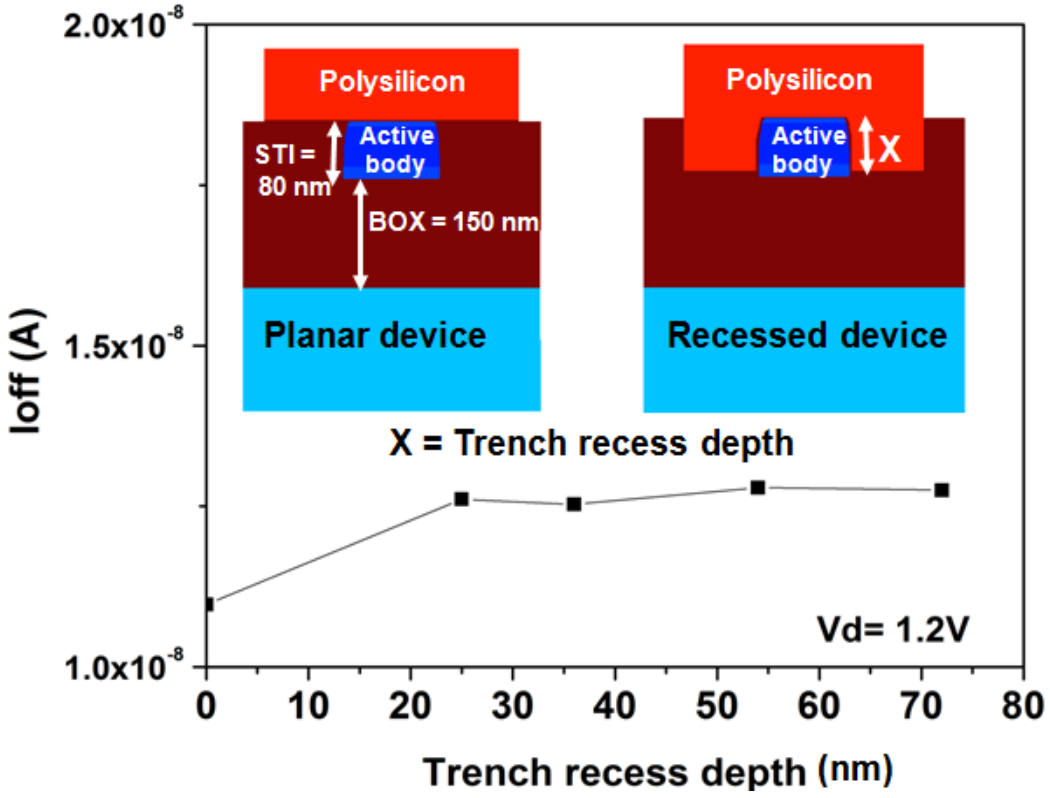


Fig. 5.1. The pre-irradiation off-state leakage current evolution with trench-recess depth.

b. Post-irradiation results: 90 nm PDSOI

Radiation-induced charge was simulated by varying the charge density uniformly at the silicon/STI interface (N_{ot}) along: (1) the entire STI sidewalls, (2) the back interface only, and (3) both sidewalls and back interface (which represents a more realistic case, although the relative values may differ due to trap density and electric field differences). The post-irradiation results for uniform sheet charge concentrations of 10^{12} and 10^{13} cm^{-2}, for the three cases described above, are shown in Fig. 5.2.

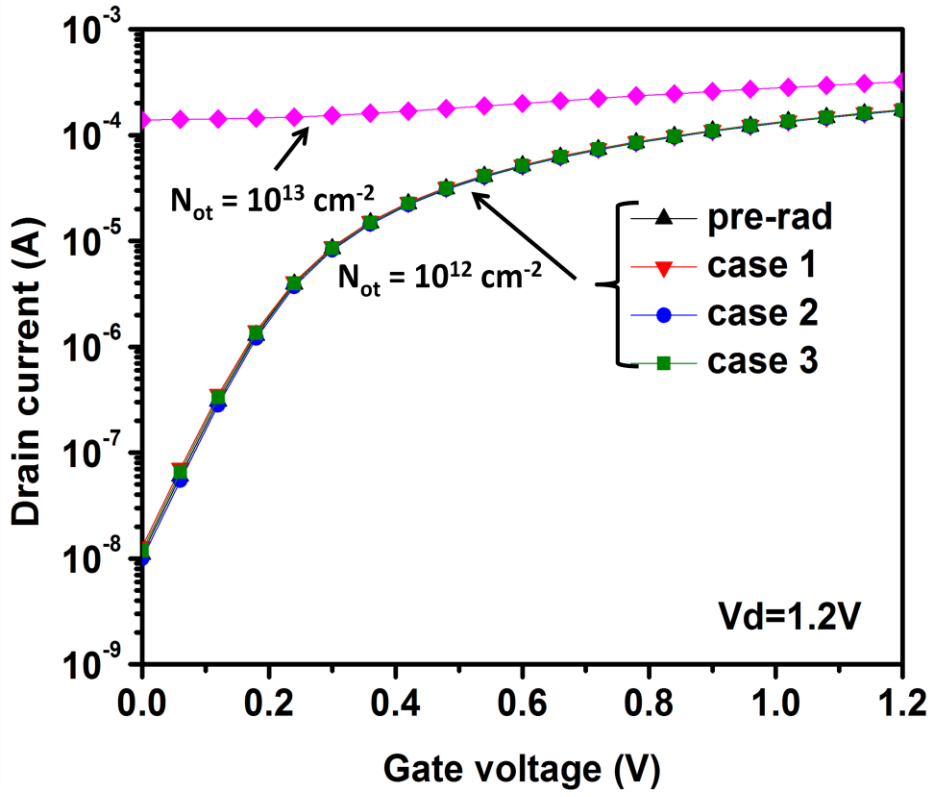


Fig. 5.2. The pre and post radiation results for the 3 cases (described in the text) for an N_{ot} = 10^{12} cm^{-2} and 10^{13} cm^{-2} [25].

The results show that there is a lack of TID sensitivity due to the high body doping inherent in the SOI devices at radiation-induced charge densities up to at least 10^{12} cm^{-2}. It is worth noting that the oxide charge areal density required to invert silicon doped at 10^{18} cm^{-3} is ~ 10^{12} cm^{-2}. Therefore a very high N_{ot} is required to overcome the high body doping, as seen for N_{ot} = 10^{13} cm^{-2}. Actual trapped charge values for a given TID depend on the specific process details. However, it has generally been found that trapped charge tends to saturate in the low 10^{12} cm^{-2} range for high quality thermal oxides [52]-[53]. Representative experimental results on a commercial floating body 45 nm NMOS SOI device, show relative insensitivity to TID, consistent with the 90 nm simulations, as shown in Fig. 5.3.

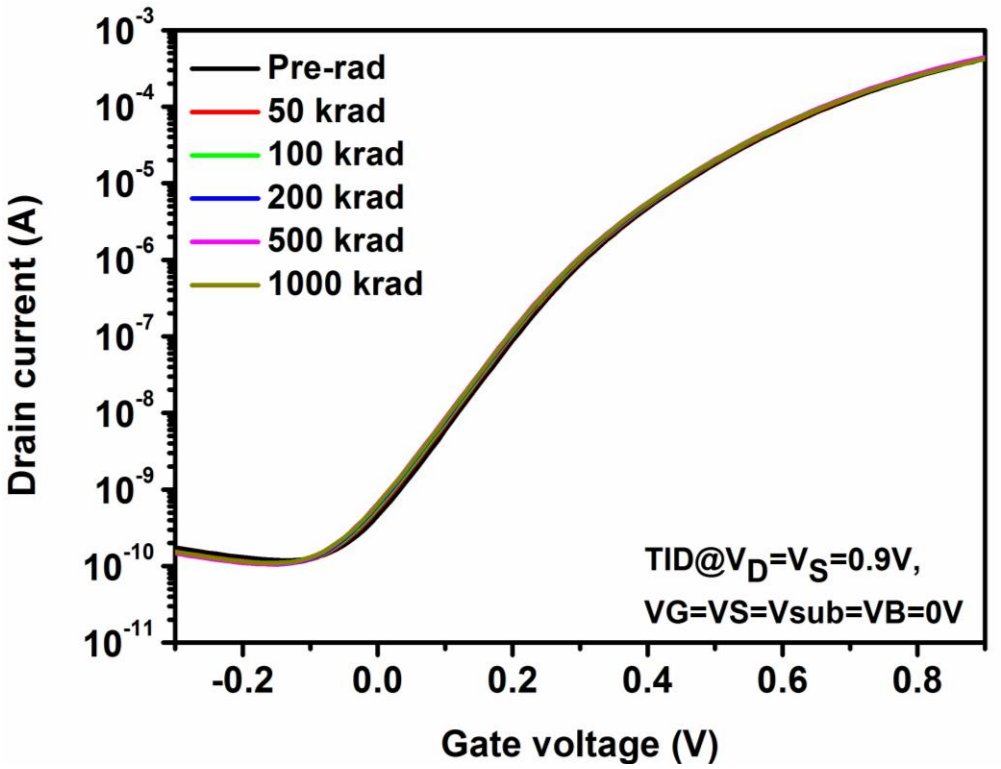
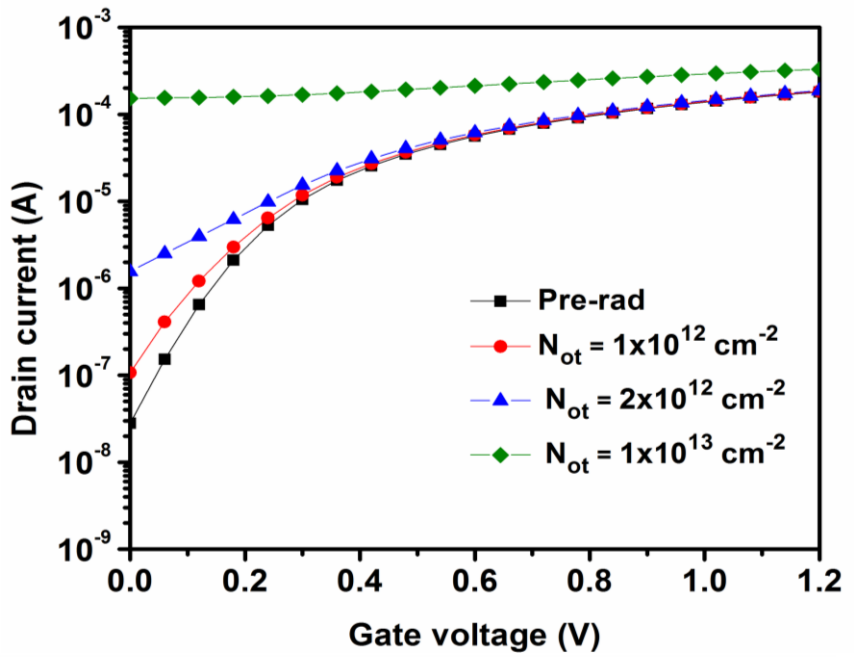
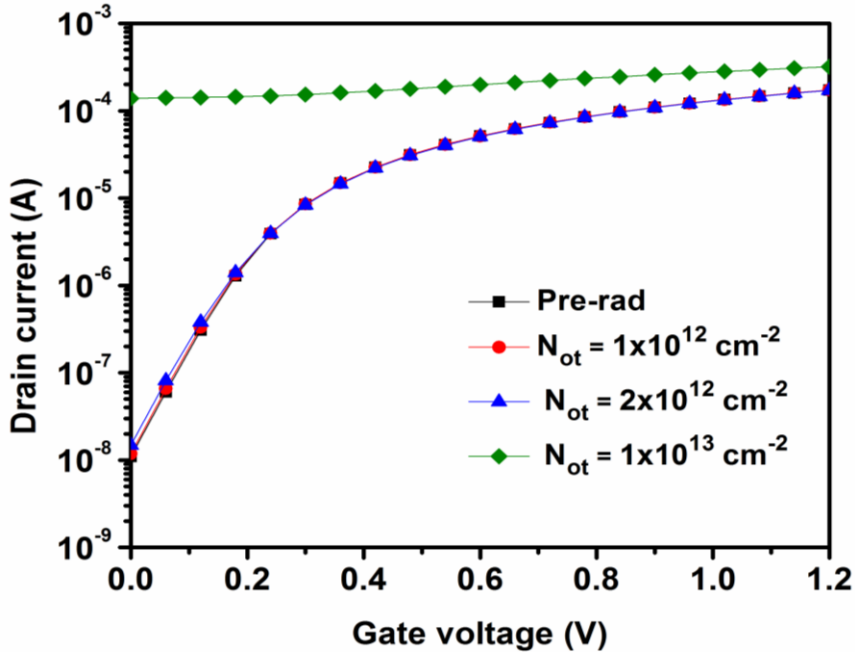


Fig. 5.3. The pre- and post-irradiation experimental results of 45 nm SOI device [25].

Fig 5.4 shows the effect of extending the well doping all the way to the sidewall. The devices are insensitive to TID only when the doping reaches the STI sidewalls and back channel. For the case where the doping does not reach the sidewalls (Fig. 5.4 (Top)), the off-state leakage current increases with N_{ot}.



(a)



(b)

Fig. 5.4. The pre and post radiation results for the cases where (a) the doping is not extended to the sidewalls, and (b) the doping is extended to the sidewalls

C. Post-irradiation results: 45 nm PDSOI and FDSOI

The previous section's results on the hypothetical 90 nm PDSOI device indicate that high

body doping in PDSOI results in insensitivity to trench recess and to TID. TCAD simulations indicate that the high doping required mitigates the TID effects in standard 90 nm SOI devices. Additional characterizations of the VU 45 nm SOI test chip have supported this and results are described in this section. A 45 nm PDSOI device was constructed in 3D Synopsys Dessis, which was calibrated to the 45 nm SOI IBM PDK. Details about the device and doping profiles can be found in chapter II. As mentioned previously, radiation-induced charge was simulated by varying the charge density uniformly at the silicon/STI interface (N_{ot}) along both sidewalls and back interface. The post-irradiation results for uniform sheet charge concentrations of 5×10^{11} cm^{-2}, 10^{12} and 2×10^{12} cm^{-2} are shown in Fig. 5.5. Only minor sensitivity is observed for the doping profile and work function chosen. In addition, a variety of 45 nm SOI devices were measured from the VU test chip, as shown in Fig. 5.6.

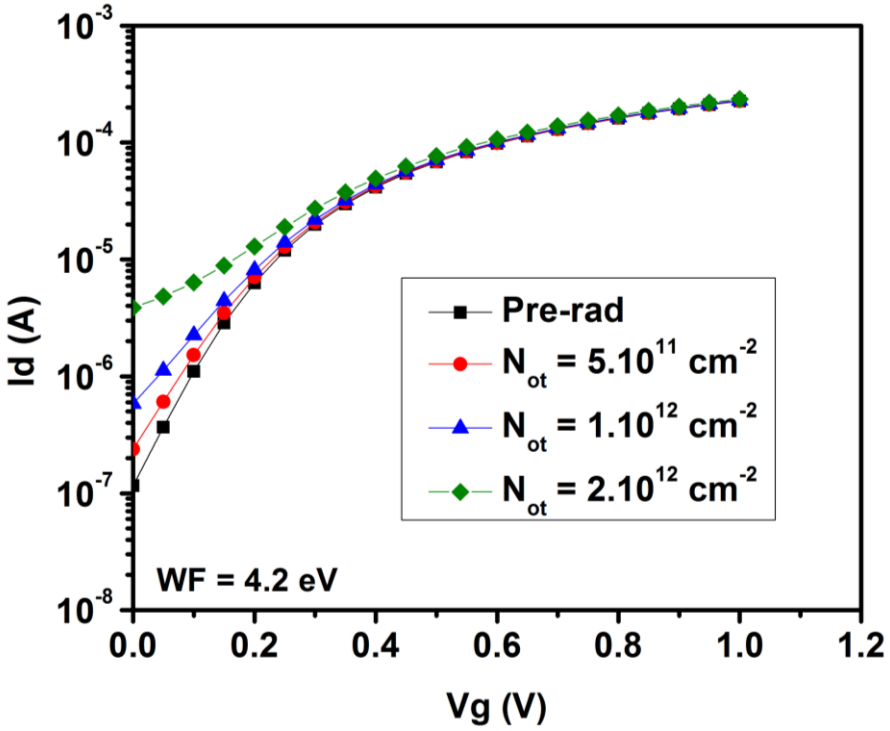


Fig. 5.5. Post-irradiation results for uniform sheet charge concentrations of 5×10^{11} cm^{-2}, 10^{12} and 2×10^{12} cm^{-2}.

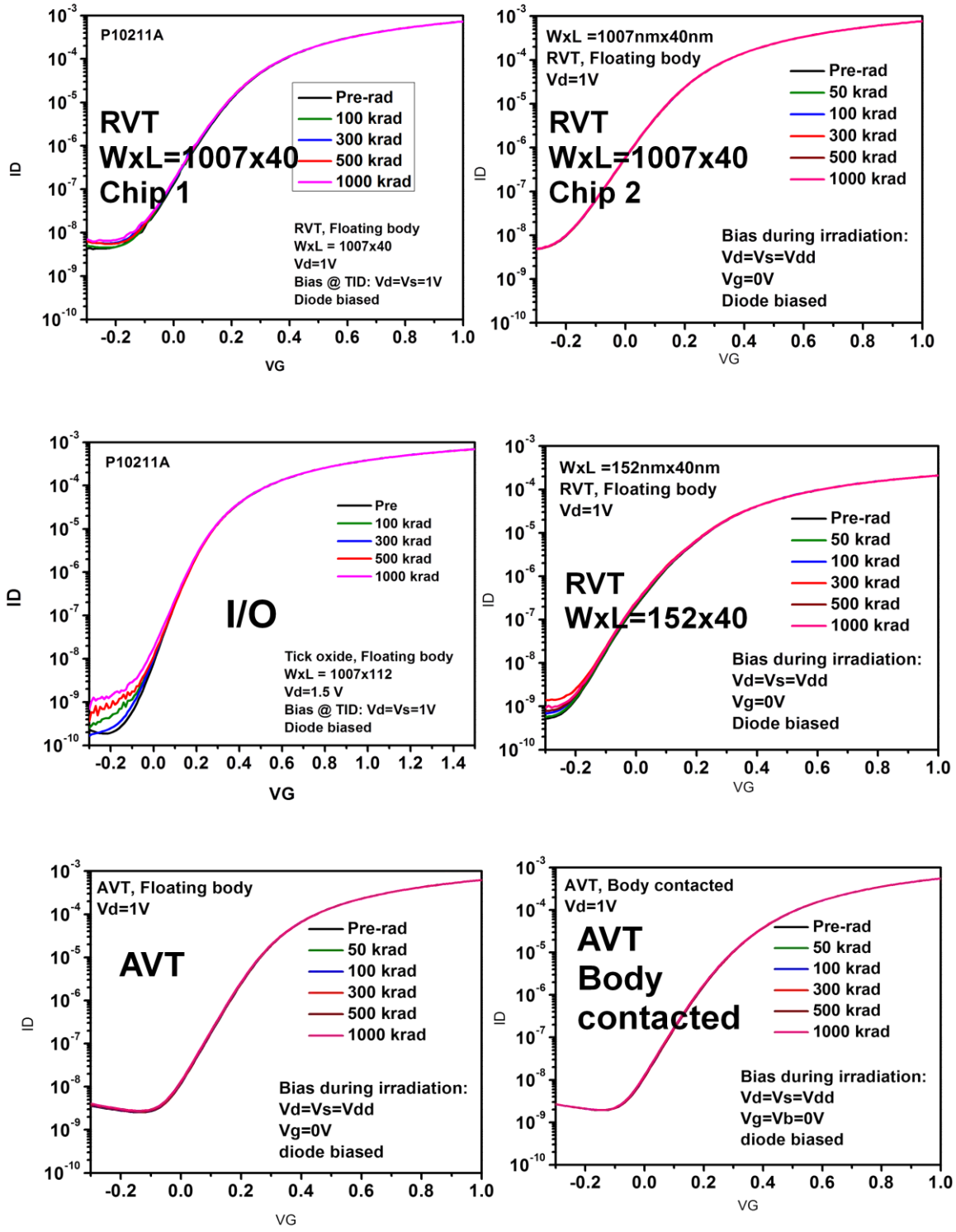


Fig. 5.6. I_dV_g of a variety of 45 nm PDSOI devices including different layout, V_T variant, as well as core vs. I/O devices.

Overall the general trend that the high body doping reduces the sensitivity to TID is still true for the 45 nm SOI technologies for different layouts (W = 1007 nm vs. W = 152 nm), V_T variants (AVT vs. RVT) and device type (core vs. IO devices).

Specially fabricated (not for commercial use) experimental 45 nm FDSOI devices were also radiation tested for comparison with 45 nm PDSOI. Previous simulations of FDSOI devices indicated that the devices were likely to be sensitive to TID [54]. The measured results reported here show that the FDSOI devices exhibit a pronounced TID sensitivity, as shown in Fig. 5.7, due to the light body doing and strong electrical coupling of the front gate to the charge trapping in the BOX.

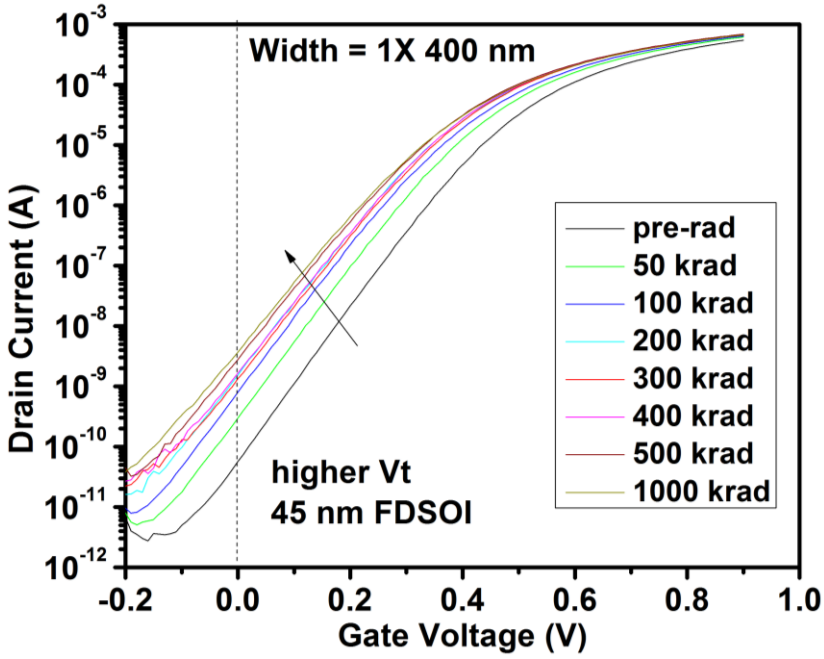


Fig. 5.7. Experimental results for specially designed 45 nm FDSOI devices [27].

d. ESD diode consideration (45 nm PDSOI) :

When measuring the 45 nm PDSOI devices with ESD diodes, it has been found that the biasing/ non-biasing of the diodes directly affects the device response before and after

irradiation, especially at low V_G as shown in Fig. 5.8. Before irradiation, the leakage current is larger by an order of magnitude when the diodes are unbiased. The gate current also increased significantly when the diodes were unbiased as shown in Fig. 5.8. Therefore, the observed leakage current comes from the ESD diodes. For the devices considered here in order to get the real device response, the diode should be biased. Therefore the biasing/non-biasing of ESD diodes on test devices can impact the observed results at low V_G and should be taken into consideration for future testing and when interpreting experimental results.

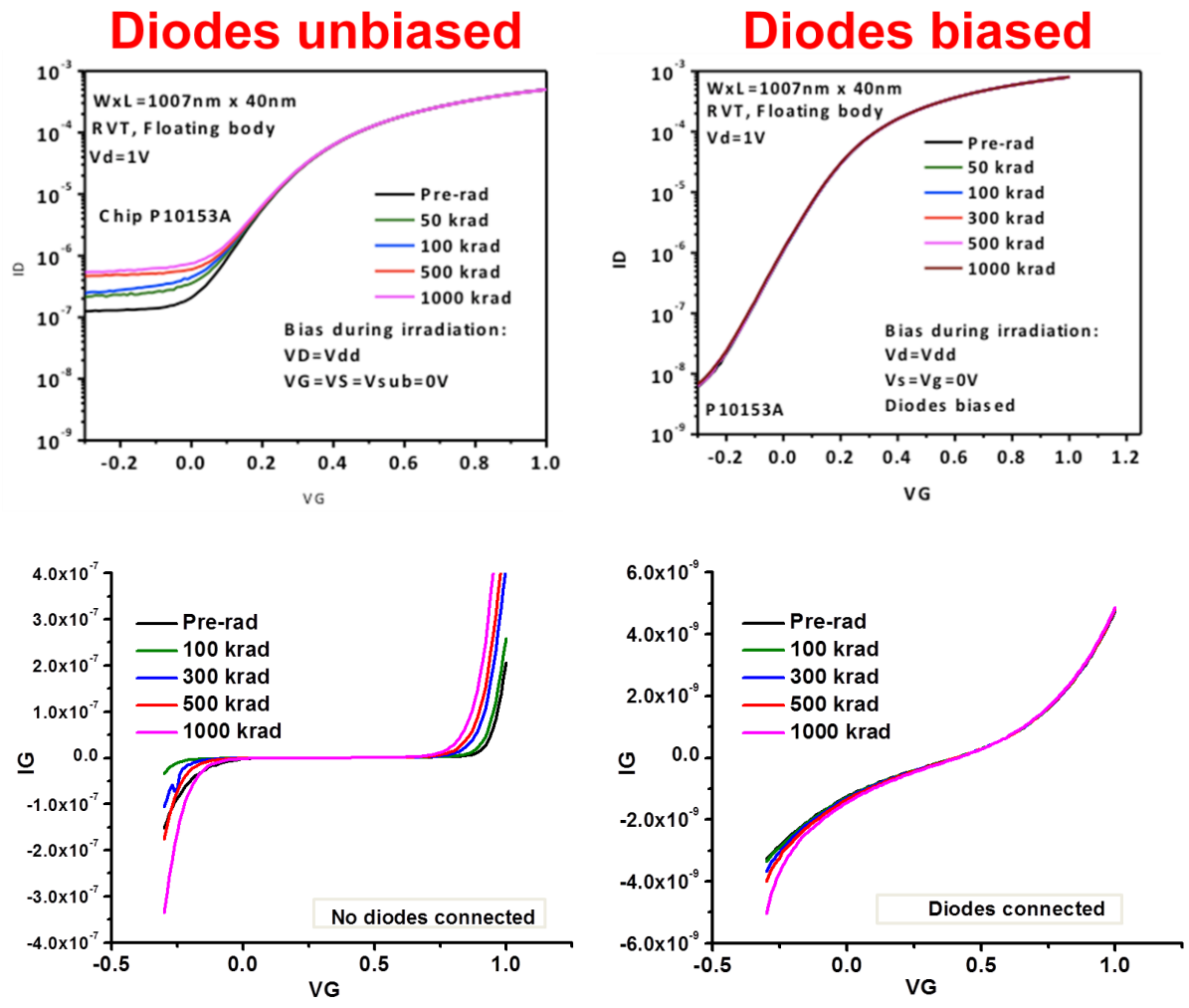


Fig. 5.8. I_dV_g (top figures) and I_gV_g (bottom figures) characteristics for the same device with (right) and without (left) biasing the ESD diodes, showing the ESD diodes effect.

C. TID response of 32 nm PDSOI using high-k metal gates

a. Introduction

Silicon dioxide has been the primary gate insulator since MOS ICs were first developed. To achieve the drive currents required by advances in IC technology, gate dielectrics are becoming extremely thin. They are reaching the point where electron tunneling can cause prohibitively large increases in power consumption [55]. To circumvent this problem, alternate gate dielectrics with high dielectric constants (also referred to as "high-k" dielectrics) have been introduced. However, replacing SiO_2 with high-k materials leads to two problems due to interaction with the polysilicon gate electrode:

1. Threshold voltage pinning – defects that arise at the gate dielectric/gate electrode boundary cause the voltage at which the transistor switches to be too high.

2. Phonon scattering – electrons are made less mobile (they slow down).

Both of these problems limit the transistor's switching speed. The solution is to use metal gates, using different metals for the NMOS and PMOS transistors. In selecting the gate metal material, the work function of the metal gate should be given the most consideration, since it determines the threshold voltage (V_T) of the MOSFET.

The 32 nm IBM PD SOI technology uses a high-k dielectric and metal gates. Since the doping profiles depend on the gate work function, the question arises as to whether doping changes associated with the metal gate work function change the TID sensitivity compared to the previous generations.

In this section, 3D TCAD simulations were applied to examine the sensitivity of device I-V characteristics to gate work function change and to charge trapped in the sidewall oxides and BOX interfaces with the active silicon regions. The choice of gate-metal work function

determines the doping profile required to get the desired threshold voltage and leakage current. The simulation results indicate that the body doping densities for the range of work functions considered can impact the TID response. Experimental TID measurements of commercial PD SOI 32 nm floating body NMOS SOI devices are consistent with these simulation results.

b. Work function calibration

A 32 nm partially-depleted NMOS SOI device was constructed in 3D Synopsys Dessis, which was calibrated to the 32 nm SOI IBM PDK. The doping profile and IV curve calibration can be found in chapter II. Three different gate work functions were simulated (4.1, 4.2 and 4.4 eV). In each case the doping was changed (within a reasonable overall doping range, consistent with previous modeling [25]), to approximately match the V_T and I_{off} of the PDK. Radiation-induced charge was simulated by varying the charge density uniformly at the silicon/STI interface (N_{ot}) along both sidewalls and the back interface.

c. Work function sensitivity study

Changing the work function shifts the threshold voltage and consequently the off state leakage current. Since V_T and I_{off} shift with the work function change, a recalibration of the doping profile to get the same V_T and I_{off} as the PDK is necessary for both $\Phi_M = 4.1$ and $\Phi_M = 4.4$ eV. For $\Phi_M = 4.1$ eV the doping magnitude is now $\sim 4 \times 10^{18}$ to 2×10^{19} cm^{-3} in order to get the same V_T and I_{off} as the PDK; both the recalibrated doping profile as well as the I_dV_g curve are shown in Fig. 5.9. Similarly the doping profile of the body was modified for $\Phi_M = 4.4$ eV to match the PDK model, and the results are shown in Fig. 5.10. The post-irradiation results for uniform sheet charge concentrations of 5×10^{11}, 10^{12} and 2×10^{12} cm^{-2}, for all three work function values, are shown in Fig. 5.11 ((a), (b), (c)). The results show that the current at $V_G = 0$ increases by an order of magnitude for the charge densities simulated in the devices with work

functions of 4.2 and 4.4 eV. Again note that the oxide charge areal density required to invert silicon doped at 10^{18} cm^{-3} is ~ 10^{12} cm^{-2}.

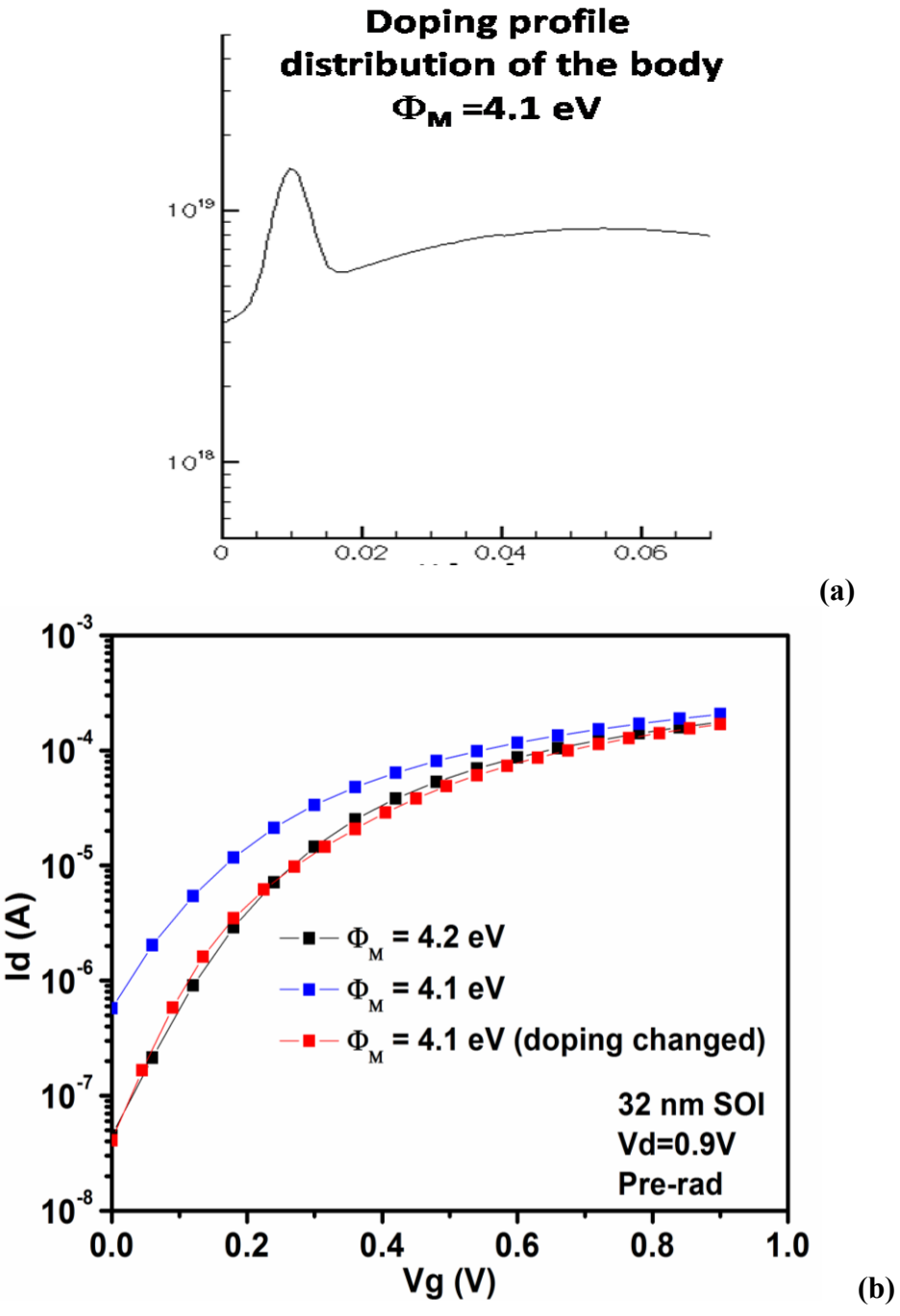
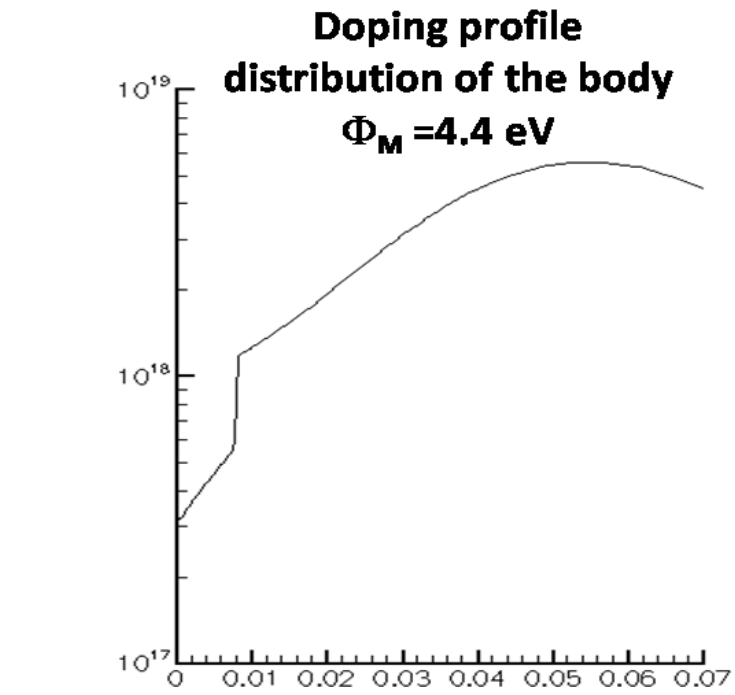
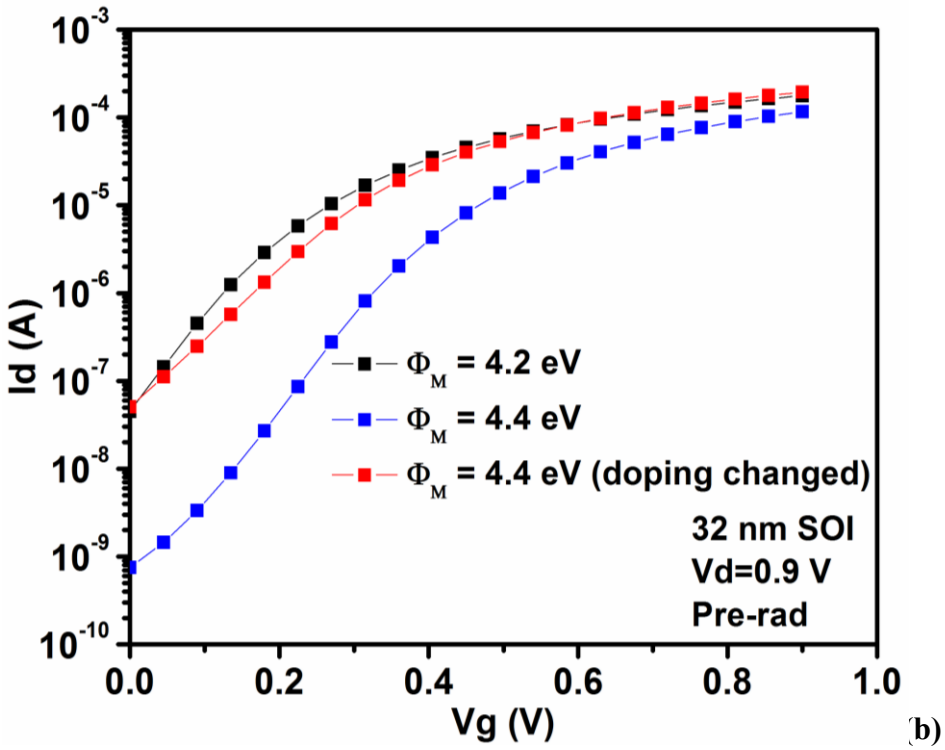


Fig. 5.9. (a) Recalibrated doping profile, and (b) I_dV_g curve resulting from doping profile change to match PDK model. (Φ_M =4.1 eV) [27].



(a)



(b)

Fig. 5.10. (a) Recalibrated doping profile, and (b) I_dV_g curve resulting from doping profile change to match PDK model. (Φ_M =4.4 eV) [27].

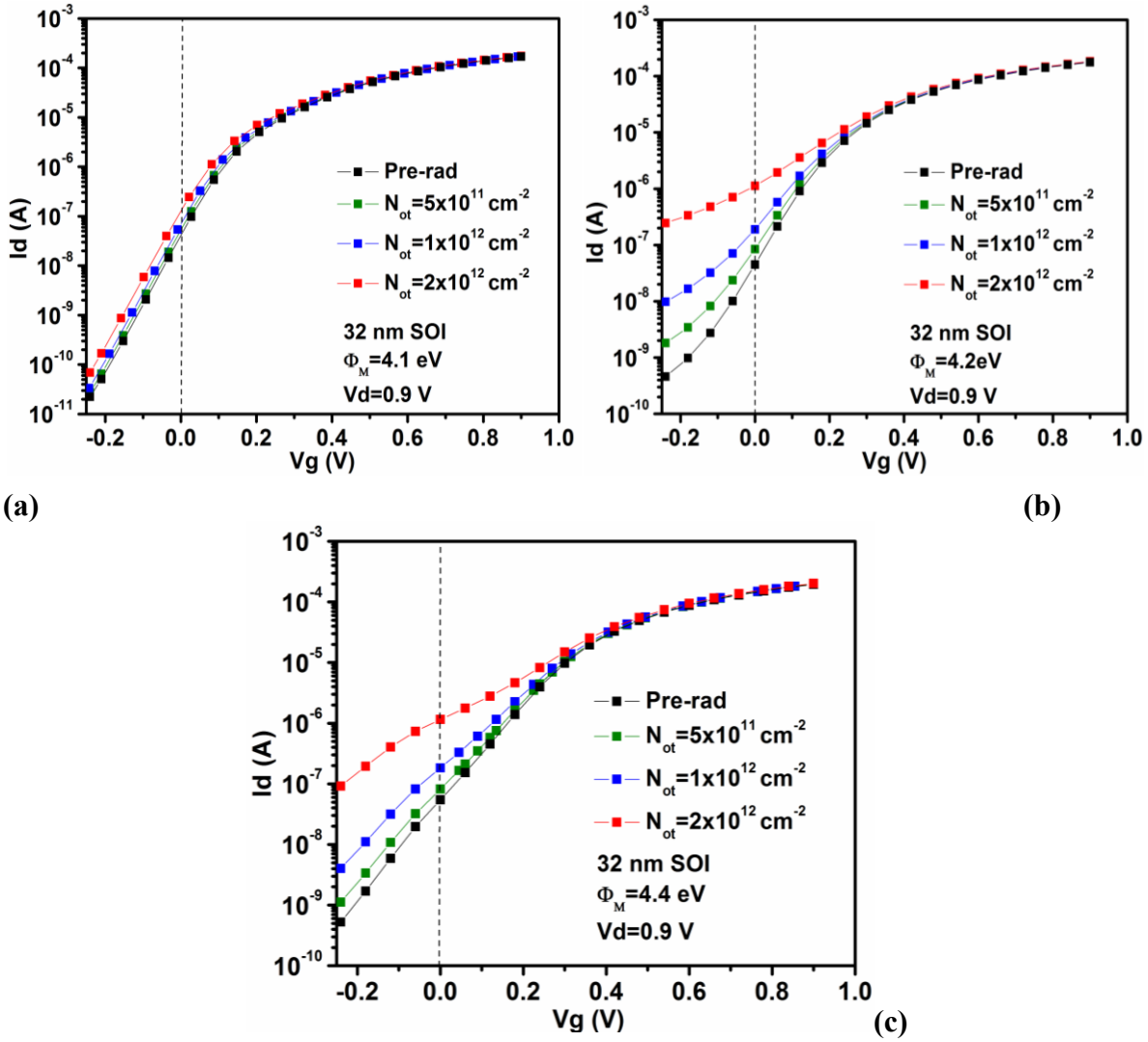


Fig .5.11. The pre- and post-irradiation simulation results for (a) Φ_M =4.1eV, (b) Φ_M =4.2 eV, and (c) Φ_M =4.4 eV [27].

d. 32 nm PDSOI data

Representative experimental results on a commercial 32 nm NMOS SOI device (both low and high V_T devices), using high-k metal gate, are shown in Fig. 5.12. The off-state current increases by about 5× at $V_G = 0$ with 1 Mrad (SiO_2) for the lower V_T device but shows negligible change in the higher V_T device.

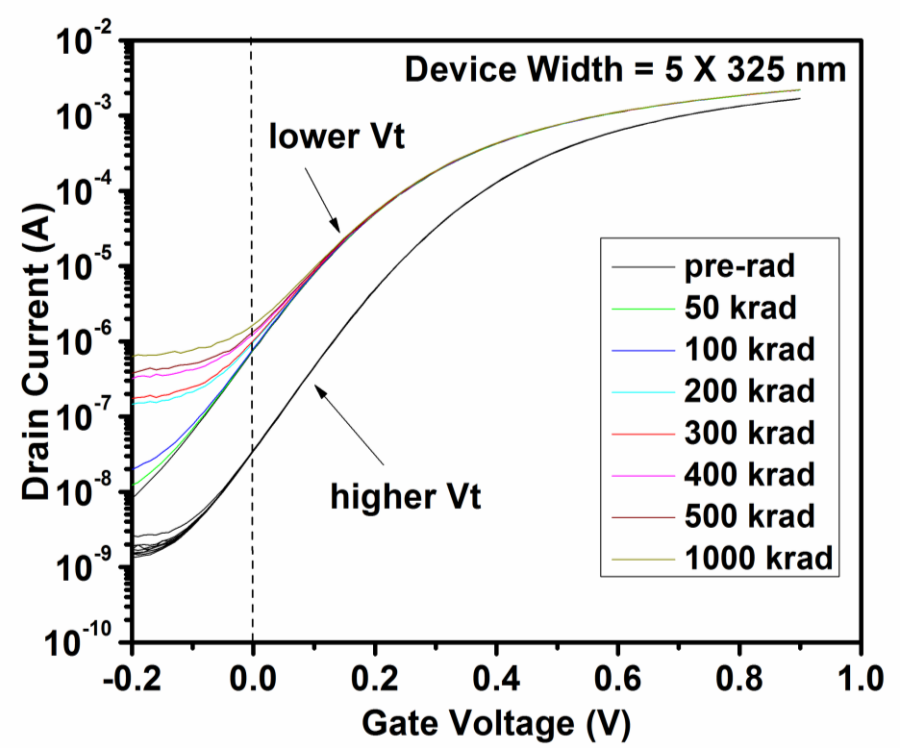


Fig 5.12. Experimental results of low and high V_T 32 nm PDSOI devices [27].

Finally a 32 nm PDSOI ring oscillator from the VU test chip was tested, to see if the insensitivity to TID observed in the indvidul devices still holds for a circuit. The ring oscillator was irradiated up to a TID of 5 Mrad(SiO_2), and no change in the frequency was observed as shown in Fig. 5.13. Also, no change in power supply current was seen with TID. Therefore, the 32 nm PDSOI ring oscillator is relatively insensitive to TID, consistent with the device-level results.

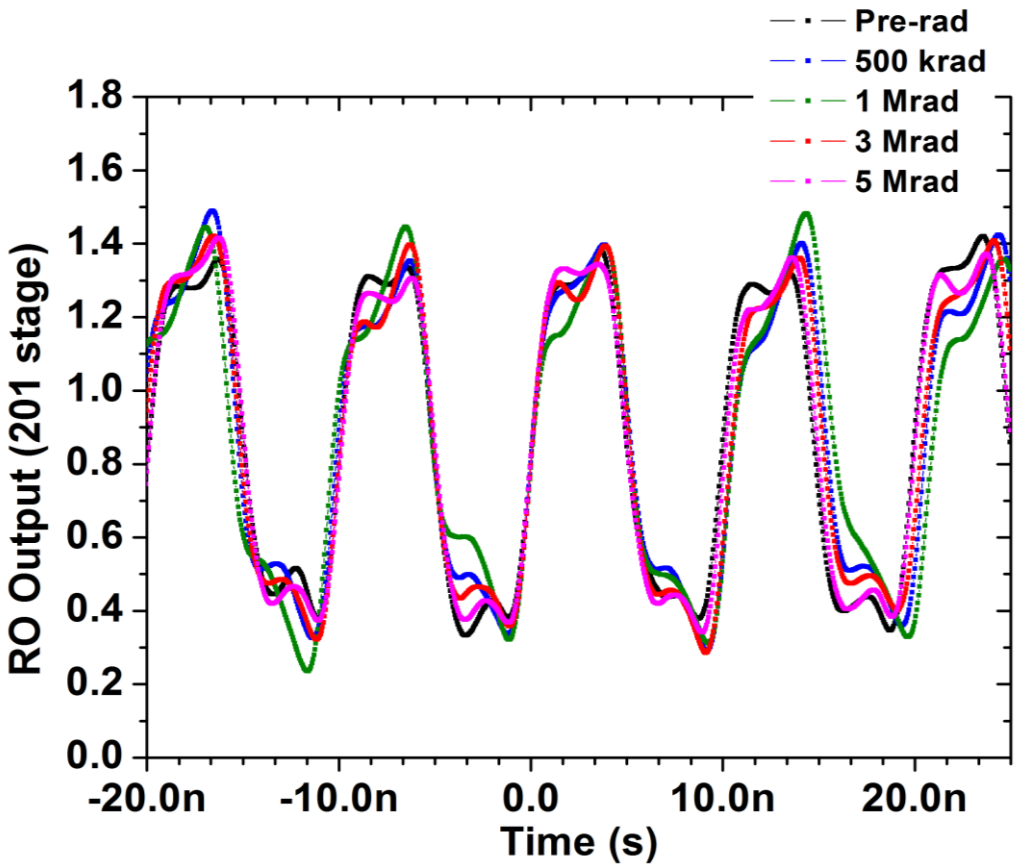


Fig. 5.13. Output waveform of 32 nm PDSOI ring oscillator.

E. Implications for future technologies

Bulk scaling relies on increasing well and halo doping concentrations to suppress short-channel effects SCE (I_{off}). Heavy channel doping creates problems such as increasing GIDL and junction leakage, as well as increasing random doping fluctuations that result in V_T variations. Therefore scaling bulk technologies below 20 nm is very challenging and new device options are needed, such as fully depleted devices with undoped thin body (ultra thin FDSOI, FinFETs, tri-gate, nanowire…).

a. Ultra-thin FDSOI

Fully-depleted (FD) SOI using a very thin, lightly-doped silicon layer, is a contender for next generation CMOS. In this case, the higher body doping used in the PDSOI devices is no longer present, and the BOX layer is electrically coupled to the front oxide, making TID-induced changes more of a concern. In FDSOI, the back and front channels are electrically coupled due to the light doping of the thin SOI layers [56]. The front-gate threshold voltage as a function of the back-gate bias is shown in Fig 5.14. As expected, the threshold voltage of the fully depleted transistor shows a strong coupling effect with the back-gate bias, which is not seen in the partially depleted curve. For TID irradiation, charge trapped in the BOX can lead to front V_T shifts.

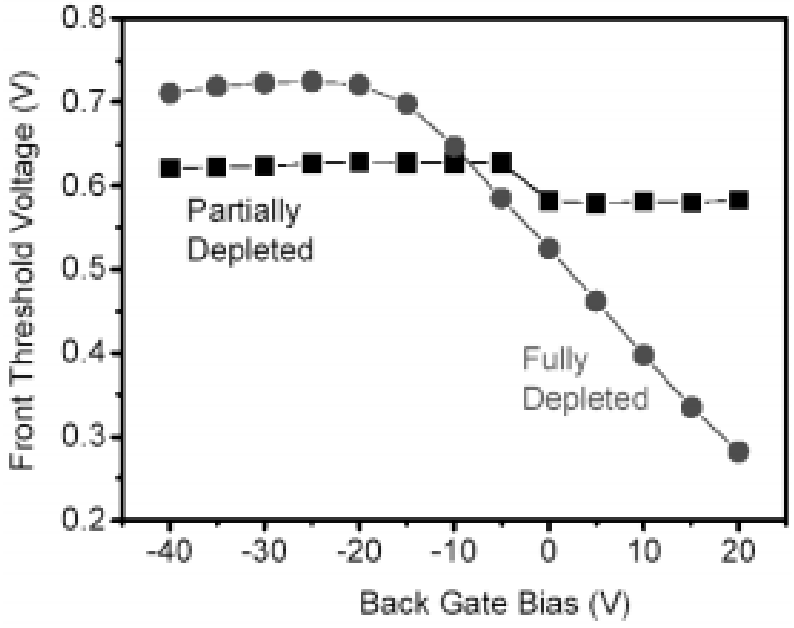


Fig. 5.14. The front gate-threshold voltage as a function of the back-gate bias [56].

A hypothetical 22 nm NMOS ultra thin fully depleted SOI device was constructed using 2D TCAD simulations, where 6 nm SOI and 25 nm BOX thicknesses were assumed. Radiation-

induced charge was simulated by varying the positive charge density uniformly at the SOI/BOX interface as shown in Fig. 5.15, for uniform sheet charge concentrations of 1×10^{11} cm^{-2} and 1×10^{12} cm^{-2}. The simulated drain current is plotted vs. gate voltage in Fig. 5.16, indicating V_T shifts of approximately 90 mV for 1×10^{12} cm^{-2} fixed charge density.

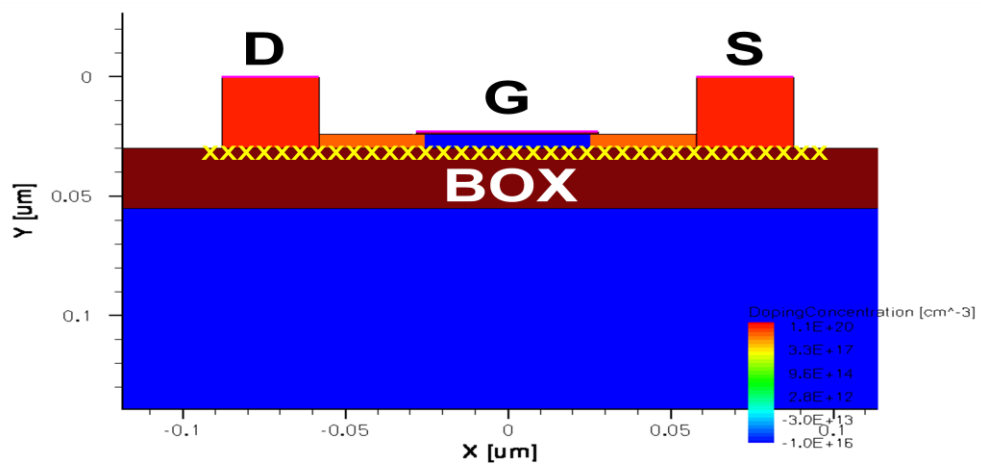


Fig. 5.15. 2D TCAD view of 22 nm UTFDSOI devices showing fixed charge sheet at the SOI/BOX interface.

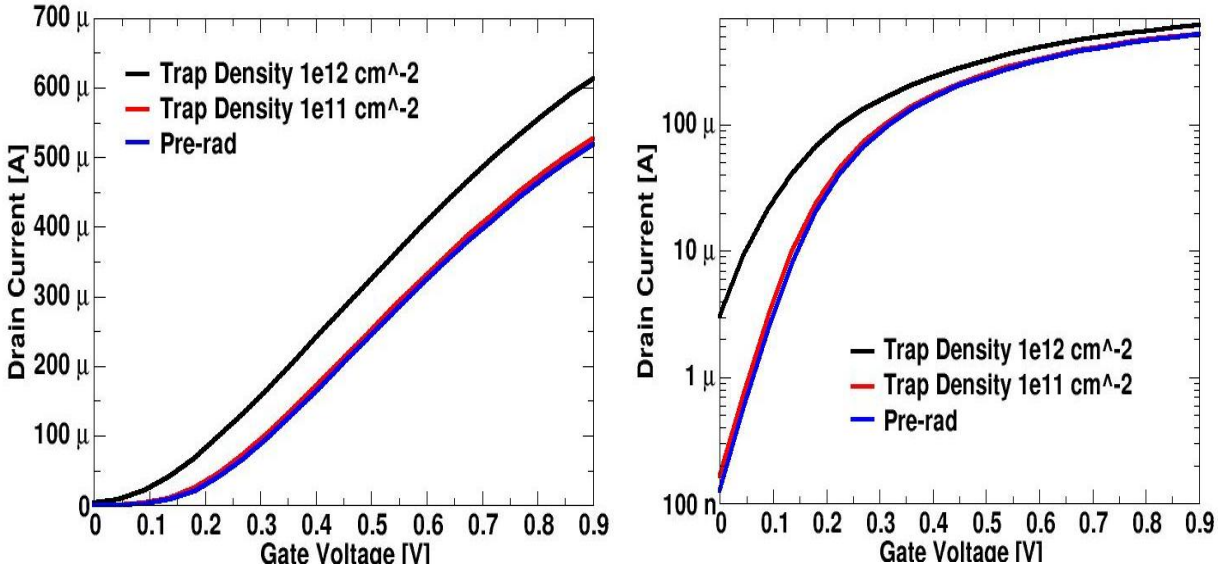


Fig. 5.16. I_dV_g in linear scale (left), and log scale (right), showing V_T shift for uniform sheet charge concentrations of 1×10^{11} cm^{-2} and 1×10^{12} cm^{-2}.

b. TID in FD FinFETS

In order to increase the current drive, enhance the control of short-channel effects, and improve the TID response of SOI devices, three-dimensional SOI MOSFETs with nonplanar (multigate) structures are under consideration, double gate SOI offer an increase in carrier mobility and velocity due to reduced influence of the scattering associated with oxide and interface charges and surface roughness. SOI FinFETs are good candidates and TID effects in FinFETs were investigated in the past few years. The results presented in Fig 5.17 show the TID response of FinFETs with different fin widths (40 nm, 65 nm and 80 nm), where wider FinFETs (80 nm) behave more like planar devices than 40-nm devices. The higher tolerance to radiation-induced charge for the narrower FinFETs is attributed to the additional lateral gate control over the body potential [57].

F. Conclusions

Device simulations and measurements indicate that sub-100 nm partially-depleted SOI devices (90 nm and 45 nm PDSOI) are relatively insensitive to TID radiation effects due to the high body doping employed. This is predicated on the assumption that the high doping extends to the device sidewalls and the BOX interface. Many device variants are possible, and this condition may not be met in all cases. In addition, non-ideal effects such as dopant depletion at insulator interfaces may result in regions of lower doping for some devices or processes. The results also show that ESD diodes can play a role in observed results and should be given consideration during measurements and interpretation of the results. Specially fabricated 45 nm FDSOI devices were found to be sensitive to TID because of BOX-front gate coupling.

Device simulations and measurements indicate that changing the work function (or using high-k metal gates) in 32 nm PDSOI devices does not increase the TID sensitivity enough to

cause problems in typical applications. Additionally, TID testing of 32 nm ring oscillators show relative insensitivity to TID.

Finally FDSOI devices show some sensitivity to TID, since charge trapping in the BOX can reduce the front channel V_T. FinFETs also exhibit V_T shifts due to charge trapping in the BOX, however for narrow fin width, the additional lateral gate control results in higher tolerance.

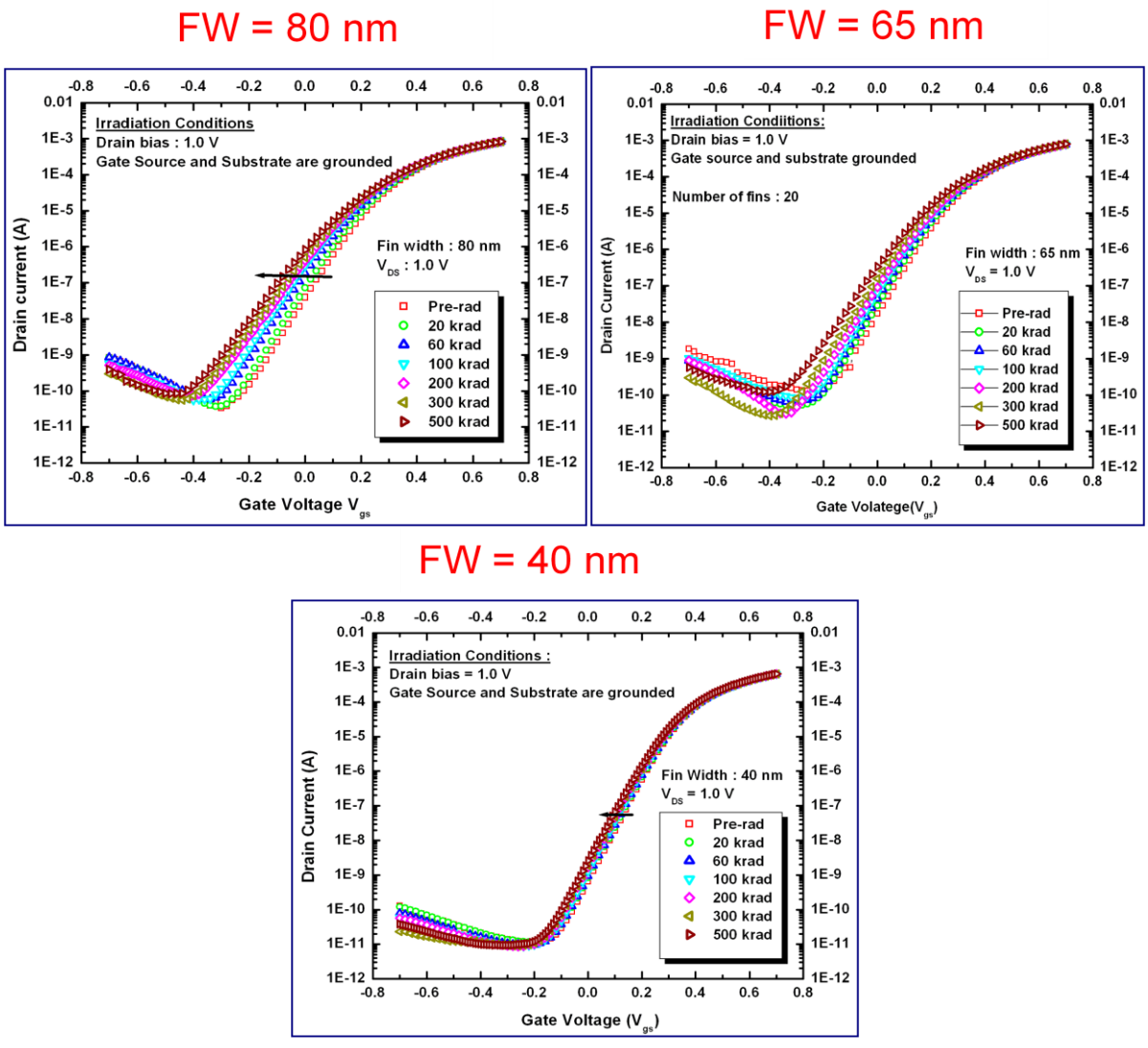


Fig. 5.17. I_dV_g characteristics of irradiated FinFETs for different fin width, 40 nm, 65 nm and 80 nm [57].

CHAPTER VI

CONCLUSIONS

The TID sensitivity of edge-related leakage current in CMOS bulk and SOI devices to key parameters: the STI contour at the active-to-isolation transition, combined with sidewall doping variations as well as layout-related stress effects was examined. These characteristics may in part account for observed differences among supposedly identically processed devices, between devices from various vendors at the same technology node, and between low power and high performance process variants. Implications for characterizing variations in TID sensitivity due to processing were noted.

The TID-induced leakage current of submicron MOSFETs has been found to increase with increasing gate-to-isolation spacing. Mechanical stress may affect the TID sensitivity through changes in dopant diffusion, boron activation, or charge trapping in the oxide. There also is a strong dependence of TID-induced current on channel width, with the narrow devices exhibiting less leakage pre-irradiation, but more leakage post-irradiation. The compressive stress dependence on the space between adjacent STI edges and doping-profile differences at the device edges affects the pre-irradiation leakage current. The enhanced radiation sensitivity for narrow devices may be related to the influence of stress in the STI oxide on the amount of positive trapped charge. Finally, mechanical stress was extracted using the measured subthreshold current characteristics. As technology scales down, stress can strongly affect radiation-induced leakage currents in ways that are difficult to predict in advance of detailed

characterization and modeling of the responses of devices across a range of representative geometries. These results are useful when designing devices for radiation environments. For the technology considered here, devices with smaller SA are less sensitive to TID; therefore designers should consider devices with minimum SA distance. Also, wider devices are less sensitive to TID compared to narrow devices.

The variability in parameters, in this case the pre- and post-irradiation off-state current, and the dependence on design parameters (device size, layout, etc.) were quantified. TID variability has been found to be most pronounced in narrow devices. In the devices investigated in this work, the effects of stress are more significant than are random dopant fluctuations. Random dopant fluctuations may contribute more significantly to variations of the threshold voltage in smaller geometries. For parasitic leakage current due to charge trapping in STI oxides, a small variation in threshold voltage that results from stress-induced changes in radiation response or random doping fluctuation can lead to a large increase in off-state leakage current.

Doping generally increases as devices become smaller for planar CMOS devices. This increase in doping decreases the sensitivity of the devices to these sources of variability in TID response of the STI. Thus, technology scaling trends for TID appear to be favorable going forward, at least until device dimensions become so small that random doping fluctuations begin to dominate the variability in response.

SOI technologies were also investigated. Device simulations and measurements indicate that sub-100 nm partially-depleted SOI devices (90 nm and 45 nm PDSOI) will tend to be insensitive to TID radiation effects due to the high body doping employed. This is predicated on the assumption that the high doping extends to the device sidewalls and the BOX interface. Many device variants are possible, and this condition may not be met in all cases. In addition,

non-ideal effects such as dopant depletion at insulator interfaces may result in regions of lower doping for some devices or processes. Specially fabricated 45 nm FDSOI devices were found to be sensitive to TID because of BOX-front gate coupling.

Through simulations and measurements it has been shown that changing the work function (or using high-k metal gates) in 32 nm PDSOI devices do not increase the TID sensitivity enough to cause problems in typical applications. Additionally TID testing of a 32 nm ring oscillator shows relative insensitivity to TID. Finally FDSOI devices show some sensitivity to TID, since charge trapping in the BOX can reduce the front channel V_T. FinFETs also exhibit V_T shifts due to charge trapping in the BOX, however for narrow fin width, the additional lateral gate control results in higher tolerance.

Therefore in advanced CMOS devices such as UTFDSOI and FD FinFETs, doping will play a role in the TID sensitivity, particularly in cases where lightly-doped regions are used.

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