TOTAL IONIZING DOSE RADIATION EFFECTS ON GERMANIUM PMOS DEVICES

By

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CHAPTER I

INTRODUCTION

Silicon has been used as a reliable and practical material for commercial Metal-Oxide-Semiconductor (MOS) devices for decades in the semiconductor industry. As the semiconductor industry approaches the physical limits of Si CMOS scaling, the introduction of novel materials and devices becomes necessary. People have been searching for alternatives to improve the performance of electronic devices. High-mobility materials are under consideration as candidates to replace Si as the channel material to achieve an electrical performance boost.

Due to the high mobility of both carriers, Ge is of great interest as an alternative channel material. However, there are still plenty of issues to be addressed in Ge MOS technology. Degradation by irradiation, high junction leakage, and low frequency noise in Ge devices are among the major challenges for practical Ge applications. In this thesis, Chapter I introduces the basic mechanisms of total ionizing dose effects and low-frequency noise analysis. Chapter II describes and reviews the devices that we investigate in the work. Chapter III explains the mechanism of high junction leakage, and Chapter IV represents the low frequency noise analysis for Ge-pMOSFETs. Chapter V summarizes and concludes the work.

1. Total ionizing dose effects

In space environments, microelectronic components are exposed to various sources of radiation such as electrons, protons, and heavy ions. Total ionizing dose irradiation remains a significant concern for the long-term reliability of electronic devices in space systems [1].

i) **Basic mechanisms of total ionizing dose irradiation**

Fig. 1.1(a) shows the normal operation of an *n*-channel MOSFET, and Fig. 1.1 (b) shows the operation of an irradiated *n*-channel MOSFET. During the normal operation, the device is turned on when a conducting channel has formed between the drain and source after an appropriate gate voltage has been applied to the gate. However, after irradiation, shown in Fig. 1.1(b), trapped charge has built up in the gate oxide and causes the threshold voltage to shift negatively. If the shift is great enough, the device may not be turned off even when 0 V is applied to the gate. In this case, the device is said to have failed by becoming depletion mode.

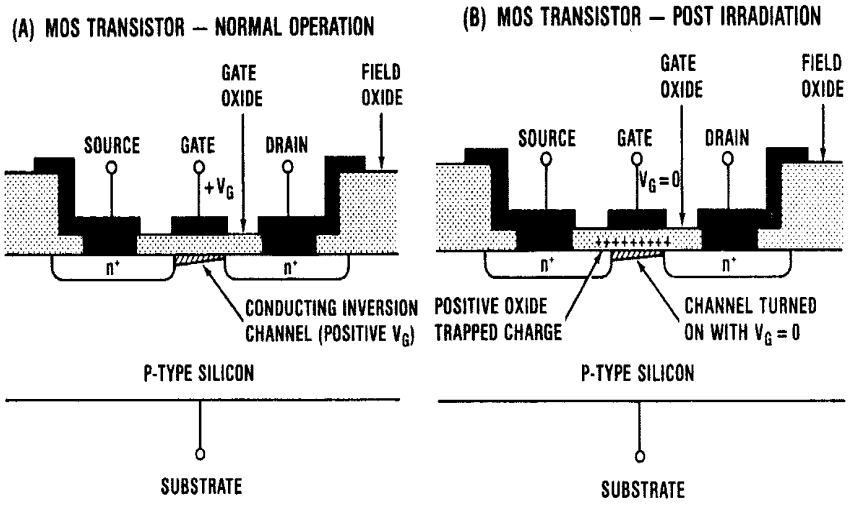


Fig. 1.1. Schematic diagram of n-channel MOSFET illustrating radiation-induced charging of the gate oxide: (a) normal operation and (b) post-irradiation. After [2].

The most sensitive parts of a MOSFET structure are the gate oxide and parasitic field oxide layers. Fig. 1.2 shows a schematic energy diagram of a MOS structure, where positive bias is applied to the gate. As a result, excess electrons are present under the gate and holes are depleted. When a device is irradiated, electron/hole pairs are generated through the oxide. Electrons are more mobile than holes and they are swept out quickly. However, a fraction of the

electrons will recombine with the holes. The holes that survive recombination may be trapped in the oxide. The processes of recombination and generation in the oxide layer will depend greatly on the energy deposited in the oxide and the type of incident particle.

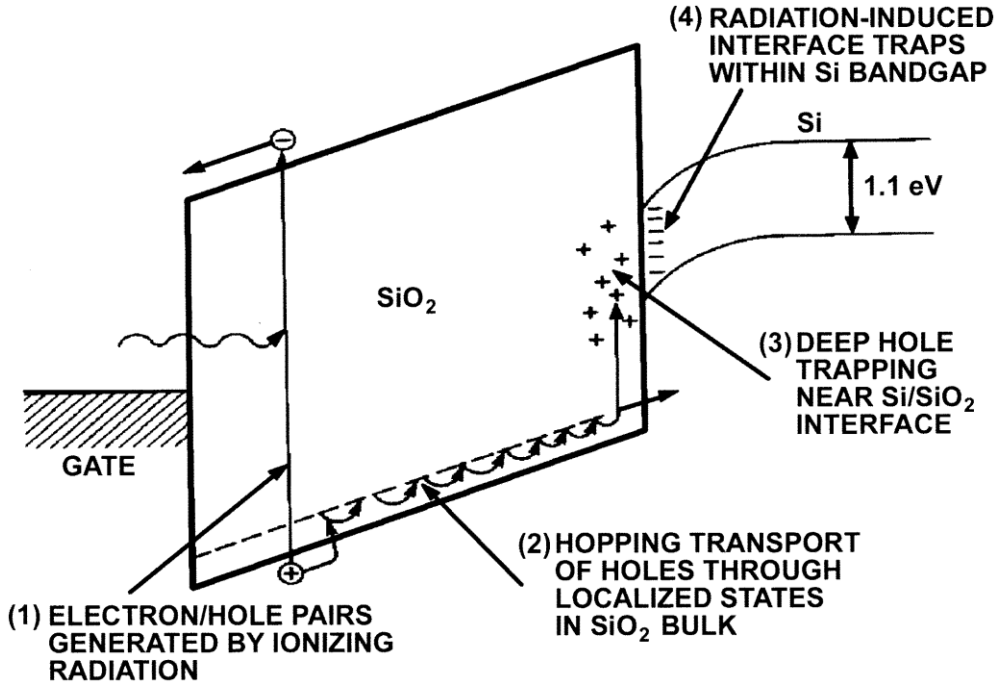


Fig. 1.2. Schematic energy band diagram for MOS structure, indicating major physical processes underlying radiation response. After [2].

ii) **Interface, oxide, and border traps**

In the gate oxides or field oxides, there are several types of process or radiation induced charges [3] [4]:

1) Fixed Oxide Charge: Q_f, N_f
2) Mobile Ionic Charge: Q_m, N_m
3) Interface Trapped Charge: Q_i, N_{it}
4) Oxide Trapped Charge: Q_{ot}, N_{ot}

5) Border Traps: Q_{bt}, N_{bt}

Both fixed oxide charge and oxide trapped charge do not communicate with the Si and stay within the oxide. Fixed oxide charge is positive and primarily due to structural defects during processing. Oxide trapped charge is net positive due to trapped holes in the oxide. Trapping results from ionizing radiation, and often can be annealed out with time. Oxygen vacancies or E' centers are electrically active states in oxides that are primarily responsible for oxide-trapped charges. The E' centers can be generated by ionizing radiation, by hole capture at a pre-existing O vacancy defect in SiO_2. A schematic illustration of an E' center is shown in Fig. 1.3. There is strong evidence that E' centers dominate the hole trapping in thermal oxides, but it is not the only defect responsible for the positive charge in thermal oxides [5]. It has also been suggested that it causes 1/*f* noise in MOS transistors [6]. Mobile ionic charge is mainly due to impurities like Na^+ during processing, and is generally not a problem for modern MOS gate oxides.

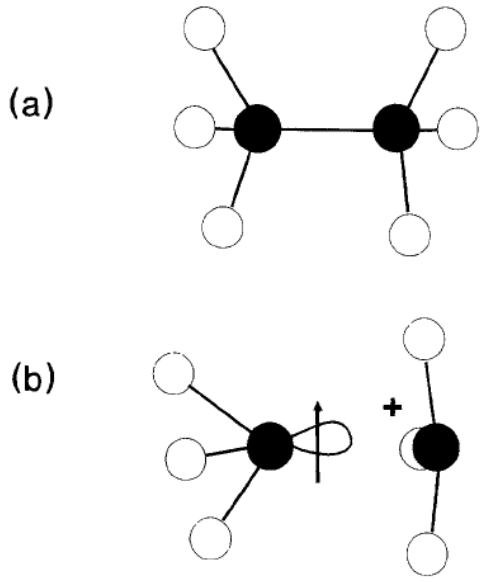


Fig. 1.3. Schematic illustration of (a) precursor and the (b) ESR active state of the E' center in SiO_2. After [5].

Interface trapped charge is located at the semiconductor-to-dielectric interface. Unlike fixed oxide charge and oxide trapped charge, interface traps are in electrical communication with the underlying silicon, so they can be charged or discharged, depending on the surface potential. Interface traps have been associated with P_b centers, which are trivalent Si defects at the interfaces of oxides and substrates [7]. Interface traps in Si typically are acceptor-like and negatively charged when filled above midgap; they are donor-like and positively charged when filled below midgap. They are charge-neutral at midgap.

Border traps lie close to the interface and are in communication with the substrate. They typically reside within a certain distance (~2 nm) in the oxide from the interface, as shown in Fig. 1.4. Border traps can also significantly impact the reliability and radiation response of MOS devices.

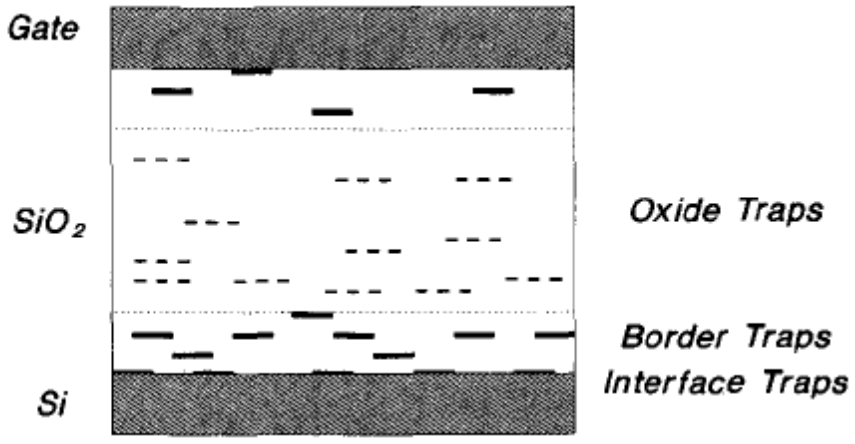


Fig. 1.4. Schematic diagram of defects in MOS structure. Border traps are in the oxide, but close to the interface. After [4].

iii) **Radiation induced degradation in MOS devices**

Radiation induced degradation in the characteristics of MOS systems can occur via the following effects:

1) Threshold voltage shift
2) Mobility degradation
3) Change in sub-threshold slope
4) Increase in junction leakage
5) Increase in noise

Threshold voltage shift and a change in sub-threshold slope can be observed from the I_d-V_g characteristics of an irradiated Ge pMOS device (one of the devices used in this work) in Fig. 1.5. The increase of off-state leakage is also shown in Fig. 1.5. The increase in junction leakage is discussed in Chapter 2 for Ge-pMOSFETs. Mobility degradation in a MOSFET with total dose irradiation is shown in Fig. 1.6.

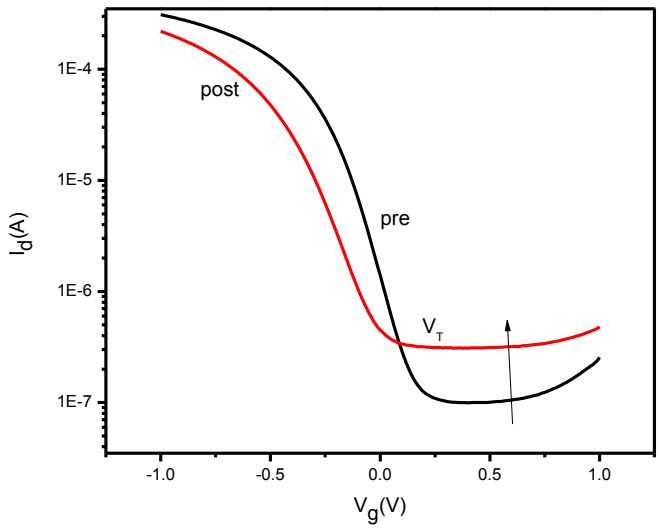


Fig. 1.5. I_d-V_g characteristics showing increase in leakage current for an irradiated Ge pMOS device.

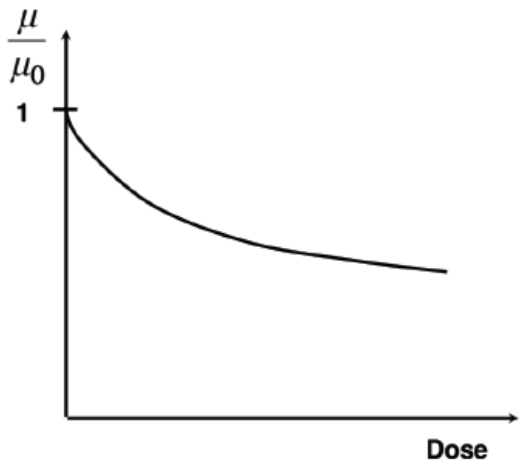


Fig. 1.6. Mobility as a function of total ionizing dose. After [8].

Most of the understanding of the basic mechanisms of radiation-induced charge generation/trapping is based on Si/SiO_2 MOS structures. However, the mechanisms are similar in high-*k* gate dielectric materials. For instance, oxygen vacancies are responsible for radiation-induced hole trapping in MOS devices with Hf-based dielectrics [9]. Nonetheless, there are differences in other aspects; for example, electron trapping is more important in high-*k* gate dielectrics than in SiO_2 [2],[10]. More work needs to be done to explore the nature and mechanisms of interactions between high-*k* materials and innovative substrate materials.

2. Annealing

Fig. 1.7 shows that the post-irradiation behavior of holes is time dependent. Shortly after initial generation of holes, they can transport under positive bias to the interface of the gate oxide and substrate, which causes short-term recovery of the threshold voltage in step (2) of Fig. 1.7. This process depends on temperature, applied electric field, oxide thickness, and processing techniques. In step (3), when transporting holes reach the interface, some of them fall into deep long-lived trap states and cause a threshold voltage shift that can persist for times as long as years. However, many of these trapped holes will anneal out in thin oxides, like the ones we

evaluate in this thesis. The last step is the interface-trap buildup right at the interface between gate oxide and substrate. The occupancy of the localized states is determined by the Fermi level and applied voltage. The positive threshold voltage shift due to "rebound" or "super-recovery" that is illustrated schematically in Fig. 1.7 only occurs for nMOS devices, and is typically not observed in thin oxides, owing to their relatively small interface-trap densities [11].

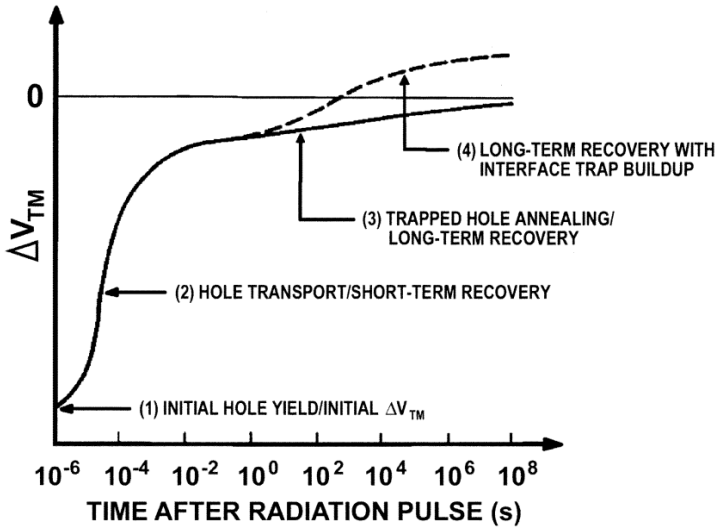


Fig. 1.7. Schematic time-dependent post-irradiation voltage recovery of n-channel MOSFET, relating major features of the response to underlying physical processes. After [2].

3. Low-frequency noise theory

There are a variety of physical models that have been proposed to describe the 1/*f*-noise of MOS transistors [12]. However, here we only consider the effects of process differences on noise related to near-interfacial oxide traps (border traps) at room temperature. We define the excess drain-voltage noise power spectral density S_V as [13]:

$$S_V = K \cdot f^{-\alpha} \cdot \frac{(Vd)^2}{(Vg-Vt)^2} \tag{1}$$

S_V is measured at room temperature in the linear regime of device operation. K is the device-dependent noise level. V_g is the gate voltage, and V_d is the drain voltage. In the devices considered here, S_V is proportional to $f^{-\alpha}$, with α approximately equal to 1.05 ± 0.15 [14] [15].

It is widely believed that the *1/f*-noise is related to the capture and emission of charge carriers from traps within the oxide and interface. The fluctuations in near-interfacial oxide trap charge couple to the channel by compensation in the inversion layer or scattering of carriers [16]. For pMOS devices, it has been suggested that *1/f*-noise involves both kinds of fluctuations. These are known as number and mobility fluctuations [17]. This will be discussed in Chapter IV.

CHAPTER II

GERMANIUM pMOS DEVICES AND EXPERIMENTS

1. Overview of Ge MOSFETs

i) High-*k* dielectrics

According to Moore's Law in Fig 2.1 [18], every two years, the physical dimensions have been diminished to double the total number of the transistors on a chip. The scaling of MOS devices has led to higher capacities of functions per unit chip, reduced cost per capacity, and increased performance. However, the shrinking size brings about other issues at the same time. When the physical thickness of the gate oxide is smaller than ~2 nm, electron tunneling and oxide leakage become unacceptably high. In order to reduce the gate leakage, high-*k* dielectric materials, along with gate control technologies, like work function control of metal gate electrodes, are now included in technologies that feature 45 nm or smaller dimensions [19].

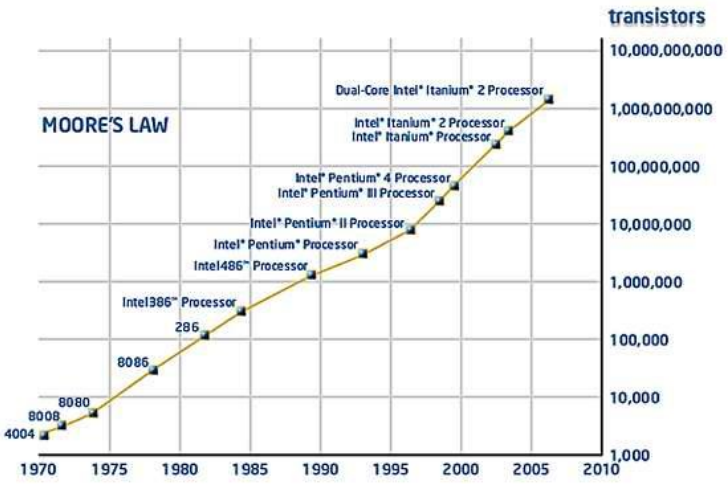


Fig. 2.1. Illustration of Moore's Law. After [18].

High-*k* materials, such as HfO_2 or ZrO_2, as listed in Table 1, can have a thicker physical gate oxide layer while maintaining low electrical oxide thickness. The 'equivalent oxide thickness' (EOT) can be defined as

$$T_{ox} = EOT = (3.9/k)\, t_{Hik} \qquad Eq\ 2$$

Here 3.9 is the dielectric constant of SiO_2. The objective is to obtain a thicker physical oxide layer with an equivalent electrical thickness.

Table 1. Dielectric constant, band gap, and band offsets for high-*k* dielectric materials (After [20]).

Material	Dieletric Constant (*K*)	Band Gap (eV)	CB Offset (eV)	VB Offset (eV)
SiO_2	3.9	8.9	3.5	4.4
Al_2O_3	9	8.7	2.8	4.9
HfO_2	25	1.5	1.5	3.4
ZrO_2	25	3.4	1.4	3.3

There are four key issues associated with oxides and the semiconductor-to-oxide interface that have been identified by the semiconductor industry [21]. The first one is the ability to continue scaling down to lower EOTs. The second one is the shift of threshold voltage. The third one is instabilities caused by the high concentration of defects in the oxide. Those latter two are related to the interaction between oxide layer and the channel. Since the oxide is in direct contact with the channel, the interface must be of high quality, in terms of surface roughness and the absence of interface defects. SiO_2 typically has a much lower defect density than high-*k* oxides. The fourth one is the loss of carriers' mobility when replacing by high-*k* dielectrics. Due

to the rougher interface and higher impurity concentration, it causes mobility degradation [22] between dielectrics and channel.

ii) **Ge MOS devices**

The limitation of channel mobility is a major bottleneck for future device scaling. Owing to its higher mobility of holes (×4) and electrons (×2) in bulk Ge than those in Si, it has been seriously considered for next generation technologies [23]. Ge has brought the microelectronics industry two Nobel prizes. Now Ge is on the research agenda again as a potential replacement for Si in high performance chips. Ge has a small hole effective mass, and hence can achieve high hole mobility in the inversion layer. This makes Ge a candidate channel material for p-MOSFETs. However, the challenges in realizing a full Ge CMOS technology are n-type dopant activation and passivation of interfaces.

The activation of n-type dopants of the source and drain regions in Ge is a major issue for high-performance nMOS with conventional transistor architectures. Dopants, such as As and P [23] [24] with active levels limited to $\sim 5 \times 10^{19}$ cm^{-3} and $\sim 2 \times 10^{19}$ cm^{-3}, are an order of magnitude lower than that required by normal nMOS. High P doping level can be very tricky during post-annealing, for the annealing of high doses results in out-diffusion. P dopants can diffuse deeper into the sample and precipitate at the peak concentration or cap oxide layer. However, this undesirable behavior will not result in an increase in activation.

Sb may be used for relatively low dose of n-type wafer manufacturing [25]. However, Sb implants into Ge at really high doses that are required by source/drain doping can bring in severe damage to the Ge surface [26]. Boron, as a primary p-type dopant for Ge, has been well studied for implantation and activation in Ge [27]. The key advantage of B as a dopant for Ge over Si is

that B is hardly diffusive in Ge over activation annealing temperature [25]. Thus, p-type doping is preferred in Ge MOS devices, and our work focuses on these devices.

The passivation of the surface is another issue for Ge MOS devices. For the fabrication of a Ge MOS device, it is difficult to obtain a stable oxide gate dielectric, since the native Ge oxide is soluble in water. As discussed above, high-*k* dielectrics have been widely used in high-performance devices. Ge MOS devices are also likely to require high-*k* dielectrics. The recent development of high quality techniques has propelled the development of Ge MOSFETs by implementing high-*k* dielectrics, improving interface stability. HfO_2 is a promising candidate for gate dielectrics, due to the thermal stability and relatively high dielectric constant value, as shown in Table 1. However, the Ge oxide-like interface underneath the HfO_2 can be very difficult to passivate. Ge can diffuse into interstitial and/or substitutional sites in the HfO_2 layer or form a Ge-O complex. All of those behaviors can generate electrically active levels in the HfO_2 layer, resulting in a poor-quality interface for the Ge/high-*k* gate stack.

To date, the most promising candidates for passivating interfacial layers are GeO_xN_y and thin Si layers [23]. GeO_xN_y has much better physical and chemical stability than other Ge oxides [28]. Nitrogen can penetrate into Ge oxide and reduce the potential inter-diffusion between the gate dielectric and gate electrode or substrate. Both physical and electrical properties of the interfacial layer and leakage have been greatly improved after processing in NH_3 (GeO_xN_y) before HfO_2 deposition [29].

Another way to improve the interface quality is to introduce a thin epi-Si layer on the Ge substrate before the HfO_2 deposition. The interface quality problem is then shifted from a Ge surface to a Si surface. A careful deposition of Si on Ge is required so that all the dangling Ge bonds are tied up by Si atoms, resulting in completely passivated Ge-Si interface. The control of

Si layer thickness must be precise to properly passivate the Si layer [30]. This thesis will focus on gate stacks of $Ge/SiO_x/HfO_2$.

2. Ge pMOSFET in this work

The devices studied in this work are Ge-on-Si substrate pMOSFETs with HfO_2 gate dielectrics. The substrates have been prepared by growing 2 μm expitaxial Ge films on Si substrates by reduced pressure chemical vapor deposition (RP-CVD). A SiO_2 layer is deposited on the Ge-on-Si substrates and patterned to define active areas. The sequence of gate stack formation starts with the thin epitaxial Si layer (Si monolayers), which is partially oxidized. The 4-8 Si monolayers in this work help with the surface passivation of the Ge surface. Above the Si monolayers (which are mostly consumed during the dielectric processing) is 4 nm of hafnium oxide, which is followed by 10 nm of tantalum nitride (TaN) and 70 nm of titanium nitride (TiN), deposited by physical vapor deposition (PVD). After the dry etch of the gate stack, a halo arsenic (As) implantation at 80 keV at varying doses (see Table 2) was performed. The p+ regions received an 11 keV BF_2 implantation at 8×10^{14} cm^{-2} and a highly doped drain (HDD) implant of 7.5 keV B to a dose of 4×10^{15} cm^{-2}, which was preceded by a Ge+ pre-amorphization implantation. This places the junction at a depth of ~80 nm below the surface. Doping activation was conducted at 550 ℃ at 5 minutes in a nitrogen ambient environment. Self-aligned nickel germanide (NiGe) was used for contacting the source, drain, and gate. The equivalent oxide thickness (EOT) value of the gate dielectric is 1.2 nm. A schematic diagram of the device is shown in Fig. 2.2. The TEM cross-section of a 65-nm gate length Ge p-MOSFET is shown in Fig. 2.3. The bonding arrangement of a germanium-gate oxide interface is shown in Fig. 2.4. The layout of the MOSFET is shown in Fig. 2.5.

Table 2. Number of Si monolayers, type of halo implantation, and pre-irradiation I_{on}/I_{off} ratio for devices used in this work. Device category D05, using an alternative deposition precursor Si_3H_8 at 350 ℃, showed a reduction in the pre-irradiation Ge/insulator interface trap density, as noted in [31].

D04	D05	D09	D10
500 ℃ SiH_4 5 Si Monolayers	350 ℃ Si_3H_8 5 Si Monolayers	500 ℃ SiH_4 8 Si Monolayers	500 ℃ SiH_4 8 Si Monolayers
As: 80 keV 5×10^{13} cm^{-2}	As: 80 keV 5×10^{13} cm^{-2}	As: 80 keV 3.5×10^{13} cm^{-2}	As: 80 keV 6.5×10^{13} cm^{-2}
Pre-rad I_{on}/I_{off} = 3100	Pre-rad I_{on}/I_{off} = 2600	Pre-rad I_{on}/I_{off} = 2100	Pre-rad I_{on}/I_{off} = 1100

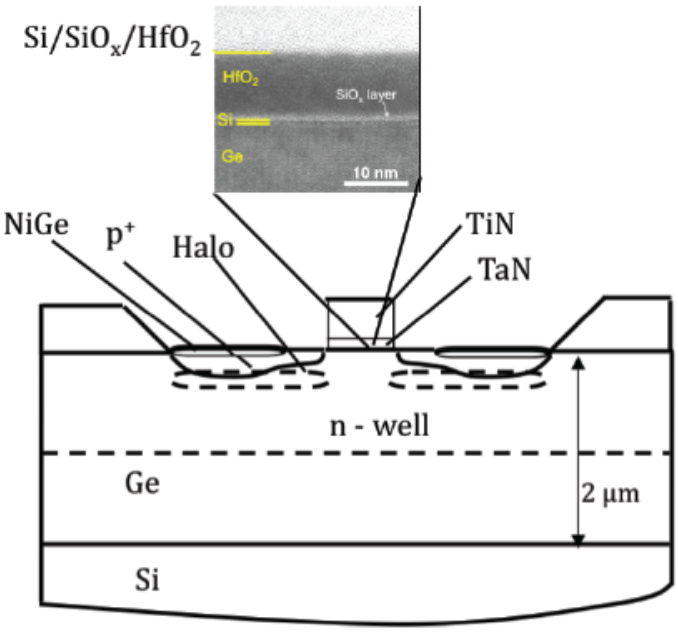


Fig. 2.2. Schematic cross-section of the p-channel Ge-substrate MOSFETs investigated in this work. After [32].

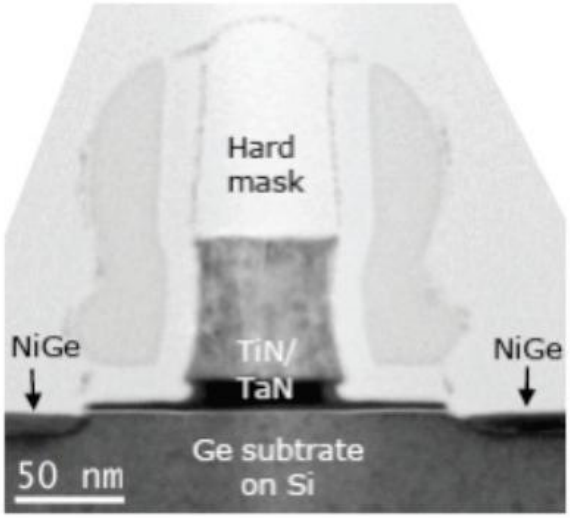


Fig. 2.3. TEM cross-section of a 65-nm gate length Ge p-MOSFET this work [33].

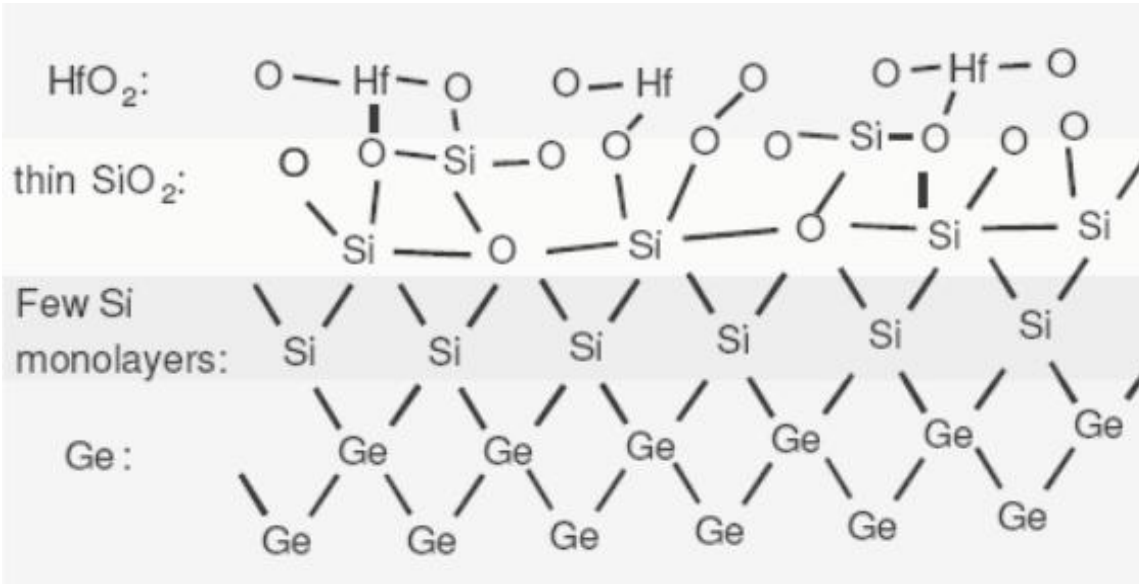


Fig. 2.4. The bonding arrangement at germanium-gate oxide interface. After [34].

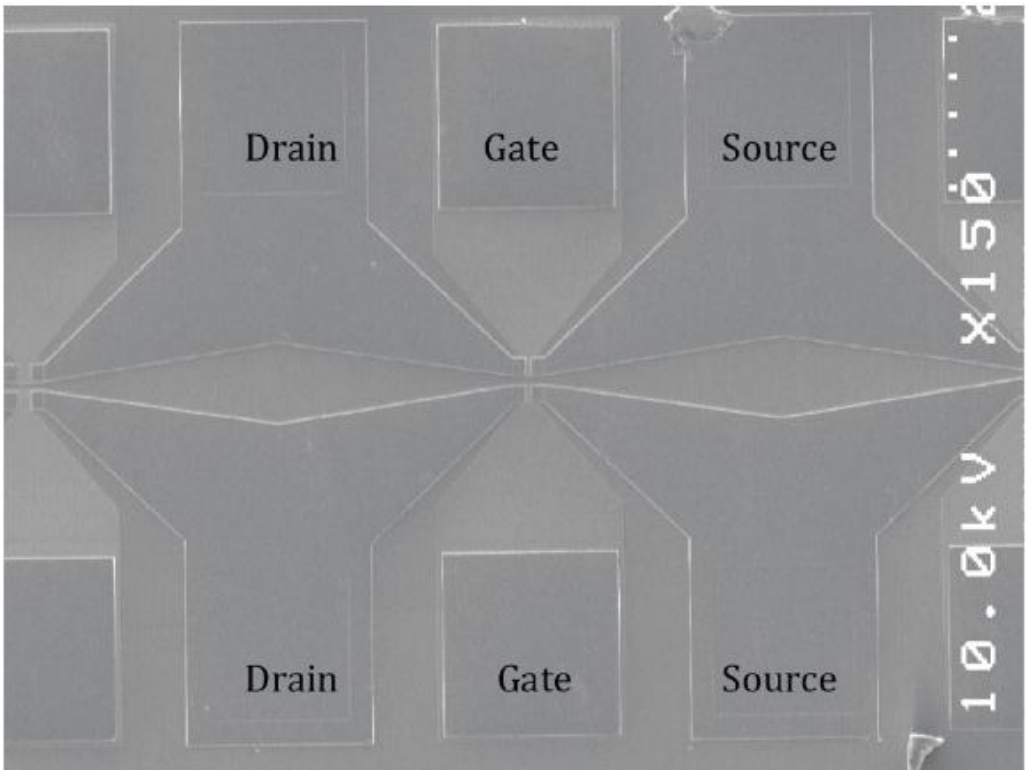


Fig. 2.5. SEM top view of the contact pads of a MOSFET. After [34].

3. Irradiation and Annealing Bias

All irradiations were performed at the wafer level with a 10-keV ARACOR x-ray source at a dose rate of 31.5 krad(SiO_2)/min at room temperature. Transmission gate bias was applied on these devices, with the drain and source biased at −1 V and the other terminals grounded during irradiation and annealing. This was found to be the worst case response for these devices, as will be discussed in Chapter III.

Device characterization was performed with a HP 4156A Semiconductor Parameter Analyzer. Current-voltage (I-V) characteristics and substrate current measurements are made in-situ. I_D-V_G and I_s-V_G were measured at a fixed V_D of −100 mV, and the gate leakage current was measured typically by sweeping V_G from 0 to −1 V with all the other terminals grounded. The four kinds of devices with different processing techniques (shown in Table 2) were measured to study their radiation response.

4. Low frequency noise measurements

Low frequency noise measurements also were performed at room temperature, before and after the devices were irradiated. For the low frequency noise measurements, the gate-to-threshold voltage difference, (V_g-V_t), was held at −0.8 V, and a constant drain voltage V_d of −100 mV was applied during the measurements. A schematic diagram for the *1/f* noise measurement is shown in Fig. 2.6 [14]. The biases are chosen to keep devices in the linear regime of operation, to simplify the measurement and the interpretation of the experimental results. The two voltages V_A and V_B were supplied by a HP 4140B constant voltage supply.

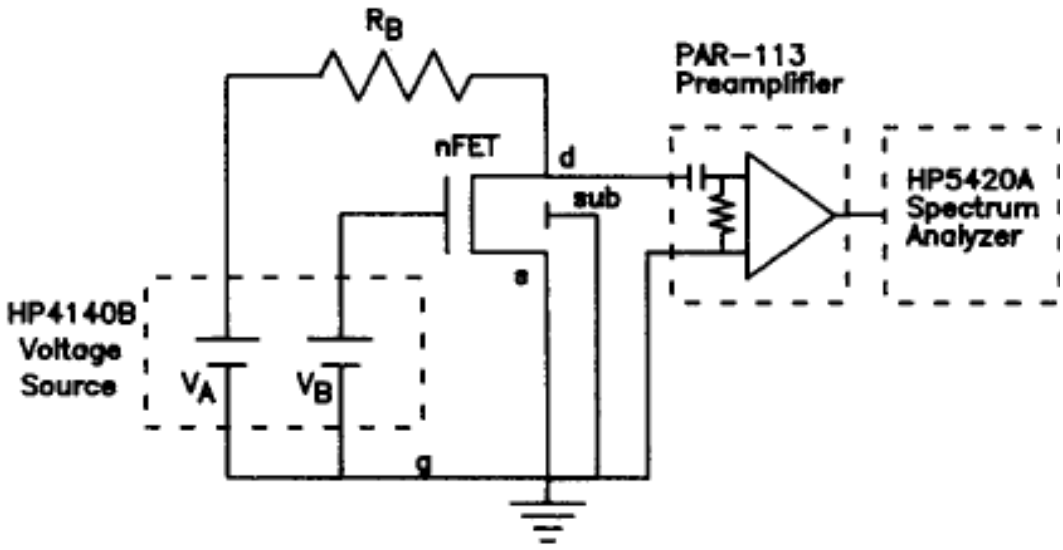


Fig. 2.6. Schematic diagram of *1/f*-noise measurement circuit. After [14].

CHAPTER III

TOTAL-DOSE EFFECTS ON JUNCTION LEAKAGE IN GERMANIUM P-MOSFETS

In this chapter, we examine the total dose irradiation and annealing response of Ge-pMOSFETs. We will consider four different devices with various numbers of Si monolayers and different doses of halo implantation. The experimental results of total ionizing dose (TID) and annealing response on p-channel enhancement mode MOSFETs fabricated on Ge-on-Si substrates with a TiN/TaN/HfO_2 gate stack are reported in this chapter.

Previous work by Arora et al. has investigated the radiation-induced drain-substrate leakage in Ge pMOS devices under positive gate bias exposure conditions [34]. A few reports on TID-induced degradation in ultra thin SiO_2/HfO_2-based Si MOSFETs are available, and radiation-induced shifts in the threshold voltage shift have been reported [31],[34]. However, the degradation that has been reported is relatively small. In Si technology, power consumption is dominated by subthreshold leakage and dynamic power consumption [35],[36], while the concern of power consumption is typically junction leakage in Ge technologies.

In this work, we evaluate the 10 keV x-ray irradiation response and annealing effects for Ge pMOSFETs as a function of device processing under transmission-gate operating conditions, which we find to be worst case for these devices. The halo implantation conditions and the number of Si monolayers at the interface can strongly affect the radiation-induced leakage. Both band-to-band tunneling and trap-assisted tunneling contribute to the observed leakage. Device

leakage before and after irradiation is found to be sensitive to halo implant dose and the number of Si monolayers at the Ge/insulator interface. Interface trap densities and body leakage also increase with dose and decrease with annealing.

1. Experimental results and discussion

Fig. 3.1 shows the drain current I_D as a function of gate voltage V_G as a function of total ionizing dose under transmission gate bias conditions, which are worst case for these devices, as we show below. The threshold voltage shifts negatively and the subthreshold slope stretches out with increasing dose, consistent with the buildup of radiation-induced oxide and interface trap charge in the gate oxide. The off-state leakage current increases and the on-state current decreases significantly, thereby reducing the on-off current ratio [32],[37],[38].

In Fig. 3.2, the drain current I_D is shown as a function of gate voltage V_G for varying annealing times. All the annealing experiments and measurements were performed at room temperature in-situ. The threshold voltage was at −0.18 V, which did not change much with total dose. However, the pre-irradiation value of off-state current was 4.8×10^{-7} A, and after 1 Mrad/(SiO_2) irradiation, the off-state current rises up to 1.3×10^{-6} A. It then decreases to 7.9×10^{-7} A after 16 hours of room temperature annealing. These high levels of leakage currents are typical for Ge devices with thin oxides [31],[36],[39].

Fig. 3.3 shows that transmission-gate bias [40] produces the largest radiation-induced changes in the ratio of the on-state current to the off-state current (I_{on}/I_{off}). The electric field at the source and drain and the built-in electric field that results from oxide and interface-trap charge buildup in these pMOS devices can affect the halo implantation region under both the source and drain significantly. This leads to enhanced leakage current in these devices, and a

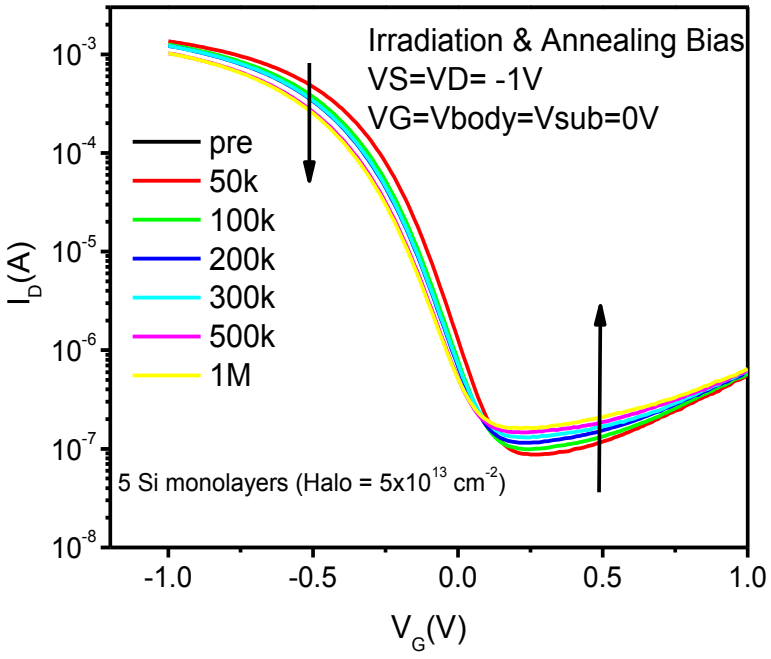


Fig. 3.1. Drain current ID as a function of gate voltage VG with varying total dose.

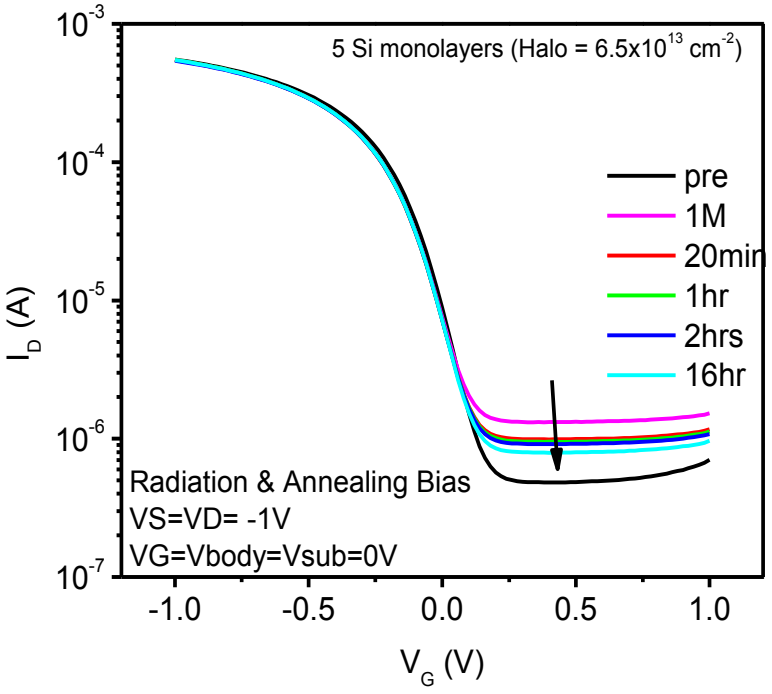


Fig. 3.2. Drain current I_D as a function of gate voltage V_G with varying annealing time.

correspondingly reduced I_{on}/I_{off}, as compared to previous work on similar devices performed under positive gate bias [32],[38]. Hence, for the remainder of the irradiation and annealing performed in this work, the drain and the source are biased at −1V and the gate and substrate are grounded.

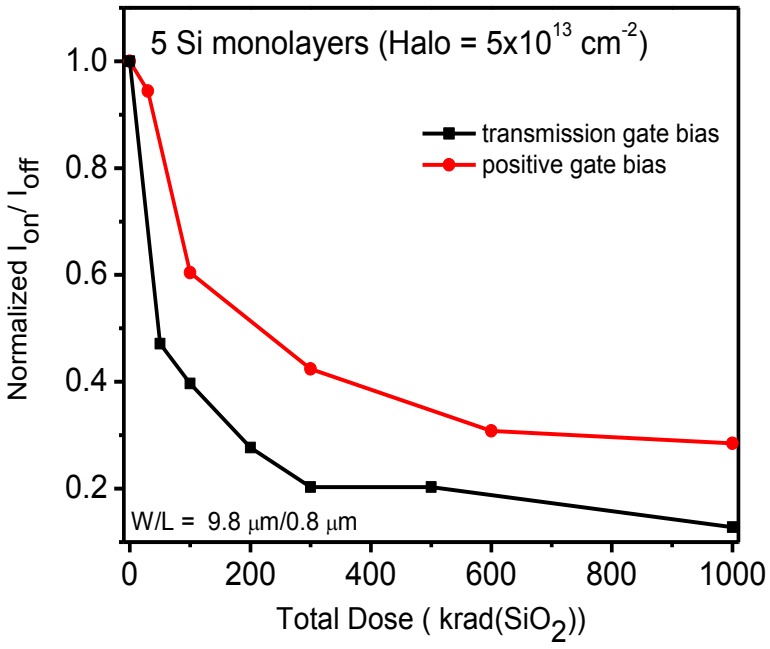


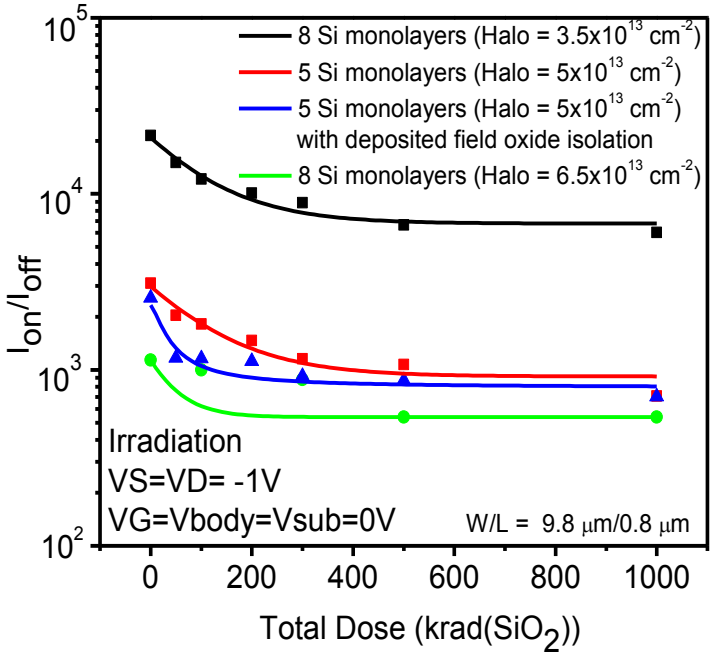
Fig. 3.3. I_{on}/I_{off}, normalized to its pre-irradiation value, as a function of total dose and radiation bias. Here we use a linear scale to highlight the differences in I_{on}/I_{off}.

Fig. 3.4 shows the I_{on}/I_{off} ratio as a function of processing for devices with W/L = 9.8 μm/0.8 μm after (a) total dose irradiation and (b) isothermal annealing. The on/off current ratio decreases with increasing total dose. This reduction in on/off current ratio is due primarily to an increase in drain-substrate junction leakage current. The increase in the off-state current is related to leakage current between the reverse-biased drain and the substrate. The electric-field-

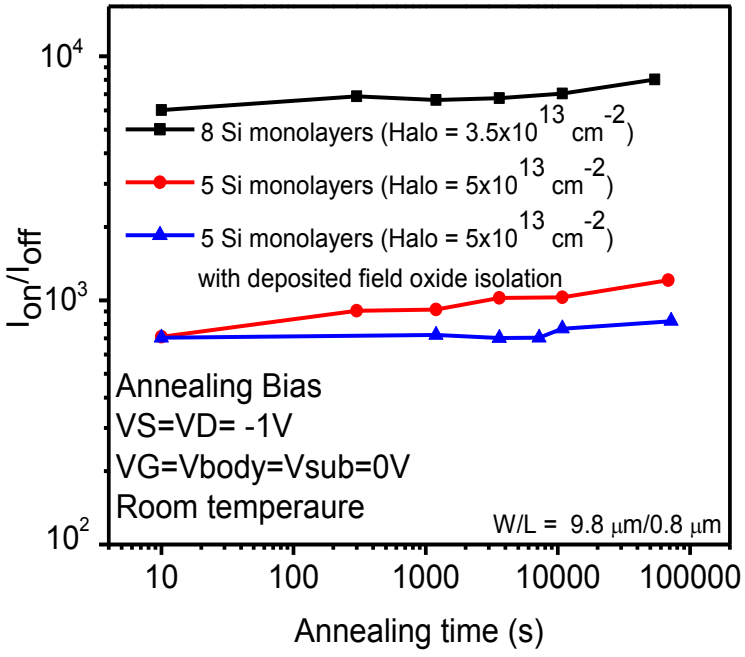
enhanced defect buildup during irradiation under transmission-gate bias enhances the reverse leakage current of a p-n junction so that the post-irradiation level is increased over pre-irradiation levels.

The on-state current decreases because of mobility degradation, and the off-state current increases as a result of the increase in radiation-induced leakage. D05 with five Si monolayers, processed with a different epitaxial Si precursor, exhibits a smaller I_{on}/I_{off} ratio than D04, showing the strong dependence of the I_{on}/I_{off} ratio on processing details. Higher halo implantation dose can also lead to a lower I_{on}/I_{off} ratio. Eight Si-monolayer devices with lower halo doping show the highest on/off current ratio of all the devices. The high threading dislocation density in devices with a high dose halo implant leads to the possibility of defect-assisted leakage before irradiation [41], and this trend continues throughout the irradiation process.

During the fabrication of the devices, the Si monolayers added onto the Ge can be converted to an interfacial oxide layer, which helps the passivation of the Ge to SiO_2 interface [33], [42]. This work shows that this conversion of Si monolayers to oxide can lead to enhanced defect buildup after the device is irradiated. In Fig. 4(b), the on/off ratio increases slightly with annealing time, during room temperature annealing.



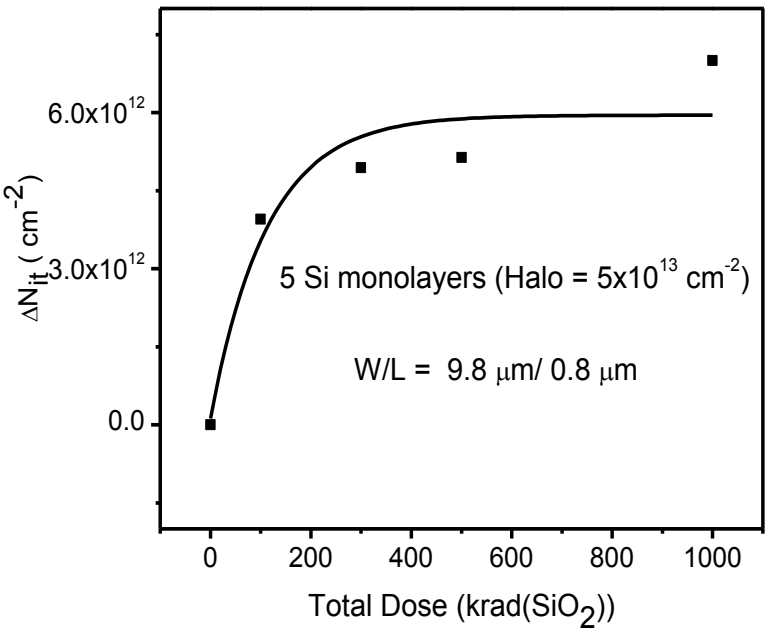
(a)



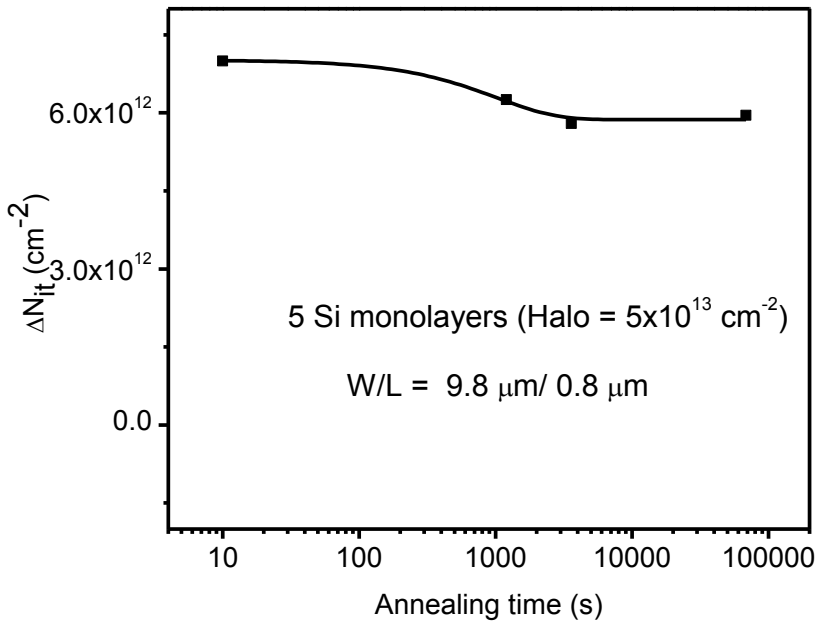
(b)

Fig. 3.4. I_{on}/I_{off} characterization as a function of total dose and annealing time for the devices with varying process conditions; all devices have W/L = 9.8 μm/0.8 μm.

Fig. 3.5 shows the change in interface trap density ΔN_{it} as a function of (a) total dose irradiation and (b) isothermal annealing for a Ge pMOSFET with width/length ratio W/L = 9.8 μm/0.8 μm, extracted from the results of I_D-V_G characterization. Fig. 3.5(a) shows the relatively high interface-trap densities after irradiation in these devices, compared to the pre-irradiation value of interface trap densities which is below 10^{11} cm^{-2} [30],[31],[43]. Fig. 3.5(b) shows that a significant fraction of the interface traps anneals out with time at room temperature. This recovery may be associated with the passivation of interface traps by hydrogen.



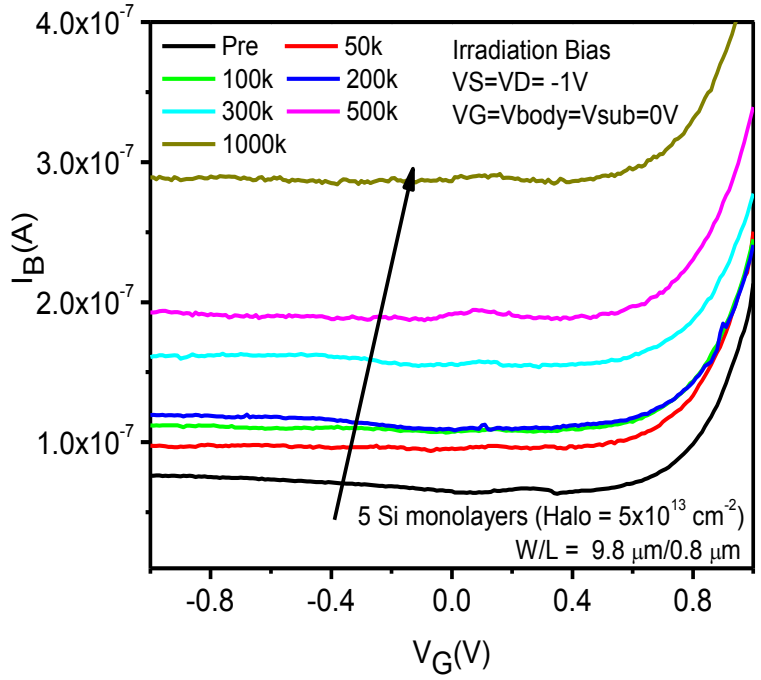
(a)



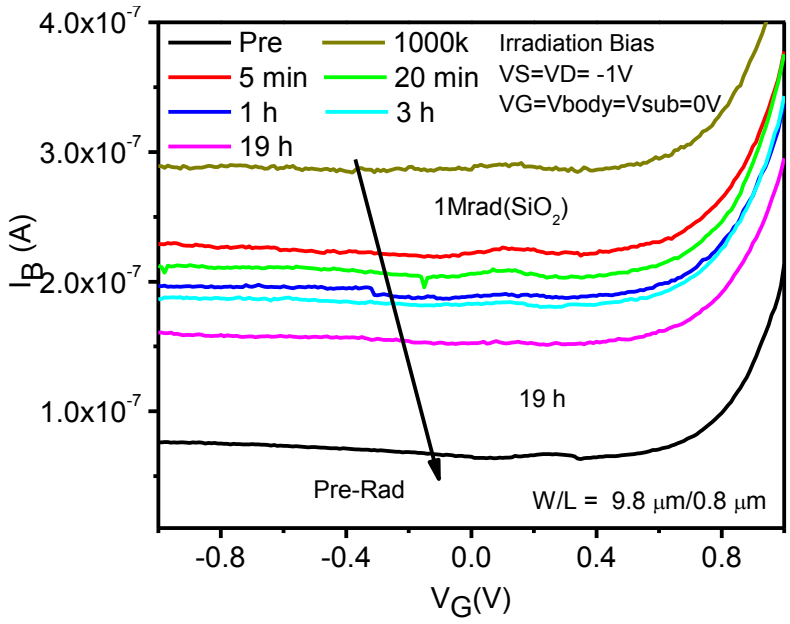
(b)

Fig. 3.5. ΔN_{it} as a function of (a) total dose and (b) room-temperature annealing time for a Ge pMOS device with W/L = 9.8 μm/0.8 μm. The lines are guides to the eye.

Figs. 3.6(a) and (b) show the body current leakage I_B as a function of gate voltage V_G for irradiation and annealing of these devices. The body current is the excess junction leakage that flows between the p-n junction formed by the drain and the substrate/body. The body leakage increases with total dose irradiation, consistent with the increase in the drain to source (channel) leakage. This body leakage is similar to that observed by Caussanel et al. in Si devices [44], and attributed to the buildup of interface traps at the perimeter of the drain junction. After irradiation, the body leakage decreases significantly with annealing time, consistent with the reduction of oxide and interface trap densities.



(a)



(b)

Fig. 3.6. Body current leakage I_B as a function of gate voltage V_G (a) as a function of irradiation and (b) as a function of isothermal annealing time at room temperature.

2. Junction Leakage

Several factors contribute to the radiation-induced increase in junction leakage. The small band gap (0.66 eV) for Ge leads to efficient band-to-band tunneling (BTBT) [45], especially when a high electric field is applied at the drain/source region, as is the case under transmission gate bias. Less BTBT will be observed for on-gate bias conditions. This may enhance the buildup of interface and oxide trap charge during the irradiations under transmission gate bias. Trap-assisted-tunneling (TAT) may also lead to enhanced junction leakage, since the introduction of radiation-induced trapped charge can increase the efficiency with which carriers can tunnel through these ultrathin oxides [46],[47]. Threading dislocations may also play a significant role in the pre-irradiation leakage [48].

Fig. 3.7 shows that total junction leakage current can be decoupled into three components: the areal leakage current J_A, the extension leakage J_E, and the isolation leakage J_I. The areal leakage J_A is generated under the area of highly doped implantation, which depends strongly on the area of the drain region. The extension leakage J_E is generated under the active region of the transistor, and depends on the transistor width W. The isolation leakage J_I is generated at the interface between the isolation region and drain area. The isolation region is formed by deposited SiO_2 wherein active windows are etched. The drain current I_D can be expressed as [37]:

$$I_D = J_A \times A + J_E \times W + J_I \times L_I \tag{2}$$

where A is the area of the drain region, W is the width of the transistor, and L_I is the active-area-to-isolation length.

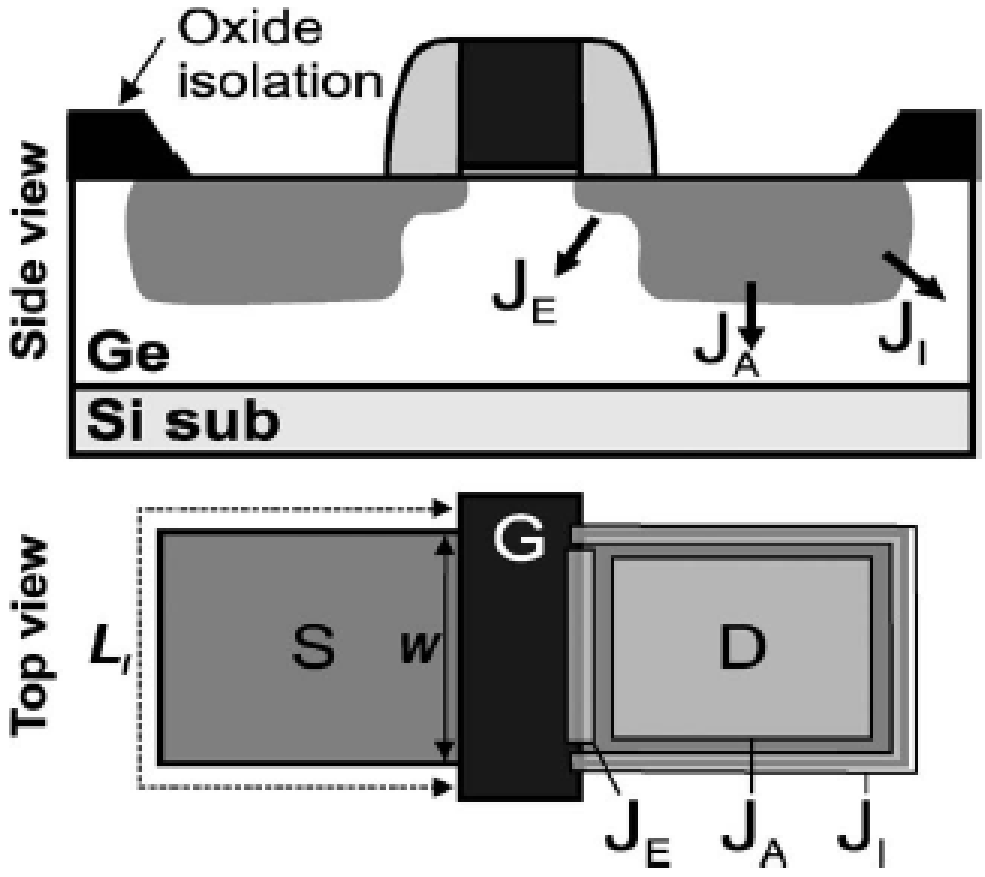


Fig. 3.7. Schematic cross section and top view of a bulk Ge-pMOS transistor, indicating the extension leakage J_E, the areal leakage J_A, and the isolation leakage J_I. After [37].

The areal leakage has been intensively studied in Ge p+/n junctions, as processed [41]. It is strongly related to the size of the device and halo implants. A careful choice of halo implants is needed, since a low doping level will increase the diffusion current and a high doping level will increase electric-field generated TAT and BTBT. A reduction from 1×10^{10} cm^{-2} to about 4 $\times10^{8}$ cm^{-2} of threading dislocation density is reported for smaller areal junction leakage by annealing at 800 or 900 ℃ in [49], again emphasizing the need to control the defect densities before irradiation. Our work demonstrates that the post-irradiation junction leakage is quite

sensitive to similar factors, with an increase in leakage caused by radiation-induced interface traps and oxide-trap charge. In lower dose rate environments, annealing effects will reduce this leakage somewhat, but it remains a significant issue to address in Ge pMOS devices. The devices that show the lowest leakage in this work may be quite suitable for application in the space radiation environment.

3. Summary of Chapter, and Conclusions

We find that the worst-case leakage in irradiated Ge pMOS devices occurs under transmission gate bias conditions. The on-off current ratio decreases with total dose and increases slightly with annealing time for all sets of devices fabricated with different processing techniques. The on-state current decreases as a result of mobility degradation, and the off-state current increases as a result of radiation-induced leakage. The device with a greater number of Si monolayers and lowest density of halo implantation displays the greatest on-off current ratio both before and after irradiation, for these devices. Band-to-band tunneling, trap-assisted tunneling, and threading dislocations all can contribute to the leakage currents observed in these devices. While the presence of Si monolayers on Ge can help passivate the interface, the presence of too many Si layers can lead to increased radiation-induced interface trap buildup. These results show that Ge pMOS devices have significant promise for future space applications.

CHAPTER IV

EFFECTS OF IONIZING RADIATION ON DEFECTS AND 1/*f*-NOISE IN Ge pMOSFETS

As discussed above, stable oxides for Ge MOS devices can now be obtained via a gate stack that includes high-*k* gate dielectrics [30],[50],[51]. The interface control of these Ge pMOS devices has been successfully achieved by Si monolayer passivation and HfO_2 gate dielectric deposition [30]. Recent work has shown that the 1/*f* noise of Ge pMOS devices is associated with carrier trapping in the passivation layers [52]; however, the nature of the defects is not well known, and the noise of irradiated devices has not yet been reported.

In this chapter, we evaluate the threshold voltage shifts for devices with differing halo implantation conditions and numbers of Si monolayers. Devices were exposed to 10 keV x-rays and annealed under transmission gate bias, which is the worst case irradiation bias for these devices [53]. The noise decreases more rapidly during annealing than either the oxide or interface trap charge, in contrast to pMOS annealing results on older generation Si technologies. These results provide insight into defects in Ge pMOS transistors with SiO_2/HfO_2 gate dielectrics.

1. Experimental Details

The devices used in this work are described in chapter II. All irradiations were performed at the wafer level with a 10-keV ARACOR x-ray source at a dose rate of 31.5 krad(SiO_2)/min at

room temperature. Transmission gate bias (worst case for radiation response [53]) was applied to these devices, with the drain and source biased at −1 V and the other terminals grounded during irradiation and annealing. Low frequency noise measurements also were performed at room temperature, before and after the devices were irradiated. For the low frequency noise measurements, the gate-to-threshold voltage difference, $V_g - V_t$, was held at −0.8 V, and a constant drain-source voltage V_{ds} of −100 mV was applied during the noise measurements. Several devices of each process type were measured; the results shown here are representative of the responses of each split.

2. Experimental Results and Analysis

A. Current-Voltage Measurements

Fig. 4.1 shows the drain current I_D as a function of gate voltage V_G for Ge pMOS transistors irradiated to 1.0 Mrad(SiO_2) under transmission gate bias conditions. The junction leakage increases with dose, which leads to a decrease in the I_{on}/I_{off} ratio. The threshold voltage shifts negatively and the subthreshold slope stretches out with increasing total ionizing dose, consistent with the buildup of radiation-induced oxide and interface trap charge in the gate oxide, as shown later. Due to the high-*k* dielectric, the dose delivered to the dielectric stack for these devices (and other high-*k* devices in the literature) likely is ~3 times the quoted equilibrium SiO_2 dose [11],[54].

Fig. 4.2 shows the inferred threshold-voltage shift produced by (a) oxide trap charge ΔV_{ot} and (b) interface trap charge ΔV_{it}, extracted from I-V characteristics, as a function of total dose, estimated via the charge separation technique of Winokur, et al. [55]. The limited range of subthreshold current (only ~ one decade) before the leakage floor introduces uncertainty into

these estimates, as is inevitably the case for devices with ultrathin oxides, owing to the need to extrapolate to the midgap current and subtract off the leakage current to obtain estimates of ΔV_{ot} and ΔV_{it} [55],[56]. The inferred value of ΔV_{ot} in Fig. 4.2(a) is −0.23 V at 1 Mrad(SiO_2) for the two splits showing the greatest oxide-trap charge. Assuming that this charge is distributed approximately uniformly in these thin, high-*k* gate dielectrics [2],[11], a shift in ΔV_{ot} of −0.23 V at 1 Mrad(SiO_2) corresponds to an effective density of oxide trap charge of ~8×10^{12}/cm^2. (Assuming a uniform distribution of charge is equivalent to reducing the moment arm of the trapped charge by a factor of two. This doubles the inferred charge density relative to the value obtained from a standard projection to the interface [2],[57]). The magnitudes of the values of ΔV_{it} in Fig. 3(b) are less than 80 mV for all doses and process splits considered; an 80 mV shift in ΔV_{it} corresponds to an effective interface-trap density of ~1.4×10^{12}/cm^2. (This estimate assumes that the traps are located at the interface.) For pMOSFETs, both interface and oxide trap charge will reduce operating speeds and decrease noise margins of circuits using these devices Compared to previous work on Si [11] for the same EOT range (1.2 nm-1.5 nm) for HfO_2-based MOSFETs, the charge trapping in Ge devices is larger, but the shifts are small enough for reliable device operation in most typical radiation environments. The dominant contribution to the threshold shift is oxide trap charge, with less contribution from interface trap charge [11]. In this device, interface traps likely are in the Si layer [44] that has been used to passivate the Ge-SiO_2 surface [30].

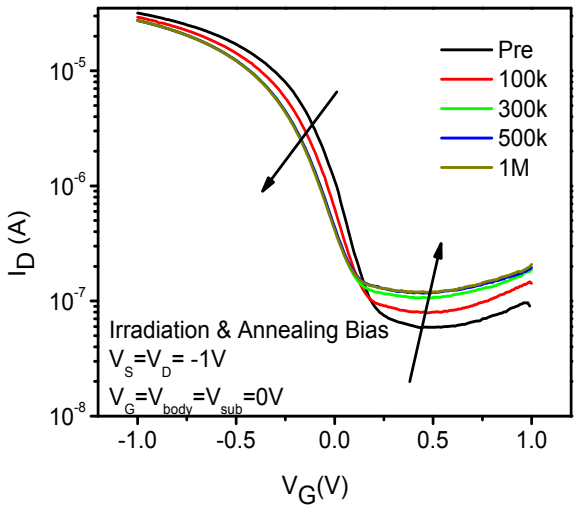
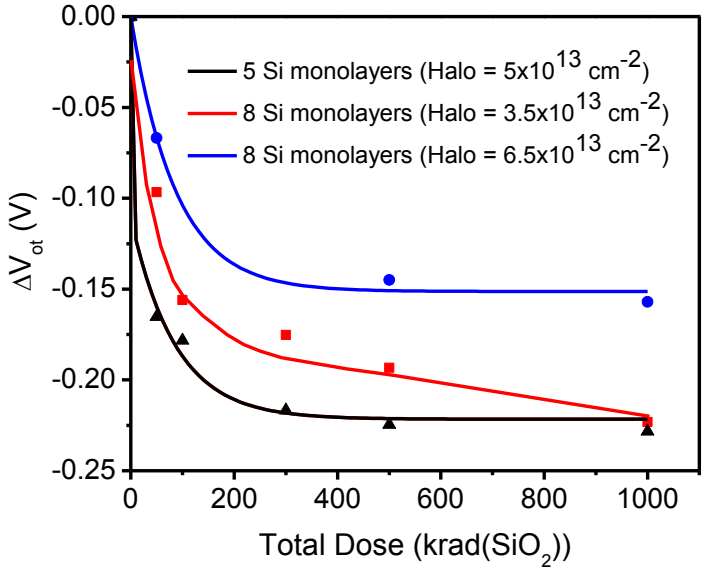


Fig. 4.1. Drain current I_D as a function of gate voltage V_G and total ionizing dose for device split D10, with W/L = 9.8 µm/10 µm.



(a)

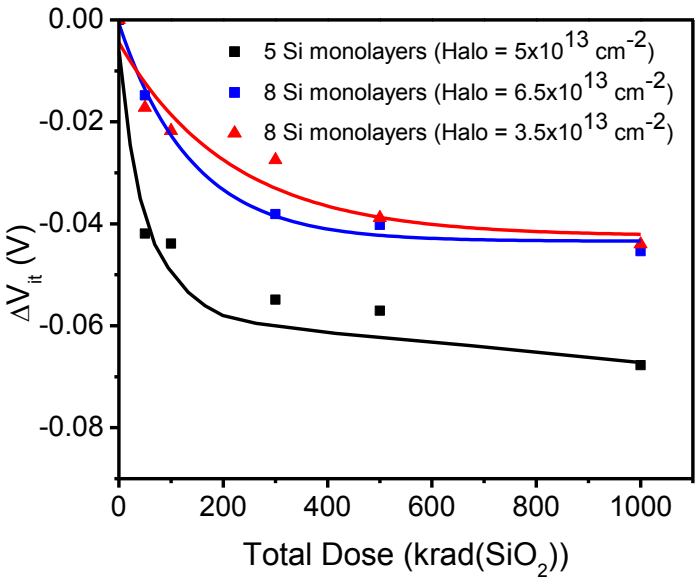


Fig. 4.2. Threshold voltage shifts due to (a) oxide trap charge ΔV_{ot} and (b) interface trap charge ΔV_{it} as a function of total dose irradiation for device splits D04, D09, and D10. Irradiations were performed at room temperature under transmission gate bias.

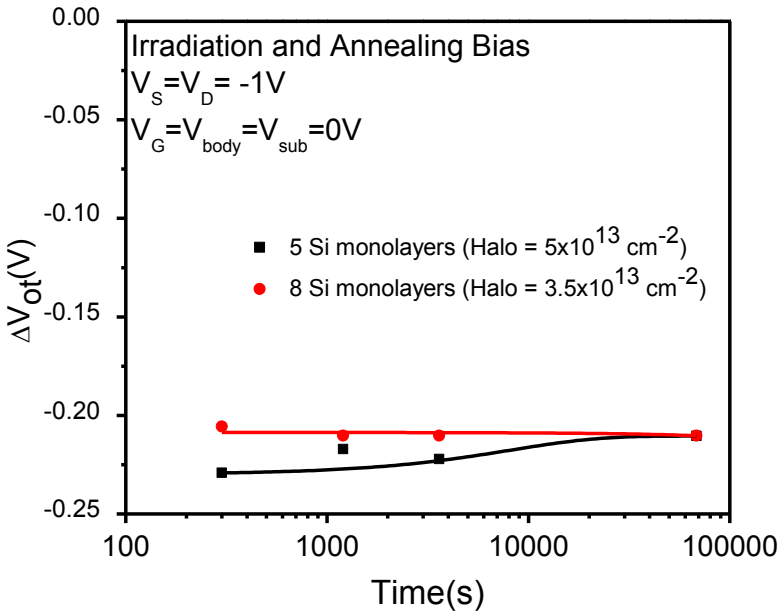
Fig. 4.3 shows (a) ΔV_{ot} and (b) ΔV_{it} for the splits D04 and D09 as a function of post-irradiation annealing time at room temperature. Compared to Fig. 4.2, some annealing of oxide-trap charge and interface traps is observed, especially for the process splits showing the largest densities of radiation-induced charge trapping. The trapped-hole annealing is attributed to the neutralization of oxide-trap charge via electron tunneling [12], and the annealing of the interface traps may be caused by hydrogen passivation, which can occur efficiently in devices with high densities of interface traps [44],[53],[58],[59].

Device split D04 with 5 Si monolayers exhibits increased buildup of both oxide traps and interface traps in Figs. 4. 3 and 4, compared to splits D09 and D10 with 8 Si monolayers. This increase in radiation-induced charge trapping may be associated with stress induced defects at the Si-Ge interface, and/or the enhanced contributions of the high-*k* portion of the gate stack to

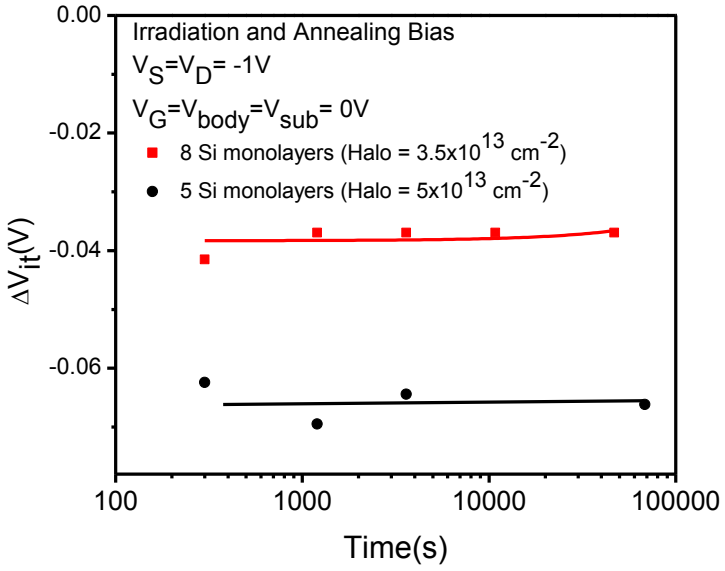
the radiation-induced charge trapping. A Si layer that is too thick will relax and create more lattice mismatch defects at the dielectric-to-semiconductor interface; a Si layer that is too thin will be over-oxidized and lead to the formation of a lower quality mixed Si/Ge oxide at the interface [60]. These tradeoffs must be considered carefully in process development.

B. Low-Frequency Noise

In Figs. 4.4(a)-(c), the excess low frequency noise power spectral density S_{Vd} is shown as a function of irradiation dose and room temperature annealing time for process splits D04, D09, and D10. The spikes in the spectra are from 60-Hz pickup and harmonics, and are ignored in the data analysis. The noise measurement circuit is similar to that described in [61].

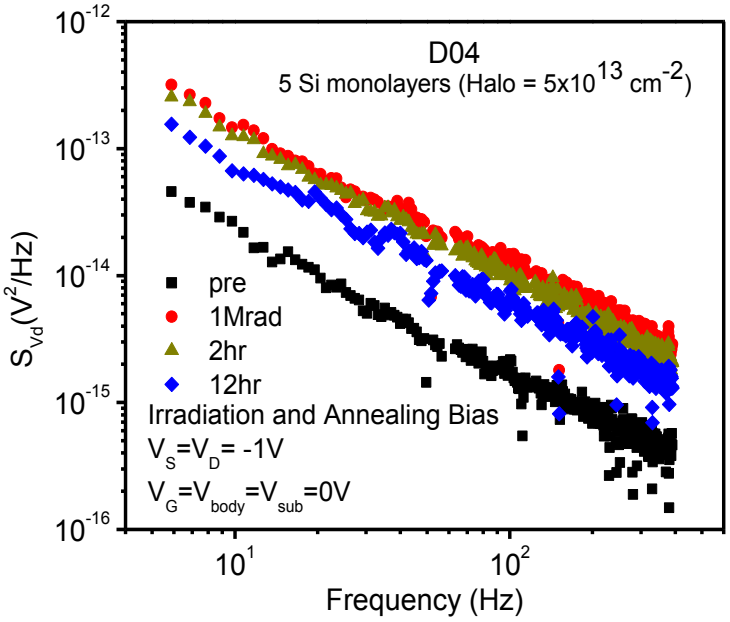


(a)

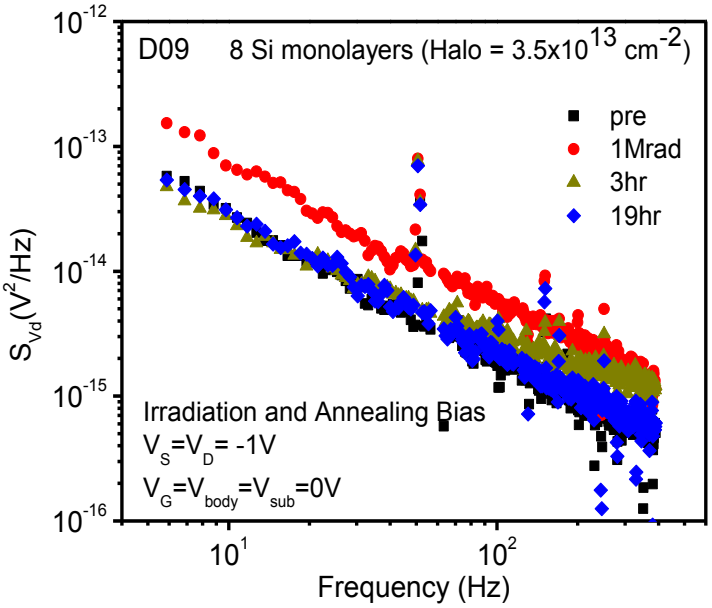


(b)

Fig. 4.3. Threshold voltage shifts due to (a) oxide trap charge ΔV_{ot} and (b) interface trap charge ΔV_{it} as a function of room-temperature annealing time after the total dose irradiation (Fig. 4.2) for process splits D04 and D09. The annealing was performed under transmission gate bias.



(a)



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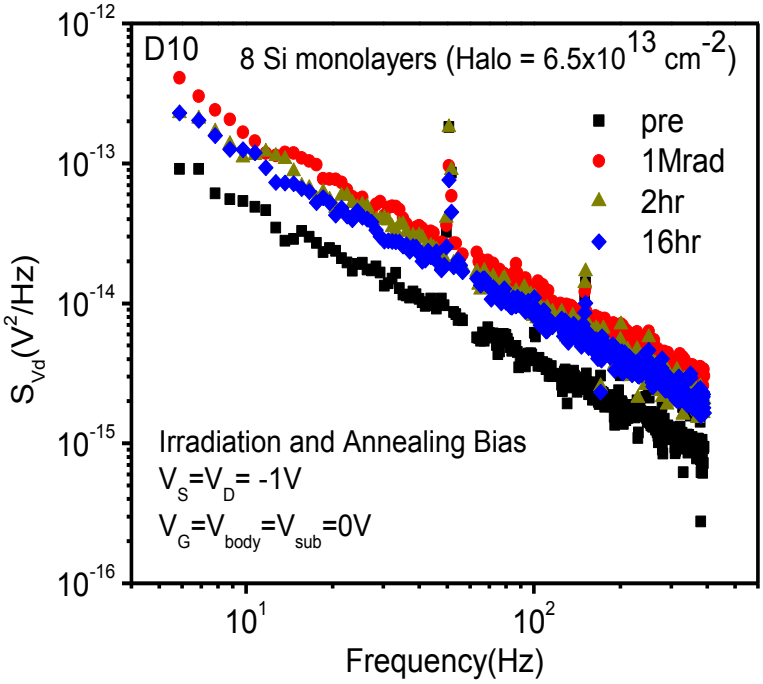

(c)

Fig. 4.4. Excess drain-voltage noise power spectral density S_{Vd} as a function of frequency for splits (a) D04, (b) D09, and (c) D10.

For all splits in Fig. 4.4, the noise increases after irradiation and decreases with room temperature annealing. The rate of the decrease in noise magnitude during post-irradiation annealing is much faster in these Ge pMOS devices than in much of the previous work on the effects of irradiation and annealing on Si pMOS devices with thicker SiO_2 gate dielectrics [13],[62]. Indeed, the noise of irradiated Si pMOS devices often increases with annealing with positive bias on the gate [13],[62], which is certainly not the case here, even with a similar electric field in the sensitive region, under transmission gate bias conditions [53].

It has been shown previously that the pre-irradiation noise of similar devices can be described to first order by a simple number fluctuation model [52],[63]-[65]. Fig. 4.6 shows the effective border-trap density inferred from the noise measurements of Fig. 4.5 as a function of total ionizing dose and annealing time. Consistent with previous work, we assume that the change in effective density of border traps after irradiation can be estimated by the same number fluctuation model of the noise [13],[6],[64]-[70]. In this model, the effective border-trap density N_{bt} can be estimated via the following expressions,

$$S_V = K \cdot f^{-\alpha} \cdot \frac{(Vd)^2}{(Vg-Vt)^2} \tag{1}$$

$$N_{bt} \approx E_g L W (\varepsilon_{ox}/t_{ox})^2 ln(\tau_1/\tau_2) K (qkT)^{-1} \tag{3}$$

where t_{ox} is the EOT (~1.2 nm), ε_{ox} is the SiO_2 dielectric constant (3.45×10^{-13} F/cm); E_g is the Ge band gap (0.66 eV), the width W = 9.8 μm and length L = 10 μm for these devices, q is the electronic charge, k is the Boltzmann constant, and T is the temperature (~295 K). We estimate the "cutoff" times for the noise processes to be $\tau_1/\tau_2 \approx 10^{12}$, consistent with previous work [6],[13],[66],[67],[69].

In Fig. 4.5, the effective border trap densities for the three process splits are ~2-6 $\times 10^{12}$ cm^{-2} before the devices are irradiated, which is consistent with many previous results for devices

with high-k gate dielectrics [52],[63]-[65],[71]-[73]. After irradiation, the effective border trap densities increase significantly for all splits, and decrease with post-irradiation annealing. Comparing the results from the different process splits, split D04 with five Si monolayers exhibits a larger increase in N_{bt} with irradiation than split D09 with eight Si monolayers. This result is consistent with the trends in ΔV_{ot} and ΔV_{it} shown previously in Fig. 4.4, suggesting that the increase in noise is associated with increases in radiation-induced trapped charge. Moreover, split D10 with a halo implant dose of 6.5×10^{13} cm^{-2} exhibits more than a 50% greater increase in noise at 1.0 Mrad(SiO_2) than D09, which received a halo implant dose of 3.5×10^{13} cm^{-2}. The annealing of the noise after irradiation is also more effective for split D09 than split D10. This emphasizes the improvement in the interfacial properties of the devices that received the lower halo implant dose, which show reduced leakage after irradiation [53], decreased interface trap buildup (Fig. 4.2b), and reduced low-frequency noise after irradiation. We note that previous workers have also noted a strong association of low-frequency noise with halo implantation dose [41],[74],[75], emphasizing the need to control these process conditions carefully.

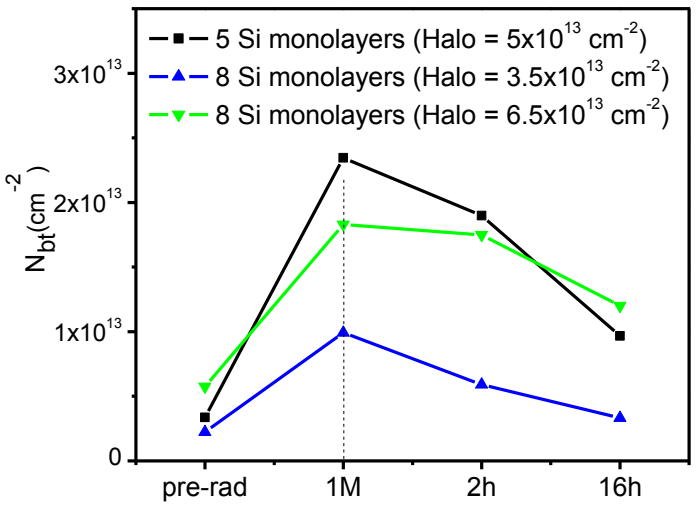

Fig. 4.5. Effective densities of border traps N_{bt} as a function of total ionizing dose and annealing time for splits D04, D09 and D10.

The effective border-trap density for split D09 is ~2 × 10^{12} cm^{-2} before irradiation, and ~10^{13} cm^{-2} after the device is irradiated to 1.0 Mrad(SiO_2). Hence, the change in N_{bt} with irradiation for this split is similar to the inferred value of ΔN_{ot} in Fig. 3 at 1.0 Mrad(SiO_2), ~8 × 10^{12} cm^{-2}. However, this excellent agreement may well be fortuitous; for the other two splits, the changes in effective border-trap densities after irradiation in Fig. 4.6 are up to a factor of ~3 larger than the values of ΔN_{ot} inferred from Fig. 4.2. The large effective border trap densities in these cases raise the possibility that other sources of noise are contributing to the fluctuations observed in these devices, as compared to split 09.

We note that it has been demonstrated that, in cases where defect reconfiguration can occur readily upon charge capture, defects over a wider range of energies can contribute to the low-frequency noise than the typical range of a few *kT*. This has discussed in detail by Zhou et al. for much thicker (field) oxides on Si in [69]. Candidates for these defects in Ge pMOS devices include (1) stretched Si-Si bonds [76]-[78] in the near-interfacial SiO_2 layer, (2) hydrogenated O vacancies in the near-interfacial SiO_2 [79] and HfO_2 [80] layers, and/or (3) O vacancy related defects in the HfO_2 layer [82]. All of these defects have multiple energy levels, which can be sensitive to the structural changes that inevitably occur upon charge capture and emission [69],[76]-[81]. For example, when carriers are metastably trapped at an O vacancy defect, the change in Si-Si bond length during capture and emission can change trap energy levels and contribute to the observed noise [76]. These defects may contribute not only to the increased low-frequency noise in these devices, but also to radiation-induced leakage in these Ge pMOS devices [53] and Si MOS devices [82] as well.

3. Summary of Chapter, and Conclusions

We have found that the threshold voltage shifts and the degradation of low frequency noise in Ge pMOS devices are small enough for reliable device operation in many typical radiation environments. The most significant contribution to the threshold voltage shift is oxide trap charge in this case. Low frequency noise in irradiated Ge pMOS devices anneals more quickly and completely than the corresponding noise observed in many irradiated Si pMOS devices. The change of trap density in gate stacks is well correlated to the low frequency noise performance. The radiation-induced oxide trap charge and the low-frequency noise after irradiation are higher for devices with five Si monolayers than for devices with eight Si monolayers. An increase in halo implant dose is found to lead to increased device leakage, enhanced interface-trap buildup, and greater $1/f$ noise in irradiated devices. These results show that low-frequency noise measurements can be a sensitive probe of defects in irradiated Ge pMOS devices.

CHAPTER V

SUMMARY AND CONCLUSION

The 10-keV x-ray radiation response of Ge-pMOSFETs is reported in this thesis. The on-off current ratio decreases with total dose and increases slightly with annealing time for all sets of devices fabricated with different processing techniques. The on-state current decreases because of mobility degradation, and off-state current increases as a result of the increase in radiation-induced leakage. The device with a greater number of Si monolayers and lowest density of halo implantation displays the greatest on-off current ratio both before and after irradiation, for these devices. The worst-case leakage in the irradiated devices occurs under transmission gate bias conditions. The reason is that the transmission gate bias affects the halo implantation region significantly under both of the source and drain significantly, leading to the enhanced leakage current in these devices.

An analysis of junction leakage suggests that extension leakage J_E dominates in the leakage currents. Area leakage J_A and isolation leakage J_I play a role in the junction leakage too. Band-to-band tunneling, trap-assisted tunneling, and threading dislocations all can contribute to the leakage currents observed in these devices. While the presence of Si monolayers on Ge can help passivate the interface, the presence of too many Si layers can lead to increased radiation-induced interface trap buildup. Our work demonstrates that the post-irradiation junction leakage is quite sensitive with an increase in leakage caused by radiation-induced interface and oxide-trap charge. Body leakage is observed to build up during irradiation, and decrease during room

temperature annealing, similar to drain current. The performance of the best of these Ge pMOS devices appears to be very promising for space applications.

Beside junction leakage, we have evaluated the threshold voltage shifts and the degradation of low frequency noise. All of them increase with total dose and decrease with annealing time. The most significant contribution to the threshold voltage shift is oxide trap charge in this case. Low frequency noise in irradiated Ge pMOS devices anneals more quickly and completely than the corresponding noise observed in many irradiated Si pMOS devices.

The change of trap density in gate stacks is well correlated to the low frequency noise performance. The radiation-induced oxide trap charge and the low-frequency noise after irradiation are higher for devices with five Si monolayers than for devices with eight Si monolayers. These results show that trap densities in Ge pMOS devices with HfO_2 oxides can be quite sensitive to the number of Si monolayers at the interface of the Ge wafer. Given the noise behavior between devices of different processing techniques, good control of Si monolayers is necessary for the degradation of devices. An increase in halo implant dose is found to lead to increased device leakage, enhanced interface-trap buildup, and greater $1/f$ noise in irradiated devices. These results show that low-frequency noise measurements are a sensitive probe of defects in irradiated Ge pMOS devices.

Compared to Si devices, the degradation of Ge devices after irradiation is relatively larger; however, Ge is still a good alternative for reliable device operation in most typical radiation environments.

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