

**DESIGN AND ANALYSIS OF ADVANCED CVD DIAMOND DIELECTRIC
STRUCTURES**

By

Patrick Taylor

Dissertation

Submitted to the Faculty of the
Graduate School of Vanderbilt University
in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

December, 2006

Nashville, Tennessee

Approved:

Professor Jim L. Davidson

Professor Weng P. Kang

Professor Norman H. Tolk

Professor Alvin M. Strauss

Professor Francis M. Wells

ACKNOWLEDGEMENTS

First, I would like to thank my advisor Dr. Jim Davidson, who for the last eight years has provided me the opportunity to continue my education. Without his knowledge and support, none of this work could have been possible. Dr. Davidson has been instrumental in transforming me from an affable young graduate student to a capable researcher and scientist. He has given me the tools to make the next step into the greater scientific community, and I will be forever grateful for his guidance and friendship.

I would like to thank Dr. Francis Wells, the greatest teacher whom I have ever had. Dr. Wells has taught me the most important lessons about engineering and the nobility of our profession. Through his mentoring, friendship, and expertise I have been provided the means to continue to grow as both an engineer and as a person.

I would also like thank Dr. Weng Poo Kang, the staff, and all students who work with the Vanderbilt Diamond Technology Laboratory. I thank Mr. Mick Howell who has been invaluable to the success of this project and all of our diamond research. I thank all of the students who have studied with the diamond group over the years. I would particularly like to thank Puteri Hamari, Supil Raina, Ka Leng Soh, Karthik Subramanian, Rohit Takalkar, and Yong Mui Wong for their help in completing this research.

I would like to thank NASA and the National Science Foundation for funding these projects.

Finally, I would like to thank the entire Vanderbilt community for twelve wonderful years with special thanks to Chris Carroll, Professor Joe Rea Phillips, and Debra Stephens for allowing me to make my Vanderbilt experience complete.

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	ii
LIST OF TABLES	vi
LIST OF FIGURES	vii
LIST OF ABBREVIATIONS	xii
Chapter	
I. INTRODUCTION	1
II. CAPACITORS	6
Capacitor Types	8
Parallel Plate Capacitors	9
Energy Storage in Capacitors.....	12
Circuit Representation	13
III. DIELECTRIC MATERIALS	15
Dielectric Constant.....	15
Charge Transport in Dielectrics	17
Polarization	18
Polarization Mechanisms	19
Space Charge Polarization	20
Dielectric Material Types	22
Nonferroelectric Materials	22
Ferroelectric Materials	26
Dielectric Losses.....	26
Complex Permittivity.....	26
Dielectric Loss Concerns	28
Corona.....	30
IV. CVD DIAMOND DIELECTRICS	31
Type of Structures.....	32
Polycrystalline Diamond Film	32
Single Crystal Diamond Film	33
Substrate Supported Diamond Film.....	33
Self-Supporting Diamond Film	34

Characterization Techniques.....	34
Dielectric Properties.....	35
Dielectric Transitions.....	36
Frequency Effects on Dielectric Behavior.....	38
Conductivity.....	40
Surface Layer Conductivity	40
Effects of Annealing	42
Grain Boundaries	44
Electrical Conduction Models.....	46
Poole-Frenkel Conduction	48
Poole-Frenkel Conduction in Diamond Films via Hill Conduction	51
Hopping Conduction and Space Charge Limited Current	53
Variable Range Hopping Conduction.....	53
Space Charge Limited Current Conductivity.....	56
Temperature	59
V. ANALYSIS OF CONDUCTIVITY MECHANISMS IN CVD DIAMOND.....	61
Characterization Methods	61
Non-Silicon Substrates.....	63
Thin-Layer Diamond on Tungsten.....	64
Thick-Layer Diamond on Molybdenum	68
Effects of Annealing on Conductivity	71
Grain Boundary Influence on Conductivity.....	86
VI. ADVANCED DIELECTRIC STRUCTURES	96
Current Capacitor Designs.....	96
Film Capacitors.....	96
Ceramic Capacitors.....	98
Electrolytic Capacitors.....	99
Miscellaneous Capacitors	100
Current Diamond Capacitor Structures.....	101
Advanced Diamond Capacitor Structures.....	102
Mechanical Multi-Layer Design.....	106
Monolithic Multi-Layer Design.....	107
Mechanical Multi-Layer CVD Diamond Capacitor	108
Performance Analysis	108
I-V Analysis	110
Capacitance Measurements.....	112
Layered Capacitor Performance	115
Monolithic Multi-Layer CVD Diamond Capacitor	127
Diamond Dielectric.....	130
Conduction Layer.....	132
Characterization	138
Electron Cyclotron Resonance Deposition on Ni	146

VII. SUMMARY AND CONCLUSIONS.....	151
VIII. FUTURE WORK.....	155
REFERENCES	156

LIST OF TABLES

Table	Page
1.1 Comparison of Semiconducting Properties	2
3.1 Dielectric constants of common materials	16
3.2 Dielectric strength of select common materials	29
4.1 Most usual mechanisms of conduction in insulators and expected current-voltage relations	48
6.1 Measured capacitor electrical properties	109
6.2 Calculated capacitor electrical properties	109
6.3 Summary of AC capacitor behavior	112
6.4 Summary of Multi-Layer Diamond Capacitance Behavior	124
6.5 Comparison of Additive Capacitance Individual Device Layers vs. Multi-Layer Capacitors	125
6.6 CVD Diamond Smooth Process Deposition Parameters	130

LIST OF FIGURES

Figure	Page
1.1 Block diagram of CVD process	3
1.2 CVD diamond growth process.....	3
1.3 Process flow of CVD growth technique	4
1.4 Schematic of microwave plasma CVD diamond system.....	5
2.1 Two isolated conductors and resultant electric field lines	6
2.2 Basic parallel plate capacitor	10
2.3 Equivalent circuit schematic of non-ideal capacitor.....	13
3.1 (a) Typical atom in the absence of an applied field (b) Typical atom under the influence of an applied field Voltage Transformer	17
3.2 Fundamental electric polarization mechanisms	20
3.3 Time relationships of different polarization mechanisms.....	22
3.4 Macroscopic scale models of (a) nonpolar and (b) polar material.....	25
4.1 Circuit model of diamond film dielectric behavior.....	35
4.2 Room temperature frequency dependence of permittivity (dielectric constant) for CVD diamond	39
4.3 Room temperature frequency dependence of loss tangent for CVD diamond	39
4.4 Raman spectra for as-grown and 870 K annealed sample	43
4.5 SEM micrographs of a CVD diamond film grown on a Si substrate.....	44
4.6 Current vs. voltage for polycrystalline diamond films (10 μ m thick, room temperature).	47
4.7 Schematic diagram illustrating the Poole-Frenkel effect.....	50
4.8 I-V characteristics at room temperature. Curve (a) as-grown, (b) annealed at 570 K,	

(c) annealed at 673 K, (d) hydrogenated after the annealing at 670 K, and (e) annealed at 670 K after hydrogenation	52
4.9 Logarithmic conductivity vs. $T^{-1/4}$ in the ohmic region for as-grown and 570 K annealed diamond film samples.....	54
4.10 Schematic diagrams illustrating an electron hopping across and an electron tunneling through a square and a triangular potential barrier	55
4.11 Schematic energy level diagrams for (a) electrons and (b) holes injecting from an ohmic contact to a semiconductor or an insulator with shallow and deep electron or hole traps	57
5.1 First generation custom test chamber with diamond film under test.....	62
5.2 Second generation custom test chamber with diamond film sample	62
5.3 Thin diamond layer on tungsten substrate	65
5.4 Leakage current measurements of thin diamond layer on tungsten substrate	66
5.5 Thick layer diamond on molybdenum substrates	68
5.6 I-V characteristic for thick-layer diamond on Mo sample Moly 1	69
5.7 I-V characteristic for thick-layer diamond on Mo sample Moly 2	69
5.8 Curve-fit of leakage profile for sample Moly 1	70
5.9 Influence of annealing on surface conductivity. 300 K conductivity after sample annealing in vacuum (i) and air (ii).....	72
5.10 Pre-annealing I-V profile of diamond dielectric film sample.....	73
5.11 I-V annealing profile of diamond dielectric film sample.....	74
5.12 Comparison of conduction profile for pre-annealed and post-annealed diamond dielectric sample	75
5.13 Surface conductance of the hydrogenated (masked) and the hydrogen-free (irradiated) part of a homoepitaxial diamond (100) layer in UHV and during exposure to air.....	76
5.14 (a) Surface conductance of a plasma hydrogenated (100) diamond single crystal as a function of annealing temperature in air. (b) Infrared spectra in the region of the C-H stretching modes after the hydrogen plasma treatment and after 190 and 230 °C	

annealing temperature, respectively.....	78
5.15 Top: Schematic picture of the hydrogenated diamond surface in contact with a water layer as it forms in air. Bottom: Evolution of band bending during the electron transfer process at the interface between diamond and the water layer.....	79
5.16 Fully-assembled Black-Potted capacitors	80
5.17 Interior design of Black-Potted capacitor. Potting compound (not shown) is added after assembly	81
5.18 (a) I-V characteristic of diamond dielectric sample Juliet 002 (b) Capacitance characteristic of diamond dielectric sample Juliet 002, (c) Dielectric loss of sample Juliet 002 with regards to temperature.....	82
5.19 Calculated energy density of Juliet series diamond film	84
5.20 Comparison of Capacitor #5 leakage profile over a six-year span	85
5.21 Comparison of diamond layer conductivity as a function of micropowder sonication duration	88
5.22 Comparison of diamond layer conductivity as a function of nanopowder sonication duration	89
5.23 Comparison of thin film diamond conductivity after 20 minutes of ultrasonic pre-treatment	90
5.24 Surface morphology of thin film diamond after silicon substrate pre-treatment. (a) No pre-treatment. (b) Nanodiamond powder ultrasonic pre-treatment. (c) Microdiamond powder ultrasonic pre-treatment	93
5.25 High resolution surface morphology of thin film diamond after silicon substrate pre-treatment. (a) Nanodiamond powder ultrasonic pre-treatment. (b) Microdiamond powder ultrasonic pre-treatment	95
6.1 CVD diamond capacitor (substrate-supported)	101
6.2 CVD diamond capacitor (freestanding).....	101
6.3 (a) Parallel combination of two capacitors. (b) Equivalent capacitance, C_{eq}	103
6.4 Mechanical stacked capacitor design (3 layers).....	106
6.5 Monolithic diamond stacked capacitor design.....	107

6.6	I-V analysis of capacitor sample Cap 011	110
6.7	I-V analysis of capacitor sample Cap 012	111
6.8	I-V analysis of capacitance sample Cap 013	111
6.9	Capacitance vs. Frequency - Sample Cap 011	113
6.10	Capacitance vs. Frequency - Sample Cap 012.....	113
6.11	Capacitance vs. Frequency - Sample Cap 013.....	114
6.12	Multi-Layered Diamond Capacitor – Overhead View.....	116
6.13	Multi-Layered Diamond Capacitor in Test Chamber	117
6.14	Multi-Layered Diamond Capacitor – Side Profile.....	117
6.15	Capacitance vs. Frequency – Two-Layer Diamond Capacitor	118
6.16	Comparison of Capacitance of Dual-Layer Capacitor and Individual Device Layers	119
6.17	Dissipation Factor vs. Frequency – Two-Layer Diamond Capacitor	119
6.18	ESR vs. Frequency – Two-Layer Diamond Capacitor	120
6.19	Oscilloscope Capture of Dual-Layer Capacitor Charge-Discharge Behavior	120
6.20	Capacitance vs. Frequency – Three-Layer Diamond Capacitor	121
6.21	Comparison of Capacitance of Triple-Layer Capacitor and Individual Device Layers.....	122
6.22	Dissipation Factor vs. Frequency – Three-Layer Diamond Capacitor	122
6.23	ESR vs. Frequency – Three-Layer Diamond Capacitor	123
6.24	Oscilloscope Capture of Triple-Layer Capacitor Charge-Discharge Behavior	123
6.25	(a) Quartz deposition process mask design for diamond layers of monolithic multi- layered diamond capacitor	127
6.25	(b) Quartz deposition process mask design for conduction layers of monolithic multi-layered diamond capacitor	128

6.26	Monolithic Multi-Layer Design Cross-Section	129
6.27	SEM photograph of base diamond layer surface morphology.....	131
6.28	Base layer of monolithic diamond capacitor with single layer of sputtered Ti-Ni conduction layer.....	135
6.29	Nickel layer of single layer monolithic capacitor	136
6.30	Interface region between Ti-Ni conduction layer and diamond dielectric layer of single layer monolithic capacitor	137
6.31	Leakage profile of base layer of monolithic diamond capacitor.....	139
6.32	Monolithic diamond capacitor after deposition of second dielectric layer.....	140
6.33	I-V comparison of dielectric layers of monolithic diamond capacitor	141
6.34	Leakage profile comparison of individual dielectric layers and composite dielectric of monolithic diamond capacitor	142
6.35	SEM images of second deposited dielectric layer of monolithic diamond capacitor prototype	144
6.36	High magnification SEM imagery of second layer carbonaceous particles	145
6.37	Electron being accelerated clockwise by periodic electric field.....	148
6.38	Electron's spiral path in external magnetic field superimposed with perpendicular periodic electric field	148
6.39	SEM photographs of ECR film deposited on Ti-Ni layer substrate	150

LIST OF ABBREVIATIONS

AC.....	Alternating Current
Ag.....	Silver
Al.....	Aluminum
C.....	Carbon
C.....	Capacitance
CH ₄	Methane
CVD.....	Chemical Vapor Deposition
DC.....	Direct Current
DUT.....	Device Under Test
ECR.....	Electron Cyclotron Resonance
ESR.....	Equivalent Series Resistance
F.....	Farad
H ₂	Hydrogen
Hz.....	Hertz
K.....	Dielectric Constant
L.....	Inductance
MRC.....	Materials Research Corporation
N.....	Nitrogen
Ni.....	Nickel
NH ₃	Ammonia
O ₂	Oxygen

PDF	Polycrystalline Diamond Film
R	Resistance
RF	Radio Frequency
RTA	Rapid Thermal Annealing
sccm	Standard cubic centimeter
SEM	Scanning Electron Microscope
Si	Silicon
Ti	Titanium
TiC	Titanium Carbide
TiH	Titanium Hydride
VDT	Vanderbilt Diamond Technology
W	Tungsten

CHAPTER I

INTRODUCTION

It is well known that natural diamond is one of the most prized substances on Earth. Diamond evokes images of beauty, wealth, and strength reserved for no other material. Diamond boasts a number of impressive properties including high thermal conductivity, wide bandgap, low thermal expansion, chemical inertness, electrical insulation, and extreme hardness. Given these many notable properties, it is no surprise to find diamond used in many diverse applications including precious gems, heat sinks, abrasives, and coatings. With its unique properties diamond has great potential as an engineering material, especially for use in electronic applications. It is well researched that manmade diamond films are one of the most attractive semiconductor materials in existence. When compared to other popular semiconductor materials, as seen in Table 1.1, diamond is superior. These qualities coupled with the fact that diamond can be produced at a competitive cost are some of the major reasons why diamond is at the forefront of advanced materials research.

Table 1.1 Comparison of semiconducting properties [1].

Properties	Diamond	β -Silicon Carbide	GaAs	Silicon
Lattice constant (Å)	3.567	4.358	5.65	5.430
Thermal expansion ($\times 10^{-6} \text{ }^\circ\text{C}$)	1.1	4.7	5.9	2.6
Density (g cm^{-3})	3.515	3.216		2.328
Melting point ($^\circ\text{C}$)	4000	2540	1238	1420
Band gap (eV)	5.45	3.0	1.43	1.1
Saturated electron velocity ($\times 10^7 \text{ cm s}^{-1}$)	2.7	2.5	1.0	1.0
Carrier mobility (cm^2/Vs)				
Electron	2200	400	8500	1500
Hole	1600	50	400	600
Breakdown ($\times 10^5 \text{ V cm}^{-1}$)	100	40	60	3
Dielectric constant	5.5	9.7	12.5	11.8
Resistivity ($\Omega \text{ cm}$)	10^{13}	150	10^8	10^3
Thermal conductivity ($\text{W cm}^{-1} \text{ K}^{-1}$)	20	5	0.46	1.5
Absorption edge (μm)	0.2	0.4		1.4
Refractive index	2.42	2.65	3.4	3.5
Hardness (kg mm^{-2})	10 000	3500	600	1000
Johnson figure of merit ($\times 10^{23} \text{ W } \Omega \text{ s}^{-2}$)	73 856	10 240	62.5	9.0
Keyes figure of merit ($\times 10^2 \text{ W cm}^{-1} \text{ s}^{-1} \text{ }^\circ\text{C}$)	444	90.3	6.3	13.8

Chemical Vapor Deposition (CVD) is often used to create manmade diamond. CVD diamond can show mechanical, tribological, and electrical properties comparable to those of natural diamond [2]. By use of chemical vapor techniques, layers of diamond can be strategically grown. The use of CVD technology and advanced etching and patterning techniques has given researchers the ability to form a number of electrical components from Polycrystalline Diamond Film (PDF).

Chemical vapor deposition involves a gas-phase chemical reaction occurring above a solid surface, which causes deposition onto that surface. All CVD techniques for producing diamond films require a means of activating gas-phase carbon containing precursor molecules. This generally involves thermal (e.g. hot filament) or plasma (D.C., R.F., or microwave) activation or use of a combustion flame (oxyacetylene or plasma torches) [2]. The growth of diamond, rather than other forms of carbon, requires that environment be maintained at a high temperature (1000-1400 K) and that the precursor gas, typically methane (CH_4), be diluted in hydrogen. Diamond grown using this method

is polycrystalline in structure. The CVD process is represented graphically in Figure 1.1. Figures 1.2 and 1.3 illustrate the formation process for CVD diamond. Figure 1.4 depicts a microwave plasma CVD system, as used by Vanderbilt Diamond Technology (VDT).

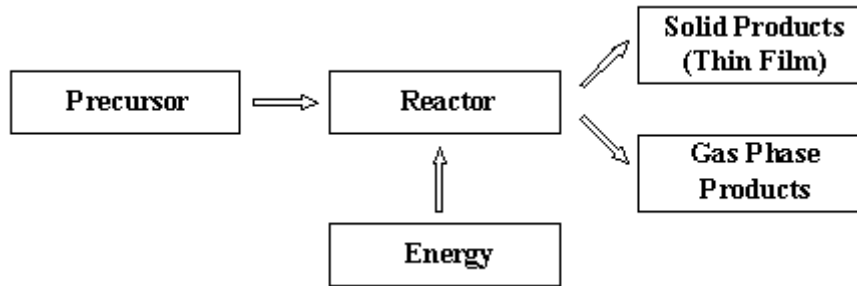


Figure 1.1 Block diagram of CVD process.

Most CVD diamond films are grown on silicon wafers. Other substrate choices such as molybdenum (Mo) and tungsten (W) are also suitable for supporting polycrystalline diamond film. All of these materials have a melting point higher than the temperature required to grow diamond, and they all are capable of forming carbides, which are beneficial to the initial growth stages of the CVD process.

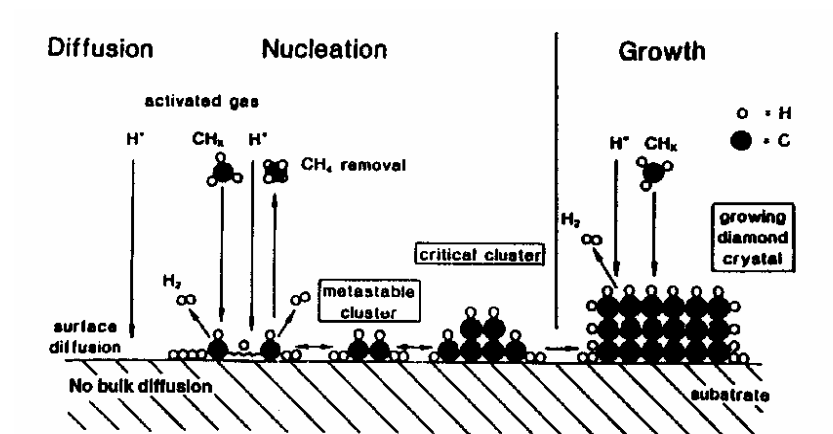


Figure 1.2 CVD diamond growth process [3].

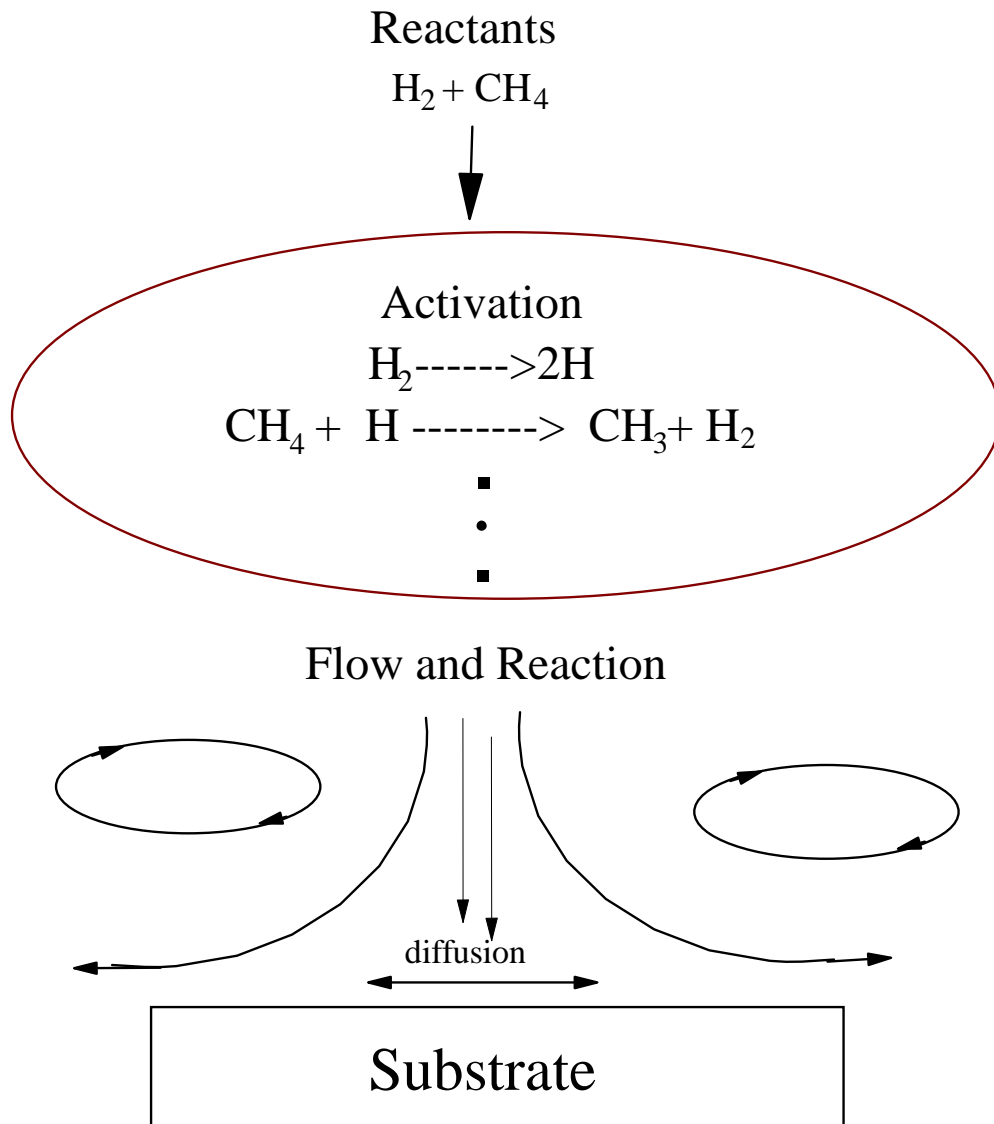


Figure 1.3 Process flow of CVD growth technique.

The electronics industry has long been the proving ground for semiconducting materials. Since CVD diamond films can be doped to have either insulating or semiconducting properties, there is a wide range of electronic applications suitable for PDF development. The rigors of the electronics industry and requirements of other specific fields have forced electronics manufacturers to explore alternatives to the traditional silicon-based

devices that have ruled the industry for the last half-century. CVD diamond devices are a natural fit for this purpose. Research and development have been conducted in the arena of alternative passive components, including CVD diamond capacitors. This work details the development, characterization, and testing of PDF dielectric materials and advanced diamond capacitor structures.

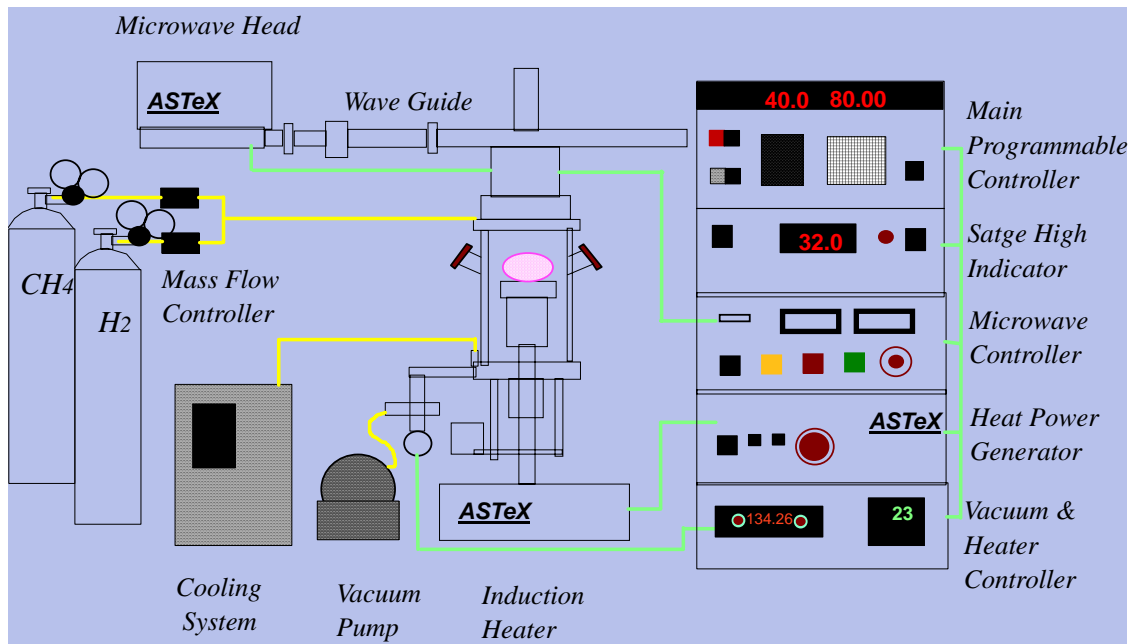


Figure 1.4 Schematic of microwave plasma CVD diamond system.

CHAPTER II

CAPACITORS

A capacitor is a dynamic element involving the time variation of an electric field produced by a voltage [4]. Capacitance is the measure of the ability of a capacitor to store energy in an electric field. Capacitors, like resistors and inductors, are passive elements. Specifically, a passive element is defined as an electrical element that cannot independently generate power to an electrical system. Passive elements can only store or dissipate energy. A capacitor is comprised of two isolated conductors separated by a material medium as shown in Figure 2.1.

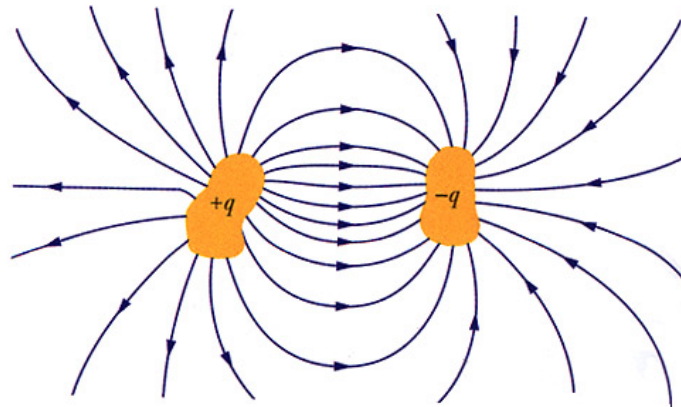


Figure 2.1 Two isolated conductors and resultant electric field lines [5].

While the conductors geometrically may be any shape, the conductors are traditionally referred to as “plates”. If the resistance of the material between the plates is sufficiently large, electric charge cannot be transported through the capacitor. When a voltage is applied to the plates of the capacitor an electric field will be formed between the plates and a current will attempt to flow through the device. Energy is stored in the electric field. The positive current flowing into one plate represents the positive charge moving to the plate from the source. The high resistivity of the separation material, called a dielectric, prevents the charge from flowing to the other plate. This charge will therefore begin to accumulate on the plate. In order for conservation laws to hold charges within the dielectric are displaced to counterbalance the charges building up on the plate. As the voltage varies with time, both the plate charges and displaced charges within the dielectric also vary with time. This time variance of the dielectric charges creates a displacement current as defined by Maxwell in the unified electromagnetic theory. This displacement current will be present wherever an electric field or voltage varies with time. The displacement current flowing internally between the capacitor plates is exactly equal to the conduction current flowing in the capacitor leads [6]. The current is proportional to the rate at which the voltage varies with time. Mathematically this is expressed as below.

$$i = C \frac{dv}{dt} \tag{2.1}$$

The current i is measured in amperes. The capacitance C is measured in farads (F). The Voltage v is measured in volts. The time t is measured in seconds. It is this

proportionality to time-varying voltage that leads to the open-circuit behavior of an ideal capacitor at DC voltages.

A farad, named in honor of British physicist and experimenter Michael Faraday, is defined as one coulomb per volt and is a very large measure of capacitance. The charge q and the potential difference V for a capacitor are proportional to each other. That is,

$$q = CV. \tag{2.2}$$

The capacitance is therefore a proportionality constant that is ultimately dependent upon the geometry of the capacitive device.

Practical capacitors are measured in submultiples of farads and most commonly have values that lie in the nanofarad (nF) to microfarad (μ F) range.

Capacitor Types

Capacitors are used for a wide variety of purposes and are made from many different materials in a variety of different geometries and styles. There are three primary groups of capacitors, as determined by use for ac, dc, and pulse applications.

1. **AC Capacitors:** AC capacitors are the most general type of capacitor. AC capacitors can be used with a measure of success for most capacitive applications and come in a variety of shapes and sizes. AC capacitors can be used in dc and pulse applications. The reverse, however, is not necessarily true.

2. **DC Capacitors:** DC capacitors are used to convert time-varying input voltages into steady dc output voltages. These capacitors are typically used in filtering applications and are sometimes called filter capacitors. DC capacitors typically only are exposed to a single polarity of voltage and are often designed accordingly. Capacitors of this design are referred to as polarized or electrolytic capacitors and are commonly made of aluminum oxide or tantalum.

3. **Pulse Capacitors:** Pulse capacitors are used in applications that require quick discharges. The fast discharge is usually used to deliver a large amount energy in a short period of time. Most pulse capacitor applications involve a long charging period followed by a discharge period in the sub-microsecond range. Pulse capacitors are often used with large voltages and currents and typically have a shorter operational lifetime than ac or dc capacitors. Pulse applications include particle accelerators, laser drivers, X-ray generators, Tesla coils, flash tubes, and impulse welders.

Parallel Plate Capacitors

The simplest and most used physical form of a capacitive device is a parallel plate capacitor, as shown in Figure 2.2. In the parallel plate capacitor, two plates of area A are separated by a distance d .

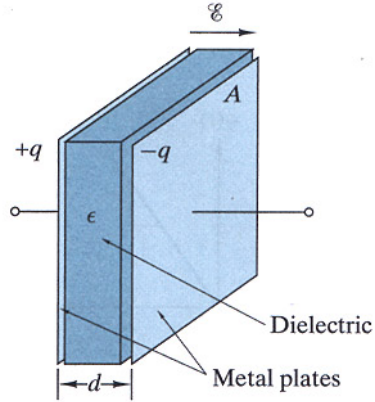


Figure 2. 2 Basic parallel plate capacitor [4].

Much of the simplicity of the parallel plate capacitor arises from the fact that the capacitance is a direct linear relationship between the geometry of the capacitor and the intrinsic physical properties of the dielectric material. If the distance between the plates is small compared to the area of the plates, a nontrivial electric field can be formed. The electric field E between the plates for a plate charge of magnitude q can be expressed via Gauss' Law as

$$q = \epsilon \oint E \cdot dA, \quad (2.3)$$

where ϵ is the permittivity of the dielectric. For the given geometry, this form reduces to

$$q = \epsilon EA. \quad (2.4)$$

The potential difference (voltage drop) between the positive and negative plates can be derived from its integral form as

$$V = \int_+^- E \cdot ds = \int_+^- E ds = E \int_0^d ds = Ed. \quad (2.5)$$

Substituting Equations 2.4 and 2.5 into the general capacitance relationship, $q = CV$, the capacitance of the parallel plate capacitor is given by

$$C = \varepsilon \frac{A}{d}. \quad (2.6)$$

Energy Storage in Capacitors

Another fundamental aspect of capacitor operation is energy storage. When a voltage is applied to a capacitor, the resulting electric field and displacement current formed within the dielectric will disturb the normal behavior of the bound charges of the material. Work is done in the associated movement of particles. The energy is stored in the dielectric as electrostatic energy. The energy can be calculated by integrating then power absorbed by the capacitor over a given interval of time. The net energy entering a capacitor over an interval is

$$W(t_0, t_1) = \int_{t_0}^{t_1} p_C(\tau) d\tau = \int_{t_0}^{t_1} v_C(\tau) i_C(\tau) d(\tau). \quad (2.7)$$

Using the definition of capacitor current derived previously,

$$W(t_0, t_1) = \int_{t_0}^{t_1} \left(v_C(\tau) C \frac{dv_C(\tau)}{d\tau} \right) d\tau = C \int_{v_C(t_0)}^{v_C(t_1)} v_C dv_C. \quad (2.8)$$

Finally,

$$W(t_0, t_1) = \frac{1}{2} C [v_C^2(t_1) - v_C^2(t_0)]. \quad (2.9)$$

The instantaneous energy stored in a capacitor is

$$W = \frac{1}{2} C v_C^2(t). \quad (2.10)$$

The change in stored energy over any given interval depends only on the value of the voltage on the capacitor at times t_0 and t_1 . The amount of stored energy is therefore independent of the type of voltage waveform that is present during the charging interval.

Circuit Representation

A non-ideal capacitor can be represented as an equivalent electric circuit. A capacitor is formed from metal and dielectric materials, each of which contributes to the operational losses of the device. The circuit model accounts for the various capacitor losses. The equivalent circuit model is shown in Figure 2.3. The series inductance L_s represents the natural inductance that is associated with any conductive material, regardless of geometry. The terminals and electrodes contribute to L_s . The series resistance R_s represents the effects of dielectric loss and conductor resistance. The parallel resistance R_p represents the leakage through the capacitor at DC.

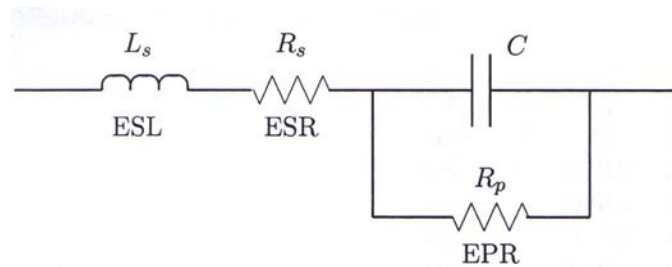


Figure 2.3 Equivalent circuit schematic of non-ideal capacitor [7].

The circuit model components are more commonly referred to as equivalent resistances or inductances. These are defined as below by the terms ESL, ESR, and EPR.

$ESL = L_S =$ Equivalent Series Inductance

$ESR = R_S =$ Equivalent Series Resistance

$EPR = R_P =$ Equivalent Parallel Resistance

CHAPTER III

DIELECTRIC MATERIALS

The effectiveness of any capacitive device is most often directly related to the materials of which it is made. The dielectric material that separates the conducting plates is in practice the most important component of any capacitor. By adjusting the size or type of material used as the dielectric, a given capacitor design can be used to generate a wide variety of capacitance values and electric tolerances.

Dielectric Constant

Dielectric materials function as the insulating medium in capacitive devices. The permittivity (ϵ) of a dielectric can be written in the form

$$\epsilon = \epsilon_r \epsilon_0, \quad (3.1)$$

where ϵ_r is the relative permittivity of the material, and ϵ_0 is the permittivity of free space ($8.85 \times 10^{-12} \text{ C}^2/\text{N} \cdot \text{m}^2$), a defined constant. The relative permittivity is often called the dielectric constant (κ) in practice. The dielectric constant indicates the relative energy storage capabilities of dielectric material compared to free-space. It is also the factor by which the capacitance is increased for a device that uses a dielectric material versus a vacuum to separate the conduction plates. By definition, the dielectric constant of a

vacuum is unity. Values of the dielectric constants of a number of materials are shown in Table 3.1.

Table 3.1 Dielectric constants of common materials [9].

Material	Static dielectric constant (ϵ_r)
Air	1.0006
Styrofoam	1.03
Paraffin	2.1
Teflon	2.1
Plywood	2.1
RT/duroid 5880	2.20
Polyethylene	2.26
RT/duroid 5870	2.35
Glass-reinforced teflon (microfiber)	2.32–2.40
Teflon quartz (woven)	2.47
Glass-reinforced teflon (woven)	2.4–2.62
Cross-linked polystyrene (unreinforced)	2.56
Polyphenelene oxide (PPO)	2.55
Glass-reinforced polystyrene	2.62
Amber	3
Soil (dry)	3
Rubber	3
Plexiglas	3.4
Lucite	3.6
Fused silica	3.78
Nylon (solid)	3.8
Quartz	3.8
Sulfur	4
Bakelite	4.8
Formica	5
Lead glass	6
Mica	6
Beryllium oxide (BeO)	6.8–7.0
Marble	8
Sapphire	$\epsilon_x = \epsilon_y = 9.4$ $\epsilon_z = 11.6$
Flint glass	10
Ferrite (Fe ₂ O ₃)	12–16
Silicon (Si)	12
Gallium arsenide (GaAs)	13
Ammonia (liquid)	22
Glycerin	50
Water	81
Rutile (TiO ₂)	$\epsilon_x = \epsilon_y = 89$ $\epsilon_z = 173$

Another effect of the introduction of a dielectric is to limit the potential difference that can be applied between the plates to a certain value V_{\max} . If this value is substantially exceeded, the dielectric material will break down and form a conducting path between the plates [5].

Charge Transport Mechanisms in Dielectrics

The dominant charges in dielectrics are bound charges. These charges are positive and negative charges restricted to a localized area by local atomic or molecular forces. They are not free to travel throughout a material like those found in conductors. In conductors, charges are free to move to the surface of the material when placed under the influence of an external electric field. Charges in a dielectric, however, will shift slightly from a centered position to form electric dipoles throughout the material. This is illustrated in Figure 3.1.

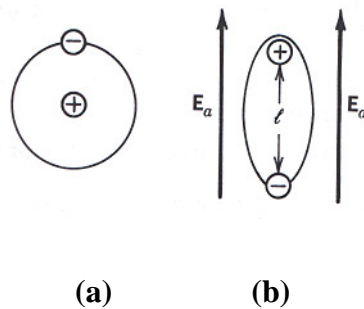


Figure 3.1 (a) Typical atom in the absence of an applied field
(b) Typical atom under the influence of an applied field [9].

Polarization

The process of forming dipoles is referred to as polarization. For each dipole a dipole moment,

$$dp = Q\ell, \quad (3.2)$$

is formed where Q is the magnitude of the charges, and ℓ is the separation between the charges. Throughout the volume of a material, assuming that the material is relatively homogenous, an average dipole moment of

$$dp = Ql_{avg} \quad (3.3)$$

can be found per atom or molecule. The electric polarization of the material can be expressed as

$$P = NQl_{avg}, \quad (3.4)$$

where N is the number of electric dipoles per unit volume. This electric polarization is based on the fact that all of the dipoles are aligned in the same direction under the influence of an external electric field. The ability of a dielectric to store electric energy is represented within the polarization of the material. The resistance of the bound charges of the dielectric to the forced shifting in position due to the external electric field

produces a source of potential energy much like that found in the act of stretching a spring.

After the external field is removed, there is there is a finite amount of time that must elapse before the material can depolarize and return to its original equilibrium state.

Polarization Mechanisms

Electric polarization occurs due to the three fundamental mechanisms as shown in Figure 3.2. Depending on the atomic or molecular makeup of the material, a given material may undergo any combination of mechanisms while under the influence of an external electric field.

1. **Dipole or Orientational Polarization:** This polarization is evident in materials that, in the absence of an applied field and owing to their structure, possess permanent dipole moments that are randomly oriented. However when an electric field is applied, the dipoles tend to align with the applied field. Water is a good example.
2. **Ionic or Molecular Polarization:** This polarization is evident in materials, such as sodium chloride (NaCl), that possess positive and negative ions and that tend to displace themselves when an electric field is applied.

3. **Electronic Polarization:** This polarization is evident in most materials, and it exists when an applied electric field displaces the electric cloud center of an atom relative to the center of the nucleus.

Mechanism	No applied field	Applied field
Dipole or orientational polarization		
Ionic or molecular polarization		
Electronic polarization		

Figure 3.2 Fundamental electric polarization mechanisms [9].

Space Charge Polarization

The perturbing of bound positive and negative charges within the atoms and molecules of a dielectric material produces the fundamental polarization mechanisms. Polarization can also be produced by mobile or trapped charges within a material. This type of polarization is space charge polarization. This type of polarization is most commonly found in polycrystalline or amorphous materials with traps. Charge carriers injected into the dielectric from electrical contacts can be trapped in the material bulk or in interface traps. The resulting impediment will form space charges in the material. The space

charges will, in turn, distort the field formation within the material and subsequently affect the polarization of the material.

Space charge polarization can occur in two possible ways.

1. **Hopping Polarization:** In hopping polarization, local charges, which can normally move freely from one site to a neighboring site within a material, will jump or tunnel through a potential barrier (depending on the barrier height and width) to reach another site. The resulting “hop” will produce a space charge, which will modify field distribution.
2. **Interfacial Polarization:** In interfacial polarization, a space charge is produced by the separation of mobile positive and negative carriers under an applied field. The separation will create space charges in the bulk of the material and at the interfaces between different materials. These space charges will then adjust the field distribution and, in turn, create a polarization.

By their nature space charge polarizations typically take longer to develop than the three fundamental polarization mechanisms. Figure 3.3 illustrates a comparison of this fact.

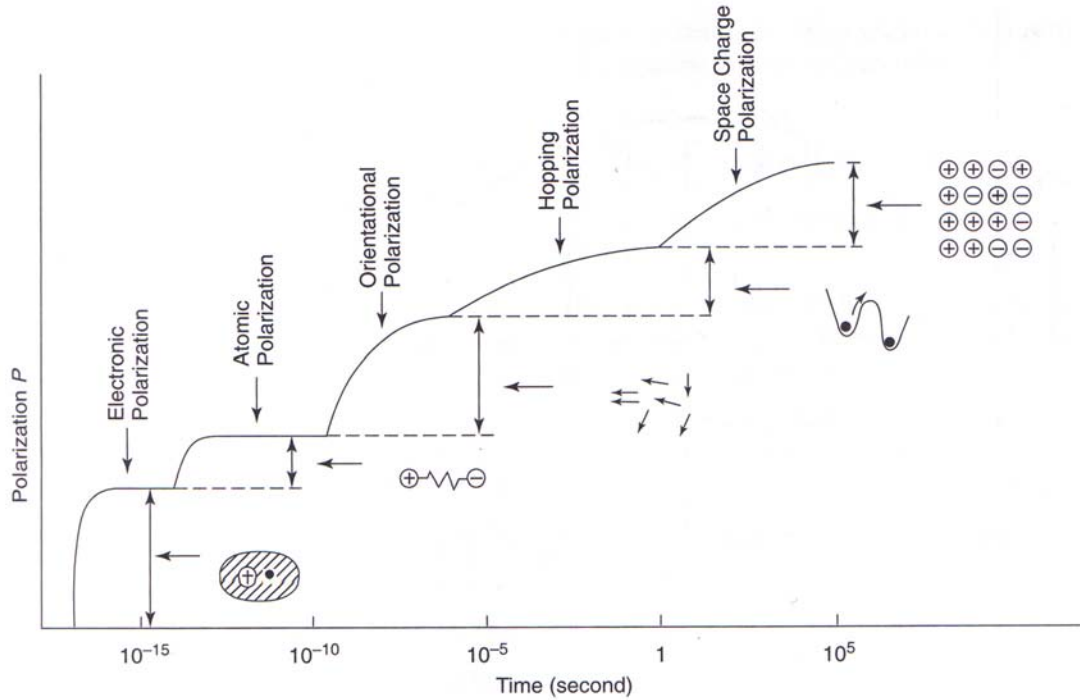


Figure 3.3 Time relationships of different polarization mechanisms [8].

Dielectric Material Types

Dielectrics are divided into two types of materials: nonferroelectric materials and ferroelectric materials. The difference between the types is due to the dominant form of polarization endured by a given material. This is chiefly governed by the atomic and molecular composition of the material.

Nonferroelectric Materials

Nonferroelectric materials are also called normal dielectrics. This is because most common dielectric materials are nonferroelectric in nature. For these materials polarization is initiated by external electric fields. The total polarizability (α) of these

materials is a function of the three electric polarization mechanisms: electronic polarization (α_e), ionic polarization (α_i), and orientational (dipole) polarization (α_o). Nonferroelectric materials are divided into three classes: nonpolar, polar, and dipolar dielectrics.

1. **Nonpolar Dielectrics:** Nonpolar materials have charges that are distributed in a manner in which positive and negative charges cancel each other throughout the material. There is no net charge, net dipole moment, or net polarization in the material in the absence of an external field. When an electric field is applied, a net nonzero polarization will result. The field will act to stretch the positive and negative components of the atoms or molecules in the material. These materials only endure electronic polarization. For nonpolar dielectrics the total polarizability is

$$\alpha = \alpha_e. \quad (3.5)$$

Nonpolar materials are referred to as elemental materials because they typically consist of a single kind of atom. Examples of nonpolar materials include silicon, diamond, and inert gases.

2. **Polar Dielectrics:** Polar materials are typically composed of molecules. The molecules are composed of a single type of atom with no permanent dipole

moment. The polarizability of polar dielectrics will have components of both electronic and ionic polarization. The electric field will displace the position of valence electrons and in turn will displace the relative position of ions within the material. The total polarizability is

$$\alpha = \alpha_e + \alpha_i . \quad (3.6)$$

Examples of polar materials include ionic crystals, benzene, and carbon tetrachloride.

3. **Dipolar Dielectrics:** Dipolar materials have permanent electric dipole moments. When subjected to an electric field the dipoles will align with the field, producing an orientational polarization. For this reason dipolar materials exhibit all three of the fundamental electrical polarizations. The total polarizability is

$$\alpha = \alpha_e + \alpha_i + \alpha_o . \quad (3.7)$$

The molecules in a polar material are under constant thermal agitation due to the natural motion of the dipoles. The external electric field, therefore, will not typically produce a complete alignment of particles. This alignment can be increased by increasing the applied field or by lowering the temperature of the material. Dipolar materials include water, sulfuric acid, and hydrochloric acid. The models in Figure 3.4 compare the reactions of nonpolar and dipolar materials

to the influence of an external field. Since they are both comprised of molecular substances, dipolar and polar materials are often grouped together and referred to as simply “polar” materials.

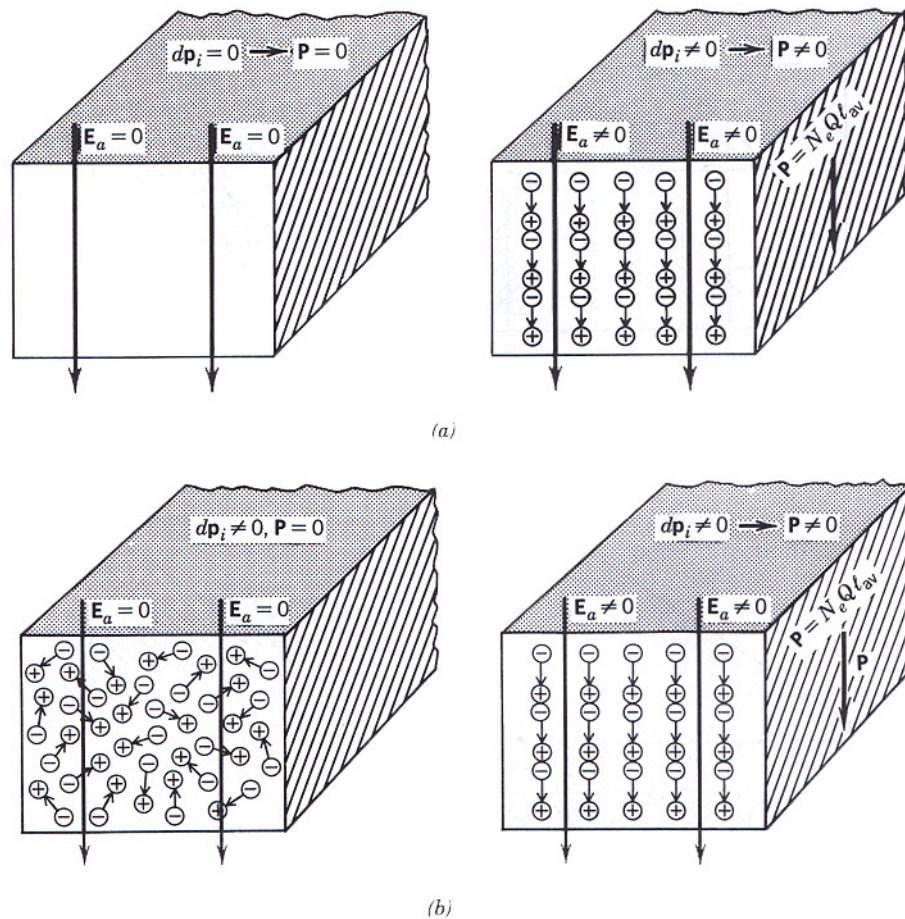


Figure 3. 4 Macroscopic scale models of (a) nonpolar and (b) polar material [9].

Ferroelectric Materials

Ferroelectric materials are normally crystalline in nature. They may be either single crystalline or polycrystalline. The dominant type of polarization in ferroelectric materials

is not electric polarization. Instead, it is spontaneous polarization. At the Curie temperature, ferroelectric materials will experience a phase transition from an ordered phase to a disordered phase. This phase transition will cause a displacement of the atoms of the crystal structure. This displacement will, in itself, create a polarization in the material. Ferroelectric materials are also subject to electric polarization. The contribution of electric polarization, however, is negligibly small compared to the spontaneous polarization in the material. Ferroelectric materials will typically also have piezoelectric, piezoelectric, and electro-optic attributes due to the mechanical deformation that often follows the changes in volume and shape induced by the phase transition.

Dielectric Losses

All electrical devices, including capacitors, are subject to operational losses. All dielectric materials are subject to two types of losses. One type of loss is a direct result of the flow of charge through the dielectric. This is conduction loss. The other loss mechanism is due to the movement of atoms or molecules in response to an electric field. This is dielectric loss.

Complex Permittivity

In order to represent the contribution of dielectric losses and allow for the friction that accompanies polarization and the movement of particles, the permittivity can be represented as a complex number. This can be written as

$$\varepsilon^* = \varepsilon - j\varepsilon', \quad (3.8)$$

where ε is the real permittivity, and ε' is the dielectric loss factor. The real permittivity is defined as

$$\varepsilon = \varepsilon_r \varepsilon_0. \quad (3.9)$$

Here, ε has the traditional definition where ε_r is the dielectric constant (relative permittivity) and ε_0 is the permittivity of free space. Using a complex permittivity, the capacitance can be represented as

$$C^* = C - jC'', \quad (3.10)$$

where C^* is the complex capacitance. With the complex representation of the permittivity and capacitance, ε^* and C^* approach the values of the real permittivity and real capacitance as the dielectric losses approach zero.

The complex permittivity can alternatively be written in polar form.

$$\varepsilon^* = |\varepsilon^*| e^{-j\delta} \quad (3.11)$$

In this form δ is defined as the dielectric loss angle. Furthermore,

$$\tan \delta = \frac{\varepsilon''}{\varepsilon'} \quad (3.12)$$

where $\tan \delta$ is defined as the loss tangent or dissipation factor (DF). The dissipation factor is the mostly commonly used representation for dielectric losses. In an ideal lossless capacitor the loss tangent is zero. For loss efficiency the dissipation factor should be as small as possible. Therefore, a material is considered to be a “good” dielectric if $\varepsilon' \gg \varepsilon''$.

In general, losses cause a dielectric to heat. The associated heat may lead to thermal breakdown and subsequent failure of the material. Dielectric losses are predominately active at low frequencies (less than 1 MHz). Conduction losses from metals as found in capacitor electrodes or terminals, on the other hand, tend to dominate at higher frequencies (10 MHz and above).

Dielectric Loss Concerns

For each material there are advantages and disadvantages with its use as a practical dielectric. An ideal dielectric would possess a high dielectric constant and a low dissipation factor. Other concerns such as breakdown voltage, temperature stability, voltage stability, frequency stability, cost, and manufacturability also play a role in the effectiveness of a dielectric under different operational conditions. No material exists that is perfect in all of these regards. Careful evaluation of dielectric characteristics is therefore necessary to properly select an appropriate dielectric for a given application.

Table 3.2 compares the strength of some common dielectric materials.

Table 3.2 Dielectric strength of select common materials [7].

Material	ϵ_r	ϵ_r	DF	DF	V_b
	60 Hz	10^6 Hz	60 Hz	10^6 Hz	V/mil
Air	1.000585	1.000585	-	-	75
Aluminum oxide	-	8.80	-	0.00033	300
Barium titanate	1250	1143	0.056	0.0105	50
Carbon tetrachloride	2.17	2.17	0.007	<0.00004	-
Castor oil	3.7	3.7	-	-	300
Glass, soda-borosilicate	-	4.84	-	0.0036	-
Heavy Soderon	3.39	3.39	0.0168	0.0283	-
Lucite	3.3	3.3	-	-	500
Mica, glass bonded	-	7.39	-	0.0013	1600
Mica, glass, titanium dioxide	-	9.0	-	0.0026	-
Mica, ruby	5.4	5.4	0.005	0.0003	-
Mylar	2.5	2.5	-	-	5000
Nylon	3.88	3.33	0.014	0.026	-
Paraffin	2.25	2.25	-	-	250
Plexiglas	3.4	2.76	0.06	0.014	-
Polycarbonate	2.7	2.7	-	-	7000
Polyethylene	2.26	2.26	<0.0002	<0.0002	4500
Polypropylene	2.25	2.25	<0.0005	<0.0005	9600
Polystyrene	2.56	2.56	<0.00005	0.00007	500
Polysulfone	3.1	3.1	-	-	8000
Polytetrafluoroethylene(teflon)	2.1	2.1	<0.0005	<0.0002	1500
Polyvinyl chloride (PVC)	3.2	2.88	0.0115	0.016	-
Quartz	3.78	3.78	0.0009	0.0001	500
Tantalum oxide	2.0	-	-	-	100
Transformer oil	2.2	-	-	-	250
Vaseline	2.16	2.16	0.0004	<0.0001	-

Corona

Dielectric loss and failure can also be contributed to compounding damage suffered over the operational lifetime of the material. There exists a voltage level, independent of the dielectric breakdown voltage, at which trapped air or air-filled voids within a dielectric will begin to ionize and partial discharge will occur. This discharge is called corona. Over time corona will degrade the dielectric and ultimately lead to failure. Commercial

capacitors are often derated after production to account for the lifetime effect of voltage cycling and corona.

CHAPTER IV

CVD DIAMOND DIELECTRICS

Chemical vapor deposition (CVD) produces diamond film that is chemically inert, has high mechanical strength and high thermal conductivity, possesses a wide band gap and high breakdown strength, and exhibits a relatively high dielectric constant. These characteristics suggest the use of diamond film as capacitor dielectrics for high voltage and high temperature applications [10]. The ideal diamond is a semiconductor with an electrical resistivity of 10^9 - 10^{12} Ω cm and an indirect bandgap of 5.5 eV. The bandgap is so wide that the diamond film is often considered to behave effectively as an insulator. However, only type IIa diamond films, non-conductive diamond films with no nitrogen impurities, are pure enough to exhibit the semiconducting properties of the undoped crystal. Other diamond films exhibit resistivities many orders of magnitude lower than that for type IIa, usually due to the presence of defect, non-diamond phases, and the scattering of carriers at grain boundaries. Nevertheless, the tendency of the sp^3 bonds of diamond to change to sp^2 during the microwave plasma-enhanced CVD process and, hence, to form non-diamond phases, including graphite, nanocrystalline diamond, and amorphous carbon, may influence the electrical or dielectric properties [11]. The development of polycrystalline diamond as a capacitive agent ultimately depends ultimately one criteria - the ability to produce diamond that is viable as a dielectric material. A great deal of research has been completed on the dielectric nature of CVD

diamond. The purposes of this chapter are to overview that research and give the necessary background for the future research to be detailed later in this body of work.

Types of Structures

CVD techniques have produced diamond films on various substrates. Diamond film has also been devised of different crystal structures. The exact growth conditions and design of the diamond film is ultimately dependent upon the application intended for the structure. The physical structure has bearing on both the electrical and mechanical performance of the film.

Polycrystalline Diamond Film

Most current research has focused on applications and analysis of polycrystalline diamond films. Polycrystalline diamond is typically cheaper and easier to fabricate than single crystal diamond. The nature of polycrystalline diamond, however, makes it difficult to produce thin films that are free from the effects of pinholes. As-deposited polycrystalline diamond thin film is very non-uniform and the surface smoothness is on the order of $\pm 2 \mu\text{m}$. Nucleation of diamond is not uniform, since the nucleation will generally occur as individual particles, which eventually coalesce to form continuous diamond thin films. The minimum thickness required for diamond thin films to be continuous is approximately 5-15 μm [10]. To date there is not an agreed upon method to suitably and accurately identify the presence of pinholes in diamond films. For these

reasons the presence of pinholes is always a factor of consideration in the effectiveness of polycrystalline thin film diamond.

Single Crystal Diamond Film

To counter the pinhole-effect, researchers have taken one of two fabrication routes. One solution is to simply grow thicker films. Thicker films, while usually free from pinholes, are not necessarily appropriate for all applications. The other approach, as evidenced by the research of Ramesham *et al.* [10], is to produce single-crystal diamond for thin film capacitor applications. Synthesis of single crystal diamond is more difficult due to the nature of the nucleation process. Ion implementation techniques can be used to help facilitate the process. This will allow the nucleation to become uniform and allow for the creation of single crystal films, which are in principle smooth and pinhole-free. This process, however, is more expensive.

Substrate Supported Diamond Film

Most dielectric characterization of CVD diamond has been performed on substrate supported diamond films. Silicon is the substrate of choice for most experiments. Other materials such as molybdenum, tungsten, and alumina have also been used. Si provides a good growth surface for CVD diamond and provides a surface that is easy to use for the application of electrical contacts. It is estimated that the effect of current conduction through a Si substrate (p-type) on the measured resistance is less than 0.1% over a wide temperature range (≤ 500 °C) and can thus be effectively ignored for most measurements.

Self-Supporting Diamond Film

Studies have also been conducted using self-supporting diamond films. In these studies, the substrate is etched away (in whole or in part) and electrical contacts are applied to both sides of the exposed diamond film. Often molybdenum and tungsten are used as the initial substrate for freestanding films. The differences in thermal expansion coefficients between these materials and diamond allow for easier and cleaner separation of the film from the substrate. The thickness of the film is an important factor in the development of self-supporting films. Thin films are more susceptible to breakage than thin films that remain on substrates. For this reason, freestanding diamond tends to be produced as thicker films.

Characterization Techniques

For the characterization of dielectrics and capacitors, two basic measurement classes are required. From AC measurements the capacitance and the relative dielectric constant may be extracted. Furthermore, DC leakage measurements are necessary for the estimation of the dielectric loss [12]. Other experimental methods such as impedance spectroscopy have also been utilized to measure aspects such as resistivity and carrier transport mechanisms, and Raman spectra is often used to examine film composition. Most of the dielectric characterization of diamond films has concentrated on capacitance-voltage ($C-V$) and current-voltage ($I-V$) relationships. This is partly due to the basic intuitive nature of the results of these experiments. Also, these tests give a set of results that are easily comparable to more established dielectric materials.

A number of methods have been used in the determination of dielectric loss at differing frequencies. Often commercial LCR instruments are used for low frequency measurements (≤ 100 MHz), and higher frequency ranges are often measured using resonant circuits or cavities.

Dielectric Properties

The dielectric properties of diamond film have been studied by a number of researchers. A number of factors including temperature, thickness, film composition, and frequency affect the dielectric behavior.

Dielectric behavior can be modeled as a double parallel RC circuit in series. The circuit is composed of the parallel combinations of resistances and capacitances from the bulk grain interior and grain boundary. The resistances represent ionic or electronic conduction mechanisms. The capacitors represent the polarizability of the diamond. Here, R_b and R_g correspond to the bulk grain interior and grain boundary resistances, respectively. C_b and C_g represent the capacitances attributed to the bulk grain interior and grain boundary [13]. Figure 4.1 illustrates this relationship.

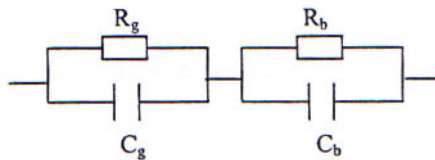


Figure 4. 1 Circuit model of diamond film dielectric behavior [13].

Experiments by Heidger *et al.* [14] have shown that the dielectric constant and loss tangent of annealed CVD diamond films exhibit steady dielectric constants ranging from 5.7 to 6 and loss tangents on the order of 0.005 over the frequency range of 100 to 10^6 Hz. This agrees closely with the established dielectric constant of natural diamond (5.5-5.7). The power dissipation in an insulator or capacitor is directly proportional to the dielectric loss factor. The measured loss tangents are within acceptable parameters.

Diamond films have breakdown strengths that approach those of natural diamond. Tests have shown that the breakdown strength varies with film thickness. In general, the breakdown strength increases as the film thickness increases.

As experimental conditions are changed, most notably temperature and frequency, a number of changes in dielectric behavior have been observed. Fluctuations in dielectric behavior could be the result of surface termination, metal contact interface effects, or a combination of factors [15].

Dielectric Transitions

As discussed previously, the polarization process governs the dielectric nature of materials. It has been observed, however, that the polarizability of diamond film is subject to changes in temperature. Using impedance spectroscopy measurements, Ye *et al.* indicated that there is a threshold temperature for the dielectric behavior of diamond film. Using thin film diamond heated from 0-500 °C, a change was seen in the dielectric behavior at 250 °C. At that temperature, analysis shows that the polarization, which dominated by the bulk interior of the diamond at temperatures below 250 °C, begins to be dominated by the grain boundaries.

Changes in crystal field caused by thermal expansion or by surface bond contraction can be explained as the physical mechanism responsible for the dielectric transition [13].

Only one primary mechanism exists for the polarization of diamond film at temperatures below 250 °C. Above 250 °C there are competing polarization mechanisms contributed from both the grain boundaries and the grain interior.

Transitions in dielectric behavior may also be due to other mechanisms that may affect the electrical conduction of diamond films. Numerous studies have speculated about these mechanisms. The movement of hydrogen and defects from deep level to non-active sites during the annealing process has been suggested as a possible mechanism. The influence of surface conduction layers has been cited as a possible contributor. Much work has been done on the effects of space charge limited currents and the Poole-Frenkel mechanism in conduction. Others have looked at frequency-independent and frequency-dependent band conduction and the effects of hopping conduction.

It can be assumed that dielectric transition threshold is directly linked to the thickness of the diamond film. As the film increases in thickness, the temperature threshold for dielectric transition should increase. This is due to the fact that the impact of the contributions of the grain boundaries decreases with increasing thickness because the grain boundaries comprise less total surface area of the film compared to that of the bulk interior. It therefore, will require a higher temperature to reach the necessary level for thermal activation of the grain boundaries.

Frequency Effects on Dielectric Behavior

The growing interest in using diamond for high frequency applications such as input windows for fusion reactors has promoted the increased study of frequency dependent dielectric behavior. Diamond films have now been studied into the GHz range. However, the nature of the loss mechanisms in polycrystalline CVD diamond is still not completely understood. It is known that electrically active defects can be recombination centers or carrier traps, and can determine carrier concentration, mobility, and other electrical properties of CVD polycrystalline diamond films. Some defects are formed during the diamond growth process. Other defects can be created by ionizing radiation and postgrowth treatment, such as annealing [16].

Ibarra *et al.* [17] studied dielectric properties at room temperature. Dielectric constant was considered to be constant for frequencies over 10^5 Hz, with a value around 5.7. For frequencies below 10^5 Hz dielectric constant increases with decreasing frequency reaching a value around 5.9 at a frequency of 1 Hz. In the case of loss tangent, a decrease with frequency from 10 to 10^{11} Hz was observed. The loss tangent dropped from 0.04 at low frequencies to 0.0005 at high frequencies. The rate of change of loss tangent was higher at low frequency than high frequency. Below 10 Hz, the loss tangent appeared to saturate. This pattern is consistent with an explanation that Hill-type conduction mechanisms may dominate the loss tangent at low frequencies. For Hill conduction the loss tangent is a function of frequency and reasonably follows the patterns seen in the Ibarra experiments in that range. Figures 4.2 and 4.3 illustrate the relationships.

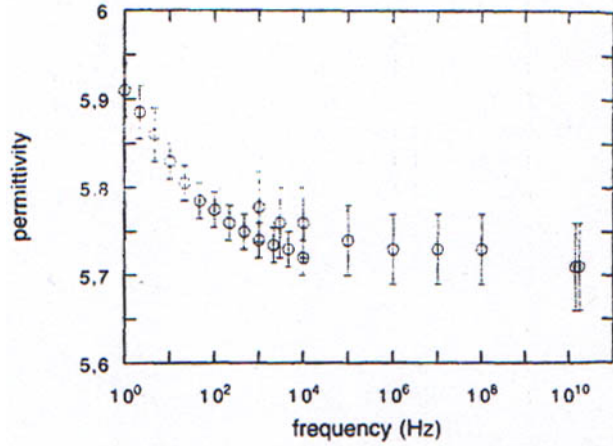


Figure 4.2 Room temperature frequency dependence of permittivity (dielectric constant) for CVD diamond [17].

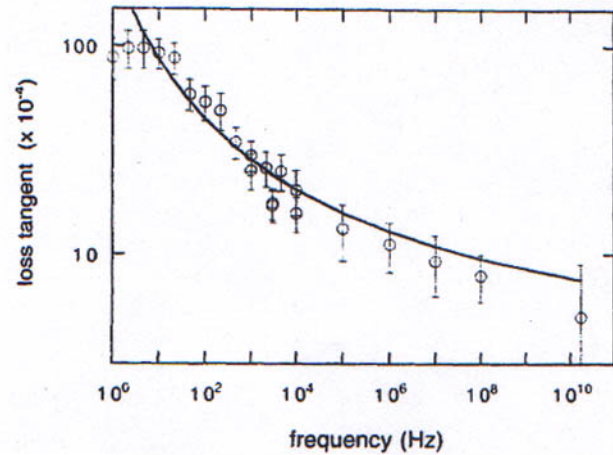


Figure 4.3 Room temperature frequency dependence of loss tangent for CVD diamond. The line is the fit to a Hill-type conduction mechanism [17].

When studied over a wide frequency range, Molla *et al.* observed irregularity in the dielectric loss of diamond film. Results indicated that several loss mechanisms might arise at different frequencies in CVD diamond. All of these loss mechanisms, however, are most likely related to defects. This gives rise to a great dispersion of measured

results, which must be related to intrinsic differences in the diamond grades measured [18].

Conductivity

A number of studies have been performed examining the nature of the conductivity of CVD diamond films. The measure of DC leakage current is the primary conductivity indicator. For a good dielectric the conductivity is low. Polycrystalline films contain various growth defects and impurities as a consequence of the CVD process. The conduction in undoped films is mainly controlled by these defects and impurities. These give rise to various electronic defect states with a consequent deterioration in carrier mobilities and other electronic properties. Therefore, there is a direct link between growth conditions and transport parameters within a given diamond film [19].

Surface Layer Conduction

As mentioned previously, an active surface layer may contribute to charge transport and conduction in diamond film. This conduction layer is attributed to the influence of hydrogen in the CVD diamond structure.

The origin of hydrogen induced conduction layers on diamond film is not fully understood. The hydrogen induced conductivity is usually detected on the surface of as-grown diamond films grown in a hydrogen rich plasma at temperatures above 800 °C, or is obtained by exposure of the diamond substrates to H-plasma at low substrate temperatures. It is known at these regimes both termination of the diamond surface with hydrogen atoms and diffusion of hydrogen into the diamond lattice to a depth of 20-60

nm occurs. Hydrogen termination produces a negative charge at the surface, which can even result in negative electron affinity [20].

Denisenko has suggested a hypothetical model for hydrogen-induced conductivity in diamond. It is proposed that the hydrogen-induced acceptors in diamond are separated from the surface by a separation layer characterized by a dielectric constant of $\epsilon \sim 50$ and a thickness of about 30-50 nm. This layer allows the complete depletion of the hydrogen-induced acceptors by a 0.5-1eV Schottky barrier, but prevents the tunneling through the barrier at forward biases. Also, this model implies that the surface of the separation layer contains a variety of electronic states, which produce different charge states. The charge of the related surface states can be affected by changing the atmospheric conditions, by the current flow via the self-heating of the film, or via the formation of surface dipoles in an electric field [20]. The theory suggests that the subsurface hydrogen induced acceptors might be essentially stable. Therefore, any approach to minimize the effects of the hydrogen conduction layer should be directed towards the stabilization or passivation of the surface states attributed to the separation layer and not necessarily at the terminated hydrogen atoms at the surface.

According to Hayashi *et al.* [19] hydrogen-related gap states due to the hydrogen incorporation exist in the near surface of the hydrogenated diamond films, some of which act as shallower acceptors causing the high conductivity. These preceding studies lead to the result that the presence of hydrogen in as-grown diamond films leads to a relatively low resistivity that obstructs the development of insulating applications for diamond film such as dielectrics.

Effects of Annealing

Manca *et al.* [21] observed that the leakage current of diamond film decreases by a few orders of magnitude after annealing in dry air. An irreversible resistance change occurs after the annealing. Several authors have observed this irreversible resistance change.

Heidger's experiments showed a relatively stable and consistent measurement of dielectric constant and loss tangent of annealed diamond. In contrast, the dielectric constant of as-deposited diamond films increased as the frequency decreased but remained relatively stable above 10 kHz. The loss tangent of the as-deposited CVD diamond exhibited exponential behavior, increasing dramatically as the frequency decreased and approaching the value of annealed samples as the frequency increased to 1 MHz. Marked improvements in the loss tangent and resistivity were observed with annealing the CVD diamond in air [19]. Some authors propose that the reason for the observed change in resistivity is related to either the movement of hydrogen within or out of the film. Other explanations are related to the presence of a conductive graphite layer or to upwards band bending due to an accumulation layer for holes.

Figure 4.4 shows the effects of annealing on the atomic composition of a diamond film.

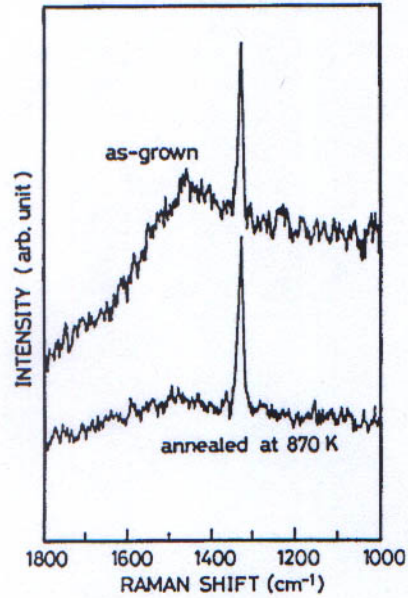


Figure 4. 4 Raman spectra for as-grown and 870 K annealed sample [22].

The sharp peak at 1333 cm^{-1} is characteristic of sp^3 diamond bonding, while the broad peak around 1500 cm^{-1} in the as-grown film is due to sp^2 -bonded carbon. This carbon component comes from graphitic material and other forms of non-diamond carbon. The secondary peak clearly disappears in the sample after annealing.

In general, the annealing process will cause geometric defects and impurity atoms to become mobile if the temperature is high enough. For diamond it is assumed that most defects and vacancies will anneal out in the $300\text{-}500\text{ }^\circ\text{C}$ range. Vacancies in the diamond lattice usually become mobile at temperatures above $600\text{ }^\circ\text{C}$. Care has to be taken, however, with the annealing process at high temperatures. As annealing temperatures reach above $600\text{ }^\circ\text{C}$ in air, diamond film enters the regime where it is susceptible to oxidation and graphitization. These temperature boundaries can be extended by

annealing the film under differing pressures, under vacuum conditions, or under different ambient gases such as argon or nitrogen.

Grain Boundaries

Grain boundary defects influence the conduction and mobility of charge carriers. The impact of grain boundary conduction has been discussed since the early days of CVD diamond development. Grain boundaries have been claimed by many researchers to be the dominant conduction path in polycrystalline diamond films. Figure 4.5 shows the grain arrangement in a polycrystalline diamond film.

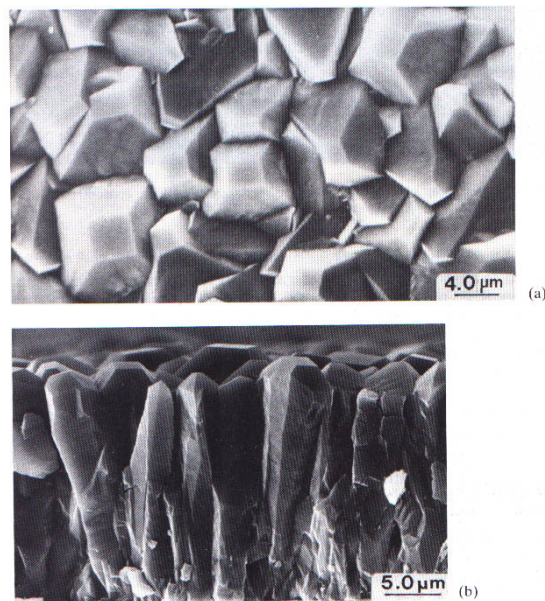


Figure 4.5 SEM micrographs of a CVD diamond film grown on a Si substrate: (a) Surface View, (b) Cross Section View [23].

Studies have shown that leakage is influenced by grain size. Controlling the density and size of grain boundaries can enhance dielectric performance.

The total area of grain boundaries increases with heating. With more grain boundaries also comes more accumulation of defects and non-diamond carbon phase impurities. Grain boundary increase is the result of lattice deformation and distortion caused by thermal expansion, thermal stress, and oxidation.

Impedance spectroscopy experiments have shown that resistivity, contributed from grain interior surfaces and grain boundaries, decreases with increase in temperature. Grain boundary impurities are not as stable as diamond grains. Impurities undergo thermal activation at around 250 °C. Typical diamond, however, does not undergo graphitization until 800 °C or greater.

Sanchez-Garrido *et al.* attribute strong low frequency dispersion to the presence and size of grain boundaries in CVD diamond and to mobility of charge carriers, namely nondiamond carbon [24]. Thermal activation of charge carriers and relaxation at the grain boundaries would increase as temperature increases, resulting in greater losses at higher temperatures. Grain boundary relaxation and/or thermal activation of nondiamond carbon species in the diamond film can explain the increase in losses at low frequency as the film increases in temperature.

Electrical Conduction Models

The electrical properties of undoped polycrystalline diamond have been investigated several times. However, the situation is not clear and different mechanisms of conduction have been invoked, like space charge limited current, Poole-Frenkel conduction, Hill conduction, or variable range hopping [25]. Several authors have performed detailed analysis of experimental results to distinguish between possible models for conduction.

The discussion of conduction modeling begins with the current-voltage characteristic $I-V$ of the diamond film. The typical $I-V$ characteristic observed for an undoped diamond film at room temperature consists of two regions. There is an ohmic region in the low-voltage range. The ohmic region is followed by a highly nonlinear (supralinear) region in the high-voltage range. The boundaries of the voltage ranges are dependent upon the quality and thickness of the film. An $I-V$ characteristic, produced by Gonon *et al.*, is shown in Figure 4.6 for $V > 0$. The $I-V$ curve is symmetric for $V < 0$. This is a typical $I-V$ characteristic for undoped polycrystalline CVD diamond films, as confirmed by the similar results of numerous other authors.

There are a variety of mechanisms that can explain the basic conduction curve. A number of possible mechanisms are listed in Table 4.1 along with the expected current-voltage relationships for those mechanisms. The mechanisms listed in Table 4.1 are bulk-related and involve the presence of deep levels in the gap [25].

The first factor that must be examined is the effect of the electrodes that are connected to the film surface. The two basic models for carrier injection at a metal-insulator interface are the Schottky emission and Fowler-Nordheim injection. The curve fittings of Figure

4.5 show that neither of these two mechanisms makes a good model for the observed I-V behavior. This theory is further supported by the fact that the I-V curve is symmetrical. Therefore, current transport and conduction due to the electrodes is not likely to be an important factor.

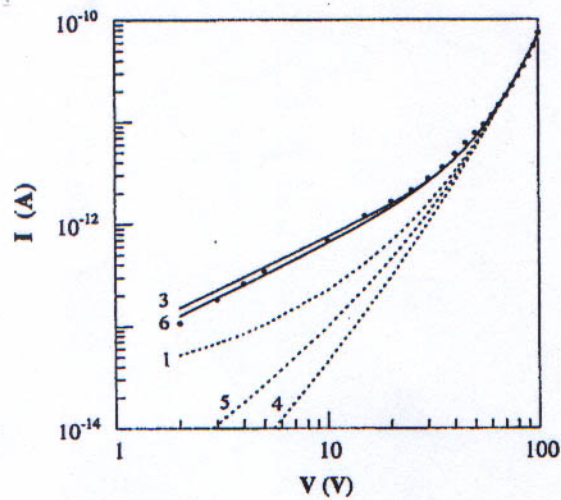


Figure 4. 6 Current vs. voltage for polycrystalline diamond films (10 μ m thick, room temperature). Experimental data (points) are fitted according to the different models listed in Table 4.1 (curves 1-6) [25].

Table 4.1 Most usual mechanisms of conduction in insulators and expected current-voltage relations [25].

Type of conduction	Current-voltage relation
(1) Schottky emission	$I \sim \exp(aV^{1/2}/kT)$
(2) Fowler–Nordheim injection	$I \sim V^2 \exp(-a/V)$
(3) space charge limited currents (SCLC)	$I \sim V$ (low fields) $I \sim V^n$ ($n > 1$, high fields)
(4) space charge limited currents with Poole–Frenkel effect	$I \sim V^2 \exp(aV^{1/2}/kT)$
(5) Poole–Frenkel conduction	$I \sim V \sinh(aV^{1/2}/kT)$
(6) Poole–Frenkel conduction with overlap of Coulombic potentials (Hill's law)	$I \sim \sinh(aV/kT)$

Based on the experimental data, two basic conduction models have been proposed. One mechanism deals with the bulk diamond grains. The other mechanism uses the grain boundaries as the primary vessel of conduction. At this time there is not enough evidence to promote one of the two alternative approaches over the other.

Poole-Frenkel Conduction

Many investigators have used the Poole-Frenkel model to interpret high-field transport phenomena in insulators and semiconductors [8]. The Poole-Frenkel effect is observed when electric conduction is bulk limited. Poole-Frenkel conduction is a conduction mechanism that involves trapped electrons or holes. The traps are generally close to the edge of the bandgap. The traps restrict the normal current flow because of a capture and emission process, which becomes the dominant current mechanism. The conduction method is dependent on the presence of an electric field. The effect of the field is to lower the potential barrier enough to allow a trapped electron to escape. In this

conduction mechanism electrons “jump” or “hop” from trap to trap under the influence of the electric field. The Poole-Frenkel effect is similar to the Schottky effect, but the amount of barrier lowering due to the Poole-Frenkel effect is twice that of the Schottky effect because the coulombic attractive force to an electron is twice as large for the Poole-Frenkel scenario. The amount of barrier lowering due to the Poole-Frenkel effect is

$$\Delta E_{pF} = \left(\frac{q^3 F}{\pi \epsilon} \right)^{1/2} = \beta F^{1/2}, \quad (4.1)$$

where β is called the Poole-Frenkel constant. This constant is material dependent.

The current is a drift current as described by

$$J = qn\mu E_N, \quad (4.2)$$

while the carrier density depends exponentially on the depth of the trap, which is corrected for the electric field. This is equivalent to the Schottky barrier lowering due to the presence of an electric field.

$$n = n_0 \exp\left[-\frac{q}{kT} \left(\phi_B - \sqrt{\frac{qE_N}{\pi\epsilon_N}}\right)\right] \quad (4.3)$$

The total current then equals:

$$J_{PF} = qn_0\mu E_N \exp\left[-\frac{q}{kT}\left(\phi_B - \sqrt{\frac{qE_N}{\pi\epsilon_N}}\right)\right] \quad (4.4)$$

Poole-Frenkel emission is a frequently observed and well-characterized conduction mechanism in other CVD materials such as CVD silicon nitride.

There are many other modifications of the original Poole-Frenkel model based on various assumptions, such as those by Hartke, Hill, Antula, and Adamic and Calderwood [8].

The band diagram of Figure 4.7 illustrates the one-dimensional model of the Poole-Frenkel effect.

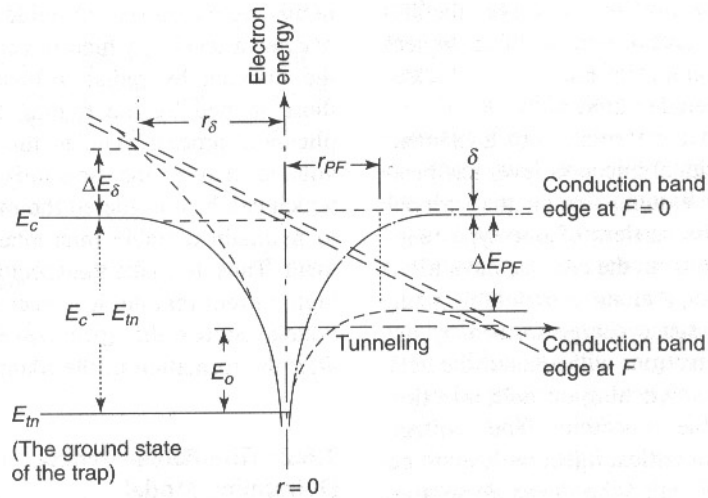


Figure 4. 7 Schematic diagram illustrating the Poole-Frenkel effect [8].

Poole-Frenkel Conduction in Diamond Films via Hill Conduction

As shown in Figure 4.6, Hill-type conduction is a possible mechanism to explain the field, temperature, and low frequency dependence of conductivity in polycrystalline diamond films [17]. Hill conduction is essentially a hopping conduction process that is nonlinear at high electric fields. Work by Gonon [25] showed that the Hill-type hopping conduction can be related to the presence of discrete acceptor states located at approximately 0.91 eV above the valence band. For Hill-type conduction, the loss tangent and conductivity are frequency dependent. It follows a power law ω^p , where p is frequency and temperature dependent.

For this relationship p is given by

$$p = 1 - \frac{6kT}{[E_i + kT \ln(\omega\tau)]}, \quad (4.4)$$

where τ , ($\tau \approx 10^{-13}$ s for diamond), is the inverse of a phonon frequency and ω is the frequency of measure. This frequency dependence helps to explain the loss tangent results reported in the Ibarra experiments (see Section 4.3.2).

Hill conduction is a subset of the Poole-Frenkel mechanism. Specifically, this conduction mechanism involves discrete energy levels located at E_i from the conduction band. For these states there is sufficient overlap of Coulombic potentials to allow carriers to hop from site to site. Carriers hop over a potential barrier E_p given by:

$$E_p = E_i - \frac{\beta^2}{es}, \quad (4.5)$$

where s is the distance separating two centers, and $\beta = e^{3/2}(\pi\epsilon\epsilon_0)^{-1/2}$ is the Poole-Frenkel constant for the material (for diamond $\epsilon = 5.5$ and $\beta = 3.23 \times 10^{-4} \text{ eV V}^{-1/2} \text{ cm}^{-1/2}$) [25].

Photoconductivity experiments by Gonon, Sugino, and Okumura [22,25] show that the conduction states are probably electron acceptor sites at $E_i \approx 0.9 \text{ eV}$, and since this type of hopping conduction requires the states to be partially filled, the Fermi level should also be located at E_i .

Evidence that the Hill/Poole-Frenkel conduction is related to the bulk diamond film comes from the analysis of annealing behavior. It has already been established that thermal annealing works by neutralizing the conduction effects of hydrogen in the film. Figure 4.8 shows the I - V characteristics of diamond films under various annealing and hydrogenation profiles as reported by Muto *et al.*

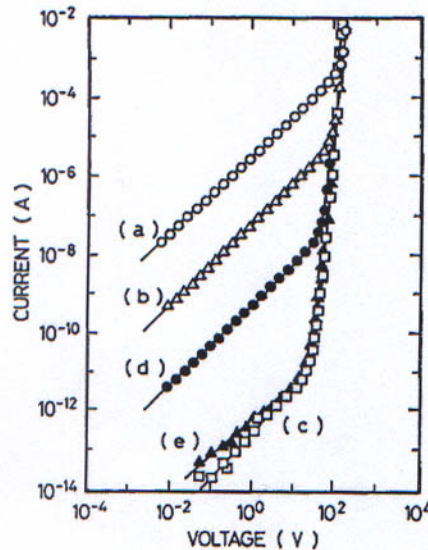


Figure 4.8 I - V characteristics at room temperature. Curve (a) as-grown, (b) annealed at 570 K, (c) annealed at 673 K, (d) hydrogenated after the annealing at 670 K, and (e) annealed at 670 K after hydrogenation [22].

The hydrogenation is performed to “reverse” the affects of the annealing process. By introducing the film to hydrogen plasma for a number of hours, hydrogen is reintroduced to the film. The temperature is slowly lowered room temperature, which suppresses the removal of the hydrogen from the film. The effective result is to nullify, in whole or in part, the effects of any prior annealing. It can be seen in Figure 4.8 that the nonlinear portion of the I - V characteristic at high voltages is essentially independent of the history of the sample. Regardless of the history, the sample retains the same basic I - V shape. For the Hill conduction model, this can rule out surface or grain boundary conduction as conduction contributors.

Hopping Conduction and Space Charge Limited Current

As shown in Figure 4.6, the experimental I - V data of the Gonon experiments can also be fitted with a function of the form $I=aV+bV^n$. This fit corresponds to an ohmic component at low electric fields, and an exponential component V^n that dominates at higher fields. Referring to Table 4.1, this corresponds to the space charge limited current model.

Variable Range Hopping Conduction

In the ohmic range, the conductivity in the diamond film is not strongly dependent on temperature. This weak temperature dependence indicates that the conductivity is due to a mechanism that arises from either the activation of shallow level energy states or from a tunneling behavior. Figure 4.9 shows the relationship between conductivity and temperature when plotted as a function of $T^{-1/4}$.

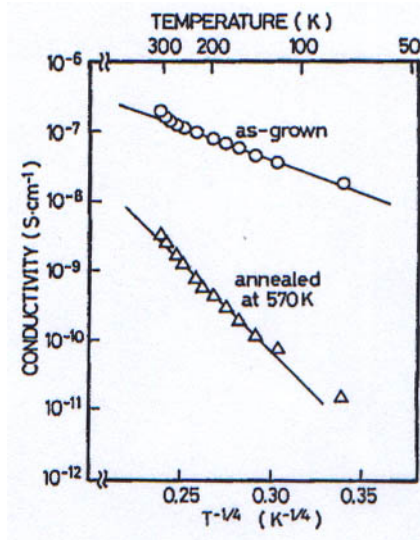


Figure 4.9 Logarithmic conductivity vs. $T^{-1/4}$ in the ohmic region for as-grown and 570 K annealed diamond film samples [22].

The as-grown sample strongly obeys the $T^{-1/4}$ law at low temperatures, while the annealed sample does not. This is consistent with phenomena of variable range hopping (VRH) conduction that is often seen in amorphous semiconductors with dense localized defects. Mott [22] described the proportionality of the logarithm of resistivity to $T^{-1/4}$ to be a clear indicator for impurity conduction due to electron hopping.

A localized electron can drift through a solid specimen by hopping from a molecule (or an atom) to a nonoccupied state of a neighboring molecule if it acquires the energy necessary to overcome the potential barrier. In general, the energy is from thermal excitation of the material. The concept of hopping transport has been familiar for a long time with ionic conduction. The concept

has also been extended to electronic conduction in amorphous and disordered nonmetallic solids [8].

In the case of polycrystalline diamond films, the impurities that are the sources of the localized defects come from the highly disordered regions of the grain boundaries. Figure 4.10 illustrates the hopping concept.

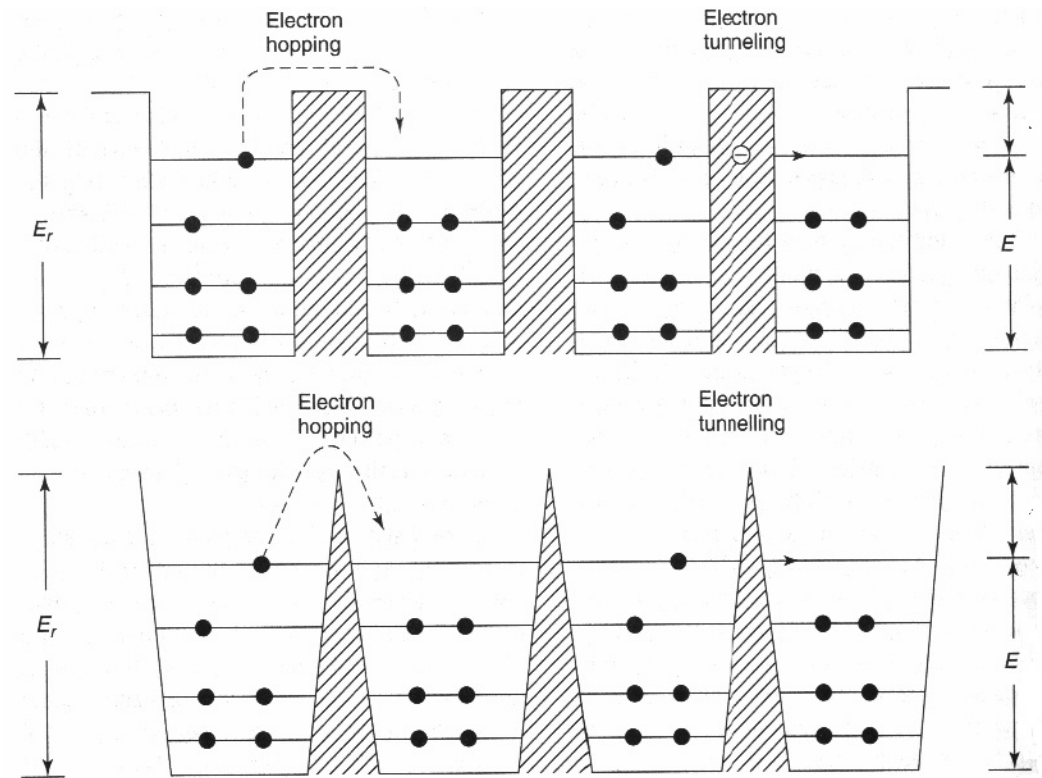


Figure 4. 10 Schematic diagrams illustrating an electron hopping across and an electron tunneling through a square and a triangular potential barrier [8].

Both the distance between the two sites and the potential barrier that must be overcome may determine the probability of a hopping transition. If the distance between the two sites is larger than 10 \AA , electrons will hop rather than tunnel

from site to site [8]. According to Mott and Gonon [25-26] the hopping distance for CVD polycrystalline diamond is approximately 400 Å at 300 K.

The lack of $T^{-1/4}$ correlation of the annealed sample of Figure 4.9 supports the VRH theory since the annealing process leads to the partial removal of the disordered graphitic material that exists between the diamond grains. It can also be seen in Figure 4.9 that the substantial decrease in conductivity of the annealed sample would coincide with the disappearance of the variable range hopping conduction. VRH conduction also can be expected to vary with frequency as shown by Fiegl *et al.*. The VRH mechanism operates according to a ω^p law with p given by:

$$p = 1 + 4 / \ln(\omega\tau). \quad (4.6)$$

This is consistent with the earlier noted frequency observations.

Space Charge Limited Current Conduction

The V^n dependence at higher electric fields indicates that the diamond film may conduct via space charge limited currents (SCLC) in this range.

Space charge conduction occurs when the contacting electrodes are capable of injecting electrons into the conduction band or holes into the valence band of a semiconductor or an insulator, and when the initial rate of such charge-carrier injection is higher than the rate of recombination, so the injected carriers will form a space charge to limit the current flow. The SCLC is therefore limited to the bulk of the material [8]. Figure 4.11 illustrates this concept.

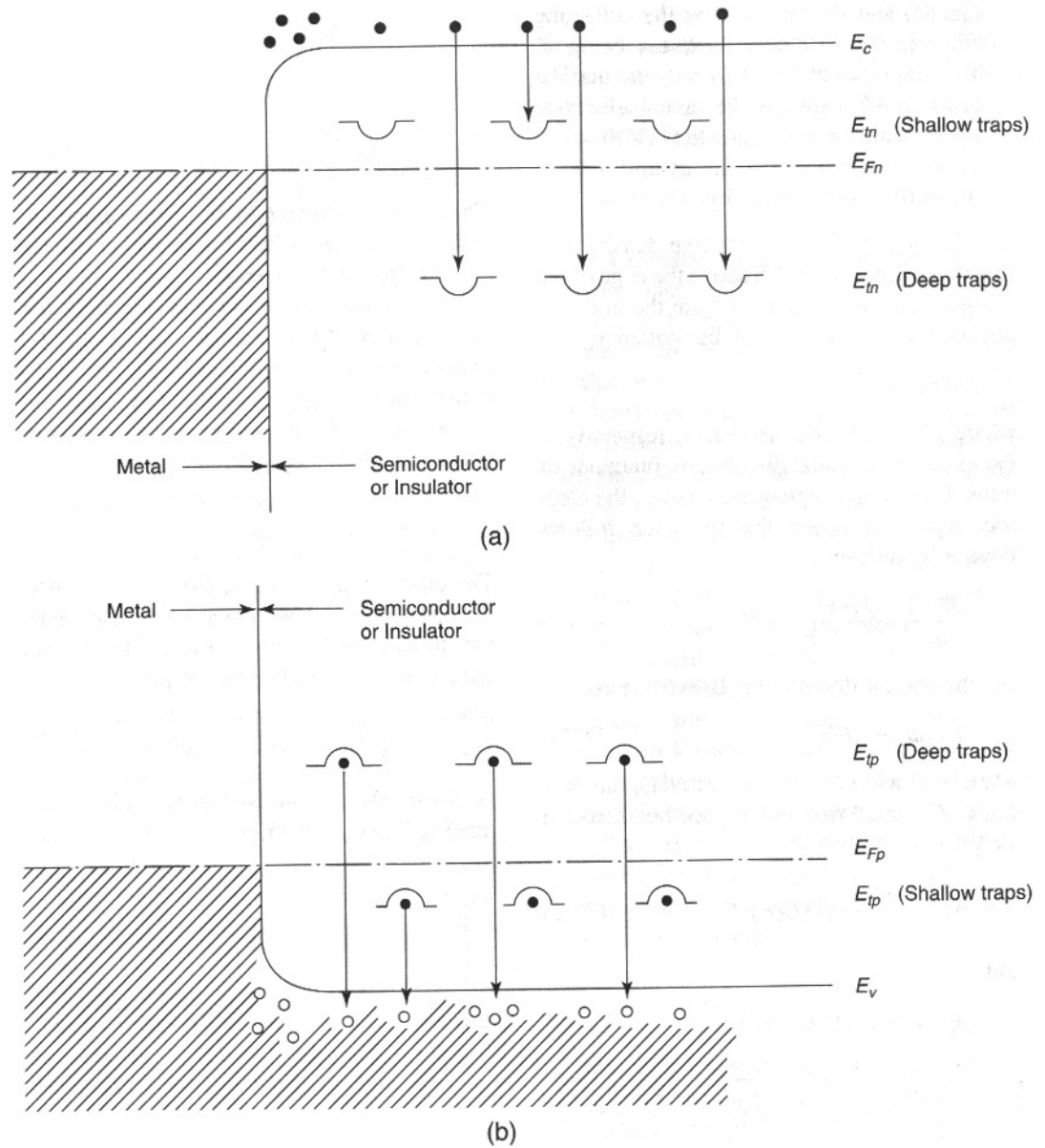


Figure 4. 11 Schematic energy level diagrams for (a) electrons and (b) holes injecting from an ohmic contact to a semiconductor or an insulator with shallow and deep electron or hole traps [8].

In wide bandgap materials, the carrier mobility is low and the intrinsic resistivity is high. SCL current is often observed in these materials even with poor carrier injecting contacts because the intrinsic resistance of the material is usually much higher than the contact resistance. For crystalline materials, there are always traps that are created by impurities and imperfections. These traps will interact with carriers injected from ohmic contacts to the material and thereby control the carrier flow. The material thickness is also of importance. The thinner the material, the more influence that there will be from the distribution of traps in the material. Thin films are especially subject to this fact because of surface topography, grain boundaries, nonuniform doping, microcrystalline defects, etc. [13]. These factors will ultimately determine the current-voltage characteristics for the material.

Experiments by Mort and Ashhok have shown that there are band-tails with high densities of states near the valence band of polycrystalline diamond. In order for SCL currents to be involved, it is assumed that there will exist a band-tail with a high density of states increasing exponentially towards the valence band. Amorphous and polycrystalline materials have trap energy levels that are distributed in accordance with certain distribution functions. Defect traps in polycrystalline materials, therefore, are generally distributed and have a rather high density, even if the material itself is chemically pure [8]. The densities of states found in the Mort and Ashhok experiments are on the order of 10^{15} - 10^{20} cm^{-3} . While these densities of states are on par with what can be found in amorphous materials, they are considered too high to be consistent with the

number of states that would be expected to exist in the bulk of the diamond grains. The grain boundaries and the highly disordered regions therein, however, can reasonably support such a density of states. Therefore, space charge limited current can exist in polycrystalline diamond as a conduction mechanism provided that the conduction occurs in the grain boundary regions.

Temperature

As has been discussed in the previous commentary, temperature plays a pivotal role in the characterization of diamond films. When compared together, leakage current depends weakly on applied voltage and strongly on temperature. Experimental data has shown a several order of magnitude variance in resistance over the range of 100 °C to 500 °C. Bulk resistance of diamond film decreases with increasing temperature. Dissipation factor of diamond is significantly lower than other insulators, such as glassy ceramics, at lower temperatures (<300 °C). Heating diamond in air or vacuum, even at relatively low temperatures, will likely alter the surface termination of the film. The resulting change in surface termination can produce an increase in resistivity and improved temperature stability of the dielectric properties. Mackey *et al.* observed that hydrogen-terminated diamond surfaces have lower sheet resistance than oxygen-terminated surfaces [27]. CVD diamond is susceptible to the effect because the surfaces of as-deposited CVD diamond samples have primarily hydrogen-terminated bonds. It has been shown that the oxygen content of the surface of diamond film typically increases with annealing, corresponding to improved thermal stability of the dielectric constant and loss tangent and increased resistivity.

In contrast to single crystal diamonds that remain stable in vacuum up to 1700 °C, an internal graphitization, predominately at grain boundaries, may take place in polycrystalline CVD diamond at lower temperatures, leading to profound modifications of the material structure [28].

CHAPTER V

ANALYSIS OF CONDUCTIVITY MECHANISMS IN CVD DIAMOND

Conductivity is the single most important electrical property of a dielectric material. Without the ability to polarize or block the flow of electrical current, a material is fundamentally useless as a dielectric. For this reason, a great deal of effort has been utilized to test and observe the conductivity of CVD diamond films. As mentioned previously, a number of factors can contribute to the effective ability of a dielectric material to resist electrical conduction. These include thickness, surface conduction factors, grain boundaries, and temperature. In order to properly select CVD diamond films that are suitable for capacitive applications, a number of testing procedures have been employed.

Characterization Methods

I-V and resistivity tests were conducted using a Keithley 6517A Electrometer and a custom-built test chamber. The spring-loaded test chamber was constructed with brass electrodes and an electrically inert, acrylic housing. It was designed to both provide solid contact for the samples under test and be versatile enough to be used for other experiments such as resistivity and capacitance. An earlier version of the chamber, as shown in Figure 5.1, vertically positioned the test sample. This design, while useful for many devices, was not able to adequately provide consistent contact pressure for thin structures. External pressure had to be applied to make the electrical contact solid and

repeatable. The chamber was redesigned, as shown in Figure 5.2, to horizontally position the sample under test. The spring was included in the new design to give consistency and repeatability to the contact pressure experienced by the electrodes.

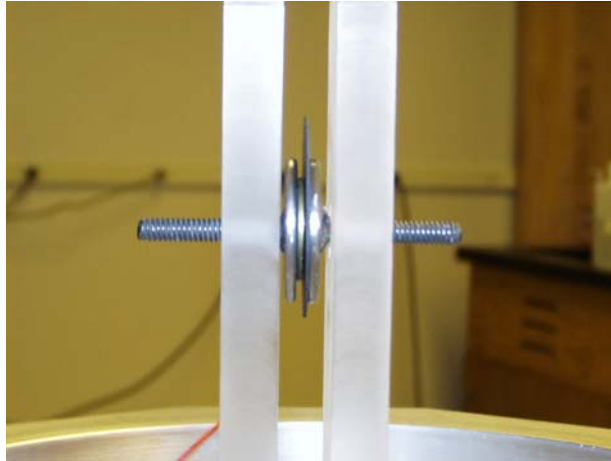


Figure 5.1 First generation custom test chamber with diamond film under test.



Figure 5.2 Second generation custom test chamber with diamond film sample.

Frequency dependent measurements (capacitance, dissipation factor, ESR, CV) were made using a HP 4275A Multi-Frequency LCR Meter.

Charge-discharge behavior was measured using a HP 54600B Oscilloscope. The sample was placed in series with a resistor to create an RC circuit. By using a HP 33120A Waveform Generator, the capacitor could be pulsed and thereby charged and discharged. The resulting waveform could then be examined to determine charge-holding ability and RC time constant (τ) of the sample. Experiments on the charge holding ability of samples had not been explored previously. Some samples, while exhibiting acceptable current leakage behavior or capacitance values, did not show the ability to adequately hold an electrical charge. These samples were normally eliminated from consideration as viable capacitor candidates. Of the samples under consideration that were scrutinized in this manner, approximately 70% displayed evidence of the ability to adequately hold an electric charge.

Non –Silicon Substrates

Most experiments relating to the development of CVD diamond dielectric devices were performed using silicon as the substrate material. Silicon has become the substrate of choice for the growth of polycrystalline CVD diamond films — mainly due to its easy availability, high quality and good growth characteristics for diamond. However, it has several disadvantages for use in the industrial production of diamond films, which encourage the investigation of alternative substrate materials. For example, the economical production of free-standing films requires high-power, high-growth-rate CVD systems that typically result in thermal fluxes to the substrate of many kilowatts.

This can produce severe thermal gradients in the substrate requiring careful thermal management to avoid compromising film quality. The modest thermal conductivity of silicon ($84 \text{ W m}^{-1} \text{ K}^{-1}$) limits the maximum power that can be used in such deposition systems. Additionally, to produce free-standing diamond films, it is necessary to chemically etch away the silicon. This destroys the substrate and has both environmental and cost consequences for the production process.

Diamond is known to nucleate well on suitably pretreated carbide-forming substrates, of which silicon is one. The refractory metals (e.g. tungsten, molybdenum, niobium, etc.) are also carbide-forming materials and benefit from high thermal conductivities and high strengths that can reduce substrate thermal management problems and substrate warpage — both of which can occur during growth on silicon [43].

With this knowledge a series of experiments were conducted using alternative substrate materials – molybdenum and tungsten specifically. These experiments were aimed at producing high quality dielectrics that were not subject to some of the mechanical concerns found with thin layer diamond on silicon.

Thin-Layer Diamond on Tungsten

The first experiment was designed to produce a thin layer diamond dielectric. With a single layer, the capacitance per unit area is inversely proportional to the thickness of the dielectric material. Tungsten, as shown in Figure 5.3, was chosen as the substrate for this series of tests. Three samples (Sample A, Sample B, Sample C, Sample D) were produced. Films were deposited using an ASTEX CVD microwave reactor under standard processing conditions (Pressure - 40 Torr, Temperature – 850 °C, Power - 1500

W, 1% CH₄ in H₂). The growth time was varied amongst the samples, but not enough to invalidate the thin film (<15 μm) requirement. Figure 5.4 shows the leakage profiles for three of the tungsten samples. Sample D was not subjected to leakage testing.

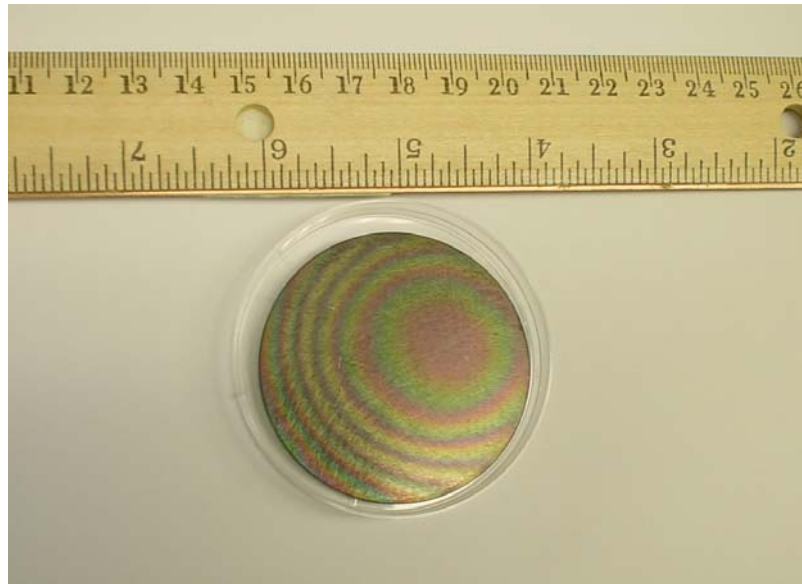
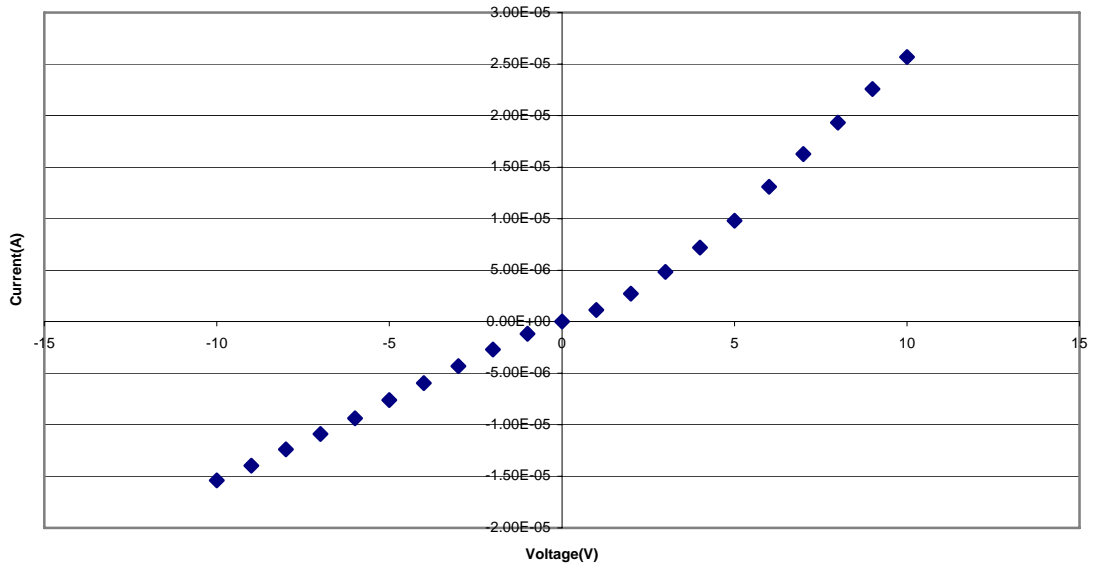


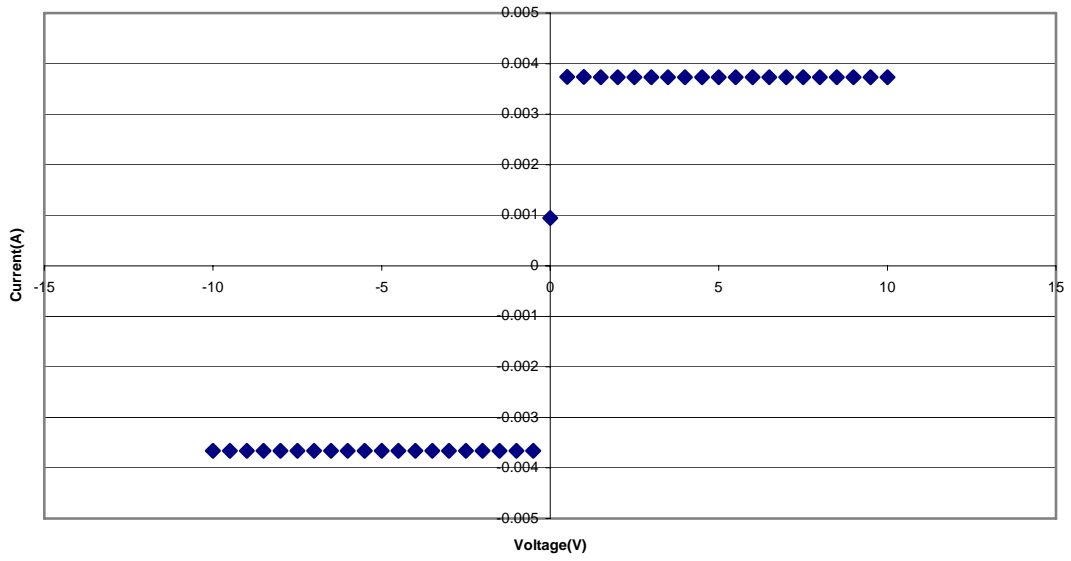
Figure 5.3 Thin diamond layer on tungsten substrate.

I vs. V - Sample A (Small Metal Plate Testing)

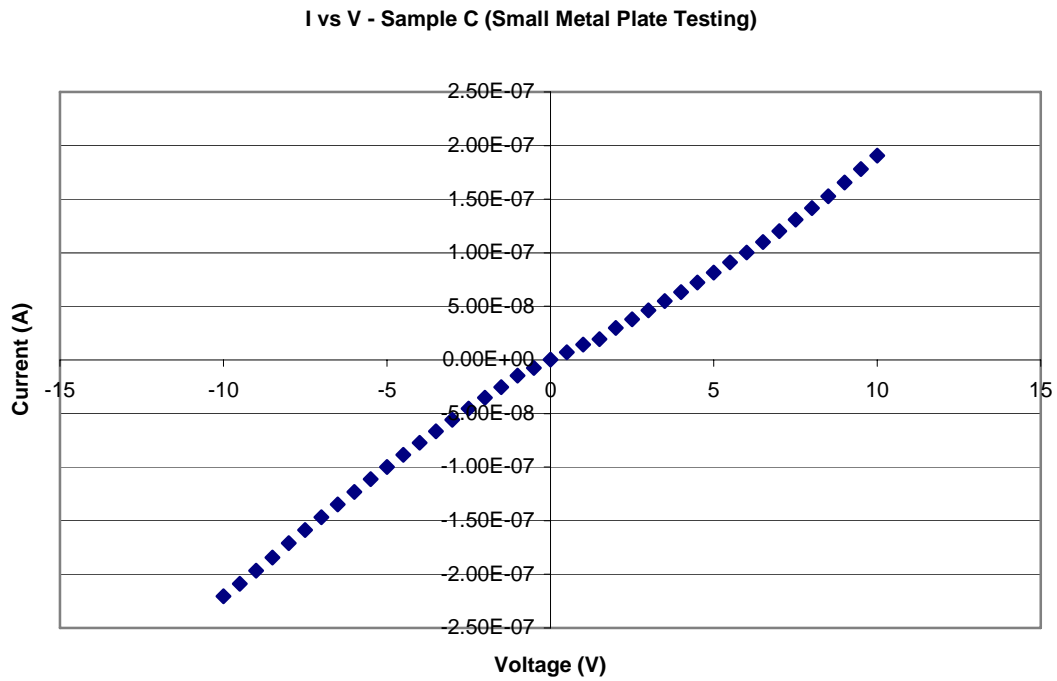


(a)

I vs. V - Sample B (Small Metal Plate Testing)



(b)



(c)

Figure 5.4 Leakage current measurements of thin diamond layer on tungsten substrate: (a) Sample A, (b) Sample B, (c) Sample C.

The figures clearly indicate a resistive relationship. The samples all proved to be conductive, even at low voltages.

It has been well documented that structural defects can develop between the diamond-tungsten interface following the growth process. After the structure is removed from the deposition reactor and cools, the difference in thermal coefficients between the diamond and tungsten can lead to delamination or breaking. These compressive stresses have been estimated to exist in the GPa range and can easily lead to cracks or exacerbate the influence of pinholes, especially in the case of thin films. For this reason, tungsten has been explored as a viable substrate for the production of freestanding thick diamond films, and successful attempts have been made in this regard. However, for capacitive

applications, where it is preferable to use thin layer diamond, the mechanical limitations of the diamond-tungsten interface have yet to yield acceptable results.

Thick-Layer Diamond on Molybdenum

In the wake of the tungsten experiments, molybdenum was tried as a substrate. Two samples were grown, Moly 1 and Moly 2. For the molybdenum samples, a thicker diamond film was used. By using a thicker film, the interface problems experienced with the tungsten samples could be avoided. Since the conductivity is the most important parameter in dielectric characterization, it was decided to tradeoff high capacitance in favor of low leakage. The thicker film would also increase the power handling capacity of the dielectric.

The samples, as shown in Figure 5.5, were grown for longer time intervals to allow for thicker films. Sample Moly 1 was grown for over 20 hours. Sample Moly 2 was grown for over 3 days.

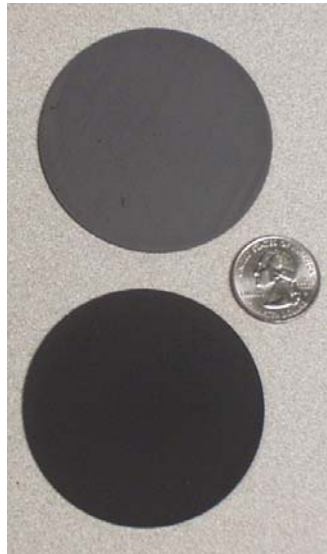


Figure 5.5 Thick layer diamond on molybdenum substrates, Moly 1 (above) and Moly 2 (below).

Leakage Profile - Sample Moly 1

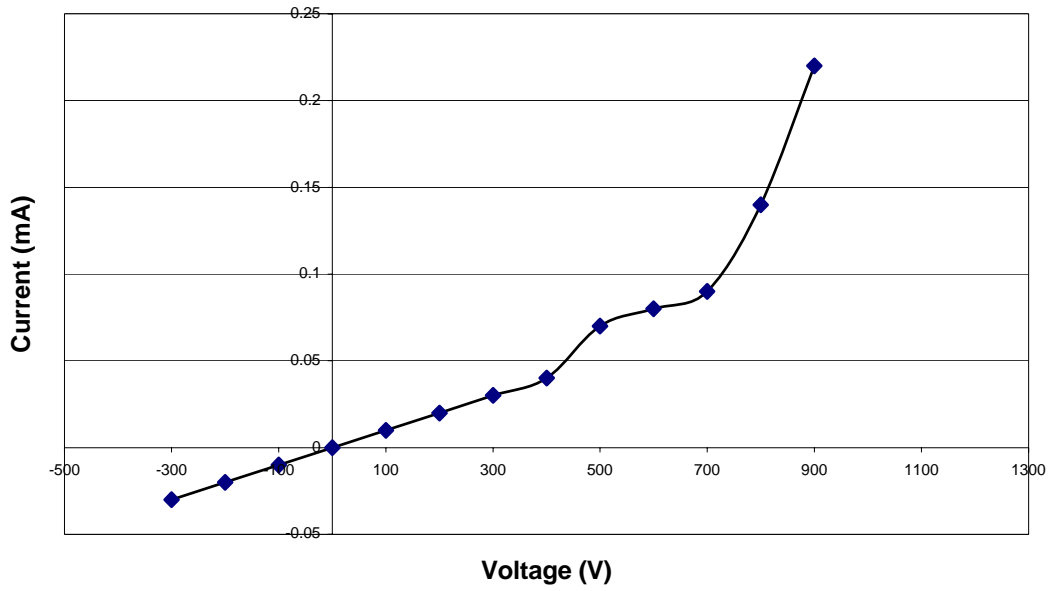


Figure 5.6 I-V characteristic for thick-layer diamond on Mo sample Moly 1.

Leakage Profile - Sample Moly 2

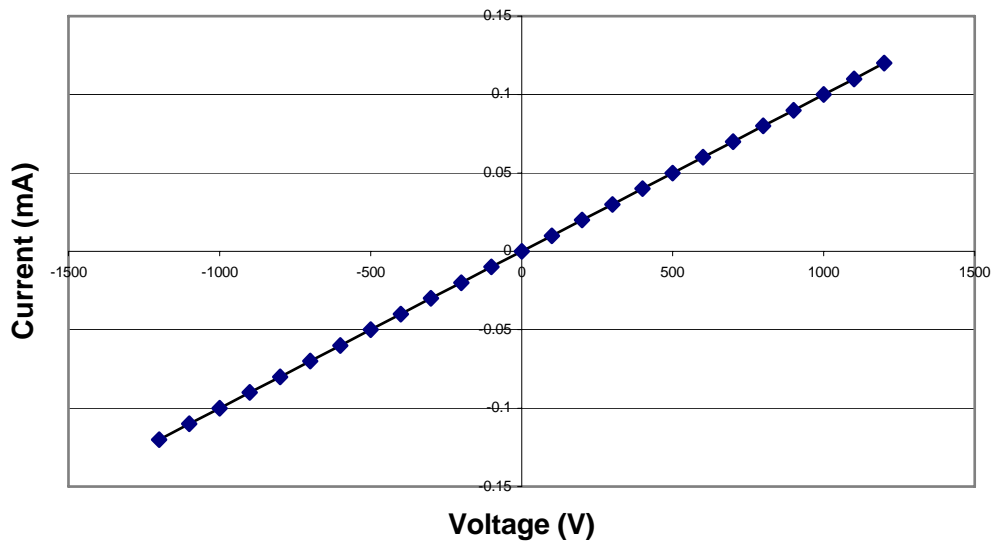


Figure 5.7 I-V characteristic for thick-layer diamond on Mo sample Moly 2.

After deposition, both samples were subjected to initial leakage characterization via multimeter. When measured with a multimeter, both samples showed no surface conductivity. Measurement of the bulk leakage was performed via I-V characterization, as shown in Figures 5.6 and 5.7. The leakage characteristic of Moly 2, as shown in Figure 5.7, shows a definite linear relationship. The leakage profile of Figure 5.6, however, has a shape similar to the typical diamond leakage characteristic as described earlier. A curve-fit of the leakage profile of Moly 1 can be seen in Figure 5.8.

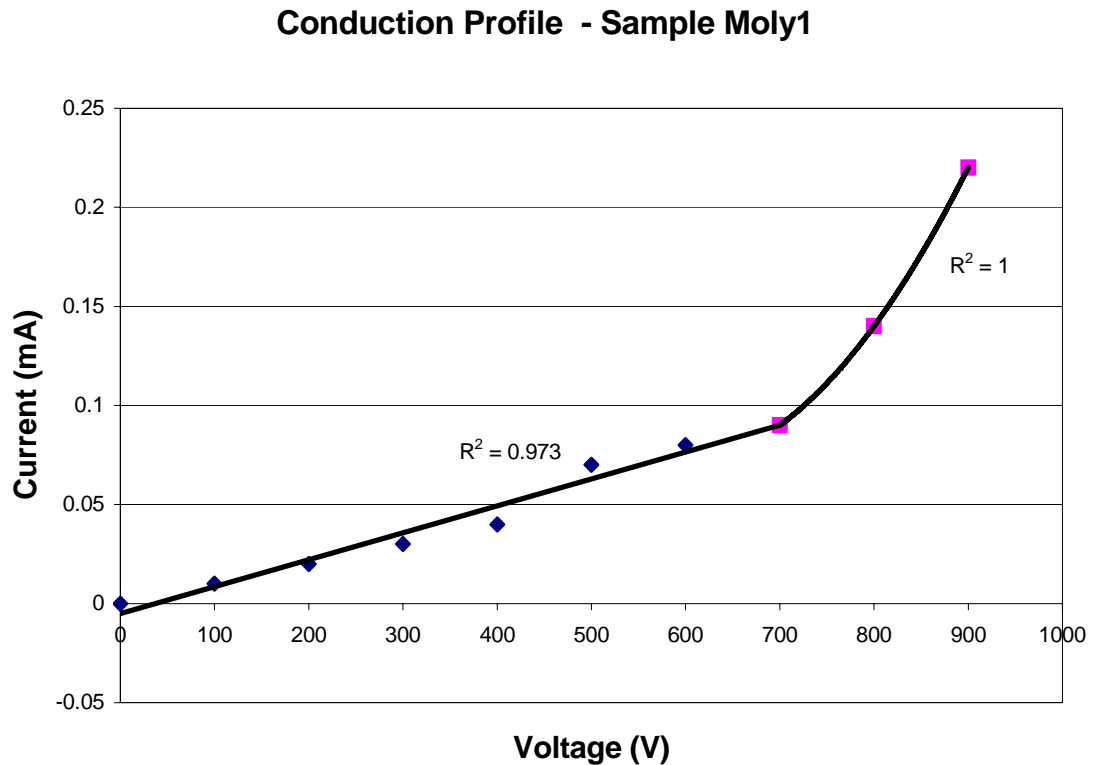


Figure 5.8 Curve-fit of leakage profile for sample Moly 1.

The conduction profile strongly correlates, as evidenced by the high R^2 values, with the previously reported (see Chapter IV) characteristic profile for dielectric diamond. Both

regions of the profile (linear and non-linear) correlate well with a $I=aV+bV^n+c$ relationship, indicating the presence of space charge limited currents as the conduction mechanism.

Because of the shorter growth time, Moly 1 had the thinner dielectric of the Mo samples. It was still, however, a thicker dielectric in comparison to other attempts on W or Si substrates. It is known that diamond deposition at high temperatures causes damage to the molybdenum structure [48]. Researchers have observed that without very careful surface preparation prior to deposition, diamond films have a tendency to peel away from the Mo substrate due to structural damage of the substrate at CVD deposition temperatures. This is especially true for thin diamond films. The failure of Moly 2 can be attributed to the extended exposure of the Mo substrate to the harsh CVD deposition environment. Moly 1 proved to be a successful candidate for dielectric applications requiring high power.

Effects of Annealing on Conductivity

The surface conduction of hydrogen on diamond films is of great importance in dielectric applications. Regardless of the quality of film produced, hydrogen surface conduction can severely retard the dielectric properties of CVD diamond. Much work [19,21,22,49] has been done on the enhancement of film conductivity parameters through the process of thermal annealing. Based on characteristics of CVD diamond films, it was postulated that post fabrication high-temperature annealing in the absence of hydrogen would reduce leakage currents at high voltage. Allowing entrapped hydrogen from the growth process to diffuse out would reduce charge-trapping sites that promote carrier “hopping” at high

fields by neutralizing the surface accumulation layer responsible for the conduction. Studies have shown that thermal annealing in air or other ambient gases at atmospheric pressures produces the best results. Figure 5.9 shows the differences observed between the reduction of surface conductivity of diamond annealed in vacuum and air, as reported by Foord.

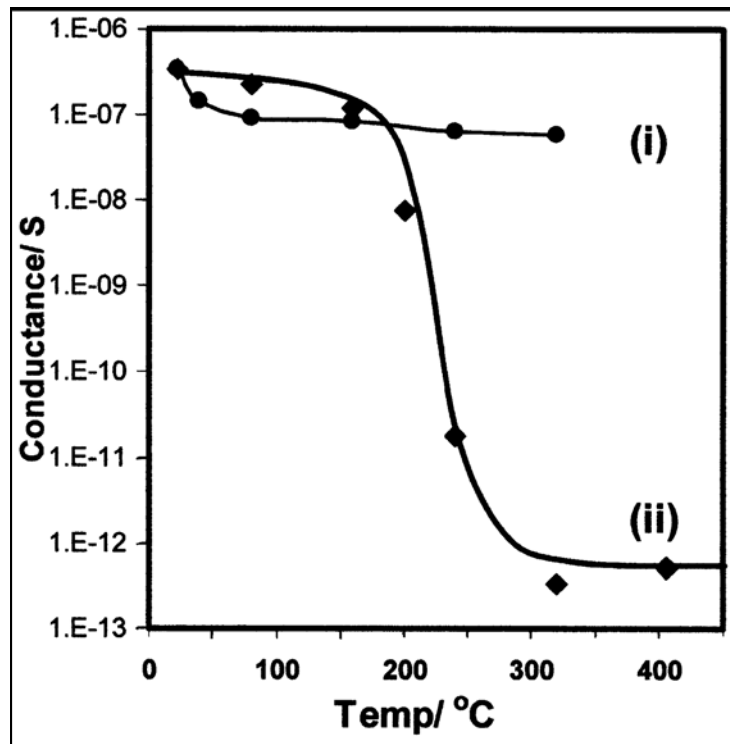


Figure 5. 9 Influence of annealing on surface conductivity. 300 K conductivity after sample annealing in vacuum (i) and air (ii) [49].

Figure 5.10 shows the I-V profile for a typical candidate sample of diamond deposited on silicon. The diamond film had exponentially increasing current leakages at high fields. While the sample did show a classic diamond I-V profile, the effective operational

voltage was limited to approximately 75 V. The sample was subjected to a series of thermal anneals to examine the effect on dielectric behavior.

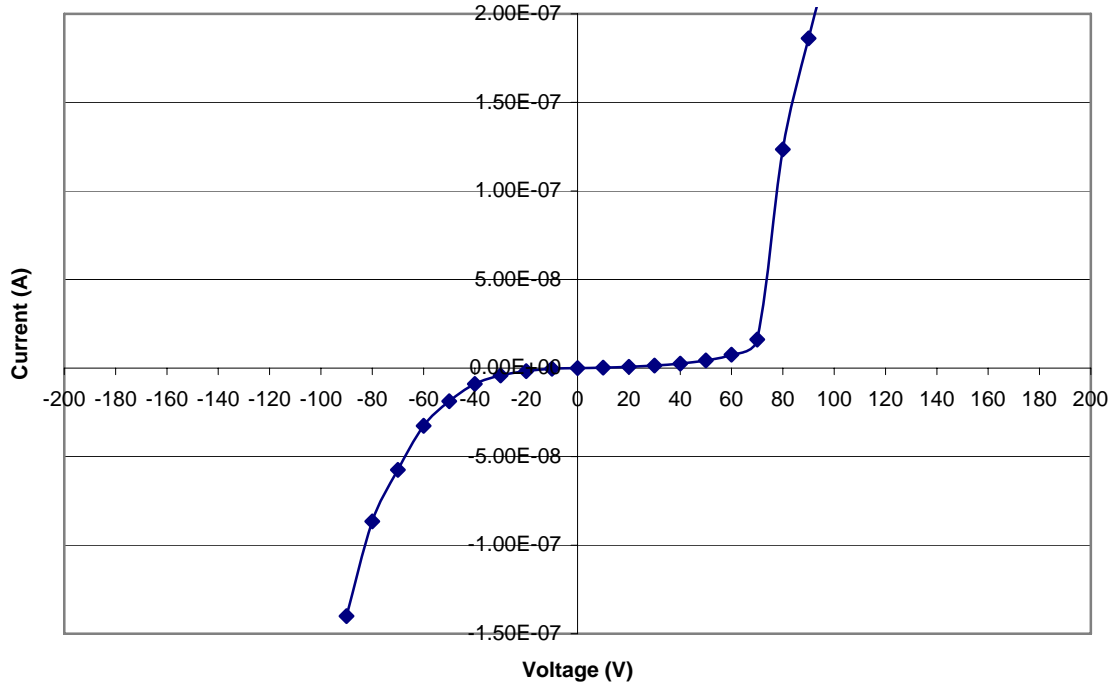


Figure 5.10 Pre-annealing I-V profile of as grown diamond dielectric film sample.

Thermal annealing was performed using a Heatpulse 210 Rapid Thermal Annealer (RTA). The sample was annealed at 1000 °C for various time periods, ranging from 60 s (Anneal 1) to 240 s (Anneal 4). To reduce the chance of oxidation of the diamond film at this temperature, the process was performed in a nitrogen ambient environment. The I-V behavior is clearly influenced by the annealing process. A comparison of the leakage profiles for the sample after the annealing process is shown in Figure 5.11.

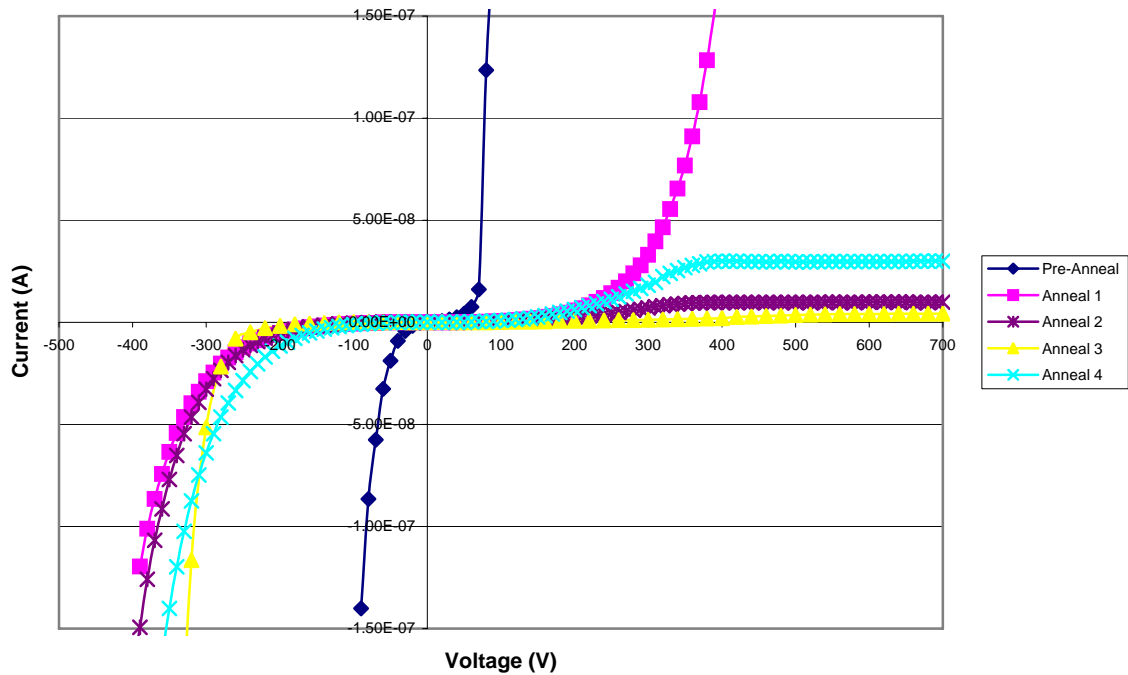


Figure 5.11 I-V annealing profile of diamond dielectric film sample.

As the annealing time is increased the leakage current is reduced. The pattern was true for the first three recorded anneal periods. A regression in the leakage is observed after the fourth anneal. At that point a threshold time may have been reached at which time substantive changes, such as oxidation, may have occurred in the diamond film. The profiles for longer anneals did not extend into the non-linear regime. This was because it was not desirable to stress the film to the point of potential failure. It can be inferred from the evidence, however, that the leakage currents would not have entered into a non-linear phase until the voltages had extended beyond 1000 V.

Closer examination of the first anneal, as illustrated in Figure 5.12, shows that the pre- and post-annealing curves retain the same conduction profile. After annealing, the profile shifts downward as the leakage current lessens for a given voltage. This trend mirrors the annealing results reported by Muto (Figure 4.8).

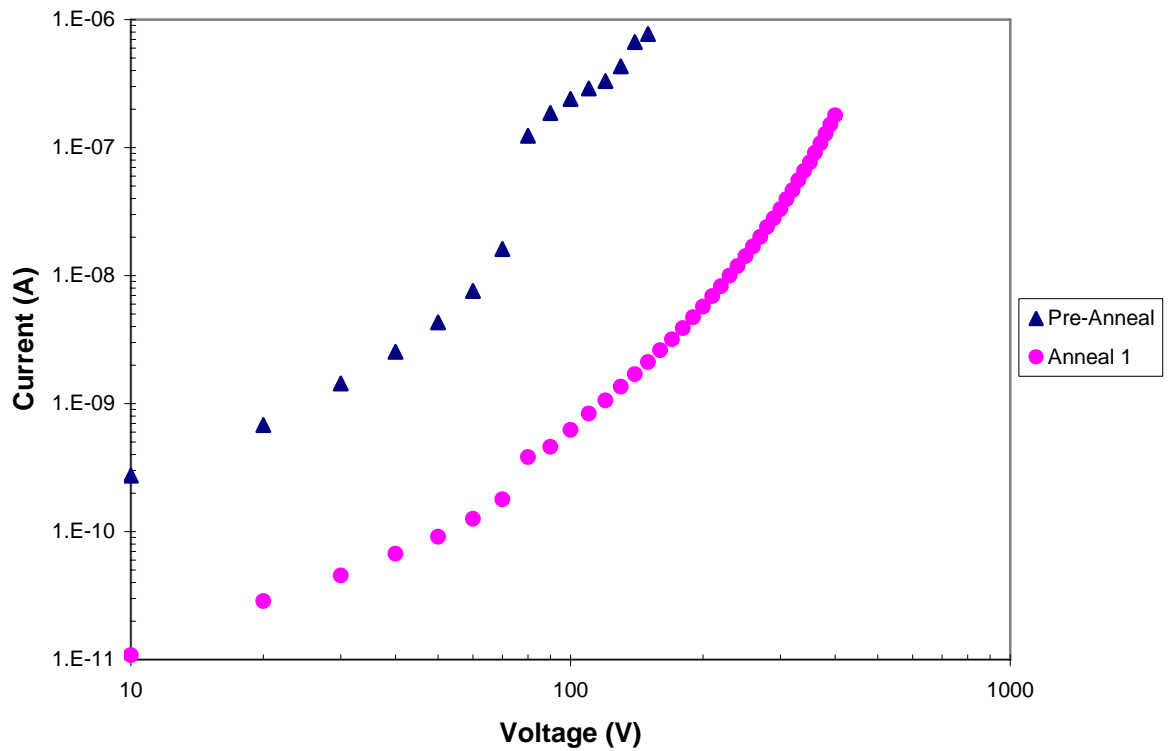


Figure 5. 12 Comparison of conduction profile for pre-annealed and post-annealed diamond dielectric sample.

The issue of surface conduction is further influenced by environmental conditions. It has been observed by Vanderbilt researchers that exposure to air increases the conductivity of diamond film over time. The fact that the effect is reversible indicates that the change in conductivity is related to surface effects rather than bulk conduction mechanisms. Qualitatively, it has been observed that a nominally non-conductive diamond film exposed to atmosphere for a prolonged period of time will begin to exhibit conductive behavior. By annealing the sample at low temperatures for long periods (500 °C, 30+ minutes) or at high temperatures for short periods (800 °C - 1000 °C), the film will return to a non-conductive state. The reversal, however, is not permanent, as repeated air exposure will continue to increase the conductivity of the film. These observations

follow closely with the theory that high surface conductivity is not merely a result of a hydrogenated film surface, but that the hydrogenated surface is affected by exposure to the atmosphere.

By masking a sample of diamond film and removing the hydrogen of the exposed half via an electron beam irradiation technique while under ultra-high vacuum (UHV), Maier [50] showed that the removal of hydrogen from the diamond surface decreases the surface conductance of the film. Under UHV the conductance of both halves of the sample remained low. After exposure to air, however, the surface conductance of the masked half increased by four orders of magnitude. Maier's findings are illustrated in Figure 5.13. After prolonged exposure to air, the conductance would eventually reach a saturation value.

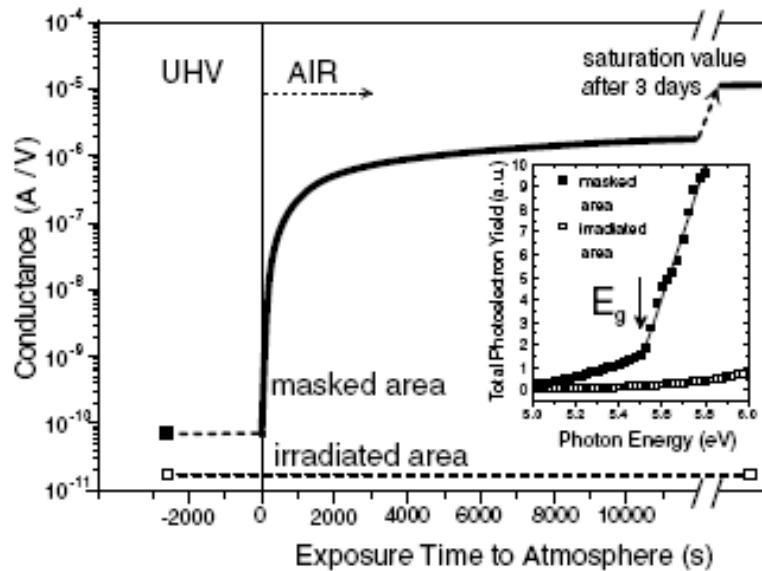


Figure 5. 13 Surface conductance of the hydrogenated (masked) and the hydrogen-free (irradiated) part of a homoepitaxial diamond (100) layer in UHV and during exposure to air. The inset shows the total photoelectron yield spectra of the two halves before exposure to air [50].

A look at the hydrocarbon species as diamond is annealed in air, Figure 5.14, shows that the C-H bonds have been broken at temperatures above 200 °C. For this reason it is common to assume temperatures above 250 °C as adequate for thermal annealing in air. It can also be assumed that hydrocarbon adsorbates are not responsible for high surface conductivity after the annealing of diamond films. For the example of Figure 5.14, it can be deduced that the presence of hydrogen termination is necessary for high surface conductivity, as evidenced by the fact that the surface conductance is high while the C-H bonds are present.

Maier's studies show that an adsorbate from the atmosphere on the hydrogen-terminated diamond surface is required to induce the surface accumulation layer responsible for high surface conduction. The band gap of diamond seemingly makes direct electron transfer from the diamond surface to the atmosphere impossible. However, a thin water layer, as it forms naturally on most surfaces exposed to atmosphere, provides an electron system that can act as a surface acceptor for diamond. Electron exchange from diamond to the water layer is governed by the redox reaction $2\text{H}_3\text{O}^+ + 2\text{e}^- \rightleftharpoons \text{H}_2 + 2\text{H}_2\text{O}$ [51].

The reaction is driven by the difference in the chemical potential of electrons in the liquid phase (μ_e) and in diamond (Fermi level E_F). As long as μ_e is below E_F , electrons are being transferred from diamond to the water layer and thereby reduce H_3O^+ to H_2 and H_2O . The compensating holes in the diamond form the accumulation layer and the associated space charge induces a potential (surface band bending) that raises μ_e [50]. At equilibrium μ_e and E_F are equal at the interface as shown schematically in Figure 5.15.

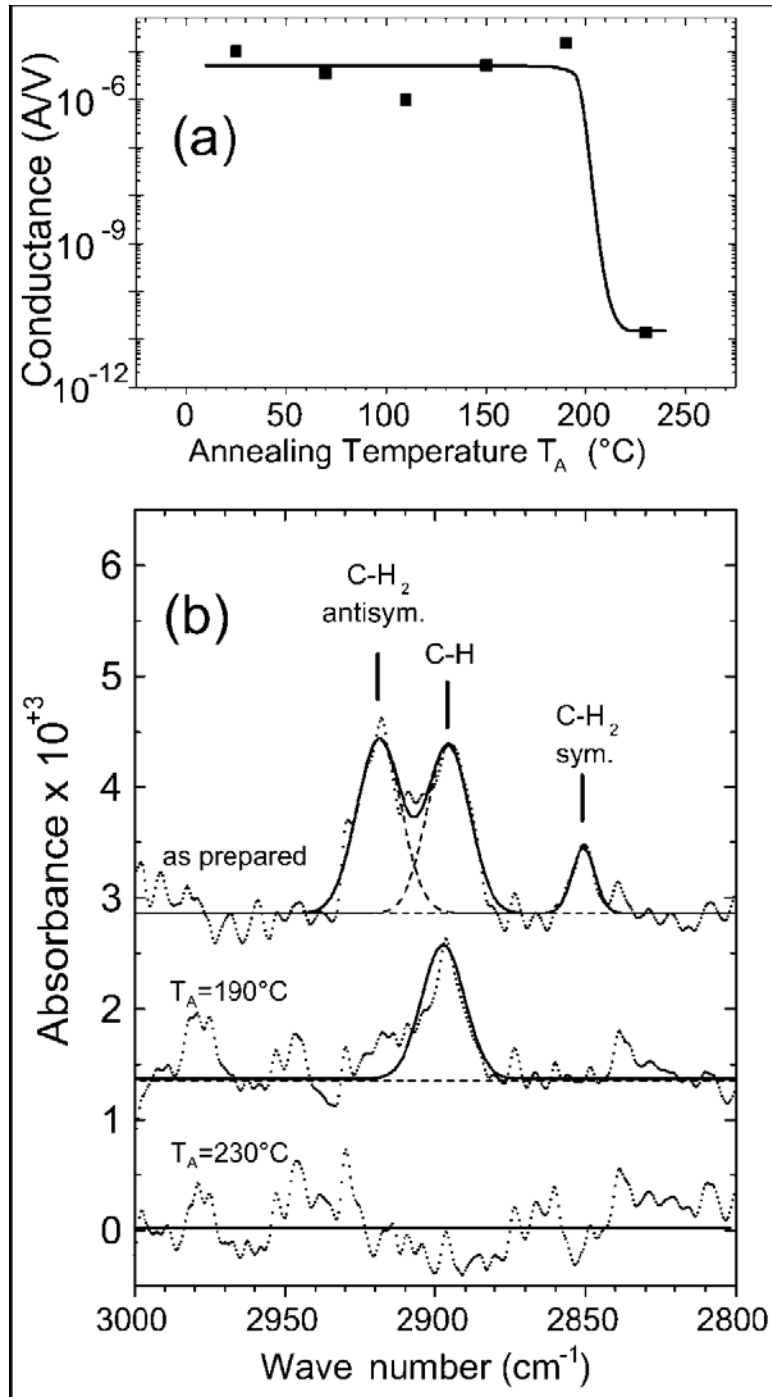


Figure 5.14 (a) Surface conductance of a plasma hydrogenated (100) diamond single crystal as a function of annealing temperature in air. (b) Infrared spectra in the region of the C-H stretching modes after the hydrogen plasma treatment and after 190 and 230 °C annealing temperature, respectively. The spectra are offset for clarity [50].

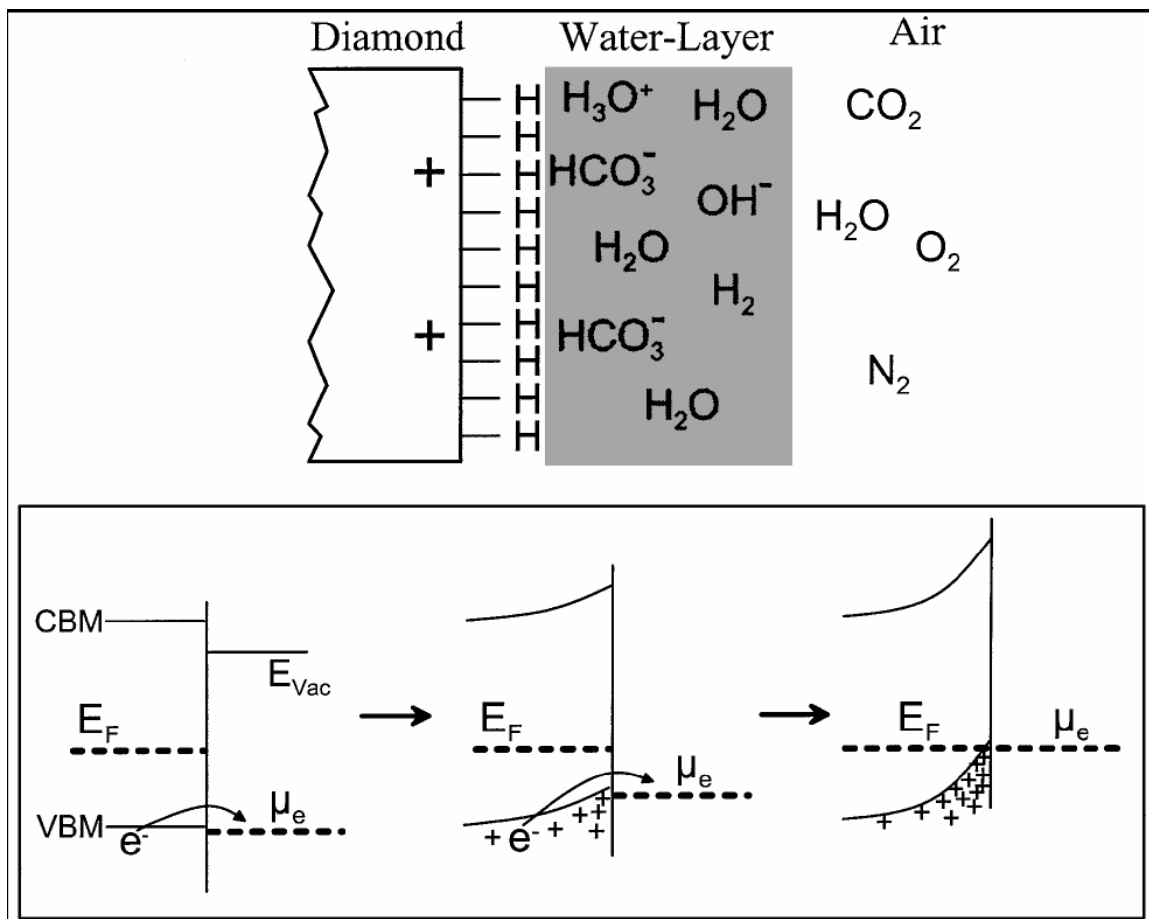


Figure 5. 15 Top: Schematic picture of the hydrogenated diamond surface in contact with a water layer as it forms in air. Bottom: Evolution of band bending during the electron transfer process at the interface between diamond and the water layer [50].

During testing and characterization, a number of methods are used to limit the exposure of diamond to air, most notably the use of desiccant chambers from storage. In actual application of a capacitor or other dielectric device, however, this is not practical. Because surface conduction poses the greatest threat to the operation of power capacitors, where larger operational voltages are desired, a series of power capacitors were designed to shield the diamond layer from exposure to atmospheric conditions. These capacitors, simply referred to as the “Black-Potted” series due to their physical appearance, were assembled from a dielectric layer of diamond grown on a Si substrate. Two examples of the Black-Potted series are shown in Figure 5.16.

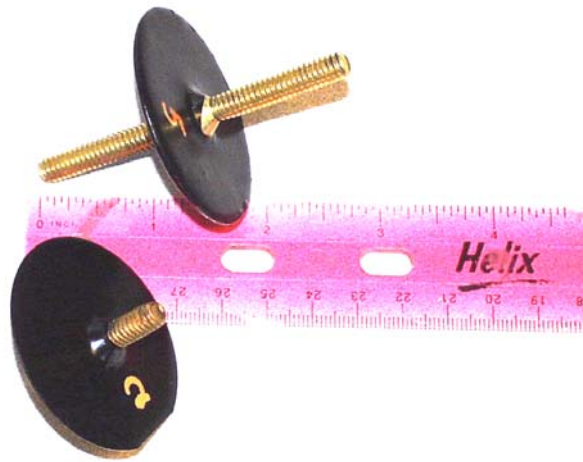


Figure 5. 16 Fully-assembled Black-Potted capacitors.

After deposition, the dielectric was immediately annealed. After annealing, the diamond layer was attached to a metal disc with a conductive silver epoxy. Electrodes were then attached to the substrate and metal disc with the same epoxy. Epotek P1011 was chosen as the epoxy because of its thermal and electrical qualities. During assembly, it was necessary to cure the epoxy, which also prevented the accumulation of water vapor at the

surface of the film. After curing, the device was encapsulated with a black potting compound designed to keep out moisture and provide electrical isolation for the device. The potting compound also was cured. The resultant device was a hard moisture-proof power capacitor.

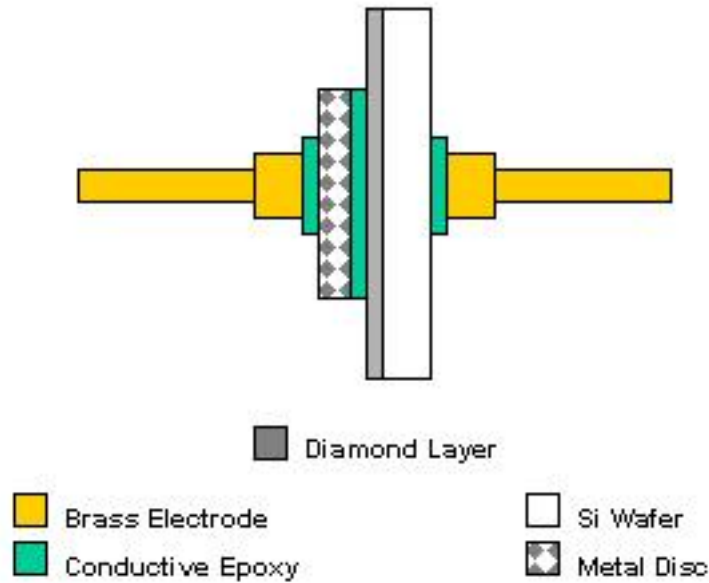
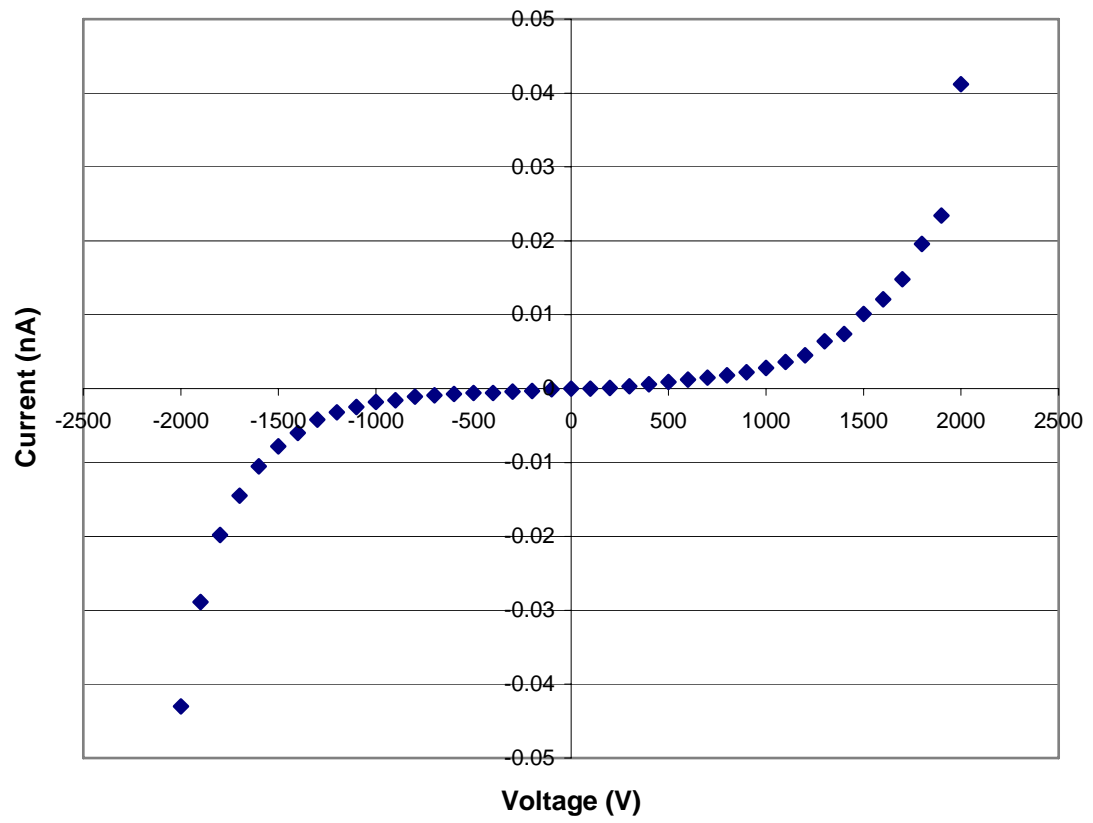


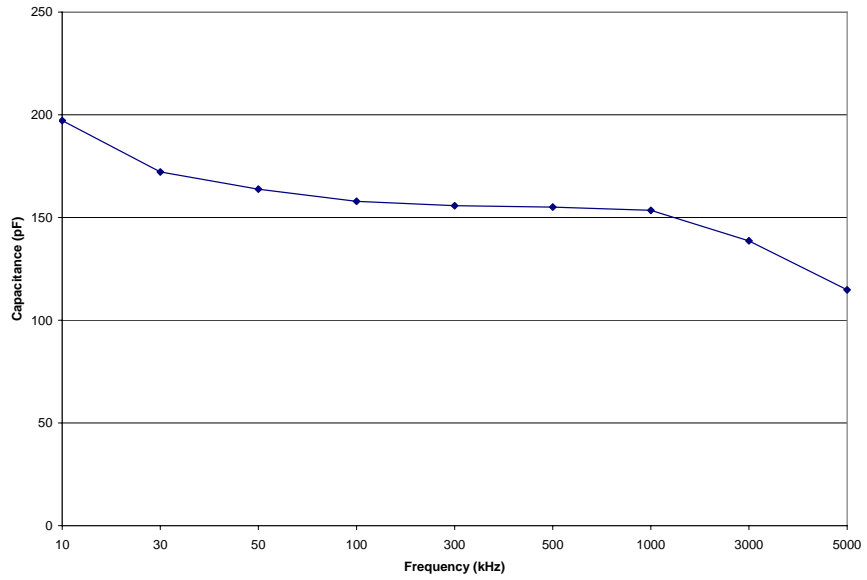
Figure 5.17 Interior design of Black-Potted capacitor. Potting compound (not shown) is added after assembly.

The Black-Potted capacitors were derived from the Alpha and Juliet series of diamond films. The names were used as designations for slightly different growth conditions. Five complete capacitors were created, designated Capacitor #1 – Capacitor #5. These films exhibited acceptable leakage performance up to 1 kV. Leakage, capacitance, and loss profiles for Juliet 002 are shown in Figure 5.18.

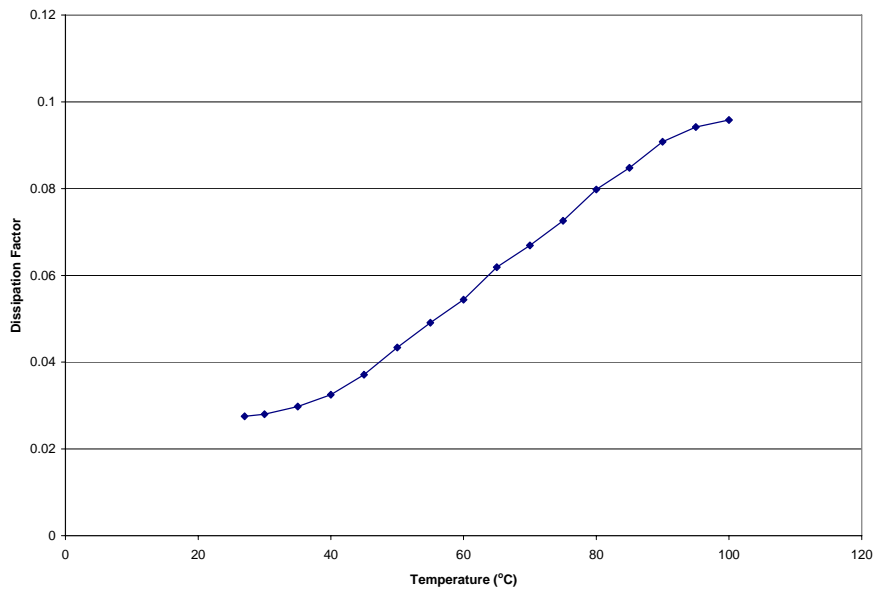


(a)

Figure 5. 18 (a) I-V characteristic of diamond dielectric sample Juliet 002.



(b)



(c)

Figure 5. 18 (b) Capacitance characteristic of diamond dielectric sample Juliet 002, (c) Dielectric loss of sample Juliet 002 with regards to temperature.

The data from Figure 5.18 indicates that the diamond film is capable of withstanding high voltages and stable capacitances over a wide frequency range. This family of diamond films also exhibited low losses with respect to temperature changes. Because of the high voltage tolerance and low dielectric losses, these capacitors were acceptable power capacitor candidates. Using a breakdown voltage for diamond, $V_B = 3 \times 10^7$ V/cm, and a density estimate of 3.51 g/cm^3 , projections of the energy density were made, as shown in Figure 5.19.

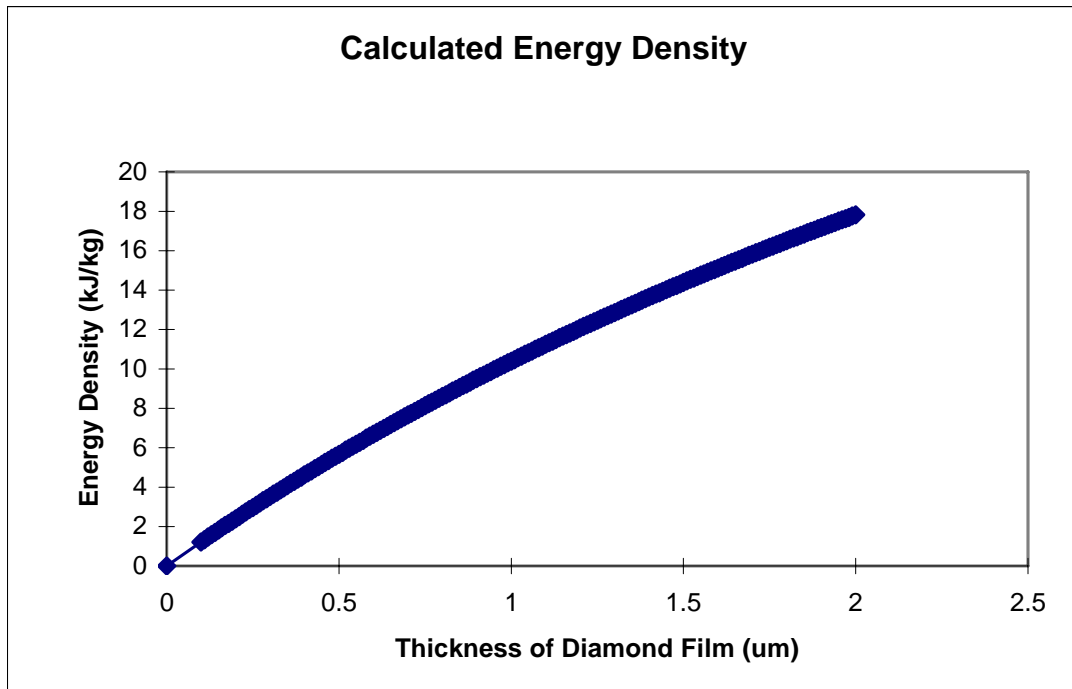


Figure 5. 19 Calculated energy density of Juliet series diamond film.

The effectiveness of the Black-Potted design to resist surface conductivity can be observed an examination of the long-term leakage characteristics of a constituent sample. Figure 5.20 shows a leakage profile for Capacitor #5. The leakage profile has not

changed much over a span of six years. On average, the leakage readings taken in 2006 are within an order of magnitude of the readings taken in 2000, directly following the construction of the device. In reality, the results may actually be closer than is indicated in the figure. The measurement equipment used in the 2006 tests had greater resolution than did the equipment available in the 2000 trials, especially at the lower end of the current spectrum. The lack of significant degradation suggests that the diamond has not been adversely affected by exposure to air, and the subsequent development of an air/water-layer electrical conduit.

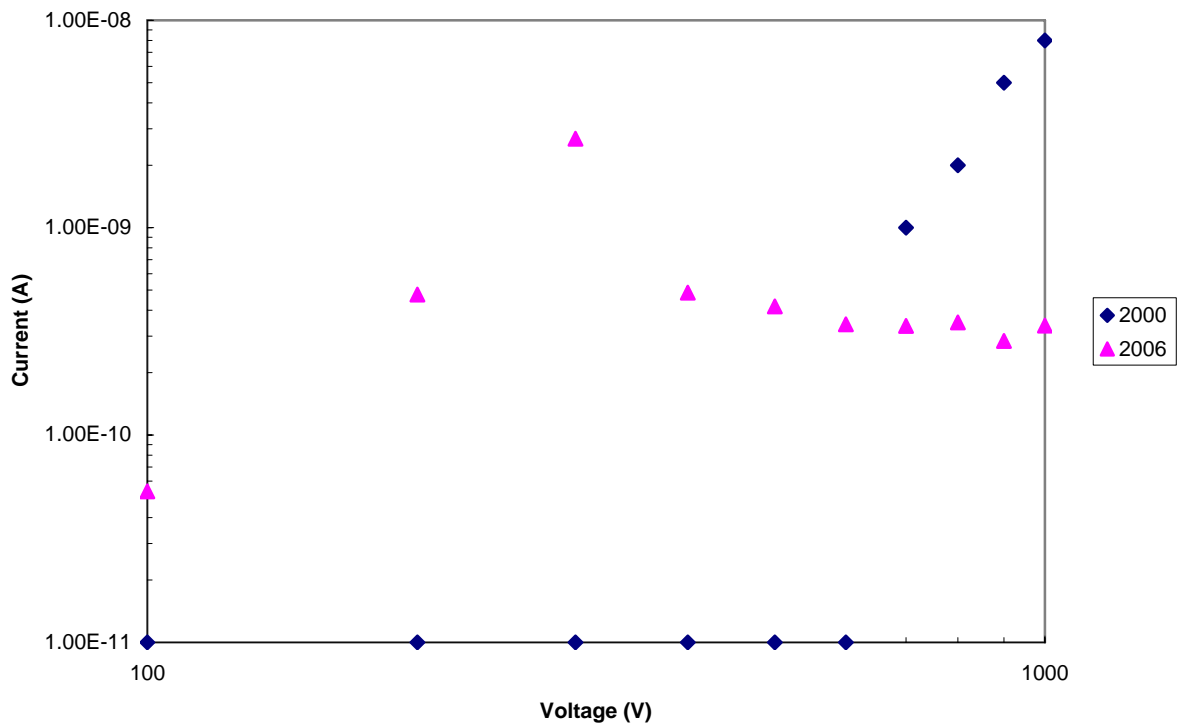


Figure 5. 20 Comparison of Capacitor #5 leakage profile over a six-year span.

Grain Boundary Influence on Conductivity

It has been established that grain boundary conduction is one of the leading causes of conductivity in thin diamond films. Film conductivity develops along the grain boundary interfaces, which represent paths of lower resistivity. Growing diamond films by CVD methods allows a reasonable control of the quality of crystallites by an optimization of deposition parameters (methane to hydrogen ratio, gas pressure, substrate temperature). Still, more understanding is needed, particularly as regards to the grain-boundary interfaces, as determined by the growth and the material electronic response [44].

The key to controlling the effects of grain boundary conduction may lie in the initial nucleation density of the diamond film. A variation in nucleation density influences the density and properties of grain-boundary interfaces, even if the growth parameters are constant. The nucleation density, ultimately, is dependent upon the number of activated nucleation sites available on the substrate surface at the initial stage of the deposition process and could affect the electronic properties of the diamond film.

A method apt to vary the film nucleation and its microstructure is to pre-treat the substrate with diamond powders of different mean sizes. These scratching techniques typically induce mechanical damage of the substrate surface and also activate the initial heterogeneous nucleation phase. The control of the density of nucleation sites determines the consequent size of crystallites and their packing in the polycrystalline samples [45].

This technique achieves different proportions of grain-boundaries, which influences the conductivity and performance of possible capacitors. It is an especially useful condition for thin film diamond because the variation of the nucleation density will affect the first

phase of deposition, when crystal grains completely cover the available substrate surface. As the film grows thicker, other selection principles, which depend only on the deposited film thickness, begin to govern the growth mechanism [46, 47].

To test the effect of nucleation conditions, a set of dielectric samples were produced. Sets of identical 2-inch silicon wafers were cut in half. One set was pre-treated with nanometer-sized diamond powder. The mean particle size of the diamond nanopowder was 35nm. The remaining set was pre-treated with micron-sized diamond powder. The mean particle size of the diamond micropowder was 1 μ m. The pre-treatment was accomplished by immersion in ultrasonic agitation to prepare the polished silicon surface. In the sonication process high frequency sound waves are used to agitate particles in a liquid suspension. Prior to sonication the samples were cleaned and placed into a solution of diamond powder and de-ionized water. The samples were then loaded into an Aquasonic Model 75D Sonicator and treated concurrently for 20 minutes, 1 hour, or 24 hours at the maximum power level. After sonication the samples were rinsed with de-ionized water, dried with air, and re-rinsed with acetone. After the rinsing cycle was complete, the samples were once again blown dry with air.

After the samples were treated, a layer of diamond was grown on each sample using the “smooth” growth process (875 °C, 11.35 Torr, 400 sccm H₂, 4 sccm CH₄, 650 W). This was done to achieve a non-conductive diamond layer with the smallest grain size. To ensure uniformity in the growth conditions, deposition on the sonicated substrates was performed concurrently in the same reactor. After visual inspection of the samples, conductivity was measured via I-V characterization.

As shown in Figure 5.21 and Figure 5.22, the effectiveness of the ultrasonic treatment is dependent on the total sonication time. The conductivity is inversely proportional to the length of the sonication interval. This relationship is true for both powder sizes. These results agree closely with the observations reported by Hirakuri, *et al.* [53]. In that study it was shown that the nucleation density peaked after no more than 30 minutes of ultrasonic pre-treatment.

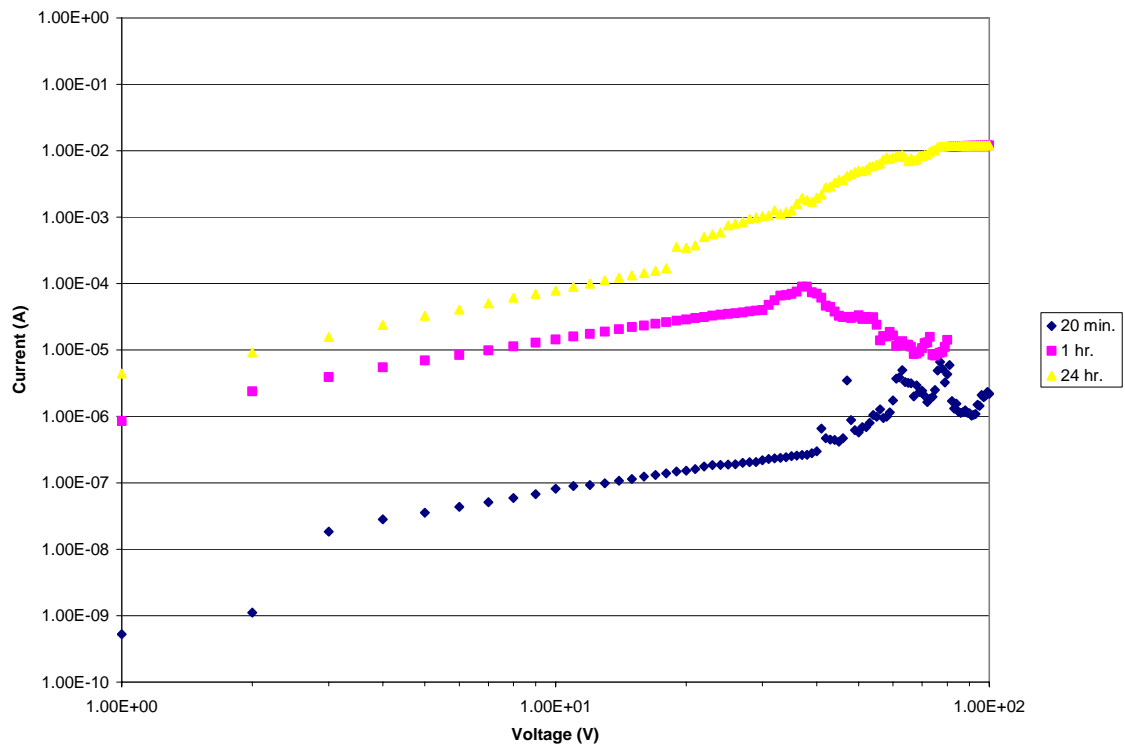


Figure 5. 21 Comparison of diamond layer conductivity as a function of micropowder sonication duration.

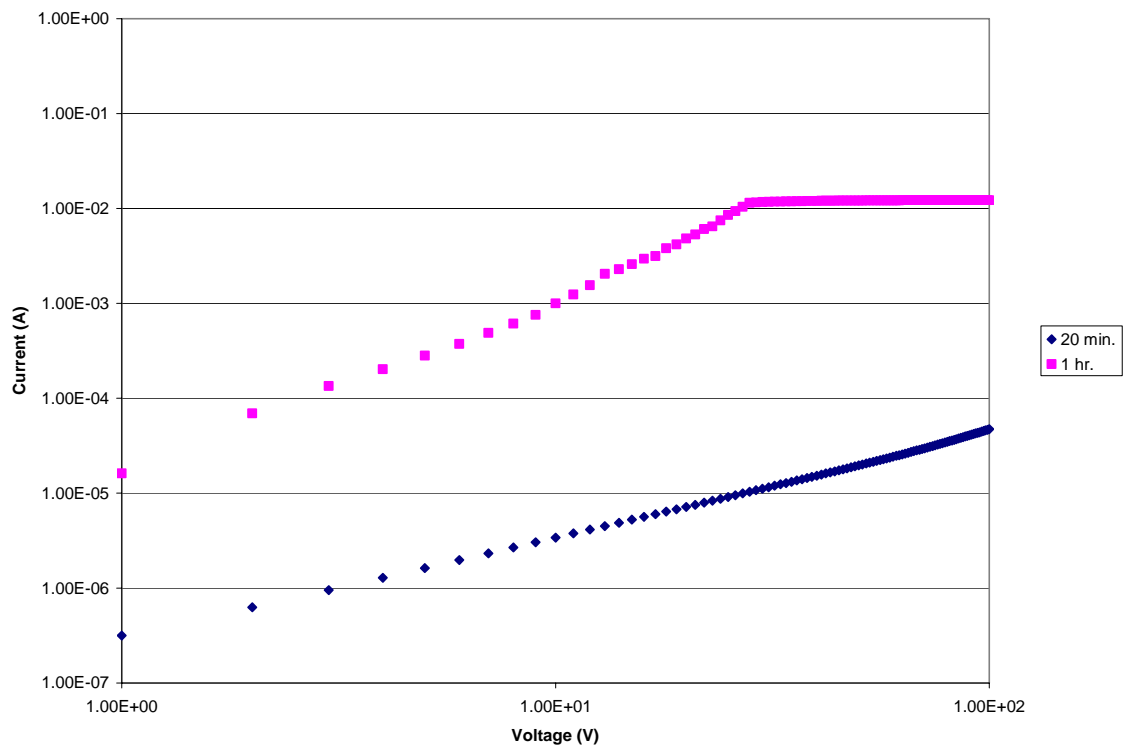


Figure 5. 22 Comparison of diamond layer conductivity as a function of nanopowder sonication duration.

As shown in Figure 5.23, the conductivity is inversely proportional to the powder grain size. During ultrasonic vibration, high frequency sound waves pass through a liquid medium and produce longitudinal pressure waves that alternate between expansion and compression waves. When the expansion waves pull the liquid apart and overcome the surface tension of liquid, a bubble (cavitation) is formed. The cavity will grow slowly, and at a critical size it will most efficiently absorb energy and grow rapidly in one expansion cycle. After this, it cannot absorb energy efficiently, and during the next compression cycle it will not continue to withstand the surface tension of the liquid.

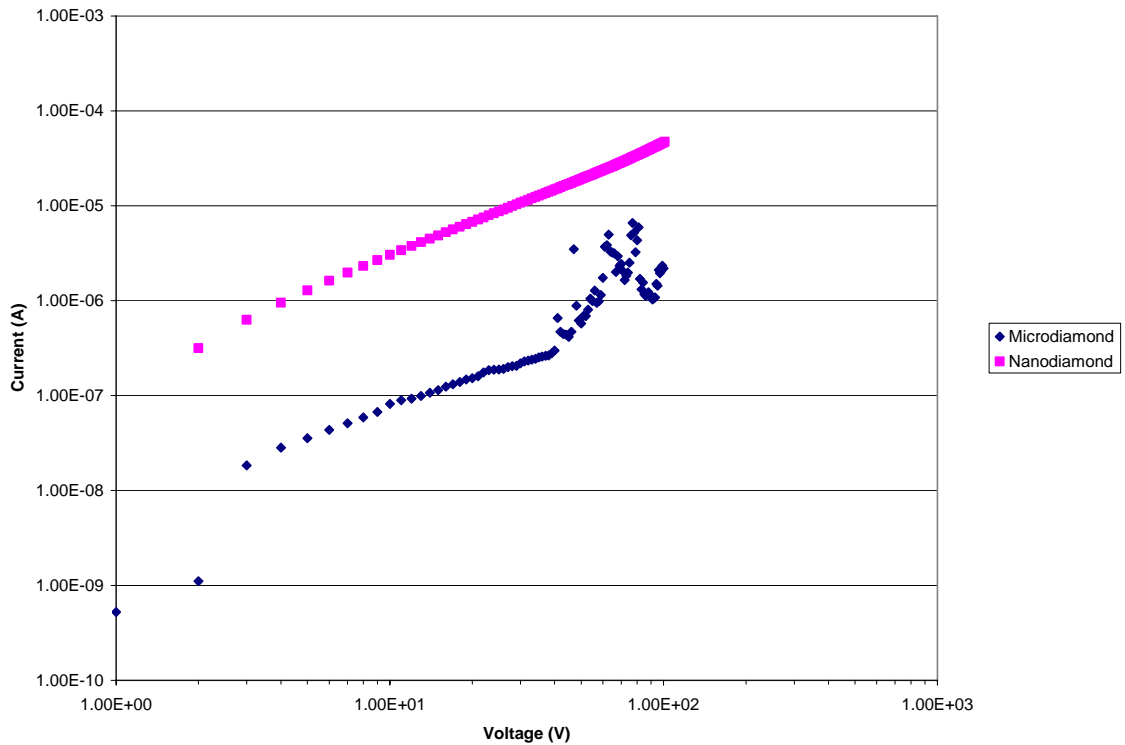


Figure 5. 23 Comparison of thin film diamond conductivity after 20 minutes of ultrasonic pre-treatment.

The liquid will rush in and the cavity implodes within less than 1 μ s. Close to surfaces the implosion is asymmetrical and a fast liquid jet stream is directed toward the surface. The velocity of the jet stream can be calculated by:

$$U = \left(\frac{2}{3} \frac{P}{\rho} \left(\frac{R_0^3}{R^3} - 1 - 3q \frac{R_0^3}{R^3} \left(\frac{R_0}{R} - 1 \right) \right) \right)^{1/2} \quad (5.1)$$

where $q^{-1} = (R_0/R)^{3\gamma}$, $q = 0.02$, $P = 1 \text{ atm}$, R cavity radius, R_0 cavity start radius, γ ratio between the specific heat capacities at constant pressure and volume, ρ density of liquid, ρ_0 density of particle material. Particles exposed to jet streams will travel at a velocity of [52]:

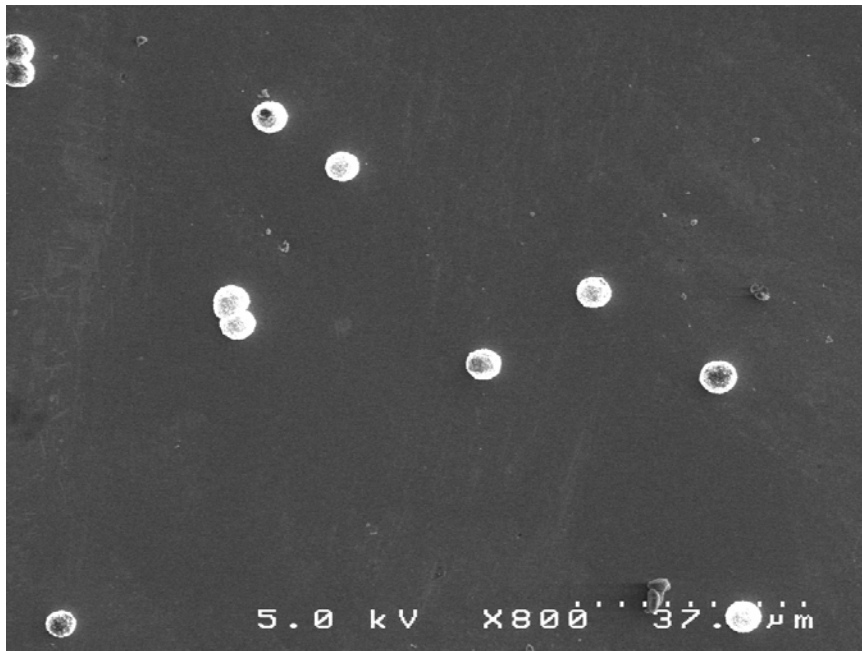
$$u = \pm(\rho - \rho_0) U / \rho \quad (5.2)$$

The jet stream velocity is not sufficient to cause defects on the surface of a substrate. Particles accelerated in the jet stream, however, can reach velocities greater than the speed of sound in the liquid. The force of impacts of particles at these velocities is enough to create defects on the substrate surface, which can act as nucleation sites.

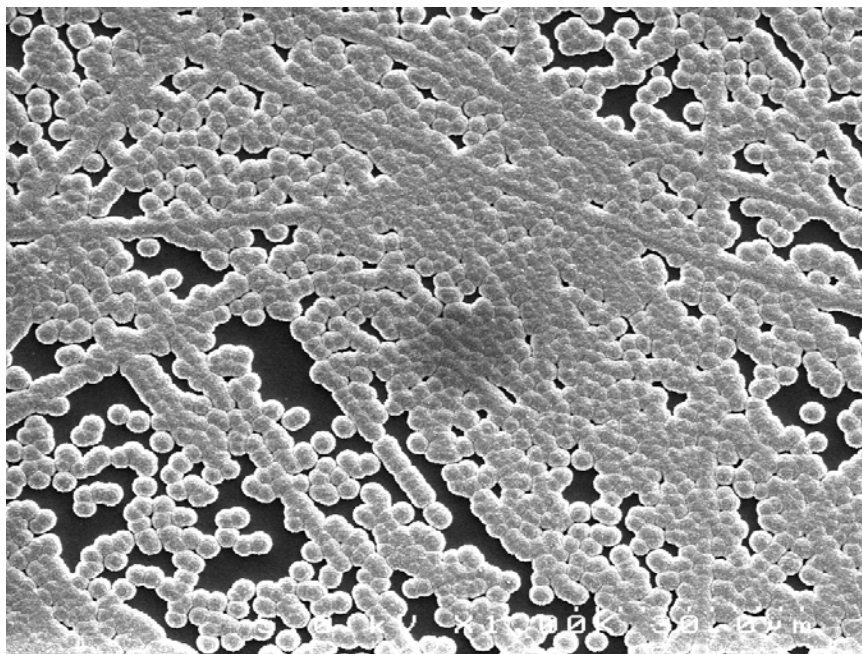
In this manner the lower conductivity of the micropowder samples may be attributed to the higher inertia of the larger moving particles during the sonication process. The larger microdiamond particles may impact the silicon with more force and presumably produce more areas favorable for diamond nucleation on the substrate surface compared to the nanodiamond particles. The higher number of defect sites on the substrate yield a higher number of nucleation sites per unit area. The resulting higher nucleation density allows

for more compact growth of diamond nuclei on the substrate and thereby lessens the amount of grain-boundary interfaces as the film grows. This reduction leads to lower conductivity in the film, as the overall conduction through the grain-boundaries is reduced.

The differences in nucleation density can be seen in Figures 5.24 and 5.25. By optically counting the number of diamond nucleation sites on the silicon surface in high magnification SEM photographs, the nucleation densities resulting from the different sizes of diamond powder were determined. The nucleation densities differ by over three orders of magnitude. After optimum sonication time (20 min) and equal deposition time (6 hours), the recorded nucleation densities were $N_D < 10^{10}/\text{cm}^2$ for microdiamond powder and $N_D < 10^7 /\text{cm}^2$ for nanodiamond powder. As the experiment shows, the conductivity in thin film diamond can be greatly influenced by the surface morphology of the substrate material. The careful control and creation of surface imperfection sites on the substrate can increase the number of suitable nucleation sites available during the CVD process.



(a)

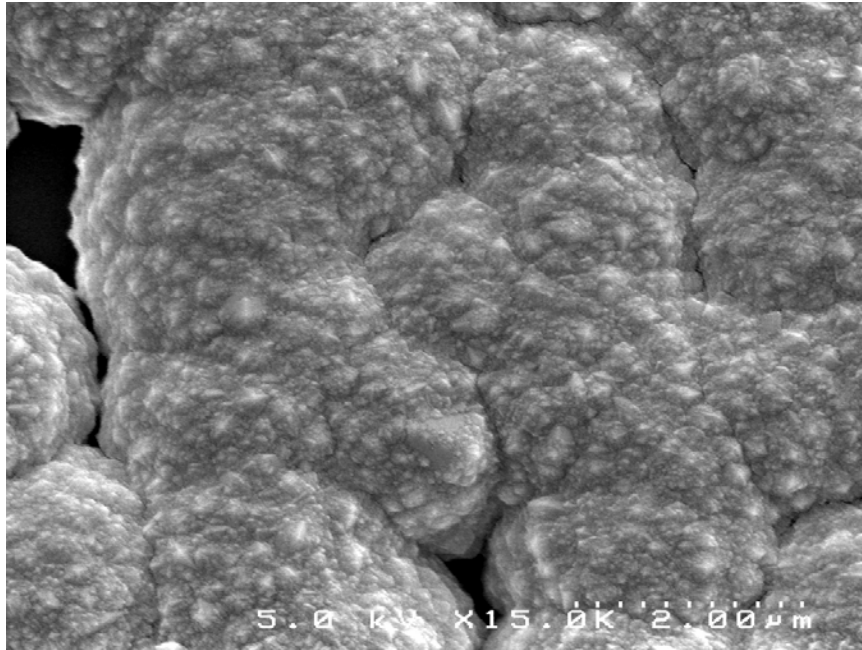


(b)

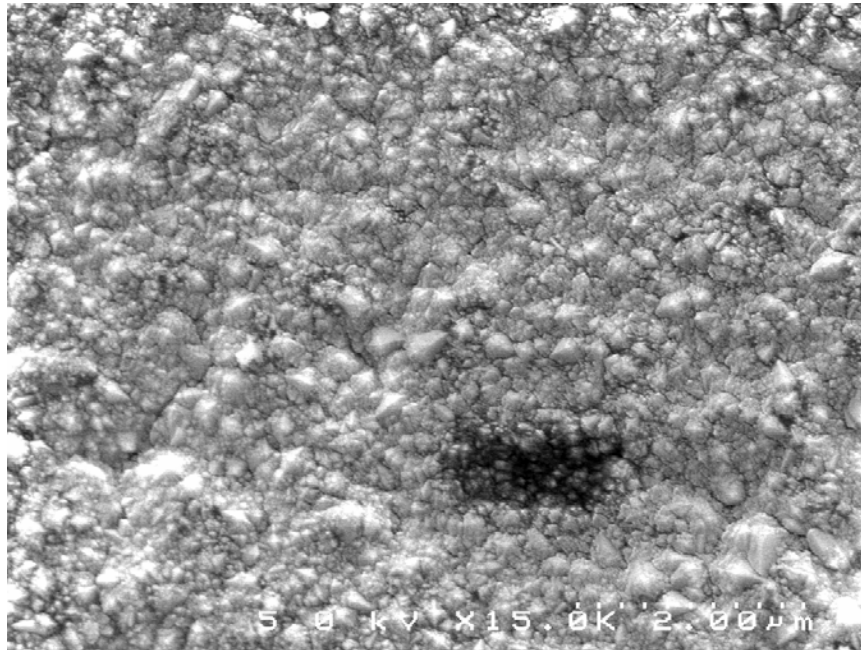


(c)

Figure 5. 24 Surface morphology of thin film diamond after silicon substrate pre-treatment. (a) No pre-treatment. (b) Nanodiamond powder ultrasonic pre-treatment. (c) Microdiamond powder ultrasonic pre-treatment.



(a)



(b)

Figure 5. 25 High resolution surface morphology of thin film diamond after silicon substrate pre-treatment. (a) Nanodiamond powder ultrasonic pre-treatment. (b) Microdiamond powder ultrasonic pre-treatment.

CHAPTER VI

ADVANCED DIELECTRIC STRUCTURES

Most of the dielectric characterization of diamond film has concentrated on capacitance-voltage characterization, isothermal capacitance transient spectroscopy, current-voltage characterization, and temperature dependence of dielectric parameters [11]. While these analyses are informative in characterizing the performance behavior of diamond films, they have to date been only performed on simple diamond dielectric structures. Most practical capacitors, however, utilize more advanced design schemes to provide the necessary tradeoffs between size and electrical performance. Simple structures are primarily based upon the parallel-plate capacitor design. Advanced dielectric structures, however, may include multi-planar designs, the use of non-dielectric support materials, or the use of specialized packaging techniques.

Current Capacitor Designs

Capacitor designs fall into four primary groups: film, ceramic, electrolytic, and miscellaneous capacitors.

Film Capacitors

Film capacitors commonly include a variety of polymer materials such as polyester, polycarbonate, Teflon, polypropylene, and polystyrene. Traditional film capacitors are mainly only available in modest sizes, $<10 \mu\text{F}$. Film capacitors typically have a longer

operational lifetime than electrolytic capacitors. In recent years, film capacitor manufacturers have sought to leverage their superior longevity compared to electrolytics, to move into some applications that call for much larger devices, even to the ranges of thousands of μF . Film capacitors come in two broad categories: film-foil and metallized film. Film-foil capacitors are made of alternating layers of plastic film and metal foil, while metallized film capacitors have the metal vacuum deposited directly on the film. In general, film-foil is better at handling high current, while metallized film capacitors are better at handling self-healing. Various hybrid types can also be found.

Advantages: Film capacitors have reasonably predictable electrical properties and offer many tradeoffs of performance and cost for applications with precise performance requirements. Parameters of interest include capacitance vs. temperature, dissipation factor, and dielectric absorption. The most notable attributes of film capacitors are low leakage and low aging.

Disadvantages: The main drawback of film capacitors is the relatively low dielectric constant (K) of the materials of which they are made. This is partly offset by the relatively good breakdown voltages of those same materials. For this reason film capacitors are physically large for their capacitance. The dielectric constants range of film materials typically range from 2.2 for Teflon to roughly 8 for other materials. Unfortunately, the rule-of-thumb is that the higher the dielectric constant (and therefore the smaller the size), the worse the electrical properties tend to be.

Ceramic Capacitors

Ceramic capacitors offer a broad range of size vs. performance tradeoffs and rank as the most popular in numbers sold. Ceramic capacitors are available in sizes from < 1 pF to thousands of μF .

Advantages: The most notable attributes of ceramic capacitors are their relatively high dielectric constants. This can vary from C0G with a K of up to 60, which has excellent electrical properties but is relatively large and expensive, to ceramics with dielectric constants in the tens of thousands but with very poor electrical properties. Large value ceramics can compete with electrolytic capacitors in high-frequency applications like switch-mode power supplies because of their lower ESR. Ceramic capacitors are especially suitable for surface mounting due to their heat resistance, mechanical integrity, and the ability to make them in very small packages. This has greatly added to their usage.

Disadvantages: Low breakdown voltage means that low-K ceramics (Class 1), which have good electrical properties, have poor volumetric efficiency, and are usually found only in small values. High-K ceramics (Class 2 and higher) have poor electrical properties, which are highly dependent on temperature, voltage, and frequency. They also suffer from having a significant rate of aging. Unlike many other capacitors, ceramics have no self-healing mechanism. This means that manufacturers must maintain a high level of quality control over the dielectric.

Electrolytic Capacitors

By definition, an "electrolytic capacitor" refers to any capacitor that requires a conductive layer between the dielectric and one electrode. In the original electrolytic capacitor, the layer was an actual electrolyte, a conductive salt in a solvent. Some modern electrolytic capacitors today do not actually use an electrolyte, but the word is still commonly used.

Electrolytic capacitors are made by growing an oxide film, the dielectric, on a metal, the anode, by electrochemical means. The films are very thin with fairly high dielectric constants (roughly 10-25), which make for a lot of capacitance in a small package. The resulting devices pass current much better in one direction than the other, making a rectifier of a sort. Because of this, the metals are sometimes called "valve" metals. The two metals presently used are aluminum and tantalum. In theory, a number of other metals could be used.

Advantages: Electrolytic capacitors are best used for applications that require a lot of capacitance in a small space at a reasonable price, such as power supply filtering, or energy storage. They are available in sizes far beyond that of other capacitors. Aluminum electrolytics are presently available from 0.1 μF to several F. Tantalum electrolytics are available from 0.1 μF to a few thousand μF .

Disadvantages: These capacitors must be applied with care because of their marginal electrical properties. The parameters to be watched include leakage, service life vs. temperature, ESR, ESL, and low-temperature performance.

Unlike other capacitors, electrolytic capacitors are not inherently non-polar, but non-polar types are available.

Miscellaneous Capacitors

Miscellaneous capacitors include materials like glass, mica, porcelain, and even gas and vacuum. A few exotic dielectrics like silicon dioxide and sapphire are used in niche applications like microwave capacitors and trimmers. Some are available in surface-mount packages.

Advantages: The electrical properties of miscellaneous capacitors are most similar to film capacitors. However, they have electrical properties that make them particularly useful for some special applications that require special handling.

Disadvantages: These materials also have dielectric constants similar to plastic films. They, therefore, have no advantage in size. Except for mica, these capacitors are commonly available only in small sizes, $< 1 \mu\text{F}$. They also tend to be more expensive than other capacitors of similar size.

Current Diamond Capacitor Structures

Current diamond dielectrics have been used primarily in R&D testing and characterization efforts. Commercial deployment is still largely unrealized. The parallel-plate model is the design structure that has been almost exclusively used for diamond film capacitors. As previously mentioned (see Chapter IV), diamond films are grown on a substrate. If it is desired, the substrate can be removed by chemical means to leave a freestanding film. When electrical contacts are on both sides of the film, a CVD diamond capacitor is formed. Figures 6.1 and 6.2 show the structure of the devices used by Ye (substrate supported CVD diamond) and Ebert (freestanding CVD diamond) in their experiments.

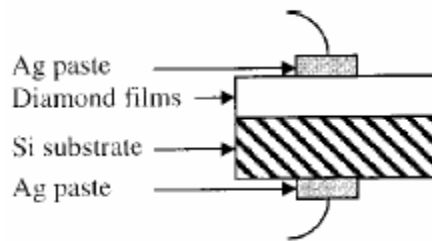


Figure 6.1 CVD diamond capacitor (substrate-supported) [11].

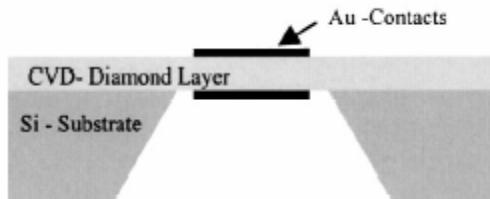


Figure 6.2 CVD diamond capacitor (freestanding) [12].

In both designs, a silicon substrate was used and contacts were applied to the exposed sides of the structures. The substrate design of Figure 6.1 also illustrates the approach of attaching electrodes to the surface via a conductive paste. In the freestanding capacitor an alternative electrode approach, thermal metal evaporation, is used. While there may be variations in the thickness of the film and the particular metal(s) used for contacts, the above examples are typical of the basic parallel-plate design of current diamond capacitors.

Advanced Diamond Capacitor Structures

Simple parallel-plate capacitor designs are limited by a number of factors. The capacitance is restricted by the parallel-plate equation,

$$C = \epsilon \frac{A}{d}. \quad (6.1)$$

Assuming that the dielectric constant is stable, the capacitance is ultimately governed by the geometry of the device. To maximize the capacitance, the area of the device must either be large relative to the thickness of the film, or the thickness of the film must be small relative to the area of the capacitor.

Both scenarios pose practical design difficulties. A capacitor with a large area is unfavorable because the added size may not be suitable for a number of applications, especially for microelectronics. There also may be issues with the cost of production of large area CVD diamond films. A capacitor with a thin dielectric may be unfavorable

because of the aforementioned concerns with thin diamond films. Leakage and breakdown strength are important factors as the dielectric becomes thinner.

One way to deal with the tradeoff between area and film thickness in capacitor design is to implement the techniques used by the film capacitor industry. By using alternating layers of dielectric material, a device with larger capacitance can be created using the same are footprint of a single layer device. This approach has long been used to increase capacitance while continuing to minimize the overall volume of commercial film capacitors. As long as each dielectric layer is thick enough to handle the voltage and field requirements of the intended application for the device, any number of layers can be stacked together to form a larger composite device.

By layering diamond dielectric films with a conductive material, it is possible to create sets of electrically parallel capacitors, which can be connected together to produce a larger stacked capacitor.

If two capacitors are connected in parallel as shown in Figure 6.3a, a circuit with an equivalent capacitance C_{eq} will result as shown in Figure 6.3b.

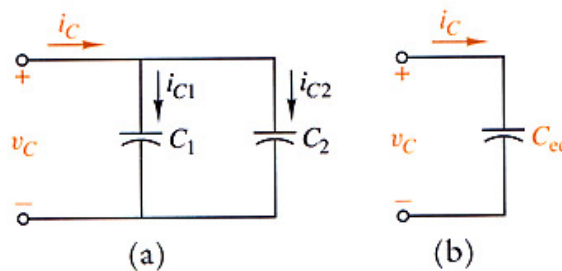


Figure 6.3 (a) Parallel combination of two capacitors. (b) Equivalent capacitance, C_{eq} [35].

Since the voltage v_C appears across each capacitor and since $i_C = i_{C_1} + i_{C_2}$, it follows that

$$i_C = i_{C_1} + i_{C_2} = C_1 \frac{dv_C}{dt} + C_2 \frac{dv_C}{dt} = (C_1 + C_2) \frac{dv_C}{dt}. \quad (6.2)$$

It can hence be stated that $C_{eq} = C_1 + C_2$.

This result can be expanded for any number of capacitors. Therefore, for n capacitors in parallel, the equivalent capacitance is

$$C_{eq} = C_1 + C_2 + \dots + C_n. \quad (6.3)$$

Because of the additive nature of parallel capacitors, it is straightforward to analyze the performance of a multi-layered capacitor. Numerically, the capacitive characteristics of any multi-layer device should approximate the sum of the performance of the individual layers.

Another approach is to create a “ribbon” of dielectric material. The dielectric material will have an increased area while maintaining a constant thickness. By layering conductive material on both sides of a dielectric material, a capacitor is formed. If the length to width ratio of the cross section is increased, the effective area of the capacitor is also increased. The width and thickness of the dielectric remains constant, and capacitance of the structure is thereby increased. If the capacitor is fabricated with a serpentine geometry, a larger capacitor can be created within the basic footprint of a standard device.

Since the stacked capacitor designs are based upon the concepts of parallel electrical circuits and dielectric ribbons, it is imperative that the isolation between the dielectric and conductive layers is adequately preserved. A short circuit at any layer interface in these types of structures can effectively disable or impair the entire device. This becomes especially pertinent at high voltages and fields, where electrical arcing and dielectric breakdown are points of concern.

These particular approaches to advanced capacitor designs have not been implemented on a characterization level diamond film device, and there are no references to such devices in the current literature. To test these advanced capacitor design concepts, two different models were used.

Mechanical Multi-Layer Design

The first multi-layer design was a mechanical approach. In this mechanical approach, discrete diamond layers were stacked with layers of metal separating the dielectrics. The diamond layers were oriented towards each other, and the metal layers were connected together such that a parallel circuit was created. Figure 6.4 illustrates the design concept.

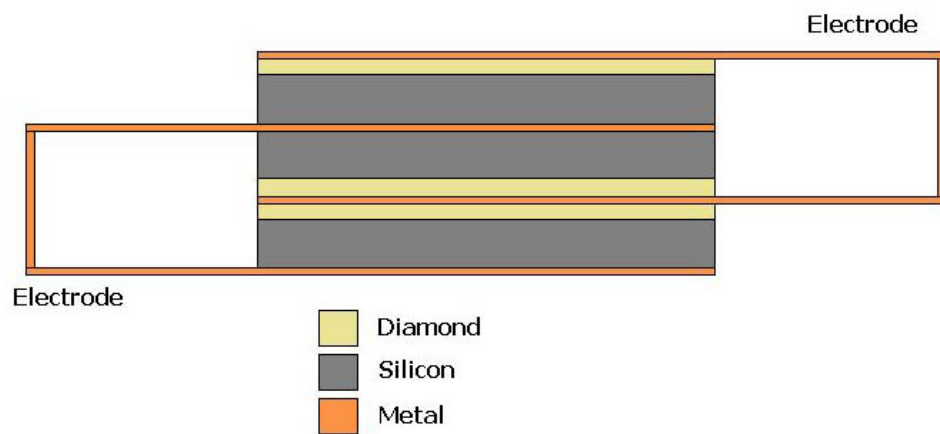


Figure 6.4 Mechanical stacked capacitor design (3 layers).

The mechanical design allows for a simple proof of concept for the stacked capacitor. The individual dielectric and metal layers can be joined by a conductive adhesive or by simple compressive force, provided that the pressure is not high enough to damage or break the diamond film.

In this design, the individual diamond layers can be tested and characterized prior to the assemblage of the larger structure. Theoretical estimates about the performance of the larger capacitor could therefore be made early in the construction process. Since this design involved the use of individual diamond films as constituents to a larger design, it

was imperative that care was taken in the preliminary testing and subsequent handling of the diamond films. Damage to any individual layer will adversely affect the performance of the whole structure.

Monolithic Multi-Layer Design

The next advanced diamond structure was a monolithic stacked capacitor design. Here, all of the layers of dielectric and conductive material were contiguously arrayed into a solid device in a serpentine structure. The serpentine geometry uses the “ribbon” concept. A basic design for the concept is illustrated in Figure 6.5.

In this design the diamond film and conductive material are patterned to provide geometrical accuracy for the constituent layers. Masks were developed (see Appendix) for the deposition process to ensure proper alignment and uniform growth.

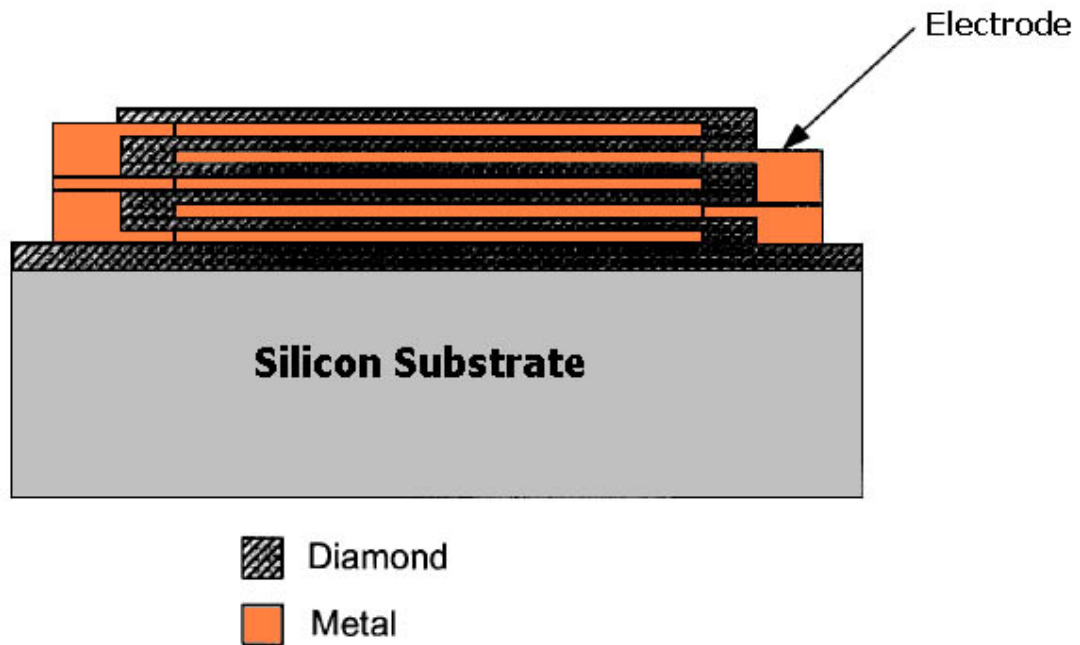


Figure 6.5 Monolithic diamond stacked capacitor design.

Mechanical Multi-Layer CVD Diamond Capacitor

To explore the dielectric behavior of multi-layer capacitors, multiple substrates were used to create a series of multi-layer capacitors. By layering diamond films with copper foil, it was possible to create sets of electrically parallel capacitors, which could be connected together to produce a larger stacked capacitor.

The samples chosen for the multi-layer experiments came from the 01 Series of diamond films. These films were created using the same growth processes that were employed to create the earlier “Black-Potted” capacitor series (see Chapter V).

The films created using this set of growing conditions provided a favorable combination of electrical and physical characteristics for utilization in a multi-layer design. Samples of similar thickness and growing conditions were used in the layered capacitors. Three samples were chosen for the multi-layer tests based on their individual testing performance having high capacitance and low leakage current for a wide range of voltages. High resistivity and a reasonable dissipation factor were other areas of consideration. The three samples selected were designated Cap 011, Cap 012, and Cap 013.

Performance Analysis

The following tables summarize the electrical properties of the dielectric candidates.

Table 6.1 Measured capacitor electrical properties.

	DC Capacitance (F)	RC time constant (τ) (s)	Resistivity (Ω-cm)
Cap 011	2.15E-09	3.00E-06	8.54E+10
Cap 012	2.10E-09	3.00E-06	3.14E+11
Cap 013	2.17E-09	3.00E-06	3.06E+11

Table 6.2 Calculated capacitor electrical properties.

	Calculated Dielectric Thickness (microns)
Cap 011	35.99
Cap 012	36.88
Cap 013	35.69

The thickness calculations of Table 6.2 are based on the classical parallel plate capacitor equation, $C = \epsilon A/d$. For the thickness calculations the dielectric constant of diamond, 5.5 was used. This value was verified by Feather [34] in previous Vanderbilt studies on the properties of dielectric diamond films.

I-V Analysis

I-V analysis shows that the leakage current for the samples is low at voltages less than 50 V. At the time of testing, mechanical difficulties had prevented the annealing of samples Cap 011, Cap 012, and Cap 013. Without annealing, the samples exhibit similar I-V profiles to other documented films in this regard. Each of the I-V curves exhibit a region of low conductivity followed by a region of exponentially increasing current. This behavior can be seen in the Figures 6.6, 6.7, and 6.8. Therefore, the capacitive behavior of stacked samples at restricted operational voltages was examined. If the samples were annealed, this voltage range was expected to increase, as shown earlier in this report.

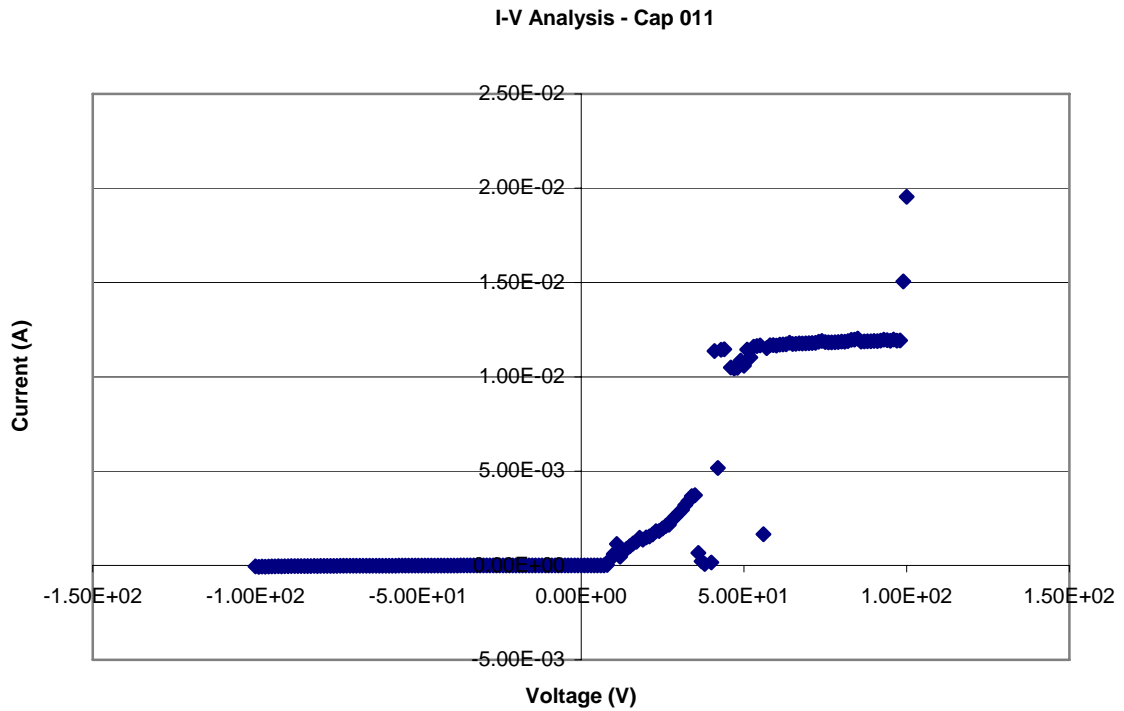


Figure 6. 6 I-V analysis of capacitor sample Cap 011.

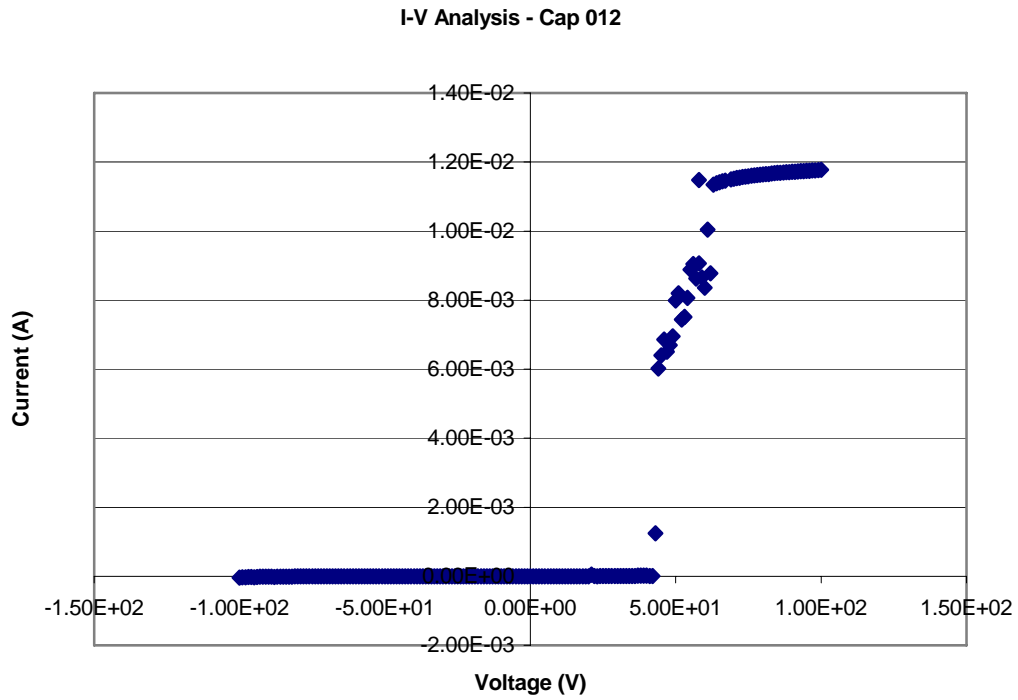


Figure 6.7 I-V analysis of capacitor sample Cap 012.

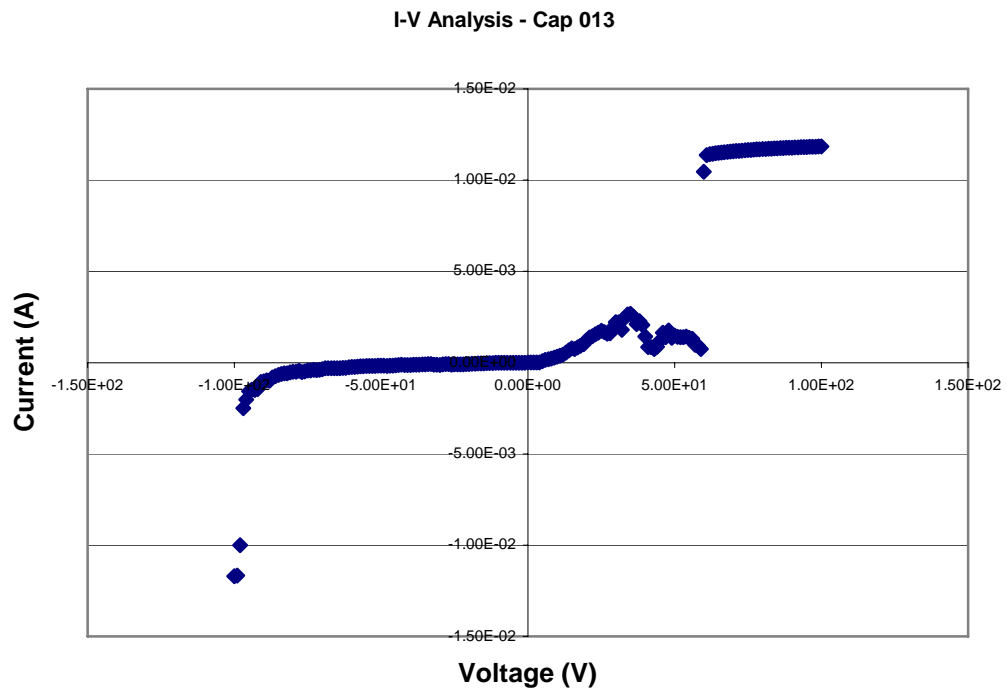


Figure 6.8 I-V analysis of capacitance sample Cap 013.

Capacitance Measurements

The following charts show the capacitance of the films at various test frequencies. The average capacitances were 425.4 pF, 485.7 pF, and 765.9 pF for Cap 011, Cap 012, and Cap 013 respectively. The capacitance decreases initially and then “flattens out” as the frequency increases. A summary of the capacitance behavior is shown in the table below.

Table 6.3 Summary of AC capacitor behavior.

	Cap 011	Cap 012	Cap 013
<u>Frequency (kHz)</u>	<u>Capacitance (F)</u>	<u>Capacitance (F)</u>	<u>Capacitance (F)</u>
10	4.58E-10	6.82E-10	1.76E-09
20	4.34E-10	6.22E-10	1.19E-09
40	4.27E-10	4.76E-10	7.41E-10
100	4.24E-10	4.60E-10	5.38E-10
200	4.23E-10	4.57E-10	5.02E-10
400	4.22E-10	4.56E-10	4.93E-10
1000	4.21E-10	4.54E-10	4.94E-10
2000	4.19E-10	4.53E-10	6.17E-10
4000	4.18E-10	4.52E-10	6.50E-10
10000	4.08E-10	4.44E-10	7.73E-10
Average Capacitance (F)	4.25E-10	4.86E-10	7.65E-10
DC Capacitance (F)	2.15E-09	2.10E-09	2.17E-09

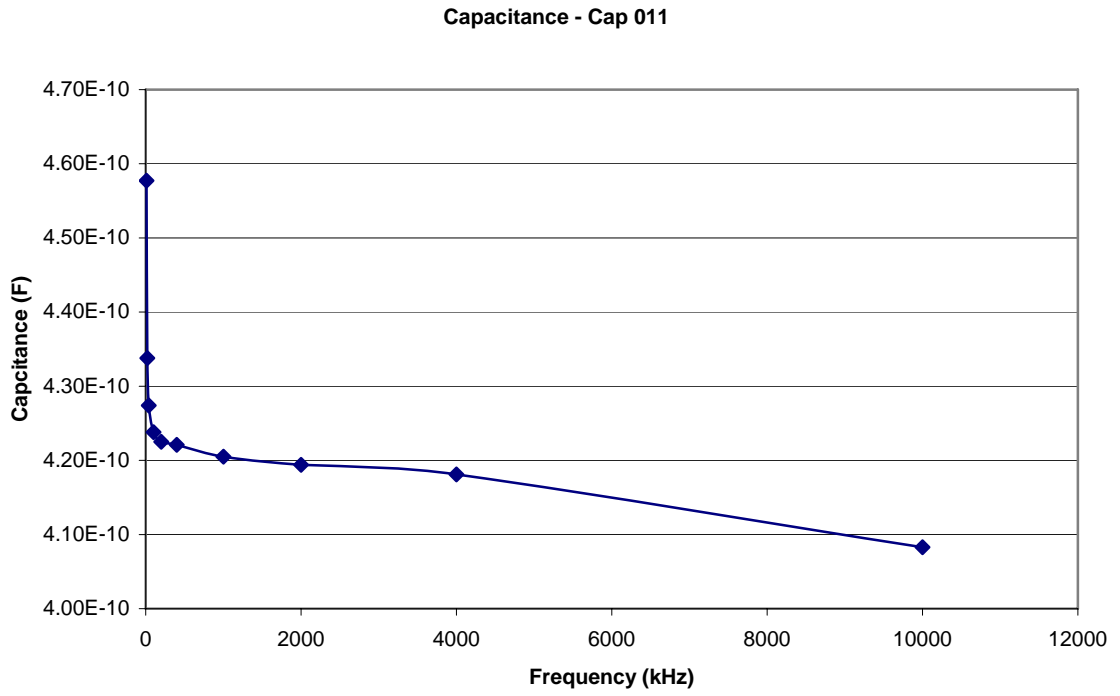


Figure 6.9 Capacitance vs. Frequency - Sample Cap 011.

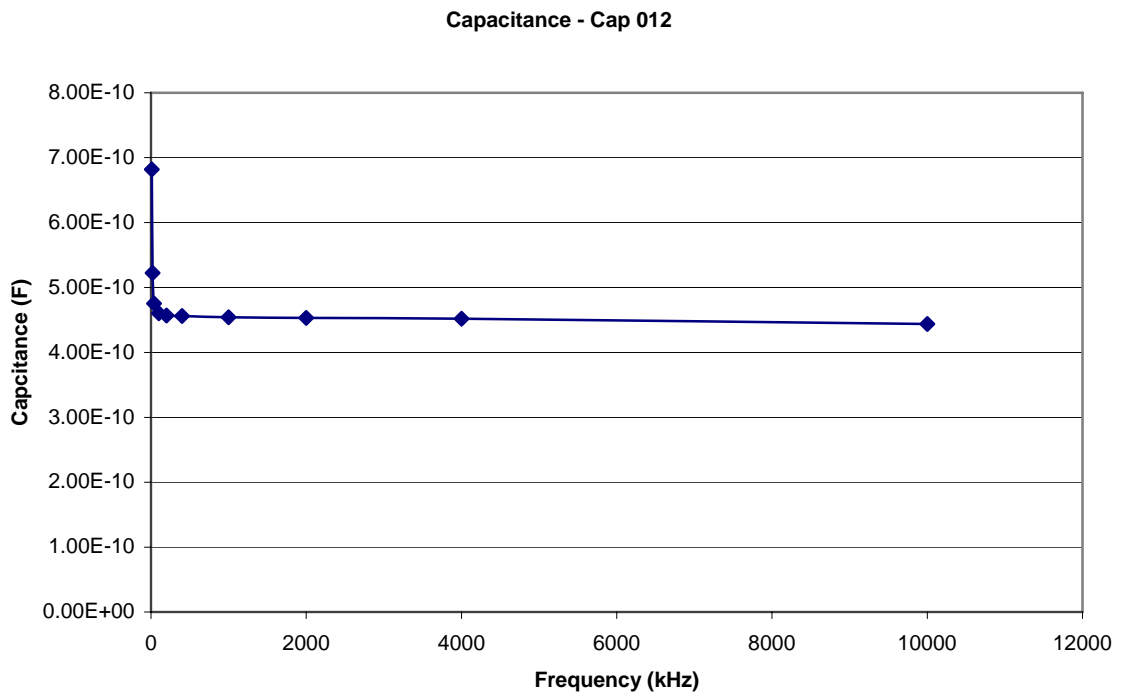


Figure 6.10 Capacitance vs. Frequency - Sample Cap 012.

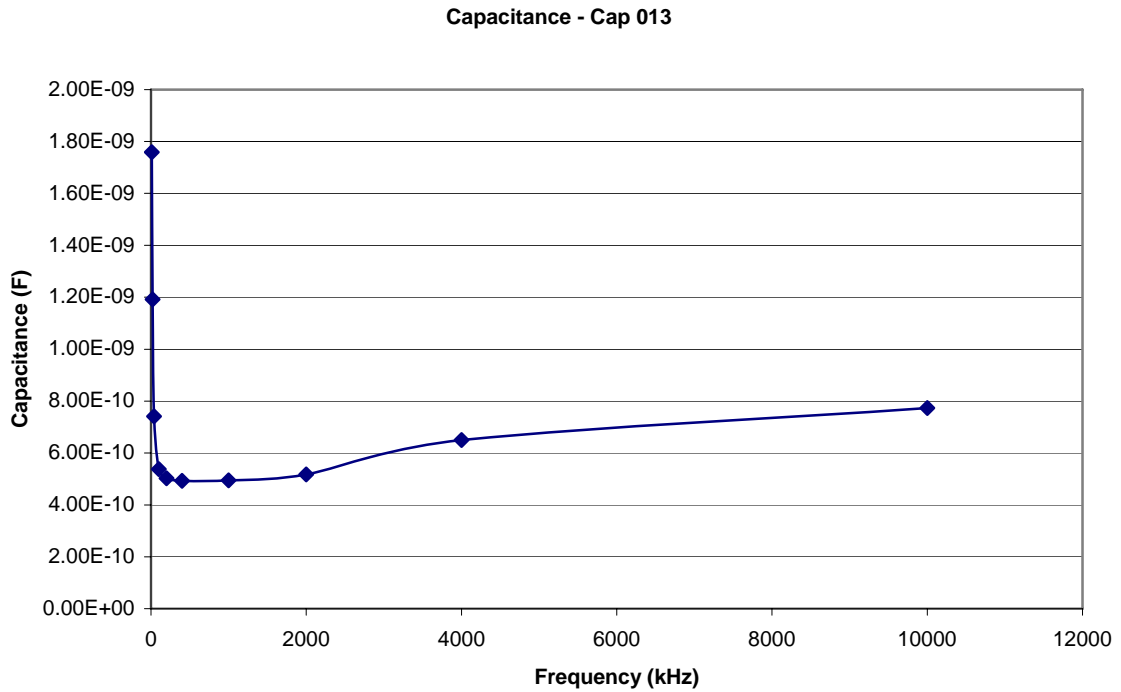


Figure 6.11 Capacitance vs. Frequency - Sample Cap 013.

The capacitance results show that there is a drop in the capacitance as frequency is increased over approximately 1Hz. The capacitance then stabilizes with respect to increasing frequency at frequencies above 100 kHz. This observation is consistent with the observations of Ibarra *et al.* [17], as reported earlier in this report. The underlying meaning of these results is that the dielectric constant (relative permittivity) of these samples is consistent for a wide range of operation for the sample set. This is mainly because space charge polarization is the dominant polarization mechanism in diamond in this frequency range. Space charges are easily able to respond to alternating fields at these frequencies, hence the measured capacitance is stable. Cap 013 shows an increase in its capacitance value after 2000 kHz. This may be attributed to slight defects in the

diamond lattice or field related interactions with the silicon substrate during AC operation.

This is an important factor to consider in the estimation of the energy handling capabilities of these capacitors. Based on an operating voltage of 1000V, which has previously been established as a workable voltage for this class of capacitors, the energy density of Cap 011 would be approximately 0.02 J/cm^3 . In light of the energy density projections discussed in Chapter V, the advantage of using devices with multiple dielectric layers is clear. High energy densities can be reached with multiple layers of diamond because of the high voltage handling capabilities of diamond films.

Layered Capacitor Performance

With the performance determined for the individual candidate samples, the next testing was the formation of multi-layered capacitors. The same tests used to characterize the individual films were employed to test the larger, multi-film capacitors. Special care had to be taken in the handling of the layered capacitors. As prototypes, they were not constructed to withstand high handling stresses. Special attention was made to assure that adequate electrical contact was maintained between conducting surfaces and that adequate space was maintained to prevent electrical shorting between the copper foil terminals of each device. For each device several copper foil contacts were fabricated. These contacts measured 1.75" in diameter and supported a 0.5" x 3" tab. The tab would be used to connect the conducting surfaces of the various layers. Figure 6.12, Figure 6.13, and Figure 6.14 show the physical orientation and configuration of the multi-layered capacitors.



Figure 6.12 Multi-Layered Diamond Capacitor – Overhead View.

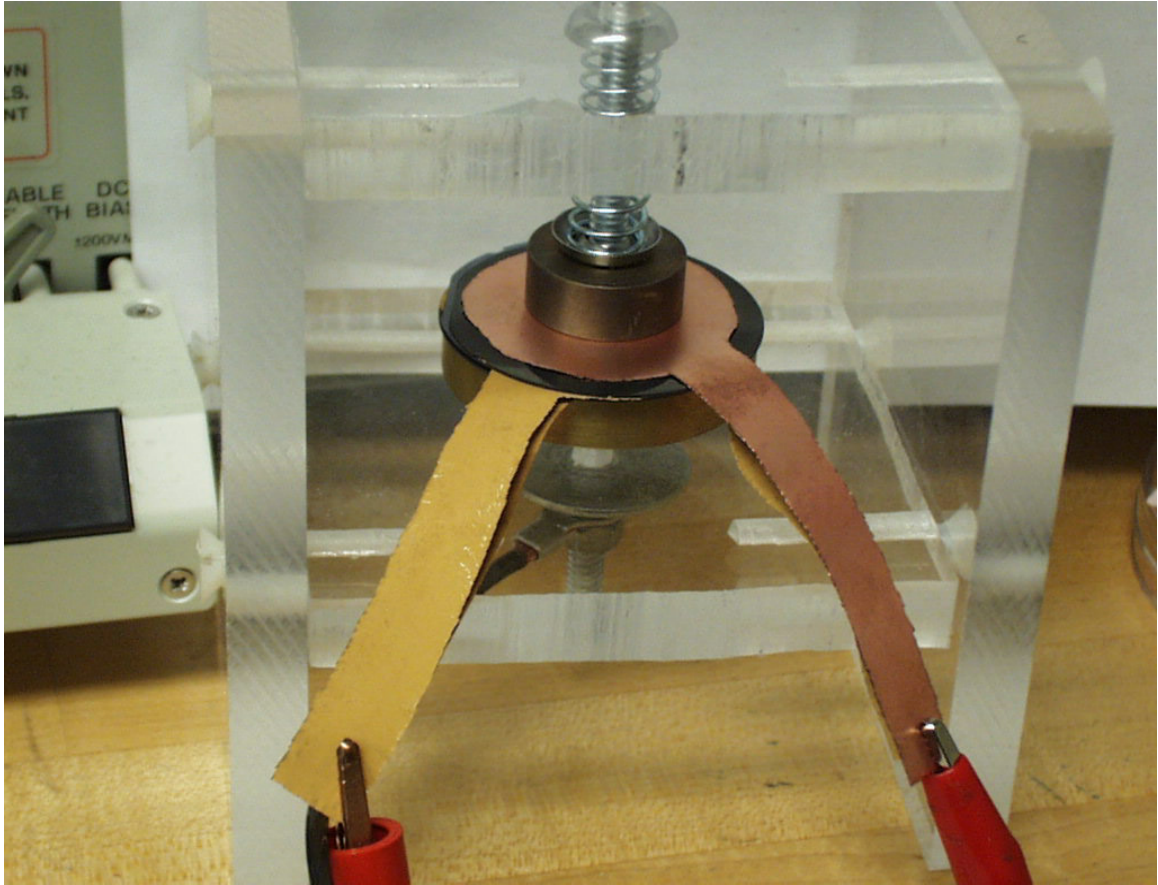


Figure 6. 13 Multi-Layered Diamond Capacitor in Test Chamber.



Figure 6. 14 Multi-Layered Diamond Capacitor – Side Profile.

The two-layer capacitor was the first to be constructed. For this design Cap 011 and Cap 012 were used as the dielectric films. The collected data for this device shows no anomalous behavior as compared to the single layer dielectric tests. The following charts, Figures 6.15 – 6.19, show the capacitance, dissipation factor, ESR, and charge-discharge behavior of the dual-layer device. When compared to Figure 6.9 and Figure 6.10, it can be seen that the capacitance of the two-layer sample, as illustrated in Figure 6.16, is indeed greater than the capacitances of Cap 011 and Cap 012 individually. The data also shows that the dissipation factor (loss tangent) and ESR remain low throughout the range of frequencies tested. The image capture from the oscilloscope, Figure 6.19, clearly shows a charging curve and subsequent discharge curve as the device is pulsed.

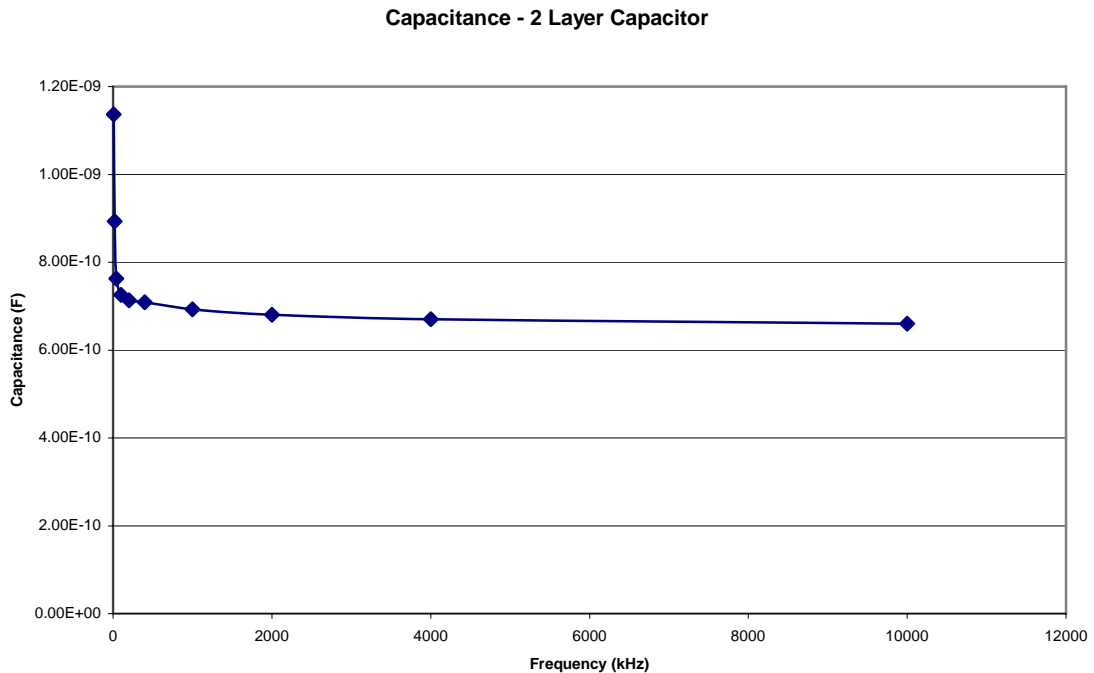


Figure 6.15 Capacitance vs. Frequency – Two-Layer Diamond Capacitor.

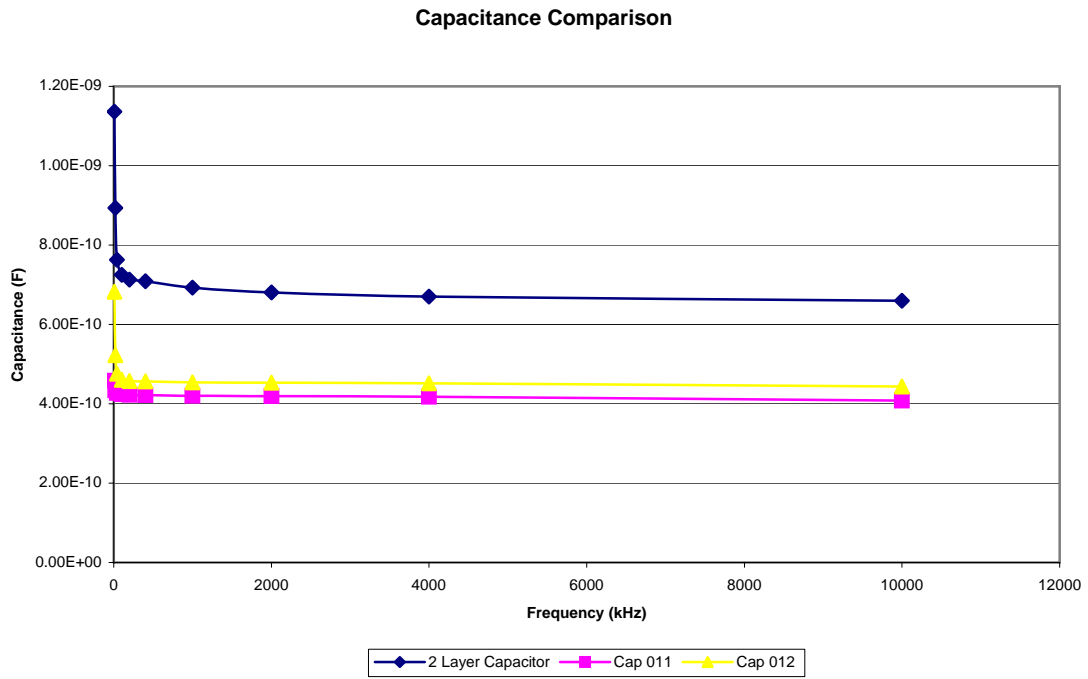


Figure 6. 16 Comparison of Capacitance of Dual-Layer Capacitor and Individual Device Layers.

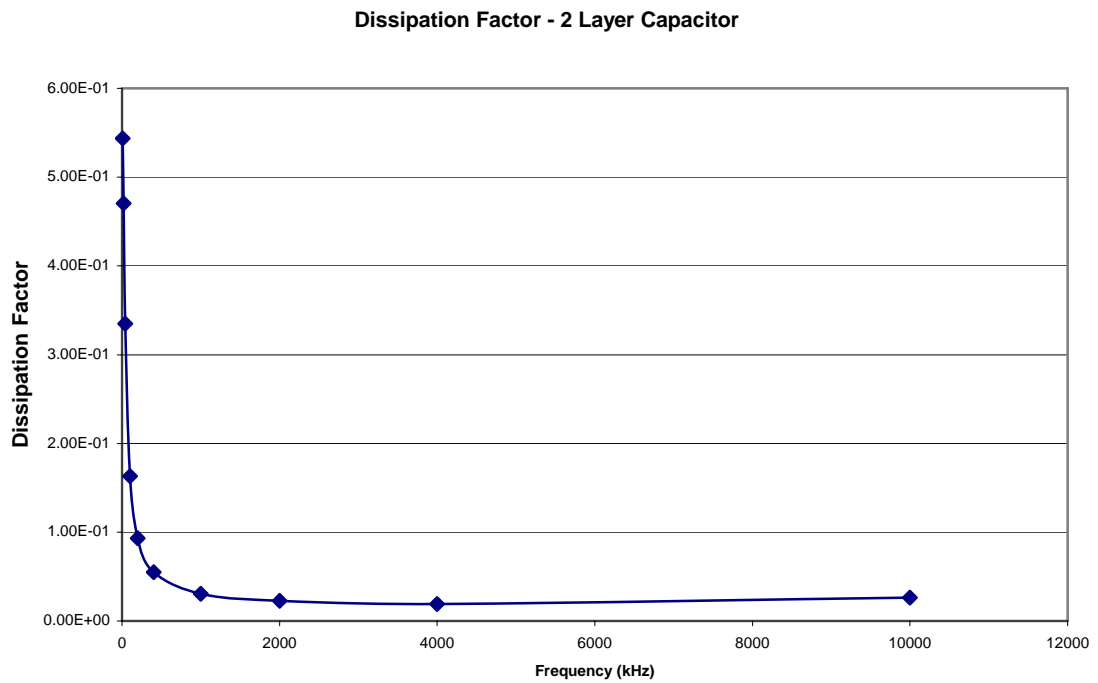


Figure 6. 17 Dissipation Factor vs. Frequency – Two-Layer Diamond Capacitor.

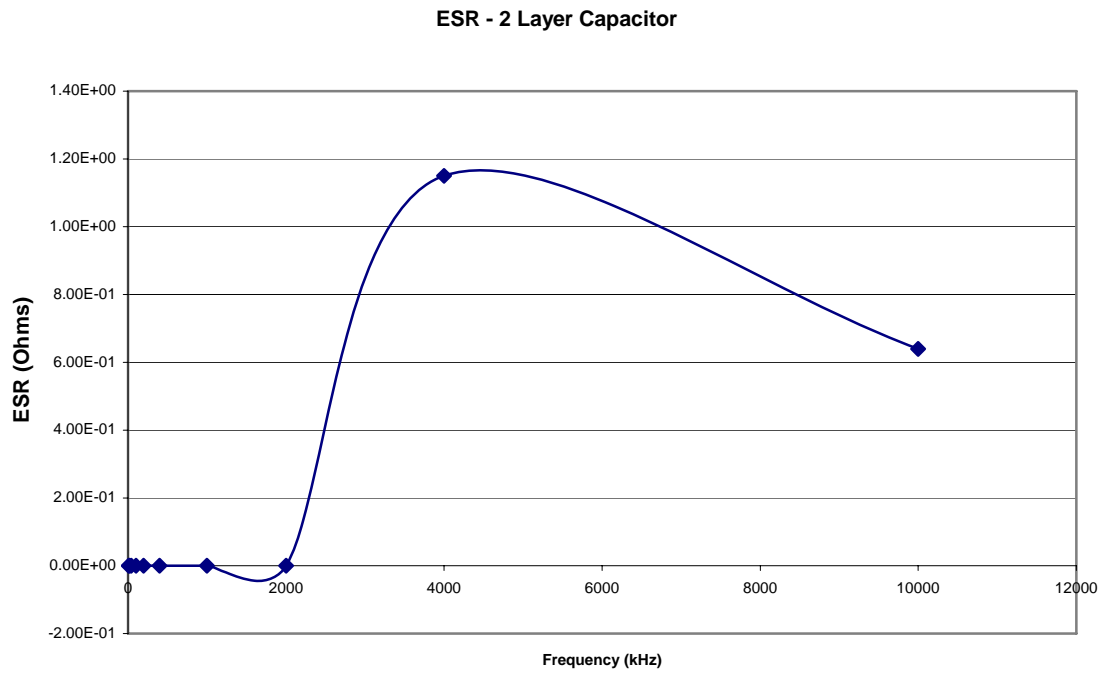


Figure 6.18 ESR vs. Frequency – Two-Layer Diamond Capacitor.

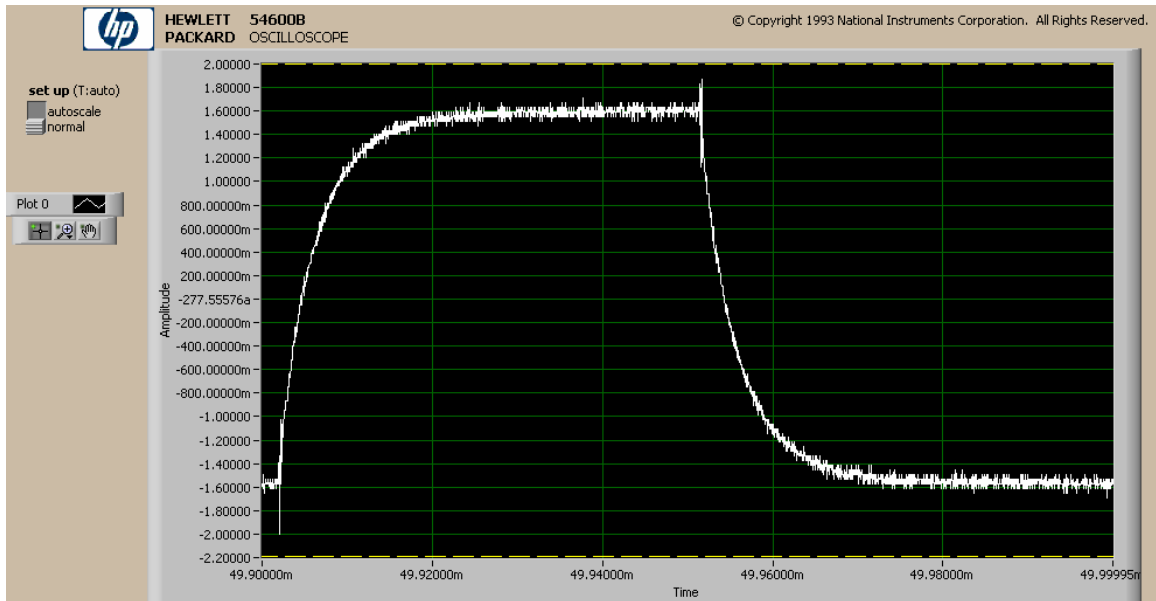


Figure 6.19 Oscilloscope Capture of Dual-Layer Capacitor Charge-Discharge Behavior.

After the two-layer device had been successfully tested, a three-layer device was created. In the three-layer device Cap 011, Cap 012, and Cap 013 were used. Figures 6.20 – 6.24 illustrate the performance of the tri-film device.

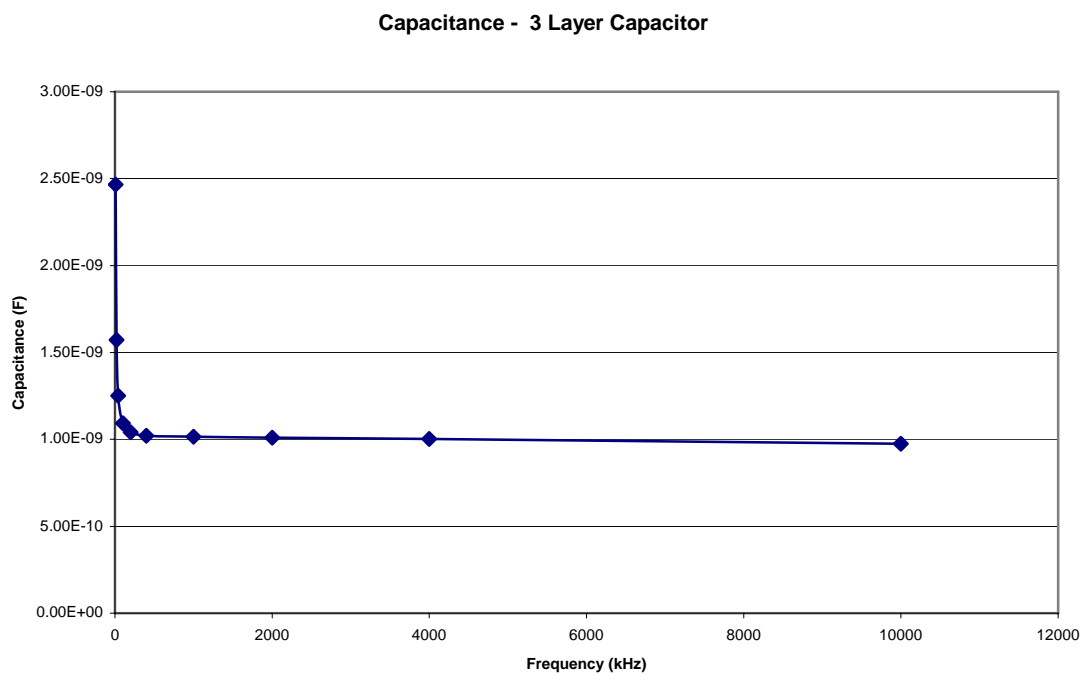


Figure 6.20 Capacitance vs. Frequency – Three-Layer Diamond Capacitor.

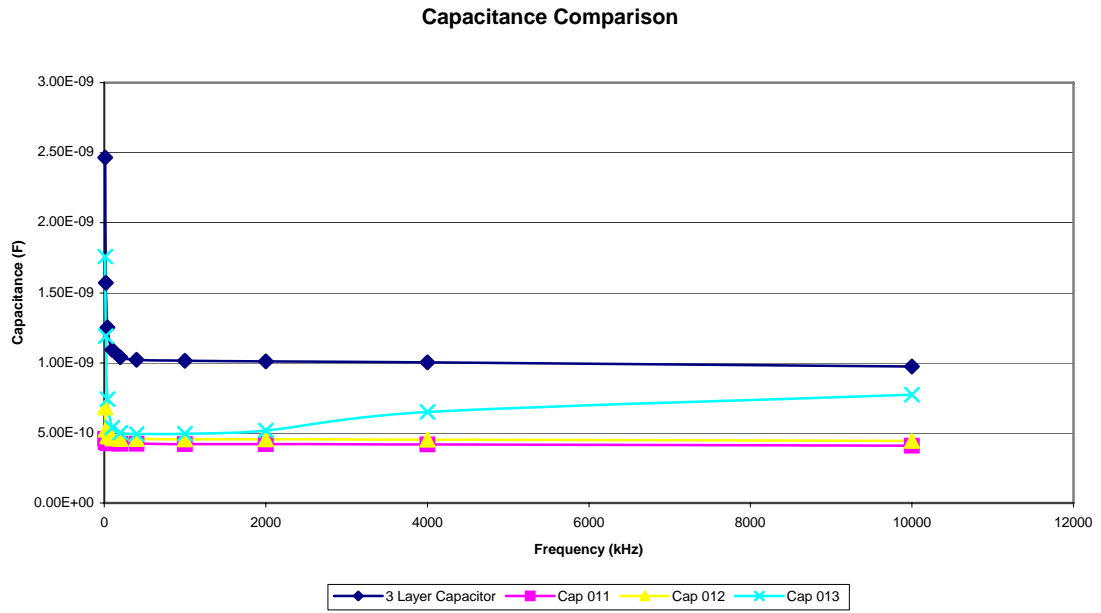


Figure 6. 21 Comparison of Capacitance of Triple-Layer Capacitor and Individual Device Layers.

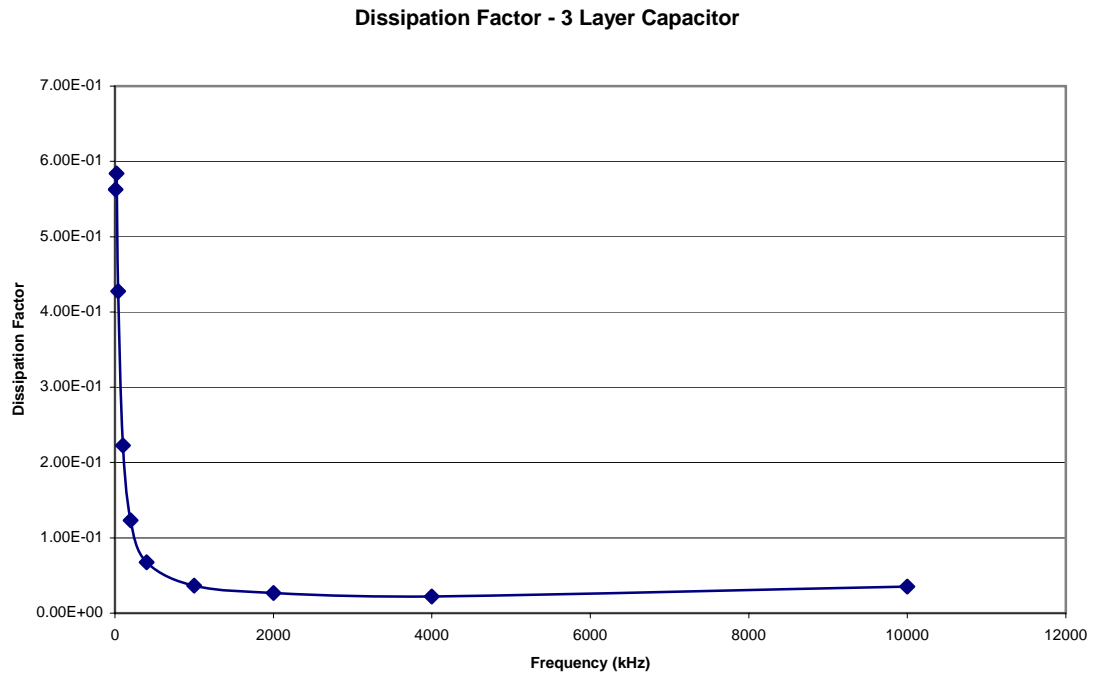


Figure 6. 22 Dissipation Factor vs. Frequency – Three-Layer Diamond Capacitor.

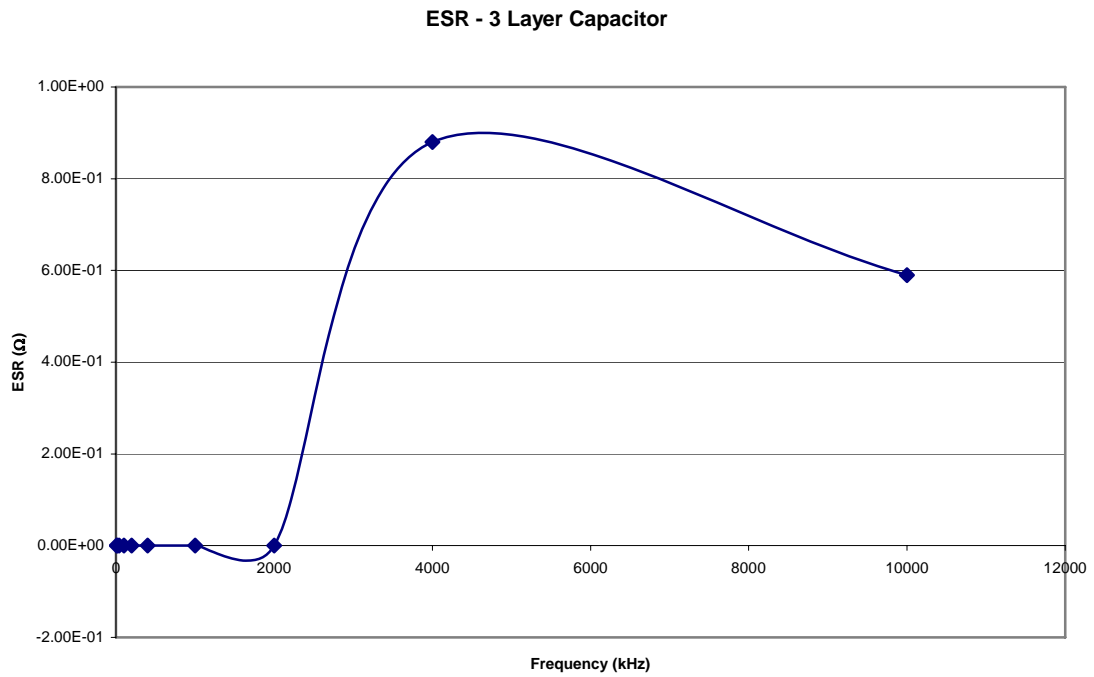


Figure 6. 23 ESR vs. Frequency – Three-Layer Diamond Capacitor.

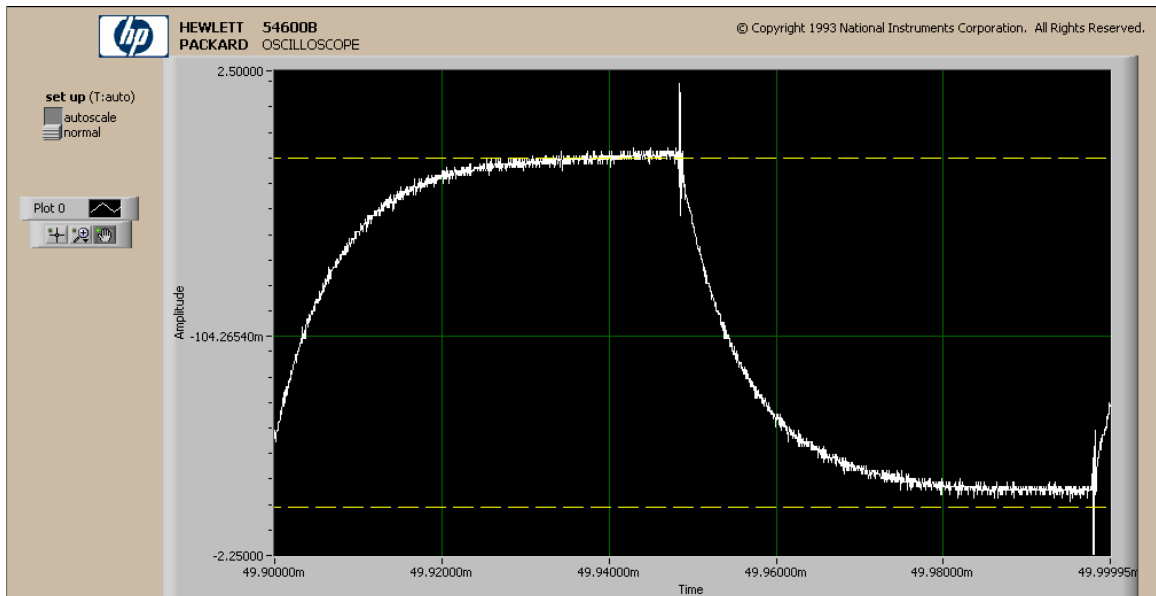


Figure 6. 24 Oscilloscope Capture of Triple-Layer Capacitor Charge-Discharge Behavior.

The three-layer capacitor exhibits similar performance to the two-layer capacitor. From the data it can be seen that the capacitance of the three-layer device is greater than that of the individual samples. The dissipation factor and ESR are shown. Charge-discharge behavior, Figure 6.24, can be seen from the oscilloscope data. Table 6.4 and Table 6.5 summarize the performance of the multi-layer capacitors.

Table 6.4 Summary of Multi-Layer Diamond Capacitance Behavior.

	<i>2- Layer Capacitor</i>	<i>3 -Layer Capacitor</i>
<u>Frequency (kHz)</u>	<u>Capacitance (F)</u>	<u>Capacitance (F)</u>
10	1.14E-09	2.47E-09
20	8.93E-10	1.57E-09
40	7.63E-10	1.25E-09
100	7.25E-10	1.09E-09
200	7.13E-10	1.04E-09
400	7.09E-10	1.02E-09
1000	6.93E-10	1.02E-09
2000	6.80E-10	1.01E-09
4000	6.70E-10	1.00E-09
10000	6.60E-10	9.75E-10
Average Capacitance (F)	7.89E-10	1.27E-09
DC Capacitance (F)	4.2E-09	6.50E-09

Table 6.5 Comparison of Additive Capacitance Individual Device Layers vs. Multi-Layer Capacitors.

	Capacitance (F) at 10 kHz
Cap 011	4.58E-10
Cap 012	6.82E-10
Cap 013	1.76E-09
Sum of Layers 1& 2	1.14E-09
2 Layer Capacitor	1.14E-09
<u>Percent Difference</u>	
0.0%	
Sum of 3 Layers	2.90E-09
3 Layer Capacitor	2.47E-09
<u>Percent Difference</u>	
14.8%	

The data shows that there is an expected additive effect on the capacitance as layers are combined together. Table 6.5 shows that a device with larger capacitance is indeed achieved from adding layers of different capacitances. The capacitances of the multi-layered devices are comparable to those expected from a direct parallel addition of individual layers. A similar observation can be made by examining the DC capacitances of the devices. The DC capacitances of the dual and triple layer devices are greater than or equal to those of the individual layers. Differences between the calculated parallel capacitances and the measured multi-layer capacitances may be due to loss factors such as contact resistances between foil layers and resistances at the interfaces between the copper foil and silicon substrates.

Monolithic Multi-Layer CVD Diamond Capacitor

In a parallel effort to explore the dielectric behavior of multi-layer capacitors, a monolithic layered device was devised. By growing thin layers of diamond on alternating layers of thin film metal, a contiguous dielectric structure could be created. By adding layers of equal thickness, the cross sectional area and therefore capacitance of the device can be increased.

In the monolithic design concept (see Figures 6.5, 6.26), geometric accuracy is vital to the electrical integrity of the device. To ensure consistent alignment of the conduction and dielectric layers, a set of quartz deposition masks were designed and produced, as shown in Figure 6.25.

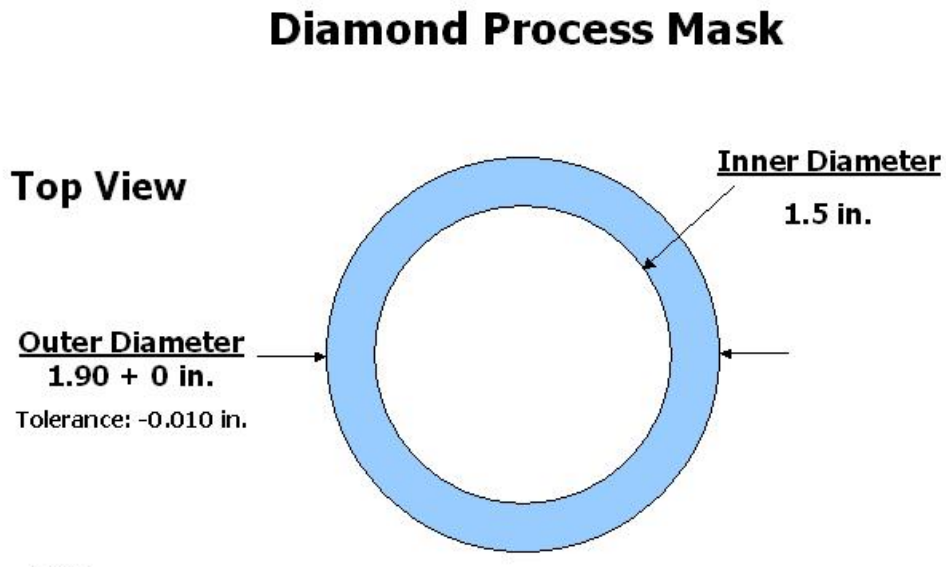


Figure 6.25 (a) Quartz deposition process mask design for diamond layers of monolithic multi-layered diamond capacitor.

Conductor Process Mask

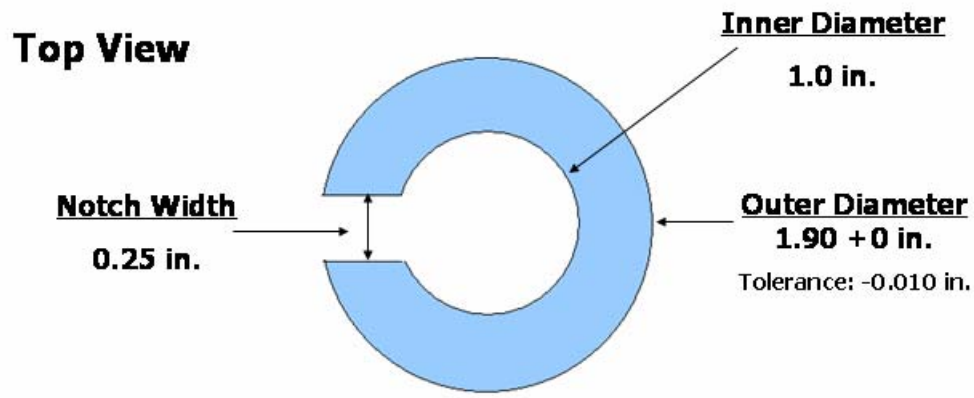


Figure 6.25 (b) Quartz deposition process mask design for conduction layers of monolithic multi-layered diamond capacitor.

Quartz was chosen as the masking material due to its ability to withstand the rigors of the CVD growth environment. Quartz pieces were laser cut to the design specifications and produced in a variety of thicknesses. This offered a degree of flexibility in mask choice for differing growth conditions.

Monolithic Multi-Layer Structure

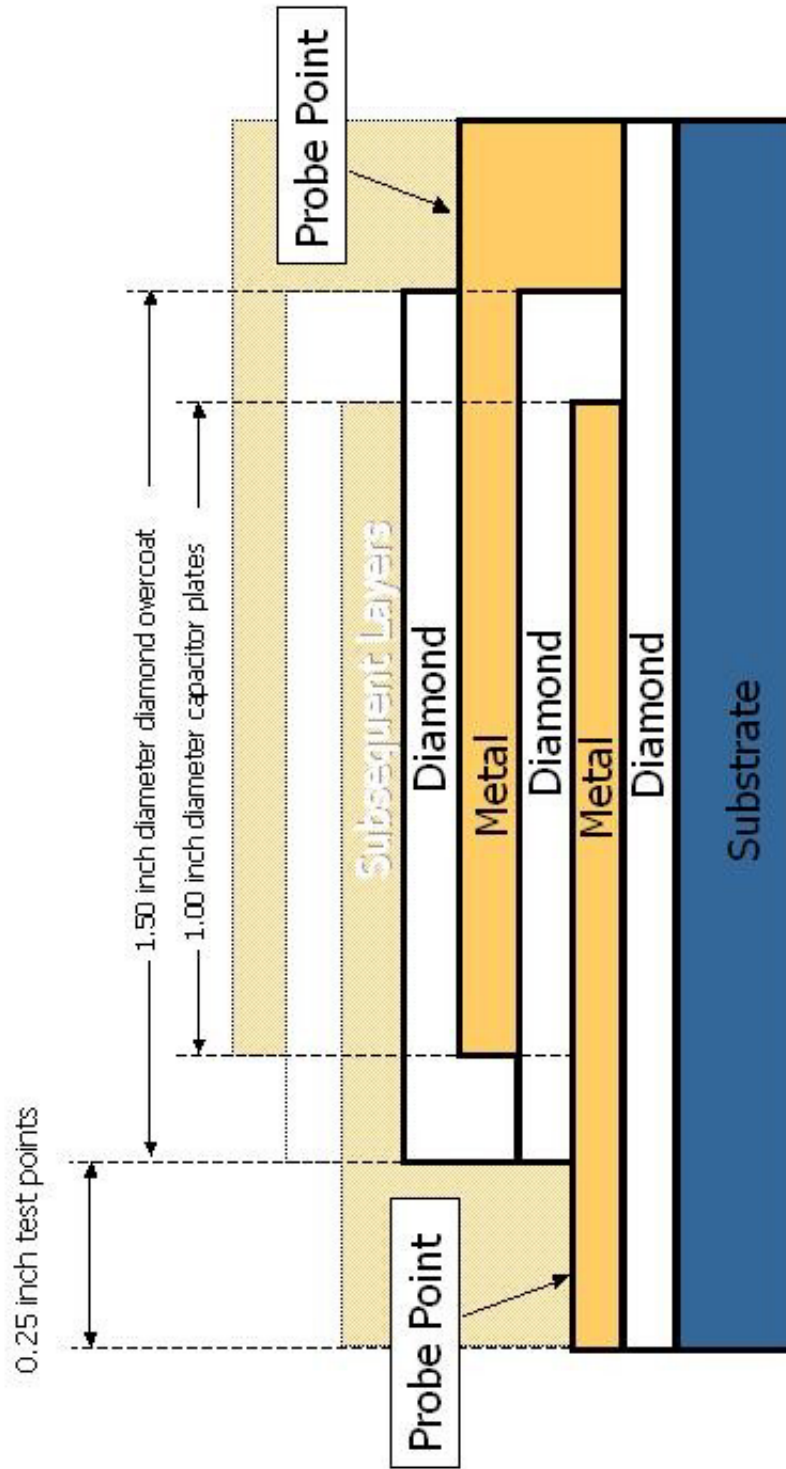


Figure 6.26 Monolithic Multi-Layer Design Cross-Section

Diamond Dielectric

The first step in the growth process was the creation of the base diamond layer. Silicon was used as the substrate for the base layer. For electrical consistency and process repeatability, all of the diamond layers were produced with identical conditions. The dielectric diamond was produced under the “smooth” program. This process is referred to as “smooth” because the finer grains produced by the process yield a more even, uniform surface morphology. The surface will therefore appear to be more “smooth” than that of other standard deposition processes when observed under high magnification. The deposition parameters were as below.

Table 6.6 CVD Diamond Smooth Process Deposition Parameters

Deposition Parameter	Smooth Deposition Process Values
Temperature	875 °C
Pressure	11.35 Torr
H ₂ content	400 sccm
CH ₄ content	4 sccm
Power	650 W
Deposition Time	6 hrs

The smooth process is often preferred for dielectric diamond due to the smaller grain boundaries and grain spacing in the deposited product. The major disadvantage is the

greater use of materials necessary for production of significant thicknesses. Fortunately, thinner diamond layers are preferred for dielectric applications.

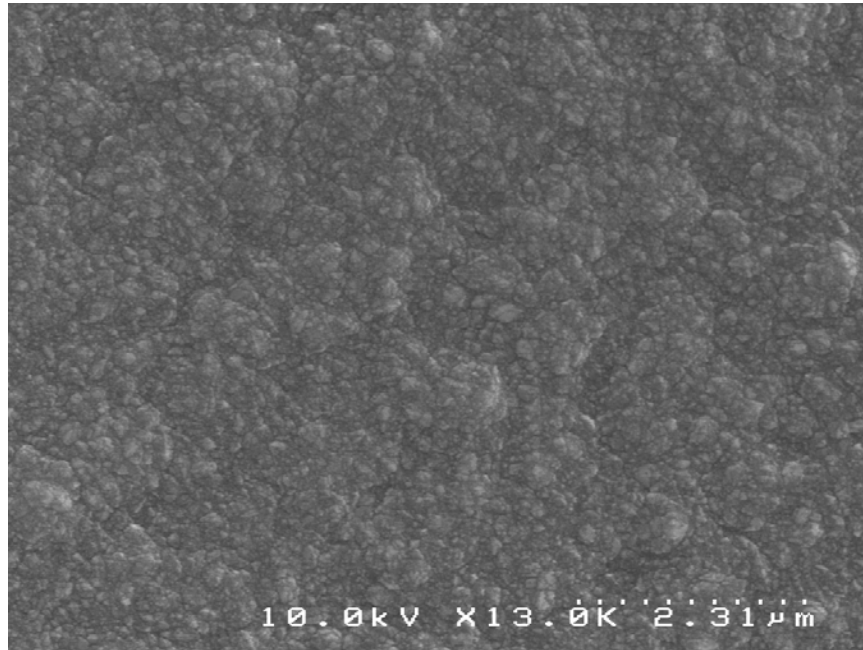


Figure 6.27 SEM photograph of base diamond layer surface morphology.

Conduction Layer

The conduction layers are ultimately the most important components of the design. They serve as the structural and electrical bridges to all of the dielectric layers of the device. The conduction layers are also, however, the most problematic element. For the monolithic prototype the conduction layers were composed of a titanium-nickel (Ti-Ni) composite that was sputtered onto the surface of the capacitor. The application of the metal was performed using a Materials Research Corporation (MRC) Type 8667A 3 kW RF Sputtering System. The sputtering details were as below. Sputtering was performed in an ambient argon atmosphere.

Conduction Layer Sputtering Profile

- Ti: 5 min., 350W
- Ni: 10 min., 350W
- Pressure: 7mTorr

Unlike the mechanical multi-layer capacitor, for which the choice of conductor materials is limited only by the availability of the chosen metal in a foil form, the selection criteria of conductor materials is pivotal for successful metallic adhesion and diamond growth. The conduction layer must both be able to provide electrical stability and serve as the substrate for the next layer of dielectric diamond. High quality diamond coatings are difficult to achieve on metal substrates for a number of reasons. Poor film adhesion occurs for many systems in part because of the large mismatch in thermal expansion coefficient between diamond and the metal substrate. At the temperatures required for diamond growth, this leads to large residual stresses at the film/metal interface and can cause delamination. In addition, some metals undergo chemical reactions during the CVD

diamond deposition process (typical growth temperatures > 700 °C) adversely altering the properties of the substrate and preventing growth of the film [60].

For successful deposition, diamond films need a surface which is stable with respect to carbon. For CVD applications, the surface material must also have a high melting point. This limits the number of metals that can be used for this design. Refractory metals, such as Ta, Ti, W, and Mo, are promising candidates as substrate materials [61]. The excellent heat, wear, and corrosion resistance of these materials provides an innate advantage over other metals when used in CVD applications. These materials will form carbides during diamond deposition. The carbide layer serves to stabilize the surface for carbon growth. For Ti, in particular, investigations by Perry and Terranova [60,61] have shown that there are multiple intermediary layers between the Ti surface and a CVD diamond film. These layers are comprised of titanium carbide (TiC), titanium hydride (TiH), graphite, and amorphous carbon. The effects of the interfacial non-diamond layers are twofold. Foremost, the intermediary areas can cause structural stresses that can damage the overlying diamond film. The diamond film will tend to delaminate from the surface of the metal substrate. This phenomenon has been previously observed and documented in this report in the evaluation of tungsten as a suitable substrate for dielectric diamond (See Chapter V). The secondary concern is the fact that the conductivity of the film can be altered by the introduction of the amorphous carbon species in the diamond matrix. In the case of the monolithic capacitor, where the thickness of the conductive layer is small, these issues form a credible threat to the successful growth of additional dielectric layers. Therefore, pure Ti was dismissed as a candidate for the metal layers.

Other non-refractory metals such as Ni, Fe, and Co have been used as substrates for diamond growth. The major problem with these metals is that many of these materials are subject to carburization. The diffusion of carbon into the surface affects the metal in numerous ways. The nucleation mechanism of diamond is suppressed by the reactions between radicals and the substrate surface [62]. This leads to a low particle density.

Of the materials above, Ni has shown the greatest ability to promote diamond growth. The major advantage of a Ni substrate is that diamond can be deposited without the formation of carbide or other carbonaceous interfacial layers. For this reason, any subsequent dielectric layers would be more structurally robust than that grown on a refractory metal. The major disadvantage of using pure Ni as the conduction layer is the unfavorable interaction between Ni and the dielectric layer on which it is deposited.

Eimori *et al*, have shown that the diamond surface changes in electronic structure just after the deposition of nickel. Significant graphitization occurs during the annealing the film. After annealing, nickel strongly diffuses into the CVD diamond film [63]. These results are mainly attributed to the catalytic nature of nickel and the mutual solubility between carbon and nickel. There are no such reported interactions between titanium and the diamond surface.

To make use of the advantages of Ti and Ni and yet minimize the disadvantages of each metal, it was decided to use a Ti-Ni composite as the conduction layer. The Ti was sputtered first to suppress the adverse reactions between Ni and the base diamond layer. Ni was sputtered as the secondary conduction layer to suppress the structural mismatches between Ti and the to-be-deposited diamond layer.

The most tenuous part of the construction process is undoubtedly the metal-diamond interface. If the CVD process cannot be sustained on a thin metal substrate, the design will not be viable. Additionally, the deposited diamond of subsequent layers must remain non-conductive to function as viable dielectric layers. Figure 6.28 shows a base dielectric layer with a single deposited conduction layer.

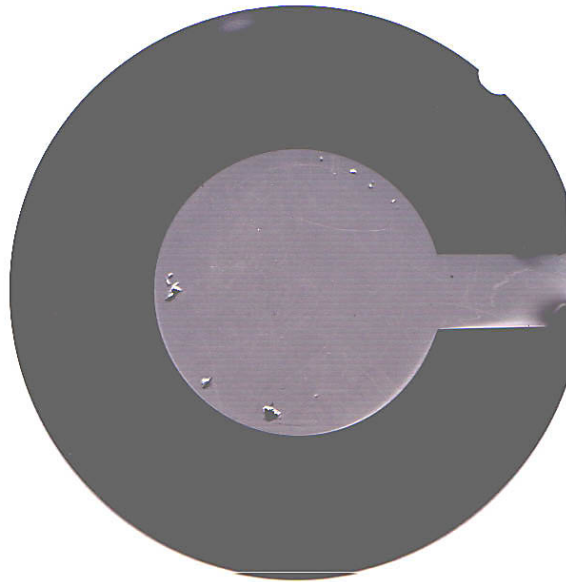
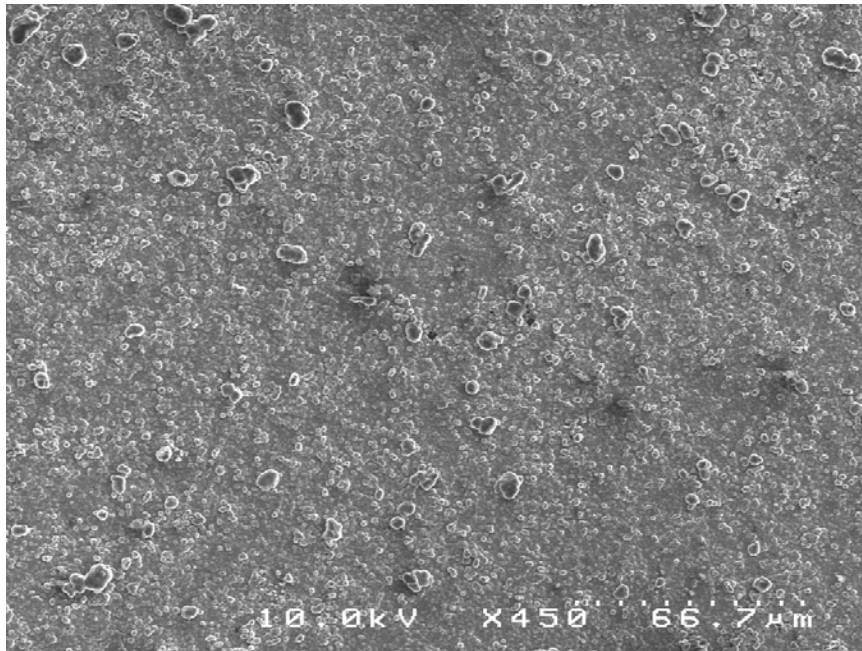


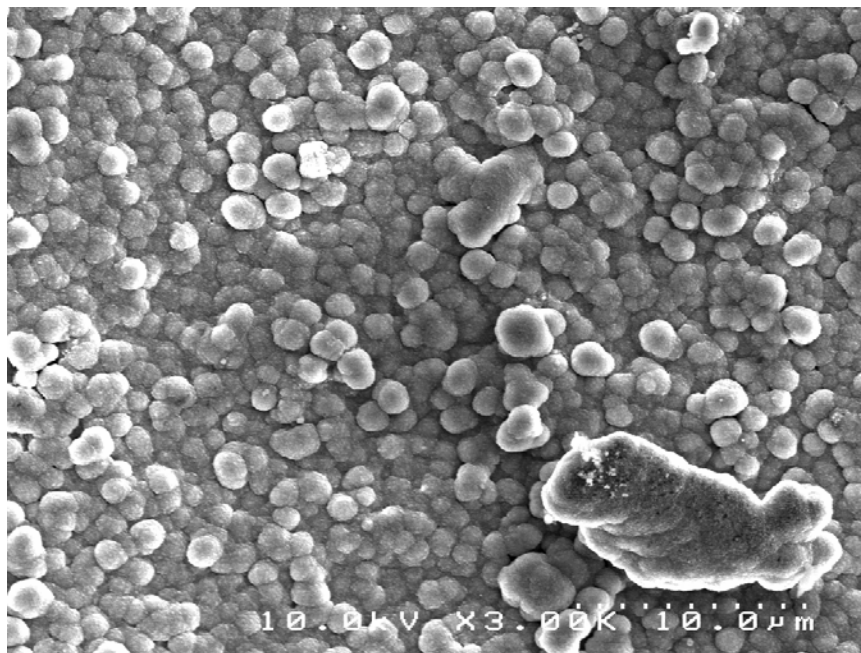
Figure 6.28 Base layer of monolithic diamond capacitor with single layer of sputtered Ti-Ni Conduction layer.

Aluminum foil wrapped around the edges of the device was used to secure the mask in place. Slight position shifts during the alignment of the sputtering machine led to minor misalignments of the conduction mask and subsequently deposited conduction metals.

Aside from the imperfections above, the deposited metal layer appears to be structurally sound. Figures 6.29 and 6.30 show the metal surface and interface region as viewed from a scanning electron microscope.

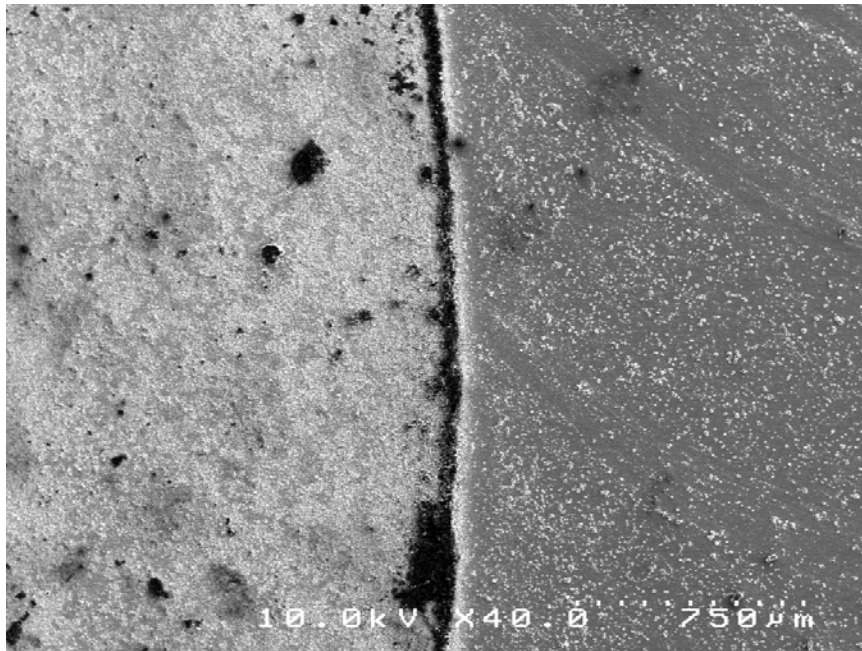


(a)



(b)

Figure 6.29 Nickel layer of single layer monolithic capacitor. (a) 450X, (b) 3000X



(a)



(b)

Figure 6.30 Interface region between Ti-Ni conduction layer and diamond dielectric layer of single layer monolithic capacitor. (a) 40X zoom, (b) 350X zoom

Characterization

Since the monolithic nature of the design would physically bond any constituent dielectric layers together during the construction of the device, the analysis of individual sections of the capacitor had to be performed at each step of the deposition process. The primary construct for characterization purposes was a two layer capacitor. It has been well demonstrated that single layer diamond capacitors can be successfully created. The successful addition of a second layer was the benchmark by which the monolithic capacitor was judged. The evaluation of the electrical and structural characteristics was the criteria by which this determination was made. It should be noted, however, that superior electrical performance was not one of the considerations by which the success of this class of capacitors was judged. This device primarily serves as a prototype to evaluate the validity of the design and construction techniques for this particular advanced capacitor geometry.

While not structurally perfect, the electrical characteristics of the conduction layer and diamond-metal interface were useful for the prototype capacitor. When probed at various points around the surface of the Ti-Ni layer, electrical conductivity and continuity was maintained. Using the Ti-Ni layer as an electrical contact, the base diamond layer was subjected to I-V analysis. Special care was taken to not scratch or otherwise damage the Ti-Ni layer during the leakage test. Any significant damage to the conductor film during the characterization stage would compromise the ability of the device to support additional diamond layers. I-V analysis was performed using a Keithley 6517A Electrometer. Figure 6.31 shows a typical leakage profile for the first dielectric layer.

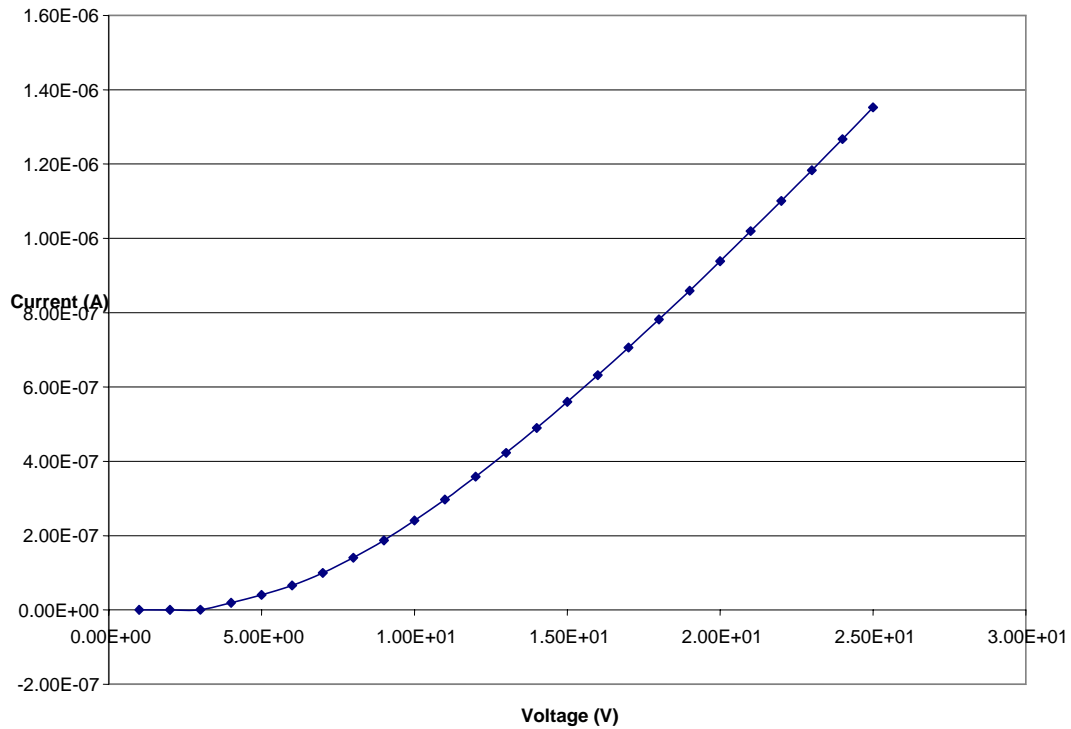


Figure 6.31 Leakage profile of base layer of monolithic diamond capacitor.

The graph illustrates the current profile for thin dielectric diamond structures. The current exhibits a short linear (ohmic) region followed by an exponentially increasing region.

Since the results for the base layer were acceptable, it was decided to proceed with the addition of a second dielectric layer to the structure. To prepare the prototype for the deposition of a second layer of diamond, the top conductor layer had to be carefully pre-treated with diamond powder to promote nucleation on the metal substrate. To accommodate the thinness of the metallic layer, the surface was subjected to ultrasonic agitation with diamond powder. The previous nucleation study (See Chapter V) showed that adequate nucleation could be obtained by sonicating the surface with microdiamond

particles. After this pre-treatment the capacitor was reintroduced to the CVD chamber with the diamond layer process mask. A diamond film layer was deposited using the smooth diamond process described earlier.

Immediately after deposition, the prototype was visually inspected for physical damage and defects. The two layer monolithic capacitor prototype is shown in Figure 6.32.

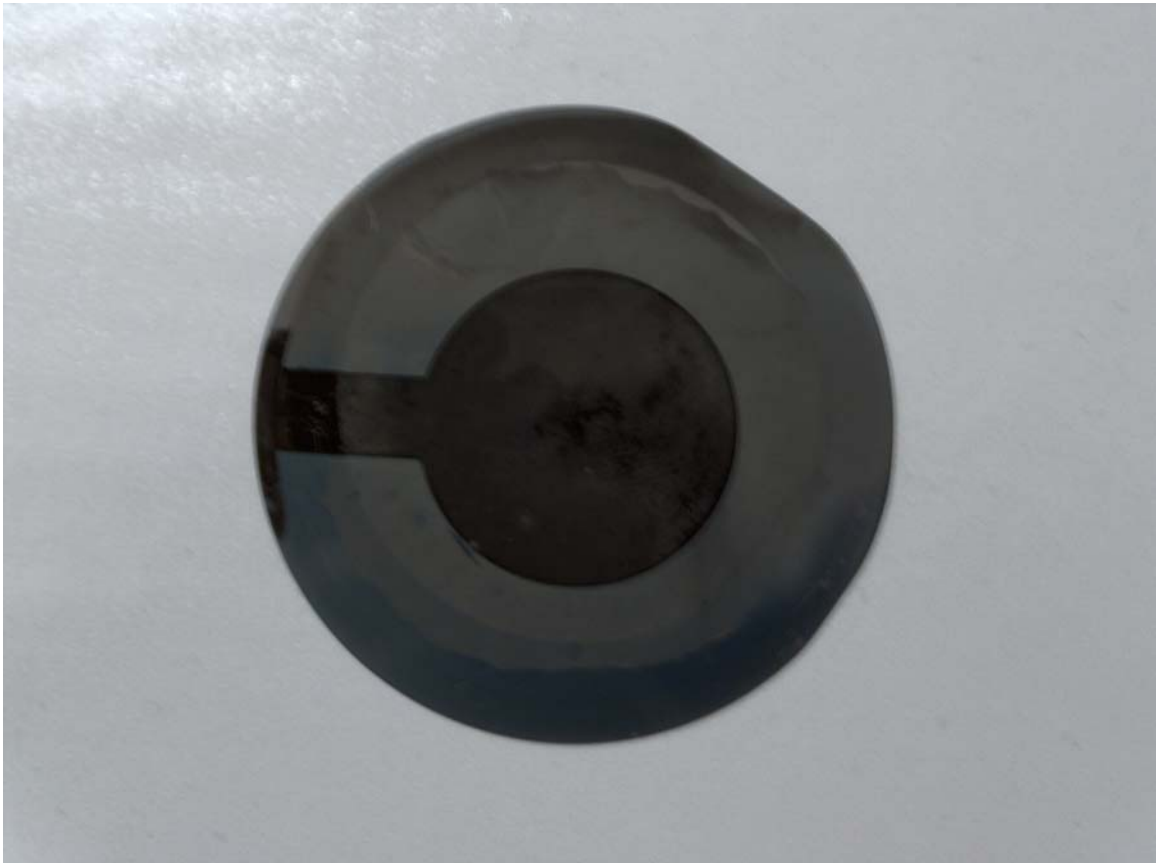


Figure 6.32 Monolithic diamond capacitor after deposition of second dielectric layer.

Unlike the smooth grayish surface of the first diamond layer, the second diamond layer was dark in appearance. In the region directly atop the Ti-Ni layer, the deposited substance was loose and granular in nature. After preliminary inspection, the sample was

once again subjected to I-V characterization. Figure 6.33 shows a comparison between the leakage profiles of the two dielectric layers of the prototype. Layer 1(i) refers to the base layer before the addition of the second layer. Layer 1(ii) references the first layer after the deposition of the second layer. Layer 2(a) and Layer 2(b) refer to the second layer at different locations along the surface.

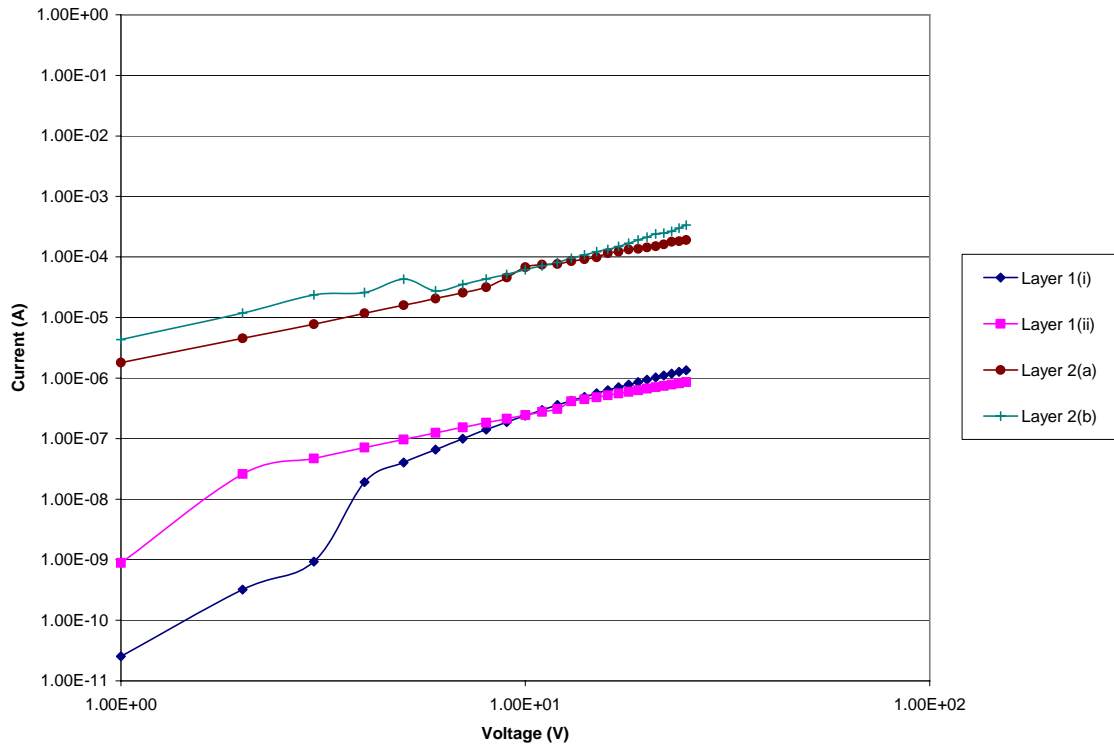


Figure 6.33 I-V comparison of dielectric layers of monolithic diamond capacitor.

The second layer was examined in different locations along the surface because of the inconsistency of the deposited surface material. Typical profiles for the different regions of the second layer are referenced in Figure 6.33 as Layer 2(a) and Layer 2(b). As shown in the figure, the leakage of the second layer is considerably higher (several orders of

magnitude) than that of the first layer. The profile indicates that the material may still exhibit dielectric properties even though the conductivity is greater than the diamond of the first deposited layer. Next, the leakage behavior of the combination of the layers was characterized. A comparison of the individual and combined I-V profiles is shown in Figure 6.34

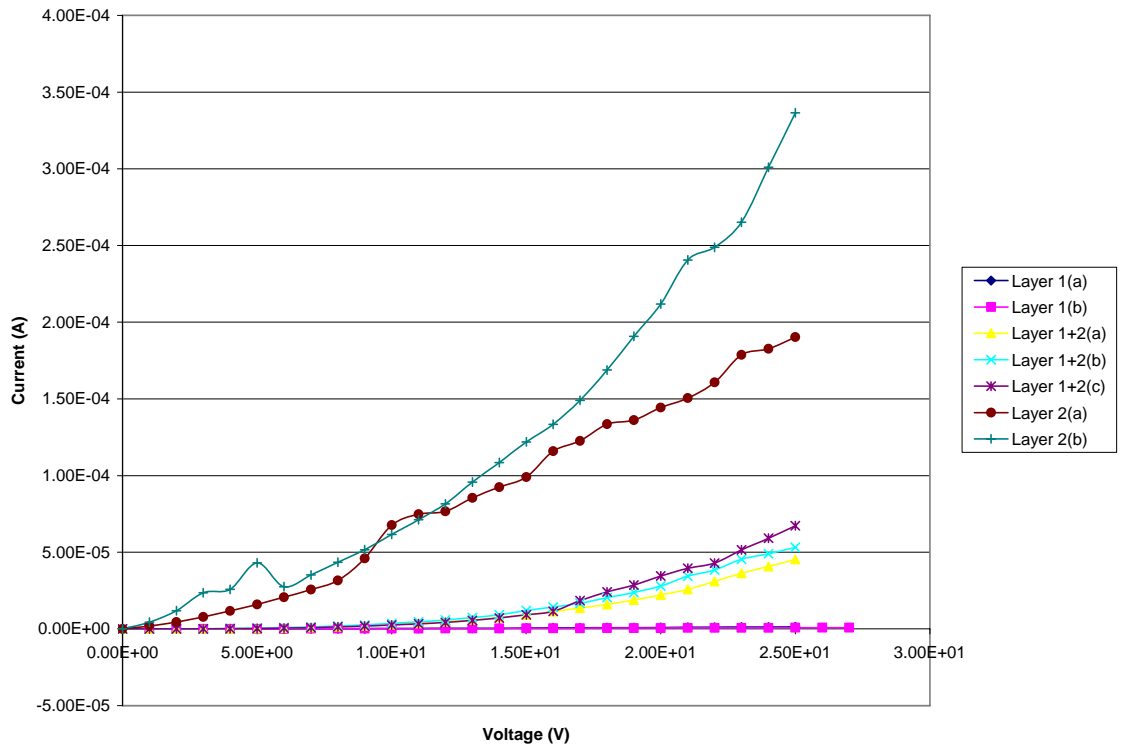
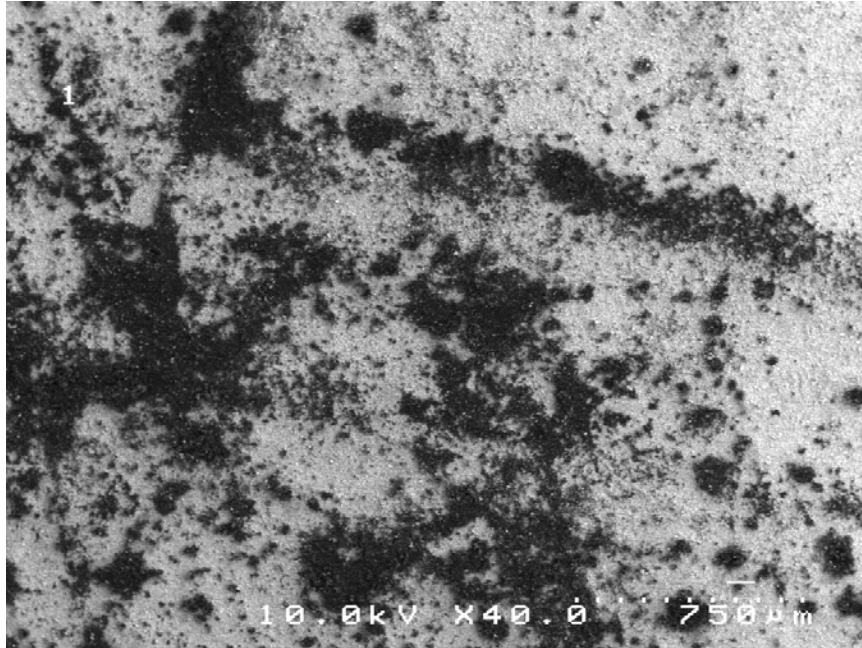


Figure 6.34 Leakage profile comparison of individual dielectric layers and composite dielectric of monolithic diamond capacitor.

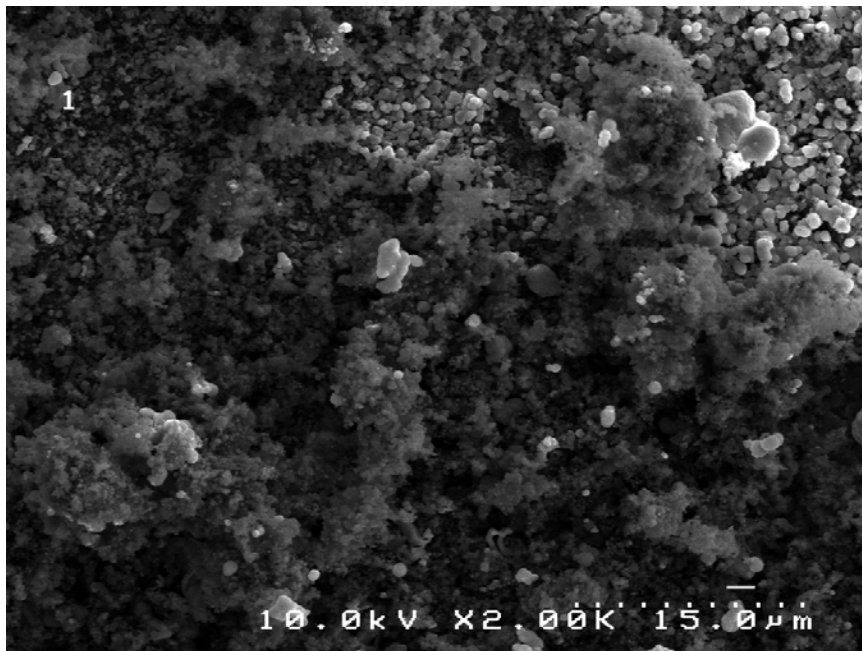
It can be clearly seen from Figure 6.34 that the material deposited as the second layer diminishes the overall dielectric capacity of the prototype. The leakage current in the combination of layers is not as high as the second layer individually, but it is markedly larger than the leakage of the first diamond layer.

Scanning electron microscopy, as shown in Figure 6.35, was used to image the surface of the second layer. The dark regions represent the material deposited as the second dielectric layer. The lighter regions correspond to the underlying Ti-Ni electrical contact. The SEM images show that the second layer is not evenly distributed atop the Ti-Ni layer. The material is contiguous in clustered regions that are randomly spread across the metal surface. The dark material appears to be an undetermined non-diamond phase. The coloring and morphology of the dark material is consistent with that interpretation. Closer examination of the SEM images reveals that there are actually two different types of material that were produced during the second deposition. Intermixed with the other deposition byproducts are several clusters of larger globules, as shown in Figure 6.36. The globules appear to be carbonaceous; however, do not appear to be diamond. While these clusters can be found throughout the deposition area, they are the most heavily concentrated in the regions outside of the Ti-Ni contact area.

Two major processing issues are present in the second dielectric layer. The first factor is the quality of the film. As noted, the materials that were deposited as the second layer were not representative of quality polycrystalline diamond. Both structurally and electrically, the materials do not exhibit attributes consistent with dielectric films. Studies by Kawarada *et al.* [62] have reported on the difficulties of growing diamond on carburizing metals. Oftentimes, the results of the deposition are various forms of

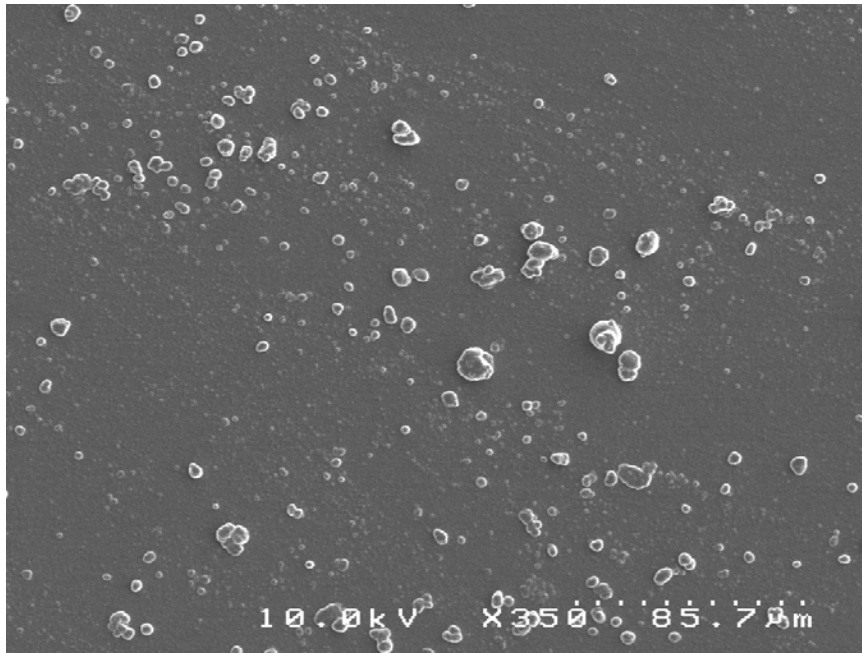


(a)

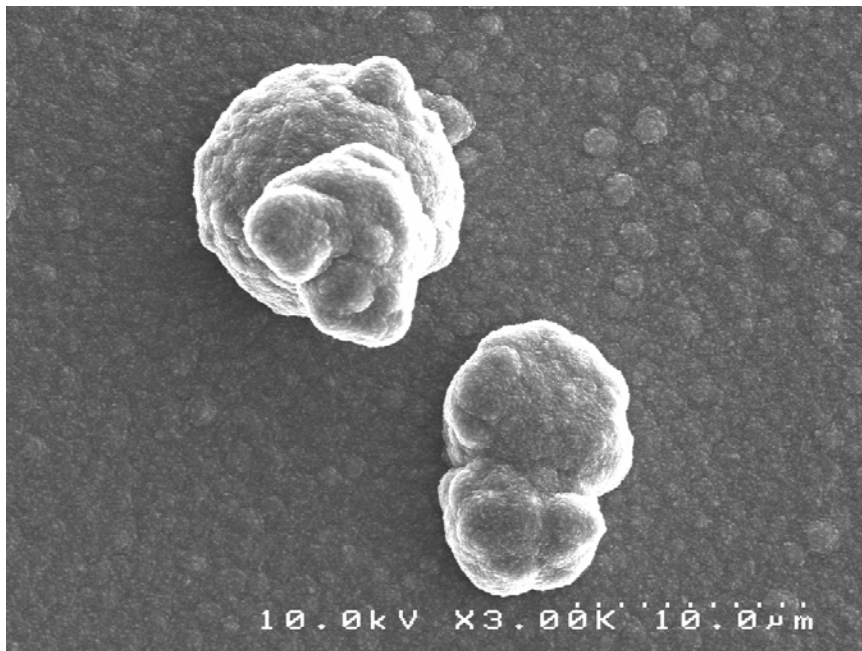


(b)

Figure 6.35 SEM images of second deposited dielectric layer of monolithic diamond capacitor prototype. (a) 40X, (b) 2000X.



(a)



(b)

Figure 6.36 High magnification SEM imagery of second layer carbonaceous particles. (a) 3000X (b) 15000X

amorphous carbon rather than high quality polycrystalline diamond. This is attributed to the inability to stabilize the metal surface with respect to carbon.

The second deposition issue was the density of the film. Regardless of film quality, the film itself was neither cohesive nor continuous. The nucleation density was low. Since the deposition time was greater than 6 hours, it is unlikely that the results would have been markedly different if the growth interval has been extended. More likely, the low nucleation density was due to inadequate nucleation site creation during the pre-treatment phase or due to undetermined chemical reactions between carbon radicals and the Ni surface in the plasma chamber.

Electron Cyclotron Resonance Deposition on Ni

With the failure to create an adequate second dielectric layer for the prototype capacitor, it was decided to examine another process to deposit diamond on a Ni substrate. Identification of a deposition process or the necessary conditions that would produce a stable diamond film on a Ti-Ni contact became the key concern in the development of the monolithic diamond capacitor. The smooth diamond program was used in the first prototype because it had demonstrated useful non-conductive films. Another advantage was the relatively low power, and hence temperature, at which diamond could be synthesized using the process. The solution to increasing the quality and nucleation of the deposited film may lie in increasing the plasma density in the CVD reaction chamber. The downside to this approach is the fact that as the reaction power is increased, the substrate temperature will also increase. If the process temperature is too high, the melting point of the contact layer may be reached, thereby destroying the metal substrate.

To explore this approach, a series of nucleation tests were conducted using silicon substrates that were sputter coated with a Ti-Ni layer. The Ti-Ni layer was sputtered under the same conditions used for the monolithic prototype. Since the goal was the successful synthesis of diamond on Ni, it was not necessary to use samples that already had a base diamond layer. Rather than using one of the standard ASTEX microwave plasma CVD machines, as had been used throughout this research to this point, the electron cyclotron resonance (ECR) CVD deposition machine was applied. ECR deposition is the alternative because it achieves greater plasma densities at lower temperatures relative to the traditional CVD process.

The Principle of Electron Cyclotron Resonance

Electrons placed in an external magnetic field will cycle around a magnetic field line if they have a velocity component perpendicular to the magnetic field. The electron cycle frequency ω in external field B is:

$$\omega = \frac{eB}{m}, \quad (6.4)$$

where e and m represent the electron's charge and mass, respectively. If there is a periodic electrical field perpendicular to the external magnetic field and at the frequency equal to the electron cycle frequency ω , then the electrons will be constantly accelerated like the electron moving clockwise in Figure 6.37. Its path eventually forms an open helix like that in Figure 6.38, and electrons quickly gain energy.

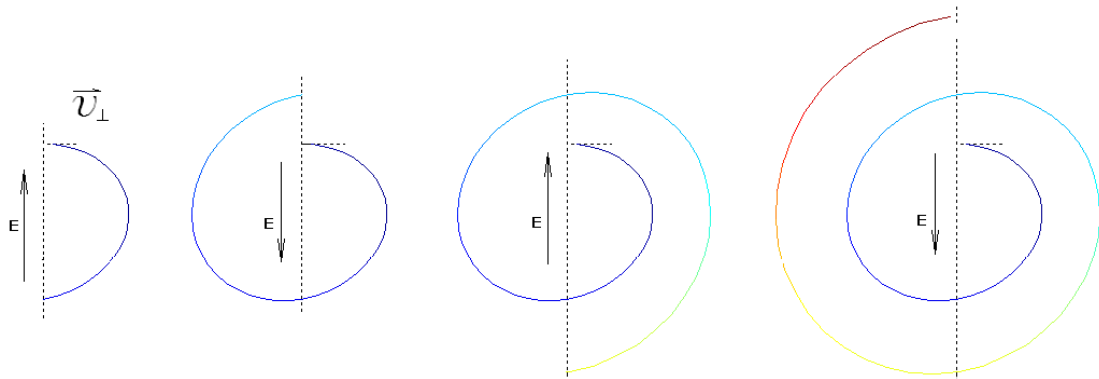


Figure 6.37 Electron being accelerated clock wisely by periodic electric field [64].

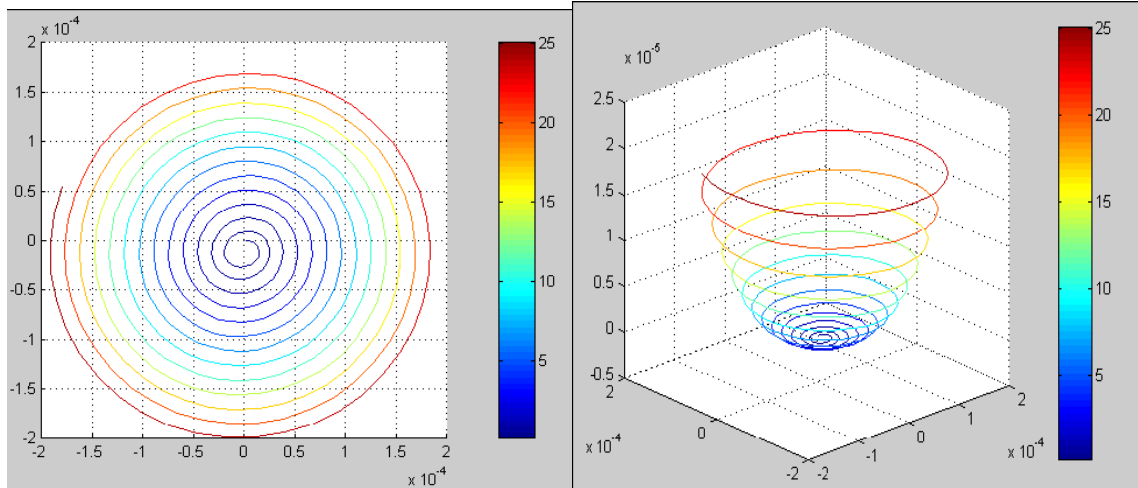


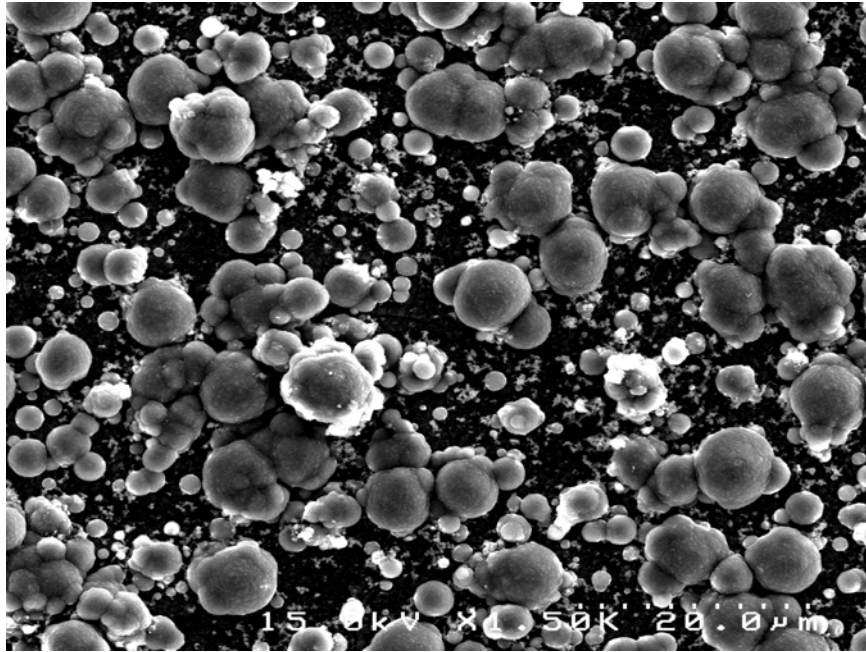
Figure 6.38 Electron's spiral path in external magnetic field superimposed with perpendicular periodic electric field [64].

When the electrons are accelerated to a large enough energy, they will ionize nearby neutral atoms to create plasma. In practical applications, it is not required

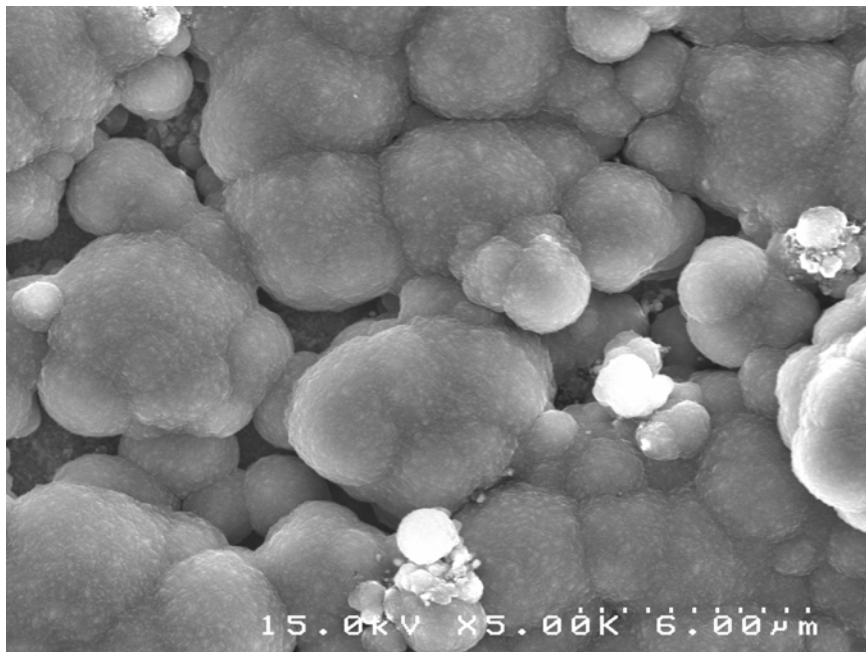
to have a uniform magnetic field to create ECR plasma. Most magnetic fields actually have only a limited shell-like ECR region. RF power absorption mostly happens around the ECR region and keeps the plasma stabilized. As the uniformity of the magnetic field increases, so does the efficiency to make ECR plasma [64].

For the ECR deposition analysis, the test substrates were loaded into the ECR chamber directly without any prior pre-treatment processing. Rather than using the mechanical damage technique to increase diamond nucleation sites, the substrates were under bias from with an external voltage source. For deposition, the substrates were biased at -200V with a 10% CH₄/H₂ ratio. After deposition, the samples were examined with a scanning electron microscope, as shown in Figure 6.39, to see the morphology of the resultant layer.

As indicated in the figure, there was particle growth on the surface of the Ni layer. The growth, however, was not always a contiguous film as evidenced by Figure 6.39(a). Higher magnification images showed that the material that was deposited was very close in size and structure to some of the material found on the prototype capacitor. The bulbous structures do not appear to be polycrystalline diamond. They once again more closely resemble the morphological structure of amorphous carbon. These results are consistent over a range of Ti-Ni samples with varying thicknesses. The experiments with ECR deposition continue, but have thus far not achieved useful films.



(a)



(b)

Figure 6.39 SEM photographs of ECR film deposited on Ti-Ni layer substrate. (a) 1500X, (b) 5000X

CHAPTER VII

SUMMARY AND CONCLUSIONS

CVD diamond has proven to be a viable material for creating dielectric films. The dielectric behavior and properties of diamond has been studied by a number of researchers. Research, however, has been limited to basic characterization of simple dielectric devices.

As this research has shown, the single most important parameter in the development of diamond dielectric capacitors is electrical conductivity. Conductivity affects all electric mechanisms in a polycrystalline diamond film. Much of this research effort was devoted to analyzing the conduction mechanisms of CVD diamond films. The control and/or suppression of these conduction mechanisms determine the dielectric properties of CVD diamond. Diamond was grown on different metals to evaluate the dielectric properties of polycrystalline diamond deposited on different carbide forming substrates. In addition to the principal substrate, Si, diamond was grown on substrates made of W and Mo. Diamond grown on tungsten proved to be impractical for dielectric applications due to the fact that structural mismatches between the materials caused damage which compromised the electrical integrity of the films. Diamond grown on Mo substrates exhibited favorable electrical results. The thickness of those films, however, limited the capacitive range that could be evaluated.

The role of annealing in the production of quality dielectric diamond was explored. It was observed that annealing diamond films at moderate to high temperatures is enough to

break the residual hydrogen bonds that appear across the surface of a diamond film after it has been exposed to an ambient atmosphere. These hydrogen bonds on the surface of the diamond film form an accumulation layer that forces band bending along the Fermi level of the diamond surface when exposed to the atmosphere. When exposed to water vapor, electrons are transferred to the surface of the film through this accumulation layer, thus creating a surface conduction layer that retards the dielectric performance of the film.

By limiting the exposure of the diamond surface to the atmosphere, the electrical performance of the films can be greatly enhanced. A series of moisture-proof, encapsulated capacitors were designed and constructed for this purpose. This “Black-Potted” series of capacitors were electrically characterized and exhibited superior behavior. These capacitors were also examined in an aging trial. The performance was reevaluated after a period of dormancy. Little change was observed in the electrical behavior of the devices demonstrating that the encapsulation technique was successful in preserving the dielectric properties of the films by eliminating the exposure to atmospheric water vapor.

The encapsulation trials primarily dealt with surface conductivity in diamond. Conduction through the grain boundaries of diamond films is another important concern. The grain boundary content related to the overall structure of the diamond film was examined. Conduction can be enhanced along grain boundaries because defects and non-diamond phases exist at these grain boundary interfaces. Annealing of the diamond film can diminish some of these effects by forcing the movement of mobile defect carriers within the diamond lattice. The annealing process, however, cannot alter the underlying

causes of the defects, which relate to the growth mechanisms of CVD diamond. It was postulated, however, that by increasing the number of nucleation sites on a substrate, the growth of diamond nuclei on the substrate can be affected. For this effort a sample set of substrates were created with different levels of pre-treatment. Pre-treatment was accomplished by immersing the substrate in an ultrasonic bath of diamond powder. Different powder sizes were used to examine the size of diamond particles necessary to provide optimum preparation and seeding of the surface of the substrate. After preparation, diamond was deposited onto the samples under identical conditions and the nucleation density was measured. The results showed that the samples that were pre-treated with microdiamond sized particles exhibited higher nucleation densities than those treated with nanodiamond. This result is postulated to be due to the higher impact energy that the larger microparticles make with the surface of the substrate in comparison to nanosize particles. Such impacts achieve more active nucleation sites on the substrate, and hence a higher nucleation density. With increased nucleation density, the growth of diamond nuclei is more compact and the conduction pathways through the grain boundaries are reduced, resulting in less measured leakage current. By reducing the effects of the major conduction mechanisms present in polycrystalline diamond, the quality of diamond dielectrics, and the application range of diamond capacitors can be greatly enhanced.

Part of this research effort also focused on the design and development of advanced capacitor structures using CVD diamond. As expressed earlier, all published work on diamond dielectrics has been limited to basic characterization experiments with simple capacitive structures. Experiments proceeded in this research that produced multi-layer

diamond capacitors. Multi-layer specimens have shown increased capacitances with increasing layers of diamond film dielectric. The first multi-layer structure was based on the concept of increasing the capacitance by taking advantage of the additive nature of electrically parallel capacitors. Discrete single-layer diamond capacitors were created and characterized. These individual layers were interconnected with foil metal contacts in parallel. Two-layer and three-layer structures were constructed and characterized. Capacitance and leakage profiles were measured. Charge-discharge behavior and dielectric loss levels for the individual layers and for the composite multi-layer structures were quantified.

The second type of multi-layer structure studied was based on the idea of increasing the capacitance by increasing the area of the capacitor. By increasing the stacked surface area of the capacitor without changing the dielectric thickness, the capacitance of a parallel-plate capacitor will be increased. This concept was explored by designing a monolithic multi-layer structure in which diamond and metal layers would be deposited in a manner to finish with a monolithic multi-layer capacitor. This design was more difficult and complex involving the use of multiple deposition masks and multiple materials. Results were not favorable for the monolithic prototype. The failure to create an adequate second dielectric layer using the metal contact layer as the substrate stalled this effort. Forms of graphite and amorphous carbon, rather than polycrystalline diamond, were observed as the result of the second deposition. Continued study on methods to stabilize the surface of Ni with respect to carbon and exploration of different deposition methods or electrode materials is a future possibility.

CHAPTER VIII

FUTURE WORK

The results of this study have been successful in establishing a base from which additional work on the behavior of advanced polycrystalline diamond capacitors can emerge. More experimentation and development, however, is needed to optimize the potential of CVD diamond as an effective dielectric material. The following items remain as areas of continued research.

1. Conduction Mechanisms in Diamond
 - a. Optimization of annealing techniques and annealing technology
 - b. Refinement and further deployment of encapsulation techniques
 - c. Raman analysis of nucleation sites and grain boundary composition

2. Mechanical Multi-Layer Capacitor
 - a. Evaluation of packaging and construction technologies
 - b. Evaluation of capacitor characteristics at elevated voltages and temperatures

3. Monolithic Multi-Layer Capacitor
 - a. Evaluation of alternative contact metals and materials (Mo, diamond, composite materials, etc.)
 - b. Continued exploration of different deposition technologies (ECR, hot filament CVD, etc.)
 - c. Spectral and optical characterization of previous deposition results

REFERENCES

- [1] J.L. Davidson, *Synthetic Diamond: Emerging CVD Science and Technology/* edited by K. Spear and J. Dismukes, Wiley, New York, 1994
- [2] P.W. May, *Endeavour Magazine* **19**(3):101 (1995)
- [3] B.V. Deryagin, D.V. Fedosayev, *Surface and Coating Technology* **38**(1-2):132 (1989)
- [4] R.E. Thomas, J.A. Rosa, *The Analysis and Design of Linear Circuits: 4th Edition*, Wiley, 2003
- [5] D. Halliday, R. Resnick, J. Walker, *Fundamentals of Physics: Fourth Edition*, Wiley, 1993
- [6] W.H. Hayt, J.E. Kemmerly, S.M. Durbin, *Engineering Circuit Analysis: Sixth Edition*, McGraw Hill, 2002
- [7] G.L. Johnson, *Solid State Tesla Coil*, Dr. Gary L. Johnson, Manhattan, KS; 2001
- [8] K.C. Kao, *Dielectric Phenomena in Solids: With Emphasis on Physical Concepts of Electronic Processes*, Elsevier Academic Press, 2004
- [9] C.A. Balanis, *Advanced Engineering Electromagnetics*, Wiley, 1989
- [10] R. Ramesham, P.E. Pehrsson, T.I. Smith, M.F. Rose, *Journal of Materials Science: Materials in Electronics* **8**:69 (1997)
- [11] H. Ye, C.Q. Sun, H. Huang, P. Hing, *Thin Solid Films* **381**:52 (2001)
- [12] W. Ebert, M. Adaschik, P. Gluche, A. Flöter, E. Kohn, *Diamond and Related Materials* **8**:1875 (1999)
- [13] H. Ye, P. Hing, *International Journal of Thermophysics* **22**, no. 4:1285 (2001)
- [14] S.L. Heidger, N.J. Baraty, J.A. Weimer, "CVD Diamond for High Power and High Temperature Electronics," *Diamond Materials VII*, Electrochemical Society Proceedings Volume 2001-25 (2002)
- [15] M. Yokoba, Y. Koide, A. Otsuki, F. Ako, T. Oku, M. Murakami, *Journal of Applied Physics* **81** (10), 6815 (1997)

- [16] V.I. Polyakov, A.I. Rukovishnikov, B.M. Garin, L.A. Avdeeva, R. Heidinger, V.V. Parshin, V.G. Ralchenko, *Diamond and Related Materials* (2004)
- [17] A. Ibarra, M. Gonzalez, R. Vila, J. Molla, *Diamond and Related Materials* **6**:856 (1997)
- [18] J. Molla, A. Ibarra, C. Maffiotte, *Diamond and Related Materials* **9**:1071 (2000)
- [19] K. Hayashi, H. Wantanabe, S. Yamanaka, *Diamond and Related Materials* **6**:303 (1997)
- [20] A. Denisenko, A. Aleksov, A. Pribil, P. Gluche, W. Ebert, E. Kohn, *Diamond and Related Materials* **9**:1138 (2000)
- [21] J.V. Manca, M. Nesladek, M. Neelen, C. Quaeys, L. De Schepper, W. De Ceuninck, *Microelectronics Reliability* **39**:269 (1999)
- [22] Y. Muto, T. Sugino, J. Shirafuji, *Applied Physics Letters* **59**(7):843 (1991)
- [23] E. Wilks, J. Wilks, *Properties and Applications of Diamond*, Butterworth-Heinemann, Cambridge University Press, 1991
- [24] O. Sanchez-Garrido, C. Gomez-Aleixandre, J. Sanchez Olias, J.M. Albella, M. Hernandez-Velez, F. Fernandez Gutierrez, *Journal of Materials Science: Materials in Electronics* **7**:297 (1996)
- [25] P. Gonon, A. Deneuve, F. Fontaine, E. Gheeraert, *Journal of Applied Physics* **78**(11):6633 (1995)
- [26] N.F. Mott, E.A. Davis, *Electronic Processes in Non-Crystalline Materials*, Oxford University Press, London, 1971.
- [27] B.L. Mackey, J.N. Russell Jr., J.E. Crowell, J.E. Butler, *Physical Review B* **52**(24), R17009 (1995)
- [28] V. Ralchenko, L. Nistor, E. Pleur, A. Khomich, I. Vlasov, R. Khmel'nitskii, *Diamond and Related Materials* **12**:1964 (2003)
- [29] X. Cheng, C. Chen, H. Zhou, *Solid-State Electronics* **48**:285 (2004)
- [30] J. Davidson, W. Kang, K. Holmes, A. Wisitsora-At, P. Taylor, R. Venkatsubramanian, F. Wells, *Diamond and Related Materials* **10**:1736 (2001)
- [31] P. Gonon, S. Praver, Y. Boiko, D.N. Jamieson, *Diamond and Related Materials* **6**:860 (1997)

- [32] M. Alam, A. Lucero, *Materials Science and Engineering B* **27**:81 (1994)
- [33] S. Nath, J.I.B. Wilson, *Diamond and Related Materials* **5**:65 (1996)
- [34] D.V. Feather, *A Study of the Dielectric Properties of Polycrystalline Diamond Film: The Diamond Capacitor*, Master of Science Thesis, Vanderbilt University, 1991
- [35] R.A. DeCarlo, P. Lin, *Linear Circuit Analysis: Time Domain, Phasor, and LaPlace Transform Approaches*, Prentice-Hall, 1995
- [36] J.W. Nilsson, S.A. Riedel, *Electric Circuits: Fifth Edition*, Addison-Wesley, 1996
- [37] D.L. Dreifus, A. Collins, T. Humphreys, K. Das, P. Pehrsson, *Diamond for Electronic Applications*, Materials Research Society, 1996
- [38] S. Whitehead, *Dielectric Breakdown of Solids*, Oxford University Press, 1951
- [39] H. Fröhlich, *Theory of Dielectrics: Dielectric Constant and Dielectric Loss*, Oxford University Press, 1958
- [40] G.F. Miner, *Lines and Electromagnetic Fields for Engineers*, Oxford University Press, 1996
- [41] N. Mott, *Conduction in Non-Crystalline Materials: Second Edition*, Oxford University Press, 1993
- [42] J.J. O'Dwyer, *The Theory of electrical Conduction and Breakdown in Solid Dielectrics*, Oxford University Press, 1973
- [43] M.D. Whitfield, J.A. Savage, R.B. Jackman, *Diamond and Related Materials* **9**:262 (2000)
- [44] D.M. Trucchi, E. Cappelli, G. Conte, G. Mattei, C. Gramaccioni, P. Ascarelli, *Diamond and Related Materials* **14**:575 (2005)
- [45] P. Ascarelli and S. Fontana, *Applied Surface Science* **64**:307 (1993)
- [46] P. Ascarelli, E. Cappelli, G. Mattei, F. Pinzari, V. Fares, C. Veroli and S. Martelli, *Diamond and Related Materials* **5**:308 (1996)
- [47] C. Wild, P. Koidl, W. Muller-Sebert, H. Walcher, R. Kohl, N. Herres, R. Locher, R. Samlenski and R. Brenn, *Diamond and Related Materials* **2**:158 (1993)
- [48] V. J. Trava-Airoldi, E. J. Corat, L. V. Santos, A. V. Diniz, J. R. Moro, N. F. Leite, *Diamond and Related Materials* **11**:532 (2002)

- [49] J. S. Foord, C. H. Lau, M. Hiramatsu, R. B. Jackman, C. E. Nebel, P. Bergonzo, *Diamond and Related Materials* **11**:856 (2002)
- [50] F. Maier, M. Riedel, B. Mantel, J. Ristein, L. Ley, *Physical Review Letters* **85**:3472 (2000)
- [51] H. Gerischer, in *Physical Chemistry*, Academic Press, 1970
- [52] K. O. Schweitz, R. B. Schou-Jensen, S. S. Eskildsen, *Diamond and Related Materials* **5**:206 (1996)
- [53] K. K. Hirakuri, M. Yoshii, G. Friedbacher and M. Grasserbauer, *Diamond and Related Materials* **6**:1031 (1997)
- [54] S. G. Wang, Qing Zhang, S. F. Yoon, J. Ahn, Q. Wang, D. J. Yang, Q. F. Huang, Rusli, W. Z. Tang and F. X. Lu, *Diamond and Related Materials* **11**:1683 (2002)
- [55] G. Cicala, P. Bruno, F. Bénédic, F. Silva, K. Hassouni and G.S. Senesi, *Diamond and Related Materials* **14**:421 (2005)
- [56] B. S. Park and Y. -J. Baik, *Diamond and Related Materials* **6**:1716 (1997)
- [57] D.M. Trucchi, E. Cappelli, G. Conte, G. Mattei, C. Gramaccioni and P. Ascarelli, *Diamond and Related Materials* **14**:575 (2005)
- [58] G. Conte, M.C. Rossi, F. Spaziani and R. Arcangeli, *Diamond and Related Materials* **14**:570 (2005)
- [59] K.C. Holmes, Piezoresistive Micro-Electro-Mechanical Applications in Diamond Films, PhD Dissertation, Vanderbilt University, 2002.
- [60] S.S. Perry, J.W. Ager, G.A. Somorjai, R.J. McClelland and M.D. Drory, *Journal of Applied Physics* **74**(12):7542 (1993)
- [61] M.L. Terranova, M. Rossi and G. Vitali, *Journal of Applied Physics* **80**(6):3552 (1996)
- [62] M. Kawarada, K. Kurihara and K. Sasaki, *Diamond and Related Materials* **2**:1083 (1993)
- [63] N. Eimori, Y. Mori, J. Moon, A. Hatta, J. S. Ma, T. Ito and A. Hiraki, *Diamond and Related Materials* **2**:537 (1993)
- [64] A.K. Sikder, T. Sharda, D.S. Misra, D. Chandrasekaram, P. Selvam, *Diamond and Related Materials* **7**:1010 (1998)

[65] S.A. Catledge, Y.K. Vohrau, *Diamond and Related Materials* **9**:1327 (2000)