ON THE IMPACT OF DEVICE ORIENTATION ON THE MULTIPLE CELL UPSET RADIATION RESPONSE IN NANOSCALE INTEGRATED CIRCUITS

By

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For Mom and Daddy — you made this possible.

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> To days of inspiration, playing hookey, making something out of nothing, the need to express, to communicate.
>
> —*Jonathan Larson, Rent*

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CHAPTER I

INTRODUCTION

> This invention relates to miniature electronic circuits, and more particularly to unique integrated electronic circuits fabricated from semiconductor material.
>
> —*Jack Kilby, U. S. Patent 3,138,743*

The Integrated Circuit

Jack Kilby of Texas Instruments was granted the first patent of the integrated circuit (IC) in 1964 [1,2]. In 1967 a patent for the complementary metal oxide semiconductor (CMOS) system was issued to Frank Wanlass of Fairchild Semiconductor Research and Development [3]. Since then, improvements in performance and packing density for each new generation of IC have been primarily achieved by shrinking transistor sizes. State-of-the-art microprocessors boast nearly a billion transistors. Such transistor densities make the metal-oxide-semiconductor field effect transistor (MOSFET) easily the most manufactured item in history.

The International Technology Roadmap for Semiconductors (ITRS) reports 65 nm as the 2007 feature size – as defined by $\frac{1}{2}$ the pitch of metal [4]. Scaling to such small feature sizes has not been easy or cheap. After development and design cost, IC Insights estimates that the required sales for positive return on investment (ROI) for a 65 nm process to be $8.3 billion. Only Intel, Samsung,

Texas Instruments, STMicroelectronics, and Toshiba had 2006 sales greater than that number [5].

Radiation Effects

The interactions of charged particles with semiconductor devices may lead to logic errors in digital ICs. Charged particles are the source of single-event effects (SEEs) in integrated circuits. In 1962 Wallmark and Marcus proposed an absolute minimum size and maximum packing density for semiconductor devices [6]. Cosmic ray interaction at ground level was identified as one limitation to the minimum device size. Other reasons included heat dissipation and dopant fluctuations. It is interesting to note that the authors concluded 10 μm to be the limiting feature size.

Binder *et al.* first reported in 1975 on single event phenomenon for space systems [7]. In 1979 May and Wood identified SEEs in commercial parts due to alpha particles from radioactive decay in packaging materials [8]. In that same year Ziegler and Lanford examined the impact of terrestrial radiation from galactic cosmic rays on ground based systems [9].

Development of the modern IC to increase functionality and performance has forced higher device densities and smaller devices. Reduction of power consumption has also become a major concern as device densities increase and has forced operating voltages to scale down as well. The trends in density and operating voltage have increased the susceptibility of ICs to radiation induced soft errors in state-of-the-art electronics [10,11]. Soft error rate (SER) refers to the rate at which data errors occur. SER not only depends on the device susceptibility to ionizing

radiation, but also the environment in which the device is expected to operate. In general, device scaling has created competing trends for some single-event effects. For bit errors, the single-bit SER has generally decreased in highly-scaled technologies, but the drastic increase in bit density has kept system level SER generally constant across generation. Fig. 1 shows the neutron induced SER/bit for Intel's 180 nm–45 nm technology nodes [10]. Each successive generation of CMOS technology shows a decrease in single bit SER.

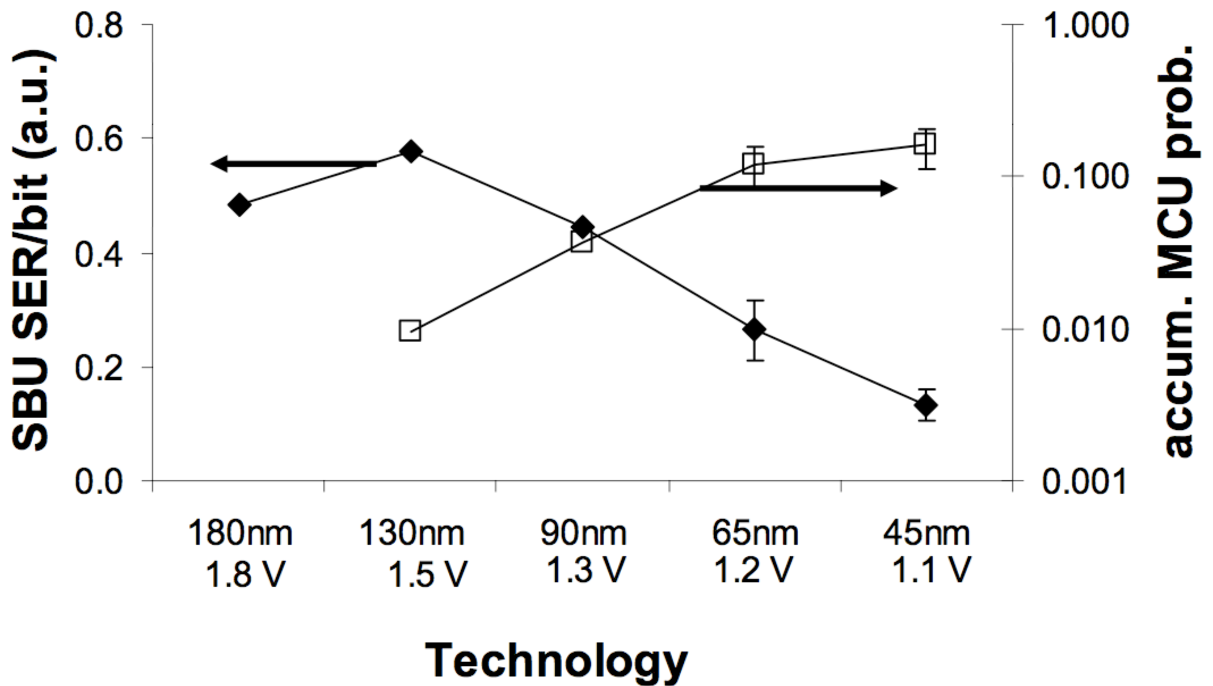


Figure 1: The neutron–induced bit soft error rate for Intel's 180 nm–45 nm technology nodes decreases with each new generation. The probability of MCU increases with each new generation because higher device densities places sensitive nodes closer together.

The Multiple Cell Upset

When a charged particle travels through material, it loses energy through their interactions with matter. In semiconductor materials, charge is generated from this energy loss along the path of the incident particle. When sufficient charge is collected on a circuit node to change its state, this leads to a corruption of the data called a single event upset (SEU). A single-cell upset (SCU) occurs when these interactions change the logic or memory state of one bit. Relative to the size of the charge track produced by the incident particles, the geometries of state-of-the-art integrated circuits are small. Interaction with multiple bits is possible for some particle trajectories and paths. Multiple-cell upset[1] (MCU) results when SCU occurs in multiple cells from a single ion. MCUs are important because may be more difficult to correct using error correction [20].

With smaller semiconductor devices, the packing density increases. Higher packing densities increase the probability that an inoizing particle will induce an MCU event. Fig. 1 shows the probability of MCU for Intel processes. The probability increases from approximately 1% in 130 nm feature sizes to 15% in their state–of–the–art 45 nm process.

Fig. 2 is an example of an MCU event from a 63 MeV proton represented in a technology computer aided design (TCAD) structure. Only this silicon material is shown as the overlayers have been omitted. The incident proton induces a

[1]The SCU and MCU effects are termed single-bit upset (SBU) and multiple-bit upset (MBU) respectively in [12–18]. This semantic change reflects the JEDEC (Joint Electron Devices Engineering Council) standard where the bit upset nomenclature is reserved for logical bit upset in the context of data words in a memory architecture [19].

nuclear reaction near silicon surface of the memory array. The shaded boxes represent sensitive regions of the silicon, each corresponding to one bit in a memory array. The incident proton enters at a grazing angle and interacts with the silicon to cause a nuclear event. The trajectories of the incident proton and secondary particles are represented by the colored lines. A 14 MeV oxygen ion is emitted from the reaction that traverses six, darker shaded, sensitive volumes. The other reaction products include a proton, gamma rays, and alpha particles. This is an example of a six-bit upset if the deposited energy is sufficient to upset the cells. The oxygen secondary ion from the nuclear reaction is responsible for the MCU event.

The probability of a given event producing an MCU increases as the size of semiconductor devices scale smaller because the distance between cells is reduced [12, 21, 22]. Fig. 1 shows the increasing probability of MCU with successively new generations of Intel's CMOS technologies because of higher device densities. MCUs from broad-beam proton and neutron irradiations have been shown to depend on the orientation of the device relative to the incident beam [12, 14, 15, 23]. Nucleons incident at large angles of incidence tend to traverse more cells and MCU increases at these orientations.

Testing of electronic devices must account for these dependences to predict the radiation response accurately. Testing at a single device orientation may not observe the worst case MCU response. Previously it was shown that MCU cross section increases an order of magnitude for 63 MeV protons at grazing angles compared to normal incidence [12]. The cross section increases because the ionizing secondary products produced by these protons have trajectories similar to

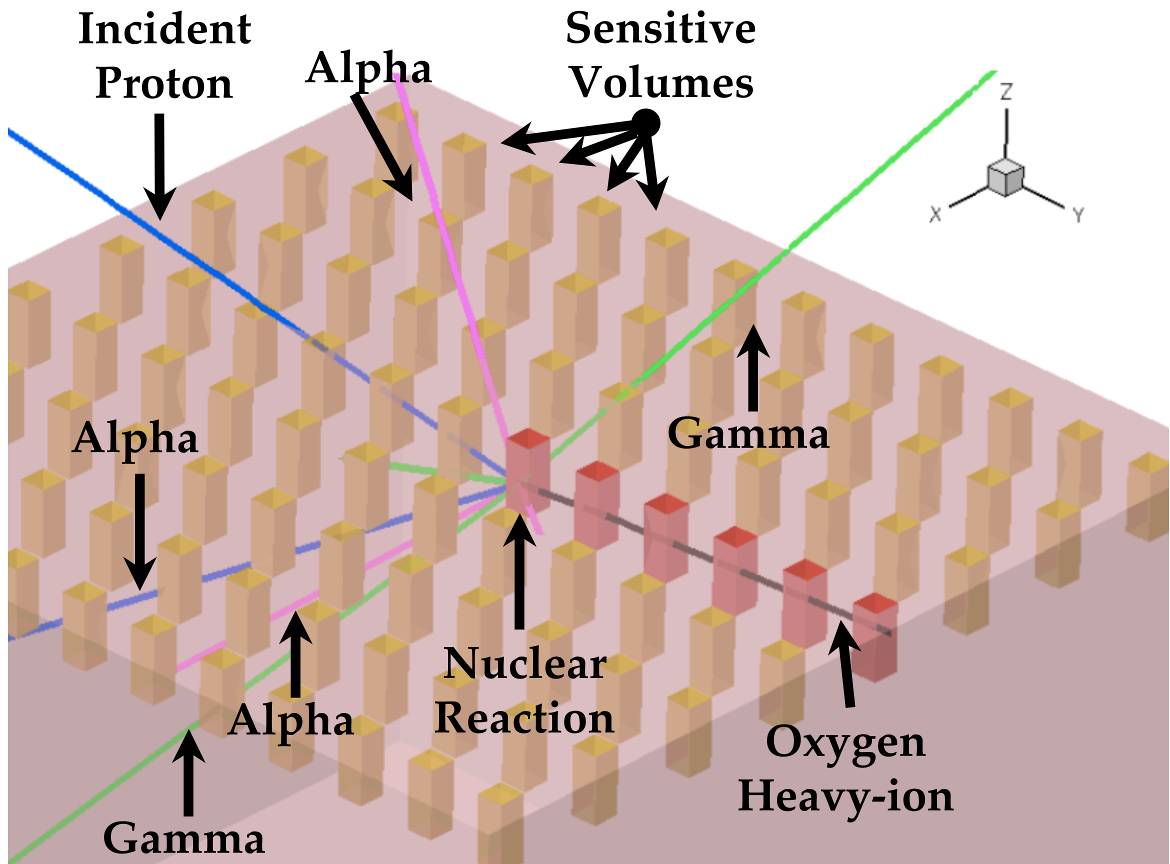


Figure 2: A TCAD representation of an MRED generated nuclear event for a 63 MeV proton incident at a grazing angle in silicon with the sensitive volumes shown by the shaded boxes. The overlayers have been omitted. The secondary products from the reaction are a 14 MeV oxygen ion, a proton, gamma rays, and alpha particles. The oxygen heavy ion transverses six sensitive volumes of SRAM cells.

the incident proton. For these protons, the maximum likelihood of interacting with multiple cells is realized at the largest grazing angles. That is, the radiation response depends on the orientation of the device relative to the trajectories of the secondary heavy ions.

Summary of this Work

In this work, device orientation effects on MCU are examined for neutrons and heavy ions. Accelerated testing is used to evaluate static random access memories (SRAMs) for MCU by changing the orientation of the device in the beam path. Experimental results from accelerated tests are used to characterize two technologies for MCU and they are used to calibrate an MCU model. The size, shape, and probability of MCU are shown to depend on orientation for both particle types. The worst case MCU events occur at large angles of incidence. Additionally, heavy ions also exhibit a strong dependence on the ion's trajectory with respect to the SRAM layout for the size and shape of MCU events.

This work analyzes the MCU response for neutrons and heavy ions using the Monte-Carlo Radiative Energy Deposition (MRED) code [24, 25]. The transport of radiation through matter is simulated using MRED. MRED is a Monte–Carlo transport code based on the Geant4 libraries [26]. These libraries model the transport of radiation through matter. The Geant4 libraries contain models for ionization and nuclear processes. MRED has been used to examine: the role of heavy ion induced nuclear reactions on SER [27,28], the role of metallization near semiconductor devices on heavy ion induced nuclear reactions [29], on–orbit SER predictions [30, 31], and the effects of nucleon induced radiation events [13, 32].

The experimental results are used to calibrate a model for the devices in this work. The radiation transport model is used to analyze MCU for real environments and compared to the accelerated response.

Chapter II discusses the background and trends of MCU in state-of-the-art microelectronics. Chapter III discusses MCU analysis of radiation events. In Chapter IV neutron–induced MCU effects are reported and the heavy ion effects are reported in Chapter V. Chapter VI details the Monte-Carlo modeling and discusses the MCU response for real environments. Finally, a discussion of the implications of MCU is found in Chapter VII.

CHAPTER II

BACKGROUND

This chapter gives a broad overview of the source and mechanisms of SEEs and MCU. The sources, types, and mechanisms of MCU are discussed. The upset mechanisms important to this work are reviewed. The origins of MCU are discussed. The development and trends in MCU are discussed for nucleon and heavy ion induced effects.

Single Event Effects (SEEs)

This section outlines the basics of SEEs important for MCU. The sources, types, and mechanisms are discussed. Finally, SRAM upset is discussed because it is the device type considered in this work.

Sources of SEEs

SEEs are the result of ionizing radiation interacting with semiconductor circuit elements. The severity and frequency of these interactions on circuit operation depends strongly on the environment in which the system will operate. Particles found in the space environment are dominated by protons and heavy ions. Galactic cosmic rays (GCR), the solar activity of the sun, and particles trapped in the Earth's magnetic fields are the sources of those particles. The distributions of energies and ion species depend on the specific orbit. Detailed discussions of the space environment can be found in [33, 34].

Protons and heavy ions are of little concern for terrestrial systems because these particles are shielded by the Earth's atmosphere. Cosmic ray interactions in the Earth's atmosphere through the strong force create cascades of secondary particles that move towards ground level. These secondary products penetrate to ground level leading to a terrestrial environment of non-ionizing neutrons that indirectly ionize through nuclear interactions. Radioactive decay by materials in and around devices are another source of SEEs for ground based systems. A discussion of the terrestrial environment can be found in [35].

Types of SEEs

SEEs are broadly grouped into two categories: destructive and non-destructive. Destructive SEEs result in permanent damage that impinges on the proper operation of a circuit element. While these effects leave circuit elements inoperable, their impact on circuit operation varies and depends on the role of the specific element in the circuit operation. Non-destrcutive SEEs occur when radiation events disrupt circuit operation. These effects do not cause permanent damage, but they can lead to interruption of normal circuit operation and, in some cases, data corruption. These errors can be transient pulses that appear as current pulses on circuit nodes that may propagate through the circuit or they can be static errors that change the state of a static circuit such as a latch [36]. This work focuses on non-destructive static SEU in SRAMs.

SEE Mechanisms

Radiation interactions in matter fall into two categories: electromagnetic interactions and nuclear interactions. Electromagnetic processes are conventionally considered only for heavy ions while nuclear processes are considered for nucleons though heavy ion nuclear interaction is possible (note, proton ionization is consider for sensitive devices such as imagers). What follows is an overview of the major interactions of concern for electronics. A more detailed discussion of these processes can be found in [37,38].

Heavy ions

From the perspective of radiation effects on ICs, heavy ions interact primarily through electromagnetic processes. In some cases, heavy ions have been shown to interact through nuclear collisions and contribute to SEEs as well [28,29,39]. When a charged particle passes through matter, its energy is transferred to the material. This process continues until the ion loses all its kinetic energy and comes to rest. Linear energy transfer (LET) is the average amount of energy lost per unit length and is usually normalized to the density of the material. The LET of a particle is dependent on the species of ion, energy of the ion, and target material. The average LET of an ion in a material is available from codes like SRIM [40].

Energy loss in a semiconductor material creates electron-hole pairs (EHPs). In silicon, 3.6 eV of energy loss produces, on average, one EHP [41]. For example, an ion with an LET of 9.7 MeV–cm^2/mg creates a charge density of 10 fC/μm. The EHPs that are created are subject to normal semiconductor transport mechanisms. From a circuit perspective, charge collection on a node appears as a current pulse

on the node. The shape of the resulting current pulse depends on the location and amount of charge generated relative to the contact where it is collected. The injection of charge leads to SEEs in integrated circuits.

Nucleons

Nucleon–induced effects differ from heavy ions because their electromagnetic interactions produce negligible or no EHPs. Rather, these particles interact mainly through nuclear interactions. Protons and neutrons can overcome the Coulomb barrier and interact with an atom's nucleus through the strong force when they are transported through semiconductor materials. Breakup of the nucleus produces secondary heavy ions and other products that in turn generate charge through electromagnetic forces. The charge produced by secondary products is the source of nucleon–induced SEEs in integrated circuits.

SEE – SRAM upset

In this work, upsets in SRAM devices are considered. Fig. 3a shows a circuit schematic diagram of a conventional four transistor (4T) SRAM circuit. The SRAM circuit is a cross coupled pair of inverters with an active feedback network. The logic diagram is shown in Fig. 3b where the two connected inverters store the data. When an ionizing particle strikes the SRAM cell, the collected charge appears as a current pulse on the circuit nodes. Whether or not the cell will upset depends on which node is struck. Typically, strikes to the diffusions of the OFF state n–MOSFET or p–MOSFET transistors will lead to upsets. A strike to the drain of the n–MOSFET is termed an "n-hit" and a strike to the p–MOSFET

is termed a "p–hit". The current pulse can discharge the node and change the potential. The feedback path is shown by the arrows in Figs. 3a and 3b.

The ON state device, the p-MOSFET in the case of an n–hit or the n–MOSFET in the case of a p–hit, will attempt to restore the node voltage. At the same time the resulting voltage transient on the struck node will propagate to the other cross coupled inverter. If sufficient charge is collected and the resulting voltage transient propagates through the feedback, then the circuit will upset. The current and voltage at the struck node of the OFF n–MOSFET in Fig. 3a are illustrated in Fig. 3c. The spike in the current is the result of the initial charged particle strike to the drain of the device. The initial drop in the voltage, which appears as a single event transient (SET) at the struck node, begins to recover as the ON p–MOSFET supplies current to restore the node. The feedback of the initial strike through the other inverter eventually drives the voltage down and results in an SEU. The total collected charge, Q_{Coll}, on the struck node is determined by integrating the current pulse. Strikes such as the one in Fig. 3c will not always result in an SEU. The size of the current peak is related to the location of the charged particle strike. The current pulse must overcome the restoring current from the ON device. The minimum charge required to induce upset is called the critical charge, Q_{Crit}, of the circuit.

The Multiple Cell Upset

In this section MCU and MBU effects are described. These effects are grouped into heavy ion and nucleon effects because the physical mechanisms for each are different.

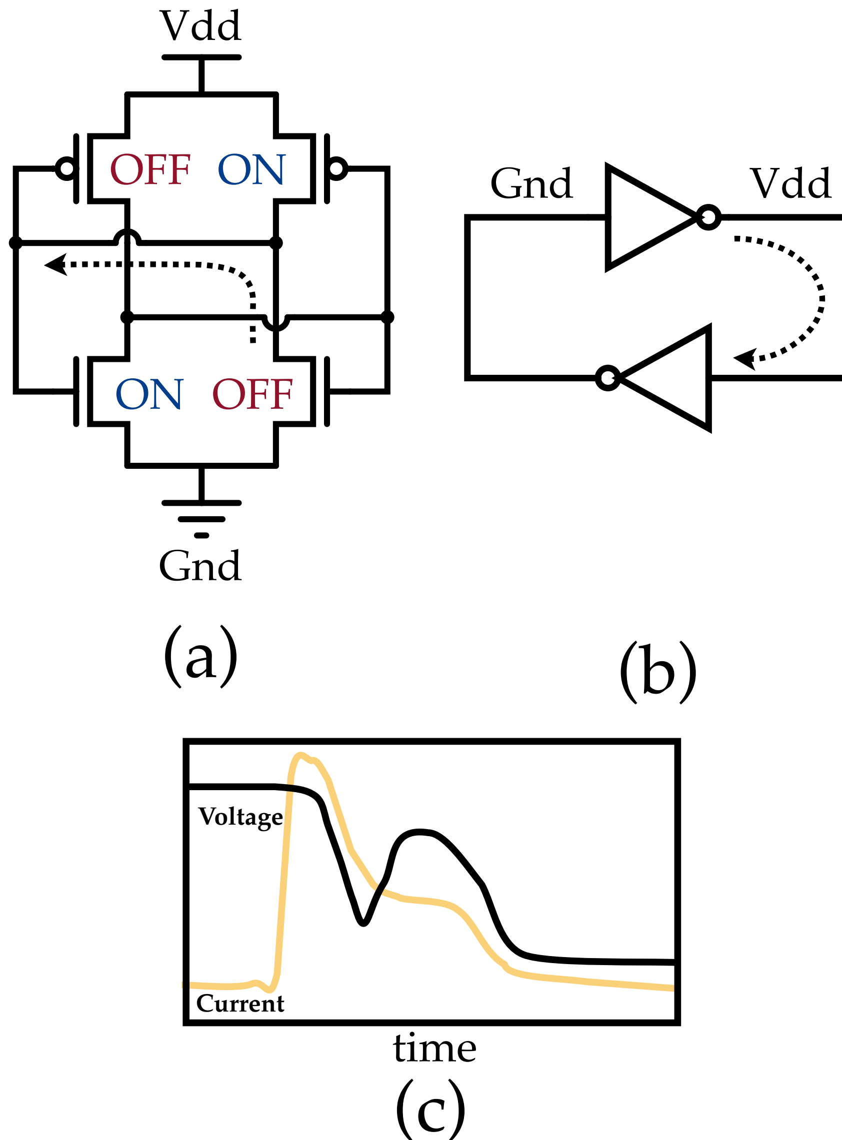


Figure 3: (a) A circuit schematic diagram of an SRAM formed by two cross–coupled inverters. The ON and OFF state devices are labeled for one possible state of the SRAM. The feedback path of a strike to the drain of the OFF n–MOSFET device is shown by the dotted line. (b) The logic diagram of the circuit shows the feedback path of a transient strike indicated by the dotted line. (c) The current and voltage transients at the node of the OFF n–MOSFET are illustrated. The initial current pulse drops the voltage at the node. The ON p–MOSFET attempts to restore the state of the node. The feedback of the initial strike and the additional collected charge eventually result in an SEU.

Many of the first uses of accelerated heavy ion broad beam SEU testing also reported MCU and MBU events. Criswell *et al.* reported the first observation of MCU in 1984 while using heavy ions for SEE testing [42]. The device under test was a 256–bit bipolar SRAM. The experimental data showed as many as 16 cells upsetting for 600 MeV/u Fe heavy ions. Bisgrove *et al.* calculated the first MCU cross sections for heavy ions in Intel 64 kbit 1.5 μm DRAMs from heavy ion and proton testing [43]. Blake *et al.* reported on-orbit observations of 1.25 μm SRAMs using bitmaps to show the physical locations of MBUs which accounted for 19% of all events [44]. SEE testing since that paper has often noted MCU and MBU. MCU/MBU evaluation are often part of the SEE testing for new technologies.

MCU and MBU have been noted in on–orbit data by several authors [44–48]. Error detection and correction (EDAC) is commonly used to correct MBU events for memory arrays [48–52]. MBU poses reliability concerns for EDAC circuitry because data corruption of multiple bits is more difficult to protect against. Bit–interleaving, where bits in the same data word are separated by distance in the memory array, is one way to increase the effectiveness of EDAC. Lack of aggressive bit–interleaving has been identified for unexpectedly high data corruption of on–orbit memories because of MCU events [48].

Alpha emission and thermal neutrons are the primary concerns for MCU and MBU in ground based systems [53–60]. Cache and memory are primarily a concern for large servers [20]. In those systems, soft errors induced by alpha particles and neutrons can induce MCU. EDAC are used extensively for large server memory arrays with bit interleaving schemes [20, 58].

Heavy Ion Induced MCU

The probability of double bit upset had been shown to depend on the radial charge density of the charge generated by ion strikes [61]. It was shown that heavy ions with larger radial tracks could more easily make direct hits to multiple memory cells. This was shown by characterizing MBU with respect to device spacing.

The right parallelepiped (RPP) sensitive volume was proposed by Pickel and Blandford [62]. This upset model for SEU assumed a fixed RPP volume in which generated charge would lead to upset. The model assumes a fixed Q_{Crit} and uses an average of all possible cord lengths for the RPP volume to determine upset. This model was updated by Petersen *et al.* [63]. An extension of this model to double bit upset was developed by Edmonds [64] then extended by Smith and Shoga [65]. Following from the RPP model, the double bit model assumes a common path length through multiple sensitive volumes due to a single heavy ion track corrected for angle. This model has its limits, however. Because of shrinking dimensions, the simple geometric approximation of the RPP becomes inadequate. Other charge collection mechanisms such as charge sharing and bipolar amplification can play roles in SEU for highly scaled technologies [66, 67].

Increased MCU has been attributed to diffused charge collection in SRAMs [68]. Device simulation was used to show the role of diffusion charge in MCU as early as 1.25 μm technologies [69–71]. It was shown that diffusive charge collection for heavy ions incident on pn-junctions was greater than for incident heavy ions that do not strike junctions. The general observation was that ions incident on junctions produced more charge collection on that node and reduced the amount of

charge that could diffuse to nearby nodes, thus reducing the probability of MCU. Bipolar charge collection was identified as another MCU mechanism [72].

Heavy ion induced MCUs can be separated into two types [73]. Type I errors are due to a heavy ion passing through multiple sensitive volumes and inducing multiple upsets. Type II MCU is due to diffusive charge and other charge collection mechanisms. The differences between the two can be seen by comparing MCUs from normally incident ions with MCUs from ions incident at oblique angles. Other causes of MBU have been attributed to heavy ion interactions with control circuitry that induce word line upset [74].

Three–dimensional mixed mode device simulation by Dodd *et al.* mapped out regions of MCU sensitivity between two nodes for Type II events [75]. Diffusion from heavy ion ionization was identified as the upset mechanism. Relative to bulk processes, epitaxial structures showed a reduced diffusion component of charge collection making them more desirable for mitigating MCU. Laser testing has also been used to map MCU sensitivities [76].

Nucleon Induced MCU

O'Gorman *et al.* measured SEU at ground level from cosmic rays [53, 77]. Dynamic Random Access Memory (DRAM) SER was tested at various altitudes above and below sea level and showed an order of magnitude increase in SER at an altitude of 3.1 km compared to sea level. That study found that not only SEU but also MBU at ground level is possible. Higher altitudes exhibited increased SER. While neutron environments have shown a decrease in the SER for single–cell upsets, MCU has increased in highly scaled devices [10, 11, 22].

Seifert *et al.* showed increased MCUs due to decreased node spacing [10] as did Baumann [11]. Device scaling reduces the charge collection sensitive volume, making upset less likely. Scaling also reduces the charge required to upset, making more likely. These competing effects have held the SEU rate relatively constant for newer and smaller CMOS processes. The MCU response is dominated by device scaling, however, and the probability of MCU has increased for smaller dimensions.

The CRRES MEP satellite noted on–orbit MCU at a high rate in [45]. The frequency of these events inside proton belts dominated the SEE and MBU responses. Reed *et al.* also observed increased proton–induced MCU at grazing angles in [78]. CUPID calculations agreed with the angular dependence observed for proton irradiation. Buchner *et al.* showed MCU events to double at large grazing angles for 63 MeV and 198 MeV protons [79]. Testing confirmed that the SEE response due to proton irradiation exhibits an angular dependence in more highly scaled SRAMs [80]. CUPID simulations in [79] and GEANT4 in [80] suggested that angular dependencies would be more pronounced for lower proton energies because of the direction of spallation products with respect to the incident proton direction. It was shown by both studies that MCU should be expected to increase with device downscaling because of reduced device dimensions.

MRED simulations of 63 MeV and 200 MeV protons on SRAMs exhibit higher MCU probabilities at grazing angles [12,13]. Fig. 4 shows the simulated probability of MCU for the IBM 8RF 130 nm bulk CMOS process from 63 MeV protons. Four angles of irradiation are shown from normal incidence to oblique grazing

angles. The energy deposition profiles are shown for generated charge in the sensitive volume of the SRAM cells. Evaluating the curve at the Q_{Crit} of the circuit yields the MCU probability. Circuit simulation suggests Q_{Crit} to be approximately 10 fC. Evaluating at this value, the highest probabilities at the largest grazing angles are approximately 5%.

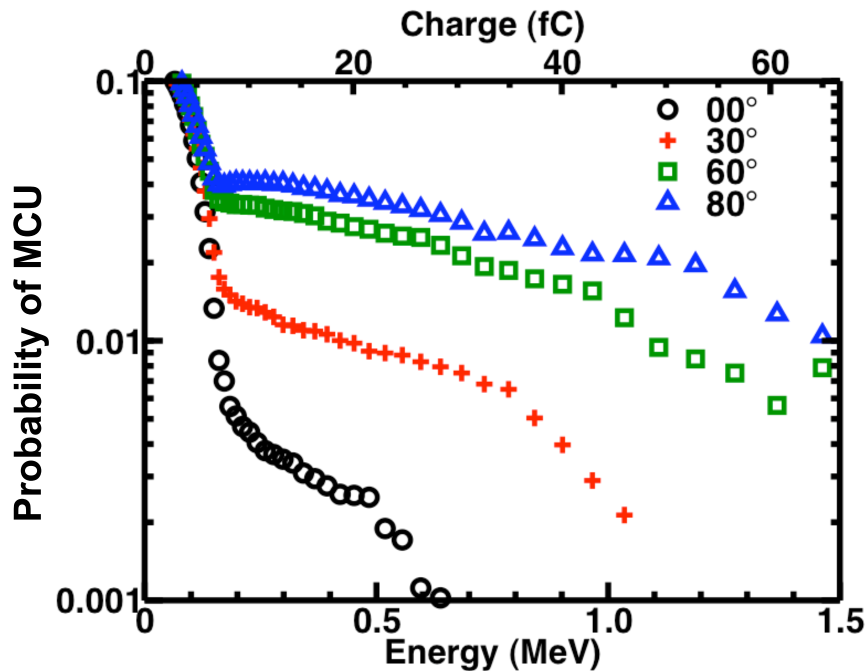


Figure 4: The probability of MCU from 63 MeV protons increases with the angle of proton incidence.

Summary

The space radiation environment important to SEEs in ICs is composed of heavy ions and protons. GCR and solar activity if the sun are the sources of those particles. GCR interaction in the atmosphere produces showers of neutrons

that penetrate to ground level. The terrestrial radiation environment is composed primarily of those neutrons and alphas.

In this work, SEEs on SRAMs are examined. The upset mechanism for SRAM cells is due to charge collection on the circuit nodes of the SRAM. The inherent feedback network of SRAM cells attempts to balance any perturbation. The minimum collected charge to upset a cell, Q_{Crit}, is an important characteristic in modeling SEEs in SRAM cells.

As the characteristic feature sizes are reduced in state–of–the–art semiconductor processes, MCU continues to increase in probability for SRAM arrays [10, 11]. The close proximity of cells is the driving force behind this increase because of the increased coupling of individual cells' charge collection during ionizing radiation events.

MCU has been observed in both the space and terrestrial radiation environments [45, 77]. Heavy ions and nucleons have different upset mechanisms: direct heavy ion ionization and ionization by secondary products from nuclear reactions induced by nucleons. Evidence for orientation dependences due to these particles in highly scaled technologies exists. Particles incident at large angles of incidence with respect to the surface of semiconductor devices exhibit higher probabilities of MCU.

In the chapters that follow, evidence of the dependence of MCU on device orientation with respect to incident heavy ions and neutrons is presented. Accelerated testing is used to examine the orientation effects and modeling of these effects is used to examine real environments.

CHAPTER III

MULTIPLE CELL UPSET ANALYSIS

In this chapter the methods used in this work for the analysis of SEU and MCU events are presented. The methods presented in this chapter will be used to analyze the MCU radiation response. The methods used to analyze the SEU response are presented first. The SEU response is separated into the analysis of SCU and MCU events. MCU analysis in this work characterizes MCU events by their multiplicity and the area of affected bits.

Single Event Upset

Ground based accelerated testing using particle accelerators is used extensively to characterize the radiation response of ICs [81]. The SEU response is used by convention to calculate and predict the SER performance of the device. Error rate predictions in a specific environment are made based on accelerated SEU testing. The primary purpose of SEU testing is to evaluate the SEU cross section versus energy deposition for use in calculating SER performance. The SEU cross section, σ_{SEU}, is the uncorrelated bit upset cross section for all bit upsets from SCU and MCU events. It is defined as

$$\sigma_{\text{SEU}} = \sum_{i=1}^{\infty} \frac{i \times \text{Event}_{i-\text{bit}}}{\Phi} = \frac{1 \times \text{Event}_{1-\text{bit}} + 2 \times \text{Event}_{2-\text{bit}} + 3 \times \text{Event}_{3-\text{bit}} + \ldots}{\Phi} \tag{1}$$

where $\text{Event}_{i-\text{bit}}$ is the number of MCU events with *i*–bits upset, and Φ is the fluence of incident particles.

For heavy ions, the σ_{SEU} is calculated for each ion at a single accelerated energy. Since it is impossible to test every ion at every energy for a space environment, ions are selected in SEU testing such that they cover a range of heavy ion LETs. Note, in this work no cross sections are reported as effective cross sections (*i.e.*, LET is not converted to effective LET and fluence is not converted to effective fluence). All fluences in this are reported as measured in the plane perpendicular to the beam line. In recent highly-scaled technologies, the traditional RPP model assumptions are no longer valid [30]. Note also, all SRAM cross sections in this work are normalized to the total number of bits in the device under test unless stated otherwise.

Multiple Cell Upset

The SEUs in an SRAM array can be divided into SCU and MCU events. An SCU event is defined as an isolated single cell upset with no other cell upsets nearby. An MCU event is defined in this work as two or more physically adjacent bits failing in the same exposure. Bits are considered to be physically adjacent for bit upsets in adjacent rows, adjacent columns, or both rows and columns (*i.e.*, diagonal bits). A cross section is defined for both types of events. The single–cell upset cross section, σ_{SCU}, is the cross section for events affecting only one cell and is given by

$$\sigma_{\text{SCU}} = \frac{\text{Event}_{1-\text{bit}}}{\Phi} \tag{2}$$

where $\text{Event}_{1-\text{bit}}$ is the number of SCUs and Φ is the fluence of incident particles.

Similarly, MCU events are characterized by events for a specific number of affected bits in the MCU cluster. Each cluster multiplicity has a distinct cross section. The cross section for an MCU event with i affected bits, $\sigma_{i\text{–bits}}$, is

$$\sigma_{i\text{–bits}} = \frac{\text{Event}_{i-\text{bit}}}{\Phi} \tag{3}$$

where i is the number of affected bits in the MCU cluster, $\text{Event}_{i-\text{bit}}$ is the number of events with i bits in the MCU cluster, and Φ is the fluence of incident particles. By this definition events are only counted once regardless of the number of events and $\sigma_{i\text{–bits}}$ represents the cross section for an event of i–bit size.

The total cross section for all MCU events, σ_{MCU}, is the event cross section for clusters of 2–bit upsets and larger, with each MCU event counting as one event, independent of the number of bits upset. σ_{MCU} is given by

$$\sigma_{\text{MCU}} = \sum_{i=2}^{\infty} \frac{\text{Event}_{i-\text{bit}}}{\Phi} = \frac{\text{Event}_{2-\text{bit}} + \text{Event}_{3-\text{bit}} + \text{Event}_{4-\text{bit}} + \ldots}{\Phi} \tag{4}$$

where the sum of σ_{SCU} and σ_{MCU} represents the total number of events. This deweighting of MCU event multiplicities allows for equal comparison of SCU and MCU events such that an explicit definition of MCU probability is defined.

Probability of MCU

The probability of MCU is an important characteristic of the MCU radiation response because of the role it plays in memory architecture design [10]. Error

detection and correction (EDAC) in memory arrays are susceptible to multiple upsets. The probability of MCU reflects the susceptibility of a technology to MCU events that may pose EDAC reliability concerns for the device. The probability of MCU is the fraction of events that result in an MCU. The probability can be written as

$$\text{Probability Of MCU} = \frac{\sum_{i=2}^{\infty} \text{Event}_{i-\text{bit}}}{\sum_{i=1}^{\infty} \text{Event}_{i-\text{bit}}} \tag{5}$$

where the summation in the numerator counts MCU events and the summation in the denominator counts all events. Note, regardless of the multiplicity of the event, each event is counted only once and are not weighted.

MCU Dimension Analysis

By convention, the size of MCU events is characterized by the number of affected bit (*e.g.*, 2–bit, 3–bit, 4–bit, *etc...*). However, this does not detail the shape of the MCU event or the spatial distribution of the upsets. For the purpose of the present discussion, a better metric of size is the affected area in dimensions of rows and columns. In this manner, the dimension of an MCU event can be written as

$$\text{MCU Dimension} = \text{N}_{\text{row}} \times \text{N}_{\text{col}} \tag{6}$$

where N_{row} is the number of affected rows and N_{col} is the number of affected columns. MCU dimension is illustrated in Fig. 5. The example illustrates a 3×3 bit array where the red blocks indicate bit upsets. Fig. 5a is an example of a SCU

event. All 1×1 events are SCUs. While Fig. 5b and Fig. 5c are both examples of 2×2 events, their bit multiplicities are 2-bit and 4-bit, respectively. They are considered to have the same dimension. Note, in this work nearby cell upsets that are not physically adjacent are not considered to be part of the same cluster.

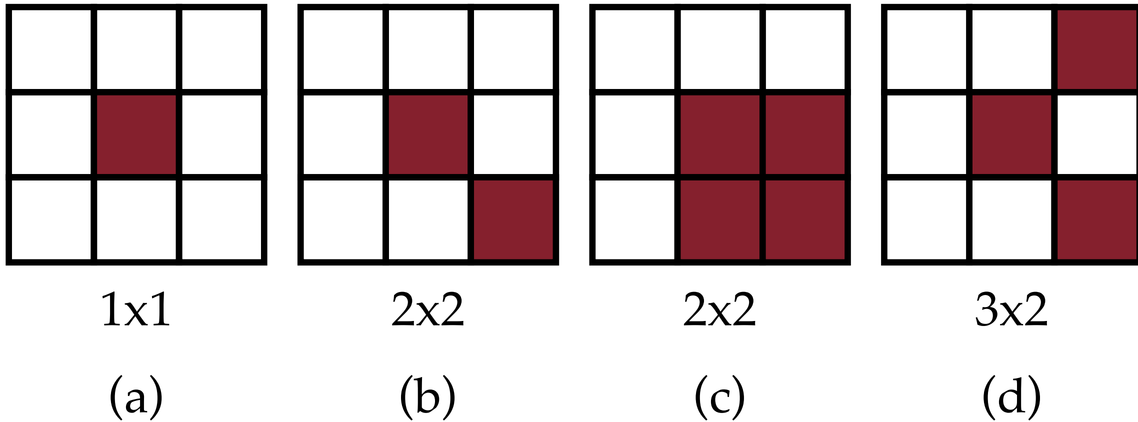


Figure 5: (a) MCU dimension is illustrated for SCU events. All SCU events are 1×1 events. (b) and (c) MCU events with dimension 2×2 are illustrated for two different event types. While their dimensions are the same, (b) is a 2-bit event and (c) is a 4-bit event. (d) A 3×2 3-bit upset is illustrated

Summary

In this chapter, the methods for quantifying MCU have been identified. SEU measurements are conventionally used to characterize the SEE response of memory arrays. All SEUs are characterized as SCU or MCU events. MCU events are characterized by the bit multiplicities of MCU clusters and the dimension of the MCU event. The MCU probability is an important metric for a technology.

CHAPTER IV

NEUTRON MCU RADIATION RESPONSE

In this chapter orientation effects from accelerated neutron irradiations are presented. The experimental detail and results are presented and then the MCU response is discussed. Neutrons incident at grazing angles (*i.e.*, parallel to the device surface) double the number of MCU events compared to normally incident neutrons. Additionally, the neutrons incident at grazing angles produce MCU events with the largest multiplicities (*i.e.*, number of affected bits).

Experimental

The device under test was a high performance 6–transistor (6T) SRAM from a Texas Instruments (TI) 90 nm bulk CMOS process that operated at 1.2 V. Neutron irradiations of the SRAM were carried out at Los Alamos National Laboratory's (LANL) Weapons Neutron Research (WNR) facility using the ICE House neutron beam line. The energy distribution of the WNR neutron beam closely resembles the shape of the atmospheric neutron energy distribution at sea level, though the flux is scaled 10^6 times greater. Fig. 6 shows both the ground–level neutron flux scaled by a factor of 10^6 and the ICE House neutron beam flux at WNR [82]. The ICE House beam closely tracks the ground–level flux out to approximately 600 MeV and then rapidly falls off for higher energies.

Neutron irradiations were performed by placing the device in the ICE house beam line. Irradiations were performed at 0°, 45°, and 90° angles of incidence to

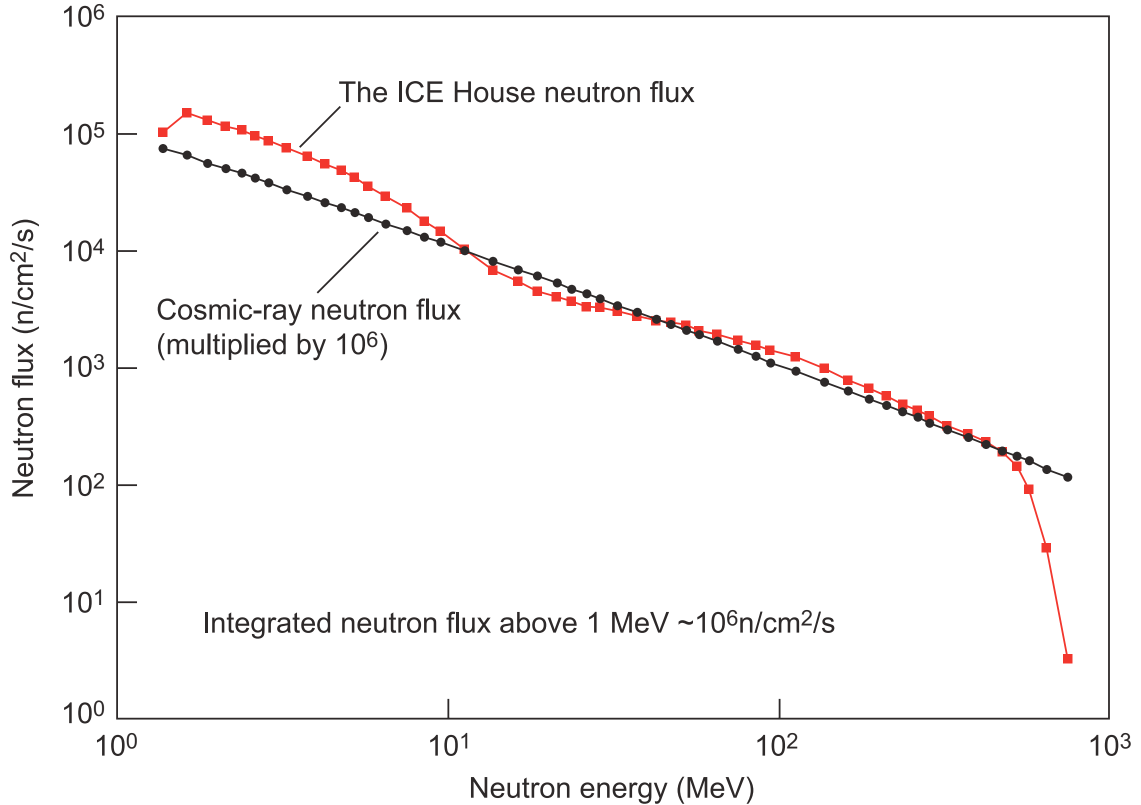


Figure 6: Ground–level neutron flux scaled by a factor of 10^6 and the ICE House neutron flux at WNR. The ICE House beam closely tracks the ground–level flux out to approximately 600 MeV and then rapidly falls off for higher energies [82].

the device surface. The device orientation with respect to the incident neutrons is shown in Fig. 7. The arrow indicates the angle of incident neutrons with respect to the surface of the die. The neutron response was measured by rotating about one axis of the device. Neutrons incident normal to the device surface correspond to 0°, while 90° neutrons arrive at a grazing angle of incidence. At 90° the test board was turned into the beam so the incident neutrons were not directly incident to the surface of the die. Rather, they are incident on the edge of the test board. Because

neutrons only interact through nuclear forces, the flux and energy distribution of the beam remains relatively unchanged at the active device.

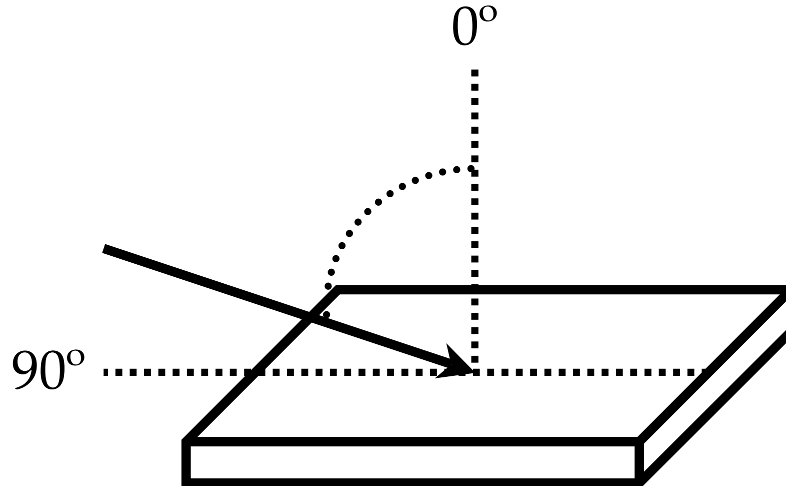


Figure 7: The device orientation is illustrated for neutrons incident on the device. The arrow indicates the direction of incidence as measured from normally incident 0° neutrons. At the largest grazing angle, 90°, the test board is rotated so that neutrons are not directly incident on the device surface. Rather, they are incident on the edge of the test board.

The memory was periodically read during irradiation to record bit errors. The flux of incident neutrons was monitored using a fission ionization detector [83]. Error data were time stamped so that SCU and MCU events could be identified.

Single Event Upset Response

Fig. 8 shows σ_{SEU} for the three angles of neutron irradiation using Eq. 1. The experimental σ_{SEU} varies little with angle of incidence for the three orientations. The error bars represent counting statistics and the error associated with the beam fluence.

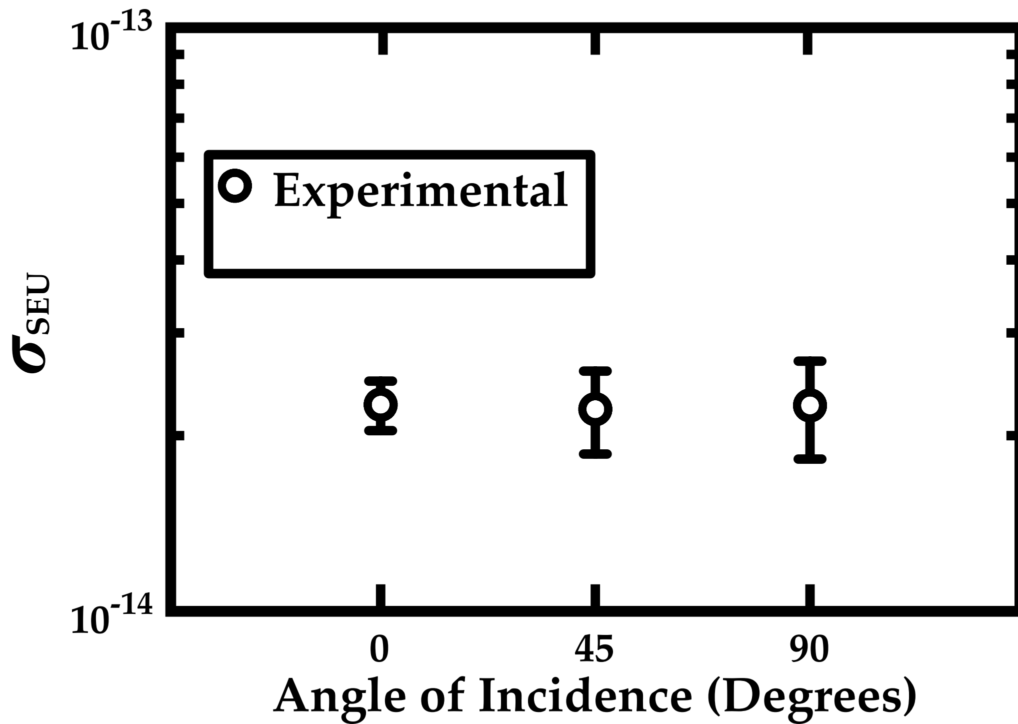


Figure 8: The experimental SEU cross section σ_{SEU} is plotted for the three different rotation angles. The SEU response varies little with the orientation of the device. The error bars represent the counting statistics and the error associated with the beam fluence.

Multiple Cell Upset Response

In this experiment, MCU is defined as two or more physically adjacent bits failing within the same memory read. Each occurrence meeting this criterion is counted as one MCU event. Fig. 9 shows the cross section for events that induce upsets in two or more adjacent cells and is calculated using Eq. 3. A value with no upset rate means no upset of that multiplicity was observed. This figure demonstrates that the average number of bits upset per MCU event increases with

the angle of incidence. The greatest number of MCUs occurs at 90°, and those events have the largest event multiplicities. At normal incidence, 89% of MCU events are two-bit events and only one event greater than three bits was recorded. The average MCU sizes for MCUs greater than two bits are listed in Table 1.

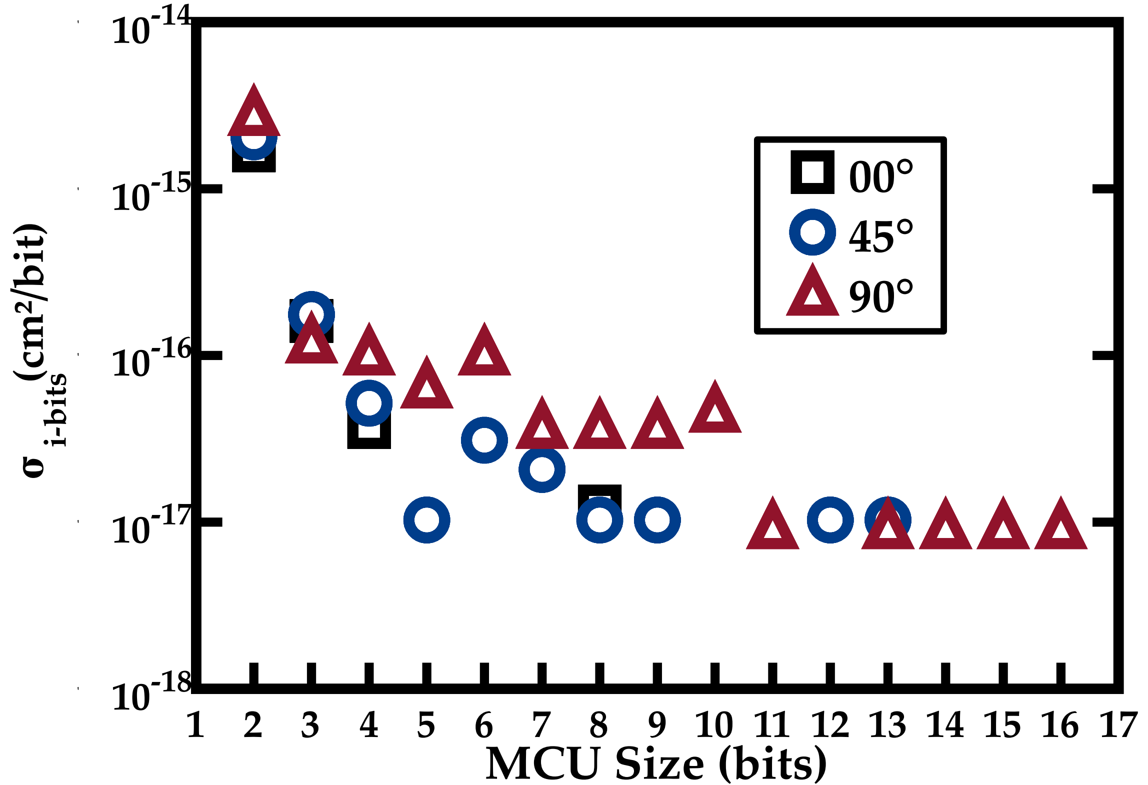


Figure 9: The $\sigma_{i\text{–bits}}$ is shown for MCU events larger than two-bits. The greatest number of MCU events and largest sized MCU events are seen at the largest angle of incidence, 90°. The average MCU size for MCUs greater than two bits is 3.4, 5.2, and 6.4 for 0°, 45°, and 90°, respectively.

Table 1: Average size of MCU clusters from neutron irradiation.

Angle of Incidence	Average Cluster Size
0°	3.4
45°	5.2
90°	6.4

Probability of MCU

The probability of MCU represents the probability that an event will upset multiple cells. Fig. 10 shows the probability of MCU at the three angles of incidence calculated using Eq. 5. Each probability is normalized to the MCU probability when neutrons are incident normal, 0°, to the device surface. The probability increases as the angle of incidence increases. The largest probability is at the highest grazing angle, 90°. In contrast to the σ_{SEU}, the probability of MCU doubles for angles farthest from normal incidence. The orientation of the device with respect to the neutron beam affects the MCU probability.

Summary

In this chapter, the impact of device orientation on the neutron–induced MCU response of a highly–scaled 90 nm technology has been examined. The accelerated neutron response was measured by rotating the device in front of the neutron beam. The SEU response is independent of the orientation, but the MCU response is not. The probability of MCU doubles at grazing angles when compared with irradiations at normal incidence. Additionally, neutrons incident at grazing angles produce the bits for MCU clusters and on average the largest events.

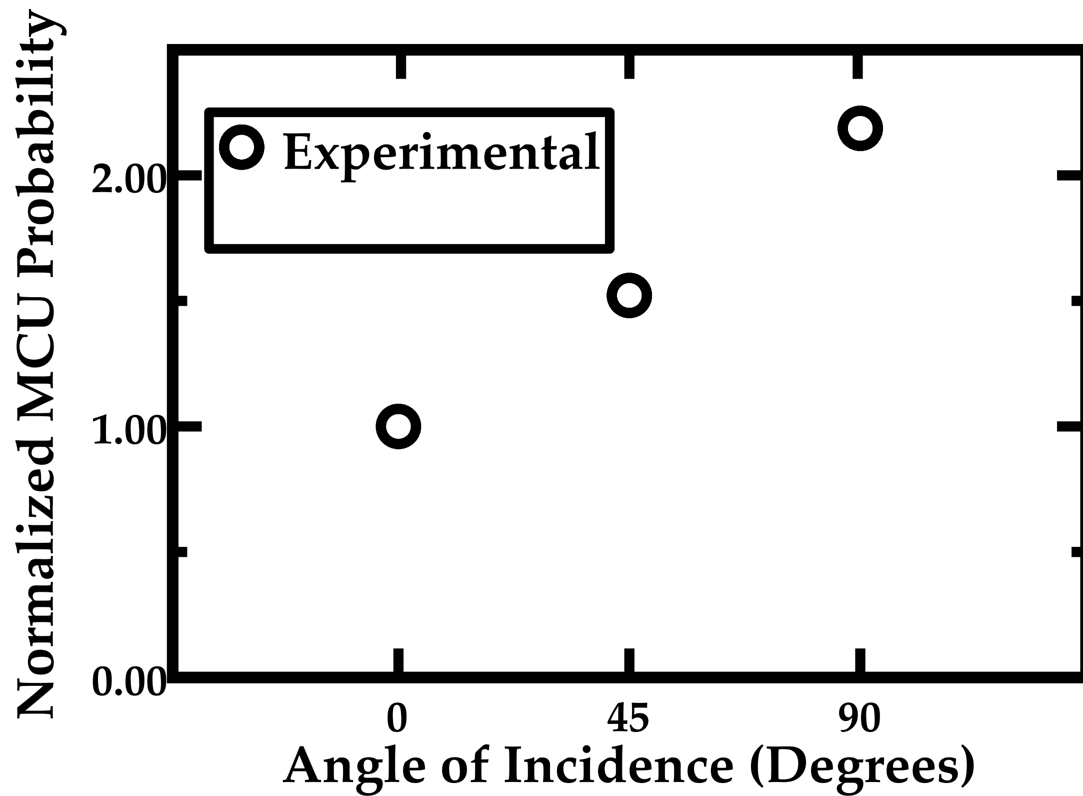


Figure 10: The probability of MCU is shown for the three angles of irradiation normalized to neutrons at normal incidence. The probability increases at grazing angles with the highest probability seen at the largest grazing angle, 90°. In contrast to the σ_{SEU}, the probability of MCU depends on the orientation of the device with respect to the beam.

These data are used in Chapter VI to analyze the MCU response in a ground–level neutron environment. In a realistic environment, neutrons are incident from all angles of incidence. MRED simulations in Ch. VI, calibrated to the data presented in this chapter that account for the orientation dependence, will be used to examine the sizes of MCU clusters.

CHAPTER V

HEAVY ION MCU RADIATION RESPONSE

In this chapter accelerated heavy ion irradiations are reported. The experimental detail including a description of the technology and results from heavy ion irradiations are presented. A discussion of the experimental results includes an analysis of the MCU events. MCUs exhibit a strong dependence on the axis of rotation of the device relative to the incident heavy ion beam for any LET. For higher LET ions, the probability of MCU approaches 100%; almost all events upset more than one bit. The sizes and shapes of the MCU events change for the different device orientations.

Technology

The device under test in this chapter was fabricated in a TI 65 nm bulk CMOS process. The test die contained 4 Mbit of a density–optimized SRAM. The SRAM operated at 1.2 V. The nominal n–well bias was 0.7 V for this test die. The die was bonded directly to a test board to reduce obstruction of the heavy ion beam by the packaging of the device at oblique angles of incidence. An FPGA–based tester was used to write and read the memory between irradiations [84].

Irradiations were carried out at several angles of incidence. The board was rotated about both the x–axis and y–axis, making two distinct die orientations to the beam. The orientations of the die will be described with respect to the

SRAM layout. The layout of the SRAM array results in alternating columns of n–MOSFET and p–MOSFET devices. From a macroscopic view, the chip is laid out with alternating columns of n–wells (containing p–MOSFET devices) and p–wells (containing n–MOSFET devices).

Fig. 11 illustrates the orientation. The alternating blue and red columns represent the wells of the device. Rotation about the x–axis is referred to as "along–the–wells" rotation because ions incident at this orientation move along the long length of the wells. Y–axis rotation is referred to as "against–the–wells" because ions incident at these angles are perpendicular to the well lengths. Additionally, the cell pitch plays an important role in the SEE response. For these cells, the cell pitch in the against–the–wells direction is twice the pitch of the along–the–wells direction. The trajectories of incident heavy ions are illustrated at the bottom of Fig. 11 by the arrows for both orientations.

Experimental

Irradiations were carried out at Texas A&M University's Cyclotron Institute. Three 15 MeV/nucleon ions were used: 299 MeV ^{20}Ne (2.8 MeV-cm^2/mg), 596 MeV ^{40}Ar (8.6 MeV-cm^2/mg), and 1248 MeV ^{84}Kr (28.9 MeV-cm^2/mg). The test board was mounted in the ion beam path and room temperature irradiations were performed at three angles: 0°, 45°, and 79°. The 79° angle was the largest angle such that the chip was not shadowed by the test setup. The die was irradiated in both orientations: along–the–wells and against–the–wells. Fig. 11 shows the board setup and axes of rotation and the trajectories of the incident heavy ions are indicated by the arrows. As the angle of incidence increases, the incident ions

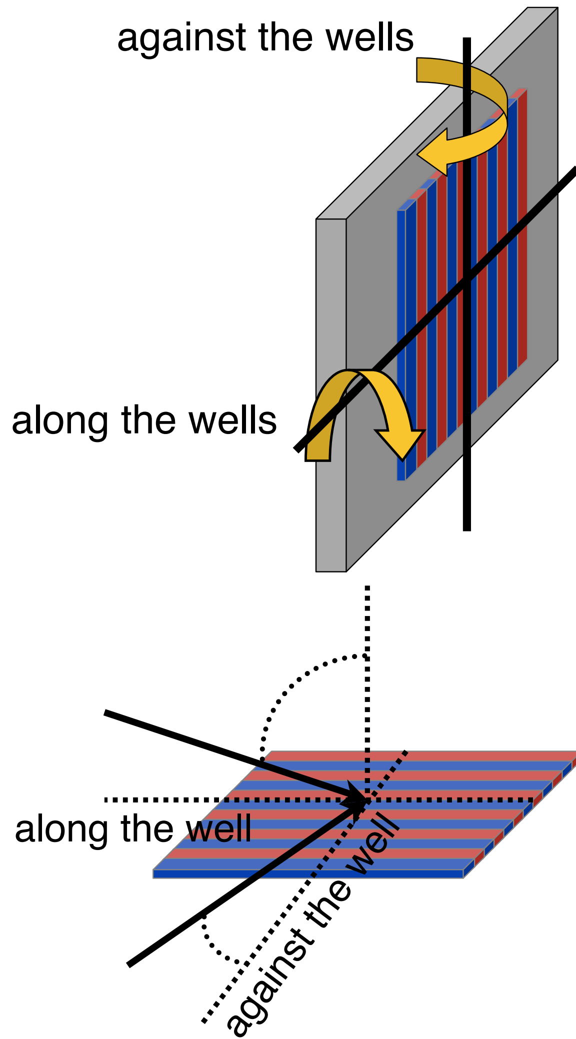


Figure 11: (top) The test board was rotated about the x–axis and y–axis. The alternating blue and red columns represent the n– and p–wells of the die. The two die orientations are defined from the wells. Rotation in the direction of the wells is called "along–the–wells" rotation while rotation in the perpendicular direction are called "against–the–wells" rotation. (bottom) The trajectories of incident ions is shown for the two orientations.

pass through more of the overlayers above the active silicon surface. The LET for each ion at the surface of the device and the estimated LETs at the silicon surface for each angle of incidence are listed in Table 2.

Table 2: LET for experimental ions at the surface of the die and the estimated LET at the silicon surface for each angle of incidence.

Ion	Energy (MeV)	LET ($MeV–cm^2/mg$) @ Die Surface	0° @ Si Surface	45° @ Si Surface	79° @ Si Surface
^{20}Ne	299	2.8	1.9	3.0	2.1
^{40}Ar	596	8.6	8.5	9.3	6.6
^{84}Kr	1248	29	28	33	23

An FPGA–tester was used to write the bits before irradiation and read them after it [84]. The logical addresses of the errors were recorded at the end of each exposure. The addresses were decoded so the physical location on the die could be determined. The upset locations were analyzed to locate SCU and MCU events.

Single Event Upset Response

SEU cross sections of the memory were calculated using Eq. 1 and are shown in Fig. 12 for all device orientations. The cross section data in Fig. 12 are shown at each ion's angle of incidence. The SRAM exhibits a cross section that increases with LET. The cross section varies little with angle and orientation for each ion type, except for the lightly ionizing ^{20}Ne at the highest angle of rotation in the against–the–wells direction.

σ_{SCU} is plotted in Fig. 13 for all device orientations using Eq. 2. The cross sections in Fig. 13 show a range of responses. The σ_{SCU} varies over an order of

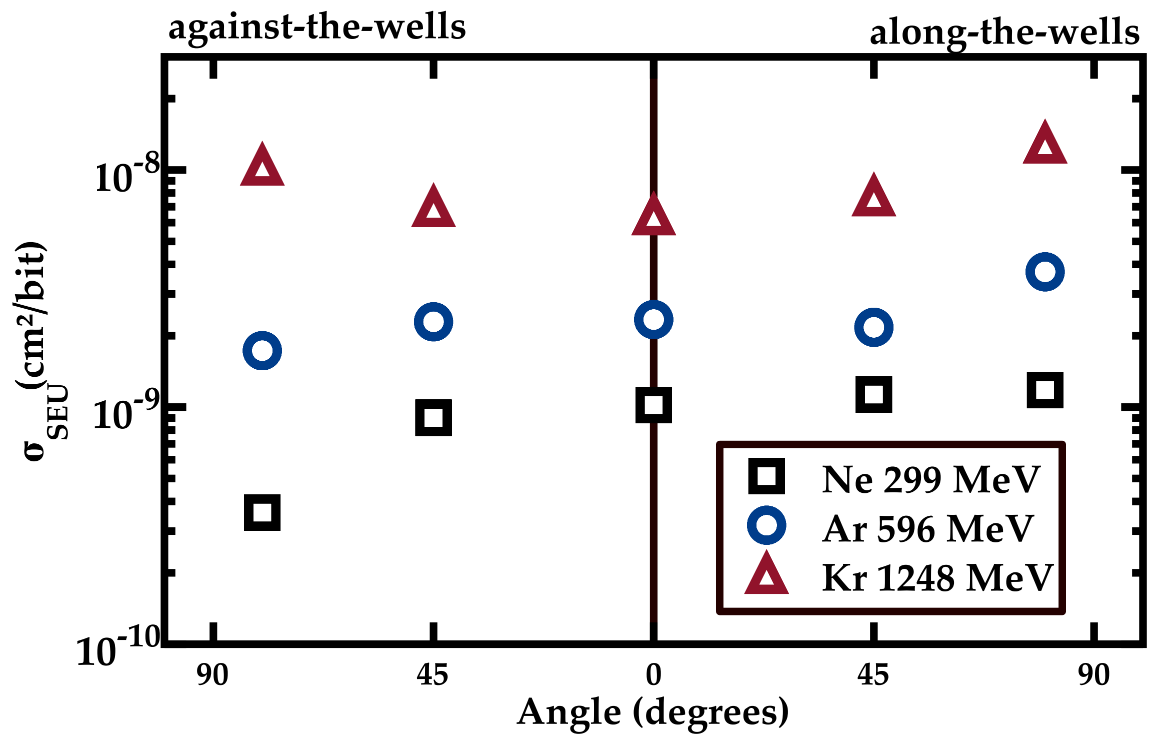


Figure 12: The single event upset cross section, σ_{SEU}, increases with LET and varies little with the orientation of the device. Cross sections are plotted for both device orientations. LET values are taken at the top of the device.

magnitude for ^{20}Ne. The orientation of the device strongly influences the heavy ion response for ions with low LET. At higher LET values, the device is less sensitive to device orientation for SCU.

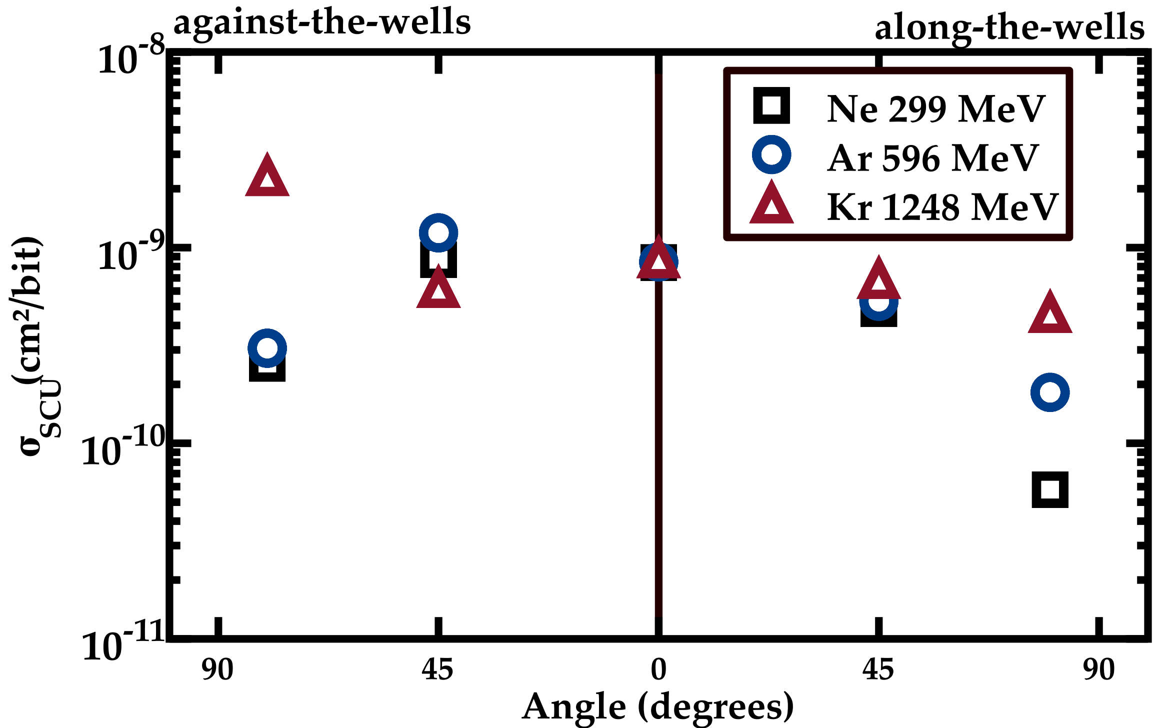


Figure 13: The single–cell upset cross section, σ_{SCU}, is plotted for both device orientations. In contrast to the SEU response, σ_{SCU} varies for each orientation. Reduced cross sections are observed at large angles of incidence because heavy ions at these angles have higher probabilities of MCU (see Fig. 15).

Multiple Cell Upset Response

Fig. 14 shows the MCU event cross section σ_{MCU} for the SRAM. Low fluence exposures were used to reduce the likelihood of an MCU event from two separate ions. σ_{MCU} increases with LET for both axes of rotation. σ_{MCU} is comparable to

σ_{SEU}, implying a high probability of MCU. Approximately 200–800 errors were recorded for each irradiation with each point representing 3–5 irradiations. Run–to–run variation in the cross section is small enough that the error bars have been omitted for clarity. The probability inducing upset in two adjacent cells with two different ions can be approximated a Poisson distribution. The probability is given by

$$P(\text{k}) = \frac{e^{-\lambda}\lambda^{k}}{k!} \tag{7}$$

where P(k) is the probability of two ions striking the same region, λ is the expected or average value and k is the number of occurrences. In this analysis, λ is the average number of cells upset

$$\lambda = \frac{\text{totalUpsets}}{4 * 10^{6} / 9} \tag{8}$$

where totalUpsets is the total number of upsets recorded, $4 * 10^{6}$ is the number of total bits, and 9 accounts for the region of influence (*i.e.*, for a single cell, there are eight possible cells that can be upset). The fraction of two or more upset from two or more ions is given by

$$1 - P(0) - P(1) \tag{9}$$

where P(0) is the fraction of regions with no upsets and P(1) is the fraction of regions with a single upset. Using Eqs. 7–9 yields a probability of $5.68 * 10^{-6}$.

Figs. 12–14 illustrate the impact of device orientation relative to the incident

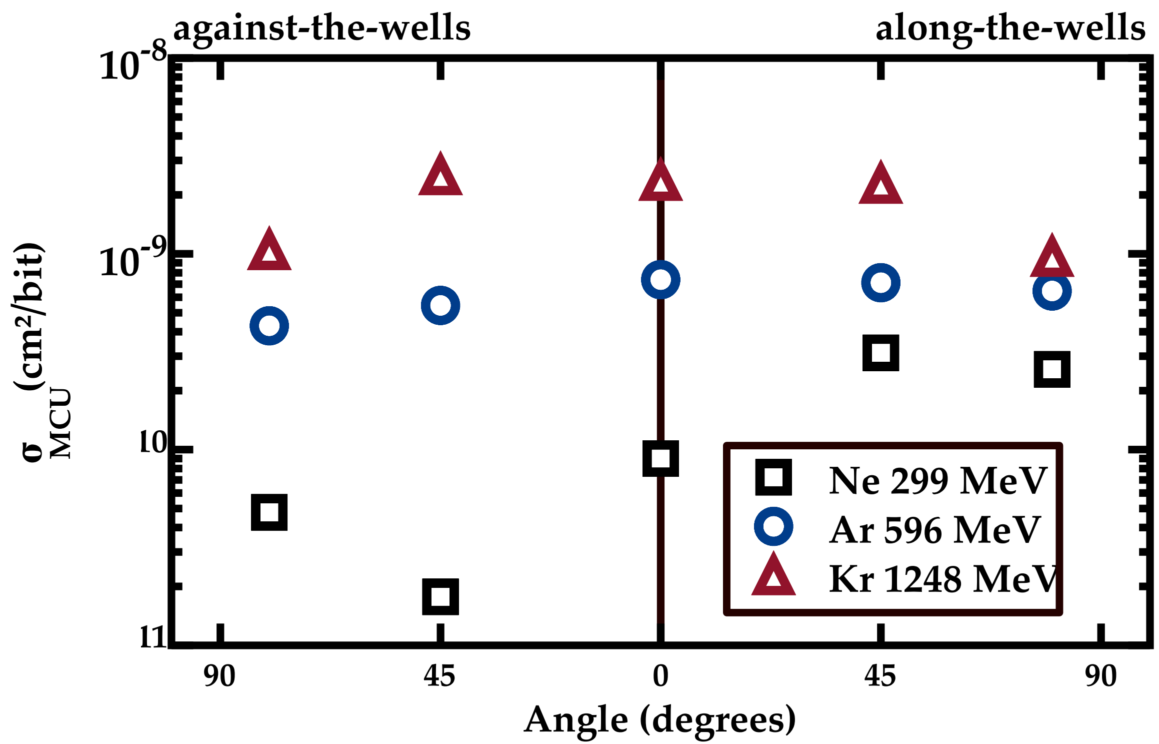


Figure 14: The multiple–cell upset cross section, σ_{MCU}, is plotted for both device orientations. The MCU response for the lightly ionizing ^{20}Ne exhibits variation for different device orientations. The shorter cell pitch in the along the wells directions increases σ_{MCU}.

heavy ions. The cell area, on the order of 10^{-9} cm^2, is comparable to the σ_{SEU} in Fig. 12. Sufficient charge generation in a nearby cell may lead to upset. The comparable cell area and cross section implies that events initiated at almost any location are capable of generating sufficient charge to upset the cell. The layout of this particular cell design is approximately twice as long as it is wide and yields a cell pitch in the against–the–wells direction that is twice the cell pitch in the along–the–wells direction. The cell pitch affects the probability of MCU, as discussed below.

Probability of MCU

The probability of MCU increases when devices scale to smaller dimensions [10]. The increase in MCU probability is a reliability concern for error correction because multiple errors may be more difficult to correct. Fig. 15 shows the MCU probability for rotation against–the–wells (left) and along–the–wells (right) using Eq. 5. At large angles, MCU probabilities approach 100% for both orientations. The trajectories of the incident ions at grazing angles are nearly parallel to the SRAM array and the ions interact with more cells, increasing the probability of MCU. The ^{20}Ne ions show the lowest probabilities when rotating against–the–wells. The probability is reduced because of the ion's low LET and larger cell pitch in the against the wells direction. Device orientation strongly impacts the MCU probability for the more lightly ionizing ^{20}Ne.

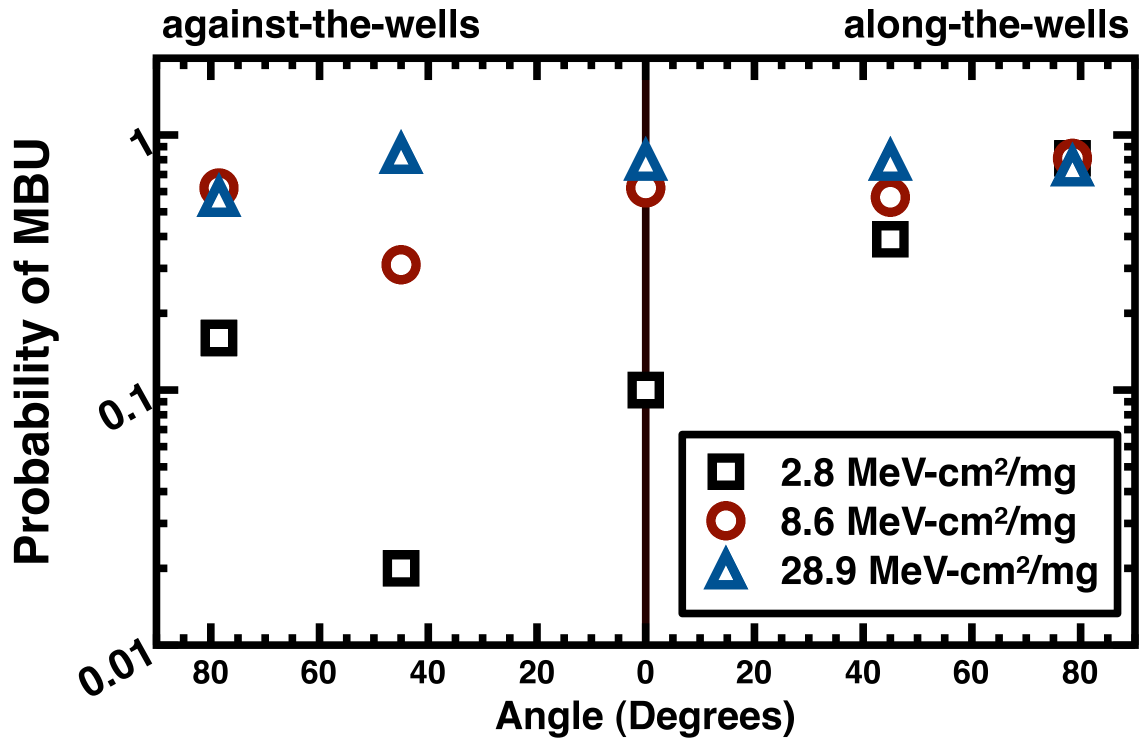


Figure 15: The probability of MBU is plotted for the against–the–wells orientation (left) and the along–the–wells orientation (right). The probability approaches 100% at large angles of incidence because the ion trajectories travel through more cells. The against–the–wells rotations exhibit lower probability for lightly ionizing ions because they produce less charge and the cell pitch is larger for these rotations.

Orientation Comparison

Fig. 16 shows the distribution of MCU dimensions for ^{40}Ar at 0°. The bars represent the counts for each dimension normalized to all events. The majority of events are 1×1 SCUs. Single and double–cell upsets account for 98% of all events at this orientation.

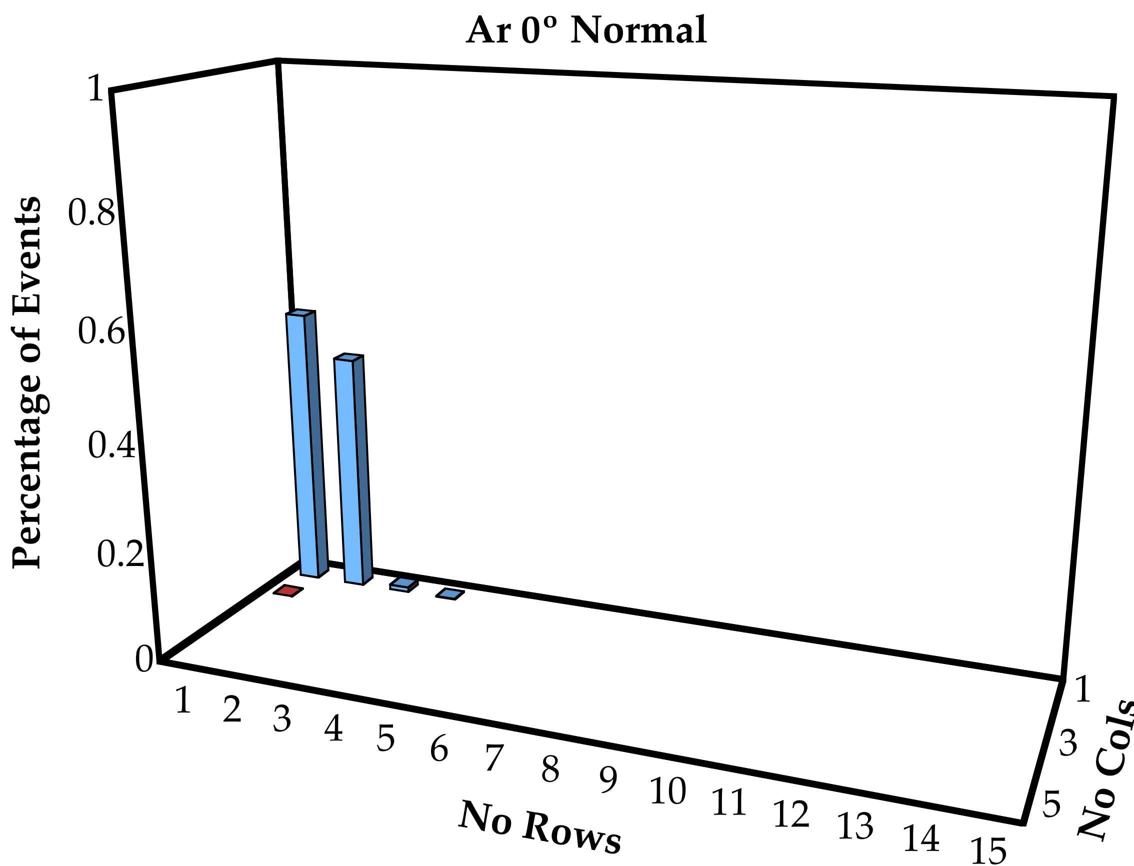


Figure 16: Normalized counts of MCU events for ^{40}Ar at 0°. The majority of events are 1×1 single–cell upsets. Single and double–bit upsets account for 98% of all events at this orientation.

In order to examine the worst case MCU response, the device was rotated to

a grazing angle. Fig. 17 shows the distribution of MCU events for the ^{40}Ar ions at the 79° grazing angle with ions incident in the along–the–wells direction. The majority of events at this orientation are single column events. This is consistent with the direction of incident particles. In the along–the–wells orientation, the trajectories of the heavy ions are in the direction of the long length of the columns, traversing multiple rows. The resulting MCU events are characterized by many affected rows and few affected columns. For the ion and orientation in Fig. 17, the largest events affect up to 15 rows. In comparison, the maximum number of affected columns, three, is relatively small.

For comparison to the along–the–wells orientation in Fig. 17, the against–the–wells orientation is shown in Fig. 18. The MCU response in Fig. 18 is shown for the same ion, ^{40}Ar, and the same angle of incidence, 79°, but the device was rotated to the against–the–wells orientation. In this orientation, the ions' trajectories are perpendicular to the wells and parallel to the long length of the rows, traversing multiple columns.

The dependence on device orientation for MCU event can be seen by comparing Fig. 17 and Fig. 18. MCU events in the against–the–wells orientation are smaller than those in the along–the–wells orientation. These events are smaller because the cell pitch in the against–the–wells direction is double the cell pitch in the other direction. Ions incident in this orientation must travel a longer distance between cells. Additionally, in the along–the–wells orientation charge can be confined to a single well (refer to Fig. 11). Long path lengths through the wells can lead to greater charge sharing and modulation of the well potential [66,67]. In the

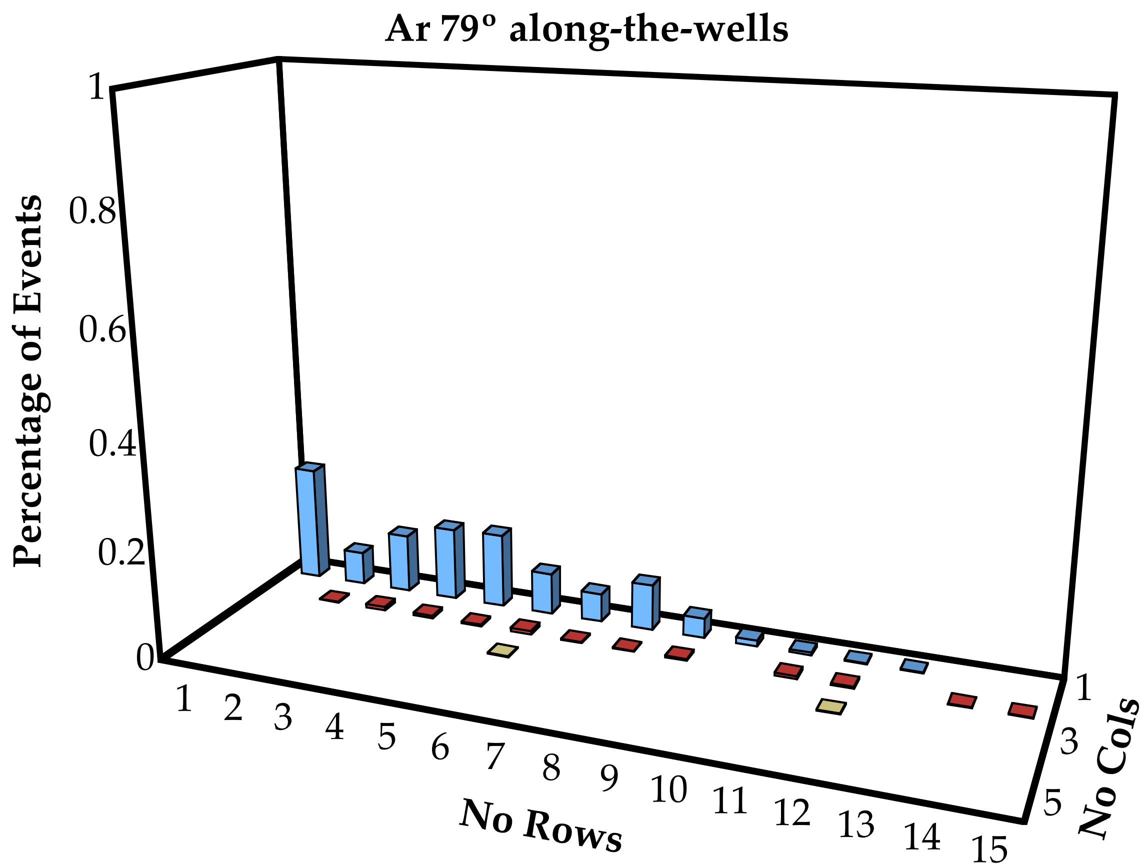


Figure 17: Normalized counts of MCU events for ^{40}Ar at the worst case 79° in the along–the–wells direction are shown for the number of affected rows and columns. MCU events at this orientation affect primarily one column because the trajectories of the heavy ions is parallel to the SRAM columns.

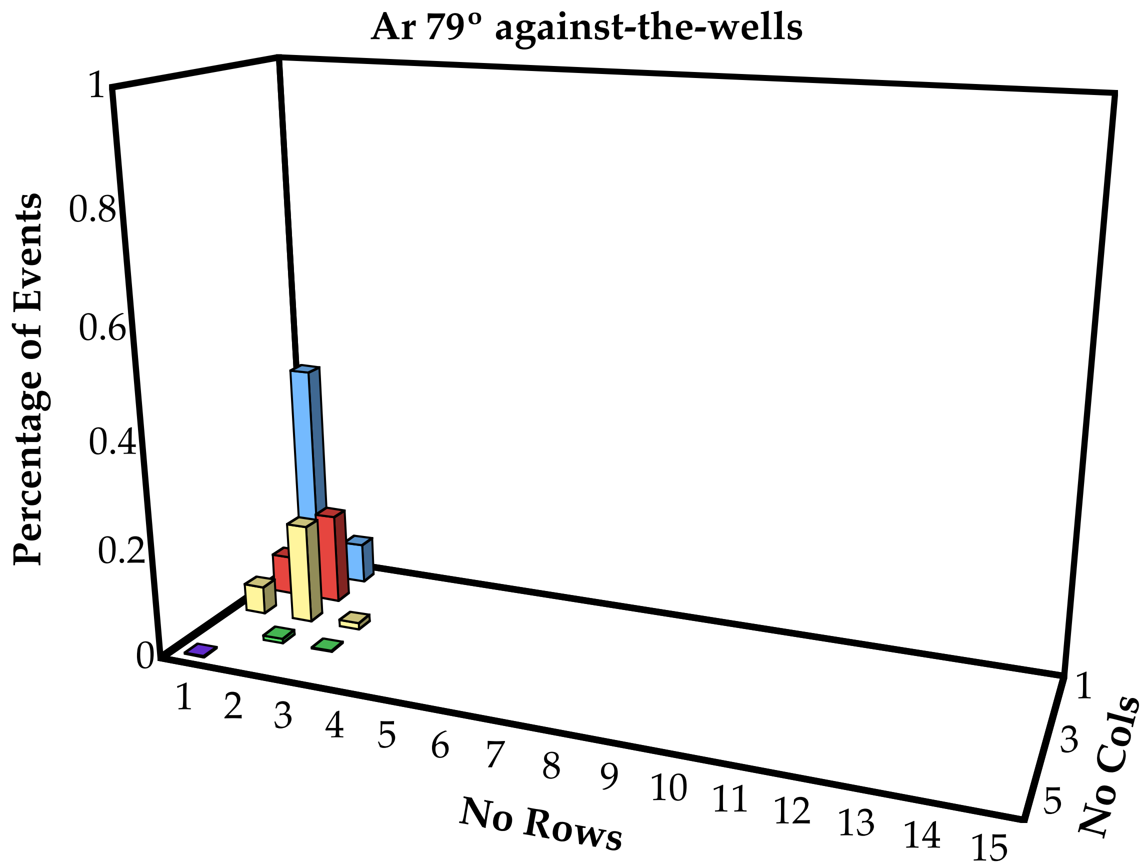


Figure 18: Normalized counts of MCU events for ^{40}Ar at worst case 79° in the against–the–wells direction are shown for the number of affected rows and columns. The trajectories of heavy ions is parallel to the rows in this direction.

against–the–wells orientation, the ion's path is separated by the alternating wells and less charge sharing takes place.

Ion Comparison

The normally incident Ar ions in Fig. 16 can be compared with normally incident Ne and Kr ions in Fig. 19 and Fig. 20, respectively. The majority of events from the more lightly ionizing Ne ions are SCUs. These account for approximately 95% of all events at normal incidence. In contrast, the Kr ions, SCUs only account for approximately 40% of events. The probability of MCU is relatively high at this orientation. A comparison of all three ions at normal incidence reveals the increasing sizes and probabilities of MCU events.

For heavy ions incident at grazing angles, the sizes of events increases with increasing LET. Figs. 21 and 22 show the grazing angle MCU response for Ne ions and Figs. 23 and 24 show the grazing angle MCU response for Kr ions. Note the difference in the number of affected columns between ions for the along–the–wells orientations. Charge collection for the higher LET Kr ions yields larger events in that direction.

Summary

Accelerated heavy ion irradiations of TI bulk silicon 65 nm CMOS SRAMs have been reported. These devices exhibit σ_{SEU} that is independent of the orientation of the device with respect to the incident heavy ions. The SEU cross section is comparable to the total cell area at the lowest LET, implying a device sensitive to charge generation at any point in the cell. However, irradiations show that the

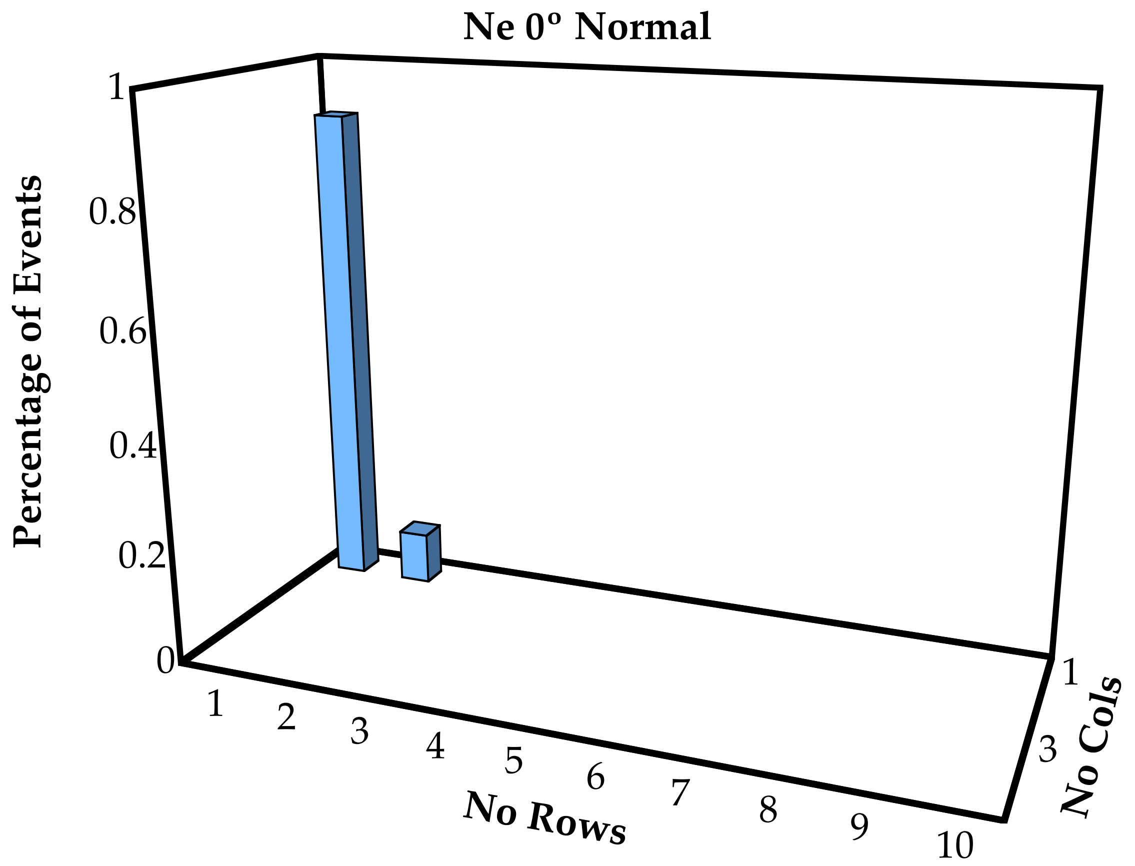


Figure 19: Ne ions incident at 0°.

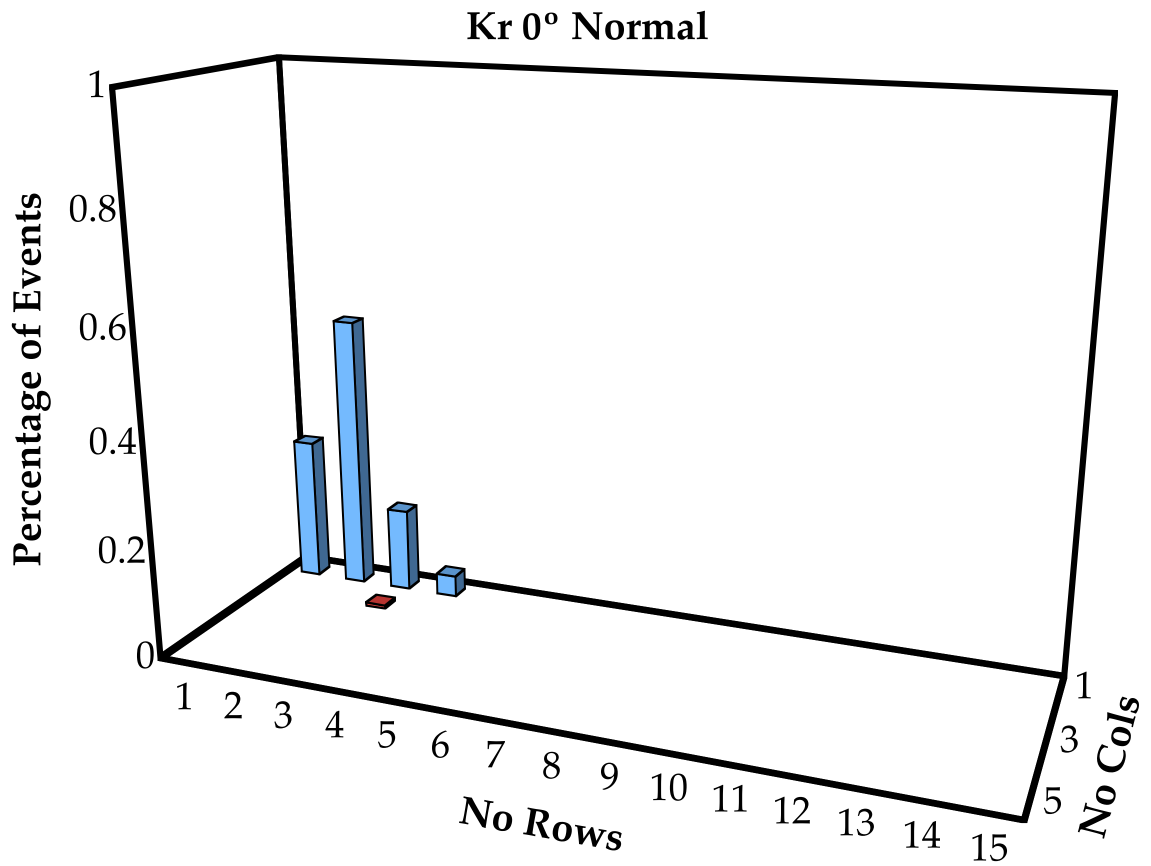


Figure 20: Kr ions incident at 0°.

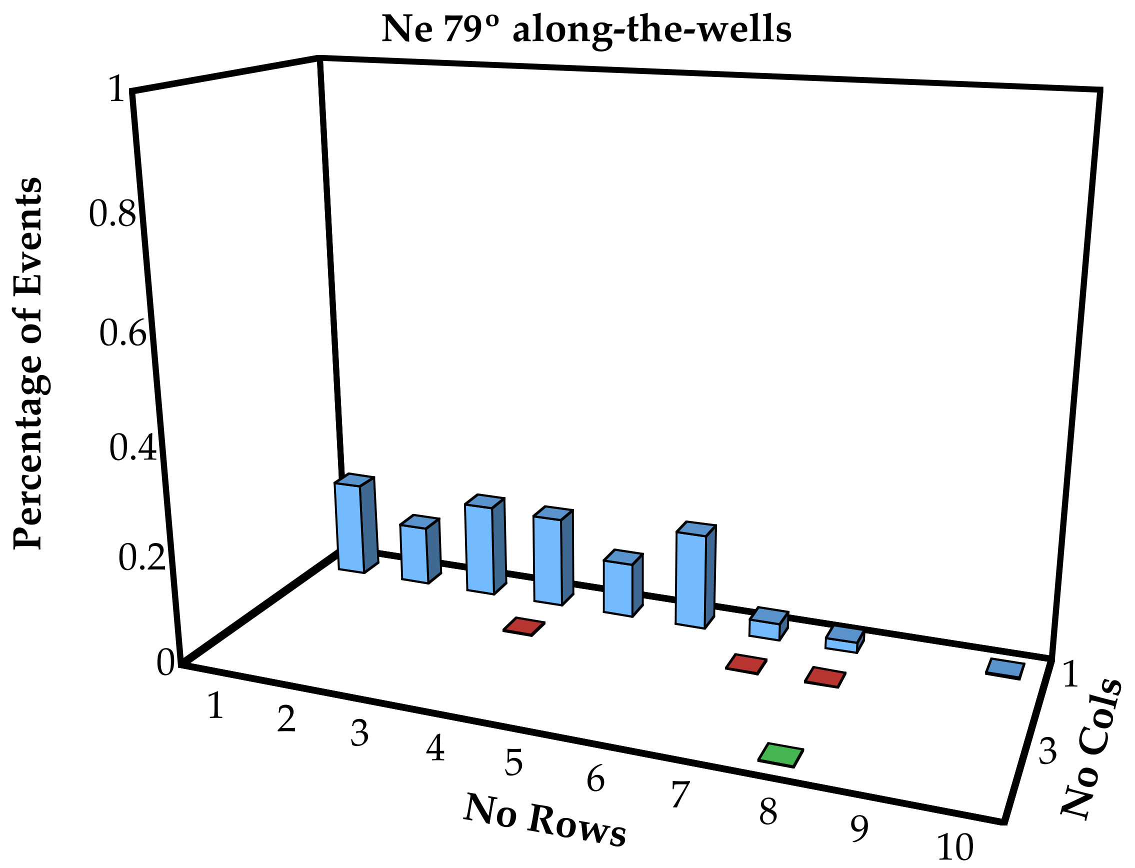


Figure 21: Ne ions incident at 79° along–the–wells.

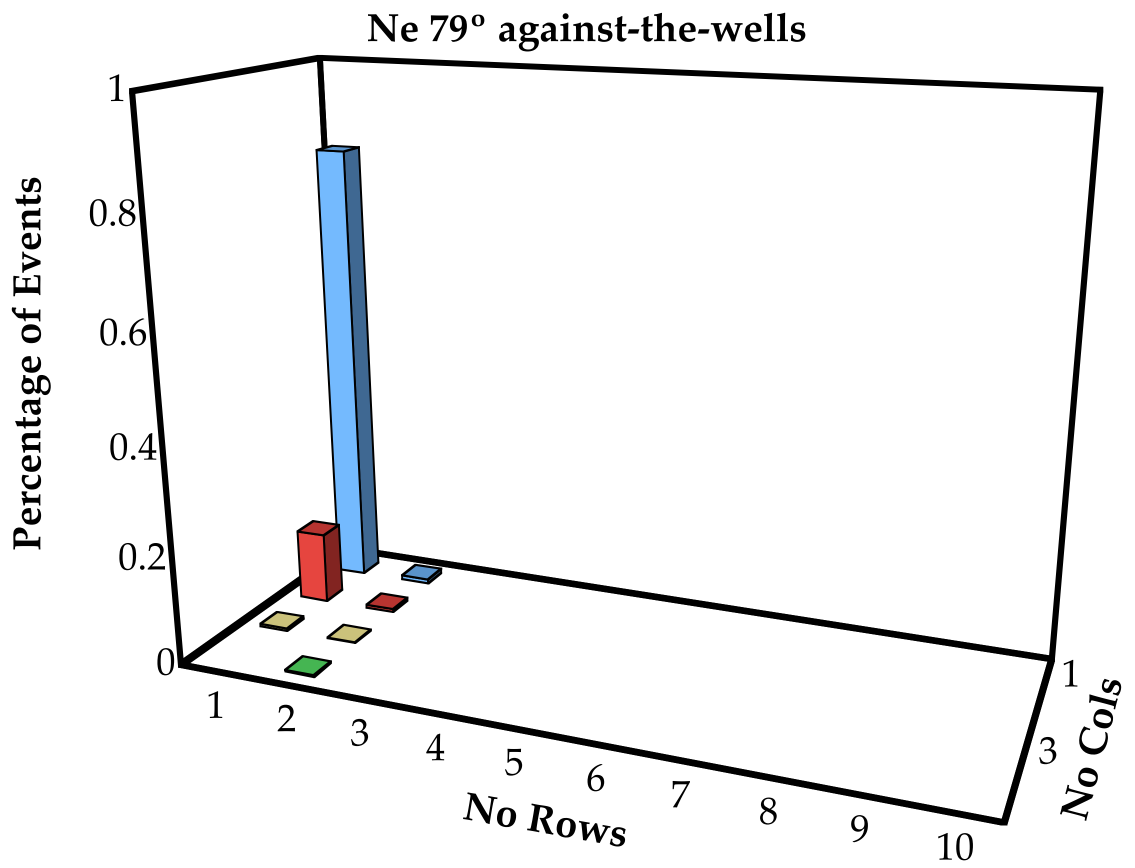


Figure 22: Ne ions incident at 79° against–the–wells.

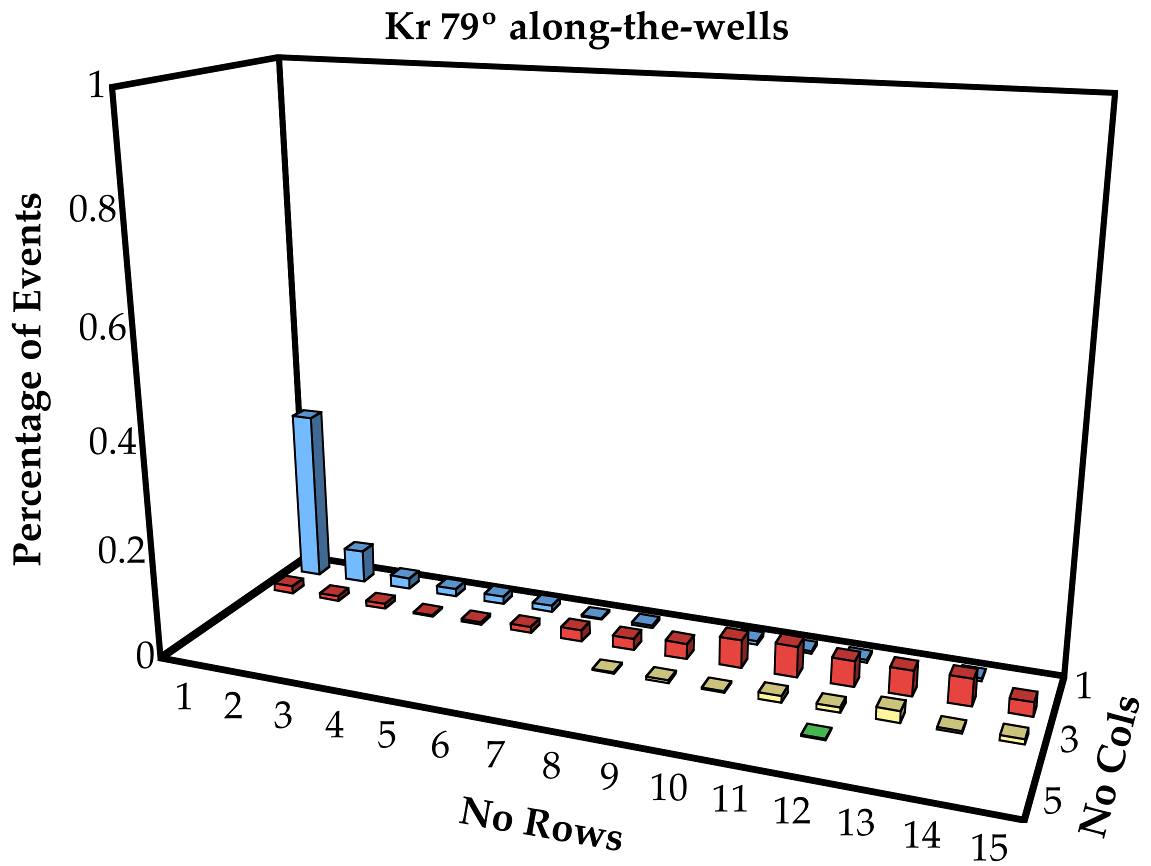


Figure 23: Kr ions incident at 79° along–the–wells.

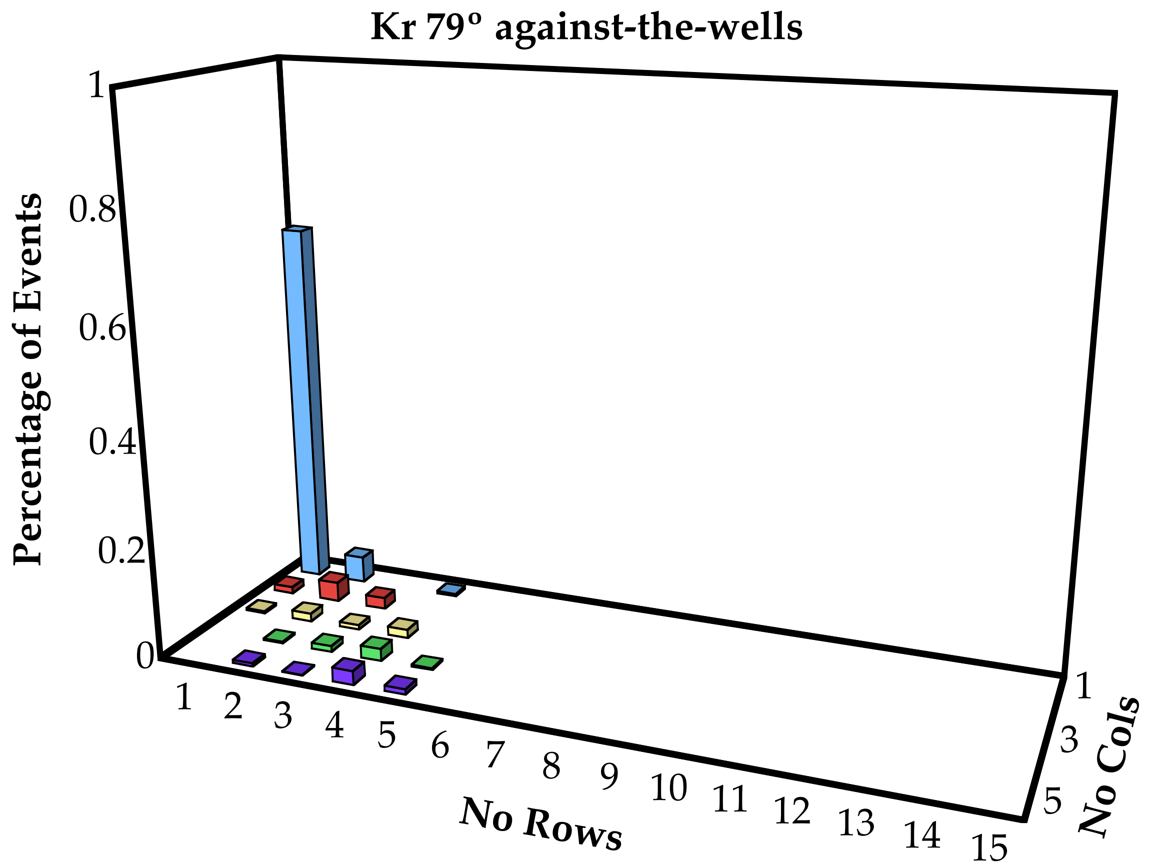


Figure 24: Kr ions incident at 79° against–the–wells.

MBU response depends on the orientation of the device during irradiation. The direction of the incident ions with respect to the layout of the cell is important. While σ_{SEU} for the devices exhibits little dependence on the orientation of the device, the shape and spatial distribution of MBU events changes with orientation. The largest MBU events occur when heavy ions are incident at grazing angles along the n– and p– wells of the device. Histograms for the complete data set can be found in Appendix B.

CHAPTER VI

MODELING MCU

In this chapter energy transport modeling is presented. The modeling methodology is first presented and then simulation results are discussed for two environments: a terrestrial neutron environment and a heavy ion environment for a geosynchronous orbit. Monte–Carlo simulation is used to examine the MCU response in terrestrial and space environments.

Monte–Carlo simulation, using codes such as MRED, is a useful tool in characterizing SEE in highly–scaled technologies. Conventional SER calculation methodologies rely upon accelerated testing to determine the σ_{SEU} over a range of LET values [81]. The resulting σ_{SEU} versus LET data are fit to a curve and used to predict the SER using the RPP model [62, 63, 85]. SER calculations are done using codes such as CREME96 [86]. The underlying assumptions of these codes breakdown in highly–scaled technologies that exhibit angular effects. Warren *et al.* showed the breakdown of the effective LET concept on a hardened–by–design latch where rolling the device and keeping the effective LET constant produced σ_{SEU} that varied as much as four orders of magnitude [30]. Additionally, such SER calculations do not account for heavy ion nuclear reactions that have been shown to under–predict on–orbit SER [27]. In addition to MRED, several other energy transport codes have been used to model soft errors [79, 87–91].

In this chapter, Monte–Carlo simulations are calibrated back to experimental data for all experimental orientations. In this manner, these models account for

any orientation dependence. Probabilistic simulation of energy transport is used to show the MCU response in an environment.

Modeling methodology

The modeling methodology is outlined in Fig. 25. The methodology begins by creating a detailed physical structure of an SRAM cell. Energy transport is then calculated for the structure using Monte–Carlo simulation. An analysis of the energy deposition is performed for each particle event to determine SCU and MCU events.

Physical Model

The physical model of the SRAM cell is created using the Synopsys TCAD tool Sentarus [92]. The Sentarus TCAD tool suite comprises computer programs for modeling semiconductor devices. The Sentarus Device tool is a semiconductor device simulator used to solve the partial differential equations associated with semiconductor devices. Sentarus Structure Editor is used to define the materials and geometry of the device.

The Sentarus Structure Editor is used to create a physical TCAD model of the SRAM cell. Process emulation is used to create the structure by importing the layout file of the SRAM cell. The back–end–of–line (BEOL) information from the process is used to determine the dimensions of the materials above the silicon surface. High–fidelity physical models that incorporate all BEOL information are important to account for energy deposition accurately. The presence of high-Z materials, such as tungsten, has been shown to increase error cross-sections in

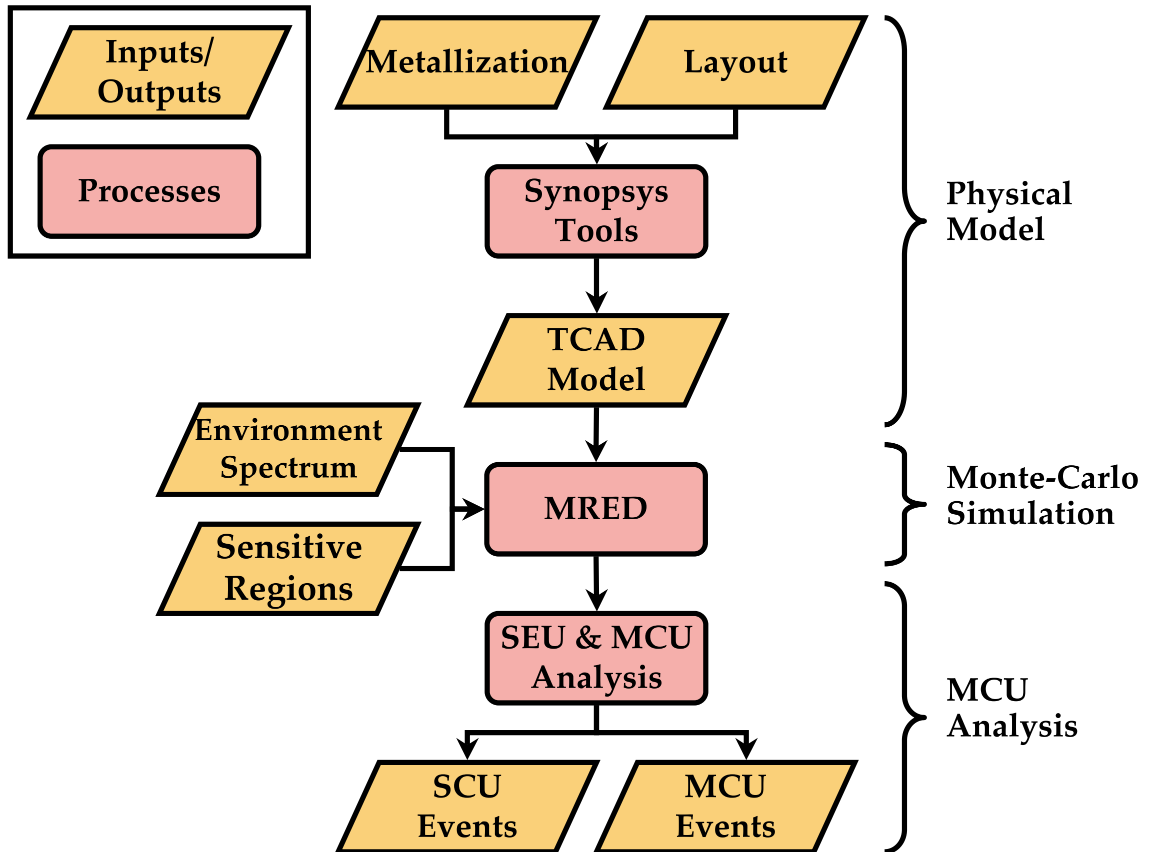


Figure 25: MCU modeling methodology. This methodology uses the Synopsys TCAD tools to create a physical model. MRED simulates energy transport through the structure and the results are analyzed to determine MCU events.

technologies with larger feature sizes [27–29]. Dielectrics containing borophosphosilicate glasses (BPSG) have been shown to impact the error rate from thermal neutron interactions with some boron isotopes [32]. All materials present in the experimental device have been included in simulation. Six layers of copper metal and tungsten vias are included in the physical model of the TI process. Fig. 26 shows an example of a TCAD model for a single SRAM cell. The interlayer dielectrics are omitted in the illustration to expose the metal interconnects and vias. Six layers of copper lines, tungsten vias, and the silicon bulk are visible.

Monte–Carlo Simulation

Radiation transport simulation was performed using MRED (Monte–Carlo Radiative Energy Deposition) [24,25]. MRED is a Monte–Carlo transport code based on the Geant4 libraries [26]. These libraries model the transport of radiation through matter. The Geant4 libraries contain models for ionization and and nuclear processes. MRED simulates random probabilistic radiation events using Monte–Carlo methods and creates statistical energy deposition profiles for the simulated structure. Events can be monitored on an event–by–event basis to determine MCU.

The TCAD model from Fig. 26 is imported into MRED. Because the physical model represents only a single SRAM cell, MRED duplicates the structure into an array of cells as defined by the user. The MRED structure is made large enough to account for edge effects for ions at the largest angles of incidence. In this manner, the size can be optimized for the performance of the code. In this work the size

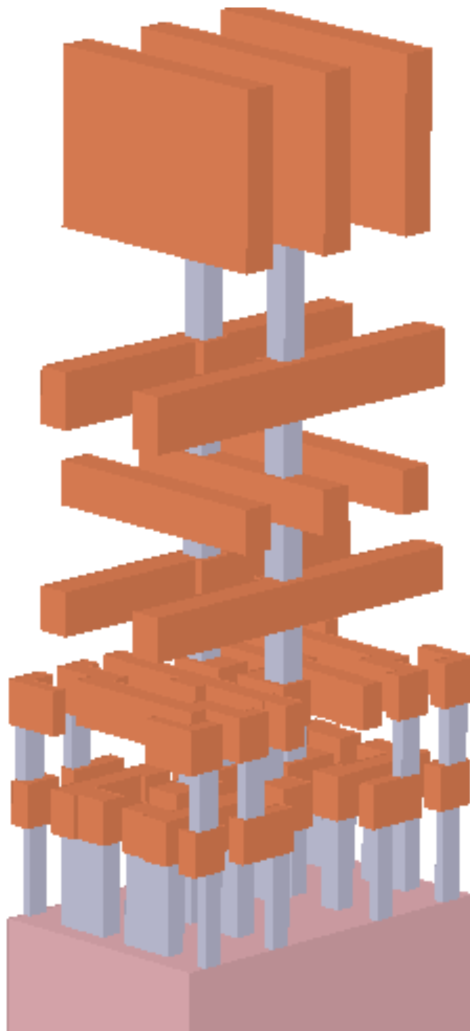


Figure 26: Physical model of a single SRAM cell created using Synopsys TCAD tools. Six layers of copper lines, tungsten vias, and silicon bulk are visible. Layout and BEOL characteristics of the process are used to create the structure. This structure is used by MRED to simulate radiation transport.

of the array was kept at 50 μm $\times$ 50 μm; these dimensions are sufficiently large for the largest MCU events.

The Sensitive Region

When a charged particle passes through matter, its energy loss leads to charge generation. The charge generated by an event is subject to normal drift and diffusion transport processes and may also recombine. The charge remains in the semiconductor material until it recombines or is collected by a contact. From a circuit perspective, upset occurs when sufficient charge is collected at a circuit node to change the logic state of the circuit. For the case of the SRAM cells considered here, the circuit sensitive nodes are associated with OFF-state n-MOSFET and p-MOSFET devices. Associated with each cell is a Q_{Crit} required for upset.

Charge collection is approximated in MRED by defining a sensitive region associated with the junction of a circuit sensitive node. When charge is transported to the pn–junction, the charge is then swept away by the electric field and collected at the contact. The volume around the junction of the sensitive node is termed the sensitive region because charge generated in and around this region may be collected and lead to upset.

These regions are defined in MRED using RPP sensitive volumes. Multiple sensitive volumes are defined for a single region that fully encompasses the region surrounding the junction as in [31]. Associated with each region is a charge collection efficiency α. This efficiency represents the fraction of charge that may be collected from a given region. Because charge further away from the junction has a lower probability of being collected, only a fraction of the charge is counted.

MRED approximates the amount of charge collected on the sensitive circuit node by defining these volumes and their respective efficiencies around the semiconductor device. Fig. 27 illustrates how the regions are defined. Fig. 27a illustrates a junction surrounded by shallow trench isolation (STI). Fig. 27b shows the overlapping sensitive volumes for the junction and their respective charge collection efficiencies. When a charged particles passes through the sensitive volumes as in Fig. 27c, the result is charge generated along the path as indicated in Fig. 27d.

The MRED–estimated total collected charge Q_{total} is given by

$$Q_{Total} = \sum_{i=1}^{n} Q_i \times \alpha_i \tag{10}$$

where Q_i is the charge generated in the *i*-th sensitive volume, α_i is the charge collection efficiency associated with that volume, and n is the number of RPP sensitive volumes. Eq. 10 is written explicitly for the three volumes in Fig. 27e.

MCU Analysis

MRED uses the physical model and sensitive volume definition for simulating energy deposition. On an event–by–event basis, energy transport is simulated through the structure and energy deposition in each sensitive volume is calculated. The Q_{Total} for each SRAM cell in the array is determined. Through circuit and device simulation the total required charge to induce upset, Q_{Crit}, can be calculated. If Q_{Total} for the sensitive region of a single SRAM cell is more than this value, then MRED counts an upset of the SRAM cell.

An example of a MRED–simulated event is shown in Fig. 28. The detail of the

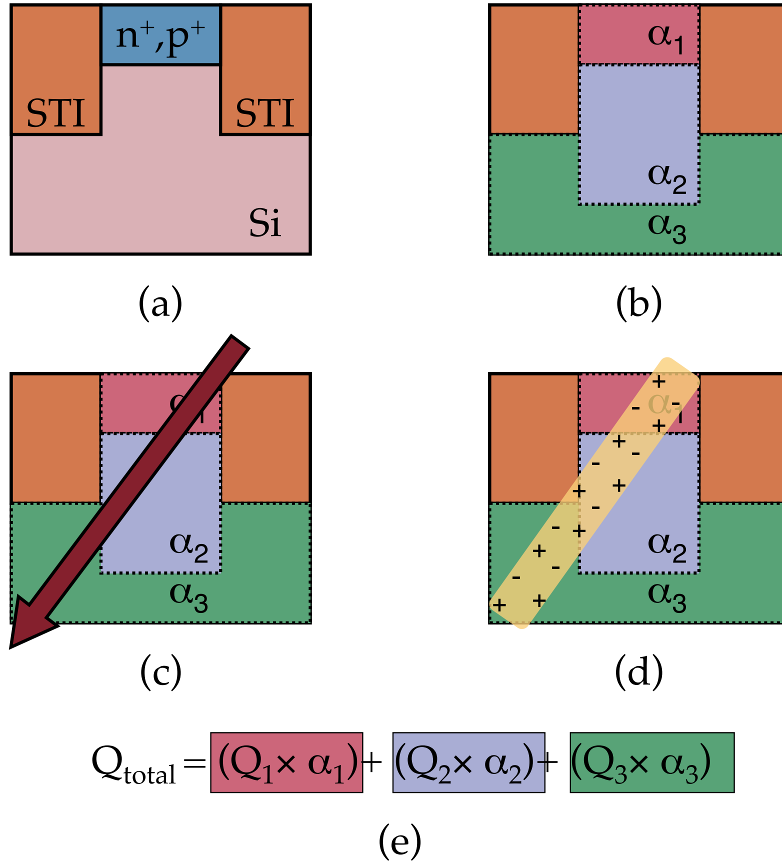


Figure 27: (a) The sensitive volume description begins with the junction of a sensitive node. (b) A set of sensitive volumes is defined for the sensitive region. Associated with each sensitive volume is a charge collection efficiency α. (c) The path of a charged particle passing through the sensitive volumes is illustrated. (d) Charge is generated along the path and Q_{total} is calculated using Eq. 10. (e) The explicit equation for Q_{total} in this illustration is shown.

BEOL metallization can be seen at the top of the figure. The incident heavy ion enters from bottom to the bulk silicon. The trajectories of the incident ion and secondary products are detailed by the colored lines. In this illustration a nuclear reaction can be seen near the surface of the silicon. MRED details each event like the one in Fig. 28 and calculates the energy deposited to determine Q_{Total} for each cell.

For each MRED event, MRED's python interface calls a python function to post process each event. For MCU analysis a specific python function was written. At the end of each MRED event the function call calculates the energy deposited in each cell's sensitive region and determines Q_{Total}. Upsets are identified on a cell by cell basis. Upsets inside the SRAM array are located by their coordinates. Coordinates of each upset are compared for proximity. SCU and MCU clusters are identified and recorded.

Discussion

In this section, simulation results for terrestrial and geosynchronous environments are presented. The models for each are based on the technologies in Ch. IV and Ch. V. The test data presented in those chapters are used to calibrate the simulations and then MRED is used to examine the MCU response for each environment.

Terrestrial Environment

The modeling methodology in Fig. 25 was used to model the TI 90 nm SRAM and experimental data presented in Ch. IV. The physical model included the

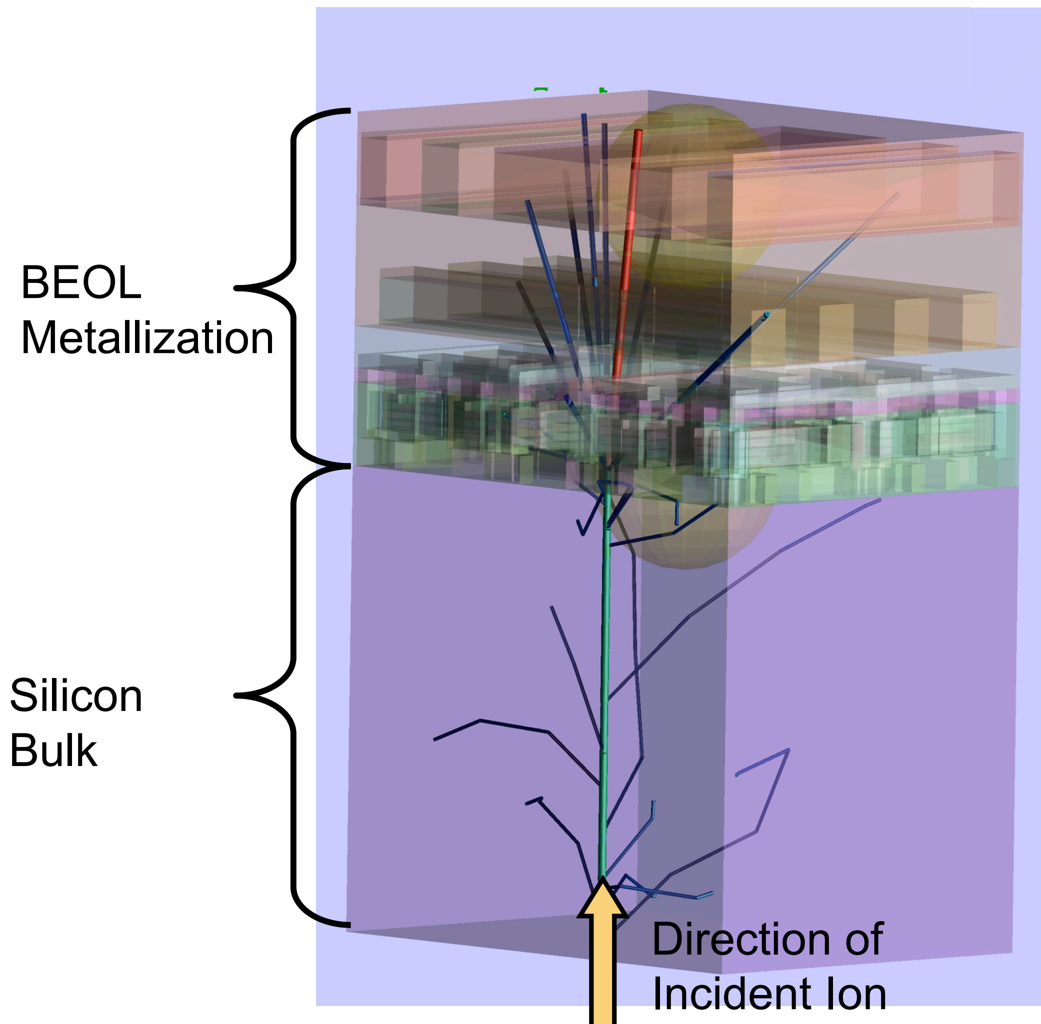


Figure 28: Example MRED generated event. The BEOL material is shown a the top of the figure. The incident heavy ion enters through the bottom of the bulk silicon and induces a nuclear reaction near the surface of the silicon. The trajectories of the incident ion and secondary products are detailed by the colored lines. Courtesy of Marcus Mendenhall.

layout and BEOL characteristics of the process. Only a single sensitive volume corresponding to the junction of the OFF state n–MOSFET transistor was used for each cell. Calibration of the device used the ICE House beam spectrum from Fig. 6.

Energy Deposition Profiles

For each neutron event simulated by MRED, energy deposition by the secondary products was tracked in and around each memory cell. Fig. 29 shows one such event. Only the bulk silicon is shown for clarity. The shaded volumes represent the regions in which charge is collected surrounding the sensitive volume of the SRAM cell. The colored lines indicate the trajectories of the incident neutron and secondary products. In this event, the incident neutron induces a nuclear reaction at the silicon surface near a sensitive node. The shower of secondary products includes alpha particles, protons, neutrons, gamma rays, and a carbon heavy ion. The reaction is given by

$$\mathrm{n{+}Si} \rightarrow \mathrm{C{+}3n{+}2p{+}3}\alpha \quad (11)$$

While the carbon heavy ion is the most ionizing particle, it is an alpha particle that produces the MCU event. The range of the alpha particle is large relative to the range of the carbon heavy ion. The charge generated in each sensitive volume is labeled for values greater than 1 fC.

Each event, like the one in Fig. 29, was analyzed to determine the occurrence of SCU and MCU. Histograms of all events were calculated over a range of charge

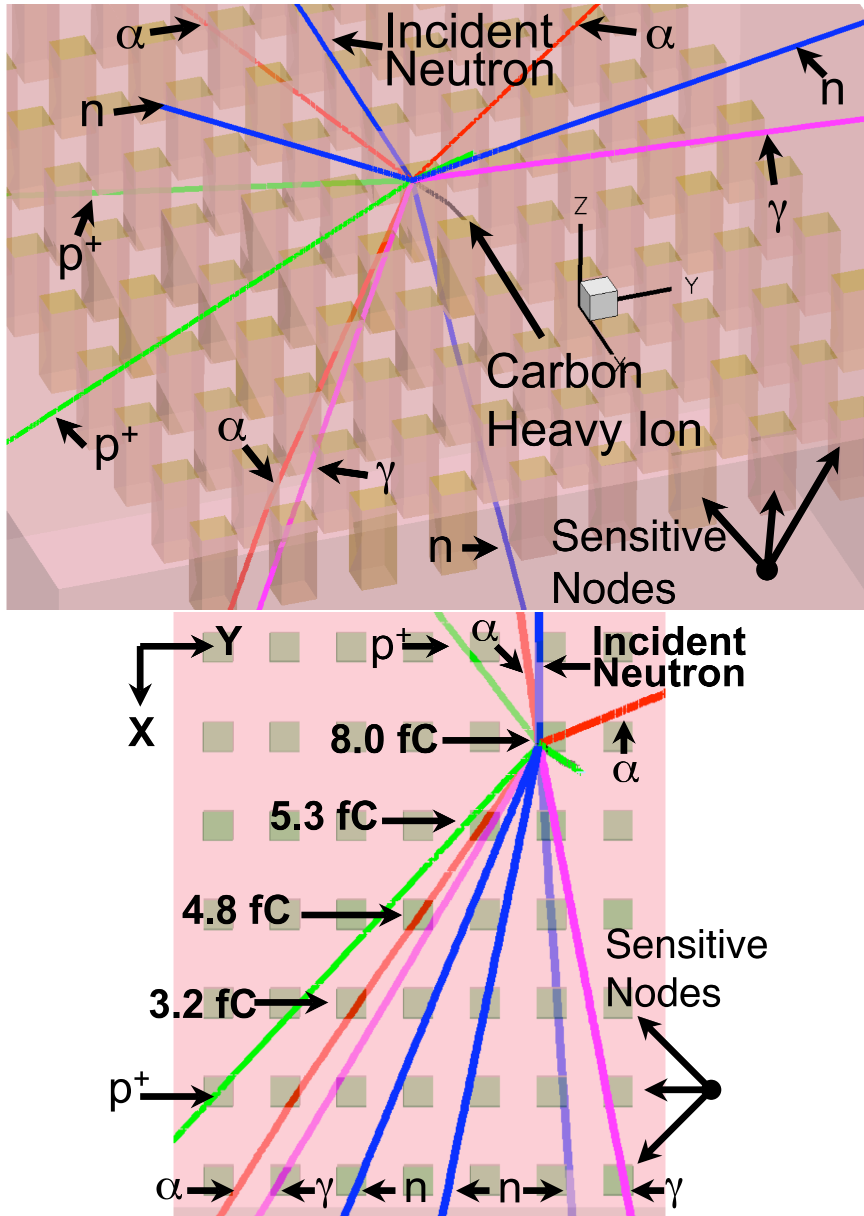


Figure 29: A TCAD representation of an MRED-generated nuclear event. Only the bulk silicon is shown for clarity. The shaded volumes represent the sensitive nodes of the memory device. The incident neutron enters and induces a nuclear event. The shower of secondary products includes alpha particles, protons, neutrons, gamma rays, and a carbon heavy ion (n+Si→C+3n+2p+3α). In the top-down view on bottom, generated charge for sensitive nodes with more than 1 fC are labeled.

generation. A cell will upset if charge greater than Q_{Crit} is generated and collected. For example, the event in Fig. 29 would only count in the MCU histogram for values less than 5.3 fC because if the Q_{Crit} is greater than this value, only one SRAM cell would be expected to upset.

Because the MRED simulation details the amount of energy deposition in each sensitive volume, the σ_{SEU} can be calculated over a range of deposited energies. In this manner, the dependence on deposited energy can be expressed as an energy deposition profile, ED(E), and can be written as

$$\mathrm{ED(E)} = \sum_{i=1}^{\infty} \frac{i \times \mathrm{Event}_{i-\mathrm{bit}}(\mathrm{E})}{\Phi} = \frac{1 \times \mathrm{Event}_{1-\mathrm{bit}}(\mathrm{E}) + 2 \times \mathrm{Event}_{2-\mathrm{bit}}(\mathrm{E}) + \ldots}{\Phi} \quad (12)$$

where $\mathrm{Event}_{i-\mathrm{bit}}(\mathrm{E})$ represents the event dependence of an i-bit upset on the deposited energy and E is the deposited energy. Evaluating each event over a discrete set of energies creates a statistical profile for SCU and MCU with respect to energy deposition. Energy can be converted to charge, recalling that 3.6 eV of energy produces one EHP in silicon. The ED(E) is shown in Fig. 30 for the ICE House beam for the three different device orientations [82]. The upset rate decreases exponentially for charge generation because highly ionizing events from neutrons are less likely. Higher Q_{Crit} will exhibit lower SEU rates. All three orientations exhibit similar responses, implying no orientation dependence.

Evaluating ED(E)curve at the Q_{Crit} of the cell yields the σ_{SEU}. Circuit simulation of the tested TI 90 nm cell suggests Q_{Crit} to be approximately 4 fC. As with the experimental data, the σ_{SEU} shows no dependence on angle of irradiation for any value of critical charge. Simulation results are compared to experimental data

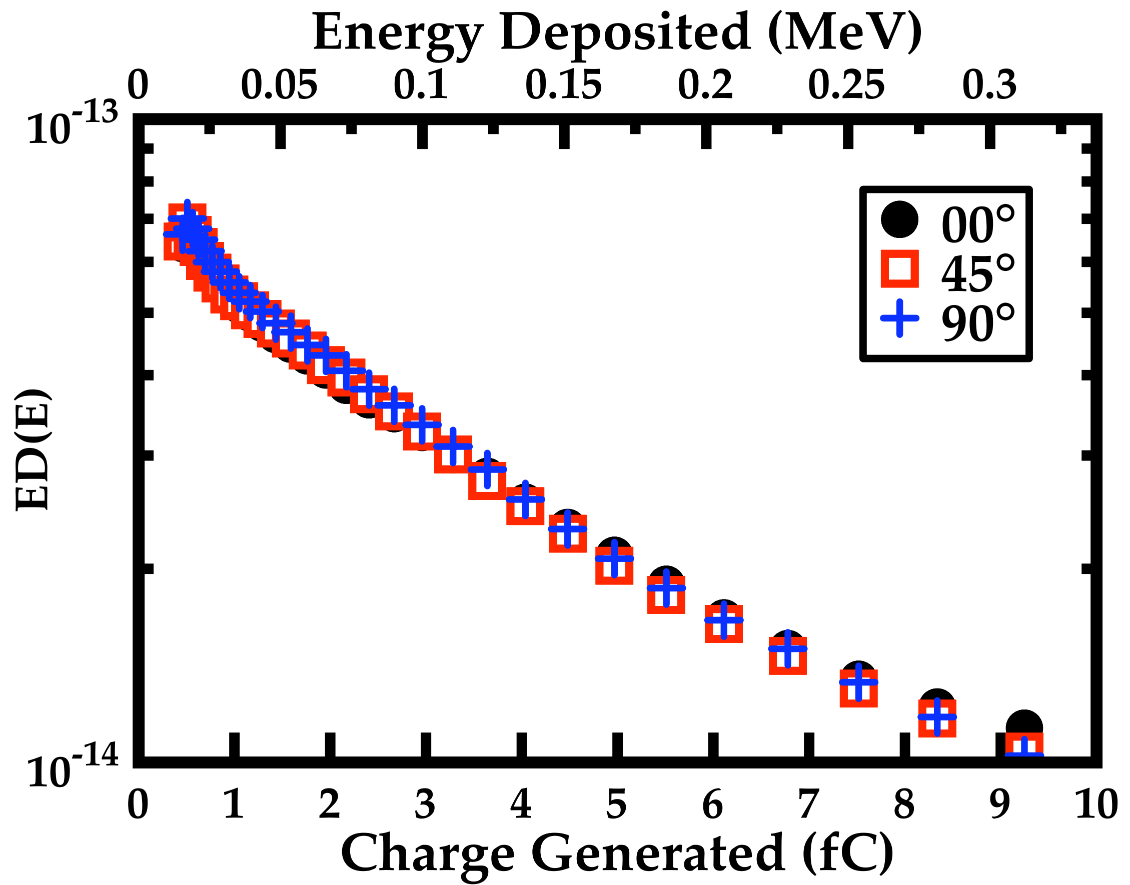


Figure 30: The MRED simulated upset rate versus charge generated for the TI 90 nm SRAM shows little dependence on the device orientation for the ICE House neutron spectrum.

in Fig. 31 for the critical charge of 4 fC. A sufficient number of SEU events, approximately 1000, were recorded during simulation to increase the counting statistics and reduce the error. Simulation error bars are only shown when visible. MRED simulation is in good agreement with the experimental response.

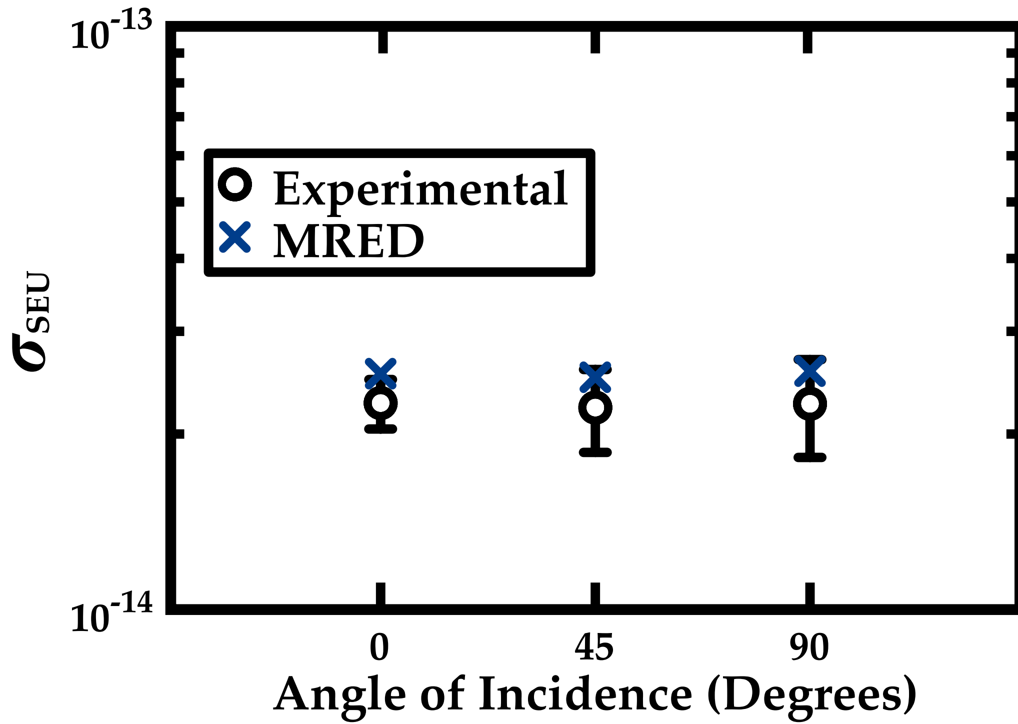


Figure 31: The σ_{SEU}(E) simulated by MRED is compared with experimental data. MRED simulation is in good agreement with the experimental data. Error bars represent the counting statistics for simulation and experimental results and they are only shown when visible.

The probability of MCU can be calculated over a range of discrete energies

from MRED simulation. The probability as a function of energy can be written as

$$\text{Probability Of MCU (E)} = \frac{\sum_{i=2}^{\infty} \text{Event}_{i-\text{bit}}(\text{E})}{\sum_{i=1}^{\infty} \text{Event}_{i-\text{bit}}(\text{E})} \tag{13}$$

The probability of MCU for generated charge is shown in Fig. 32. The probability increases with the angle of the incident neutrons. The probability increases for neutrons at grazing angles because the secondary products from nuclear reactions tend to scatter in the forward direction. At grazing angles, the forward direction is parallel to the surface of the die, increasing the likelihood that the particles will affect more than one cell. The SEU response does not exhibit the same dependence because MCU events only account for approximately 10% of all events, most of those having low multiplicities. The simulated probability is compared in Fig. 33 for a Q_{Crit} of 4 fC.

The simulation results do not fully agree with the measured MCU data at 90°. The experimental data are taken by turning the test board 90° into the beam. The neutron beam is no longer incident on the surface of the device, but on the edge of the test board. It is unclear what, if any, impact this might have on the probability of MCU, but modeling does not accurately predict the data at this angle. More investigation of this is needed.

Ground Level Neutron Response

The ground level neutron flux spectrum from Fig. 6 was used to simulate the SRAM described in Ch. IV. The previously discussed calibration of these data

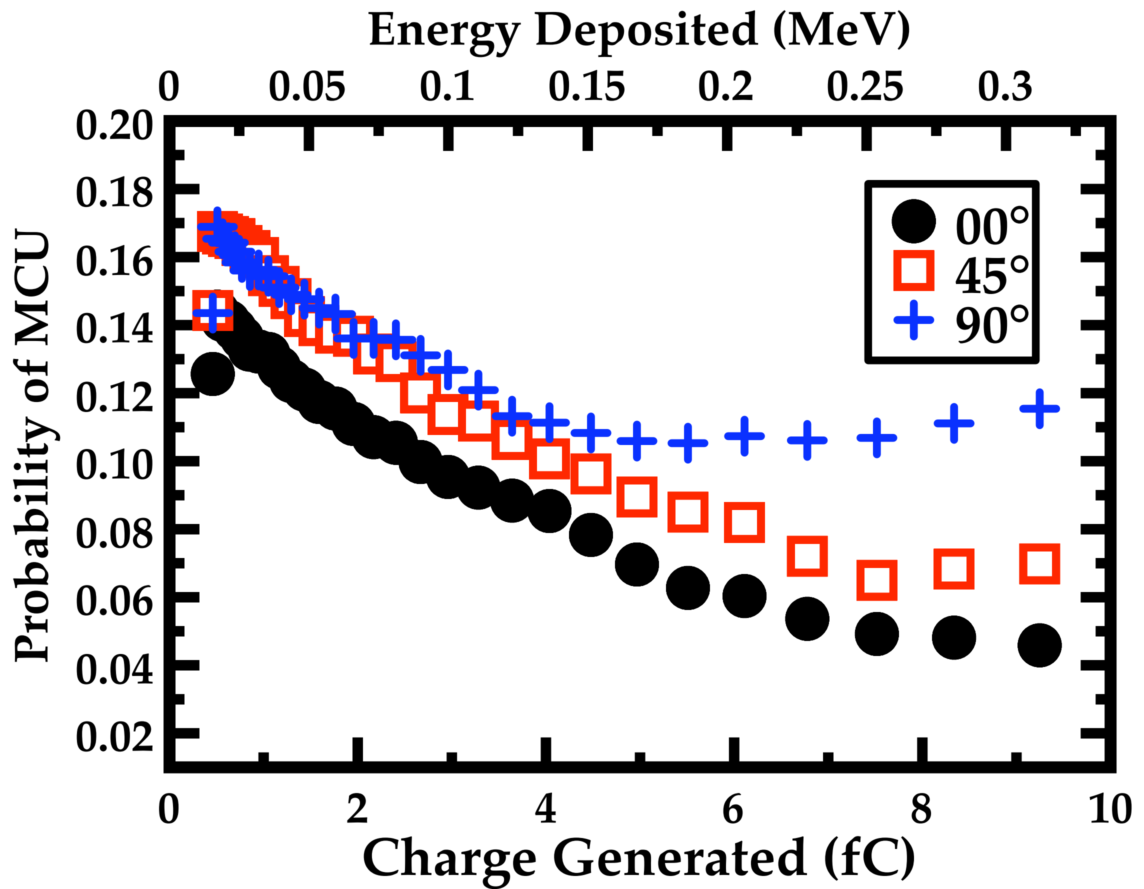


Figure 32: The MRED simulated probability of MCU versus charge generated shows a dependence on the orientation of the device. The probability increases at grazing angles because the secondary products tend to scatter in the forward direction.

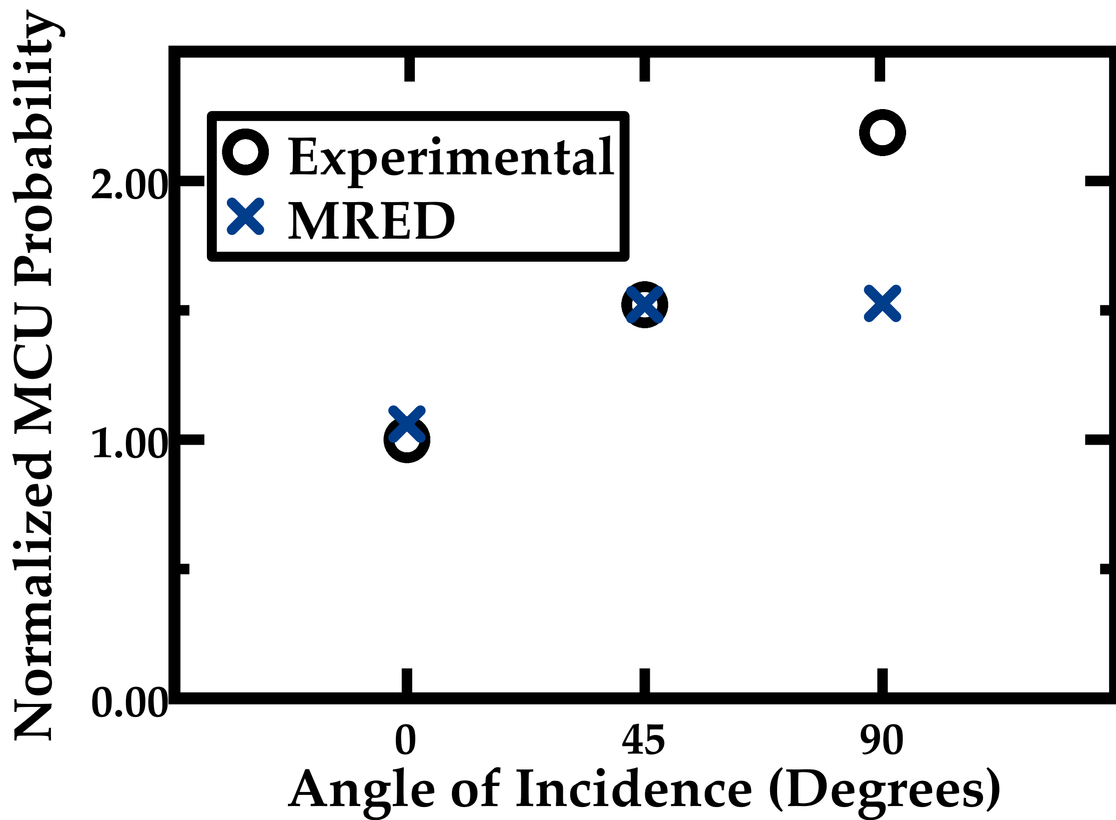


Figure 33: The probability of MCU simulated by MRED is compared with experimental data. MRED simulation is in good agreement except at the largest grazing angles where the board obstructs the beam path.

to simulation allows calculation of the error rate corresponding to fully isotropic irradiation in a specific environment. The spectrum has a range of neutrons from meV to GeV. Fig. 34 shows the $\sigma_{i\text{-bit}}$ at sea level for single–cell to four–cell upsets. The failure–in–time (FIT) rate is also plotted for sea level operation of 1 Mbit of memory. The rate represents the number of failures for 10^9 hours of operation at sea level. The neutron–induced FIT rate for sea level operation is computed from the experimental data by

$$\text{Fit Rate} = \frac{\text{Event}_{i-\text{bit}}}{\Phi \times \text{bits}} \times 15 \times 10^9 \tag{14}$$

where $\text{Event}_{i-\text{bit}}$ is the number of i-bit upsets, bits is the total size of the tested SRAM in bits, Φ is the fluence of incident neutrons, 15 represents the integral sea level neutron fluence in one hour, and 10^9 normalizes to one billion hours of operation. An error rate of approximately 400 FIT/Mbit for device operation at ground level is estimated for the cell equivalent to one bit failure every two weeks for a personal computer with one GB of memory, where one byte is equal to eight bits.

The probability of MCU is shown in Fig. 35 for ground level operation. The probability decreases as the Q_{Crit} increases. A probability of approximately 90% is predicted for the cell at ground level.

Geosynchronous Environment

The modeling methodology in Fig. 25 was used to model the TI 65 nm SRAM and experimental data presented in Ch. V. The physical model included the

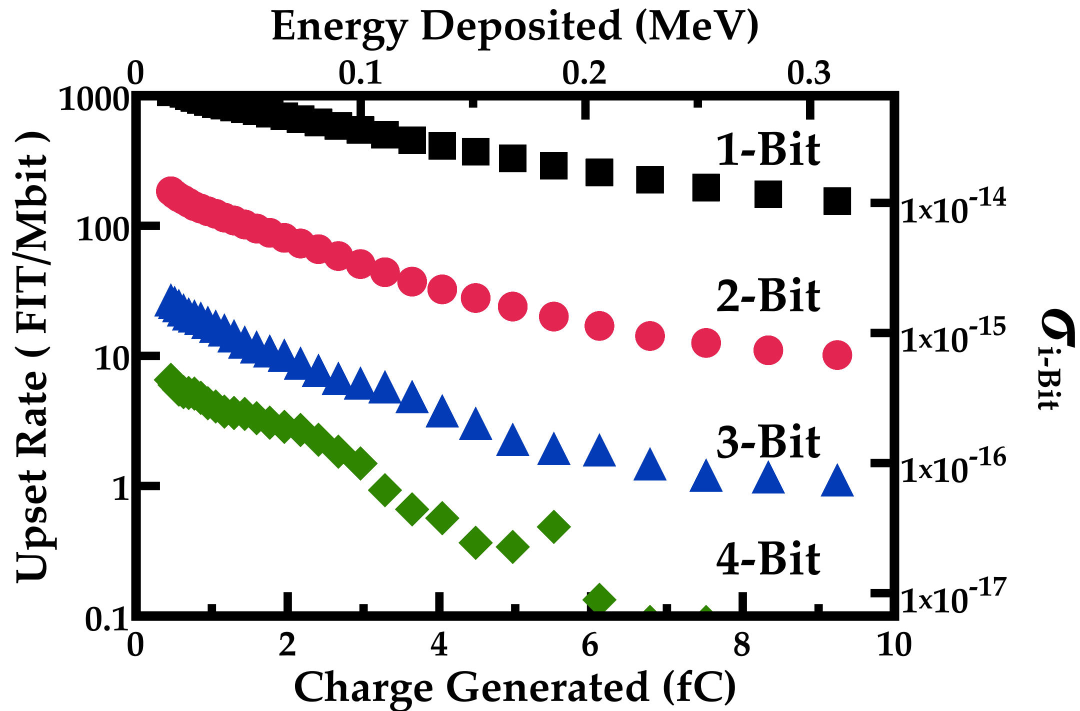


Figure 34: The MRED simulated error rate versus generated charge is shown for single–cell to four–cell upsets for ground level operation. An upset rate of approximately 400 FIT/Mbit is predicted for the cell at ground level.

layout and BEOL characteristics of the process. Two sets of sensitive volumes were used for each cell corresponding to the junctions of the OFF state n–MOSFET and p–MOSFET transistors. The nested volume approach from Fig. 27 was used for each junction and consisted of three RPP volumes.

The charge generation caused by heavy ions was simulated using the same test conditions used in collecting the experimental data in Ch. V. Each event was analyzed to determine the location and spatial distribution of MCU events in the SRAM array. The MRED model was calibrated to the experimental data

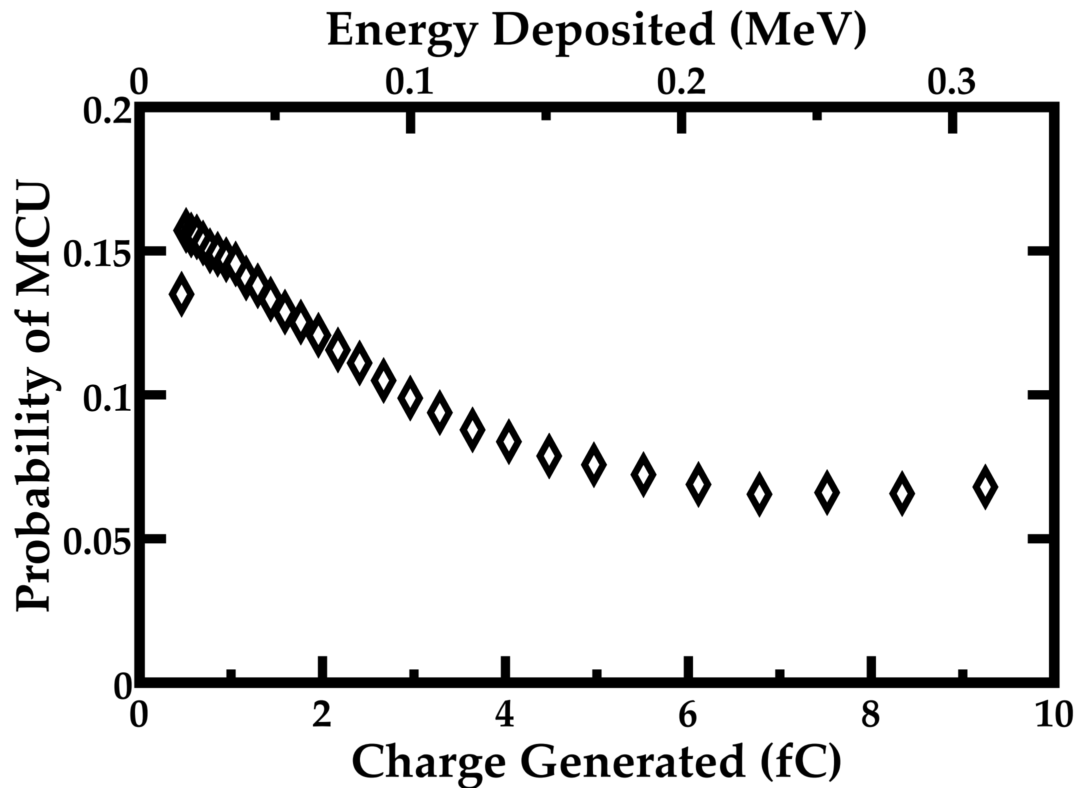


Figure 35: The MRED simulated probability of MCU versus generated charge is shown for ground level operation. A probability of approximately 10% is predicted for the cell at ground level.

by adjusting the location, size, and charge collection efficiency of each collection volume. The simulations were calibrated for all ions at both orientations and all angles of incidence for which experimental data were available. Fig 36 shows the calibration between MRED simulation and the experimental.

The ion spectrum from a space environment (geosynchronous orbit) was simulated. The spectrum, taken from CREME96 and transported through 100 mils of aluminum using the CREME96 TRANS algorithm, includes ions with atomic numbers of 1 to 92. The spectrum was implemented as in [27]. The spectrum is shown in Fig. 37. Each ion spectrum was simulated over a distribution of energies

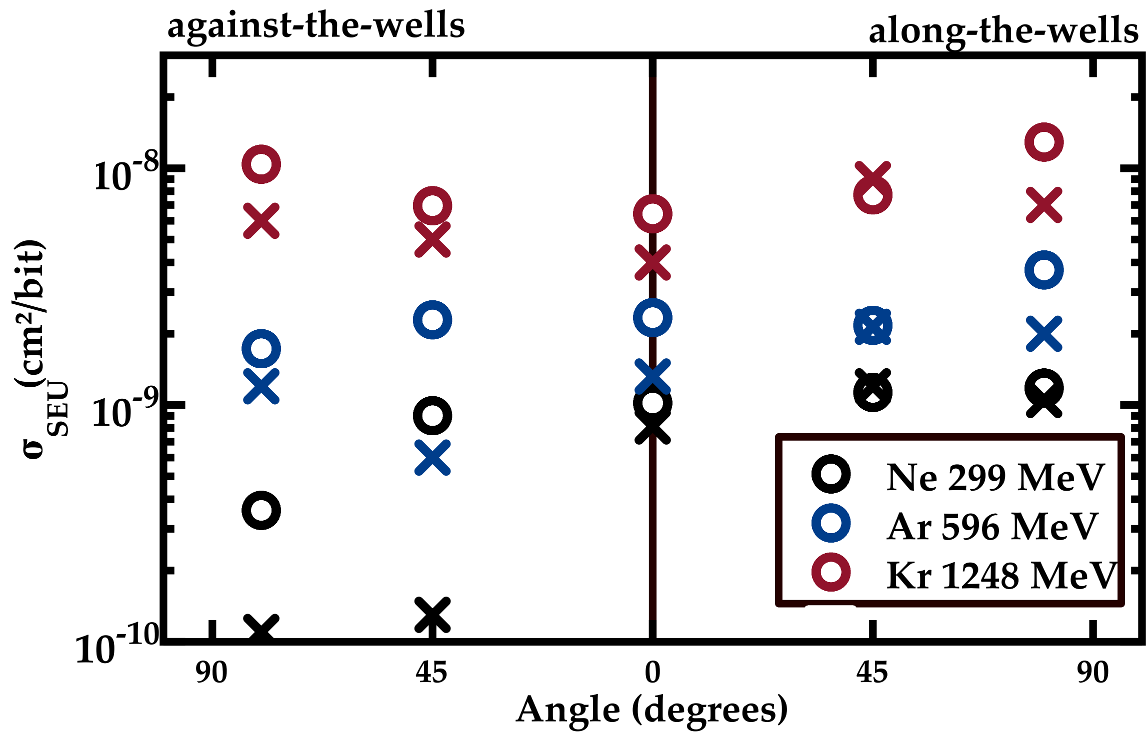


Figure 36: The calibrated MRED response (indicated by the Xs) is compared with experimental data (indicated by the circles).

and the direction of each event randomized to simulate omni–directional irradiation. Each event was analyzed for SEU, SCU, and MCU using the same criteria as the experimental data. Since the simulations are calibrated to the experimental data, but consider all angles, particle types, and energies, they allow extension of the data set to a realistic space environment.

Fig. 38 shows the probability of an MCU event in the GEO environment calculated using Eq. 5. The probabilities are shown for one– and two–column events. Single–cell upsets with dimension 1×1 account for approximately 90%

of all events. Of the remaining events, small dimensions dominate the MCU response. The probability decreases exponentially as the event dimensions grows, with nine–row upsets accounting for one in every 10^5 events. While large events are measured during broad-beam tests, the probability of these large events in this heavy–ion environment is low.

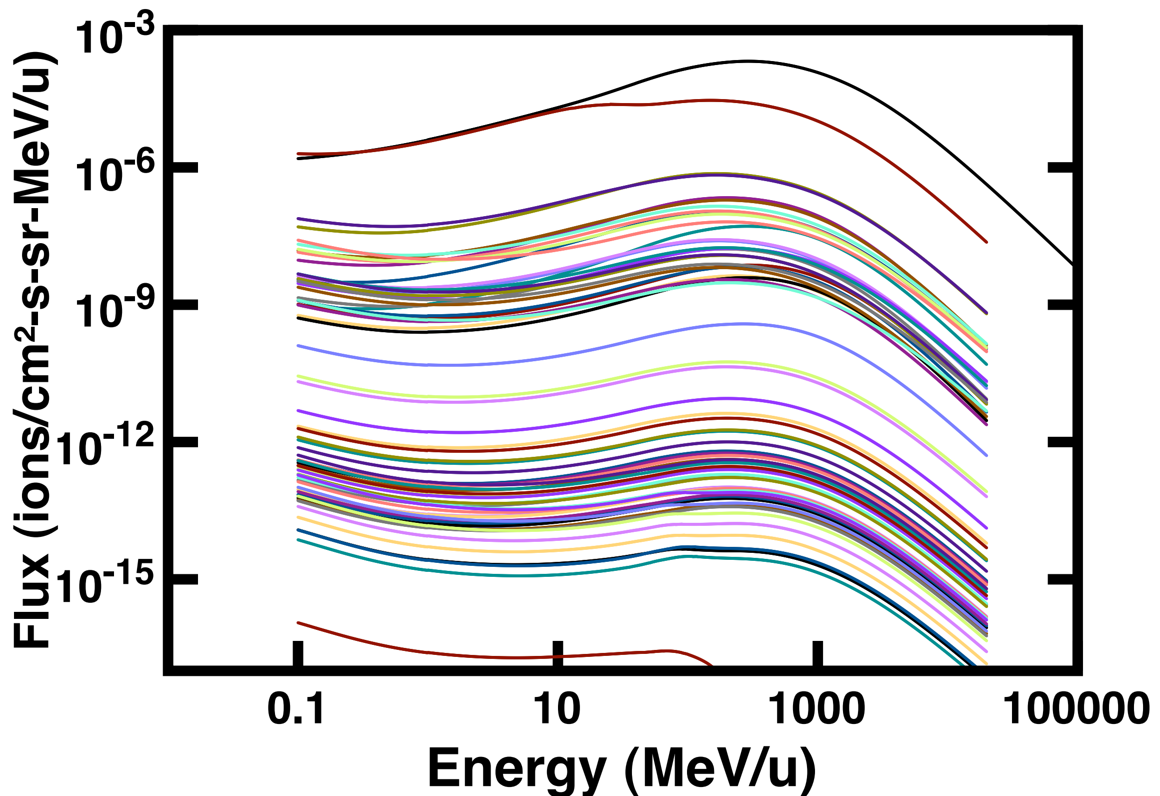


Figure 37: The heavy ion flux spectrum for the GEO environment for ions with atomic numbers 1-92. The spectrum is taken from the CREME96 TRANS algorithm through 100 mils of aluminum.

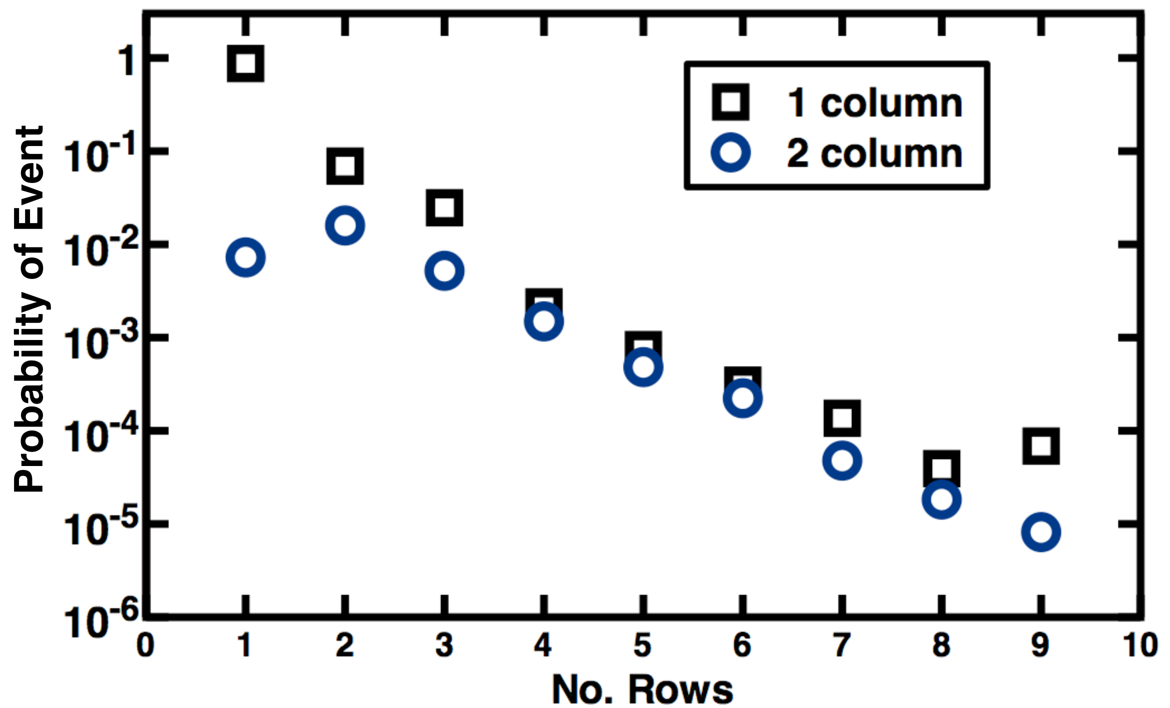


Figure 38: The probability of MCU events for 1 and 2 column events versus the number of affected rows. Approximately 90% of events are SCU, 1×1, events. Small dimension events dominate the MCU response. Events affecting nine rows account for one in every 10^5 event.

Summary

MRED simulation has been calibrated to neutron and heavy ion irradiations using high fidelity physical models of the irradiated SRAM cells. The simulation methodology presented here accounts for the orientation dependences of the experimental data. The neutron environment at ground level exhibits a probability of MCU of approximately 10%. Similarly, the heavy ion spectrum from a geosynchronous orbit produces a radiation response where the probability of MCU events is approximately 10%. The responses in both environments cannot be fully characterized through accelerated testing at a single device orientation because the response is dependent upon the device orientation. Since the MCU probability increases at grazing angles for both neutrons and heavy ions, using only normally incident particles will under predict the MCU probability. For heavy ions, the sizes of MCU events depend on the axis of rotation.

CHAPTER VII

IMPLICATIONS OF MULTIPLE CELLS UPSETS

This chapter is a discussion of the implications of MCU on scaling trends, hardness assurance, and memory design.

Recent Scaling Trends

MCU is commonly evaluated by commercial vendors when characterizing the radiation response of highly–scaled technologies [58, 59, 93–98]. As noted previously, the per bit SER in these technologies remains constant or decreases [11,22]. However, for MCU events the trend is opposite. The plot of Intel's most recent technologies in Fig. 1 demonstrates the increasing probability of MCU as feature sizes shrink [10].

The trend in increasing MCU with smaller feature sizes should be expected to increase in future technologies. MCU has a strong dependence on feature size because higher device densities increase the probability of an MCU event interacting with multiple cells. Fig. 39 demonstrates this trend [10]. The probabilities of MCU for Intel's CMOS processes are plotted for varying MCU cluster sizes (*i.e.*, the maximum distance of affected bits in an MCU cluster). Probabilities exhibit similar dependence on size for the four generations of Intel's process. Because smaller feature sizes produce more closely packed devices, smaller cluster sizes are possible. The ranges of ionizing particles are independent of feature size and

constant for all technologies. Therefore, it should be expected that MCU will increase in future generations with smaller feature sizes.

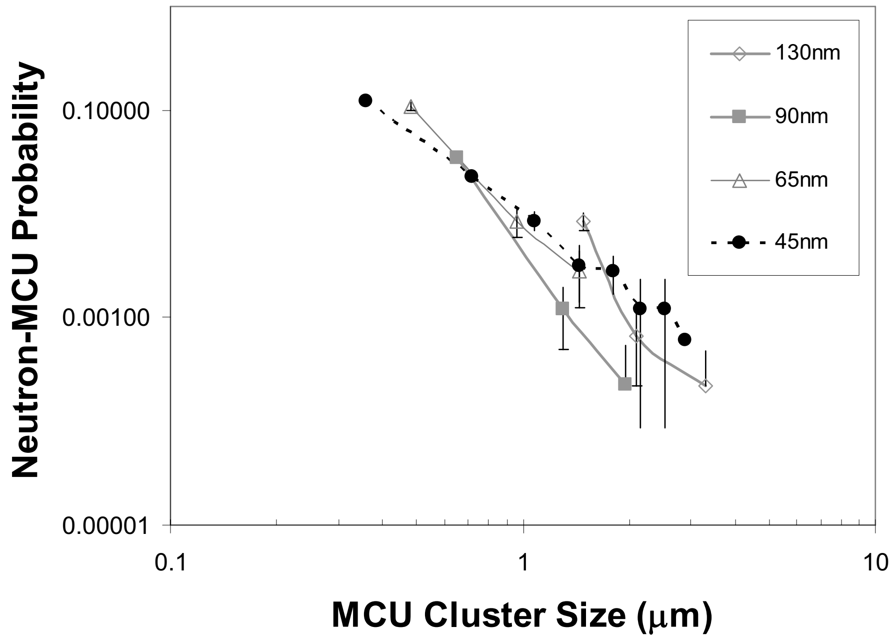


Figure 39: The probability of MCU is shown for four generations of Intel's CMOS process. The MCU cluster size represents the maximum distance in an MCU cluster. The trends in probability for all generations exhibit a similar dependence on the size of the cluster.

Hardness Assurance

MCU hardness assurance of highly–scaled devices, such as the SRAMs presented in this work, presents a major challenge for future CMOS generations. The dependence of the MCU response to the orientation of the device must be considered in accelerated testing. A combination of testing and simulation is an efficient and effective method of predicting SER performance.

Orientation effects

A crucial challenge facing accelerated test methods for hardness assurance are the increasing presence of orientation effects from these tests. The experimental results presented in this work show orientation dependences for both neutrons and heavy ions. Other authors have noted orientation dependences using accelerated testing [79, 80, 99–103]. Fig. 40 compares the total number of SEU upsets and double–bit upsets from 198 MeV protons from 0° to 90° [79]. The device under test was a 16 Mbit NEC DRAM. Similar to the experimental data in this work, SEU shows no dependence on the angle of incidence, but double–bit upsets double at grazing angles. This work demonstrates the importance of examining multiple device orientations.

Testing & Simulation

The heavy ion response reported in Chapter V demonstrates how the MCU response can change with the device orientation. A critical component of hardness assurance is characterizing the worst case radiation response. As was reported, significantly larger MCU events are possible when irradiations are performed by rotation along–the–wells. A similar dependence for heavy ion induced single–event latchup has been reported for the same TI 65 nm process [103]. Test techniques for future CMOS generations should include a robust suite of accelerated testing from multiple device orientations.

As noted previously, simulation has been used extensively to examine radiation responses. Coupling SEE testing and high energy transport simulation extends the fidelity of SER predictions. For thorough hardness assurance evaluation

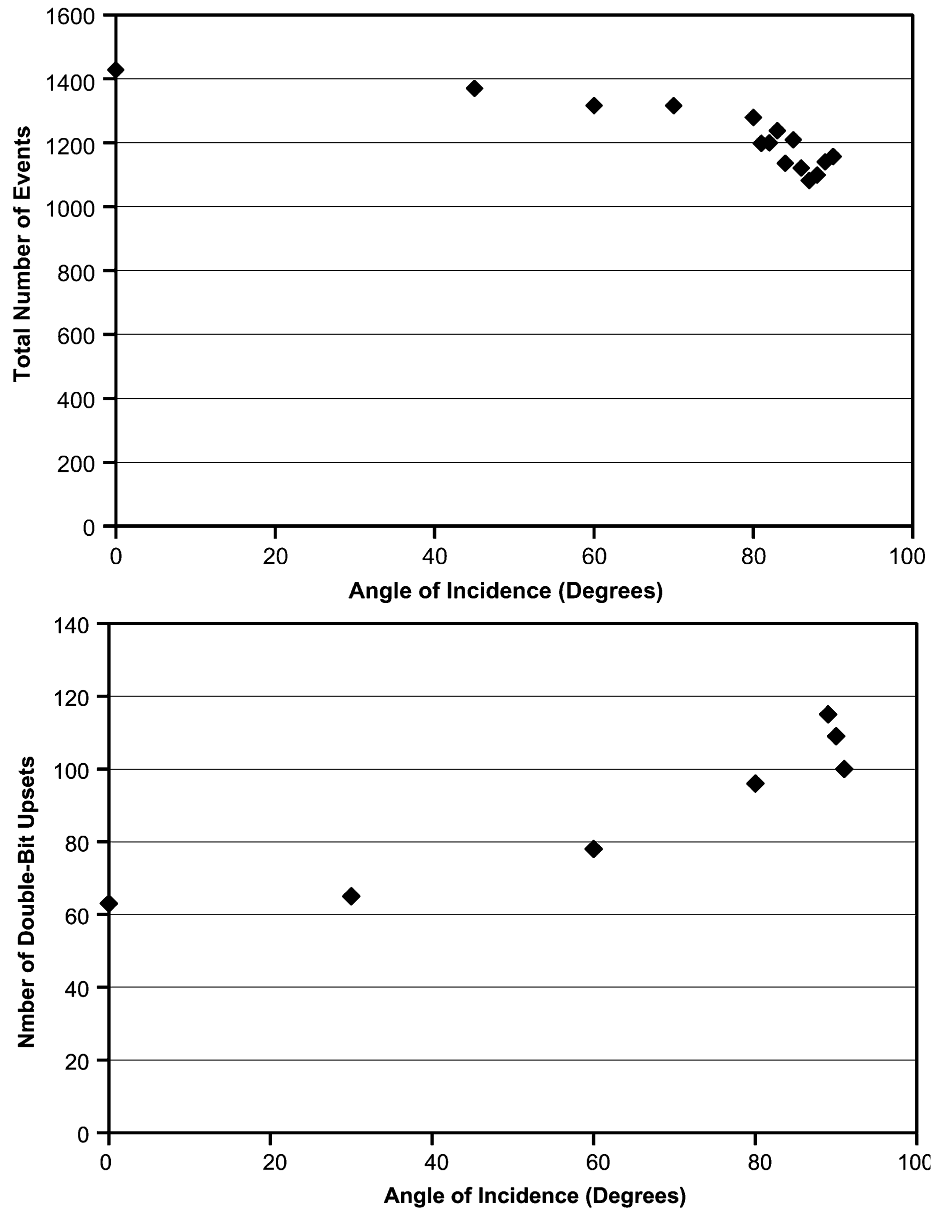


Figure 40: Comparison of total SEUs (top) and total double–bit upsets (bottom) for a 16 Mbit NEC DRAM from 198 MeV protons. The device was rotated to a grazing angle where the number of double–bit upsets doubled.

and accurate SER prediction, it is recommended that energy transport simulation calibrated to a complete set of SEE testing be used to calculate the MCU response.

Memory Design

EDAC is commonly implemented to protect against soft errors, particularly for large server mainframes [20]. These techniques range from simple parity bits to powerful double error correct/triple error detect (DEC–TED) schemes. The most common are single error correct/double error detect (SEC–DED) and single byte correct/double byte detect (SBC–DBD) schemes. Byte correcting codes are useful because they can correct entire memory words rather than single bits. The more powerful (DEC–TED) architectures are not commonly used because of the increased performance penalties, increased latency, and irregular word lengths.

Common to all of these schemes are their inability to correct large numbers of multiple errors. For this reason, bit–interleaving is used. Interleaving spaces individual bits of a byte apart in the memory array. Since the probability of MCU is primarily driven by the bit spacing in highly–scaled technologies, placing bits further apart greatly decreases the probability of unrecoverable errors. Failure to space bits sufficient distances apart has been a noted failure of EDAC for heavy ions. Swift *et al.* noted a predictable number of upsets, but a high rate of uncorrectable errors in the Cassini solid–state recorder [48]. MBUs associated with cells not sufficiently bit–interleaved were identified as the failure. Fig. 41 shows the ratio of uncorrectable EDAC errors to all bit errors versus LET for the memory device from the Cassini recorder. One in three errors were uncorrectable for the highest LET values. Because the probability of MCU increases with LET in the

device, the EDAC scheme was easily overwhelmed with errors. These on–orbit data demonstrate the importance of proper EDAC bit–interleaving schemes.

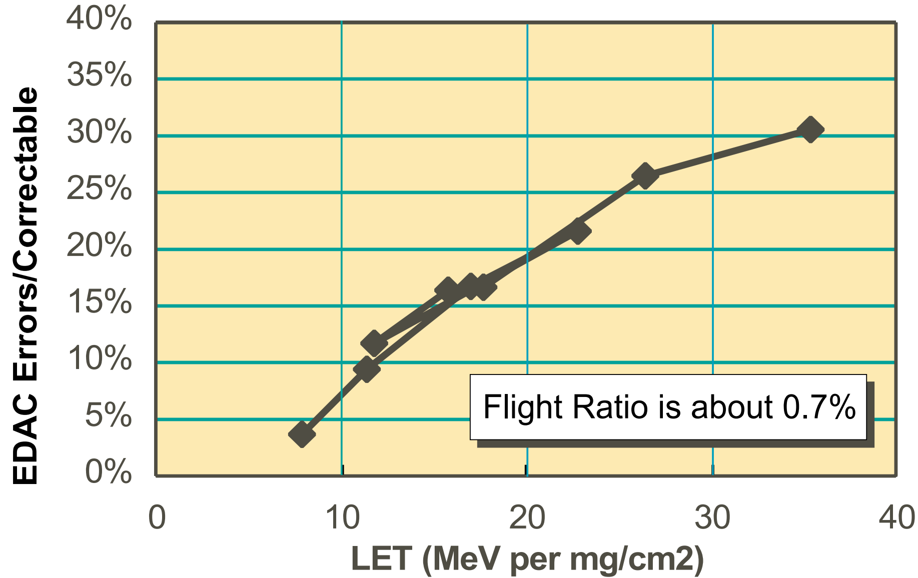


Figure 41: Ratio of uncorrectable EDAC errors to all bit errors versus LET for the Cassini solid–state recorder. Poor bit–interleaving was identified for the high number of uncorrectable errors.

Summary

Recent scaling trends show MCU increasing in future CMOS processes. This trend should be expected to increase because the feature sizes of future process will be small relative to the range of ionizing particles. High packing densities from small feature sizes has also increased the dependence of device orientation in accelerated testing. Hardness assurance test methods should include multiple

device orientations to account for these dependences. A coupled testing and simulation approach is recommend to accurately predict MCU performance. Characterizing devices through thorough testing and simulation are necessary to determine the most effective memory designs to protect against MBU. MCUs have been shown to decrease the effectiveness for on–orbit DRAMs because of insufficient bit–interleaving.

CHAPTER VIII

CONCLUSIONS

In this work the effects of device orientation on the MCU response have been examined. MCUs in SRAMs in highly scaled technologies exhibit a strong dependence on orientation where heavy ions and neutrons incident at large grazing angles have the highest probabilities of producing an MCU event. MCU dimensions of events from heavy ions depend on the orientation of the n– and p– wells of the device.

Since Jack Kilby's patent for the first IC, semiconductor devices have scaled to the nanometer regime. Scaling has produced faster and denser transistors that have enabled the advances in microelectronics since Kilby's invention. Smaller feature sizes produce SRAM arrays that are more susceptible to MCU events. Seifert *et al.* showed the increasing probability of MCU with each new generation of Intel's CMOS processes [10].

This work reports neutron irradiations on 90 nm SRAMs. Neutron irradiations exhibit a device orientation dependence for the MCU radiation response. Neutrons show a probability of MCU that doubles at large grazing angles when compared with normally incident neutrons. Additionally, the size of MCU clusters doubles at those angles as well.

This work also reports heavy ion irradiations on 65 nm SRAMs. Heavy ions also exhibit a device orientation dependence for the MCU radiation response. For heavy ions with low LETs, the σ_{MCU} shows a dependence on orientation because

of low probabilities of MCU. At larger LETs, the high MCU probability (> 80%) yields a σ_{MCU} that is independent of orientation. However, examining the dimension of MCU events reveals qualitatively different MCU events depending on the axis of rotation. Irradiations along–the–wells of the device produce MCU events that affect many rows of the SRAM array while irradiations against–the–wells produce smaller, more clustered events.

The MCU modeling presented in this work incorporates high fidelity physical models of the experimental devices. MRED simulates energy deposition in those structures. Analysis of a terrestrial neutron environment shows the probability of MCU to be approximately 10% for the TI 90 nm technology. Analysis of a GEO environment shows a similar probability of MCU, approximately 10% for the TI 65 nm technology. Larger events, as measured by MCU dimension, exhibit sizes similar to those seen through accelerated testing, but have extremely low probabilities.

Baumann and Seifert showed the decreasing per bit SER starting from 0.5 μm feature sizes [10, 11]. Seifert's evaluation of increasing MCU suggests that the probability of MCU will increase for nucleons in future generations [10]. Neutron irradiations in this work have exhibited probabilities similar to Seifert's findings. Heavy ion irradiations in this work exhibit high probabilities of MCU at all orientations for more highly ionizing ions. Modeling of MCU for both the terrestrial and GEO environments exhibit similar probabilities of MCU. This trend should be expected to continue for future processes because smaller device dimensions

increase the probability of a radiation event interacting with multiple devices. Because future CMOS processes will rely on downscaling to improve performance, increased MCU effects are certain.

The impact of device orientation on the MCU radiation response has been examined. SRAMs from state–of–the–art technologies exhibit a strong dependence on the orientation of the device with respect to the incident particle. The evaluation of the MCU response in these technologies must account for the MCU response dependence on orientation. Conventional test techniques should incorporate these dependencies. Testing methodologies must include irradiations at multiple orientations of the device. Monte–Carlo simulations are a useful tool in the evaluation of both SEU and MCU in new technologies because they account for different device responses at multiple orientations.

Hierarchical memory design techniques should account for these dependences. Bit interleaving of SRAM cells is important for the performance of error correction schemes employed in memory designs. These designs should incorporate minimum spacings for the largest MCU events.

APPENDIX A

HEAVY ION DIMENSION PLOTS

This appendix includes histograms of the dimensions of MCU events for all device orientation presented in Chapter V.

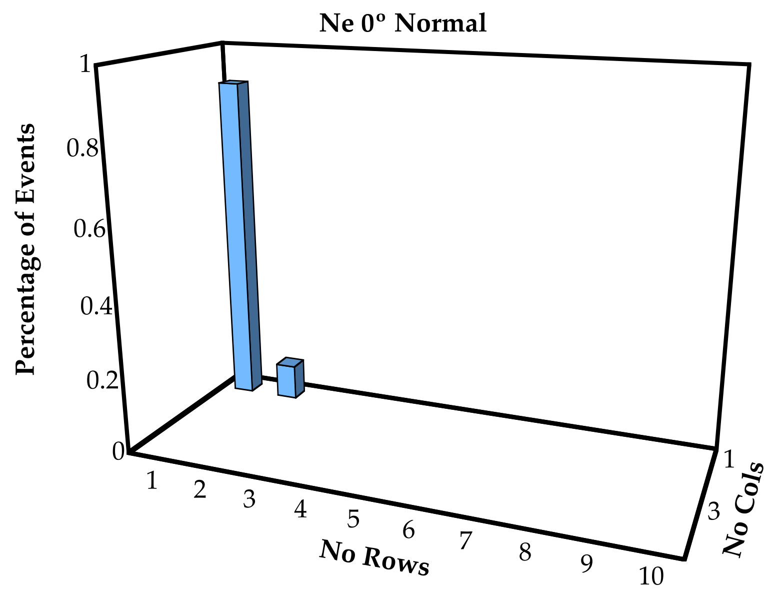
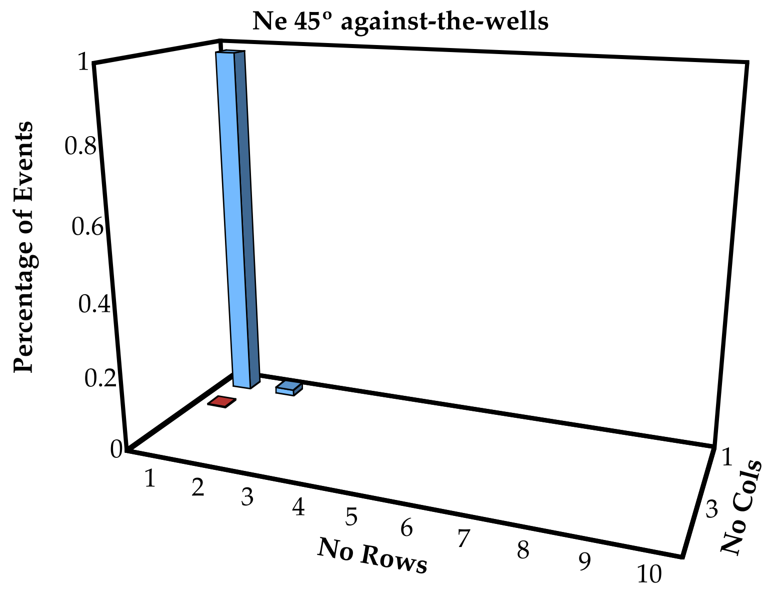


Figure 42: Ne ions incident at 0°.



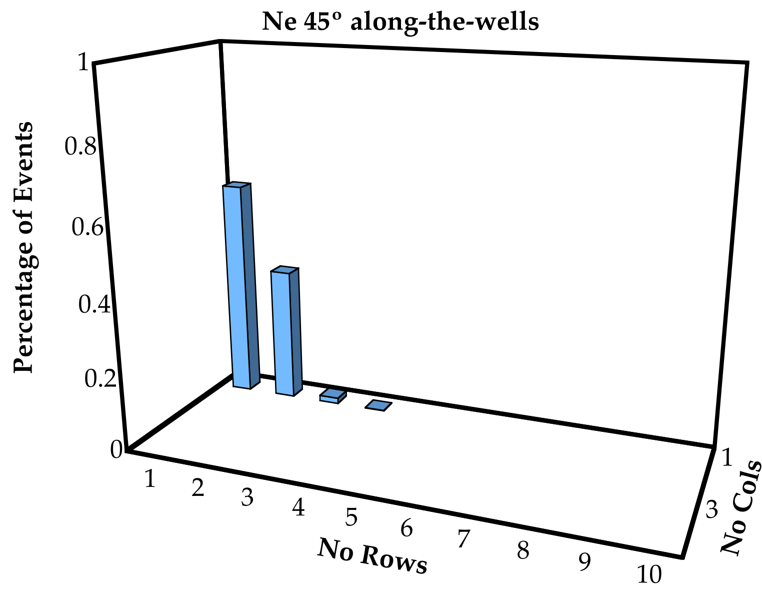
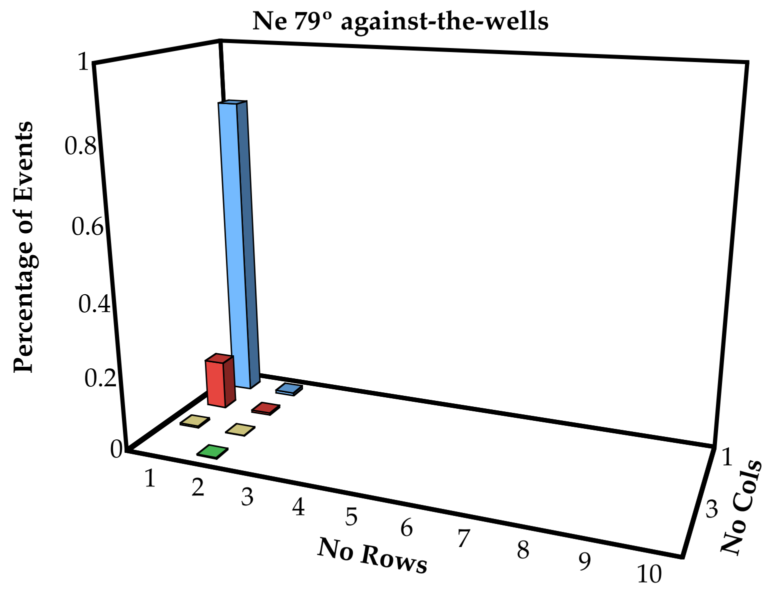


Figure 43: Ne ions incident at 45°.



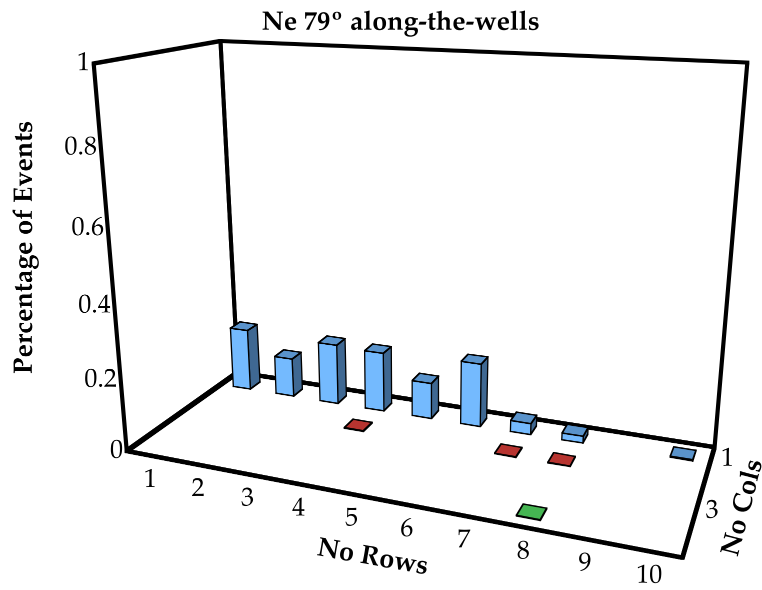


Figure 44: Ne ions incident at 79°.

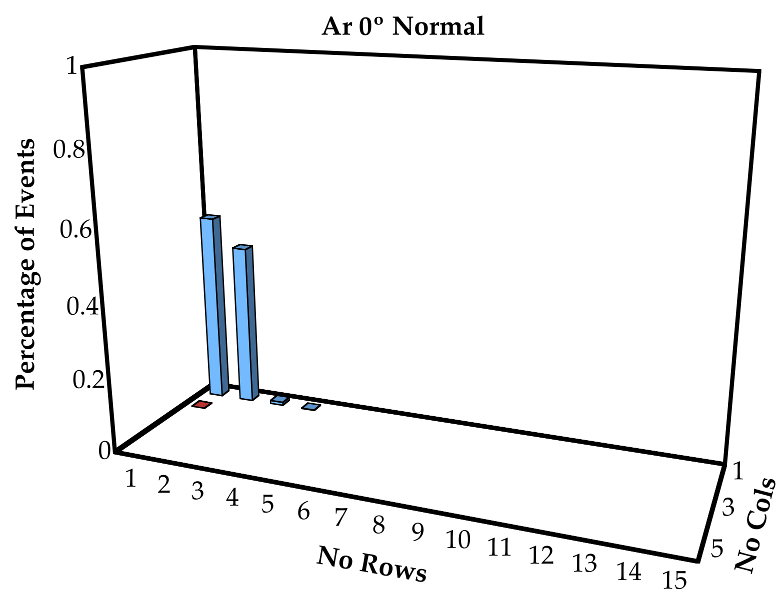
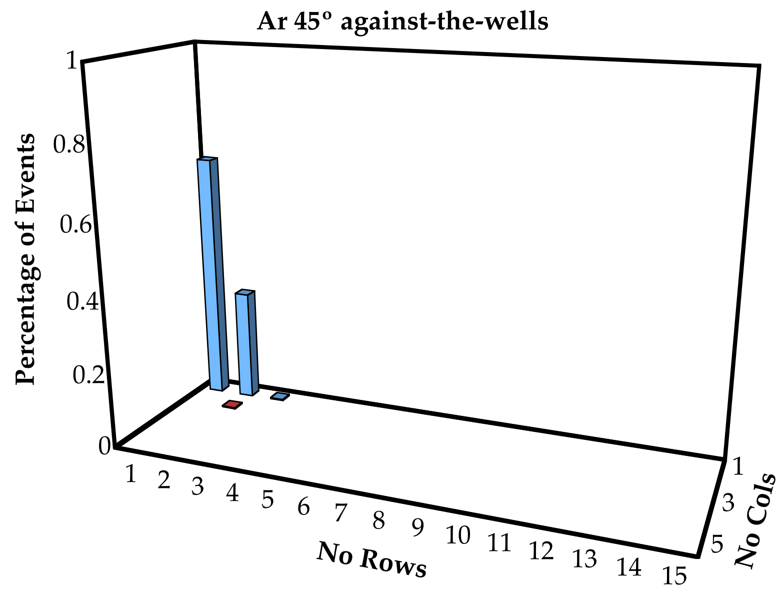


Figure 45: Ar ions incident at 0°.



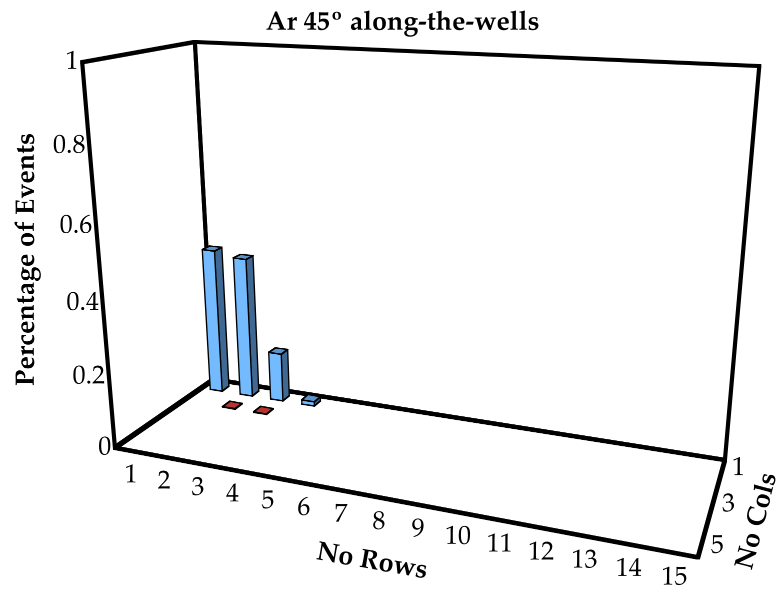
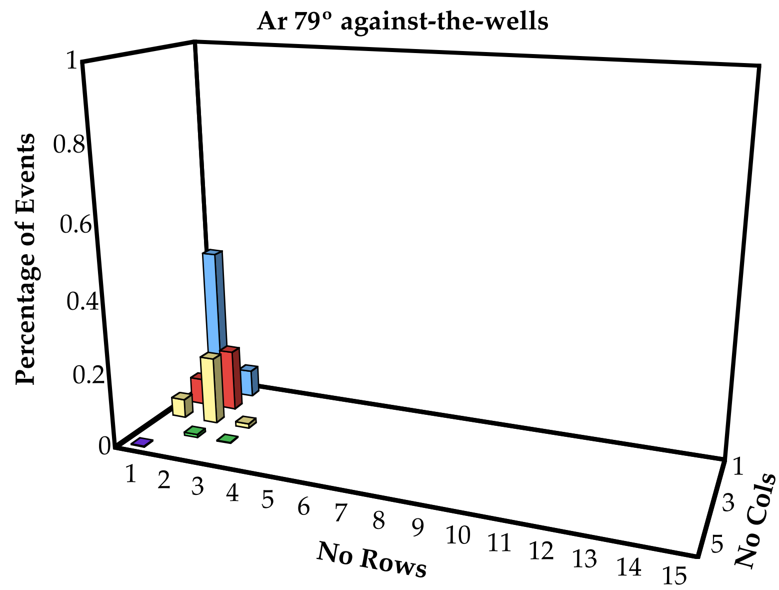


Figure 46: Ar ions incident at 45°.



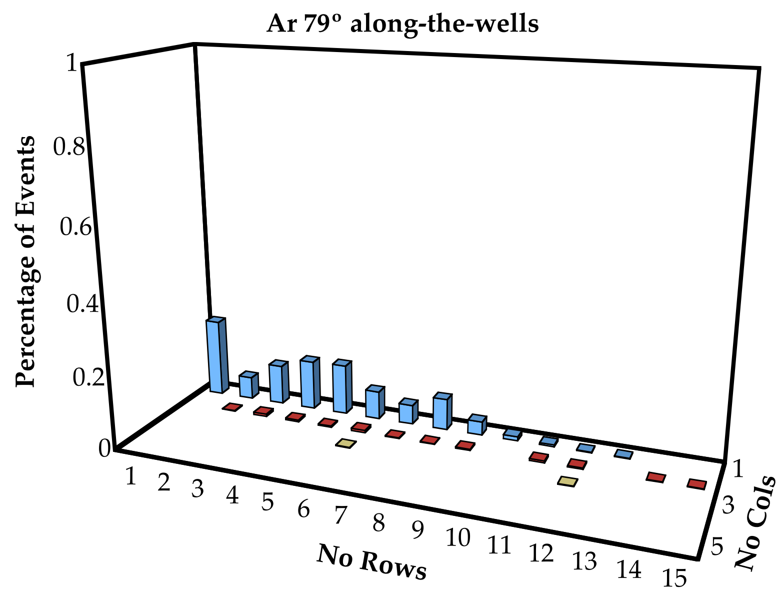


Figure 47: Ar ions incident at 79°.

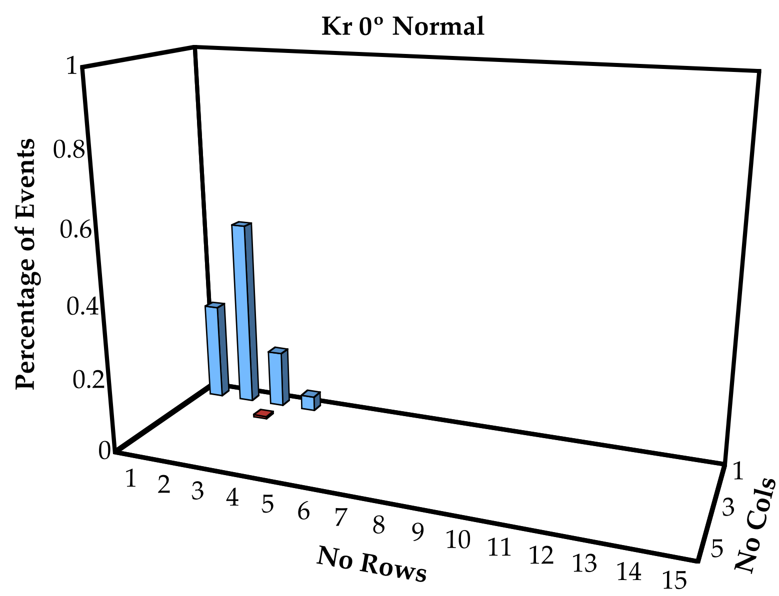
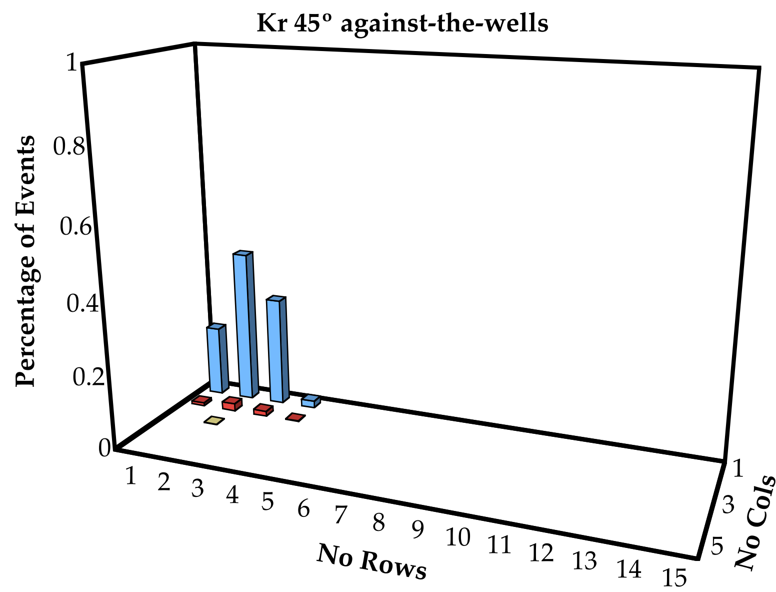


Figure 48: Kr ions incident at 0°.



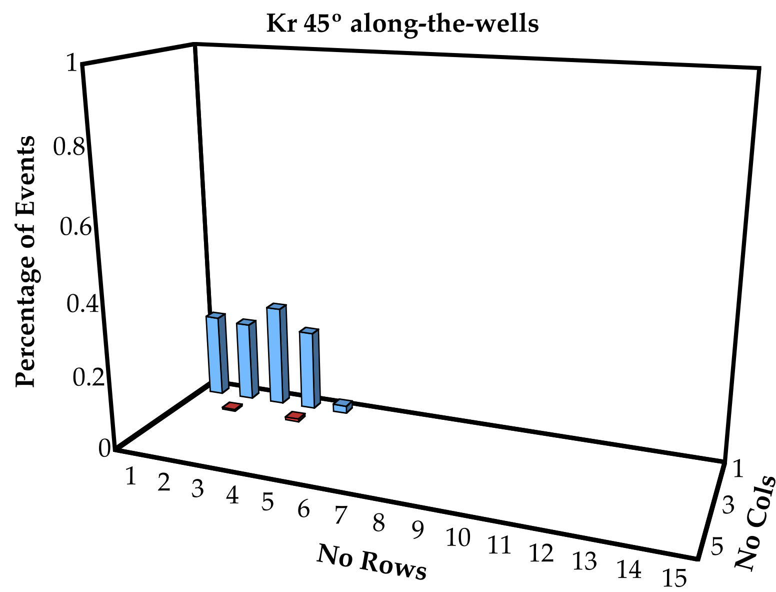
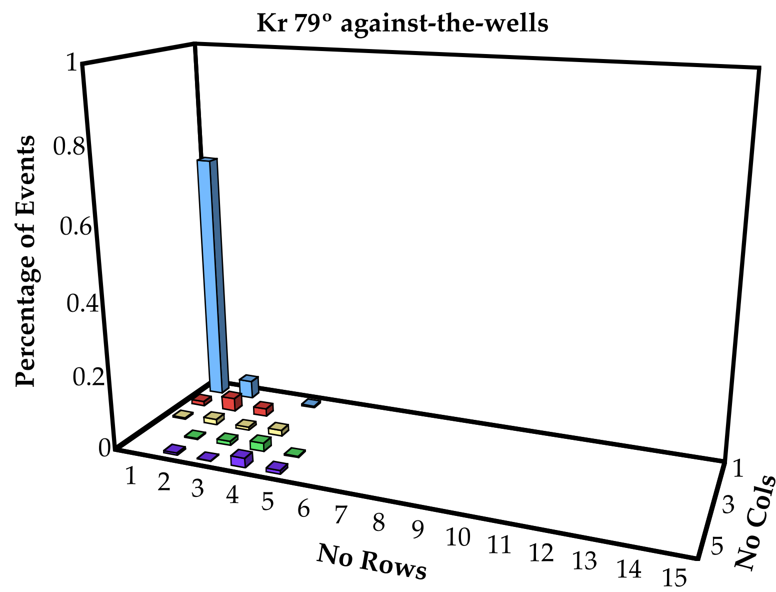


Figure 49: Kr ions incident at 45°.



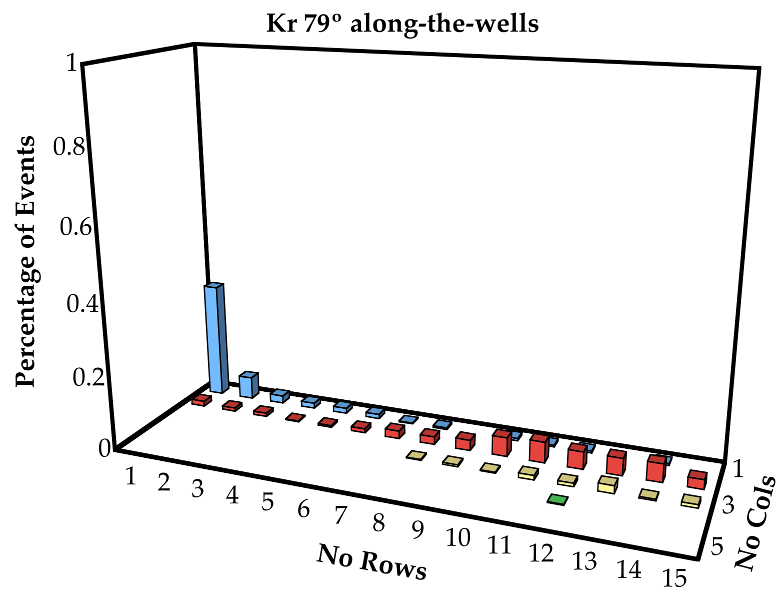


Figure 50: Kr ions incident at 79°.

APPENDIX B

MRED CODE

```
#!/usr/bin/python
import os, sys, cPickle, base64, time, numpy


importVars=eval(sys.argv.pop(-1))
print importVars


execfile('run_mred.py')


#Physic Setup
G4Core.ExecuteCommand('/control/verbose 0')
G4Core.ExecuteCommand('/run/verbose 0')
mred8.physics.addModule('StandardScreened')
mred8.physics.addModule('HadronElastic')
mred8.physics.addModule('HadronInelastic')
mred8.physics.addModule('PiKInelastic')
mred8.physics.addModule('NucleonInelasticA')
mred8.physics.addModule('AltIonInelastic')
mred8.physics.list.SetBiasPrimaryOnly(True)
mred8.physics.list.SetSigmaBiasFactor(200.)
```

```
mred8.physics.list.SetUseTrackWeighting(True)

print mred8.physics.list.GetSigmaBiasInfo()

mred8.physics.range_cuts = 50*micrometer


# This sets up a tcad structure named final_msh.grd

# this imports the TI 65 nm grd file

mred8.setDevice('tcad')

mred8.material.enableBasicElectronicMaterials()

mred8.device.structure_file_name='inputFiles/structure/grd/TI65nmCell.grd'

mred8.device_replicas=(17,37,1)

print mred8.device_replicas


mred8.init()


#The section on Section on the sensitive volume description

#has been omitted as the information is proprietary.


#Gun Setup

# This sets up the gun for the heavy ions used at the TAMU testing in Dec. 2007

# Ne = 182.18 +/- 0.42 MeV

# Ar = 325.19 +/- 0.97 MeV

# Kr = 569.97 +/- 2.63 MeV


mred8.hdf5.include_energies=False
```

```
mred8.hdf5.include_tracks=False

mred8.hdf5.include_hits=False

mred8.hdf5.include_histograms=False

mred8.hdf5.include_seeds=False

mred8.hdf5.write_output_files=False


mred8.gun.setDefaults()


def setGun(ionType,xIonAngle,yIonAngle, beamE):

if ionType == 'Ne':

mred8.gun.setParticle('ion', 10, 20)

elif ionType == 'Ar':

mred8.gun.setParticle('ion', 18, 22)

elif ionType == 'Kr':

mred8.gun.setParticle('ion', 36, 48)

mred8.gun.energy=beamE

if xIonAngle==0:

xDir=0

elif xIonAngle==45:

xDir=1

elif xIonAngle==78:

xDir=4.7

if yIonAngle==0:

        yDir=0
```

```
elif yIonAngle==45:
        yDir=1
elif yIonAngle==78:
        yDir=4.7
mred8.gun.direction = vector3d(xDir, yDir, 1)
print 'Gun direction is ', mred8.gun.direction
print 'Gun position is ', mred8.gun.position
print 'Gun ion is ', mred8.gun.particle.name()
print 'Gun energy is ', mred8.gun.energy


setGun(importVars['ionType'],importVars['xIonAngle'],
importVars['yIonAngle'], importVars['beamE'])
mred8.gun.random_flux=True
mred8.gun.random_hemisphere=False
mred8.gun.random_isotropic=False


if os.path.exists('hdf5_output/'+importVars['runName']):
print 'Output directory exists!'
else:
os.mkdir('hdf5_output/'+importVars['runName'])
print 'Output directory CREATED!'


print mred8.gun.fluence_unit
```

```
mred8.progress_interval=importVars['nIons']/10

nmosBin=#***#
pmosBin=#***#

bitUpsets=numpy.zeros(50)
(histogram, xBins, yBins)=
numpy.histogram2d([0],[0], bins=(49, 49), range=([1,50], [1,50]), normed=False)

centers=
mred8.runAct.GetNewHistogram('myHistogram', 100*eV, 100*MeV, 600, True).x()

numbits=svCounter/8

coordsTemp=[]
xcount=0
ycount=0

for x in xCenters:
for y in yCenters:
coordsTemp.append([xcount,1,ycount,1])
coordsTemp.append([xcount,1,ycount,0])
coordsTemp.append([xcount,0,ycount,0])
coordsTemp.append([xcount,0,ycount,1])
```

```
ycount += 1
xcount+=1

coords=[]
for x in coordsTemp:
coords.append([x[0]*2+x[1],x[2]*2+x[3]])

del(coordsTemp)

def getEnergyDepositions():
energies=numpy.array([x.energy for x in sd.sv_vector])
energies.shape=(len(energies)/numbits,numbits)
energiesX=energies[0]+(2/3.)*(energies[1])+(1/6.)*
(energies[2]-energies[1])+(0.075)*(energies[3]-energies[2])
energiesY=energies[4]+(2/3.)*(energies[5])+(1/6.)*
(energies[6]-energies[5])+(0.075)*(energies[7]-energies[6])
return (energiesX, energiesY)

def getUpsetCoords(energiesX, energiesY):
global coords
upsetCoords=[]
for x in range(numbits):
if energiesX[x] > centers[nmosBin]:
upsetCoords.append(coords[x])
```

```
elif energiesY[x] > centers[pmosBin]:
upsetCoords.append(coords[x])
return upsetCoords


def findClusterSizes(upsetCoords):
allClusters=[]
while upsetCoords != []:
cluster=[]
cluster.append(upsetCoords[0])
upsetCoords.remove(cluster[0])
for x in cluster:
distance=[]
for y in upsetCoords:
distance.append(((x[1]-y[1])**2+(x[0]-y[0])**2)**0.5)
datarange=range(len(distance))
datarange.reverse()
for y in datarange:
if distance[y] < 1.5:
cluster.append(upsetCoords[y])
upsetCoords.remove(upsetCoords[y])
allClusters.append(cluster)
return allClusters


def histogramClusters(allClusters, eventWeight):
```

```
global bitUpsets, histogram
xDim=[]
yDim=[]
for x in allClusters:
bitUpsets[len(x)]+=eventWeight
xDim.append(max([y[0] for y in x])-min([y[0] for y in x])+1)
yDim.append(max([y[1] for y in x])-min([y[1] for y in x])+1)
histogram+=numpy.histogram2d(xDim,yDim, bins=(49, 49), range=([1,50], [1,50]),
normed=False, weights=[eventWeight for x in xDim])[0]

def validEvent(evt):
global histogram
eventWeight=evt.eventWeight
(energiesX, energiesY)=getEnergyDepositions()
upsetCoords=getUpsetCoords(energiesX, energiesY)
if upsetCoords==[]:
return
allClusters=findClusterSizes(upsetCoords)
histogramClusters(allClusters, eventWeight)
return

def outputData():
stats={'totalTime': totalTime, 'nIon': importVars['nIons'],
'rate':(importVars['nIons']/totalTime)}
```

```
print stats

output=[histogram, bitUpsets, stats]

f=open(str('hdf5_output/'+importVars['runName']+'/'+importVars['runName']+

importVars['isotime']+'.'+"%03d"%(importVars['index'])+'.pick'),'wb')

cPickle.dump(output,f,-1)

f.close()


startTime=time.time()

mred8.runSingleEventMode(importVars['nIons'], validEvent)

endTime=time.time()

totalTime=endTime-startTime


outputData()
```

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