AGING AND IRRADIATION RESPONSE OF 1/F NOISE IN METAL OXIDE

SEMICONDUCTOR DEVICES

By

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CHAPTER 1

INTRODUCTION

The field of radiation effects in microelectronics is an active area of research today, especially for space and defense applications, as technologies are continually becoming more and more advanced. Consequently, hardness assurance and reliability testing have become central and critical issues for electronics operating in radiation-harsh environments, and, as a result, a vast amount of resources has been invested in testing and qualifying parts for these environments. The most effective way to test parts for hardness and reliability is to subject them to the conditions they would encounter during their deployment, namely, by exposing them to ionizing radiation. While significant insight can be gained about device performance, these tests are typically destructive, and therefore the devices cannot be used afterwards. Furthermore, devices that are tested form a limited sample (and consequently a limited representation) of a specific lot, which introduces a degree of uncertainty, since device responses from these tests may or may not differ from responses of the actual fielded devices. As a result, much effort has been exerted in finding nondestructive, reliable tests for radiation hardness in microelectronics.

Over the last 20 years, $1/f$ noise measurements have emerged as a potentially insightful and nondestructive test for radiation hardness and reliability in MOS devices [1]-[5]. Work has been done that links characteristics of MOS $1/f$ noise with characteristics of the device radiation response. Further studies have shown the significance of bias and temperature conditions during irradiation and annealing on MOS

1/f noise and radiation response [2], [3], particularly the differences observed between n-channel and p-channel devices.

Previous work has shown that MOS radiation response can change with aging, and strongly suggests that moisture is a primary agent in the aging process [6], [7]. This can have a significant impact on the reliability and radiation hardness of devices employed for long periods of time or used after long-term storage in non-hermetic environments. Further studies have shown that moisture exposure can seriously degrade the 1/f noise and radiation response of both nMOS and pMOS transistors, with the effects on pMOS transistors more enhanced, suggesting differences in the mechanisms of the moisture absorption process between nMOS and pMOS devices [8]-[10].

In recent years, alternative-channel materials have been explored as a viable option to replace silicon, in an effort to overcome the issues inherent in downscaling. Due to its high electron and hole mobility, and relatively simple integration with standard silicon processes, germanium is emerging as a promising material for future CMOS technologies [11], [12]. One of the critical issues surrounding Ge MOS systems is control of the Ge/gate dielectric interface [11], [13]. In previous work, both charge pumping and 1/f noise measurements were used to evaluate the near-interfacial defects in Ge pMOSFETs [14]-[21]; however, the nature of these defects, particularly those related to the noise, is not well understood. Therefore, characterizing this interface is of great importance, particularly in evaluating performance and understanding the reliability issues inherent in Ge-channel devices related to radiation-induced degradation.

This research effort focuses on characterizing MOS device radiation response and reliability, primarily through investigating the defects that lie at or near the

semiconductor-oxide interface. The first part of this work explores the effects of aging, moisture exposure at elevated temperature, and total dose irradiation on the $1/f$ noise in silicon MOS transistors, primarily focusing on the gate-voltage and temperature dependence of the noise. The gate-voltage dependence of the noise is studied in detail for both nMOS and pMOS devices throughout these experiments. Results show that moisture exposure has a more significant impact on pMOS noise than for nMOS devices; furthermore, analysis of the $1/f$ noise gate-voltage dependence indicates that changes in the defect energy distributions are responsible for the observed gate-voltage dependences for both nMOS and pMOS devices, indicating that carrier-number fluctuation dominate the noise process for these devices. Changes in the temperature dependence of the noise were observed after irradiation, and reflect the changes in the gate-voltage dependence of the noise. Additionally, charge pumping measurements were used to characterize the interface trap density as a function of energy, before and after irradiation, in an effort to gain additional insight into the interface trap distributions and their relationship to the border traps responsible for the noise; the results of these measurements were consistent with those obtained through $1/f$ noise measurements.

The second part of this work focuses on the characterization of germanium pMOS transistors before and after irradiation. For these devices, processing has a strong impact on the radiation-induced trap charge buildup, evident from $1/f$ noise and charge pumping measurements performed through irradiation and annealing. Results show that the defects contributing to the noise are different from those contributing to the charge pumping current, and suggest that the noise is most likely dominated by traps located in the gate dielectric layer. Furthermore, noise measurements show that the border trap density

increases significantly toward the Ge valence band edge, while three-level charge pumping reveals an interface trap density that increases slightly toward midgap.

This thesis is organized as follows: Chapter 2 discusses the basic mechanisms of $1/f$ noise in MOSFET transistors and the models used in this study, and provides an overview of radiation effects, and aging and moisture effects in MOS devices. Chapter 3 describes the devices used in this work, the $1/f$ noise measurement setup and the charge pumping techniques used to characterize these devices. Chapter 4 focuses on the $1/f$ noise gate-voltage dependence of Si nMOS and pMOS transistors as a function of total dose irradiation, and the effects of aging and moisture exposure on each. Experimental results on the temperature dependence of the noise are also presented and discussed for moisture-exposed and control (non-exposed) pMOS transistors. Chapter 5 describes the results of the charge pumping measurements for these moisture-exposed and control pMOS devices, before and after irradiation. In Chapter 6, the Ge pMOS devices are presented, and results from $1/f$ noise measurements, *I-V* curves, and charge pumping measurements are shown. Chapter 7 provides the summary and conclusions of this work.

CHAPTER 2

BACKGROUND

This chapter contains background information about low frequency noise in MOS devices, radiation effects, and aging and reliability issues. The models that are used in analyzing the 1/f noise results of the MOSFET devices in this study are described. Effects of total dose radiation exposure on MOS devices are then recounted, followed by a discussion of the effects of aging and moisture exposure on MOS reliability.

Low Frequency Noise in MOS Devices

Many physical systems exhibit fluctuations with spectral densities that vary approximately as 1/f over a large range of frequencies. The 1/f-like fluctuations in metals and semiconducting materials are particularly interesting, due to the information they can reveal about the physical structures of these systems and the physical processes involved in the 1/f noise that is characteristic of each system.

A variety of models have been used to explain the 1/f noise in MOSFET devices [22]-[36]. It has been generally accepted that the 1/f noise in the conduction channel of the device is primarily associated with the capture and emission of charge carriers from trap sites in the oxide, at or near the Si/SiO$_2$ interface. Fluctuations in the oxide-trap charge couple to the channel, both directly through fluctuations in the inversion layer charge density, and indirectly through fluctuations in scattering associated with fluctuations in trap occupancy. These fluctuations in inversion charge are referred to as carrier-number fluctuations. At variance with this mechanism, carrier-mobility

fluctuations are described as fluctuations in carrier mobility due to phonon scattering. In general, studies tend to show that n-channel MOSFET noise is primarily dominated by number fluctuations, while p-channel noise is frequently interpreted to be due both to number and mobility fluctuations. The most widely accepted models for describing the two different mechanisms attributed to MOS $1/f$ noise are based on models originally proposed by McWhorter [23]-[30], and Hooge [31], [32]. Others have developed models to account for the tunneling mechanism and charge trapping responsible for $1/f$ noise in MOS devices [4], [23], including carrier-number fluctuation models that account for mobility fluctuations caused by carrier trapping [33]-[36]. In this thesis, we will use a model that describes MOS $1/f$ noise primarily due to number fluctuations, assuming that any scattering due to trapped carriers produces a less significant fluctuation in mobility.
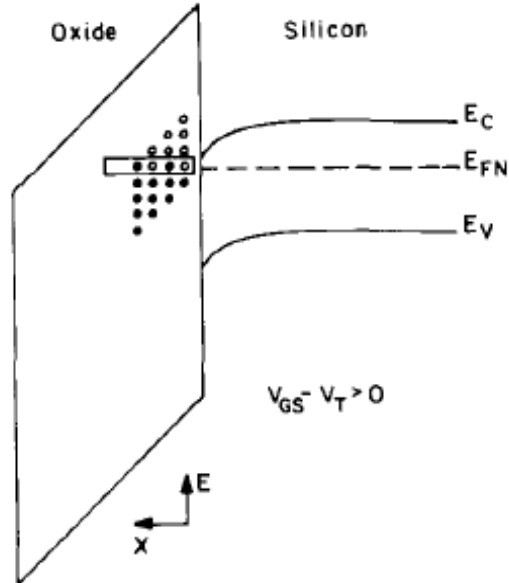
Figure 1: Schematic representation of the energy and space window accessed by a typical 1/f noise measurement for an nMOS transistor biased into strong inversion, after [36].

In the number fluctuation model, the oxide traps that exchange charge with the device channel are assumed to exist uniformly in space (throughout the oxide) and in energy (in the silicon band gap), as illustrated schematically in Figure 1 [36].

Charge carriers tunnel directly into and out of these traps. The power spectral density of fluctuations in the total number of trapped charges N_t is given by

$$S_{N_t}(f,T) = \frac{k_B T D_t(E_f)}{LW ln(\tau_1/\tau_0)} \frac{1}{f}, \tag{2.1}$$

where $D_t(E_f)$ is the oxide trap density at the Fermi level E_f, L and W are the device channel length and width, respectively, and τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [4]. Thus, the noise magnitude is determined by the density of traps near the Fermi level, which depends on T, at a distance from the interface that depends on f. For a MOS transistor operated in strong inversion, the fluctuations in trapped charge result in a fluctuation in the effective gate voltage, and under constant drain current conditions, causes a fluctuation in the drain voltage, given by

$$S_V(f,T,V_D,V_G) = \frac{q^2}{C_{ox}^2} \frac{V_D^2}{(V_G - V_T)^2} S_{N_t}(f,T)$$

$$= \frac{q^2}{C_{ox}^2} \frac{V_D^2}{(V_G - V_T)^2} \frac{k_B T D_t(E_f)}{LW ln(\tau_1/\tau_0)} \frac{1}{f}, \tag{2.2}$$

where C_{ox} is the gate oxide capacitance, V_D and V_G are the drain voltage and gate voltage, respectively, and V_T is the threshold voltage of the device [4]. For a fixed drain voltage, S_V is proportional to $(V_G - V_T)^{-2}$. Any non-uniformity in $D_t(E_f)$ would show up in the gate-voltage dependence, temperature dependence, and/or frequency dependence of the noise in Eq. (2.2). It should be noted that many standard simplifying assumptions are made in the derivation of Eq. (2.2), and good agreement with this model and experimental data obtained on parts similar to these has been reported [1]-[5], [37], [38].

Past work involving studies of the 1/f noise of thin-metal films as a function of temperature has revealed significant insight into the nature and energy structure of the defects that cause the noise [39], [40]. Dutta and Horn have shown that the noise magnitude of metal films typically has a strong temperature dependence, with a well-defined peak structure that is characteristic of the metal being studied [39]. In particular, they demonstrated that the temperature dependence of the 1/f noise of many different types of metal films could be explained if it is assumed that the noise is due to a thermally activated process with a distribution of characteristic times (alternatively, the noise could be due to a random, activated process with a distribution of activation energies.) Furthermore, this process need not have a constant distribution of activation energies, but one that varies slowly with $k_B T$ will produce a 1/f^α spectrum, where, typically $0.8 \leq \alpha \leq 1.4$. When $D(E_0)$ varies slowly over any range $\Delta E \sim k_B T$, the energy distribution of defects causing the noise can be related to the noise spectral density through

$$D(E_0) \propto \frac{\omega}{k_B T} S(\omega, T), \tag{2.3}$$

where $\omega = 2\pi f$. The activation energy of the defect, E_0, is related to the temperature and frequency by

$$E_0 \approx k_B T ln(\omega \tau_0), \tag{2.4}$$

where τ_0 is the characteristic time for the defect. Dutta and Horn also derived an expression for the frequency and temperature dependence of the noise, given by

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega \tau_0)} \left(\frac{\delta \ln S(\omega, T)}{\delta \ln T} - 1 \right), \tag{2.5}$$

where the frequency exponent α is defined as

$$\alpha = -\frac{\partial \ln S}{\partial \ln f}. \tag{2.6}$$

It was shown that the distribution of activation energies, $D(E_0)$, could be inferred directly from $S(\omega, T)$, through Eq. (2.3). The relationships developed in [39] have become instrumental in the analysis of $1/f$ noise in semiconductor devices. In particular, past work has demonstrated that the $1/f$ noise of most bulk MOS and buried oxide transistors satisfies the Dutta-Horn criteria [38], [41]-[44], enabling use of the equations above in extracting useful information about the defect energies and distributions from noise measurements as a function of temperature for those particular devices.

Radiation Effects in MOS Devices

Ionizing radiation causes damage in solid-state devices. Exposure to ionizing radiation can alter the physical microstructure of the device, temporarily or permanently, causing changes in device properties and operating characteristics. This is obviously a major concern for microelectronics operating in radiation environments, particularly for defense and space applications. As such, much time and resources have been devoted to understanding as much as possible about radiation effects in microelectronics, the short-term and long-term damage, time-dependent responses, and mitigation techniques. Sources of radiation in space and defense environments include x-rays, energetic electrons, protons, and heavy ionized particles, the effects of which can be observed and studied on the material level (semiconductor, oxide material), device level (diode, capacitor, transistor), circuit level (e. g., memory, logic), and chip level (e. g. , microprocessors). These can be separated into two different areas of study: total dose effects and single event effects. Total dose effects entail the damage and degradation

accumulated over time from radiation exposure, while single event effects include device or circuit response to interaction with a single ionizing particle. For this study, we focus on total dose effects in MOS devices, which are described next in detail.

For MOS devices, the oxide is the most total-dose radiation-sensitive part; the radiation response of the device is dominated by four main physical processes, illustrated in Figure 2, after [45]. When a MOS device is exposed to ionizing radiation, electron-hole pairs are created in the oxide (process 1). Because electrons have a much higher mobility than holes in SiO_2, the majority of the electrons are swept out of the oxide, under the influence of the gate bias. Some fraction of the electrons and holes will recombine after the initial exposure, the amount of which depends on the strength of the electric field in the oxide and the energy of the incident irradiation.
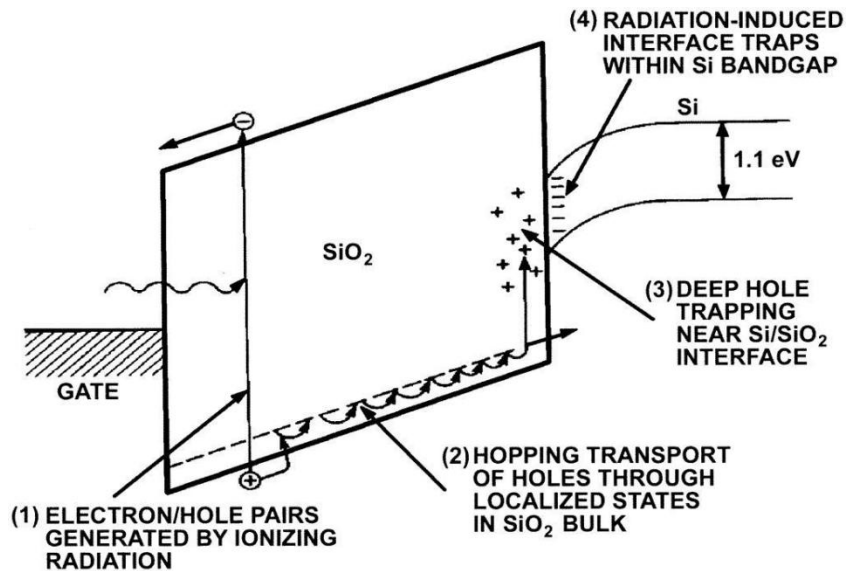
Figure 2: Band diagram of a MOS system with a positive gate bias, after [45].

The holes that escape recombination then transport through the oxide to the Si/SiO$_2$ interface (process 2), where some fall into deep trap states (process 3). The fourth major process in MOS radiation response is the buildup of interface traps at the Si/SiO$_2$ interface. As the holes transport through the oxide, they free hydrogen, in the form of protons, which then migrate to the interface and can depassivate Si-H bonds, forming H$_2$ and silicon dangling bonds, which can act as interface traps (process 4) [45], [46]. The charge state of these traps depends on the gate bias.

Radiation-induced oxide trapped charge and interface traps are a significant concern for MOS transistors, particularly because of their effects on device operating parameters. The positive oxide trapped charge generated by ionizing radiation causes a negative shift in the threshold voltage of MOS transistors. Interface trapped charge depends on the gate bias. For an nMOS transistor (positive gate bias), the interface trapped charge is negative, which causes a positive shift in threshold voltage; for a pMOS transistor (negative gate bias), the interface trapped charge is positive, causing a negative shift in threshold voltage [47]. The oxide charge buildup is greatest after initial irradiation, and anneals with time, while interface trap buildup typically continues to increase with time. Depending on the radiation-tolerance of the oxide, radiation-induced damage can be quite severe for MOS transistors, even causing device failure.

In addition to an increase in charge density within the oxide and trap density at the oxide-silicon interface, radiation exposure increases the low frequency noise levels of MOS devices [1]-[3], [37], [48], [49]. The pre-irradiation 1/f noise of MOS devices has been found to correlate strongly with the post-irradiation threshold voltage shift due to oxide trapped charge. In particular, Scofield *et al.* showed a nearly linear relationship

between the pre-irradiation normalized noise magnitudes of devices and ΔV_{ot}, with the noisiest devices exhibiting the largest ΔV_{ot}, as shown in Figure 3 [1]; much less correlation was found to exist between the noise and threshold voltage shift due to interface traps, ΔV_{it}.
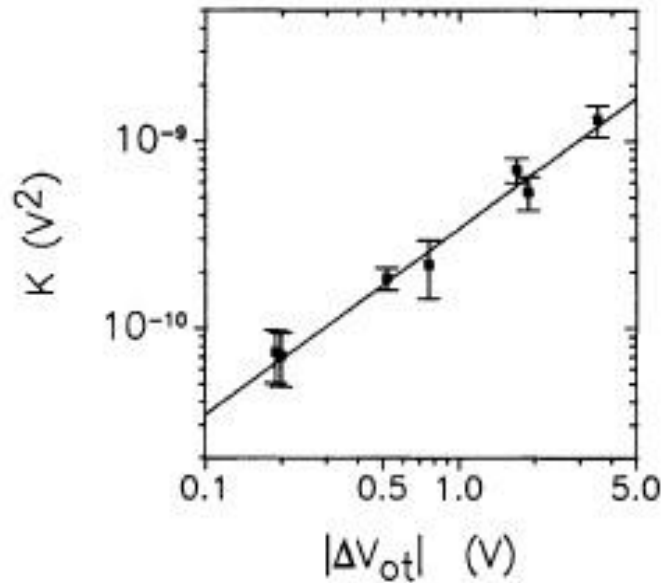
Figure 3: Noise magnitude K as a function of radiation-induced threshold voltage shift due to oxide trapped charge ΔV_{ot}, after [1].

Furthermore, in [3], the 1/f noise was observed to increase with increasing oxide trapped charge during irradiation for both nMOS and pMOS devices. These studies led to the conclusion that oxide traps within a few nanometers of the Si/SiO_2 interface were responsible for the 1/f noise in MOS devices. These traps were termed 'border traps' [49].

Aging, Reliability and Moisture Exposure

In addition to radiation exposure, harsh operating and storage conditions, as well as the normal aging process, all can degrade device performance, with moisture

absorption affecting these significantly. If water is introduced into devices during processing, water molecules can diffuse into the gate oxides of MOS devices during long-term storage in non-hermetic environments.

Rodgers *et al.* showed that the irradiation and annealing responses of nMOS transistors could change significantly after 17 years of room-temperature storage [6]. These devices experienced a much larger increase in threshold-voltage rebound during post-irradiation annealing than devices from the same wafer that were tested in the original study in 1988. They attributed these shifts in threshold voltage to an increase in interface trap generation during irradiation and annealing, and found that baking these devices prior to irradiation reduced the shifts significantly. They concluded that the aging-related changes observed in these devices were likely due to water molecules absorbed during non-hermetic storage.

Work done by Batyrev *et al.* with devices from the same lot as in [6] showed that exposure to moisture at elevated temperatures significantly increased the interface trap buildup during post-irradiation annealing, as compared to devices that were not exposed to moisture, and devices that were baked prior to irradiation [7]. All devices in the study showed an increase in interface trap buildup compared to devices irradiated in the original study.

In a more recent study, moisture was intentionally introduced into the oxides of nMOS and pMOS transistors [8]-[10], which led to enhanced degradation in the radiation response of these devices. However, the moisture-related effects were more significant in the pMOS transistors. These results were confirmed by $1/f$ noise measurements, where

the moisture-exposed pMOS devices experienced a larger increase in $1/f$ noise, while little appreciable change in the noise was observed for the exposed nMOS devices.

It was shown that water absorption in SiO_2 can create defects in the oxide, and enhance defect generation during irradiation [7], [50]. For the devices of this study, phosphorus dopants inevitably penetrate the oxide regions that overlie the source/drain junctions in the nMOS devices, and, likewise, boron dopants penetrate the oxide regions that overlie the source/drain junctions in the pMOS devices, during the source/drain implant steps. Phosphorus has been shown to suppress water penetration in doped oxides, while boron can increase the number of molecular water sites without reacting with the diffusing water, allowing penetration deep into the film [51], [52]. These differences have led to enhanced defect generation in the pMOS oxides, compared to nMOS devices, resulting in the increased noise in the moisture-exposed pMOS devices before and after irradiation [9], [10].

These studies demonstrate the importance of aging-related effects on MOS response. In particular, MOS response and reliability does not remain constant over time, but can degrade, with the extent of degradation greatly influenced by the storage and operating conditions. Furthermore, these studies highlight the critical role water absorption can play in MOS radiation and aging response.

CHAPTER 3

DEVICES AND EXPERIMENTAL DETAILS

This chapter describes the Si and Ge transistors used in this study, the different measurement techniques used to characterize these devices, and the experimental conditions to which they were subjected.

Devices

Si nMOS and pMOS

The Si nMOS and pMOS transistors used in this study were fabricated in 1984 at Sandia National Laboratories, and packaged in 1987. These transistors have poly-crystalline silicon gates and come from two process lots, G1916A (wafer 10) and G1928A (wafer 16 and 28). The devices from wafer 10 have an oxide thickness of 37 nm, and received a 30-minute, 1100 °C N_2 post-oxidation anneal. This type of processing is known to greatly increase the density of oxygen vacancies and vacancy complexes in SiO_2 [3], [41], [53]-[55]. Wafer 16 devices have an oxide thickness of 25.4 nm, and wafer 28 devices have an oxide thickness of 68.2 nm. The nMOS transistors have a doping concentration of $\sim 2.7 \times 10^{15}$ cm^{-3} and the pMOS transistors have a doping concentration of $\sim 4 \times 10^{15}$ cm^{-3}. All parts were stored for 20 years prior to noise measurements. Some devices were exposed to 85 % relative humidity at 130 °C for one week; control devices either remained hermetically sealed during this process or were not exposed at all [8].

Ge pMOS

The Ge devices are pMOSFETs with a Ge layer deposited onto Si, built at imec on Ge-on-Si epitaxial substrates [15]. Devices from process splits D05/D10 had 5/8 Si monolayers deposited onto the Ge layer before gate-dielectric formation and received As halo implants at a dose of $5 \times 10^{13}/6.5 \times 10^{13}$ cm^{-2} [15], [20]. Above the Si monolayers is 4 nm of hafnium oxide (HfO$_2$), which is followed by 10 nm of tantalum nitride (TaN) and 70 nm of titanium nitride (TiN), deposited by physical vapor deposition. The equivalent oxide thickness (EOT) of the gate dielectric is ~1.2 nm. A cross-section of this device is shown in Figure 4 below.
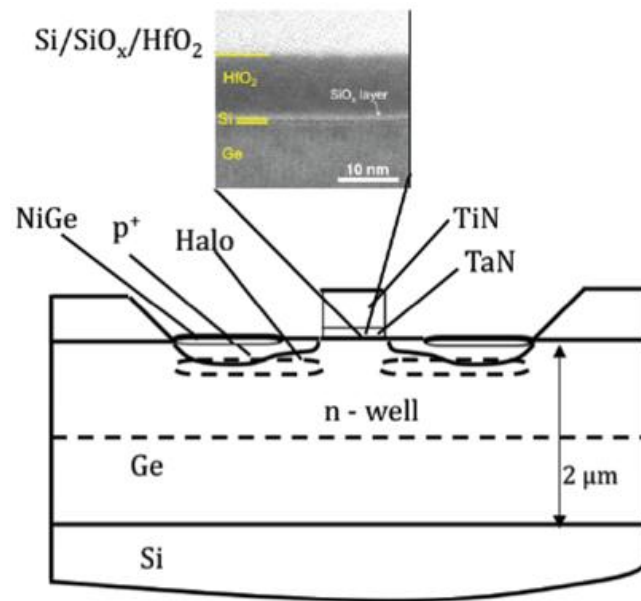
Figure 4: Cross-section of the Ge pMOS transistors used in this study [15], [20], [68].

Experimental Setup and Measurement Techniques

Noise measurements

Excess noise measurements (corrected for background noise) were performed on these transistors operating in strong inversion in their linear regimes, using a setup similar to that in [1], shown below in Figure 5. A constant voltage source V_A in series with a 20 kΩ resistor was connected to the MOSFET drain. A second, constant voltage source V_B was connected directly to the gate. Both the source and drain were grounded. The drain voltage noise was amplified using a low-noise preamplifier, the output of which was connected to the input of a spectrum analyzer for calculating the power spectral density spectrum.
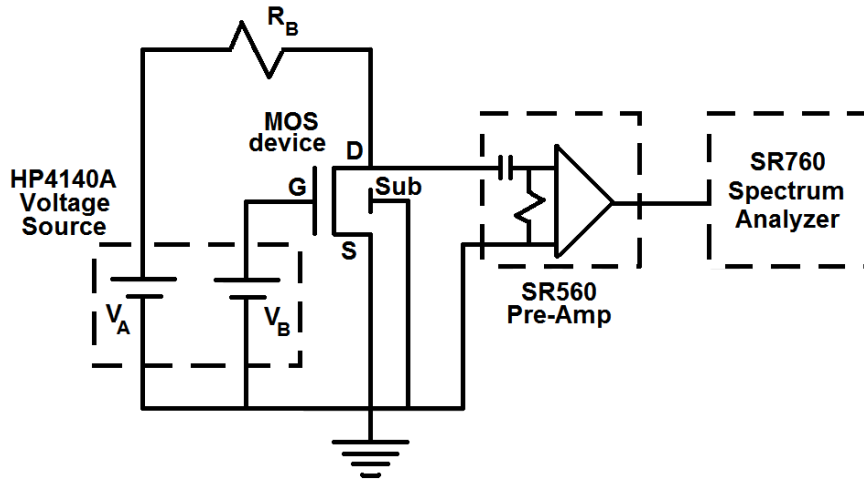
Figure 5: 1/f noise measuring circuit diagram.

The frequency span of the noise measurements either extended from approximately 6 Hz to 400 Hz, or 4 Hz to 1000 Hz. During the noise measurements, the drain voltage V_D was held at a constant $\pm$ 100 mV ('+' for nMOS devices, '−' for pMOS

devices). The gate-to-threshold voltage V_G–V_T was varied during the measurements. The dependence of the excess noise on frequency, drain voltage, and gate voltage was described by

$$S_V(f, V_D, V_G) = \frac{K}{f^\alpha} \frac{V_D^2}{(V_G - V_T)^\beta},$$ (3.1)

where K is the normalized noise magnitude of the device, α represents the frequency dependence, and β is a measure of the gate-voltage dependence, where $S_V \propto (V_G - V_T)^{-\beta}$ [1], [3]. The frequency exponent α is determined by the best fit to S_V over the entire, accessible frequency span [39].

To determine the gate-voltage dependence of these devices, S_V was measured for varying $\left| V_G - V_T \right|$. Log-log plots of S_V (at ~10Hz) versus $\left| V_G - V_T \right|$ were produced, and a linear fit was performed on the plotted data to determine the slope, β.

Charge pumping

Charge pumping is a widely used and sensitive method for characterizing the semiconductor-dielectric interface of MOS devices. Different variations of this measurement have been developed to determine the mean density of interface traps, their energy and spatial distributions, and capture cross sections [56]-[63]; however, the basic principle throughout all of these variations is the same. For a MOS transistor, a voltage pulse is applied to the gate, the source and drain are tied together and slightly reverse-biased, or grounded, and current is measured at the substrate as the gate is pulsed between inversion and accumulation. A typical measurement setup is shown in Figure 6.
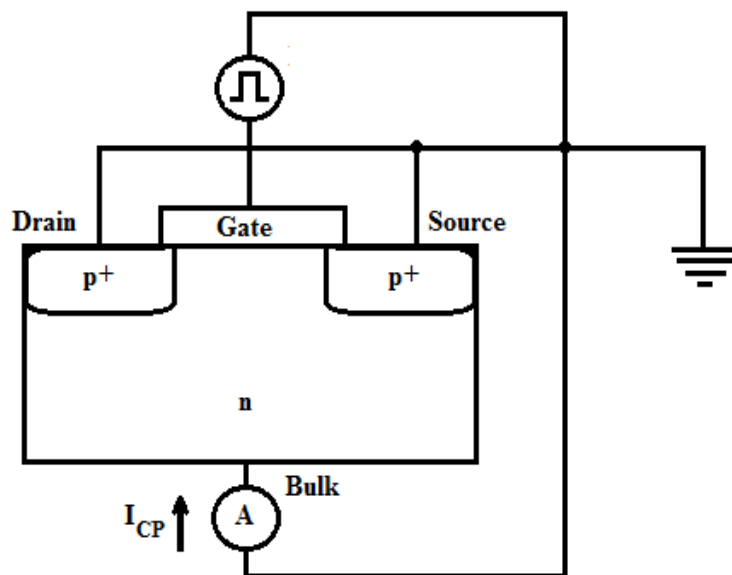
Figure 6: Typical bias and measurement circuit for measuring recombination current I_{CP}.

During inversion, holes (electrons for nMOS) flow to the surface from the source and drain, and are captured by interface traps. When the gate is switched to accumulation, the remaining holes flow back to the source and drain, and the interface is flooded with electrons. Some of these electrons are captured by the interface traps and recombine with the trapped holes, producing a net recombination current measured at the substrate. This current is proportional to the density of interface traps.

For these devices, two charge pumping techniques were used to characterize the interface trap densities: the square pulse method [14], [57]-[59], and the three-level method [60]-[63]. During the square pulse method, a pulse of constant amplitude is applied to the gate, and the charge pumping current is measured as a function of the base voltage, V_{base}. The voltage pulse is incremented from below the flat band voltage V_{FB} to above the threshold voltage V_T, as illustrated in the left hand part of the figure below.
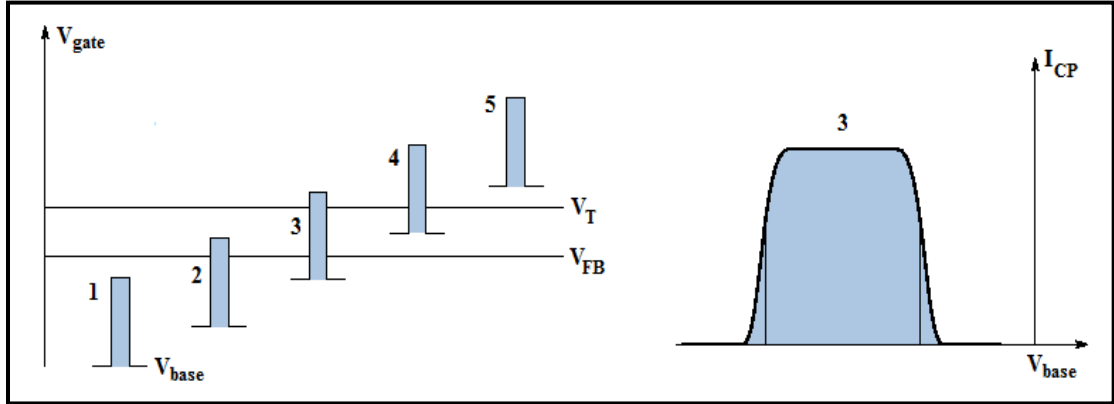
Figure 7: Illustration of variable base, square pulse charge pumping method, [64].

When the charge pumping current I_{CP} is plotted as a function of V_{base}, a shape similar to what is shown in the right hand part of Figure 7 results, with the peak of the curve occurring when the bottom of the pulse is below the flat band voltage and the top of the pulse is above the threshold voltage (numbered '3'). From these values, the interface trap density can be estimated by [14], [57]-[59],

$$I_{CP} = qA_G f D_{it} \Delta\Psi_S. \tag{3.2}$$

Here, q is the electronic charge, A_G is the device area, f is the charge pumping frequency, $\Delta\Psi_S$ is the change in surface potential, and D_{it} (cm^{-2}eV^{-1}) is the mean interface trap density, averaged over the energy levels swept through by the Fermi level.

The three-level method was used to determine the interface trap density as a function of energy [60]-[63]. This method is similar to the one previously described, with the exception of a mid-level step voltage, V_{STEP}, incorporated into the gate pulse, as shown in Figure 8.
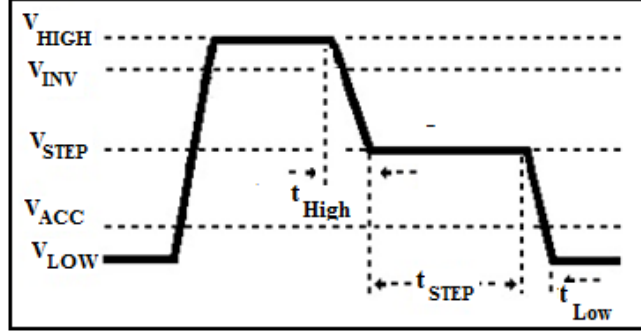
Figure 8: Three-level voltage waveform applied to gate.

When the voltage level of the pulse is at V_{HIGH}, the device is in strong inversion, and the interface traps are filled with holes. When the pulse is switched to V_{STEP}, many of the trapped holes are emitted back to the valence band. For sufficiently long values of t_{STEP}, the trapped holes above a certain energy level, determined by V_{STEP}, will be emitted, and the trap occupancy will reach equilibrium. Then, when V_{LOW} is reached, electrons are brought back to the interface to recombine with the remaining trapped holes, producing the charge pumping current. As V_{STEP} is varied, the equilibrium trap occupancy level will vary, resulting in a change in I_{CP}.

The relationship between the I_{CP}, V_{STEP}, and the interface trap density is given by [60]-[63]

$$D_{it}(E_t) = \frac{1}{qfA_G} \frac{dI_{CP}}{dV_{STEP}} \frac{dV_{STEP}}{d\Phi_S},\tag{3.3}$$

where Φ_S is the surface potential established by V_{STEP}. The timing features of the waveform are described by t_{High}, t_{STEP}, and t_{LOW}. For Eq. (3.3) to be used, the time constant of the emission process, τ_E, must fall between t_{LOW} and t_{STEP}, that is,

$$t_L < \tau_E < t_{STEP} \ . \tag{3.4}$$

In this the region, $\delta I_{CP}/\delta V_{STEP}$ is directly proportional to D_{it} [63].

Irradiation experiments

Irradiation experiments were performed using an ARACOR Model 4100 10-keV X-ray irradiator. For the Si devices, the gates were biased at +6 V and all other terminals were grounded. For the Ge pMOS transistors, transmission gate bias was applied (worst case for leakage current degradation in these devices [15], [20]), with the drain and source biased at −1 V and all other terminals grounded. The Ge pMOS devices were annealed under these same conditions. All parts were irradiated at a dose rate of 31.5 krad(SiO$_2$)/min.

CHAPTER 4

EFFECTS OF MOISTURE EXPOSURE AND TOTAL DOSE IRRADIATION ON
THE 1/F NOISE AND GATE-VOLTAGE DEPENDENCE OF NMOS AND PMOS
TRANSISTORS

This chapter presents results on the low frequency noise data of moisture-exposed

and control Si n-channel and p-channel devices before and after total dose irradiation,

focusing on the effects of moisture exposure and irradiation on the frequency, gate-

voltage, and temperature dependences of the noise in these devices. Significant changes

in defect energy distributions are observed after irradiation.

Low Frequency Noise Gate-Voltage and Frequency Dependence of MOS Devices

Figure 9 shows the excess drain-voltage noise power spectral density S_V at ~10

Hz as a function of $\left| V_G - V_T \right|$ for 2-μm channel-length, 16-μm channel-width nMOS and

pMOS transistors from the wafer 10 ($t_{ox} = 37$ nm, N_2 post-oxidation anneal) control part,

prior to irradiation. For the nMOS device, the slope $\beta = 1.7$. For the pMOS device, $\beta =$

0.5, indicating a trap energy distribution that deviates much more significantly from

uniformity than for the nMOS device [1], [37].
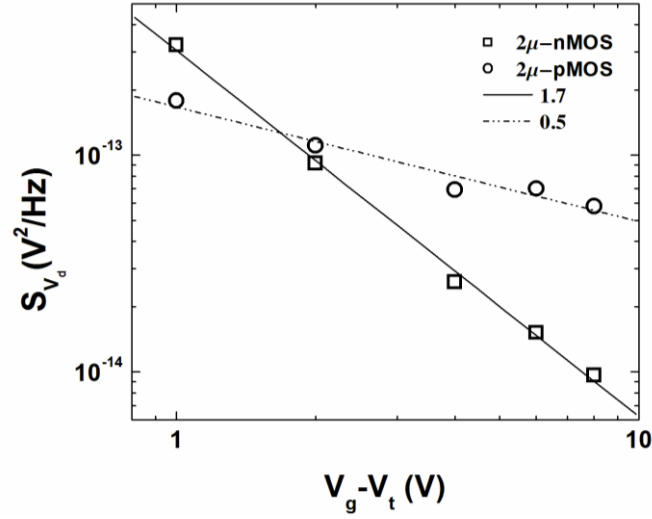
Figure 9: Excess drain-voltage noise power spectral density S_V at ~10 Hz as a function of the absolute value of V_G–V_T for 2 μm x 16 μm nMOS and pMOS transistors from the control part of wafer 10, prior to irradiation, after [10].

Figure 10 shows S_V as a function of frequency f for 3-μm nMOS and pMOS control devices from wafer 10, prior to irradiation. There is a difference in the frequency dependence of the noise for the nMOS and pMOS devices, indicated by the differences in the slopes of the spectra. For the nMOS device, the frequency exponent, α, is close to unity, as expected for $1/f$ noise resulting from relatively uniform densities of traps in energy and space [1]-[4], [39], consistent with the results in Figure 9. For the pMOS device, α is greater than unity, again reflecting a departure from uniformity in $D_t(E_f)$, which is also consistent with the results in Figure 9. The nMOS and pMOS gate-voltage dependences presented in Figure 9, and the frequency dependences illustrated in Figure 10, are all typical of the $1/f$ noise dependences observed for these types of devices in this study (from different wafers and process lots), prior to irradiation, and are consistent with results reported previously on similarly processed devices [1]- [3], [37].

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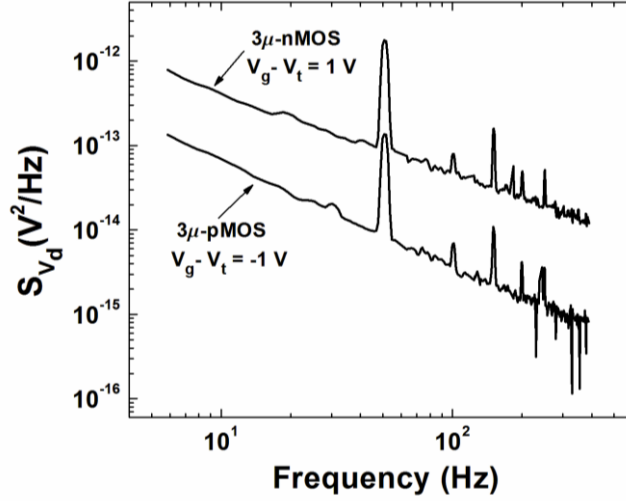
Figure 10: S_V as a function of frequency for 3 µm x 16 µm nMOS and pMOS transistors from the control part of wafer 10, prior to irradiation. The spikes in the spectra are from 60 Hz pickup and its harmonics, which are ignored in the data analysis, after [10].

Figure 11 shows S_V as a function of frequency f for 3 µm × 16 µm (length L × width W) n-channel moisture-exposed and control transistors from wafer 10 before and after 500 krad(SiO$_2$) total dose irradiation at $V_G–V_T = 1$ V.
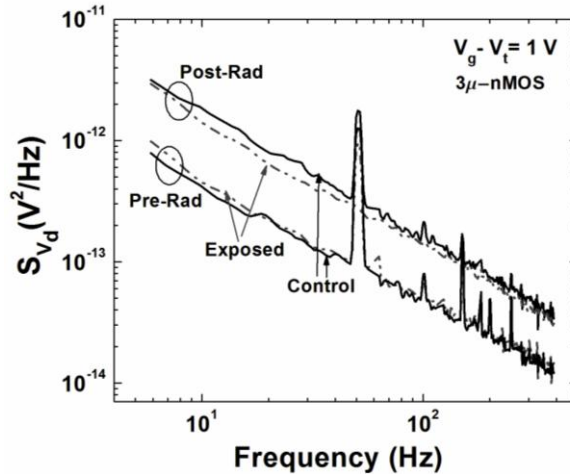
Figure 11: S_V as a function of frequency for 3 µm x 16 µm nMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO$_2$) total dose irradiation. The background noise was subtracted to obtain the excess noise. The spikes in the spectra are from 60 Hz pickup and its harmonics; these are neglected in the analysis of the noise, after [10].

There is no significant difference between the pre-irradiation noise for the nMOS control and exposed devices; the post-irradiation noise for the control device is slightly larger than that for the moisture-exposed device. For both the control and exposed devices, the frequency exponent α is close to unity before and after irradiation, as expected for $1/f$ noise resulting from relatively uniform densities of traps in energy and space [1]-[4], [39].

Figure 12 plots S_V at ~10 Hz as a function of V_G–V_T for the 3 μm n-channel moisture-exposed and control devices of Figure 11 before and after 500 krad(SiO$_2$) total dose irradiation. There is relatively little change in the gate-voltage dependence of the noise for both the exposed and control devices after irradiation. For the exposed device, prior to irradiation, $\beta = 1.5$, and after irradiation $\beta = 1.8$; for the control device, prior to irradiation, $\beta = 1.7$, and after irradiation $\beta = 1.9$. These dependences are in reasonable agreement with Eq. (2.2), indicating a more uniform $D_t(E_f)$ after irradiation, consistent with the frequency dependences observed in Figure 11.
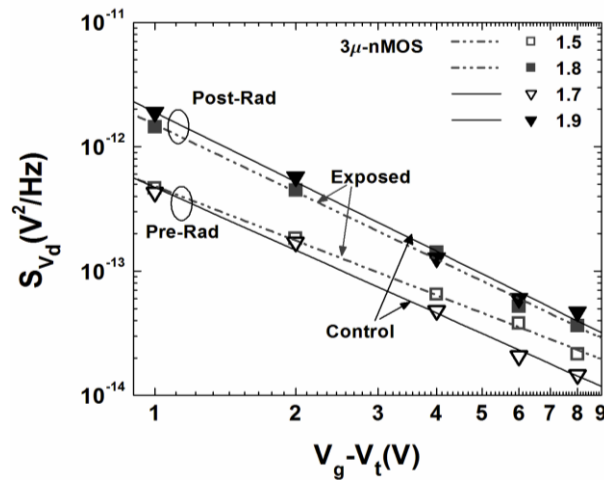
Figure 12: S_V at ~10 Hz as a function of V_G–V_T for 3 μm x 16 μm nMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO$_2$) total dose irradiation, after [10].

Figure 13 shows S_V versus f for 3 μm x 16 μm p-channel moisture-exposed and control transistors from wafer 10 before and after 500 krad(SiO$_2$) total dose irradiation at $V_G - V_T = -1$ V. In contrast to the nMOS devices of Figure 11, the pre-irradiation and post-irradiation noise for the exposed pMOS device is much higher than that for the control device.
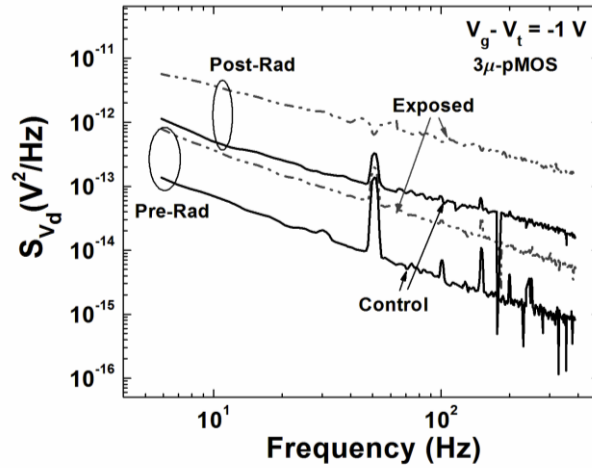
Figure 13: S_V as a function of frequency for 3 μm x 16 μm pMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO$_2$) total dose irradiation, after [10].

These results demonstrate enhanced pMOS sensitivity to moisture, compared to nMOS devices [8]-[10]. Furthermore, there is an obvious change in the frequency dependence of the noise for the pMOS devices of Figure 13 after irradiation. For the control pMOS device, prior to irradiation, $\alpha = 1.3$, and for the exposed device $\alpha = 1.2$. After irradiation, $\alpha = 1.1$ for the control device and $\alpha = 0.9$ for the exposed device,

indicating a more uniform trap energy distribution after moisture exposure and irradiation than before [1]-[4], [39].

Figure 14 shows S_V at ~10 Hz as a function of $\left|V_G{-}V_T\right|$ for the 3 μm p-channel moisture-exposed and control devices of Figure 13 before and after total dose irradiation. There is a significant change in the gate-voltage dependence of the noise with irradiation for both devices, signified by the increase in β. These results, along with the changes in frequency dependence illustrated in Figure 13, reflect a change in the trap energy distributions with irradiation for both the exposed and control devices. In particular, for the moisture-exposed device, $\beta \approx 2$ after irradiation, indicating a more uniform $D_t(E_f)$.
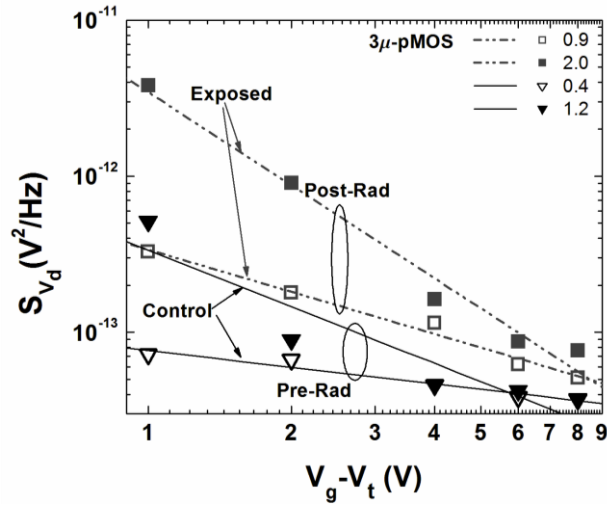
Figure 14: S_V at ~10 Hz as a function of $\left|V_G{-}V_T\right|$ for 3 μm x 16 μm pMOS transistors from the control and moisture-exposed parts from wafer 10, before and after 500 krad(SiO$_2$) total dose irradiation, after [10].

Figure 15 shows the gate-voltage dependence of moisture exposed pMOS devices from wafer 16 after 500 krad(SiO$_2$) total dose irradiation. For all three transistor channel lengths, $\beta \approx 3$ over a significant fraction of the voltage range. To the best of our knowledge, this behavior has not been reported previously in the literature. One possible

explanation is that irradiation, after moisture exposure, has significantly altered the trap energy distributions for these devices, so that $D_t(E_f)$ is now increasing toward midgap. The frequency dependences for these devices is much less than unity at $\left| V_G-V_T \right| = 1$ V, but increases with increasing $\left| V_G-V_T \right|$, as shown in Figure 16. We now explore this possibility further.
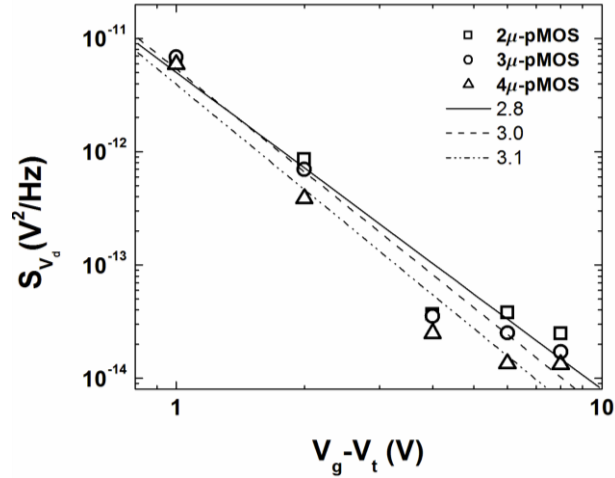
Figure 15: S_V at ~10 Hz as a function of $\left| V_G-V_T \right|$ for pMOS transistors from the moisture-exposed part from wafer 16, after 500 krad(SiO$_2$) total dose irradiation, after [10].
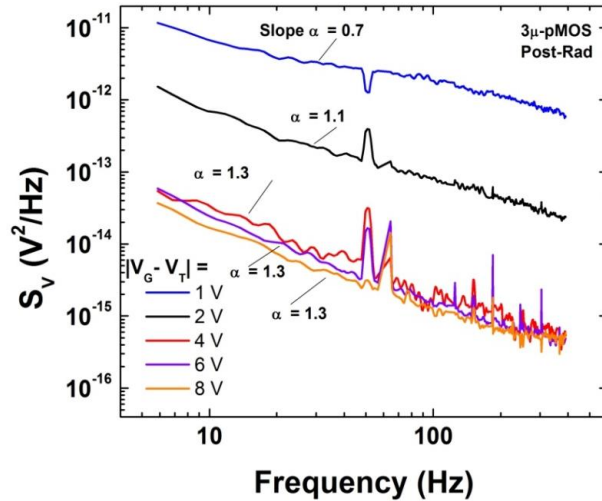
Figure 16: S_V as a function of frequency and $\left| V_G-V_T \right|$ for the 3-μm pMOS transistor of Figure 15.

Figure 17 and Figure 18 show $D_t(E_f)$, calculated from Eq. 1 at $f \approx 10$ Hz and for $V_g-V_t = 1, 2, 4, 6,$ and 8 V, as a function of energy for the 3 μm x 16 μm moisture-exposed nMOS and pMOS transistors of Figure 12, Figure 14 and Figure 15. From these measurements, we can approximate the energy level of $D_t(E_f)$ for each V_g-V_t, and examine the variation of the trap density through energy in the silicon band gap. Here we estimate $\tau_1/\tau_0 \approx 10^{12}$ to be consistent with previous work [3], [5], [49], [70].
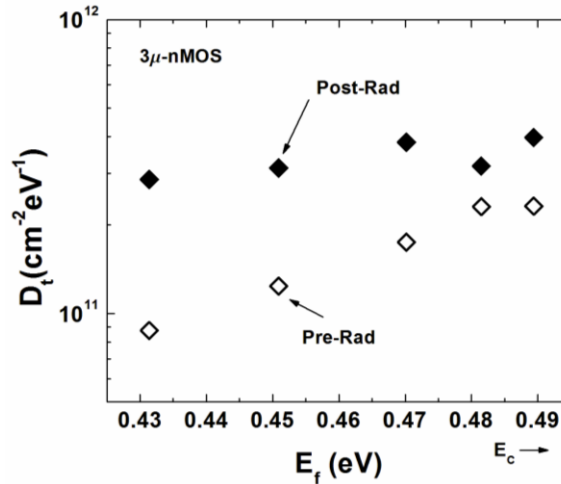
Figure 17: Inferred trap distribution as a function of energy for the 3 μm x 16 μm nMOS transistor from the moisture-exposed wafer 10 part, before and after 500 krad(SiO_2) total dose irradiation, after [10].

In Figure 17, the inferred pre-irradiation and post-irradiation trap densities for the nMOS devices do not vary significantly over the voltage range shown. There is a slight change in the shape of $D_t(E_f)$ with irradiation, with the post-irradiation density more uniform across the voltage range, corresponding to the change in β in Figure 12 to a value closer to 2.
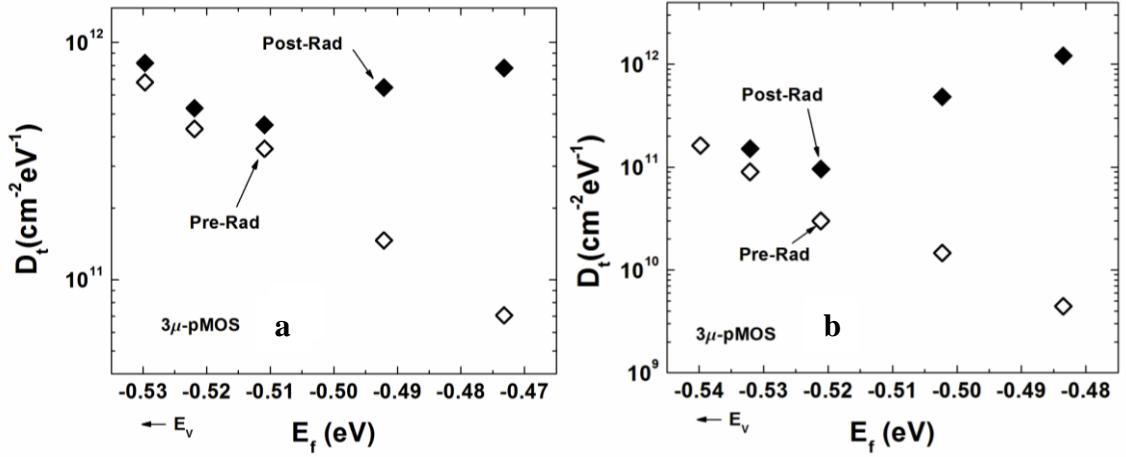
Figure 18: Inferred trap distribution as a function of energy for 3 μm x 16 μm moisture-exposed pMOS transistors from (a) wafer 10 and (b) wafer 16, before and after 500 krad(SiO$_2$) total dose irradiation, after [10].

In Figure 18, however, the trap density profiles for the pMOS devices change drastically with irradiation, corresponding to the large changes in β in Figure 14 and Figure 15. In particular, the pre-irradiation $D_t(E_f)$ is increasing with increasing $|V_G{-}V_T|$ for both pMOS devices. After irradiation, $D_t(E_f)$ for the device of Figure 18(a) appears more uniform, corresponding to $\beta \approx 2$ in Figure 14, while $D_t(E_f)$ for the device of Figure 18(b) is now decreasing with increasing $|V_G{-}V_T|$, corresponding to $\beta = 3$ in Figure 15.

These data not only demonstrate the significant differences in the way nMOS and pMOS 1/f noise (and consequently the border trap densities) are affected by direct moisture exposure and total dose irradiation, but also indicate that water absorption in the control pMOS oxides, possible due to long-term storage [6], [7], has led to the significant changes observed in the gate-voltage dependence with irradiation for these devices as well. Furthermore, 1/f noise measurements, in particular the frequency and gate-voltage dependences, have proven to be a useful tool in revealing changes in the trap energy distributions of these devices before and after irradiation.

<u>Temperature Dependence of the 1/*f* Noise of pMOS Devices</u>

Figure 19 shows the excess drain-voltage power spectral density S_V at ~10 Hz as a function of temperature T and defect energy E_0 for 2 μm x 16 μm unirradiated, moisture-exposed and control pMOS devices from wafer 16 (t_{ox} = 25.4 nm). E_0 is the activation energy inferred from the Dutta-Horn relation of Eq. (2.3).
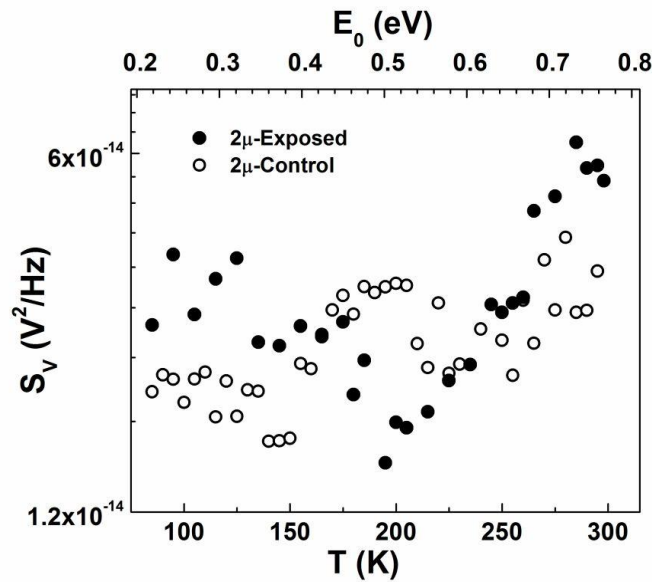
Figure 19: S_V at ~10 Hz as a function of temperature T and E_0 for 2 μm x 16 μm unirradiated, moisture-exposed and control pMOS transistors from wafer 16. The energy scale inferred from the Dutta-Horn model is on the upper x-axis.

Since S_V is proportional to the trap density [1]-[4], [38], [39], [41], the energy distribution of the trap densities can be inferred by a representation of S_V as a function of E_0. The data for the moisture-exposed device are denoted by the solid black symbols, and the data for the control device are represented by the open symbols. For these parts, the noise levels closer to room temperature are higher than those below room temperature, with the room temperature noise of the moisture-exposed device larger than that of the

control device, consistent with previous work at ~300 K [8]. For the moisture-exposed device, S_V has peaks in the lower temperature range, decreases toward 200 K, then increases again toward room temperature. For the control device, S_V has a peak around 200 K, decreases around 225 K, then increases again toward room temperature.

To determine whether the noise of these devices can be described by the Dutta-Horn model, Eq. (2.5) is used to calculate the temperature dependence of the frequency exponent, $\alpha(T)$, from the noise measured as a function of temperature, and compared to the measured values of $\alpha(T)$. A value of 1.8×10^{-15} s is used for τ_0, corresponding to a typical inverse-phonon frequency in the near-interfacial SiO_2 [41], [65], [66]. Figure 20 shows the results of this comparison for the moisture-exposed device of Figure 19.
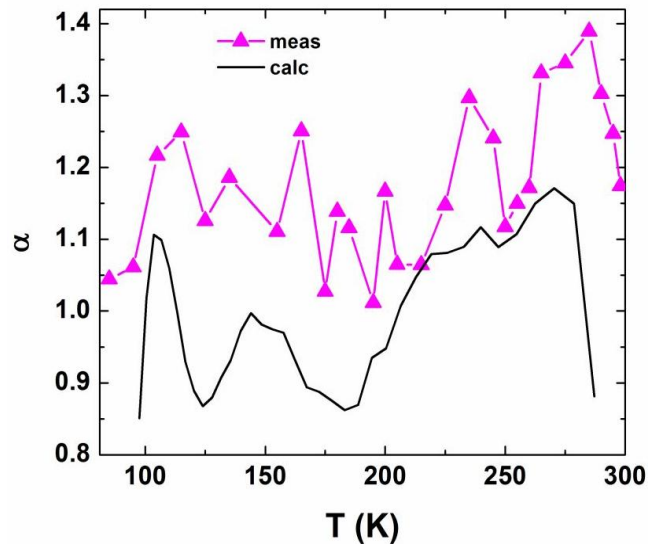
Figure 20: Frequency exponent α as a function of T for the 2 μm x 16 μm moisture-exposed pMOS transistor of Figure 19. The solid triangles represent measured data, and the solid line denotes data calculated from Eq. (2.5).

For the device of Figure 19, the calculated values of $\alpha(T)$ are smaller in magnitude in than the measured $\alpha(T)$ in most places throughout the temperature range.

However, the calculated values seem to follow the general trend in peaks of measured $\alpha(T)$, particularly in the lower temperature range. From about 200 K, calculated $\alpha(T)$ increases toward room temperature, similar to measured $\alpha(T)$, although there is no clear double-peaked feature like that in the measured values.

Figure 21 shows S_V ~10 Hz as a function of $\left|V_G\text{–}V_T\right|$ for the moisture-exposed pMOS device of Figure 19 at temperatures of 145 K, 245 K, and room temperature. A line with a slope of –2 is drawn in the figure as a reference.
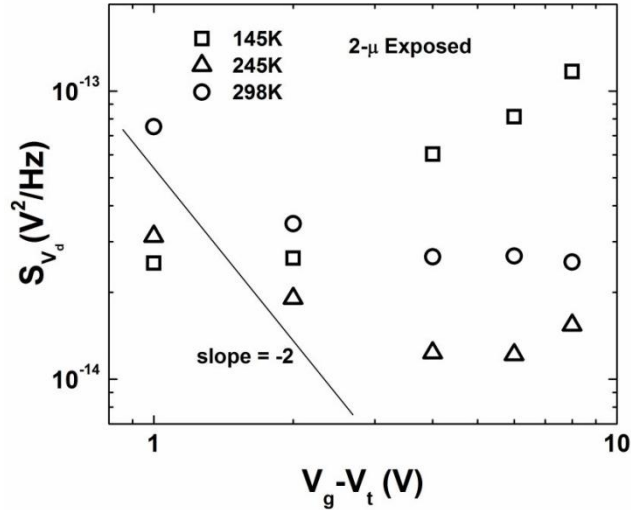
Figure 21: S_V at ~10 Hz as a function of $\left|V_G\text{–}V_T\right|$ for the 2 µm x 16 µm unirradiated, moisture-exposed pMOS transistor of Figure 19 at 145 K, 245 K, and 298 K.

The gate-voltage dependence of the noise at 245 K and 298 K is significantly less than a $(V_G\text{–}V_T)^{-2}$ dependence, indicating a non-uniform trap energy distribution. There is a distinct change in the voltage dependence of the noise at these temperatures, particularly at voltages higher than $\left|V_G\text{–}V_T\right|$ = 4 V. From Figure 19 and Figure 20, S_V increases up to 245 K, then decreases to 250 K; α decreases from 235 K to 250 K. Near

room temperature, S_V increases slightly from 290 K to 295 K, then decreases to 298 K; α decreases from 290 K to 295 K. In contrast to what is observed at 245 K and 298 K, the noise increases dramatically (compared to the other two temperatures investigated) with increasing $\left| V_G - V_T \right|$ for $\left| V_G - V_T \right| > 2$ V at 145 K. From Figure 19 and Figure 20, S_V decreases sharply from 125 K to 145 K, then increases to 155 K; α decreases from 135 K to 145 K, then increases again to 155 K. These changes in the frequency and temperature dependence of the noise are correlated with the changes in the gate-voltage dependence of the noise, and reflect changes in the underlying defect energy distributions [37]-[39], [41].

Figure 22 shows S_V at ~10 Hz as a function of T and E_0 for a 3 μm x 16 μm moisture-exposed pMOS device, and a 2 μm x 16 μm control pMOS device from wafer 16 after 500 krad(SiO$_2$) total dose irradiation. In contrast to the noise observed for the unirradiated pMOS devices, for the moisture-exposed part, S_V increases steadily with energy over the entire range investigated. The energy structure of the defects has also changed with irradiation for the control device.
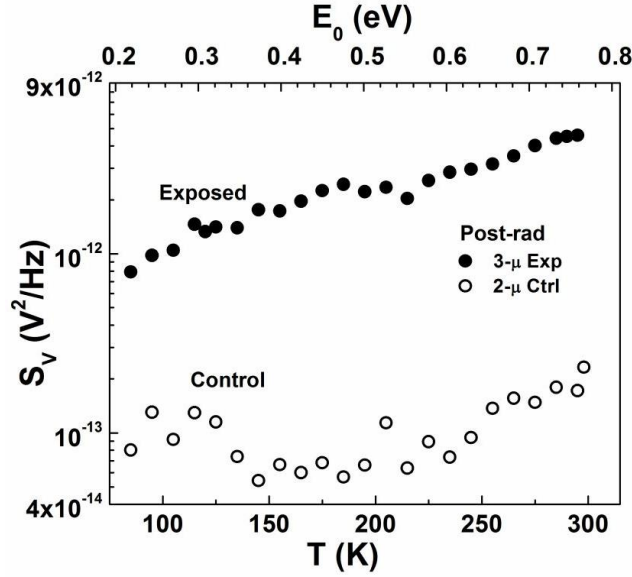
Figure 22: S_V at ~10 Hz as a function of temperature T and E_0 for 3 μm x 16 μm moisture-exposed pMOS transistor and 2 μm x 16 μm control pMOS transistor from wafer 16 after 500 krad(SiO_2) total dose irradiation.

The noise of the moisture-exposed device is much larger than the noise of the control device, even considering transistor size, over the entire temperature range, indicating enhanced trap generation during irradiation over all the energies probed with these measurements. This illustrates a significant difference in the nature of the defects introduced by irradiation alone, and by both moisture exposure and irradiation in these devices.

Figure 23 shows S_V at ~10 Hz as a function of $\left| V_G - V_T \right|$ for the moisture-exposed pMOS device of Figure 22 at 298 K before irradiation, and at 205 K and 298 K after irradiation. Again, a line with a slope of −2 is drawn in the figure as a reference. Prior to irradiation, the gate-voltage dependence is much less than a $(V_G - V_T)^{-2}$ dependence at room temperature, indicating a non-uniform trap energy distribution, similar to those observed in Figure 21. After irradiation, for both temperatures shown, the gate-voltage dependence of the noise is significantly larger than a $(V_G - V_T)^{-2}$ dependence, with the

room temperature gate-voltage dependence having the larger slope. Compared to the pre-irradiation values, the post-irradiation trap energy distribution is now mostly increasing with energy, although this increase is slightly less near 205 K.
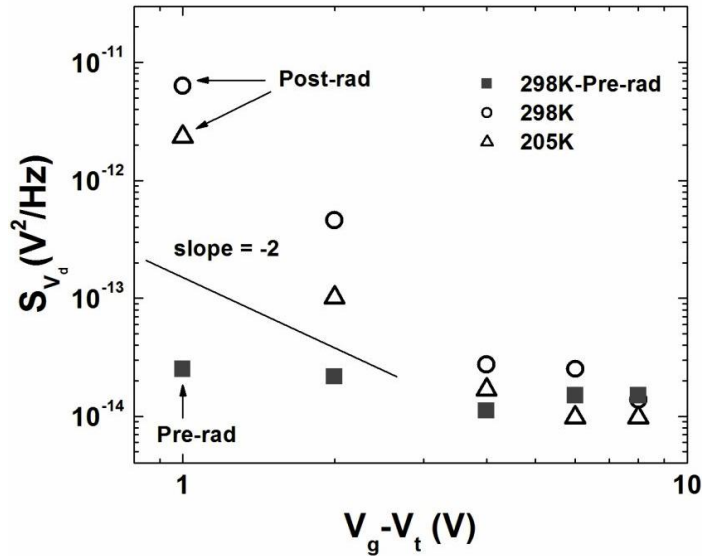
Figure 23: S_V at ~10 Hz as a function of $\left| V_G - V_T \right|$ for the 3 μm x 16 μm moisture-exposed pMOS transistor of Figure 22 at 205 K and 298 K, before and after 500 krad(SiO$_2$) total dose irradiation.

There is also a distinct transition between regions with different voltage dependences for all data sets depicted here, similar to what was observed for the unirradiated pMOS device of Figure 21 at temperatures of 245 K and 298 K. However, for this part, after irradiation, S_V varies over several orders of magnitude between $\left| V_G - V_T \right| = 1$ V and $\left| V_G - V_T \right| = 4$ V, then decreases much more slowly with increasing $\left| V_G - V_T \right|$ up to $\left| V_G - V_T \right| = 8$ V.

These results further demonstrate the effects of moisture on 1/f noise, and, hence, the border trap density of pMOS devices before and after irradiation, and provide new insight into the dominant defects introduced by moisture exposure and irradiation in these

devices. In particular, the pre-irradiation noise of the moisture-exposed device is larger than that of the control device near room temperature, suggesting that the defects introduced by moisture exposure can exchange charge more efficiently in this temperature range but not at ones immediately below this, indicating a variation in either the microstructure or type of the defect present [41]. After irradiation, the noise of the moisture-exposed device mostly increases with energy, and the defect density is much more uniform across the entire energy range. These thermally activated processes are consistent with the attributes of oxygen vacancies in the near-interfacial SiO_2 [3], [41], [54].

In addition, there are considerable differences in the gate-voltage dependence of the noise at different temperatures for the moisture-exposed device, reflecting differences in the border trap densities as a function of energy [10], [37]. After irradiation, the gate-voltage dependence changes significantly. The increase in S_V with irradiation is largest at smaller $\left| V_G - V_T \right|$ (consistent with the results on pMOS parts shown earlier in this chapter), indicating that defect creation due to moisture and irradiation is more enhanced at energy levels closer to midgap [10].

CHAPTER 5

CHARGE PUMPING AND LOW FREQUENCY NOISE IN MOISTURE-EXPOSED
AND CONTROL SI PMOS DEVICES

This chapter describes results obtained on the moisture-exposed and control Si

pMOS transistors using the three-level charge pumping technique. The $1/f$ noise and

charge pumping current are analyzed before and after irradiation, and comparisons

between the border trap density and interface trap density as a function of energy are

illustrated. Changes in the trap densities as a function of energy are detected, consistent

with estimates based on $1/f$ noise measurements.

Three-Level Charge Pumping and $1/f$ Noise

Figure 24 shows the magnitude of the recombination current, I_{CP}, as a function of

step voltage, V_{STEP}, for a 3 μm × 16 μm ($L \times W$) unirradiated, moisture-exposed transistor

from wafer 28 ($t_{ox} = 68.2$ nm), generated from a three-level pulse applied to the gate, with

frequency of 15 kHz and step time of 27.4 μs. The current was measured at the body

terminal, with the source and drain grounded.

The shape of the I_{CP}-V_{STEP} curve is typical of this three-level charge pumping

method [61], [63]. The current generally increases from left to right, as the step voltage

moves from accumulation to strong inversion. When V_{STEP} places the device in strong

inversion, the interface traps have time constants shorter than t_{Low} (the falling edge of the

pulse, see Figure 8), and some traps will emit their charge before accumulation is reached

[61], [63]. A similar process occurs when V_{STEP} places the device in accumulation, except the traps are too slow to de-trap their charge, and equilibrium is not established.
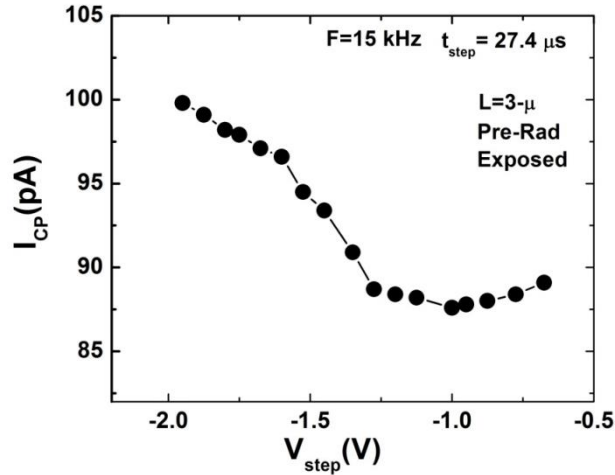
Figure 24: Recombination current I_{CP} as a function of step voltage V_{STEP} for a 3-μm length moisture-exposed pMOS transistor before irradiation. The absolute value of the current is plotted for all cases shown; the actual current is negative for pMOS devices.

However, in the region in between, the traps have time constants that satisfy Eq. (3.4), and the slope of the curve is proportional to the interface trap density, as given by Eq. (3.3).

Figure 25 shows I_{CP} as a function of V_{STEP} for varying values of (a) t_{Low} and (b) t_{High} for the device in Figure 24. All other features of the waveform remained the same during these measurements. In Figure 25(a), t_{Low} is varied from 300 ns to 1000 ns. As t_{Low} decreases, the current increases, since, from Eq. (3.4) the detectable range of time constants increases, and thus a broader range of trap levels can contribute to I_{CP} [61].
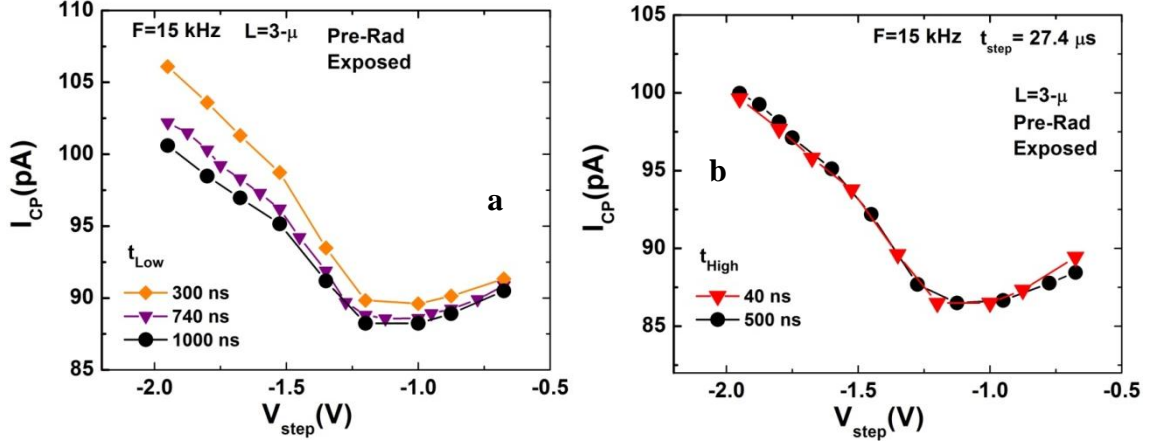
Figure 25: I_{CP} as a function of V_{STEP} for varying times of (a) t_{Low} and (b) t_{High} for the moisture-exposed pMOS transistors of Figure 24.

In Figure 25(b), I_{CP} is measured for t_{High} = 40 ns and 500 ns. There is hardly any difference between the two curves, with the exception of a slight increase in I_{CP} as V_{STEP} decreases in magnitude for t_{High} = 40 ns. As t_{High} becomes shorter, there is less time for the inversion layer charge to exit the channel before t_{STEP} is reached, and an additional current is generated, referred to as a geometric current[56], [58], [63]. This current becomes significant as V_{STEP} approaches accumulation.

Figure 26 shows the I_{CP}, as a function of V_{STEP}, for (a) L = 2 μm and (b) L = 4 μm, W = 16 μm unirradiated, control and moisture-exposed pMOS transistors from wafer 28. In this case, the frequency of the pulse was 100 kHz and the step time was 4 μs.
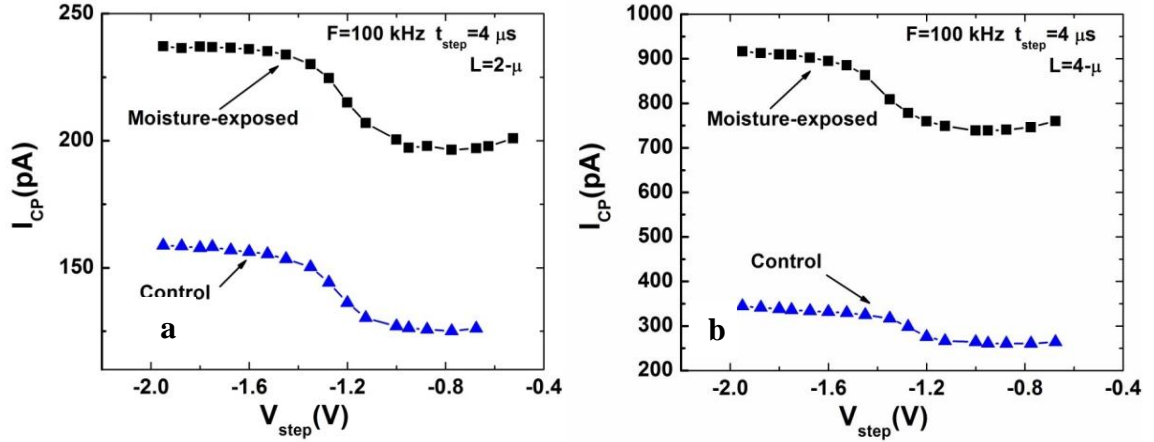
Figure 26: Recombination current I$_{CP}$ as a function of step voltage V$_{STEP}$ for (a) 2-μm and (b) 4- μm length moisture-exposed and control pMOS transistors before irradiation.

The current is much larger for the moisture-exposed devices compared to the control devices, indicating an overall larger interface trap density for the exposed devices. Additionally the current is larger for the 4-μm length devices in Figure 26(b), since I_{CP} is proportional to the gate area (Eq. (3.2)) [14], [57]-[59]. From the data in Figure 26, the slope of the curve of the moisture-exposed device is greater than that of the control device, indicating a larger density of interface traps. These results are consistent with previous work, in which it was shown that moisture exposure and aging-related effects enhance interface trap buildup in MOS devices [6]-[8].

Figure 27 shows I_{CP} as a function of step time t_{STEP} for the 4-μm moisture-exposed device of Figure 26. For values of t_{STEP} that are sufficiently long, I_{CP} will saturate as traps above the Fermi level emit all charge, and equilibrium is reached. However, for shorter values of t_{STEP}, the emission process will not fully complete before V_{LOW} is reached, resulting in a non-equilibrium condition, and Eq. (3.3) is no longer valid [60]-[63].
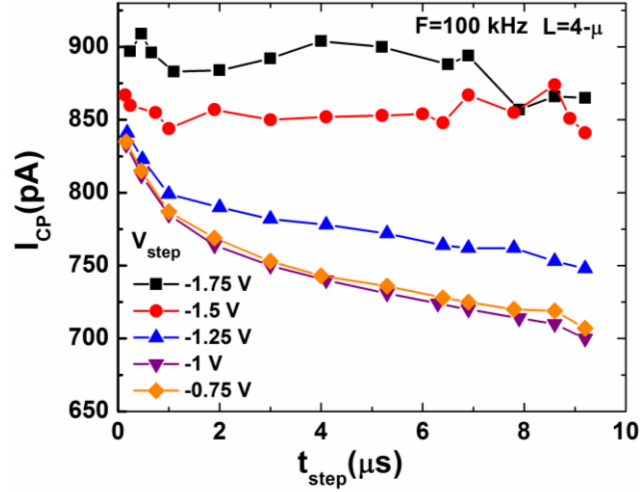
Figure 27: I_{CP} *as a function of step time* t_{STEP} *for 4- μm length moisture-exposed pMOS transistor of Figure 26.*

From Figure 27, I_{CP} decreases for increasing t_{STEP} for each value of step voltage, and begins to saturate at longer times, corresponding to an equilibrium condition, where traps above the Fermi level are empty, and those below are filled [61]. From the data in Figure 26 and Eq. (3.3), the interface trap density as a function of energy can be estimated. These results are illustrated below for the unirradiated 4-μm moisture-exposed and control devices.
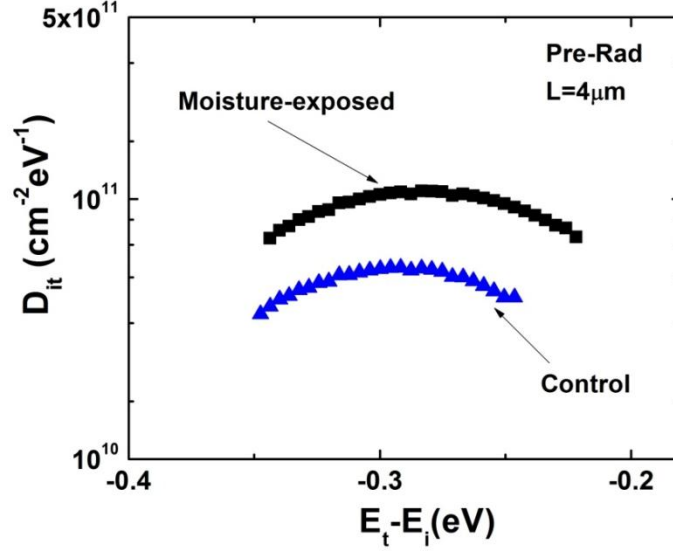
Figure 28: Interface trap density D_{it} estimated from the data of Figure 26(b) using Eq. (3.3) as a function of trap energy E_t-E_i before irradiation.

Figure 28 shows the interface trap density D_{it} as a function of trap energy E_t-E_i for the 4-μm length moisture-exposed and control pMOS devices of Figure 26(b). The trap density varies little over the energy range probed. D_{it} increases slightly with decreasing $|E_t\text{-}E_i|$ (toward midgap), then begins to decrease again. These measurements scanned a relatively small portion of the lower bandgap; however, the values of D_{it} are quite consistent with those estimated using the square-pulse charge pumping method, where D_{it} = 8.2 × 10^{10} cm^{-2}eV^{-1} for the exposed device, which provides a mean density over the entire bandgap.

For comparison to the interface trap density, Figure 29 plots S_V at 10 Hz as a function of $|V_G\text{-}V_T|$ for the 4-μm moisture-exposed and control device before irradiation. A line with slope of −2 is drawn on the graph for reference. For both devices, the slope, β, is significantly less than −2, indicating a border trap density D_{bt} that is not

uniform, but increases toward the valence band edge [10], [37], similar to other pMOS transistors in this study. This is illustrated in Figure 30.
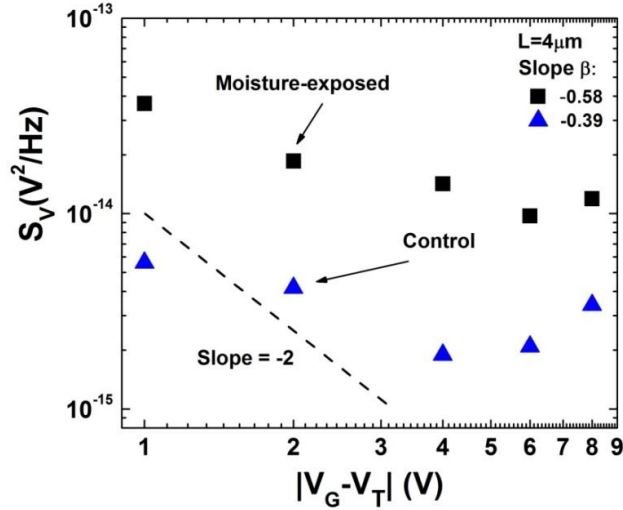
Figure 29: S_V *at 10 Hz as a function of* $|V_G\text{-}V_T|$ *for the 4-μm moisture-exposed and control device of Figure 26(b) before irradiation.*
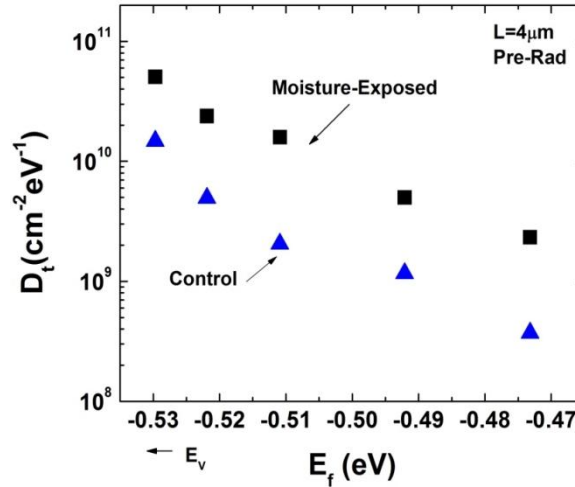
Figure 30: Border trap density as a function of energy for the devices of Figure 29.

The inferred border trap density increases with increasing energy toward the valence band edge. Furthermore, D_t varies by more than order of magnitude over the

energy range investigated, while the D_{it} estimated from three-level charge pumping varies significantly less.

After irradiation, both the interface trap and border trap distributions change significantly, for both the moisture-exposed and control devices, with the exposed device experiencing the largest changes. Figure 31 and Figure 32 illustrate these changes below. In Figure 31, I_{CP} is plotted as a function of V_{STEP} (a), and as a function of t_{STEP} (b), for the 4-μm moisture-exposed device after 100 krad(SiO$_2$) total dose irradiation. The same gate pulse that was used to produce the data in Figure 26 and Figure 27 was used here, with adjustments made in V_{HIGH} and V_{LOW} to accommodate the radiation-induced shift in threshold voltage.
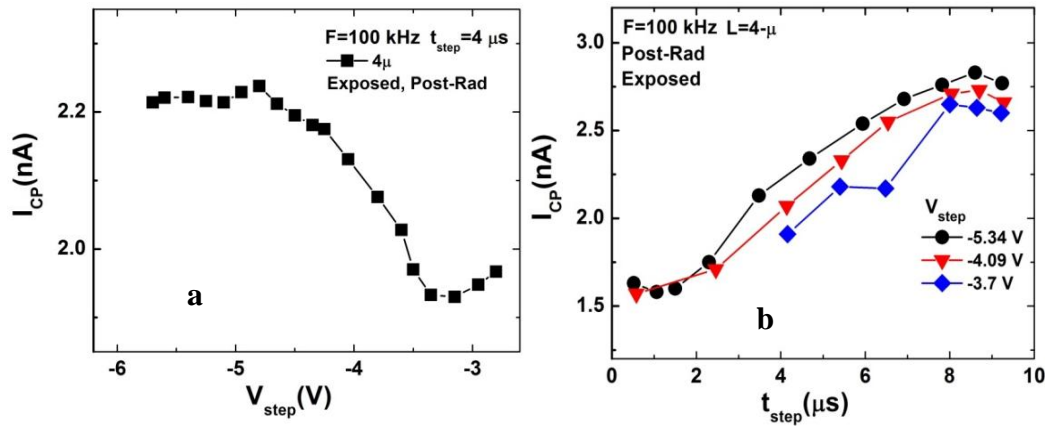
Figure 31: *I_{CP} as a function of (a) V_{STEP} and (b) t_{STEP} for the 4-μm moisture-exposed device after 100 krad(SiO$_2$) total dose irradiation.*

In addition to the increase in magnitude of I_{CP}, there is a considerable increase in the slope $\delta I_{CP}/\delta V_{STEP}$ after irradiation, indicating a significant increase in interface trap density. From Figure 31 (b), in contrast to what was observed in Figure 27 (and in contrast to what is typically observed for these measurements [62], [72]), I_{CP} now

increases with increasing t_{STEP}, and virtually no saturation occurs at all. Likely, this is due to an increase in the radiation-induced traps that are near enough to the interface to exchange charge with the semiconductor during the time scale of the measurement (border traps), and has been observed in the frequency dependence of the charge pumping current of MOS devices after irradiation [60], [73]. For a device with a large density of traps located near the Si-SiO$_2$ interface, charge may be exchanged with these traps if the trapping time constant is shorter than the duration of the device in inversion/accumulation, either directly from the silicon or indirectly via interface traps, resulting in an increase in the charge recombined per cycle ($Q_{CP} = I_{CP}/f$ theoretically is constant [58]), and thus an increase in I_{CP}. From these measurements, Eq. (3.3) cannot accurately be used to estimate D_{it} as a function of energy [60]-[63].

Figure 32 shows the post-irradiation gate-voltage dependence of the noise for the moisture-exposed device. Consistent with moisture exposure on these parts, both the noise and the slope β increase significantly after irradiation. Figure 33 plots the post-irradiation border trap density estimated from Figure 32, and the pre-irradiation border trap density for the moisture-exposed device.
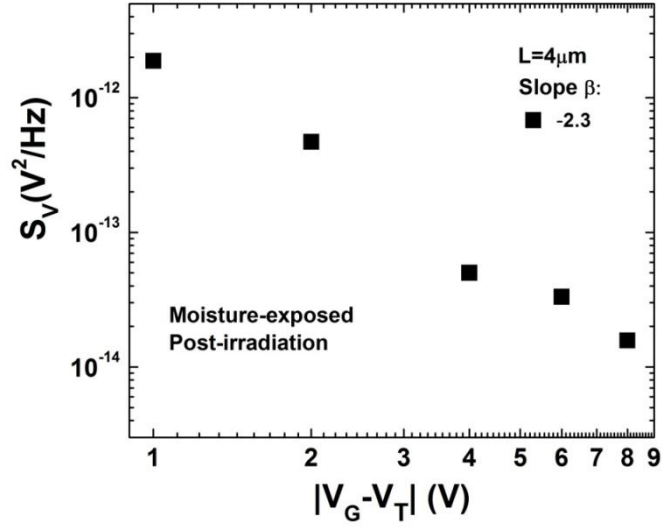
Figure 32: S_V as a function of $\left|V_G\text{-}V_T\right|$ for the 4-μm moisture-exposed device after 100 krad(SiO₂) total dose irradiation.
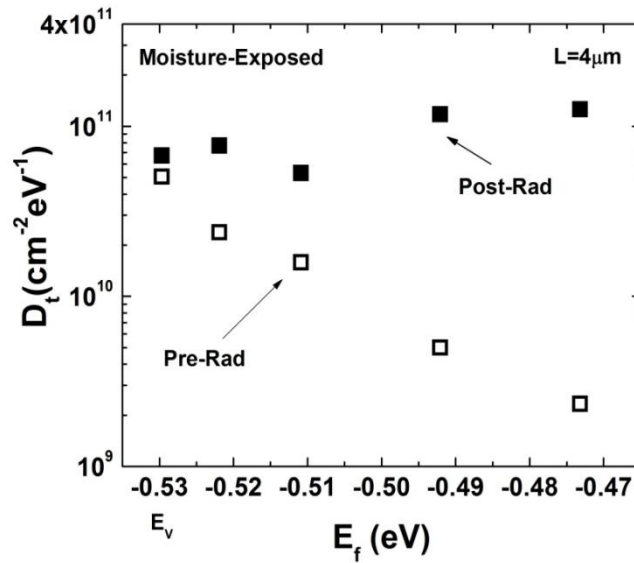
Figure 33: Border trap density as a function of energy for the 4-μm moisture-exposed device before and after 100 krad(SiO₂) total dose irradiation.

These results, combined with those of Figure 31, illustrate the changes in the trap energy distributions as a function of energy and space, for this transistor after total dose irradiation. Furthermore, some interface traps that contribute to I_{CP} can contribute to the

noise, and some "fast" border traps that contribute to the noise can contribute to I_{CP}, as most likely is the case in Figure 31(b), resulting in an abnormally increasing current with increasing step time. Therefore, these measurements can provide useful and complimentary information on the radiation-induced defects at and near the interface that contribute to device degradation.

CHAPTER 6

CHARGE PUMPING AND 1/F NOISE IN GE PMOS DEVICES

This chapter describes the 1/*f* noise and charge pumping results of irradiated Ge pMOS transistors from two different process splits. Border trap and interface trap densities are estimated from 1/*f* noise measurements, square pulse and three-level charge pumping measurements. Results demonstrate the different effects of processing on the radiation-induced charge trapping and 1/*f* noise levels, and also suggest that the noise is dominated by bulk oxide traps in the gate dielectric.

Interface Trap and Border Trap Densities

Figure 34 shows the drain current I_D as a function of V_G for a Ge pMOS transistor ($L = 5$ μm, $W = 9.8$ μm) from split D10 before irradiation, and after 100, 200, 500, and 1000 krad(SiO$_2$) total dose.
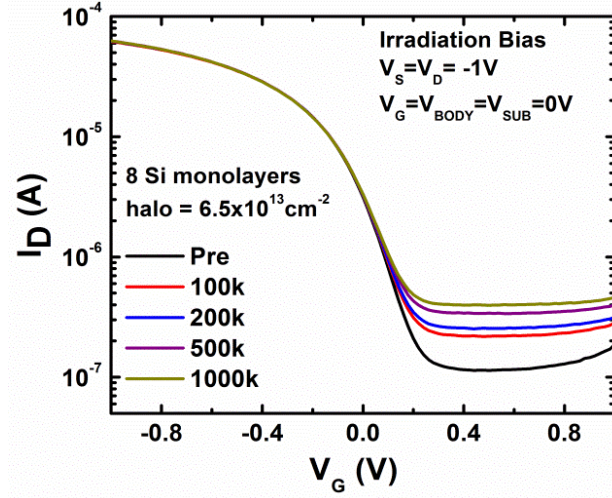
Figure 34: Absolute value of the drain current I_D as a function of gate voltage V_G, before and after total dose irradiation, after [74].

The shift in V_T with increasing total dose is extremely small. The stretch-out of the sub-threshold slope is typically proportional to the radiation-induced interface trap density [67], so the results in Figure 34 suggest there is a very small increase in interface trap density with increasing total dose. The threshold voltage shift due to interface trap charge, ΔV_{it}, is estimated to be ~ -18 mV at 1000 krad(SiO_2). This value corresponds to an increase in interface trap density ΔD_{it} of $\sim 3.2 \times 10^{11}$ $cm^{-2}eV^{-1}$. Additionally, there is an increase in the off-state leakage current with irradiation, associated with the radiation-induced leakage at the perimeter of the drain junction [20], [68].

Figure 35 shows the magnitude of the recombination current, I_{CP}, as a function of base voltage, V_{base} for a Ge pMOS transistor from split D10 with $L = 5$ μm and $W = 9.8$ μm, measured before and after total dose irradiation and 10-hour annealing using the square pulse charge pumping method. The pulse frequency was 500 kHz, with rise and fall times of 35 ns, and the base voltage (with constant amplitude of -1 V) was

incremented from −1 V to +0.5 V. The recombination current was measured at the body

terminal, with the source and drain grounded. Again, the absolute value of I_{CP} is plotted.
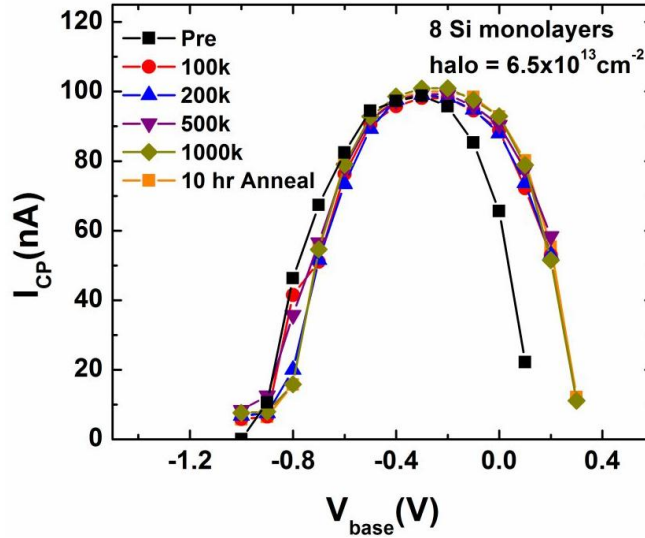
Figure 35: Magnitude of the recombination current I_{CP} as a function of base voltage V_{base} before and after total dose irradiation and 10-hour annealing. Transmission gate bias was applied during irradiation and annealing, after [74].

There is relatively little change in the charge pumping current with irradiation,

with I_{CP} increasing slightly after each dose, and remaining unchanged through the anneal.

It should be noted that, at room temperature, standard charge pumping techniques can

underestimate the total interface-trap density in Ge because traps near the band edges are

not measured [14]. At lower temperatures, the electron and hole emission levels move

closer to the band edges, [14], [69], and a wider portion of the band gap can be measured.

For all the parts investigated from split D10, relatively small increases in the

charge pumping current were observed with increasing total dose. From Eq. (3.2) and the

data in Figure 35, D_{it} is estimated to be ~4.6×10^{12} cm^{-2}eV^{-1} before irradiation and ~$4.7 \times$

10^{12} cm^{-2}eV^{-1} after 1000 krad(SiO$_2$). This corresponds to an increase of ~$1.0 \times$

10^{11} cm^{-2}eV^{-1} with irradiation, which is less than the estimate of the radiation-induced

interface trap density from the midgap method in Figure 34. This suggests a portion of the stretch-out in the I_D-V_G characteristics may be caused by border traps [49], [70]; additionally, non-uniformities in either trapped oxide charge or in $D_{it}(E)$ can contribute to this difference.

Figure 36 shows S_V as a function of frequency for a Ge pMOS transistor from split D10, measured before and after total dose irradiation and 10-hour annealing. Here, V_G−V_T = −0.8 V and V_D = −100 mV. The frequency exponent α remained between 1 and 1.1 for all devices during each measurement, indicating that the traps contributing to the noise are nearly constant in energy and space [1], [3], [10], [39].
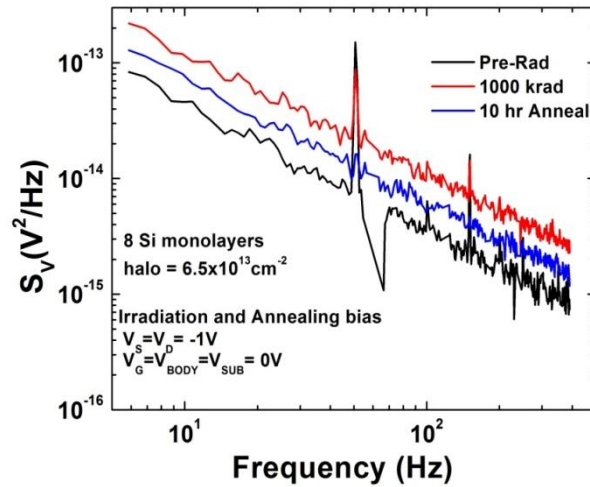
Figure 36: S_V as a function of frequency, before and after total dose irradiation and 10-hour annealing at V_G−V_T = −0.8V and V_D = −100 mV. Transmission gate bias was applied during irradiation and annealing [74].

In contrast to the small changes in I_{CP} observed in Figure 35, the noise increases significantly with total dose irradiation, and decreases after annealing. This suggests a potentially large increase in border-trap density [3], [49], [54], [70]. From Eq. (2.2) and the noise data shown in Figure 36, the pre-irradiation border trap density $D_{bt}(E_f)$ is

estimated to be $\sim 6.9 \times 10^{12}$ cm^{-2}eV^{-1}. After 1000 krad(SiO$_2$) irradiation, D_{bt} increases to a value of $\sim 1.3 \times 10^{13}$ cm^{-2}eV^{-1}, and then decreases to $\sim 1.1 \times 10^{13}$ cm^{-2}eV^{-1} after annealing. This corresponds to an estimated increase in border trap density of $\sim 5.7 \times 10^{12}$ cm^{-2}eV^{-1} after 1000 krad(SiO$_2$) total dose irradiation. Hence, the increase in border traps is much larger than the increase in interface traps, for the devices with eight Si monolayers.

Figure 37 shows (a) I_{CP} as a function of V_{base} and (b) S_V as a function of frequency at $V_G - V_T = -0.8$ V and $V_D = -100$ mV, for a device from split D05, $L = 5$ μm and $W = 9.8$ μm, before and after 1000 krad(SiO$_2$) total dose irradiation and 12-hour annealing.
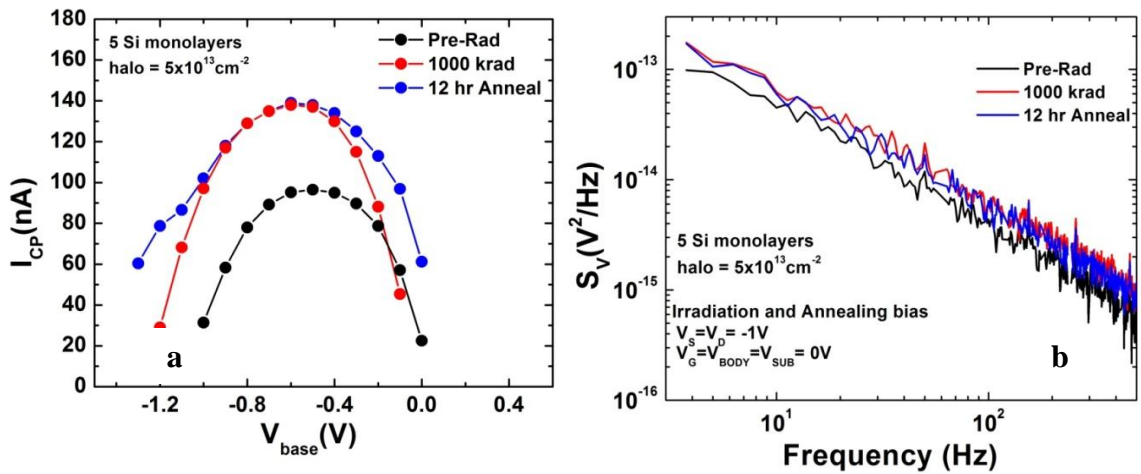
Figure 37: (a) I_{CP} as a function of V_{base} and (b) S_V as a function of frequency, before and after total dose irradiation and 12-hour annealing, after [74].

For the devices with five Si monolayers, the increase in charge pumping current is greater than that observed for the devices with eight Si monolayers, indicating relatively more radiation-induced interface traps, and the increase in noise is less than observed for the devices with eight Si monolayers, indicating fewer radiation-induced border traps.

There is also a negative shift in the I_{CP}-V_{base} curve after irradiation, indicating an increase in radiation-induced bulk oxide-trap charge.

Figure 38 shows the effective densities of border traps, D_{bt}, and interface traps, D_{it}, estimated from the noise and charge pumping data in Figure 37, respectively. The border trap density and interface trap density increase nearly the same amount after 1000 krad(SiO$_2$) total dose irradiation. However, the noise decreases after annealing, while the interface trap density remains approximately constant. These results are qualitatively consistent with the results of [15], where devices with the lowest halo implantation doses exhibited the smallest increases in noise after irradiation, and devices processed with fewer Si monolayers exhibited enhanced oxide and interface trap charge buildup. We note that low-frequency noise results from split D05 with eight Si monolayers were not included in [15].
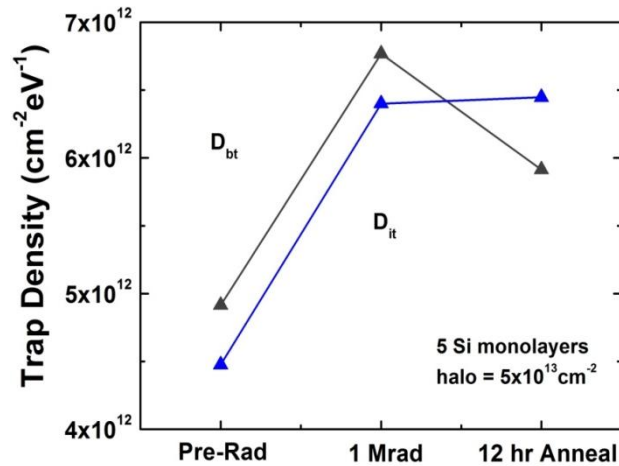
Figure 38: Effective densities of border traps D_{bt} and interface traps D_{it} before and after1000 krad(SiO$_2$) total dose irradiation and 12-hour annealing, after [74].

The results of Figure 36-Figure 38 suggest that different mechanisms are involved in the different irradiation responses of the noise and charge pumping current. Specifically, the noise is most likely dominated by bulk traps in the HfO_2 dielectric layer [16], [18], rather than by interface traps located either directly at the Si/SiO_2 interface or in the ultrathin SiO_x layer that lies between the Ge channel and the HfO_2 passivation layer. The bulk HfO_2 trapped charge densities are enhanced significantly during irradiation, and decrease with annealing [15], while the interface trap density increases with irradiation, and changes very little with annealing [15], [71].

Energy Dependence of Trap Densities

To investigate the energy dependence of the traps contributing to the $1/f$ noise, S_V was measured as a function of $|V_G-V_T|$ for the D05 devices of Figure 37, before and after 1000 krad(SiO_2) total dose irradiation and 12-hour annealing. Here, $V_D = -100$ mV, and V_G-V_T varies from -0.3 V to -0.8 V. These results are illustrated in Figure 39.
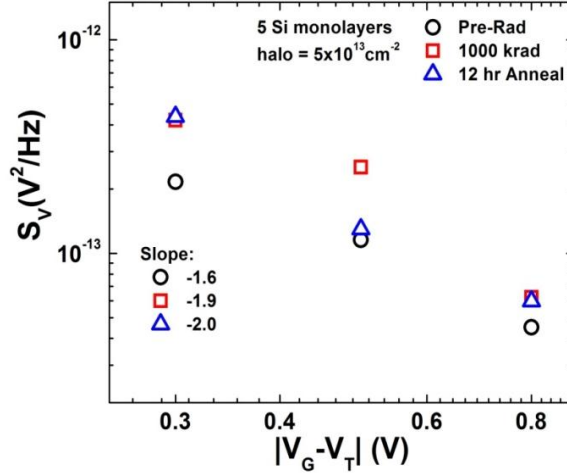
Figure 39: S_V at 10 Hz as a function of $\left| V_G - V_T \right|$ before and after 1000 krad(SiO$_2$) total dose irradiation and 12-hour annealing, after [74].

Prior to irradiation, the slope of the data, β, is ~ -1.6. After irradiation, β increases, and then increases again with annealing. For these parts, in the energy range investigated, the pre-irradiation slope is less than -2, indicating a trap distribution that is increasing toward the valence band edge, consistent with what is often observed for pMOS devices on Si [10], [37]. However, after irradiation and annealing, the data suggest a more uniform trap distribution. All parts from all splits investigated exhibited similar dependences.

The three-level charge pumping technique was used to investigate the interface trap density as a function of energy. The gate pulse had a frequency of 500 kHz, and rise and fall times of 90 ns, while V_{STEP} or t_{STEP} were varied. Figure 40 shows I_{CP} as a function of step voltage V_{STEP} for the device of Figure 37, before irradiation, after 1000 krad(SiO$_2$) total dose irradiation, and after 12-hour annealing.
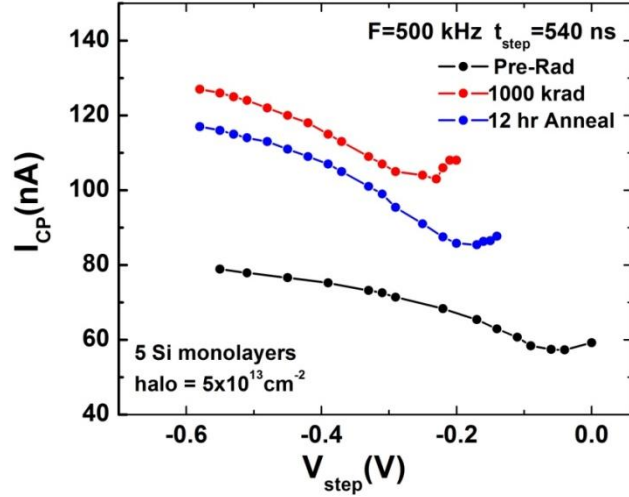
Figure 40: I_{CP} as a function of step voltage V_{STEP} before and after1000 krad(SiO$_2$) total dose irradiation and 12-hour annealing, after [74].

There is a shift in the I_{CP} curves after irradiation and annealing similar to what is observed in Figure 37(a), consistent with radiation-induced hole trapping. The magnitude of the current increases with irradiation and then decreases with annealing. The slope of the curve, $\delta I_{CP}/\delta V_{STEP}$, increases after irradiation, and then increases further after annealing, indicating an increase in interface trap density.

Figure 41 shows I_{CP} as a function of step time t_{STEP} for different values of step voltage. For the pulse frequency used in these measurements, I_{CP} saturates, up to and shorter than the t_{STEP} value used for the data produced in this work, indicating that equilibrium is established during these step times and at these particular step voltages [60], [61]. This occurs when traps above the Fermi level corresponding to V_{STEP} are empty, and those below it are occupied, and empty only by electron capture, thus recombining and contributing to I_{CP}. This confirms that we can use the three-level charge pumping measurements and Eq. (3.3) to estimate the energy distributions of interface traps in these devices [60]-[63].
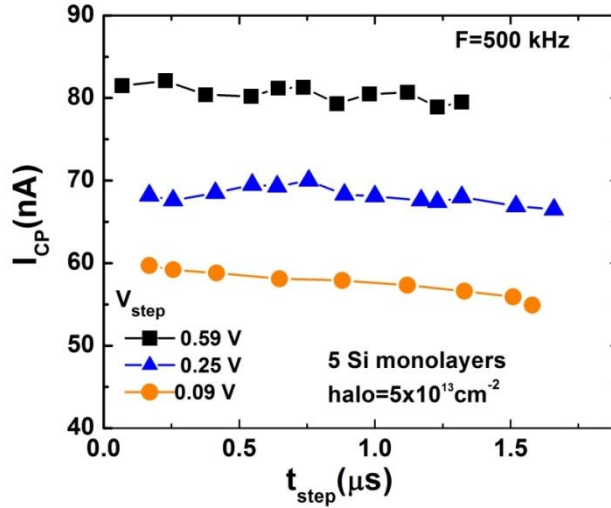
Figure 41: I_{CP} as a function of step time t_{STEP} for different values of V_{STEP}, prior to irradiation, after [74].

To compare the border trap and interface trap density distributions, D_{bt} and D_{it} from three-level charge pumping (3LCP), and D_{it} from square pulse charge pumping (SPCP), are plotted as a function of trap energy $E_t - E_i$, before and after 1000 krad(SiO$_2$) total dose irradiation and after 12-hour annealing in Figure 42.

The values of D_{it} estimated from the square pulse method represent the mean density of interface traps measured across the band gap; however, for illustrative purposes, these data points are placed at midgap (where the most effective trapping occurs). The border trap density is estimated from the data in Figure 39 using Eq. (2.2) and a smooth fit to the data, and the interface trap density is estimated from the data in Figure 40 using Eq. (3.3). The values corresponding to $V_G - V_T = -0.8$ V are indicated on the graph. During the noise measurements, the applied gate voltage was such that the device was operating from moderate to strong inversion, while D_{it} from three-level charge pumping was calculated from an interval of data spanning depletion to weak

inversion. The shape of D_{it} estimated from three-level charge pumping is very similar throughout the irradiation and annealing sequence. The density of interface traps increases gradually as energy decreases, and then levels off, and begins to decrease slightly.
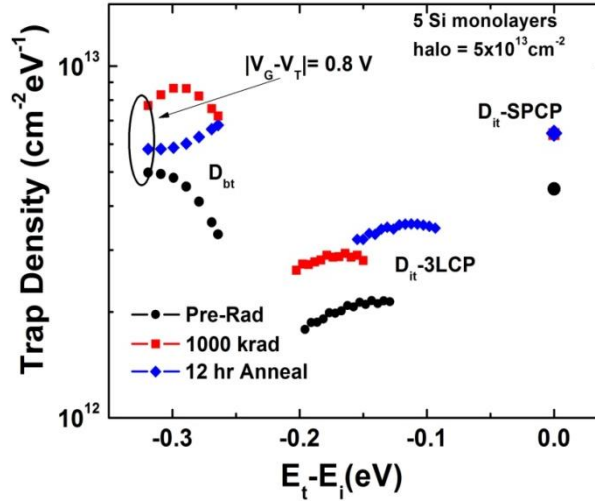
Figure 42: D_{bt}, D_{it} from three-level CP, and D_{it} from square pulse CP, as a function of trap energy E_t-E_i before and after total dose irradiation and 12-hour annealing, after [74].

D_{it} estimated from the three-level charge pumping differs from the values obtained from the square pulse method, providing additional insight into the interface trap densities for this device. Not only are the trap densities smaller in magnitude than the values estimated from the square pulse method, but also increase beyond the post-irradiation values with annealing, while D_{it} from square pulse changes little with annealing. These differences occur because, from the square pulse method, D_{it} is estimated from the peak recombination current, which occurs when the voltage range of the pulse sweeps from below flat band to above threshold, while, during the three-level technique, V_{STEP} controls the upper boundary of the region contributing to I_{CP}. Therefore,

the interface trap density that is estimated from I_{CP} sweeps a smaller portion of the band gap than the region accessed during the square pulse method. These combined results demonstrate that the interface-trap density can vary significantly with energy across the Ge band gap.

In contrast to D_{it}, the energy dependence of the border trap density inferred from the $1/f$ noise measurements differs significantly, both in magnitude and distribution, as illustrated in Figure 42. The pre-irradiation border trap density increases rapidly with increasing $E_t - E_i$ toward stronger inversion. After irradiation, D_{bt} becomes roughly peaked, and after annealing tends to decrease with increasing energy, but overall varies much less over the measured energy range. Of course, traps with differing microstructure, located in different regions of the device, are being measured over different energy ranges in the band gap. Nonetheless, these measurements provide useful and independent information about the different trap densities in these devices, and how each varies with energy. The border traps that lead to the noise are likely located in the near interfacial SiO_2 and bulk HfO_2, while the interface traps are located at the Ge/SiO_2 interface.

CHAPTER 7

CONCLUSIONS

This work has focused on the characterization of defects that lie at or near the semiconductor-oxide interface of MOS transistors using 1/f noise measurements and charge pumping measurements. The frequency and gate-voltage dependences of the noise were investigated for moisture-exposed and control Si nMOS and pMOS transistors before and after irradiation. For the nMOS devices, moisture exposure did not significantly enhance or change the noise after irradiation compared to control devices. For the exposed pMOS parts, significant changes in the noise, and hence, border trap density, were observed, both through changes in the frequency dependence and gate-voltage dependence of the noise. Control pMOS devices exhibited similar responses, but to a lesser degree, presumably due to aging-related effects. The temperature dependence of the noise was also investigated for the moisture-exposed and control pMOS parts. Qualitatively different temperature dependences were observed for moisture-exposed and control devices; changes in the temperature dependence and gate-voltage dependence of the noise were observed after irradiation for the exposed device, reflecting changes in the trap distributions.

Three-level charge pumping measurements, in conjunction with noise measurements, were used to probe the interface and near-interfacial trap densities of these pMOS devices before and after irradiation. The two methods provide complementary and consistent estimates of interface trap and border trap densities. In particular, for the exposed device, enhanced radiation-induced border trap densities were

observed through an increase in the charge recombined charge per cycle, consistent with the increased noise and the change in gate-voltage dependence of the noise.

The techniques described above were applied to Ge pMOS transistors in a similar manner, to gain insight into the properties of the semiconductor/gate-dielectric interface, and to determine the effects of processing on the defects within that region. The number of silicon monolayers and the halo implantation dose strongly affect the radiation response and $1/f$ noise levels of these devices. In addition, significantly different border trap and interface trap energy distributions were estimated via $1/f$ noise and charge pumping measurements, strongly suggesting that the noise in these devices is not dominated by defects in the near-interfacial SiO_2 layer, but rather by bulk oxide traps in the dielectric layer.

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