UPSET TRENDS IN FLIP-FLOP DESIGNS AT DEEP

SUBMICRON TECHNOLOGIES

By

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# CHAPTER I

## INTRODUCTION TO SEE

**S**ingle-event effects (SEE) in microelectronics are caused when highly energetic particles pass through a semiconductor material creating electron-hole pairs (EHPs) (figure 1) along its strike path until it has lost all its energy or left the semiconductor. The particle strike may cause a soft-error (e.g. transient disruption of circuit operation, change of logic state) or even permanent damage to the device (hard-error), based on factors such as circuit topology and amount of charge collected. [1, 2]
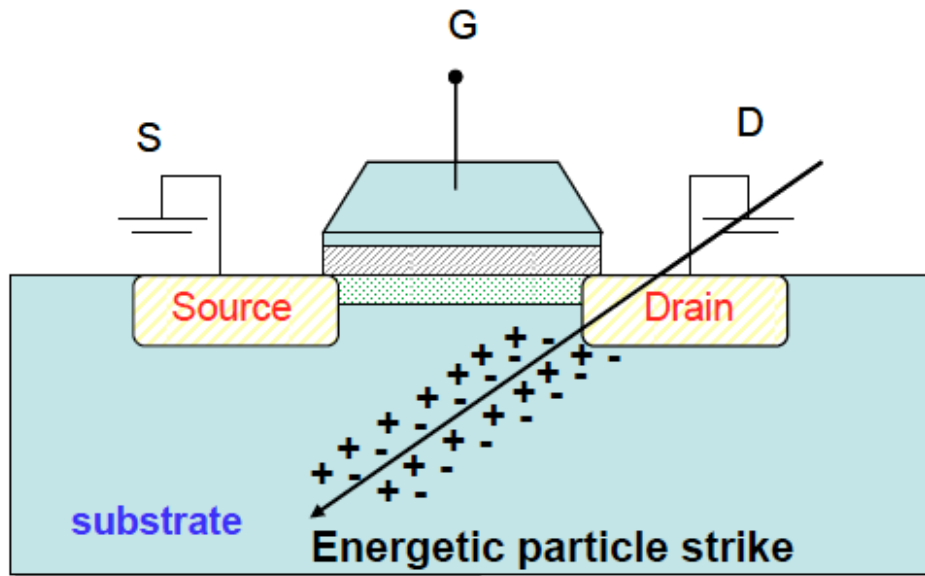


Figure 1: A particle strike generating electron-hole pairs in the device. [3]

In case of the soft-error, the SE results in data corruption while the device remains intact. Hence, the erroneous data can be corrected by writing new data. On the other

hand, a hard-error occurs when the SE causes physical damage to the device is physically damaged resulting in permanent data loss.
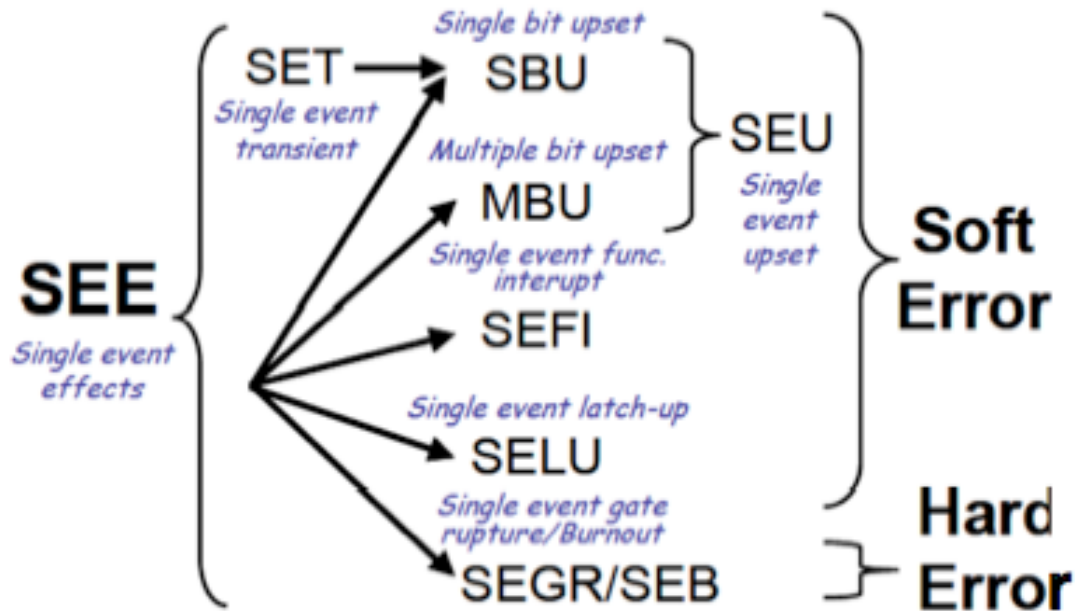
Figure 2: Basic classification of Single-event effects [4]

A single event transient (SET) is a transient voltage pulse created due to a single event (SE) at a node in an integrated circuit. Under certain conditions, this transient pulse can propagate through the integrated circuit and eventually appear at the circuit's output. It may also be captured if it appears at the input of the latch during the setup and hold time of the latch (also known as window of vulnerability). A SET, thus captured, becomes a single event upset (SEU) (figure 3). [5]

An SEU can also be generated within a latch when a radiation event causes enough charge to be collected at a sensitive node in the latch. The minimum charge required to

flip the state of the latch is termed as critical charge ($Q_{crit}$). $Q_{crit}$ is a property of the particular circuit and depends on factors such as individual transistor currents and nodal capacitances.
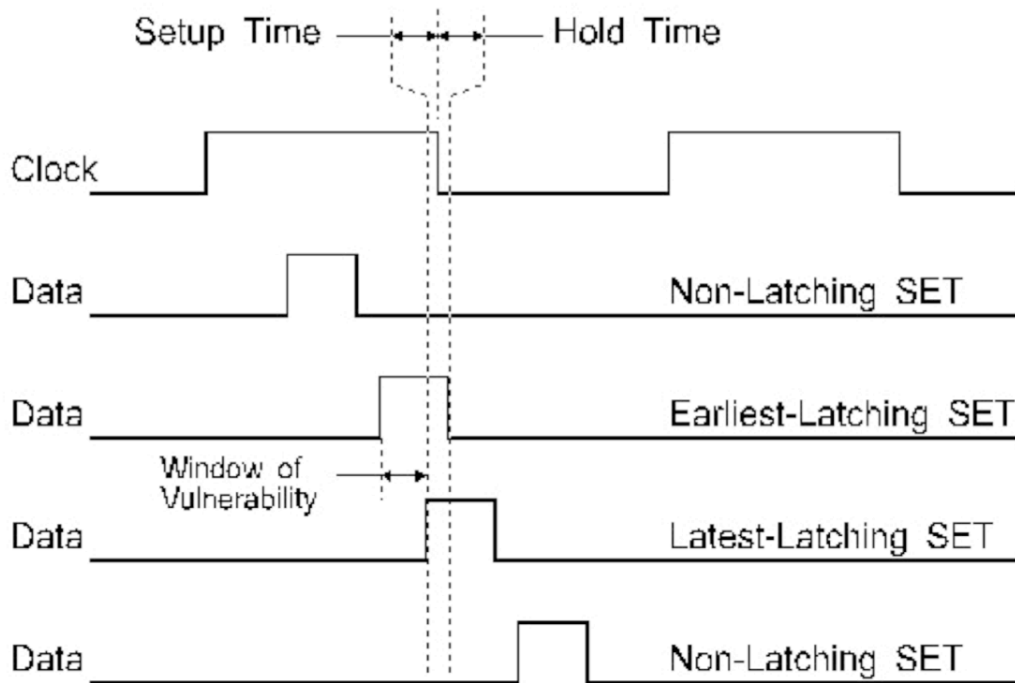


Figure 3: An illustration showing latching of a transient pulse [6]

There are various soft-error mitigation techniques that can be implemented at the device, circuit and architecture levels. For instance, triple-well and silicon-on-insulator technologies are effective mitigation strategies at the device level, Triple Mode Redundancy (TMR) [7] and Dual Interlocked Cell (DICE) [8] are mitigation techniques at the circuit-level whereas error correcting codes (ECC) and redundant execution are some of the soft-error mitigation schemes at the architecture-level.

# CHAPTER II

## BACKGROUND ON SEE & SCALING

Advances in fabrication technologies for semiconductor integrated circuits (ICs) have resulted in rapidly shrinking technology node and aggressive scaling of voltage. This has resulted in an increase in the probability of soft-errors in advanced CMOS digital logic circuits.

In most modern microprocessors large memory arrays such as caches or register files are protected Error detection and correction (EDAC) schemes. As a result, the chip level soft error rates (SER) are dominated by the error rates of the flip-flops in the microprocessor. [9]

### $Q_{crit}$ scaling

The critical charges of the sequential nodes approximately scale according to

$$Q_{crit} \approx V_{cc} \times C \qquad (1),$$
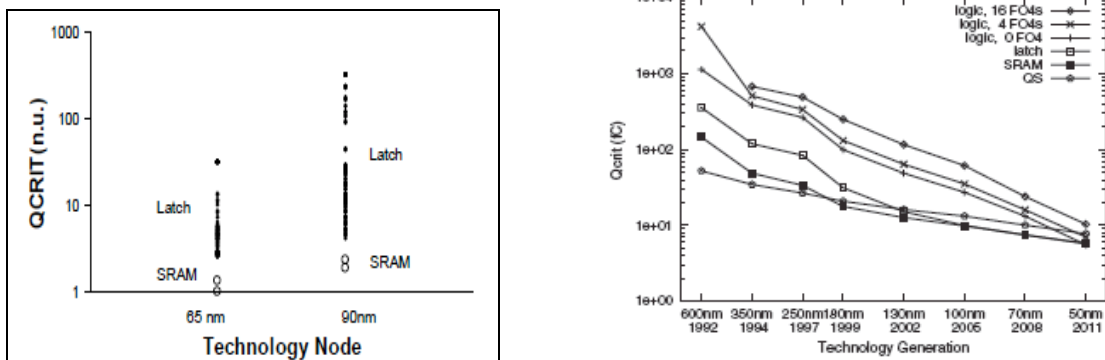


Figure 4: (a) $Q_{crit}$ of latches and SRAM plotted for all transitions and state nodes. [9] (b) $Q_{crit}$ decreases with feature size [10]

In (1), $V_{cc}$ equals the power supply voltage, and C denotes the node capacitance. Scaling is known to decrease both $V_{cc}$ and C. Hence, $Q_{crit}$ is also expected to decrease as a result of technology scaling [9] and is a cause of concern as technology advances into nanometer technology (figure 4). Trends in $Q_{crit}$ scaling for flip-flops will be revisited in Chapter 3.

SER scaling

$$SER = \kappa A_{diff} \exp(-Q_{crit}/\eta) \tag{2},$$

where $A_{diff}$ is the sensitive drain diffusion area, $Q_{crit}$ is the critical charge, $\kappa$ denotes an overall scaling factor and $\eta$ is the charge collection efficiency[11, 12]. Technology scaling affects factors governing the SER such as the sensitive drain diffusion area, $A_{diff,}$ and the critical charge, $Q_{crit}$. Since scaling reduces both $Q_{crit}$ and the efficiency, $\eta$, there have been inconsistencies concerning the experimental data on SER for latches / flip-flop in some of previous research in this area, as illustrated in figure 5. These inconsistencies can be attributed to the variation is the design of the latch considered in each of these experiments.
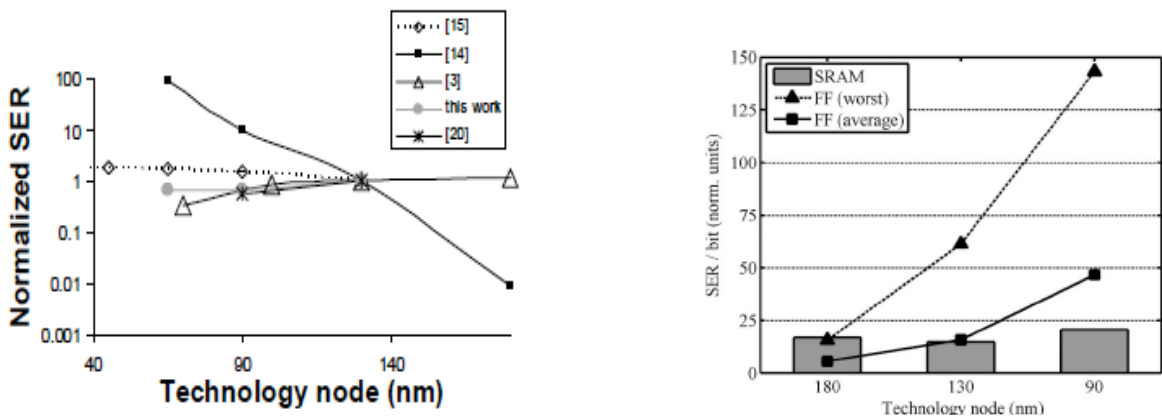


Figure 5: Impact of technology scaling on Soft error rate of flip-flops [9, 12]

Charge sharing
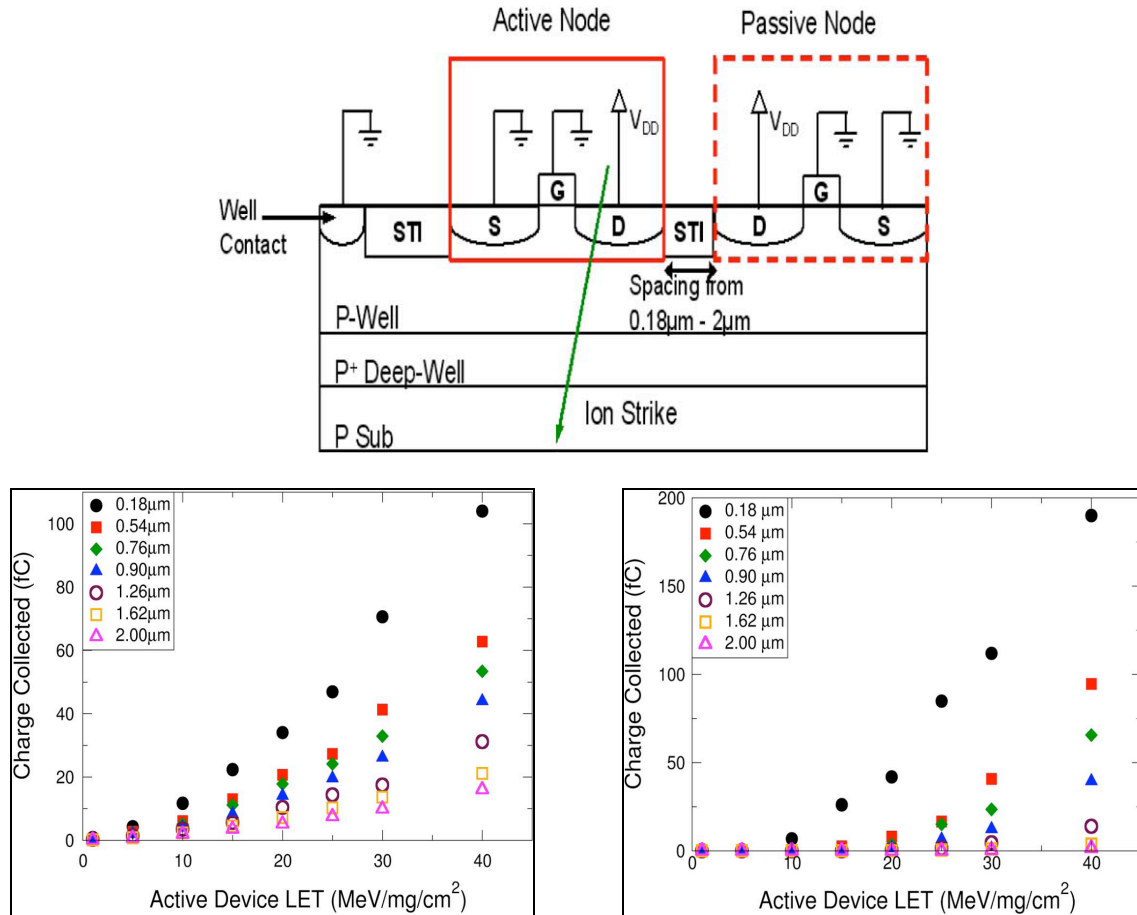


Figure 6: Illustration showing (a) nodal separation between two devices (b) charge sharing between two PMOS devices (c) charge sharing between two NMOS devices [13]

Decreasing technology feature size has resulted in higher packing densities. As a result of this, charge generated by a single particle strike may be collected at multiple nodes [14]. This multiple node charge collection may have an increasing impact on the vulnerability of the circuit to single-events as devices are scaled down. Charge sharing studies by Amusan *et al* showed that the main mechanism for charge sharing in PMOS devices is the parasitic bipolar transistor; while in the case of NMOS devices it is diffusion. [13]

In the case of SRAM if the radiation event is of a very high energy, more than a single bit maybe affected, creating a multi-bit upset (MBU). Decreasing feature sizes have resulted in smaller cell sizes in SRAM and hence the probability of MBU is increasing as shown in figure 7.
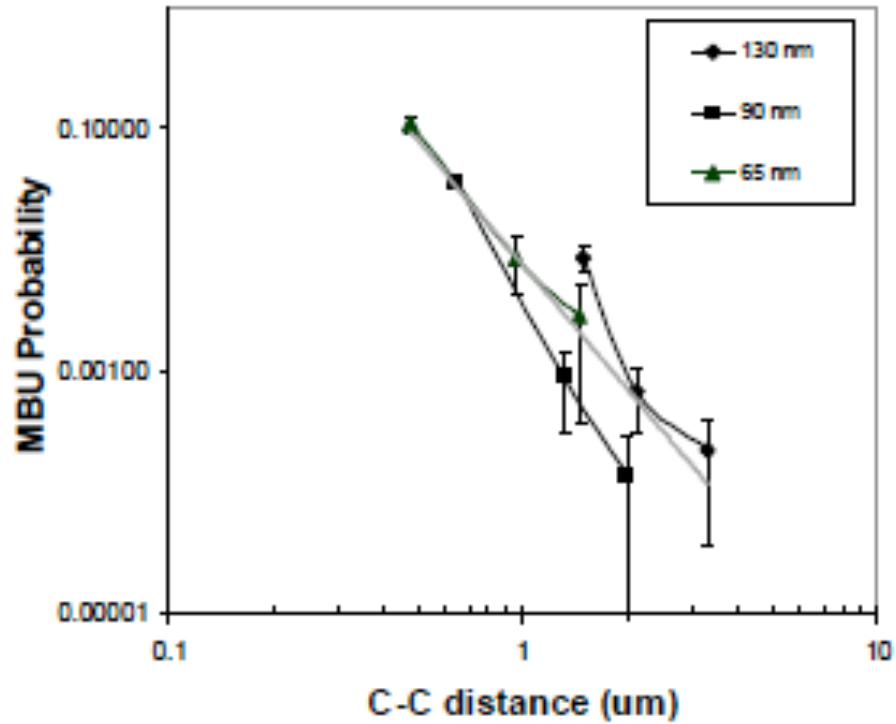


Figure 7: Probability of MBU increases as inter-cell (C-C) distance reduces [9]

Mitigating SEU will become more complex as many traditional design approaches to mitigate soft errors, such as the DICE, are based on the assumption that an incident particle affects only one circuit node. The DICE latch has been shown to be vulnerable to SEU at low LET when multiple nodes of the latch collect charge. [15]

This work focuses on investigating the effects of $Q_{crit}$ scaling and multi-node charge collection on the SER trend, keeping the design geometry constant across the technology nodes considered. Chapter III of the thesis discusses the trends in critical charge for

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upsets occurring due to single and multiple-node charge collection. Chapter IV describes the Monte Carlo simulations that have been carried out in order to study the probability of upsets in the flip-flop and how technology scaling affects this probability.

# CHAPTER III

# CRITICAL CHARGE TRENDS

<u>Flip-flop designs</u>

Four different flip-flop designs with varying levels of area, power, speed, and soft-error hardness were considered for this study. The flip-flops designs, as shown in figure 9, are:

(a) Conventional master-slave D flip-flop design (MS DFF),

(b) A low-power version of the D flip-flop design (LPFF).

(c) SEU-tolerant master-slave Dual-Interlocked Cell flip-flop (MS DICE FF) [8],

(d) A master-slave flip-flop, with an 8T storage cell (Q8FF),

The MS DFF has two storage nodes each stage, which form a complimentary pair. The LPFF has the same number of storage nodes as the DFF. The DICE design consists of cross-coupled inverters. Each stage of the design has four storage nodes, two of which are redundant. A voltage transient on one storage node requires a large amount of time to propagate through the remaining three storage nodes and as a result, the three storage

TABLE 1. POWER AND DELAY OF THE FLIP-FLOPS NORMALIZED W.R.T DFF

| Flip-flop | No. of transistors | 45 nm | | 65 nm | | 90 nm | |
|---|---|---|---|---|---|---|---|
| | | max. C-Q delay | Power | max. C-Q delay | Power | max. C-Q delay | Power |
| LPFF | 28 | 0.64 | 0.90 | 0.68 | 0.88 | 0.92 | 0.83 |
| DFF | 20 | 1 | 1 | 1 | 1 | 1 | 1 |
| DICE | 40 | 1.38 | 2.23 | 1.26 | 1.87 | 1.11 | 2.65 |
| Q8FF | 40 | 1.55 | 1.34 | 1.24 | 2.10 | 1.41 | 1.64 |

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nodes restore the flip-flop's state to normalcy. Hence, the DICE design is considered immune to upset when only one of the storage nodes is perturbed [15].



(a)



(b)

(c)
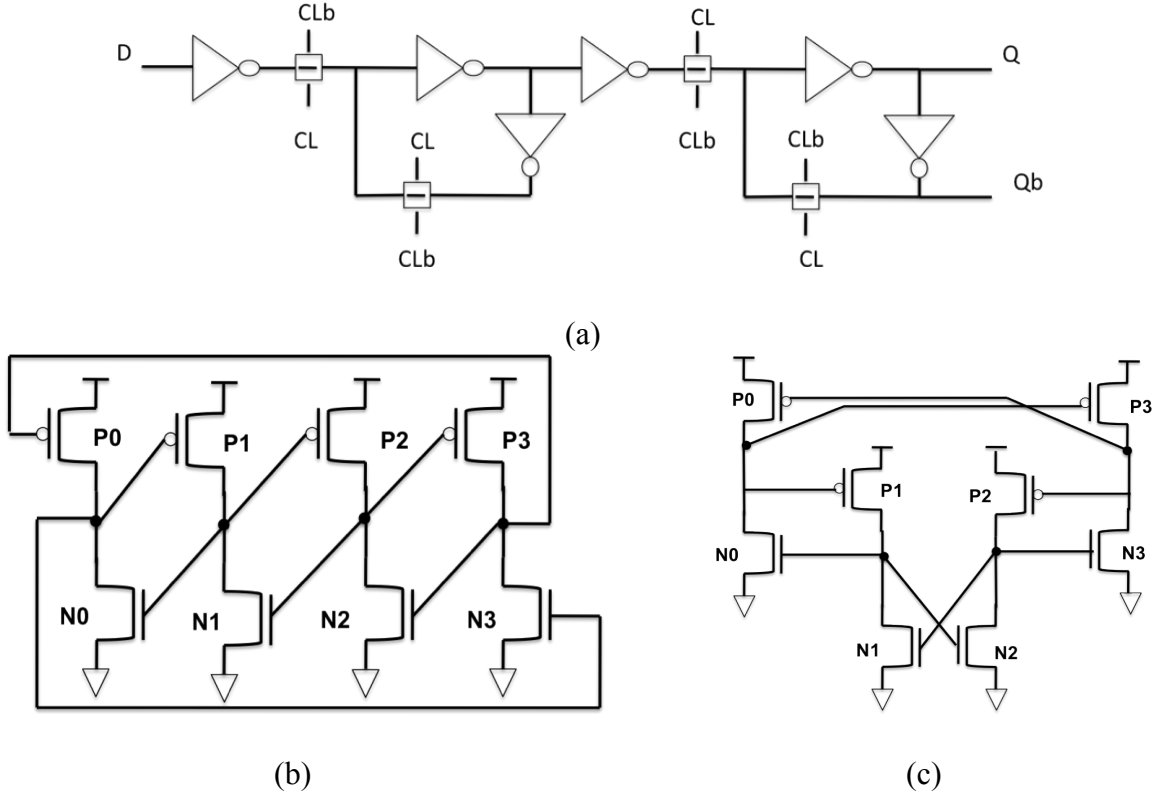
Figure 8: (a) MS DFF (b) one stage of the DICE flip-flop (c) 8T storage cell of Q8FF

The Q8FF also, same as DICE, has four storage nodes per stage including two redundant nodes. However, the Q8FF is coupled differently than the DICE flip-flop. The power and delay of the flip-flops, normalized with respect to the DFF for each technology node considered, are given in Table 1. The max. C-Q delay refers to the clock to Q delay in the flip-flops and is the maximum delay observed over both stages of the flip-flop and both states of the data (i.e., Data = HIGH and Data = LOW).

SEU due to single-node charge collection

Circuit-level simulations of the designs were carried out using Cadence® Virtuoso® Spectre® Circuit Simulator tool [16]. The Spectre® Circuit Simulator provides accurate and detailed transistor-level SPICE-level analysis of analog and digital circuits.

The flip-flop designs were simulated in three different technologies, namely IBM 90nm, IBM 65nm and TSMC 45nm technologies. The FET model used in these PDK was BSIM4. Sensitive nodes in the flip-flop, upon sufficient charge collection (a.k.a. critical charge), will cause the circuit to erroneously flip its state. To identify such sensitive nodes and estimate their critical charge ($Q_{crit}$), charge was deposited on each node in the circuit by connecting a current source based on 3D TCAD simulations [17], to the node in consideration. The shape of the current pulse is illustrated in figure 9(a). The charge deposited on a node was varied until an upset was observed; the amount of charge for which an upset occurred is the $Q_{crit}$ for that node. The sensitive nodes and the vulnerable transistors of one stage of the DFF for Data = 'HIGH' is shown in figure 9(b).



(a)                                                                (b)
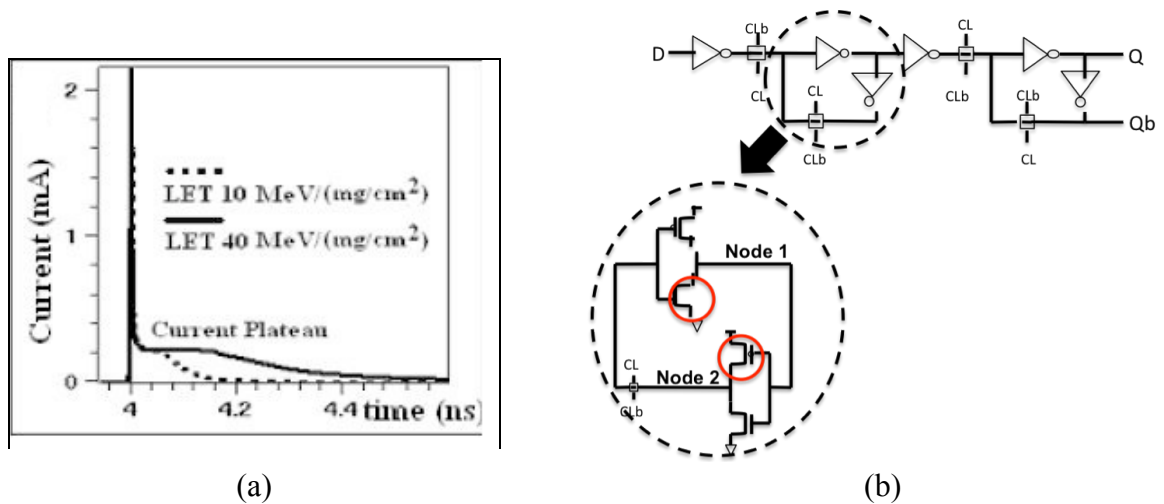
Figure 9: (a) shape of the current source [17] (b) Sensitive nodes and vulnerable transistors in one stage of the DFF
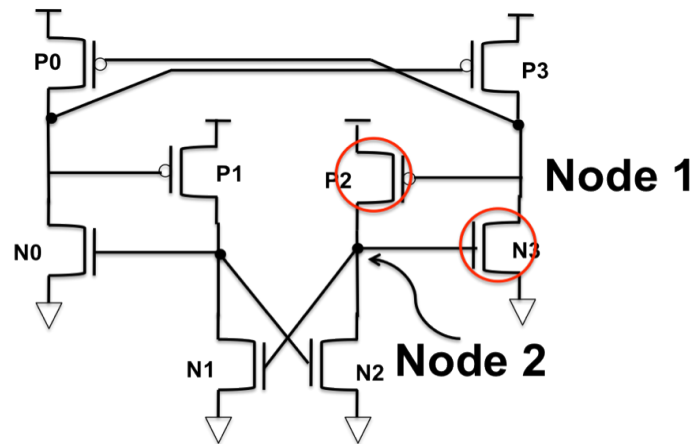
Figure 10: Sensitive nodes and vulnerable transistors of Q8FF
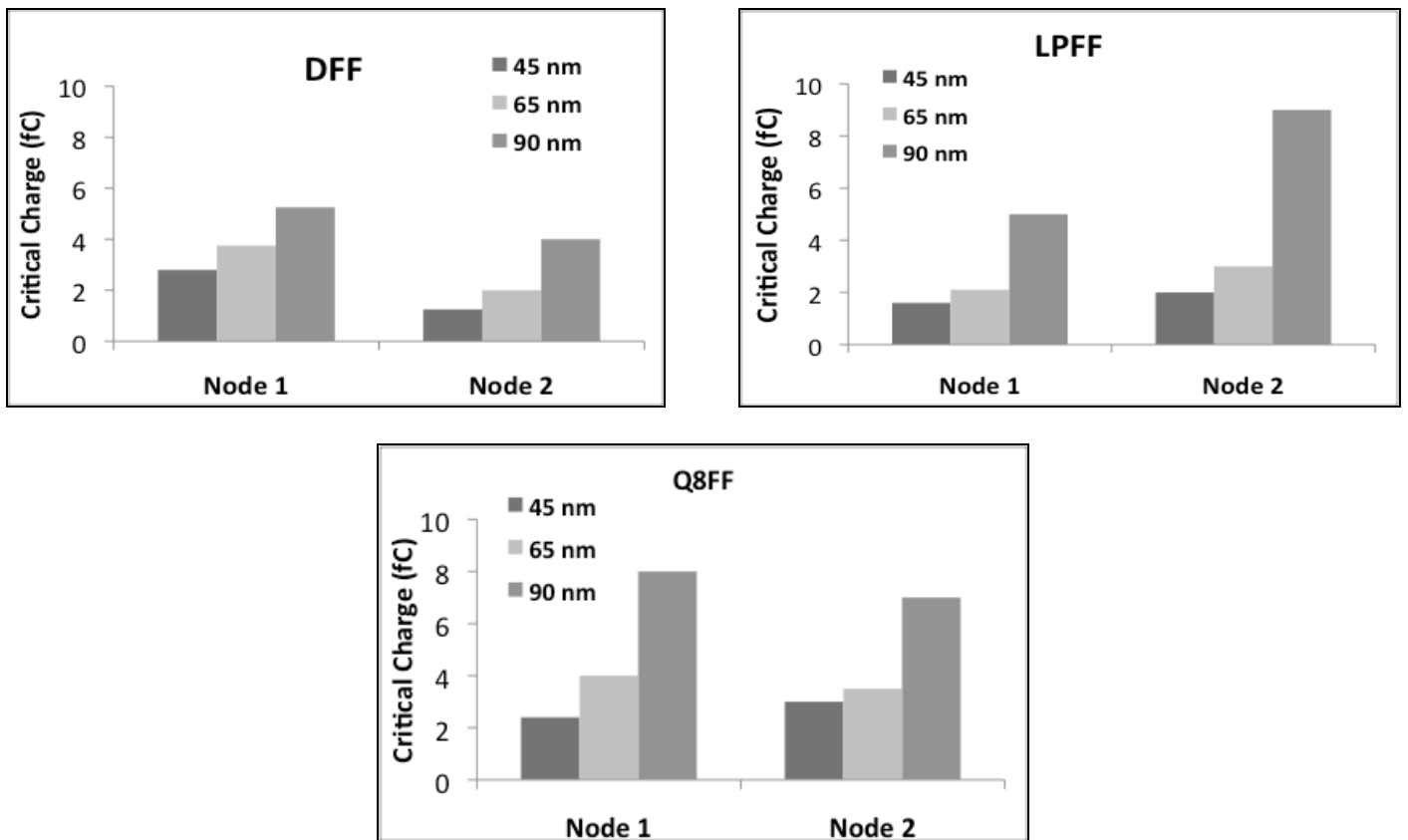


Figure 11: $Q_{crit}$ for one stage of DFF, LPFF and Q8FF

In the Q8FF, only two of the four nodes of the storage cell were found susceptible. The sensitive nodes of Q8FF for Data = 'HIGH' and their $Q_{crit}$ values are shown in figure 12. The DICE flip-flop, being a radiation-hardened design, did not show any upsets due to charge deposition on a single node for a large range of deposited charge. Figures 11 & 12 indicate that the critical charge decreases as technology scales. This is consistent with previous findings of [9, 10], already discussed in Chapter 2 of this thesis.

SEU due to multiple-node charge collection

In deep sub-micrometer technologies, feature size scaling and high transistor packing densities has lead to reduced nodal charge and reduced spacing between transistors. Due to this, charge generated due to an ion strike can be collected at multiple nodes in a circuit [13, 14]. It has been shown by Amusan *et al.* [15] that charge collection by multiple nodes (a.k.a *charge sharing*) will lead to increased susceptibility of hardened flip-flop designs.

A sensitive node pair is defined as a pair of nodes that, upon simultaneous charge collection, causes the latch to upset. To simulate charge collection by two nodes, charge is deposited simultaneously on the node pairs using multiple current sources and varied to obtain a number of charge deposition combinations at which the flip-flops upset. As multi-node charge collection is a strong function of layout, and the layout may contain any of these nodes in physical proximity, all possible combinations of node pairs were simulated. The sensitive pairs in DICE latch are indicated in figure 12(a) and the corresponding charge combinations are represented as charge threshold plots in 12(b).



(a)



(b)



(c)
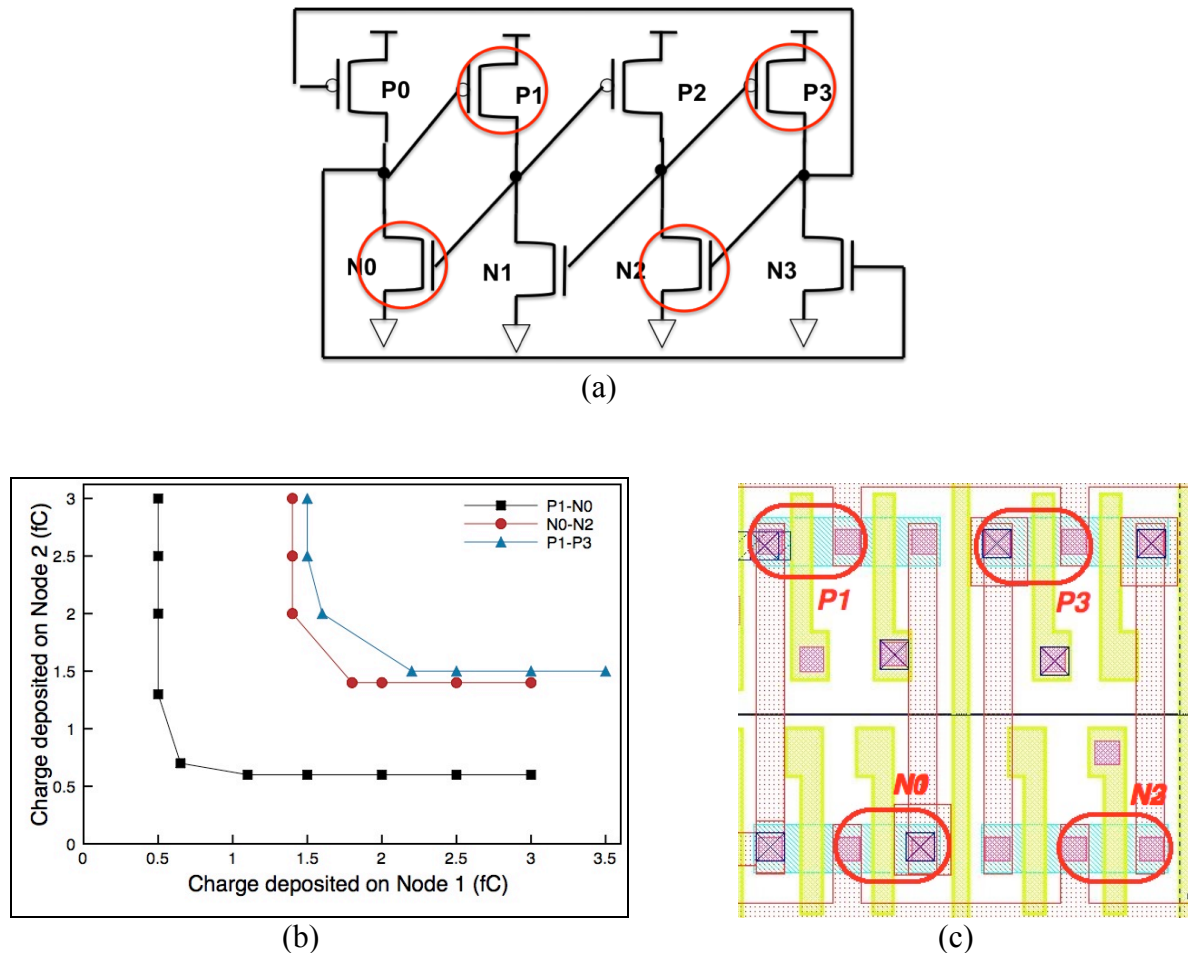
Figure 12(a) Sensitive pairs of a DICE latch are marked on the schematic (b) Critical charge combinations for all the sensitive pairs of DICE (c) position of sensitive nodes on the layout of DICE latch

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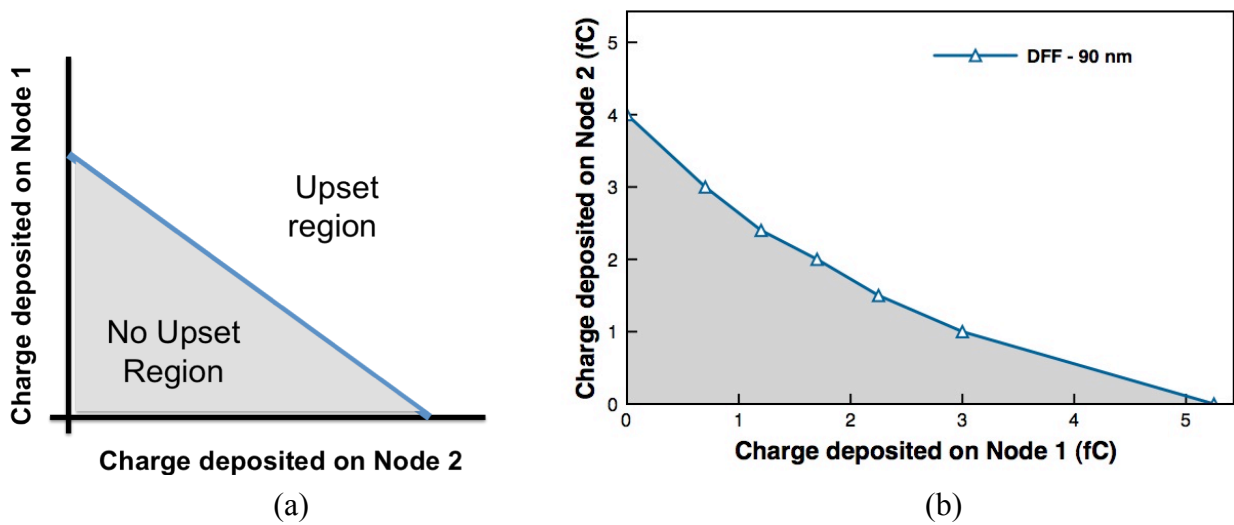
Figure 13: (a) A general charge threshold plot indicating the upset boundary. (b) Charge threshold plot of DFF

The charge threshold curves in figure 12(b) represent the boundary between upset and no upset regions, as illustrated in figure 13. The data points on the curves indicate the charge required to be deposited simultaneously on each node to cause an upset.

Any combination of charge deposition that falls in the region above the curve will cause an error whereas any combination that falls in the region below the curve does not cause an upset. The point of intersection of the curve and the axis gives the amount of single-node charge collection required to cause an upset. Since the DICE flip-flop did not upset for single-node strikes, the curves in figure 12(b) do not intersect the axes. Sensitive pairs (P1, N0) and (P3, N2) exhibit same charge combination requirement and hence, only one of the pairs has been plotted. (P1, N2) and (P3, N0) did not exhibit any vulnerability. Also, it may be noted from the charge combination curves in 13(b) that (P1, N0) is the most vulnerable node pair. Similarly, the most vulnerable node pairs were identified in all the flip-flop designs in each of the technology node considered, with the

help of charge combination curves. Figure 14 shows the charge combination curves for the most vulnerable node pairs in the flip-flops at each technology node.
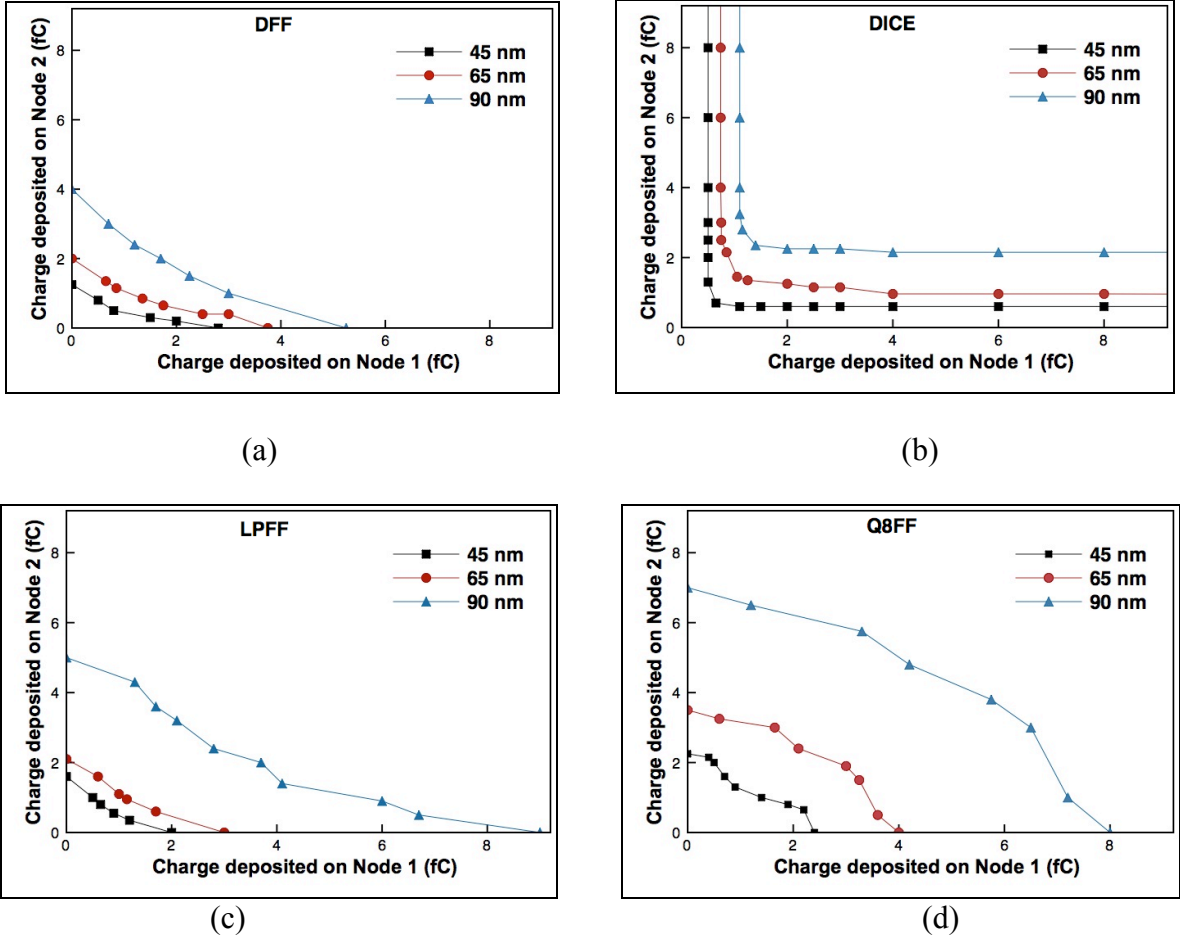


Figure 14: Critical charge combinations for most vulnerable node pairs of (a) DFF (b) DICE (c) LPFF (d) Q8FF

From the above plots, the charge requirement for multi-node upsets was found to be lesser that for single-node upsets, which implies that even if two nodes collected charge less than the $Q_{crit,}$ there is still a chance for an upset to occur. All the four designs are compared at all the three technology nodes in figure 15
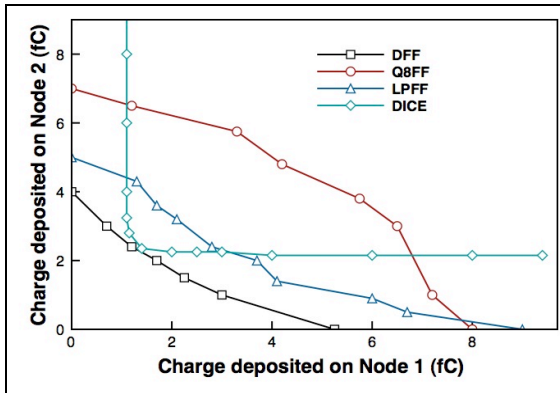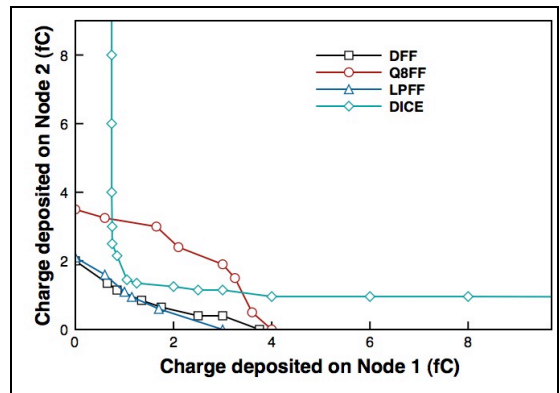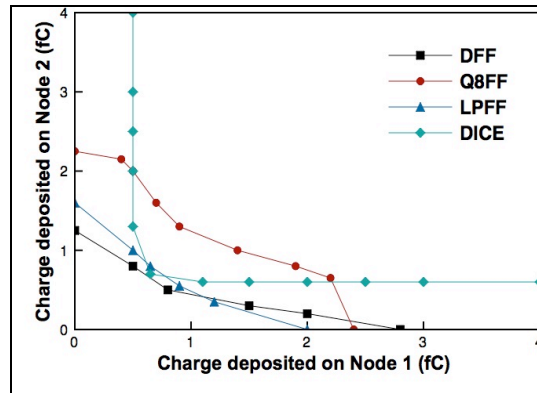
Figure 15: Comparison of all the designs at (a) 90nm (b) 65nm (c) 45nm technology node

**CHAPTER IV**

**MONTE CARLO SIMULATIONS**

Monte Carlo experiments are a class of computational algorithms that rely on repeated random sampling to compute their results. Monte Carlo simulation methods are useful for modeling phenomena that have significant uncertainty in their inputs.

MRED (Monte Carlo Radiative Energy Deposition) is one of the several tools available for Monte Carlo analysis of single event effects. The MRED tool is based on the Geant4 libraries, which comprise computational physics models for the transport of radiation through matter. Along with the information on device and circuit level response to SE, MRED can be used to analyze single event effects in microelectronic circuits [18].



Figure 16: (a) Illustration of a conceptual transistor (b) representing the sensitive drain by a nested sensitive volume group [18]

The energy deposition in the semiconductor material or device can be modeled and due to the radiation environment is estimated by the use of sensitive volumes. Sensitive

volumes represent regions of sensitivity within the semiconductor materials. A concentric weighted sensitive volume model provides a good approximation to the relationship between deposited energy and collected charge. Sensitive volumes are arranged with each volume cent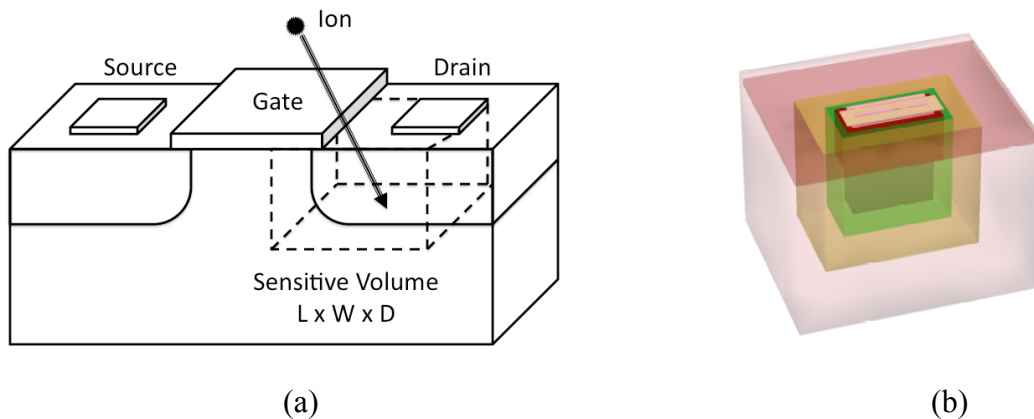ered about the same point, as illustrated in figure 16. A collection efficiency parameter, $\alpha_i$, is associated with each sensitive volume. The charge collected due to energy deposition by an individual particle event is calculated by using the relation [18]:

$$Q_{coll} = \frac{1pC}{22.5\,MeV} \sum_{i=0}^{N} \alpha_i \times E_i \tag{3}$$

Construction of the flip-flop models

As previously discussed, charge collected by a sensitive node can be defined by a group of concentric / nested sensitive volumes. The total collected charge at the transistor node is a function of the charge generated in each sub-volume of the nested sensitive volume group and is given by:

$$Q_{total} = \sum_{i=1}^{n} \alpha_i Q_i \tag{4},$$

where $\alpha_i$ is the efficiency of the $i^{th}$ sensitive volume and $Q_i$ is the deposited charge in the $i^{th}$ sensitive volume [19]. The deposited charge is calculated using the relation:

$$Q_{deposited} = 0.01035 \cdot LET \cdot l \tag{5},$$

where LET, in pC/µm, is the stopping power in the material and $l$, in µm, is the path length of the particle in the material [20]. From (4) and (5), charge collected in each sub-volume of the nested sensitive volume group can be estimated using:

$$Q_{coll_i} = 0.01035 \cdot LET \cdot \alpha_i \cdot l_i \tag{6}$$

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In this thesis, the MRED tool will be used to estimate the charge collected by the sensitive nodes of the flip-flop designs in a terrestrial neutron environment. For this, each sensitive node of the flip-flop has to be modeled as a nested sensitive volume in order to determine the charge collected by that node. These nested sensitive volumes are defined based on 3D TCAD (Technology Computer-Aided Design) simulations of charge deposition in MOSFET structures. The TCAD simulator consists of numerical solvers of continuity and transport equations for electrons and holes at pre-defined points of interest in the semiconductor device. Single-event simulations were performed by depositing charge in the semiconductor devices, which have been calibrated to IBM 9SF 90nm CMOS bulk process. In [17], the authors discuss the construction and calibration of these devices.



(a)                                                                              (b)
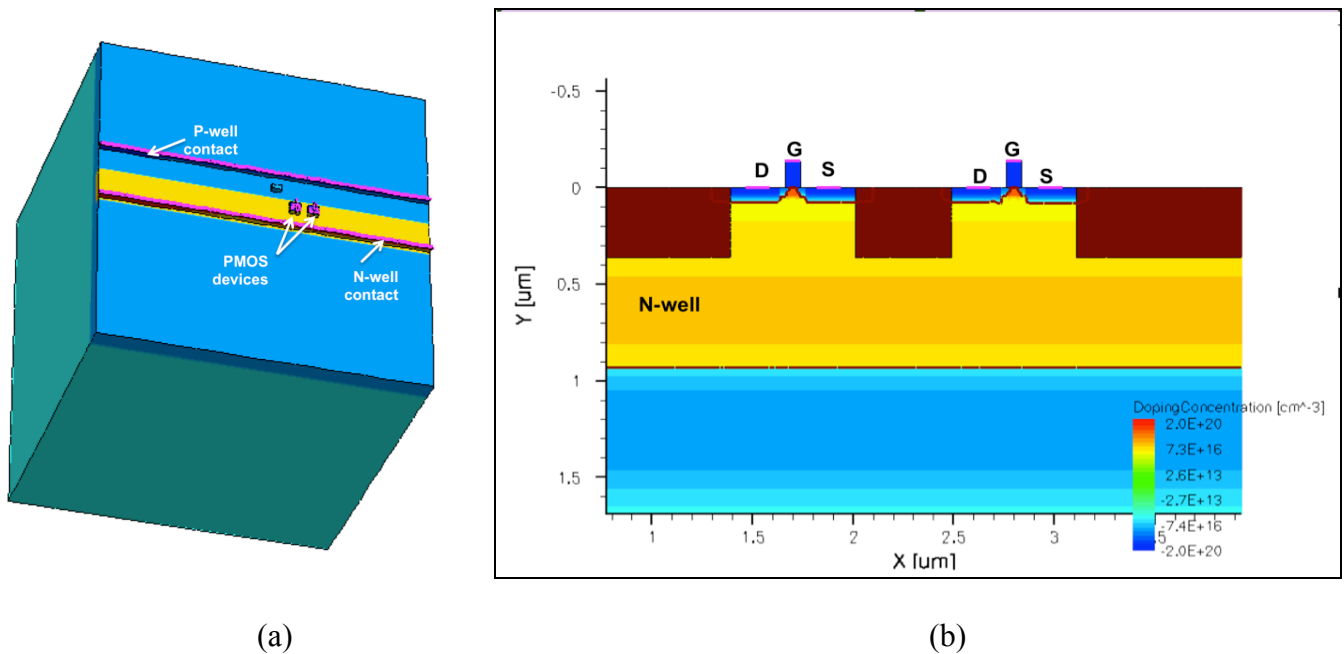
Figure 17: (a) 3D TCAD model of the two PMOS devices subjected to single-event simulations (b) zoomed-in 2D view of the structure showing the PMOS transistors in the n-well.

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Charge deposition simulations were performed on a pair of PMOS devices, 0.5μm apart, (figure 17) to simulate a single-event/particle strike. The range of LET chosen for these simulations was $1 - 5$ MeV cm$^2$/mg. The source and gate of the PMOS transistors were biased to $V_{DD}$ to ensure the transistors were in the OFF state. The strike location was varied along the horizontal axis, keeping the transistor drain as the reference point and the charge collected for each instance is determined by integrating the transient pulse occurring in the drain current due to the particle strike. Similarly single-event simulations were preformed on NMOS transistor pair to determine the charge collected at the drain when particle strikes occur at various points around the transistor drain. The collected charge is plotted as a function of the distance of strike location relative to the drain, as shown in figure 18.

With the information on various strike locations, LET and the corresponding value of collected charge from these TCAD simulations, the parameters $\alpha_i$ and $l_i$ in equation (6), can be adjusted so that the linear relation between collected charge ($Q_{coll}$) and LET established by equation (6) is satisfied over the chosen range of LET and strike locations.



(a)                                           (b)

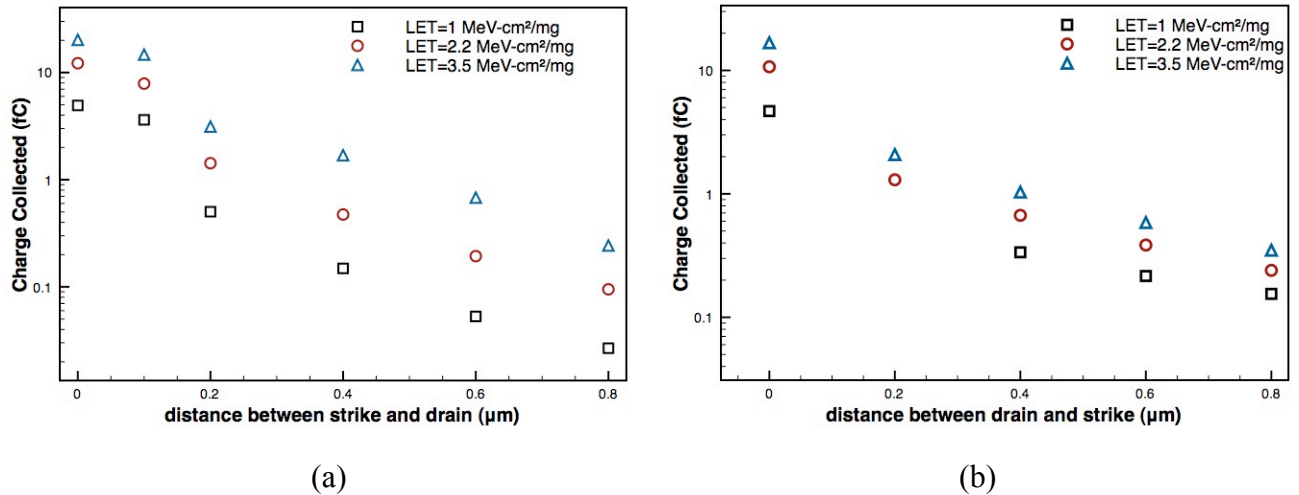Figure 18: The $Q_{coll}$ is plotted as a function of the distance between strike location and the drain of the transistor for (a) PMOS device (b) NMOS device
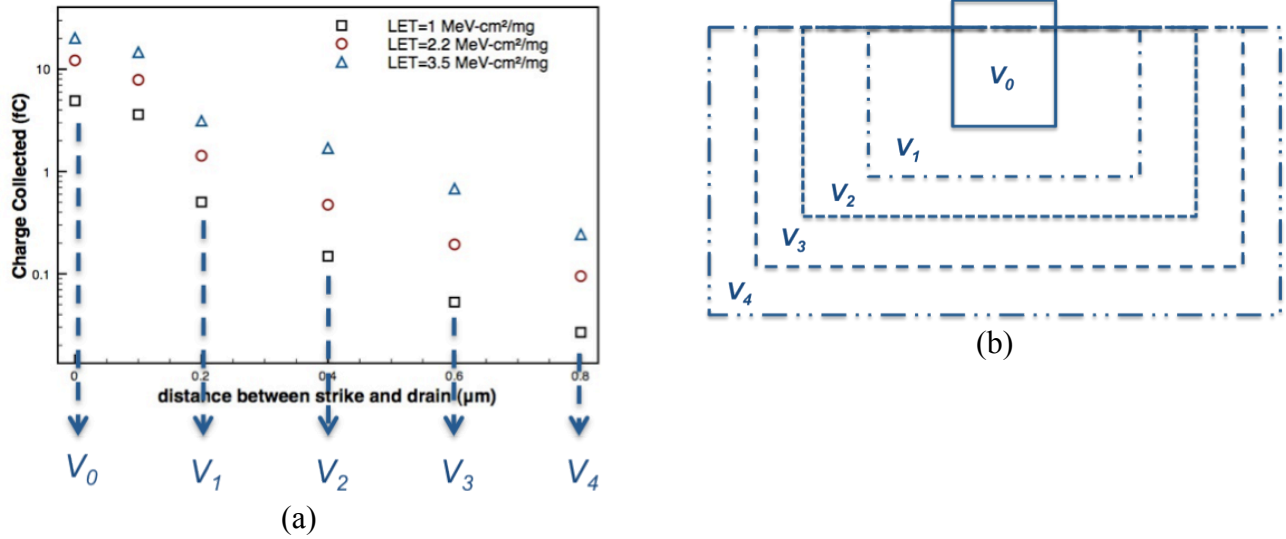
Figure 19: (a) Defining sensitive volumes for the PMOS transistors using the TCAD charge collection data. (b) Conceptual 2-D cross sectional drawing of a sensitive volume set, which defines an individual transistor

Curve fitting by least squares method was used to fit the two parameters, $\alpha_i$ and $l_i$, which correspond to the collection efficiency and the depth of the $i^{th}$ sensitive volume in the nested group. The drain region of the transistor was modeled as the innermost sensitive volume with the highest collection efficiency.
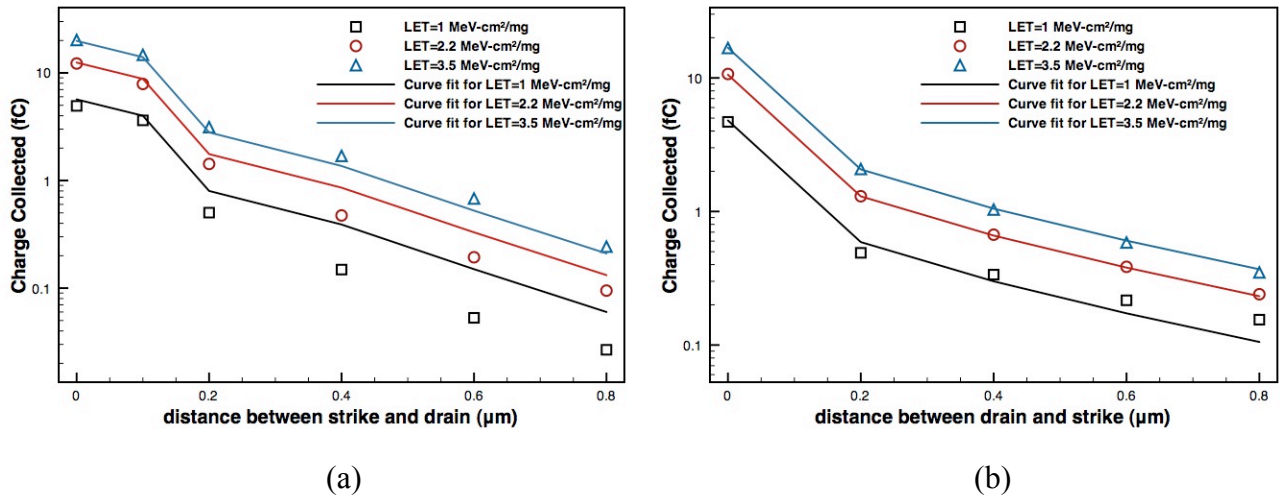


Figure 20: A reasonable fit was obtained with the least squares method for the (a) PMOS and (b) NMOS transistors.

Figure 21: The positioning of the sensitive nodes on the flip-flop layout is shown for (a) DFF (b) DICE and (c) Q8FF. (d) Sensitive volume group for each transistor

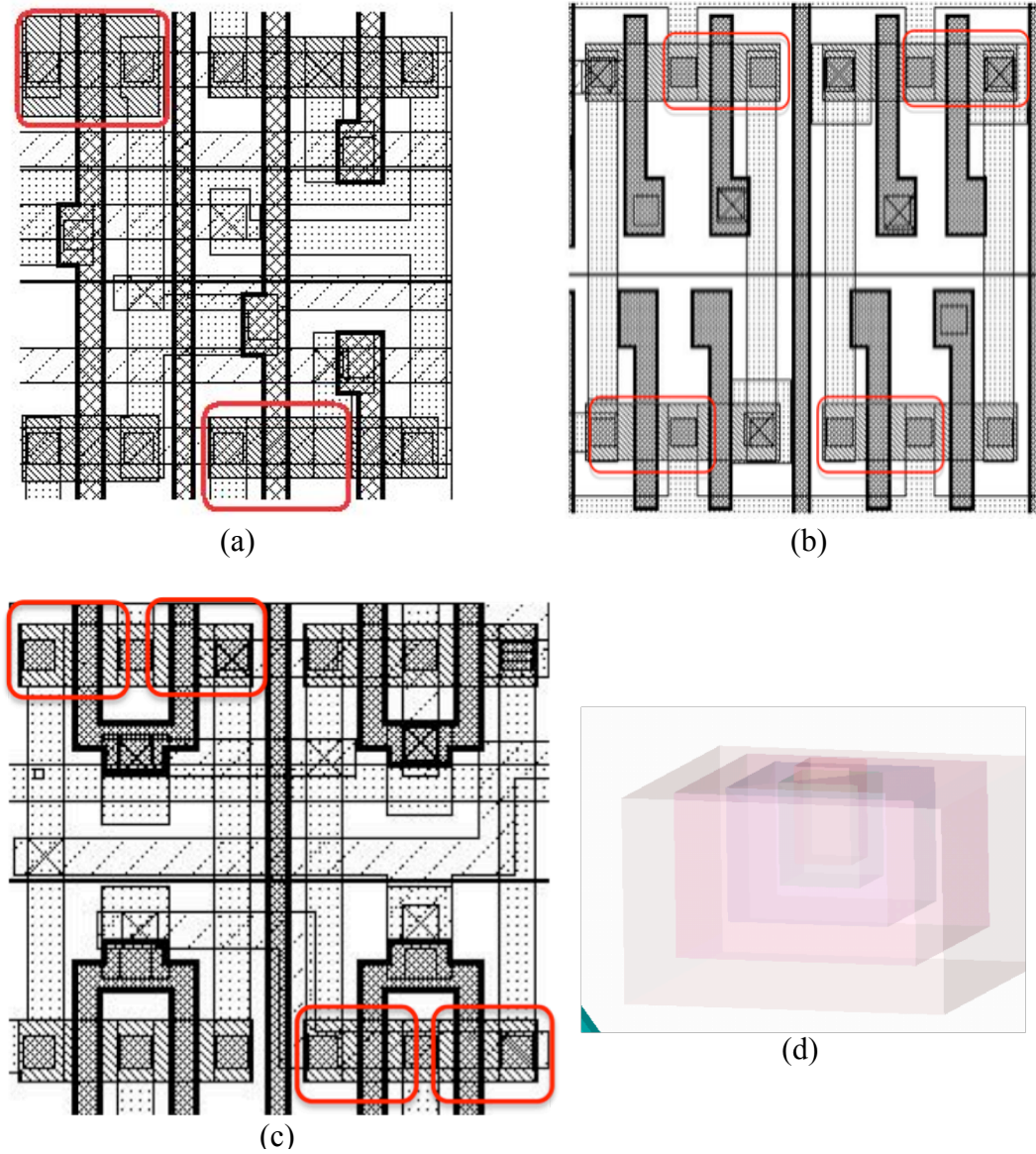The placement of the sensitive volume group, thus derived, in the MRED model was dependant on the position of the sensitive nodes in the physical layout of the flip-flop designs.
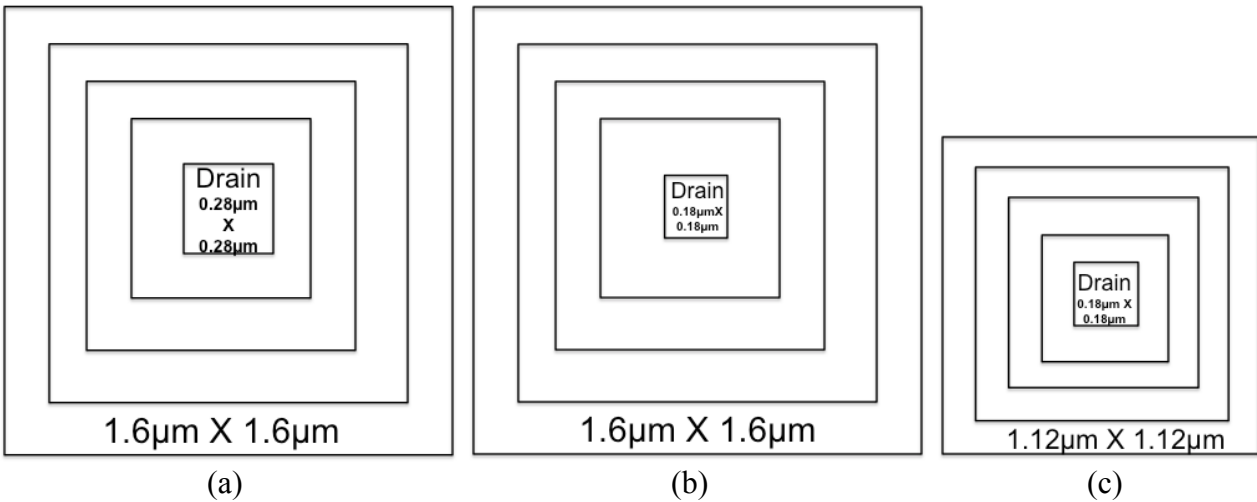
Figure 22: A conceptual drawing of the scaling of sensitive volumes (a) TCAD calibrated sensitive volumes (b) Drain-scaled model and (c) All-volumes-scaled model for the 65nm designs

For the 65nm and 45nm processes, scaled versions of the flip-flop models were developed. This scaling, as done previously by Narasimham *et al.* in [21], was based on the following two assumptions:

1. Only the drain area, the innermost volume in the sensitive volume group, scales with technology node (Drain-scaled model)

2. All the volumes in the in the sensitive volume group scale with technology (All-volumes-scaled model)

MRED Simulations

The MRED tool allows the user to specify, among other parameters, the energy-depositing particle for e.g., heavy-ions etc. For this work, a terrestrial neutron environment is chosen for the Monte Carlo simulations and particle strikes are simulated at a normal angle of incidence. The physics modules included for the simulation were StandardScreened, HadronElastic, HadronInelastic, PiKInelastic, NucleonInelastic and

IonInelastic. For every particle strike, charge collected in each sensitive volume group, representing a sensitive node is estimated and compared to the critical charge data obtained from SPICE simulations, as discussed in Chapter 3 of this thesis.

In the charge threshold curves obtained from SPICE simulations, charge collected by one sensitive node (say, Q2) is plotted as a function of charge collected by the other node (say, Q1) of the sensitive node pair.
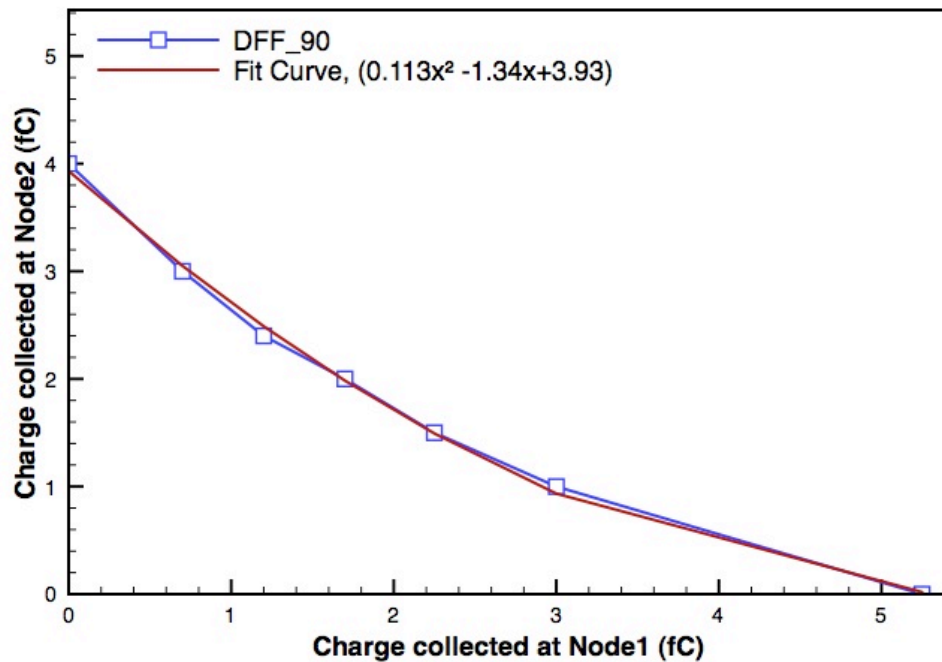


Figure 23: The charge threshold curve for DFF designed at 90nm process is fitted to a parabolic equation that defines the upset-no upset boundary for that design.

This can be represented mathematically, for e.g., figure 23 shows that the upset-no upset boundary for a DFF designed at 90nm technology node, can be represented by mathematically by the equation: $Q_2 = 0.113Q_1^2 - 1.34Q_1 + 3.93$. An upset is said to have occurred if the charge collected by the sensitive node pair is greater than or equal to the

value of the pair $(Q_2, Q_1)$ that can satisfy the equation. An upset is considered a single-node upset when one of the nodes in the sensitive node pair collects charge greater than or equal to the $Q_{crit}$ associated with that node while the charge collected by the other node is a negligible value $(\Delta)$, as illustrated in figure 24. A low $\Delta$ implies a reduced occurrence of single-node upsets. Any upset that is not counted as a single-node upset is regarded as a multiple-node upset. The upset cross-section for single-node and multiple-node upsets is obtained by dividing the weighted count of upsets by the total fluence.
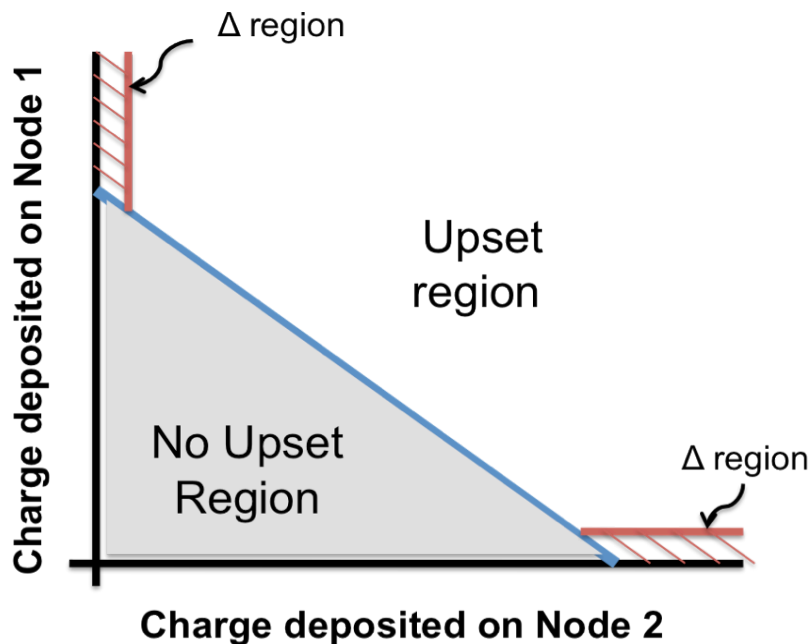


Figure 24: Illustration of the $\Delta$ margin concept for defining single-node upsets.

Simulation results

The upset cross-section is normalized with respect to the results of the MRED model at 90nm technology node (simulated for a terrestrial neutron environment) and plotted for the technology nodes considered. The multiple-node upset cross-section for the DICE

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flip-flop, in figure 25, indicates that there is an increased probability of multiple-node upsets at advanced technologies for both drain-scaled and all-volumes scaled cases.

Since the DFF, LPFF and Q8FF are vulnerable to both single-node and multi-node upsets, the $\Delta$ margin was defined as 5% of the $Q_{crit}$ associated with that sensitive node. The single-node and multi-node cross-sections, normalized with the multi-node cross-section value at 90nm technology node, for these flip-flop designs are shown is figure 26.
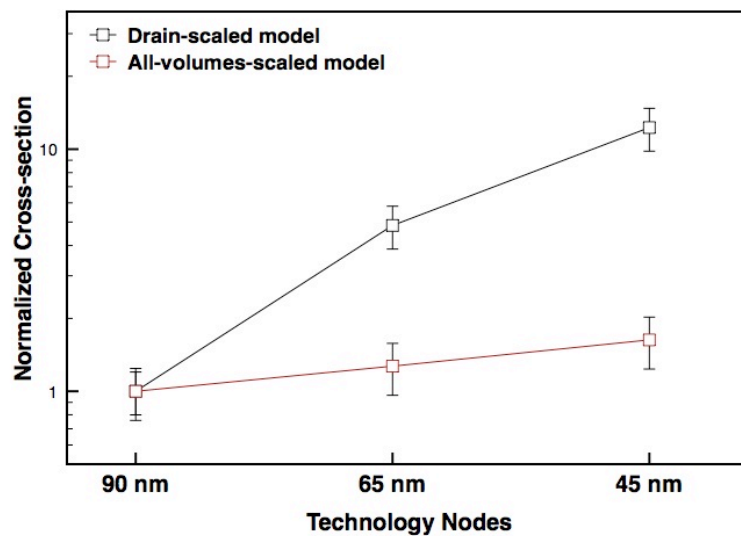


Figure 25: The normalized cross-section for multi-node upsets in DICE

From figure 26, it can be noted that the multiple-node upsets, for the drain-scaled case, increases as the technology advances whereas for the assumption that all the volumes in the sensitive volume group scale, the multi-node upset probability increases for the 65nm flip-flop design as compared to the 90nm design but the probability is almost constant between the 65nm and 45nm designs. The single-node upset cross-section is unaffected by the scaling assumptions. Also, the single-node upset cross-section value for the 45nm flip-flop design is lower than that of the 90nm designs. This may be because the surface

area of the sensitive nodes in the 45nm design is approximately half of that in the 90nm design and hence a smaller area implies a lesser chance getting struck by a charged particle.
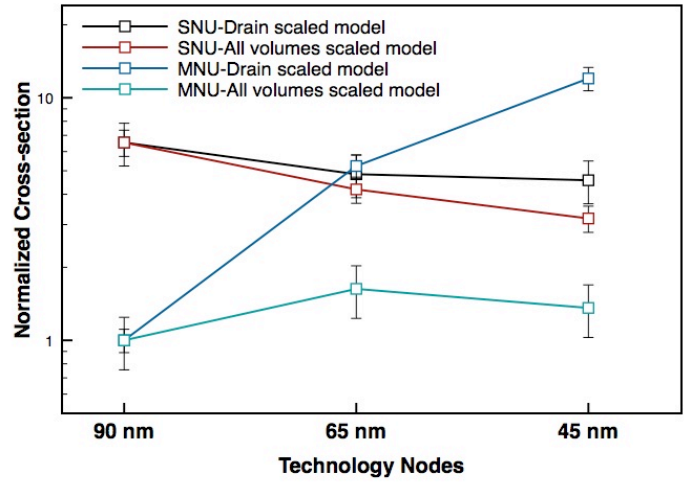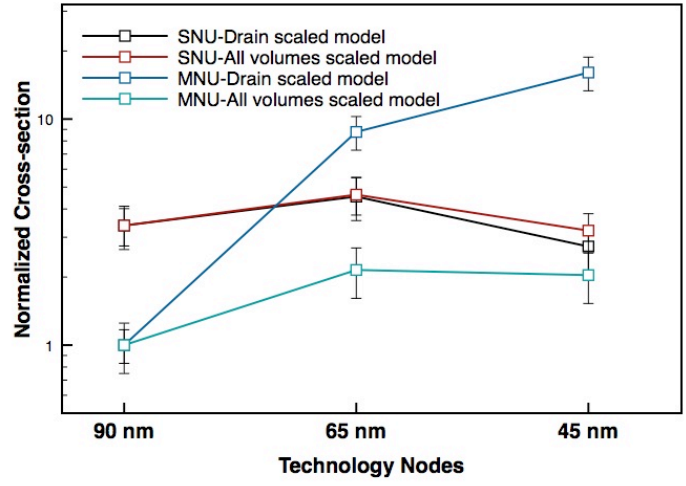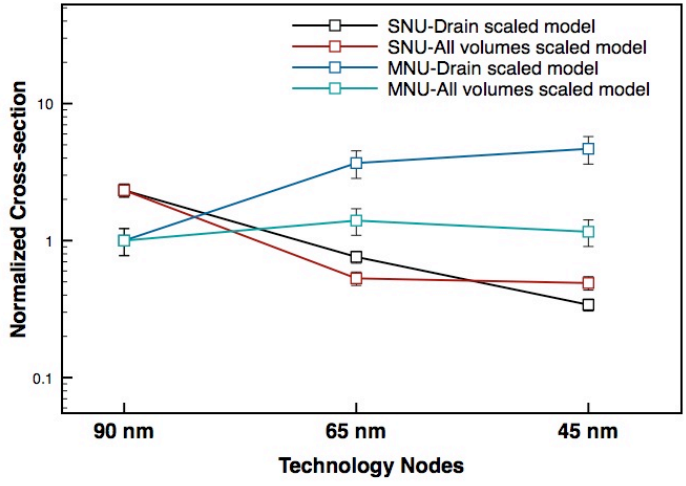
Figure 26: Normalized single and multi-node cross-sections for (a) DFF (b) LPFF and (c) Q8FF
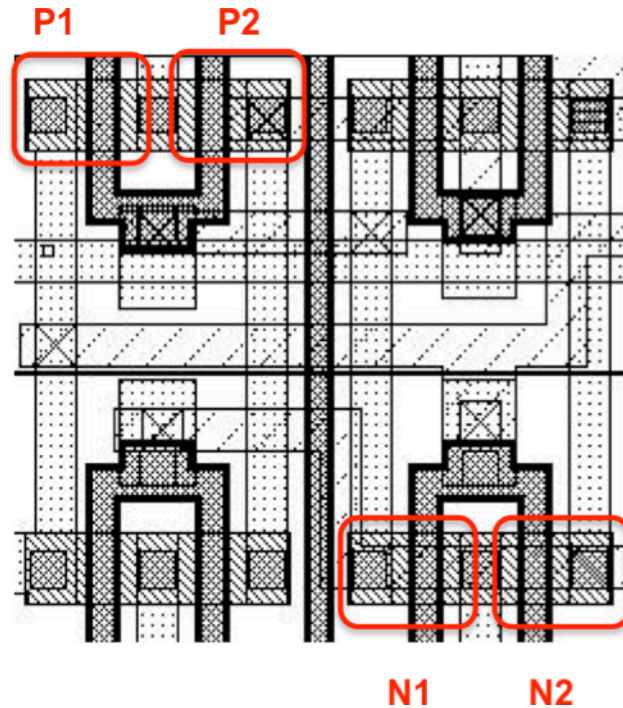
Figure 27: The layout of Q8FF with the three sensitive node pairs, (P1, P2), (N1, N2) and (P2, N2). Sensitive nodes P2 and N2 are affected by single-node charge collection as well.

The rate of decrease in single-node upsets across the technology nodes considered is more for the Q8FF than the other designs (figure 26(c)). This is due to the fact that the Q8FF has four sensitive nodes that form three sensitive node pairs, as illustrated in figure 27 and only two sensitive nodes are affected by single-node charge collection. The DFF and LPFF, on the other hand, have only two sensitive nodes that not only form a sensitive node pair but also upset for single-node charge collection. The presence of three sensitive node pairs in the Q8FF results in a higher multi-node upset cross-section than the DFF and LPFF and since the single-node upset cross-section, in comparison, reduces as the MRED models scale.

The value of Δ is varied 1% and 10% of Qcrit of the sensitive node in the flip-flop, to investigate whether it impacts the upset cross-sections. The single-node and multi-node upset cross-sections are shown in figure 29. The results indicate that varying the Δ value

does not influence the upset cross-sections of the flip-flops greatly. The change in the

upset cross-section of the flip-flops for the 45nm model as compared to the data from the

90nm flip-flop models is given in the table below.

TABLE 2. VARIATION IN UPSET CROSS-SECTIONS OF THE FLIP-FLOPS NORMALIZED W.R.T THE 90NM MODEL
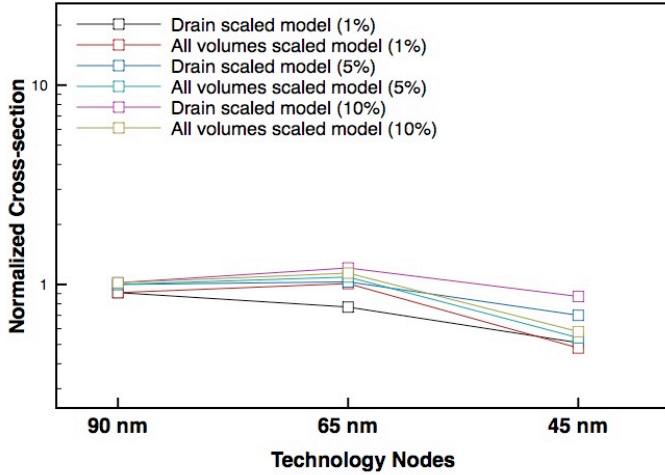
| | DFF | | LPFF | | Q8FF | | DICE | |
|---|---|---|---|---|---|---|---|---|
| | DSM* | AVSM** | DSM | AVSM | DSM | AVSM | DSM | AVSM |
| SNU cross-section | 0.7X | 0.5X | 0.95X | 0.8X | 0.18X | 0.21X | N/A | N/A |
| MNU cross-section | 12.01X | 1.36X | 16.06X | 2.04X | 4.68X | 1.16X | 13.3X | 1.63X |

Since charged particles in space can strike the circuit from all possible directions, the

angle of incidence was changed from normal to grazing angle as the latter has a higher

chance of affecting multiple transistors in a single strike than the former. The results, as

seen in figure 28, show that the change in the angle of incidence has minimal impact on

the multiple-node upset cross-section.
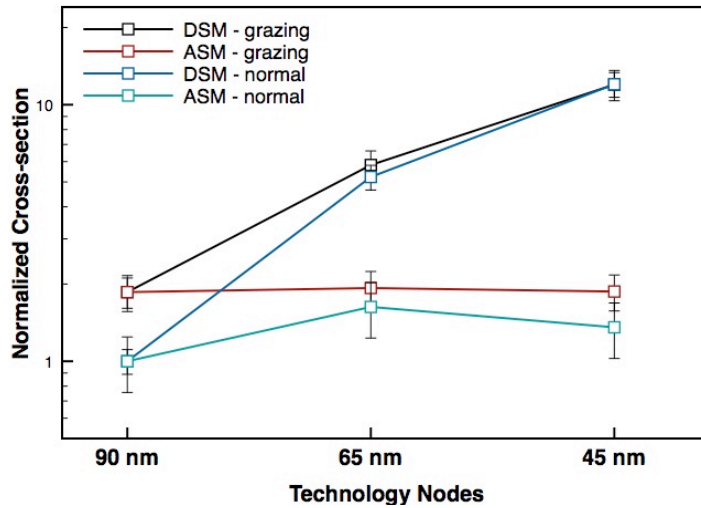


*DSM = Drain-scaled model*
*ASM = All-volumes-scaled model*
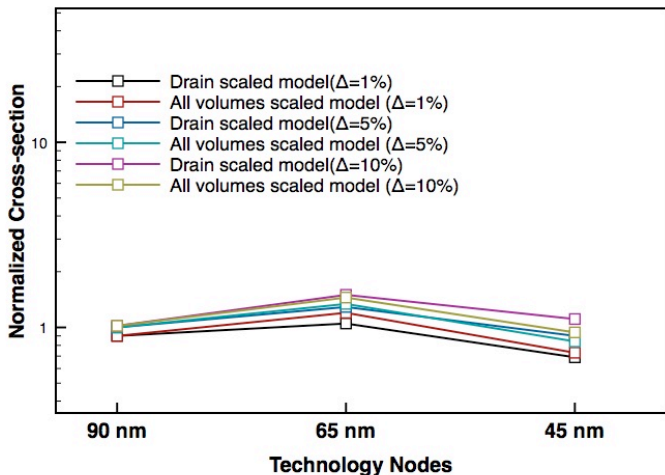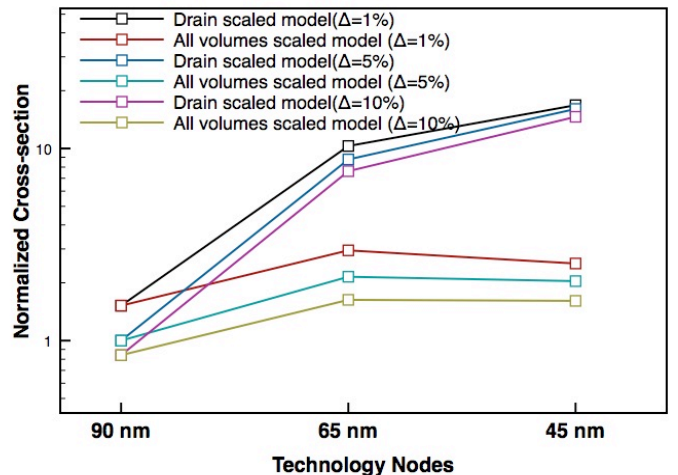
Figure 28: Comparison between normal and grazing angle of incidence
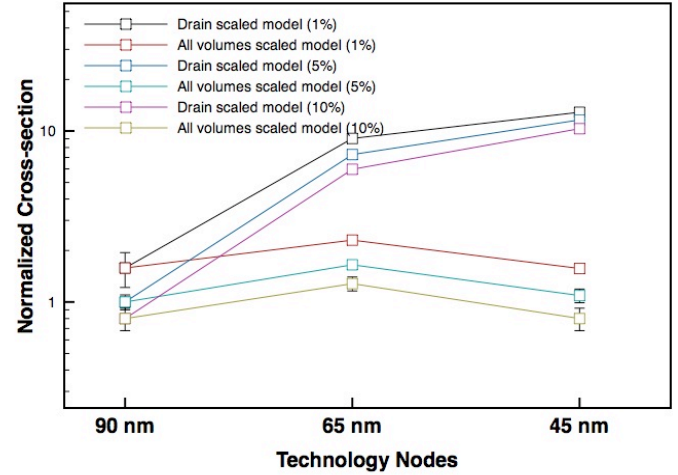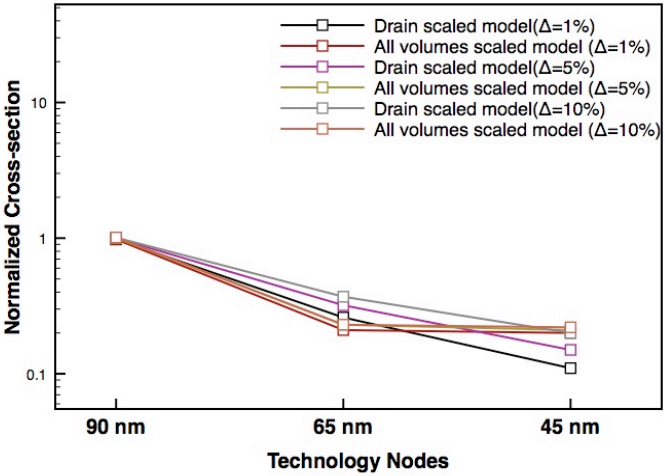
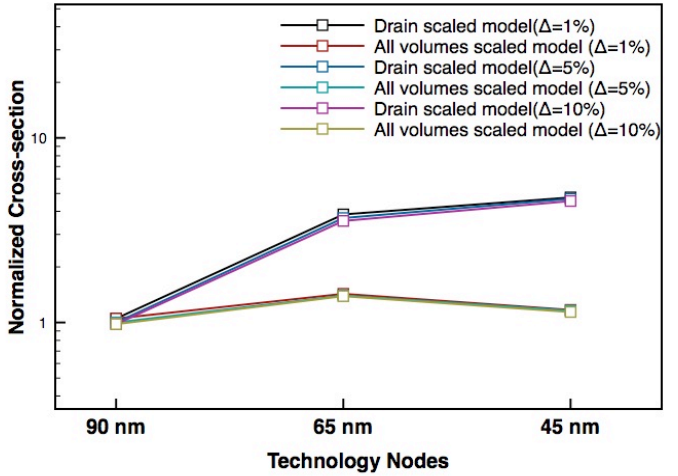Figure 29: The effect of varying Δ margin on single-node upset cross-section is seen for (a) DFF (c) LPFF (e) Q8FF and on multi-node upset cross-section is seen for DFF, LPFF &Q8FF in (b), (d) &(f) respectively. Evidently, choosing 1,5 or 10% Δ margin does not impact the upset cross-sections significantly.

# CHAPTER V

## SUMMARY

This thesis investigates the trends in upset due to single-node and multi-node charge collection using SPICE and Monte Carlo simulations. Two factors influence the upsets in a flip-flop design: charge required to upset the flip-flop ($Q_{crit}$) and probability of that amount of charge getting collected at the node. Circuit-level simulations of four flip-flop designs at 90nm, 65nm and 45nm technology nodes show that the charge required for an upset due to both single-node and multi-node charge collection reduces with technology scaling.

The resulting trends from the Monte Carlo simulations of energy deposition simulations of 3D models of the flip-flops indicated the following:

   i. Probability of upsets due to multiple-node charge collection increased by 5X – 16X if only the drain scales with technology and 1.2X – 2X if all collection volumes scale with technology

   ii. Probability of upsets due to single-node charge collection reduced by 10% – 50% (for the Q8FF, however, single-node charge collection reduced by 80%) and this trend was, for all practical purposes, unaffected by the scaling of the collection volumes.

This methodology, involving circuit & device-level simulations, can be used to predict error rates provided the collection volumes are known for given technology.

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A. Current source:

    The double exponential current source has been traditionally used to inject charge on a node in the single-event simulations at the circuit level for technologies older than the 90nm technology node. However, for deep submicron technologies, the current source derived from TCAD simulations (as discussed in Chapter 3) are used in simulations to estimate the critical charge. A comparison was made between the exponential current source and the current source derived from TCAD, used in this work (figure 30).
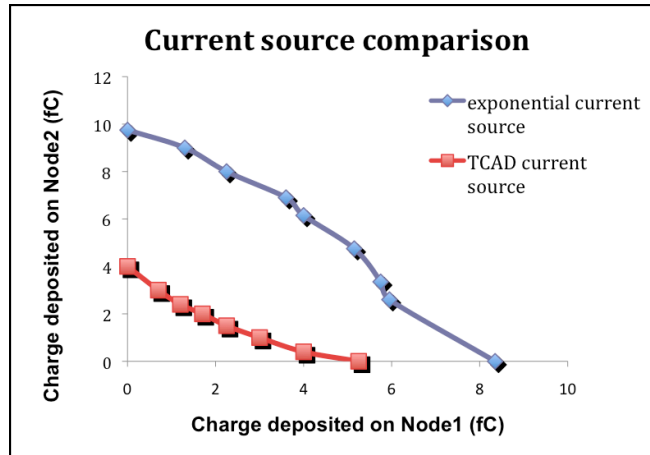


Figure 30: Comparison between double exponential current source and the current source used in this thesis. The double exponential overestimates the $Q_{crit}$ for the flip-flop design considered

B. Strip contact v/s single contact.



(a)                                             (b)
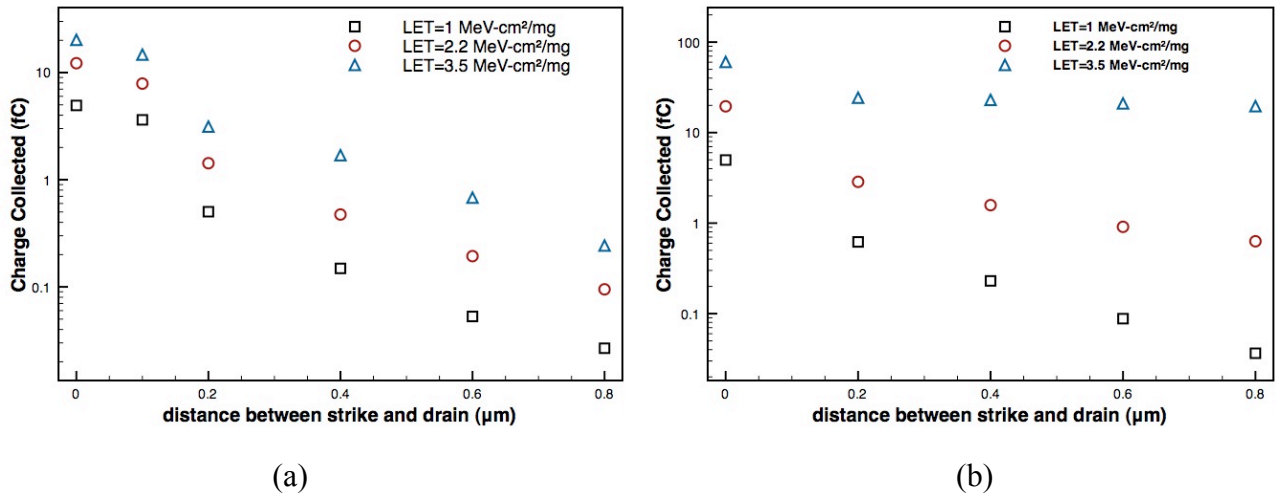
Figure 31: Comparison between a strip of contacts and single contact for the n-well.

The n-well contacting scheme used in the TCAD simulation in Chapter 4 consisted of a strip of contacts that extended along the length of the well. This strip is replaced by a single contact for the n-well and SE simulations are performed as before. The results, as shown in figure 31, indicate that the charge collected by the transistor is higher when the strip of contacts is replaced by a single contact. This emphasizes the impact of the contacting scheme on SEE and implies that a strip of contacts assist in hardening the circuit against soft-errors occurring due to single-events.

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