# Total Ionizing Dose Effects in Silicon Bulk FinFETs at Cryogenic Temperatures

By

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# CHAPTER I

# INTRODUCTION

As science missions in space venture farther and into more intense environments, the accompanying electronic systems will be exposed to increasingly harsh conditions that affect the way they function. Operation in the most interesting extra-terrestrial locations requires a spacecraft to be capable of surviving any number and combination of hostile factors. In particular, the exploration of many of the icy bodies of the solar system, which present themselves as some of the highest priority targets for missions, would require devices to be capable of withstanding radiation while at extremely low temperatures. Understanding the way that these environments might interfere with the modern devices that will compose future spacecraft is crucial in order to successfully design for these environments.

In this work, the operation of silicon bulk FinFET devices in both in cryogenic and combined cryogenic and radiation environments is reported. The devices are cooled to cryogenic temperatures with Liquid Nitrogen, then irradiated with protons while held at temperature. The resulting Total Ionizing Dose (TID) effects are explored. Device performance is typically enhanced at cryogenic temperatures, but degraded with dose. FinFETs are promising candidates to succeed planar devices and extend device size and power downscaling, and as such are ideal for the needs of exploratory spacecraft bound for icy bodies. The response of these devices to extreme environments will demonstrate the viability of their use in future systems.

Chapter II details the motivation of this research by discussing the space environments and exploration of the solar system's icy bodies, and by presenting the benefits of FinFETs through a comparison of planar CMOS and FinFET device characteristics.

Chapter III presents an overview of low temperature and radiation effects in MOS devices. The mechanisms by which low temperature and ionizing radiation respectively alter device operation will be explored. This chapter will also present previous work conducted on the effects of TID on FinFET devices at room temperature, and oxide hole trapping and interface trap generation in planar devices at cryogenic temperatures.

Chapter IV details the nature of the cryogenic and cryogenic irradiation experiments by presenting the equipment and processes used to maintain the requisite environments. This chapter also describes the geometry and processing details of the devices under test.

Chapter V contains the results and analysis of the performed experiments. Comparisons are drawn between irradiation at room temperature and at cryogenic temperatures, and between different device geometries. The mechanisms affecting the devices apparent from the experimental data will be discussed.

Chapter VI presents the conclusions on usage of FinFETs in extreme environments, and suggests future work.

# CHAPTER II

# MOTIVATION AND BACKGROUND

Cryogenic radiation environments exist at some of the highest priority targets for NASA and other space agencies. Electronic systems bound for deep space and icy celestial bodies will be exposed to the harsh space irradiation environment, as well as extremely low temperatures. FinFET devices are possible candidates to make up these electronic systems. Large device manufacturing companies such as Intel, Global Foundries, TSMC, and Samsung have largely adopted the multi-gate device geometry in their modern technology nodes due to the increased performance and decreased power consumption they offer compared to planar devices [1].

This chapter presents the concepts and benefits of FinFET technologies in comparison to conventional planar FET. Additionally, two high profile future missions by NASA into cryogenic and cryogenic irradiation environments will be discussed.

## 2.1 FinFETs as a Solution to CMOS Scaling

Exponential size downscaling of MOSFET devices from generation to generation has resulted in significant enhancements in circuit capabilities and performance. However, moving into the sub-22 nm nodes presents a set of processing and material limitations for conventional MOS structures. Alternative architectures to planar structures have been introduced to overcome these limitations. In particular, the “multi-gate” architecture of the FinFET has been demonstrated to be capable of increasing device density and performance.

In planar FET devices, the conducting channel is located underneath the gate and gate oxide, surrounded by isolation regions. Applied voltage on the gate is able to modulate the field only from the top of the channel. For FinFETs, that conducting channel is located in a three-

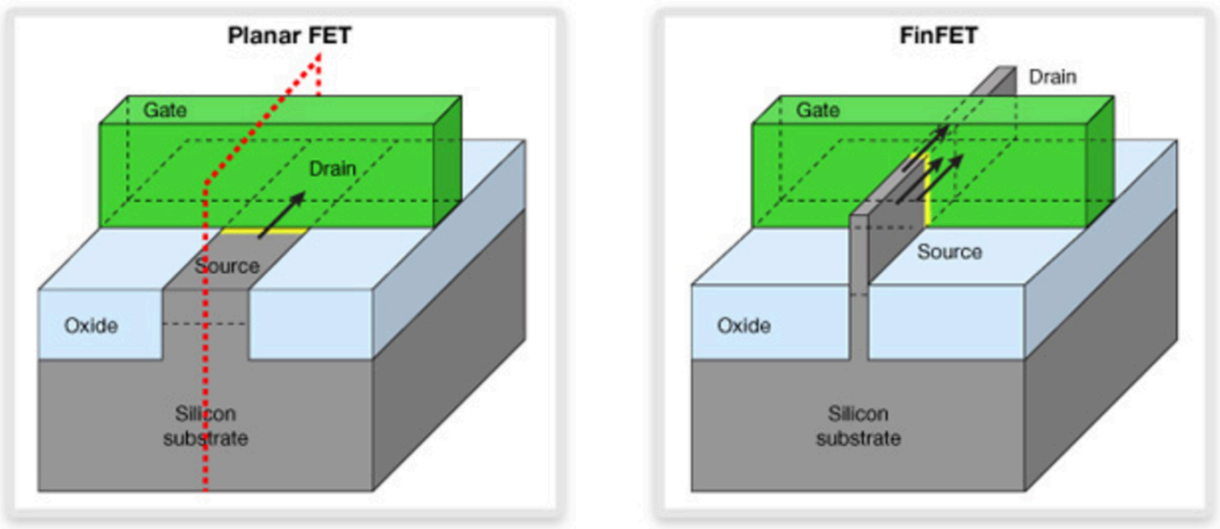


*Figure 2.1: Comparison of planar FET and FinFET device geometries. (From [2] Kawa, 2013)*

dimensional fin that extends up from the silicon substrate, as pictured in Figure 2.1. The gate is able to wrap around the conducting channel, effectively providing three gates – one on the top, and one on each side. Alternate designs involve architectures with only the two vertical gates, or different fin shapes. FinFETs have also been called MuGFETs, for multi-gate FETs.

In comparison to planar technologies, the 3-dimensional FinFET geometry results in enhanced performance for several distinct metrics. Because the gate is wrapped around the conductive channel, FinFET devices exhibit far more electrostatic control than comparably sized planar devices. The gate is able to more effectively choke-off the current in the off state, allowing for orders of magnitude smaller subthreshold leakage currents. This increased electrostatic control also provides protection against the complex short channel effects that plague highly scaled planar devices, which would otherwise result in threshold voltage modulations and additional parasitic leakage paths.

Another benefit inherent to the FinFET geometry is the capability for increased device areal density. Reductions in leakage and short channel effects both enable scaling, but another

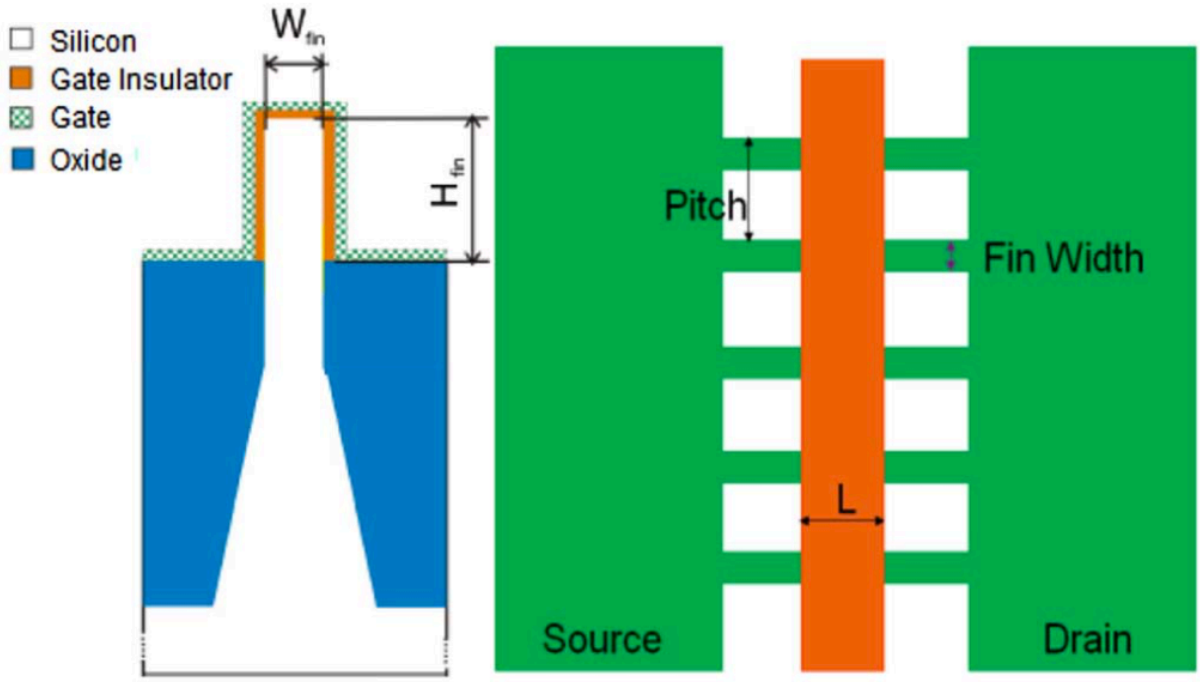


*Figure 2.2: Definitions of important FinFET device parameters for a bulk FinFET. (From [3] Put, 2010)*

factor is the ability to extend fin heights, taking advantage of the third dimension, which allows for more devices per two dimensional area [1]. Important device geometry definitions are depicted in Figure 2.2.

Finally, the amount of doping in the channel of FinFETs in order to provide electrical isolation and some immunity to latch-up and punch-through is far less than is necessary for planar devices. Some FinFET device technologies take advantage of solely doping the bottom portion of the fin and allowing the top of the fin to remain un-doped. While providing some protections, increased doping creates part to part variability and decreased mobility, and if the doping is non-uniform it results in increased capacitance in the device [4]. The fin geometry in FinFETs allows manufacturers to opt for lower doped channels, minimizing these negative effects while maintaining device protection.

## 2.2 Space Environments and High Profile Missions

The radiation environment encountered by space-borne missions largely consists of particles from three main sources – particles trapped in the magnetic field of a celestial body, galactic cosmic rays, and particles from solar events.

Particles that are trapped in the magnetic field are of particular issue when planning for missions in orbits around planets with significant magnetospheres, such as Earth and Jupiter. The magnetic fields of these planets confine charged particles into belts around the planet that will constantly irradiate spacecraft within them. Earth's belts, the Van Allen Belts, are comprised of electrons with energies of several MeV, and protons with energies of several hundred MeV. The magnetic field around Jupiter is orders of magnitude stronger and constitutes a far harsher environment. Galactic cosmic rays are charged particles originating outside the solar system, primarily composed of protons, alpha particles, and extremely energetic heavy ions. Particles from solar events are emitted from the Sun, consisting of x-rays, protons and heavy ions with energies in the hundreds of MeV [5].

| Distance from Sun | Spacecraft Temperature (Sphere, Abs. = 1, Emiss. = 1 Internal Power = 0) | |
|---|---|---|
| Mercury | 448 K | 175 °C |
| Venus | 328 K | 55 °C |
| Earth | 279 K | 6 °C |
| Mars | 226 K | -47 °C |
| Jupiter | 122 K | -151 °C |
| Saturn | 90 K | -183 °C |
| Uranus | 64 K | -209 °C |
| Neptune | 51 K | -222 °C |
| *Pluto (former)* | 44 K | -229 °C |

*Figure 2.3: Temperature data for various planetary missions. (From [6] Patterson, 2008)*

Besides just radiation environments, space-borne electronics also have to deal with extreme temperature conditions. Spacecraft bound for deep space will experience extremely cold temperatures and background radiation in transit. The temperature of a spacecraft traveling in the solar system with no built-in internal heating is presented in Figure 2.3. Additionally, some of the most interesting potential targets for space exploration and research are into the radiation and extreme cold environments presented by the icy bodies of the solar system. This section presents two high profile missions, future and present, into the cryogenic radiation environment around Jupiter.

*2.2.1 Juno*

Juno is NASA's spacecraft designed to orbit and examine Jupiter. The spacecraft arrived at Jupiter on July 4$^{th}$, 2016, with the mission of determining how much water is in Jupiter's atmosphere, retrieving information from below Jupiter's atmosphere, and mapping Jupiter's

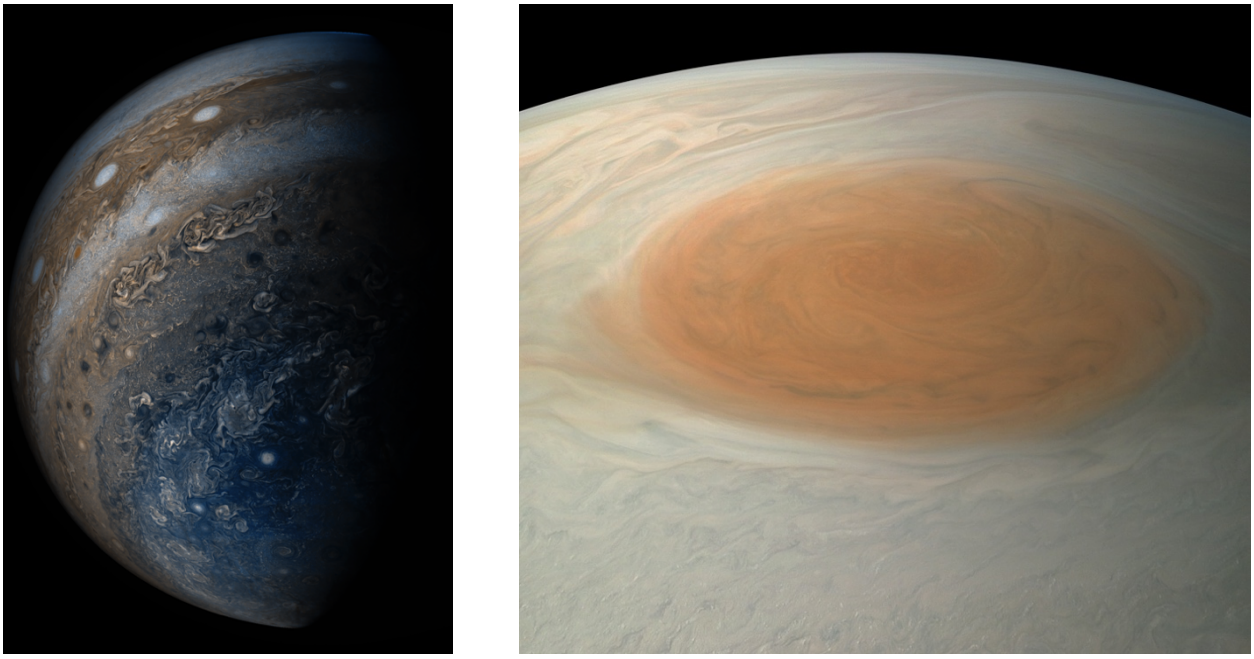

*Figure 2.4: Color processed images from data captured by the JunoCam imager on NASA's Juno spacecraft. Pictured are Jupiter's southern pole [10] and "red spot" [11].*

magnetic and gravity poles. These tasks are aimed at understanding the origin and development of Jupiter, and provide a look at its interior.

While experiencing the cryogenic temperatures inherent in deep space (Figure 2.2), the probe also will be faced with the previously mentioned severe radiation belts around Jupiter. Jupiter's magnetic dipole is 428000nT compared to Earth's 30760nT, resulting in a radiation environment in Jupiter's belts orders of magnitude more intense than those in Earth's belts [8]. In one planned low-passing maneuver to examine the inner atmosphere of Jupiter, the spacecraft will take a 14-day elliptical orbit bringing the probe within 5000km of Jupiter, and exposing the craft to 20 Mrad [6]. The spacecraft is designed to orbit Jupiter for 20 months, after which it will descend into Jupiter and be destroyed to prevent any possible contamination of Europa [10].

### *2.2.2 Europa Clipper*

Images of Europa from first the Voyager, then Galileo spacecraft missions depicted chaotic terrain that appears to be made up of icy crustal blocks. The shape of cracks and impacts in this icy shell suggest the existence of an underground ocean, 20 kilometers below the surface. In addition, the magnetic field and the oxidant-creating rradiation environment could provide the materials and environment to sustain basic forms of life. In order to learn more about Europa, and to collect the data needed to determine if Europa is or was ever able to sustain life, a mission titled the "Europa Clipper", which is designed to repeatedly fly past Europa and observe its habitability [11].

The radiation environment close to Jupiter is extremely harsh due to Jupiter's strong magnetosphere. Close contact with Europa will inevitably bring a spacecraft into Jupiter's harsh radiation environment. In addition, the temperature on Europa's equator never rises above 113K, and at the poles never rises above 53K. The launch of the Europa clipper is planned for the 2020s.

# CHAPTER III

# EXTREME ENVIRONMENT EFFECTS OVERVIEW

When planning and designing for missions targeting hostile low temperature and radiation environments in space, the reliability of microelectronic devices and circuits in those environments is crucial to success. This work focuses on the effects of cryogenic temperature and radiation on FinFET devices. This chapter presents an overview of the basic mechanisms and effects of low temperature and radiation on device operation. Previous work on the total ionizing dose response of FinFET devices at room temperature is discussed.

## 3.1 Cryogenic Temperature Effects

Temperature plays an important role in the electrical and physical characteristics of semiconductor materials. When transistors are exposed to extremely cold temperatures, their operation is altered by changes in the semiconductor material characteristics. Figure 3.1 shows the Fermi level and band gap positioning of Silicon as a function of temperature for various doping concentrations. As the plot suggests, at cryogenic temperatures, the band-gap of silicon increases slightly at low temperatures and the difference between the Fermi level $E_F$ and the intrinsic Fermi level $E_i$ increases as the temperature decreases. The increase in the band-gap is due to the increased energy needed to excite an electron from the valence band into the conduction band at lower temperatures. When temperature decreases, the semiconductor lattice compresses and the inter-atomic bonds are strengthened, demanding more energy from electrons to break free. Because of the increase in band-gap and the decrease in thermal energy in the system, the intrinsic carrier concentration is decreased. Equation 3.1 shows the exponential relationship between the intrinsic carrier concentration and temperature [12].

$$n_i = \sqrt{N_C N_V} \exp(^{-E_G}/_{kT}) \qquad \text{(Equation 3.1)}$$

The increased magnitude of $E_F$ - $E_i$ shown in Figure 3.1 is due to the decrease in the intrinsic concentration at low temperatures. Equation 3.2 expresses this relationship [12].

$$E_F - E_i = kT\ ln\left(\frac{n}{n_i}\right) = -kT\ ln\left(\frac{p}{n_i}\right) \qquad \text{(Equation 3.2)}$$

As temperature decreases below the extrinsic T-region, fewer and fewer dopant atoms have the thermal energy required to ionize, leaving donor sites occupied and acceptor sites empty. At extremely low temperatures approaching 0 K, the number of charge carriers diminishes [12]. This

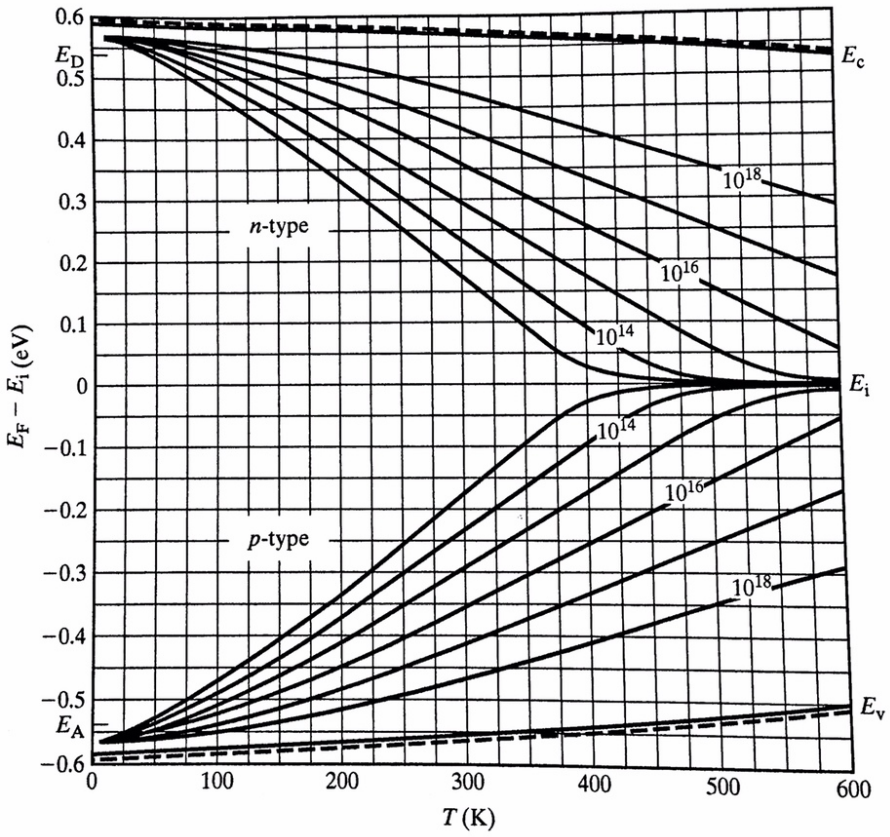


*Figure 3.1: Fermi level positioning in Si as a function of temperature for several doping concentrations, assuming one type of dopant and dopant ionization energies of 0.045 eV. (From [12] Pierret, 2003)*

is described as carrier freeze-out. However, this only becomes a significant factor in device operation at temperatures below those examined in this work.

An additional factor of note is the increase in mobility that carriers experience at lower temperatures. When temperature is decreased, lattice vibrations are decreased, resulting in less lattice scattering events and increased mobility. At very low temperatures, impurity scattering, which increases with decreasing temperature, becomes dominant [12]. The amount of impurity scattering in a semiconductor would depend on the doping concentration, with heavily doped semiconductors experiencing more impurity scattering.

Historically, significant research was conducted on planar devices at cryogenic temperatures because the changes in semiconductor characteristics resulted in device improvement for several key performance metrics. At lower temperatures, devices exhibit increased drive current, shifted threshold voltage magnitude, increased subthreshold slope, and decreased subthreshold current, as depicted in Figure 3.2.

The increased drive current and increased transconductance at low temperatures are caused by increased carrier mobility. For long channel MOSFET devices, the drive current and transconductance in the linear and saturation modes are proportional to the carrier mobility in the channel. Equation 3.3 and Equation 3.4 show this relationship for drain currents and transconductance for devices in the linear region [12].

$$I_{D(lin)} = \mu_{eff} C_{OX} \frac{W}{L} (V_G - V_T) V_{DS} \qquad \text{(Equation 3.3)}$$

$$g_{m(lin)} = \frac{dI_{D(lin)}}{dV_G} = \mu_{eff} C_{OX} \frac{W}{L} V_{DS} \qquad \text{(Equation 3.4)}$$

When the temperature of a device is reduced, the individual atoms in the device material's semiconductor lattice lose thermal energy. This decrease in lattice vibration results in fewer collisions between charge carriers and the semiconductor lattice ("lattice scattering" or "phonon scattering"), allowing the carriers to flow more easily through the device material. For long channel devices, this means that at lower temperatures, devices will experience increases in both transconductance and drive current (Figure 3.2). The amount the mobility will be increased is dependent on channel doping, with lower-doped channels experiencing a greater increase due to mobility being primarily dependent on lattice scattering as opposed to interaction impurities (Figure 3.3). The effect of increased mobility is also dependent on channel length. The drive current of devices with smaller channels is less dependent on channel mobility and more dependent on the saturation velocity of the charge carriers. Saturation velocity is only weakly dependent on temperature, so shorter channel devices have smaller increases in transconductance and drive

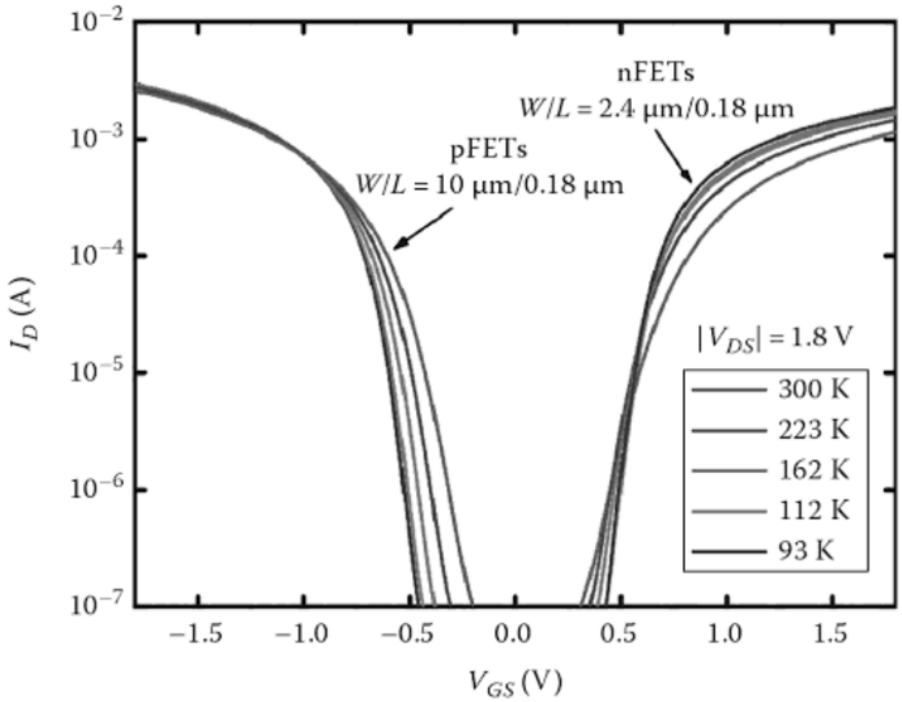


*Figure 3.2: Transfer characteristics of 180nm CMOS devices at various temperatures. (From [15] Appaswamy, 2013)*

current with decreasing temperature [15]. For all devices, drive current will also be increased secondarily by the decreased series drain to source resistance at lower temperatures.

Depending on system tolerances, the benefits of increased drive current and transconductance may be offset by the increase in threshold voltage magnitude at lower temperatures. The equations for threshold voltage for p- and n- channel devices with no channel-body bias are described in Equations 3.5(a-b) [12].

$$V_{T(n-channel)} = V_{FB} + 2|\phi_p| + \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_a}\sqrt{2|\phi_p|} \qquad \text{(Equation 3.5(a))}$$

$$V_{T(p-channel)} = V_{FB} - 2|\phi_n| - \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_d}\sqrt{2|\phi_n|} \qquad \text{(Equation 3.5(b))}$$

The temperature dependence of the threshold voltage is from the flatband voltage, $V_{FB}$, and the bulk potentials $\phi_p$ and $\phi_n$. As discussed previously, as temperature is decreased, the intrinsic carrier concentration decreases exponentially, increasing the difference between the Fermi and intrinsic Fermi energy levels. This increases the magnitude of the bulk potentials, which are equivalent to the magnitude of the difference between $E_F$ and $E_i$. The temperature dependence of the flatband voltage is through the work function difference, which varies with the bulk potential. These relationships are shown in Equations 3.6(a-c) [12].

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{x_{OX}} \frac{x}{x_{OX}}\rho(x)dx \qquad \text{(Equation 3.6(a))}$$

$$\Phi_{MS(p-channel)} = \Phi_M - (X + \frac{E_g}{2q} + |\phi_p|) \qquad \text{(Equation 3.6(b))}$$

$$\Phi_{MS(n-channel)} = \Phi_M - (X + \frac{E_g}{2q} - |\phi_n|) \qquad \text{(Equation 3.6(c))}$$

As the bulk potential magnitude goes up with decreasing temperature, the work function difference goes down for n-channel and up for p-channel devices, resulting in the same changes for the respective flatband voltages. However, the decreased flatband voltages in n-channel devices

and the increased flatband voltages in p-channel devices with lower temperature are overcome by the increased bulk potential magnitude, as can be shown by combining Equations 3.6(a-c) with Equations 3.5(a-b). This results in an increase in threshold voltage for n-channel devices, and a decrease in threshold voltage for p-channel devices. Because the threshold voltage is positive for n-channel devices and negative for p-channel, for both types of devices decreasing the temperature results in an increased threshold voltage magnitude.

This same phenomenon has the side benefit of decreasing subthreshold current in larger channel devices. The equation for subthreshold current is described in Equation 3.6 [16].

$$I_{D(sub)} = \mu_{eff} C_{OX} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 \exp\left(\frac{q(V_G - V_T)}{mkT}\right), \; m = 1 + \frac{C_d + C_{it}}{C_{ox}} \qquad \text{(Equation 3.7)}$$

As equation 3.6 shows, for devices whose subthreshold leakage is dominated by drain to source leakage, typically in the range of channel lengths of 180nm, the subthreshold current is exponentially related to temperature. In the subthreshold bias region, drain to source current is primarily caused by caused by the density gradient of minority carriers in the channel diffusing injected carriers across the channel. When the intrinsic carrier concentration is diminished, the minority carrier concentration is diminished proportionally, resulting in fewer minority carriers to provide the gradient that would cause diffusion across the channel. This results in decreased subthreshold current. With smaller devices on the scale of 90 nm or below, leakage is generally dominated by direct tunneling through the much thinner gate oxide instead of directly from drain to source. For these devices, subthreshold current is more weakly dependent on temperature [16].

The exponential decrease in subthreshold current corresponds to an increase in subthreshold slope, or a decrease in subthreshold swing, as shown in Equation 3.7 [16].

$$SS = \left(\frac{d log_{10}(I_{D(sub)})}{dV_G}\right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \qquad \text{(Equation 3.8)}$$

Subthreshold swing is linear with temperature, with subthreshold swing decreasing as temperature decreases. This relationship can be observed in Figure 3.2.

Gate induced drain leakage (GIDL) and drain induced barrier lowering (DIBL) are additional mechanisms that increase off state leakage in CMOS transistors. GIDL in NMOS devices occurs when strong electric fields at the gate-drain interface are created by applying a very low gate voltage compared to the drain voltage. These strong electric fields promote tunneling from the drain to the body, increasing off state leakage, and also degrade device performance by injecting hot carriers into the gate oxide. GIDL has been proven to be a thermally activated process and lower temperatures significantly reduce the impact of GIDL. DIBL refers to the decrease in threshold voltage in short channel devices due to a large drain electric field. With short channel devices, the proximity of the drain and source allows a strong drain field to modulate the source-body junction in conjunction with the gate voltage. The drain field lowers the energy barrier,

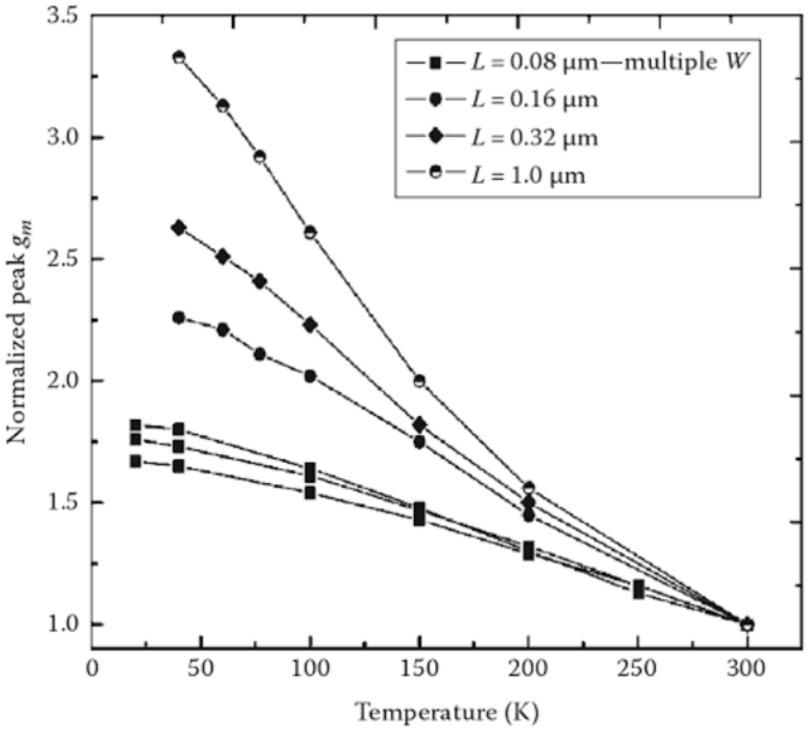


*Figure 3.3: Normalized peak transconductance as a function of temperature for different device gate lengths. (From [15] Appaswamy, 2009)*

reducing the threshold voltage and increasing subthreshold leakage. DIBL is not thermally activated and is not substantially affected by decreasing temperature [17].

## 3.2 Basics of TID Radiation Effects

Semiconductor devices are often required to operate in hostile radiation environments, especially in the space-borne missions that this work aims to support. The effects of those radiation environments, and the resultant damage to semiconductor devices, can be broadly defined by two distinct categories: ionization effects and displacement damage. Ionization effects can include Total Ionizing Dose (TID) effects from the accumulated dose deposited by charged particles over time, or Single Event Effects (SEE) which refer to the effects caused by single particles. Displacement Damage (DD) refers to the non-ionizing kinetic damage caused by particles striking a target semiconductor lattice. This section introduces the general mechanisms of radiation and TID effects in semiconductor devices, and presents previous work on the effects of TID on FinFETs at room temperature.

### *3.2.1 Interactions Between Radiation and Matter*

Radiation can exist in several forms, from charged particles such as protons, electrons, and ions, to energetic photons. When these forms of radiation pass through a material, they deposit energy into that material. This energy is described as the absorbed dose. For a given slice of material, the absorbed dose is equivalent to the difference between energy of the particle when it enters the slice and the energy of the particle when it leaves. The standard unit for dose is the rad, where 1 rad = 0.01 J/kg. This unit is normalized for the density of the target material, and as such is often used in reference to specific common target materials, such as rad(Si) and rad($SiO_2$). Dose can be deposited as some combination of ionic and kinetic energy. If an ion has an energy greater than the band-gap of the target material, it is able to pull electrons away from their corresponding

nucleus to create electron-hole pairs [18]. If the energies of the generated carriers are greater than the band-gap of the target material, they are also able to generate subsequent electron-hole pairs. With a substantially energetic initial charged particle, this can result in a cascade of carriers freeing other carriers until they no longer have energies greater than the band-gap of the material.

### *3.2.2 Total Ionizing Dose in MOS Structures and Transistors*

Total Ionizing Dose (TID) refers to the cumulative ionizing energy deposited by incident radiation. The effects of TID on MOS devices are caused by deposition in the insulating oxide layers of a device, resulting in trapped charge in the device oxide and interface traps at the silicon-oxide interface. The ionizing radiation generates electron-hole pairs within the oxide. If an electric field is present in the oxide, the electrons and holes will immediately move in opposite directions – electrons in the direction of higher potential and holes in the direction of lower potential. Electrons are highly mobile compared to holes and will be quickly transported out of the oxide, while holes will drift more slowly to the oxide interface. Some of these carrier pairs will recombine before all of the electrons are swept out of the oxide in an "initial" recombination. The fraction of holes that remain after the initial recombination is the "charge yield", and is highly dependent on the magnitude of the electric field present in the oxide. In MOS structures, if a positive gate bias is applied, these un-recombined holes will transport to the $Si/SiO_2$ interface. This transport is slow, and occurs primarily through "polaron hopping" between localized states. When the holes get near the $Si/SiO_2$ interface, a fraction of the holes become trapped in oxygen vacancies created by out-diffusion from the oxide. The build up of this trapped charge in the oxide near the interface is one of the factors caused by TID that degrades MOS device performance. Trapped holes are generally neutralized with time by electrons available through tunneling or thermal emission. These

electrons don't remove the trapped holes, and if a reverse bias is applied much of the trapped charge will be restored [19].

The hopping process by which holes transport in $SiO_2$ causes an energy exchange in the oxide lattice, resulting in a release of protons. In the presence of an electric field, these protons migrate to the $Si/SiO_2$ interface and form interface traps. Additionally, defects in the $SiO_2$ structure caused by ionizing radiation straining chemical bonds can trap holes and can additionally create interface traps (Figure 3.3) [20,21,22].

In planar MOS transistors, the accumulation of charge due to TID causes three primary changes in device performance: a shift in threshold voltage, transconductance degradation, and increased leakage current (Figure 3.4). TID causes trapped charge to build up in the oxides of MOS transistors. The location of accumulated charge is crucial to the effect that it has on device performance. The planar MOS platform has two major variants: bulk and silicon on insulator (SOI). Bulk devices have channels that are directly connected to the substrate, while SOI devices have an insulating layer, a buried oxide (BOX), between the channel and the substrate. In modern

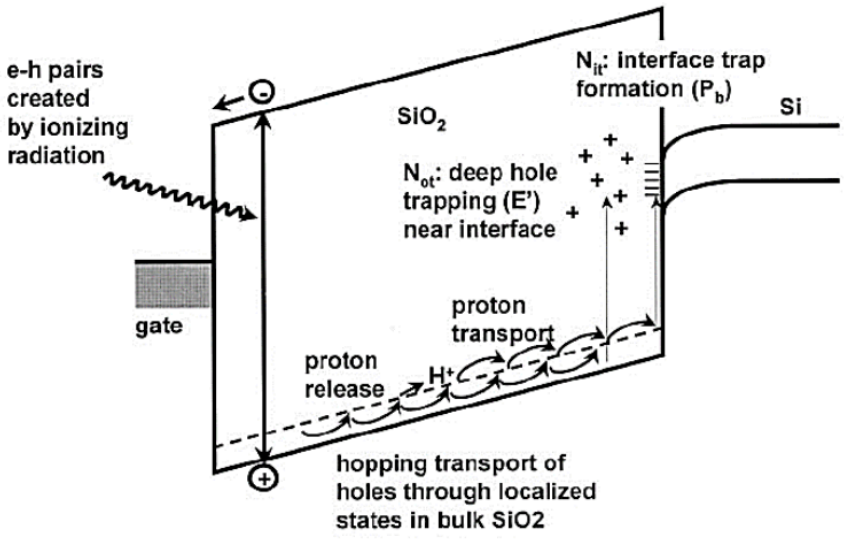


*Figure 3.4: Band diagram depicting the physical mechanisms of TID in a p-substrate MOS capacitor. (From [20] McLean, 1980)*

bulk devices, the primary location of trapped charge that affects device performance is in insulating regions that electrically isolate separate devices on the same semiconductor wafer, typically consisting of $SiO_2$. For modern SOI devices, charge trapped in the BOX dominates the TID response.

For devices in older technology nodes that feature relatively thick gate oxides, charge that accumulates in the gate oxide modulates the effectiveness of an applied gate voltage. The typically positive charge accumulated at the silicon-oxide interface decreases the voltage needed to invert the channel. For n-channel devices, if enough charge is accumulated, the device will remain "on", passing a substantial amount of current, at zero applied volts. For p-channel devices with negative threshold voltages, accumulated charge in the gate oxide increases the threshold voltage magnitude, making the devices harder to turn on. Radiation-induced threshold voltage shift has become far less significant in highly scaled devices due to the decrease in gate insulator volume and decrease in supply voltages, both decreasing the charge accumulation in the gate oxide.

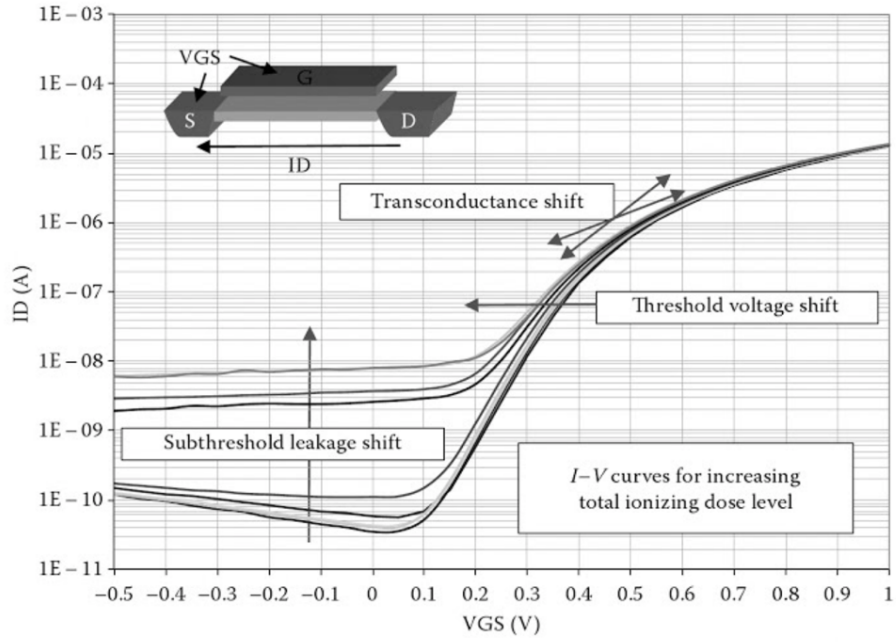


*Figure 3.5: I-V curves for a 90nm bulk NMOS device exposed to total ionizing dose radiation. (From [23] Massengill, 2013)*

Generated charge in thin insulators is readily able to escape through tunneling or other transport mechanisms, and as such, devices with gate oxide thicknesses of 10nm or less show essentially no threshold voltage shift [20, 21].

Transconductance degradation in MOS transistors is caused primarily by generated interface traps allowing for charge exchange with the channel. Additional degradation is caused by trapped charge at or near the channel of the device. Interface traps and near-interface trapped charge degrade the mobility of carriers in the channel, resulting in decreased transconductance. Degradation in transconductance can critically affect a device by causing incomplete switching or a delay in signal propagation [21].

Radiation induced leakage current is one of the most pressing issues for modern highly scaled devices, as its effects are enhanced by decreasing feature sizes. A common modern technique to electrically isolate transistors from another is by use of shallow trench isolation (STI), the formation of an insulating oxide trench that surrounds the device. STI oxides are larger and of lower quality than the gate oxides, causing them to be far more susceptible to charge trapping from TID irradiation. In NMOS devices, trapped charge in the STI of a device can cause a leakage path from source to drain along the edge of the STI, known as “edge leakage”. This increases the drain current while a device is in the off state. In both NMOS and PMOS, trapped charge in the STI can also result in leakage across the STI between the two different devices being isolated [21,22].

### 3.3 Total Ionizing Dose Effects in FinFETs

Because FinFETs have largely been adopted by major electronic manufacturers to succeed planar CMOS, a significant amount of research has been conducted regarding the radiation response of FinFET geometries. While the mechanisms of charge capture and the resulting

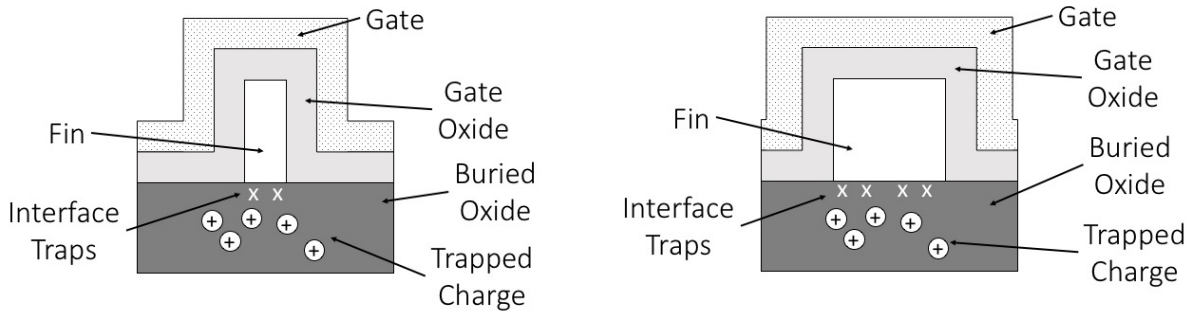


*Figure 3.6: Diagram illustrating relative positions of interface traps and oxide trapped charge in the BOX of a narrower fin SOI FinFET (left) and wider fin SOI FinFET (right). Not to scale.*

degradation in performance are nearly identical to that of planar CMOS, the three dimensional nature of FinFETs adds complexity to the device response to cumulative dose.

*3.3.1 TID in SOI FinFETs*

In SOI FinFETs, as with planar MOSFETs, the primary degradation of performance from TID is caused by charge deposited in the BOX of the device. Charge trapped in the BOX couples with the gate, resulting in threshold voltage modulation. Trapped charge near the oxide-channel interface can also cause some subthreshold slope degradation. Interface traps on the BOX-channel interface additionally degrade the subthreshold slope. The lateral gates of SOI FinFETs enhance the electrostatic control over the channel, helping to screen it from the effects of trapped charge in the oxide. The effectiveness of the lateral gate screening is dependent on the fin-width, meaning that the fin-width of an SOI device is an extremely significant factor in regards to its TID sensitivity. In addition, the area of the buried oxide that is in contact with the conducting channel is proportional to fin-width as pictured in Figure 3.6, meaning that larger fin devices have larger quantities of trapped charge in the BOX near the channel [24]. Because of these factors, SOI FinFETs with smaller fin widths tend to be much more resistant to TID than those with larger fin

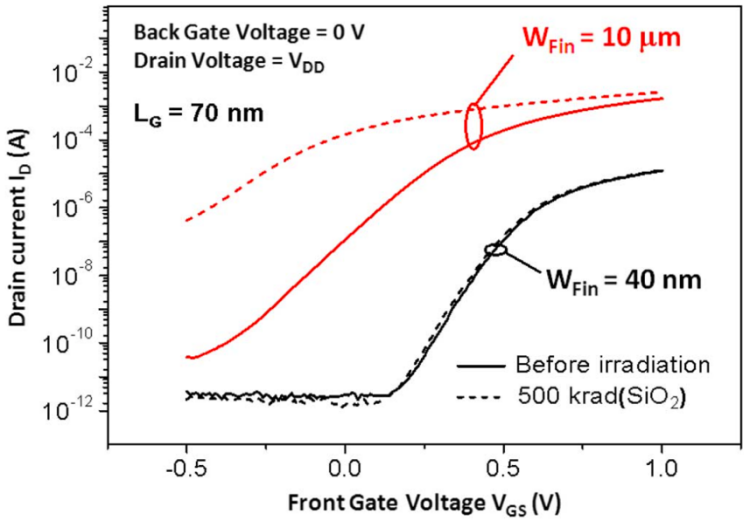


*Figure 3.7: $I_D$-$V_{GS}$ curve of SOI MuGFETs with various fin widths, both before irradiation and after 500 krad($SiO_2$). The gate length is 70 nm. The bias condition is "OFF". (From [34] Simoen et. al., 2013)*

widths [5], as demonstrated in Figure 3.6. The worst-case bias condition for SOI FinFETs is process and structure dependent. Partially depleted and some fully depleted SOI transistors and have worst-case TID conditions in transmission gate bias, with the source and drain held at $V_{DD}$ and the gate and body grounded [25, 26]. Other SOI technologies have been shown to be worst case with the "on" bias, with the drain held at $V_{DD}$ and all other terminals grounded [27,28,29].

*3.3.2 TID in Bulk FinFETs*

For bulk FinFETs, like in the planar bulk devices discussed previously, the primary degradation in performance is caused by the buildup of trapped charge and interface traps in the isolation oxide. Interface traps and border trapped charge degrade device transconductance, and charge trapped in the oxide enable parasitic leakage paths. High electric fields present in the corners of the STI during device operation especially enhance the increase leakage response [30]. Opposite SOI devices, bulk devices with narrower fins are more susceptible to TID damage than larger fin devices. For devices with narrower fins, trapped charge and interface traps are much closer to the center of the channel than for devices with wider fins, as depicted in Figure 3.8.

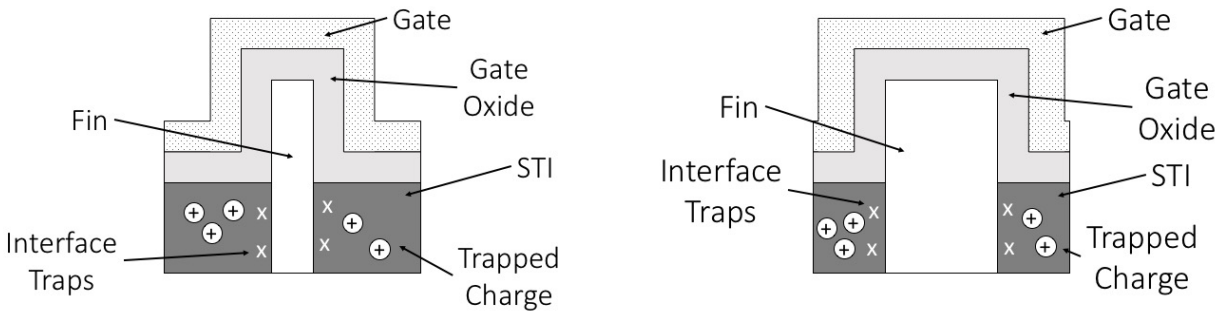


*Figure 3.8: Diagram illustrating relative positions of interface traps and oxide trapped charge in the STI of a narrower fin bulk FinFET (left) and wider fin bulk FinFET (right). Not to scale.*

Because of this, the same amount of accumulated dose in the STI of a narrow fin device is has a greater effect than it would in the STI of a wide fin device. Unlike trapped charge and interface traps in the BOX of SOI FinFETs, the amount of trapped charge near the channel and traps on the interface are not proportional to the fin-width for bulk devices. Figure 3.9 demonstrates the TID response of devices with different fin widths. Figure 3.10 depicts simulations from Chatterjee et al., illustrating the induced off-state leakage paths in a narrow and wider fin geometry. Off-state

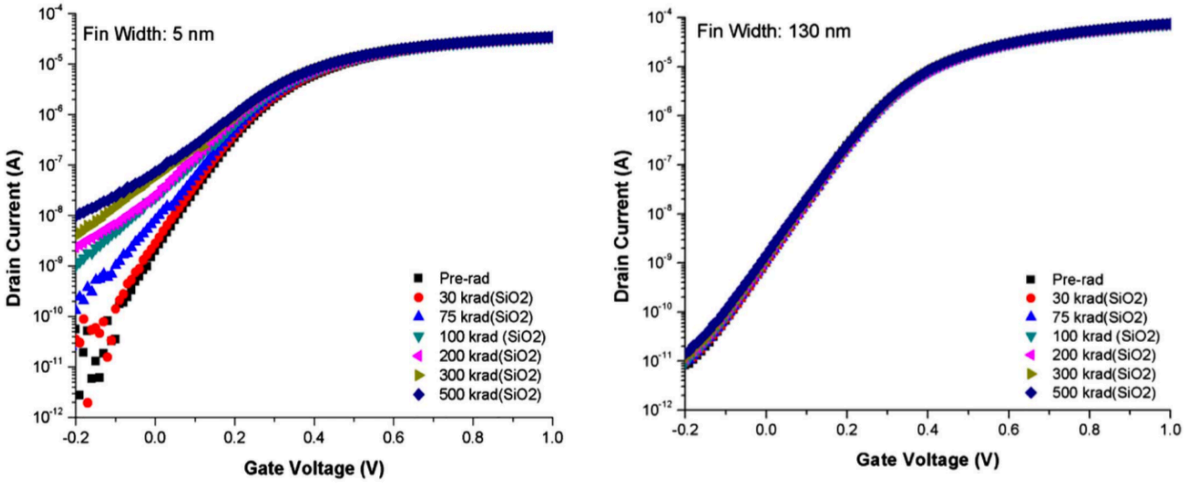


*Figure 3.9: $I_D$-$V_{GS}$ curves of bulk FinFETs with various fin widths as a function of dose. The gate length is 70 nm. The bias condition is "OFF", measurement condition is $V_D$ = 50 mV. (From [36] Chatterjee et. al., 2014)*

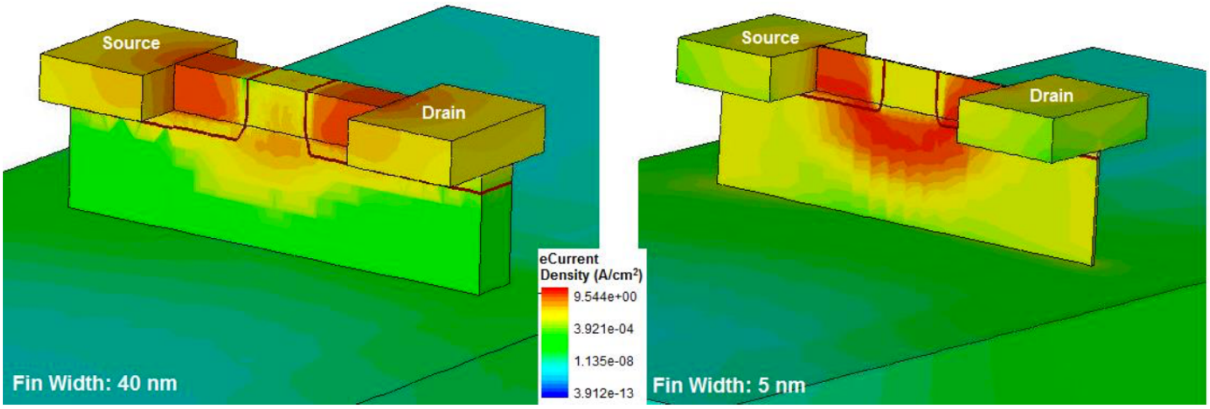


*Figure 3.10: TCAD simulation of electron current density in FinFETs with different fin-widths after irradiation, showing greater subsurface leakage in the 5nm fin-width. (From [36] Chatterjee, 2014)*

leakage is induced by a parasitic subsurface transistor, which is turned on by charge accumulated in the STI. The subsurface leakage is shown to be far greater in the narrower fin geometry [31,32]. Unlike SOI devices, the worst-case bias condition for TID irradiation of these devices has been found to be "OFF", with the drain positively biased and the source and gate grounded.

Further simulations and experiments on the geometry dependence of TID in both SOI and bulk FinFETs also showed that longer channel devices experienced less leakage due to the decreased possible drain current in the parasitic transistor. FinFET devices with increased pitch experience greater leakage than those with narrower pitch, because wider pitch increases the effective thickness of the STI, allowing more more trapped charge to reach the STI – silicon interface [31].

### 3.4 Low Temperature Hole Trapping and Interface Trap Generation in MOS Devices

When ionizing radiation generates electron hole pairs in the oxides of MOS devices at cryogenic temperatures, the response is significantly changed. Like at room temperature, electrons are quickly swept away from the point of generation and out of the oxide. However, at temperatures below 120 K, generated holes are immobilized near where they originated, as opposed to becoming

trapped in defect sites in the oxide [33]. Because of this immobilization, hole trapping efficiency is increased to nearly 100% for the generated holes [34]. These "trapped" holes can be removed either through electron tunneling from the interface, or by simply raising the oxide temperature enough that the holes are able to transport via polaron hopping. Because the low temperature hole trapping does not necessarily occur at defect sites, the hole yield in the oxide of a devices irradiated at cryogenic temperature is largely process dependent and remains high for oxides hardened to charge trapping at room temperature [33].

Generation of long term interface traps in MOS devices at cryogenic temperatures, however, has been shown to be significantly decreased. Saks et al. found that the interface trap density decreased by up to a factor of 300 in the large p-channel transistors tested in [35]. The mechanism for generating interface traps by proton transport to the interface is frozen out at temperatures below 200 K [46]. Raising the temperature of cryogenically irradiated devices to this threshold allows the generated holes to begin polaron hopping, freeing protons to transport to the interface and form interface traps with the same density as would have been generated at room temperature. Devices still experienced radiation-induced degradation in operation at low temperatures. This work presented the model that the degradation at low temperatures, in particular the degradation in subthreshold slope, is primarily due to lateral non-uniformities (LNUs) modulating the electric field in the channel [35, 36, 37]. LNUs have a greater effect on devices at low temperatures because of the increased hole trapping, which provides the charge for greater non-uniformities. Additionally, because the subthreshold slope is significantly enhanced at cryogenic temperatures, the degradation due to LNUs is more significant [35, 36].

### 3.5 Summary

In this chapter, key concepts on device operation in cryogenic conditions were described. Cryogenic temperature was shown to alter device performance because of increased electrical mobility and decreased carrier concentrations. A brief summary of the mechanisms behind radiation damage and the resulting effects on planar and FinFET transistor technologies was explored. The TID response of FinFET devices was shown to be highly dependent on device geometry. Previous work on oxide hole trapping and interface trap generation at low temperatures and the related effects were discussed.

CHAPTER IV

DEVICE AND EXPERIMENT DETAILS

## 4.1 Device Details

This work utilizes bulk and n- and p-FinFET devices that were fabricated at imec. The device cross sections are pictured in Figure 4.1. All device fin heights are 60nm, with 200nm fin pitch. The gate lengths utilized were 1um. FinFETs with fin widths of 15nm and 40nm were tested. The gates of the devices utilize a high-k dielectric of 2.3 nm HfSiON (EOT 0.641 nm $SiO_2$) on a 1 nm interfacial oxide. The metal gates are made of 5nm of TiN, and are covered in 100 nm of poly-crystalline silicon. Epitaxial growth of Silicon followed by NiPt silicidation was used to form the source and drain access regions [38].

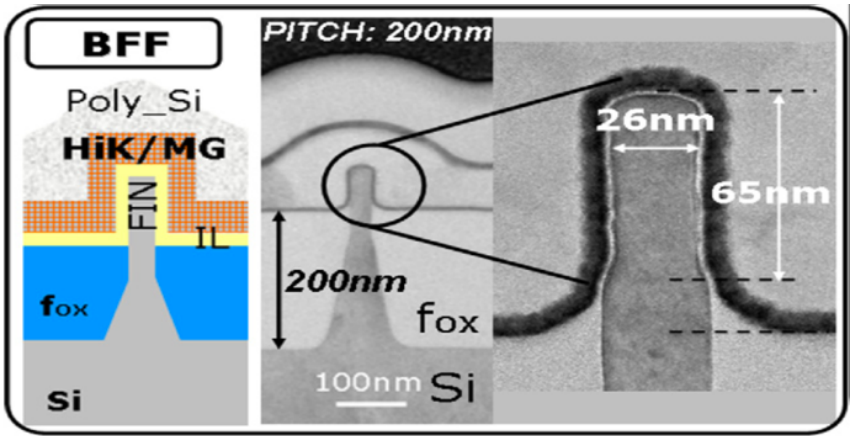


*Figure 4.1: Bulk and SOI FinFET gate stacks. (from [39] Chiarella, 2010)*

## 4.2 Cryogenic Irradiation Experiment Details

In order to test devices at cryogenic temperatures, this work utilizes a custom dewar that uses liquid nitrogen to cool a low temperature chamber that can host electrical devices. Packaged devices are mounted to a brass "cold-finger" that thermally connects the device to the dewar's liquid cryogen tanks. The chamber is held under vacuum to thermally isolate the liquid nitrogen

tanks and low temperature components from the room temperature shielding. Vacuum sealed ports allow for electrical access to the device through K-connector feedthroughs. Temperature inside the dewar is be monitored by a Lakeshore 331 Temperature Controller through two Silicon diodes fixed in the low temperature chamber. One diode is attached to the cold plate, and the other is attached to the cold finger next to the device.

*Figure 4.2: Internal view of the Vanderbilt dewar from the bottom with a packaged device.*

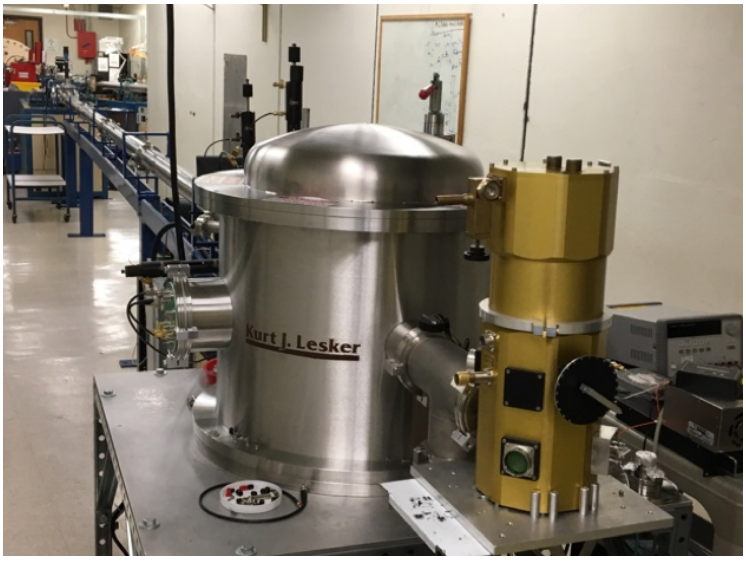


*Figure 4.3: Dewar connected by vacuum flange to the Vanderbilt Pelletron in order to perform cryogenic irradiations.*

Inside the chamber, high speed minibend cables are used to connect the high speed package to the inside of the electrical feedthrough (Figure 4.2). Copper braid is used to short the thermal connection between the cold finger and the cold plate, to increase the cool down rate and lower the achievable temperatures.

The dewar shielding has an opening that allows for irradiation in the vacuum sealed environment. For experiments in this work, the dewar was attached to the Vanderbilt Pelletron with a vacuum sealed flange, allowing the dewar and the Pelletron to share the same vacuum environment (Figure 4.3, Figure 4.4). The cold finger positions mounted devices at the center of the shield opening in order to apply proton dose to the device. Devices were irradiated with 1.8 MeV protons. Both room temperature and cryogenic irradiations are performed inside the dewar in order to maintain near identical conditions.

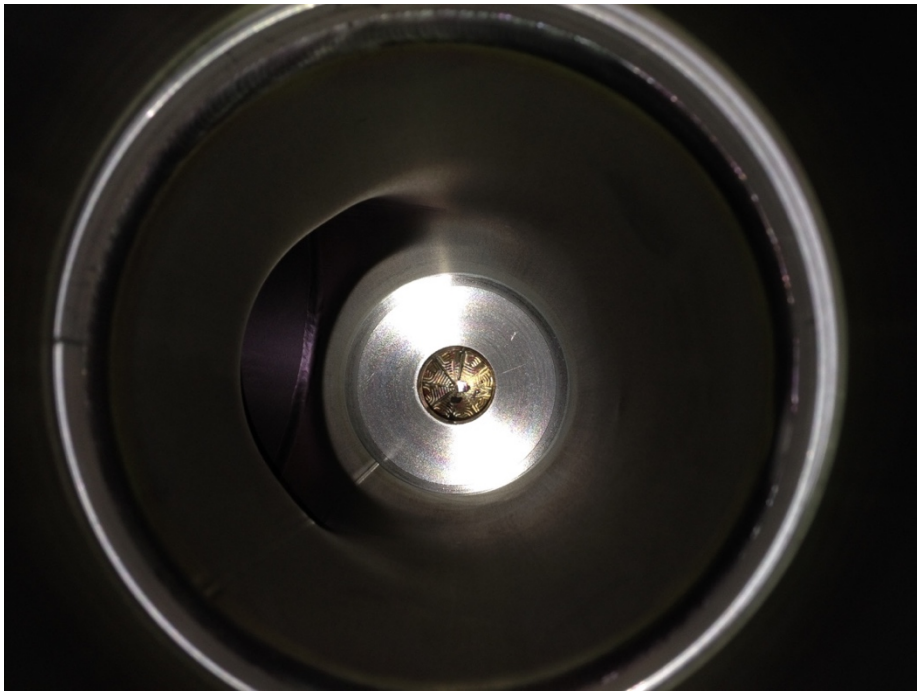

*Figure 4.4: Mounted and packaged device inside the dewar pictured through the beam-line of the Pelletron..*

# CHAPTER V

# EXPERIMENTAL RESULTS AND DISCUSSION

This chapter presents and discusses the results from experiments regarding the effects of temperature on bulk Silicon FinFET device operation and total ionizing dose response. Results from cryogenic irradiation experiments are compared with experimental results from duplicate devices irradiated at room temperature.

## 5.1 Bulk n-FinFET Operation at Cryogenic Temperatures

This section investigates the operation of bulk Silicon n-FinFET devices at cryogenic temperatures for two different fin-widths, with gate lengths of 1μm. Both devices were mounted on one high speed package, with source terminals tied to ground, and drain and gate terminals wired to a feed-through. Measurements were performed consecutively for both devices at each temperature step by biasing the drain terminals at 50 mV and sweeping the gate voltages.

Figure 5.1 shows I-V characteristics at decreasing temperatures for two different fin widths (15 nm and 40 nm). Because the devices were biased with relatively small drain voltages, the drain current in the linear on-state and the subthreshold regions can be represented by Equations 3.3 and 3.7 respectively. In the measured devices, for gate voltages biasing the devices in the linear region, $I_D$ increased with decreasing temperatures, following the previously discussed linear relationship with mobility. For subthreshold gate voltages, $I_D$ decreased with decreasing temperatures, following the discussed decreased diffusive transport.

Figure 5.2 shows the $g_m$-V characteristics for the two devices as a function of temperature. As temperature was decreased, the peak transconductance is shown to have both to increased and to shifted to higher gate voltages due to the increase in threshold voltage.

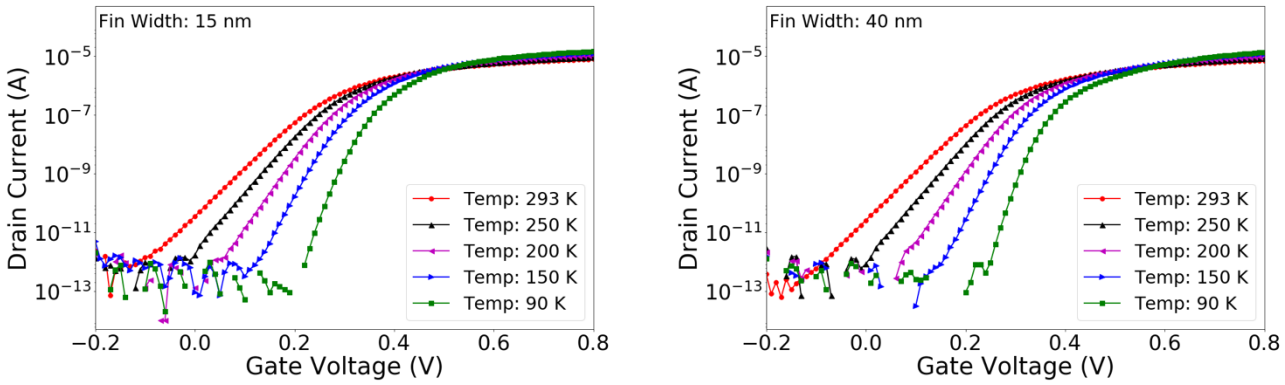


*Figure 5.1: $I_D$ - $V_G$ characteristics at various temperatures for bulk Silicon n-FinFETs with 1μm gate length, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV.*

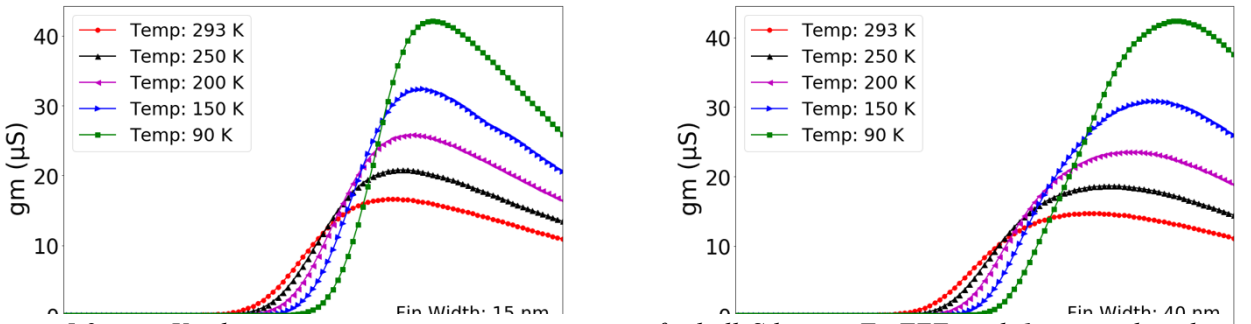


*Figure 5.2: $g_m$ - $V_G$ characteristics at various temperatures for bulk Silicon n-FinFETs with 1μm gate length, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV.*

The peak transconductance, plotted in Figure 5.3(a), is shown to be increasing with decreasing temperature, in agreement with the previously discussed proportional relationship with mobility described in Equation 3.4. The extracted values linearly increase on a semi-log plot with decreasing temperature, indicating an exponential relationship between effective mobility and temperature. In lightly doped silicon, the electron mobility has been shown by [40] to be dominated by lattice scattering in the temperature range of this work, proportional to $T^{-\eta}$, where $\eta$ is a constant. From the measured data, $\eta$ was found to be 2.05 for the 15 nm fin width device, and 2.06 for the 40 nm fin width device.

The shift in threshold voltage with respect to temperature is plotted in Figure 5.3(b). Threshold voltage was calculated using Extrapolation in the Linear Region [41]. Following with the previously discussed relationship between threshold voltage and intrinsic carrier concentration,

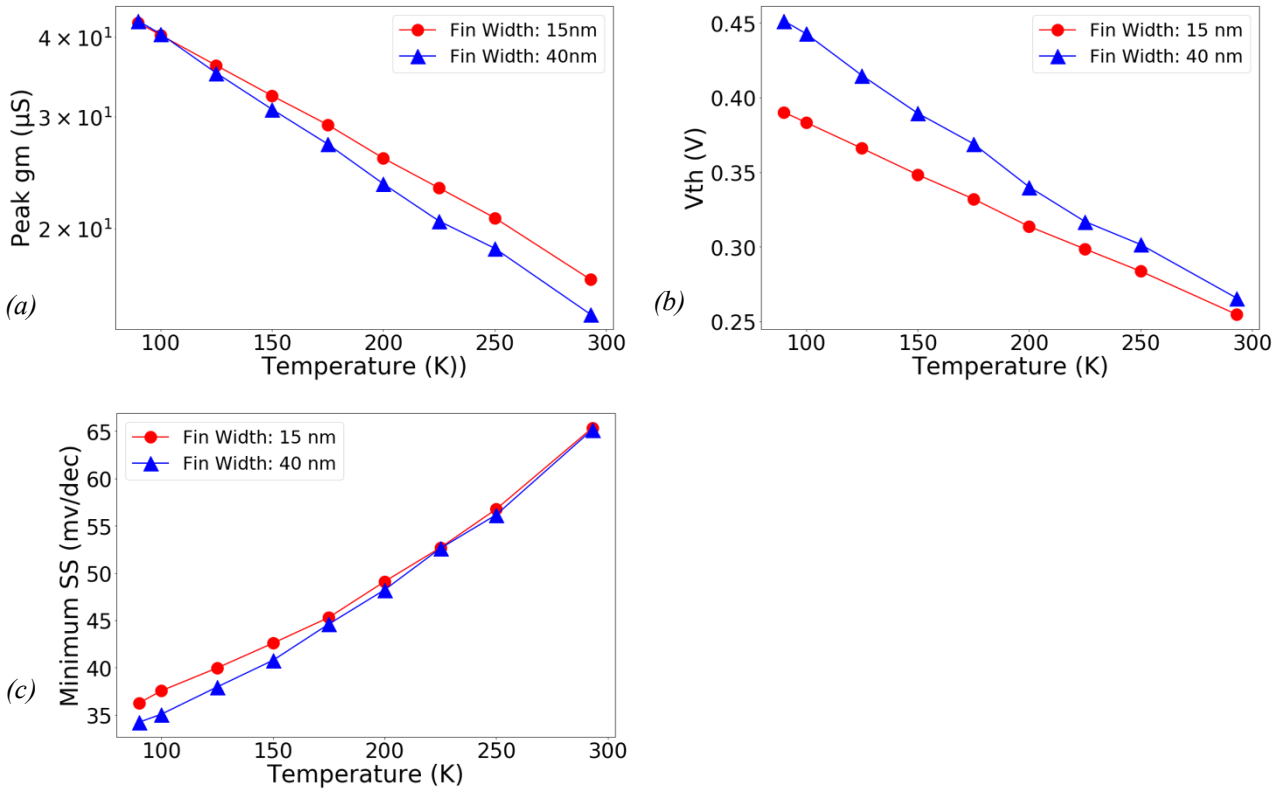


*Figure 5.3: Peak transconductance (a), threshold voltage (b), and subthreshold swing (c) as functions of temperature for bulk Silicon n-FinFETs with 1μm gate length, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV.*

the threshold voltage magnitude is shown to be increasing with decreasing temperatures. That relationship is also shown to be approximately linear, following with the common approximation described in Equation 5.1, where $T_0$ is a reference temperature and $\alpha_{VT}$ is a negative constant [42,43].

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0) \qquad \text{(Equation 5.1)}$$

For the narrow fin-width device, over the temperature range of 293 K to 90 K, the threshold voltage changed by $\alpha_{VT}$ = ~ -0.67 mV/K. The larger fin-width device's threshold changed by $\alpha_{VT}$ = ~ -0.92 mV/K. A possible explanation for the decreased constant in the linear threshold voltage-temperature relationship for the smaller fin-width device is a difference in surface potential. As described in [47], which examined the high temperature operation of MuGFETs,

threshold voltage temperature dependence not only comes from bulk potential, but also from the surface potential. In FinFETs, surface potential is dependent on fin width [47]. Devices with smaller fin widths have increased Silicon film capacitances, which causes the surface potential to be less dependent on temperature. This in turn decreases the temperature dependence of the threshold voltage, as shown in Equation 5.2 [48,49], where $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the Silicon film capacitance.

$$V_T = \phi_S^* + V_{FB} + \frac{Q_D}{2C_{OX}}\sqrt{1 + \frac{2kTC_{OX}}{qQ_D}} \qquad \text{(Equation 5.2 (a))}$$

$$\phi_S^* = 2\phi_F + \frac{kT}{q}\ln\left(\frac{C_{OX}}{4C_{Si}}\frac{1}{1-\exp\left(-\frac{q}{kT}\frac{Q_D}{8C_{Si}}\right)}\right) \qquad \text{(Equation 5.2 (b))}$$

The minimum subthreshold swing of the devices is shown in Figure 5.3(c) to be decreasing with decreasing temperature, following the relationship described in Equation 3.7. Although the relationship between subthreshold slope and temperature is described to be linear in Equation 3.7, the plots themselves suggest a nonlinear relationship. This non-linearity matches findings by [50], in which SIMOX devices experienced sub-linear variation of subthreshold swing with very low temperature. The explanation for this decreased variation at very low temperatures is the increase in interface trap capacitance [50]. As Equation 3.8 shows, the subthreshold swing is dependent on both temperature and the capacitive coupling between the oxide and the channel. As temperature decreases, the Fermi level approaches the edges of the band-gap, rapidly increasing the interface trap capacitance [50]. This increase in capacitance diminishes the variation with temperature as temperature decreases. As the temperature dropped from 293 K to 90 K, the subthreshold swing for the 15nm device decreased from ~65 mV/dec to ~36 mV/dec, and the subthreshold swing for the 40nm device decreased from ~65 mV/dec to ~34 mV/dec.

| | $g_m$ (μS) | | $I_{dsat}$ (μA) | | SS (mV/dec) | | Vth (V) | |
|---|---|---|---|---|---|---|---|---|
| Temp. (K) | FW = 15 nm | FW = 40 nm | FW = 15 nm | FW = 40 nm | FW = 15 nm | FW = 40 nm | FW = 15 nm | FW = 40nm |
| 293 | 16.6 | 14.7 | 1.24 | 1.13 | 65.4 | 65.2 | 0.255 | 0.266 |
| 250 | 20.8 | 18.6 | 1.55 | 1.50 | 56.8 | 56.2 | 0.284 | 0.301 |
| 225 | 23.2 | 20.6 | 1.61 | 1.56 | 52.7 | 52.6 | 0.298 | 0.317 |
| 200 | 25.8 | 23.5 | 1.89 | 1.94 | 49.1 | 48.2 | 0.314 | 0.34 |
| 175 | 29.1 | 27.2 | 2.16 | 2.16 | 45.3 | 44.6 | 0.332 | 0.369 |
| 150 | 32.4 | 30.8 | 2.2 | 2.34 | 42.6 | 40.8 | 0.348 | 0.39 |
| 125 | 36.1 | 35.1 | 2.51 | 2.79 | 40 | 37.9 | 0.366 | 0.415 |
| 100 | 40.3 | 40.5 | 2.89 | 3.26 | 37.5 | 35.1 | 0.383 | 0.443 |
| 90 | 42.1 | 42.4 | 3.13 | 3.45 | 36.2 | 34.2 | 0.39 | 0.451 |

*Table 5.1: Key device parameters at temperatures from 293 K to 90 K for two bulk Silicon n-FinFETs with 1μm gate lengths, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV.*

While these devices are not being directly compared to planar MOS technologies, the comparatively low channel doping in FinFETs would result in more significant improvements in mobility. Table 5.1 details the values of key device parameters at various temperatures. Both the peak transconductance and the on-state current (which is calculated at arbitrary voltage $V_G = V_{TH}$ + 0.3 V) are shown to be increased with temperature, confirming the dependence with mobility discussed previously.

### 5.2 TID Effects in Bulk n-FinFETs at 293 K and 89 K

This section reports on the total ionizing dose response of bulk Silicon FinFETs at cryogenic temperatures, compared to the response at room temperature, for the two geometries. Like the previously described cryogenic experiments, a device of each geometry was mounted to the same high speed package with its source terminals grounded and its drain and gate terminals wired to the electrical feed-through. For the cryogenic irradiation, both geometries were mounted in the low temperature chamber, cooled to cryogenic temperatures, then irradiated simultaneously. The TID response was measured at several dose steps up to 1 Mrad(Si) while the temperature was maintained at 89 K. For the room temperature irradiation, separate devices with the same geometry

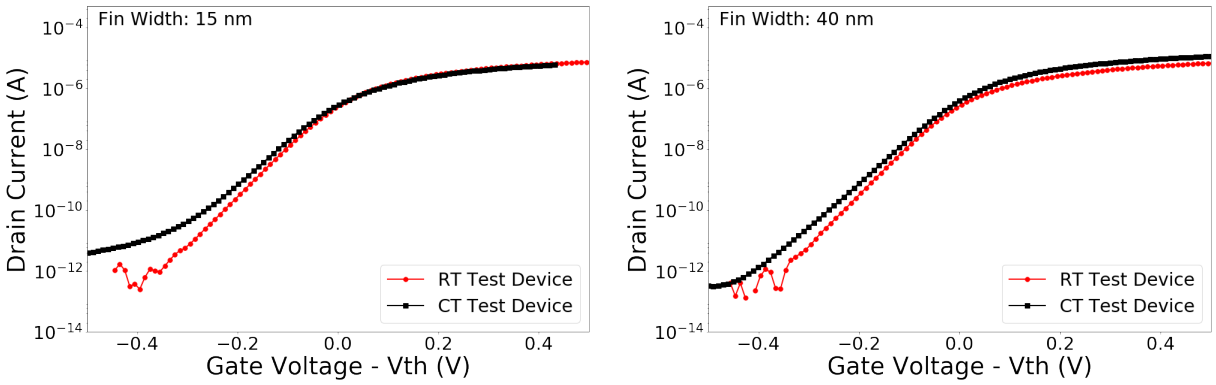


*Figure 5.4: Room temperature pre-irradiation comparison of the devices used in each experiment, for bulk Silicon n-FinFETs with 1μm gate length, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV. "CT" devices were used for cryogenic tests. "RT" devices were used for room temperature tests.*

and comparable behavior were mounted in the low temperature chamber and irradiated simultaneously without being cooled. These duplicate devices were from a different location on the wafer and bonded to a different package than the original devices, so some part to part variation is apparent as depicted in Figure 5.4.

Irradiation was performed with 1.8 MeV protons. Devices were biased in the "OFF" configuration, which was determined by [31] to be the worst case for TID in bulk FinFETs at room temperature. Drains were biased at 0.7 V, and gates and sources were grounded. Figure 5.5 shows the I-V characteristics of the 15 nm and 40 nm fin width devices at room temperature and at 89 K as a function of applied dose. For both cryogenic and room temperature irradiations, the 15 nm fin- width device proved to be much more vulnerable to TID than the 40 nm fin-width device. This demonstrates that the increased total dose sensitivity of narrow fin-width bulk FinFETs holds for cryogenic temperatures. For gate voltages less than 0 V, radiation induced drain leakage current was less for the devices irradiated at cryogenic temperatures than for those irradiated at room temperature. This is because trap assisted tunneling and parasitic STI leakage channels are decreased at lower temperatures [44].

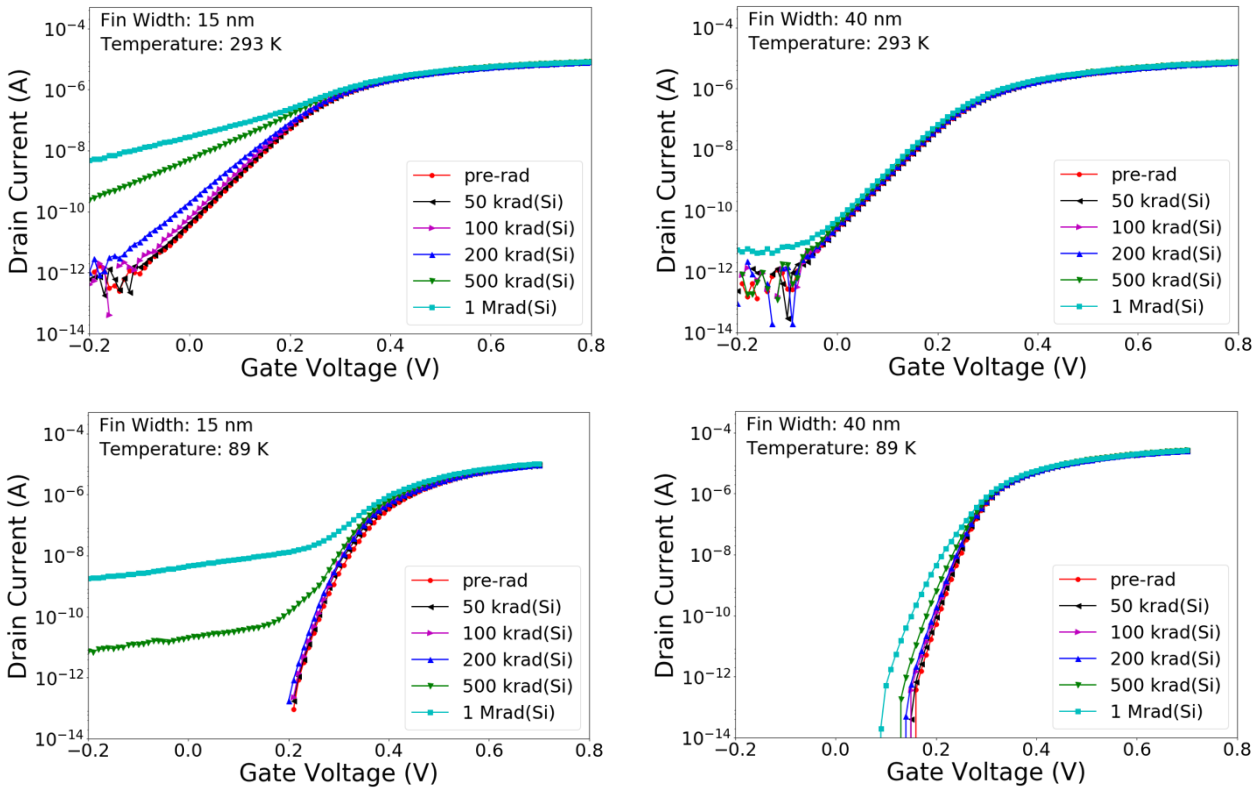


*Figure 5.5: Room temperature and cryogenic temperature I-V characteristics for bulk Silicon n-FinFETs with 1μm gate length, 5 fins, at two different fin widths, measured at $V_D$ = 50 mV.*

Normalized peak transconductance is plotted in Figure 5.6(a). For the devices irradiated at room temperature, the peak transconductance slightly increased with increasing dose, while for the devices irradiated at cryogenic temperature the transconductance first slightly increased, then decreased. The increase in transconductance at lower doses is potentially due to a balancing that takes place between radiation induced trapped charge and defects present in the pre-irradiated devices. Presented in a model by Subramanian et. al., at lower doses the generated interface and oxide fixed charge traps can negate the degradation caused by existing defects by balancing charge and diminishing the interaction with the channel [45]. At lower temperatures, interface trap generation is significantly diminished, resulting in the devices irradiated at cryogenic temperatures not experiencing the same enhancement in transconductance.

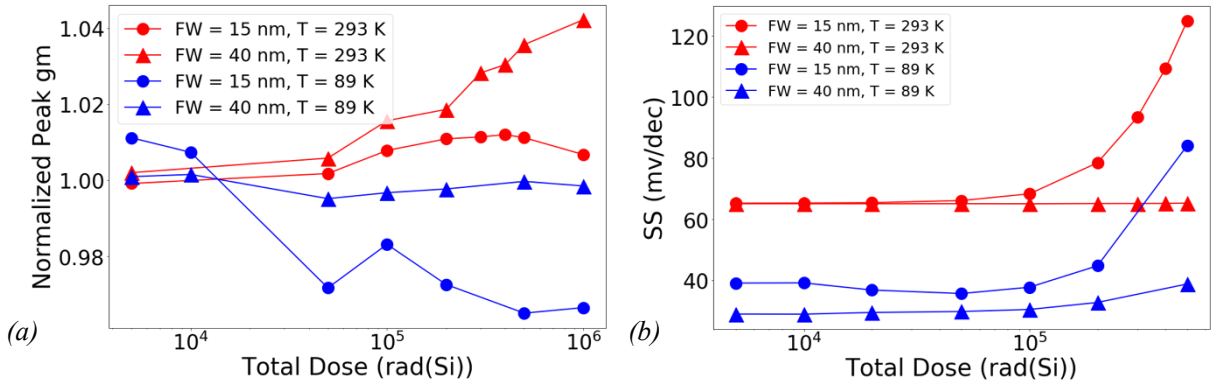


*Figure 5.6: Normalized peak transconductance (a) and subthreshold swing (b) as functions of dose for all devices under consideration. Measured at $V_D$ = 50 mV.*

The minimum subthreshold swing response of the devices is pictured in Figure 5.6(b). The 15 nm fin-width device irradiated at room temperature experienced the greatest degradation in subthreshold swing, increasing by ~99 mV/dec. The 15 nm fin-width device irradiated at 89 K increased by ~45 mV/dec. The 40 nm fin-width device irradiated at room temperature increased by ~1 mV/dec, and the 40 nm fin-width device irradiated at 89 K increased by ~10 mV/dec. The devices that were irradiated at cryogenic temperature show better subthreshold swing characteristics at 1 Mrad(Si) dose than their counterparts irradiated at room temperature. However, the relative degradation of subthreshold swing compared to the pre-rad condition is greater at cryogenic temperatures. In room temperature irradiations, degradation in subthreshold slope is primarily attributed to charge exchange with interface traps and near-interface trapped charge. For low temperature irradiations, subthreshold swing degradation is primarily attributed to LNUs modulating the electric field in the channel, enhanced by the increase in hole trapping. The narrower fin-width devices at both temperatures would be more affected by applied dose, due to the closer proximity of traps and LNUs to the center of the fin. However, large increase in experimental subthreshold swing measurements for the 15 nm fin-width devices is most likely due to the increased leakage current affecting the slope of the IV curve.

### 5.3 TID Effects in Bulk p-FinFETs at 293 K and 89 K

Room temperature and cryogenic irradiations were also performed on two p-type bulk FinFETs of the same geometry, with 40 nm fin-widths and 1 μm channel lengths. The I-V characteristics of these devices as a function of applied dose are plotted in Figure 5.7. The irradiation conditions on these devices were all terminals grounded, and measurement coonditions were drain biased at -200 mV and gate voltage swept.

Like the n-channel devices, degradation in performance is primarily due to electron-hole pair generation in the STI. Interface traps exchange energy with the channel, and lateral nonuniformities in the oxide modulate the electric field in the channel. For p-type devices, positive charge build up in the lateral STI near the channel also prevent inversion in that region, decreasing the effective width of the channel [51]. As shown by equations 3.3 and 3.4, this degrades the drive current and transconductance of irradiated p-type devices.

The minimum subthrehsold swing degradation after irradiation for the measured devices was negligible, degrading less than 1 mV/dec for both devices. The normalized peak transconductance is plotted in Figure 5.8. The device irradiated at cryogenic temperatures experienced a greater shift in normalized peak transconductance, likely due to the increased hole trapping causing a greater degradation due to increased effective width degredation. Noteably, both the devices experienced immediate degradation in transconductance. This can be attributed to the nature of the radiation-induced defects. In p-type devices in saturation, interface traps and positive trapped oxide charge tend to reinforce each other, rather than compensate like in n-type devices [51].

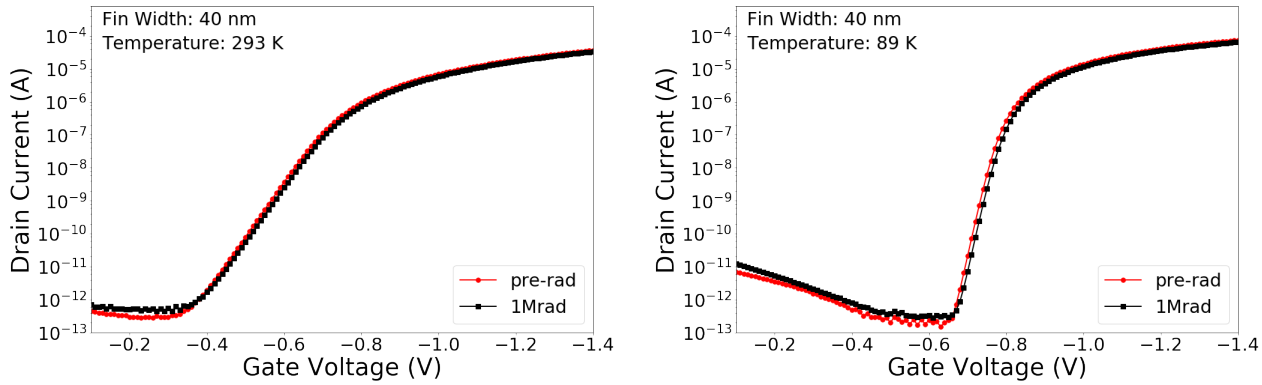


*Figure 5.7: Room temperature and cryogenic temperature I-V characteristics for bulk Silicon p-FinFETs with 1μm gate length, 5 fins, two different fin widths, irradiated with all ports 0 V, and measured at $V_D$ = 200 mV.*

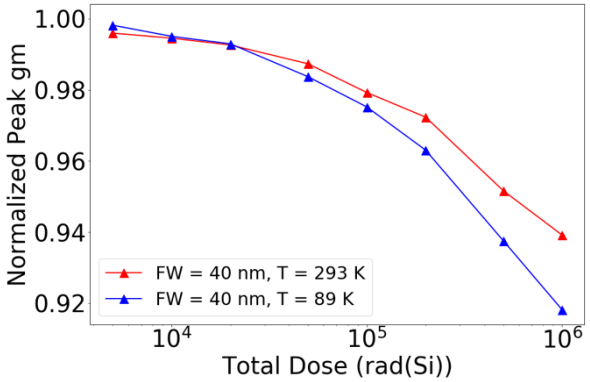


*Figure 5.8: Normalized peak transconductance as a function of dose for devices under consideration. Measured at $V_D$ = -200 mV.*

While p-type devices are typically more radiation hard because the positive charge trapped in the oxides are directed away from the channel, the minimal radiation response of these transistors compared to the n-type devices is more likely due to the irradiation condition. During irradiation these devices were biased with all terminals grounded, meaning that no (or minimal) electric field was present across the oxide. Because of this, generated electron and hole pairs would not be quickly separated, and many would likely recombine.

### 5.4 Summary

The bulk n-FinFETs tested for pre-rad cryogenic operation exhibited similar responses to those seen in planar FETs. At decreasing temperatures, the devices experience increases in

transconductance, saturation current, and threshold voltage, and decreases in subthreshold swing. Different fin-widths lead to slightly different magnitudes of effect, with the larger fin-width device having a greater threshold voltage increase. Bulk n-FinFET devices irradiated at both cryogenic and room temperatures demonstrated the difference in total dose response for the two fin-widths. At 1 Mrad, the devices irradiated at cryogenic temperatures still displayed superior performance to the devices irradiated at room temperature. Radiation induced off state leakage was diminished at lower temperatures, but relative subthreshold swing and peak transconductance degradation was enhanced. P-type FinFETs irradiated at cryogenic and room temperature showed similar greater transconductance degradation, but results were limited by the experimental bias condition.

# CHAPTER VI

# CONCLUSIONS

The goal of this work was to explore the cryogenic total ionizing dose response of FinFET devices to examine their capability for use in extreme space environments. This work has presented data on the cryogenic operation of Silicon bulk FinFET devices, and experimental results from room temperature and cryogenic proton irradiations. While these results are far from conclusive, they do provide a methodology for experimentation and an insight into the response of these modern devices to radiation at lower temperatures.

These results show that FinFET devices experience several of the same performance enhancements at cryogenic temperatures as is seen in planar FET devices. The already superior subthreshold characteristics of FinFETs compared to conventional planar devices at room temperature are enhanced at lower temperatures. The response of these devices to irradiation by 1.8 MeV protons shows that the effects of radiation in FinFETs are significantly temperature dependent. With irradiation at cryogenic temperatures as opposed to room temperature, these devices were not as prone to off-state leakage current increases, due to the decrease in band-to-band tunneling and STI interface leakage paths at lower temperatures. However, they did experience increased transconductance degradation and relatively greater subthreshold slope degradation, likely due to the increased oxide hole trapping, decreased interface state generation, and increased relative effect of LNUs at lower temperatures. Future work to explore these phenomena might include irradiation at room temperature and subsequent cooling, or irradiation at cryogenic temperature and subsequent heating in order to better understand the mechanisms of degradation in these devices at low temperatures.

At the doses tested in these experiments, the degraded transconductance and subthreshold swing of the devices at cryogenic temperatures were still far superior to those of the devices irradiated at room temperature. However, at extremely high doses, it is possible that the subthreshold and transconductance characteristics of the FinFETs might degrade so much that performance would be worse for devices irradiated at cryogenic temperatures compared to devices irradiated at room temperature. Given how much the transconductance, subthreshold swing and subthreshold leakage operation is improved at cryogenic temperatures, it seems extremely unlikely that FinFETs in electronic systems operating in extreme environments would receive enough dose to degrade beyond room temperature values before other critical system failure. The responses of the FinFET devices tested in this work point to FinFETs being optimal candidates for cryogenic radiation missions.

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