SIMULATION-BASED STUDY OF SINGLE EVENT TRANSIENTS IN A SIGE BICMOS LOW POWER OPERATIONAL AMPLIFIER

By

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Thesis

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LIST OF ABBREVIATIONS

SEE – Single Event Effect

LET – Linear Energy Transfer

SET – Single Event Transient

SEU – Single Event Upset

BiCMOS – Bipolar Complementary Metal Oxide Semiconductor

op amp – operational amplifier

SiGe – Silicon-Germanium

HBT – Heterojunction Bipolar Transistors

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

TID – Total Ionizing Dose

PDK – Product Development Kit

CHAPTER I

INTRODUCTION

Electronics used today in units destined for space, where there are high levels of radiation, are vulnerable to single-event effects (SEEs), and the susceptibility increases as device feature size decreases and operating speeds increase [1]. Single events occur when regions of a microelectronic circuit are hit with high energy particles. When the high energy particle strikes the circuit, it creates electron-hole pairs in the semiconductor material along the path it travels until it loses its energy. The length of the path it travels until it loses its energy is called the particle's range. Linear energy transfer (LET) describes the energy loss in each unit path length, and the value is normalized by the hit material's density [2]. The electron-hole pairs separate and recombine at the pn junctions of the hit device. This induces unwanted currents in the hit device, and may disrupt the function of the device [3].

A single event may cause a single event transient (SET), which is when a single event results in an undesirable analog signal propagated through a circuit. A single event upset (SEU) is the digital version of a SET, and usually results in the incorrect change of a logic value. The first SEU was documented in 1975 by Binder, et al. [4]. Since then, as electronics have gotten smaller and faster, the number of upsets has also increased [3]. As a result, circuits built today must undergo heavy testing and modification to ensure they will work correctly when in harsh radiation environments.

The bipolar complementary metal oxide semiconductor (BiCMOS) low power operational amplifier (op amp) studied in this thesis has been implemented in the silicon-germanium (SiGe) 0.5-µm process. The op amp was designed by Yarlagadda et al. [5] and adapted from Babanezhad et al. [6]. Miniaturizing systems and design for wide temperature ranges is important for electronics operating in space radiation environments. The SiGe heterojunction bipolar transistors (HBTs) used in this circuit improve the circuit's ability to withstand radiation and cryogenic temperatures more effectively than if its silicon counterpart, bipolar junction transistors, were used [7, 8]. Designing low power circuits is becoming more important since electronics are becoming more mobile and conserving power is important. It is particularly vital in space applications to increase and conserve battery life since recharging is intricate [9].

Many techniques to reduce or eliminate SEEs have been discovered such as adding capacitances, resistances, and guard rings [10, 11]. This thesis will utilize simulations to determine regions of sensitivity, predict SETs for certain configurations, and evaluate the SET's dependence on the single event pulse model parameters. Using these results, this thesis will consider the effectiveness of adding guard rings to the HBTs as a possible approach to reduce SEEs. A guard ring is a region of higher doped material surrounding the metal-oxide-semiconductor field-effect transistor (MOSFET) and is biased by either the power supply or ground depending on the type of transistor. Guard rings do increase the device size, but advantages are gained since the bias helps maintain the potentials, which assists in prevent latch-up. Latch-up occurs when a chip continues to draw current from its power supplies, but the circuit fails to operate

correctly [12]. The conclusions drawn from this thesis will not apply to proton strikes since there are two components of a protons strike instead of one. The first component is the result of the direct proton strike, and the second component is the result of secondary electrons that are collected by devices after their creation by the proton strike [13].

The second chapter of the thesis discusses the stages of the op amp circuit. The third chapter discusses the current pulses that will be used to simulate ion strikes in the circuit. The fourth chapter will explain the simulation process and show the results of those simulations. The fifth chapter will show the results of a study of the sensitivity of the op amp circuit to changes in charge collected from an ion strike and ion strike magnitude, with and without the presence of guard rings. The sixth chapter will give conclusions drawn from the simulations.

CHAPTER 2

OPERATIONAL AMPLIFIER CIRCUIT

The low power BiCMOS op amp circuit is composed of HBTs and MOSFETs. The HBTs and MOSFETs are utilized to employ their strengths of total ionizing dose (TID) immunity, high gain, and performance capability at extremely low temperatures [6]. TID is the amount of trapped charge accumulated over time. While these strengths will not be discussed in this study they are important in space bound circuits. In this chapter the layout and function of the circuit is described. This chapter is a summary of Chapter 3 of Yarlagadda's thesis [5].

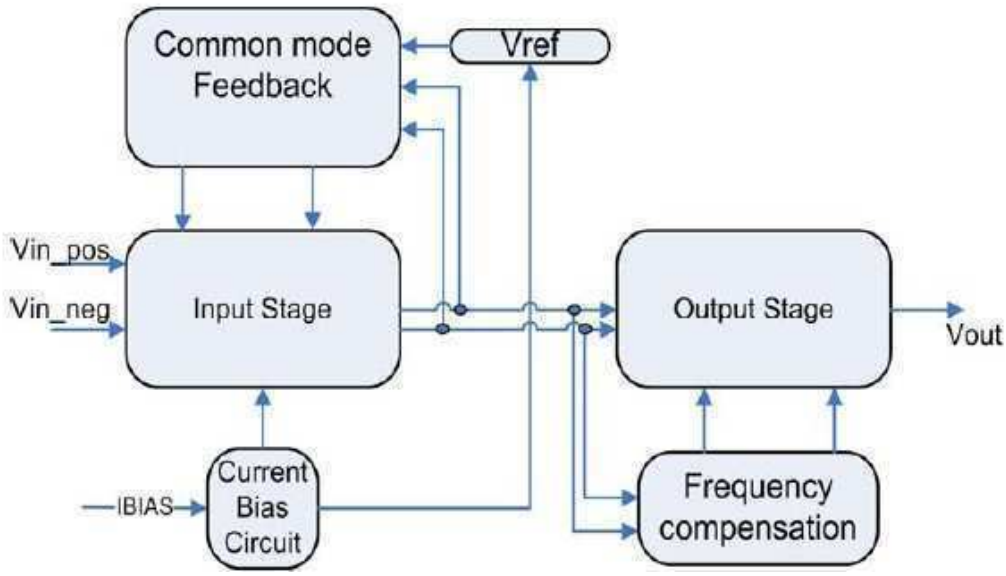

Figure 1 Op amp block diagram. After [5].

Stages of the Operational Amplifier

The SiGe BiCMOS low power op amp has two effective gain stages, the input and output stages. The common-mode feedback circuit, frequency compensation, and biasing circuitry are the other stages of the op amp. Figure 1 shows a block diagram of the op amp, and an explanation of the different stages is in the following sections.

Input Stage

The input stage, shown in Figure 2, is the first gain stage, a differential gain stage, which provides the majority of the open-loop gain. Since the gain of the second stage is dependent on its output load, it is important that the gain of this stage be large and controlled. The HBTs operate in the forward-active region, and the PMOS devices operate in the saturation region in this stage [5].

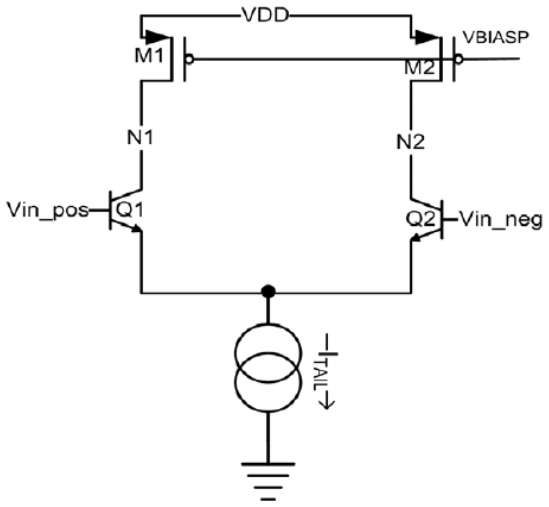

Figure 2 Input stage of op amp. After [5].

Common-mode Feedback Circuit

The common-mode feedback circuit, shown in Figure 3, guarantees that the collectors of the input HBTs (N1 and N2) will remain at a precise quiescent voltage instead of floating [5].

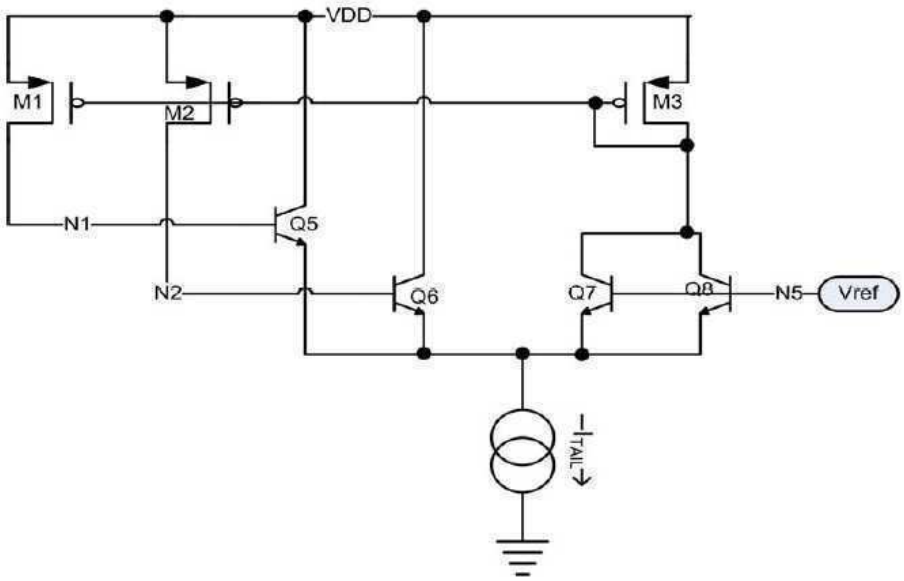

Figure 3 Common mode feedback circuit of op amp. After [5].

Output Stage

The output stage is the second gain stage and shown in Figure 4. The output stage runs on low power during standby and drives a capacitive load with high gain. The current in the output stage is independent of the supply voltage, and instead depends solely on the input bias current. The bias current sets the current in Q10 proportionally to the sizes of the devices, which in turn sets the current in M4 and M5. Since the sources of M4, M8, and M10 are all at the same potential, and the drains of these transistors are also at the same potential, the current flowing through these devices is proportional to their respective sizes [5].

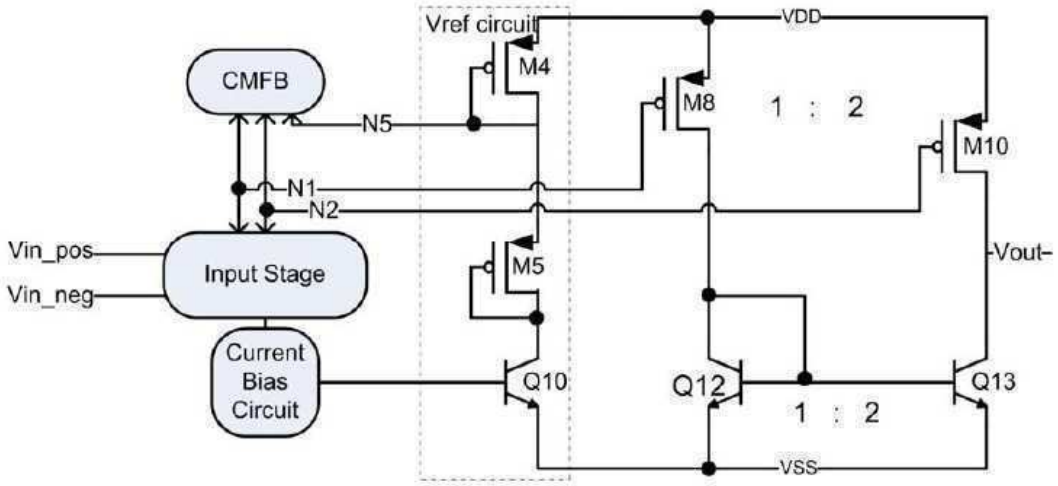

Figure 4 Simplified output stage of op amp. After [5].

Frequency Compensation

The frequency compensation, shown in Figure 5, is required for the op amp to have unity-gain stability, which is stability when the output is connected directly to the input. The stability is achieved by adding a Miller compensation capacitor to the circuit C_{C1} and C_{C2}. M9 and M11 are added as effective resistors to negate the frequency response effects of adding the compensation capacitors [5]. The entire op amp circuit is shown on the next page in Figure 6.

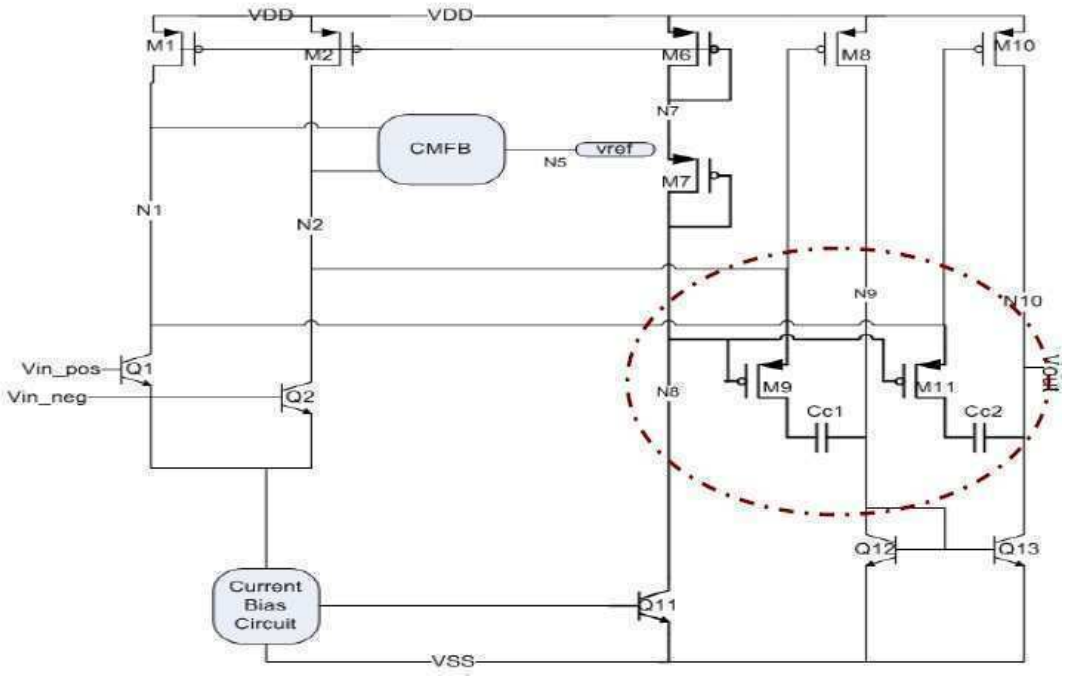

Figure 5 Frequency compensation circuit of the op amp. After [5].

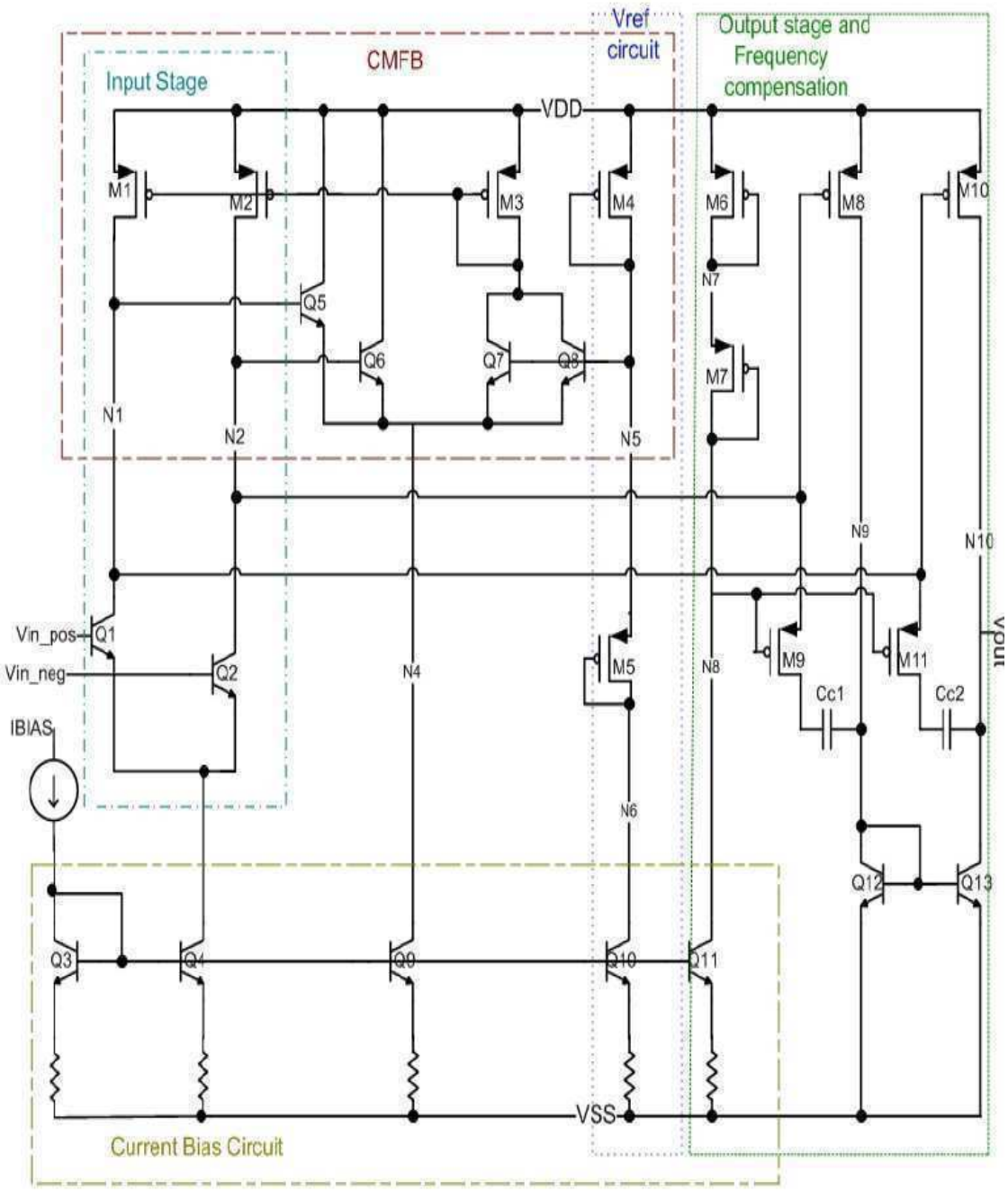

Figure 6 Complete schematic of op amp. After [5].

CHAPTER 3

EXPERIMENTAL CURRENT PULSES

In this thesis, simulations are done using Cadence's Spectre simulation tool. Simulating an ion strike in Spectre is achieved by assigning a current pulse to the node that is to be struck by the ion [14]. Published results from simulated and measured TCAD current pulses and collected charges across multiple technology generations of SiGe HBT devices (0.5 µm and 0.18 µm) [11, 15-17] were used as a starting point to determine the reasonable bounds for current pulses in this study [11, 15-17]. The profiles for the current pulses were similar in magnitude and pulse width, so application of similar current pulse parameters can be made to this thesis.

Ion strike Inside the Trench

The current pulse for an ion strike inside the trench is modeled with a double exponential with a peak of 3 mA, a rising time constant of 2.5 ps, falling time constant of 250 ps, which translates to approximately a rise time of 10 ps and fall time of 1 ns. The current pulse is shown in Figure 7. The collected charge was calculated as 778 fC using the calculator that is built into the data capture program within Spectre.

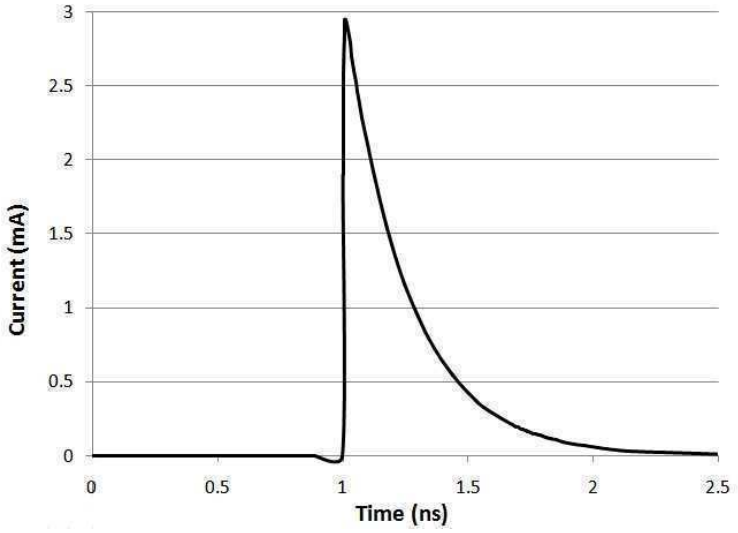

Figure 7 Current pulse for simulated ion strike inside trench.

Ion Strike Outside the Trench without a Guard Ring

The current pulse for an ion strike outside the trench with no guard ring present is modeled with a double exponential with a peak of 4.5 μA, a rising time constant of 1.9 ns, and a falling time constant of 9 ns, which translates to approximately a rise time of 6 ns and fall time of 42 ns. The current pulse is shown in Figure 8. An ion strike from the literature, simulated with nanoTCAD, deposited a charge of 0.7 pC, but only 0.07 pC of charge was collected on the transistor [11]. The double exponential current pulse is used to model the deposited charge of the ion strike. To simulate hits outside the trench with higher charge values, the magnitude of the pulse was increased. The efficiency of the ion strike in from the nanoTCAD results was only about one tenth of the charge the incident ion strike deposited, since only one tenth of the energy in the incident ion strike was collected on the transistor [11]. Accordingly, all current pulses simulated outside the trench in this study will be assumed to come from ion strikes with

integrated charge values ten times the charge the pulse deposited on the op amp circuit.

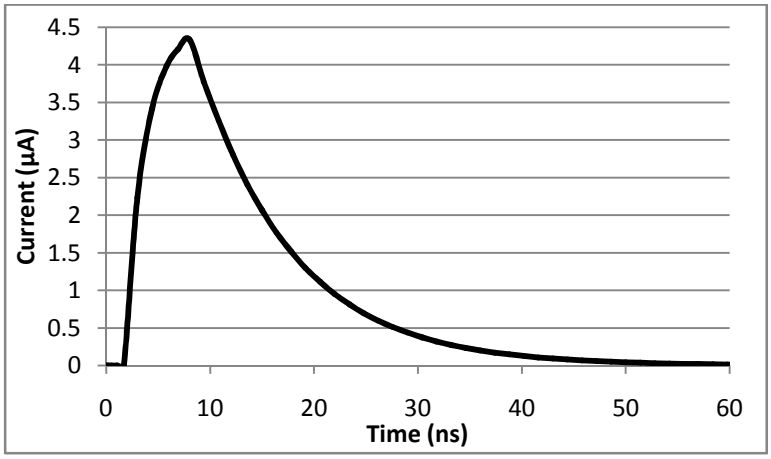

Figure 8 Current pulse for simulated ion strikes outside of trench.

The collected charge of the current pulse used for simulations was calculated as 61.4 fC using the calculator that is built into the data capture program within Spectre by performing an integrate function on the current pulse.

Ion Strike Outside the Trench with a Guard Ring

The boundary conditions for parameters of the current pulse used to model an ion strike outside the trench with a guard ring present were derived from the nanoTCAD simulations [11]. Results from the nanoTCAD simulations showed that adding a guard ring to the HBT decreased the collected charge to 16 fC from 70 fC collected by the HBT without the guard ring [11]. This was a decrease of 77 % from the nominal HBT. For strikes outside the trench at a given LET, simulations of an ion strike on an HBT with guard rings were reproduced with a current pulse with an integrated charge that was 22

% of the integrated charge of the pulse representing a strike to an HBT with no guard ring. As an example, for an ion strike with a charge of 2 pC on an HBT with no guard ring, the collected charge was 202 fC. For a ion strike with a charge of 2 pC on an HBT with a guard ring, the HBT would only collect 44 fC (22 % of 202 fC). Thus a current pulse with an integrated charge of 44 fC will be used to simulate an ion strike depositing 2 pC to an HBT with a guard ring. Simulations to be discussed in Chapter 4 will illustrate that the shape of the pulse delivering the charge is not important since the amount of charge collected dictates the response of the circuit. Therefore, emphasis is placed on simulating the correct total charge, and not much importance is placed on the shape of the pulse.

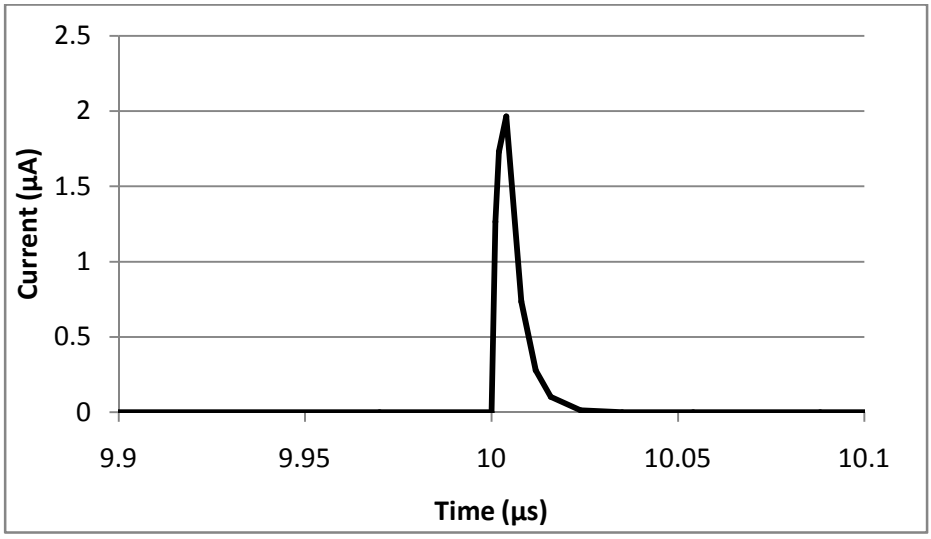

Figure 9 Current pulse for an ion strike simulated outside of the trench with guard rings.

The collected charges simulated for the HBTs without a guard ring were used to calculate the values of collected charge that would be used to simulate the HBT with a guard ring. An ion strike outside the trench for an HBT with a guard ring is simulated

with the current pulse in Figure 9, and the collected charge corresponds to 22 % of the collected charge of the current pulse in Figure 8 for an HBT without a guard ring. The collected charge of the current pulse in Figure 9 is 14 fC. Table 1 shows the magnitude and collected charge of current pulses used to simulate ion strikes both with and without guard rings.

Table 1 Current magnitudes and collected charge for the different current pulses that will be used to simulate ion strikes with and without guard rings

Charge Deposited by strike (pC)	without guard rings		with guard rings	
	Current magnitude (μA)	collected charge (fC)	Current Magnitude (μA)	collected charge (fC)
0.6	4.5	61.37	2	14.1
1.0	7	95.9	3	21.17
1.4	10	135.5	4.3	30.35
2.0	15	201.8	6.5	45.8
2.7	20	268	8.7	61.3
4.0	30	403.6	13	91.4
5.4	40	538.2	17.5	122.9

CHAPTER 4

SIMULATION AND RESULTS

Simulation Process

Simulations of the op amp circuit were done using Cadence's Spectre, a spice circuit simulator, using IBM 5AM (analog metal) product development kit (PDK) models. When simulating a strike on an HBT, the current pulse was applied from the collector to the substrate.

When a particle strikes a transistor, charge is collected at all four terminals of the device. A simulation applying a current pulse from the collector to substrate does not capture the effects of the charge collected on the base and emitter terminals. A spot check was completed to ensure that results using the single current pulse were correct. The results of this spot check followed the trends captured with the single current pulse.

The response of the output voltage to the current pulse was examined. The op amp was simulated in three configurations; voltage follower, inverting amplifier with a gain of 10, and non-inverting amplifier with a gain of 10. To determine the vulnerable transistors, every transistor in the circuit was simulated with the current pulse attached, and with the op amp set up as a voltage follower. Only the vulnerable transistors were simulated in the inverting and non-inverting amplifier setups.

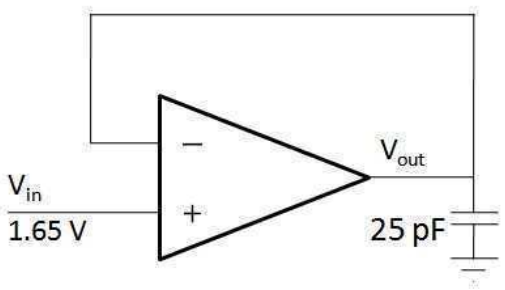

Figure 10 Voltage follower op amp setup.

Voltage Follower Setup

The first set of simulations were done with the op amp set up as a voltage follower with a 25 pF capacitive load and 1.65 V applied to the positive input terminal as shown in Figure 10. To simulate ion strikes to the op amp, a current pulse that emulates the response of an ion strike with an integrated charge of 0.78 pC is used. This current pulse was discussed in Chapter 3.

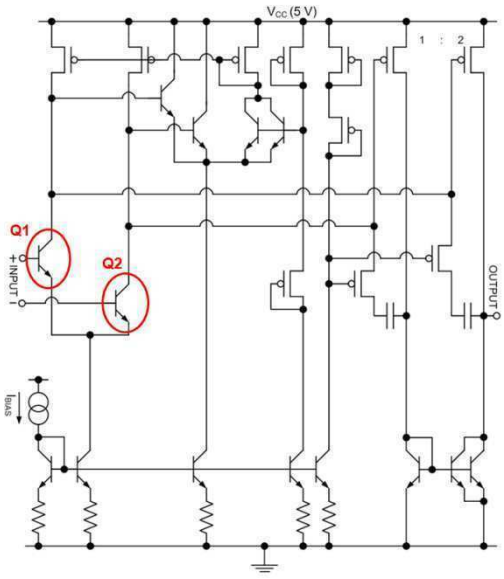

Figure 11 Transistors vulnerable to ion strikes. After [5].

Two HBTs in the input stage exhibited a significant change when the current pulse inside the trench was applied. The location of these two problematic HBTs, Q1 and Q2, are shown in Figure 11. The response of the output voltage to the ion strike on both transistors can be seen in Figure 12. The base terminals of the Q1 and Q2 transistors are the positive and negative input terminals of the op amp respectively.

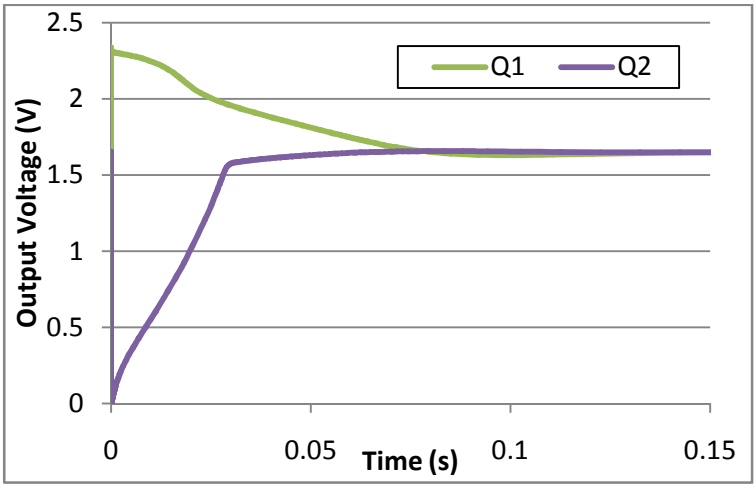

Figure 12 Output voltage response for ion strike inside the trench, integrate charge of 0.78 pC, at Q1 and Q2.

The pulse widths of the SETs shown are very long, approximately 80 ms. In a study done by Boulghassoul et al. [18], it was hypothesized that these millisecond-long pulses were due in part to the feedback loop in the bias/startup circuitry. It was also observed that lower supply voltages increased the pulse length as well [18]. The supply voltage on the op amp simulated in this study has V_{DD} of 3.3 V and V_{SS} of 0 V, so the long SET pulses are not surprising.

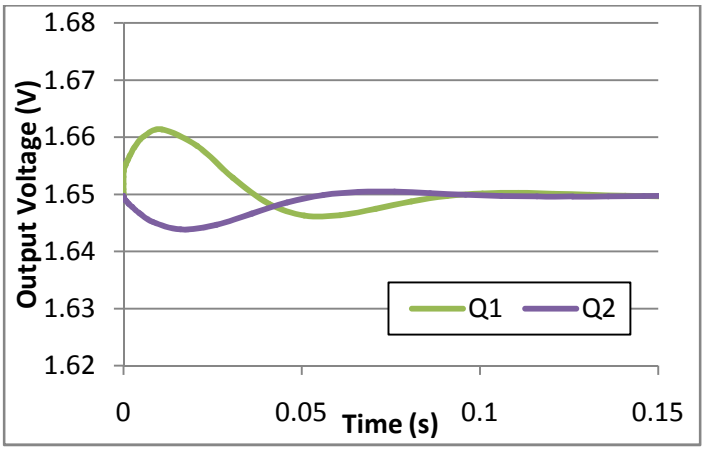

Figure 13 Output voltage response for ion strike outside the trench with integrated charge of 61 fC at Q1 and Q2.

The problematic transistors from the above case were hit again with a current pulse representing an ion strike outside the trench without guard rings that deposits 0.61 pC of charge. Figure 13 shows that the current pulse had an insignificant effect on the transistors, a deviation of less than 1 % from steady state. Therefore, we can assume that ion strikes with low deposited charge, occurring outside the trench, will have negligible effect on the performance of the op amp.

Inverting Amplifier Setup

The second set of simulations were done with the op amp set up as an inverting amplifier with a gain of 10 and a 25 pF capacitive load as shown in Figure 14. In this set of simulations, the two transistors that exhibited problems in the voltage follower setup were the only transistors at which the ion strike was simulated.

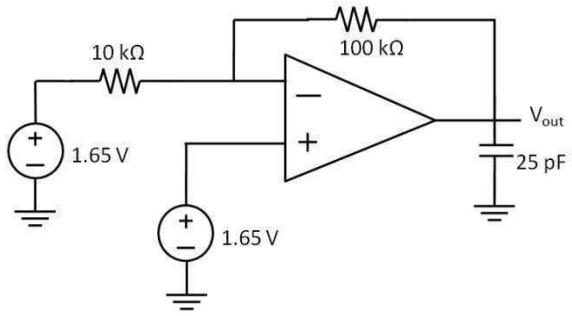

Figure 14 Inverting amplifier op amp setup.

The response of the output voltage to the ion strike on each of the transistors can be seen in Figure 15. The output voltage response was a significant deviation from the steady state output voltage, but the SET pulse width was much shorter than the voltage follower case.

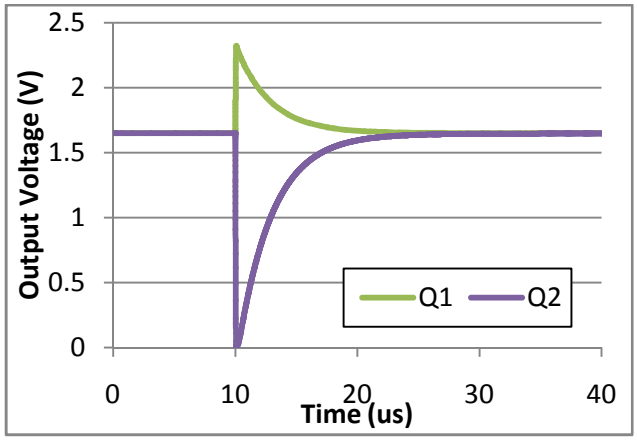

Figure 15 Output voltage response for ion strike inside the trench simulated for Q1 and Q2.

The problematic transistors from the above case were hit again with a current pulse described in Chapter 3 representing an ion strike outside the trench without guard rings. The pulse represented a strike that deposited 0.6 pC of charge, and only a charge of 0.06 pC was collected on the transistor. As can be seen in Figure 16, the output

voltage response barely deviates from the steady state output voltage, an error of less than 0.01 %.

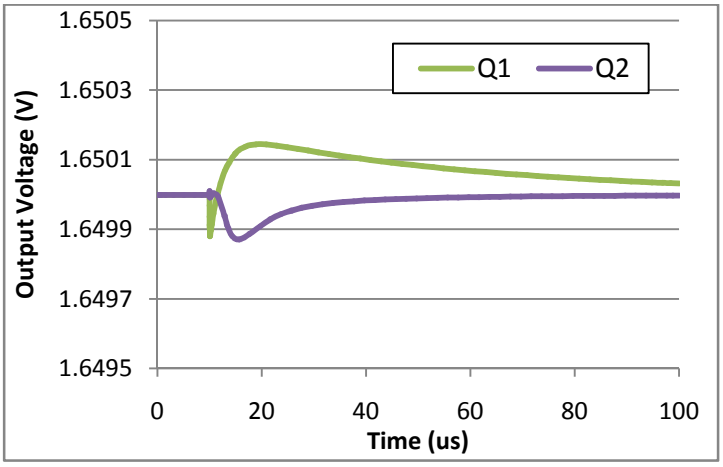

Figure 16 Output voltage response of ion strike outside the trench simulated for Q1 and Q2.

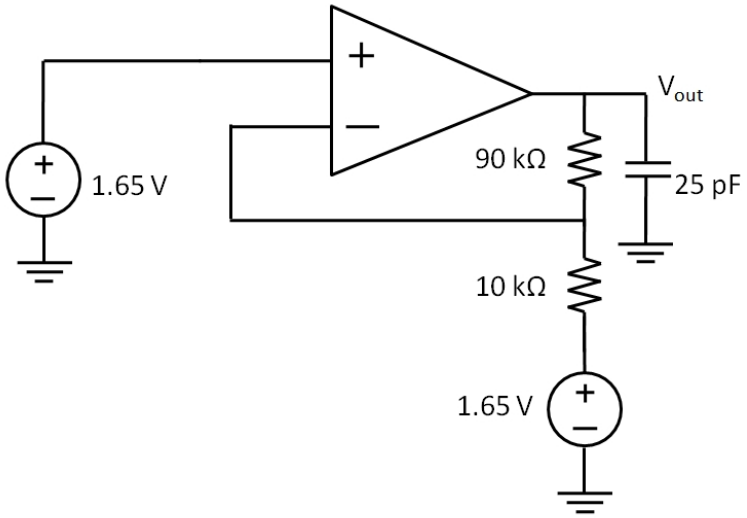

Figure 17 Non-inverting amplifier op amp setup.

Non-Inverting Amplifier Setup

The third set of simulations were done with the op amp set up as a non-inverting amplifier with a gain of 10 and a 25 pF capacitive load as shown in Figure 17. The same

range of current pulses were simulated for this setup, and the output voltage response for pulse hits on this setup were very similar to the response for hits on the inverting amplifier setup, seen in Figure 18. This is to be expected since the only difference between the two setups is the value of the feedback resistor. The reasoning for the setups of the inverting and non-inverting amplifiers being so close was to make the steady state output voltage fall at mid-supply, which is 1.65 V. This feature should ensure that the worst case deviation from the steady state output voltage is observed.

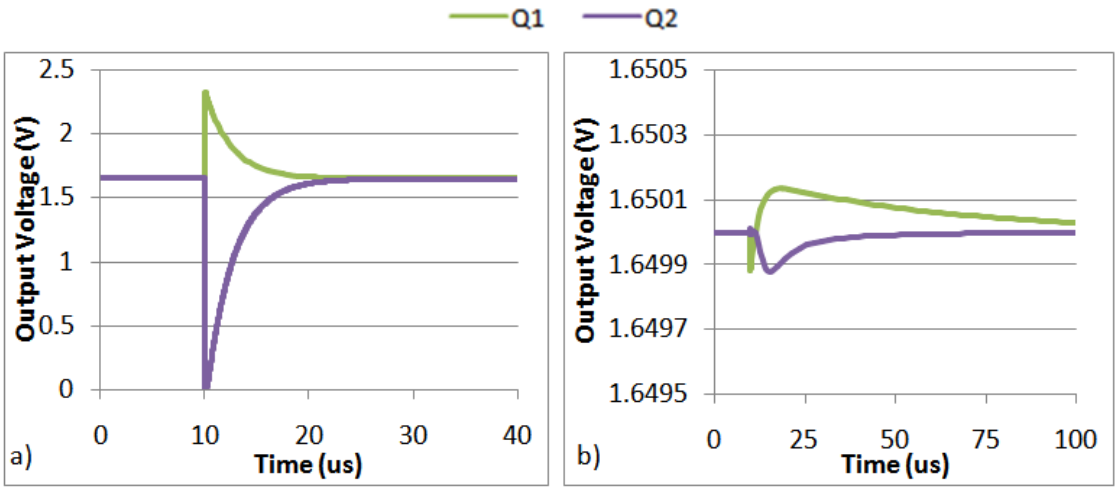

Figure 18 Output voltage response for an ion strike a) inside the trench and b) outside the trench simulated for Q1 and Q2.

Conclusion

The output voltage response to an ion strike for the different setups, voltage follower, inverting amplifier, and non-inverting amplifier, are all similar as can be seen in Figure 19 for HBT Q1. The deviation from steady state output voltage is the same for all three setups. The difference is seen in the width of the SET. The width of the SET for the inverting and non-inverting amplifier setup is essentially the same at about 15 ns,

while strikes on the voltage follower setup result in SETs of about 150 ms long. This difference in pulse width may be accredited to amplification of the error by the feedback loop in the voltage follower setup as previously seen by Wongfoo et al. [19]. The response of the op amp for strikes with low deposited charge outside the trench did not deviate much from steady state. More simulations will be completed in Chapter 5 with strikes representing higher levels of deposited charge.

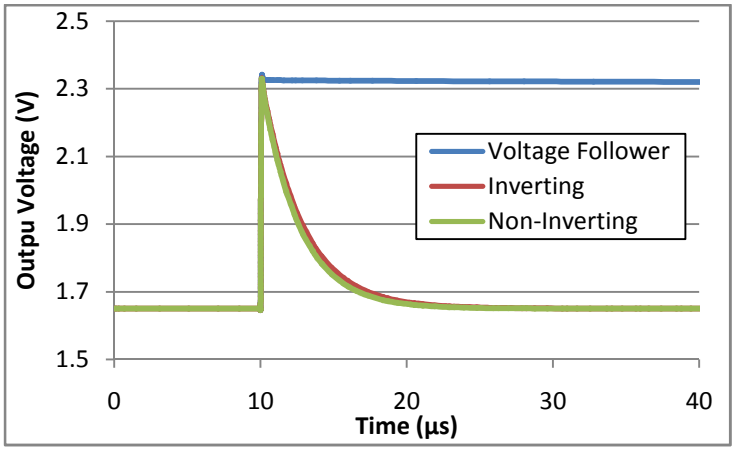

Figure 19 Output voltage response for an ion strike inside the trench on Q1.

CHAPTER 5

SENSITIVITY STUDY

Simulations were done to determine the two vulnerable transistors' sensitivity to changes in collected charge and in the magnitude of a pulse outside the trench with and without a guard ring. Sensitivity to changes in collected charge was determined by changing both the magnitude and duration of the ion strike, but keeping the integrated charge the same. Sensitivity to changes in ion strike magnitude were simulated with increasing values of charge, 0.6 to 5.4 pC for strikes outside the trench, and a constant pulse width. The magnitude of the current pulse ranged from 4.5 to 40 μA for simulations on HBTs without a guard ring. Simulations on HBTs with a guard ring had a magnitude change of 2 to 17.5 μA in the current pulse. The circuit was simulated in the voltage follower setup for this study since the SET exhibited by this setup was the worst case.

Sensitivity to Collected Charge

Sensitivity to charge collected by the circuit was examined by comparing the response of the output voltage to several current pulses with the same collected charge but different strike magnitude and duration. Figure 20 shows that different strikes with the same integrated charge evoke the same response of the output voltage for an integrated charge of 0.5 pC. Comparisons were also done with integrated charge of 0.8,

1.1, and 1.8 pC. All of the transistors simulated have no sensitivity to magnitude and duration. This characteristic will be useful while simulating current pulses outside the trench on HBTs with guard rings since collected charge is the only information available about that type of ion strike.

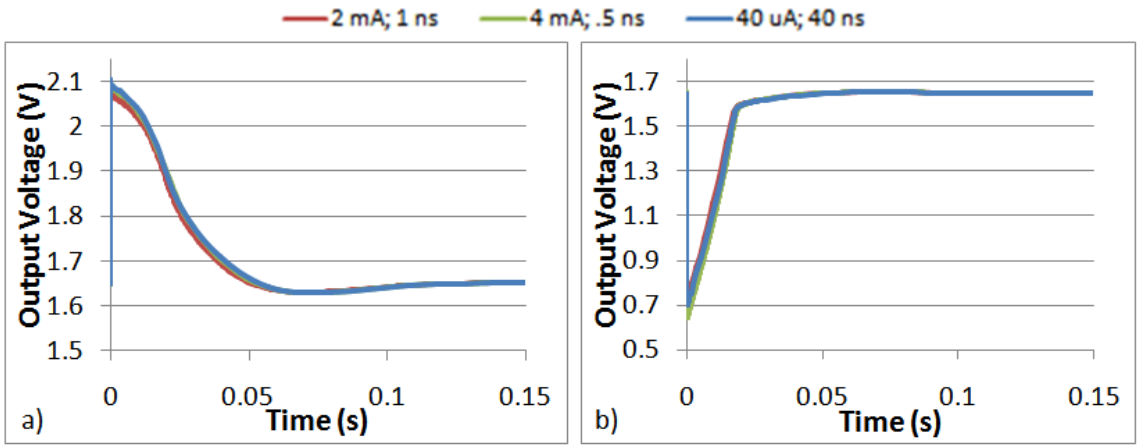

Figure 20 Output voltage response of different ion strikes with the same collected charge of .5 pC for a) Q1 and b) Q2.

Sensitivity to Magnitude of Ion Strike Outside the Trench

Without Guard Rings

Sensitivity to the magnitude of an ion strike occurring outside the trench for a circuit without guard rings was examined starting with the pulse described in Chapter 3. The magnitude of the current pulse was increased incrementally to 40 µA. Figure 21 shows the results of the simulations with the different current pulses. The simulated magnitudes and the corresponding deposited charge values of the ion strike are shown at the top of the figure; all values of charge are in pC. For low values of deposited charge, below 1.4 pC, the simulation results show that no guard rings are necessary, but

for high values of deposited charge, SETs occur that might cause the circuit to output undesirable values.

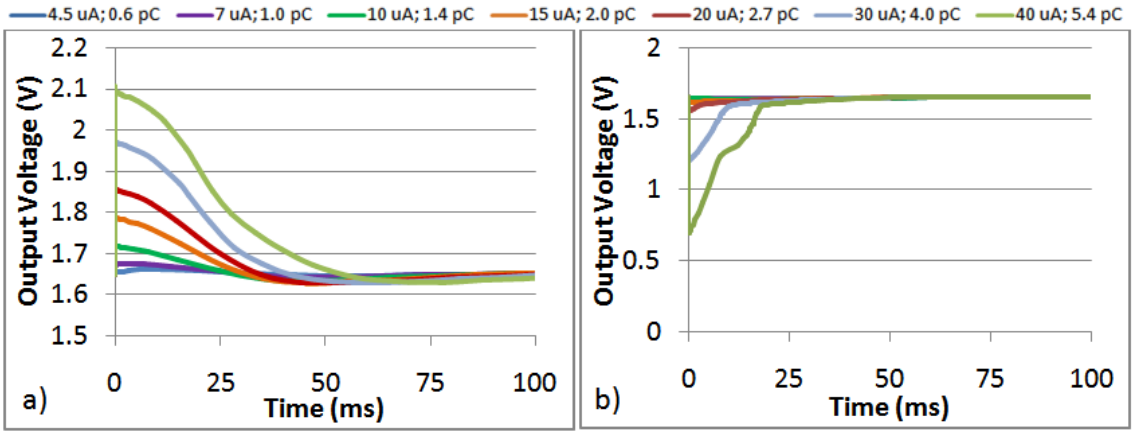

Figure 21 Output voltage response to current pulses outside of the trench with different values of deposited charge for a) Q1 and b) Q2 without guard rings.

With Guard Rings

Sensitivity to the magnitude of an ion strike outside the trench for a circuit with guard rings was examined starting with the pulse described in Chapter 3. The magnitude of the current pulse was increased incrementally to 17.5 µA, and the results can be seen in Figure 22. The simulated magnitudes and the corresponding values of deposited charge of the ion strike are shown at the top of the figure. These simulation results show that with guard rings implemented, a deviation from steady state output voltage barely occurs. The most deviation is with the 5.4 pC strike on Q1, and the deviation is still less than 50 mV, a deviation less than 3 % from steady state.

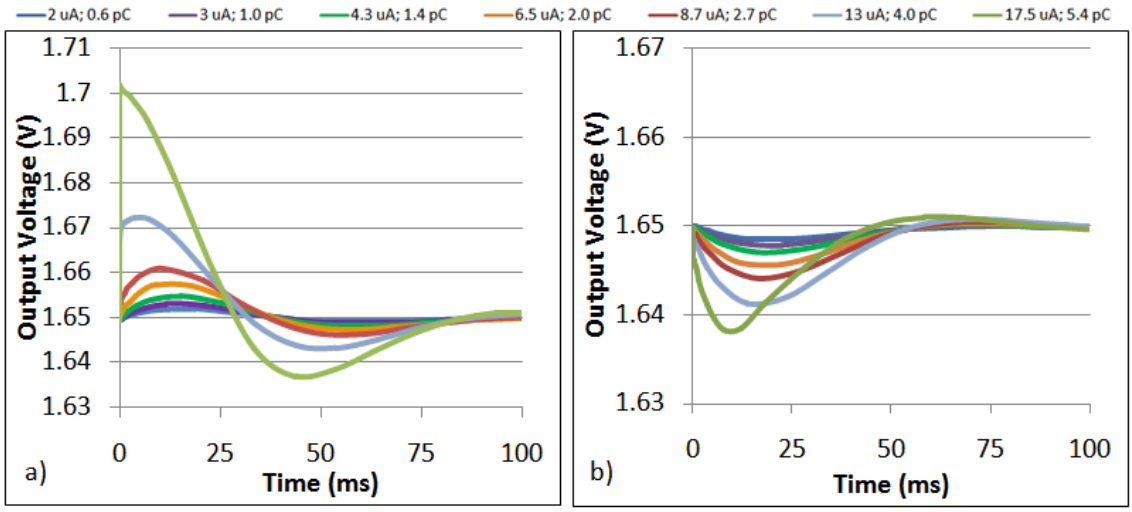

Figure 22 Output voltage response to current pulses outside of the trench with different values of deposited charge for a) Q1 and b) Q2 with guard rings.

Conclusion

The sensitivity study for collected charge exemplifies that, providing the integrated charge in the current pulse is the correct value, then the shape of the current pulse is not incredibly significant to acquire the correct results. A comparison of the presence and absence of guard rings in Q1 and Q2 is shown in Figure 23. Strikes representing lower values of deposited charge result in a small change in the response of the circuit for both cases. However, for high values of deposited charge, adding guard rings to the HBT devices might mitigate the effects of single events as illustrated, assuming viable current pulse models have been used.

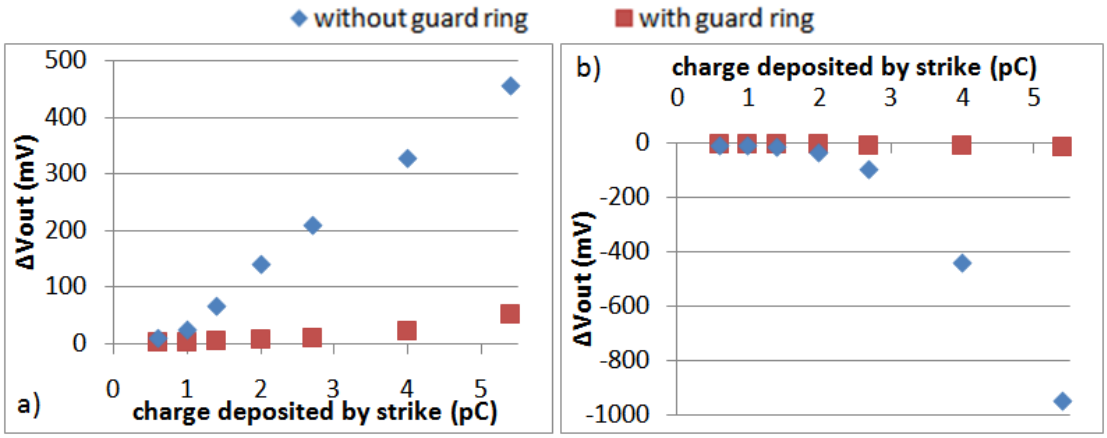

Figure 23 Change in output voltage from steady state as a response to an ion strike representing different values of deposited charge for a) Q1 and b) Q2 with and without guard rings.

CHAPTER 6

CONCLUSION

In this thesis, we have investigated the effects of ion strikes on a low power BiCMOS op amp in the form of current pulses. The starting point and bound for the parameters of the current pulses used in simulations were taken from published literature [11, 15-17]. These current pulses were used to locate areas in the circuit that are vulnerable to ion strikes. Further simulations were completed to understand the impact of implementing a guard ring in the op amp circuitry to improve radiation hardening.

Two HBT transistors were found to be vulnerable to ion strikes inside the trench. Q1 and Q2 were connected to the positive and negative inputs of the op amp respectively. Q1 was on the positive input side of the op amp, and the effect of the current pulses on this HBT caused the output voltage to increase approximately 0.6 V. Q2 was on the negative input of the op amp, and, as expected, the response of the output voltage was to decrease to zero volts, a change of 1.65 V. These transistors are seen to cause considerable errors in the response of the op amp, and will need to utilize further radiation hardening techniques.

Simulations were done with a current pulse that represented the amount of charge that a transistor would see from an ion strike depositing 0.6 pC of charge outside the trench without a guard ring. The response of the output voltage upon seeing the

strike to one of its transistors without a guard ring did not vary much from its steady state voltage. Further study was done with current pulses that represented ion strikes with higher values of deposited charge, up to 5.4 pC for transistors with and without a guard ring. The response of the output voltage to the higher values of deposited charge applied to a transistor without a guard ring deviated about 1 V below the steady state output voltage. For ion strikes with high values of deposited charge outside the trench, the protection of the trench is simply not sufficient and more hardening is needed.

The addition of guard rings to the HBT devices has been presented as a viable option to increase the hardening to radiation for the low power BiCMOS op amp. The guard ring would protect the HBTs from collecting as much charge from ion strikes occurring outside of the guard ring. Our findings show that the addition of guard rings lessens the magnitude of the SETs to a deviation of 3 % from the steady state output voltage for a strike depositing a charge of 5.4 pC on the HBT. For lower values of deposited charge, the effects on the output voltage were even less. Conclusions can be made that the addition of guard rings could be an effective mitigation strategy against ion strikes depositing high values of charge outside of the trench.

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