

**SINGLE EVENT MECHANISMS IN 90 nm TRIPLE-WELL CMOS
DEVICES**

by

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CHAPTER I

INTRODUCTION

1.1 Overview

In complementary metal oxide semiconductor (CMOS) technology, both PMOSFETs and NMOSFETs are used. The PMOSFETs are built on an n-substrate, and the NMOSFETs are built on a p-substrate. There are two basic CMOS technologies – the n-well process and the p-well process. The twin (dual) well process includes both n-wells and p-wells built on a lightly doped substrate that is either p-type or n-type (Fig. 1(a)). There is yet a third process, called the triple well process. The triple-well technology comprises a buried n-well layer that isolates the p-well from the p-substrate (Fig. 1 (b)). In a dual well technology, the p-well is not isolated from the p-type substrate. The p-well – n-well junctions alter the single event performance of an NMOSFET built in a triple-well technology from that in dual well [1-5]. The single event charge collection in triple-well NMOSFETs may be higher than that in dual-well structures in some circumstances [5]. The mechanisms behind the charge collection are analyzed in this thesis using 3-D TCAD simulations. In the simulations, the parameters for well design are varied and their effects on charge collection are explained. It is seen that large and frequently placed p-well contacts reduce charge collection. Increasing the depth of the p-well reduces the effect of the charge deposited by the ion strike on the well potential. Also, deepening the p+ doped region of the p-well contact reduces charge collection.

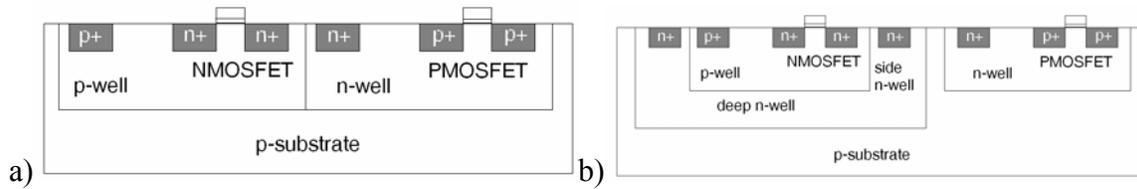


Fig. 1. Well technologies in CMOS. a) Dual well process, b) isolated triple well process – the n-well surrounding the p-well in which the NMOSFET is built is isolated from the n-well in which the PMOSFET is built. In a merged triple well process, the PMOSFET is built in the side n-well which contacts the p-well in which the NMOSFET is built.

1.2 Triple well technology

Substrate noise coupling has been a serious problem in analog RF and mixed signal circuits. The deep n-well in the triple well technology isolates the p-substrate from the p-well, thus reducing substrate noise coupling. Triple wells can be fabricated in a number of ways. In a p-type substrate having a doping density of $1 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{16} \text{ cm}^{-3}$, an n-type implant can be made. Arsenic atoms are typically implanted as opposed to phosphorus, because As diffuses slower than P and has a better lattice match with silicon. The n-type implant must be deep enough to prevent it from influencing the device behavior of the NMOSFETs that are fabricated in the p-well. Surrounding this buried n-well, using a separate mask, n-type implants are made. This surrounds the NMOS device or a group of devices in the same island. The n-type implant must contact the buried n-type implant, and there should be no p-type layer between the n-type implant and the STI. Following these steps, a p-type layer is grown epitaxially. This forms the p-well. It is necessary that the STI within the p-well does not reach the buried triple well. The MOSFETs are built conventionally in the wells thus formed [6]. Fig. 2 shows the triple well structure. If each NMOSFET is built in a separate p-well that is surrounded by the n-

type implants, the threshold voltage of each transistor can be controlled individually by adjusting the bias on the p-well.

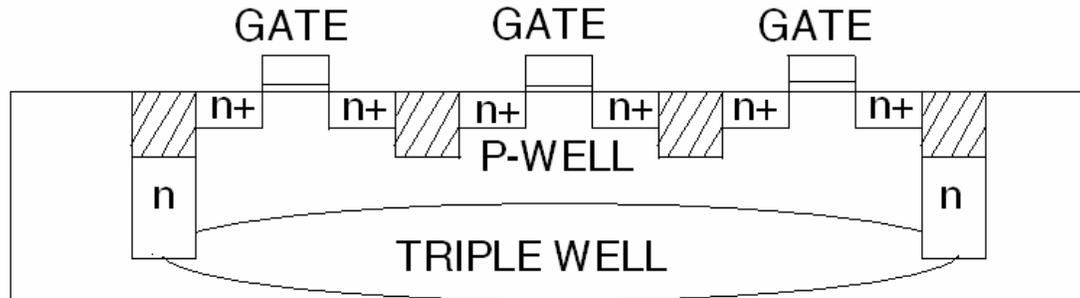


Fig. 2. Triple well structure with the deep n-well under an epitaxially grown p-well.

An alternate method of fabricating triple wells begins by growing a p-layer epitaxially, followed by implanting the n-well [7]. Boron is implanted at a dose between $1 \times 10^{15} \text{ cm}^{-2}$ and $5 \times 10^{15} \text{ cm}^{-2}$ at an energy between 2 keV and 10 keV, into a p-type substrate having a doping density between $1 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{16} \text{ cm}^{-3}$. A Ge implant preceding this imparts a degree of amorphousness to the substrate, allowing higher dopant concentrations. A mono-crystalline p-type layer is grown epitaxially. This layer is lightly doped, having doping of the same order of magnitude as the substrate. An n-type ion implantation is performed next to form the n-well, and a p-type implantation is performed for the p-well. In the p-well, arsenic is implanted to form a buried n-layer. The n-type buried layer could be made discontinuous by leaving a gap in the layer. This allows a contact between the p-well and the p-type buried implant. The p+ contact to the p-well is made exactly above the gap in the n-layer. The transistors and the well contacts are made using the conventional process. Leaving the gap in the deep n-layer allows the

diode leakage current with increasing dose of P implant, followed by a decrease in dislocation density and leakage current. The threading dislocations are responsible for increased leakage current in triple-well devices as compared to dual-well devices, which do not have the additional P implant. At higher doses, the damage production rate increases to the extent of initiating amorphization of silicon. The threshold voltage of a triple-well NMOS device, similarly, increases first with increasing implant dose, and then decreases due to amorphization of silicon. [8]

Triple-well devices have been used in mainstream circuitry for two main reasons. Having individual NMOS transistors built in separate p-wells in the triple-well scheme allows the variable control of substrate bias. A 0.3 μm CMOS triple-well technology was employed to obtain a dynamically varying threshold voltage scheme [9]. Low supply voltage V_{DD} and threshold voltage V_{th} enables high-speed and low-power operations, but increases the standby power dissipation. Dynamically controlling the threshold voltage helps reduce power dissipation, while maintaining high speed operations. Triple well technology enables application of substrate voltage separately to each transistor and allows the threshold voltage of the transistors to be altered dynamically.

Secondly, the capacitance of the additional n-well – p-well junctions have been put to use in low-noise amplifiers [10]. The gain of the amplifier is limited by the drain-bulk capacitance at high frequencies. In a triple-well system, the capacitance of the isolated p-well and the deep n-well junction is in series with the n-well substrate capacitance, thus lowering the effective drain-bulk capacitance.

The additional n-well – p-well junction in the triple well can alter the single event performance of an NMOS device significantly. A 600 \times reduction in alpha-particle-

induced soft error rate (SER) was reported in [1] for a 0.5 μm BiCMOS technology. A 4Mb SRAM was fabricated in a triple well, and also in a p-well/p-substrate with a p+ buried layer. While p-well/n-substrate CMOS structures were reported to produce lower SER compared to p-well/p-substrate CMOS devices, the use of triple wells or p+ buried layers reduced SER dramatically. The soft error rates were measured for alpha-particle strikes. It was postulated that the reverse-biased n-p junctions of the triple well resulted in lower error rates in these devices. An $8\times$ reduction was noted when a p+ buried layer was used. However, as device dimensions scale, the reverse-biased n-p junction might not help reduce SER because of additional effects caused by potential modulations within the wells, as is observed later in this thesis.

In a different technology, a shallow triple well and four-transistor SRAM cell with stacked capacitor were used to improve the soft error rate by 3.5 orders of magnitude compared with the conventional SRAM cell [7]. In this 0.25 μm process, the authors demonstrate an increase of storage node capacitance from 8 to 25 fC by using a stacked-type capacitance with two-layer polysilicon. The $64\text{K} \times 36$ bit SRAM, with a speed of 500 MHz, was tested with alpha particles and neutrons. The increased storage capacitance prevents the particle-generated charge from overwhelming the stored data, exponentially improving the soft error immunity. It is claimed in this paper that a shallow triple-well structure reduces the possibility for charge to be generated because the distance of the p-type well that the ion strike passes through is short [7]. The effect of the deep n-well was used along with the effect of increased storage node capacitance to obtain low soft error rate (SER).

While these papers reflect a positive effect of triple wells, with newer technologies, triple wells have been reported to increase soft error rates. In a 0.15 μm technology, it was shown that the use of triple wells increased FIT (Failure In Time) rates [8]. A large number of p-well taps was recommended to reduce upsets related to charge collection by NMOSFETs. It was mentioned that there was a trade-off between NMOS and PMOS performance in a merged triple-well structure. While the electrons accumulate in the n-well, which contains the PMOSFET, the holes also are confined in the same n-well, because the sparse p-taps in the p-well resist the movement of holes into the p-well. However, it is implicit that if electrons accumulate in the n-well, the potential of the n-well is lowered. The presence of holes in the n-well prevents the reduction of n-well potential. There should be fewer upsets associated with charge collection by the PMOSFET compared to the NMOSFET. This concept opposes the argument put forth by the authors of [8].

However, a publication in 2005 claimed that triple wells brought about a 25% decrease in alpha-particle SER in SRAMs built in 90 nm technology, and a 40% decrease for 130 nm [9]. No information was provided about well ties, and the well cross section. Hence, a conclusive analysis can not be made of the data that this paper provided.

Kontos et al. showed that triple-well structures are more immune to latchup than dual-well structures when electrons are injected by the n⁺ diffusion in the p-well [10]. To trigger a latchup condition, the parasitic pnp bipolar transistor, constituted by the PMOSFET's source, the n-well and the p-well, needs to be triggered by the base current of the n-p-n bipolar structure. Due to the buried n-well, the base current of the parasitic npn transistor in the triple well is not efficient enough to trigger the parasitic pnp on.

However, in case of hole injection by the source of the PMOSFET, triple-well structures are more vulnerable to latchup than dual-well structures. The buried n-well makes it easier for the electrons injected by the emitter (source) to reach the collector (n-well).

At the same conference as above, Puchner et al. suggested that some triple-well structures may be immune to single-event latchup [11]. No single event latchup was observed experimentally for neutron irradiation at 20 MeV, 50 MeV, 100 MeV and 180 MeV. However, elevated temperature testing was not done in this case.

In a recent publication on triple wells, an increase in SER was shown with alpha and neutron testing on 65 nm SRAMs [12]. It was claimed that with an increase in p-well ties, the bipolar charge collection for triple-well devices could be reduced.

As device dimensions scale, the fact that triple well technology helps reduce charge collection at the drain of the NMOSFET by collecting charge in the n-well [1-2] does not explain the whole phenomenon of charge collection. Due to the potential redistributions at the well contacts, there are associated effects of charge injection by the source that may affect the single event performance of triple-well NMOSFETs adversely. In this thesis, it is shown that a single NMOSFET built in a triple well collects more charge than an NMOSFET built in a dual well. This agrees with the observation of increased SER by Puchner et al. [3] and Gasiot et al. [12]. Also, it is seen that increasing the p-well contact size reduces charge collection, which agrees with the observations in [3] and [12]. It can be postulated from the mechanisms of charge collection proposed in the thesis that, in a large well, placing p-well contacts frequently helps in the recovery of the system from the upset. This conforms to the observations in [3].

1.4 Overview of Thesis

This thesis concentrates on the physical mechanisms responsible for charge collection in triple-well CMOS devices. Simulations are used to understand the mechanisms. Chapter II describes the simulation setup that is used throughout the thesis.

In Chapter III, the single-event response of a single n⁺ diffusion in a p-well that is part of a triple-well technology is compared with that of an n⁺ diffusion in a p-well/p-substrate that is part of a dual-well technology to illustrate the differences in charge collection. The potentials in various regions of the dual-well and triple-well system are compared to account for the difference in charge collection mechanisms in the two well technologies. The n-well of a triple well collects electrons deposited from the ion strike and reduces the charge collected by the struck n⁺ diffusion in the p-well.

In Chapter IV, the single event upset voltage and current pulses in an NMOS device are studied for different LETs. For ion strikes having low LETs, the upset pulses are double-exponential in shape. The dual-well and triple-well NMOSFET drain collect approximately equal charge when struck with an ion of low LET. However, for high-LET ion strikes, triple-well drain collects more charge than the dual-well drain, when contact sizes for the two cases are the same.

In Chapter V, the mechanisms for charge collection in triple-well devices are examined. Charge carriers deposited by an ion strike cause the potential of the p-well of a dual-well and triple-well system to change. In a triple well, the reverse bias across the p-well – n-well junction causes separation of the carriers, and results in accumulation of holes in the p-well. Thus, there is a stronger de-bias of p-well potential in a triple well when compared with a dual well. The rise in p-well potential is reflected by the potential

difference between the p^+ and p regions at the p -well contact. The p -well potential rises much higher for a triple well than for a dual well. The p -well potential rise reduces the source – p -well potential barrier so that the junction is forward biased in the case of the triple well, while the source – p -well junction remains reverse-biased in the case of the dual well. The elimination of the source – p -well barrier in a triple well results in the injection of electrons into the p -well from the source. These additional electrons cause higher charge collection at the drain for a triple-well NMOSFET when compared with a dual-well NMOSFET. The rate at which the system recovers from the single event is determined by the rate of removal of holes from the p -well. The description of these physical mechanisms is the crux of this thesis.

The effects of varying well design parameters on charge collection and single event voltage and current pulse widths are studied in Chapter VI, with the understanding of the mechanisms that cause these effects. P -well contact size and contact doping depth are the two parameters that influence the single event pulse width the most. P -well contact doping depth plays a role in reducing p -well de-bias by expediting hole removal from the p -well, and can be employed to reduce upset pulse width without imposing any area penalty. Apart from these two techniques, the p -well contact placement, the well junction depth and the n -well contact area are varied to observe the effect of these variations on the single event pulse width.

While the physical mechanisms and the effects of well design parameter variations on single event pulse width are discussed considering a single device in a small p -well, the effects of p -well de-bias when the p -well is large are studied in Chapter VII. When an ion strikes one region of the p -well, the regions distant from the strike are less

affected. The potential de-bias of the p-well is, thus, different in various parts of the well, which causes a potential gradient to occur along the well. An n+ diffusion closer to the strike sees a stronger forward bias across the n+-p junction than for an n+ diffusion away from the strike.

The drain of the NMOSFET is current limited instead of being voltage limited like the source. The factors responsible for the value of the drain voltage during the single event are studied in the Appendix by comparing the potentials in various parts of the well. Both the dual-well and the triple-well cases are considered. Also, the SDE and SDevice scripts used in the simulations are included in the Appendix.

CHAPTER II

SIMULATION SETUP

Simulations are used to compare the single event performance of triple-well NMOSFETs with dual-well NMOSFETs. Simulation results in the form of electrostatic potential and carrier concentration plots are used to explain the physical mechanisms of charge collection in triple-well devices. The device structures simulated using TCAD are described in this chapter. A diode and an NMOSFET are constructed in 3-D in dual and triple wells to simulate single event upsets caused by ion strikes on the n⁺ region of diodes and the drain of the NMOSFETs. The n⁺ diffusion of the diode and the drain of the NMOSFET are loaded with a PMOSFET to simulate an inverter, so that circuit effects on the behavior of the device can be obtained. The aspect ratio of the PMOSFET simulated by means of a compact model is detailed in this chapter. Also, the parameters of the ion strike simulated on the devices are mentioned.

2.1 TCAD structure

The Devise tool from Synopsys is used to create the 3-D device whose single event performance is studied. In this chapter, only the NMOSFET structure is shown. The diode is constructed with a single n⁺ diffusion in the p-well. The n⁺ diffusion is of the same size and doping profile as the drain of the NMOSFET. The simulated device, shown in Figs. 4 and 5, is representative of a 90 nm technology. On a p-substrate having a constant doping of $1 \times 10^{16} \text{ cm}^{-3}$, a buried n-well is made having a Gaussian doping

profile. The p-well built above the n-well has a Gaussian doping profile that peaks at $1 \times 10^{18} \text{ cm}^{-3}$. The doping and dimensions for the dual-well NMOS system were obtained from a public domain report from the technology analysis company Chipworks on the IBM 130 nm technology [13]. The n-well doping was adjusted so that the net doping at the surface where the NMOS device was built remained the same for both the dual- and triple-well schemes. The substrate did not have a deep p+-implant below the buried n-well. A dual-well NMOS device was also built for comparison with the triple-well device in Fig. 3. Fig. 4 shows the 2-D views of the simulated structure, and the doping profile along a vertical cutline through the drain of the device. The substrate is 10 μm deep.

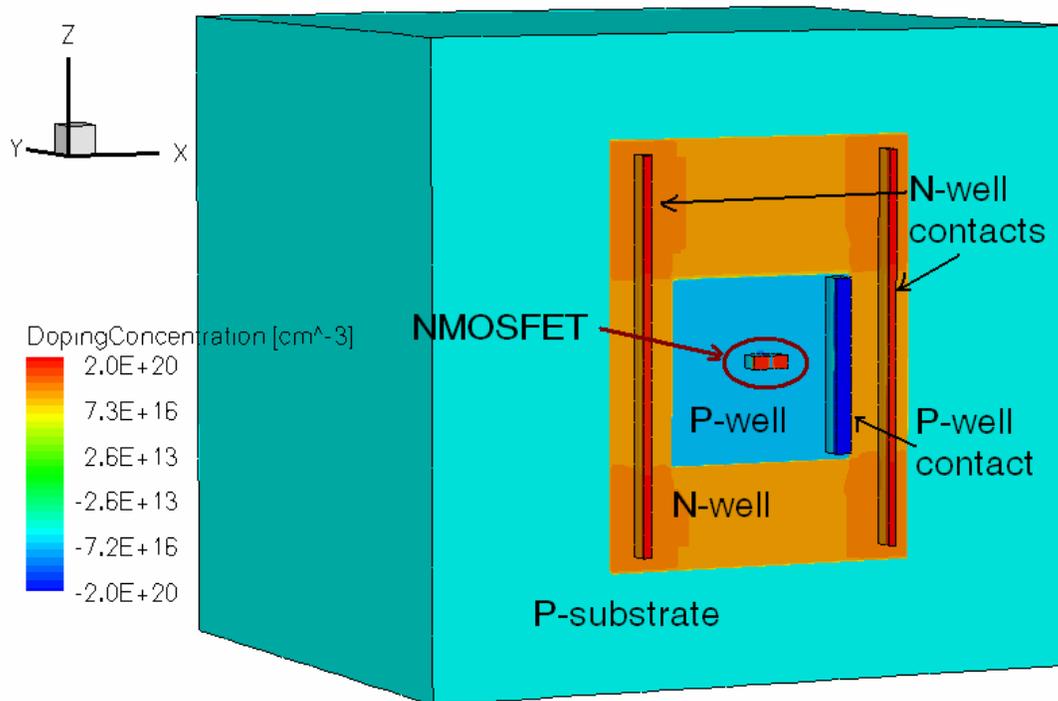


Fig. 4. 3-D view of the triple-well NMOSFET simulated in TCAD.

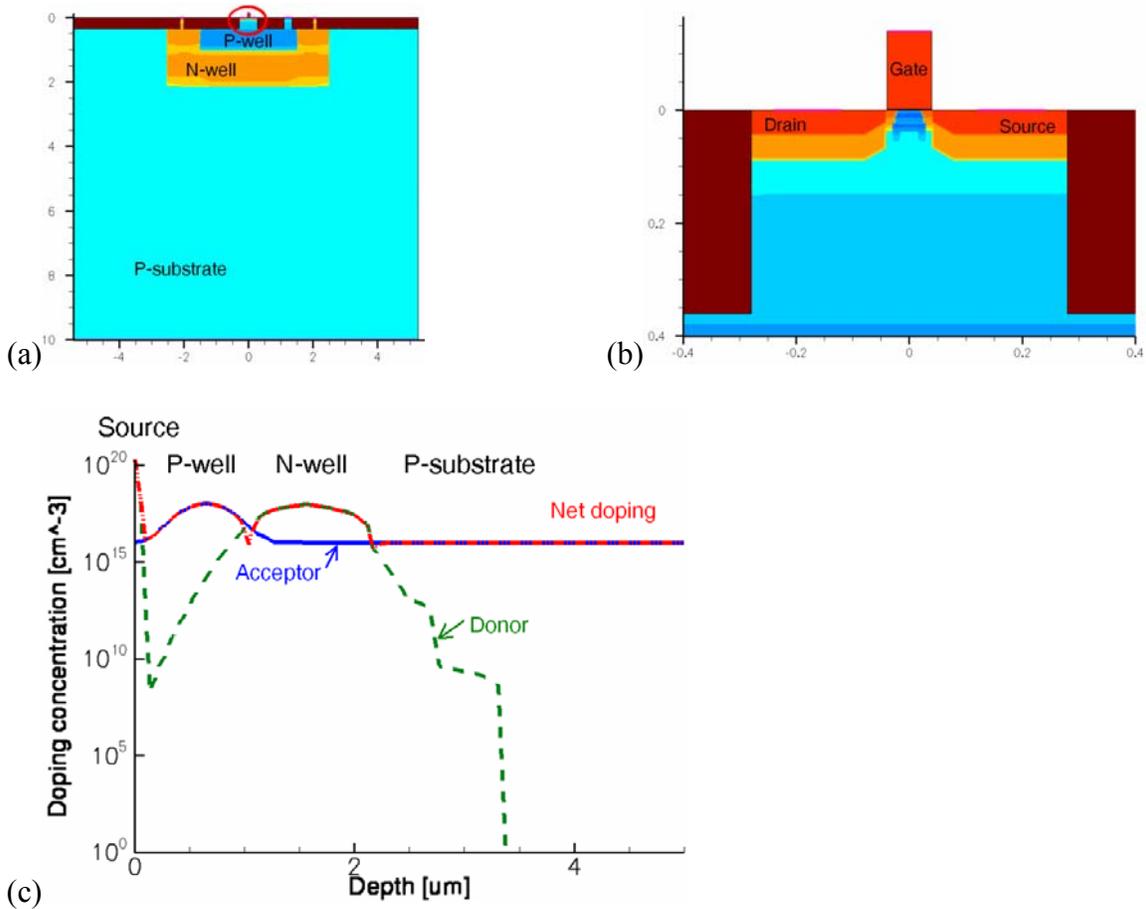


Fig. 5. 2-D slices of the triple-well TCAD device. (a) The complete structure, (b) the NMOSFET. (c) 1-D slice showing the doping concentration along a vertical cutline taken through the source of the NMOSFET.

The NMOS device built with TCAD was calibrated to the electrical parameters of the NMOSFET in the 90 nm IBM Process Design Kit (PDK). The dc characteristics of the MOSFET are shown in Figs. 6-7.

The triple-well NMOS transistor was calibrated by altering the doping of the LDD implants, the threshold adjustment implants, the implants below the threshold adjustment implants and the STI implants from those of the calibrated dual-well NMOS device. The device in the PDK, noticeably, has a larger subthreshold leakage current than the TCAD

device. The threshold voltage and the drive current of the TCAD device show good matching with those of the PDK.

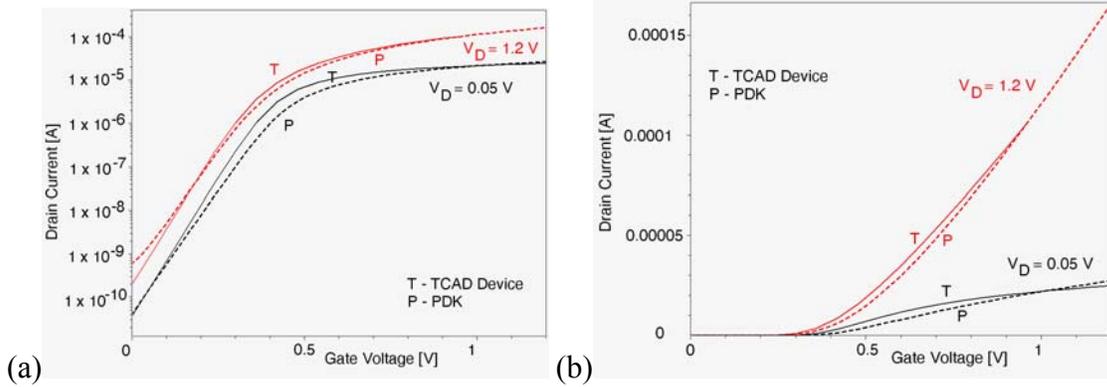


Fig. 6. $I_D - V_G$ curves for triple well NMOSFET. Dashed lines are from PDK. Solid lines are of the calibrated simulation device model.

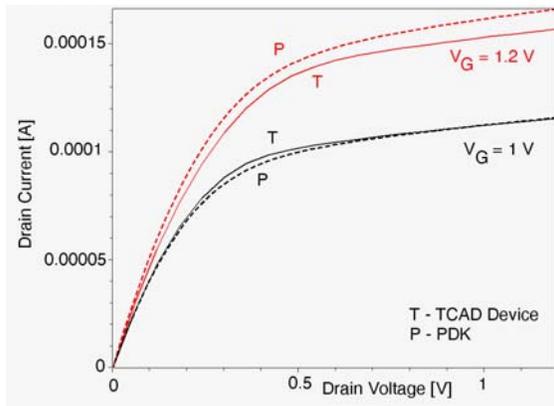


Fig. 7. $I_D - V_D$ curves for triple well NMOSFET. Dashed lines are from IBM PDK. Solid lines are of the calibrated simulation device model.

2.2 Mixed-mode setup

The TCAD NMOS transistor described in the previous section is connected to a PMOS device of $W/L = 480$ nm/ 80 nm. A calibrated BSIM3 compact model of the PMOS transistor is used. The simulations are carried out on a single inverter thus formed. The mixed mode simulations are performed to obtain the effect of an active load on the

struck node, and to observe the circuit effects on the voltage and current at the struck node.

2.3 Ion strike

The drain of the NMOSFET is struck with a single ionizing particle. The ion strike is simulated as a track of radius 50 nm and constant energy deposition using the HeavyIon command in Dessis [14]. The strike goes 7 μm deep into the substrate. Simulations were carried out with strikes having LET values of 0.25, 1, 10 and 40 $\text{MeV}\cdot\text{cm}^2/\text{mg}$. An equivalent setup was created for a dual-well NMOS device (Fig. 8).

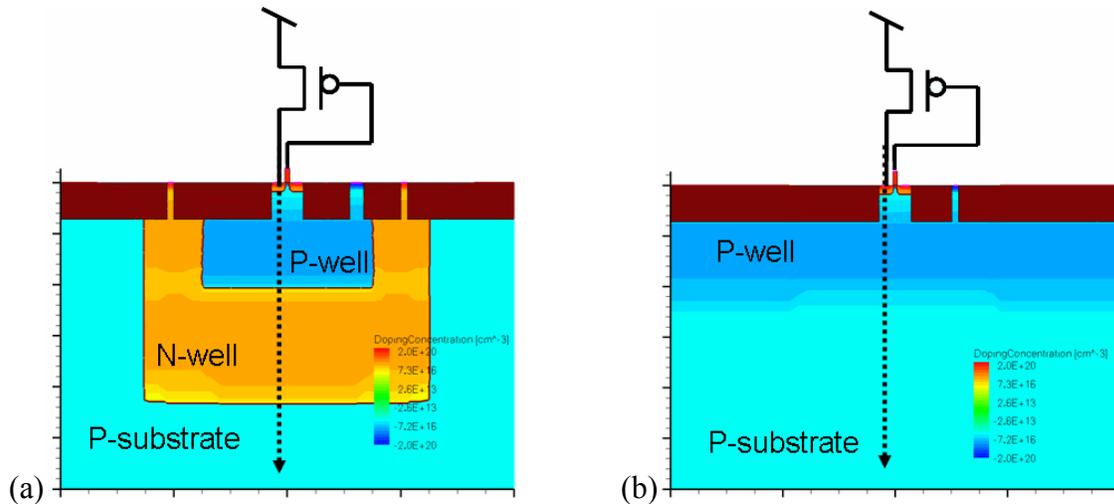


Fig. 8. Simulation setup (a) triple-well NMOS device, (b) dual-well NMOS device. An inverter is formed with the NMOSFET constructed using 3-D TCAD and the compact model of a matched PMOSFET.

2.4 Summary

The device structure and the setup used for the simulation of single event effects in dual-well and triple-well devices are described in this chapter. The following chapters

describe the result of simulating ion strikes on the devices described here. The mechanisms of charge collection in these devices are developed based on the results obtained from the simulations.

CHAPTER III

ION STRIKES ON SINGLE N+ DIFFUSION IN DUAL AND TRIPLE WELLS

Ion strikes are simulated on single n+ diffusion in dual and triple wells. The observations are discussed, and the electrostatic potentials in such structures are understood keeping in mind the conventions of potential reference in TCAD. The basic mechanism of charge collection in single n+ diffusions is described. This prepares the stage for understanding the mechanism of charge collection when another n+ diffusion is added to the well to form an NMOS device in subsequent chapters. The discussion here establishes the role of the deep n-well of triple well structures in determining the single-event response of NMOS devices.

3.1 Potential reference in TCAD

It becomes necessary to understand how the electrostatic potential is referred to in TCAD plots to identify the numerical values of the potentials at various terminals in the devices that have been simulated. The intrinsic Fermi level in silicon is considered to represent the potential in all the discussions here. The reference potential is the Fermi level in a region that is at 0 V. Let us consider the NMOS device that is described in the previous chapter. The source of the NMOS device and the p-well contact are connected to 0 V, so the potentials are referred to the position of the Fermi level in these regions. The potential profiles along cutlines taken at the source and at the p-well contact are plotted in Fig. 9.

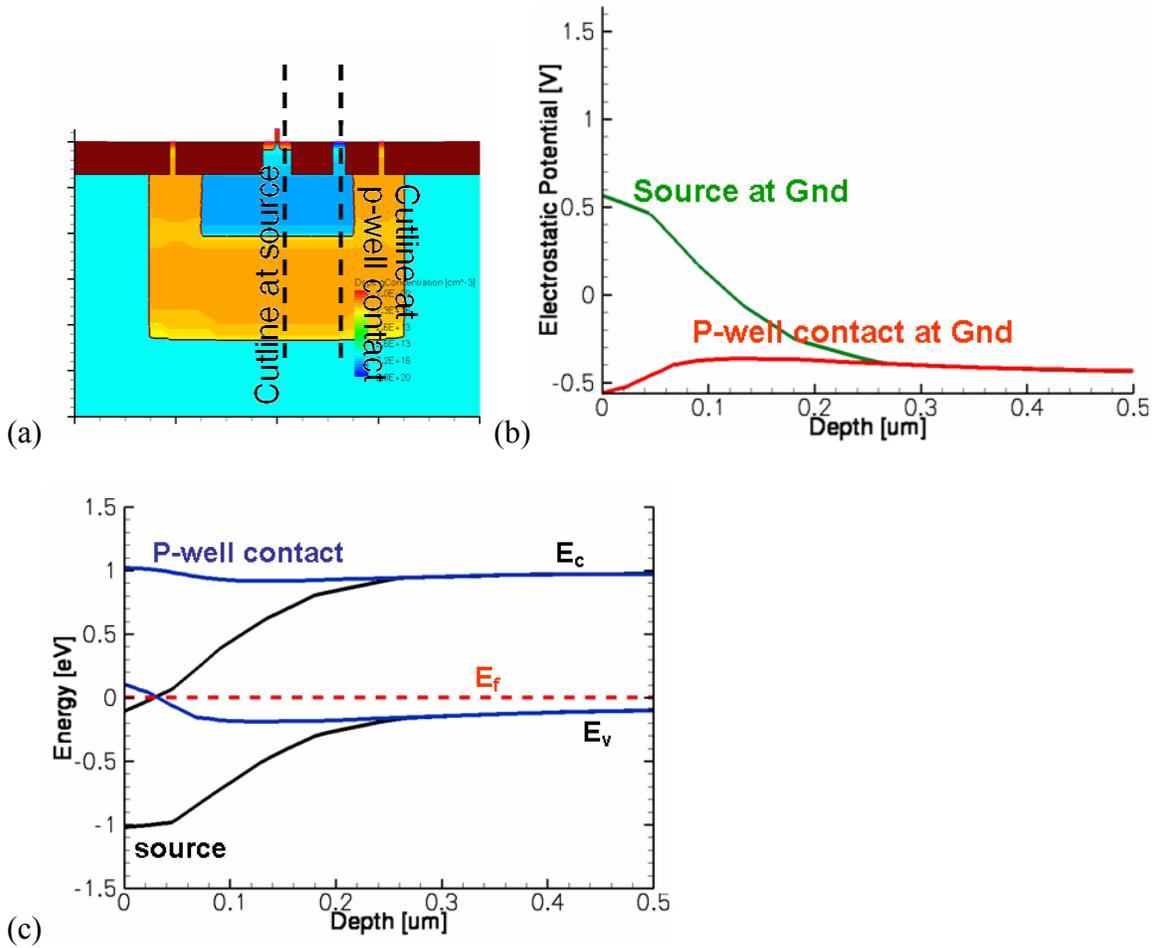


Fig. 9. (a) Simulated structure – black dashed lines show cuts taken along which (b) and (c) are plotted. (b) Potential along cutlines through source and p-well contact as a function of depth of structure. (c) Energy band diagram along those cutlines.

In Fig. 9, though both the terminals are externally at 0 V, the source potential is 0.56 V at the surface, while the p-well contact has a potential of -0.56 V at the surface. This is because when 0 V is supplied to the metal contact, the Fermi level of the metal is at 0 V. The Fermi level of the semiconductor aligns with the metal Fermi level. Thus, in the n-type region of the source, the Fermi level is half the band gap above the intrinsic Fermi level while in the p-type region of the p-well contact, the Fermi level is half the band gap below E_i . The dopings of both the n-type source and the p-well contact have

their Gaussian peak at $2 \times 10^{20} \text{ cm}^{-3}$. Thus, the Fermi level is approximately at the conduction band edge for the n-type region, and at the valence band edge for the p-type region.

3.2 Single event charge collection for single n+ diffusion

To understand the differences in the mechanisms of charge collection in an NMOSFET built in dual and triple wells, the effect of the n-well on charges deposited by the ion strike is studied in this section. Fig. 10 (a) shows a triple-well diode. The TCAD device described in the previous chapter is altered. The p-well has a single n+ diffusion instead of two as in the case of an NMOSFET. Thus dual-well and triple-well diodes are formed. An ion strike with an LET of $40 \text{ MeV-cm}^2/\text{mg}$ strikes the n+ diffusion. The generation of carriers due to an ion striking a part of the semiconductor is dependent on the linear energy transfer (LET), specified in this case as $40 \text{ MeV-cm}^2/\text{mg}$ or $0.4 \text{ pC}/\mu\text{m}$. This is dependent on the length of the ion track, which is specified as $7 \mu\text{m}$. The carrier generation rate has both temporal and spatial variations [14]. The temporal distribution of the generation rate is a Gaussian function with a characteristic value of 2 ps . The time of strike or the peak of this Gaussian function is specified as 1 ns in the simulations. The radial spatial variation of the generation rate is a Gaussian function with a characteristic length of 50 nm , which is specified in the simulations. The peak of this Gaussian is in the center of the n+ diffusion. The voltage and current pulses at the hit node are shown in Fig. 10(b,c). The diode was loaded with a PMOS device, simulated with a compact model.

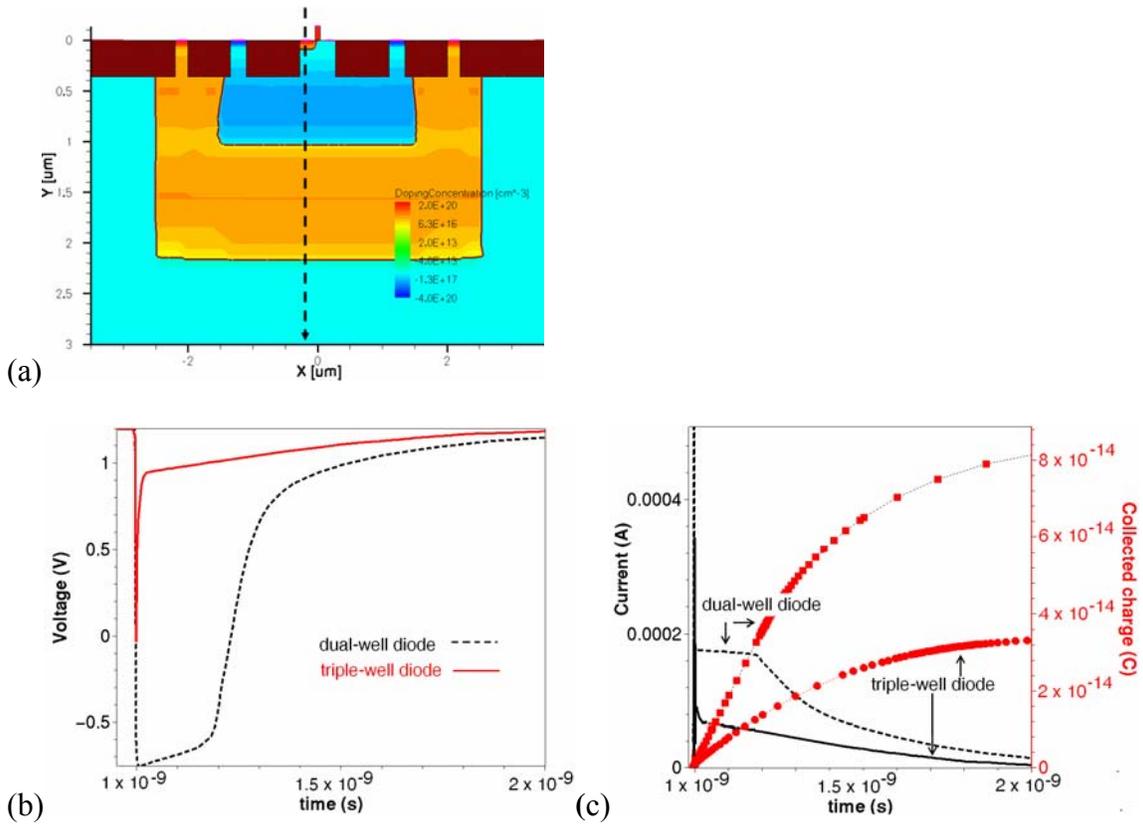


Fig 10. (a) Simulated structure – cross section of n+ diffusion in triple well. (b) Voltage, (c) Current and collected charge vs. time at the n+ diffusion contact for dual and triple-well diodes for an ion strike of LET = 40 MeV-cm²/mg.

3.3 Mechanisms behind charge collection

As seen in Fig. 10 (b-c), the n+ region in the dual-well structure collects more than twice the charge collected by the n+ region in the triple-well diode. The electrons deposited by the ion strike drift into the n-well across the reverse-biased p-well – n-well junction. Thus, the triple well here acts to reduce the collection volume. The various terminal currents in the triple- and dual-well diodes are shown in Fig. 11. The electrons that move into the n-well are collected at the n-well contact, as can be seen from the large

n-well currents. The holes are collected by the substrate and the p-well. Thus, the n+ diffusion in the triple well collects much less charge than in the dual-well case.

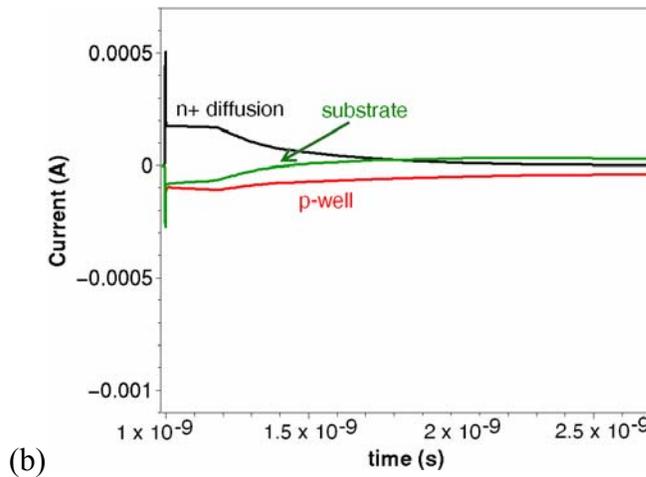
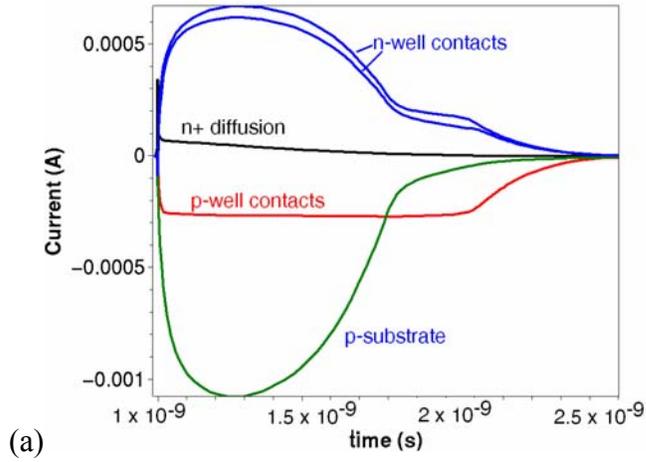


Fig 11. Terminal currents in (a) triple-well, (b) dual-well structure having a single n+ diffusion.

Also, the separation of charge by the electric fields across the reverse-biased junctions allows faster recovery of the system in the triple-well case. In the dual-well case, there are residual charges even after the upset voltage recovers at the n+ diffusion, as can be seen by the presence of a finite substrate current even after the n+ diffusion

current goes to zero. Fig. 12 shows the substrate current components in dual and triple wells. These currents are plotted at the substrate terminal.

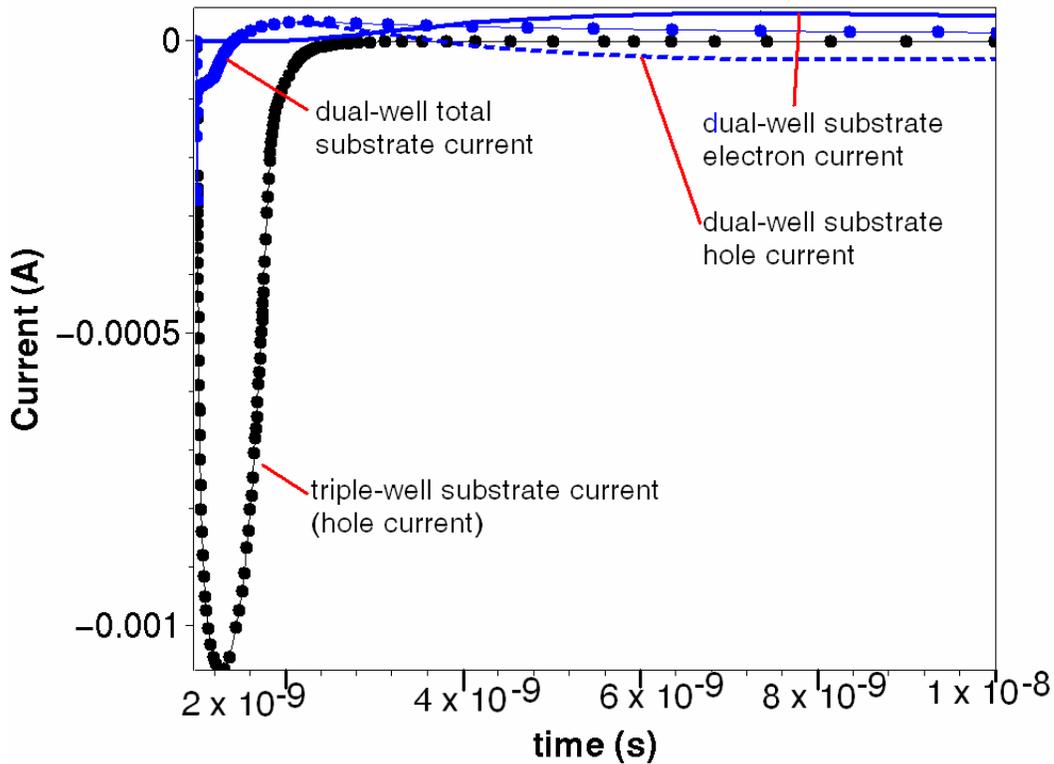


Fig. 12. Substrate current components in dual- and triple-well structures.

3.4 Accounting for potential differences at various terminals

The upset voltage levels at the n^+ diffusion in dual- and triple-well cases are different. The reason for this difference is explained mathematically in this section. The potentials at various terminals of the dual- and triple-well structures are noted from the simulation outputs. Calculations are made to show how the potential at one terminal correlates with the potential at the other.

Prior to the ion strike when the system is in equilibrium, there is a small amount of potential drop at the p^+-p region at the p -well contact. The drop is given by

$$\frac{kT}{q} \ln \frac{N_{p^+}}{N_p} \quad (1)$$

where N_{p^+} is the doping density at the p⁺ region and N_p is the doping density at the p region. Roughly, the potential drop comes to 0.14 V at room temperature.

After an ion strike, there is an increase in free carriers in the p-well. Considering the case of the triple well, electrons generated by the ion strike drift into the n-well across the reverse-biased n-well – p-well junction. The p-well has, in abundance, carriers of one type, i.e., holes. In the dual-well case, there are both electrons and holes in the well. Poisson's equation at the p-well contact region for the dual-well system can be written as:

$$\frac{d^2\phi}{dx^2} = \frac{q(n-p)}{\epsilon} = \frac{dE}{dx}; n \approx p \quad (2)$$

where ϵ is the dielectric constant of the semiconductor.

Poisson's equation at the p-well contact region for the triple-well system can be written as:

$$\frac{d^2\phi}{dx^2} = \frac{q(n-p)}{\epsilon} = \frac{dE}{dx}; n \ll p \quad (3)$$

Thus, the potential drop at the p-well/p⁺ contact for the triple well structure is greater than that in the dual well structure. The contact is externally pinned at 0 V. So, the potential in the p-well goes higher than 0 V, in both cases, while the rise is higher for the triple-well case. Figs. 13-14 illustrate this effect. In these figures, the electrostatic potentials along vertical cutlines taken through the n⁺ diffusion and the p-well contact are shown. The potential difference at the p⁺-p region of the dual-well system is much lower than that in the triple-well system. The n⁺ diffusion is connected to the drain of a PMOSFET. The PMOSFET acts like a constant current source. So, the potential at the n⁺ diffusion's

terminal is allowed to vary while the net current through the drain of the PMOSFET and n+ diffusion terminal remains constant. The charge deposited by the strike neutralizes some of the depletion charge and reduces the potential barrier that existed between the n+ diffusion and the p-well. The rise of the p-well potential now determines the potential at the contact of the n+ diffusion. The quantitative analysis that follows explains the relationship between the potentials at each terminal.

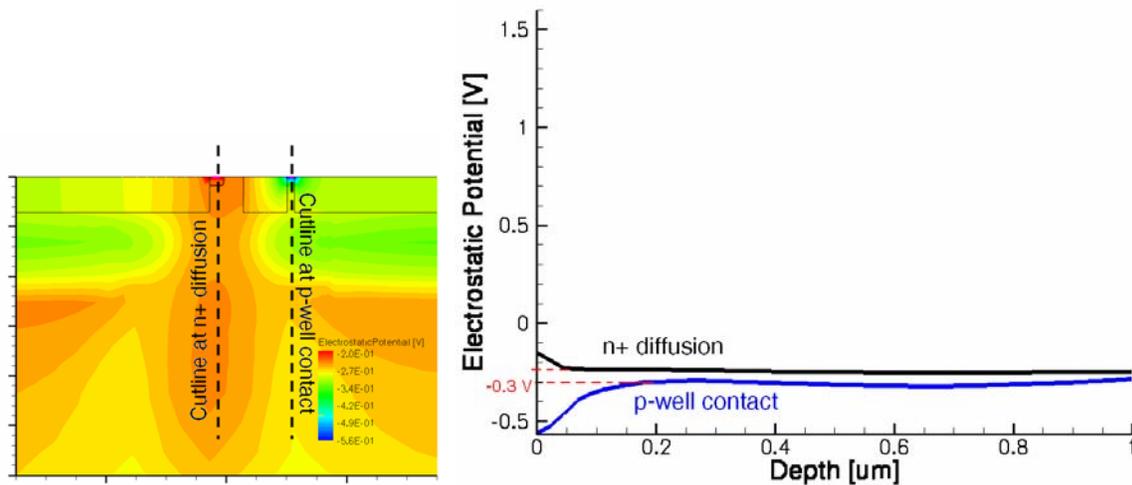


Fig 13. Electrostatic potential along the black dotted lines shown in the cross-section for dual-well system.

Any potential difference occurring between the p+ and p region at the p-well contact is reflected by a corresponding change in potential at the n+ diffusion. From Fig. 12, at the n+ diffusion contact, the potential is approximately -0.15 V, which translates to $(-0.15 - 0.56) \text{ V} = -0.71 \text{ V}$ in the potential reference system described above. Fig. 10 (b) shows the potential at the n+ diffusion to be at that level. The surface of the p-well contact is at -0.56 V (Fig. 13). There is a potential difference of about 0.26 V between the surface and at a depth of 0.2 μm below the contact. There is a drop of approximately 0.05

V between the n+ diffusion and the p-well. This makes the n+ diffusion contact go up by approximately 0.2 V, since the potential at the p-well contact is 0 V. Thus, the potential at the n+ diffusion goes $(0.2 + 0.56) \text{ V} = 0.76 \text{ V}$ below 0 V at the time of the upset. This is approximately the same value as obtained earlier.

In the case of the triple well (Fig. 14), at the n+ diffusion, the potential difference between the n+ diffusion and the p-well is the same as in the dual-well case, of $\sim 0.05 \text{ V}$. The surface of the n+ diffusion is at $\sim 1.56 \text{ V}$ with respect to E_i in the p-well. Thus, it is measured as $\sim 1 \text{ V}$. The potential of the upset voltage in Fig. 10 (c) is also approximately at that level.

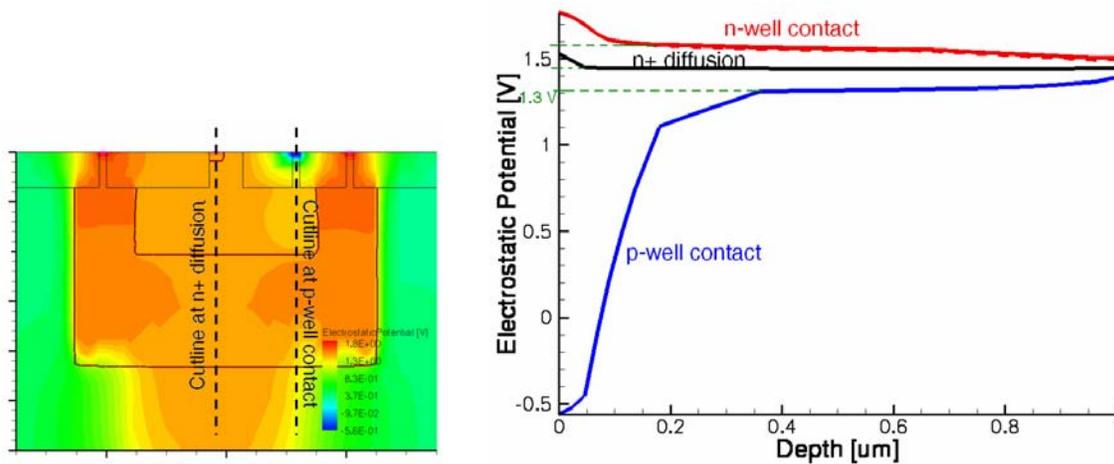


Fig 14. Electrostatic potential along the black dotted lines shown in the cross-section for triple-well system.

The potential difference between the p+ and p region at the p-well contact is high, around 1.86 V. This is because of the accumulation of holes in the p-well. A detailed explanation of this observation is given in Chapter 5. The p-well potential rises far above ground, $(1.3 - 0.56) \text{ V} = 0.74 \text{ V}$. The n-well contact is 1.76 V higher than E_i in the p-well, which could be measured as 1.2 V externally. There is a potential drop of $\sim 0.26 \text{ V}$

between the n⁺ and n region of each n-well contact. Thus, the n-well is at $(1.2 - 0.26 + 0.56) \text{ V} = 1.5 \text{ V}$. This ensures that the p-well – n-well junction is still reverse-biased. Since the n-well contact and the p-well contact are tied to fixed potentials, the total drop along the path connecting the two contacts is 1.2 V. The rise in p-well potential from ground (0.76 V), the difference between the p-well and n-well potentials ($\sim 0.1 \text{ V}$) and the drop at the n⁺-n region at the n-well contact ($\sim 0.26 \text{ V}$) adds up to roughly 1.2 V, as expected.

Now, considering the path connecting the p-well contact and the n⁺ diffusion contact, the p-well rises to 1.3 V due to the potential difference between the p⁺ and p regions at the well contact. The drop between the n⁺ diffusion and p-well is 0.05 V. Thus, the potential at the contact should be $(1.3 + 0.05 - 0.56) \text{ V} = 0.79 \text{ V}$, which is approximately what is obtained.

The potential difference occurring between the p⁺ and p regions at the p-well contact is caused by the excess carriers deposited by the ion strike. The LET of the strike determines the number of excess carriers generated. This alters the potential difference across the p⁺/p region of the well contact, and in turn, alters the potential at the n⁺ diffusion terminal.

3.5 Summary

When an ion strike hits the n⁺ region of a diode in a triple well, the charge collected at the struck node is less than that when an n⁺ region in a dual well is struck. The potential of the p-well rises above ground due to accumulation of holes, creating a potential difference between the p⁺-p region at the p-well contact. The degree of potential

difference depends on the number of carriers of one type dominating over carriers of the other type. The numerical calculations carried out in this chapter compare the conventions of potential reference in TCAD with reality. The calculations also demonstrate the potential redistributions occurring at different locations in the dual- and triple-well systems. A correlation between the potential differences at various junctions is obtained. The potential difference between the p⁺ and p regions of the p-well contact is determined by the p-well potential. Since the deposited charge neutralizes the depletion charge at the n⁺-p junction, the p-well potential determines the potential at the terminal of the n⁺ diffusion. The n⁺ diffusion contact is held by a current source, and its potential is allowed to change. Had its terminal been pinned to a constant voltage source, the effect of p-well potential would be on controlling the potential barrier between the n⁺ and p regions. In the following chapters, the impact of p-well potential on an n⁺ diffusion that is pinned to a constant voltage source is seen.

CHAPTER IV

ION STRIKES ON DRAIN OF DUAL-WELL AND TRIPLE-WELL NMOS DEVICES

In the previous chapter, single event effects in dual-well and triple-well substrates having a single n⁺ diffusion were considered. In this chapter, an NMOS device is simulated and the drain of the NMOSFET is struck with ions. Ion strikes of different LET values are considered. The p-well contacts of the dual-well and triple-well devices are of comparable sizes. The upset pulses at drain of an NMOSFET built in a triple well are compared with those in a dual well. The single-event upset voltage and current pulses are shown here. The physics behind these observations is dealt with in Chapter V.

4.1 Voltage and current pulses

Ion strikes that deposit a maximum initial charge density lower than the background doping of the substrate are classified here as low-LET ion strikes. Fig. 15 shows the acceptor and donor concentrations and the free carrier densities before and 10 ps after the peak of the carrier generation occurs for an ion strike of LET 1 and 40 MeV-cm²/mg.

It can be seen that the charge density deposited by an ion strike of LET = 1 MeV-cm²/mg at the peak of the Gaussian temporal profile (time t = 1 ns) hardly surpasses the background doping, while that by an ion having LET = 40 MeV-cm²/mg deposits a charge density two orders of magnitude greater than the background doping density at the

peak of the Gaussian temporal profile (time $t = 1$ ns. The difference in the physics of these two cases shall be explained in the following chapter.

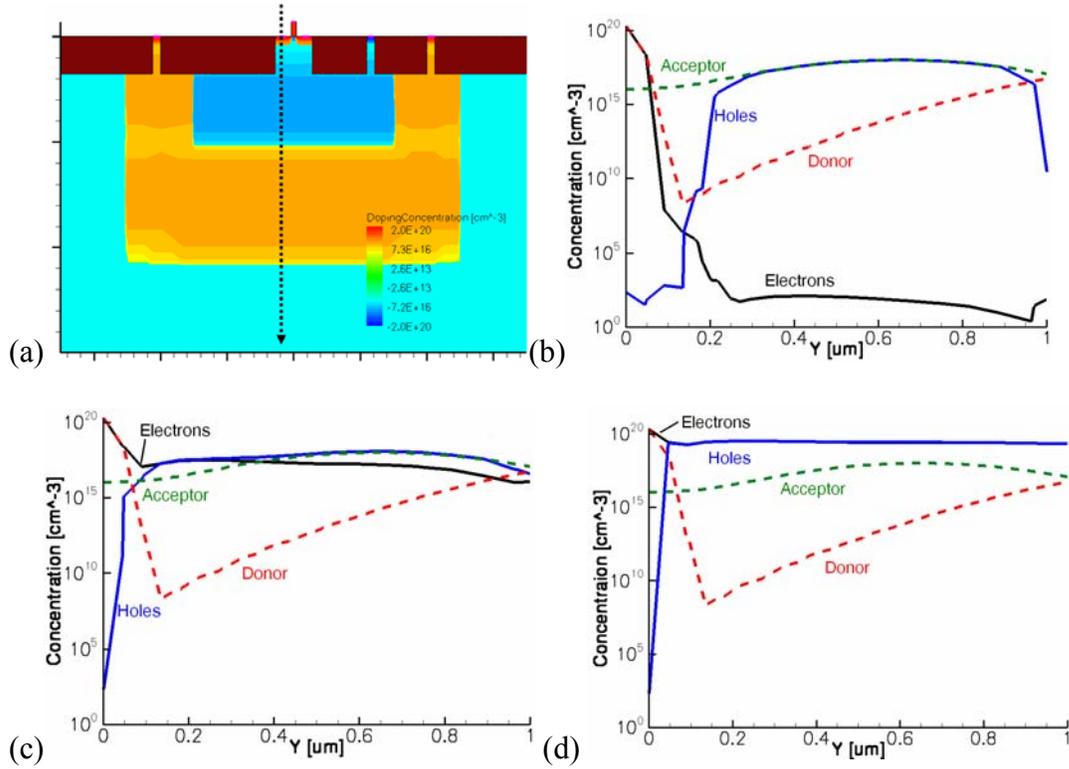


Fig. 15. (a) Cross section of a triple-well NMOSFET. The dotted arrow shows the location of the ion strike. Doping density and carrier concentrations in p-well (b) prior to ion strike, (c) 10 ps after an ion strike of LET = 1 MeV-cm²/mg, and (d) 10 ps after an ion strike of LET = 40 MeV-cm²/mg.

The upset pulse width depends on the LET of the ion. Figs. 16-23 show the voltage and current waveforms of dual- and triple-well NMOS drains when struck by ions having different energies. First, the results of a low-LET ion strike are shown. LETs of 0.25 and 1 MeV-cm²/mg are considered for low-LET strikes. LETs of 10 and 40 MeV-cm²/mg are considered for high-LET strikes.

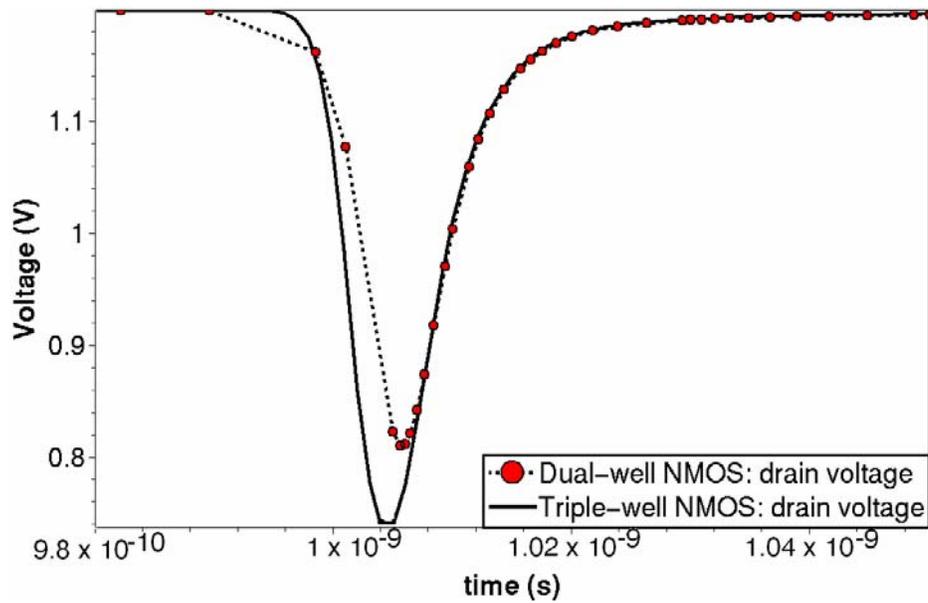


Fig. 16. Voltage at drain vs. time for an ion strike with LET = 0.25 MeV-cm²/mg

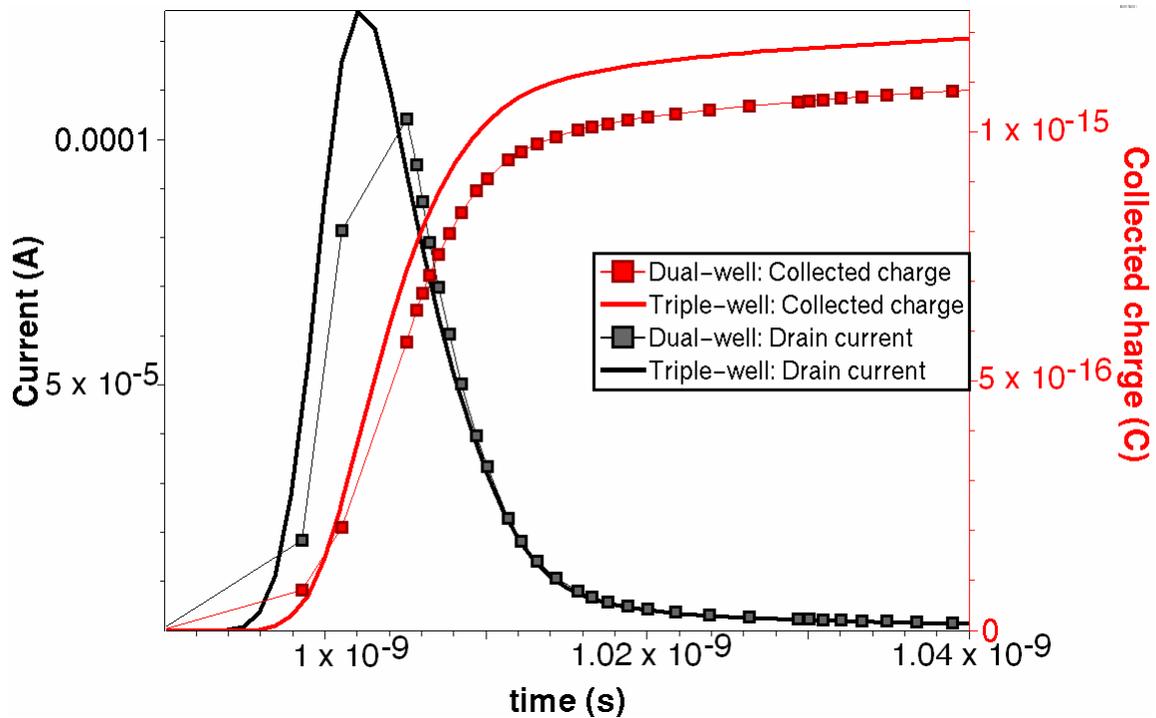


Fig. 17. Current and collected charge at drain vs. time for an ion strike with LET = 0.25 MeV-cm²/mg

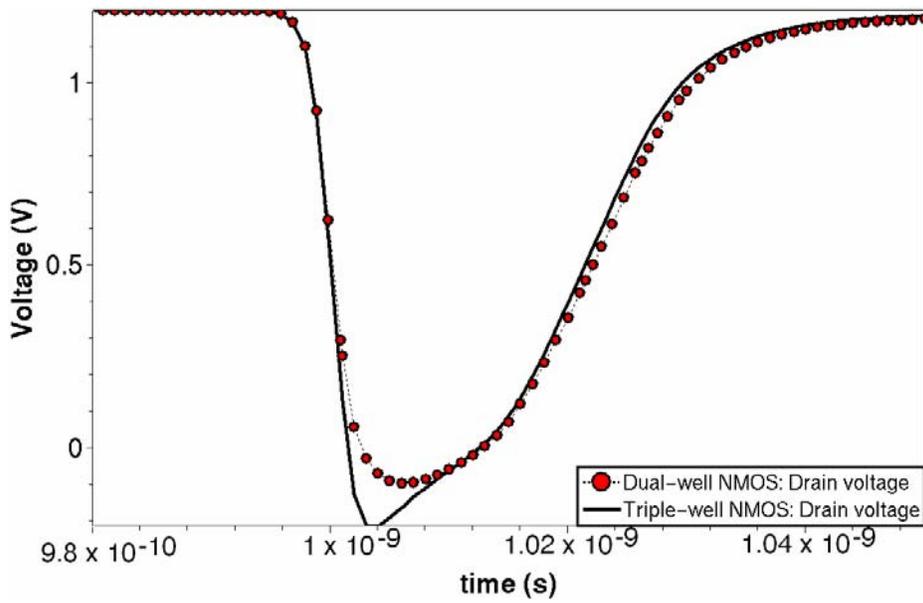


Fig. 18. Voltage at drain vs. time for an ion strike with LET = 1 MeV-cm²/mg.

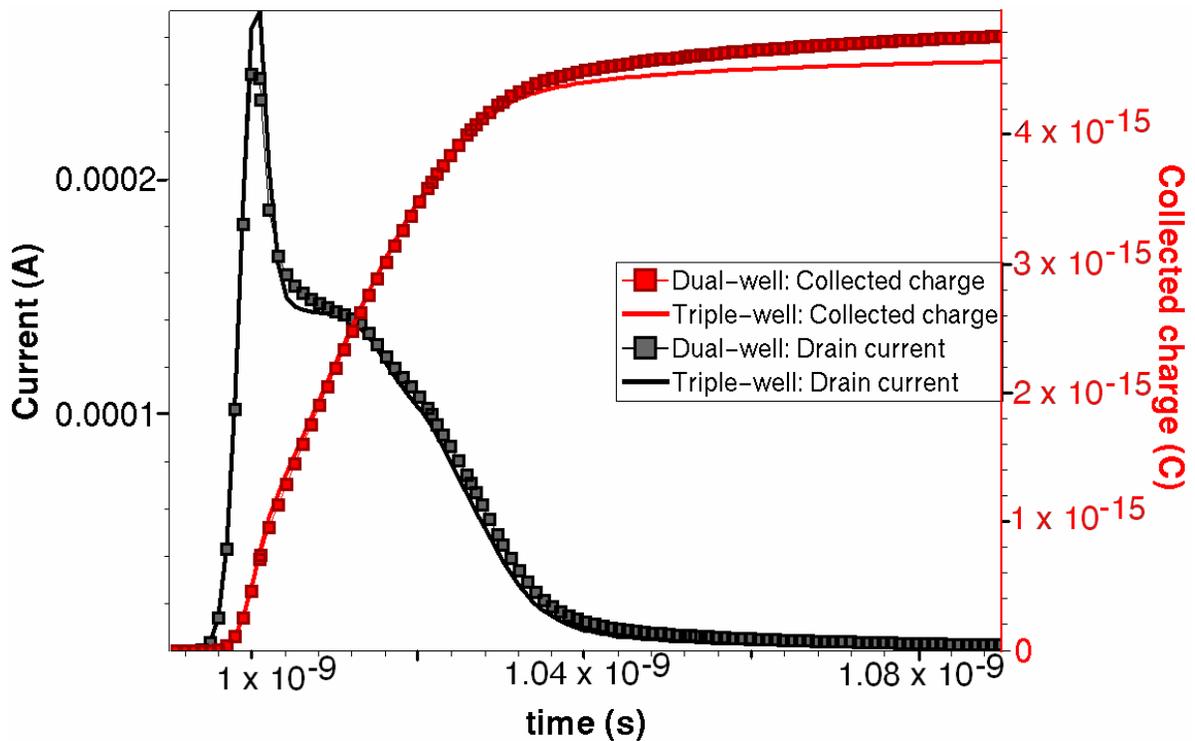


Fig. 19. Current and collected charge at drain vs. time for an ion strike with LET = 1 MeV-cm²/mg

From Figs. 16-19, it is seen that the voltage and current pulses that result from a low-LET ion strike on the NMOSFET drain are shaped as double exponentials. The difference in charge collected by the triple-well and dual-well NMOSFET is around a few tenths of a femtocoulomb. The current and voltage pulses are of the same width for the dual- and triple-well devices.

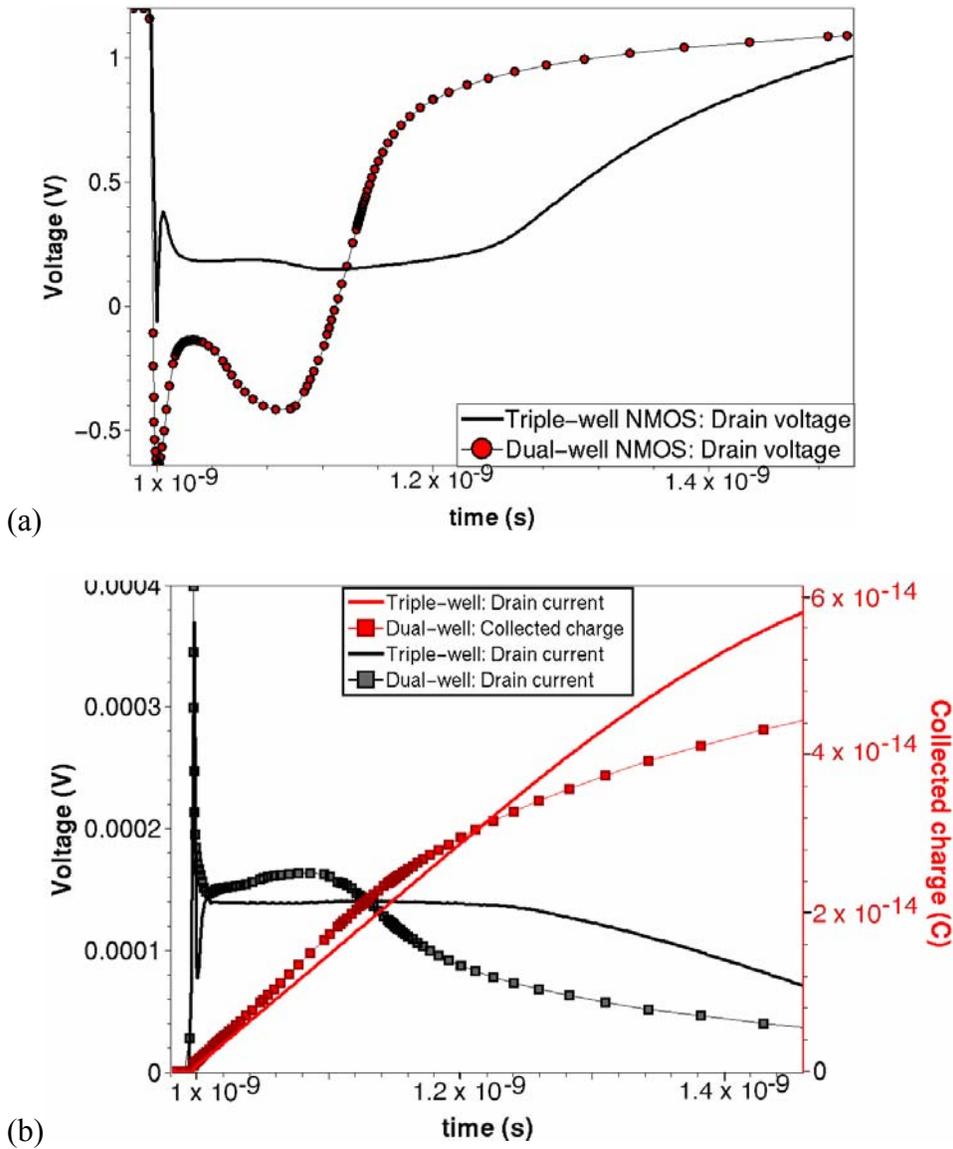


Fig. 20. (a) Drain voltage, (b) Drain current and collected charge vs. time for an ion strike with LET = 10 MeV-cm²/mg

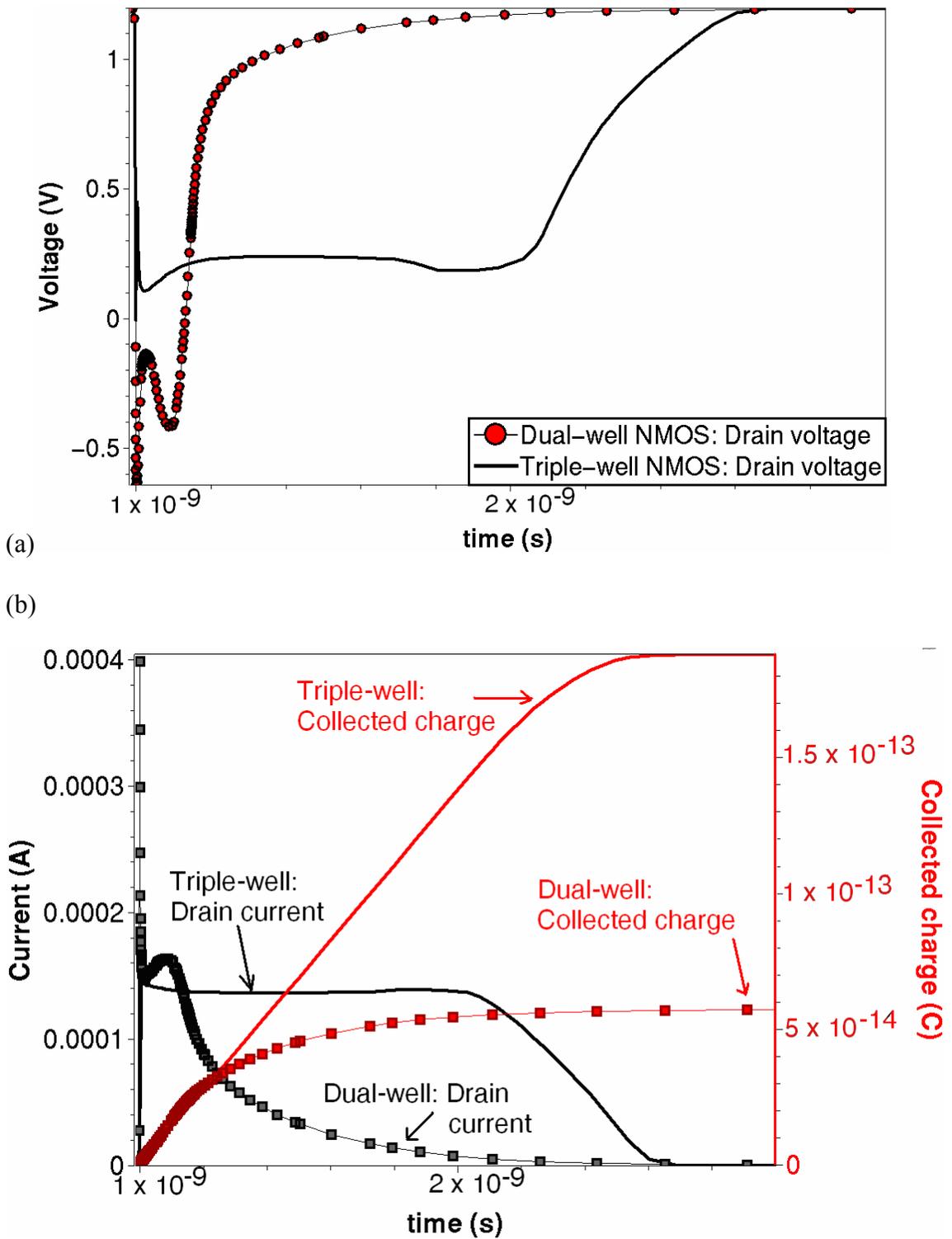


Fig. 21 (a) Voltage at drain, (b) Current and collected charge at drain vs. time for LET 40 MeV-cm²/mg

When the charge deposited by the ion strike is greater than the background doping of the substrate, the current and voltage waveforms show a distinct plateau, deviating from the classical double-exponential, as shown in Figs. 20-21. The reason behind the formation of this plateau is explained in [15]. The drain of the NMOSFET is restrained by a current source, the PMOSFET. The voltage at the drain is determined by the potential of the p-well. For an LET of 10 MeV-cm²/mg, the triple-well NMOS device shows current and voltage pulses twice as wide as the dual-well's. The charge collected by the triple-well NMOS drain is 1.3× the charge collected by a dual-well NMOS drain. An ion having LET of 40 MeV-cm²/mg causes pulse widths to widen to 6× as much as that of a dual-well NMOS device. The triple-well drain collects three times the charge that a dual-well drain collects.

4.2 Comparison of charge collected by single n+ diffusion and drain of NMOSFET in triple well

In Chapter III, the charge collected when a single n+ diffusion was struck with an ion with LET of 40 MeV-cm²/mg was noted. The increase in collected charge when another n+ region is implanted in the p-well to form an NMOSFET is shown in Fig. 22. The charge collected by the triple-well NMOS drain is twice that by the n+ diffusion of the diode in triple well in this case. This observation emphasizes the importance of the source in determining the single-event response of a triple-well device. This aspect is considered in detail in Chapter V.

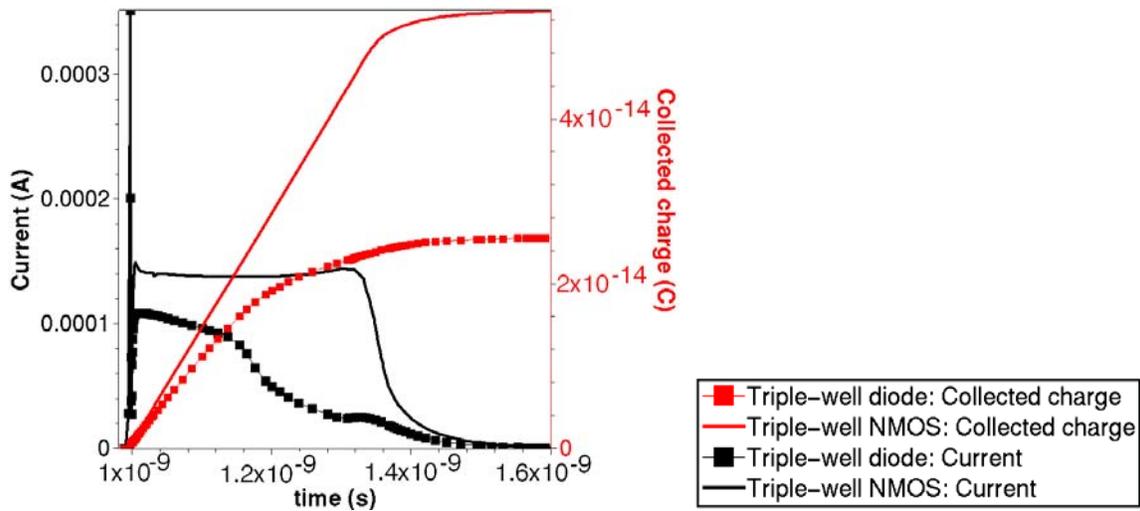


Fig 22. Current and collected charge vs. time for triple-well diode and NMOS.

4.3 Summary

Triple-well NMOS devices show wider single event pulses than dual-well devices for ion strikes that deposit a charge density greater than the background doping. When the charge deposited does not exceed the background doping, the classical double-exponential shape of the upset pulse is observed. The size of the NMOS and the p-well contact was the same for both the dual and triple well devices in this comparison. Also, the effect of the source in increased charge collection by a triple-well NMOSFET's drain as compared to a single n+ diffusion in a triple well is seen.

CHAPTER V

MECHANISMS BEHIND CHARGE COLLECTION IN TRIPLE-WELL NMOS DEVICES

In Chapter IV, it is shown that a triple-well NMOS device shows higher charge collection than a dual-well device, if the well contact sizes are the same. This chapter demonstrates why this is the case. The underlying difference between the charge collection mechanisms in dual-well and triple-well structures is explained. High-LET ion strikes depositing charge greater than the background doping of the substrate are considered here, primarily. Fig. 23 gives an overview of the mechanisms of charge collection in triple-well devices.

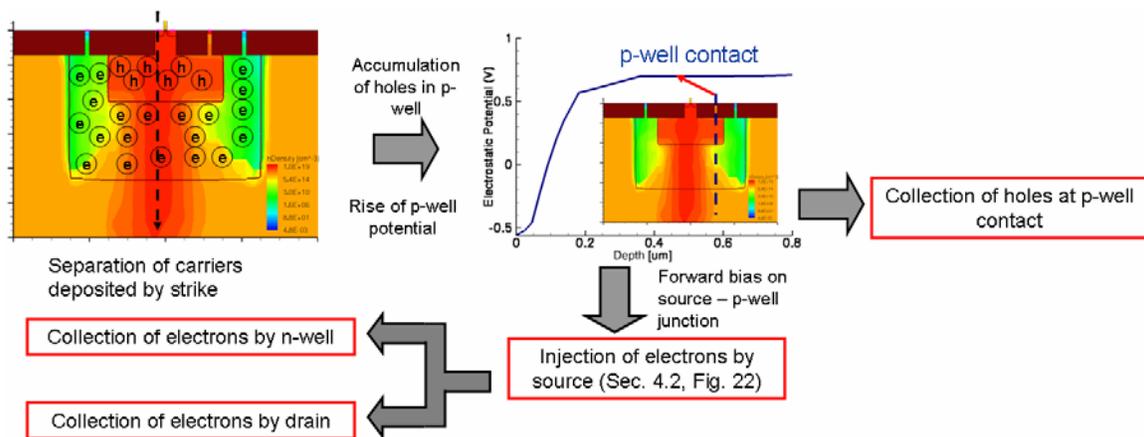


Fig. 23. Overview of the mechanisms of charge collection in triple well.

5.1 Separation of carriers

The major difference in the charge collection dynamics of dual-well and triple-well devices is the separation of generated carriers by the p-well – n-well junction of the triple well. When an ion strikes the drain of an NMOSFET and generates carriers, the carriers diffuse into the substrate. In a dual well, the electrons and holes diffuse all along the p-well and the p-substrate. In a triple well, the electrons drift into the n-well across the reverse-biased n-well – p-well junction. This leaves uncompensated holes behind in the p-well.

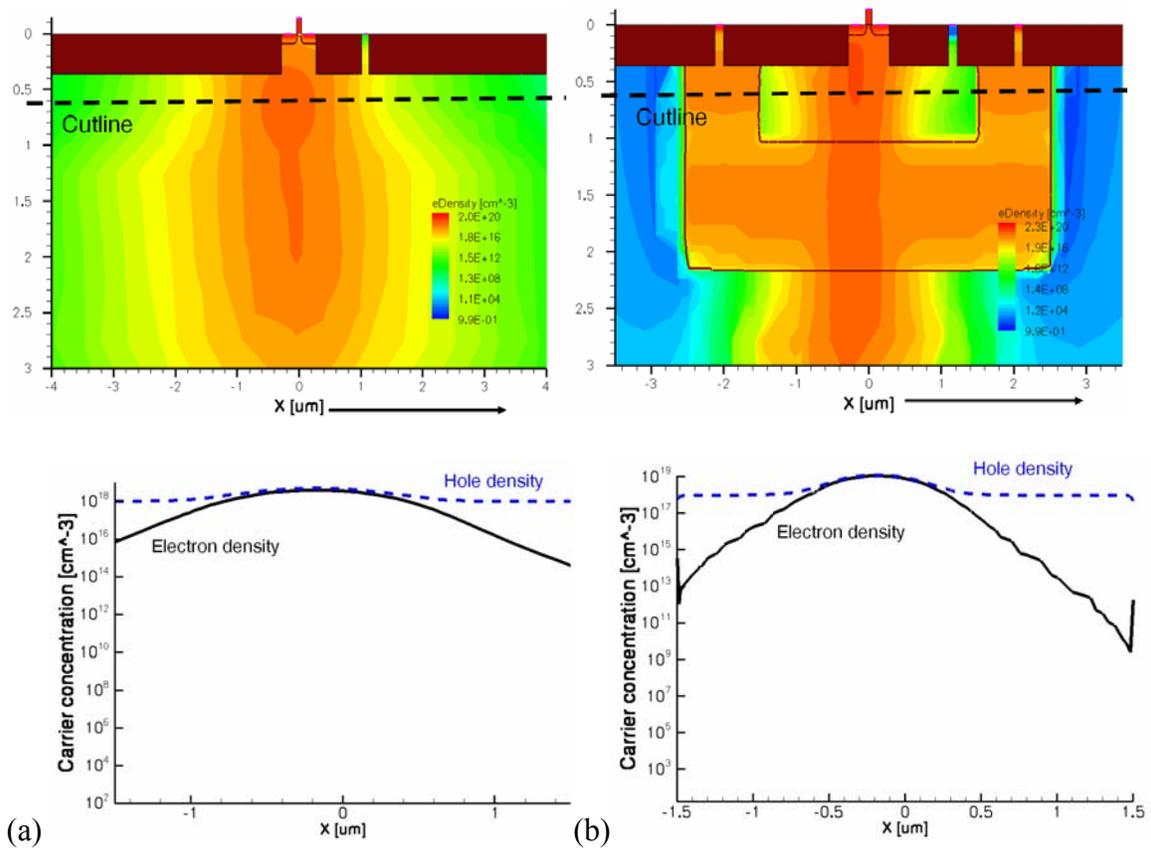


Fig. 24. Carrier concentration in (a) dual-well, (b) triple-well NMOS 10 ps after strike.

The n-well makes the most fundamental difference between a dual-well and the triple-well system by causing a separation of carriers and reducing the ambipolar nature of diffusion. In the case of the dual well, the electrons and holes deposited by the ion strike, although they have opposite charge, diffuse in the same direction, the direction that tends to minimize their energy. This diffusion is termed ambipolar diffusion. A net electric field is created due to charge separation as the carriers attempt to diffuse at different rates [16]. However, both types of carriers diffuse at approximately the same rate due to the electrostatic attraction between the positive and negative charges. The effective electron mobility gets reduced to approximately $400 \text{ cm}^2/\text{V}\cdot\text{s}$. The net electric field is negligible, therefore. Fig. 24 shows the difference in carrier concentrations in the primary well after the strike. There are more electrons in the p-well of the dual-well system than in the triple-well system. The ambipolar nature of diffusion is reduced in a triple well since the electrons are removed more effectively.

5.2 P-well de-bias

The accumulation of carriers of one kind in the p-well affects the potential of the well. The accumulation of holes in the p-well causes the potential of the p-well to rise. There is a difference in the potential redistributions in a triple well due to carrier confinement when compared to a dual well. In a dual well, the p-well gets de-biased much less than the p-well of a triple well. This section discusses the phenomenon of well de-biasing using Poisson's equation.

In Fig. 25, the electrostatic potentials along vertical cutlines taken at the drain, source and the p-well contact are shown for both dual- and triple-well cases. The drain –

p-well junction gets obliterated by the large number of carriers deposited by the ion strike in both cases. Significant differences are observed in the potential at the source and at the p-well contact.

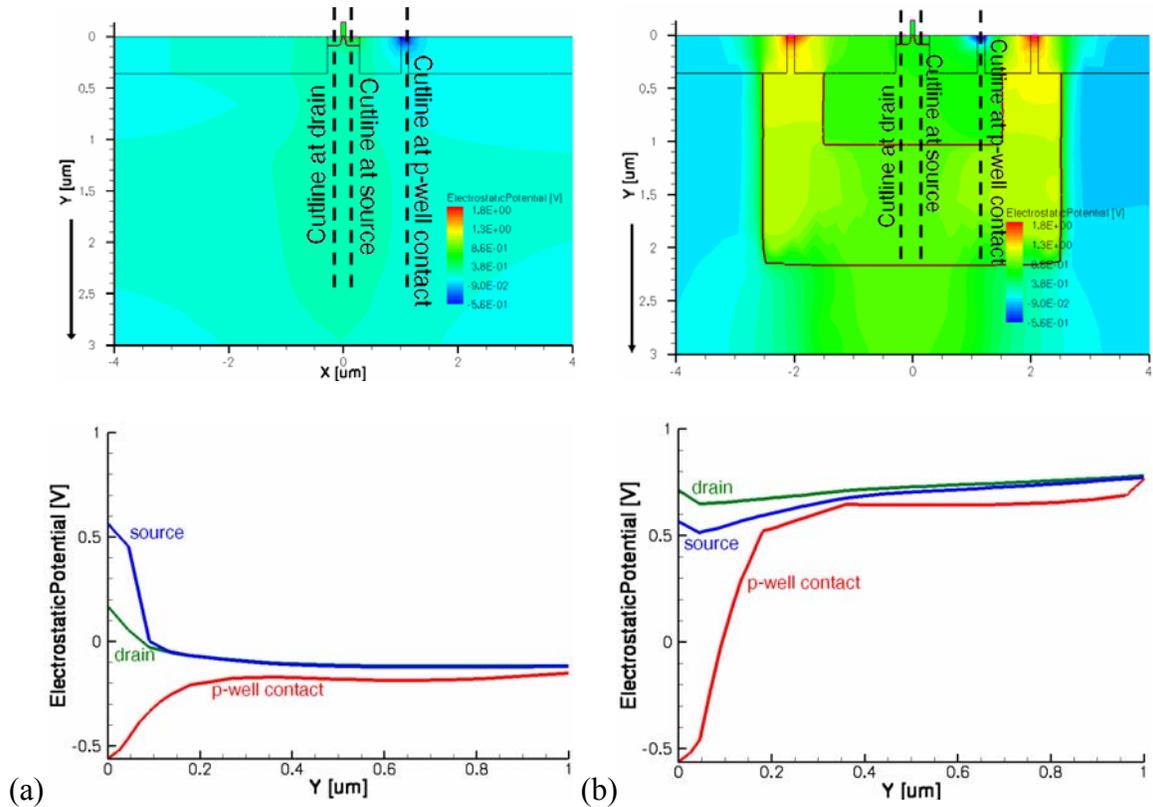


Fig. 25. Electrostatic potential for (a) dual-well. (b) triple-well NMOS devices along the cutlines shown by black dashed lines in the cross-sections.

From Fig. 25, it can be noted that the p-well potential in the triple-well structure rises to a value higher than that in the dual-well case. The effect of the rise of p-well potential on the p⁺ region of the well contact is shown here with an analysis of potentials and carrier concentrations.

The carriers generated from an ion strike diffuse into the surrounding region. The doping in the body of the p-well is approximately 10^{17} - 10^{18} atoms/cm³. The electric field

and the potential difference can be obtained by solving Poisson's equation at every point in the well. Let two regions in the well be considered: (a) the body of the well which has a Gaussian doping profile, and (b) the region near the well contact where the Gaussian profile of the well and the Gaussian profile of the contact intersect. First, the situation at equilibrium is considered. Fig. 26 shows the charge density and the electrostatic potential along vertical cutlines through region (a) and (b).

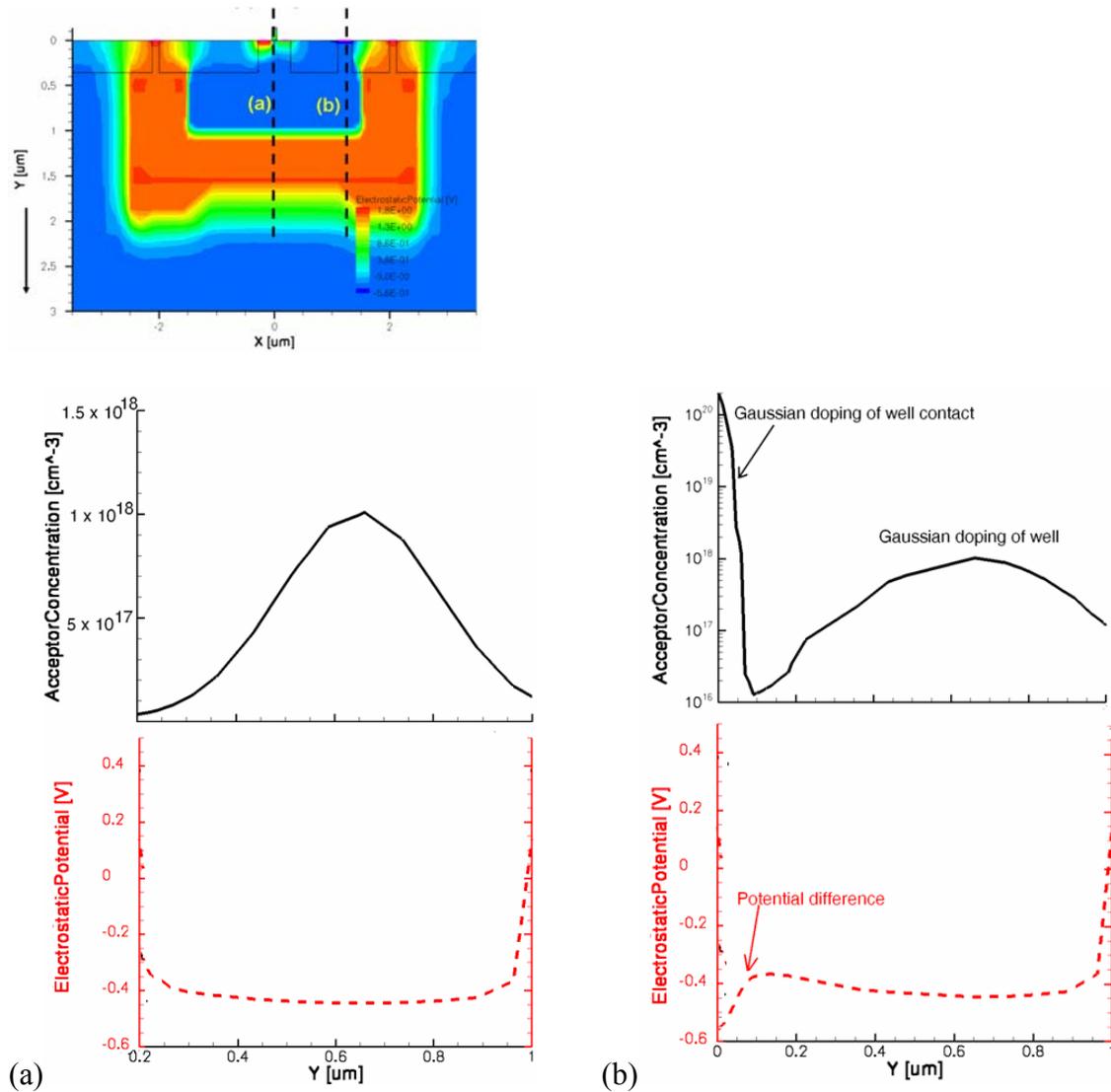


Fig. 26. Charge density and electrostatic potential during equilibrium along the black dashed lines shown in the cross section. (a) a cutline through the body of the well. (b) a cutline through the p-well contact.

Along the depth of the well (y-axis), the doping has a Gaussian profile. The hole density in the p-well is hence a Gaussian, as well. Let the well be divided into planes of constant doping. The difference in potential between any two such planes is given by

$$\frac{kT}{q} \ln \frac{N_m}{N_n} \quad (4)$$

where the subscripts denote different planes. The Gaussian doping chosen for the well has a peak which is about one order of magnitude higher than the valley of the Gaussian profile. This gives a potential difference of around 60 mV at room temperature. But, at the p+-p contact, there is a difference of four orders of magnitude in the peak doping of the p+ contact and the valley of the p-well Gaussian. This brings about a potential difference of around 0.2 V in the p+-p region.

The potential drop across a region of length x is given by Poisson's equation as:

$$V = \iint \frac{q}{\epsilon} (N_a + n - N_d - p) dx dx \quad (5)$$

where N_a and N_d stand for acceptor and donor concentrations, respectively while n and p stand for free electrons and holes, respectively. The potential difference is accounted for by the net charge enclosed in a region. At equilibrium, in the quasi-neutral region, the number of holes is given by the acceptor concentration and the number of electrons is given by the donor concentration. In the depletion region, the space charge is composed of uncompensated dopant atoms. So, in the depletion region $p - N_a$ or $n - N_d$ is negative, showing that the free carriers are less than the uncompensated acceptors. This is in accordance with the fact that in reality, the depletion region is not completely devoid of free carriers. Thus, in equation (5), the net charge given by $(n - N_d) - (p - N_a)$ gives the resultant electrostatic potential.

For the analysis of the situation during a single event, three cases are compared – (1) a dual-well system in equilibrium, which is equivalent to the triple-well system in equilibrium, (2) the dual-well system when struck with an ion, and (3) a triple-well system when struck with an ion. In Fig. 27, the carrier concentrations over and above the background doping are plotted along the depth of the p-well contact and the doping of the p-well body at equilibrium. The dual-well system is considered first.

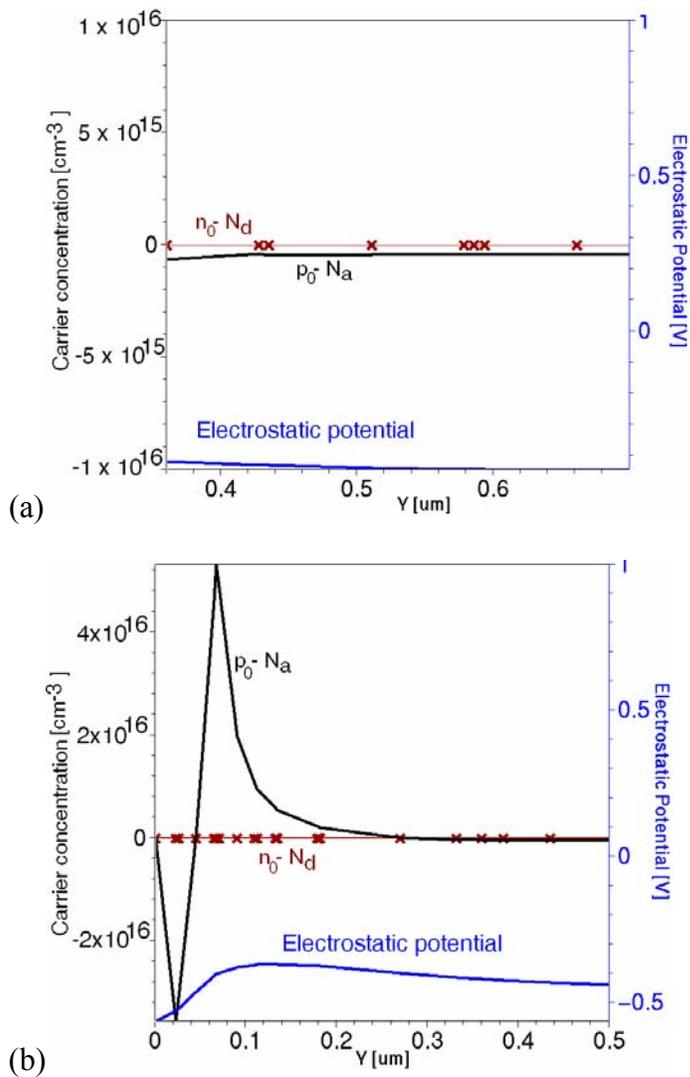


Fig. 27. $(p_0 - N_a)$, $(n_0 - N_d)$ and electrostatic potential at (a) p-well body, (b) p-well contact at equilibrium in a dual-well system.

Along the depth of the p-well, during equilibrium, there is a negligible number of carriers exceeding the background doping. Thus, the potential difference along the depth of the well is negligible. Whenever there is a doping gradient, the diffusion of carriers needs to be opposed by an electric field resulting from uncompensated donors and acceptors. There is an excess hole concentration due to holes diffusing from the p+ region into the p region. So, at the p+-p region of the well contact, the holes diffuse from the p+ region into the p region, causing an accumulation of holes there. The accumulated hole density surpasses the background acceptor concentration by $1 \times 10^{16} \text{ cm}^{-3}$ till a distance of 70 nm below the p-well contact. This accounts for 0.13 V of potential difference when integrated over this region. The electrostatic potential plot in Fig 27 (b) shows a similar value.

Now, considering the dual-well system again, when a strike occurs on the drain of the NMOS device with an LET of, say $40 \text{ MeV-cm}^2/\text{mg}$, around 10^{20} carriers cm^{-3} of both kinds are deposited along the ion track. In the dual-well system, ambipolar diffusion of carriers takes place. Thus, at any point between the struck region and the well contact, the number of holes approximately equals the number of electrons. Thus, there is hardly a potential drop across the entire well prior to the well contact. When the carriers reach the well contact, they cause the excess hole density to go beyond the background acceptor density by $\sim 1 \times 10^{16} \text{ cm}^{-3}$ for around $0.2 \text{ }\mu\text{m}$. Beyond this point, the excess electron density above the background donor concentration equals the excess hole density, thus nullifying the potential difference. Fig 28 (a) and (b) illustrates the situation. From (5), the potential difference across the p+-p region comes to approximately 0.3 V. The electrostatic potential in Fig 28 (b) corroborates this argument.

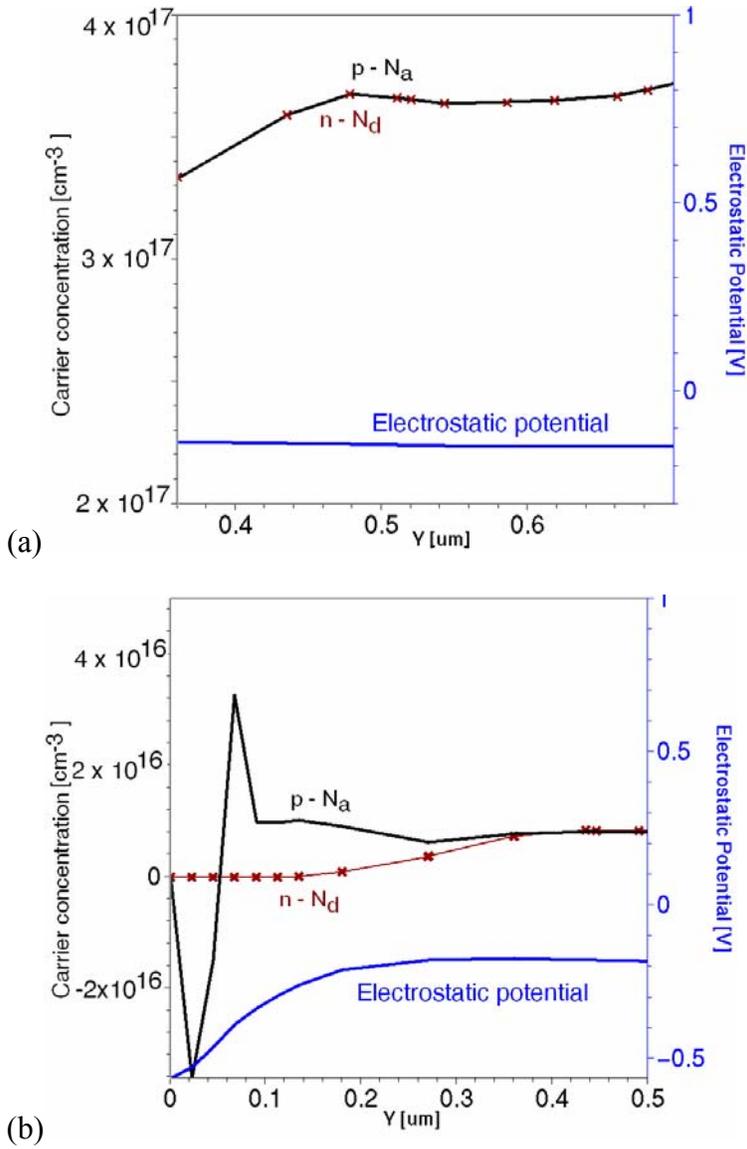


Fig. 28. ($p - N_a$), ($n - N_d$) and electrostatic potential at (a) p-well body, (b) p-well contact 50 ps after strike in a dual-well system. Here, $p = p_0$ (number of carriers at equilibrium) + δp (injected carriers), and $n = n_0 + \delta n$.

Now, the case of the triple well is considered. Fig. 29 shows the excess carrier concentrations in the triple-well after the strike. As the n-well effectively draws in electrons from the strike, there is a difference in excess hole and electron concentrations in the p-well body. But, the difference is around $1 \times 10^{15} \text{ cm}^{-3}$, which translates to a

potential difference of 0.03 V. between the top of the well (under the STI) and the bottom of the well (above the deep n-well). Near the contact, the excess hole density is $1 \times 10^{16} \text{ cm}^{-3}$, like the dual-well case. But since the p-well accumulates holes, this concentration is maintained for a distance of around $0.4 \text{ }\mu\text{m}$ down the contact, as opposed to the $0.2 \text{ }\mu\text{m}$ in the dual-well case. The potential difference across this region is calculated to be around 1.2 V. The potential plot in Fig. 29 (b) corroborates this value.

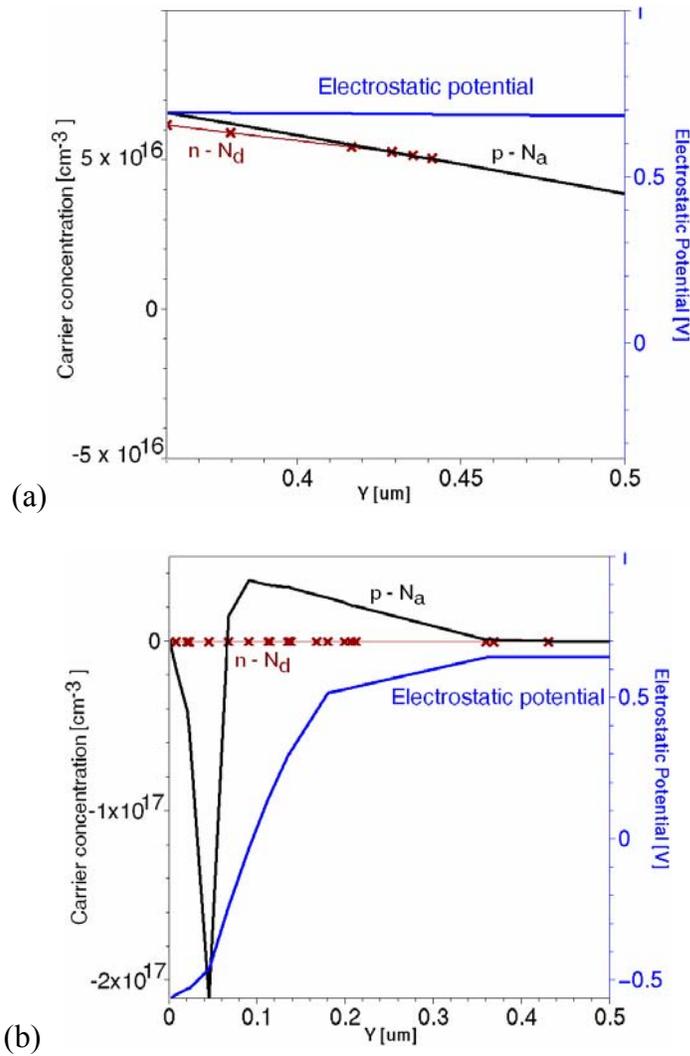


Fig. 29. $(p - N_a)$, $(n - N_d)$ and electrostatic potential at (a) p-well body, (b) p-well contact at equilibrium in a triple-well system. Here, $p = p_0$ (number of carriers at equilibrium) + δp (injected carriers), and $n = n_0 + \delta n$.

It can also be noticed that the depletion charge in the p⁺ region of the triple well (Fig. 29 (b)) is greater than the depletion charge in the p⁺ region of the dual well (Fig. 28 (b)). The greater rise in p-well potential in the triple well compared to the dual well causes an adjustment of potential across the p⁺-p junction at the p-well contact. A greater amount of depletion charge in the p⁺ region of the triple well accommodates a stronger field and a higher potential difference at the junction between the p⁺ and p regions.

To summarize the arguments, the accumulation of holes in the p-well causes the potential of the p-well to rise. The rise of potential of the p-well in the triple-well case is higher than the dual-well case, because the p-well accumulates more holes in the triple well case. Since the p-well contact is pinned to 0 V, the p-well potential rise is manifested by a large potential difference across the p⁺-p junction. The p-well potential is shown to be around 0.65 V with respect to the intrinsic Fermi potential of the semiconductor, as opposed to -0.2 V for the p-well in the dual-well case. The effect of confinement of one kind of carrier causes the p-well of the triple well to be more de-biased compared to the p-well in a dual-well system.

5.3 Electron injection by source

The difference between the source of an NMOSFET in dual well and the source of a triple-well NMOSFET lies in the injection of electrons into the well in the triple-well case. Until now, the events occurring in the triple-well case have been exactly the same as those in the case where a single n⁺ diffusion was present in the p-well of a triple well. The presence of a source in the NMOS device makes a significant difference to the single-event response of devices that are built in a well, which, in turn, is surrounded by

another well of the opposite kind of dopant. This difference was observed in Fig. 23 of Chapter IV.

Figure 25 shows the electrostatic potential under the source in the dual-well and the triple-well case. The dual-well source has a potential barrier with the p-well, which is almost eliminated in the triple-well case. When the device is not yet struck with an ion, there is a potential barrier between the n-type source and the p-type well. When the p-well potential rises (as explained in 5.2), the barrier between the source and the p-well starts getting eliminated, effectively forward biasing the junction. This facilitates the movement of carriers of both types across the junction. The source, being n-type, injects electrons into the p-well. Thus, besides the electrons that were deposited by the strike, there are electrons injected by the source.

In Fig. 30, the source current components of a dual-well and a triple-well NMOSFET are shown. For the dual-well case, the electron current goes into the source, showing the electrons are moving from the p-well into the n-type source. This indicates that the source – p-well junction is reverse-biased. The hole current is negligible, since there are not many minority carriers in the heavily doped n-type source. In the triple-well device, the electron and hole currents are in the same direction. This implies that electrons are moving from the source into the p-well and holes are moving in the opposite direction. This resembles diffusion current across a forward-biased p-n junction. The source will continue to inject electrons into the p-well as long as the p-well remains de-biased, that is, as long as there are excess holes in the p-well which keep the p-well potential high.

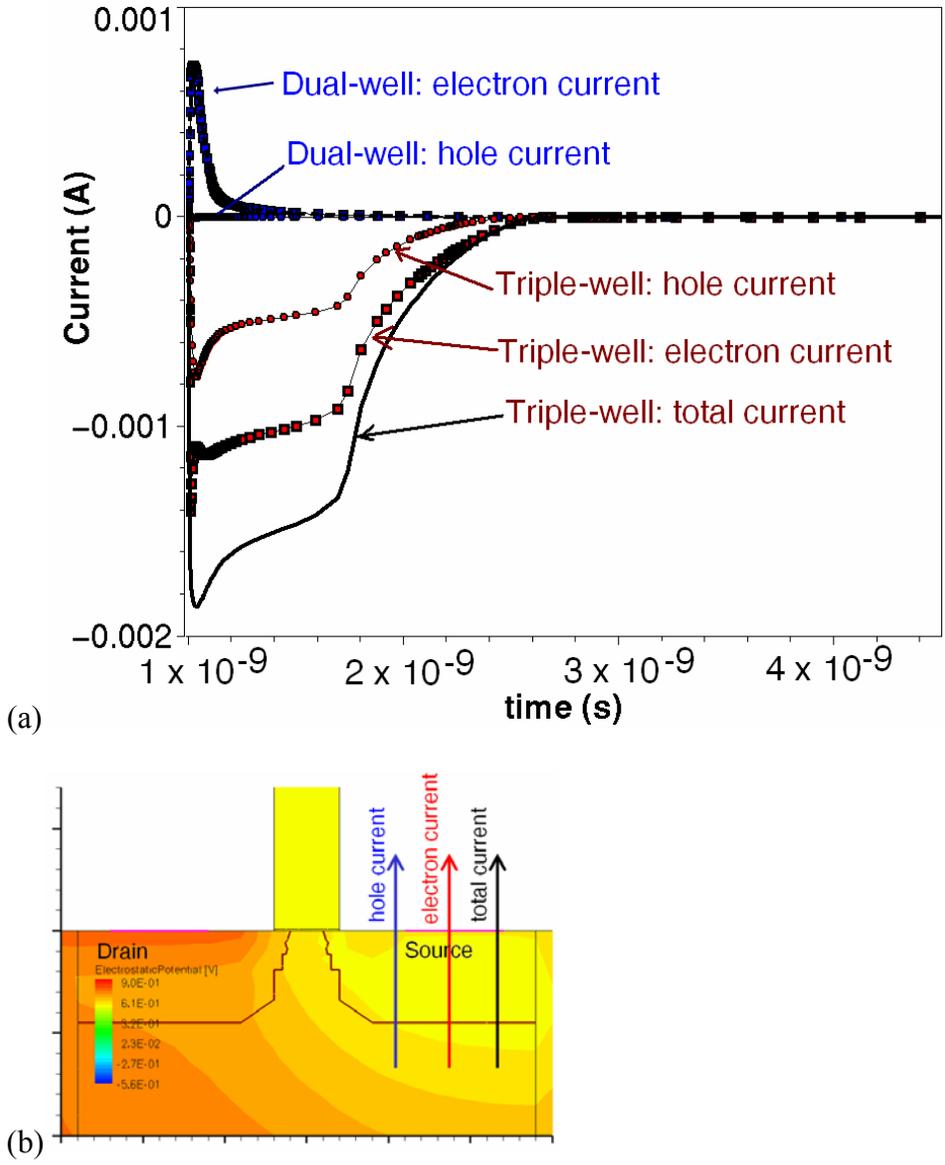


Fig. 30. (a) Source current components of dual-well and triple-well NMOS devices, (b) direction of currents in triple-well source.

5.4 Source – p-well – drain current path

Since the source injects electrons into the p-well in a triple well, it is useful to investigate where those electrons are collected. From here on, the triple well is discussed solely. The dual-well case is discussed in detail in [15]. Once the electrons are injected into the p-well of a triple well by an ion strike, they need to be collected into an n-type

region. The drain of the NMOS device is one possible region into which the electrons can flow. To investigate the possibilities, the energy bands along the path connecting the source to the drain through the p-well are shown in Fig. 31 (c). The quasi-Fermi levels give an indication of the carrier concentrations along the path. There is a negligible energy barrier between the drain and the substrate. Thus, there is negligible electric field that can help electrons (minority carriers in the p-well) drift into the drain. There can be diffusion alone, and a diffusion gradient of around 4×10^{18} electrons per cm^{-3} exists between the drain and the p-well for approximately $0.4 \mu\text{m}$. The total electron current density as a function of the gradient in quasi-Fermi gradient is given as:

$$J_n = -q\mu_n n \frac{dE_{F_n}}{dx} \quad (6)$$

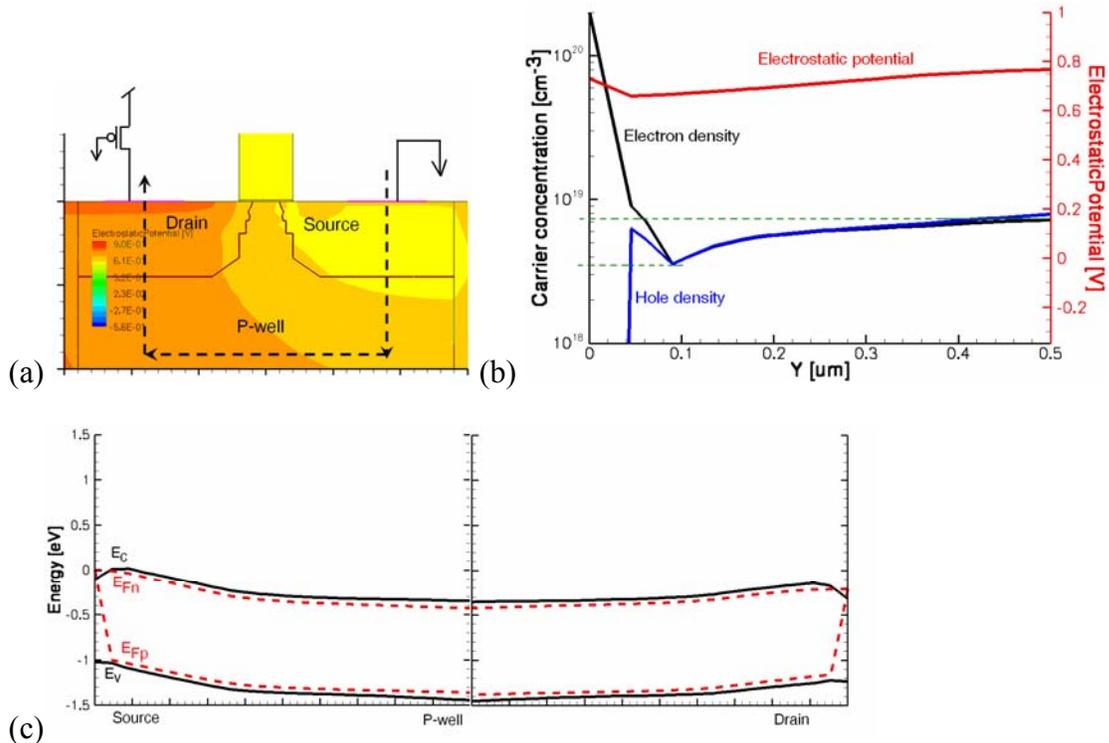


Fig. 31. (a) Cross-section of an NMOSFET showing the current flow path between source and drain through the p-well. (b) Electron and hole concentration and electrostatic potential along a vertical cutline through the drain (c) Energy band diagrams along the path shown in (a).

The existence of a finite quasi-Fermi level gradient and the presence of a large number of carriers in the region cause a large current to flow into the drain from the p-well. Hence, the source – p-well – drain path can drain out some electrons from the p-well, but not all.

5.5 Source – p-well – n-well current path

The source – p-well – drain path allows electrons to diffuse out of the drain. The other prospective path of electron flow is the source – p-well – n-well path. The p-well – n-well junction is reverse-biased in equilibrium. Except for the part of the junction whose barrier gets obliterated by the large number of carriers deposited by the ion strike, most of the junction remains intact and reverse-biased. Fig. 32 illustrates the collection path from NMOS source to the n-well.

The n-well collects more electrons than the drain because of the large area of the reverse-biased n-well – p-well junction. Fig. 33 shows the total n-well current and the total source current as a function of time. There are two n-well contacts. The source current is seen to almost equal the total n-well current through the two contacts at any instant of time. Thus, the electrons deposited from the ion strike, and those injected by the source are mostly collected by the n-well.

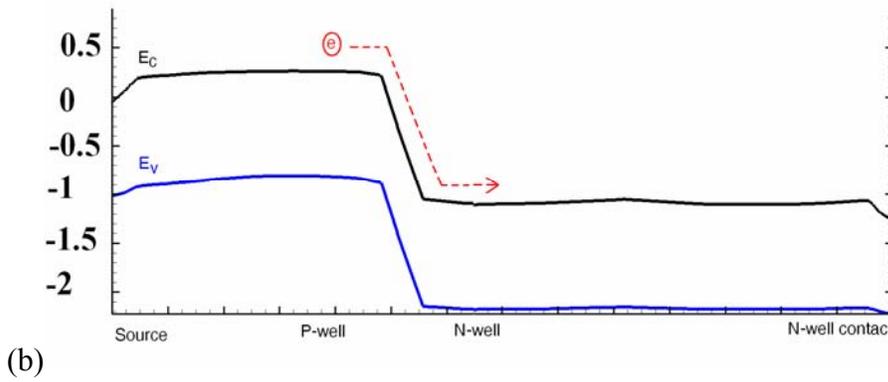
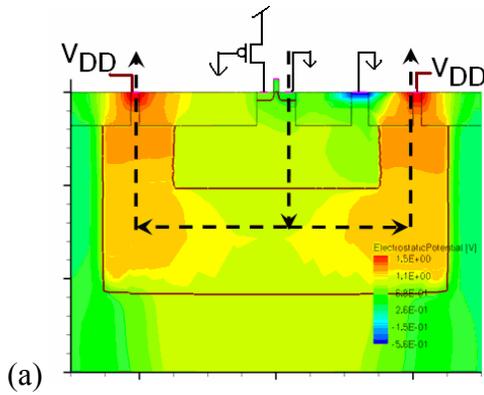


Fig. 32. (a) Cross-section of triple-well NMOSFET showing a current path connecting the source to the n-well through the p-well. (b) Energy band diagram along the path in (a).

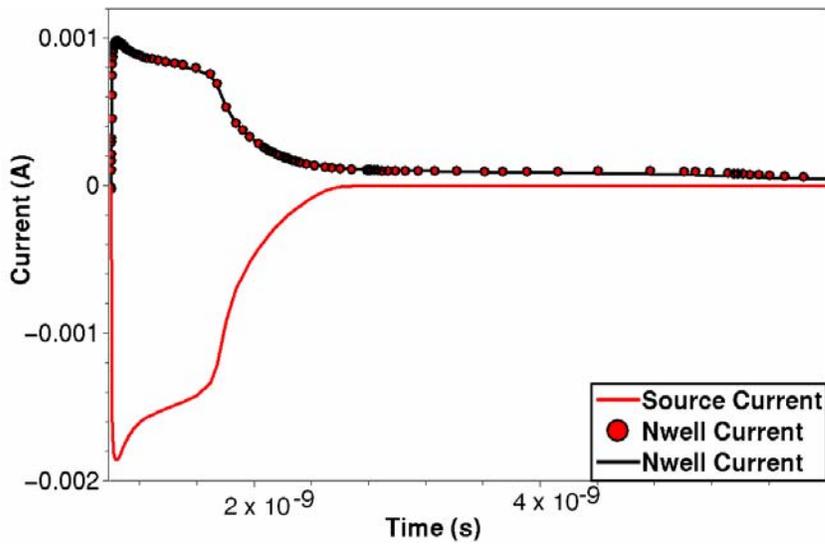


Fig. 33. Source and n-well current vs. time for a triple-well NMOS device. There are two n-well contacts shown. The source current is approximately equal to the total n-well current.

5.6 Summary of charge collection mechanisms in triple well

In this chapter, the mechanisms behind single-event charge collection are discussed and a comparison is made between charge collection mechanism in dual-well and triple-well NMOS devices. In both dual- and triple-well structures, the potential of the p-well rises from its equilibrium value. In the case of the triple well, the p-well accumulates more holes than electrons. This causes the p-well potential to rise higher in the case of the triple well. The p⁺ region of the p-well contact is pinned to 0 V. The rise in the p-well potential is reflected by the enhancement of the potential barrier between the p and the p⁺ regions. The effect of the rise in p-well potential should be similar for the source diffusion region which is pinned to 0 V, except for the source being an n-type region. Thus, the effect of the rise of p-well potential is the reduction of the potential barrier between the source and the p-well, effectively forward-biasing the source – p-well junction. This causes the source to inject electrons into the p-well. In the case of the dual well, the p-well potential does not rise high enough to forward-bias the source – p-well junction.

The electrons injected by the source and those deposited by the strike can be collected by the drain and the n-well. Since the n-well – p-well junction is much larger than the drain – p-well junction, the n-well collects more electrons than the drain. However, the diffusion gradient at the drain is high enough to allow the flow of electrons into the drain, causing triple well to collect more charge than dual well. The recovery of the system depends upon the rate of removal of holes from the p-well. As long as the p-well remains de-biased, the source continues to inject electrons into the well. The key to

faster recovery of the system lies in the effectiveness of the p-well contact in the removal of holes.

5.7 Low-LET ion strikes

The analysis above has been made for a deposited charge density surpassing the background doping density. When the ion striking the drain has a relatively low LET, the charge deposited by the strike is not enough to perturb the equilibrium significantly. The upset voltage pulses follow a double-exponential shape due to the reduction and renewal of the space charge at the junctions (charging and discharging of junction capacitances). At the p-well contact, the situation is not too different from equilibrium for an LET of $0.25 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. For an LET of $1 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the excess holes create a significant potential difference at the p+-p region of the p-well contact. But, in neither case does the potential of the p-well rise enough to forward bias the source – p-well junction.

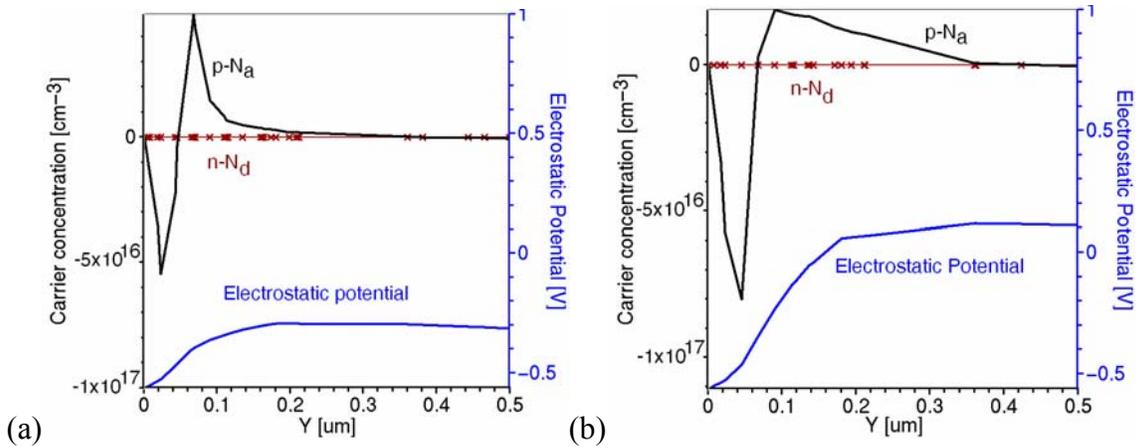


Fig. 34. $(p - N_a)$, $(n - N_d)$ and electrostatic potential at p-well contact in a triple-well system during an ion strike of (a) $0.25 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, (b) $1 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. Here, $p = p_0$ (number of carriers at equilibrium) + δp (injected carriers), and $n = n_0 + \delta n$.

5.8 Summary

In this chapter, the mechanism of charge collection in triple-well NMOS devices is explained. The mechanism is compared with charge collection mechanisms in dual-well NMOSFETs. The charge collection mechanisms are explained for high-LET ion strikes. The primary mechanism is de-biasing of the inner p-well and forward-biasing of the NMOS source, which injects electrons into the inner p-well. The fundamental physics is applicable to low-LET ion strikes as well, and it is demonstrated that the perturbation of the well bias for low LETs is not sufficient to forward-bias the NMOS source. The mechanisms of charge collection outlined here are important for devising techniques of single event upset mitigation. It is seen that the removal of holes from the p-well is essential in recovering from the upset. Also, preventing or, at least, reducing p-well de-bias is useful in reducing upset pulse widths. The factors affecting the NMOSFET's drain potential during the single event are explained in Appendix I. The theory developed here is applicable for explaining the charge collected when a PMOSFET's drain is struck with an ion.

CHAPTER VI

EFFECT OF WELL DESIGN PARAMETER VARIATIONS ON SINGLE EVENT PULSE WIDTH

In the previous chapter, the observation is made that the key to recovery of the single-event upset lies in the rate at which excess holes are removed from the p-well of a triple-well system. In this chapter, four design parameters in triple-well engineering are varied to test the effect of those variations on the upset voltage pulse width. The well contact size, p-well contact doping depth and placement, and p-well – n-well junction depth are varied. Also, the bias on the p-well is varied. The effects of these variations are explained with the help of the mechanisms of charge collection developed in the previous chapter. Ion strikes with LET of 40 MeV-cm²/mg have been used in all cases.

6.1 Contact size

The size of the well contacts can be altered to speed up the removal of carriers from the wells. In this section, initially the p-well contact size is varied, keeping the n-well contact sizes the same. The voltage and current pulses are plotted after the single event ion strike. Then, the n-well contact size is changed for the same p-well contacts, and the current and voltage pulses plotted. In all cases, a backside contact for the substrate that extends all along the length and breadth of the substrate is used to simulate the strong substrate contacts in real devices. A weak substrate contact reduces the reverse-bias on the n-well – p-substrate junction and makes the n-well less effective in

drawing electrons into it. In such a case, the p-well de-bias is low compared to when the substrate is strongly contacted. Thus, the pulse width is narrower for a weakly contacted substrate than for a strongly contacted one.

6.1.1 P-well contact size

First the size of the p-well contact is varied to study its effect on the upset voltage pulse. The contacting schemes are shown from a layout view of the structures in Fig. 35. In one structure, the p-well contact is of an area of $0.36 \mu\text{m}^2$, while in the other, the p-well contact area was increased to $2.125 \mu\text{m}^2$. After a single event strike of LET $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ to the drain of the NMOS device in the off state occurs for the two structures, the current and voltage at the drain are plotted with respect to time. Fig. 36 shows the results.

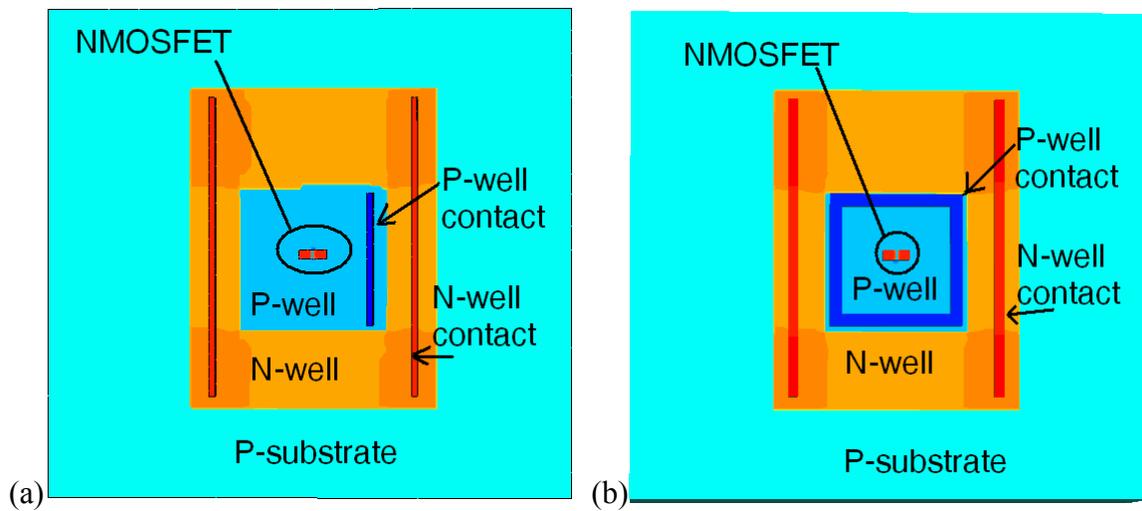


Fig. 35. Layout showing p-well contacting schemes. (a) The small p-well contact has an area of $0.36 \mu\text{m}^2$. (b) The large p-well contacts, surrounding the NMOS device, occupy a total area of $2.125 \mu\text{m}^2$. The area of the large contacts is 6 times that of the small contact.

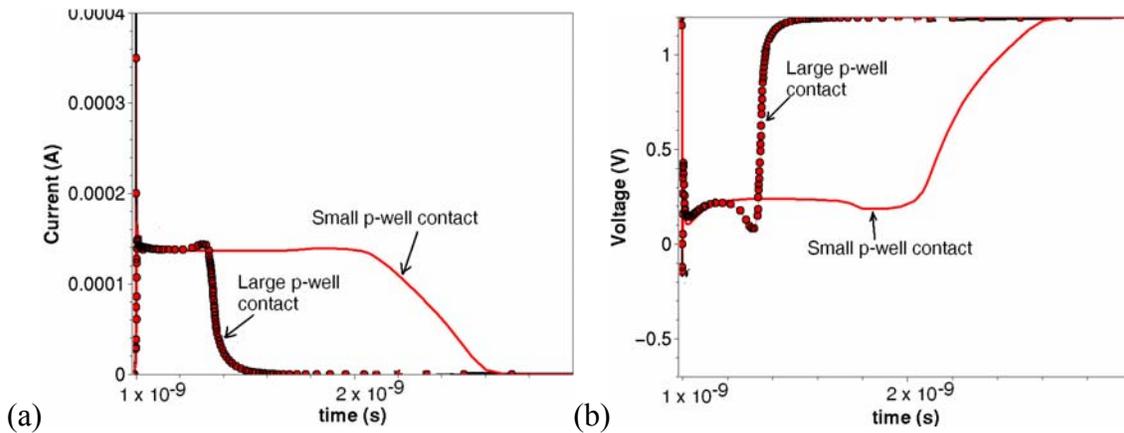


Fig. 36. (a) Current and (b) voltage vs. time for triple-well NMOS drains for large and small p-well contacts.

The reason why a larger primary (p-well) contact helps in the reduction of upset voltage/current pulse width can be explained easily. The larger contact expedites the removal of holes from the p-well because of a larger surface through which carriers can move, helping the recovery of the system. In order to analyze the difference due to variation in contact sizes, the electric field and electrostatic potential at the p⁺-p region of the p-well contact in a triple-well structure with small and large contacts are plotted in Fig. 37. The electric field plotted is the vector sum of the horizontal and vertical electric fields. At the small contact, a larger potential gradient occurs because of a slightly stronger electric field. The larger contact removes holes more effectively from the p-well compared to the smaller contact. The p-well potential is, hence, lower for the larger contact than for the smaller contact. The potential gradient across the p⁺-p region at the well contact is greater for the smaller contact than for the larger contact. The holes deposited from the strike diffuse into the p-well. When the holes come near the contact, the rate of removal of the holes across the p⁺-p region is limited by the number of holes that can reach the contact. The opening to the contact creates an accumulation of holes at

the neck of the STI, and repels additional holes from entering into the contact region. The large p-well contact reduces this effect by allowing more holes to drift out of the p-region into the heavily doped p+ region.

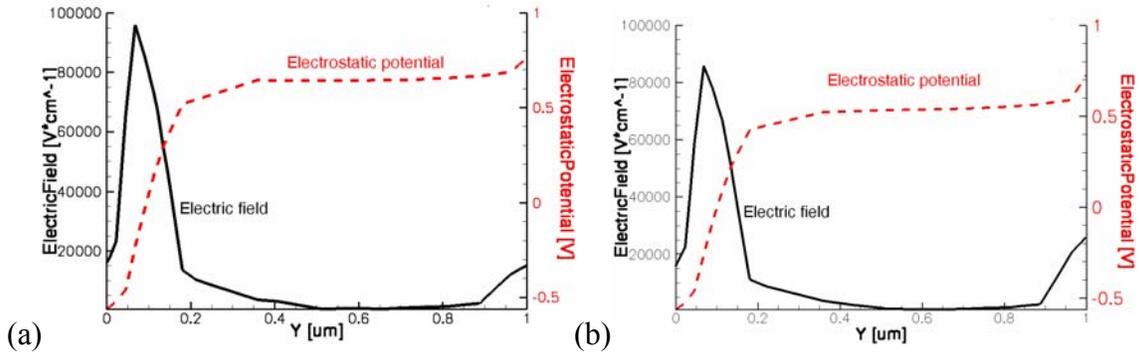


Fig. 37. Net electric field and potential at the p+-p contact region for a triple-well structure with (a) small p-well contact (b) large p-well contact.

There is another mechanism that affects the collection of holes at the p-well contact. The p-well contacts hold the potential of the well near the contact to ground. When the potential of the well near the strike floats up due to the deposition of the charges, the regions below the contact still remain close to ground. There is thus a potential gradient along the well that aids in the movement of holes towards the contact. A larger contact helps faster removal of holes in this way. In Fig. 38, this effect is shown. A horizontal cutline is taken across the entire substrate at a depth of 0.6 μm . At the struck region the potential is high. The p-well contacts on either side of the p-well holds the potential of the well to a low. A potential hill is created, helping holes to move at a higher rate to the contacts. Hence a large well contact results in speedy removal of holes, not only because it provides a large area for carrier collection at the contact, but also because of the potential gradient it creates inside the well. It should be remembered that, in the

case of the large contacts, diffusion of injected carriers is assisted by drift in the same direction.

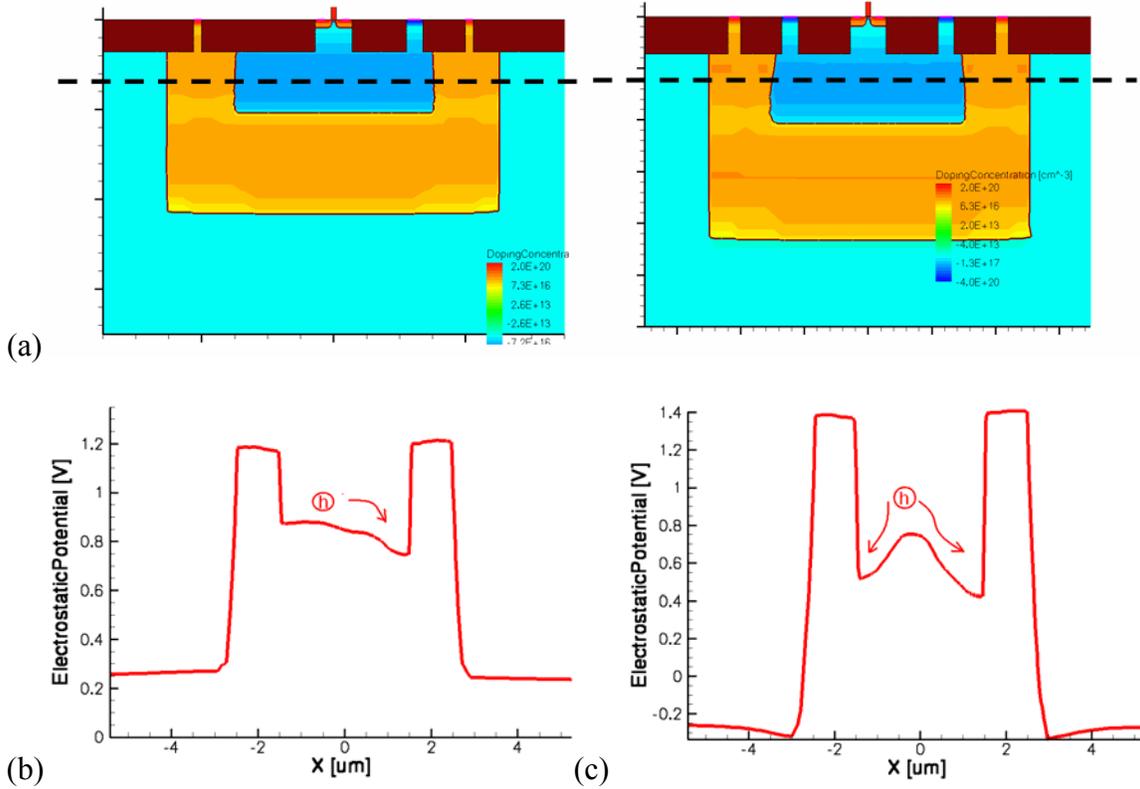


Fig. 38. (a) Cross section of two triple-well structures, one with a smaller p-well contact and the other with a larger p-well contact. Electrostatic potential along black dotted line for structure with (b) smaller contact, (c) larger contact 100 ps after an ion strike with $LET = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

6.1.2 N-well contact size

In the next set of simulations the n-well contact area for the triple-well structure is varied, keeping the size of the p-well contact the same. Fig. 39 shows the current and voltage pulses at the drain of the NMOS device when struck with a particle having $LET = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. In one case, the n-well contact has an area of $1.44 \text{ }\mu\text{m}^2$, while in the other the area is $3 \text{ }\mu\text{m}^2$, roughly twice the area of the smaller contact. The pulse width

decreases by $\sim 10\%$ when the contact size is doubled. This shows the width of the upset pulse depends only slightly on the n-well contact size. The charge collected for the large contact case is 1 fC, while that for the smaller contact is ~ 0.9 fC. A 10% decrease in charge collection is observed when using a larger n-well contact.

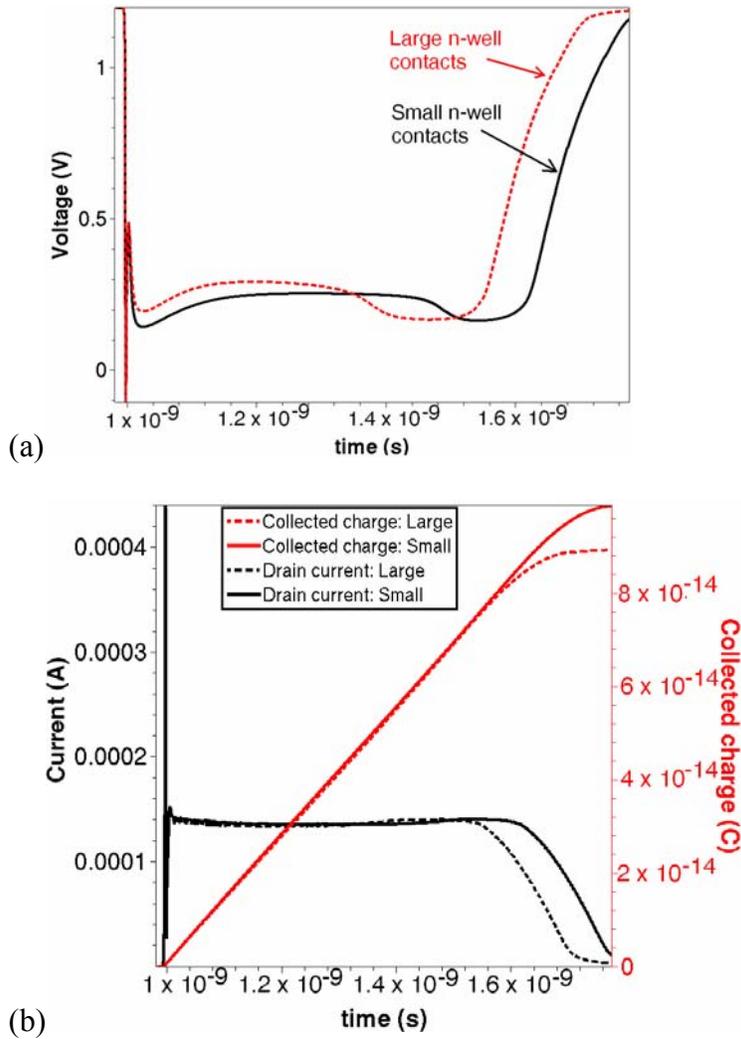


Fig. 39. (a) Voltage, (b) Current and collected charge vs. time at triple-well NMOSFET drains with small and large n-well contacts.

To analyze the variations caused by varying n-well contact size, the electrostatic potential at the p-well contact and n-well contacts for the two contacting schemes are plotted in Fig. 40. When the n-well contact has a larger area, the potential drop across the n+-n region is smaller, as was the case with the p-well contacts in 6.1.1. Now, the path connecting the n-well contact to the p-well contact is considered. The terminals are all pinned to fixed potentials, so whatever drop occurs across one junction is mirrored at the other. For a larger drop across the n+-n contact, the p+-p contact should have a lower drop so that the net drop remains at 1.2 V. So, for the larger contact, there is a smaller potential drop across the n+-n region, which causes a higher potential difference across the p+-p region, thus causing a higher rise of the p-well potential.

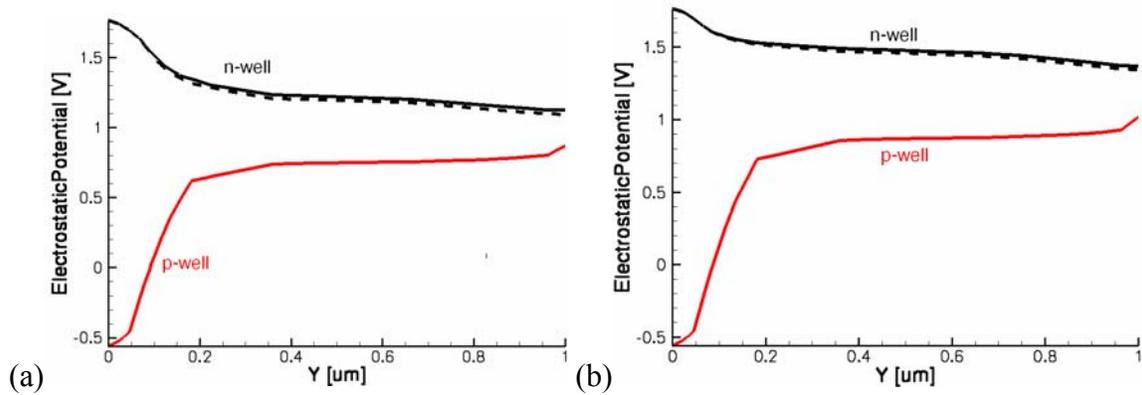


Fig. 40. Electrostatic potentials along a vertical cutline through the n-well contacts and the p-well contact for (a) small n-well contacts (b) large n-well contacts. Note: There are two n-well contacts, one shown by a black solid line, the other shown by a black dashed line. The plots are obtained 100 ps after the strike.

Now, when the p-well reaches a higher potential for a larger n-well contact, the forward bias on the source – p-well junction is greater, causing higher injection of electrons by the source. The stronger reverse bias on the p-well – n-well junction for

larger n-well contacts helps the electrons drift into the n-well, leading to larger n-well current. Fig. 41 shows the source and n-well currents for the two cases. However, it can also be noticed that the recovery of the currents occurs sooner for the case with large n-well contacts than for small contacts.

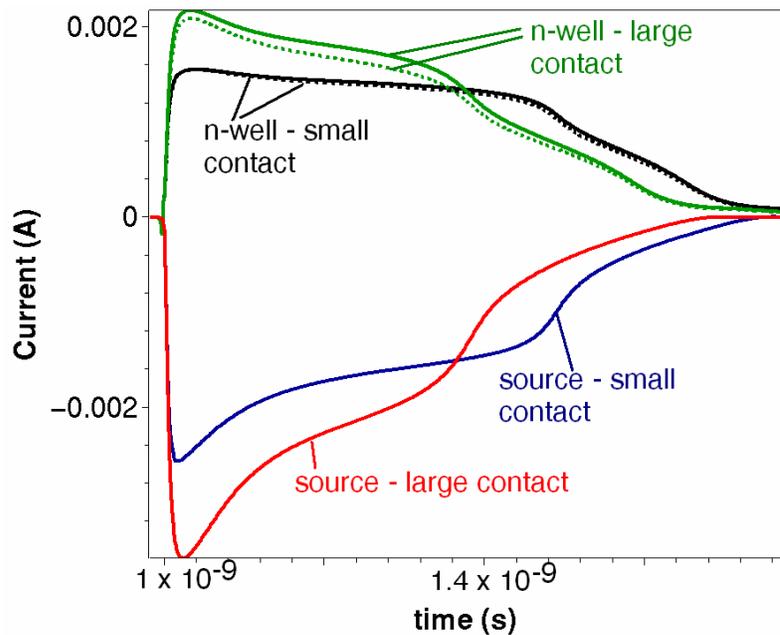


Fig. 41. Source and n-well currents for large and small n-well contacts

Figure 42 shows the potential along a horizontal cutline $0.5 \mu\text{m}$ under the surface of the substrate, for both large and small contacts. Due to a stronger reverse bias on the well junction, the potential hill of 6.1.1 (Fig. 38) is steeper for the large n-well contacts than for the small n-well contacts. This potential gradient aids in faster removal of majority carriers (holes) from the p-well.

Thus, the effect of the n-well contacts on upset voltage pulse width has two components. On one hand, the larger n-well contact causes the p-well potential to rise higher than when a smaller n-well contact is used. This increases source current injection.

However, the larger contact ensures stronger reverse bias on the n-well – p-well junction, which causes a steeper potential gradient along the horizontal plane of the p-well. This facilitates faster recovery of the system by increasing the hole current to the p-well contact. However, the effect of the n-well contact size on upset pulse width is relatively small.

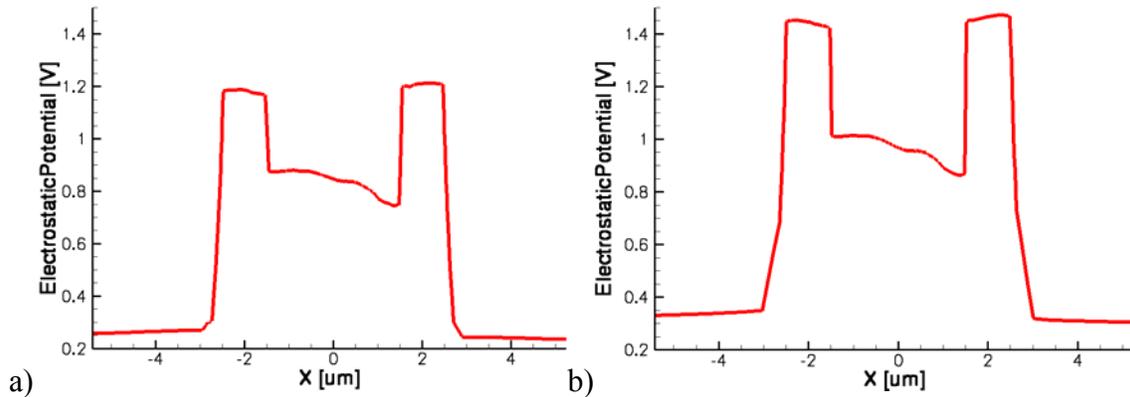


Fig. 42. Electrostatic potentials along a horizontal cutline running $0.5 \mu\text{m}$ below the surface for (a) small n-well contacts (b) large n-well contacts 100 ps after an ion strike with $\text{LET} = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

6.2 P-well contact depth

The alteration of contact sizes is the task of the layout designer. Using this technique may involve a considerable area penalty for obtaining a sizeable reduction in upset pulse width. In this section, a process design change is considered to reduce upset voltage pulse width, which does not involve any area penalty. To maximize the chance of formation of an ohmic contact between the contact metal and the semiconductor, the semiconductor contact region is highly doped near the surface. The standard depth for the highly doped region of the well contacts is typically the same as for the drain and source implantations, which for the 90 nm technology node is about 60 nm [13]. The depth of

this highly doped region is referred to as “contact depth” in the rest of the text. To examine the effect of this p+ contact doping, simulations are carried out by increasing the contact depth to 200 nm and 300 nm. Fig. 43 shows how the contact depths were altered. The peak doping of the contact is kept the same while the Gaussian profile is allowed to roll off at a different distance from the peak. Practically, the energy of the ion during the implantation process needs to be increased to increase the depth of the contact.

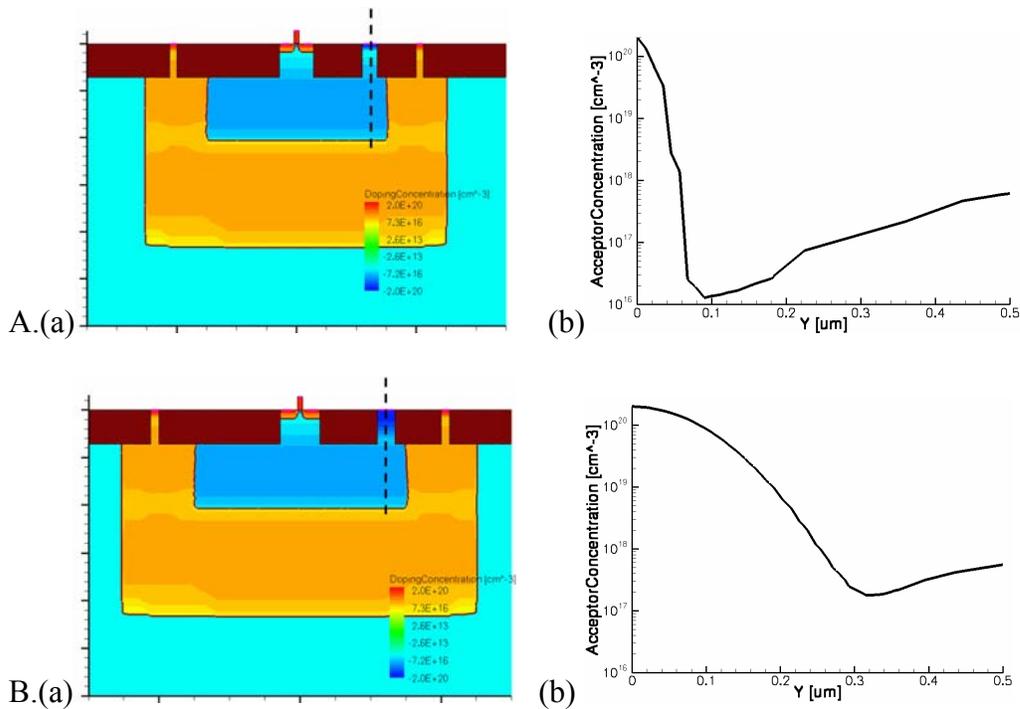


Fig. 43. A. (a) Cross-section of a triple-well device with p-well contact depth of 60 nm. (b) Acceptor dopant concentration along the dashed line in (a). B. (a) Cross-section of a triple-well device with p-well contact depth of 300 nm. (b) Acceptor dopant concentration along the dashed line in (a).

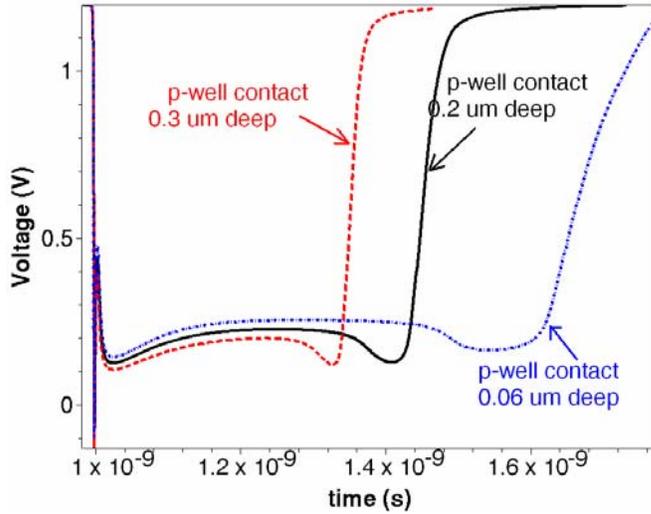


Fig. 44. Voltage vs. time at drain for different depths of p-well contact.

Figure 45 shows the electrostatic potential along a vertical cutline through the p-well contacts, one contact being 60 nm deep and the other 300 nm deep. The excess free carrier densities for the two kinds of contact are shown. For the deeper p-well contact, the p⁺-p junction occurs at a larger distance from the surface than for the shallower contact. The free hole density that exceeds the background acceptor density, $p-N_a$, which is essentially the injected hole density, is lower and is significant over a shorter distance for a deeper contact when compared with a smaller contact. Thus, using equation (5), the p⁺-p potential difference is much lower for the deeper contact as opposed to the shallow contact. This leads to a smaller rise in p-well potential for the structure with deeper p-well contacts.

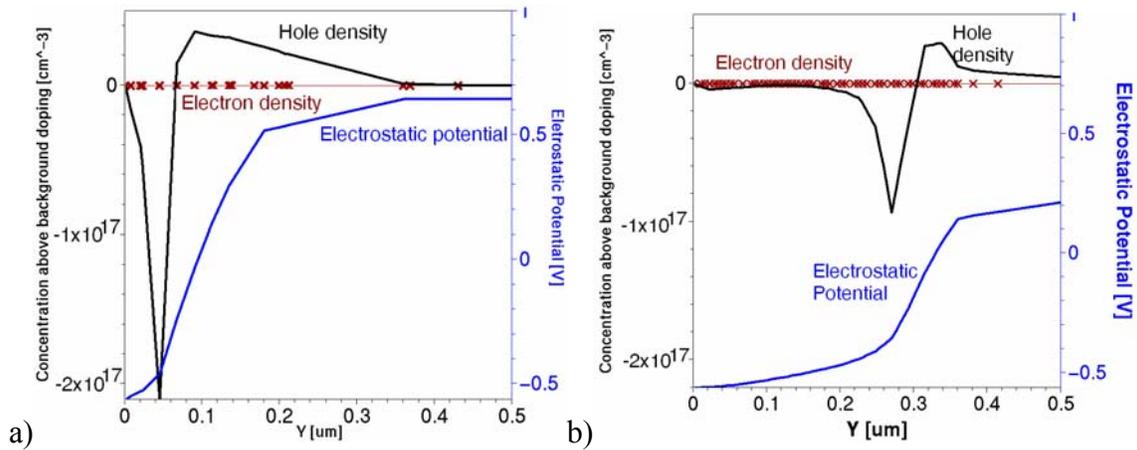


Fig. 45. $(p - N_a)$, $(n - N_d)$ and electrostatic potential at p-well contact for p-well contact a) 60 nm deep, b) 300 nm deep. Here, $p = p_0$ (number of carriers at equilibrium) + δp (injected carriers), and $n = n_0 + \delta n$.

The p-well potential is low when the contact doping is deep, resulting in reduced injection of source electrons into the p-well, as opposed to a shallow contact doping. The recovery of the upset occurs faster for the deep contact case, because of speedier hole removal from the p-well. Fig. 46 shows the electrostatic potential along a horizontal cutline in the p-well, 0.56 μm below the surface of the well. The potential hill sees a strong depression under the p-well contact when the contact is made deeper. This helps holes move along the well much faster than when the contact is shallow.

Thus, the greater the contact depth, the narrower the upset voltage pulse. It can be claimed that further deepening of the p-well contact will limit the potential of the well to a level that will not forward bias the source – p-well junction at all. This will bring the upset pulse to the same width as that of a dual-well NMOSFET.

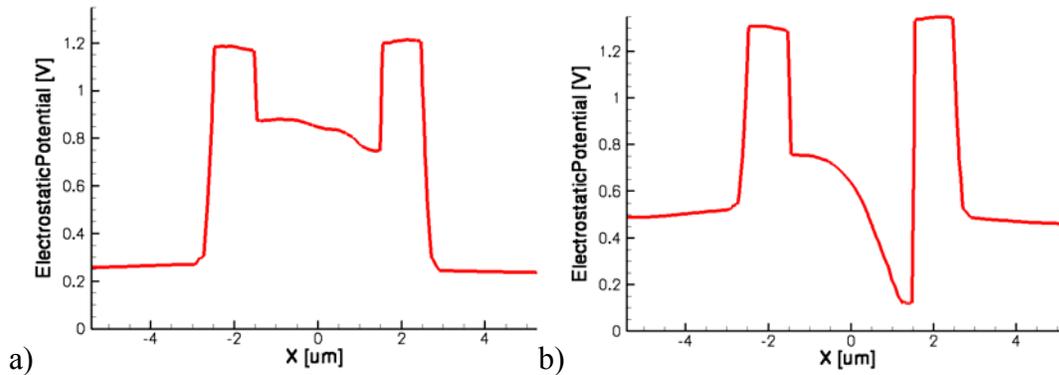


Fig. 46. Electrostatic potential along a horizontal cutline running $0.56 \mu\text{m}$ below the surface of the structure for p-well contact (a) 60 nm deep, (b) 300 nm deep 100 ps after an ion strike with $\text{LET} = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

The impact of the p^+ doping depth on the pulse width can be explained in another way. The deeper p^+ doping is more effective in draining out holes from the p-well by reducing the lightly doped region across which the hole has to diffuse to reach the contact. Also increasing the depth of the p^+ doping facilitates the movement of holes because of the admittance of the heavily doped region. The thickness of the heavily doped region and the thickness of the lightly doped region sum up to the thickness of the STI.

6.3 P-well contact placement

The layout designer can alter the placement of well contacts to alter the upset voltage pulse widths. According to the argument put forth in 6.1.1, the p-well contact induces a depression in the potential hill along the p-well. The location of the contact simply alters the location of the depression, thus changing the potential gradient along the well. In this section several simulations with different p-well contact locations are discussed, one with p-well contact $0.25 \mu\text{m}$ away from the struck location, another with a

contact 1 μm away from the struck location. The drain voltage is shown as a function of time in Fig. 47. No significant difference in pulse width is observed. This is because the p-well is 3 μm wide. The limited extent of the inner p-well does not allow the potential gradient to change much with the distance of the contact from the struck region. However, it can be observed that the closer the p-well contact is to the struck region, the shorter is the upset pulse width. Thus, placing contacts frequently assures speedy removal of carriers deposited by an ion strike, and reduces upset voltage pulse width. However, the application of this practice is limited by the area penalty.

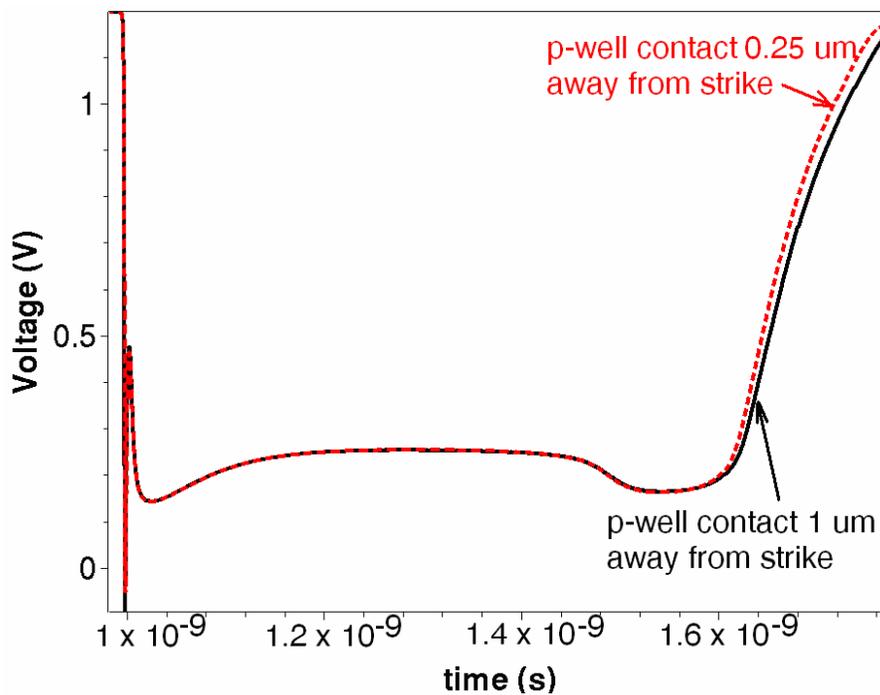


Fig 47. Drain voltage vs. time for different contact placement schemes.

6.4 P-well – n-well junction depth

Another factor that affects carrier and potential profiles is the distance of the deep n-well boundary from the p-well contact and the NMOS source. To study the effect of the

n-well – p-well junction depth on the upset pulse width, the p-well was made 1 μm deep in one case, and 2 μm deep in the other. The drain voltage pulses for the two cases are shown in Fig. 48.

There are two major observations to be made from Fig. 48. Initially the pulse seems to be narrower for the deeper p-well than for the shallow p-well. Around 0.7 ns after the strike, the rate of recovery changes for the two cases. The deeper p-well resembles a dual-well system, because the influence of the well junctions is removed to some extent. So, the electron injection by the source is lower when the p-well is 2 μm deep than when the p-well is just 1 μm deep. In a dual-well case, as was seen in Section 3.3, the recovery of the system is slow, because there are residual charges in the wells. Similarly, for a deeper p-well, the recovery occurs slower in comparison to a shallower p-well.

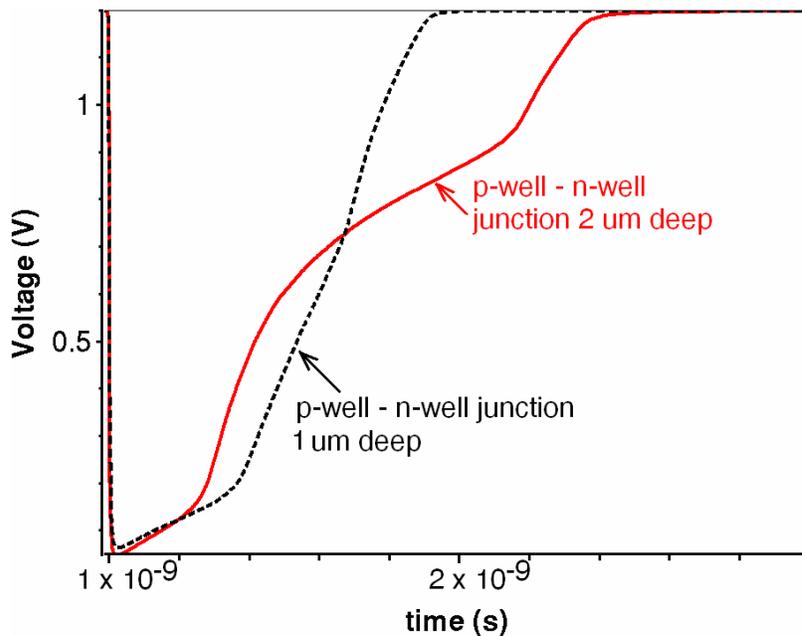


Fig. 48. Voltage vs. time at drain for varying p-well – n-well junction depths.

6.5 Variation in operating conditions – p-well bias voltage

When the bias on the p-well is changed from 0 V to -1 V, the pulse width decreases, as seen in Fig. 49. Changing the p-well bias to -1 V causes a stronger reverse bias on the p-well – n-well junction than when the p-well bias is at 0 V. More electrons can drift into the n-well, leaving more holes to accumulate in the p-well. This causes the p-well potential to rise higher than when the well is biased at 0 V. Fig. 50 (a) shows the potentials along cutlines taken through the drain, source and p-well contact. It is seen that the source – p-well barrier is reduced by the high potential of the p-well. The potential difference between the p+ and p region of the well contact is approximately 2 V. Fig. 50 (b) shows the hole and electron densities along a cutline through the p-well contact. The p+-p potential difference is accounted for by the high hole density in the p-region of the contact.

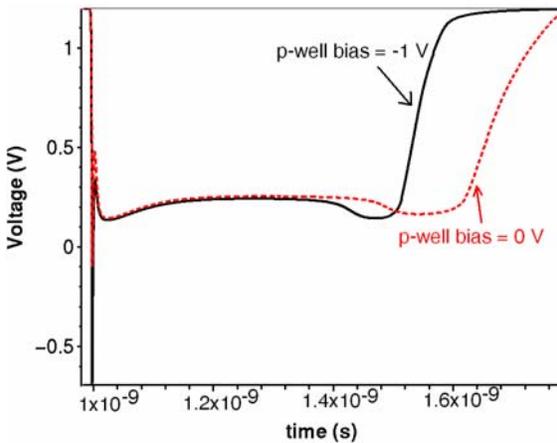


Fig. 49. Drain voltage vs. time for p-well bias of 0 V and -1 V.

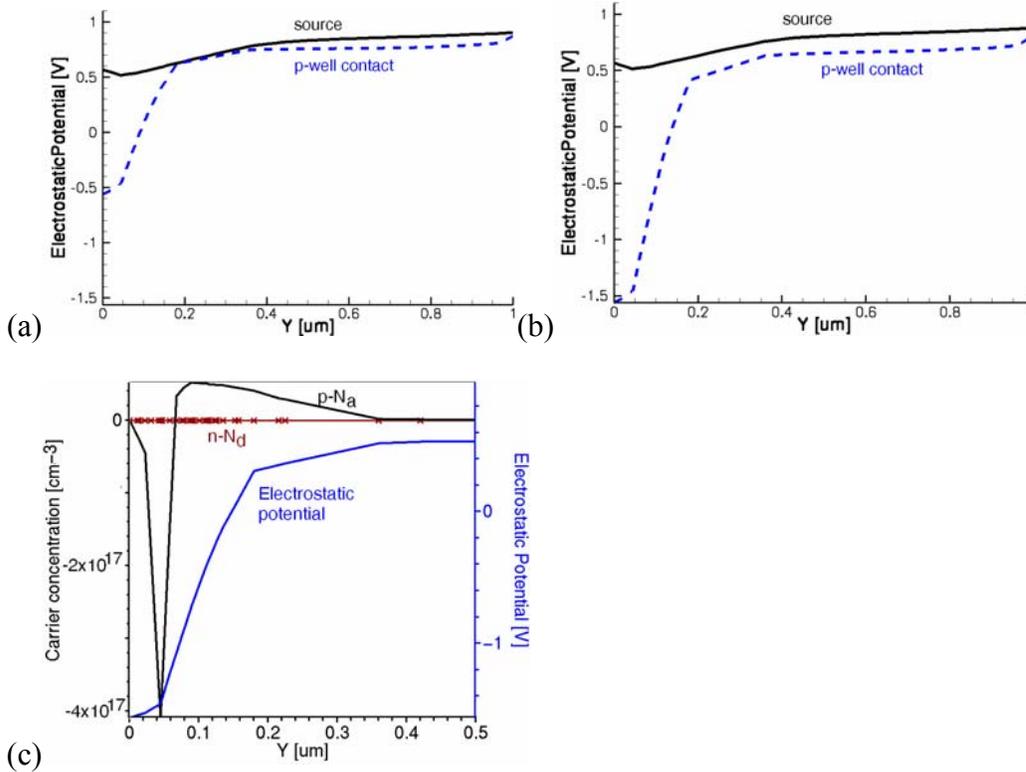


Fig. 50. Electrostatic potential along vertical cutlines through source and p-well contact for p-well biased at (a) 0 V and (b) -1 V. (c) $(p - N_a)$, $(n - N_d)$ and electrostatic potential at p-well contact for p-well biased at -1 V. $p = p_0$ (number of carriers at equilibrium) + δp (injected carriers), and $n = n_0 + \delta n$.

6.6 Summary

The effects of well contact area, depth, placement and well junction depth have been studied. For a faster recovery of the system, it is necessary to allow faster removal of holes from the p-well. A larger contact area is useful for that purpose. However, this can come with severe area penalty. Placing the p-well contact close to the struck region may also expedite hole removal from the p-well. However, it is not always possible to have a p-well contact in proximity to the device.

A simple way of reducing the source injection is by deepening the p-well contact. However, since this usually is the same implant as the source/drain of a p-channel

MOSFET, it may not be possible in typical processes without adding fabrication steps. This does not impose an area penalty to the layout, nor does it affect the NMOS device performance in equilibrium conditions, since it can be produced by using a higher energy and dose implantation. Using higher doping at the contact decreases the number of holes exceeding the acceptor concentration. This causes a lower potential gradient in the p+-p region. Since it might not be feasible to exceed the contact doping beyond $2 \times 10^{20} \text{ cm}^{-3}$, just increasing the depth of the implant is recommended for controlling the upset voltage pulse width.

CHAPTER VII

CIRCUIT AND LAYOUT EFFECTS IN TRIPLE-WELL NMOSFET

The previous chapters discuss the physical mechanisms responsible for charge collection in triple-well NMOSFETs. In this chapter, circuit and layout effects in triple-well NMOSFETs are described. The mechanisms of charge collection are incorporated in a compact model of a triple-well NMOSFET during a single event. The effect of having multiple NMOSFETs in the same p-well is discussed next.

7.1 Compact model of triple-well NMOSFET

The physical mechanisms of charge collection in triple-well devices have been described in the previous chapters. This information is utilized in this chapter to make a compact model of a triple-well NMOS device when the drain of the device is struck with an ion. Fig. 51 (a) shows the compact model.

The p-well – source junction is represented with a p-n diode, which can become forward biased when the p-well potential rises. The space charge region of the p⁺ - p region at the contact is represented by a capacitor C_p . The electrons injected by the source flow into the n-well, emulating an npn bipolar transistor operating in the active mode. This is represented by the BJT Q. The resistances are representative of the change in potential with the current through the various locations in the semiconductor. The resistances are a function of time. Fig. 51 (b) shows the electron density in a triple well

10 ps after an ion strike having LET = 40 MeV-cm²/mg. The carrier concentrations change with time. Hence, the impedances shown in the compact model vary with time.

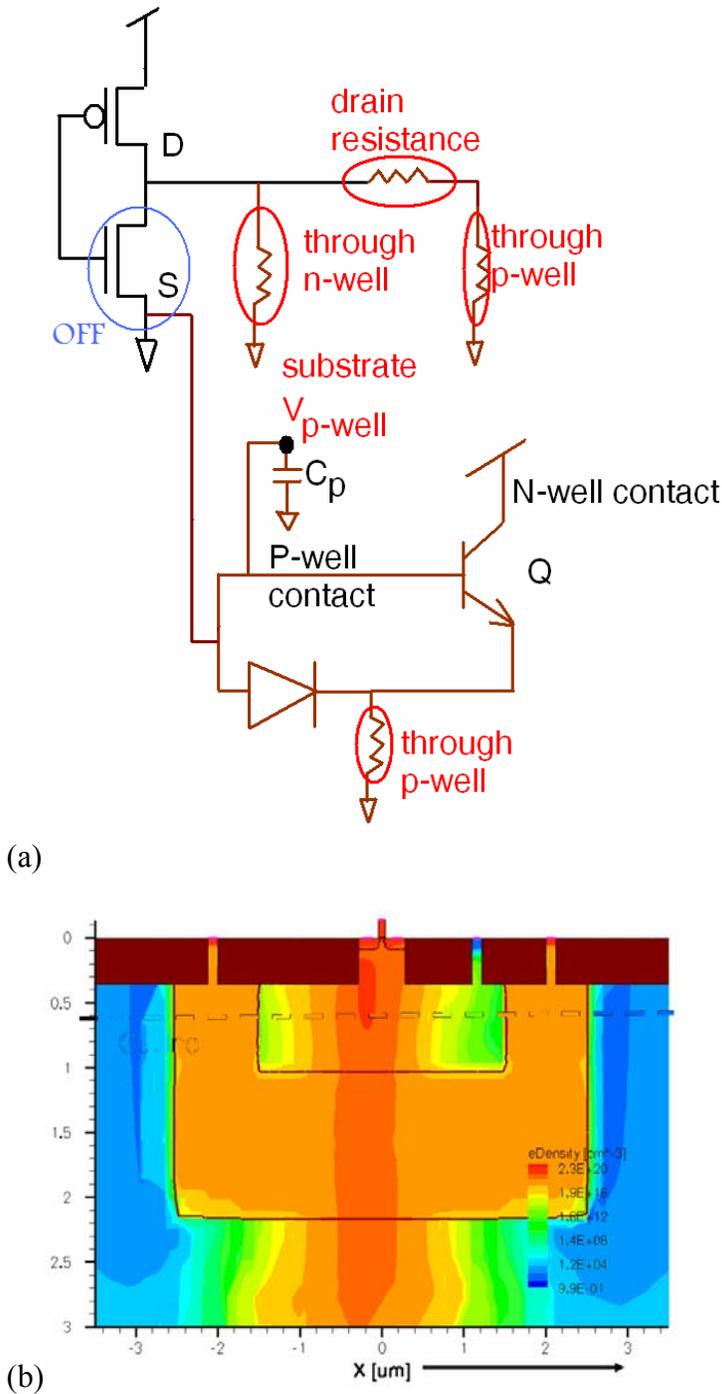


Fig. 51. (a) Compact model of a triple-well NMOS device. (b) Electron density in triple well 10 ps after strike.

7.2 Multiple NMOS devices in the same p-well

Realizing an integrated circuit typically involves building multiple transistors in the same well. A strike on one device might upset another device because of the potential redistribution all through the well. This section describes the circuit effects associated with having more than one device in the same p-well in a triple well system. For simplicity, two NMOS transistors are considered in the p-well of a triple well system. A similar arrangement is made for a dual-well system for comparison. Fig. 52 shows the simulation setup.

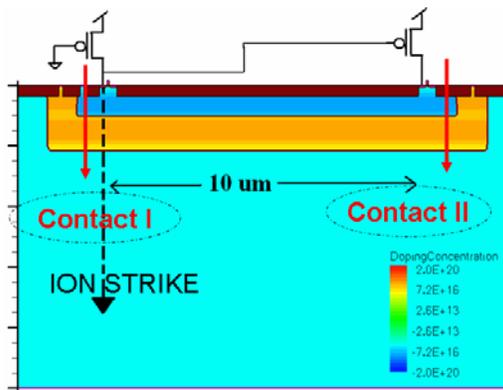


Fig. 52. Triple well structure consisting of two NMOS devices in the same p-well. A two-inverter chain is formed. The p-well contact location is varied – once kept close to the struck device and next kept close to the second device.

In Fig. 52, a two-inverter chain is shown with the devices in the same p-well. The drain of the left-most NMOSFET is struck with an ion of LET $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The effect of contact placement is studied by means of 2-D simulations. In the first case, the p-well contact is placed $1 \mu\text{m}$ to the left of the hit node, while in the second case, the p-well contact is $11 \mu\text{m}$ away on the right side of the well (Contact I and Contact II in Fig 52). The drain of the left device is biased high and the drain of the right device low prior

to the strike, so the drain of the first NMOSFET (left side of the well) goes low during the strike and the second NMOSFET (right side of the well) drain goes high.

It is helpful to examine the equivalent dual-well system before analyzing the triple-well results. Fig. 53 shows potentials in dual-well systems with p-well contact close to the strike and far from the strike. In the first case, the p-well contact is $\sim 1 \mu\text{m}$ away from the strike location. In the second case, the p-well contact is $5 \mu\text{m}$ away from the strike and is in between the two NMOSFETs. In the third case, the p-well contact is $11 \mu\text{m}$ away from the strike and close to the second NMOSFET that is not struck by the ion. The p-well contact of the dual well holds the potential of the region around it near 0 V. In all three contacting schemes, there is negligible potential gradient along the body of the well. Due to the strike, the region around the first NMOSFET is affected. The potential of the p-well rises slightly because of the holes deposited in the p-well. However, the rise is not high enough to cause a significant potential gradient between the affected and unaffected parts of the large p-well. The potential of the unaffected part of the p-well remains close to the equilibrium value.

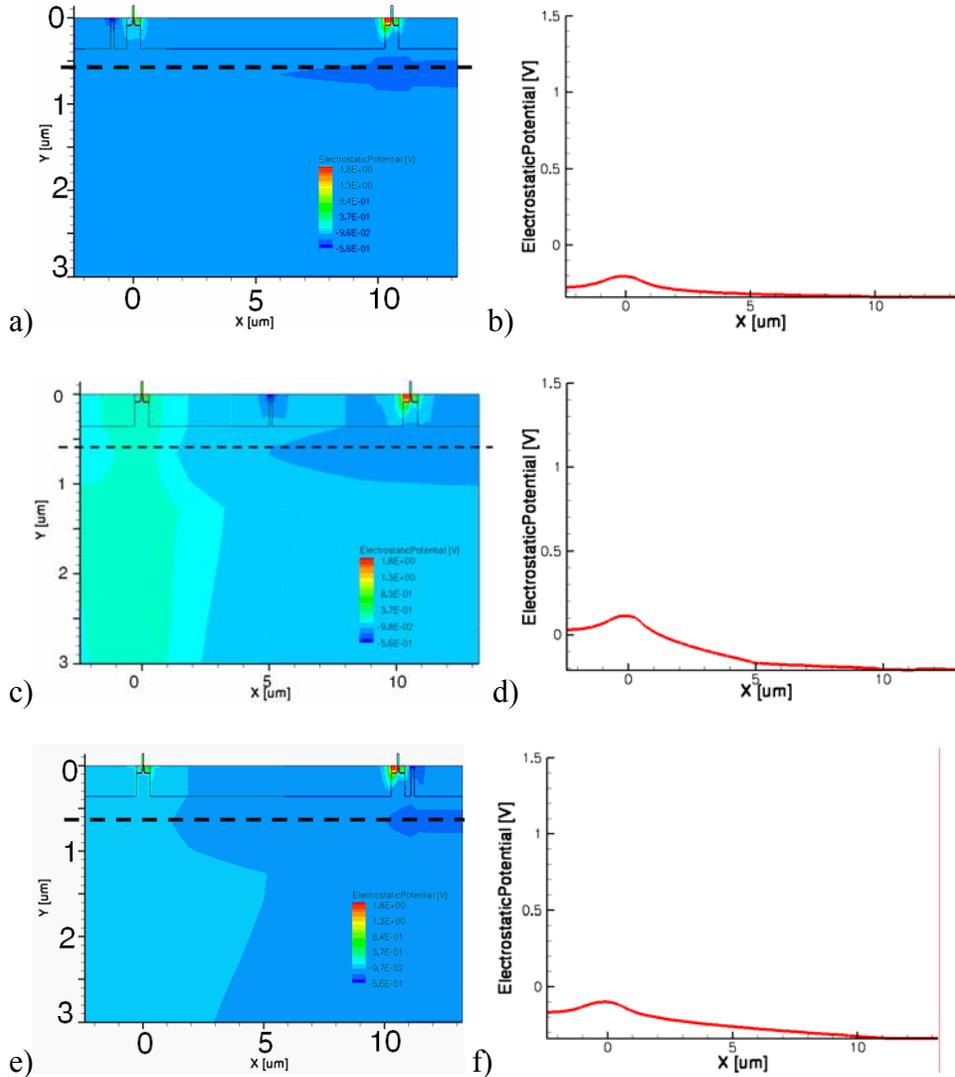


Fig. 53. Cross sections of dual-well systems having two NMOS devices, with p-well contact placed a) close to strike, c) 5 μm away from strike, e) 11 μm away from strike. b) Electrostatic potential along the dashed line in (a). d) Electrostatic potential along the dashed line in (c). f) Electrostatic potential along the dashed line in (e). These occur 50 ps after an ion strike of $\text{LET} = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

In contrast, the gradient of potential along the p-well in a triple-well structure is much higher than for the dual-well structure, but appears to be relatively independent of contact position. Fig. 54 shows the electrostatic potential along a horizontal cutline through the triple well structure for the three contact placements. In the triple-well case,

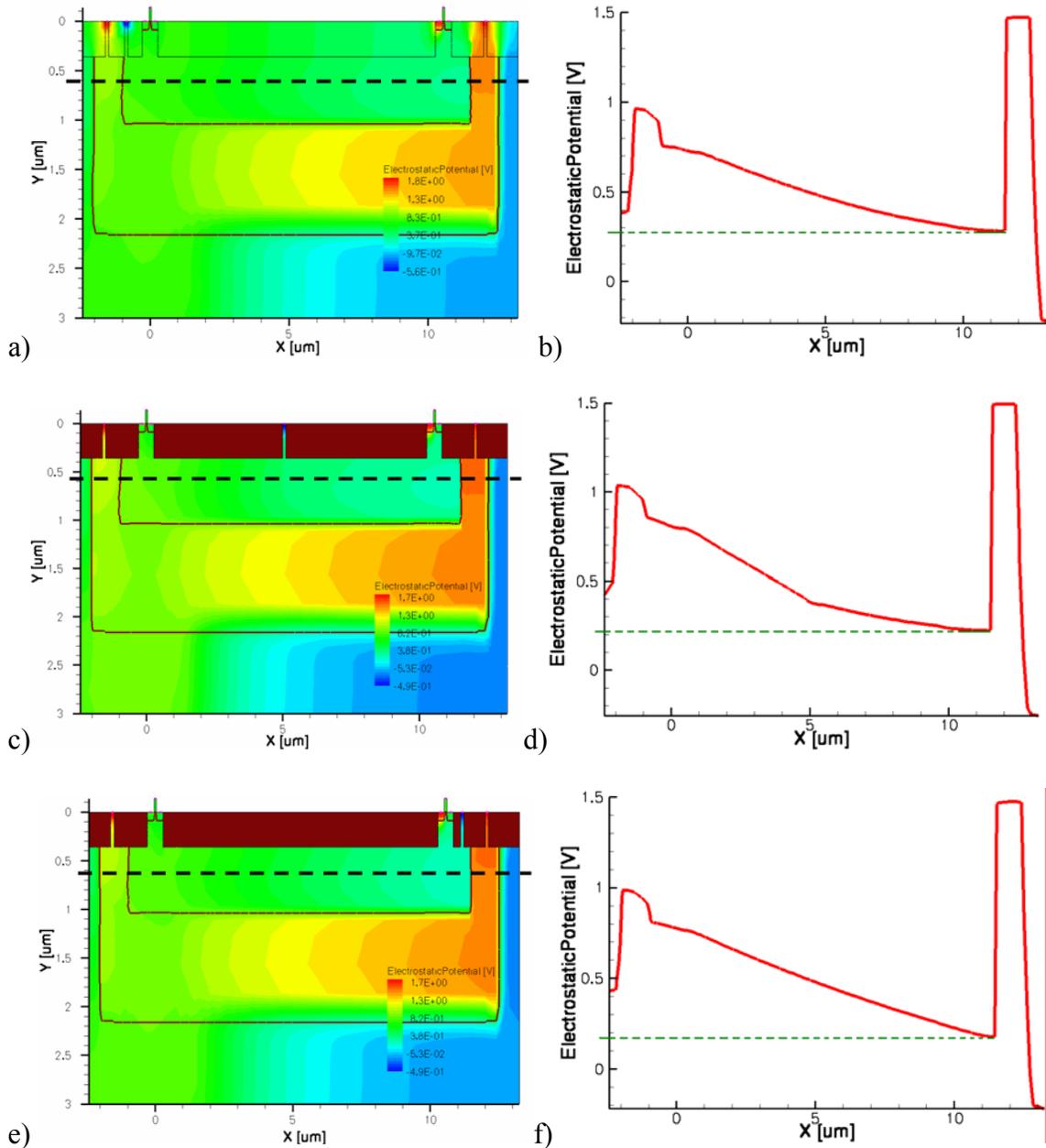


Fig. 54. Cross sections of dual-well systems having two NMOS devices, with p-well contact placed a) close to strike, c) 5 μm away from strike, e) 11 μm away from strike. b) Electrostatic potential along the dashed line in (a). d) Electrostatic potential along the dashed line in (c). f) Electrostatic potential along the dashed line in (e). These occur at 100 ps after an ion strike with $\text{LET} = 40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

the accumulation of holes in the p-well causes a rise in the p-well potential all through the well, though not uniformly. There is a significant monotonic potential gradient along the

body of the p-well, unlike the dual-well case. This implies that there is a finite electric field along the body of the well which assists in the movement of carriers along the well. The evidence of this was already shown in Chapter VI, Section 6.1.1, 6.1.2 and 6.2.

In the triple-well case, the potential of the p-well rises due to the accumulation of holes. The rise of potential all along the well is not uniform. The region around the struck device is more affected than the region around the second NMOSFET which is $11\ \mu\text{m}$ away from the first NMOSFET. This differential rise in potential along the body of the p-well causes a significant potential gradient for the triple-well case.

The ion strike is asymmetric with respect to the structure. This causes unequal potential drops at the two n-well contacts. There is a higher potential difference for the n-well contact close to the strike than for the n-well contact far from the strike. Fig. 55 shows this effect. The potential along a vertical cutline through the n-well contacts is shown here. There is a potential drop of 0.3 V at the n-well contact located further away from the strike. The potential drop at the n-well contact close to the strike is $\sim 1\ \text{V}$. This causes each side of the n-well to have a different potential, both side n-well contacts being tied to 1.2 V. This difference is compensated by a potential gradient along the p-well body. The potential gradient observed for a small p-well, as was discussed in the earlier chapters, is not as pronounced as in the case of the large p-well here. For a small p-well, the strike location is quite symmetric compared to the two side n-wells, resulting in almost equal potentials of the two sides.

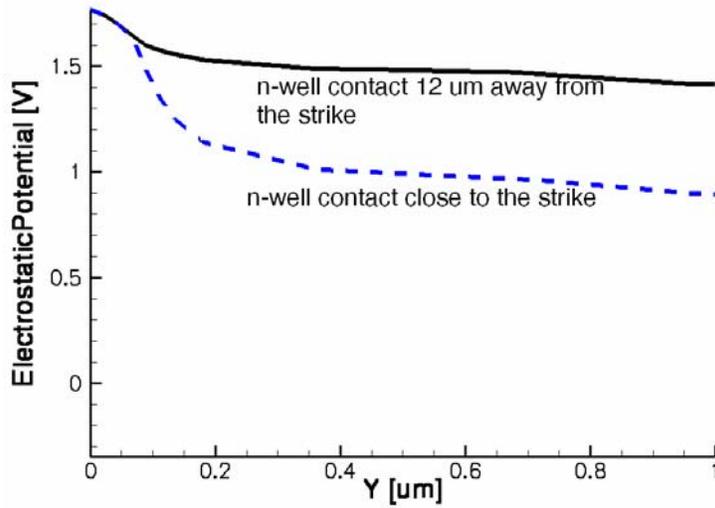


Fig. 55. Electrostatic potential along vertical cutlines through the two n-well contacts in a triple-well system.

An identical effect is seen when a single NMOSFET is simulated in a long p-well described above. Fig. 56 shows the electrostatic potential of the triple-well structure with a single NMOSFET. The potential gradient along a horizontal cutline through the p-well is seen here, as well. This proves that the potential gradient is not related to the second NMOSFET located at the other end of the p-well.

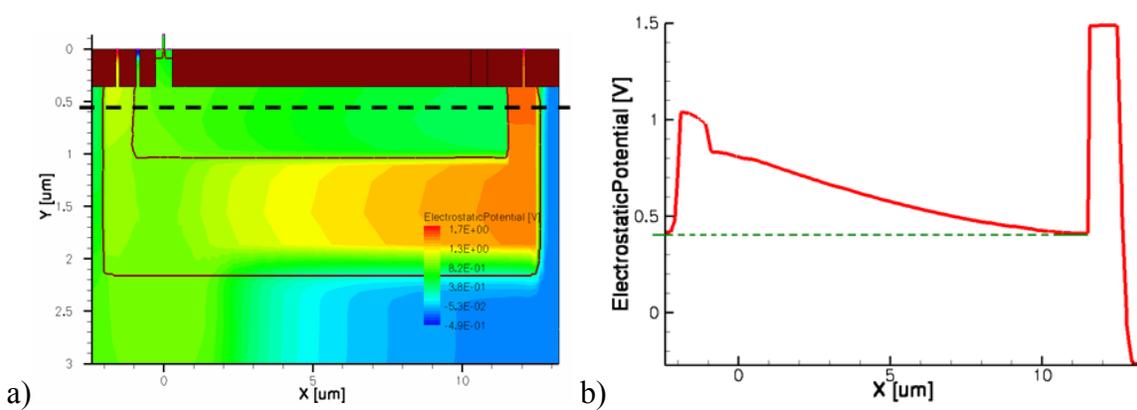


Fig. 56. a) Cross section of a triple-well NMOSFET in a long p-well. b) Electrostatic potential along the black dashed line in (a).

7.3 Summary

A circuit model for simulating the single event response of a triple-well NMOSFET is proposed in this chapter. The model needs further verification, and the components of the model need to be characterized. A circuit level effect of shortening of pulse width is observed when a two-inverter chain is formed, the input of the first inverter being low. The cause of this has been explained. When an ion strikes one end of a large p-well, the other end remains relatively unaffected by the strike. This causes a potential gradient between the two regions. The potential gradient along the body of the p-well in a triple well is more pronounced than the gradient in a dual well.

CONCLUSION

Investigation of single event mechanisms in 90 nm triple-well NMOS devices indicates that triple-well devices may collect more charge compared to dual-well devices because the source in triple-well NMOS devices injects electrons into the p-well. The n-well of a triple well collects electrons, which results in accumulation of holes in the p-well. The p-well potential rises and this forward biases the source – p-well junction. Electrons are injected by the source into the p-well across the forward-biased source – p-well junction, leading to a higher charge collection by the drain of a triple-well NMOSFET as compared to a dual-well NMOSFET. Electrons get injected into the p-well as long as the p-well potential remains high enough to forward bias the source – p-well junction. Thus, the key to the recovery of the system lies in the removal of holes from the p-well through the p-well contact.

Charge collection on the NMOS drain node can be reduced by increasing the well contact areas. Also, the p-well contacts might be placed closer to the struck region to remove charge more effectively. Frequently placed and large well contacts can help reduce charge collection in a large p-well. In a small p-well whose length is less than the diffusion length of holes, placement of p-well contact does not affect the single event pulse width significantly. Additionally, the p-well – n-well junction could be made deeper. An effective way to reduce charge collection is by deepening the p-well contact. This lowers the p-well potential, and reduces electron injection by source.

Effects of p-well de-bias on circuits is shown considering a chain of two inverters. In a large p-well, the parts of the p-well which are further away from the struck location

remain comparatively less affected by the strike. Thus, a potential gradient develops along the body of the p-well in a triple-well system where holes are confined in the p-well. The potential gradient is not as pronounced in a dual well as in a triple well because charges are not confined in a dual well.

The case of the triple-well NMOSFET is no different than that of a dual-well NMOSFET. Single event mechanisms in both dual-well and triple-well technology are similar. The presence of a large p-n junction as the p-well – n-well junction makes the potential redistributions in the dual-well case more pronounced than in its triple-well counterpart.

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APPENDIX I

FACTORS RESPONSIBLE FOR THE DRAIN POTENTIAL

The drain voltage of an NMOS during a strike depends on many factors. The drain voltage of the NMOSFET is at 1.2 V (V_{DD}) under normal operation of the inverter. (An inverter with the gate voltage at 0 V has been simulated throughout this document.) During the single event, the drain of the NMOSFET goes low. The drain potential is not fixed. The total drain current is fixed by the PMOSFET's drain current. How the drain voltage is determined during the single event is shown in this section. Fig. 57 shows an NMOSFET in a p-well. The drain, source and p-well contact are shown in the p-well. The source and the p-well contact are both fixed to 0 V. The drain of the NMOSFET is connected to the drain of the PMOSFET.

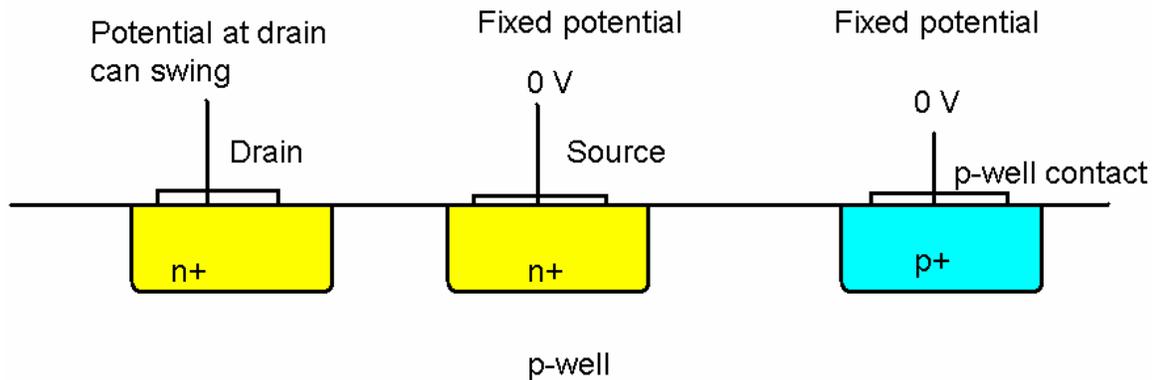


Fig. 57. NMOSFET in p-well. The bias voltages are shown here.

Three cases are analyzed numerically. First, a dual well in equilibrium is considered. This is identical to a triple well in equilibrium. Then, a dual well during a single event is considered followed by a triple well during the single event. An ion strike

having $LET = 40 \text{ MeV-cm}^2/\text{mg}$ is considered. The electrostatic potentials at various regions in the dual- and triple-well structure are noted.

Case I. Dual well in equilibrium

The electrostatic potentials at various regions in the dual-well structure are shown in Fig. 58. The source and the p-well contact are fixed to 0 V. The drain of the NMOSFET is at 1.2 V. There is a potential difference between the p+ and p regions of the p-well contact due to the difference in doping in the two regions. This potential difference is approximately 0.2 V. The p-well contact potential is -0.56 V. So, the p-well potential is approximately -0.3 V. The source contact potential is 0.56 V. There is a slight potential difference across the entire n+ diffusion of the source because of the doping gradient. Accounting for that difference, the potential difference between the n+ source and the p-well is approximately 0.8 V. Thus, the potential difference is approximately the built-in potential between the n and p regions. Similarly, the potential difference across the n+ drain and the p-well is approximately 1.8 V, because the drain is at a potential of 1.2 V.

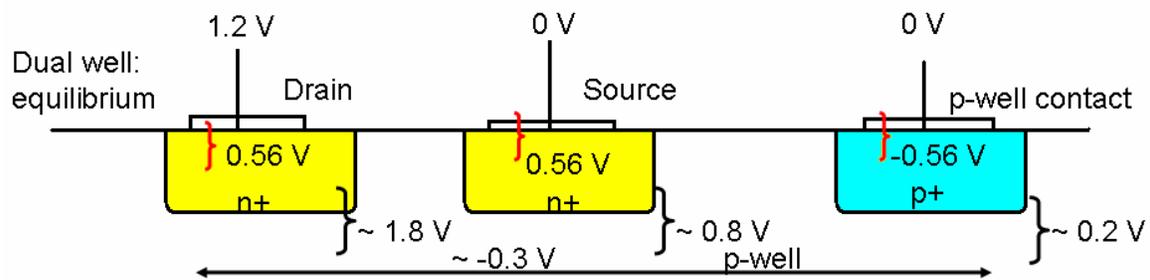


Fig. 58. Electrostatic potentials in dual well at equilibrium. The numerical values denote the potential difference between the top and the bottom of the curly brackets.

Case II. Dual well during strike

In a dual well, when a strike deposits carriers of both types, the p-well potential rises slightly. The p-well already has some holes at equilibrium. Thus, after the strike, the p-well has slightly more holes than electrons which causes a net rise in p-well potential. The p-well potential is approximately -0.1 V , which is higher than its equilibrium value. The rise in p-well potential is manifested as a potential difference of $\sim 0.4\text{ V}$ between the p and p+ regions at the well contact. At the source which is n-type, the rise in p-well potential lowers the source – p-well potential difference. But, source – p-well junction is not forward biased yet. The n-type drain is current-limited and not voltage-limited. The potential at the drain terminal goes down from the equilibrium value of 1.2 V . Since there is no fixed potential at the drain, the drain – p-well depletion region gets obliterated by the large number of charged carriers deposited by the ion strike. There is only a 0.1 V of potential difference across the junction. The drain ohmic contact accommodates a potential difference of 0.56 V between the metal and the n-type semiconductor. So, the drain metal sees a potential of $(\sim 0\text{ V} - 0.56\text{ V}) \approx -0.56\text{ V}$. This calculation explains why the drain voltage goes below the rail for a dual-well NMOSFET.

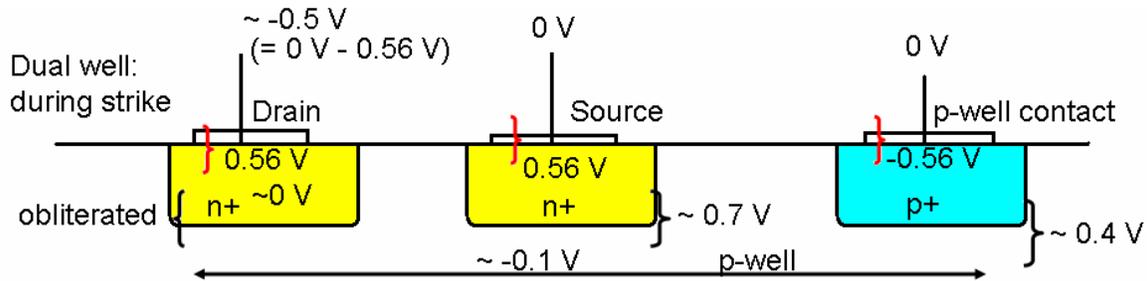


Fig. 59. Electrostatic potentials in dual well 50 ps after strike. The numerical values denote the potential difference between the top and the bottom of the curly brackets.

Case III. Triple well during strike

In a triple well, the holes deposited by the ion strike accumulate in the p-well. This causes a rise in p-well potential. The p-well potential rises to ~ 0.8 V, around 1.1 V above its equilibrium value. The rise in potential is manifested by a huge potential difference between the p and p+ regions of the p-well contact. At the n-type source, the barrier between the source and the p-well reduces to the extent of forward biasing the source – p-well junction. The n-type drain is not pinned to a constant potential. Thus, the rise in potential is reflected at the drain terminal. Allowing only a hundred millivolt across the obliterated drain – p-well junction, the drain terminal sees the potential of the p-well after the contact potential between the metal and the n-type semiconductor is subtracted from it. So, the drain potential is $(0.9 \text{ V} - 0.56 \text{ V}) \approx 0.4 \text{ V}$. Thus, the drain voltage of a triple-well NMOSFET remains above the rail during the single event.

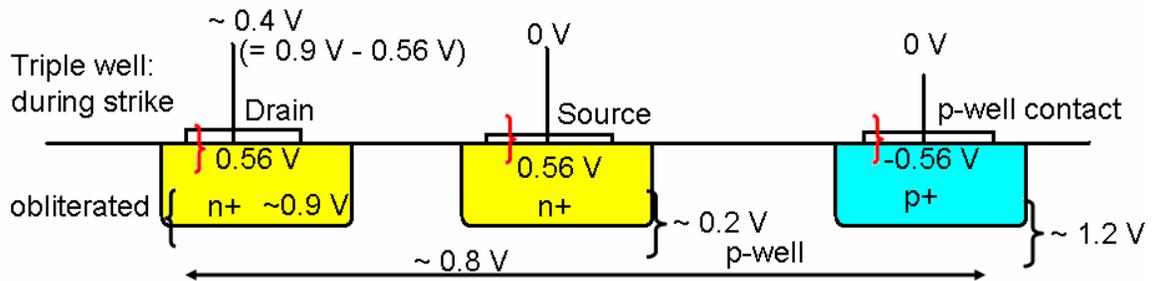


Fig. 60. Electrostatic potentials in triple well 50 ps after strike. The numerical values denote the potential difference between the top and the bottom of the curly brackets.

APPENDIX II

SDEVICE SCRIPT

Triple well SDevice script for HeavyIon simulation

```
Device NMOS {  
  
  Electrode {  
    { Name="source_nmos" Voltage=0 }  
    { Name="drain_nmos" Voltage=0 }  
    { Name="gate" Voltage=0 }  
    { Name="pwell" Voltage=0 }  
    { Name="substrate" Voltage=0 }  
    { Name="nwell" Voltage=1.2 }  
    { Name="nwell2" Voltage=1.2 }  
  
  }  
  
  File {  
    # input files:  
    Grid = "show_msh.grd"  
    Doping = "show_msh.dat"  
    Param = "dessis.par"  
    # Load = "showlargebias_des.sav"  
  
  }  
  
  Physics {  
    Mobility( PhuMob ( Arsenic ) HighFieldsat Enormal )  
    Fermi  
    EffectiveIntrinsicDensity( OldSlotboom )  
    Recombination ( SRH Auger )  
    HeavyIon (   
      PicoCoulomb  
      Direction=(0,1,0)  
      Location=(-0.18,0,0.1)  
      Length=7  
      Time=1e-9  
      LET_f=0.4  
      wt_hi=0.05  
      Gaussian  
    )  
  
  }  
}  
  
File {  
  Plot="showlet40.dat"  
  Current="showlet40.plt"  
  SPICEPath = "."  
  
}  
  
System {
```

```
NMOS nmos ("pwell"=0 "gate"=n1 "drain_nmos"=n2 "source_nmos"=0 "nwell"=n3 "nwell2"=n3
"substrate"=0)
```

```

                                rvt_pfet                                MP1 (n2 n1
n4 n4)
                                {w = 0.480e-6
                                pd = 1.440e-6
                                ad = 11.52e-14
                                l = 0.08e-6
                                ps = 1.440e-6
                                as = 11.52e-14
                                nrd = 0.01 nrs = 0.01
                                }

```

```
Vsource_pset v1 (n3 0) {dc = 1.2}
Vsource_pset v2 (n4 0) {dc = 1.2}
Vsource_pset v3 (n1 0) {dc = 0}
}
```

```
Plot {
eDensity hDensity eCurrent hCurrent
Potential SpaceCharge ElectricField
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
ConductionBandEnergy ValenceBandEnergy
AugerRecombination
HeavyIonChargeDensity
eQuasiFermiPotential
hQuasiFermiPotential
}
```

```
Math {
NoAutomaticCircuitContact
WallClock
Extrapolate
Derivatives
Newdiscretization
RecBoxIntegr
Method=ILS
RelErrControl
Spice_gmin=1e-15
Iterations=20
notdamped=100
}
```

```
# Initial Solution build-up
```

```
Solve {
Coupled (Iterations=100) {Poisson}
Coupled (Iterations=100) {Poisson Circuit}
Coupled (Iterations=100) {Poisson Contact Circuit}
Coupled (Iterations=100) {Poisson Hole Contact Circuit}
Coupled (Iterations=100) {Poisson Hole Electron Contact Circuit}
}
```

```
NewCurrentFile="showlet40"
```

```
Transient (  
  InitialTime=0 FinalTime=0.95e-9 InitialStep=1e-11 MaxStep=1e-10  
  Increment=1.2)  
{  
  Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }  
  Plot (FilePrefix="showLET40A" Time=(0.85e-9) NoOverwrite)  
}
```

```
Transient (  
  InitialTime=0.95e-9 FinalTime=2.1e-9 InitialStep=1e-13 MaxStep=1e-12  
  Increment=1.2)  
{  
  Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }  
  Plot (FilePrefix="showLET40B" Time=(1.001e-9;1.01e-9;1.02e-9;1.05e-9;1.1e-9;1.3e-9;1.5e-9)  
  NoOverwrite)  
}
```

```
Transient (  
  InitialTime=2.1e-9 FinalTime=10e-9 InitialStep=1e-12 MaxStep=1e-10  
  Increment=1.3)  
{  
  Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }  
}
```

```
}
```