RADIATION EFFECTS, NEGATIVE-BIAS-TEMPERATURE INSTABILITY, AND LOW-FREQUENCY 1/*f* NOISE IN $SiGe/SiO_2/HfO_2$ PMOS DEVICES

By

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To My Wife and Kid,

With Love

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CHAPTER I

Introduction

For the past forty years, the performance of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has increased greatly after tremendously and aggressively scaling down the size of MOSFETs. The channel length and the gate oxide thickness are two of the major scaling parameters. During the last twenty years the gate length has been scaled down by a factor of over twenty, as shown in Fig. 1.1. At present, semiconductor companies have produced sub-22 nm gate length MOS transistors ahead of the roadmap in Fig. 1.1, and the physical channel length in these devices is typically shorter than the drawn length.

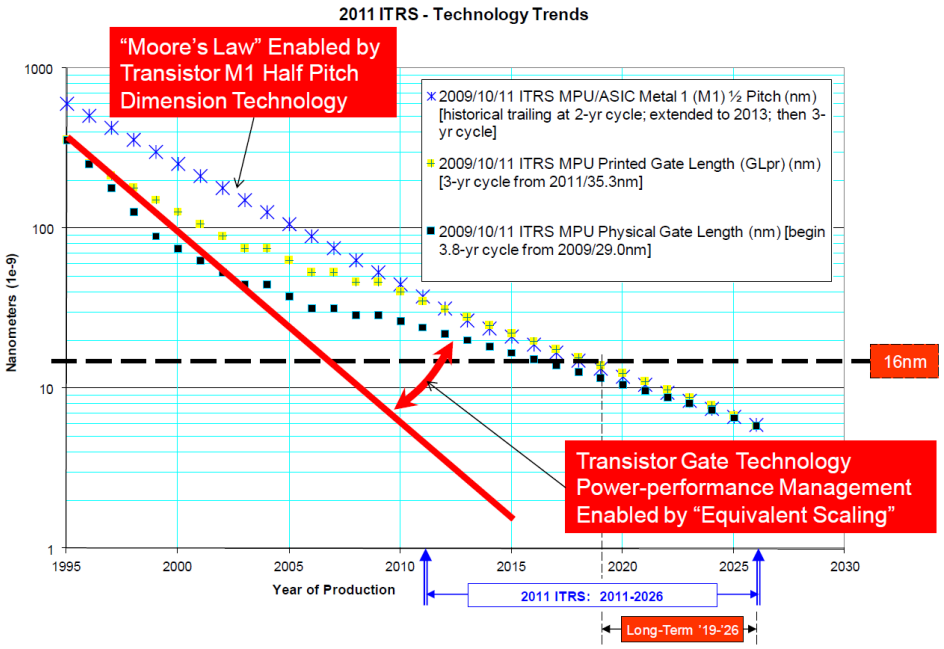


Fig. 1.1. MOS gate length trends and the 2011 International Technology Roadmap for Semiconductors (ITRS 2011) (after [1]).

The most widely accepted rule to keep transistors properly functioning is that both the supply voltages and dimensions are shrunk by the same factor in order to maintain an electric field in the small-sized device that is the same as for large devices. However, the thicknesses of conventional bulk SiO_2 gate dielectrics have reached the physical limitation (10-12 Å) [2], which is only a few atomic layers thick, due to the exponential increase in leakage current. To surmount this critical problem, high-permittivity (high-K) materials such as hafnium-based, zirconium and aluminum oxides [3] have been introduced as alternative gate dielectrics in place of the conventional SiO_2. High-K materials allow a further increase of the physical thickness of the gate stack to overcome the physical constrains and excessive leakage current, while keeping the equivalent oxide thickness (EOT) constant

$$\mathrm{EOT} = \frac{\varepsilon_{high\text{-}K}}{\varepsilon_{SiO_2}} d_{high\text{-}K},$$

where ε_{SiO_2} and $\varepsilon_{high\text{-}K}$ are the dielectric constant of silicon oxide and high-K material, respectively. $d_{high\text{-}K}$ is the physical thickness of high-K dielectric.

Not every high-K oxide can be a good substitute for SiO_2. Thermal Si oxide, which has been studied intensively for more than 40 years, forms an excellent interface with the Si. In addition to the high dielectric constant compared to SiO_2, there are several requirements for high-K materials that can be used as a MOS gate dielectric material. They must be thermodynamically stable with the Si channel and the gate electrode, and they should be kinetically stable and be compatible with processing to no less than 500 ℃. Moreover, they should have band offsets with Si of over 1 eV so that the carrier injection into the oxide is minimized, have a high-quality interface with Si, and low bulk-oxide trap density. Table 1

summarizes various characteristics and main features of several alternative high-K gate dielectrics that were considered as potential materials for MOS gate dielectric applications.

Table 1. Comparison of the major characteristics, advantages, and disadvantages of existing and potential high-k gate dielectrics (After [3]).

Dielectric	Dielectric constant	Bandgap (eV)	Conduction band offset (eV)	Merits	Drawbacks
SiO_2	3.9	8.9	3.15	Excellent Si interface, low Q_{ox} and D_{it}	Low-k
Si_3N_4	7-7.8	5.3	2.1	Good interface and bulk properties, medium Q_{ox} and D_{it}	Low-k
Al_2O_3	9-10	8.8	2.8	E_g comparable to SiO_2, amorphous	Medium Q_{ox} and D_{it}, medium k
Ta_2O_5	25	4.4	0.36	High-K	Unacceptable ΔE_C, not stable on Si
La_2O_3	~27	5.8	2.3	High-K, better thermal stability	Moisture absorption, unstable with Si
Y_2O_3	~15	6	2.3	Large E_g	Low crystallization temperature, high D_{it}, silicide formation
HfO_2	~20	5.6-5.7	1.3-1.5	Most suitable compared to other candidates	Crystallization, silicate and silicide formation
ZrO_2	~23	4.5-5.7	0.8-1.4	Similar to HfO_2	High Q_{ox} and D_{it}, Marginal stable with Si, crystallization, silicide formation

Among these, Hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) are the materials with greatest potential to replace SiO_2 in MOS devices, mainly due to their relatively high dielectric constants compared to other high-K materials and better band offsets than most other high-K dielectrics, as shown in Fig. 1.2. HfO_2 is found to be thermodynamically stable when it forms an interfacial layer SiO_2 with Si, whereas the ZrO_2/Si interface is unstable [4]. The presence of a SiO_2 layer that is compatible with the Si substrate can separate the high-K oxide from the Si channel, which reduces the remote scattering caused by defects in high-K oxide. The stable interface with silicon makes HfO_2 a preferred candidate to replace SiO_2 as a gate dielectric over ZrO_2 [5],[6].

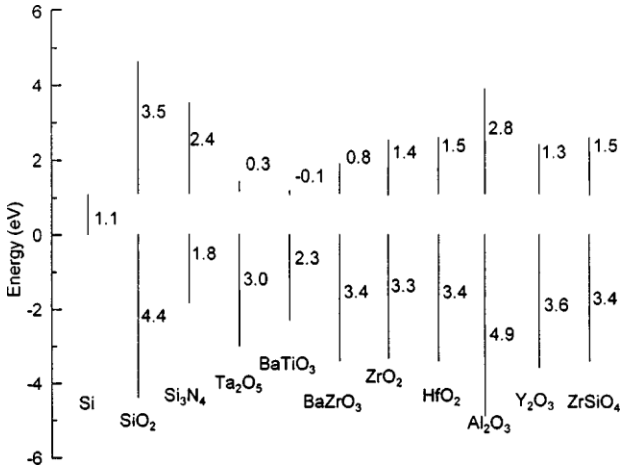
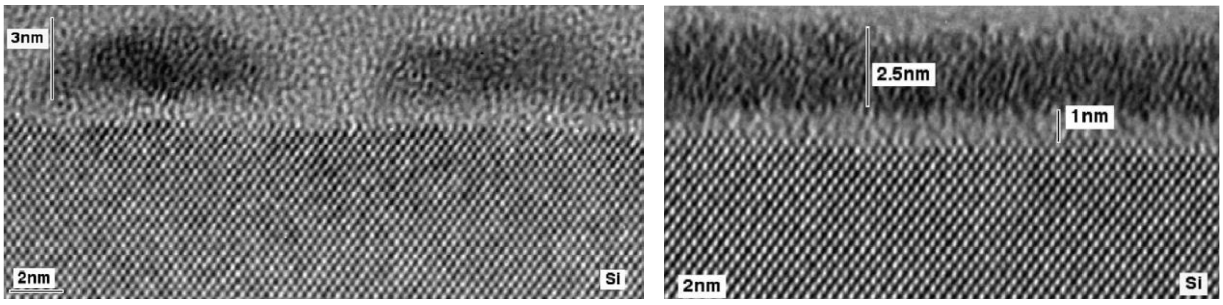


Fig. 1.2. Calculated conduction band and valence band offsets of various alternate oxides on Si (After [3]).

1.1 HfO_2

Atomic layer deposition (ALD) has emerged as an important technique for depositing thin high-K gate oxides in the MOSFET structure. However, the inefficient ALD nucleation is a very serious issue for the deposition of ultrathin high-K gate dielectric films. To grow an extremely uniform layer-by-layer ALD film, which is needed to ensure uniform electrical performance across the entire gate oxide, the nucleation of ALD precursors with the initial

surface species needs to be efficient on the very first ALD cycle. E. P. Gusev et al. [7] reported ultrathin hafnium oxide films deposited by ALD using sequential exposures of $HfCl_4$ and H_2O at 300 ℃ on a bare hydrogen-passivated silicon surface or a thin thermally grown SiO_2-based interlayer. High-resolution transmission electron microscopy (HRTEM) reveals that HfO_2 deposited on HF-last treated Si surfaces shows a non-uniform, island-like morphology and poor electrical properties due to inefficient nucleation on H-terminated Si as shown in Fig. 1.3(a). However, Fig. 1.3(b) captures a uniform HfO_2 ALD film on an ultrathin SiO_2 interlayer on the initial Si surface, which shows good electrical properties with respect to conventional SiO_2 gate dielectrics, which justifies its consideration as a candidate for high-K dielectric for MOSFETs. These comparison results highlight the important role of an ultrathin SiO_2 coating (< 1 nm) on Si in high surface qualities and electrical properties.



(a) (b)

Fig. 1.3. HRTEM cross-section of a HfO_2 ALD film deposited on (a) a Si wafer immediately after HF-last surface treatment and (b) a SiO_2 layer on a Si wafer (after [7]).

G. Bersuker et al. [8] captured the oxygen removal from the underlying SiO_2 layer due to deposition and processing of the standard HfO_2 in electron spin resonance (ESR) spectra as shown in Fig. 1.4. The dominant electrically active defects at the Si/SiO_2 interface are P_b centers (P_{b0} and P_{b1}, as will be discussed later), which involve an unpaired electron on a Si atom back bonded to three other Si atoms of the substrate at the Si/SiO_2 interface. The dominant defects in

the bulk SiO_2 observed here are E' center defects, which consist of an unpaired electron on a Si atom back-bonded to three oxygen atoms. These E' center defects are oxygen vacancies. Though the density of P_b centers can be maintained at an acceptable level through hydrogen passivation, a potential consequence is that hydrogen could be released during device operation, under elevated temperature or under certain gate voltage conditions, thereby affecting device reliability.

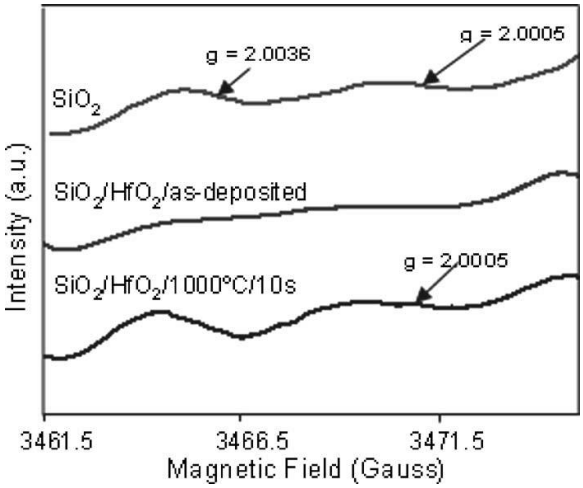


Fig. 1.4. ESR spectra of the starting 1.1 nm SiO_2 layer, the same layer after ALD HfO_2 deposition, and after subsequent 1000 ℃ annealing (after [8]).

1.2 SiGe

In addition to the introduction of high-K material in MOS devices, the incorporation of several new materials and structural changes is required for continuing MOSFET evolution. The lattice constant of silicon is about 0.54 nm in a diamond cubic crystal structure [9]. The shorter the channel is, the easier it is to carry high currents. The key parameters are the inversion layer mobility and the density of charge in the inversion layer. People have been searching for alternative channel materials to replace silicon at the wafer surface, in an effort to improve the performance of MOS devices. Owing to the high hole mobility and compatibility with standard silicon processes, silicon germanium (SiGe) is of great interest as an alternative channel material

to achieve a performance boost for *p*MOSFETs [10]. In July 2015, IBM announced that it made the advance by using SiGe instead of pure silicon in the first working sample of a chip with 7 nm transistors in the world. So SiGe is a promising candidate for the semiconductor industry at 7 nm nodes.

However, there are many issues that need to be solved for SiGe MOS devices. One of the significant issues concerning SiGe MOS fabrication is forming a stable interface between the gate dielectric and SiGe channel. Conventionally, a thin Si cap layer is used for SiGe surface passivation. The holes traveling in the SiGe channel are expected to have enhanced mobility by fundamentally altering the band structure of the channel due to the presence of the germanium. Furthermore, since the SiGe is separated from the gate oxide by a thin silicon cap layer, the surface scattering should be negligible. Q. Ouyang et. al. [11] proposed a novel *p*MOSFET with a SiGe S/D and a strained SiGe quantum well channel, as shown in Fig. 1.5. It has improved device performance and scalability to levels better as compared to those of a conventional Si *p*MOSFET.

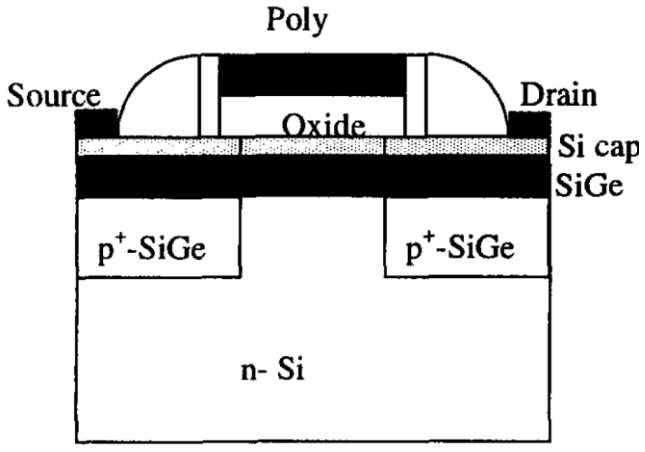


Fig. 1.5. Schematic diagram of a novel *p*MOSFET with a SiGe S/D, a Si cap layer and a strained SiGe quantum well channel (after [11]).

1.3 Thesis Organization

It is necessary to evaluate the charge trapping characteristics and long-term reliability of SiGe/high-k structure devices for potential space-exploration applications. In this thesis, total-ionizing dose radiation effects, bias-temperature stress effects and low-frequency 1/*f* noise on SiGe/high-k structure are explored. This thesis is organized as follows: Chapter II goes over the basic mechanisms of total ionizing dose (TID) radiation effect and some popular models of negative bias temperature stability (NBTI) in *p*MOS. Chapter III introduces the background for analyzing noise in CMOS transistors. We review the basic mechanisms and models of 1/*f* noise in MOSFET transistors. Chapter IV focuses on the irradiation bias dependence of SiGe *p*MOS FinFETs as a function of total dose irradiation, and chapter V describes the negative bias temperature stress results on SiGe-*p*MOSFETs. Chapter VI presents and discusses experimental results on the temperature dependence of the 1/*f* noise on SiGe-*p*MOSFETs. Chapter VII concludes the thesis.

CHAPTER II

NBTI and TID mechanisms

The first part of this chapter contains background information about total ionizing dose effects in MOS devices. The second part of this chapter describes the mechanisms of negative bias temperature instability (NBTI) in MOS devices. The midgap and subthreshold swing methods that are used in his work to separate the threshold voltage shifts due to oxide-trap charge (ΔV_{ot}) and interface-trap charge (ΔV_{it}) are described in detail.

2.1 Total ionizing dose effects in MOS devices

The microelectronic components in space are exposed to various types of radiation such as protons and electrons, which interact with the semiconductor material to cause ionizing damage, atomic displacement, and/or single event effects. Total-dose irradiation is a significant concern for the long-term reliability of MOS devices. It is extremely important to understand radiation effects on semiconductor devices for the application of advanced technologies and materials in space environments. This section will discuss the basic effects of radiation-induced charge buildup in MOS devices, including oxide, interface, and border traps.

Fig. 2.1 shows a schematic energy diagram of a MOS structure under positive bias applied to the gate and indicates four major physical processes that contribute to the radiation response of a MOS device. For MOS devices, the most total-dose radiation-sensitive parts are the oxide insulators. When a MOS device is exposed to high-energy ionizing radiation, electron-hole pairs are created in the oxide by the deposited energy (process 1). Because the electrons are much more mobile (20 cm^2/V sec at 300 K in fused quartz [12]) than the holes ($\sim 4 \times 10^{-9}$ cm^2/V

sec at 300 K) in SiO_2, most of the electrons are rapidly swept out of the oxide (within picoseconds), and holes are trapped in micro-structural defects and pre-existing traps. However, even before the electrons leave the oxide, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the charge yield. The fraction depends greatly on the strength of the electric field in the oxide and the energy of the incident particle. The generation and recombination of electron-hole pairs are the first processes shown in Fig 2.1. Those holes that escape initial recombination will further transport toward the Si/SiO_2 interface by hopping via localized states in the oxide (process 2) [13]. This process typically takes less than a second [14], but may take place over many decades in time. Because hole transport in SiO_2 is highly dispersive [15], as a result, the "tail" of the transport extends over several decades in time.

As the holes approach the Si/SiO_2 interface, some fraction of the holes are neutralized by electrons tunneling from silicon or thermal emission from the trap sites, and others get trapped at relatively deep trap states, forming positive oxide trap charges (process 3). These oxide trapped charges can cause a shift in the threshold voltage and an increase of radiation-induced leakage current (RILC) in these devices. RILC involves an inelastic tunneling process assisted by neutral traps in the oxide. The neutral electron trap likely originates as radiation-induced holes trapped at E' centers (E' centers will be described in detail later) in the oxide. The Electron Spin Resonance (ESR) measurements performed by P. M. Lenahan et al. have shown a link between E' centers and RILC [17].

Meanwhile, hydrogen ions (protons) can be released in the oxide bulk as holes transport toward the interface through the oxide. Those protons can drift to the Si/SiO_2 interface under positive gate bias where they may react with Si-H to form H_2, leaving silicon dangling bonds at

the interface (process 4). These dangling bonds can act as interface traps, which are localized states in the Si band-gap. Their occupancy is determined by the Fermi level, leading to a change of threshold voltage and a decrease of carrier mobility.

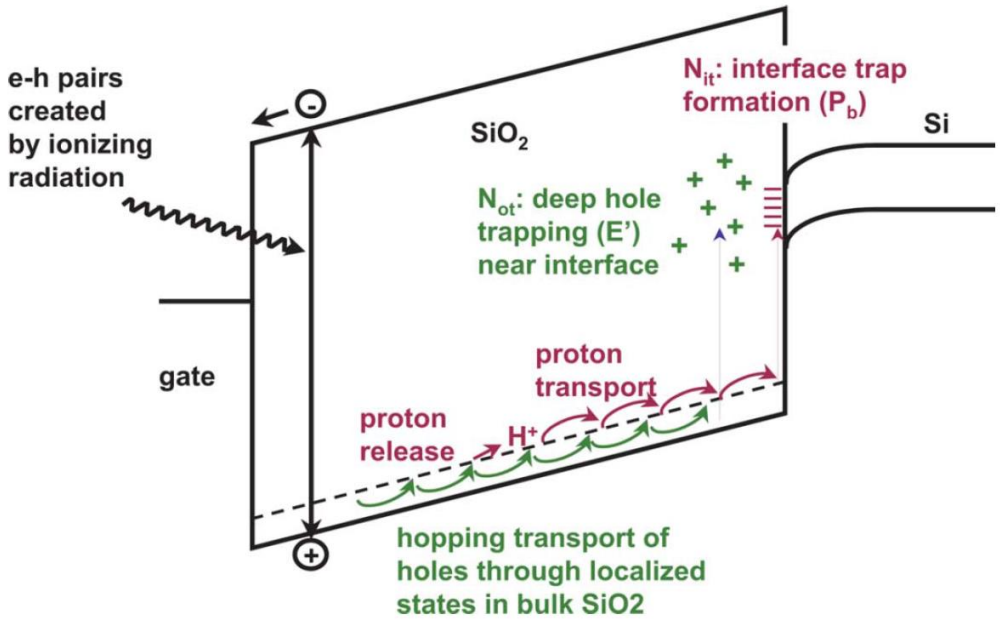


Fig. 2.1. Schematic energy band diagram for MOS structure under positive bias, indicating major physical processes underlying radiation response. After [16].

As previously mentioned, some fraction of the radiation-induced holes will recombine with the electrons before the electrons are swept out of silicon dioxide, in a time on the order of a picosecond. The fraction of holes escaping initial recombination (f_y) depends strongly on the magnitude of the electric field through the oxide. When an electric field is applied across the oxide of a MOS device, the radiation-induced electron-hole pairs will immediately be separated and begin to transport in opposite directions. As the electric field strength increases to separate pairs more efficiently, the probability that a hole will recombine with an electron decreases, and the charge yield increases. Fig. 2.2 plots the fraction of holes that escape recombination for 10-keV x-ray irradiation as a function of the electric field. When the electric field is higher than 4 MV/cm, more than 80% of radiation-induced holes escape initial recombination.

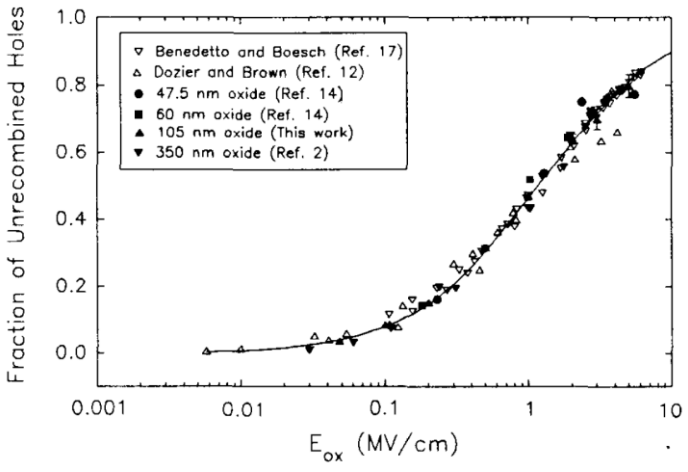


Fig. 2.2. Fraction of holes which escape recombination for 10-keV x-ray irradiations as a function of oxide field. The solid line is a fit to data. After [18].

In recent years, although manufacturers have been able to reduce EOT and increase physical oxide thickness by introducing high-K dielectric, the electric field present in the channel and gate dielectric has been increasing. Moreover, tunneling into the bulk high-K oxide increases as the interfacial SiO_2 oxide of the SiO_2/high-K dielectric stack composing the gate dielectric becomes thinner. As a result, operating temperatures have increased, too. Time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), and bias temperature instability (BTI) are three major reliability issues in modern CMOS technology. Among the three, BTI increases most sharply with electric field and temperature. BTI is a shift in threshold voltage with applied stress at elevated temperature. From the standpoint of lifetime of modern MOS transistors, the devices are considered to have failed when the shift exceeds typically 30 mV [19]. For highly scaled pMOSFETs, NBTI has been a more serious concern than positive BTI (PBTI). In 2014, J. H. Stathis et al. [19] showed operation voltage reduction requirement for gate oxide scaling at the 2014 IEEE Electron Device Meeting (IEDM) in Fig. 2.3. The 2013 ITRS roadmap anticipates sufficient voltage reduction to maintain nMOS scaling. However, NBTI may limit silicon-based pMOS scaling unless new materials such SiGe channel devices are adopted.

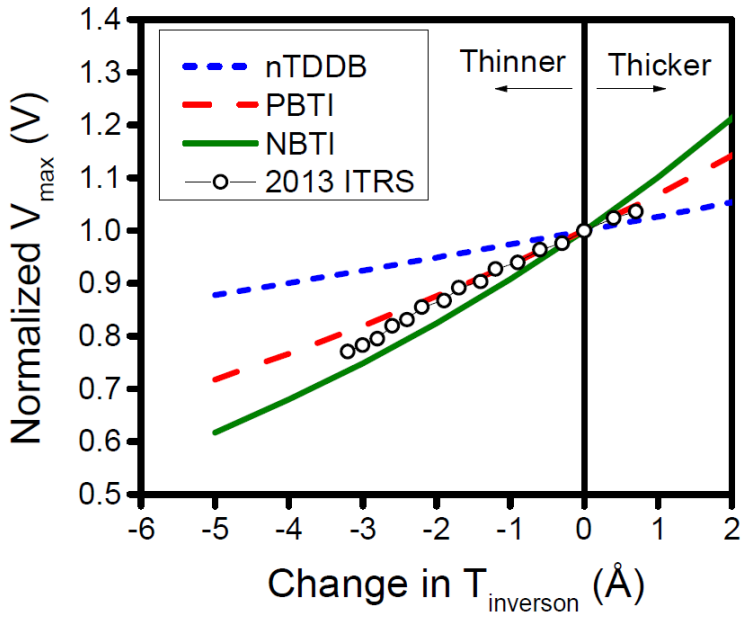


Fig. 2.3. Trend of maximum operation voltage V_{max} for constant reliability for the three major gate dielectric failure modes, and ITRS roadmap trend for V_{dd} and EOT scaling from 10nm node (after [19]).

2.2 What does NBTI do?

NBTI is associated with the creation of oxide charge and interface traps at the Si/oxide interface, when negative bias is applied to the gate at elevated temperatures. NBTI has a significant impact on pMOSFETs since these devices work under negative bias conditions during high-performance chip operation. Oxide-trapped charges are located within the oxide, and are not in electrical communication with the underlying Si. Interface traps are located at the Si/SiO_2 interface and in electrical communication with the underlying Si. Border traps are near-interfacial oxide traps that exchange charge with the underlying Si on the time scale of the measurements [20].

2.2.1 Oxide traps

There are a large number of oxygen vacancies close to the interface where oxidation is not complete. The oxygen vacancy can be activated into the paramagnetic state by irradiation or

electrical field stress. That radiation-induced or stress-induced paramagnetic center is termed an E’ defect, which is identified as a "trivalent silicon” back-bonded to three oxygen atoms in the oxide. There is one oxygen atom missing from the usual Si-O-Si lattice configuration, leaving a weak Si–Si bond. That an E’ center is an oxygen vacancy can be verified by ESR. J. T. Ryan et al. have observed that ESR spectra due to E’ center defects are generated by elevated temperature and modest negative gate bias and quickly disappear once the stress is removed [21]. E’ centers or oxygen vacancies are primarily responsible for hole traps in *p*MOS devices during NBTI. F. J. Feigl, W. B. Fowler and K. L. Yip proposed an oxygen vacancy model (Feigl-Fowler-Yip model) for the E’ center [22]. As illustrated in Fig. 2.4, after the hole is trapped in the precursor bridging-oxygen vacancy, a weak strained Si-Si bond configuration is broken. One of the Si atoms then relaxes back into a planar configuration, leaving it positively charged. The other Si remains neutral, with a dangling orbital containing one unpaired electron. An E’ center consists of these two trivalent Si atoms together. The E’ signal in ESR is actually obtained by resonant flipping of the spin of the unpaired electron on the neutral Si atom.

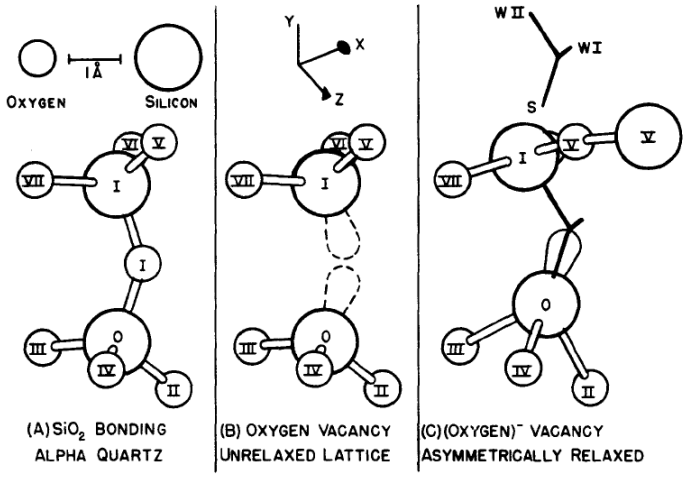


Fig. 2.4. Oxygen vacancy model for the E’ center in SiO_2. (a) Normal oxygen vacancy. An important feature is the existence of two inequivalent Si-O bonds. (b) Unrelaxed lattice oxygen vacancy. (c) Asymmetrically relaxed O^- vacancy (After [22]).

2.2.2 Interface traps

In addition to oxide traps, NBTI can also cause the formation of interface traps at the Si/SiO_2 interface. J. P. Campbell et al. [23] utilized spin-dependent recombination (SDR) to observe and identify two silicon dangling bond centers (P_{b0} and P_{b1} defects) at the Si/SiO_2 interface generated by a negative bias temperature in *p*MOSFETs. This P_b center is also a "trivalent silicon" as is E' center, but in this case the silicon is bonded to three Si atoms, with a dangling bond extending into the oxide, as schematically represented in Fig. 2.5. Because of the energy level within the Si bandgap and location at the interface, the interface defect is amphoteric, negatively charged above midgap, approximately neutral near midgap, and positively charged below midgap.

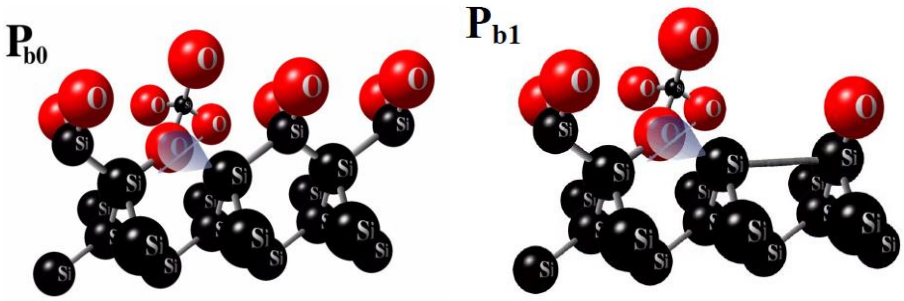
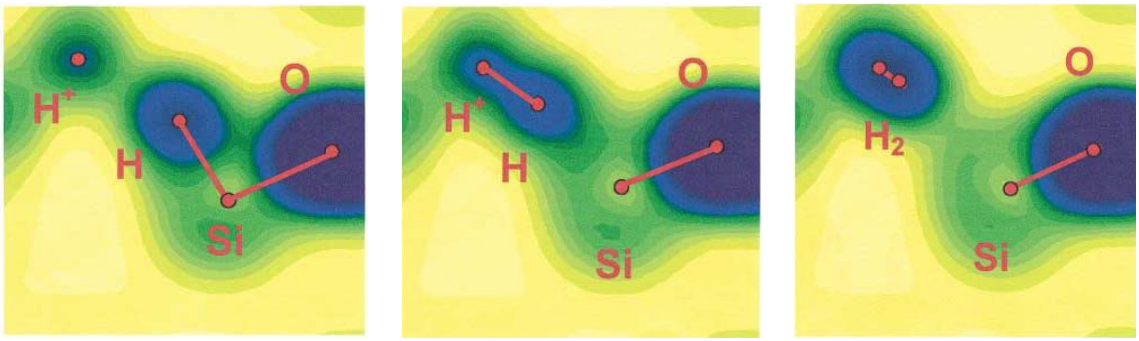


Fig. 2.5. Schematic diagrams of P_{b0} and P_{b1} Si/SiO_2 interface traps (after [23]).

Density functional theory calculations by Rashkeev et al. [24] strongly suggest that protons interact directly and break the Si-H bonds (P_b-H precursor sites) at the Si/SiO_2 interface via the simple reaction:

$$H^+ + Si\text{-}H = Si^+ + H_2$$

Fig. 2.6 traces the computed electric density contours in the region around a Si dangling bond passivated by hydrogen at the Si/SiO_2 interface during the depassivation process. The calculations suggest that two electrons leave the Si-H through $Si\text{-}H\text{-}H^+$ bridge, forming a neutral H_2 molecule and leaving a dangling bond positively charged.



(a) (b) (c)

Fig. 2.6. Electronic density at different stages of the reaction between H^+ and a Si-H bond: (a) a proton approaches a Si-H bond; (b) an Si-H-H^+ bridge is created; (c) an H_2 molecule and a D^+ defect are formed (after [24]).

2.2.3 Border traps

A standard name for near-interfacial oxide traps that communicate with the Si was proposed as "border traps" by D. M. Fleetwood in 1992 [20]. Border traps are defined as near-interfacial oxide traps that are able to rapidly or slowly exchange charge with the underlying Si substrate over a very wide range of time scales. There is growing evidence that a large percentage of these defects are likely associated with E' centers [20],[25],[26]. Border traps typically are located within a certain distance (~2 nm) in the oxide from the interface, as shown in Fig. 2.7.

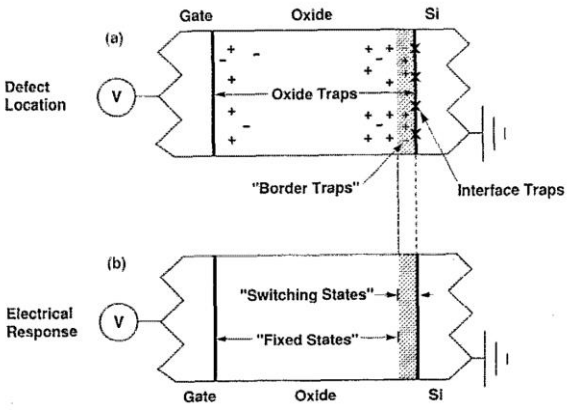


Fig. 2.7. Schematic representation of (a) the physical location of oxide, interface, and border traps and (b) their electrical response (after [20]).

2.2.4 Charge separation techniques

To separate the effects of oxide and interface trap charge, the overall radiation response of a MOS device needs to be separated into its components:

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \tag{2.1}$$

Here ΔV_{ot} and ΔV_{it} are the threshold voltage shifts due to oxide traps and interface traps, respectively. There are different methods for separating ΔV_{th} into its components.

Midgap charge separation method:

The midgap charge separation method is based on the observation that the interface traps are approximately charge neutral for a device biased at midgap [28],[29]. The interface traps are amphoteric. In the upper portion of the band gap the interface traps are mostly acceptor-like. These are negatively charged when filled and neutral when empty. In the bottom portion of the band gap they are donor-like; these are neutral when filled and positively charged when empty, as shown in Fig. 2.8. In this case, the net oxide-trapped charge density changes can be estimated by the shifts in the midgap voltages (ΔV_{mg}):

$$\Delta V_{ot} = \Delta V_{mg} \tag{2.2}$$

$$\Delta V_{it} = \Delta V_{th} - \Delta V_{mg} \tag{2.3}$$

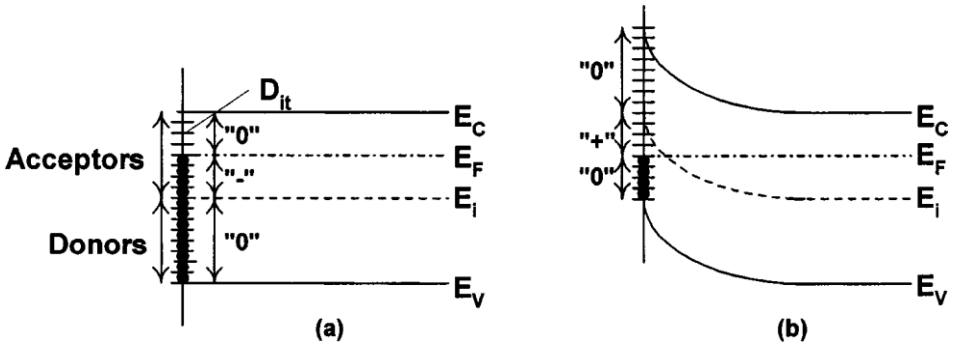


Fig. 2.8. Band diagrams of the Si substrate of a p-channel MOS device showing the occupancy of interface traps and the various charge polarities with (a) negative interface trap charge at flatband and (b) positive interface trap charge at inversion (after [30]).

The midgap voltages (V_{mg}) can be determined from subthreshold-current curves, as illustrated in Fig. 2.9. The interface trap charge density change (ΔN_{it}) and oxide trap charge density change projected to the Si/SiO_2 interface (ΔN_{ot}) were estimated for MOS capacitors by the following equations:

$$\Delta N_{ot} = -C_{ox}\frac{\Delta V_{mg}}{qA} \tag{2.4}$$

$$\Delta N_{it} = C_{ox}\frac{(\Delta V_{th} - \Delta V_{mg})}{qA} \tag{2.5}$$

Here C_{ox} is the oxide capacitance, –q is the electronic charge, and A is the area.

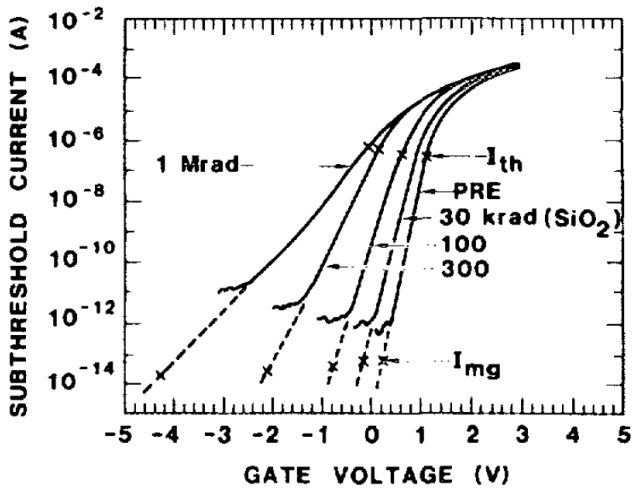


Fig. 2.9. Subthreshold-current curves for an MOS transistor before and after irradiation (after [28]).

Subthreshold swing method:

The subthreshold technique is based on standard I-V characteristics [29]. When plotted as log I_D versus V_G, comparing the pre- and post-irradiation characteristics, the change in subthreshold swing, ΔS, can be determined. The subthreshold swing method of the charge separation technique is based on the calculation of the radiation induced voltage shift due to interface traps, ΔV_{it}, using the change subthreshold swing, ΔS:

$$\Delta V_{it} = \frac{q\phi_s}{kT \ln 10} \Delta S \,, \tag{2.6}$$

$$\Delta V_{ot} = \Delta V_{th} - \Delta V_{it} \,, \tag{2.7}$$

Here ϕ_s is the surface potential, k is Boltzmann's constant, and T is the absolute temperature.

2.3 How does NBTI work?

Although NBTI has been known for more than 30 years, the mechanism for NBTI is still under debate, only recently has a consensus begun to emerge. A number of mechanisms to explain NBTI have been proposed and discarded.

2.3.1 Reaction-Diffusion model

NBTI has often been interpreted by some form of reaction-diffusion (RD) model, as originally proposed by Jeppson and Svensson [31]. The RD model is diffusion controlled and assumes that Si-H bonds at the semiconductor/oxide interface are broken at higher temperatures and electric fields, causing some hydrogen species to be released from previously passivated interface defects and then dispersively diffuse into the oxide.

Another RD model proposed by L. Tsetseris et al. [32] involves the depassivation of dopants in Si and subsequent movement of hydrogen species to the interface. First-principles calculations show that a direct depassivation reaction, $Si_3{\equiv}SiH + H^+ \rightarrow Si_3{\equiv}Si\bullet + H_2$, is in fact possible. Here $Si_3{\equiv}SiH$ is a hydrogen-passivated interface trap and $Si_3{\equiv}Si\bullet$ an interface trap with the dot representing the dangling bond. The hydrogen is assumed to be released from P-H bonds as the n-type Si surface is biased to depletion at elevated temperature. The hydrogen becomes positively charged (H^+) by trapping a hole. H^+ is swept to the interface by the negative bias, and subsequently reacts with the Si-H bond to form H_2 leaving behind a positively charged Si dangling bond (or P_b center). The H_2 diffuses from the interface into the oxide.

However, recent studies of NBTI [33],[34] find that interface-trap creation is not the sole source of degradation but a major hole trapping effect also occurs, especially when electric fields during NBTI stress approaches or exceeds ~ 10 MV/cm. Additionally, a large number of detailed recovery studies published in the last decade [34],[35] cannot be fully accounted for by the reaction-diffusion mechanism family. As a consequence, recent research focus has shifted back toward charge trapping. Interestingly, this hole trapping mechanism was also suggested in the pioneering paper on the RD model by Jeppson and Svensson [31].

2.3.2 Two-stage model

In 2009 Grasser et al. developed a comprehensive quantitative two-stage model able to capture a large number of the features [36], suggesting the degradation is due to interface trap generation and/or oxide charge buildup. The degradation is assumed to proceed in two coupled stages. For the first stage, the NBTI degradation process is initiated (stage 1) when inversion layer hole capture occurs at an E' precursor site, e.g., a neutral oxygen vacancy. The hole capture leads to positively charged E' centers (paramagnetic defects observable with ESR) in the oxide, thereby creating a switching trap, as illustrated in Fig. 2.10. Upon hole capture, the Si–Si bond breaks and a positively charged E'_{γ} center is created (state 2). Hole emission (electron capture) neutralizes the E'_{γ} center (state 3). Being in state 3, two options exist: a hole can be captured again, causing a transition to state 2, or the structure can relax back to its equilibrium configuration (state 1). For the second stage, oxide silicon dangling bonds (E' centers) created in the stage one process trigger the creation of P_b centers via hydrogen exchange with a P_b center at the interface. ESR measurements further confirmed that E' centers are generated during NBTI stress and very quickly recover upon removal of the stress [21]. The E' defect density does not change during zero oxide bias at elevated temperature or negative oxide bias at room temperature.

These observations support hole capture at an E' precursor site and the creation of interface traps. Recently Grasser et al. [37]-[39] have also included hydrogen related centers associated with NBTI. Complexes incorporating oxygen and hydrogen (e.g., the hydrogen bridge, which is a hydrogen atom at a dimer O vacancy in SiO_2 [37]-[39], and the hydroxyl E' center, a strained O bonded to a hydrogen atom [40],[41]) may also affect NBTI. In contrast to the E_δ'-centers, these defects are modified structurally and/or chemically via NBTI. Moreover, the hydrogen-related defects increase in density as a result of NBTI.

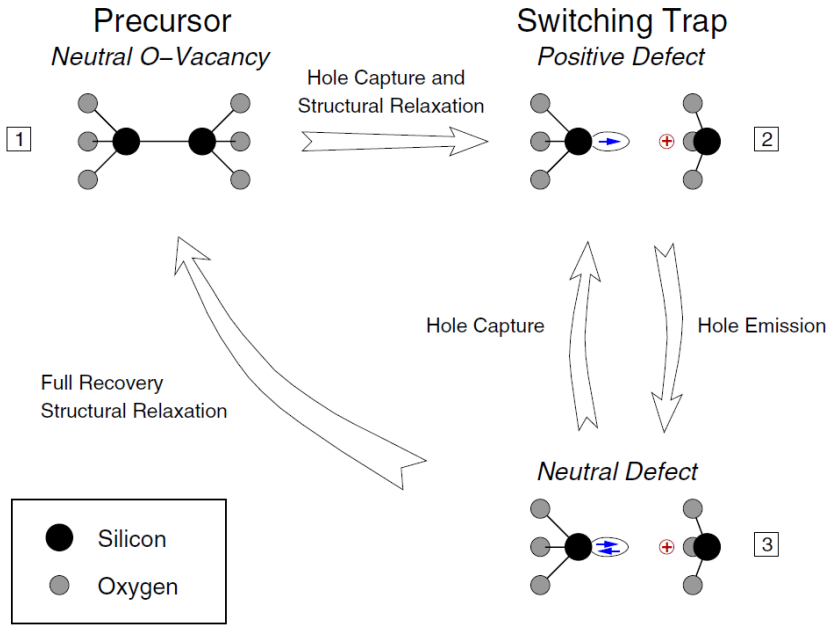


Fig. 2.10. Switching oxide trap model. After [36].

CHAPTER III

1/*f* noise theory

Many physical systems exhibit fluctuations with spectral densities that vary approximately as 1/*f* over a large range of frequencies. Several mechanisms exist that generate noise in semiconductors leading to a unique spectral power distribution in the frequency domain. Of these sources, the noise behavior of bulk CMOS devices is dominated primarily by two noise sources: thermal noise, flicker (1/*f*) noise. Other sources present in the noise spectrum include shot noise, generation/recombination (G-R) noise and random telegraph signal (RTS) noise. Fig. 3.1 shows a typical noise spectrum in a MOS transistor, in which the drain voltage power spectral density S_V is plotted as a function of frequency, showing the dominance of 1/*f* noise at low frequencies and thermal noise at higher frequencies.

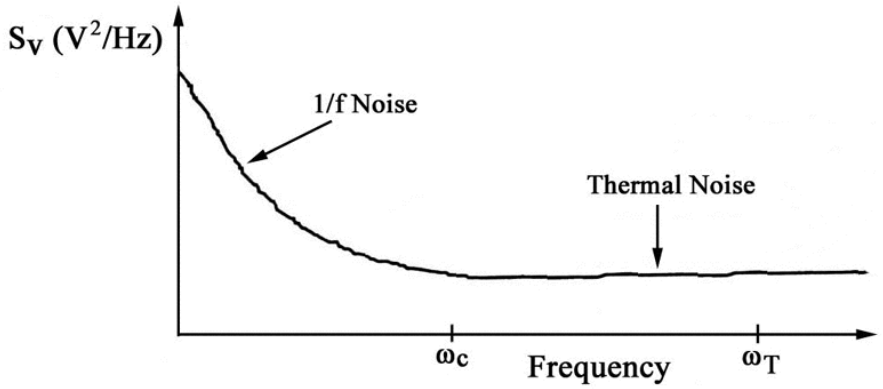


Fig. 3.1. Schematic variation of S_V with frequency, showing the dominant 1/*f* noise at low frequencies, and dominant thermal noise at high frequencies (after [42]).

Thermal noise:

Thermal noise is intrinsic to all resistors and caused by the random thermal motion of charge carriers at any finite temperature. This noise is sometimes known as the Johnson-Nyquist

noise. The internal noise voltage source V_t^2 (V^2) of the thermal noise across a resistor with resistance R is described by the Nyquist equation [43],[44]:

$$V_t^2 = 4kTR\Delta f \tag{3.1}$$

Here k is the Boltzmann constant, T is the absolute temperature, and Δf is the frequency bandwidth. V_t^2 depends on the temperature T, resistance R, and frequency f, but is independent of the current through the resistor. The voltage noise power spectral density of thermal noise S_{Vt} (V^2/Hz), $dV_t^2/df = 4kTR$, is independent of frequency. Thus, the thermal noise is the white noise.

3.1 Flicker noise

Flicker noise dominates the noise spectrum at low frequency. Flicker noise was first observed in vacuum tubes ninety years ago [45]. Flicker noise is also commonly called $1/f$ noise, because the noise spectrum varies as $1/f^{\alpha}$, where the exponent $\alpha, -\frac{\partial \ln S_V}{\partial \ln f}$, is close to unity (~0.7 < α < ~1.3). Here S_V is the excess noise after the thermal noise S_{Vt} is subtracted. $1/f$ noise is present in nearly all kinds of electronic devices under bias, including metal films, MOSFETs, BJTs, and diodes. A typical spectrum of $1/f$ noise in MOSFET with high-K gate dielectric stack is plotted in Fig. 3.2.

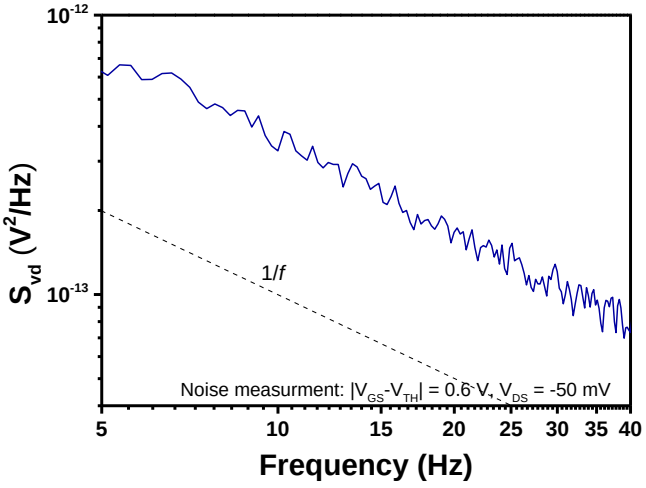


Fig. 3.2. $1/f$ noise in TiN/HfO_2/SiO_2 pMOSFET biased at V_{GS}-V_{th} = -0.6 V and V_{DS} = -0.05 V and at T = 360 K.

Although this noise is a nearly universal phenomenon in active devices, a variety of models have been proposed to explain $1/f$ noise in MOSFETs [46]-[48]. Two popular models have appeared in the literature to explain the occurrence of flicker noise in MOSFETs: the McWhorter number fluctuation theory and the Hooge mobility fluctuation theory. However, the thorough review of low-frequency $1/f$ noise by Fleetwood [49] shows a wealth of data demonstrating that the $1/f$ noise of semiconductor devices is due to carrier number fluctuations and not mobility fluctuations.

3.2 The McWhorter Model (Number Fluctuations)

In 1957, McWhorter proposed that flicker noise is primarily a surface effect. The McWhorter number fluctuation (ΔN) theory states that flicker noise is generated by fluctuations in the number of carriers due to charge trapping in surface states. McWhorter obtained the necessary $1/f$ spectrum by assuming that the time constant τ of the surface states varied with a $1/\tau$ distribution. That is, $1/f$ characteristics superpose many different spectra of G-R noise, where free carriers are randomly trapped and trapped by trap centers with different life times. This was the basic concept behind the McWhorter model which assumed that: (a) trap centers are uniformly distributed in the silicon oxide near the silicon surface; (b) the carrier tunneling to trap centers decreases exponentially with the distance from the surface; (c) the time constants increase with the distance from the surface; and (d) separate centers involved in trapping/detrapping are independent.

A number of applications of the McWhorter theory to MOSFETs have been done. For example, the McWhorter model as adapted to MOS transistors enables one to obtain first-order estimates of effective trap densities for defects with energy levels that are reasonably close to the Si conduction band (for *n*MOS transistors) or valence band (for *p*MOS transistors), using the assumption that $1/f$ noise is associated with the capture and emission of charge carriers in the

conducting channel by trap sites in the oxide, at or near the Si/SiO_2 interface. In experiments the excess drain voltage noise power spectral density (PSD) with the devices operated in the linear region in strong inversion is measured. At strong inversion bias condition, drain voltage PSD can be expressed approximately as [50]:

$$S_{vd}(f, V_d, V_g) = \frac{K}{f^{\alpha}} \frac{V_d^2}{(V_g - V_t)^{\beta}} \tag{3.2}$$

where α and β are fitting parameters that reflect the observed frequency dependence and gate-voltage dependence, respectively. K is the normalized low-frequency l/*f* noise magnitude as defined in Eq. (3.2). In the number fluctuation model that describes 1/*f* noise in MOSFETs:

$$K = \frac{q^2 kTD_{bt} t_{ox}^2}{LW\varepsilon_{ox}^2 \ln(t_{\max} / t_{\min})} \tag{3.3}$$

Here *k* is the Boltzmann constant, *T* is the absolute temperature, D_{bt} is the effective density of border traps per unit area per unit energy which can contribute to the l/*f* noise process, *A* is the channel surface area ($W \times L$), and t_{max} and t_{min} are presumed maximum and minimum "cutoff" times associated with the tunneling or thermally activated processes that lead to the observed noise.

In comparative studies with radiation effects, a strong correlation has been shown between the 1/*f* noise of MOS transistors and oxide-trap charge in SiO_2, whereas no correlation is generally observed between low frequency 1/*f* noise and interface-trap charge [50]-[52]. The 1/*f* noise of n-channel MOS devices increases with increasing oxide-trap charge during irradiation and decreases with decreasing oxide-trap charge during postirradiation annealing. Like hole trapping generated by negative bias-temperature stressing, the radiation-induced-hole trap was also identified as an E' center introduced in chapter 2. So reducing the number of oxygen vacancies in the oxide can significantly reduce the l/*f* noise of MOS devices.

3.3 The Dutta-Horn Model

The obvious candidates besides tunneling distances are activation energies. In 1979, Dutta, Dimon, and Horn [54] proposed that the nearly 1/*f* spectrum in metals was due to a broad distribution of activation energies. This technique was applied first to analyze the nearly 1/*f* spectrum noise in thin metal films, and then extend to Si- and compound-semiconductor-based microelectronic devices and materials.

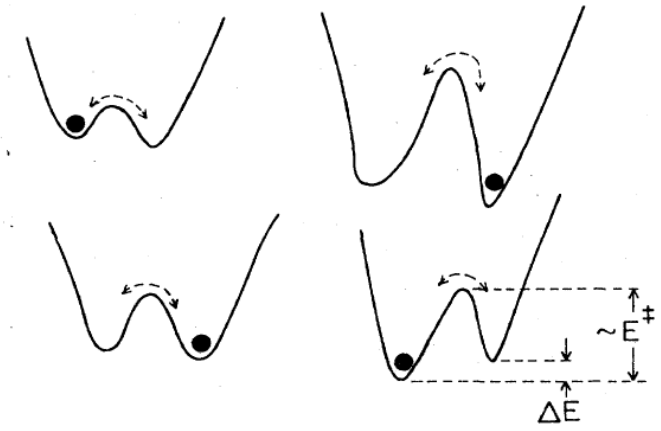


Fig. 3.3. The distinction between the two energies: the energy difference between the states (ΔE) and thermal activation energy ($E^{\pm}$)—for a two-level system in the classical regime (after [53]).

Dutta and Horn demonstrated that, if the noise is the result of thermally activated processes involving two energy levels separated by an energy barrier of E_o that the system must overcome for the system to move from one configurational state to another [48],[53],[54], as shown in Fig. 3.3. A single two-state system can be characterized by two energies: the energy difference between the states, ΔE, and the thermal activation energy for making the transition, E_o or $E^{\pm}$, which is inferred from the temperature dependence of the noise. In a collection of two-state systems defects have an energy distribution $D(E_o)$. The frequency exponent shows a temperature dependence described by:

$$\alpha(\omega,T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1\right). \tag{3.4}$$

Here

$$\alpha = -\frac{\partial \ln S_V}{\partial \ln f}, \tag{3.5}$$

S_V is the excess voltage-noise power spectral density after the thermal noise is subtracted, and τ_o is the characteristic time of the process leading to the noise. For noise that is successfully described by Eq. (3.4), one can infer the shape of the defect-energy distribution $D(E_o)$ over a wide range of energies from noise measurements as a function of temperature T via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega,T) \tag{3.6}$$

where the defect energy barrier is related to the temperature and frequency of the noise measurements through:

$$E_o \approx -kT\ln(\omega\tau_o) \tag{3.7}$$

In this work, low frequency 1/*f* noise measurements will be employed as a sensitive probe of defects that affect the devices threshold voltage and transconductance for SiGe *p*MOSFETs with HfO_2/SiO_2 gate oxide stack during NBTI.

CHAPTER IV

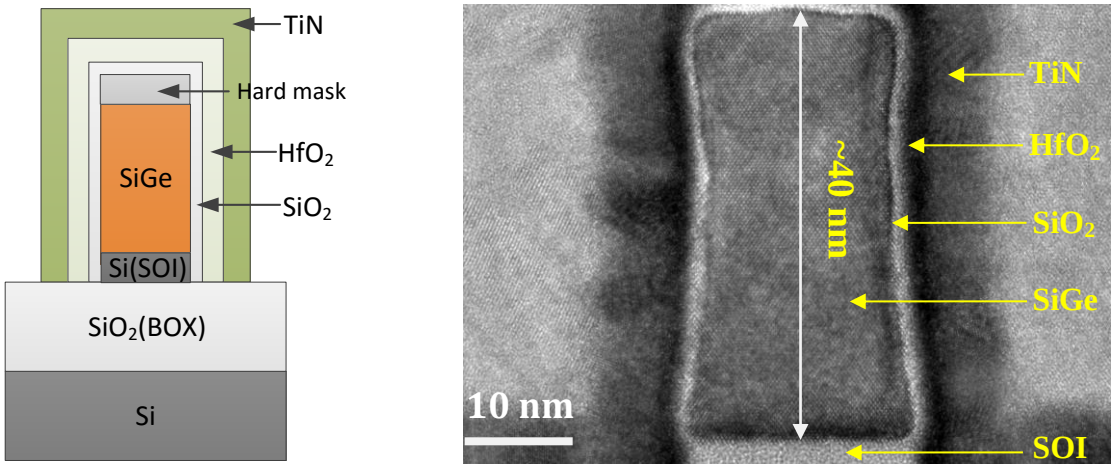
Total ionizing dose irradiation responses of SiGe *p*MOS devices

This chapter explores the effects of 10-keV X-ray irradiation on SiGe *p*MOS FinFETs with a $SiO_2/HfO_2/TiN$ gate stack under different irradiation biases. Negative threshold voltage shifts are observed in all cases, due to net positive oxide-trap charge. Negative bias irradiation leads to the worst-case degradation in the TID response of these devices. We attribute this to modification of the net trapped positive charge density in the HfO_2 layer as a result of additional radiation-induced holes that are generated in the SiO_2 interfacial layer of the bilayer insulating structure which, under negative bias, transport into and become trapped in the HfO_2. This leads to a more negative threshold voltage shift compared to 0 V irradiation. During positive bias irradiation, a number of radiation-induced electrons are generated in the SiO_2. These can similarly transport into and become trapped in the HfO_2, leading to a less negative threshold voltage shift than during 0 V irradiation.

4.1 Experimental details

*p*MOS FinFETs were fabricated on SOI wafers with strained $Si_{0.75}Ge_{0.25}$ fins that are intrinsically under ~1% compressive strain due to the lattice mismatch with the silicon buffer layer [55]. After the SiGe fin etching process, an HfO_2 layer (~2 nm) was formed by atomic layer deposition, and TiN and amorphous-Si were deposited. A ~1 nm SiO_2 interfacial layer (IL) was formed between the HfO_2 and SiGe fin, leading to an effective oxide thickness (EOT) of about 1.5 nm. Through this process, a high quality interface on SiGe can be achieved without the need for a Si cap layer [55]. This HfO_2/SiGe *p*MOS FinFET structure is shown schematically in Fig.

4.1(a). A TEM picture of the gate dielectric given in Fig. 4.1(b) clearly shows a SiO_2 interfacial layer existing between SiGe channel and HfO_2 dielectric. The work function difference between the TiN gate and SiGe is ~0.35 eV, as verified by Sentaurus device simulation [57]. The resulting structure has a built-in electric field of ~ 2MV/cm with 0 V applied bias.



(a) (b)

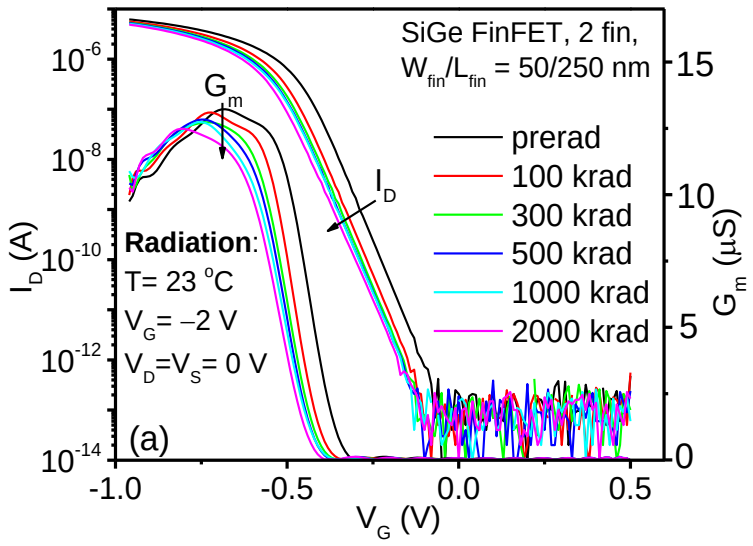
Fig. 4.1. (a) schematic and (b) TEM cross-section of a SiGe *p*MOS FinFET with HfO_2/SiO_2 gate dielectric (after [56]).

In this work, we have tested devices with a fin height (H_{fin}) of 40 nm and fin length (L_{fin}) of 250 nm. To examine the effects of the fin width (W_{fin}) on the TID response, two different as-drawn fin widths were measured: 50 and 100 nm. Although we follow the usual convention of quoting as-drawn fin widths in the descriptions of the experimental results that follow, the actual fin widths decrease with respect to the drawn width after device fabrication. In this case, the 50 nm drawn fin width is reduced to 25 nm in the fabricated device, while the 100 nm as-drawn fin-width is reduced to 70 nm. The presence of a hard mask on the top of the fin ensured double-gate instead of a trigate operation [55],[58]. The undoped Si layer that underlies the SiGe effectively decouples the device channel from the buried oxide [55],[58], consistent with the radiation response we report below.

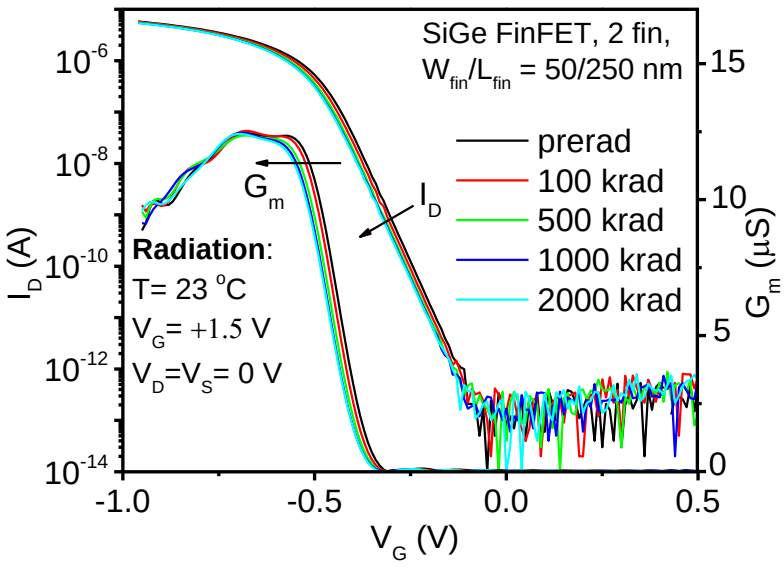
Unlidded devices were irradiated at a dose rate of 31.5 krad(SiO_2)/min using a 10 keV ARACOR x-ray source, under positive, negative, and 0 V gate bias, with other terminals grounded, at room temperature. I_D-V_G curves were measured to determine threshold voltage shifts (ΔV_{th}), and components due to oxide-trap charge (ΔV_{ot}) and effective interface-trap (ΔV_{it}) density using the midgap charge separation technique as introduced in Chapter 2.2.4. We note that the effective interface-trap density most likely also includes contributions from fast border traps [59],[60]. Device characterization was performed in air with a HP 4156B Semiconductor Parameter Analyzer. During I_D-V_G measurement, the source-drain voltage V_{SD} was kept at 50 mV, while the gate voltage was swept from 0.5 V to −1 V. Stress-induced degradation without irradiation was also measured at comparable irradiation times and biases. All irradiations and electrical stresses and measurements were performed at room temperature. At least three devices were measured for each case.

4.2 Experimental results and discussion

Figs. 4.2(a) and (b) show the drain current I_D at V_{SD} = 50 mV and transconductance G_m versus gate voltage V_G as a function of total dose at room temperature under negative and positive irradiation bias, respectively. The devices were irradiated up to 2 Mrad(SiO_2) at a gate bias of −2 V and +1.5 V, respectively, with all other terminals grounded. The I_D-V_G curves shift negatively with total dose under both positive and negative gate bias, consistent with the buildup of net oxide-trap charge primarily in the HfO_2 dielectric layer [61]-[64], since no stable hole trapping is expected in the ultrathin SiO_2 layer [65]. No excess leakage due to charge trapping in the buried oxide is observed.



(a)



(b)

Fig. 4.2. Drain current I_D and transconductance G_m as a function of gate voltage V_G and varying total dose with applied gate bias of (a) −2 V and (b) +1.5 V on devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm. The maximum effective mobility $g_{m,max}$ is degraded from ~352 ($cm^2/V•s$) to ~325 ($cm^2/V•s$) after 2 Mrad(SiO_2) irradiation under worst-case negative bias, as calculated via the equation $g_{m,max} = u_{eff,max}C_{ox}(W/L)V_{DS}$ in the non-saturated regime. Here C_{ox} = 2.3 μF/cm, effective gate width W =2 × H_{fin} = 80 nm, L = 250 nm, and V_{DS} = 50 mV (after [56]).

In Fig. 4.3, SiGe *p*MOS FinFETs are subjected to the same negative bias stress as in Fig. 4.2, with and without irradiation. The time scale on the top axis is matched to the time required for the total dose at the bottom axis for irradiation at a dose rate of 31.5 krad(SiO_2). The threshold voltage shift during negative gate bias is due to the tunneling of holes from the fin. The relatively large shifts at room temperature for high electric field indicate that shallow hole traps exist in the HfO_2 [63],[64]. In order to correct for the effect of the charge trapping that occurs as a result of electrical stress, adjusted values of purely radiation-induced ΔV_{th} (blue triangles) are obtained by subtracting ΔV_{th} due to negative bias stress without irradiation (black squares) from that due to negative-bias irradiation under negative bias (red circles).

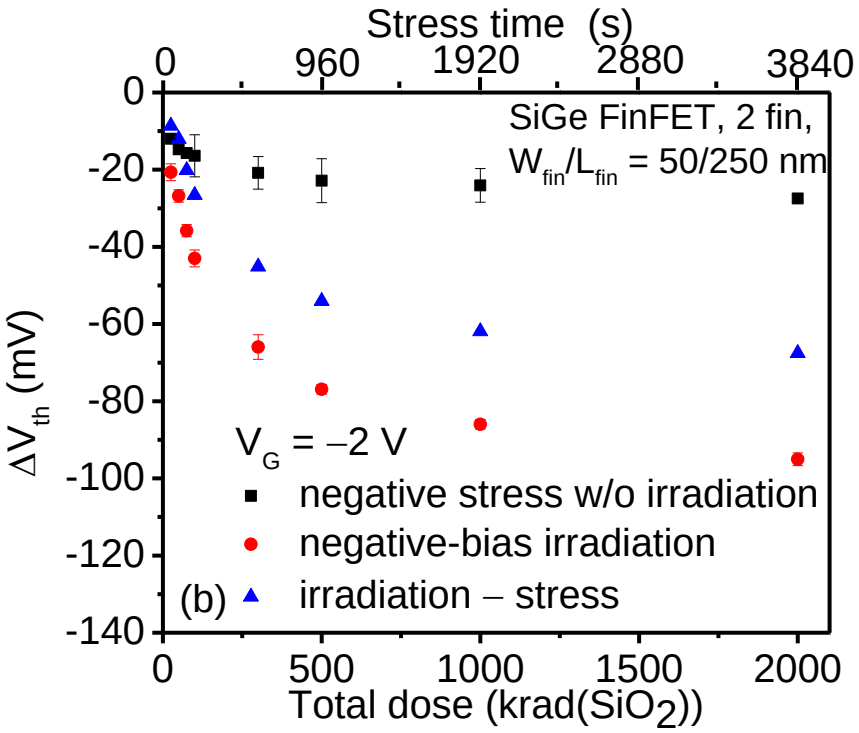


Fig. 4.3 Threshold voltage shift due to negative-bias irradiation as a function of total dose and due to negative stress without irradiation as stress time on devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm (after [56]).

Fig. 4.4 shows the threshold voltage shifts as a function of total dose and corresponding stress times at an applied gate bias of +1.5 V for SiGe *p*MOS FinFETs with a HfO_2/SiO_2 gate

dielectric stack. No significant threshold voltage shifts are observed for these devices under similar stressing conditions for positive gate bias, without irradiation, indicating negligible stress-induced negative-charge trapping in the bulk of the HfO_2/SiO_2. The absence of electron trapping under positive bias stress is likely due to the presence of the interfacial layer SiO_2 which acts as an effective barrier for electron tunneling into HfO_2. Thus, we conclude that the threshold voltage shifts observed during positive bias X-ray exposure are only induced by the irradiation.

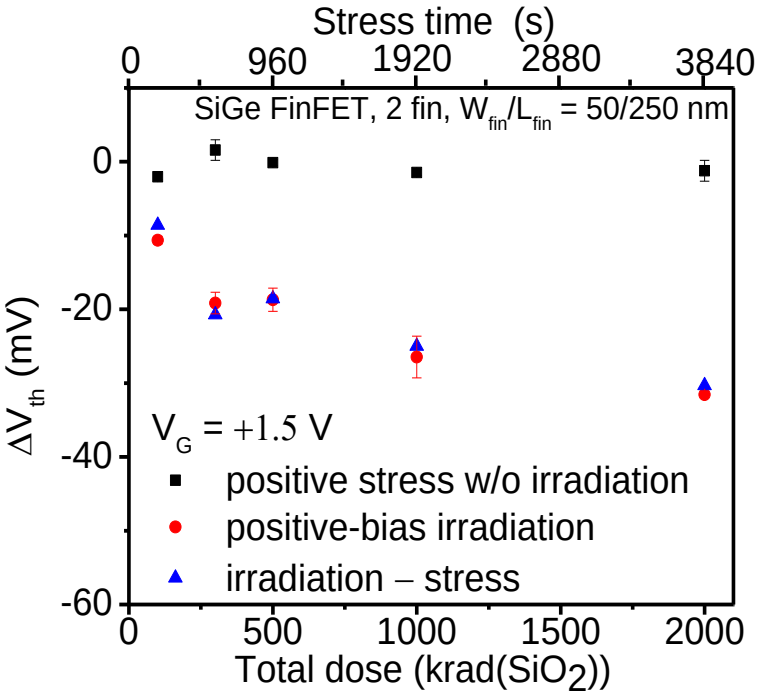


Fig. 4.4 ΔV_{th} as a function of dose for SiGe *p*MOS FinFETs irradiated with 10-keV X-rays at a dose rate of 31 krad(SiO_2)/min and as function of stress time without irradiation under +1.5 V (after [56]).

Fig. 4.5 shows the adjusted radiation responses of SiGe *p*MOS FinFETs irradiated with 10 keV X-rays up to 2 Mrad(SiO_2). The applied biases are +1.5 V for positive-bias irradiation and −2 V for negative-bias irradiation. Including the work function, the applied electric field for positive bias irradiation was ~ 12 MV/cm, 2 MV/cm for 0 V irradiation, and −11 MV/cm for negative bias irradiation. The largest threshold shift is observed for negative-bias irradiation, in contrast to what is typically observed for Si devices with SiO_2 or HfO_2 gate dielectrics [64].

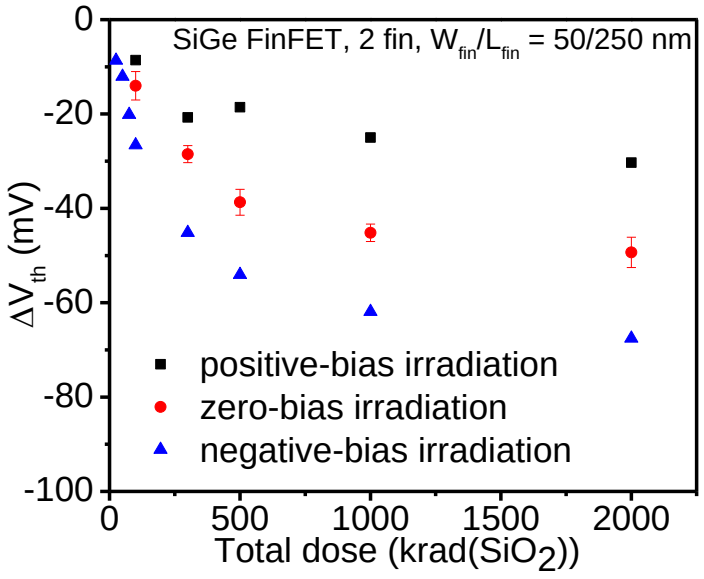


Fig. 4.5 Adjusted ΔV_{th} as a function of dose under different irradiation bias conditions. The gate biases during irradiation are +1.5 V, 0 V, and –2 V (after [56]).

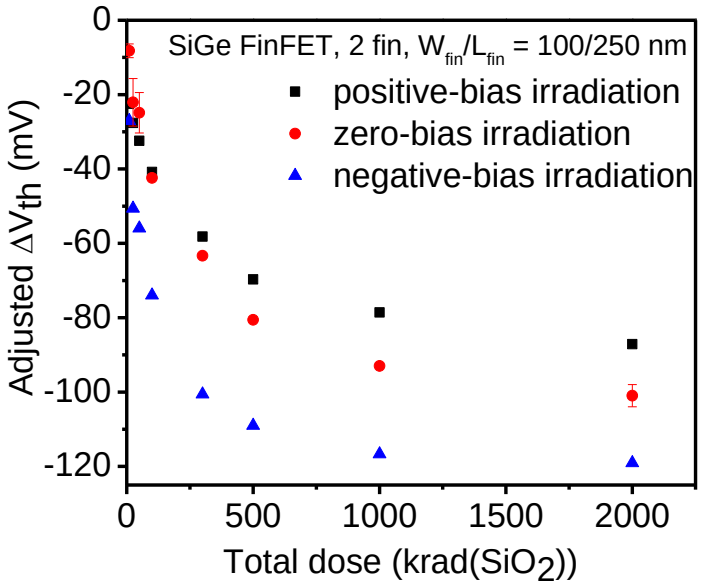


Fig. 4.6. Adjusted ΔV_{th} as a function of dose under different irradiation bias conditions for devices with 100 nm fin width and 250 nm fin length. The gate biases during irradiation are +1.5 V, 0 V, and –2 V (after [56]).

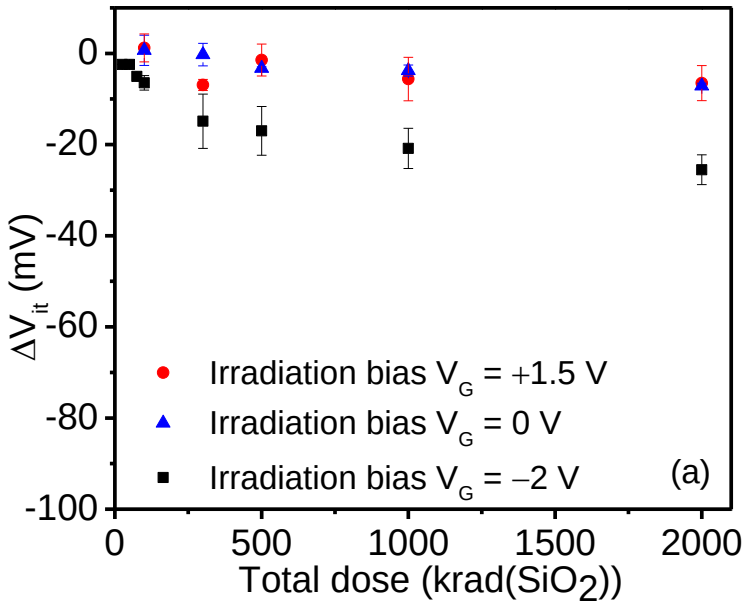
Fig. 4.6 plots the adjusted threshold shifts as a function of total dose for wide FinFETs having a gate length of 250 nm and fin width of 100 nm under the same bias conditions as for narrow FinFETs having a fin width of 50 nm. The negative bias configuration is again the worst-

case irradiation bias condition up to 2 Mrad(SiO_2). However, the threshold voltage shift (Fig. 4.6) for devices with a fin width of 100 nm is significantly larger than that of devices with 50 nm fin width (Fig. 4.5). That narrow fin devices exhibit reduced threshold voltage shifts as compared with wider fin devices in SOI FinFETs is commonly observed, which is usually attributed to the higher fringing electric fields and therefore enhanced charge yields that are observed in the wider fin devices [66],[67]. Given the already large applied electric fields in these devices, it seems unlikely that only fringing fields are responsible for the differences in Figs. 4.5 and 4.6, and differences in stress and therefore precursor defect density [68],[69] with fin width may be a more likely explanation. Despite the differences in overall charge trapping levels, the same relative differences are observed among the positive, 0 V, and negative bias irradiations, suggesting that these relative differences in response with applied bias are associated with differences in charge transport in the insulating layers of the gate stack.

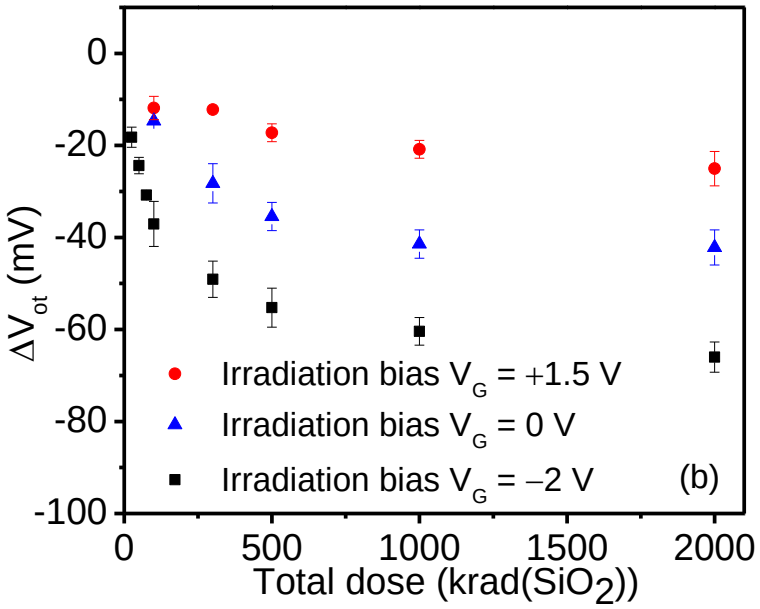
4.3 Discussion

In Figs. 4.7(a) and (b), values of ΔV_{it} and ΔV_{ot} are plotted for the devices of Figs. 4.5 and 4.6, respectively. The largest shifts for both ΔV_{it} and ΔV_{ot} are observed for negative-bias irradiation. HfO_2 is known to trap both electrons and holes efficiently during radiation exposure and/or high-field stress [64],[70],[71]. We first considered that the differences in radiation response with bias could be caused by differences in charge trapping in the buried oxide, as is commonly the case for triple-gate FinFET devices [66],[72],[73]. However, as discussed above, these devices are designed and fabricated to minimize the effects of both the top and back channels on device operation [55],[58], consistent with the I_D-V_G curves in Fig. 4.2. These show no back-channel leakage and very little subthreshold stretch-out, in contrast to devices with significant contributions from charge in the buried oxide to SOI FinFET radiation response

[66],[72],[73]. This again suggests that charge transport effects in the insulating layers of the gate stack lead to the observed differences in radiation response with differences in applied bias.

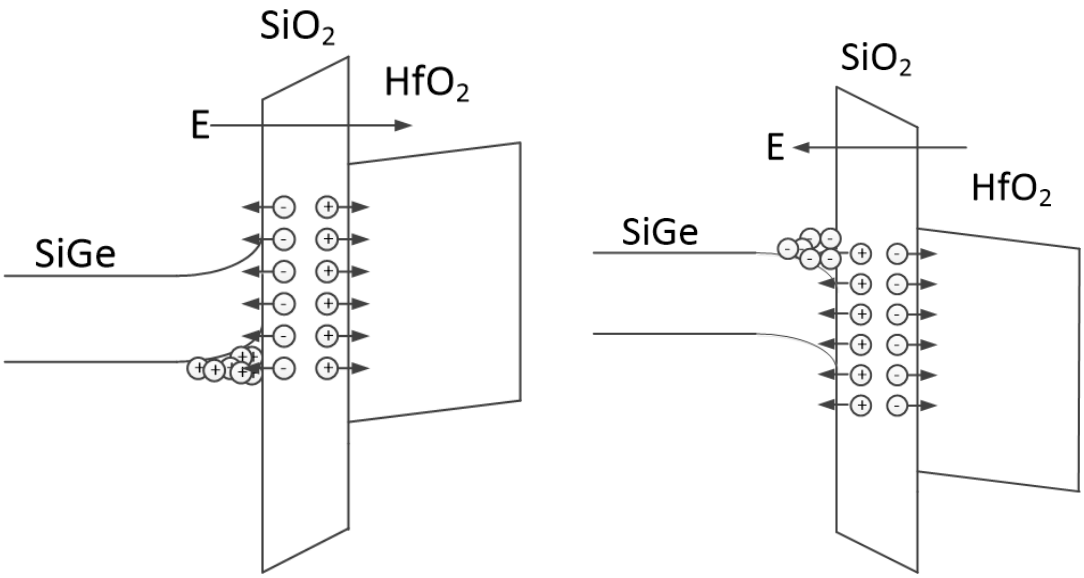


(a)



(b)

Fig. 4.7. (a) ΔV_{it} and (b) ΔV_{ot} as a function of total dose for devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm at room temperature. The gate biases applied during irradiation are +1.5 V, 0 V and −2 V. The effective interface- and oxide-trap charge densities for 2 Mrad(SiO_2) irradiation under worst-case negative bias are ~ 4×10^{11} cm^{-2} and ~ 9×10^{11} cm^{-2} in (a) and (b), respectively (after [56]).



(a) (b)

Fig. 4.8. Schematic energy-band diagram of a SiO_2/HfO_2/TiN gate stack under (a) −2 V and (b) +1.5 V gate bias. The radiation-induced electrons and holes can transport and become trapped in the defects located in the HfO_2 under electric field (after [56]).

The increase in net positive charge trapping in the negative bias case compared with the 0 V case suggests that the excess hole trapping observed during negative bias irradiation likely results from additional charge trapping in the HfO_2 due to radiation-induced holes that are generated in the SiO_2 and transport into the HfO_2. Similarly, during positive bias irradiation, radiation-induced electrons generated in the SiO_2 can transport into the HfO_2 and become trapped, leading instead to a less negative threshold voltage shift than observed for 0 V applied bias. This mechanism, depicted schematically in Fig. 4.8, and is consistent with the expected trapping responses of high-K dielectrics with relatively high electron and hole trap densities that overlie a SiO_2 layer with lower trapping densities [66],[70],[71]. It is also remarkably similar to the responses of thicker bilayer Si_3N_4/SiO_2 structures [74]-[76] that similarly pair an overlying material (Si_3N_4) that traps both electrons and holes efficiently with a SiO_2 layer with much lower trap density.

It is important to determine whether such a mechanism is plausible for these types of gate stacks with ultrathin SiO_2 layers. To do so, we estimate the percentage of radiation-induced electrons and holes $f_{e,h}$ generated in the ultrathin SiO_2 layer that would have to be trapped in the HfO_2 in Figs. 4.7 to account for the differences in response with radiation bias using the expression [77]:

$$f_{e,h} = \frac{\pm \Delta V_{e,h} \varepsilon_{ox}}{q \kappa_g f_y t_{ox}^2 D} \tag{4.1}$$

Here $\Delta V_{e,h}$ is the difference in threshold voltage shift due to excess electron or hole trapping as a result of the mechanism described above, ε_{ox} is the dielectric constant of SiO_2, $-q$ is the electronic charge, κ_g is the number of electron-hole pairs generated per unit dose in SiO_2 ($\sim 8.1 \times 10^{12}$ $cm^{-3} rad^{-1}(SiO_2)$), f_y is the charge yield of SiO_2, t_{ox} is the physical thickness of SiO_2 (~1 nm), and D is the total dose. We obtain first-order estimates of the values of $\Delta V_{e,h}$ by comparing the values of ΔV_{ot} at positive, negative, and 0 V bias in Figs. 4.5 and 4.6 for the narrow and wide fin width devices, respectively. Specifically, $\Delta V_e \approx (\Delta V_{ot})_{+1.5V\ bias} - (\Delta V_{ot})_{0V\ bias}$ and $\Delta V_h \approx (\Delta V_{ot})_{-2V\ bias} - (\Delta V_{ot})_{0V\ bias}$. The charge yield f_y is estimated as ~0.9 in the SiO_2 at large positive or negative electric fields from [18]. The dose enhancement factor is estimated to be 2.5 for a thin SiO_2 layer surrounded by TiN, HfO_2, and Si from [78]. Applying these assumptions to the 2 Mrad(SiO_2) data in Figs. 4.5 and 4.6, we estimate an effective value of (11 $\pm$ 3) % for f_h and (10 $\pm$ 2) % for f_e. These results are quite plausible when compared with trapping efficiencies observed in past studies of similar structures [79]. We emphasize that this calculation applies only to the *differences* in charge trapping that occur for different applied gate bias; a more comprehensive model of both positive and negative charge trapping would be required to characterize fully the electron and hole trapping in the insulating layers of these gate stacks, which is beyond the scope of the present study.

Finally, we note that the effective interface-trap buildup in these devices is smaller than the trapped-positive charge buildup, and is maximized for negative-bias irradiation. This suggests that the interface (or border) traps in these devices are not created via the release of hydrogen in the HfO_2 or SiO_2 layer, but may instead be due to hydrogen that is released from dopant atoms in the SiGe channel layer [80].

4.4 Summary of Chapter, and Conclusions

In this chapter, we report the irradiation and bias stress responses of SiGe *p*MOS FinFETs with HfO_2/SiO_2 gate dielectric stacks irradiated with 10 keV x-rays up to 2 Mrad(SiO_2). Experimental results suggest that negative bias irradiation leads to the worst-case degradation in the total dose response of SiGe *p*MOS FinFETs. We attribute this result to an increase in density of additional radiation-induced holes that become trapped in the HfO_2 under negative bias, and additional electron trapping under positive bias in the HfO_2, as compared with the 0 V irradiation case. A simple model of the structure suggests that these excess carriers originate in the near-interfacial SiO_2.

CHAPTER V

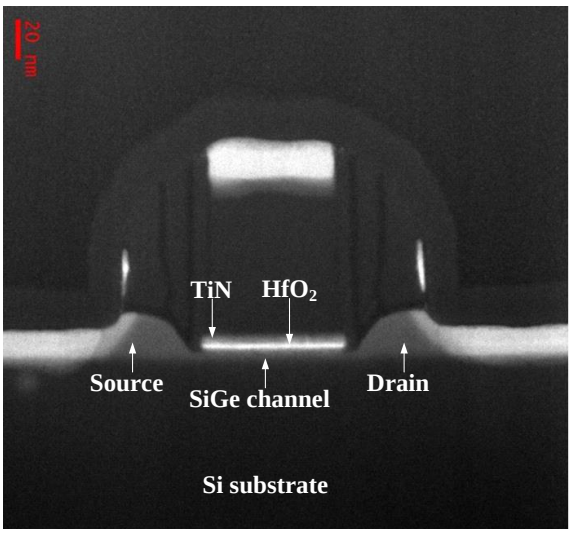
Negative bias temperature instability responses of SiGe *p*MOS devices

In this chapter, we investigate negative-bias temperature instabilities in planar SiGe *p*MOSFETs with SiO_2/HfO_2 gate dielectrics. The measured activation energies for interface-trap charge buildup during negative bias-temperature stress are lower for SiGe channel *p*MOSFETs with SiO_2/HfO_2 gate dielectrics and Si capping layers than for conventional Si channel *p*MOSFETs with SiO_2 gate dielectrics. Electron energy loss spectroscopy and scanning transmission electron microscopy images demonstrate that Ge atoms can diffuse from the SiGe layer into the Si capping layer, which is adjacent to the SiO_2/HfO_2 gate dielectric. Density functional calculations show that these Ge atoms reduce the strength of nearby Si-H bonds, and that Ge-H bond energies are lower still, thereby reducing the activation energy for interface-trap generation for the SiGe devices. Activation energies for oxide-trap charge buildup during negative bias-temperature stress are similarly small for SiGe *p*MOSFETs with SiO_2/HfO_2 gate dielectrics and Si *p*MOSFETs with SiO_2 gate dielectrics, suggesting that in both cases the oxide-trap charge buildup likely is rate-limited by hole tunneling into the near-interfacial SiO_2.

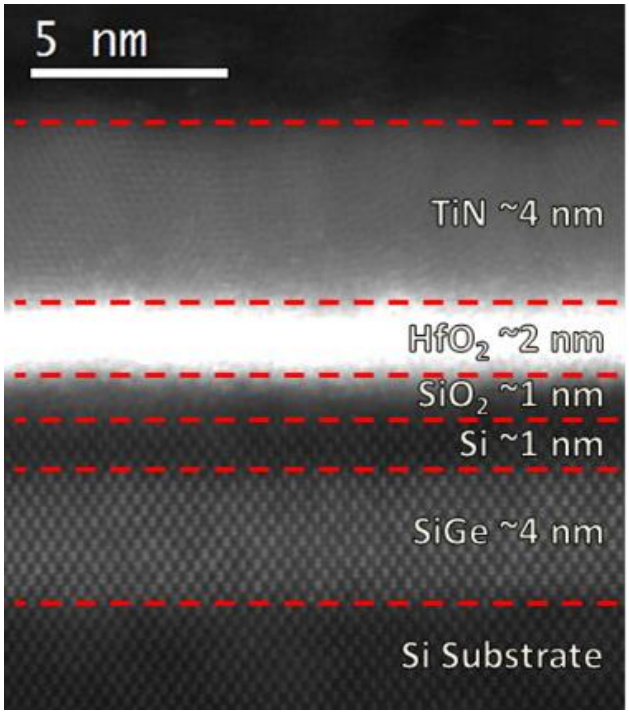
5.1 Experimental details

The MOSFETs used in this work were provided by IMEC. The $Si_{0.55}Ge_{0.45}$ *p*MOSFETs were fabricated on an *n*-type Si wafer with a 4.0 nm $Si_{0.55}Ge_{0.45}$ layer deposited onto a 2.0 nm Si buffer. On top of the 1.4 nm Si capping layer, a ~2 nm HfO_2 layer and TiN metal gate were deposited. A cross sectional scanning transmission electron microscope (STEM) image of the fabricated SiGe *p*MOSFET with HfO_2/SiO_2 gate dielectric is shown in Fig 5.1(a) (All STEM

images shown in this thesis are obtained by Jordan Hatchtel at Oak Ridge National Laboratory). The 1.4 nm Si cap was partially oxidized, yielding a ~1 nm SiO_2 interfacial layer (IL) and an unconsumed 1.0 nm thick Si capping layer to passivate the $Si_{0.55}Ge_{0.45}$ surface and improve the interface quality. A higher resolution STEM cross-sectional image, depicted in Fig. 5.1(b), provides an atomistic picture of the Si-capped SiGe MOS structure and different atoms distribution from the Si substrate to TiN metal gate. Fig. 5.1(b) clearly shows both an amorphous SiO_2 layer (~1 nm) and the unconsumed, crystalline Si capping layer (~1 nm). No crystal lattice dislocations from the Si substrate through the Si capping layer are observed in either image, indicating that the Ge alloyed layer thickness (~4 nm) has not exceeded the critical relaxation thickness and that the SiGe channel is strained [82]. Due to the valence-band offset between SiGe and the Si cap (band diagram is shown in Fig 5.2), inversion holes are confined in the SiGe channel, which therefore acts as an implant free quantum well (IFQW). The equivalent oxide thickness (EOT) of the gate dielectric stack is about 1.5 nm. For comparison of the charge trapping properties, Si *p*MOS FinFETs with 2 nm SiO_2 gate dielectrics with fin width of 65 nm and fin length of 250 nm [72] were also measured.



(a)



(b)

Fig. 5.1. (a) STEM of the structural composition of the SiGe-on-Si MOS structure. (b) High resolution (5 nm) STEM cross-sections are shown for a SiGe *p*MOSFET with HfO_2/SiO_2 gate dielectric. The 1.4 nm Si cap was partially oxidized, yielding a ~1 nm SiO_2 interfacial layer and an unconsumed 1.0 nm thick Si capping layer (after [81]).

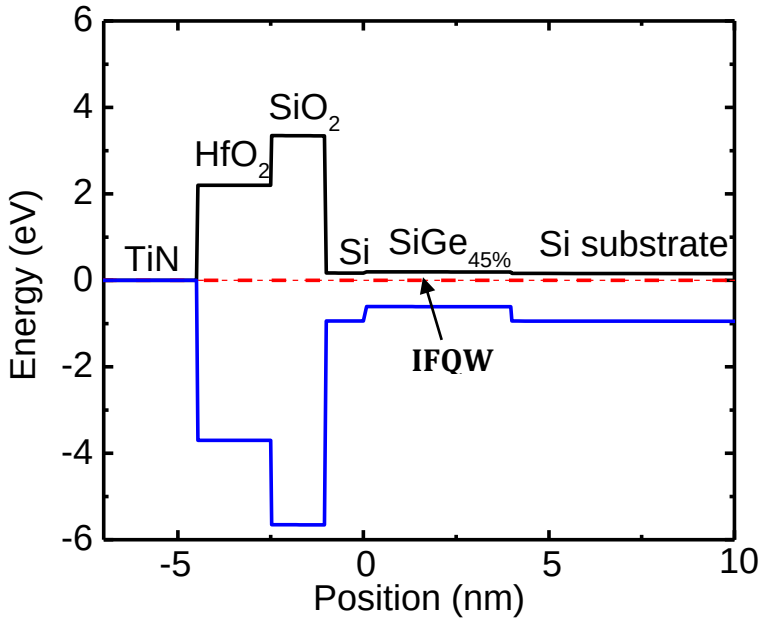


Fig. 5.2 Band diagram sketch of SiGe device(after [81]).

NBTI stress experiments were performed using the measure–stress–measure technique, as shown in Fig. 5.3. The $Si_{0.55}Ge_{0.45}$ and Si devices were stressed at electric fields (E_{ox}) of approximately −11.1 MV/cm and −10.3 MV/cm in the SiO_2, respectively (−2 V on the gate for the $Si_{0.55}Ge_{0.45}$ devices, and −2.5 V for the Si devices). This ensures that the critical, near-interfacial SiO_2 layers in both the Si and SiGe devices have similar electric fields during stress. Devices were stressed at temperatures from 125 ℃ to 250 ℃. Pre- and post-stress I_D-V_G curves were measured after devices were cooled to room temperature. Pre- and post-stress I_D-V_G curves were measured after devices were cooled to room temperature. Device characterization was performed in air with a HP 4156B Semiconductor Parameter Analyzer. During I_D-V_G measurement, the source-drain voltage V_{SD} was 50 mV, while the gate voltage was swept from 0.5 V to −1 V. At least five devices were measured for each case.

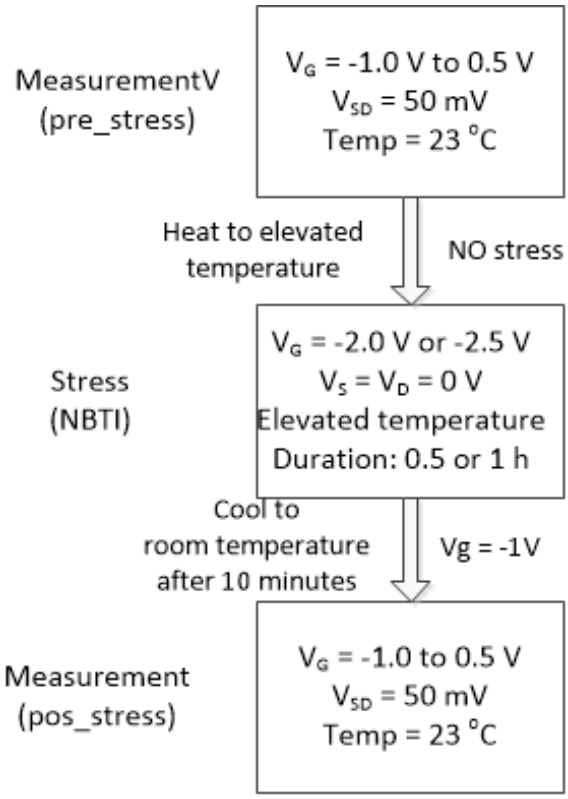
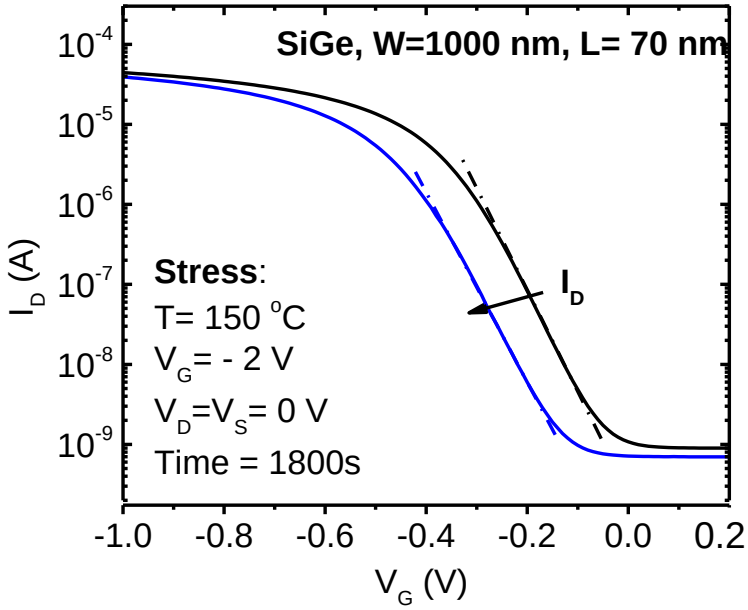
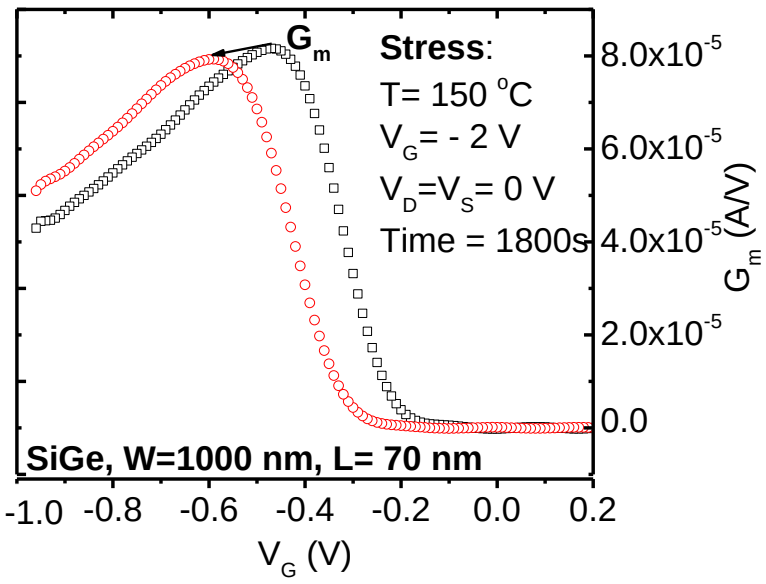


Fig. 5.3 NBTI experiment measurement flow chart.

5.2 Experimental Results and Analysis



(a)



(b)

Fig 5.4 (a) I_D-V_G and (b) G_m characterization as a function of gate voltage V_G measured at room temperature for a 1 μm × 0.07 μm $SiGe_{0.45}$ *p*MOSFET after 30 min stress time. The stress bias is −2 V on the gate and the stress temperature is 150 ℃ (after [81]).

Fig. 5.4 shows the I_D-V_G and transconductance G_m characteristics as a function of gate voltage V_G measured at room temperature before and after negative gate bias stress at -2 V. The I_D-V_G curves shift negatively after 30 min of negative gate bias, and the peak G_m is reduced with bias-temperature stress, which is due to the reduction of carrier mobility in the channel caused by charges trapped at (interface traps), or very close to (border traps), the Si/SiO_2 interface [59].

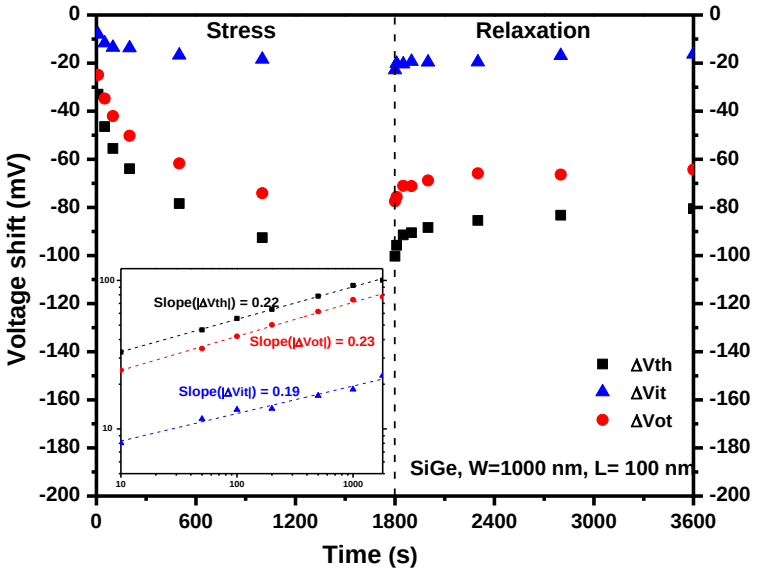
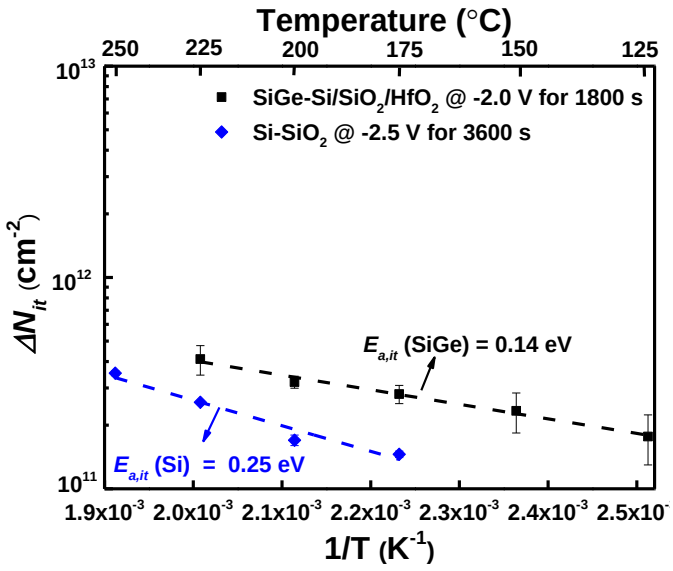
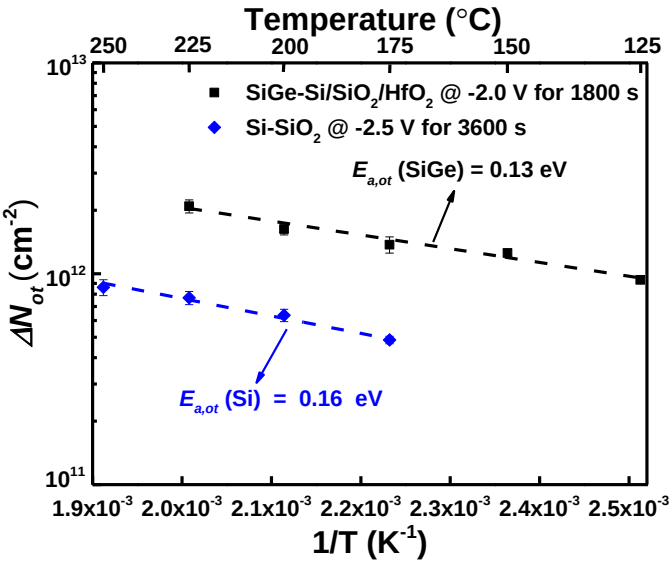


Fig. 5.5 Threshold voltage shift ΔV_{th}, as well as components due to oxide trap charge ΔV_{ot} and interface traps ΔV_{it}, as a function of stress time for $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with W/L = 1 µm/0.1 µm at 150 °C for V_{stress} = -2 V and $V_{relaxation}$ = 0 V. The inset shows stress time exponents for ΔV_{th}, ΔV_{ot} and ΔV_{it} (after [81]).

Threshold voltages due to oxide-trap ΔV_{ot} and effective interface-trap charge ΔV_{it}, estimated via the subthreshold swing technique as introduced in Chapter 2.1.4, are shown as functions of stress and recovery time in Fig. 5.5. The threshold voltage shift is mainly due to oxide-trap charge, with a smaller contribution from interface traps. The effective interface-trap charge density likely also includes contributions from fast border traps [59],[60]. The inset of Fig. 5.5 shows that V_{th} and its components due to oxide and interface trap charge have power law time t dependences; the $t^{\sim 0.21 \pm 0.02}$ time dependencies are similar to values observed for ΔV_{th} in previous work for $Si/SiO_2/HfO_2/TiN$ structures [83].



(a)



(b)

Fig. 5.6. Arrhenius plots of effective (a) interface trap generation $\Delta N_{it} = -C_{ox}\,\Delta V_{it}/q$ and (b) oxide trap charge $\Delta N_{ot} = -C_{ox}\,\Delta V_{ot}/q$ densities for $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with high-K dielectrics stressed at -11.1 MV/cm and for Si *p*MOSFETs with SiO_2 dielectric stressed at -10.3 MV/cm. Here C_{ox} is the capacitance of oxide layer, and q is the electronic charge. The SiGe devices with SiO_2/HfO_2 gate stacks show higher oxide-trap (~3x) and interface-trap (0.5 to 1.0x) charge densities than the Si devices with SiO_2 gate dielectrics, consistent with higher trap densities for devices with high-K gate stacks than with SiO_2 gate dielectrics (after [81]).

Fig. 5.6 shows changes of effective interface-trap and oxide-trap charge densities as functions of stress temperature for SiGe *p*MOSFETs and Si *p*MOS FinFETs. These devices were stressed with −2 V and −2.5 V on the gates, respectively. The activation energy values extracted from Arrhenius plots in Fig. 5.6(a) for effective interface-trap generation $E_{a,it}$ for the $Si_{0.55}Ge_{0.45}$ and Si *p*MOSFETs are 0.14 eV and 0.25 eV, respectively. The $E_{a,it}$ values for the Si *p*MOS FinFETs are similar to those reported for planar *p*MOS devices with SiO_2 gate dielectrics in the literature [84],[85]. The value of E_a for the interface-trap buildup in the $Si_{0.55}Ge_{0.45}$ structures is 45% lower than the value for the Si/SiO_2 structure. Such a large percentage difference will lead to significant differences in estimates of long-term reliability under typical device operating conditions for these structures. In contrast, the extracted activation energy for oxide-trap charge $E_{a,ot}$ is 0.13 eV for the $Si_{0.55}Ge_{0.45}$ *p*MOSFETs and 0.16 eV for the Si pMOSFETs, as shown in Fig. 5.6(b). Moreover, the SiGe device with the SiO_2/HfO_2 gate stack shows both higher oxide-trap (~3x) and effective interface-trap charge densities than the Si device with the SiO_2 dielectric. Higher trapped charge densities are observed, as expected, for devices with high-K gate stacks than for devices with SiO_2 gate dielectrics. Note that incorporation of Ge into the channel can significantly reduce NBTI degradation for devices with high-K gate dielectrics [86].

Similarly small activation energies for oxide-trap charge indicate that both cases likely are dominated by hole tunneling into defects (oxygen vacancies) in the near-interfacial SiO_2 and HfO_2 [87],[88], although a role for H^+ trapping [32] cannot be ruled out. Fig. 5.7 shows the band diagram for negative gate bias, including pre-existing oxygen vacancy energy levels in the near-interfacial SiO_2 and HfO_2 layers. In both structures, under high electric field conditions, holes from the channel tunnel into oxygen vacancies in the near-interfacial SiO_2. In SiO_2 devices, holes are trapped in *E′* defects (O vacancies) [21],[23],[32],[88]. The weak temperature dependence

and the similarities of the activation energies for the two types of structures in Fig. 5.6(b) suggest that the hole injection into the near-interfacial SiO_2 via tunneling is most likely the rate limiting step in this process, since the energy levels of defects in HfO_2 and SiO_2 are quite different, in general [70],[90]. In the $Si_{0.55}Ge_{0.45}$ *p*MOSFETs, holes that would otherwise transport across the ultrathin SiO_2 without becoming trapped may instead become trapped in the HfO_2 [86],[88]. This will lead to a more negative shift in threshold voltage, but similar trapping kinetics, as long as hole injection is the rate limiting step in each case.

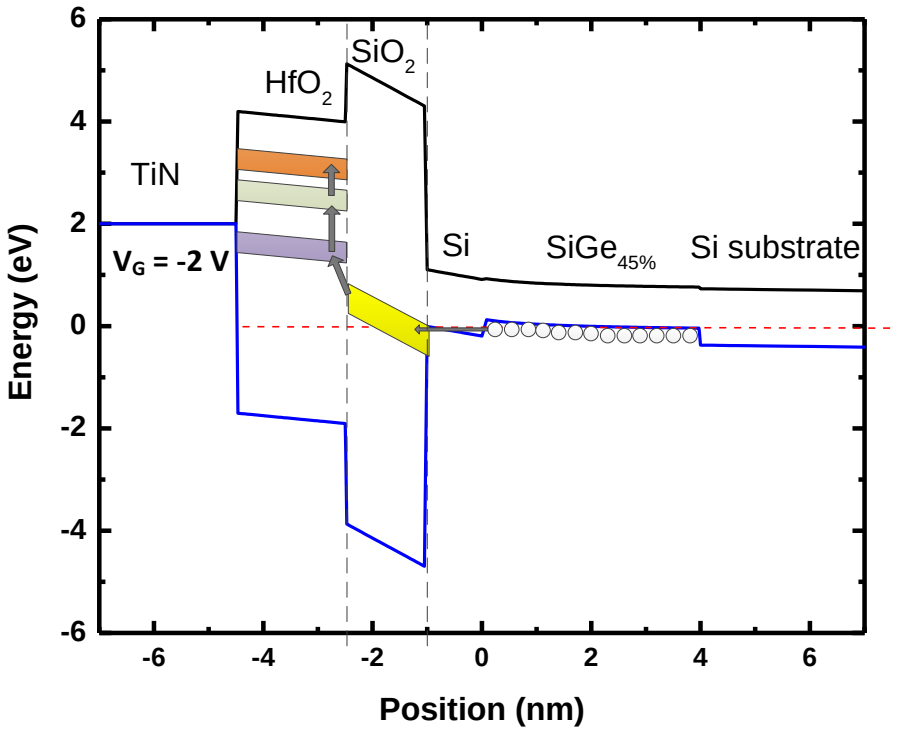


Fig. 5.7. Schematic diagram for negative gate bias in SiGe *p*MOSFETs, including different defect bands associated with oxygen vacancies in the interfacial layer and HfO_2 (after [70],[86]).

It has been shown that the interface trap generation observed at measuring times comparable to those in this work in Si MOS transistors during NBT stress is governed by the depassivation of interface Si-H bonds [85]. Tsetseris et al. [32] performed density functional calculations which showed that Si-H bonds cannot be broken by direct hole capture from the

substrate. However, these bonds can be broken through direct reaction with protons ($\mathrm{Si-H+H^+ \rightarrow Si^+ + H_2}$) that are released from dopants in the semiconductor and drift under negative bias toward the semiconductor-dielectric interface [32],[91]. Here $\mathrm{Si^+}$ denotes a positively charged Si dangling bond. At temperatures above 100 ℃, the balance of the reaction is controlled by the diffusion of the product $\mathrm{H_2}$. The activation energy E_a for interface trap generation is $E_a = \frac{1}{2}\Delta E + \frac{1}{4}\phi_D$, where ΔE is the reaction energy of the depassivation process and ϕ_D is the diffusion barrier of $\mathrm{H_2}$ in $\mathrm{SiO_2}$ [32],[91],[92]. Assuming the diffusion barrier of $\mathrm{H_2}$ in $\mathrm{SiO_2}$ is the same in the Si capped SiGe MOS and Si MOS structures, the 0.11 eV difference in the E_a for interface trap generation, as shown in Fig. 5.6(a), suggests that, on average, the reaction energy ΔE for the Si capped SiGe MOS structure is 0.22 eV lower than that for the Si MOS structure. As shown below, this reduction of reaction energy occurs because Ge atoms are present in the Si capping layer.

STEM provides an atomistic picture of the Si-capped SiGe MOS structure and Ge distribution. Annular bright field (ABF) and high angle annular dark field (HAADF) images obtained using an aberration-corrected STEM operating at 200 kV are shown in Figs. 5.8(a) and (b), which clearly show both an amorphous $\mathrm{SiO_2}$ layer (~1 nm) and the unconsumed, crystalline Si capping layer (~1 nm). No crystal lattice dislocations from the Si substrate through the Si capping layer are observed in either image, indicating that the Ge alloyed layer thickness (~4 nm) has not exceeded the critical relaxation thickness and that the SiGe channel is strained [82]. Aligning two-dimensional spectral images of the chemical concentrations of O, Ge, and Si and their integrated intensities obtained via electron energy loss spectroscopy (EELS) with the STEM images, as shown in Figs. 5.8(c)-(f), we can determine the chemical content in each layer. Figs.

5.8(d) and (f) both a strong Ge EELS signal throughout the capping layer and partially within the oxide layer, confirming a significant amount of Ge diffusion into the cap during device processing [93].

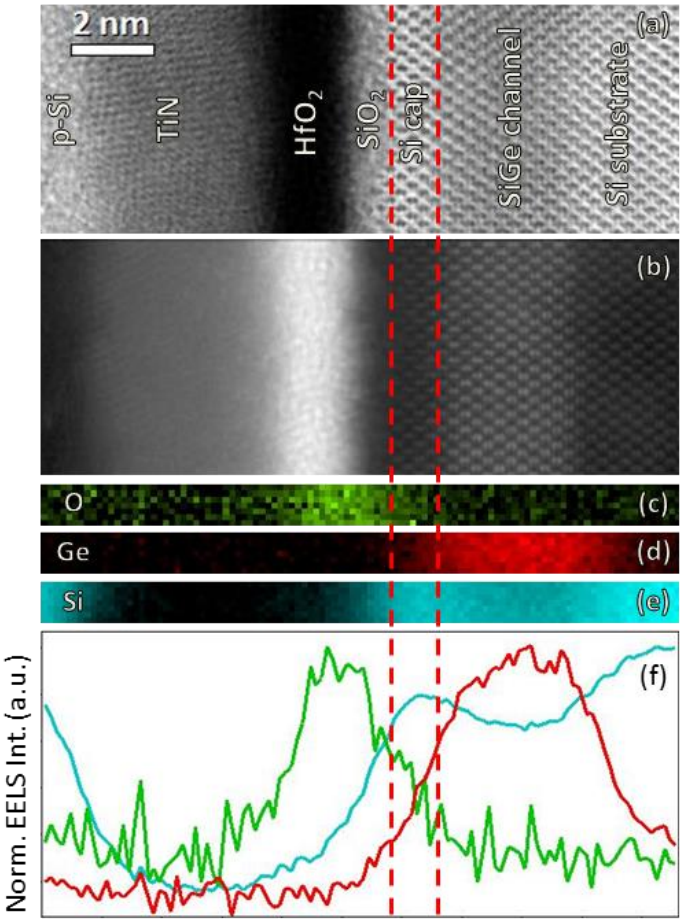


Fig. 5.8. Scanning transmission electron microscope analysis of structural composition. Annular (a) bright and (b) dark field images of the structure. The lack of interfacial misfit dislocations shows that the crystal lattices in the channel and capping layer have not expanded due to the Ge, but are instead strained. Two dimensional elemental maps of the device are shown in (c)-(e). The electron energy loss spectra (EELS) for O (c), Ge (d), and Si (e) are shown across same regions in (a) and (b). The EELS intensities from (c)-(e) are vertically summed in (f), normalized to the maximum value for each element, and then plotted jointly. There is significant Ge diffusion into the Si capping layer, all the way up to the oxide layer (after [81]).

Density functional calculations [94] show that, on the hydrogenated SiGe surface, the presence of Ge can reduce the reaction energy and barrier of hydrogen desorption from the surface. Here we evaluate the effects of near-interface Ge on the reaction energy ΔE of hydrogen depassivation ($Si-H+H^+ \rightarrow Si^+ + H_2$) at the Si/SiO_2 interface. The calculations were done by Xiao Shen who was from Department of Physics and Astronomy at Vanderbilt University and now an associate professor in University of Memphis using an interface model of a ($2\sqrt{2}\times 2\sqrt{2}$) unit cell of Si (100) surface constructed by a Monte-Carlo bond-switching method [95]. The model consists of a slab of crystalline Si with a thickness of 17 Å and an amorphous SiO_2 layer with a thickness of 13 Å. At the interface, there is one Si dangling bond passivated by a H atom, as shown in Fig. 5.9(a). The calculations use the Perdew-Burke-Ernzerhof (PBE) [96] version of exchange-correlation functional, projector augmented wave (PAW) potentials [97], and planewave basis as implemented in the VASP (Vienna ab initio simulation package) code [98]. The planewave kinetic energy cutoff is 283 eV. The structural relaxations are converged to 10^{-3} eV for the total energy difference between two ionic steps. A single k-point at (0.25, 0.25, 0.25) is used for Brillouin zone sampling.

We first compute the reaction energy ΔE at the Si/SiO_2 interface without Ge, as shown in Fig. 5.9(a). The initial and final states of the reaction are shown in Figs. 5.9(b) and 4.9(c). A reaction energy ΔE of 0.44 eV is obtained, which is in good agreement with the value of 0.5 eV from a previous study [99]. Calculations show that, when the Si atom in the Si-H bond has a Ge neighbor, as shown in Fig. 5.9(d), the reaction energy ΔE is reduced by 0.10 eV. When the Ge atom replaces the Si atom in Si-H bond, as shown in Fig. 5.9(e), the reaction energy ΔE is reduced by 0.51 eV and becomes negative. The large reduction of reaction energy for depassivating a Ge-H bond compared to a Si-H bond suggests that having Ge exposed near the

interface can pose potentially significant reliability concerns, which highlights the importance of the Si capping layer employed in these devices. The observed reduction of 0.22 eV in ΔE (0.11 eV in E_a) is likely the averaged value of depassivation from a majority of Si-H bonds with Ge neighbors and from a small number of Ge-H bonds directly at the interface.

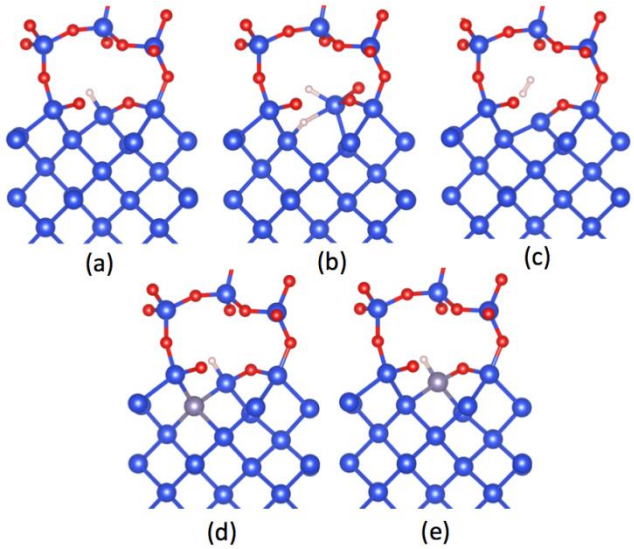


Fig. 5.9. Models of the Si/SiO_2 interface for calculating the reaction energies (blue: Si, red: O, white: H, grey: Ge): (a) an interface model with an Si-H bond; (b) the initial configuration of the depassivation reaction with an H^+ at the vicinity of the Si-H bond; (c) the final configuration of the depassivation reaction with a H_2 molecule and a Si dangling bond; (d) an interface model with an Si-H bond similar to (a), with the Si atom in the Si-H bond having a Ge neighbor; (e) an interface model similar to (a), with a Ge atom replacing the Si atom in Si-H bond (after [81]).

5.3 Conclusion of Chapter

In summary, positive oxide-trap charge trapping is the dominant defect responsible for NBTI in $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with high-K dielectrics. The experimental results show similarly small values of E_a for oxide-trap charge buildup, while E_a is lower for interface-trap buildup in the *p*MOSFETs with $Si_{0.55}Ge_{0.45}$ channel and high-K gate stacks, compared to the Si channel devices with SiO_2 gate dielectrics. The similar activation energies for oxide-trap charge

in these two structures suggests that hole injection into the near-interfacial SiO_2 via tunneling is evidently the rate-limiting process for oxide-trap charge buildup during negative-bias stress. Electron energy loss spectroscopy shows the presence of Ge atoms in the Si capping layer. First-principles calculations show that Ge atoms near the Si/SiO_2 interface are primarily responsible for the reduced activation energies for interface traps in the SiGe *p*MOS devices, as compared with the Si *p*MOS devices.

CHAPTER VI

Low-frequency 1/*f* noise in SiGe *p*MOSFETs

This chapter explores the low-frequency 1/*f* noise on $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with a SiO_2/HfO_2/TiN gate stack. Low-frequency 1/*f* noise measurements can provide insight into the density and energy distributions of defects in gate dielectrics in a wide range of applications [49],[50],[100]-[104]. It has been demonstrated that the 1/*f* noise of *p*MOS devices with SiO_2, oxynitride, and/or high-K dielectric layers increase with negative-bias-temperature stress [104]-[110]. To date, most of these noise measurements have been performed at room temperature, which limits the amount of information that can be obtained about defect densities and energies to a narrow range of energy levels. In our experiment, we extend the available temperature range from 100 K to 450 K, which is essentially the regular operation temperature of MOS transistors, corresponding to 0.26 eV to 1.13 eV of observable energy window contributing to NBTI. Fig. 6.1 shows low-frequency 1/*f* noise measurements as a function of temperature (100-440 K) for devices with or without negative-bias-temperature stress (NBTS) for $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with a Si capping layer and SiO_2/HfO_2/TiN gate stack. Clearly, the lower-temperature noise is relatively unchanged by NBTS, but the higher-temperature noise is changed significantly. In this chapter, we describe the devices, experimental test conditions, and analysis of a series of experiments that were performed to obtain insight into the underlying defects responsible for the device degradation and increased low-frequency noise in these devices. The results suggest a significant role for hydrogen-related defects in the near-interfacial SiO_2/HfO_2 dielectric layers, and provide insight into the densities and energy levels of these defects.

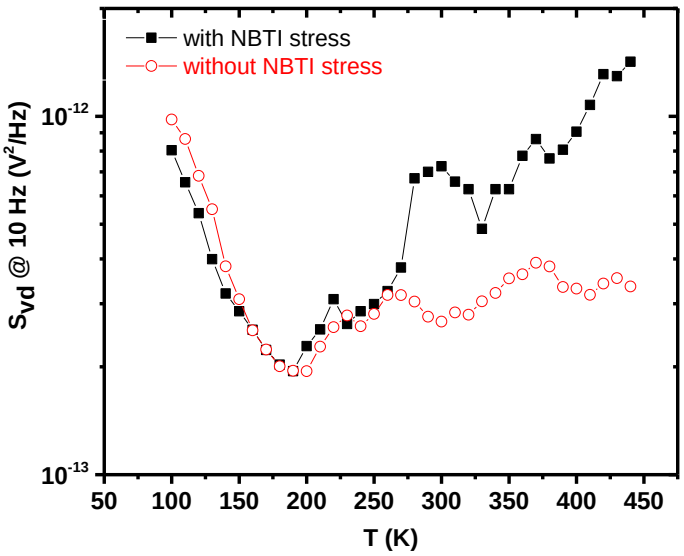


Fig. 6.1. Noise magnitude S_{vd} at f = 10 Hz as a function of temperature from 100 K to 440 K for a SiGe *p*MOSFET with a Si capping layer and SiO_2/HfO_2 gate dielectric. The stressed device was held at a constant gate bias of -2 V for ~ 10 min at each successively higher temperature before noise measurements were performed. The unstressed device was held with all pins grounded for a similar amount of time at each successively higher temperature. During the noise measurement, the transistor was biased at V_D = −50 mV and V_{GS}-V_{th} = −0.6 V.

6.1 Experimental Details

The information on devices used in the noise measurement refers to that in Chapter 4.1. Figs. 5.8(c) and 3(f) both show a weak oxygen EELS signal throughout the interfacial layer SiO_2 and at the SiO_2/HfO_2 interface, confirming a relatively high density of oxygen vacancies in those regions. The wafers were first diced to individual dies. Then the diced die, containing the isolated SiGe *p*MOSFETs, was mounted on a high speed package which has a good contact with the stage of bonder. The package, mounting the device under study (DUT), was removed from the stage and put in an electro-static discharge (ESD) proof box every time when the bonder needs to generate a ball at the tip of gold wire by sparkling. This was to ensure the survival of devices from possible transient spikes or ESD during sparking. A grounded wrist strap was

always used while handling the devices.

Packaged $Si_{0.55}Ge_{0.45}$ devices were stressed at electric fields (E_{ox}) of approximately −11.1 MV/cm in the SiO_2 (−2 V on the gate) for fixed duration of 10 min at temperatures from 100 K to 440 K in a vacuum cryostat with an automatic temperature controller. I_D-V_G curves were measured before and 5 min after stress to allow recovery of the fast component of negative-bias-temperature instability (NBTI), so that NBTI degradation remains almost constant during I_D-V_G and 1/*f* noise measurements. Device DC characterization was performed in vacuum with a HP 4156B Semiconductor Parameter Analyzer. During I_D-V_G measurement, the source-drain voltage V_{SD} was −50 mV, while the gate voltage was swept from 0.5 V to −1 V. Low frequency 1/*f* noise measurements were performed in the linear mode of device operation using the setup in Fig. 6.2 [111], before and after NBTI stress.

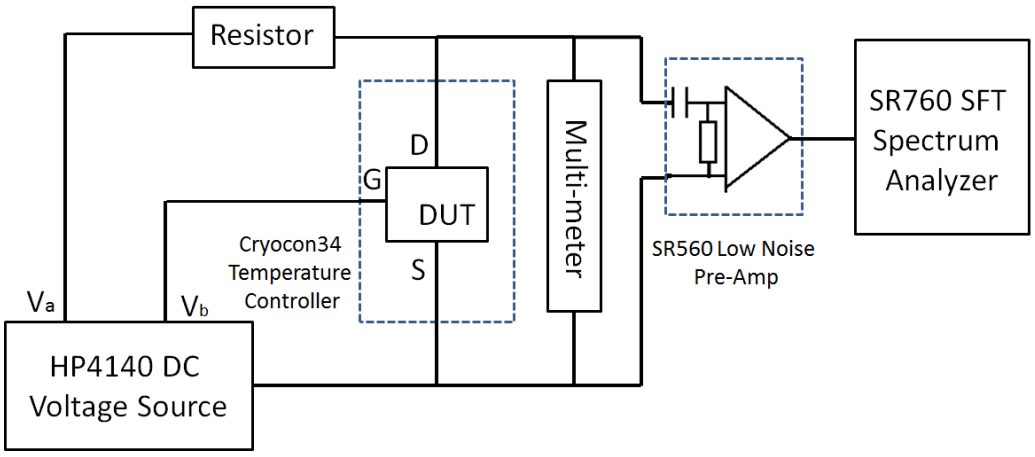


Fig. 6.2. Low frequency 1/*f* noise measurement setup. (After Xiong et al. [111].)

6.2 Experimental Results and Analysis

6.2.1 Temperature dependence of 1/f noise without stress

Drain voltage noise power spectral densities (V^2/Hz) for a SiGe *p*MOSFET with a gate width W = 1 μm and gate length L = 0.47 μm were measured from 100 K to 440 K in steps of 10

K. During the noise measurement, the transistor was biased in the linear mode of device operation at each temperature with constant V_D = -50 mV and V_{GS}-V_{th} = -0.6 V. Fig. 6.3 shows the PSD of signal noise measured at -50 mV drain bias and background noise measured at 0 V drain bias at 300 K. The background noise is usually caused by thermal noise and shot noise. Fig. 6.4 shows excess noise S_{vd} spectra with the background noise subtracted at different temperatures. The inset of Fig. 6.4 shows the threshold voltage of an unstressed device as a function of temperature. The threshold voltage was measured from the I_D-V_G curve at each temperature to ensure that V_{GS}-V_{th} was held constant for all noise measurements, to ensure a constant surface potential. We fit excess S_{vd} curves similar to those in Fig. 6.4 for f = 5 Hz to 40 Hz to extract the frequency exponent α (Eqs. (3.5)), as well as the value of $\partial \log S_{vd}/\partial \log f$ (Eq. (3.4)). For these devices and measurement conditions, S_{vd} was observed to be of the "generic" $1/f^{\alpha}$ type. The extracted frequency exponent α varies between 0.7 and 1.1 for the devices of Fig. 6.4. The results in Fig. 6.4 (and those that follow) are representative of three nominally identical devices that showed similar results.

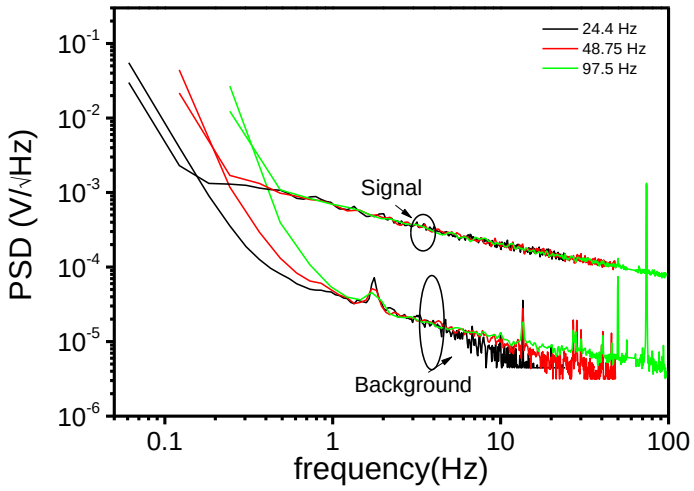


Fig. 6.3. Log-log plots of PSD of signal and background vs. frequency at 300 K with 0 V stress during heating. The signal noise is measured in the linear region of device operation, with V_{DS} = -50 mV and V_{GS}-V_{th} = -0.6 V. The background noise is measured with V_{DS} = 0mV and V_{GS}-V_{th} = -0.6 V.

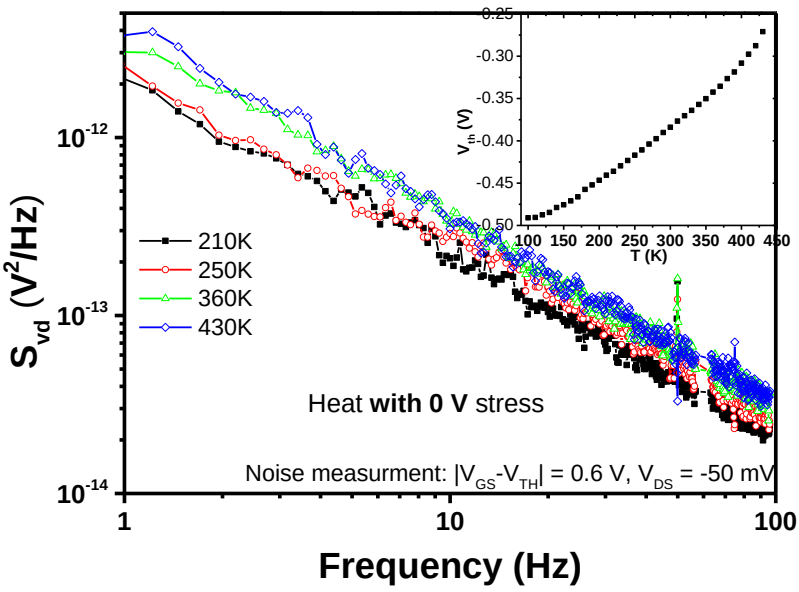


Fig. 6.4. Log-log plots of excess voltage noise power spectral density S_{vd} vs. frequency in a temperature of 100 K to 440 K with 0 V stress during heating. The noise is measured in the linear region of device operation, with V_{DS} = -50 mV and V_{GS}-V_{th} = -0.6 V. The inset shows the threshold voltage as a function of temperature for fresh device. We measured the threshold voltage from I_D-V_G curve at each temperature point to ensure that V_{GS}-V_{th} was constant during the measurement of the temperature dependence of the 1/*f* noise.

Fig. 6.5 shows the excess drain voltage noise power spectral density (left hand scale) and frequency exponent α (right hand scale) for the unstressed device of Fig. 6.4. Both the noise magnitude S_{vd} at 10 Hz and frequency dependence between 5 Hz and 40 Hz vary strongly with temperature. Excellent agreement is observed between the measured values of α (Eq. (3.5)) and predicted values obtained from Eq. (3.4) over the entire temperature region. For these calculations, the attempt time τ_0 was estimated to be 1.8×10^{-15} s, consistent with previous studies of MOS devices [49],[112],[113]. This confirms the applicability of the Dutta-Horn model of 1/*f* noise to these devices, and demonstrates that the noise is due to a random thermally activated process having a broad distribution of energies [48],[49],[53],[54]. This and studies of the temperature dependence of the noise in other MOS devices essentially rule out simple tunneling models, in which the rate-limiting steps in the 1/*f* noise of these MOS transistors were primarily

due to charge carriers tunneling into and out of traps in the oxide [49],[53],[114],[115]. The agreement between experimental data and the Dutta-Horn model allows us to estimate defect energy distributions $D(E_o)$ via Eq. (3.6), as we will discuss in Chapter 3.3.

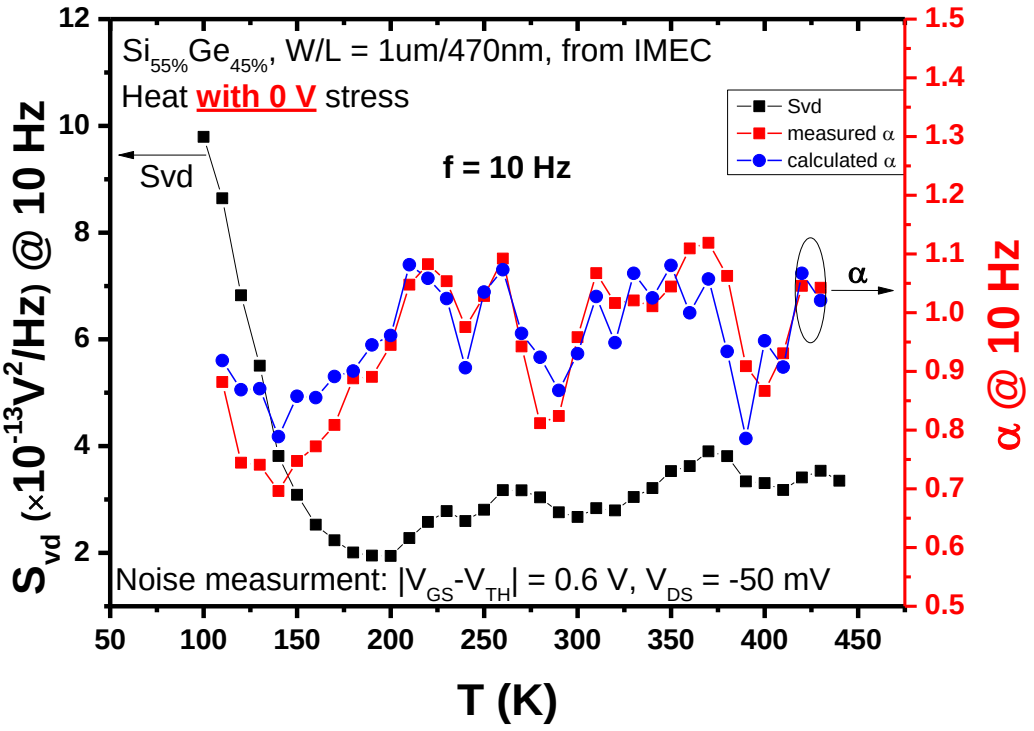


Fig. 6.5. S_{vd} at 10 Hz (left axis) and spectral slope α at 10 Hz as a function of temperature [right axis: red squares denote measured data, and blue circles denote calculated values from Dutta-Horn analysis via Eq. (3.4)].

6.2.2 Temperature dependence of 1/f noise with -2 V stress

Fig. 6.6 shows excess noise spectra S_{vd} at different temperatures on the same device used in Fig. 6.4, but now with NBTS applied. The noise measurement conditions were similar to those of Fig. 6.4, except the device was stressed at a constant gate bias of -2 V for approximately 10 minutes between successive noise measurement as the device was heated from 100 K to 440 K. I_D-V_G curves were measured before and 5 minutes after stress to allow recovery of the fast component of NBTI degradation before V_{th} and 1/f noise measurements. A comparison of Figs. 6.4 and 6.6 shows that the threshold voltage of the device was modified by NBTS at higher

temperatures (insets), and the noise magnitude also significantly increases at higher temperatures. Fig. 6.1 above presents the comparative results of the noise measurements of Figs. 6.4 and 6.6, showing similar levels of noise at lower temperatures in stressed and unstressed devices, but significantly higher levels of noise for stressed devices at elevated temperatures. At ~ 430 K, for example, the noise of the stressed device is ~ 3× larger than that of the unstressed device. Because the noise of the unstressed device varies only weakly with temperature from ~ 260 K to ~ 430 K, we conclude that the increased noise in the stressed device results primarily from defects that are created by the NBTS.

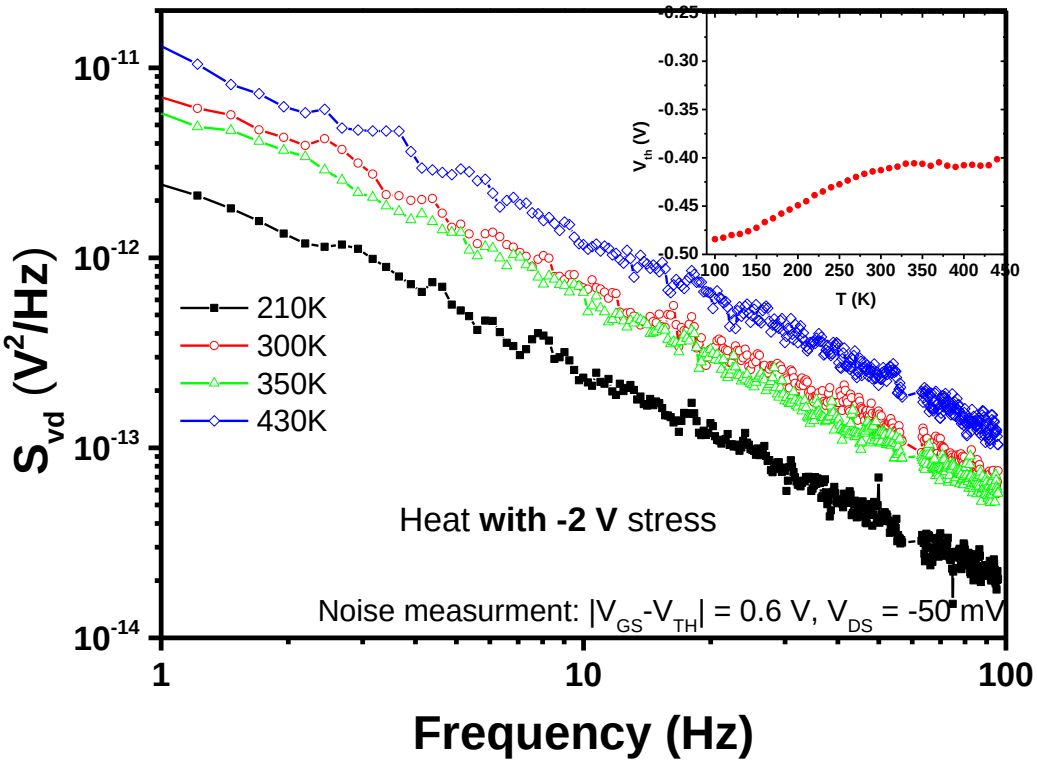


Fig. 6.6. Log-log plots of excess voltage noise power spectral density S_{vd} vs. frequency at four temperatures, for the device of Fig. 6.4, now subjected to NBTS. The noise is measured in the linear region of device operation, with V_{DS} = -50 mV and V_{GS}-V_{th} = -0.6 V. The inset shows the threshold voltage as a function of temperature for the stressed device. We measured the threshold voltage from an I_D-V_G curve at each temperature point to ensure that V_{GS}-V_{th} was constant during the measurement of the temperature dependence of the 1/*f* noise.

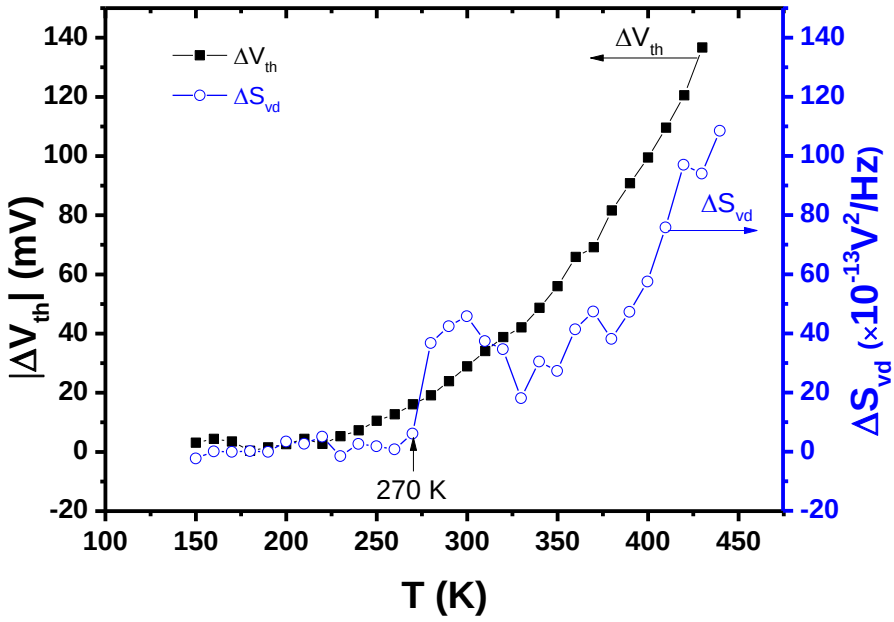


Fig. 6.7. Absolute values of threshold voltage shifts (left axis) and noise magnitude shifts at 10 Hz (right axis) versus temperature for stressed devices (Fig. 6.6), relative to the values for unstressed devices (Fig. 6.4). The solid curves are guides to the eye through the measured data.

Fig. 6.7 further compares the changes in noise and threshold voltage that are caused by NBTS in Figs. 6.1, 6.4, and 6.6. Here $\Delta S_{vd} = S_{vd,stressed} - S_{vd,unstressed}$, and $\Delta V_{th} = V_{th,stressed} - V_{th,unstressed}$. The magnitude of the change in threshold voltage with NBTS ΔV_{th} increases monotonically with increasing temperature, indicating an increase in the number of donor-like traps [42],[81],[106]-[110],[116]-[118]. The change in excess drain voltage noise power spectral density shift with NBTS ΔS_{vd} also tends to generally increase with temperature after NBTI stress. However, in contrast to the changes in V_{th}, the changes in S_{vd} are not strictly monotonic. There are two possible reasons for this non-monotonicity in ΔS_{vd}. The first is that, at least over a relatively small temperature range, some defects that lead to a significant amount of noise that are created at lower temperatures may anneal out thermally as the device is heated [49],[50],[106]-[108]. The second possibility is that defects are being created by NBTS that have a much more sharply peaked defect energy distribution than the defects introduced by device

processing [49],[50],[111],[112]. Each of these is quite plausible, as it is quite likely that both the defect density and energy distribution are changing as the device is subjected to NBTS [42],[106]-[108],[116]-[118], consistent with what happens when a device is exposed to ionizing radiation and then is annealed at elevated temperature [27],[49]-[51],[60],[111],[112],[119].

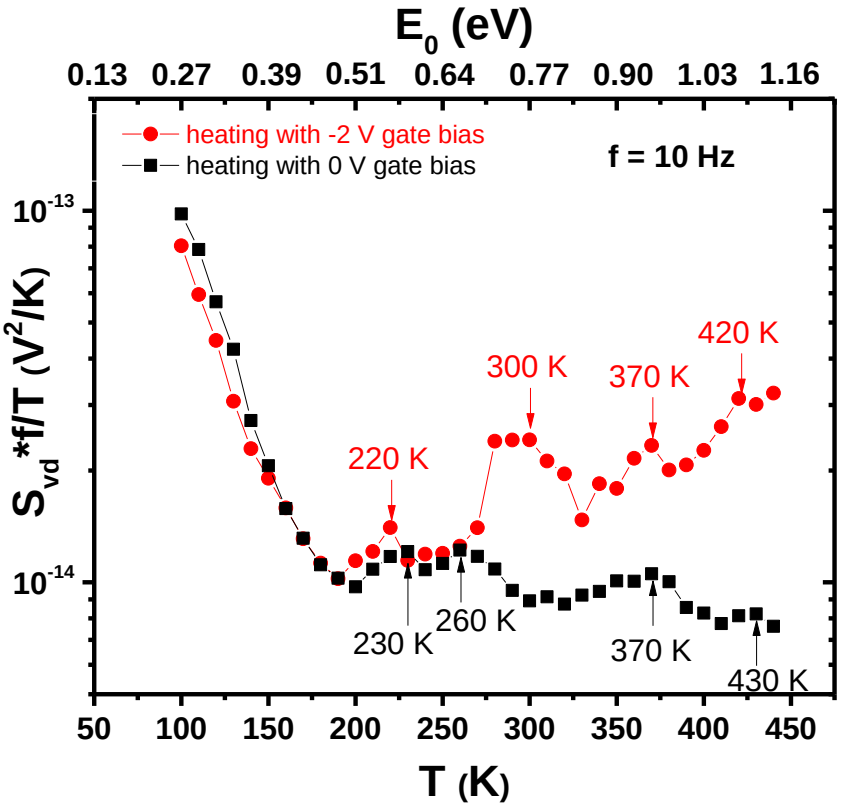


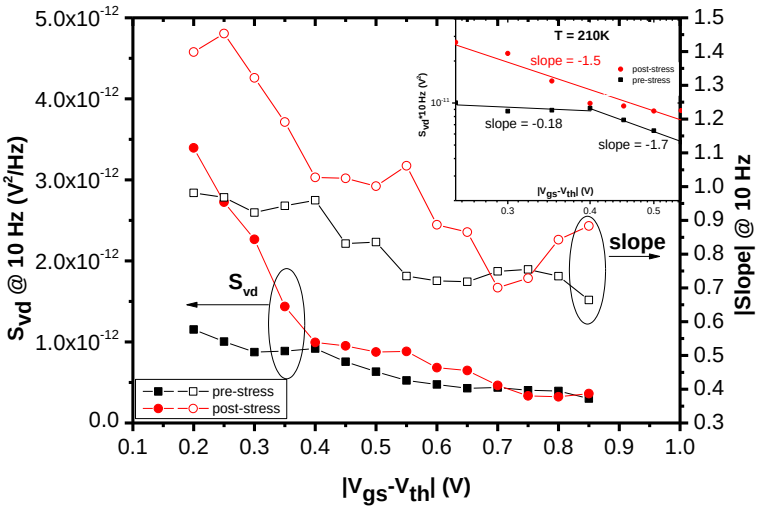
Fig. 6.8. Temperature dependent noise measurements at f = 10 Hz as a function of temperature ranging from 100 K to 440 K (bottom x-axis) before and after NBTI stress. The noise is measured under the same conditions as in Figs. 6.4 and 6.6. The temperature range corresponds to an energy barrier scale ranging from 0.26 eV to 1.13 eV (top x-axis). The concentration of defects increased significantly at energy barrier levels of ~ 0.77, ~ 0.95 and ~ 1.1 eV after the device was stressed at -2 V.

We now apply the Dutta-Horn model to estimate defect-energy distributions $D(E_o)$ in SiGe pMOSFETs with SiO_2/HfO_2 gate dielectric stack via Eq. (3.6). In Fig. 6.8, we plot $S_{vd}f/T$ (proportional to $D(E_o)$) at f = 10 Hz as a function of temperature from 100 K to 440 K (bottom x-

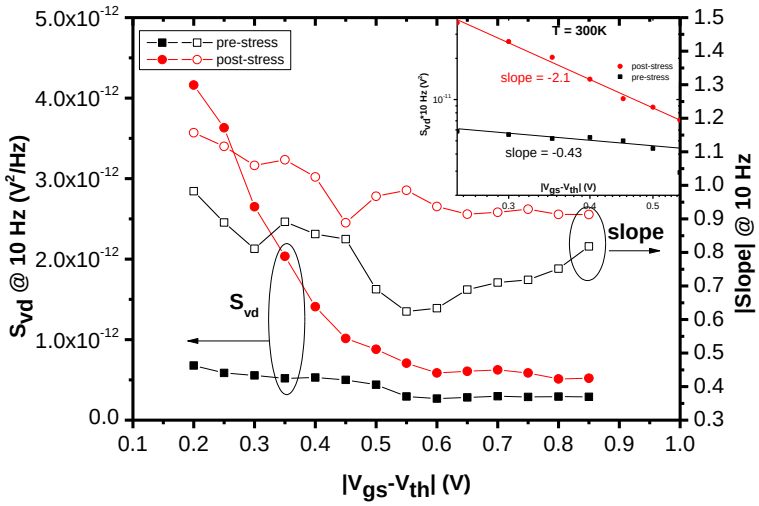
axis) and energy E_o via Eq. (3.7) from 0.26 eV to 1.13 eV (top x-axis). Before stress, the fresh device shows a large peak at low temperatures, and four smaller peaks in the defect-energy distribution at ~ 230 K (0.6 eV), ~ 260 K (0.65 eV), ~ 370 K (0.95 eV) and ~ 430 K (1.1 eV). The uncertainty in the inferred E_o at each peak is ~ 0.025 eV due to the 10 K temperature increment. The stressed device shows all of these peaks and a new peak at ~ 300 K (0.75 eV). The magnitudes of the peaks at ~ 300 K, ~ 370 K, and ~ 430 K increase significantly with NBTS, while the lower energy peaks are affected less. The values of E_o at higher energies (in the range 0.5–1.2 eV) inferred from the temperature dependence of the low-frequency 1/*f* noise of the stressed devices in Fig. 6.8 are quite consistent with the activation energies of individual defects in other devices with similar near-interfacial gate dielectric layers measured by other techniques, e.g., time dependent defect spectroscopy (TDDS) [117],[118].

6.2.3 Gate voltage dependence of low-frequency 1/f noise

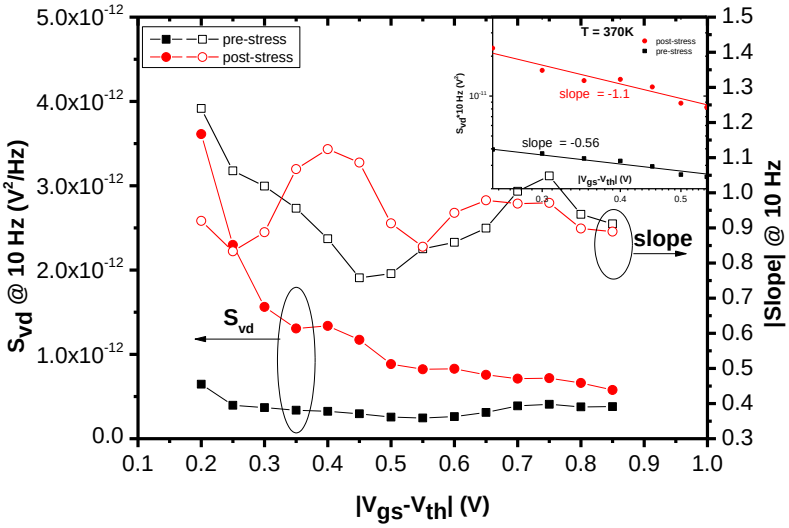
As illustrated by the temperature dependence of the noise magnitude in Fig. 6.5, demonstrating the thermally activated nature of low-frequency noise, defects responsible for low-frequency noise in *p*MOSFETs are not usually distributed uniformly in energy and/or space. For thermally activated noise, it is not as easy to infer the spatial distribution of the defects, but varying the gate bias enables one to probe different regions of the Si/SiO_2 band gaps and provides useful and complementary information to varying the temperature [114]. If a peak exists in a non-uniform defect energy distribution, then varying the voltage also leads to a corresponding peak in noise vs. gate voltage, as following reasons: only traps near the Si/SiO_2 interface and within a few *kT* of the quasi-fermi level communicate with the silicon; The fermi level changes with temperature while the trap energy levels move (relative to the fermi level) with gate voltage.


T = 210K
slope = -1.5
slope = -0.18
slope = -1.7
post-stress
pre-stress
S_{vd}
slope
pre-stress
post-stress
S_{vd} @ 10 Hz (V^2/Hz)
|Slope| @ 10 Hz
$|V_{gs}-V_{th}|$ (V)

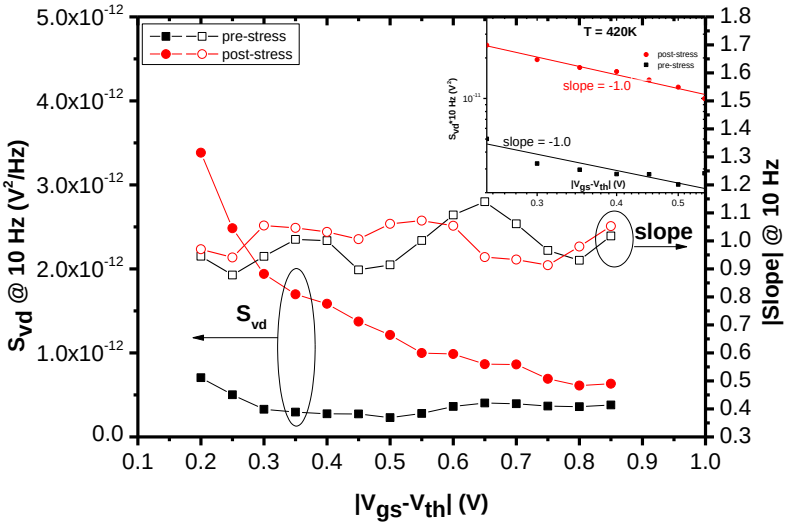
(a)


T = 300K
slope = -2.1
slope = -0.43
pre-stress
post-stress
S_{vd}
slope
S_{vd} @ 10 Hz (V^2/Hz)
|Slope| @ 10 Hz
$|V_{gs}-V_{th}|$ (V)

(b)


T = 370K
slope = -1.1
slope = -0.56
pre-stress
post-stress
S_{vd}
slope
S_{vd} @ 10 Hz (V^2/Hz)
|Slope| @ 10 Hz
$|V_{gs}-V_{th}|$ (V)

(c)



(d)

Fig. 6.9. Excess drain voltage noise power spectral density S_{vd} at 10 Hz vs. $|V_{gs}–V_{th}|$ for SiGe *p*MOSFETs before and after NBTS at temperatures of (a) 210K, (b) 300 K, (c) 370 K, and (d) 420 K. The noise is measured in the linear region of device response, with V_{ds} = -0.05 V and $|V_{gs}$-$V_{th}|$ = [0.2, 0.85] V. During NBTI, devices are stressed at V_G = -2 V for 10^4 s, then annealed at 0 V gate bias stress for 10^4 s to allow fast recovery of NBTI degradation as much as possible. Insets extract the slope of gate-source overdrive dependence of S_{vd} at different temperatures.

Fig. 6.9 shows the pre- and post-stress excess drain voltage noise power spectral density S_{vd} at 10 Hz and fixed V_D = -50 mV and extracted slope α over 5-40 Hz versus gate overdrive V_{GS}-V_{th}. The device with same geometries as one of Figs. 6.4 and 6.6 was stressed with V_G = -2 V (all other terminals were grounded during stressing) for during of 10^4 s. Post-stress excess noise was measured after 10^4 s recovery with V_G = 0 V after stress. Neither pre- nor post-stress S_{vd} at 10 Hz shows clear peaks at the different temperatures which have been observed in temperature dependence of noise, suggesting that it is not easy to quantitatively map the voltage dependence of the noise into a defect-energy distribution. But the gate voltage dependence of noise can still provide us complementary information about defect distribution. Increase of noise magnitude after NBTI is observed at different temperatures except 210 K, indicating the defects associated with 300 K, 370 K and 420 K have major contribution to NBTI. This is consistent

with the results in Fig. 6.7. Only the slope at 300 K has an obvious change after NBTI, indicating the change of defect distribution caused by NBTI probably due to the reconfiguration after hole trapping. This is consistent with the results in Fig. 6.8. And α = ~1at 300 K (post-stress), 370 K (pre- and post-stress), 420 K (pre- and post-stress) is an evidence of uniform defect distribution, because generation of traps due to NBTS makes the trap density distribution more uniform. A α > 1 (post-stress) at 210 K indicate there is an excess of slow sites which can be speeded up by raising the temperature [54]. Combining the temperature dependence and gate voltage dependence of low-frequency 1/*f* noise can identify the major defect energies contributing to NBTI: ~ 0.77 eV (configurational changes), ~ 0.95 eV and 1.08 eV. These defect states are essential for the understanding of the NBTI mechanism and modeling. The insets in Fig. 6.9 extract the slopes of drain voltage noise spectral density dependence on the gate voltage overdrive ($|V_{gs}–V_{th}|$) before and after NBTI stress. The slopes are strong temperature dependence and change greatly after NBTS because NBTS can change the non-uniform $D(E_o)$. At 300 K, the slope is -2.1 after NBTS, which highlights that the 1/*f* noise of SiGe devices is due to carrier number fluctuations [120]. This is not surprising since the SiGe channel can form an implant free quantum well (IFQW) which can significantly reduce the coulomb scattering from HfO_2/SiO_2 gate stack. At high temperatures, the slopes tend to be 1.0 after NBTS. The changes of slopes at different temperature after NBTS need further study.

6.3 Discussion

A significant number of experimental and theoretical studies have identified oxygen vacancy-related defects in SiO_2 as a dominant defect responsible for the low frequency 1/*f* noise of MOS transistors [27],[49]-[51],[60],[106]-[108],[119]. First-principles calculations based on density functional theory [121] have been used to identify oxygen vacancies in amorphous SiO_2

networks [112],[113]. At least two kinds of oxygen vacancies in amorphous SiO_2 are known to be important to this process. The first has a dimer configuration and is frequently identified with the E_δ' -center [49],[112],[122]-[125]. The second is the E_γ' -center which has a dimer configuration in the neutral state and puckers in its positively charged state with significant lattice relaxation [22],[106],[112],[122]-[127].

For SiO_2, approximately 90% of oxygen vacancy defects exhibit little structural relaxation upon the capture of a hole, meaning that those defects still maintain the dimer configuration in the positively charged and neutral states [122]. The E_δ' -center has been associated with shallow hole trapping and/or retarded hole transport in SiO_2 [122]-[125], with energies ranging from ~ 0.5 to ~1.0 eV [25],[112],[122]. So dimer O vacancies may contribute significantly to the noise observed between ~ 200 K and ~ 400 K in Fig. 6.8. Indeed, these defects may dominate the observed noise before and after stress at intermediate temperatures, e.g., the small peaks at energies of ~ 0.5 to ~ 0.65 eV in Fig. 6.8 that do not change with NBTS. Dimer O vacancies will not contribute to the relatively stable threshold voltage shifts observed at higher temperatures. But they are likely to contribute to the fast component of NBTI for measurements and above room temperature [22],[49],[106]-[108],[110],[117]. These defects do not undergo any permanent, structural changes through the NBTS process.

E_γ'-centers in SiO_2 have higher energies than E_δ'-centers, and on the basis of a significant amount of work on MOS devices subjected to ionizing radiation and/or bias-temperature stress, are strong candidates for higher-energy noise peaks [36],[49],[50],[106]-[108],[116]-[118]. Complexes incorporating oxygen and hydrogen (e.g., the hydrogen bridge, which is a hydrogen atom at a dimer O vacancy in SiO_2 [37]-[39],[112],[128], and the hydroxyl E' center, a strained O bonded to a hydrogen atom [40],[41]) may also affect the higher-temperature noise, especially

after NBTS. In contrast to the $E_{\delta}^{'}$-centers, these defects are modified structurally and/or chemically via NBTS. Moreover, the hydrogen-related defects increase in density as a result of NBTS [37]-[41],[32],[91],[128].

Consistent with the above interpretation, we note that the regions throughout the interfacial layer SiO_2 and at the SiO_2/HfO_2 interface are rich in oxygen vacancies, as shown in Fig. 5.8. Moreover, calculations of oxygen-vacancy and/or hydrogen-related defect energy levels in HfO_2 show that similar defects in HfO_2 also likely contribute to the observed noise before and after NBTS [49],[70],[129]-[132]. The absence of the large peak at low temperatures in Fig. 6.8 in previous studies of the temperature dependence of the low-frequency noise of MOS transistors with SiO_2 gate dielectrics [49],[112],[113],[133] suggests that at least some of the low-energy peak in Fig. 6.8 may be associated with defects in the HfO_2 layer. However, we also note that the binding energy of atomic hydrogen at dopants in the SiGe layer drops to ~ 0.2 eV to ~ 0.3 eV under negative bias [134], suggesting that the capture and release of hydrogen by dopants in the SiGe channel layer may also contribute to the low-temperature noise peak in these devices. This process would occur on much faster time scales than can be sensed by low-frequency noise measurements at higher temperatures, where the noise appears to be dominant by the exchange of charge between the channel and the dielectric layers.

6.4 Summary and Conclusions of Chapter

We have measured the temperature dependence of the low-frequency 1/*f* noise of SiGe *p*MOSFETs with SiO_2/HfO_2 gate dielectrics with and without exposure to negative bias-temperature stress (NBTS). Information about defects contributing to NBTI is obtained for effective defect energy levels from ~ 0.2 eV to ~ 1.1 eV. At temperatures below ~ 270 K (energies below ~ 0.65 eV), the defects responsible for the low-frequency noise in these devices

are not significantly affected by NBTS. At higher temperature and energies, threshold voltage shifts due to NBTI are observed, as is a corresponding increase in noise. Noise at the lowest temperatures (< 200 K) may result primarily from defects in the HfO_2 layer and/or hydrogen motion in the SiGe layer. Noise at intermediate temperatures (200 K to 270 K) evidently results from dimer O vacancies in SiO_2. Noise at higher temperatures appears to result from a combination of hydrogen- and O-vacancy-related defects in the SiO_2 and/or HfO_2 layers. Noise levels in these particular devices at temperatures below ~ 270 K are not affected significantly by NBTS, but both levels at higher temperatures are affected quite significantly by NBTS. These results illustrate that both low-frequency noise and NBTI-related degradation in MOS transistors are affected strongly by several different types of defects that are distributed broadly in energy. Significant information about defect densities and effective energy distributions can be obtained via low-frequency noise measurements.

CHAPTER VII

Conclusions

This work has focused on the characterization of defects associated with TID and NBTI in the HfO_2/SiO_2 gate dielectric stack of *p*MOS transistors. In TID experiment, we find that negative bias irradiation leads to the worst-case degradation in the total dose response of SiGe *p*MOS FinFETs. We attribute this result to an increase in density of additional radiation-induced holes that become trapped in the HfO_2 under negative bias, and additional electron trapping under positive bias in the HfO_2, as compared with the 0 V irradiation case. A simple model of the structure suggests that these excess carriers originate in the near-interfacial SiO_2.

In the NBTI experiment, positive oxide-trap charge trapping is the dominant defect responsible for NBTI in $Si_{0.55}Ge_{0.45}$ *p*MOSFETs with high-K dielectrics. The experimental results show similarly small values of E_a for oxide-trap charge buildup, while E_a is lower for interface-trap buildup in the *p*MOSFETs with $Si_{0.55}Ge_{0.45}$ channel and high-K gate stacks, compared to the Si channel devices with SiO_2 gate dielectrics. The similar activation energies for oxide-trap charge in these two structures suggests that hole injection into the near-interfacial SiO_2 via tunneling is evidently the rate-limiting process for oxide-trap charge buildup during negative-bias stress. Electron energy loss spectroscopy shows the presence of Ge atoms in the Si capping layer. First-principles calculations show that Ge atoms near the Si/SiO_2 interface are primarily responsible for the reduced activation energies for interface traps in the SiGe *p*MOS devices, as compared with the Si *p*MOS devices.

The frequency and gate-voltage dependences of the low-frequency 1/*f* noise were investigated for SiGe *p*MOSFETs with SiO_2/HfO_2 gate dielectrics with and without exposure to negative bias-temperature stress (NBTS). Information about defects contributing to NBTI is obtained for effective defect energy levels from ~ 0.2 eV to ~ 1.1 eV. At temperatures below ~ 270 K (energies below ~ 0.65 eV), the defects responsible for the low-frequency noise in these devices are not significantly affected by NBTS. At higher temperature and energies, threshold voltage shifts due to NBTI are observed, as is a corresponding increase in noise. Noise at the lowest temperatures (< 200 K) may result primarily from defects in the HfO_2 layer and/or hydrogen motion in the SiGe layer. Noise at intermediate temperatures (200 K to 270 K) evidently results from dimer O vacancies in SiO_2. Noise at higher temperatures appears to result from a combination of hydrogen- and O-vacancy-related defects in the SiO_2 and/or HfO_2 layers. Noise levels in these particular devices at temperatures below ~ 270 K are not affected significantly by NBTS, but both levels at higher temperatures are affected quite significantly by NBTS. These results illustrate that both low-frequency noise and NBTI-related degradation in MOS transistors are affected strongly by several different types of defects that are distributed broadly in energy. Significant information about defect densities and effective energy distributions can be obtained via low-frequency noise measurements.

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