CHARACTERIZATION OF HEAVY-ION INDUCED SINGLE EVENT TRANSIENTS IN 32nm AND 45nm SILICON-ON-INSULATOR TECHNOLOGIES

By

Jeffrey Alan Maharrey

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Professor W. Timothy Holman

Professor Lloyd W. Massengill

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CHAPTER I

INTRODUCTION

The earliest paper from the radiation effects community on digital single event transients (DSETs) was published in 1983 by Diehl et al. [1]. Since they were first observed, SETs have become increasingly important to characterize especially since operating frequencies have surpassed 100 MHz, at which point SETs are capable of propagating through logic and causing errors. In modern digital CMOS integrated circuits (ICs), SETs are the dominant contributor in the soft-error response [2]–[4]. Consequently, it is vital to characterize both the SET pulse width and cross-section for advanced technologies in order to confidently design radiation-robust circuitry in those advanced technologies.

In this thesis, SET pulse width data gathered from heavy-ion irradiation of 32nm and 45nm partially-depleted silicon-on-insulator (PDSOI) technologies are presented. It is now commonly known that single-LET beam exposure produces a distribution of pulse widths and that using the worst case pulse width often leads to an overestimation of the sensitivity of a circuit. This thesis shows with experimental data that the distribution of pulse widths from inverter chains at a given LET is significantly impacted by the choice of standard Process Design Kit (PDK) MOS variants and layout variations such as threshold voltage and body contact. While inverters may or may not provide the longest SETs, they allow the most straightforward comparison for the device variants in that they minimize the circuit aspects (for example logic states and numbers of inputs). Also, an experimental comparison between the single event response of 45nm and 32nm PDSOI is made in order to determine how SETs are scaling with technology.

CHAPTER II

RADIATION EFFECTS BACKGROUND

The possibility of cosmic radiation interacting with a semiconductor device to produce undesirable effects was first postulated by Wallmark and Marcus in 1962, although it had been known for some time that radiation from other sources affected semiconductor devices [5]–[7]. The first observation of errors due to cosmic radiation was in 1975 by Binder, Smith and Holman [8]. Since then, extensive research has been done to understand how radiation affects electronics.

Radiation Effects Overview

The effects of radiation interaction with a semiconductor material are categorized into two broad categories, ionization effects and displacement damage effects. Displacement damage occurs when incident energetic particles collide with atoms in the lattice of the semiconductor causing the lattice atoms to move from their original location. Ionization effects are the result of energetic particles causing excess carriers to be formed in the semiconducting material. Ionization effects may be further categorized as total ionizing dose (TID) or single event (SE) effects. Total ionizing dose is a long term ionization effect which causes degradation by introducing excess charge in the insulating material of a semiconductor device. A single event effect (SEE) is a short term confined ionization effect in which a single particle interacts with the semiconductor material, causing the deposition of excess charge along the entirety of its path through the material.

Single Event Effects Overview

Single event effects may manifest themselves as single event transients or single event upsets (SEU). Single event transients are ionization induced signals in a circuit that compete with the nominal signals. If these SETs propagate through logic and are latched as incorrect data then they become soft errors. Single event upsets produce soft errors by the direct interaction of radiation with a storage element or latch. Soft errors due to single event upsets do not depend on clock frequency while soft errors due to SETs depend linearly on frequency. Thus, as technology scales and clock frequencies increase, SETs become an ever increasing problem. This thesis focuses on the measurement of SETs in advanced SOI materials.

Single Event Charge Generation

As an energetic particle passes through a semiconductor it liberates electron-hole pairs through the ionization of bound electrons into the conduction band. A common metric used in calculating the amount of charge deposited in a specific material from a heavy-ion is the linear energy transfer (LET) of the ion. LET has units of energy per unit length. More commonly, LET is quoted for a given ion mass, ion energy and target material density so that the units are $MeV*cm^2/mg$. The amount of charge deposited per unit length due to a certain heavy-ion passing through silicon can be calculated using the following equation:

$$Q[fC] = 10.8 \text{ x } L[\mu m] \text{x LET } [MeV * cm^2/mg] \quad (1)$$

The aerial density of silicon is 0.242 mg/cm^2 for a $1\mu m$ thickness. In silicon, in order to create 1 electron-hole pair, 3.6 eV of energy is needed. Also, 1 electron corresponds to

1.60 x 10^{-4} fC of charge. The constant in the equation above is specific for silicon and is calculated as:

$$10.8\ \left[\frac{fC*mg}{cm^2*\mu m*MeV}\right] = \frac{1.6x10^4[fC]}{3.6\ [eV]} * 0.242\ \left[\frac{mg}{cm^2*\mu m}\right] * \frac{10^6[eV]}{1\ [MeV]} \quad (2)$$

It is important to note that LET varies with distance traveled through a material, thus the equation for Q, can only be used for short path lengths where the LET does not change significantly.

Single Event Transient Induced Errors

A common topology for sequential circuits is seen in Fig. 1. An error signal due to the production of an SET within the combinational logic of sequential circuitry can propagate to a latching element and result in a soft error if certain timing criteria are met. An SET will be latched as an error if it is present at the latch a setup time before the clock edge and a hold time after the clock edge as illustrated in Fig. 2 [3]. The summation of the setup and hold times of the latch is known as the window of vulnerability. A longer SET pulse width corresponds to a higher probability of being latched as can be seen in Fig. 2. It has also been shown that errors from SETs depends linearly on clock frequency [9].

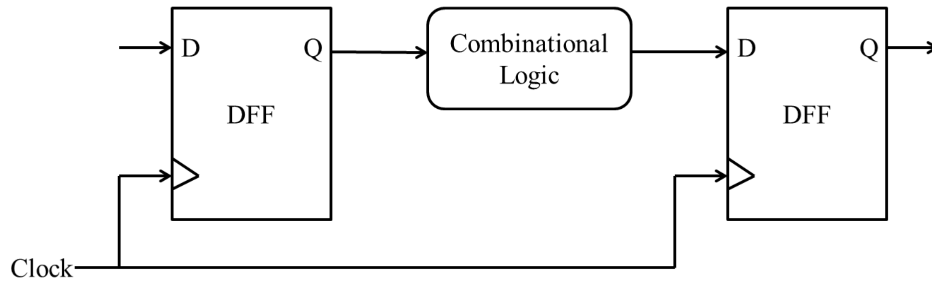

Fig. 1. Basic diagram of sequential circuitry.

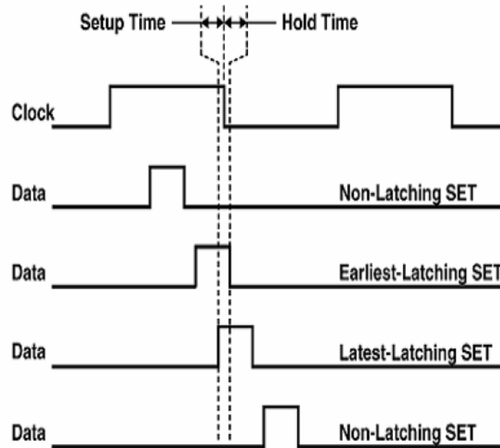

Fig. 2. Window of vulnerability for latching an SET.

Single Event Charge Collection in Silicon-on-Insulator Technology

As the name suggests, silicon-on-insulator technology is formed such that each transistor is in a layer of silicon on top of an insulating material, typically referred to as the buried oxide (BOX). SOI may be either partially depleted or fully depleted, which refers to whether or not the body of the SOI transistor is capable of being fully depleted of mobile carriers or not. Partially depleted SOI typically has a thicker silicon body compared to fully depleted SOI. Because of the thicker silicon body, the body is not able

to be fully depleted of all its mobile carriers. All technology used in this thesis was partially depleted SOI.

In a conventional bulk technology an ion may deposit charge within the first few micrometers of the body. Some of the deposited charge is promptly collected through the process of drift due to the influence of the electric field in the in the drain-body depletion region (See Fig. 3). Some of the deposited charge is collected more slowly through the process of diffusion in which mobile carriers diffuse and are eventually collected by a junction through a drift process.

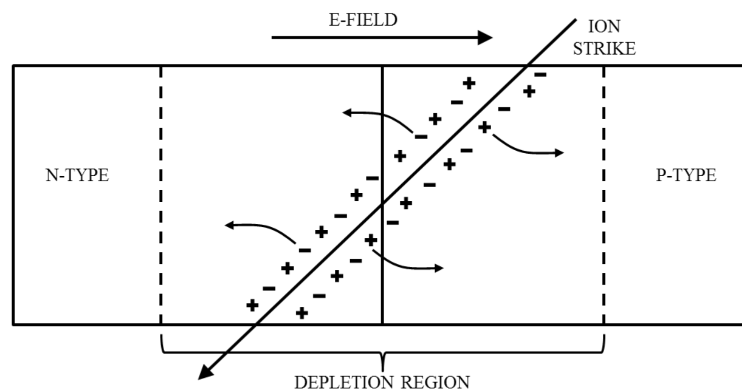

Fig. 3. Drift collection in pn junction.

In SOI, the charge deposition path is limited compared to bulk due to the depth of the silicon body on top of the BOX. However, there is an inherent parasitic bipolar transistor between the source, body and drain of any MOSFET (SOI or bulk) that may be turned on if the body potential is modulated enough. In bulk the parasitic bipolar is only of concern for devices built in wells (typically PFETs); however, in SOI all devices are sensitive because all devices are isolated (see Fig. 4). The isolation of the body makes the

device more sensitive to body potential modulation from a single event. If the parasitic bipolar is turned on, it causes charge to be collected in excess of what was deposited by the ion. This effect is termed bipolar amplification. For this reason, SOI technology typically performs only marginally better than its bulk counterpart [3]. Excess charge will be collected even for a bipolar gain of less than 1.

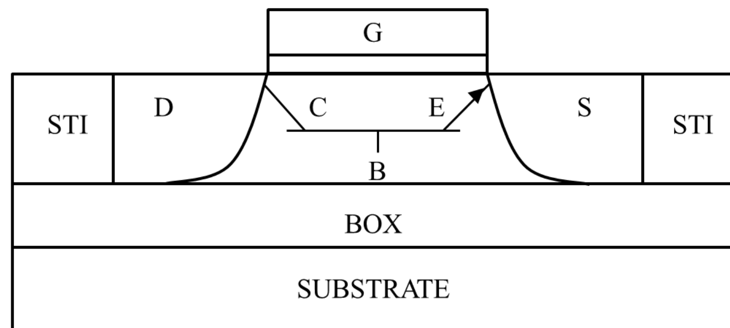

Fig. 4. Parasitic bipolar in SOI NFET.

Propagation Induced Pulse Broadening

As a pulse propagates through a chain of logic gates it can potentially stretch out. This is called propagation induced pulse broadening (PIPB). In any technology it is possible for a pulse to broaden (or narrow) if it is introduced to a chain of inverters that have asymmetric drives and loads. In SOI technology, especially partially-depleted SOI, PIPB can occur due to a hysteretic floating-body effect. It occurs because the body potential is allowed to float, which modifies the threshold voltage and switching characteristics of the inverter. Each inverter in the chain will be affected differently due to the alternating nature of the pulse in an inverter chain. This alternating effect causes a the pulse to broaden similar to a staggered drive/load situation [10]–[12].

CHAPTER III

ON-CHIP MEASUREMENT TECHNIQUE FOR SINGLE EVENT TRANSIENTS

Several methods have been developed to measure SETs and [4] offers a great overview of the most common measurement techniques. The two main categories of measurement methods include SET counting and SET pulse width measurement techniques. The measurement method used in this work is a pulse width measurement technique that was first developed by Nicoladis et al. in [13] and later improved upon by Narasimham et al. and Loveless et al. [14], [15]. Specifically, this section describes an autonomous pulse width measurement technique which was implemented in 32nm and 45nm SOI.

Overview of Autonomous SET Measurement Circuit

The initial design was done by Narasimham et al. in [14]. The actual measurement circuit used in this work was designed by Loveless et al. in [15]. The major difference between the measurement circuits of Narasimham and Loveless is that Loveless included a variable trigger delay which allowed for the characterization of error within the measurement circuit, which is discussed in a later section. In Fig. 5 the basic schematic for the autonomous pulse capture circuit is shown. Previous pulse capture circuits used a similar latching method as the one shown in Fig. 5; however they all used an external trigger to send a flag back to the chip in order for the pulse to be captured. Narasimham designed the pulse capture circuit to create its own self-trigger so that an external trigger was not necessary. This is extremely useful for heavy-ion testing in

which case the timing of ion interaction with the target is impossible to know (as opposed to laser testing for example). Fig. 6 shows more detail on the function of the self-trigger. Basically, the output of the nth stage is constantly monitored. When an SET propagates through the nth stage, a trigger is formed after some delay which then sends a hold signal through a series of buffers to all the latches. If the first latch has recovered to its initial state once the SET is captured then the SET pulse width has been fully captured and the pulse width can be known to within the accuracy of the measurement circuit. However, if the SET is captured before the first latch has recovered to its initial stated then the SET pulse width cannot be fully known since it is possible that the SET was much longer than what was captured. The reason for the delay in the trigger is that the SET needs enough time to fully propagate in to the pulse capture circuit [14]. This delay, is precisely what Loveless improved upon in [15]. By making this delay a variable delay, the SET is able to be captured in different segments of the pulse capture circuit. In a following section of this paper the quantification of error in the pulse capture circuit will be explained which is possible due to the variable delay.

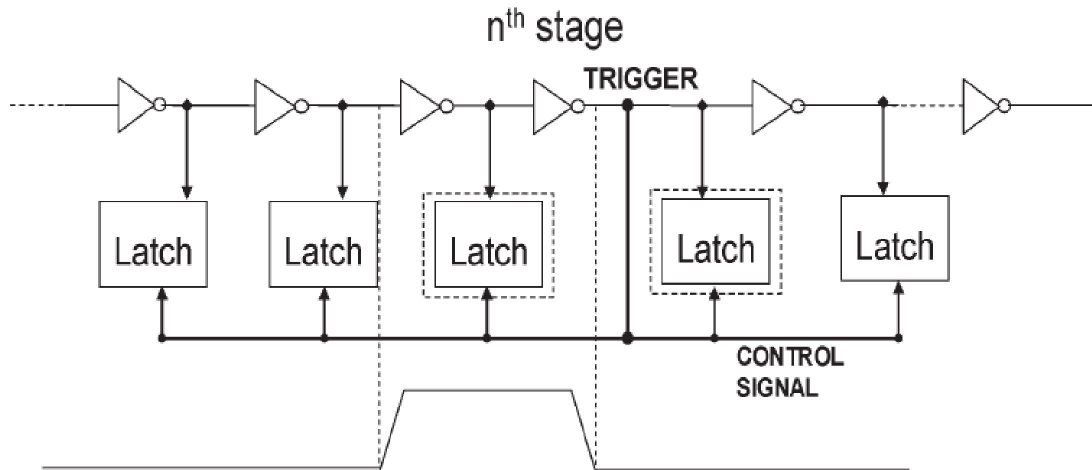

Fig. 5. Schematic diagram of the pulse capture circuitry. SETs enter the capture circuit as shown above. As the SET propagates through the inverters it upsets multiple outputs at any given time. Once it reaches the nth stage, a trigger is created which sends a hold signal to the latches [11].

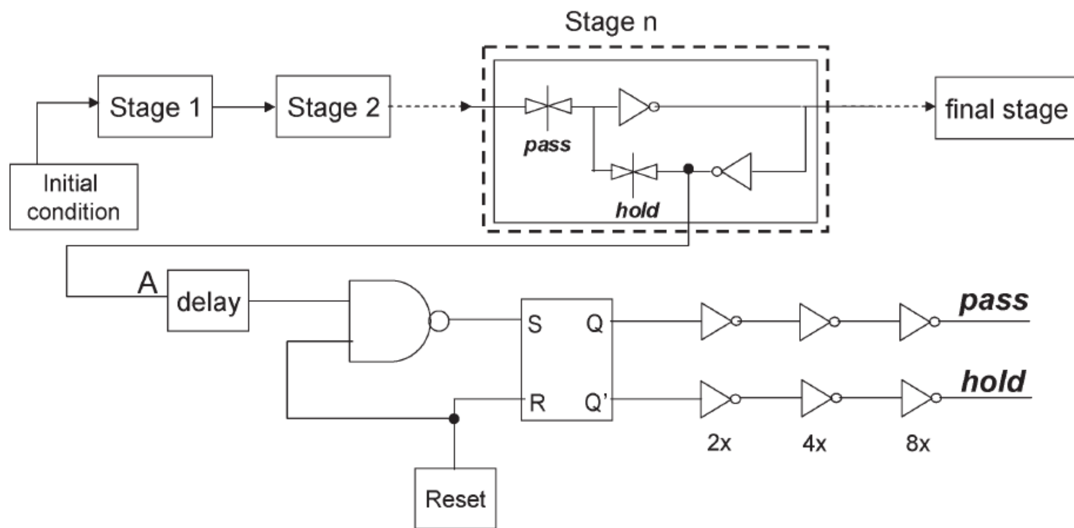

Fig. 6. Schematic diagram of the pulse capture circuitry with detail on the self-triggering mechanism. As the SET propagates through stage n, a trigger is created from the SET itself which causes a pass or hold signal to be sent back to the transmission gates of each stage [11].

Overview of 32nm and 45nm Measurement Chips

The three basic parts of the autonomous SET measurement chips are: single-event target circuitry for ion interaction and SET formation, a distribution network for the transfer of the SET to appropriate measurement circuitry, and measurement circuitry for the capture of the SET. For the 32nm and 45nm SET test chips of this work, a variety of inverter chains integrating many of the PDK-standard MOS device variants were used as targets. A balanced OR-gate tree was used as the distribution network, and the Vanderbilt autonomous measurement circuit was used to capture the SETs. These test chips were designed by Jeff Kauppila and Dr. Daniel Loveless [15]. Shown in Fig. 7 is the basic diagram of the SET measurement circuit used in the 32nm and 45nm measurement chips.

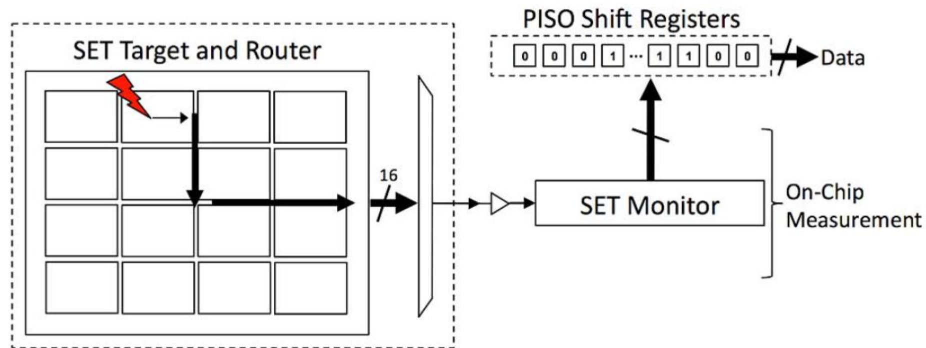

Fig. 7. Basic diagram of the SET measurement circuit used in 32-nm and 45-nm SOI [15].

There are 16 targets on each test chip. Most of the targets are inverter arrays with various PDK device types and layout configurations. Each measurement chip also contains targets that are calibration structures to aid in the extraction and quantification of measurement error. Each inverter array target consists of short chains of serially

connected inverters, 8-24 per chain (unless the chain is specified as “long”), with the input of all of the chains connected in parallel, and the output of the chains combined using a balanced OR-gate tree. The short chain length helps to reduce pulse broadening, while the parallel connection helps to maintain a large total cross section for the target circuitry. A few of the targets on each chip were laid out as “long” chains in order to quantify pulse broadening. The 32nm chip, which is a first-generation (revision 1) autonomous SET test chip, has approximately 24,000 inverters per target while the 45 nm chip, which is a second generation (revision 2) autonomous SET test chip, has approximately 48,000 inverters per target. The number of inverters was increased for the second-generation test chip in order to obtain improved statistics within a given beam time.

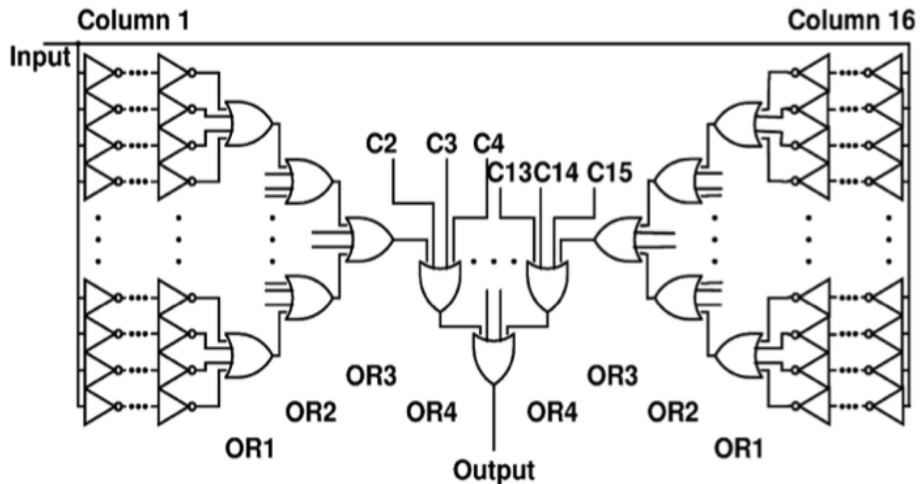

Fig. 8. Schematic diagram of target and distribution network. This represents one of the sixteen targets that are on each chip. Each target consists of 16 columns. Each column consists of chains of inverters whose inputs are in parallel and outputs are routed through the distribution network. The distribution network is a hierarchical cascade of OR gates that takes the outputs of several chains of inverters and combines them into one output [15].

An OR-gate tree propagates the SETs generated in each chain to a single output as seen in Fig. 8. The propagation of the SET from the OR-gate tree to the measurement circuit is a series of buffers and a 16-channel analog multiplexer. The OR-gate tree was designed to have a minimal influence on the measurement of SETs generated in the target circuitry. The cross section of the OR-gate tree accounts for less than 10% of the total cross-sectional area. Also, the OR-gate tree on both test chips was laid out to have matched impedances at the output of each chain of inverters within a given target, which helps to reduce any spatial dependencies due to RC filtering.

The VU Autonomous measurement circuit was used to capture SETs for both the 32nm and 45nm test chips. It uses a basic time to digital converter to quantize the SET pulse width. This measurement technique is only capable of measuring pulse widths not pulse heights. The only information about pulse height that is known is that it is the minimum pulse height for unhindered propagation through the inverter chain targets.

Sources of Measurement Error

When measuring transient signals that are on the order of tens to thousands of picoseconds (a VERY short time!) it is inevitable that they will be affected or altered by the measurement technique. This error in the measurement can arise from several places in the overall measurement chip. The next few sections will address the error that is associated with the SET measurement and break it into three segments: error in the target circuitry, error in the distribution network, and error in the pulse capture circuit.

SET target circuitry was traditionally organized as long chains of logic gates in order that the overall cross-section of the target could be maximized. This method was expected to give a fairly accurate look at the SETs generated in a given technology.

However, in 2007, Ferlet-Cavrois et al. observed and explained that SETs could broaden as they propagate through a chain of logic gates. This effect is called propagation-induced pulse broadening (PIPB), and it is a cumulative effect in that it is worse for long chains than it is for short ones [10]. PIPB can occur for reasons. One is that if the inverters in a chain have asymmetric drives and loads. The second reason PIPB can occur is due to MOS V_T hysteresis [11]. This newly discovered effect shed doubt on the validity of previously gathered SET data that used long logic chains. It is also possible that an SET is attenuated as it propagates if it is not as long as the intrinsic rise and fall time of the logic gate [11]. In order to diminish the PIPB effect as much as possible in the 32nm and 45nm chips of this work, the target circuitry was laid out in short chains of inverters (8-12 per chain) with the input of each chain connected together and the outputs routed through the distribution network. These short chains of logic gates help to reduce the effect of PIPB on the generated SETs.

Since the target circuitry was laid out in short chains, an extensive distribution network had to be designed to bring the output of each chain of inverters to a single node in order that an SET generated in any chain could be measured. Fig. 8 shows the schematic of the distribution network which logically ORs the outputs of each chain of inverters together. There are few ways in which the distribution network can contribute errors to the measurement of SETs generated in the target circuitry. The distribution network inherently gives rise to RC loading on the target circuitry. Anytime there is an RC load then there is the possibility of RC filtering. The distribution network acts as a low pass filter on the output of the target circuitry. When really short pulses (SETs) go through this filter it is possible that they will be attenuated to a shorter pulse or be

completely diminished. This effect cannot be eliminated as long as a there is a distribution network. However, in order to not introduce more error, the distribution network can be designed such that every inverter chain in a target has the same RC load attached to its output. This is how the 32nm and 45nm chips were designed. This eliminates any spatial dependency due to RC attenuation since SETs from one chain are not filtered more than SETs from another chain. A second way that the distribution network can introduce error is by capturing an SET that was generated within the distribution network instead of the target circuitry. In order to mitigate this error, the test chip was designed such that the distribution network could be monitored separately from the target circuitry. By monitoring the distribution network separately and irradiating the test chip, a cross-section can be calculated for the distribution network which can later be compared to and subtracted from the measured target cross-section since the total cross-section is the sum of the target, distribution, and pulse capture circuit cross-sections.

Another error that is possible is double or concatenated pulses. Double pulses, two SETs near each other in time but not overlapping, are capable of being measured. However, if these two pulses are concatenated as they propagate the OR gate tree then it is possible that two SETs will be measured as one long SET. The probability that two pulses are concatenated (overlapped in time) during propagation through the OR-gate tree is lower than that of a double pulse occurring since the time frame that a double pulse can occur in is much larger than the time frame for two overlapping pulses. Given the fact that double pulse were rarely seen in testing, it is logical to assume that concatenated pulses are extremely rare events that will have little bearing on the cross-section or average pulse width.

The SET capture circuit also introduces error into the SET measurement. As discussed above, PIPB can alter the SET as it propagates through the target circuitry. The same is also true for the SET capture circuit. As the SET propagates into the pulse capture circuit it will experience broadening. This broadening alters the pulse width and causes the capture circuit to incorrectly measure the generated SET. The main source of error in the measurement circuit is due to the uncertainty in the width of the SET due to quantization error that is inherent to the measurement technique. Since the SET capture circuit digitizes the transient signal into multiples of a given delay, it is impossible to know the exact width of the pulse since the capture circuit has limited resolution. Narasimham et al. characterized the resolution in [14]. It was determined that the SET could be resolved to plus or minus one half of a stage delay.

Quantification of Measurement Error

With the sources of error identified, it is imperative that the error be quantified and extracted as much as possible from the SET measurement. There are several methods used on both the 32nm and 45nm chips. One such method is by way of simulation. In order to quantize the effect of RC attenuation of an SET as it propagates through the distribution network, simulations were performed in Cadence. The simulation is fairly simple. A range of pulses (10 ps to 500 ps) are injected at the input to the target chain. Each pulse is then measured at the input of the SET capture circuit to check for attenuation. Once this is done, each nominal bin, as calculated using equation 3, is modified to account for the attenuation through the distribution network. For example, say a pulse was measured that corresponded to 3 delays in the pulse capture circuit. Those 5 delays ideally correspond to a pulse that was 3*1 delay long to within plus or

minus one half a delay. Assume the measured pulse was between 50 ps and 70 ps. To extract the attenuation error, pulses between 60 ps and 80 ps were injected via simulation to the input of a target chain. Assume for this example that the range of pulses measured at the input of the SET capture circuit were between 50 ps and 70 ps. This means that the original pulse was 10 ps longer before it propagated through the distribution network. Thus the SET will be recorded as being between 60 ps and 80 ps instead of 50 ps and 70 ps.

Another method for extracting the error due to RC attenuation is to experimentally inject pulses of a comparable width to an SET into the measurement chip. Sending in pulses on the order of tens of picoseconds is practically impossible to do off-chip due to parasitic capacitance, inductance and resistance. However, with an on-chip pulse generator this is possible. The 32nm test chip was designed with on on-chip fast pulse generator that can produce pulses between 100 ps and 750 ps. The pulse-generator produces a pulse that is injected at the input of the target circuitry. This allows for error quantification not only due to the RC attenuation in the distribution network but also partially for PIPB through the target circuitry. Fig. 9 shows the pulse generated by the on-chip pulse generator alongside the pulse measured by the SET capture circuit. There is good agreement between the generated and measured pulse.

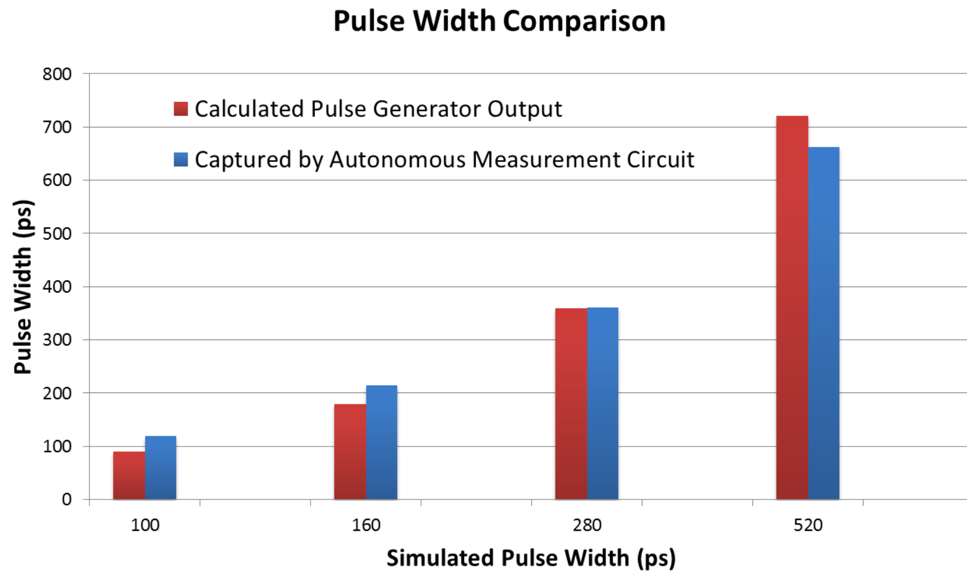

Fig. 9. Plot of experimentally injected pulses and experimentally measured pulses using the on-chip pulse generator. There is good agreement between the pulse produced by the pulse generator and the pulse captured by the SET capture circuit.

As mentioned above, the SET capture circuit itself can introduce error into the SET measurement. In [15], Loveless et al. characterized the error that the loading of the SET capture circuit has on the propagating SET. By using a digitally controlled variable delay, SETs were able to be captured at different points in the SET capture circuit (see Fig. 10). This effect was characterized experimentally as seen in Fig. 11. Percentage of measurement circuit utilized refers to the distance the SET was allowed to propagate into the SET capture circuit before being captured. The general trend is an increase in SET pulse width as the SET travels further into the SET capture circuit due to PIPB. There is a slight decrease in the average SET pulse width between 49% and 56% utilization due to capacitive loading caused by a bend in the physical layout of the measurement circuit [15].

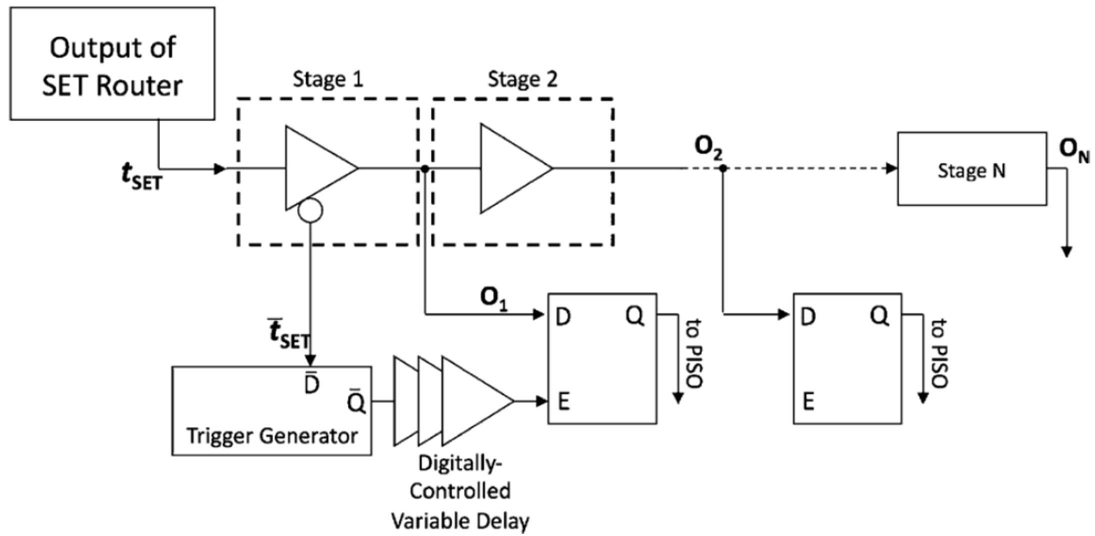

Fig. 10. Schematic diagram of the SET capture circuit with the digitally controlled variable trigger delay [15].

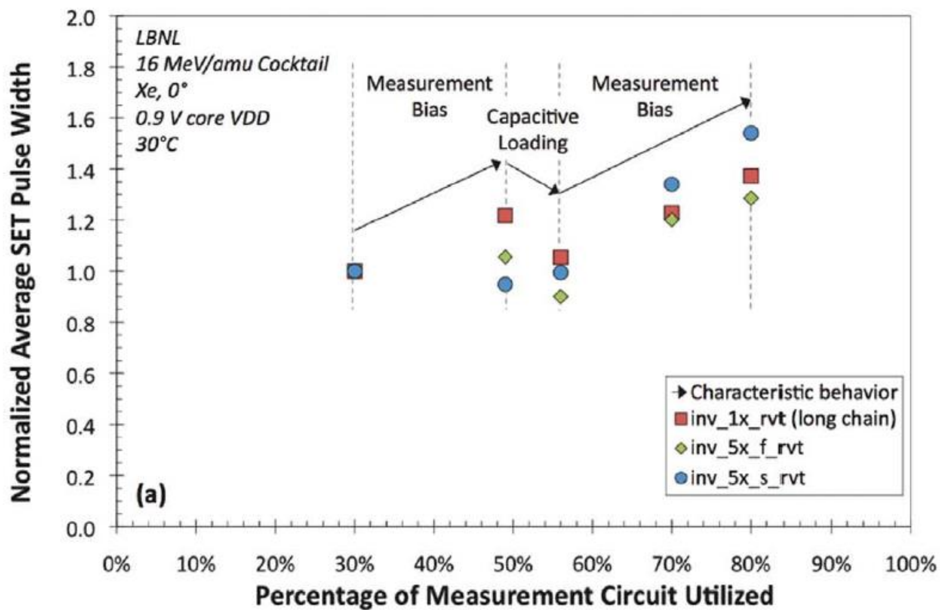

Fig. 11. Plot of the effect that the SET capture circuit has on the SET pulse width [15].

Although an attempt was made to extract many known sources of error, there are still some that were not accounted for. The effect of process variation was not directly measured, however tests were performed on the same target across multiple chips. Temperature can also cause variations in the electrical characteristics of a circuit. The temperature was not monitored during experimentation. These are just a few of the known unknown sources of error. Of course, there are always the unknown-unknowns.

CHAPTER IV

EXPERIMENTAL SETUP

This chapter provides the experimental details for all data presented in this paper. Both the 32nm and 45nm test chips were irradiated in a heavy-ion broadbeam environment using the 88" cyclotron at Lawrence Berkeley National Laboratory (LBNL). The setup used an Altera FPGA to extract the data from each chip. The extracted data was then processed into histograms. The nominal histogram bin widths for each test chip were calculated by measuring the frequency of an on-chip ring oscillator having the same number of stages as the measurement circuit calculated as

$$t_{bin} = \frac{1}{frequency * \# \, stages} \quad (3)$$

since there are two inverters per stage for the measurement circuit. The following sections will outline the details for both the 32nm and 45nm test chips.

Experimental Conditions

All data in this thesis was collected using a beam energy of 10 MeV/u. All of the data is from broadbeam irradiation using the heavy-ion Xe unless otherwise stated. At a beam energy of 10 MeV/u, Xe has an LET of 58.8 MeV-cm^2/mg at normal (0°) incidence. The supply voltage for the I/O was 1.8 V. The voltage for the core was 0.9 V. The targets all operate at the core voltage except for the thick oxide targets which operate at 1.5 V which is stepped down from the I/O voltage.

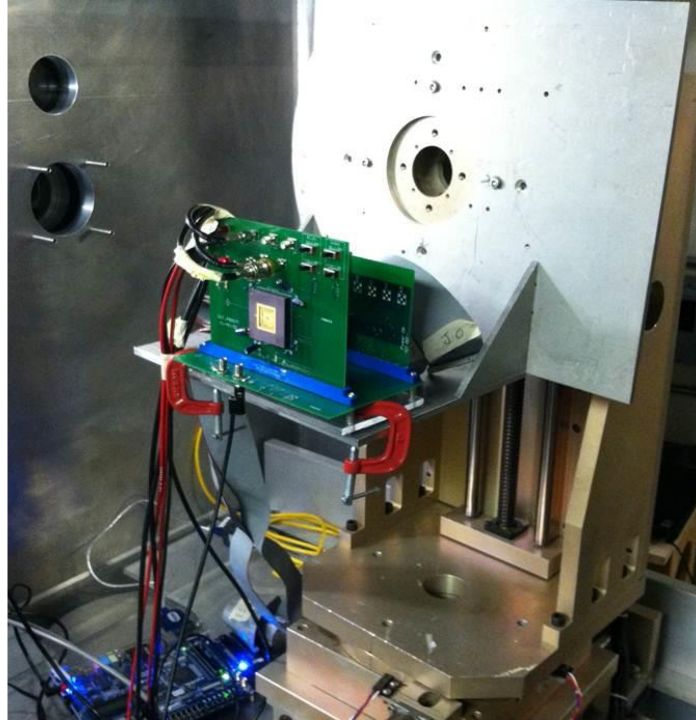

Fig. 12. Test setup for 32nm chip at Lawrence Berkeley National Laboratory.

32nm Targets

Details for all targets tested on the 32nm chip are shown below in Table 1. All of targets 1-3 were laid out according to the minimum sized NMOS device available in the technology. These are fast devices intended for digital applications. It is important to note that these three targets differ only by threshold voltage. Target 4 is a minimum sized thick oxide device. Thick oxide devices are intended for applications where operating at a higher supply voltage is desirable. Target 5 is an analog threshold voltage device intended for fast operation in analog and RF circuitry. Since analog devices are typically much larger, this target was laid out to be larger than the digital devices. Targets 6 and 7 are the same device type as target 1, however they were laid out to have 3X larger widths than target 1 to characterize what affect sizing may have on SETs. Target 6 is a single

finger device, while target 7 was laid out to have 3 fingers with a combined width equal to target 6.

Table 1. Target details for 32nm test chip. The “X 2” or “X 3” refers to the number of fingers in each device

Ref #	Circuit	Technology Node	PMOS W/L [nm]	NMOS W/L [nm]	V_{DD} [V]
1	Low VT	32	214 / 40	104 / 40	0.9
2	Mid V_T	32	214 / 40	104 / 40	0.9
3	High V_T	32	214 / 40	104 / 40	0.9
4	Thick Oxide	32	500 / 100	312 / 100	1.5
5	Analog V_T	32	1074 / 56 X 2	624 / 56	0.9
6	3X Low V_T	32	642 / 40	312 / 40	0.9
7	3X Low V_T	32	214 / 40 X 3	104 / 40 X 3	0.9

45nm Test Chip

The 45nm data was collected using a beam energy of 10 MeV/u. Unless otherwise stated, all tests were performed using the Xe ion which has an LET of 58.8 MeV-cm^2/mg at normal (0°) incidence. All of the circuits were operated at their nominal supply voltage of 0.9 V. Table 2 shows some of the relevant information for each target that was irradiated.

The bin widths for the autonomous measurement circuit on both test chips were calibrated by measuring the frequency of an on-chip ring oscillator that consists of an equivalent number of stages as the measurement circuit, exactly the same as the method used in [15]. Additional calibration was performed on the 32nm test chip using an on-chip pulse generator to send pulses of known widths to the measurement circuit as seen in

[16]. The minimum detectable pulse of the autonomous SET measurement circuit is 23 ps for the 32nm and 30 ps for the 45nm chip with a nominal resolution of 17 ps per bin for the 32nm chip and 30 ps per bin for the 45nm chip. The minimum detectable pulse corresponds to the shortest pulse that will propagate from the target and still be at least 1/2 a bin of resolution when it reaches the trigger of the measurement circuit. The quantization error of the SET measurement circuit is less than 1 bin of resolution.

45nm Targets

Details for the 45nm targets are shown in Table 2. Targets 8-10 were laid out according to the minimum sized NMOS device available in the technology. It is important to note that these three targets differ only by threshold voltage. Also, targets 8-10 are very similar to 32nm targets 1-3 from Table 1. Target 11 is a minimum sized thick oxide device similar to target 4 in Table 1. Targets 12 and 13 are larger thick oxide devices with multiple fingers. Target 14 is a floating-body analog threshold voltage device, and target 15 is a body-tied version of target 14.

Table 2. Target details for 45nm test chip. The “X 2” or “X 8” refers to the number of fingers in each device

Ref #	Circuit	Technology Node	PMOS W/L [nm]	NMOS W/L [nm]	V_{DD} [V]
8	Low VT	45	266 / 40	152 / 40	0.9
9	Mid V_T	45	266 / 40	152 / 40	0.9
10	High V_T	45	266 / 40	152 / 40	0.9
11	Thick Oxide	45	736 / 112	312 / 112	1.5
12	2X Thick Oxide	45	1144 / 112 X 2	654 / 112 X 2	1.5
13	8X Thick Oxide	45	1144 / 472 X 8	654 / 472 X 8	1.5
14	Analog VT	45	1144 / 56	654 / 56	0.9
15	Analog VT , body-tied	45	1144 / 56	654 / 56	0.9

High Current State

Upon heavy-ion irradiation, a high current state was encountered in the I/O pad ring of the 32 nm test chip. A high current state is defined as the supply current going to compliance and staying until a reset is performed. The high current state did not appear to have any effect on the fidelity of the data, however, for the sake of completeness a summary of the high current state is provided below.

The first attempt at circumventing the high current state was to increase the I/O current compliance from its initial compliance of 300 mA. The normal operating current of the I/O was approximately 5mA. In this approach the device under test (DUT) was initially operated at a compliance of 300 mA and then irradiated. The high current state occurred at the onset of irradiation. Irradiation was stopped, and the DUT I/O supply was reset. The DUT operated normally after the supply reset. The compliance was raised by approximately 100 mA. The DUT was irradiated again, and the high current state appeared just as before. The above process was repeated in 100 mA steps up to 1 A. High current states above ~750 mA caused bond wires to melt. When the latter occurred, resetting the DUT supply caused the DUT to operate normally, and the high current state could not be achieved. However, the DUT lost some functionality due to melted bondwires.

The second approach was to use thick copper foil as shielding to cover the I/O pad ring. This approach allowed for normal incident irradiation up to an LET of 58.8 MeV-cm^2/mg.

The high current state was reproduced in lab using a professional camera flash. At the nominal I/O voltage of 1.8 V, the flash caused the I/O to enter the high current

state, dropping the voltage to 0.7 V. The I/O voltage would remain at 0.7 V unless the power was cycled. The I/O response to the flash varied with decreasing I/O voltage. At 1.5 V, the I/O temporarily entered the high current state, dropping the voltage to 0.5 V for several hundreds of milliseconds before recovering to 1.8 V (transient high current state). At 1.3 V, the flash did not induce a transient. For the chip tested, 1.37 V appeared to be the boundary for the onset of the flash induced transient.

The third approach was to operate the I/O at the lowest voltage possible while still maintaining functionality. The I/O could be lowered from 1.8 V to 1 V. This approach had proven adequate to prevent the high current state when the DUT was exposed to a camera flash. Using this method, a different 32nm test chip, was able to be irradiated up to an LET of 20 MeV-cm^2/mg before exhibiting any abnormal effects. Irradiating slightly above 20 MeV-cm^2/mg caused transient high current states to appear on the I/O. Irradiating significantly above 20 MeV-cm^2/mg caused the sustained high current state. From all experiments, it is apparent that the I/O high current state is dependent upon supply voltage and LET.

CHAPTER V

SINGLE EVENT TRANSIENT RESULTS

32nm SET Distributions

Seen in Fig. 13 is a typical distribution from this work for 32nm SET pulse widths generated in a heavy-ion environment. This particular distribution is for a 1x minimum size, high V_T, floating-body inverter (Table 1 target 3). A large number of pulses captured were at the minimum measurement capability of the autonomous measurement circuit, between 23 and 31 ps. The longest captured pulse was between 90 and 107 ps. This accumulation of pulses at the lower end of the measurement capability was also seen in [15] and is due RC attenuation as the pulse propagates through the series of logic from the output of the target chain to the input of the measurement circuit and is worse for shorter pulses (< ~40 ps) than for longer ones. Designers are typically more concerned with the longer pulse widths; therefore attenuation of shorter pulse widths is of little consequence. The bin widths have been adjusted to account for RC filtering. The lowest bin in Fig. 13 represents an SET that was long enough to trigger the measurement circuit but not long enough to be latched. The second lowest bin represents the shortest SET pulse width capable of being latched by the measurement circuit. The number of longer pulses diminish due to a decrease in the area in which an ion can strike and still produce the longer pulse (i.e. towards the center of the body).

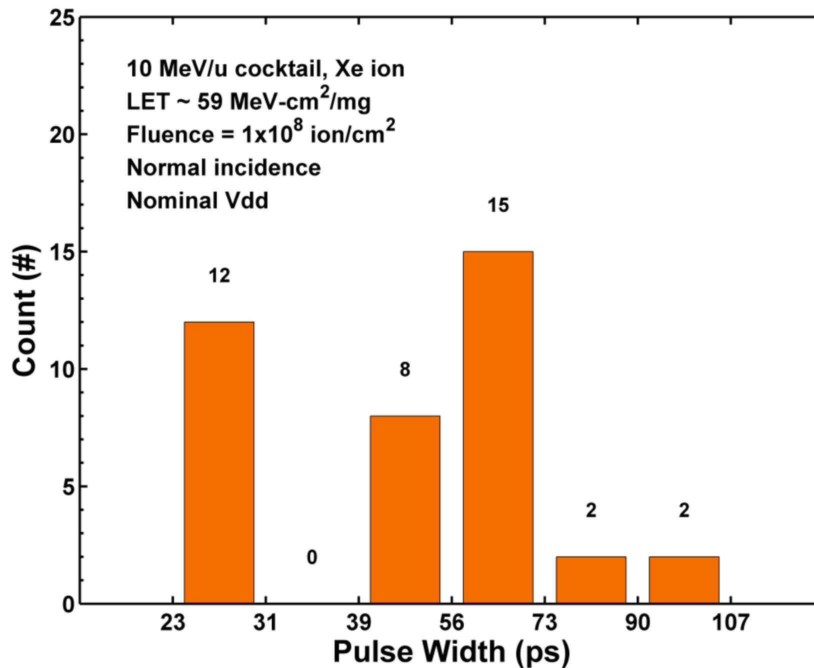

Fig. 13. SET pulse width distribution for a 1X minimum size, high V_T, floating-body inverter in 32nm SOI collected from a heavy-ion broadbeam environment.

45nm SET Distributions

Fig. 14 is a typical distribution from this work for 45nm SET pulse widths generated in a heavy-ion environment. Specifically this plot shows data for a minimum size, high V_T, floating-body inverter (Table 2 target 10). In Fig. 14 we see that, contrary to the 32nm data, the majority of pulse widths are not at the minimum resolution of the measurement circuit, and that we have an approximately Gaussian distribution of pulse widths as is expected for a single LET [15]. This is due to an increase in buffering in the SET propagation path for the 45nm test chip which decreased the attenuation of shorter pulses. The 45nm data also shows a larger maximum pulse width of 182-211 ps compared to 90-107 ps for 32nm. This is due in part to the 32nm technology having an increased drive strength compared to 45nm devices when both have equivalent drawn

gate widths and lengths [17], [18]. An increase in drive strength leads to a faster recovery time after an event and thus a shorter pulse.

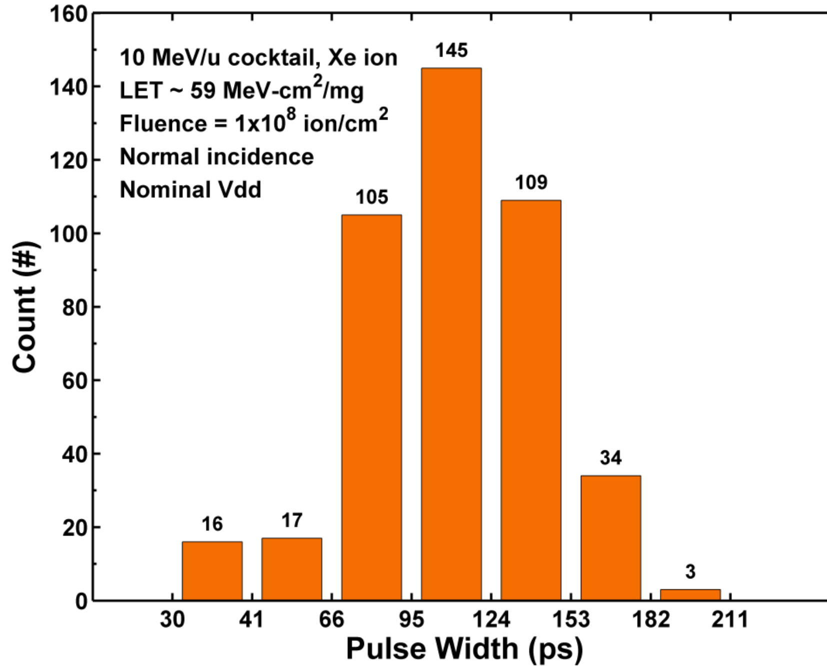

Fig. 14. SET pulse width distribution for a minimum size, high V_T floating-body inverter in 45nm SOI collected from a heavy-ion broadbeam environment.

Cumulative Cross-Section

Converting a count distribution to a cumulative distribution has been used in previous work, and it can be a very useful way to visualize relevant information from one or several count distributions in a single plot [19]–[21]. In a typical cumulative distribution, each y-value corresponds to a value on the x-axis or less; however, in a reverse cumulative distribution, each y-value corresponds to a value on the x-axis or greater. In [20], by Benedetto et al., the SET measurement technique inherently gave rise to a reverse cumulative distribution. Ferlet-Cavrois et al., in [21], showed how plotting the reverse cumulative distribution of collected charge can be useful for comparing

several devices at different technology nodes. In this paper, the reverse cumulative distribution is extracted from a count distribution of experimental pulse widths and is used to compare several different devices within the same technology, 32nm or 45nm SOI. This approach was also used by Makino et al. in [19]. Seen in Fig. 15 is the reverse cumulative distribution for the pulse width count distribution seen in Fig. 14. Each data point in Fig. 15 represents the cross section for a given pulse width or greater. At the peak of the distribution in Fig. 14 we see the cumulative cross section in Fig. 15 begin to saturate. This is expected for an approximately Gaussian distribution as seen in Fig. 14. However, depending on how much of the generated pulse width distribution is captured, the saturation in the cumulative cross section may or may not be seen. The error bars in Fig. 15 and all other cumulative cross section plots in this thesis represent the standard error, calculated as

$$error = \frac{cross\text{-}section}{\sqrt{\#\ events}}. \tag{4}$$

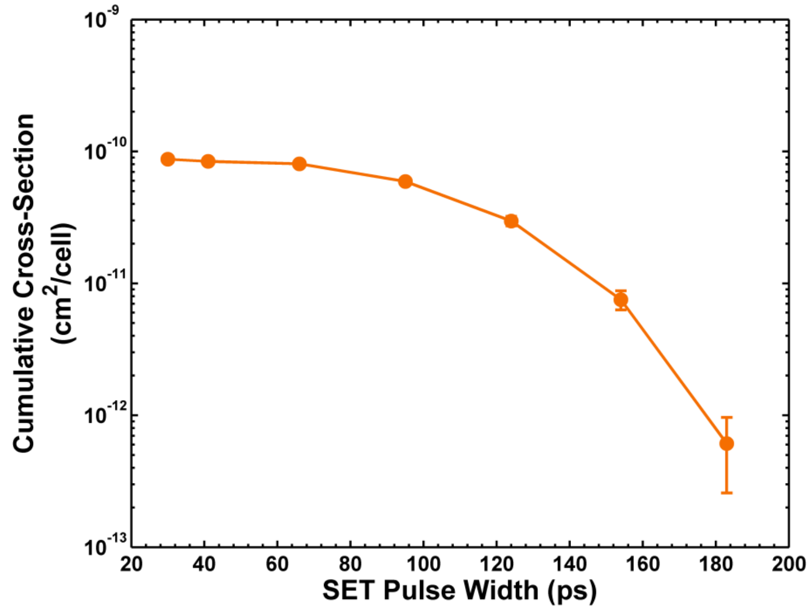

Fig. 15. Cross-section for a minimum size, high V_T floating-body inverter in 45nm SOI collected from a heavy-ion broadbeam environment.

SET Scaling

It is important to know how SETs are scaling with technology. One difficulty analyzing scaling trends is that often the two devices being compared are not very similar. Therefore, it is often unclear how to distinguish between the effects of design choices and scaling. Simulations have been performed in the past that suggest pulse widths will decrease with scaling in SOI [2]. This thesis experimentally verifies the latter statement by comparing the SET response of similar devices at both the 45nm and 32nm technology node.

Shown in Fig. 16 is the cross-section vs. SET pulse width for two similar high threshold voltage, floating-body inverters (target 3 and target 10 from Table 1 and Table 2). It is clear that there is a decrease in both cross-section and pulse width as technology goes from 45nm to 32nm.

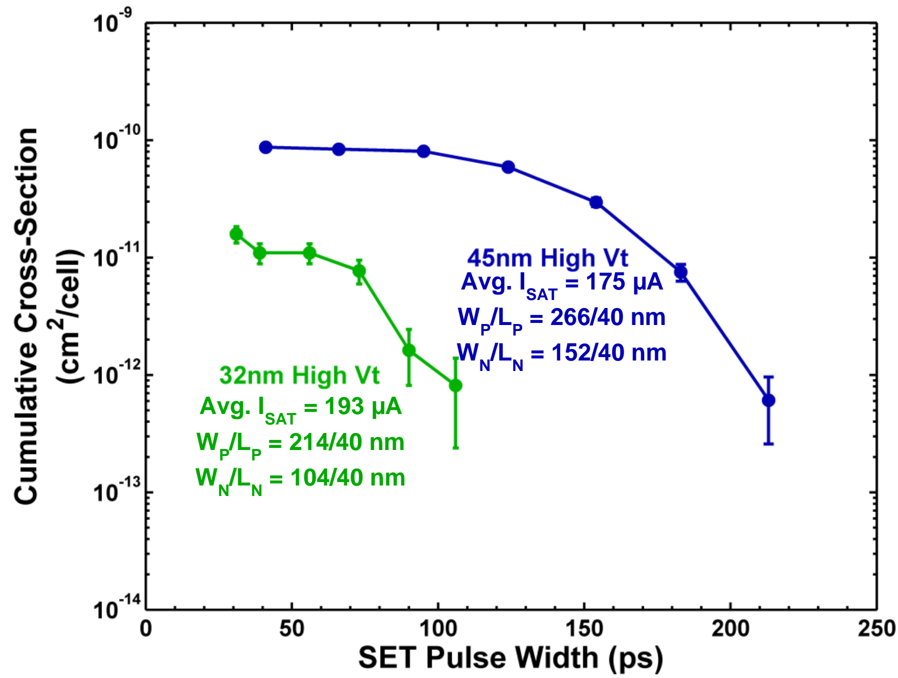

Fig. 16. Impact of technology scaling in high V_T inverters.

Shown in Fig. 17 is the cross-section vs. SET pulse width for two similar thick oxide inverters (target 4 and target 11 from Table 1 and Table 2). The nfet devices of each inverter are almost identically sized, while the pfet device of the 45nm inverter is slightly larger than the pfet device of the 32nm inverter. Both inverters operate at a supply voltage of 1.5 V. Fig. 17 shows exactly the same trend as Fig. 16 in that as SOI technology scales from the 45nm node to the 32nm node, the cross-section and SET pulse width tend to decrease.

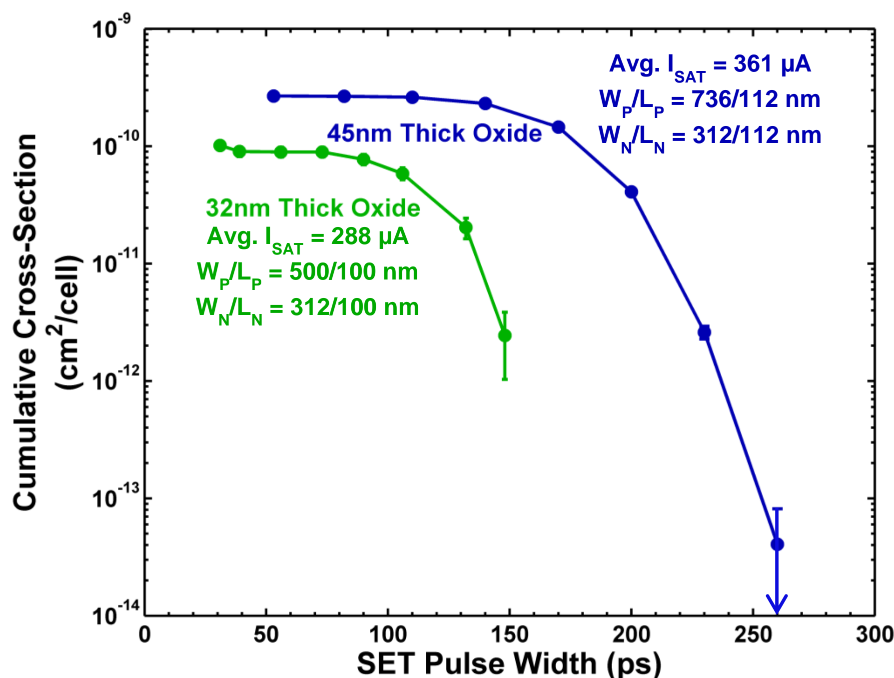

Fig. 17. SET scaling in thick oxide inverters

The simulated scaling trends in [22] were due to decreasing body thickness. However, both the 32nm and 45nm technologies are believed to have the same body thickness although this has not been verified. Thus the scaling effect seen here is possibly not due to decreasing body thickness. The 32nm technology does have a higher operating frequency and drive strength than the 45nm technology. It is likely that the device properties influencing the higher operating frequency and drive strength are also the same properties that cause a decrease in the SET pulse width from 45nm to 32nm. This can be understood by considering what affects charge collection and the charge dissipation rate in each of the devices. Both devices are geometrically similar, which means that they would have similar bipolar amplification of charge. This leads to the devices having a similar charge collection since bipolar amplification is one of the main contributors to charge collection in PDSOI. The charge dissipation rate is determined by the drive

strength of the device since current is just the time rate change of charge. Since the 32nm devices have higher restoring currents or drive strengths than the geometrically equivalent 45nm device, the 32nm device has a higher charge dissipation rate. This increased charge dissipation rate causes the transients to be shorter in 32nm than 45nm SOI since they have similar charge collection. One possible explanation for the decrease in cross-section from 45nm to 32nm is that the 32nm may have a higher threshold LET which would decrease the relative cross-section from 45nm to 32nm for a given LET. The cross-section vs. LET for targets 3 and 10 are shown in Fig. 18 and Fig. 19 [23]. The 45nm cross-section seems to saturate between an LET of ~20 to 30 MeV-cm^2/mg while the 32nm cross-section does not saturate up to an LET of ~ 60 MeV-cm^2/mg.

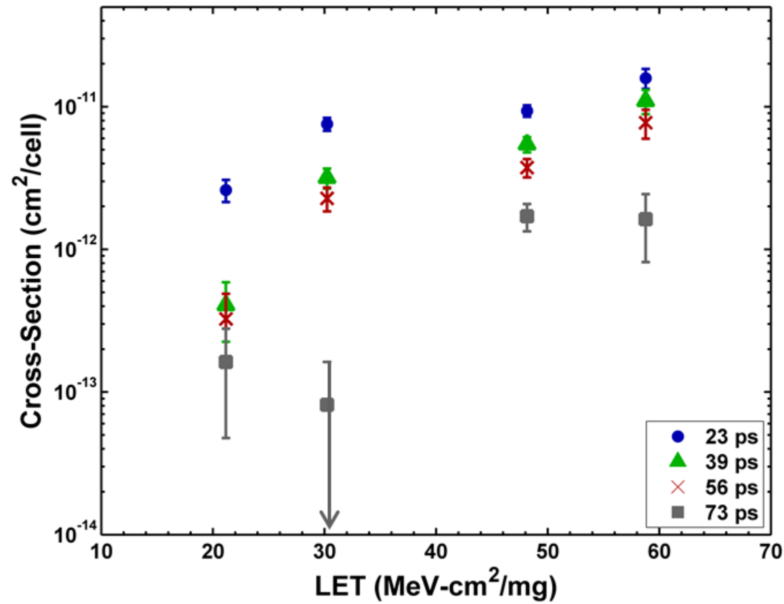

Fig. 18. Cross-section vs. LET for a minimum sized, high-threshold voltage floating-body inverter in 32nm SOI.

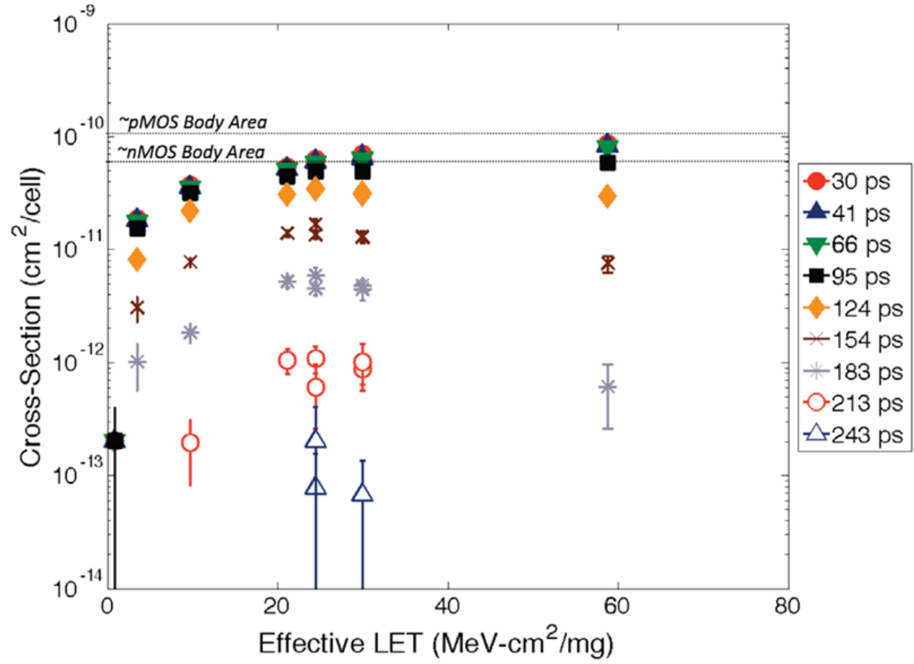

Fig. 19. Cross-section vs. LET for a minimum sized, high-threshold voltage floating-body inverter in 45nm SOI [12].

Effect of PDK MOS Variants and Layouts on SET Distributions

It is often the case that the heavy-ion induced SET response of a particular technology is represented with data collected from elementary devices [21]. While this is often a good first look a technology's SET response, it is not representative of the complete SET response of a technology due to the effect that PDK-standard MOS variants and layout variations such as threshold voltage, body contact, and oxide thickness can have on the SET distributions. Seen in Fig. 20 is the cumulative cross section for several inverter targets representing a variety of standard MOS design parameters available in the 32nm and 45nm PDKs. Table 1 and Table 2 summarize the devices represented in Fig. 20. It is clear that, within a single technology, both the cross section and pulse width cover a broad range of values due to PDK-standard MOS variants and layout techniques such as those mentioned above. In order to rule out any statistical error caused by chip to chip variation, the same target was irradiated on two separate test die. The observed variation between chips was less than the variation due to device parameters.

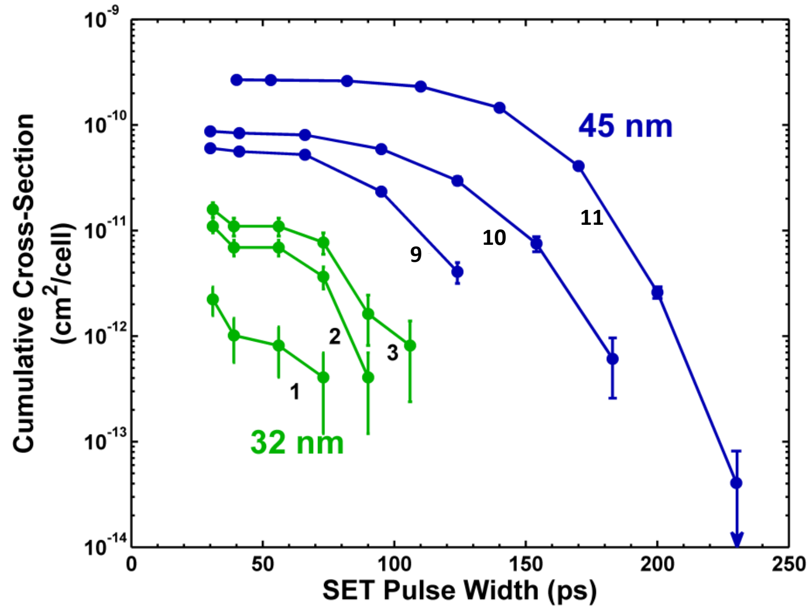

Fig. 20. Variation in SET response due to several different PDK device variants. See Tables I and II for device details.

Body Contact

One choice a designer has when creating a circuit is whether or not to use a body contact. Body contacts help to stabilize the potential in the body, thus reducing a number of negative effects that are inherent to a floating body device. Two typical tradeoffs of including a body contact are reduced switching speed and increased area. One major advantage of a body contact in radiation hardened designs is that it reduces the amount of charge collected after a single event. It does this by reducing or preventing the turn on of the parasitic bipolar that is inherent in SOI. Reduced charge collection lead to a lesser single event effect. Fig. 21 gives experimental evidence to the fact that a body contact provides an improvement in the single event response of a device. Both devices are identical analog devices (Table 1 ref. 5) except that one includes a body contact to the source (or power rail). The floating body device produced 56 transients with the longest

transients being ~106 ps long. The body-contacted device produced only 3 transients when irradiated to the same fluence, with the longest transient being only 56 ps long. Clearly, the body contact is effective in reducing the SET pulse widths. Also, the data suggests that the charge collection in these devices is dominated by the charge enhancement due to the parasitic bipolar.

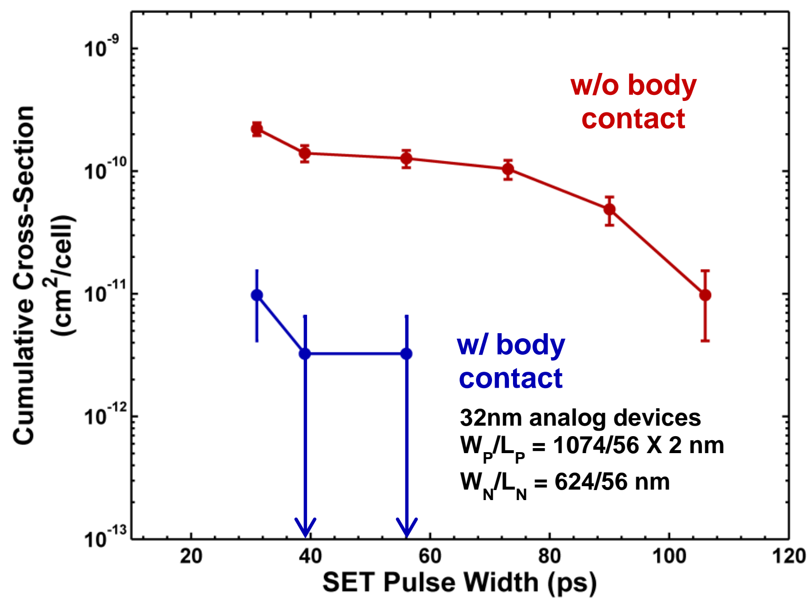

Fig. 21. Reverse cumulative cross section for 32nm analog devices. Only 3 events were measured for the body contacted device compared to 56 events for the floating body device. See Table 1 Ref. 5 for device information.

The effect of the body contact was also measured using 45nm devices. The cross-section vs. SET pulse width curves are shown in Fig. 22. All are thick oxide devices. The highest number of counts corresponds to a thick oxide, floating-body inverter with one finger, while the other distributions is for a body contacted device having two fingers (Table 2 Ref. 12). Once again the body-contacted device shows an improved single event response compared to the floating body devices. The improvement is not quite as drastic

as the 32nm case in Fig. 21. Another floating-body vs. body contacted test was done using analog devices in the 45nm technology. The results from this test are shown in Fig. 23. The analog devices, which are geometrically identical except for the body contact, show a very similar SET response. Upon closer examination, it is clear that the body-contacted devices actually produced a higher number of long transients than the floating-body device which is evidenced by the increase in cross-section at ~170 ps. The increase in the number of long transients is most likely due to the fact that the body contacted device has a slightly lower restoring current than the floating-body device. This result raises the question of the effectiveness of the body contact in 45nm SOI.

Although the thick oxide devices showed an improved SET response with a body contact, the improvement could also be due to geometrical and electrical differences that affect the charge collect and charge dissipation rate. The floating body device in Fig. 22 has a width of 312 nm while the body-contacted device has a finger width of 654 nm with 2 fingers. The width of the affected body strongly determines the amount of bipolar amplification; however, bipolar amplification only occurs in the area of the body that has been modulated. In small devices, the whole body is likely modulated, thus bipolar amplification occurs along the whole width of the device. In wider devices, it is possible that the single event does not modulate the whole body, thus the bipolar amplification is geometrically limited to the modulated region of the body. It is possible that both devices in Fig. 22 have similar charge collection if the bipolar effect is geometrically limited in both devices. Another way to think about this is that both devices are wider than the maximum area that the single event can modulate. If both devices have similar charge collection, then it would make sense that the floating-body device produces longer

transients because it has approximately half the drive of the body-contacted device. Thus, the argument for wider transients is that the floating-body device has a decreased charge dissipation rate but similar charge collection compared to the body-contacted device.

If the above argument is true, then there are two separate tests that show the body-contact is not effective at improving the SET response of 45nm devices. The explanation for this lies in the resistance of the body contact seen along the body of the device. It could be that there is a highly resistive region near the body contact that prohibits the contact from stabilizing the body potential in a timely manner.

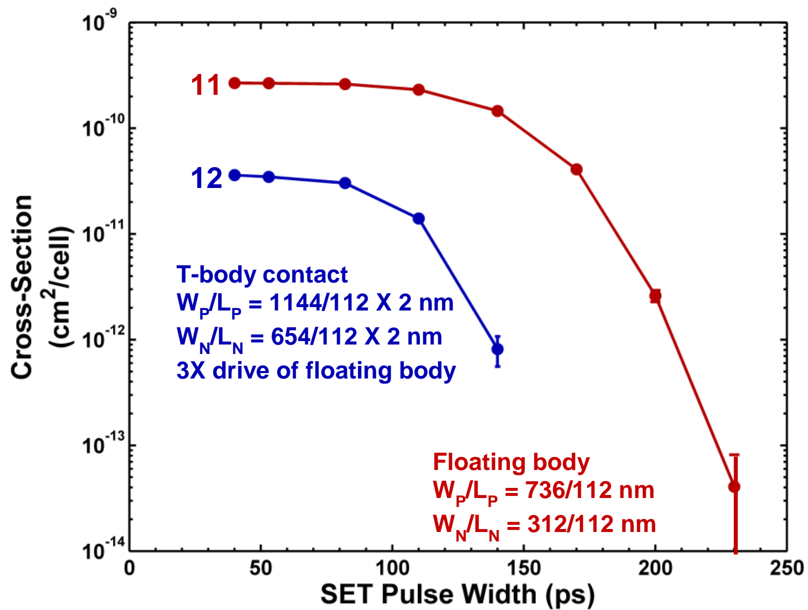

Fig. 22. SET response for 45nm thick oxide devices. See Table 2 Ref. 11 and 12 for device information

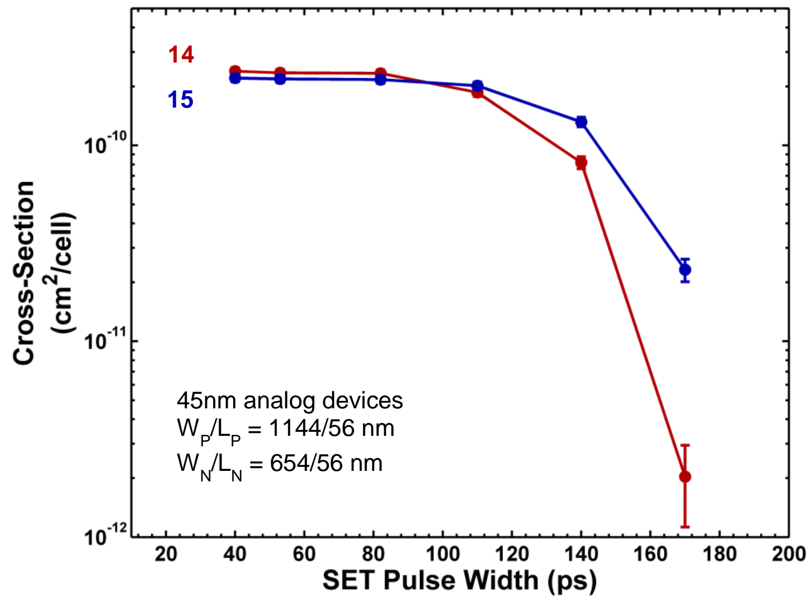

Fig. 23. Reverse cumulative cross section for 45nm floating-body and body-contacted analog devices.

Threshold Voltage

Modern PDKs offer designers a variety of different levels of threshold voltage for a device. Data was obtained for 3 of 5 different V_T variants available in the 32nm and 45nm PDKs. The reverse cumulative distributions for all 6 targets are shown in Fig. 24. Within each technology, a general trend of increasing maximum pulse width with increasing threshold voltage is seen.

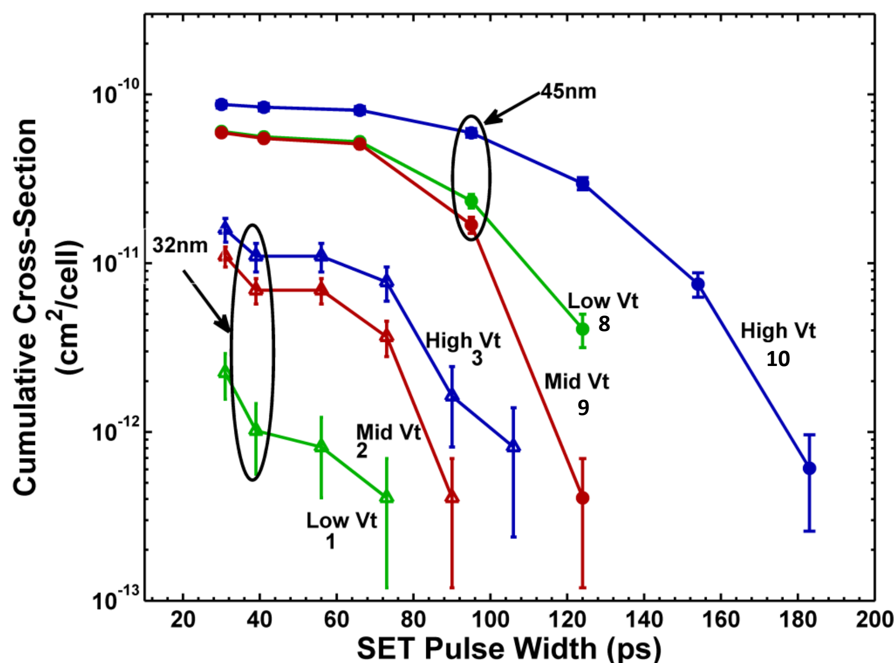

Fig. 24. Reverse cumulative cross section for several different threshold voltage devices at both the 32nm and 45nm technology nodes. The number next to each curve corresponds to the reference number in Table 1 and Table 2. The 45nm devices have W_P/L_P = 266/40 nm and W_N/L_N = 152/40 nm. The 32nm devices have W_P/L_P = 214/40 nm and W_N/L_N = 104/40nm.

One explanation for the increased pulse widths with increasing V_T is that the charge dissipation rate decreases with increasing V_T while the charge collection remains constant. Bipolar amplification plays a significant role in the charge collection process. The amount of bipolar current is strongly dependent on the width of the device. Since, the threshold variants tested had the same device geometry (within each technology), it is reasonable to assume that they have a similar bipolar effect. Thus, it is also reasonable to assume that each device will have similar charge collection. The most important factor that the threshold voltage varies (concerning SETs) is the current through the device. As the threshold voltage increases, the current for a given bias decreases. This decrease in current corresponds to a decrease in the charge dissipation rate of the device after a single

event. To summarize, if device geometry is held constant while the threshold voltage is increased, then charge collection will be constant but the charge dissipation rate will decrease. Thus, higher threshold voltage devices produce longer SETs than devices with lower threshold voltages.

Device Width

It is often the case that designer needs to scale a transistor up from the minimum size, say in order to accommodate a larger load. Increasing transistor size is done by increasing the width. In order to measure the effect that increasing transistor width has on the SET response, both a 1X and 3X sized device were tested. 1X and 3X refer to the width of the device relative to the minimum width available in the technology. Increasing the device width impacts both the single event charge collection via increased bipolar current and the charge dissipation rate via increased drive strength. The results from this test can be seen in Fig. 25. There are two noticeable differences in the SET response of these two devices. (1) The cross-section for the 1X device is drastically lower than the cross-section of the 3X device. Although the 3X device does have a physically larger cross-section (3X larger actually), this alone does not completely explain the difference. It is important to note that these cross-sections are for measured transients, not all transients. It is very likely that the 1X device was producing many more transients that were below the measurement threshold of the test chip. This is evidenced by the fact that the cross-section vs. SET pulse width curve has not saturated at the lowest measured pulse width. (2) The 3X device produced transients over a much larger range (23-106 ps) compared to the 1X device which only produced transients from 23-73 ps. Although the

3X device has three times the drive strength of the 1X device (increased charge dissipation rate), it still produced longer transients. This has to be due to the 3X device had increased charge collection. Since the 3X device is wider than the 1X device, it would have increased bipolar current after a single event. Thus, this test suggests that increasing the width enhances charge collection more so than it enhances the charge dissipation rate.

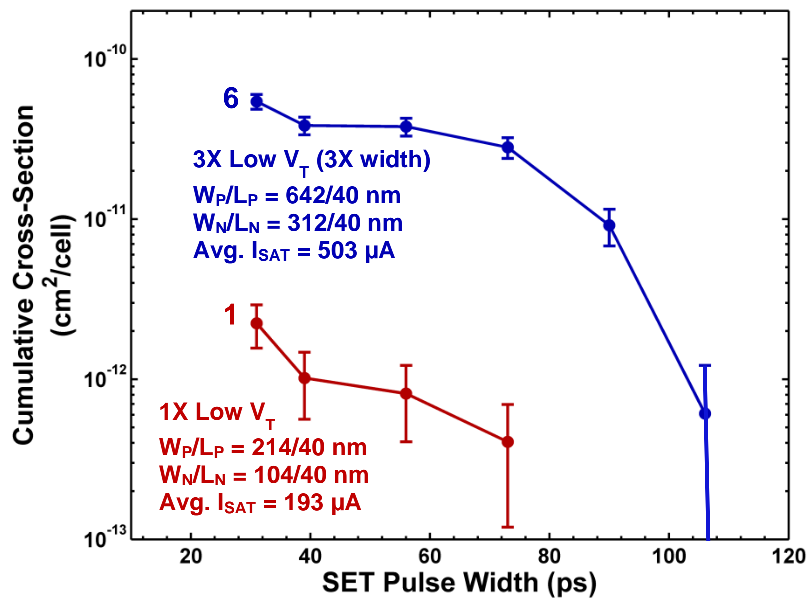

Fig. 25. Reverse cumulative cross section for 32nm 1X and 3X devices.

Folding

Sometimes a device must be made wider than a specified cell height. In order to accomplish this, a technique called folding is used. Basically, it is a layout technique that allows transistors to be connected in parallel in order to achieve a large overall width. The normal technique is shown in Fig. 26. Neighboring transistors share source/drain areas. Each source, drain and gate is connected to every other source, drain and gate. As

drawn in Fig. 26, the folded device has three times the drive of the non-folded device. In order to test the geometrical influence of folding without a corresponding increase in drive, a folding technique as shown in Fig. 27 was used (source, drain and gate connections not shown for clarity). Here the folded device has three fingers, with a width per finger that is 1/3 that of the non-folded device. This gives both devices an equivalent W/L ratio, thus they only vary in their geometrical layout.

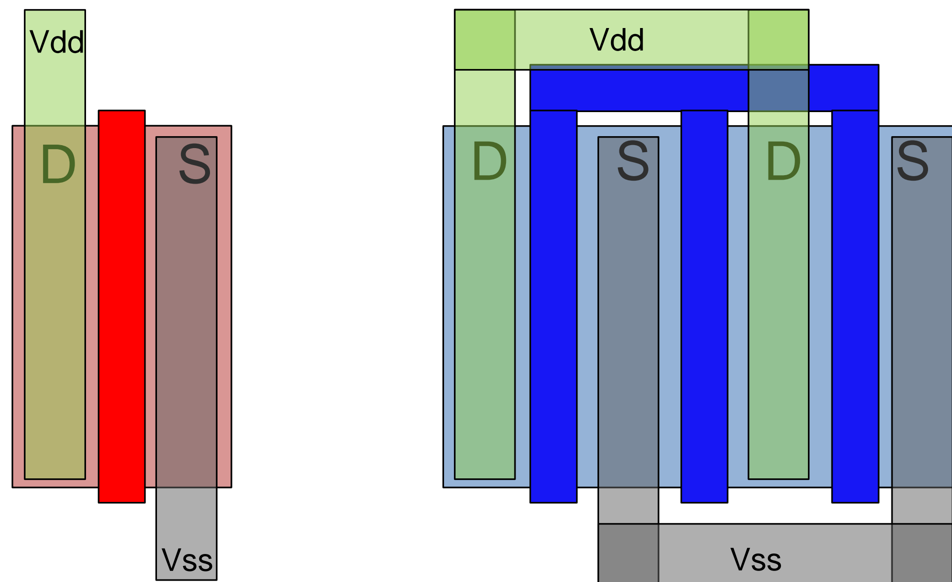

Fig. 26. Layout technique called folding. The device on the left has three times the drive of the device on the left

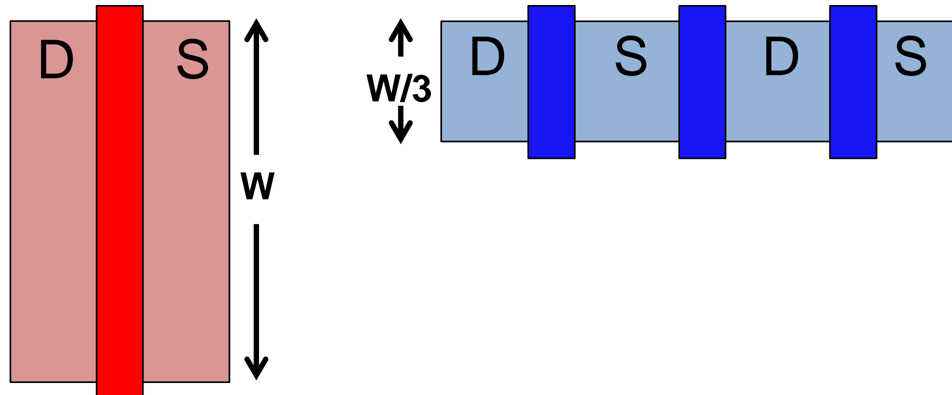

Fig. 27. Alternate folding technique used in heavy-ion tests. Both devices have equivalent drive strengths (W/L ratio).

These devices were irradiated at normal incidence. We have already seen in the previous section that the 3X non-folded device produced a larger range of transients than the 1X device. From the layout in Fig. 27, we can see that the width per finger of the folded device is the same as the width for the 1X device. From this observation, it seems logical that the folded device should produce transients that are in the same range or shorter than the 1X device since the 3X folded device has an increased restoring current. This would in fact be true if the single event affected only one body of the folded device at a time. However, as seen in Fig. 28, the folded and non-folded devices have the same SET response. The only explanation for this is that the single event affected more than one body of the folded device at the same time. This is an interesting result in that it gives us an idea for the effective track radius for the heavy-ion used, Xe. In typical simulations a track radius of 20-50 nm is used. However, in a 2011 paper by Rodbell *et al.*, it was shown that the effective track radius was dependent on the ion. For 10 MeV/u Xe in 32nm SOI, it was determined that the effective track radius was 195 nm in a nFET and 138 nm in a pFET [24]. The nfet of the non-folded device has a width of 312 nm, and the gate to gate pitch (leftmost to rightmost) of the folded nfet is 290 nm. Both of these

measurements fall under the effective track diameter of Xe which is 390 nm. Since the heavy ion is affecting the entire body region(s) in each device, and each device is electrically similar then the results in Fig. 28 do make sense. This also suggests that irradiation with Xe at angle would most likely produce a similar SET response for each device. It is important to note that the folded device had a similar response to the non-folded device for this specific experiment. Generally, if there is enough separation between bodies in the folded device, then a single event would not upset all of the body regions and an improved SET response would be expected. Ions with a smaller effective track radius would also produce the same result if the track radius was below that necessary to upset multiple bodies.

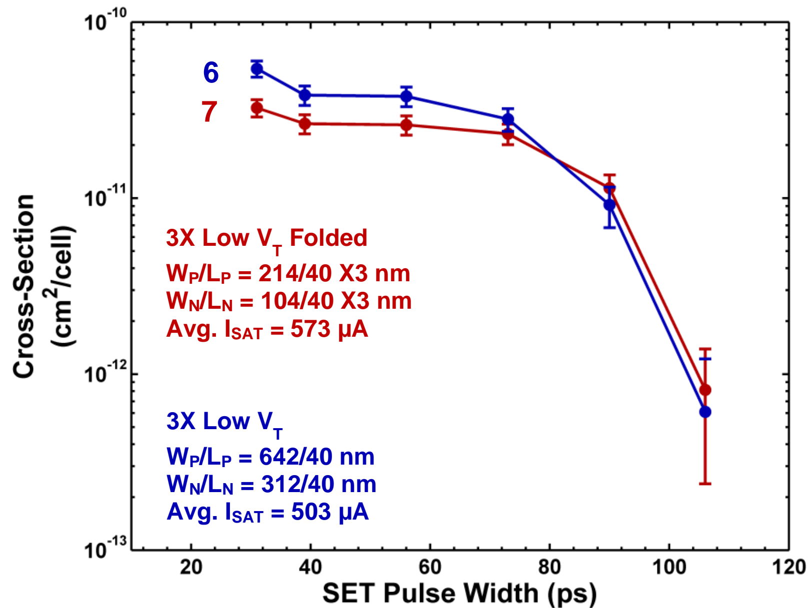

Fig. 28. Reverse cumulative cross section for 32nm 3X folded and non-folded devices at normal incidence.

Cross-section Scaling

SOI transistors are manufactured atop a layer of a buried oxide (BOX) as opposed to bulk technology which is manufactured atop a thick silicon bulk. In bulk the cross-section was highly dependent upon the area of the depletion region between the drain and body; however in SOI the depletion region below the drain does not exist due to the BOX. Therefore, the most sensitive region of a SOI transistor is the area under the gate (commonly called the body). Fig. 29 is TCAD simulation of targets 6 and 7 from Table 1 showing that ion strikes in the center of the gate (body) produce pulse widths that are much higher relative to pulse widths generated from ion strikes in the drain and source areas.

Since the body of the SOI transistor is the most sensitive region, it is logical that the saturated cross-section should be proportional to the area of the body. Fig. 30 shows the cross-section for several 32nm targets. Comparing the average saturated cross-sections of targets 2 and 3 to the average saturated cross-sections of targets 5 and 6, there is a 3.2X increase in the average saturated cross-section. The average body area of the pfet and nfet for targets 2 and 3 is 6.36×10^3 nm^2. For targets 5 and 6 the average body area of the pfet and nfet is 1.91×10^4 nm^2. Thus, a 3X increase in body area corresponds to a 3.2X increase in cross-section. This correlation also holds true when comparing targets 5 and 6 to target 4. The average body area of target 4, 5×10^4 nm^2, is 2.1X larger than targets 5 and 6. The saturated cross-section of target 4 is 2.3X larger than the average saturated cross-section of targets 5 and 6, in good agreement with the increase in body area.

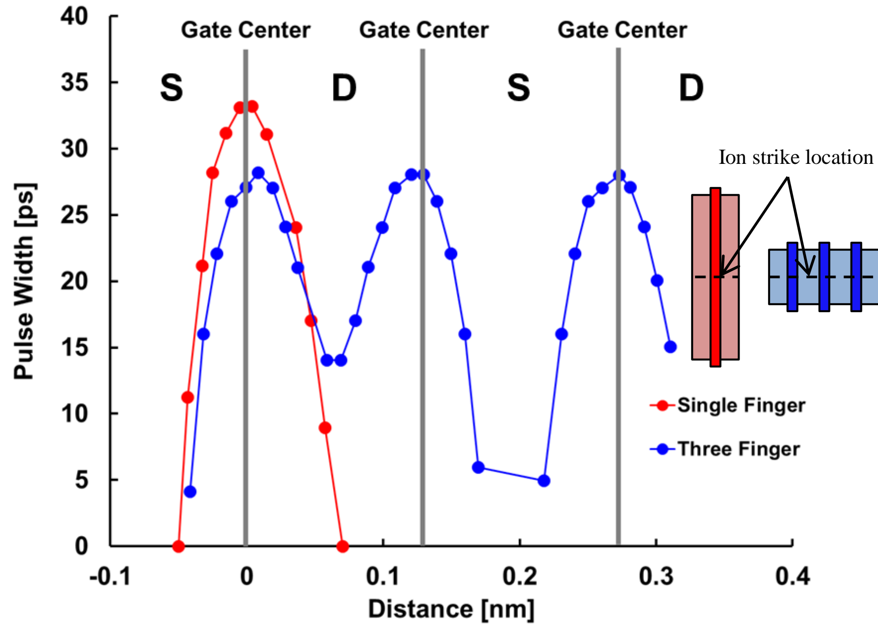

Fig. 29. Relative SET sensitivity of drain, body and source regions of SOI transistor.

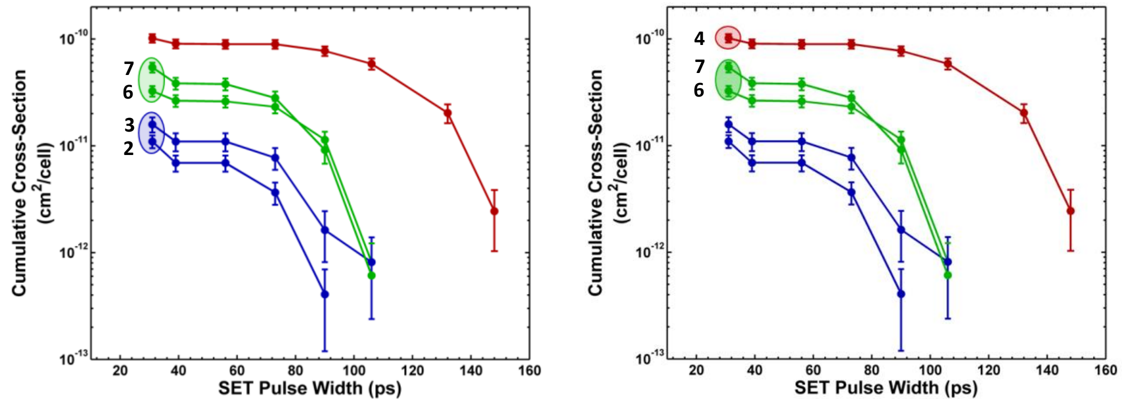

Fig. 30. Reverse cumulative cross section for several different device variants at both the 32nm and 45nm technology nodes. The number next to each curve corresponds to the "Target Reference" in Table I

Design Considerations

Previous work has shown how a distribution of pulse widths for a given device due to a single LET can significantly impact the estimated SET sensitivity of a circuit [19]–[21]. This work shows how the choice of PDK-standard device parameters can significantly impact the SET response of a circuit. To obtain a more quantitative look at

how the threshold voltage can impact the SET sensitivity of a circuit, an example is shown in Fig. 31. From Fig. 31, we can see that for a given cross section of 4x10-11 cm^2/cell, we would need 40 ps more temporal filtering, a 50% increase, to maintain the same cross section if we chose a high threshold voltage for a device as opposed to a mid threshold voltage.

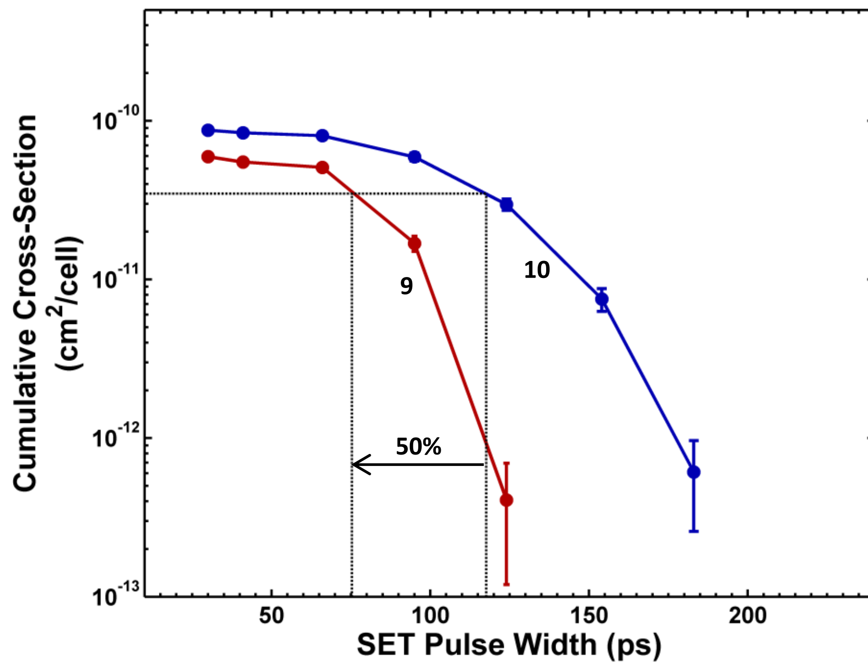

Fig. 31. Example showing the impact threshold voltage can have on the SET sensitivity of a circuit. These are 45nm mid and high threshold voltage devices (targets 9 and 10).

Another example is illustrated in Fig. 32, showing how the cumulative cross section vs. SET pulse width plot can be used to perform a speed/hardness trade-off analysis. Since a device in space will be exposed to a broad range of particles, each with a different LET, it is important that a trade-off analysis include a broad range of LET. Fig. 32 represents data collected from a 45nm, minimum sized, high threshold inverter

target exposed to 4 different heavy-ions at normal incidence: Ne, Ar, Cu, and Xe. In Fig. 32 it is clear that there is much more of a cross-section reduction for a given increase in temporal filtering for regions of high slope than there is regions of less slope. For example, if the temporal filtering is decreased by 50% from 150 ps to 75 ps (increased circuit speed), the trade-off is a 3.5X increase in the cross section of unfiltered transients (reduced reliability) for an LET of 21.2 MeV-cm2/mg. The same analysis may be performed for others values of LET in Fig. 32.

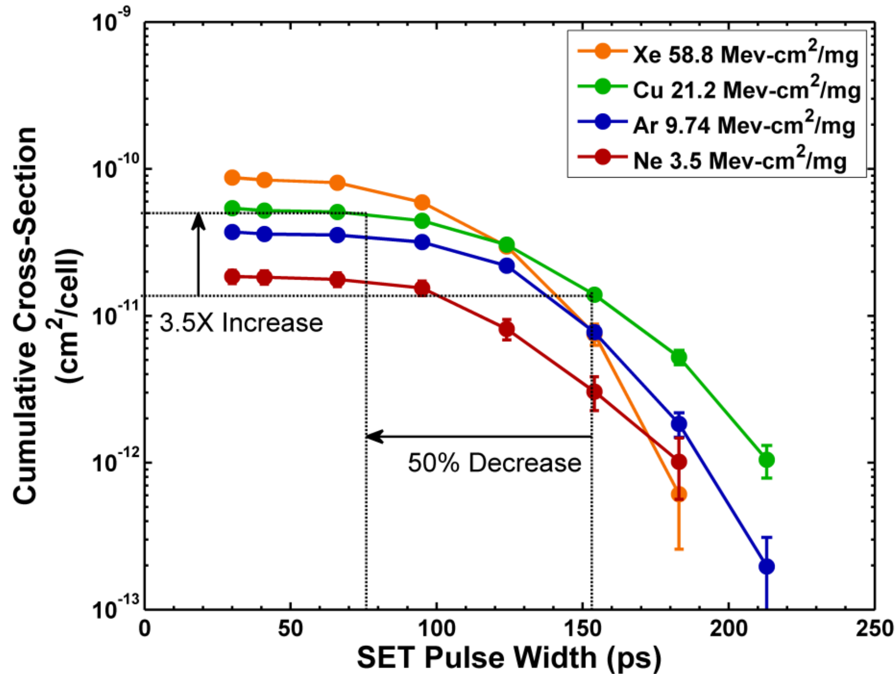

Fig. 32. Example showing the trade-off between cross section and circuit speed. This is for target 10 from Table 2, a minimum sized, high threshold voltage inverter.

CHAPTER VII

CONCLUSIONS

This thesis describes an autonomous SET measurement technique which was implemented in 32nm and 45nm SOI. The measurement technique essentially behaves as a time to digital converter that digitizes the SET pulse width in terms of individual stage delays. Significant attention was given to the errors associated with the measurement technique which included PIPB, RC attenuation, SET concatenation, and digitization uncertainty. Methods for quantifying some of these errors were discussed.

The choice of standard PDK design variants was shown to impact the single event response of devices within a technology. The data collected in this work suggests that the SET response of any variant in a technology is controlled by the countering effects of bipolar amplification and restoring current. The minimum sized, low threshold voltage devices showed the best SET response in both technologies due to their width-limited bipolar charge amplification and high restoring current. The thick oxide devices showed the worst SET response in both technologies due to large widths (more bipolar) and relatively low drive strengths. Body-contacting proved to be useful in SET mitigation at the 32nm node, although it was not effective at the 45nm node. Using a folded layout to increase width did not change the SET response for the specific case tested (3 finger device and Xe ion) due to the fact that the ion was able to upset all three bodies of the folded device simultaneously. Generally, folding would provide an improved SET response if many more fingers were used or if an ion with a lower effective track radius were used.

The cross-section of partially depleted SOI MOSFETs was experimentally shown to change proportionally with the area of the body for device variants within the same technology. Finally, SETs pulse widths were shown to decrease with technology scaling in partially depleted SOI from the 45nm to 32nm technology node for similar devices. This was attributed to a higher current density in the 32nm technology which gives devices a higher charge dissipation rate. This gives hope that future technologies will be even better in their single event response than previous technologies.

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