Temperature and Total Ionizing Dose Characterization of a Voltage Reference in a 180 nm CMOS Technology

By

Kevin Joseph Shetler

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Lloyd W. Massengill

W. Timothy Holman

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CHAPTER 1

INTRODUCTION

A precision voltage reference circuit is an important component of analog/mixed-signal (AMS) systems. It provides a DC output that is used in various other system components, such as bias networks and data converters. When designing a voltage reference, the precision is of critical importance. For example, in order to maintain signal integrity in an analog-to-digital converter (ADC), any shift in the reference output must be less than half of the least significant bit; for an ADC with 8 bits of resolution, this corresponds to approximately 0.2%. A reference circuit must be designed such that its output exhibits minimal change due to external factors, including power supply variation, noise, and temperature. Additionally, in an environment where ionizing radiation is present, it is necessary to minimize shifts in the reference voltage due to radiation degradation.

In this thesis, a voltage reference circuit fabricated in a 180nm process utilizing techniques to minimize any shift in the output voltage due to changing temperature and radiation exposure and was tested. First, a brief background is provided on radiation effects and voltage reference design. This is followed by a presentation of the techniques implemented on the voltage reference test chip. Experimental details and results are presented to verify their effectiveness of these techniques.

CHAPTER II

RADIATION EFFECTS OVERVIEW

In this chapter, background is provided on radiation effects in integrated circuits. The two primary types of radiation degradation are total ionizing dose (TID) and single-event effects (SEEs). TID is the primary focus of this work.

Total Ionizing Dose

In certain environments, such as space, an abundance of ionizing particles exist, and these particles can deposit a significant amount of charge in semiconductor material. This charge accumulates via electron-hole pair generation as ionizing in the semiconductor material. The accumulation of this charge in a circuit or device is referred to as total ionizing dose (TID) and primarily occurs in the insulator oxide, including gate oxides of MOSFETs and the field oxide that separates devices. As radiation does increases, the trapped charge can alter device characteristics and cause degradation in circuit components. [1]–[3]

In bipolar junction transistors (BJTs), the primary negative effects of TID are an increase in leakage current and a decrease in current gain. This occurs because the surface of p-type semiconductor is inverted when enough positive charge is built up in the oxide of an integrated circuit (IC), increasing the number of recombination centers in the emitter-base depletion region. The main cause of current gain decreases is the increase in base current due to the increased recombination [3], [4]. Additionally, BJTs are susceptible to enhanced low-dose-rate sensitivity (ELDRS). The ELDRS effect is when a low dose rate can result in increased degradation than an

equivalent dose at a larger dose rate. This makes it more difficult to assess the behavior of BJT-based circuits in laboratory testing and can lead to greater radiation sensitivity during operation [5], [6].

There are two primary effects of TID in CMOS ICs. The first of these is threshold voltage shifts. Threshold voltage shifts are caused by the accumulation of charge in MOSFET gate oxides. When electron-hole pairs are created in the oxide, the high mobility electrons are sept away, leaving the positively-charged holes to remain in the oxide or semiconductor-oxide interface. The positive oxide-trapped charge causes a negative shift in threshold voltage, making n-type MOSFETs (nFETs) require a lower gate-source voltage to turn off and p-type MOSFETs (pFETs) require a greater source-gate voltage to turn on. However, interface-trapped charge increases the subthreshold swing in MOSFETs. This causes both nFETs and pFETs to require a larger gate-source or source-gate voltage to turn on, an increase in the threshold voltages of nFETs and decrease in that of pFETs. As the thickness of gate oxides has decreased with technology scaling, threshold shifts due to charge trapped in oxides have also decreased, making smaller modern processes increasingly TID tolerant. This is because electrons are more easily able to tunnel through the oxides and recombine with trapped holes. [1]–[3], [7]–[9]

The other primary effect of TID in CMOS ICs is increased field oxide leakage current. When enough positive charge is built up, it can cause inversion in the p-type substrate, allowing

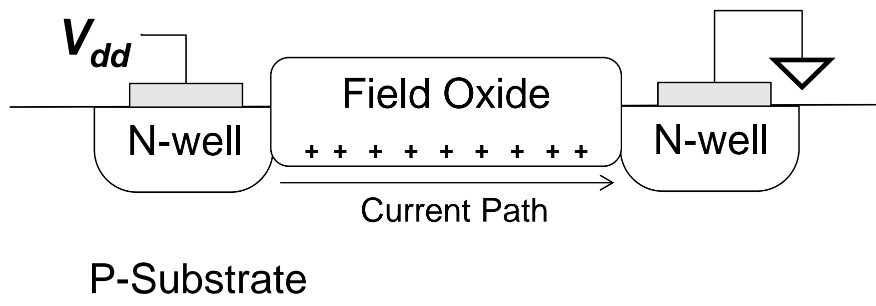

Figure 1: Basic field oxide leakage.

for current to flow. A basic illustration of the current is shown in Figure 1. This can occur between the source and drain of the same nFET or between those of adjacent nFETs. These current increases can have several different negative effects, including increasing bias current and overall supply current and loss of gate control. A common way to minimize leakage current is with transistor layout techniques. One technique is edgeless layout, which eliminates the leakage path between the source and drain around the poly gate at the edges of transistor by increasing the poly length at the edge. Another technique is using p+ guard rings to minimize the inversion that allows current to flow; this makes it necessary for a larger amount of charge to accumulate in order to invert the surface and allow leakage to flow. Unlike gate oxides, field oxides are still quite thick in modern processes, so TID-induced leakage current has not shown the same decreases with technology scaling as threshold voltage shifts. [1]–[3], [8]–[10]

CHAPTER III

VOLTAGE REFERENCE CIRCUITS

A voltage reference is a critical part of many AMS systems because it provides a stable voltage, a global signal used for various system functions, such as quantization of analog signals. Therefore, when designing a typical voltage reference, it is important to minimize variation due to factors such as power supply variability and temperature. This chapter describes a bandgap voltage reference, a basic and commonly used reference design, and a similar CMOS design, which is simpler to implement in standard IC processes and more suitable for radiation tolerant design.

Bandgap Voltage References

An ideal voltage reference exhibits no dependence on temperature. The bandgap voltage reference topology is designed to minimize temperature dependence, based on the predictable temperature dependence of a forward-biased p-n junction. The forward voltage (V_f) of a p-n junction has a negative temperature coefficient (tempco), which is the first order temperature dependence of a voltage, making it a complementary-to-absolute-temperature (CTAT) voltage. Additionally, V_f becomes less negative with increasing current density in the junction. Therefore the difference between the voltages of two p-n junctions of different current densities has a positive tempco and is a proportional-to-absolute temperature (PTAT) voltage. By summing PTAT and CTAT voltages of equal magnitude, a zero tempco (ZTC) can be achieved [11].

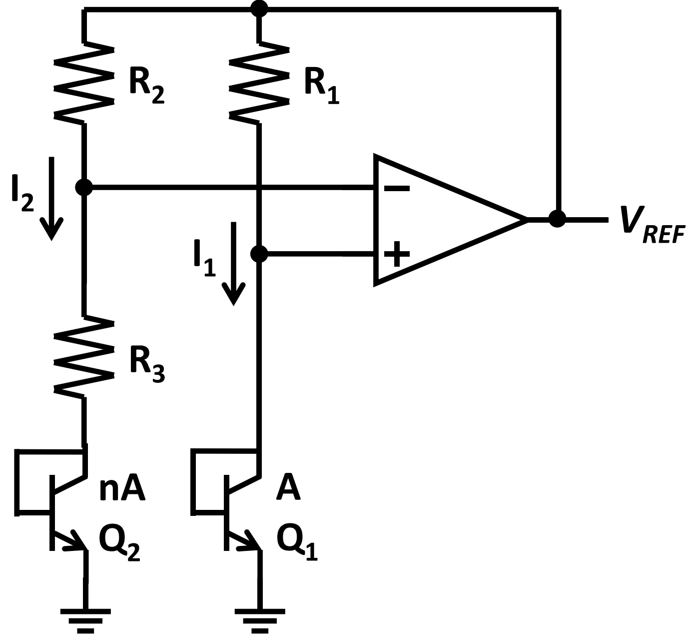

Figure 2: Conventional bandgap voltage reference circuit.

The basic implementation of a bandgap reference is shown in Figure 2. The forward-biased p-n junctions are implemented using diode-connected npn bipolar junction transistors (BJTs) [12]. The BJT Q_2 is scaled to be n times the area of Q_1. The resistors R_1 and R_2 are matched, so due to the high gain of the op amp forcing the two input voltages to be nearly identical, the currents I_1 and I_2 are through the resistors are assumed to be equal. The voltage reference output (V_{REF}) can be expressed as:

$$V_{REF} = V_{BE2} + (R_2 + R_3)I_2, \tag{1}$$

and the currents I_1 and I_2 can be expressed as:

$$I_1 = I_2 = \frac{V_{BE1} - V_{BE2}}{R_3}. \tag{2}$$

Using the current-voltage characteristics of a forward-biased diode connected BJT, expressions for V_{BE1} and V_{BE2} can be derived as:

$$I = I_S e^{\frac{qV_{BE}}{kT}}, V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_1}{I_S}\right), V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_1}{nI_S}\right). \tag{3}$$

Combining (2) and (3), I_2 can be expressed as:

$$I_2 = \frac{1}{R_3}\frac{kT}{q}\left[\ln\left(\frac{I_1}{I_S}\right) - \ln\left(\frac{I_1}{nI_S}\right)\right] = \frac{1}{R_3}\frac{kT}{q}\left[\ln\left(\frac{I_1}{I_S}\right) - \ln\left(\frac{I_1}{I_S}\right) + \ln(n)\right] = \frac{1}{R_3}\frac{kT}{q}\ln(n). \quad (4)$$

Because of the identical currents I_1 and I_2, and sizing difference in the transistors Q_1 and Q_2, represented by the n term in the equation for V_{BE2} in (3), the transistors have different current densities and temperature coefficients. This allows for a PTAT voltage to be generated using the difference between the transistor base-emitter voltages, which are CTAT voltages. Combining (4) with (1), the reference output V_{REF} is:

$$V_{REF} = V_{BE2} + \frac{R_2+R_3}{R_3}\frac{kT}{q}\ln(n). \quad (5)$$

The first term of this equation is a CTAT voltage because the tempco of V_{BE2} is negative, and the second term is a PTAT voltage, as the temperature seen directly in the term. Therefore, if the resistors and transistors are sized appropriately, first order tempco cancellation can be achieved. The circuit is called a bandgap reference because, when designed properly, its output is approximately 1.2 V, nearly the bandgap voltage of silicon.

Despite minimizing the first-order temperature dependence in a bandgap reference, the precision is still limited by second-order dependence. This causes some curvature in the reference output in relation to temperature, leading to a small positive or negative temperature dependence at temperatures above or below the ZTC temperature, the temperature point where first order tempco cancellation is achieved and the tempco is zero. Various techniques have been developed to correct this second-order curvature and increase the range of temperature cancellation [13], [14].

Integrated CMOS Voltage References

A design similar to the bandgap reference can be implemented using integrated CMOS devices. For the purposes of this work, it allows for the design to use MOS devices as a low-voltage replacement for the BJTs in the previous design and leverage the increasing radiation

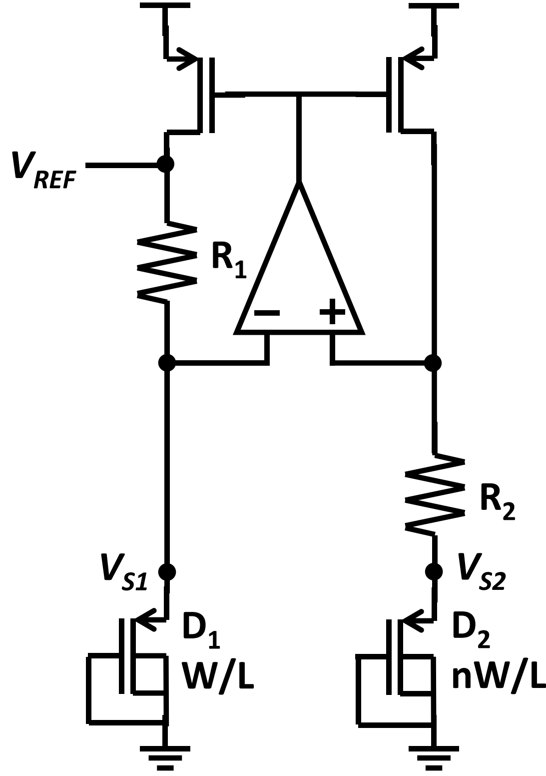

Figure 3: CMOS bandgap voltage reference circuit using dynamic-threshold MOS transistors (DTMOSTs).

tolerance with technology scaling of modern CMOS IC processes. An example of this type of design is shown in Figure 3. The design uses a p-type MOSFET (pFET) current mirror to source identical current through scaled dynamic-threshold MOS transistors (DTMOSTs), which create the necessary p-n junctions for first-order tempco cancellation. DTMOSTs are simply pFETs with the gate and body connected; in this case the DTMOSTs are diode-connected devices, so the drain is also connected to the gate, as would be in any diode-connected pFET. The DTMOST has demonstrated superior radiation hardness compared to typical n- and p-type MOSFETs [15]–[17], so it is particularly suitable for this work; this is discussed further in Chapter V.

The reference output of the circuit in Figure 3 can be expressed as:

$$VREF = V_{S1} + \frac{R_1}{R_2}(V_{S1} - V_{S2}). \tag{6}$$

As with a diode-connected BJT, the tempco of the source voltage of single DTMOST is negative and becomes more negative with decreasing current density. Therefore, if the current density in M_2 is less than that of M_1, the tempco of the voltage $(V_{S1} - V_{S2})$ is positive, and the resistors R_1 and R_2 can be scaled to achieve first-order tempco cancellation. In this circuit, the different current densities in the DTMOST reference devices are achieved by scaling the widths of the two devices by a factor of n. This design is the basis for the voltage references tested in this work.[18]

Additionally, the voltage reference circuit of Figure 3 can also be implemented using diode-connected nFETs or pFETs to create the necessary p-n junction in place of the DTMOSTs. The equation for the reference voltage is calculated in the same way as that of the DTMOST-based reference. These reference designs are not as suitable for a radiation tolerant reference however, because the radiation tolerance of typical n- and p-type MOSFETs is inferior to DTMOSTs.

CHAPTER IV

TEMPERATURE EFFECTS IN VOLTAGE REFERNCES

One of the most important design considerations for all voltage reference circuits is minimizing the variation of the output with changes in temperature. There are various techniques that can be implemented, including the first-order temperature coefficient (tempco) cancellation of the bandgap reference topologies discussed in Chapter III. In this chapter, a description and experimental results are presented for a voltage reference fabricated in an IBM 180nm process that incorporates two techniques to minimize temperature effects.

First-Order Temperature Coefficient Cancellation

The fully integrated voltage reference circuit tested in this work was fabricated in 180nm IBM CMRF7SF technology. The reference core of the circuit is shown in Figure 4. This design is very similar to the design of Figure 3, with a few minor changes, primarily motivated by the desire for increased radiation tolerance. One change is the replacement of the typical p-type MOSFET (pFET) current mirror with a resistive current mirror, using a single pFET and the scaled resistors R and $R/2$. The gain of the op amp forces an equal voltage drop across the two resistors, so the currents through the two branches of the circuit are scaled by 2. Along with this, the dynamic-threshold MOS transistor (DTMOST) reference devices are of equal size; however, the DTMOST current densities are still different because the currents are scaled rather than identically sourced, so first-order tempco cancellation can still be implemented in a similar way as before, using the sum of a p-n junction forward voltage – negative tempco – and the difference between the voltage

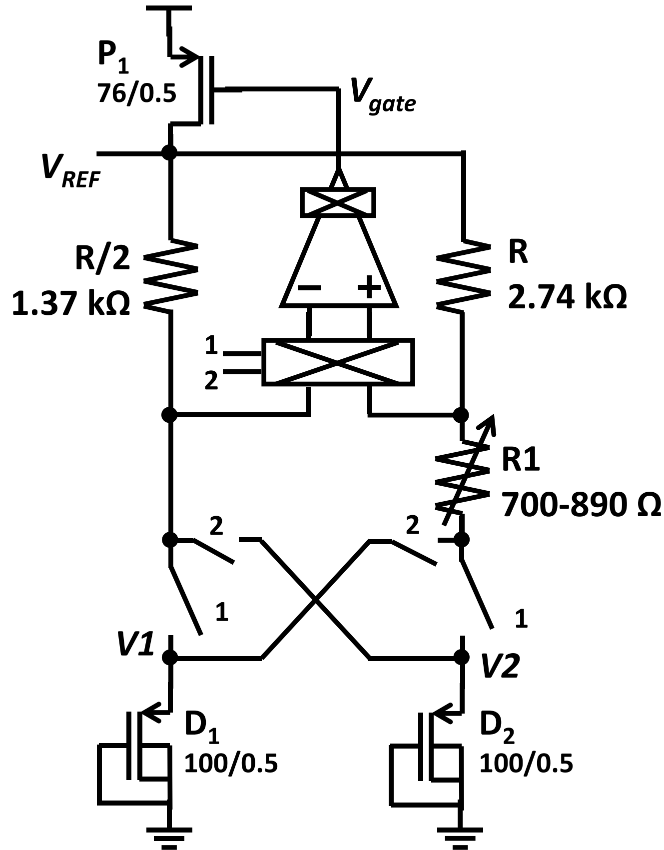

Figure 4: Voltage reference core circuit on 180nm IBM CMRF7SF test chip.

of two p-n junctions with different current densities – positive tempco. Finally, chopper stabilization, a method of dynamic offset cancellation, is incorporated in both the DTMOST reference devices and op amp. The use of chopper stabilization does not affect the basic functionality of the circuit. The benefits of both the resistive current mirror and chopper stabilization for radiation tolerance are discussed in Chapter V. [18]

The reference output (*VREF*) of the circuit of Figure 4 is the same as that of Figure 3 and is expressed as:

$$VREF = V1 + \frac{R}{R1}(V1 - V2). \tag{7}$$

As in (6), *V1* has a negative tempco and *(V1 – V2)* has a positive tempco, so the resistances can be scaled for first-order tempco cancellation. The resistor R1 can be adjusted using a 6-bit digital

trimming scheme, therefore adjusting the R/R1 ratio as well. This way, the optimal value for R1, the resistance that leads to the smallest change in the output voltage throughout the desired temperature range, can be determined experimentally. The op amp of the circuit is a p-input operational transconductance amplifier (OTA) with chopper stabilization; the design is discussed further in Chapter V.

The digital trimming scheme can be implemented using either a series or parallel scheme [18]. In a series scheme, a number of resistors is connected in series with a n-type MOSFET (nFET) in parallel with each; the number of resistors should be one greater than the number of bits desired. When one of the nFETs is turned on with a digital "1" input, all current is diverted from the corresponding resistor; all "1" inputs lead to the minimum resistance, and all "0" inputs lead to the maximum resistance. An example schematic of a 4-bit series digital trimming scheme is shown in Figure 5. The least significant bit (LSB) resistance is equal to the difference between the desired maximum and minimum resistances divided by 2^n, where n is the number of bits. The resistance of each resistor is twice that of the prior resistance, so the most significant resistance is equal to the LSB resistance times 2^{n-1}. In this trimming scheme, the W/L ratios of the nFETs must be fairly large to minimize their ON resistances, because no current should flow through the resistors, which is achieved with a zero resistance in the ON nFETs. [18] In the parallel trimming scheme, a number of branches are connected in parallel, each containing a nFET and resistor connected in series. An example of a 4-bit parallel trimming scheme is shown in Figure 6. In this scheme, when a nFET is turned on with a high digital input, the branch no longer has infinite resistance, and the corresponding resistor becomes part of a parallel combination, decreasing the overall resistance. In the parallel scheme, the maximum resistance is the sum of the resistors R_S and R_P, and the minimum resistance is the sum of R_S and the parallel combination of R_P and R_{lsb},

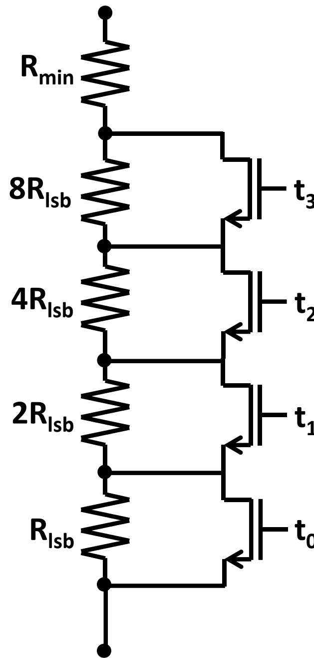

Figure 5: Series digital trimming scheme.

the LSB resistance. Additionally, the W/L ratios do not need to be as large because the ON resistance only needs to be sufficiently lower than its corresponding resistor. For the circuit of interest in this work, radiation tolerance is the most important consideration when choosing which trimming scheme to use. The parameter affected most significantly by radiation exposure is the ON resistance of the nFET switches due to threshold voltage shifts. The ON resistance of the switches is a much more critical factor in the series scheme, because the current must be completely diverted, where in the parallel scheme each branch is easily dominated by the resistors. When the difference between the minimum and maximum resistance and the LSB resistance are small, a parallel scheme is optimal because the nFET switches in a series scheme would need to be very large. [18] For this reason, a parallel trimming scheme was used for the resistor R1 in Figure 4 on the 180nm voltage reference chip tested, where the difference between the maximum

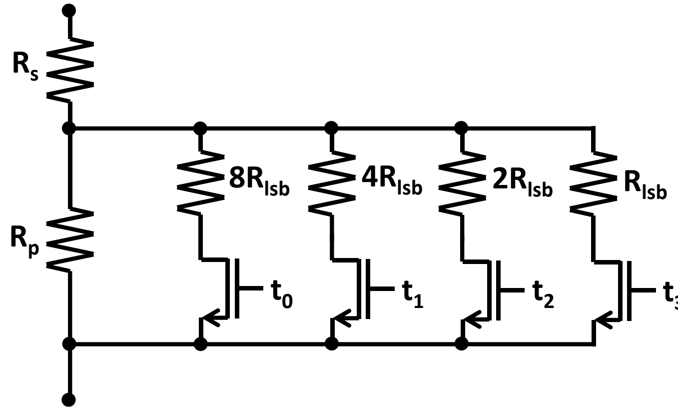

Figure 6: Parallel digital trimming scheme.

and minimum resistances is only 190 Ω. Additional details on the digital trimming schemes and guidelines for use in a radiation hardened circuit can be found in [18].

The temperature response of the voltage reference was tested using the TestEquity Model 140 temperature chamber. The test chip was bonded in a package and connected to a custom printed circuit board (PCB), which was placed in the chamber. Six different temperatures were chosen for the experiment: 37.5˚C, 50˚C, 62.5˚C, 75˚C, 87.5˚C, and 100˚C. At each temperature, the ambient temperature of the chamber was allowed to settle, and each of the 64 trim codes for the trimmable resistor R1 were applied and the reference output measured for each trim code; at each temperature, 100 measurements were made, and the average and standard deviation were calculated afterwards. The measurements were taken using the HP 34401A 6 ½-digit multimeter, which can provide accuracy up to thousandths of millivolts in the voltage range of the voltage reference output – hundreds of millivolts [19]. This experiment both demonstrates the effectiveness of first-order tempco cancellation in the voltage reference, as well as determines the optimal trim code for minimum voltage reference variation across the desired temperature range.

The temperature response of the voltage reference at various trim codes for the 6-bit trimmable resistor R1 is plotted in Figure 7. The figure shows every fourth trim code plus the

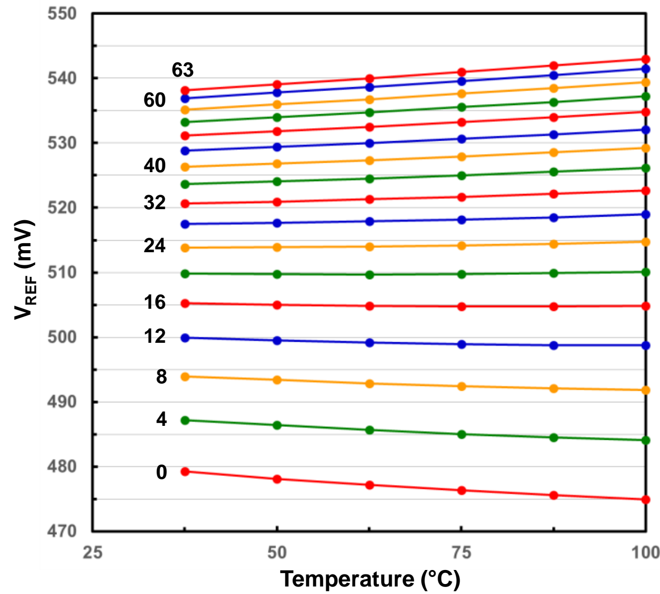

Figure 7: Temperature response of 180nm voltage reference circuit for every fourth trim code, across complete range of codes.

maximum, and the labels represent the decimal value of the binary code. The standard deviation is not plotted because it would be completely hidden by the data points; the largest standard deviation for any of the measurements made was less than 0.05 mV. This plot shows how decreasing the resistance of R1 – by increasing the trim code – causes an increase in the slope of the temperature response of the voltage reference. From this plot, it appears visually that the trim codes in the range of a decimal value of 16 to 20 lead to the smallest variation in the reference output voltage throughout the temperature range, so the optimal trim code for minimizing output variation due to temperature is likely in this range. In Figure 8, data from the same reference is plotted, limited to the trim codes from 14 (001110) to 22 (010110). Additionally, the maximum variation over the complete temperature range for each of these trim codes, along with the maximum and minimum codes, is shown in Table 1. The table and plot show that applying a trim code of 18 (010010) leads to a maximum variation in the reference voltage across the complete temperature range of 0.263 mV. This the smallest variation for any trim code and confirms what

Table 1: Maximum reference variation over temperature range for selected trim codes from voltage reference of Figure 8.

Trim Code	Binary	Max Variation (mV)
0	000000	4.288
14	001110	0.812
15	001111	0.653
16	010000	0.498
17	010001	0.373
18	010010	0.263
19	010011	0.308
20	010100	0.414
21	010101	0.503
22	010110	0.619
63	111111	4.782

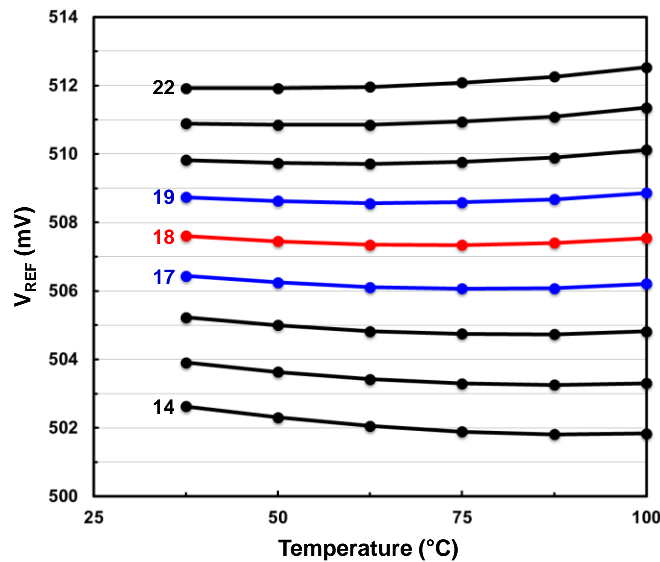

Figure 8: Temperature response of 180nm voltage reference circuit for trim codes from 14 (001110) to 22 (010110). This is the range of trim codes where the overall temperature variation is smallest.

was observed visually in Figure 8. Based on the output at 37.5˚C of 507.606 mV, this a maximum shift of only 0.05%. This is significantly better than a maximum variation of 4.288 mV (0.84%) for a trim code of 0 (000000) and 4.782 mV (0.94%) for a trim code of 63 (111111); this demonstrates the effectiveness of proper resistor scaling for first-order tempco cancellation. The

Table 2: Maximum reference variation over temperature range for selected trim codes from voltage reference of Figure 9.

Trim Code	Binary	Max Variation (mV)
19	001011	0.690
20	001100	0.528
21	001101	0.382
22	001110	0.236
23	001111	0.123
24	010000	0.130
25	010001	0.281
26	010010	0.436
27	010011	0.727

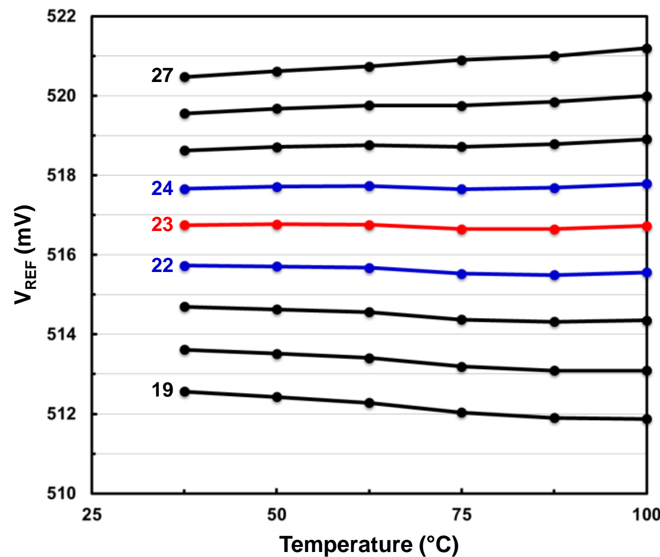

Figure 9: Temperature response of a second 180nm voltage reference circuit for trim codes from 19 (010011) to 27 (011011). This is the range of trim codes where the overall temperature variation is smallest.

data in Figure 8 also shows some curvature due to second-order temperature dependence. However, between the curves of Figures 7 and 8, it can be seen the first-order dependence is the dominant factor in the overall temperature dependence.

The temperature response of an additional voltage reference chip tested in the same way is plotted in Figure 9; the plot shows trim codes from 19 (010011) to 27(011011). Table 2 shows the

maximum reference output variation across the temperature range for each of these trim codes. These show that a trim code of 23 (010111) is optimal for this circuit, leading to a maximum variation of 0.123 mV (0.02%). As with the data for the first chip, this shows the effectiveness of first-order tempco cancellation with proper resistor scaling and the slight curvature due to second-order effects. Additionally, the experiment on a second chip shows that another benefit of the digital trimming scheme is the ability to account for process variation. The difference between the optimal trim codes for the two reference circuits is 5, so if the circuit was designed with a simple resistor, it is likely that the first-order tempco cancellation could not be adjusted to minimize variation and would be less effective that a design using a digitally trimmed resistor, and there would be significant chip-to-chip variation.

Temperature Regulation

The voltage reference circuits tested in this work also employ a method of thermal regulation that can reduce the effects of second-order tempco drift in references that employ a first-order bandgap design. This is done using a feedback loop and an on-chip heater to maintain the on-chip temperature, rather than only minimizing variation due to the external temperature.

The basic concept of the thermal feedback is a heater driven by an op amp; one of the op amp inputs is temperature dependent and set to be equal to the other input at the desired set temperature point. This way, at temperatures lower than the set point, there is a difference between the op amp inputs, driving the heater and increasing the temperature. This continues until the chip reaches the desired temperature, where the op amp inputs are equal. Combining this feedback with first-order tempco cancellation, the temperature variation can be reduced significantly. A basic overview of how this feedback is implemented is shown in Figure 10 with the heater represented

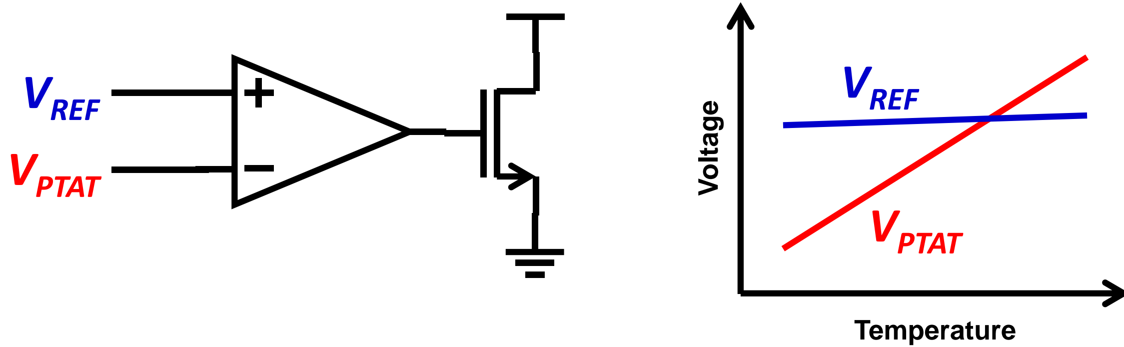

Figure 10: Basic overview of thermal feedback technique. The two input voltages of the op amp driving the nFET heater are set to be equal at the desired feedback temperature.

by a n-type MOSFET (nFET); one of the op amp inputs is a proportional-to-absolute-temperature (PTAT) voltage, and the other is the reference voltage output. The region of the graph to the left of the intersection of the two lines is where the heater is active, and as the difference between the two voltages increases, the amount of heat required does as well. [18]

Figure 11 shows the additional circuitry connected to reference core from Figure 4 to implement thermal regulation in the reference. The voltage reference output is connected to the positive terminal of the op amp. The voltage across the digitally trimmed resistor R2 is connected to the other op amp input, and the current through this resistor is sourced by the pFET P2, connected to P1 in Figure 4 in a typical current mirror configuration. To create the PTAT voltage across R2, the digital trimming scheme is designed using poly resistors with a positive tempco; the series trimming scheme was used for this resistor. The op amp drives an nFET with a large W/L, which generates heat when current flows from *hplus* to *hminus*. The node *hminus* is grounded, and *hplus* is connected to either a 5 V DC source or ground to enable or disable the temperature regulation, respectively. The op amp driving the nFET heater is a high-voltage op amp, created by a 1.8-V-powered p-input operational transconductance amplifier (OTA) followed by a 5-V-powered common source stage. [18]

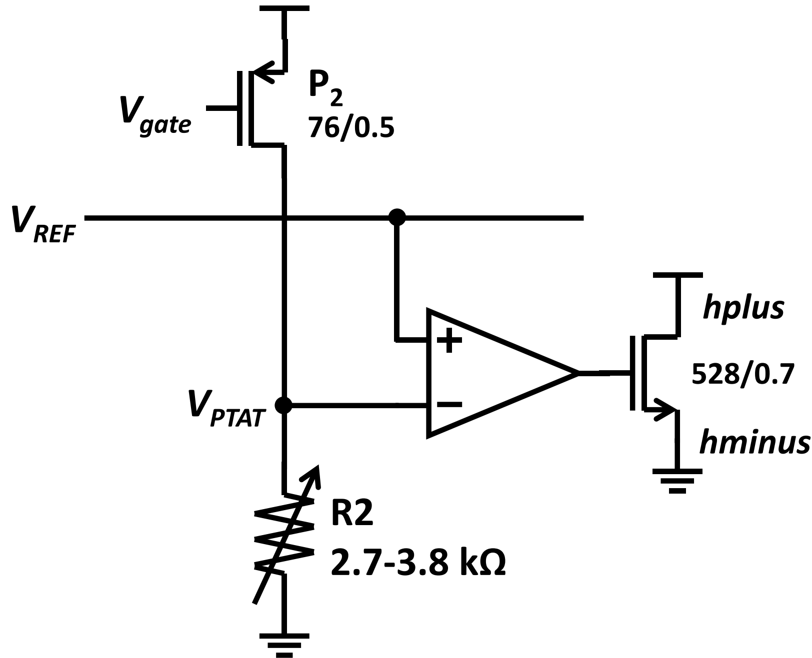

Figure 11: Additional circuitry added to the voltage reference core circuit of Figure 4 for thermal regulation.

In order to determine the optimal trim code for the PTAT resistor R2, another experiment was performed using the temperature chamber and HP 34401A 6 ½-digit multimeter. At 20˚C, 30˚C, and 40˚C the PTAT voltage V_{PTAT} was measured for each trim code, as well as the reference voltage V_{REF}, with the optimal trim code for R1 for first-order tempco cancellation applied; for this experiment, the output was observed to the nearest tenth of a millivolt, the smallest accuracy that could be observed reliably.. The goal of this experiment was to find the trim code at which V_{REF} and V_{PTAT} are equal at 30˚C; this temperature was chosen as the set temperature point because the circuit was designed with it as the desired operating die temperature. However, the circuit would function the same way with any set point. Figure 12 shows the results of this experiment for select trim codes for the same reference chip from Figures 7 and 8. This data shows a trim code of 3 (00011) leads to the two voltages being equivalent as close as possible to 30˚C.

After determining the optimal trim code for R2, the overall effectiveness of the temperature regulation can be demonstrated experimentally. An experiment was performed on the same chip

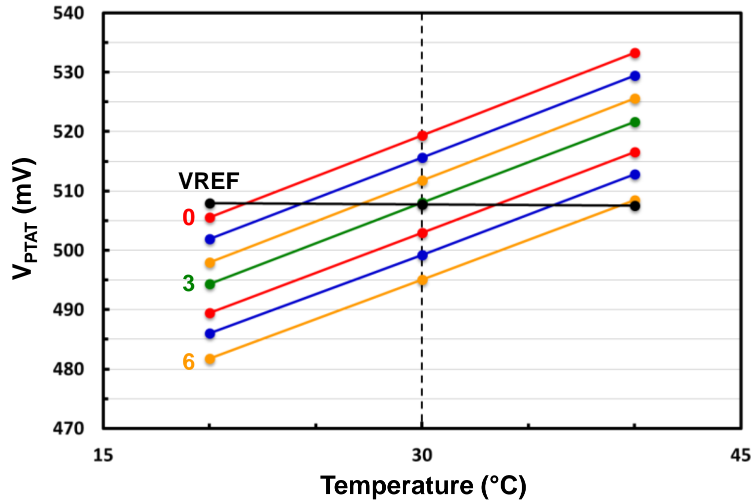

Figure 12: Temperature response of the output and PTAT regulation voltage of 180nm voltage reference circuit for heater trim codes from 0 (00000) to 6 (00110). Optimal trimming for first-order tempco cancellation, shown in Figure 8, was applied during testing.

with optimal trim codes for both R1 and R2 applied and the heater enabled. The temperature in the chamber was varied from 0˚C to 100˚C, in increments of 10˚C throughout most of the range. The increment was decreased near the temperature set point to observe the behavior of the reference when the ambient temperature is near the transition between regulation with the heater and basic first order tempco cancellation. At each temperature, the reference output, PTAT heater control voltage, and the on-chip temperature were measured in the same manner as the prior experiment to determine the optimal trim code for R2. The on-chip temperature is measured using a voltage divider implemented with two poly resistors, one with a positive tempco and one with a negative, which was characterized using the temperature chamber prior to this experiment.

The results of this experiment are shown in Figures 13 and 14. Figure 13 shows the change in the reference output over the entire temperature range. It is important to note that the entire vertical axis is only 1 mV. In the region where thermal feedback is active, there is only a 0.1 mV shift in the reference voltage, a shift of approximately 0.02% from 507.7 mV. At temperatures greater than 30˚C, the reference exhibits the expected second-order curvature of a reference

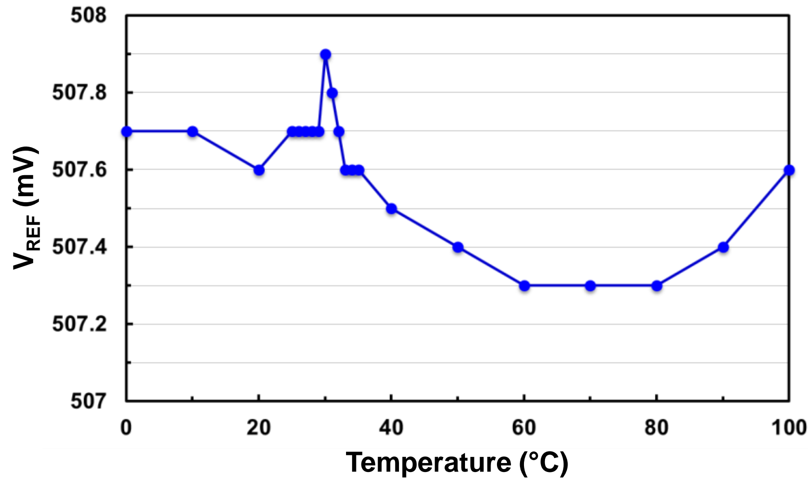

Figure 13: Temperature response of 180nm voltage reference circuit with resistors trimmed for optimal first-order tempco cancellation and thermal feedback at 30°C.

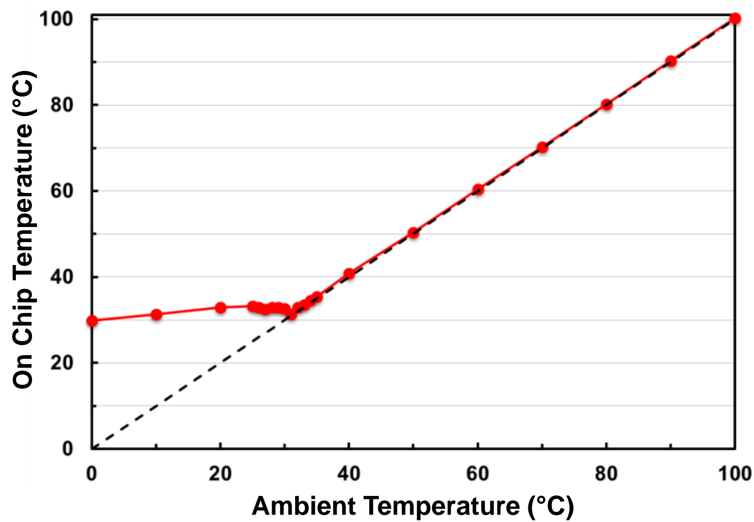

Figure 14: Ambient and on-chip temperature during the test from Figure 13. The dotted line has a slope of 1 and indicates an equal ambient and on-chip temperature.

implementing first-order tempco cancellation. Overall, the reference only showed a shift of 0.6 mV (0.11%) during this test. Additionally, if the small spike near the transition point is not considered, the total variation is only 0.4 mV (0.08%). This data shows the improvement that the thermal feedback loop can provide over the already small shifts in the initial bandgap based design. Also, the on-chip temperature throughout the test is shown in Figure 14. The figure shows that

when the ambient temperature is lower than the set temperature point (30˚C), the chip is heated up to that temperature; at greater temperatures, the on-chip temperature is simply the same as the ambient temperature. So, as the temperature increases, the on-chip temperature stays approximately 30˚C, and once the ambient temperature reaches 30˚C, the on-chip temperature increases linearly with the ambient temperature.

Summary

In this chapter, the effectiveness of several techniques for minimizing shifts in the voltage reference output due to changing temperature was analyzed. First-order tempco cancellation in a DTMOST-based voltage reference and an active temperature regulation scheme were presented. A reference chip fabricated in a 180nm technology was used to experimentally demonstrate the effectiveness of these techniques. By implementing digitally trimmed resistors, experiments showed that with proper design, these techniques can significantly reduce reference variation due to temperature changes.

CHAPTER V

RADIATION HARDENING OF CMOS VOLTAGE REFERENCES

For systems operating in an environment where there is an abundance of ionizing radiation present, it is important to design a voltage reference such that shift in the output voltage due to radiation are minimized. This chapter describes several radiation-hardened-by-design (RHBD) techniques for voltage references that are used on the 180nm reference chip described. Also, experimental results are presented to show the effectiveness of the techniques used.

Dynamic Threshold MOS Transistors

As discussed in Chapter IV, the 180nm voltage reference circuit tested in this work uses dynamic-threshold MOS transistors (DTMOSTs) in place of the bipolar junction transistors of a typical bandgap reference. A DTMOST is p-type MOSFET (pFET) with the gate and body connected, as well as the drain in this application. This diode-connected DTMOST is a low voltage CMOS replacement for the p-n junction required for the first-order tempco cancellation in a bandgap reference. However, the main benefit of the DTMOST for this work is its demonstrated radiation tolerance [15]. Because these reference devices directly generate the reference output, the overall radiation response is fundamentally dependent on the individual radiation sensitivity of the DTMOSTs.

The voltage reference chip designed in 180nm IBM CMRF7SF technology also contains two isolated matched DTMOSTs, which are identical to the DTMOSTs used in the reference circuit. In this section, the operation and radiation response of these isolated devices are analyzed

experimentally. Both devices have a size of 100 μm/0.5μm and use an edgeless layout. Six pairs of DTMOSTs were tested using the ARACOR 4100 10-keV X-ray source. The DTMOSTs was biased differently during irradiation, with two devices at each bias condition; these bias conditions are shown in Table 3. The radiation steps for this test were 0, 50, 100, 200, 300, 500, 750, and 1000 krad(SiO_2), and the dose rate was 31.5 krad(SiO_2)/min. The devices were tested by performing five I-V sweeps at each irradiation level using the HP4156A Semiconductor Parameter Analyzer. Additionally, the same measurements were performed after 10 minutes of room-temperature. The range of the sweep was from 0 to 450 μA; this maximum was an arbitrarily chosen value that was sufficiently larger than the typical bias currents of the devices in the complete voltage reference circuit, which can range from 1 to around 300 μA. After testing, the average and standard deviation of each sweep measurement taken was calculated, and the results from these sweeps was used to calculate the shift in the source voltage required to maintain a specific current. Despite only five sweeps being performed, the standard deviation of the data is still quite small, generally less than 0.05 mV for all data outside of zero bias, so the data can be considered an accurate representation of the device behavior. A simple I-V sweep is suitable for this testing because the DTMOST devices of interest are two-terminal devices.

First, the basic operation of the DTMOSTs tested is analyzed. The pre-irradiation current-voltage characteristics of the DTMOST 1 on chip 1 is shown in Figure 15. It can be seen that the DTMOST shows an exponential relationship between current and voltage, similar to a diode or diode-connected bipolar junction transistor or MOSFET. This is expected, as the DTMOST is intended to operate as a p-n junction in the voltage reference. The other benefit of this data is it allows for proper selection of the irradiation bias conditions. Table 3 shows the bias conditions chosen, and the points in Figure 15 were added to denote where on the I-V curve the devices were

Table 3: Irradiation bias conditions for isolated DTMOSTs tested.

V (mV)	I (μA)
0	0
250	4
300	14
350	46
400	122
500	408

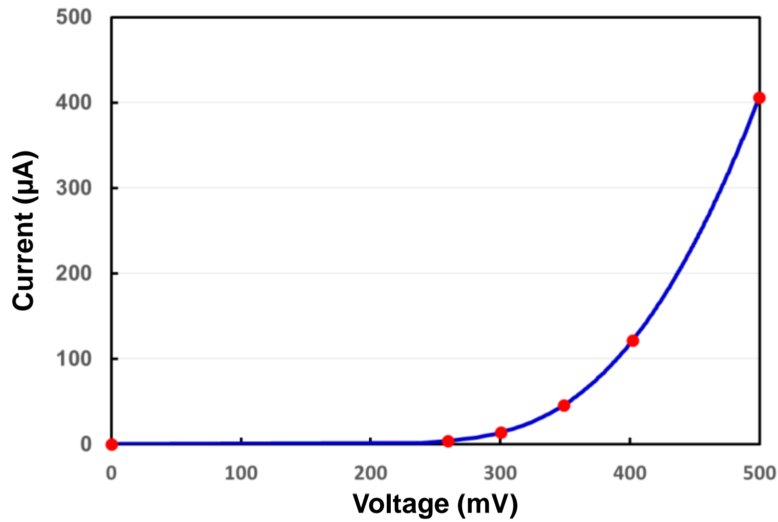

Figure 15: Current-voltage characteristics of a 100-μm/0.5-μm DTMOST on 180nm voltage reference chip with points added to indicate bias points of different devices during irradiation.

biased. These bias conditions were chosen to provide a balanced perspective throughout the devices' range of operation.

Next, the radiation response of the DTMOSTs is analyzed based on their operation in the voltage reference circuit. In a reference, the reference devices are at a constant DC voltage and current, and it is required for first-order tempco cancellation that the two devices in the circuit operate at different currents (and voltages). Therefore, it is appropriate to analyze the radiation degradation in the devices by calculating the change in source voltage required to maintain the pre-rad bias current. The voltage delta required to maintain a constant current for the each pair of

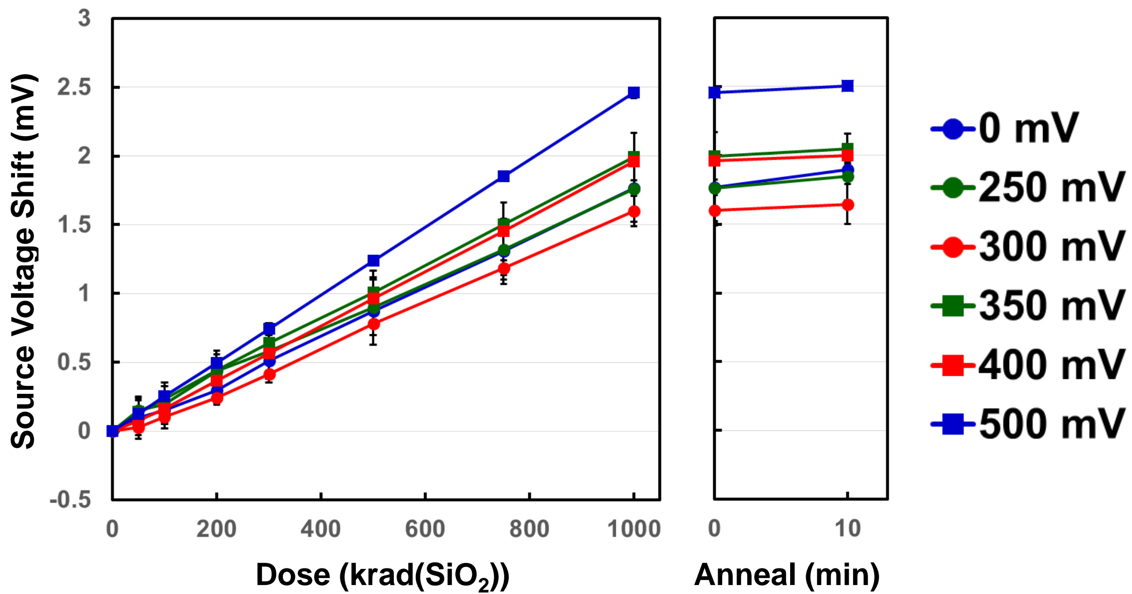

Figure 16: Voltage shifts in the source voltage of DTMOSTs required to maintain the constant current from the irradiation bias. The legend represents the voltage for these currents pre-irradiation. Error bars represent the standard deviation between the two devices at each bias.

DTMOSTs biased at the same voltage during irradiation were averaged, and the standard deviation was calculated; this is plotted in Figure 16. The constant currents maintained correspond to the values in Table 3, with the exception of the DTMOSTs biased at 0 mV during irradiation. Because the irradiation voltage for these DTMOSTs was zero, the device was essentially turned off, with negligible current. Because the change in voltage required to maintain a few picoamps of current would not be relevant, 2 μA was used as the constant current to be maintained for the calculation. This was chosen because it is slightly above where the device begins to conduct a significant current, which occurs at approximately 240 mV.

The trends shown in the radiation-induced shift in the source voltage of the DTMOST required to maintain the pre-rad current, shown in Figure 16, appear to be qualitatively similar and varies slightly depending on bias conditions. This shift in voltage increases in a fairly linear fashion with additional radiation exposure, and larger increases are seen in the devices with larger bias voltages (and currents). The annealing post-irradiation has very little effect on the voltage required

to maintain the bias current. Overall, these shifts in the DTMOST source voltage are fairly small; the maximum is approximately 2.5 mV and occurs after 1 Mrad(SiO_2) of radiation exposure in the DTMOST with the largest I-V bias conditions. Also, the shifts are even smaller at lower doses; the maximum at 500 krad(SiO_2) is less than 1.2 mV. This experimental data shows that with proper design, a DTMOST-based voltage reference circuit can show small shifts in the output due to degradation in the DTMOST devices.

The analysis presented shows that the bias current and voltage are a significant factor in how radiation affects the source voltage necessary to maintain that bias current. However, it is unclear whether this is due to bias conditions or the fact that, in the analysis, the current maintained was different for each device. It is possible that the differences seen in Figure 16 are due to differences in radiation response throughout the I-V curve rather than the irradiation bias conditions. While this determination is not critical to the operation of a voltage reference because the DTMOSTs operate at a constant DC bias, it is beneficial for comprehensive analysis of the devices. To analyze the overall shift in the I-V curve, the voltage shifts required to maintain three different currents for each device was calculated from the I-V curves measured. These three currents – 10 μA, 100 μA, and 300 μA – are the same for all devices, unlike the previous analysis where calculations were done based on a different current for each device. Table 4 shows the corresponding voltage for each of these currents for one DTMOST; this is very similar for all devices.

Figure 17 shows plots of the shift in voltage required to maintain the three constant currents chosen; for each pair of devices with the same irradiation bias, the average and standard deviation of these shifts was calculated. The qualitative trends are similar in each plot, and match up with those of Figure 16. In Figure 17(a), there is slightly more variation between the devices in the

Table 4: Constant currents used for calculating DTMOST shifts and corresponding voltages.

I (μA)	V (mV)
10	288
100	388
300	467

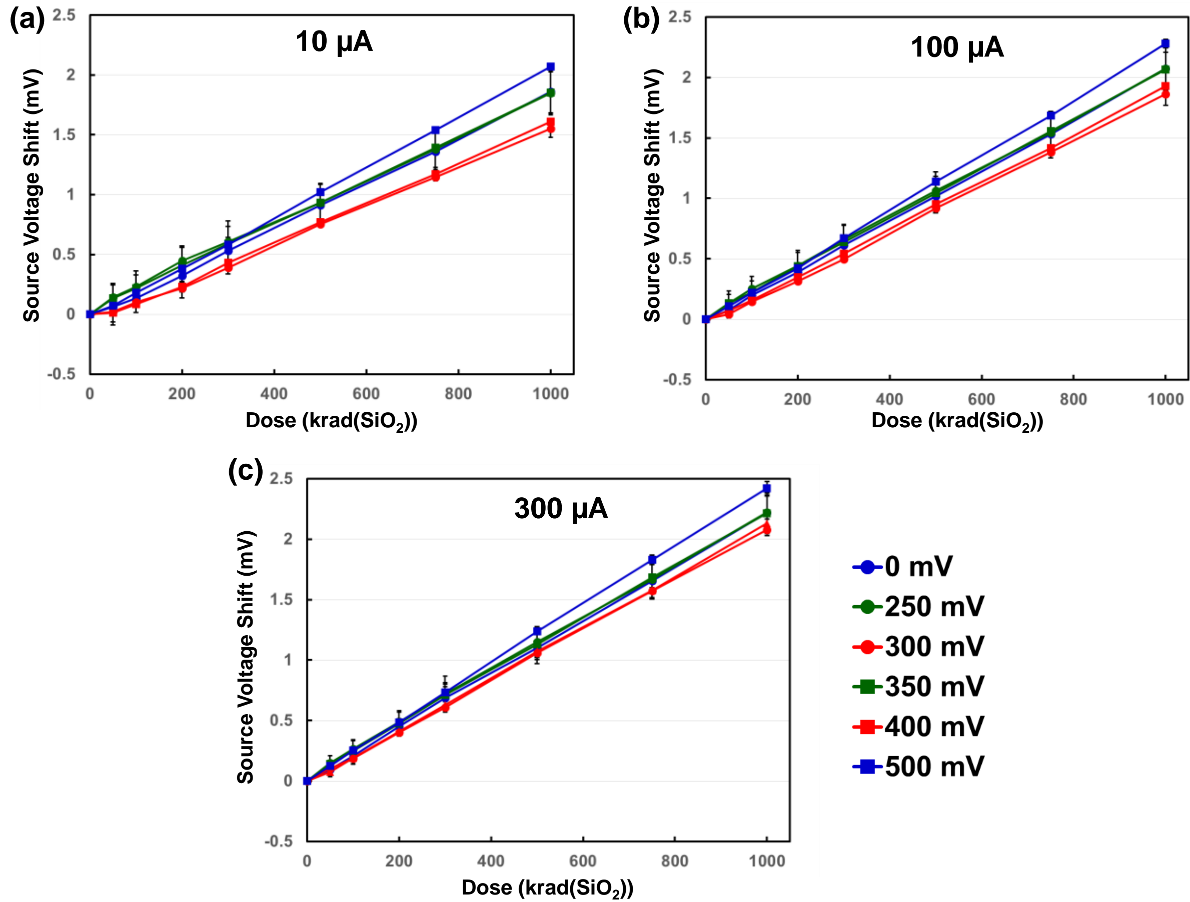

Figure 17: Voltage shifts in the source voltage of DTMOSTs required to maintain a specific current for all devices tested. The legend represents the source voltage during irradiation of each device.

voltage shift to maintain 10 μA, compared to the other two currents. This is because the slope of the I-V curve is smaller at that point than for the other two currents, so small changes in current cause more significant shifts in voltage than at the larger currents, making small variations appear more pronounced in the analysis for 10 μA. Additionally, the slight differences between devices in voltage shifts to maintain the same current do not show a clear trend based on the irradiation

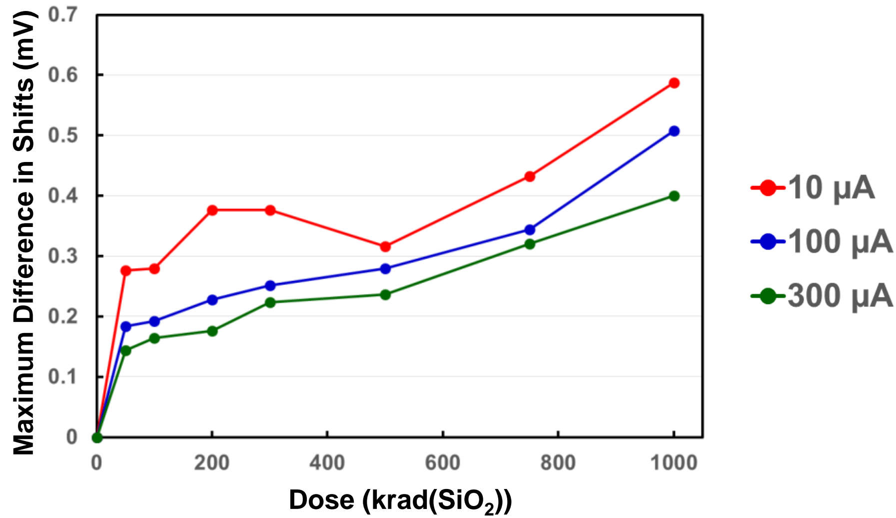

Figure 18: Maximum difference in source voltage shifts required to maintain the same current through DTMOSTs. This is the difference between the maximum and minimum value from each plot in Figure 17.

bias, especially considering how much the error bars for each curve overlap. It is possible that the differences are more due to natural experimental and process variation rather than different irradiation biases. The maximum variation between the voltage shifts from Figure 17 at each radiation step for each current to be maintained is shown in Figure 18. It was calculated by finding the difference between the maximum and minimum shifts at each irradiation step in the plots of Figure 17. This allows for the visualization of the differences in radiation response across the different devices; additionally, the different plotlines for each current compare how much variation there is between the voltage shifts at the different currents. The plot shows that the maximum difference is always less than 0.6 mV, and generally even lower, especially for maintaining 100 μA and 300 μA. It is also beneficial to compare the variation between the pairs of devices on the same chip and compare that to the overall variation. Figure 19 shows the difference in the voltage shift to maintain each of the 3 currents between the two DTMOSTs on the same chip. The maximum variation for each current from Figure 18 is also shown; the other six plotlines represent each pair of devices. This data shows that shifts are smaller when only comparing the devices on

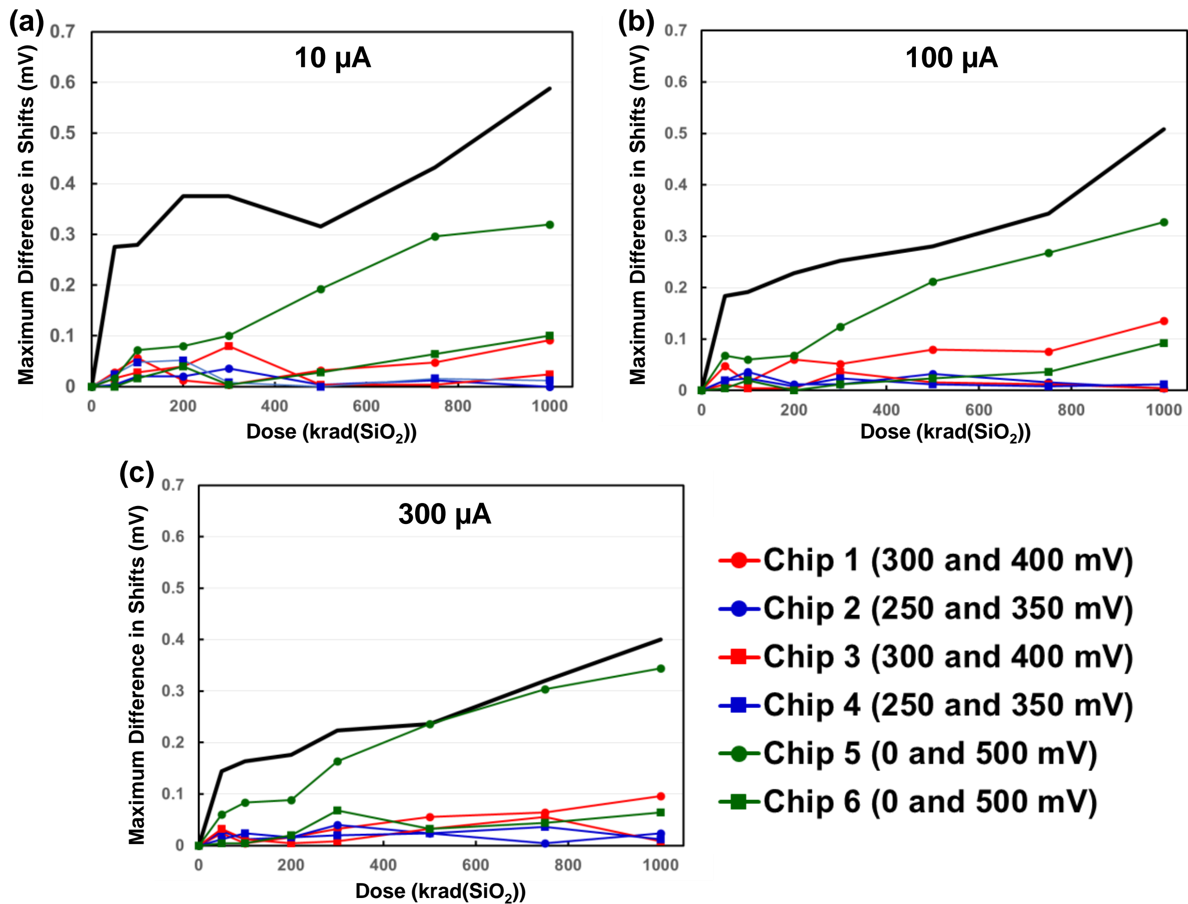

Figure 19: Difference in source voltage shifts required to maintain the same current through two DTMOSTs on the same chip, along with maximum difference in shifts across all devices from Figure 18.

the same chip. This is especially apparent in the shift required to maintain 10 μA, which showed the most variation previously. Only chip 5 showed more than a 1.2 mV difference in the shift in source voltage required to maintain any of the three currents at any radiation level. The two devices on this chip were biased at 0 and 500 mV during irradiation. So while it is possible that the irradiation bias makes some difference in voltage shifts to maintain current, it was only significant when the irradiation biases were significantly different. Overall, this experiment shows that the difference in shifts to maintain different currents, shown in Figure 16, is primarily due to the different currents maintained for the calculation, rather than the bias conditions during irradiation.

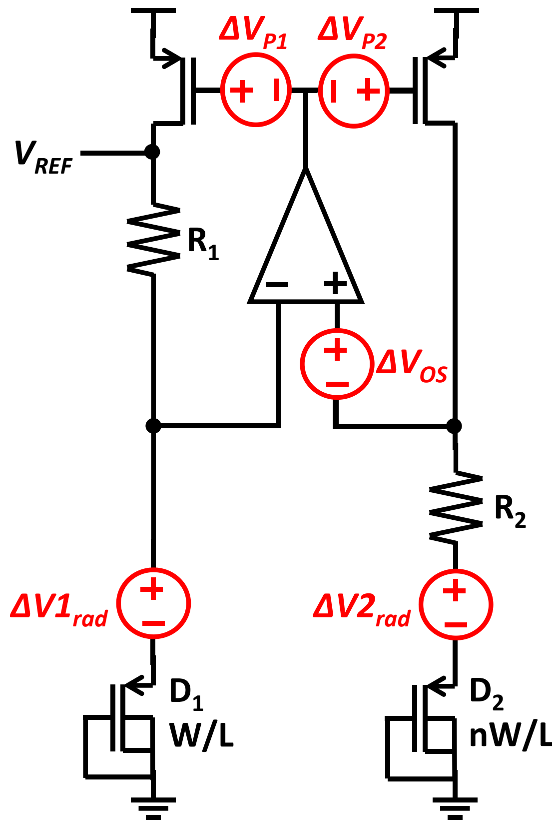

Figure 20: DTMOST-based voltage reference of Figure 3, reproduced with the addition of red voltage sources to represent radiation-induced shifts.

Radiation Hardened Voltage Reference

The voltage reference circuit from Chapter IV was also designed for increased radiation tolerance. This section details its design and the experimental results of radiation testing.

The basic DTMOST-based voltage reference schematic of Figure 3 is reproduced in Figure 20 with the addition of voltage sources (in red) to represent the overall effects of radiation in the circuit components. These added sources represent the overall combined effect of threshold voltage shifts and leakage current increases. As calculated in [18] and [20], the shift in the reference voltage output due to radiation can be expressed as:

$$\Delta VREF = -A\Delta V_{OS}$$

$$+\Delta V1_{rad} - A(\Delta V2_{rad} - \Delta V1_{rad})$$

$$-A(R_1 + r_{m2})r_{mp}(\Delta V_{P1} - \Delta V_{P2}), \quad (8)$$

where A is the fundamental system gain defined as:

$$A = \frac{R_2 + r_{s1}}{R_1 - (r_{s1} - r_{s2})}. \quad (9)$$

The equations show that the all the individual shifts are amplified in the output, with offset in the current mirror amplified the most. Additionally, in [18] and [20] experiments showed that the shifts in the op amp input voltage are the largest. In order to maximize the radiation tolerance of the reference circuit, all three of the sources of radiation-induced degradation must be addressed.

Several radiation hardening techniques were used in the 180m voltage reference circuit of Figure 4 [18]. The first RHBD technique implemented in the circuit is replacing the pFET current mirror of Figures 3 and 21 with a single pFET current source and using resistors to scale that current. Because the high gain of the op amp forces equal voltages at its input terminals, the voltage drop across the resistors R and R/2 is equivalent, so the current through them can be controlled with the relative size of the resistors; in this circuit, this scaling factor is 2. Using a single pFET and scaling its current with resistors eliminates the term in (8) containing the offset between the current mirror pFETs [18]. In order to scale the currents accurately, the resistors R and R/2 were designed using combinations of unit cell poly resistors. The other technique used in the reference circuit is chopper stabilization, a method of dynamic offset cancellation. Offset cancellation can minimize the effects of radiation-induced mismatch, and chopper stabilization is the technique best suited to a DC circuit, such as a voltage reference [21]–[23]. The basic chopper circuit and symbol are presented in Figure 21. The chopper has two inputs and two outputs, and the connection between them is alternated in two non-overlapping clock phases; IN1 is connected to OUT1 in the first phase and to OUT2 in the second phase, with IN2 connected to the remaining output. The

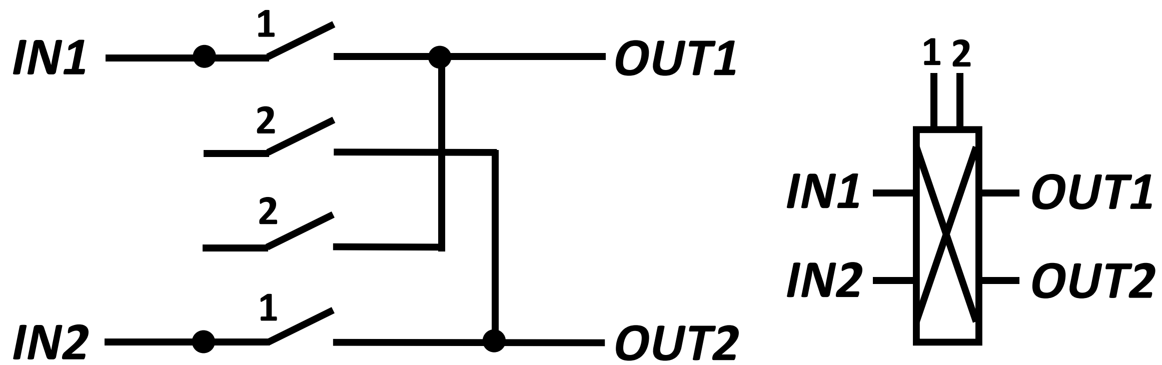

Figure 21: Chopper circuit and symbol.

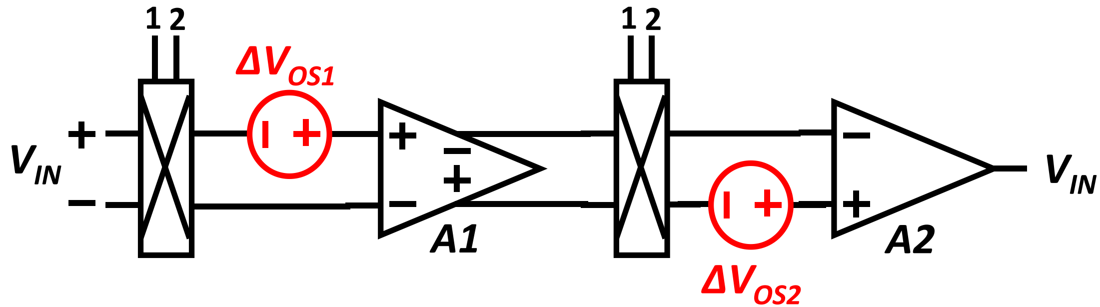

Figure 22: Chopped operational amplifier.

implementation of a chopper amplifier is shown in Figure 22. The output voltage of the amplifier can be expressed as:

$$V_{OUT} = A1A2(V_{IN} \pm V_{OS1}), \tag{10}$$

where the ± is addition in phase 1 and subtraction in phase 2. Therefore, if the output during the two phases are averaged out using a low-pass filter, the input offset of the op amp is completely eliminated in the output. [18]

In the hardened voltage reference circuit, chopper stabilization is implemented in the op amp and the DTMOST reference devices. The op amp is simply replaced with the chopped op amp of Figure 22. This chopped op amp is a p-input chopper operational transconductance amplifier

(OTA) based on the design presented in [24]. The input chopper switches are implemented using nFETs because the common-mode range of the input stage is low, and pFETs are used for the output switches because the high-impedance output typically high; the devices can be minimum-sized to minimize charge injection because they switch high-impedance nodes and conduct negligible current [18]. Because the output of the chopped op amp is close to a square wave, it is necessary to filter the output. This was done by connecting a 10 nF capacitor to the output of the op amp; the size was chosen to create an adequate low-pass filter based on the size of on-chip resistor and experimentally verified to filter the signal below the noise levels. A chopping scheme was also implemented in the DTMOST reference devices. Because the currents in the two devices were scaled rather than sourced identically, different current densities in the two reference devices, as required for first-order tempco cancellation, can be achieved using devices of equal size. Therefore, the devices can be chopped without affecting the functionality of the circuit. These chopper switches are implemented using nFETs as well; however, it is necessary to increase the W/L ratios because the switches conduct significant current. In this circuit, 100-μm/0.18-μm nFETs were used for the switches; the size was determined in simulation to be large enough that changes in the ON resistances have little effect on the output, less than 50 μV for a pessimistic 10 mV threshold voltage shift [18]. It is also necessary to filter the wave created by this chopping. This was done by connecting a 47 nF capacitor to the voltage reference output. The value of the capacitor was experimentally determined to be large enough that the output signal variation was not noticeable above noise levels. By implementing chopper stabilization in the circuit, both the term containing the op amp and the term containing the difference in shifts between the DTMOST devices in (8) are eliminated [18].

The shift in the output of the voltage reference in Figure 22, hardened using the resistive current mirror and chopper stabilization can be expressed as:

$$\Delta VREF = \frac{1}{2}(\Delta V1_{rad} + \Delta V2_{rad}). \quad (11)$$

The only term left from (8) is the single $\Delta V1_{rad}$ term. However, due to the chopping, D1 and D2 in this circuit each act as the D1 from the original circuit for half of the clock cycle, and $\Delta V1_{rad}$ and $\Delta V2_{rad}$ in this circuit act as $\Delta V1_{rad}$ from the original circuit for half of the clock cycle. Therefore, the $\Delta V1_{rad}$ shift in the original equation becomes the average of $\Delta V1_{rad}$ and $\Delta V2_{rad}$ in this equation. The experimental results from the previous section show that by limiting the overall shift to only unamplified shifts in DTMOST devices, small shifts can be achieved.

The 180nm fully integrated voltage reference circuit was also tested using the ARACOR X-ray source to verify the effectiveness of the radiation hardening techniques implemented. Reference circuits on two different chips were tested, referred to as the static reference and chopped reference. In the static reference, chopper stabilization was disabled by grounding the clock input. In the chopped reference, a clock input of 200 kHz was applied, implementing chopper stabilization at 100 kHz due a divide-by-two circuit in the clocking circuitry. The frequency was divided in order to ensure a 50% duty cycle. The trim code for the digitally trimmed resistor R_1 was set to the optimal value as determined by simulation, although the value has little effect on the radiation response. The output of the references were measured using the HP 34401A 6 ½-digit multimeter; approximately 200 measurements were made at each radiation step, and the minimum, maximum, and average of these measurements were recorded. The circuits were powered on and irradiated at a dose rate of 31.5 krad(SiO_2)/min with measurements pre-rad and at 25, 50, 100, 150, 200, 250, 300, 400, 500, 750, and 1000 krad(SiO2).

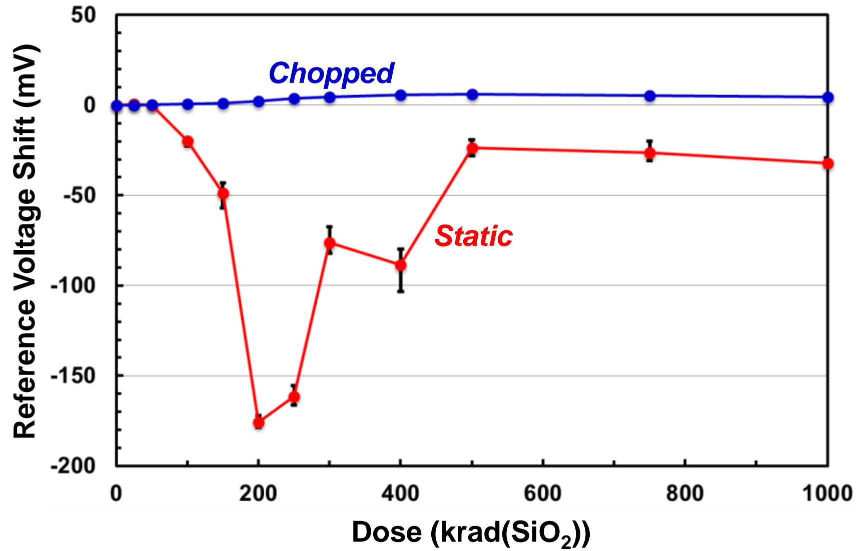

Figure 23: Radiation-induced shift from pre-rad value in voltage reference output for chopped and static voltage references. Error bars represent maximum and minimum measured shifts.

In Figure 23, the change in output of each reference from the pre-rad is plotted as a function of total dose. The pre-rad reference voltage output values were 489.1 mV for the static reference and 527.1 mV for the chopped reference. In the plot, the error bars represent the minimum and maximum measurements made. The static reference output showed a maximum shift from pre-rad of 175.9 mV, occurring at 200 krad(SiO_2), and the output voltage at 1 Mrad(SiO_2), the maximum dose measured, was 32.1 mV less than pre-rad. These are shifts in the output of 36.0% and 6.6%, respectively. The chopped reference output showed a maximum shift from pre-rad of 6.0 mV at 500 krad(SiO_2) and at 1 Mrad(SiO_2), the output voltage is 4.6 mV greater than the pre-rad output. These are reference output shifts of 1.1% and 0.8% shift, respectively. This data shows that the maximum change in the output reference voltage from the pre-rad value is 96.6% smaller in the chopped reference than the static reference. Additionally, the difference in the output voltage at 1 Mrad(SiO_2) from the pre-rad value is 85.7% smaller in the chopped reference than the static reference. In the plot, it can be seen that the static reference shows massive shifts in the 200-250

krad(SiO_2) range, before recovering to smaller shifts at larger doses. This is because the voltage reference circuit is a complex system with many competing, independent radiation-induced effects that can either combine or cancel each other out, and have different relative impacts at different doses. In the chopped reference, many of the shifts are eliminated with the chopping scheme, leading to much smaller shifts in the reference output. Overall, this experiment shows that the implementation of chopper stabilization in the op amp and reference devices of a voltage reference can dramatically reduce radiation-induced shift in the output.

It is beneficial to compare this hardened voltage reference to other radiation-tolerant reference designs commercially available and previously published in literature. Commercially available radiation tolerant voltage references have achieved output shifts ranging from 0.1% to 0.25% after 150 to 300 krad(SiO_2) of radiation exposure [25]–[27]. The hardened 180nm voltage reference tested in this work, the chopped reference in Figure 23, shows a shift in the output of 2.2 mV (0.4%) at 200 krad(SiO_2). The commercial devices show a slight improvement over the 180nm reference tested here, approximately a factor of two. The maximum output shift of the hardened 180nm reference over the entire 1 Mrad(SiO_2) is 6.0 mV (1.1%) at 500 krad(SiO_2), which is a larger dose than the commercial devices are rated for, so an accurate comparison cannot be made. While the commercial voltage references discussed show slightly improved radiation tolerance than the fully integrated 180nm reference tested in this work, all of these commercial devices provide reference voltages greater than 1.2 V and therefore require supply voltages larger than their outputs. For this reason and the fact that the references are discrete components, it is much more difficult to integrate the commercial references in a system compared to the fully integrated reference presented, and impossible to integrate the commercial references in a system-on-a-chip.

When compared to other integrated CMOS radiation hardened voltage reference, the presented technique also shows comparable or improved performance at the radiation dose tested – 1 Mrad(SiO_2). The 1.1% maximum output shift is an improvement over the approximate 2.5% shift shown in [28]. The most radiation tolerant designs in [17] show similar radiation tolerance – an approximate 0.4% shift – to the reference tested in this work. Finally, the reference of [15] shows superior radiation tolerance to that of this work, showing output shifts of approximately 0.1% in the range of 1 Mrad(SiO_2). However, the voltage reference designs of [17] and [15], which show comparable and improved radiation tolerance, respectively, both benefit from the inherent increased radiation tolerance of the 130nm process used. The hardening techniques presented in this work can be implemented in any process, so radiation tolerance will continue to increase when the techniques are used in newer processes with smaller feature sizes.

Summary

In this chapter, the radiation hardening techniques implemented in a DTMOST based voltage reference circuit fabricated in a 180nm technology were presented. Additionally, the radiation tolerance of the DTMOST devices and the chopper stabilized voltage reference circuit were experimentally verified.

CHAPTER VI

CONCLUSIONS

In this thesis, several design techniques used to minimize the shift in the output of a voltage reference due to varying temperature and radiation exposure were presented. These techniques included first-order temperature coefficient (tempco) cancellation and active thermal regulation for temperature, and dynamic-threshold MOS transistors (DTMOSTs) as a p-n junction replacement, a resistive current mirror, and chopper stabilization. A voltage reference circuit fabricated in 180nm IBM CMRF7SF process was used to experimentally verify the techniques presented.

Temperature testing was performed using a TestEquity temperature chamber. By using digitally trimmed resistors, the effectiveness of properly sizing and scaling resistors to implement first order tempco cancellation was demonstrated. Additionally, an active temperature regulation scheme was implemented using thermal feedback and an on-chip heater. The experiment showed that the thermal regulation combined with first-order tempco cancellation can reduce variation in the reference output even further.

The reason DTMOSTs were used as the reference devices for the voltage reference circuit because of their inherent radiation hardness compared to typical n- or p-type MOSFETs and bipolar junction transistors. Isolated DTMOSTs were also available on the voltage reference chip, so the radiation response of the devices could be tested. Radiation testing using the ARACOR X-ray source confirmed relatively small shifts overall, with shifts differing in magnitude at different

current-voltage points. However, the bias during irradiation did not have an effect on the shifts in the device.

Finally, the voltage reference circuit was tested using the ARACOR to compare a static voltage reference to one using chopper stabilization. The chopped voltage reference showed significantly reduced shifts compared to the static voltage reference, demonstrating the effectiveness of chopper stabilization as radiation hardening technique. Overall, the voltage reference circuit tested in this work has been shown to be very resilient to both variations in temperature and increased radiation exposure.

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