THE DESIGN OF SINGLE-EVENT HARDENED ANALOG AND MIXED-SIGNAL CIRCUITS

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CHAPTER I

INTRODUCTION

The physical world is inherently analog in nature. This is a very broad statement, but it has an important impact on electronics and microelectronic circuit design. A system-on-a-chip must have an analog component in order to interact with the physical world. Advances in technology have enabled incredibly high packing densities for digital circuits, but have not, and cannot alleviate this need for things of an analog nature, like power management, data conversion, and signal processing. The indispensible nature of analog circuits, coupled with the economic incentive to incorporate them and highly packed digital components onto a single chip has necessitated that analog and mixed-signal (A/MS) circuits be designed at increasingly advanced technology nodes (smaller minimum feature size).

Analog circuits at advanced sub 100 nm complementary metal-oxide semiconductor (CMOS) technology nodes often have feature sizes much greater than the technology minimum. This is done primarily to facilitate the precise matching necessary in these designs. The devices themselves are larger, but they are still closer together in active-to-active spacing, with smaller nodal capacitance and quiescent currents than the previous generations of analog design. It is for this reason, that much like their digital counterparts, analog circuits are becoming increasingly more vulnerable to the effects of ionizing radiation.

The effects of ionizing radiation are a growing concern in the microelectronic industry. Ionizing particles exist not only in the space atmosphere, but also terrestrially. They can penetrate the semiconductor material common to circuit components, and generate free carriers through their interactions with the material. The free carriers then collect via various mechanisms at different device nodes in an integrated circuit, resulting in undesirable circuit response. The response is dependent upon the circuit, the amount of charge deposited, and how much of the subsequent charge is collected. An ionizing particle interacting with a semiconductor in this manner is called a single-event (SE). The results of these SEs are typically called single-event effects (SEE) and an effect of particular concern for this work is the single-event transient (SET). An SET is an asynchronous signal that can propagate through a circuit, causing a variety of responses. In digital circuits, this SET can propagate to a latch. If it meets certain set-up and hold times, the erroneous signal can be latched and become a single-event upset (SEU). In analog and mixed-signal applications the definition of a SEU is more complicated and depends on the circuit topology.

The digital design community has made significant strides in single-event circuit hardening in recent years. The radiation effects literature provides a large amount of insight into how and when to harden critical digital circuits blocks. As an example, hardening techniques like the dual interlocked cell (DICE) for latches have been explored in great detail and specific guidance on how to implement these techniques is available and continuously being reevaluated in the literature. In contrast to the digital design community, the analog literature lacks some of the specificity in the hardening of critical analog and mixed-signal (A/MS) circuit blocks. This research will help rectify this

knowledge gap through the introduction, verification, and application of novel hardening techniques.

This work introduces three novel radiation-hardened by design (RHBD) techniques that can be classified into two broad categories, hardening via charge sharing or hardening via node splitting. The first two techniques, Differential charge cancellation (DCC) layout and sensitive node active charge cancellation (SNACC) use charge sharing to mitigate SEEs. A DCC layout uses charge sharing to turn a single-ended SE error signal into a common-mode signal that will be rejected by a differential circuit's inherent common-mode rejection property. SNACC on the other hand, uses charge sharing to sense that a SE has occurred and then activate compensation circuitry to either sink or source the necessary current to mitigate its effect. The compensation circuitry needed for SNACC can be added to the circuit design or in some cases can already be a part of the original circuit. The final hardening technique, a peeled layout is an example of hardening via node splitting.

All three of these hardening techniques will be experimentally verified on a single ended output operational amplifier (op amp), a differential output op amp, or both, using a two-photon absorption (TPA) SE laser testing technique. An op amp was chosen as the test vehicle because it is an essential building block and ubiquitous in A/MS design. Op amps are critical components in everything from DC applications, like bias circuits, to sophisticated AC applications, like amplifiers and filters. After experimental verification of these techniques and a characterization of their impacts on the op amp's performance, an in-depth simulation study will look at how they can be applied to other fundamental building blocks of A/MS design. This simulation study will provide greater context to the

radiation effects design community for hardening A/MS circuits against SE causing radiation.

The simulation study will focus on a few basic circuits because much like their digital counterparts, large portions of the circuits in the A/MS design space are designed using a few fundamental building blocks. An examination of the single-event (SE) vulnerabilities of these building blocks, circuits like differential amplifiers, basic current sink/sources topologies, and cascode amplifiers amongst others, can provide insight into the majority of A/MS circuitry. In similar fashion a study of how to harden these types of circuits against SE causing radiation can be extended across the A/MS design space. This work will explore this via a bias dependent SE model in the Cadence Spectre Environment using an IBM 180 nm process design kit (PDK).

This examination of the fundamental building blocks will look at which technique works best for each fundamental circuit topology, if a certain technique is chosen for that topology what the expected decrease in sensitive area is, and finally what are the design penalties or tradeoffs associated with the chosen hardening technique.

Dissertation Organization

The research presented in this dissertation deals with mitigating single-event effects in A/MS circuits. Each chapter provides insight into the information necessary to understand and implement three novel RHBD techniques to a large array of A/MS circuit architectures.

Chapter II covers the necessary background on single-event effects needed to understand the motivation for this work as well as its impact. It will also briefly explore the pertinent work already completed in this area.

Chapter III discusses the necessary background information in modeling and radiation testing to enable the reader to comprehend the simulation and experimental results presented throughout. The final section of this chapter details the op amp designs used in the experiments detailed in chapters IV and V.

Chapter IV introduces the concept of hardening via charge sharing. In this portion of the dissertation two novel hardening techniques, DCC layout and SNACC are introduced and experimentally verified.

Chapter V introduces the hardening via node splitting concept. The peeled layout hardening technique is then experimentally verified. The final part of this chapter presents experimental evidence that a DCC layout and a peeled layout can be combined to achieve greater mitigation.

Chapter VI is a detailed SE simulation study of the fundamental building blocks of A/MS circuit design. Nine different circuits are systematically studied to determine how to best harden them against SEs. The end result contains some assertions for an A/MS circuit designer. One of these assertions changes the fundamental nature in which all A/MS circuits are laid out.

Chapter VII concludes the dissertation with a summary of the findings.

CHAPTER II

SINGLE-EVENTS AND THEIR EFFECTS IN A/MS CIRCUITS

Introduction

In order for a circuit designer to develop a circuit or system that is hardened against ionizing radiation he or she must first fully characterize the problem. Understanding and scoping the problem to something manageable can be a challenge within the radiation effects field. In fact, since the first confirmed electronic malfunction of a part in space from an analog single-event transient (ASET) in 1992 a significant amount of effort has been spent on this issue [1].

This chapter will briefly examine the mechanisms causing single-events (SEs), the SEs themselves to include ASETs, look at the effect relevant circuit parameters have on ASETs, and finally discuss traditional A/MS hardening techniques. The mechanisms behind SEs beginning with an ionizing particle interacting with silicon through charge collection are very similar for analog and digital circuits. When charge is collected by a single or multiple circuit nodes the biggest distinction between analog and digital SEs occurs. This difference is that the ASET is indistinguishable from a legitimate analog signal. This inability to separate erroneous from legitimate single in an analog system make the final topic discussed (A/MS hardening techniques) so difficult.

At the end of this chapter all the necessary background for understanding the need for and the research itself will be complete. The reader will then be better prepared to grasp the novel nature of the A/MS hardening techniques presented in chapter IV and V.

Single-Event Mechanisms

Heavy ions, alpha particles, and trapped protons from radiation environments discussed in [2], can all cause damage to semiconductor devices. The basic mechanism for this is an ionizing particle losing energy in the semiconductor material via Coulombic interactions, creating a dense cloud of electron hole pairs in its wake. The electron-hole pairs are collected at circuit nodes and can cause undesirable circuit behavior.

Charge Generation

Ionizing radiation generates a charge in a semiconductor via two primary mechanisms, indirect and direct ionization. Indirect ionization is the result of nuclear interactions between an energetic particle and the struck material, resulting in ionization by secondary particles. The energetic particle in this case is low mass like a proton or neutron and can cause some very significant upset rates due to indirect mechanisms by undergoing inelastic collisions with a target nucleus [3, 4].

Lighter particles striking Silicon can create nuclear reactions such as elastic collisions producing a Silicon recoil or alpha/gamma particle emission and recoil of the daughter nucleus. An example of the latter is when Silicon emits an alpha particle and a recoiling daughter Mg nucleus. Another type of nuclear reaction is a spallation reaction, where the target nucleus is broken into two fragments. An example of this is Silicon breaking into Carbon and Oxygen ions and all of these could recoil [5]. Any of the nuclear reactions described can produce heavier particles than the original incident proton or neutron. These heavier particles can then cause direct ionization.

Direct ionization is the primary charge deposition mechanism of heavier incident particles ($Z \geq 2$). Direction Ionization is when an energetic particle passes through a

semiconductor and frees electron-hole pairs along its path, as it loses energy. The distance the particle travels before it comes to rest is often referred to as its range. Another common term used to describe these mechanisms is linear energy transfer (LET), which is defined as the energy loss per unit path length (MeV/cm) normalized by the density of the target material (mg/cm^3). So LET has the units of $MeV\text{-}cm^2/mg$. Silicon requires 3.6 eV to generate an electron hole pair and has a density of 2328 mg/cm^3, so an LET of 97 deposits 1pC/μm of charge. A ratio of a 100:1is often used to approximate this.

Charge Collection

The excess electrons and holes generated following a SE strike can become a problem for circuit performance when collected at a circuit node. If the excess charge is generated near a p-n junction, then the built-in electric field at that junction will cause the holes to be swept to the p region and the electrons to the n region. This is known as drift current, Fig. II-1. Drift current is limited by the saturation velocity of the carriers, resulting in a current transient typically on the order of picoseconds in length [6].

Ionizing particle strikes on a p-n junction can create a plasma track of free carriers distorting the potential gradient along the track length creating a field-funnel [7]. This plasma track of free carriers between n and p regions effectively creates an electrical connection or wire between the regions along the track. This wire allows the electrons to move towards and the holes away from positively charged n-regions. The spreading resistance along wire results in a voltage drop along its length and a collapse in the junction's electric field. The resulting phenomenon takes the potential initially isolated event across the depletion region and spreads it down the plasma track, exposing carriers

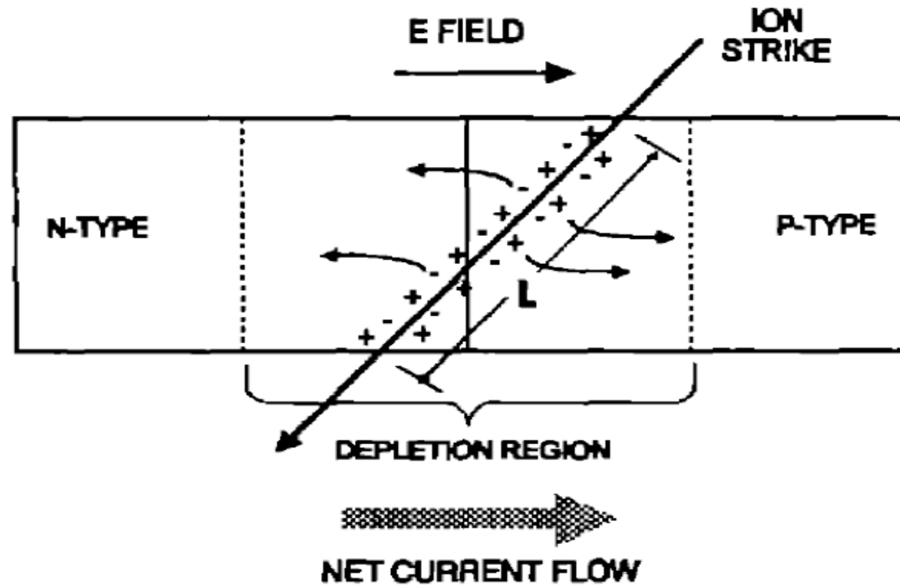


Fig. II-1 Depletion region drift collection from an ion strike [6]

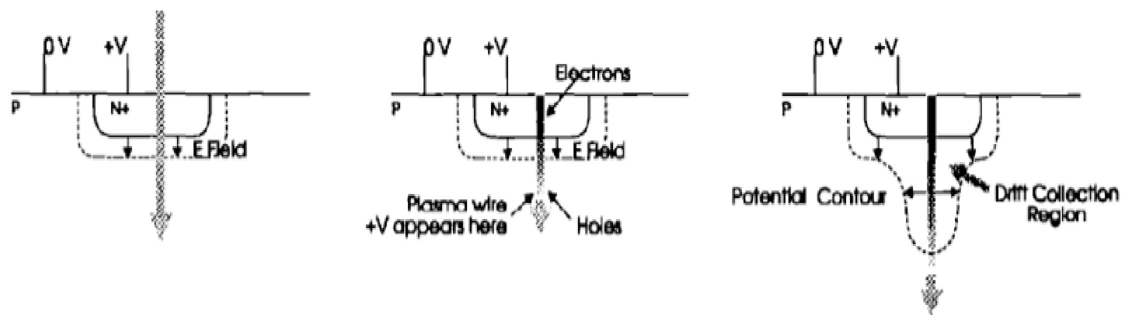


Fig. II-2 The funnel effect; from left to right, (a) a plasma track of free carriers formed, (b) movement of electrons towards positive bias, (c) potential drop along the track and redistribution of equipotential lines down the track [6]

outside the depletion region to its electric field [6]. This effect increases the amount of charge collected via drift and is depicted in Fig. II-2. As devices scale further below 100 nm, this process becomes more complex because the plasma wire is on the order of device size [8,9].

Charge that is not collected via drift may still be collected through diffusion. Diffusion occurs when charge is generated from an ionizing particle within a diffusion length of a junction. A struck node, a neighboring node, or multiple nodes within that length can therefore collect charge. Diffusion collection takes longer than drift collection and can be on the order of hundreds of pico-seconds to nano-seconds. The fact that this collection takes longer makes the free carriers more susceptible to recombination mechanisms, therefore reducing that total amount of charge collected [10]. Fig. II-3 depicts charge collection and recombination in a reversed biased n-p junction [11]. The initial prompt collection is through drift and then subsequent collection from diffusion through the substrate.

In modern ICs there are other very important mechanisms that play a role in charge collection, like the ion shunt effect and parasitic bipolar effect. The ion shunt effect occurs when an ion strikes through two proximal junctions, creating a dense plasma of carriers between them. If these two junctions are of the same type, this path can conduct current and increase the total amount of charge collected at the node.

The parasitic bipolar effect also can increase the total amount of charge collected by a node. It occurs primarily after SE strikes to PMOS devices in n-wells in dual well technologies, such as the ones used in this work. The collection of SE deposited electrons in the n-well reduces its potential. This potential collapse with extra carriers in the substrate turns on the parasitic PNP bipolar device between the drain (collector), body (base), and source (emitter). This effect depicted in Fig. II-4 can greatly increase the amount of total charge collected following a SE strike.

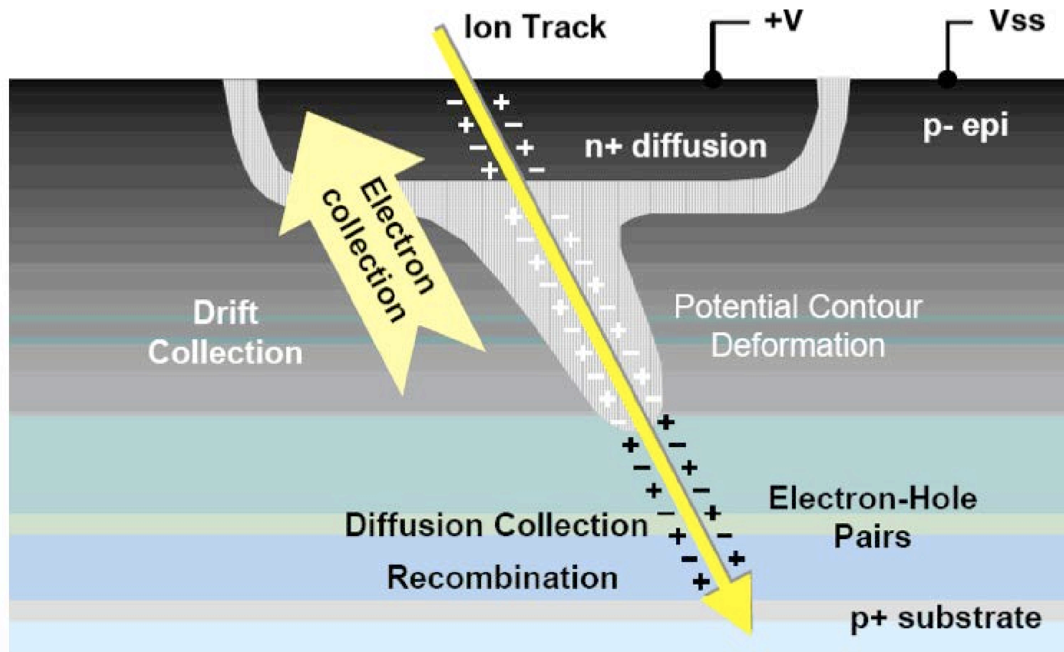


Fig. II-3 Illustration of an ion strike on a reversed biased n-p junction [11]

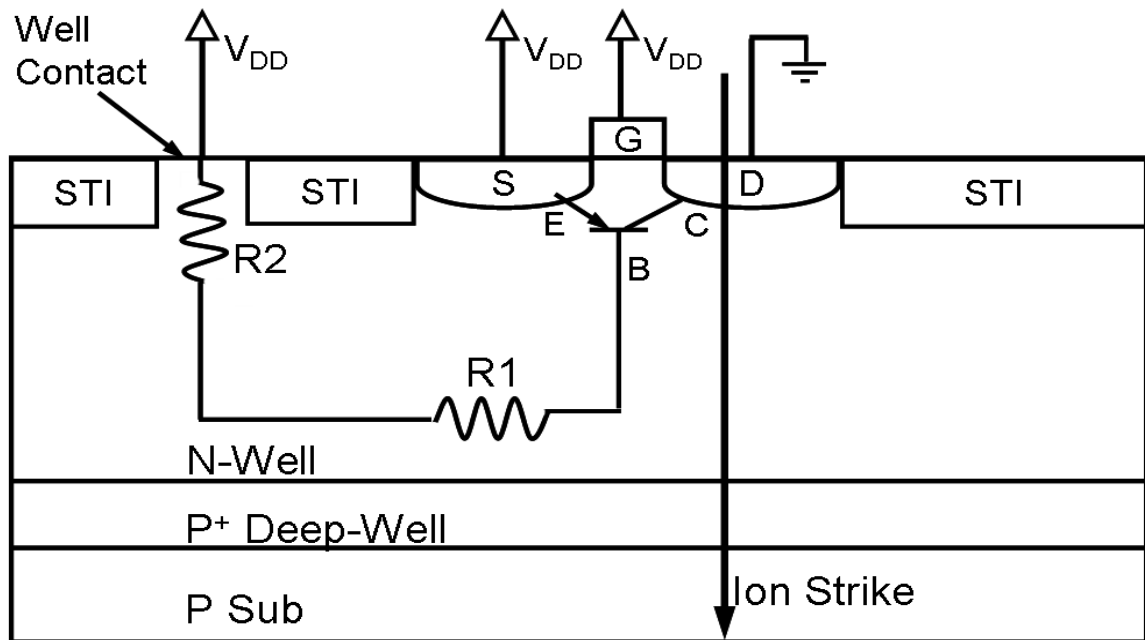


Fig. II-4 Illustration of the parasitic bipolar structure [8]

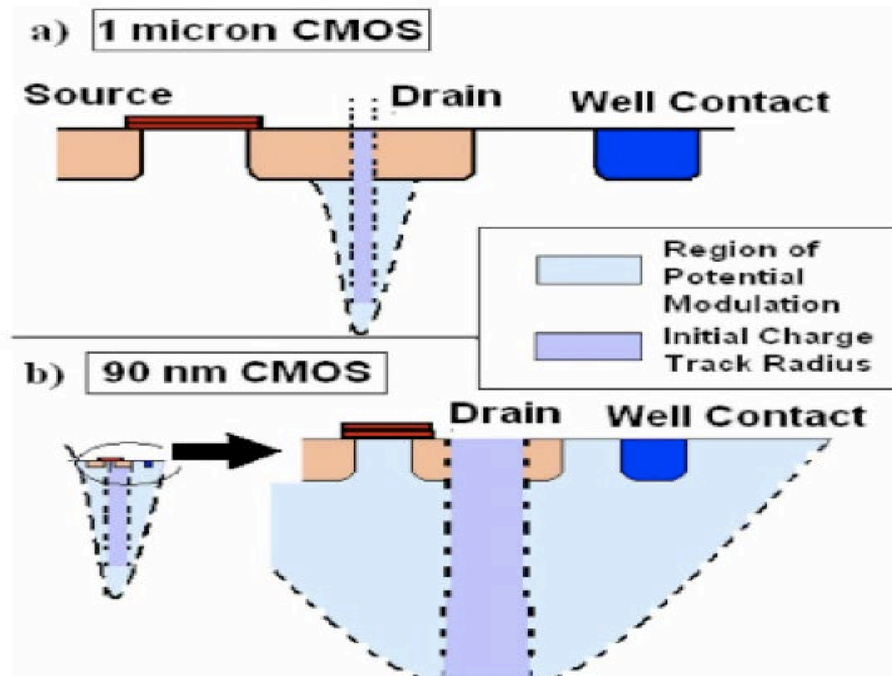


Fig. II-5 Relative size of an electron-hole cloud following a SE strike for a 1μm device vs. a 90 nm device (a) shows that the cloud only effects a small portion of the drain (b) shows that at a 90 nm technology node that same SE strike radius structure encompasses all four terminals of the device [8]

There is one more very important charge collection effect that is becoming more prevalent as devices scale further below 90nm, charge sharing. The driving force behind charge sharing or multi-node charge collection is depicted in Fig. II-5 [8]. As devices decrease in size and packing densities increase, more devices become susceptible to the electron-hole cloud created following a SE strike. The width of the electron-hole cloud is independent of the technology node, so what previously only encompassed a single drain may now cover several devices. This charge sharing effect can have many ramifications, to include potential modulation of multiple junctions and current transients at multiple junctions. Another mechanism that can lead to charge sharing is depicted in Fig II-6 [12]. In this work, it was demonstrated that nuclear reactions from an

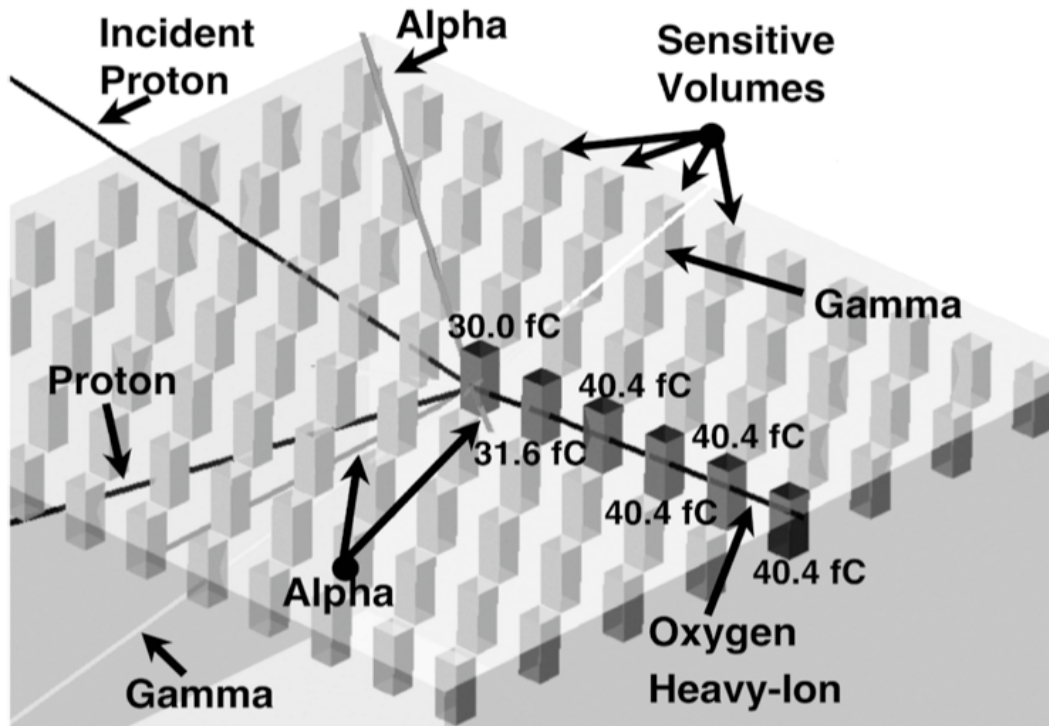


Fig. II-6 Depiction of the results of a 63 MeV proton nuclear event, the proton interacts with a Silicon nucleus creating energetic secondary particles, to include a 14 MeV Oxygen ion, proton, gamma rays, and alpha particles. The oxygen ion traverses six sensitive volumes and deposits between 30 and 40 fC of charge in each [12].

incident 63 MeV proton and a Silicon nucleus could create secondary particles like a 14 MeV Oxygen ion, proton, gamma rays, and alpha particles. Simulations in this work, showed that the Oxygen ion would traverse six sensitive volumes of Silicon and deposit between 30 and 40 fC in each volume [12]. These types of events and the collection of charge at multiple junctions from a single ion strike can create multiple-bit-upsets (MBUs) and are expected to become increasingly important for future device and circuit single-event characterizations.

Single-Event Effects

When the excess carriers are collected at circuit nodes following SE strikes via the mechanisms previously discussed, multiple types of SEE can occur. Some of the SEE result in catastrophic system failure and are referred to as hard errors. Examples of these hard errors include single-event burnout (SEB), single-event gate rupture (SEGR), and single-event latchup. These effects, while important, are not the focus of this work. The interested reader can find more information about these effects in the references [5, 13, 14, 15].

Single-event strikes in CMOS devices often result in temporary glitches or errors and are referred to as soft errors. One type of soft error of particular interest for analog and mixed-signal application is the single-event transient (SET). A single-event transient is an unwanted asynchronous electrical pulse that can propagate through the signal path causing unintended circuit behavior.

In a digital circuit a SET can become a single-event upset (SEU) if the transient results in a change of a latched state (i.e. a "0" becomes a "1"). If the result of the ion strike is a perturbation of multiple nodes leading to multiple miss latched bits then it is referred to as a multiple-bit upset (MBU). These SEUs and MBUs can lead to a circuit error if the incorrectly latched bit or bits makes it to an output node.

Analog Single-Event Transients

Single-event transients in analog and mixed-signal circuits, termed ASETs are much more difficult to deal with than there digital counterparts. The first confirmed malfunction due to an ASET was shortly after NASA launched the TOPEX/Poseidon satellite in 1992 [1]. In the Poseidon case the SE occurred in an OP-15 operational

amplifier that was connected to a digital counter. The ASET in this case was fairly easy to identify and quantify because it manifested itself as a SEU, much like its digital counterpart. However, identifying and quantifying ASETs is not always this easy, in fact it encompasses multiple challenges. The largest challenge is that the erroneous ASET signal is indistinguishable from a legitimate analog signal. A second challenge is determining if the ASET created a SEU. Errors in an analog world are not discrete and as easy to recognize as a bit flip that gets latched, like in a digital circuit. Past and current research spend a large amount of effort just characterizing and analyzing ASETs [1,16-21].

In this chapter there are several examples of works that define analog SEUs in varying manners. This is a challenge for the A/MS radiation effects design community. An accurate definition of an analog SEU is completely dependent on the system. As an example a stage of an op amp in one application may appear to be completely immune to SEE because it only produces low voltage long duration ASETs. Yet, in a different application, the duration may be the critical criterion and that stage could be the deemed the most sensitive.

An example of a system that could possibly have ASET duration as the critical parameter is an analog-to-digital converter (ADC). An ASET that has a duration of multiple clock cycles can create multiple errors if the amplitude is significant enough. This is an issue because op amps, like most analog circuits, use devices that are much larger than the technology minimums their digital counterparts rely on. These larger devices are used for increased current drive and better matching, amongst other reasons. The drawback of these larger devices, is their increased nodal capacitances lead to larger

time constants and hence longer transients in many cases. The works that will be discussed in this section often report transients on the scale of micro to milliseconds [22].

The circuit dependence of ASETs and the errors generated by them necessitate a designer to narrow his scope when trying to design a hardened circuit or system. In this work operational amplifiers (op amps) are used extensively as a test vehicle. Therefore it is appropriate to analyze SEEs in this circuit topology available throughout the literature.

Single-Event Effects in Operational Amplifiers

To date, much of the work on single-event effects in operational amplifiers has focused on the characterization of commercial parts and the development of improved characterization techniques. In this section the results that are directly applicable from these works will be discussed in detail. An analysis of how op amp parameters and external circuitry affect SE response is important to understanding the SE response of the entire op amp. For this reason, this section will begin by looking at a paper that explored these topics in detail.

In a 2002, a paper took a detailed look at many aspects of an op amp that are critical to understanding this research [23]. The paper built on knowledge that ASETs are dependent on circuit loading, input/bias voltages, power supply voltages, the configuration of the amplifier, and even the parts manufacturing [24-28]. The op amp used was the LM 124 configured as an inverting amplifier and the paper used simulations calibrated to laser testing data.

After calibrating a SE simulation tool in the SmartSPICE circuit simulator from Silvaco, SE simulated strikes to the LM124's input stage were performed varying

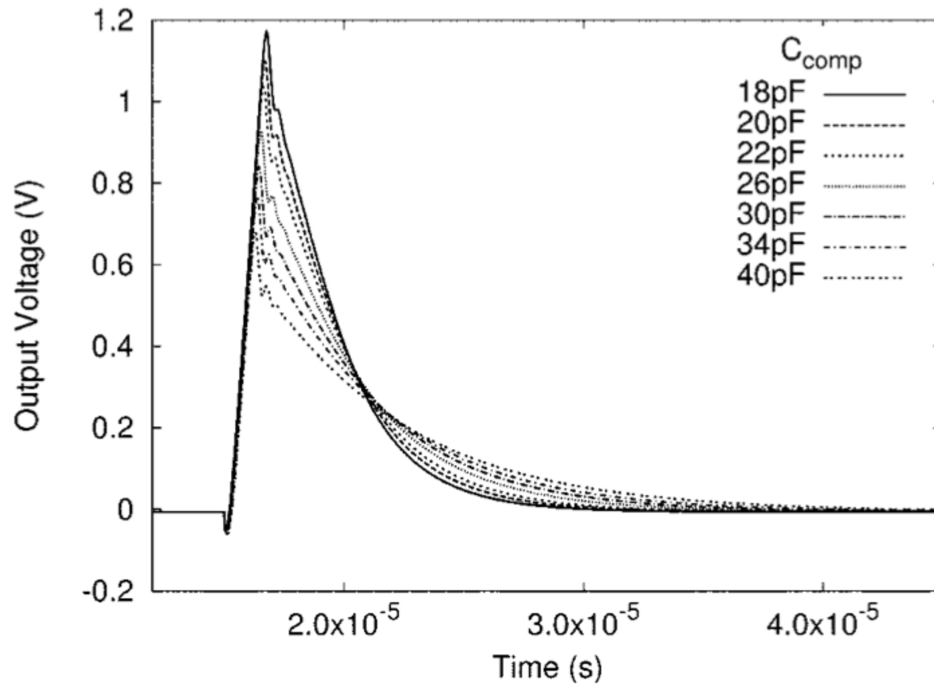


Fig. II-7 The SET dependence on the size of the compensation capacitor, given a SE strike in the input stage of the amplifier [23]

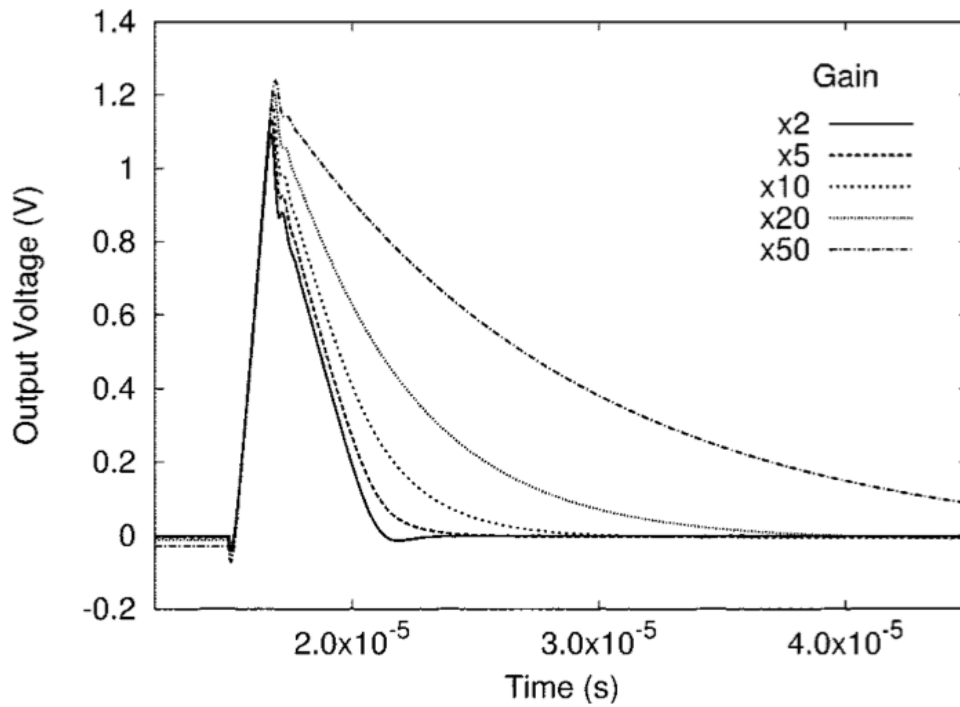


Fig. II-8 SET dependence on the closed loop gain, given a SE strike in the input stage of the amplifier [23]

certain parameters. Fig. II-7 contains the simulation results for different value compensation capacitors, varying from 18 to 40 pF. As the compensation capacitor got larger, the ASETs decreased in amplitude and increased in duration. This was attributed to the fact that the rest of the signal path acted as a low pass filter. The cutoff frequency of the low pass filter was determined by the value of the capacitor.

The closed loop gain of the op amp also plays an important role in its SE response. In effort to understand this, simulated SE strikes to the input stage of the amplifier for gains varying from 2 to 50 V/V were performed. The results of these simulations are in Fig. II-8. The larger gain values led to transients with larger peak amplitudes. However, the large stretch out in duration is very similar to the results seen for the varying compensation capacitor. The increased gain configurations have a lower bandwidth due to the gain bandwidth product (GBWP) property of the amplifier. The simulations with larger compensation capacitors also had smaller bandwidths. This fact was used to argue that in both cases the mechanism for the elongated transients is the same, the rest of the signal path acting as a low pass filter. The difference in Fig. II-8 is that the peak of the transients is larger with the lower bandwidth simulation, unlike Fig. II-7. This is directly tied to the increased gain for these simulations that is not present in the compensation capacitor simulations.

The final important parameter investigated was the value of the feedback resistor. The authors were investigating whether or not a different resistor value, achieving that same closed loop gain, would change the amplifiers SET response. Their main goal here was to try and separate the effects of RC time constant from GBWP adjustments.

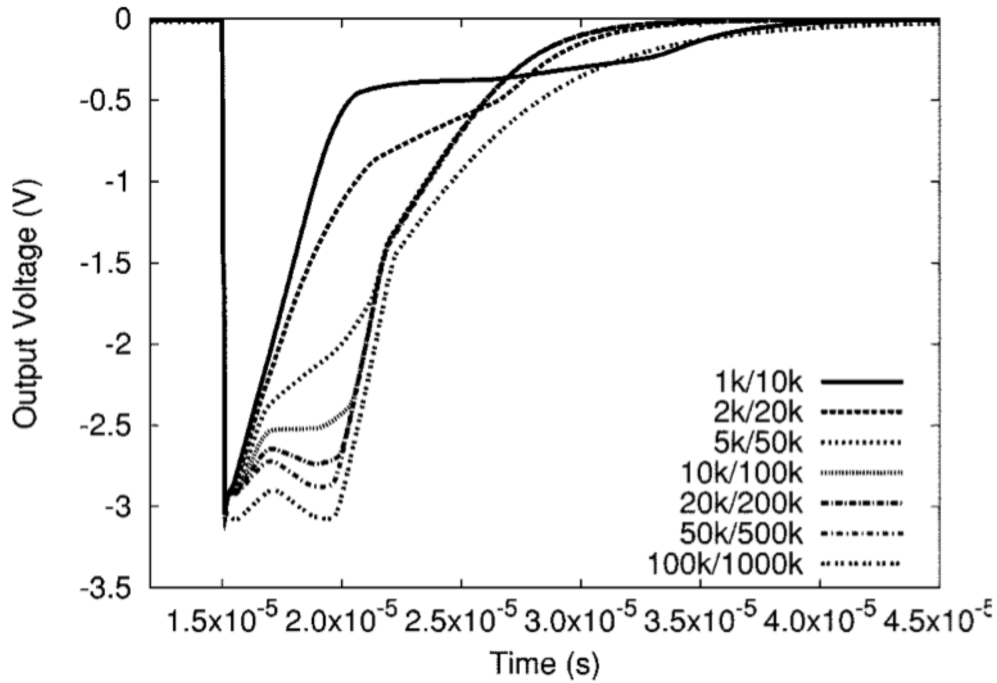


Fig. II-9 SET dependence on the value of the feedback resistors for a constant closed loop gain (10 V/V) [23]

To accomplish this, simulations were performed for varying combinations of feedback resistors all achieving a gain of 10 V/V. Fig. II-9 shows that there is a strong dependence on the resistor values chosen in the feedback loop. The authors concluded their analysis by pointing out that the SET response of the LM124 showed a coupling between resistors used in the feedback loop, closed loop gain, and bandwidth. They also stated that because op amps typically share the same functional bocks, that this analysis should be applicable to any standard op amp design.

Another common commercial op amp design is the LM6144 from National Semiconductor Corporation. In 2004, a paper with experimental test results showing an abnormally long duration pulse (LDP) following SE strikes was published [22].

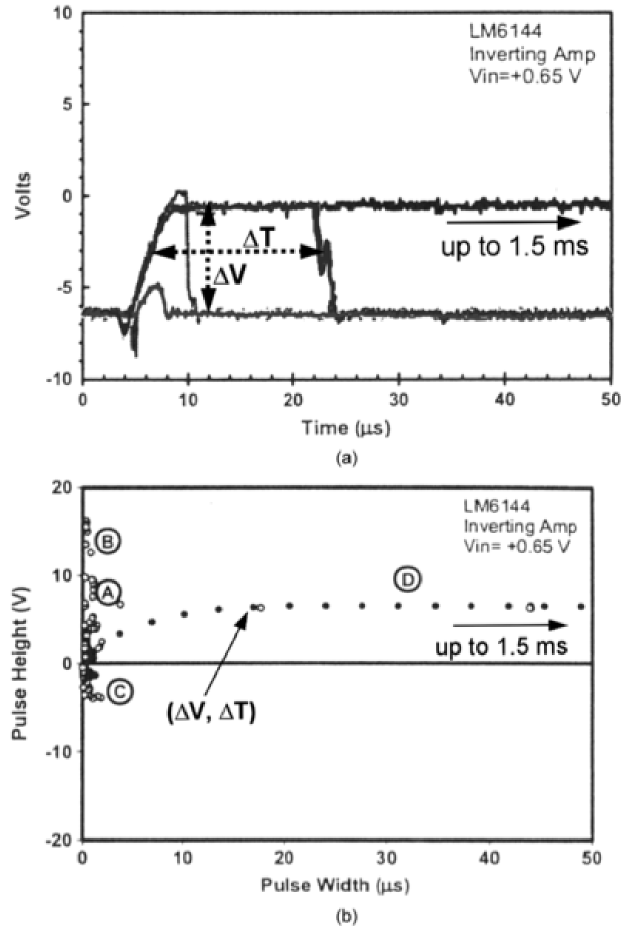


Fig II-10 Heavy ion test results of the LM6144 op amp (a) the oscilloscope reading of initial long duration pulse (b) all ASET represented using FWHM labeling distinct groups of transients [22]

These heavy ion test results were taken at the Texas A&M Cyclotron facility. During the test, the LM6144 was in an inverting configuration with a closed loop gain of -10 V/V. the feedback resistors were 1 and 10 kΩ and the bias was 650 mV with 10 V power rails. The LDPs were on the order of 1.5 milliseconds, which was particularly alarming because it was three orders of magnitude longer than any previously reported ASETs in these types of circuits. The LDPs were captured on an oscilloscope as shown in Fig. II-10 (a). The initial experiment was only originally configured to capture more typical pulses

of 50 microseconds or shorter, as the figure shows. Fig. II-10 (b) shows all of the ASETs captured depicting the maximum pulse heights on the y-axis and the pulse duration on the x-axis. The pulse duration is defined using the full-width half maximum (FWHM) convention. FWHM defines the pulse duration from the start when the pulse first rises to half of its maximum value until the time it falls back to half its maximum value. Inside Fig. II-10 (b), the authors labeled four distinct groups of ASET types, (a) fast bipolar, (b) fast positive going, (c) fast negative going, and (d) LDPs. The FWHM method has a shortcoming when dealing with bipolar pulses, because it only accounts for time of the dominant/larger of the two pulses. This will be addressed in following chapters.

In order to determine the cause of the LDPs, the LM6144 was taken to Naval Research Laboratories (NRL) for single-photon absorption (SPA) laser testing. Using the laser the authors were able to pin point the source of the LDPs to a pair of NPN transistors in the bias/start up circuitry. Further investigation of the LDPs revealed that their duration was tied to the supply voltage, with a lower voltage producing a longer transient. Another interesting discovery was that once the LDP was initiated, all sources of radiation (to include the ambient room lighting) had to be removed to get the op amp to settle to the expected output. Eventually, these LDPs were explained through a parasitic radiation-induced bi-stable state. In order to prevent the LM6144 from entering this unwanted bi-stable state, the authors proposed adding a capacitor to the start up circuitry. This capacitor implemented two low pass filters enhanced through the miller effect that would filter the initial glitches and prevent the circuit from entering this unwanted state. The capacitor had a negligible electrical impact on the op amp performance, primarily because once the op amp successfully powered on, the startup

circuitry powered off and did not affect the op amp in steady state. The capacitor did however, have two important radiation response impacts. First, it increased the critical charge (Q_{crit}) necessary to initiate an LDP. Secondly, it significantly shortened an LDP if it did occur, down to approximately 20 microseconds.

This paper is relevant for several reasons. First, it clearly illustrates the extreme errors that can occur in complex analog circuits, like an op amp. Another very important point this paper also illustrates is the power of laser testing. Laser testing allowed the authors to clearly identify the source of the problem and design a solution.

This final paper explored in this section is of particular interest because it contains results of heavy ion testing of the LM6144 op amp, conducted at the Texas A&M cyclotron [29]. During the testing, the op amp was placed in three different configurations: as an inverting amplifier, a non-inverting amplifier, and a voltage follower. The inverting and non-inverting amplifier configurations both were tested with a closed loop gain of 10 V/V. This is interesting considering the results of the previously discussed papers, because the feedback resistors were different values for the two cases. Figs. II-11, II-12, and II-13 are plots of the experimental results for the three configurations depicting pulse width (FWHM) vs. pulse height (maximum perturbation). The inverting and non-inverting amplifiers (II-11 and II-12) have a very similar distribution of ASETs. This is generally as expected because the amplifiers have the same loop gain, even though the feedback resistors to achieve that gain are different. The voltage follower configuration has a very different ASET distribution.

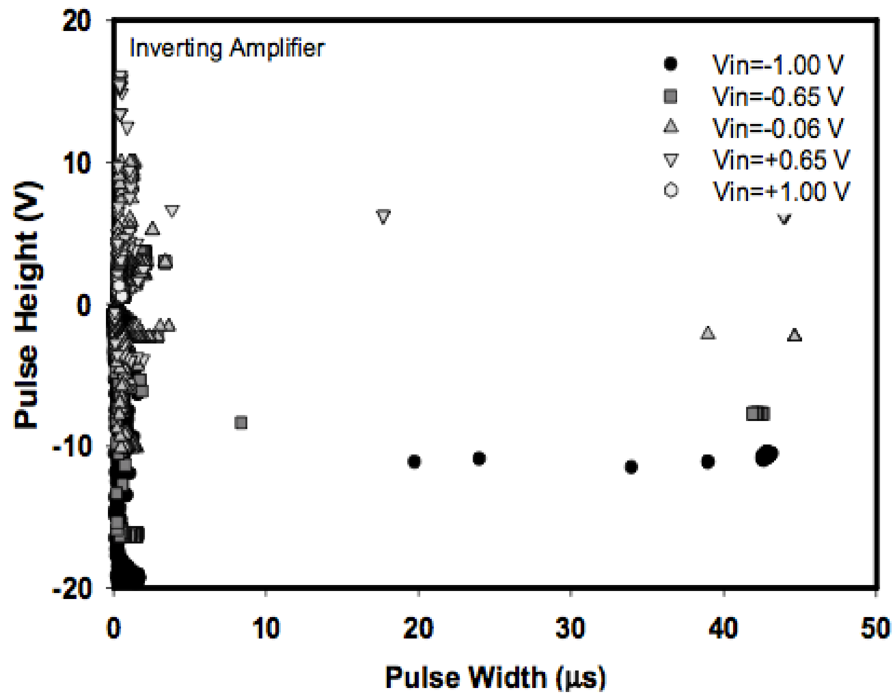


Fig. II-11 Heavy ion induced transients in the LM6144 op amp configured as an inverting amplifier for varying input bias voltages. Gain of 10 V/V [29]

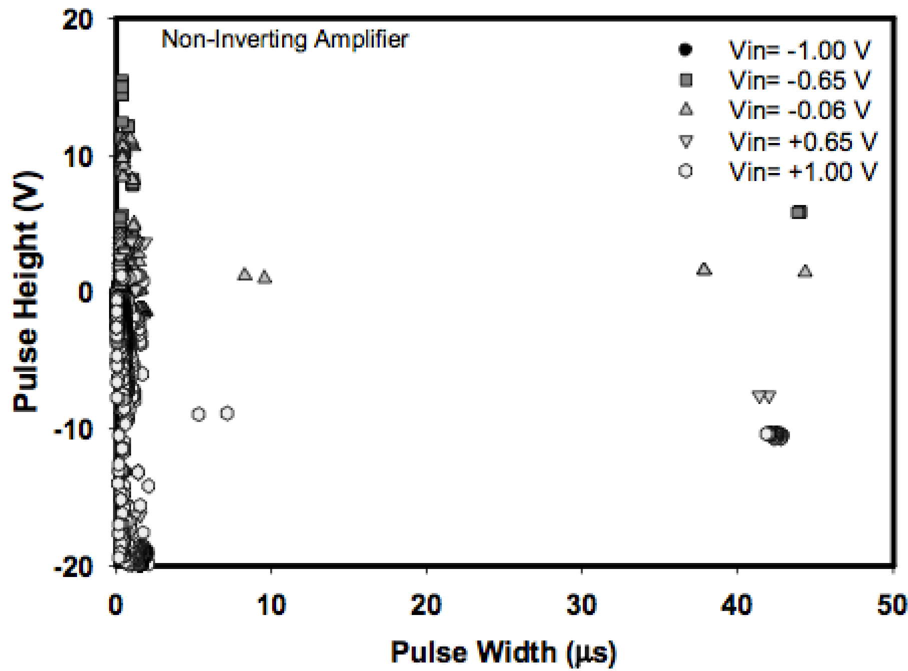


Fig. II-12 Heavy ion induced transients in the LM6144 op amp configured as a non-inverting amplifier for varying input voltages. Gain of 10 V/V [29]

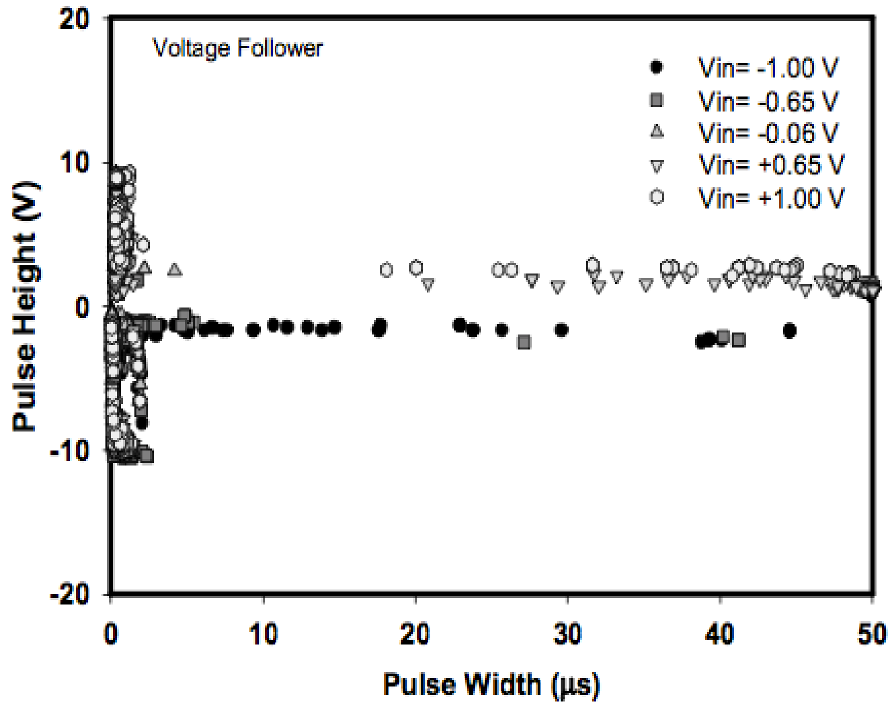


Fig. II-13 Heavy ion induced transients in the LM6144 op amp configured as a voltage follower for varying input voltages. Gain of 1 V/V [29]

The previously analyzed work would suggest that the voltage follower should have a shorter pulse, because amplifiers with higher gain and hence lower bandwidth exhibit longer pulses. However, this author's work shows that the amplifier with no gain (gain =1) has much longer duration pulses than either of the configurations with a closed loop gain. The author does not provide explanation.

Hardening by Design

Generally, most of the SE radiation hardening done in the analog and mixed signal arena to this point has been brute force. An example of this type of hardening technique is designing circuits with high operating currents [30]. These higher currents accomplish two things. They make the collected charge less significant when compared to the quiescent current and most importantly they allow the excess collected charge from

a SE to be removed from the node quicker. These two added benefits reduce the impact of a SE, but at a high cost in terms of power consumption and area needed for the large devices supplying the current.

Another brute force technique is to apply capacitance to a node, often serving as a low pass filter. This technique can be effective in attenuating the maximum voltage of perturbations. However, it has been shown to actually extend their durations, which could possibly make them more detrimental [31]. Added nodal capacitance also comes with a substantial speed and area penalty. The inability to distinguish an ASET from a legitimate signal means that legitimate signals also could be filtered.

In digital circuits, hardening can often be achieved via triple modular redundancy (TMR). This technique uses three identical copies of a single circuit and voting circuitry. The concept is based off a majority vote, if a SE perturbs one circuit, then the other two circuits will win the vote and ensure the proper information gets passed to the next stage. An idea similar to this can be applied in the analog world. Recent work has shown the N copies of an A/MS circuit can be averaged through a resistor to reduce the perturbation by a strike on a single circuit by $\Delta V/N$ [32]. This technique, while effective, has a severe area and power penalty.

The remainder of this dissertation seeks to add to the RHBD arsenal available to an A/MS circuit designer. The work to develop novel hardening techniques with minimal penalty, in chapter IV and V, will revolve around the op amp. In chapter VI a larger view of A/MS circuit will provide insight into hardening any circuit using these techniques.

CHAPTER III

THE DESIGN AND VERIFICATION PROCESS OF RHBD TECHNIQUES

Introduction

The design and qualification of an A/MS circuit for a radiation environment, such as space is a challenging process. In order for parts to survive the harsh environment and effects discussed in the previous chapter they must be designed from the start with those realities in mind. Integrating SEE mitigation into the circuit design flow could be an entire research field in itself. There are several design flow tools available, all having their respective merits. The circuits in this work were simulated using a compact bias-dependent SE model, discussed in the next section. The bias-dependent model's characteristics were chosen carefully, with an attempt to create a design process that any circuit designer would be able and willing to follow.

After the simulation/design phase and fabrication of an A/MS part, it must still be certified for use. Directly testing these parts for performance in their intended environment is often impossible. Therefore, the radiation effects community has spent a significant amount of effort developing testing facilities and procedures to replicate these environments. The testing in this work was done using a readily available and relatively inexpensive method (~ 12 years old) referred to as two-photon absorption SE laser testing. This testing method and the fundamental concepts behind it will be discussed in the second section of this chapter.

The final section of this chapter discusses in detail the circuits that will be used to experimentally validate the hardening techniques presented in this dissertation. This work uses three different operational amplifier designs in three different technologies (two different feature sizes). The critical design parameters are discussed as well as the pertinent testing configurations, such as inverting with a gain of 10 V/V etc.

Compact Modeling

Microelectronic circuit designers rely heavily on modeling to predict a circuit's behavior for various unknowns, such as process variation and environmental variables. The models they use typically are embedded inside of process design kits (PDKs). At the center of these PDKs is the MOSFET model. These MOSFET models are the most complex and complete of any of the models used throughout the semiconductor industry today. The most widely used of these are the Berkley Short Channel IGFET Models (BSIM) developed for Simulated Program with Integrated Circuit Emphasis (SPICE) simulators. Typically, the final check off for any design intended for fabrication is a complete transistor simulation using these compact models across all parameters, to include process variations, voltage, and temperature fluctuations.

Circuits designed for ionizing radiation environments must meet additional requirements before their designs should be fabricated. If they are not designed and simulated with radiation-enabled models then a designer is using intuition or best guesses to determine appropriate hardening methods. This intuition or guessing is extremely dangerous, because these parts are possibly intended for multi-million dollar systems as pieces of billion dollar programs.

There are many ways to simulate a device or circuit response to ionizing radiation. Each of these techniques and tools have their pros and cons. The methodology used to determine the most appropriate modeling technique in this work is depicted in Fig. III-1, adapted from [33]. Fig. III-1 depicts an iterative process where the user starts on the left with the least accurate simplest model; in this case it could be a simple current source to simulate a SE. Following some analysis and testing, which may come through a literature search, the model is refined with added complexity and accuracy and the process is repeated. The desired end-state of this process is the simplest model with only as much complexity as necessary to achieve the desired accuracy. There is one more factor that comes into play with this model choice, and that is time. The time to learn how to use the model and to actually run the simulations is a key factor. There are models out there that can produce almost exact answers through complex solutions to multiple physics equations. However, these models can take multiple days and multi-threaded computers to run. Circuit designers, for whom this work is intended, tend to frown on these excessive tools. It is for this reason and the fact that the necessary accuracy can be obtained within a SPICE like simulator that this work will only use compact models.

Bias Dependent Model

An ideal way to design a circuit for an ionizing radiation environment is by augmenting the existing BSIM models with a radiation model through a spice sub-circuit, a Verilog-A description, or both. This way a designer can run their usual simulations across process variations, voltages, and temperatures as well as the SE simulations across

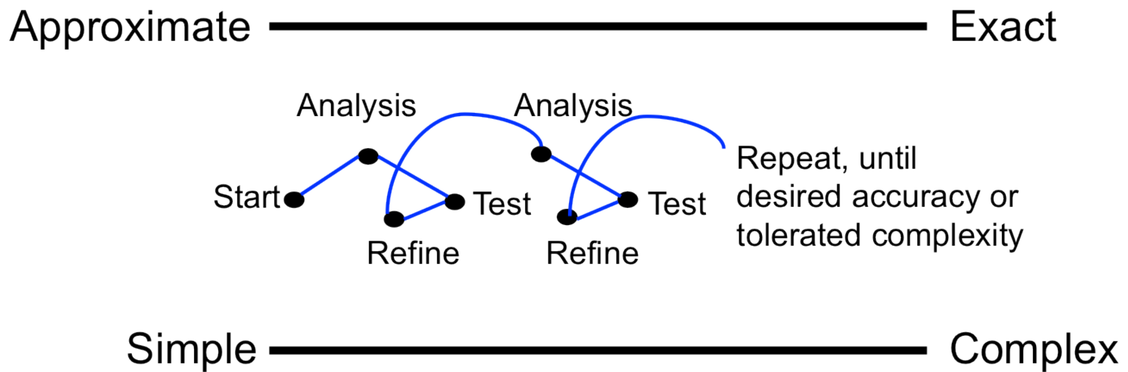


Fig. III-1 Modeling methodology adapted from [33]

desired LETs. However, in the highly scaled technology nodes used throughout the microelectronic industry modeling and simulating SEs can be very complicated.

A major complication with modeling SEs is that circuit response times are starting to be on the order of the characteristic charge generation and collection times following a SE. This is a challenge because the charge collected dynamically interacts and is shaped by the circuit response itself. A second complicating factor is the emergence of the charge-sharing phenomenon [34,35]. Designing hardened circuits using models that account for these complications often require the designer to understand the inner workings of the model itself. The designer must also account for how charge sharing can affect the chosen layout structure.

Traditionally, SEs were modeled at the circuit level using the double exponential current source available in most SPICE simulators [36]. These current sources have adjustable parameters such as rise/fall time and delay that can be used to calibrate to some sort of verified data, either from TCAD or an experiment. The total collected charge can be determined by a simple integration of the double exponential waveform. Equation III-1 relates LET to deposited charge. Equation III-2 is the waveform of the

double exponential used by most SPICE simulators. Finally the last equation, III-3 from the time integral of III-1 gives the peak current of the current source. In III-2 and III-3, τ_R is the characteristic rise time, τ_F the fall time, t_D is the delay time, and I_1 is the peak current at time t_D [37].

$$dQ\left[\frac{pC}{\mu m}\right] = 1.035 * 10^{-2} * LET\left[\frac{MeV * cm^2}{mg}\right] \qquad \text{(III-1)}$$

$$I(t) = \begin{cases} I_1\left(1 - e^{\frac{-t}{\tau_R}}\right) & t < t_D \\ I_1\left(1 - e^{\frac{-t_D}{\tau_R}}\right) & t \geq t_D \end{cases} \qquad \text{(III-2)}$$

$$I_1 = \frac{Q}{t_D + \tau_F - \tau_R - (\tau_F - \tau_R) * e^{\frac{t_D}{\tau_R}}} \qquad \text{(III-3)}$$

The biggest problem with using a double exponential current source and fitting it to a TCAD result with these three equations is that the ideal current source provides the specified current independently of the circuit's behavior. Neglecting the circuit's bias condition and applying this current can force unrealistic voltages at circuit nodes. Fig. III-2 is an illustration of this. It depicts the response of an inverter following a 30 MeV-cm^2/mg strike for a TCAD simulation and a SPICE type simulation utilizing a double exponential current source [38]. Using the previous discussed modeling axiom, the double exponential is simple enough, but lacks the necessary accuracy.

Previous research has shown the importance capturing the bias dependence of the SE response [38, 39]. This work shows that the loading of the struck device also affected the elongated plateau effect of the response. A compact model that accounts for these

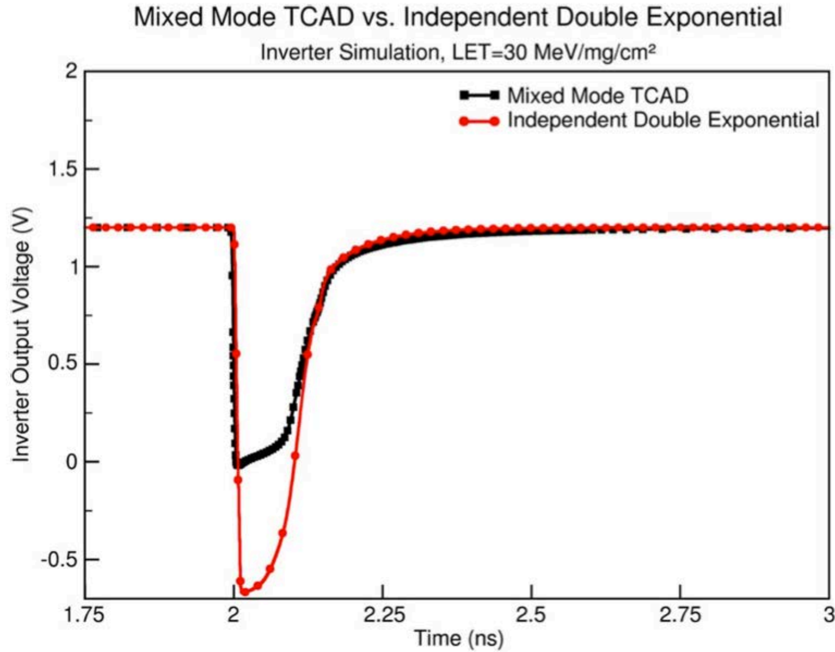


Fig. III-2 Comparison of the response of an inverter following the simulated strike of an ion using a double exponential current source and TCAD [38]

effects is required for a more accurate response. The models used in this work do just that and can be used as standalone current sources or in a BSIM4 integrated version [38]. Fig. III-3 shows a schematic of the model that is implemented in Verilog-A to solve equations III-4 through III-7.

In equation III-4, I_{SRC} represent the time to current profile of the deposited charge from the ion strike and can often use the same values as the double exponential previously discussed. The capacitor C_s ensures charge conservation and acts as a storage element. The voltage across the capacitor is proportional to the charge not dissipated by the two dependent current sources in Fig. III-3. The gain is used typically to represent parasitic bipolar amplification; otherwise it is equal to one. G_{REC} accounts for the recombination in the device and the RecombParameter in III-5 controls that.

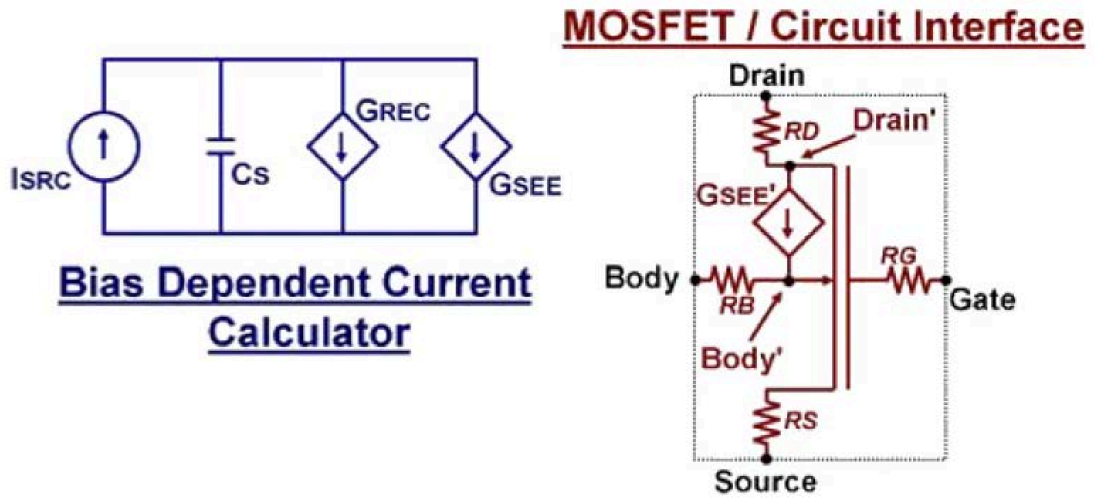


Fig. III-3 Schematic the bias dependent Verilog-A model used throughout this work [38]

$$I_{SRC}(t) + \frac{C_s dV(C_s)}{dt} = G_{REC}(t) + G_{SEE}(t) \qquad \text{III-4}$$

$$G_{REC}(t) = f(V(C_s), C_s, RecombParameter \qquad \text{III-5}$$

$$G_{SEE}(t) = f\left(V(C_s), C_s, f\left(V(drain', body')\right)\right) \qquad \text{III-6}$$

$$G'_{SEE}(t) = G_{SEE}(t) * Gain \qquad \text{III-7}$$

It also significantly impacts the plateau effect. G_{SEE} and G'_{SEE} represent the SE junction current, where G_{SEE} discharges the capacitor and G'_{SEE} is tied to the parasitic resistances of the junctions [38]. Fig. III-4 is the same as Fig. III-2, however this time it compares the bias dependent model versus TCAD for different LETs [38]. Fig. III-4 shows the bias dependent model does a much better job matching the response of TCAD. This model

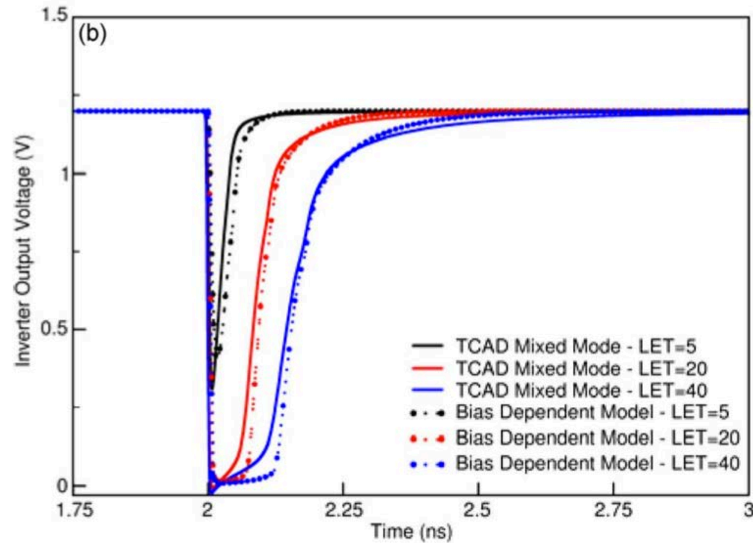


Fig. III-4 The output response of an inverter comparing simulated strikes from TCAD and a bias dependent SE model [38]

can also be used in a SPICE simulation; therefore it meets the modeling axiom's desired simplicity as well.

The bias dependent SE model developed at Vanderbilt University satisfies the requirement to represent a SE in a SPICE like simulator, but this dissertation's research also will explore charge sharing extensively. In fact, because of scaling and the subsequent close proximity of devices in current technologies any models that cannot account for charge sharing and a circuit's susceptibility to it are inadequate. For a model to account for charge sharing as desired it must have some sort of calibration to account for collected charge between adjacent devices and the associated timing parameters.

This work will account for charge sharing in a SPICE based simulation by using a one-time TCAD calibration that measures the amount of charge collected at various distances from a strike and the corresponding timing parameters. This information can be used in a lookup table in conjunction with multiple of the bias dependent current sources previously discussed [40]. Each of the bias dependent sources can have separate timing

and collected charge parameters to correspond to the TCAD calibration. While this technique of accounting for charge sharing is an adequate representation, it does not actually take into account the layout. Using this method it is difficult to compare circuits with different amounts of sensitive area from added devices. These added devices increase the probability of a strike occurring and therefore in certain cases it can be critical that they are accounted for.

Another recently developed Vanderbilt University model can directly take into account the circuit's layout [41]. This tool uses a one-time TCAD calibration as previously discussed including the effects across well boundaries and with different contact spacing. This information is then used in conjunction with the previously discussed bias dependent model. The difference with this model and the previously discussed way of accounting for charge sharing is that the calibration data and bias dependent model are tied together with a series of programming scripts. These scripts build a mesh or series of squares over the entire layout. In each small square of the mesh a strike occurs. The script measures the distance from the strike location to the sensitive junctions in the layout, then cross references the calibrations table to feed the bias dependent models, in the schematic the appropriate information for each corresponding junction. This process is repeated for each square of the mesh and produces a result very similar to a laser raster scan (discussed in the next section). Using this tool each square has an area, therefore a total sensitive area versus some circuit error threshold can be determined and compared from circuit to circuit independent of the circuit's total area. This tool is obviously a little further towards the complex side of the modeling axiom, so it will only be used when necessary.

Laser Testing

Following simulation and fabrication, a part must be tested and qualified for space or for another ionizing radiation environment. The ideal way to test an electronic part of any type for a particular radiation environment is to place the part in that environment for an extended period of time and evaluate its performance. For an electronic part in a multimillion-dollar system intended for space, this is basically impossible. In lieu of this unreasonable type of testing, research communities have attempted to replicate these environmental conditions terrestrially. The most standard way to do this is via a particle accelerator.

Ion accelerator testing with various ion species and LETs is generally considered the most standard test method. However, this type of testing has several drawbacks. There are only a few facilities where this testing can be conducted, so availability of this resource can be an issue. Access to an ion accelerator-testing site, often referred to as beam time is also very expensive. The two of these things coupled together make it extremely difficult to get a thorough evaluation of a part, particularly an A/MS part. Digital parts designed for testing are often large arrays of memory or vast chains of inverters that present extensive sensitive area for the ions to hit as a target. This allows for a statistically relevant number of SEs to occur in a reasonable amount of time. Creating a large array of sensitive area can be much more difficult for an A/MS circuit, which leads to the need for more beam time and therefore even higher cost. Another significant drawback of heavy ion testing is part degradation. The testing’s required exposure to a high fluence can lead to significant degradation or complete part failure.

The drawbacks above were part of the reason that the radiation effects community started to research alternative testing methods. Laser testing, the subject of this section surfaced as an attractive alternative. Laser testing is not only cheaper and more easily available, but it also adds the capability to gain spatial and temporal information that ion testing does not (spatial information is starting to become available with micro-beam testing now). Another significant advantage of laser testing is that if the laser's energy is monitored carefully part degradation can be avoided completely.

Laser testing was originally developed using lasers with wavelengths greater than the bandgap, approximately 590 nm. In this region, Beer's Law absorption, where each absorbed photon generates a corresponding electron-hole pair and the generated carrier density decreases exponentially into the incident material is dominant [42]. This exponential decay of carrier density with depth into the material, requires the device under test (DUT) to be tested from the top. The increased densities and levels of metallization coupled with the design rules of modern processes make this extremely difficult if not altogether impossible. This led to the development of two-photon absorption (TPA) testing.

TPA uses sub-bandgap wavelength lasers with femtosecond pulses. Due to the sub-bandgap wavelength of the laser negligible amounts of electron-hole pairs are generated from a single photon at low intensities [43-44]. In the case where this light is highly focused however, it is possible for two photons to be absorbed simultaneously in the region where the light intensity is the greatest, creating an electron-hole pair. The need for a highly focused area of the laser allows electron-hole pairs to be generated only at desired location inside the DUT [42]. As the next few paragraphs will discuss it also

removes the exponential decrease of carrier density from the surface of the target material, allowing for testing through the backside of the wafer. This allows for testing in these advanced processes that was difficult if not impossible with the single-photon absorption method previously discussed.

Fig. III-5 shows the absorption spectrum of silicon across regions of the electro-magnetic spectrum [42]. The silicon absorption spectrum depicted in Fig. III-5 shows very little to no absorption in the sub-bandgap region. Wavelengths greater than 1150 nm have a negligible absorption coefficient. This implies that the majority of carriers generated with a wavelength greater than 1150 nm are created via multi-photon absorption. The wavelength of the testing facility used in this work, Naval Research Laboratory (NRL) is 1.26 μm with a photon energy of approximately 1 eV. Lasers used for SE testing typically have a Gaussian radial intensity distribution. Fig. III-6 is the longitudinal profile of such a beam with the appropriate variables labeled [45]. The variables in this figure can be derived with a few equations. The radius of the beam, which is defined as the point where the laser intensity has decayed to 1/e of its peak value is given in (III-8), where w_o is the 1/e radius of the beam waste, λ is the wavelength, z is the direction of beam propagation, and n is the index of refraction for the medium. The beams confocal parameter (III-9) is the region in which w_o is less than or equal to $\sqrt{2}w_o$.

$$w(z)^2 = w_o^2[1 + (\frac{\lambda z}{\pi w_0^2 n})^2] \quad \text{(III-8)}$$

$$b = \pm \frac{\pi n w_0^2}{\lambda} \quad \text{(III-9)}$$

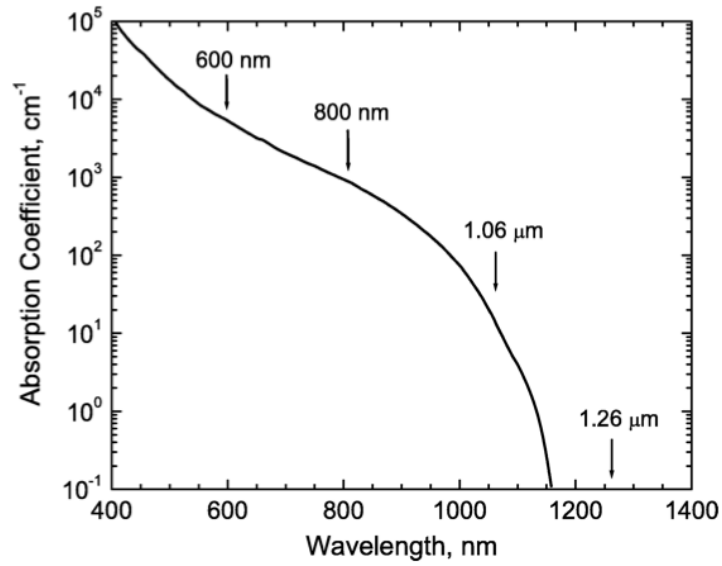


Fig. III-5 Absorption spectrum of silicon at room temperature [42]

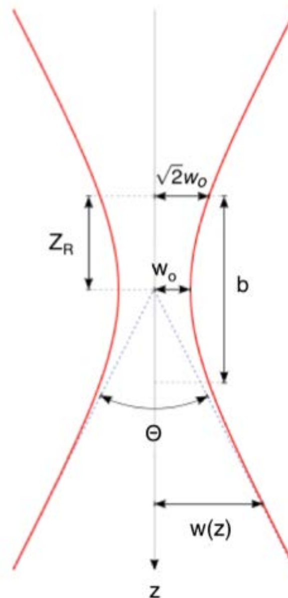


Fig. III-6 Gaussian beam longitudinal profile with appropriate parameters labeled [45]

Half of the confocal parameter b is the Rayleigh range Z_R. The beam remains well collimated for twice the confocal parameter within the vicinity of w_o. The total angular speed is twice the beam divergence and denoted by Θ. The radial dependence of the pulse irradiance is given in (III-10), where P is pulse power and r is the distance relative to the z axis [45].

$$I(r,z) = \frac{2P}{\pi w^2} e^{\left(\frac{-2r^2}{w^2}\right)} \qquad \text{(III-10)}$$

In a Gaussian beam the product of the width and the divergence is minimized. This implies that once the beam is focused to a spot, it will spread out rapidly as you move away from that spot. This is desirable for SE testing because it means that electron-hole pairs will only be generated in the immediate vicinity of the laser spot.

A brief explanation of the details of TPA will be provided in this section, a more detailed description of the mathematics and physics behind it can be found in [42]. In order to get a complete mathematical description of carrier generation and pulse propagation in silicon a solution of a set of coupled differential equations is required and is fairly complex. However, equation III-11 is the primary equation responsible for carrier generation and will suffice for this works intent. In III-11, N is the density of free carriers, α is the single photon absorption coefficient (Beer's Law absorption), I is the pulse irradiance, β is the two photon absorption coefficient, and ħω is the photon energy. The two in the denominator of the second term in the equation accounts for the requirements of two photons being absorbed to generate a single electron-hole pair in

$$\frac{dN(r,z)}{dt} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \quad \text{(III-11)}$$

$$\frac{dN(r,z)}{dt} = \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \quad \text{(III-12)}$$

TPA. For TPA, an above bandgap wavelength is chosen, this sends α in III-8 to zero, reducing III-11 to equation III-12 [42].

The absence of Beer's Law absorption in equation III-9, shows that the carrier generation from TPA is proportional to the square of the laser pulse energy. This also demonstrates that the attenuation from Beer's law absorption is absent, allowing significant carrier generation to occur only in the focal region of a focused laser beam [42]. Figs. III-7 through III-9 will further help demonstrate the difference [42]. In Fig. III-7 the exponential decay of carrier generation with penetration depth in single-photon absorption according to Beer's Law is clearly present in the simulation result. In contrast, Fig. III-8 depicts the carrier generation from a TPA process (1.26 µm wavelength) where the carriers are highly concentrated in the high irradiance region near the focus of the beam. This highly concentrated region can be directed to any depth in the target material.

Fig. III-9 is an enlargement of the simulated confocal region of Fig. III-8. The comparison of carrier distributions in Figs. III-7 and III-9 clearly shows that the results in III-9 much more closely resemble the track of the highly energetic particle they are intended to represent. There are two primary reasons for the better representation. First, the carrier density does not decrease exponentially along its track like in SPA. The second reason is due to the I^2 dependence, which forces the carrier density to fall off outside the confocal region.

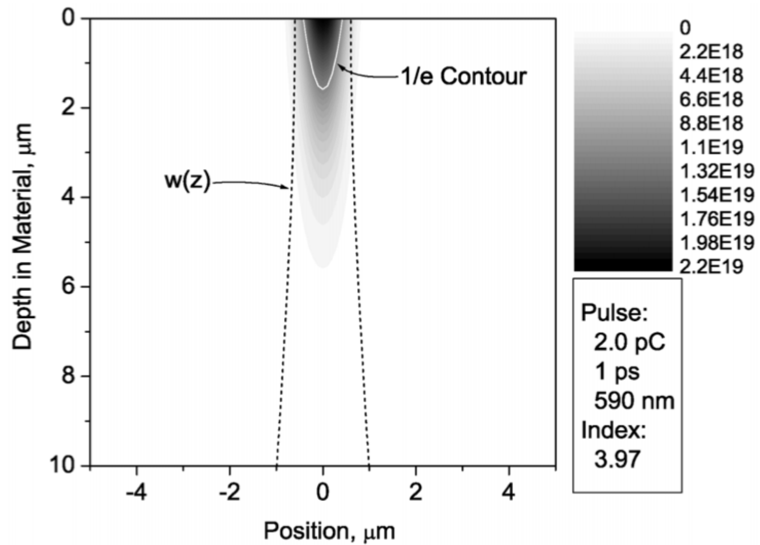


Fig. III-7 A graphical representation of the carrier generation from SPA, where the exponential roll off with penetration depth is clearly present [42]

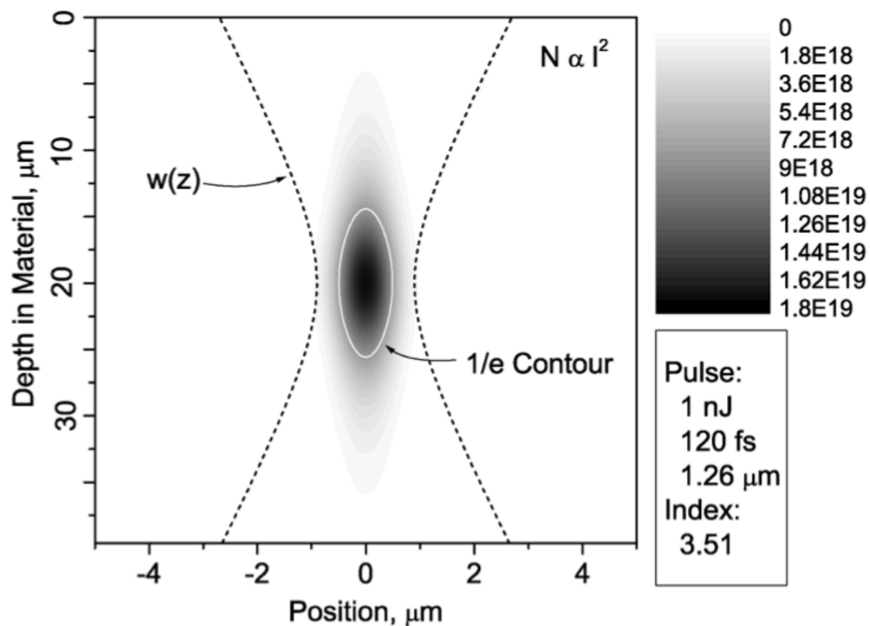


Fig. III-8 The carrier generation of a TPA process where the carriers are highly concentrated around the focus of the beam, without the exponential decay related to penetration depth in SPA [42]

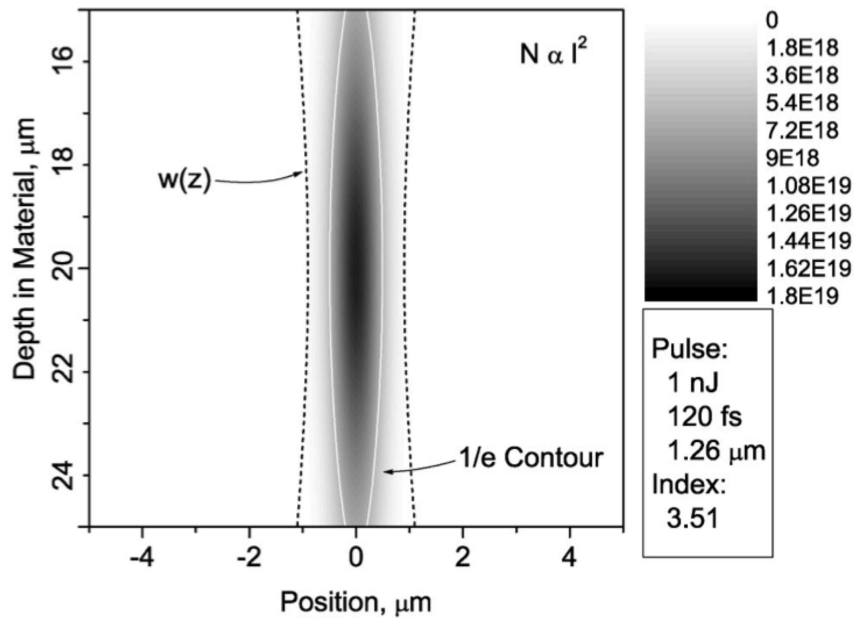


Fig. III-9 Carrier density plot of Fig. III-4 blown up around the confocal region [42]

The abilities for carrier generation to be confined to the high-irradiance region of a sub-bandgap beam and to move that region anywhere within Silicon allows three dimensional SE testing through the backside of ICs [46, 47]. The facilities at Naval Research Laboratory (NRL) were used extensively for this purpose throughout this research. The TPA setup at NRL, depicted in Fig. III-10 uses an amplified Titanium sapphire laser (Clark-MXR CPA 1000) tuning an optical parametric amplifier. This produces a 140 fs optical pulse with a wavelength of 1.26 μm and approximate energy of 100 μJ [47]. As shown in the figure the beam is attenuated by a waveplate polarizer combination to help precisely control and vary the intensity reaching the tested device. The energy reaching the tested device is monitored by an InGaAs photodiode. The beam is then focused through a microscope (100X for this research) resulting in a Gaussian beam with an approximate spot size of 1 μm. That beam can then be moved across the tested device in 100 nm steps using a motorized xyz translation platform [47]. At each

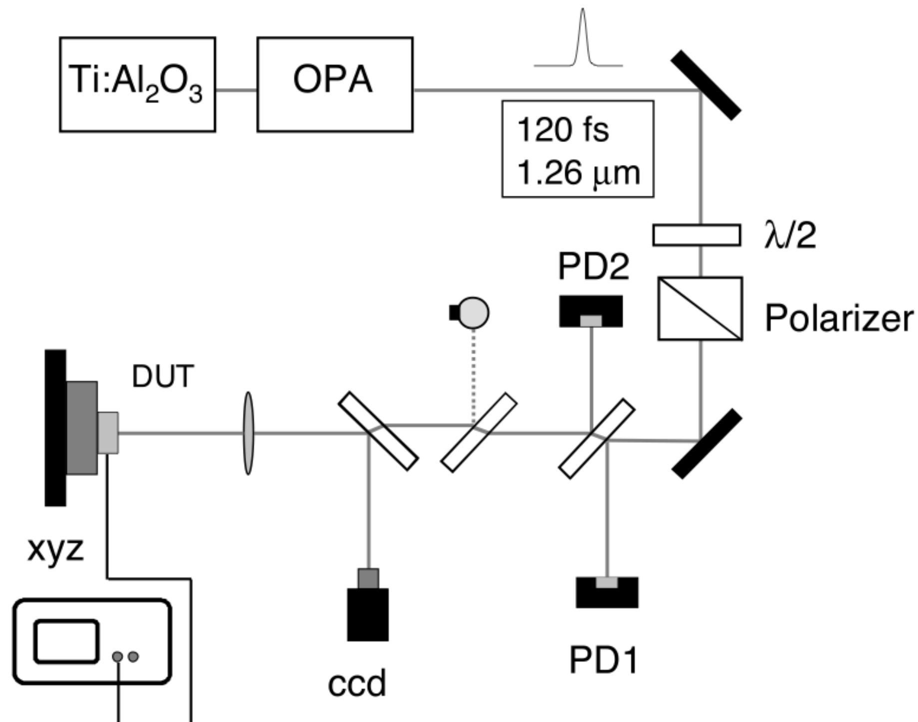


Fig. III-10 Experimental setup of TPA system at NRL [47]

100nm or larger step a SE occurs and the results can be recorded, allowing for a correlation of the response and spatial location in the tested device.

Operational Amplifiers

Operational amplifiers (op amps) are essential building blocks that are ubiquitous in analog and mixed-signal (A/MS) design. They are critical components in everything from DC applications, like bias circuits, to sophisticated AC applications, like amplifiers and filters. The array of applications where op amps can be used, often as the primary component, includes integrators, differentiators, comparators, and negative impedance converters. In more complex systems they serve as critical components for things like

analog-to-digital (A to D) converters and reference circuits. There are very few non-trivial A/MS designs that do not include op amps.

The importance of op amps to A/MS design coupled with economic incentive to integrate op amps and digital circuits into single integrated circuits at cutting edge feature sizes has created significant challenges for op amp designers. Examples of these challenges are lower transconductance when compared to their bipolar counterparts and less voltage headroom. In an effort to combat these difficulties and create quality amplifiers, designers have developed a multitude of different op amp variants. The three op amps used in this work are all variants of a folded cascode design. This op amp design was chosen because it has become one of the most common designs since first being introduced in 1994 [48].

The three different versions of the folded cascode op amp used in this work were also built in three separate technologies. These separate technologies were used for a multitude of reasons to include availability, sponsoring agent desires, industry norms, and finally to investigate both bulk and silicon-on-insulator (SOI) technologies. The IBM 180 nm bulk technology was of particular interest to not only research sponsors, but also the industry at large. The 180 nm technology node is considered an analog “sweet spot” to many in industry because it provides a good balance between small feature size and voltage headroom. The use of multiple IBM technologies with a 180 nm feature size (CMHV7SF and CMRF7SF) was primarily driven by silicon availability. The use of IBM’s 32 nm SOI technology (CMOS32SOI) was driven by two factors, availability and desire to prove that node splitting works as a hardening mechanism in SOI as well as

bulk. The fact that 32nm was a cutting edge feature size, particularly for A/MS design was an added benefit.

Fig. III-11 depicts the single-ended output, bulk technology, folded-cascode op amp used in this work with each of its stages labeled. The complementary topology with both an NMOS and PMOS input pair was chosen because of its rail-to-rail input range. The design also has a self-biased cascode stage that provides a resistive load for the input stage and therefore a high voltage gain. Finally, the push-pull source follower output buffer is used to isolate the cascode output stage from the chip and packages output pads.

The test chip had designs of this op amp with both 0.5 μm and 2 μm channel length input devices. These variants were included for multiple reasons. The first is that longer channel length devices are often used to minimize offset voltage. The other reason was to experimentally prove that the effectiveness of the hardness technique was tied to the active-to-active spacing rules of the PDK and not the channel length. The op amp has an open loop gain of approximately 73 dB and a power supply rejection ratio (PSRR) of 123 dB to both the positive and negative voltage rails. The gain-bandwidth product (GBWP) is approximately 5 MHz; with a ± 10 mV input referred offset voltage. The layout of this op amp can be seen in Fig. III-12.

The fully differential op amp used in this work is shown in Fig. III-13. This op amp was designed in the IBM CMRF7SF 180 nm process. This op amp is a modified version of the op amp in Fig. III-11. The input and bias stages remain unchanged, the cascode output stage was modified to become fully differential, and common-mode feedback circuits were added to prevent the DC component of the output voltage form drifting. The op amp open loop gain is 71 dB with a GBWP of 35 MHz. The input

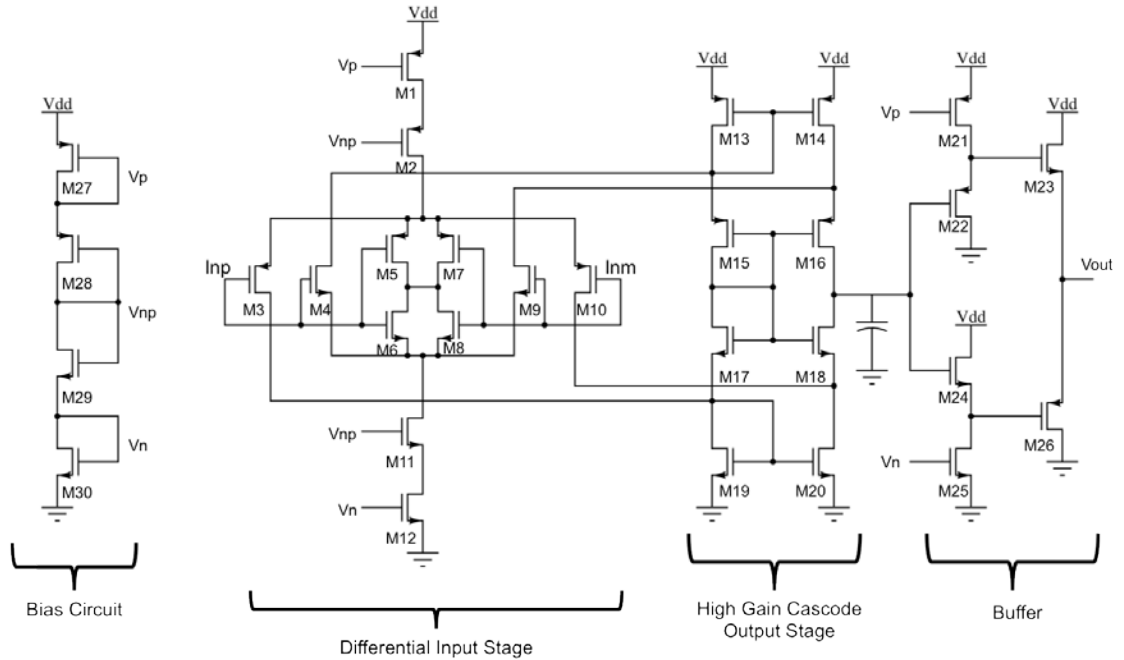


Fig. III-11 The single-ended output folded cascode op amp used in this work, design in an IBM bulk 180 nm process

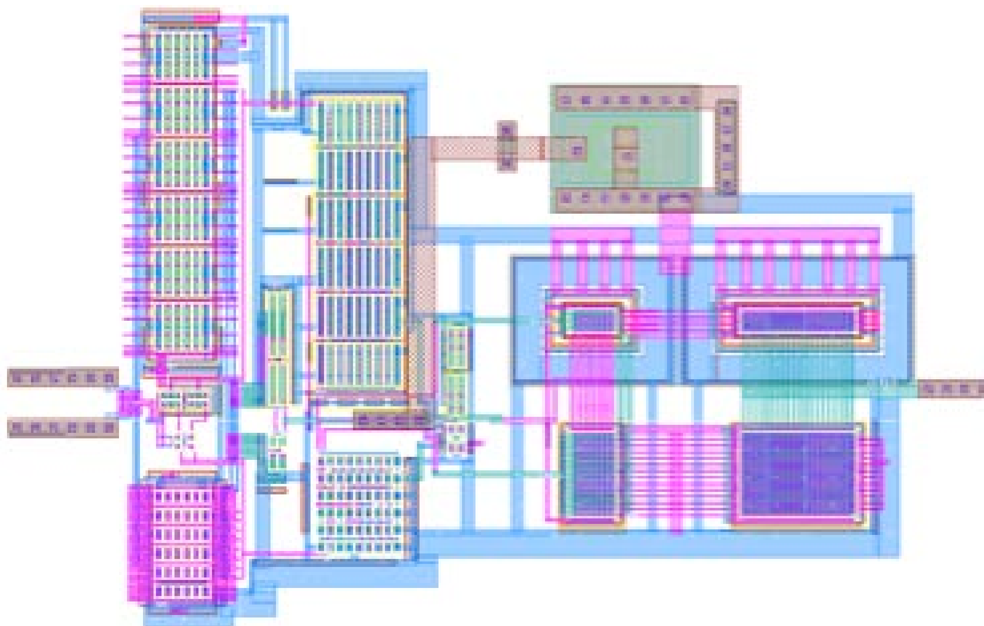


Fig. III-12 Layout of the single-ended output folded cascode op amp used in this work, design in an IBM bulk 180 nm process

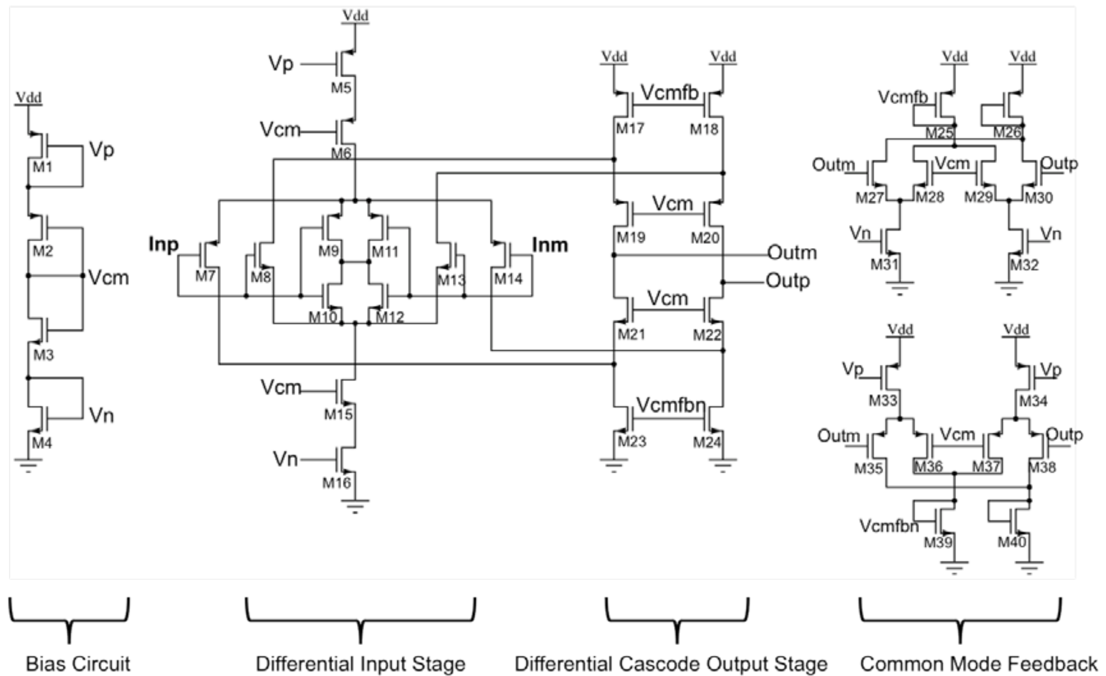


Fig. III-13 The fully differential complementary folded cascode op amp used in this work design in an IBM 180 nm process

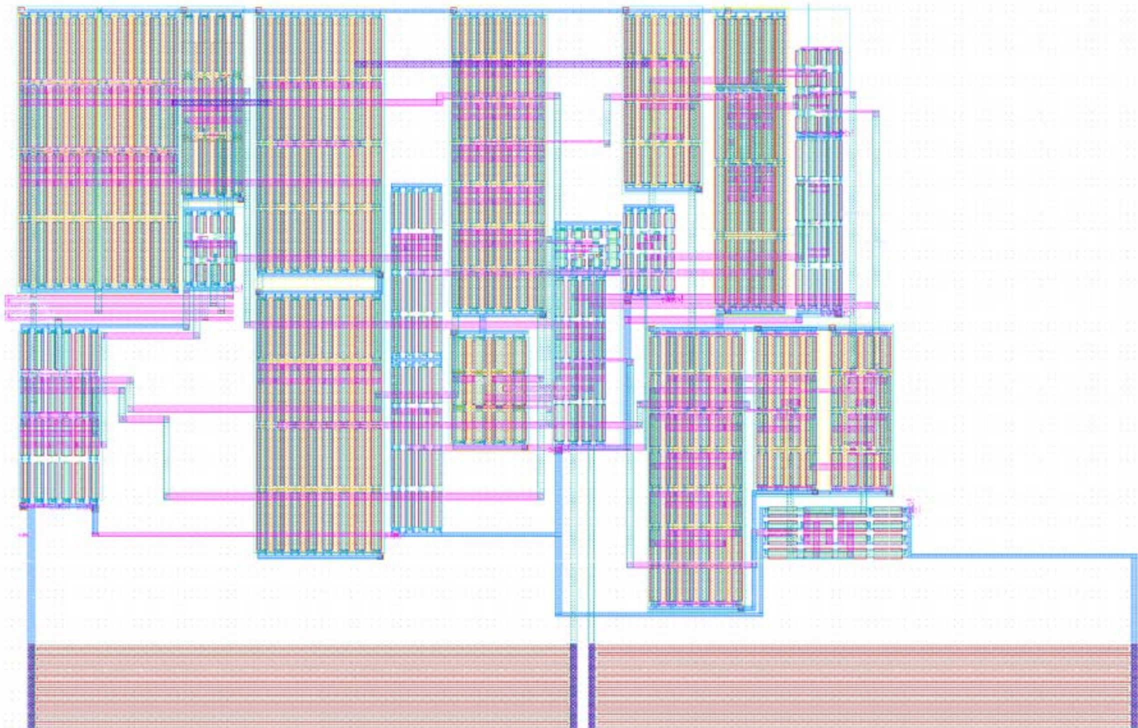


Fig. III-14 Layout of the fully differential complementary folded cascode op amp used in this work design in an IBM 180 nm process

referred offset voltage is approximately ± 10 mV with a CMRR of 140 dB. All the devices in this design have a 0.5 μm channel length and use a 1.8 V voltage supply. The op amps layout is depicted in Fig. III-14.

The final op amp used in this works was based on the complementary folded cascode design from Fig. III-11, but had to be significantly modified to work in a 32 nm SOI process. Unlike the previously discussed 180 nm op amps, the 32 nm op amp does not run on a 1.8 V voltage supply. It only uses 900 mV, requiring an innovative biasing structure to overcome the low voltage headroom. The other significant challenge posed by the 32 nm SOI technology was the very limited choices for channel length with the analog threshold voltage body-tied devices used in this design. There were four possible options for channel lengths, the amplifier itself used the devices with the 490 nm channel length while the bias circuit primarily used devices with a 100 nm channel length. The smaller device length could be used in the bias circuit because matching was of much less concern because it does not directly affect the offset voltage.

The bias circuit used for the 32 nm design is shown in Fig. III-15. The bias circuit is composed of a modified bootstrap current source and a current mirror network that is used to generate biasing voltages for the op amp. The bootstrap current source, labeled current source in Fig. III-15 is a modified version of the analog building block traditional current source that will be discussed in chapter VI. This modified version has a differential amplifier built into it (M9 and M10). The purpose of the differential amplifier is to sense a voltage difference between the drains of M8 and M11 and regulate them to be the same. The result is an effective increase M11’s output resistance. This regulation

scheme uses feedback, therefore stability is of concern and that is why the MOSFET between M5 and M12 is present as a capacitor.

The actual op amp used in the 32 nm SOI design is shown in Fig. III-16. The basic design is very similar to that of Fig. III-11 with complementary input devices that give a rail-to-rail input range. The cascode output stage has been modified to add floating current sources M19-M22 to combat the limited voltage headroom. Finally, this design has a push-pull amplifier in the buffer stage giving it a significant advantage of rail-to-rail output swing when compared to that of Fig. III-11 (at the cost of CMRR). This design has an open loop gain of approximately 76 dB and a GBWP of 650 MHz. The CMRR and PSRR for this design are a little lower than the single-ended 180nm design at 73 and 90 dB respectively. The aggressive GBWP of this design forced its phase margin to be close to zero and therefore have marginal stability in a unity-gain configuration. It is for this reason that this device was tested with a large loop gain, maintaining stability. Fig. III-17 shows the layout of the design.

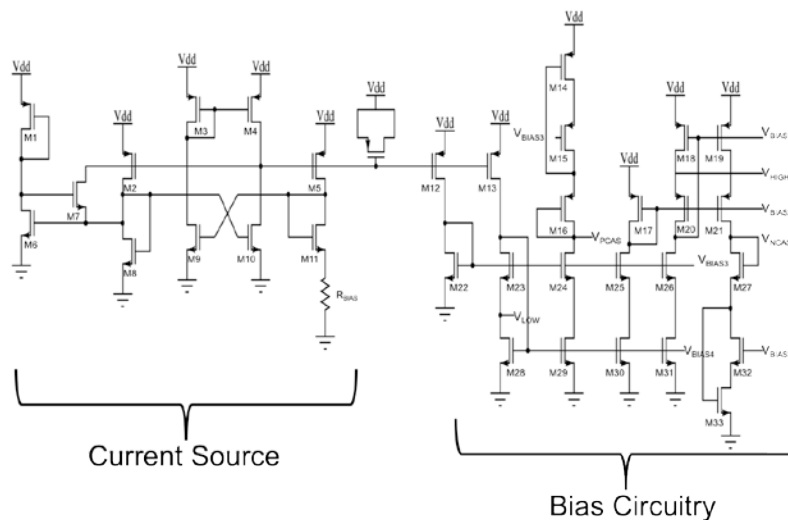


Fig. III-15 The bias circuit used in the 32 nm SOI op amp design. It is composed of two parts, the actual current source and a current mirror network that biases various parts of the amplifier

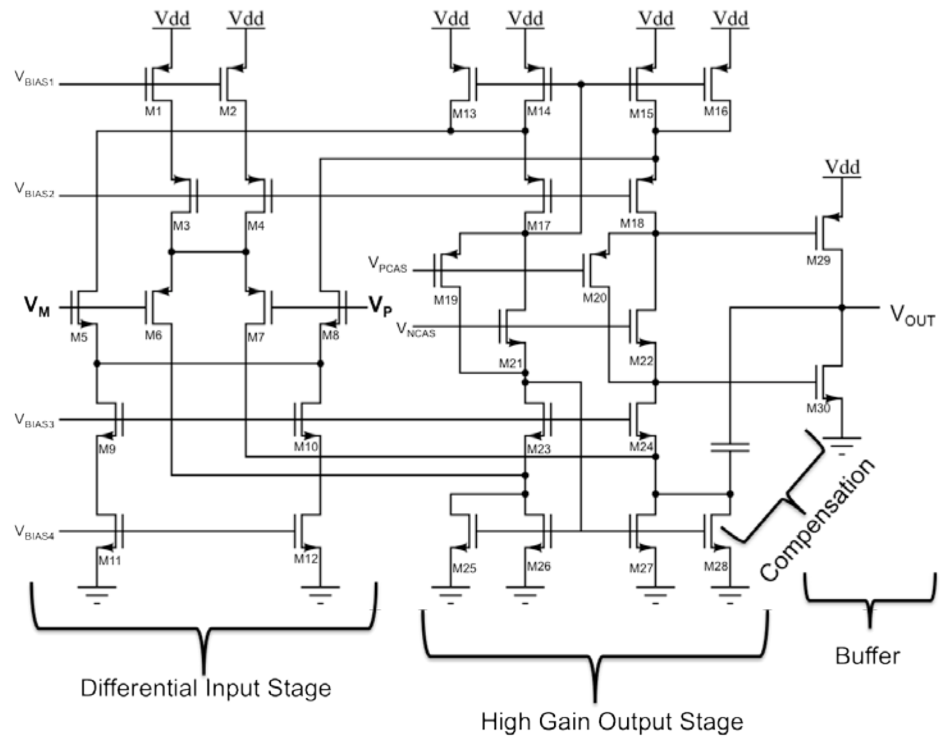


Fig. III-16 The complementary folded cascode op amp design used in the 32 nm SOI test chip designs

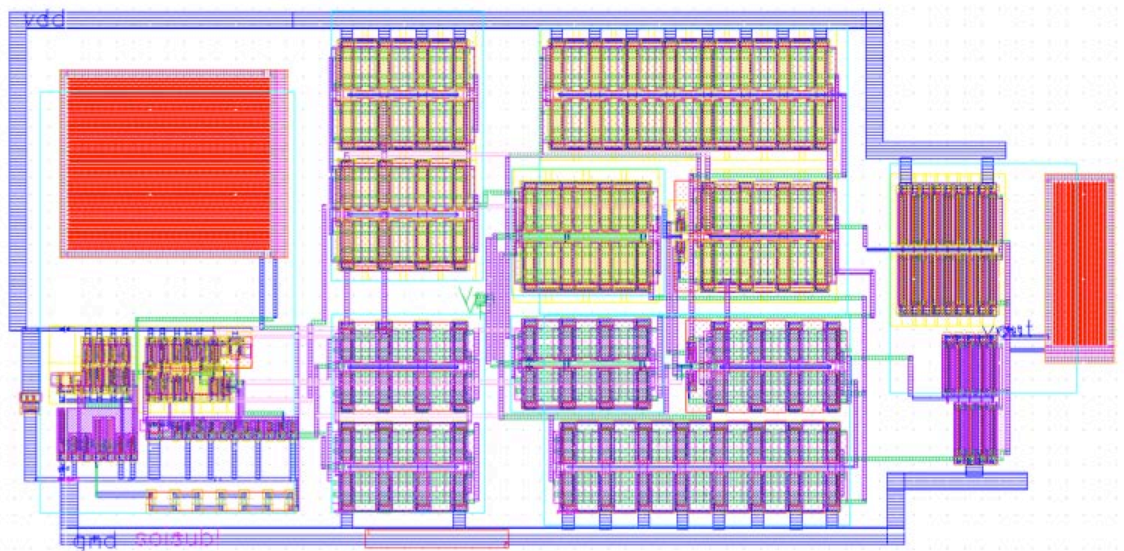


Fig. III-17 Layout of the baseline 32 nm SOI complementary folded cascode op amp design used in this work

Table III-1 is a provides a reference for each of the three previously discussed op amps with the pertinent measured design specifications.

Op Amp	A_{OL} (dB)	GBWP (dB)	CMRR (dB)	V_{OS} (mV)
180 nm Single Ended Output Op Amp	73	123	5	± 10
180 nm Full Diff Op Amp	71	140	35	± 10
32 nm Single Ended Output Op Amp	76	73	650	± 10

Table III-1 Design parameters of the three operational amplifiers used for experimental verification

Conclusion

This chapter presented a basic modeling methodology for SE environments intended for use by A/MS circuit designers. The model chosen using this methodology avoids the pit falls of unrealistic nodal voltages encountered by traditional models. It also has the ability to represent charge sharing which is a critical phenomenon in modern processes. The model can be used in a multitude of ways but maintains the key idea of simplicity for the circuit designer.

The second section of the chapter focused on a verification process of a part designed for SE environments. A cheap, accurate, and readily available technique called two-photon absorption was described in detail. This technique not only replicates the track of an energetic ion as it interacts with silicon, but it also can be directed to any specific location in an IC. These modeling and testing techniques will be used extensively in the following chapters.

Finally, the three op amps that are used as test vehicles for verification of the novel radiation hardening techniques in this work were introduced. These three different variants of the folded cascode op amp, designed in three different technologies, were chosen for their simplicity and because of the fundamental nature of the design. The next chapter will discuss the first class of these hardening techniques, hardening via charge sharing, using the modeling, laser testing, and op amps discussed in this chapter.

CHAPTER IV

HARDENING VIA CHARGE SHARING

Introduction

Chapter II discussed some common hardening techniques for A/MS circuits. The majority of these traditional techniques can be considered brute force, and come with significant penalties in terms of area, speed, and/or power. This section will introduce two novel radiation hardened by design (RHBD) techniques geared specifically for A/MS design. The novel RHBD techniques introduced in this chapter can be classified into one of the two broad hardening categories introduced in this dissertation, hardening via charge sharing.

Differential charge cancellation (DCC) layout and sensitive node active charge cancellation (SNACC) both leverage charge sharing. DCC layout uses charge sharing to turn a single-ended SE error signal into a common-mode signal that will be rejected by a differential circuit's inherent common-mode rejection property. SNACC on the other hand uses charge sharing to sense that a SE has occurred and then active compensation circuitry to either sink or source the necessary current to mitigate its effects. The compensation circuitry needed for SNACC can be added to the original circuit design or in some cases is already part of the original circuit, requiring no additional circuitry. These two hardening by charge sharing techniques will be experimentally verified on a single ended output operational amplifier (op amp), a differential output op amp, or both,

using the two-photon absorption (TPA) laser testing technique described in the previous chapter.

Differential Charge Cancellation (DCC) Layout

The hardening technique coined differential charge cancellation (DCC) layout for the first time in this research is not an entirely new idea. This idea is actually as old as differential circuits themselves. Noise suppression due to common mode rejection is one of the fundamental advantages of differential circuits. The first time that common-mode rejection is emphasized in the radiation effects literature was in 2006 [49]. In this paper, the authors described a radiation-hardened (total ionizing dose and SEE), wideband, low-noise amplifier (LNA). The amplifier was built in a 0.25 µm SiGe BiCMOS process. The authors, in this paper were attempting to thwart the single-event latchup (SEL) problems inherent to this BiCMOS process through careful layout. They noted in the process that they "fortuitously" discovered that the layout techniques they were exploring, to include common-centroid layout, had added SE mitigation benefits. It was noted that a common-centroid layout could increase the likelihood that a SE could appear as a common-mode disturbance. The authors explain this mechanism in detail, but do not appear to suggest maximizing this layout by altering traditional common-centroid layout to a radiation-hardened version. The direct comparison is also slightly clouded by the fact that the devices were bipolar, as opposed to the CMOS devices used in this work.

In 2007, a paper first suggests altering the traditional common-centroid layout to maximize the relatively new phenomenon of charge sharing between sister devices in a differential signal path [50]. The idea was to maximize the amount of common charge

collected between the two devices. Doing so would turn the typically single-ended SE error signal into a common-mode signal that the circuit's common-mode rejection property would negate. The fundamental difference between this work and the previously discussed work, besides the technology used, is the concept of enhancing the amount of common charge collection.

This novel idea was to alter the traditional common-centroid layout technique of interleaving unit-cell sister devices to maximize symmetry and therefore matching. This alteration would alternate devices with the two proximal devices drains closest to each other, maximizing charge sharing. The hypothesis was that the gain in SE immunity would prove more beneficial than the loss of symmetry/matching. In order to test this hypothesis, three-dimensional TCAD simulations were performed on the structures shown in Figs. IV-1 and IV-2. The simulations were calibrated to a commercially available 130 nm CMOS process. Only the areas in the figures surrounded by the black boxes were simulated. Symmetry was used to predict the performance of the remaining portions of the devices. This was done to allow the simulations to have a dense enough mesh for realistic results and still converge in a reasonable amount of time.

The results of these simulations are shown in Fig. IV-3. The results are presented as the amount of differential charge collected for each of the two layouts in Figs. IV-1 and IV-2. The concept is that the total amount of charge collected between the two cases was the same, therefore any reduction in differential charge corresponds to an increase in common charge collection. Common charge collection leads to common-mode signals and therefore rejection. This TCAD simulation data was applied to the input switches, external to the op amp in a sample-and-hold amplifier to perform a mixed-mode TCAD

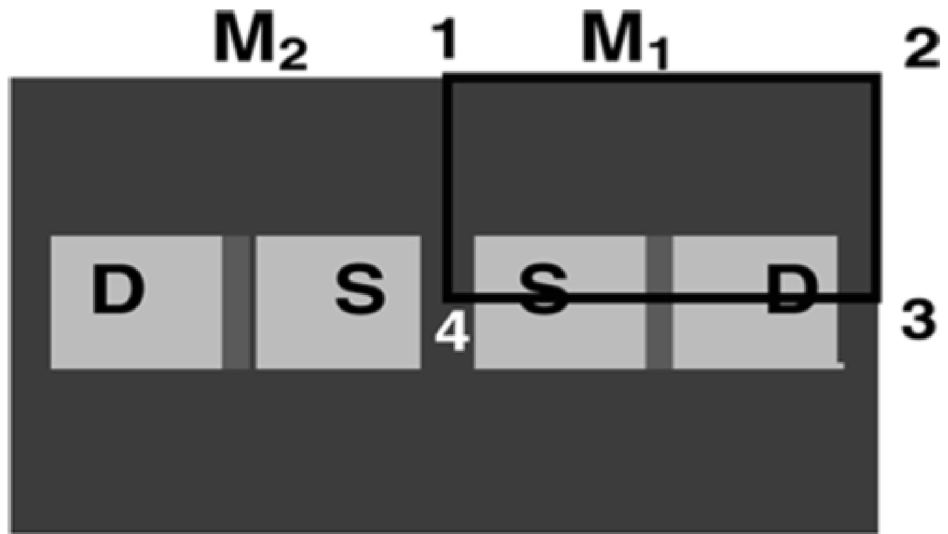


Fig. IV-1 The structure simulated via 3D TCAD to represent a traditional common centroid layout. [50]

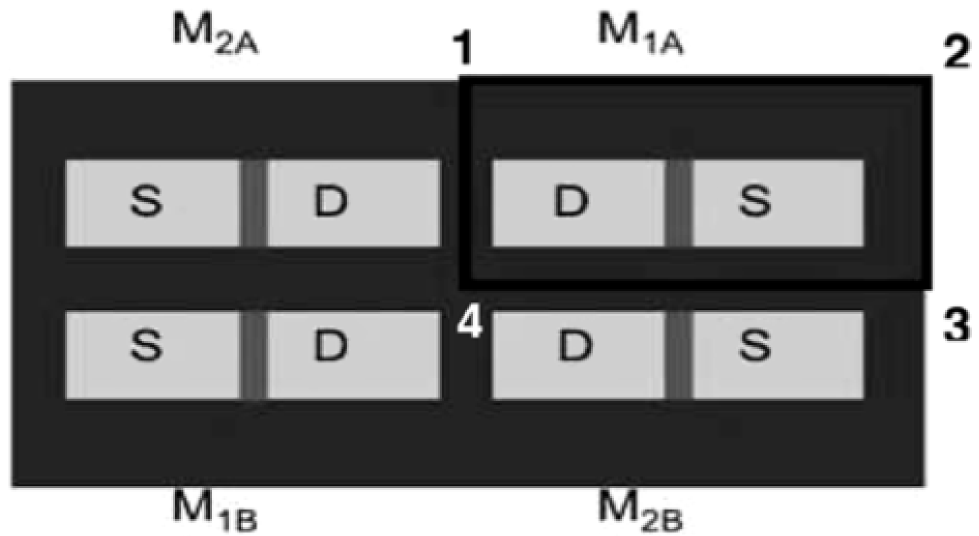


Fig. IV-2 The structure simulated via 3D TCAD to represent the propose alteration of common centroid layout where sister devices have the drains placed at minimal spacing. [50]

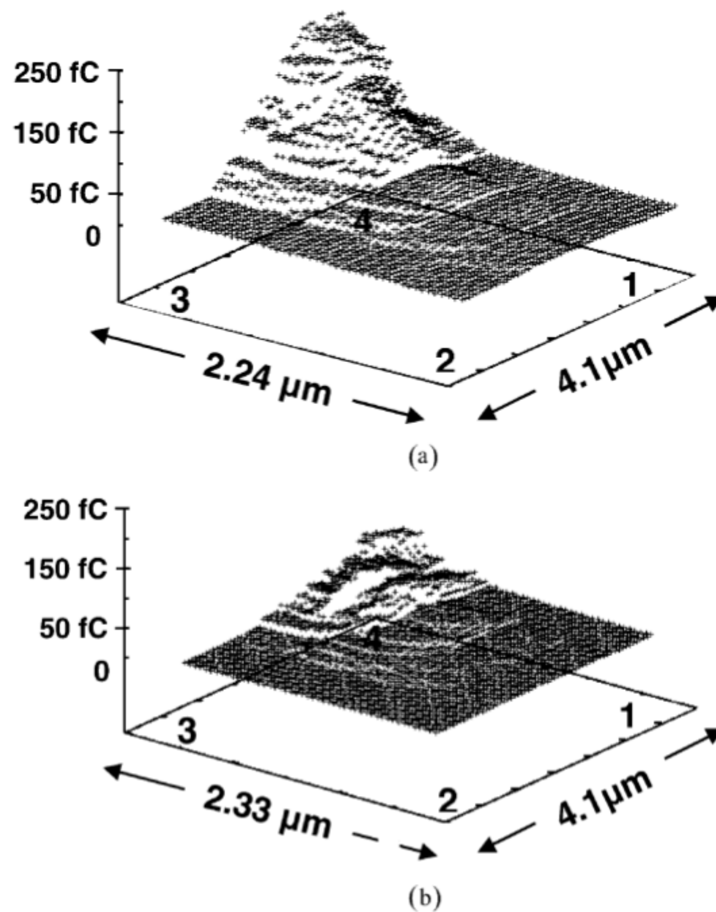


Fig. IV-3 3D TCAD results indicating a reduction of differential charge collected via the layout in IV-9 (b) compared to the layout of IV-8 (a) for a 50 MeV-cm^2/mg strike. The implies the amount of common charge collected increase in (b) [50]

simulation. These simulations suggested that a large reduction in voltage perturbation greater than 100 mV could be achieved by applying this technique to devices in a differential signal path.

The next step in the evolution of this concept was to build some physical structure to verify these simulations, and that is what was done in [51]. Structures were fabricated very similar to those in IV-1 and IV-2, using a 65 nm technology node. These test structures were taken to NRL for through-wafer two-photon absorption (TPA) testing.

For the laser test, two sets of NMOS devices, laid out as shown in Fig. IV-4, were scanned using a 0.3 µm step size. At each point in the scanning process a charge measurement circuit determined the amount of charge collected following the SE strike. This measurement of charge was done via a voltage on a capacitor and the Q=CV relationship. Readers interested in the measurement circuit itself are directed to [50] for further detail. Following the scans of the two devices, the authors were able to determine the amount of differential charge collected in very much in the same way as the previous paper discussed [50]. Fig. IV-4 is a sample of these results. The results indicate that the sensitive area can by reduced by at least 50% over the baseline case by using this technique.

The final section of this work, discusses using the technique to harden an actual circuit. This technique was applied to a differential pair in a SerDes sub-circuit. Using the Cadence Spectre environment and a 90 nm process design kit (PDK), simulated strikes to these devices were conducted using the collected charge values determined during the previously discussed laser experiment. These simulations showed a 56% reduction in maximum perturbation using this technique.

The previous three papers laid an extensive groundwork for the concept of a differential charge cancellation layout. However, the only thing they definitively proved was that the change in layout, from a traditional common-centroid to a DCC layout with sister devices having their drains placed at minimal technology spacing, would decrease the amount of differential collected charge. The authors suggest that this technique could significantly harden a circuit against SEEs, but to what extent and with what penalty was left undefined or only speculated upon.

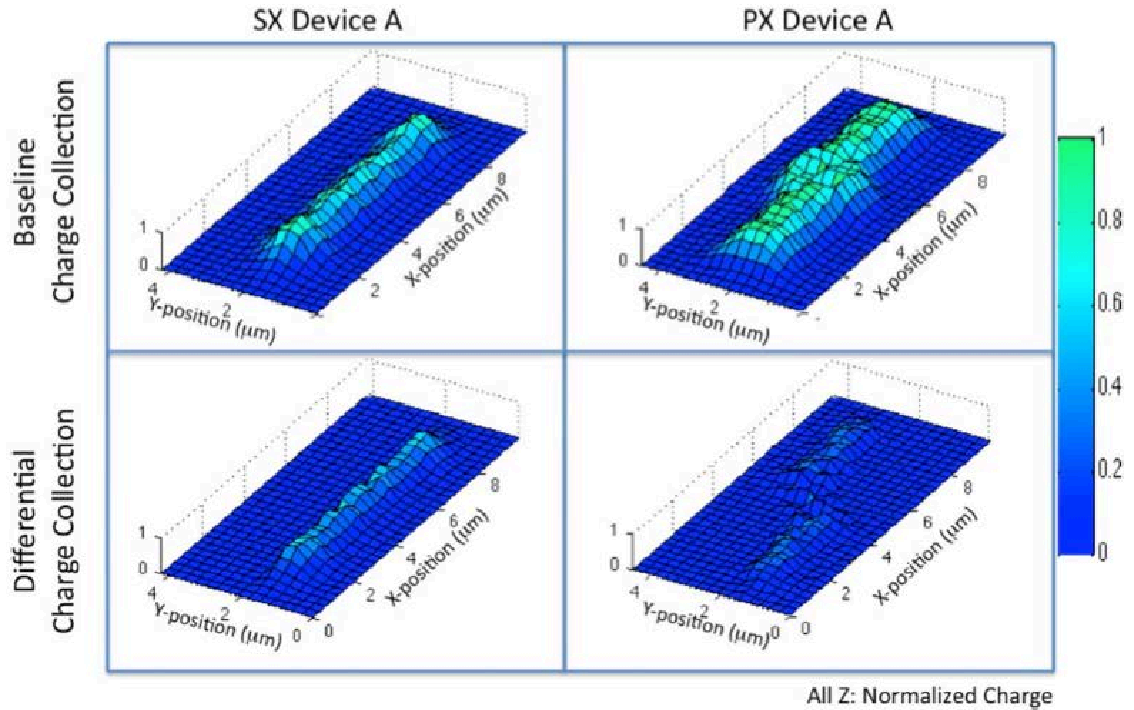


Fig. IV-4 Results from Armstrong *et. al.*'s, laser experiment on the devices shown in IV-10 designed in a 65 nm process and tested via TPA at NRL. Differential charge collection is plotted in the z plane, normalized to maximum charge collected [51]

In order to address these shortcomings in the development of this technique a test chip was design using the IBM 180 nm PDK and the op amp described in Fig. III-11. The chip contains four distinct variants of this op amp for the purpose of the test, two designs with 0.5 µm channel length input devices one with a traditional common centroid layout and one with a DCC layout. There are two more op amp variants with 2 µm channel lengths with and without hardening. The reason for the two different channel lengths was as discussed in chapter III. Representative layouts of the traditional common-centroid layout (unhardened) and DCC hardened PMOS input stages are shown in Fig. IV-5 (a) and (b) respectively.

Experiments were performed at the Naval Research Laboratory (NRL) using the through-wafer TPA laser facility to mimic the charge deposition of ion strikes in active

silicon areas as discussed in the chapter III. Two-dimensional scans were performed for the input stages of the unhardened (common-centroid layout) and RHBD (DCC layout) operational amplifier designs on the 180-nm test chip. At each x-y point in the scan, sixteen laser-induced transients were captured and averaged on an oscilloscope.

The operational amplifiers were tested in an inverting configuration with a gain of 10 V/V, using resistor values of 1 MΩ and 100 kΩ. The supply voltage VDD was set to 1.8 VDC, with a 0.9 VDC common-mode input voltage. For the short-channel layout, two-dimensional scans of the complementary PMOS and NMOS input transistors were conducted with a resolution of 200 nm in the x-dimension and 700 nm in the y-dimension. For the long-channel layout, 400 x 1200 nm and 300 x 1000 nm scans were performed for the complementary PMOS and NMOS input transistors, respectively. The scans were performed at three different laser energies of 2.3 nJ, 3.1 nJ, and 5.1 nJ. One-dimensional scans were also performed at six different laser energies ranging from 1.7 to 5.1 nJ. The two primary error metrics used in this work were maximum voltage perturbation and settling time, where settling time was defined as the time the output voltage exceeded a given threshold voltage until it settled back within that threshold and did not exceed it again.

A 5.1 nJ laser energy error map comparing the maximum perturbations of the unhardened and hardened short-channel PMOS input transistors is shown in Fig. IV-6 (a) and (b), respectively. The device layout arrays in Fig. IV-6 consists of four rows of four 8.5 μm width x 0.5 μm length devices interleaved as shown in Fig. IV-5. This set of sixteen interleaved devices is surrounded by dummy transistors in order to minimize edge effects and improve matching.

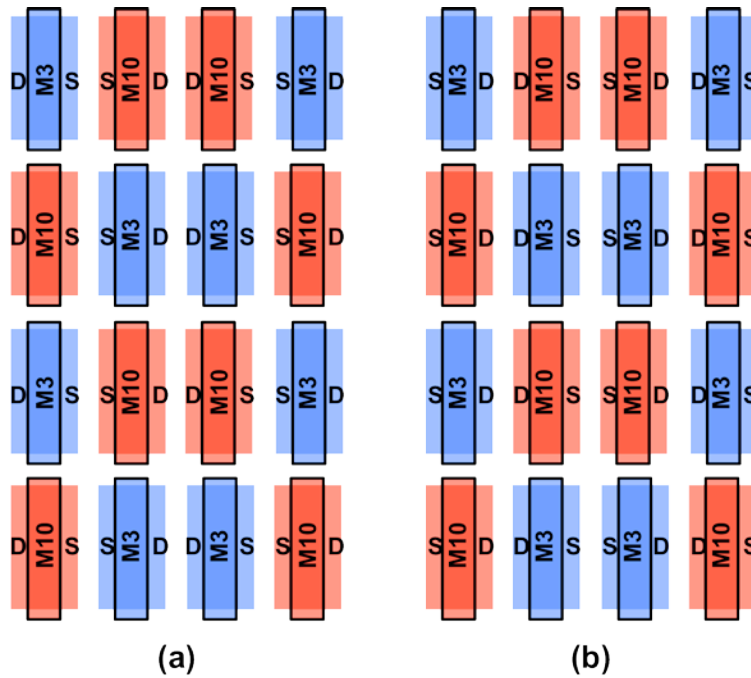


Fig. IV-5 Standard common-centroid layout (a) versus a DCC layout (b) of the PMOS input stage devices (M3 and M10) shown in Fig IV-1.

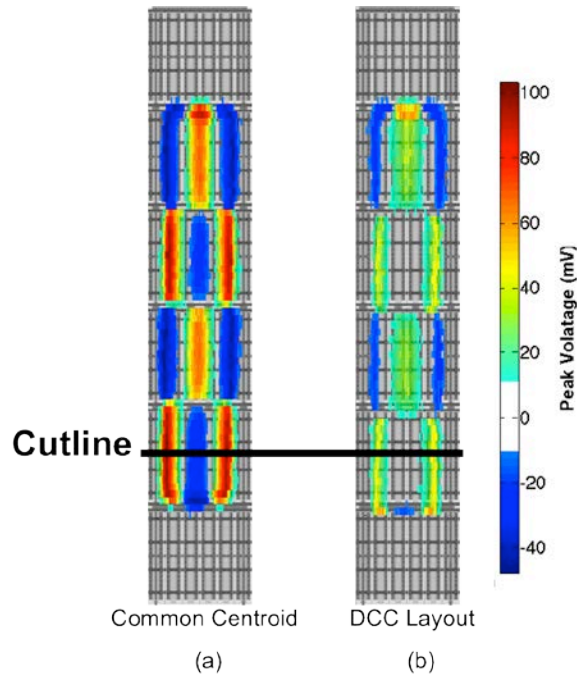


Fig. IV-6 Error map of the maximum perturbation following 5.1 nJ laser strikes to the PMOS input transistors M10 and M3 (shown in Fig. IV-1) of the short channel design without (a) and with (b) DCC hardening. The device pattern is identical to Fig. IV-5, the cutline is used in Fig. IV-8 [52]

This depiction shows that the DCC layout (Fig. IV-6 (b)) significantly reduced voltage perturbations, as noted by the reduction of sensitive area and the lighter colors shown on the sensitive regions [52]. A more quantitative look at the extent of the voltage reduction will be discussed in subsequent paragraphs. The positive-going transients tended to dominate the response of strikes on the short-channel PMOS input devices. Fig. IV-7 shows that negative-going transients tended to dominate the response of the short-channel NMOS input transistors, but an overall reduction in maximum perturbation was still present. The NMOS input stage devices, M4 and M9 from Fig. III-11, are laid out in four rows of four 2.25 μm width x 0.5 μm length devices interleaved in the same pattern as Fig. IV-5 [52]. Dummy transistors used to improve matching also surround these sixteen devices.

Plotting a one-dimensional cut of the data along the cutline in Fig. IV-6 gives a more qualitative look at the improvement a DCC layout makes in the SE hardness of a differential pair. Fig. IV-8 shows this as the maximum voltage perturbation versus horizontal distance for that one-dimensional cut, plotted for several different laser energies. Fig. IV-8 shows that (a) the unhardened design and (b) the DCC-hardened design had increases in maximum perturbation as the laser energy increased from 1.7 to 2.7 nJ. However, at a 3.4 nJ laser energy the maximum perturbation of (a) increased while the perturbation of (b) actually decreased to a level similar to the 1.7 nJ tests. Similar behavior was observed at the highest tested laser energy of 5.1 nJ, where maximum perturbations in (b) were still lower than the 2.7 nJ tests. This trend indicates that the DCC layout technique becomes more effective at higher deposited charge levels, which can be equated to higher LET (or effective LET) single-event strikes. This

observation strongly suggests that DCC layout hardening will be more effective for angled strikes or smaller technology nodes [52].

In fig. IV-8 there appears to be a positive shift in the voltage curves at higher tested laser energies. This is because the starting point for these scans was determined using the lowest tested laser energy. At higher laser energies the deposited charge was collected at greater distances from the active material, causing transients to occur at wider locations in the scan. These are not positive shifts in the curves. They are incomplete curves, because the scans were not wide enough at higher tested energies. This problem of a widening collection range is much more pronounced for the baseline design because as Fig. IV-5 shows the baseline design has isolated device drains on the outside of the scanned row, while the DCC layout does not.

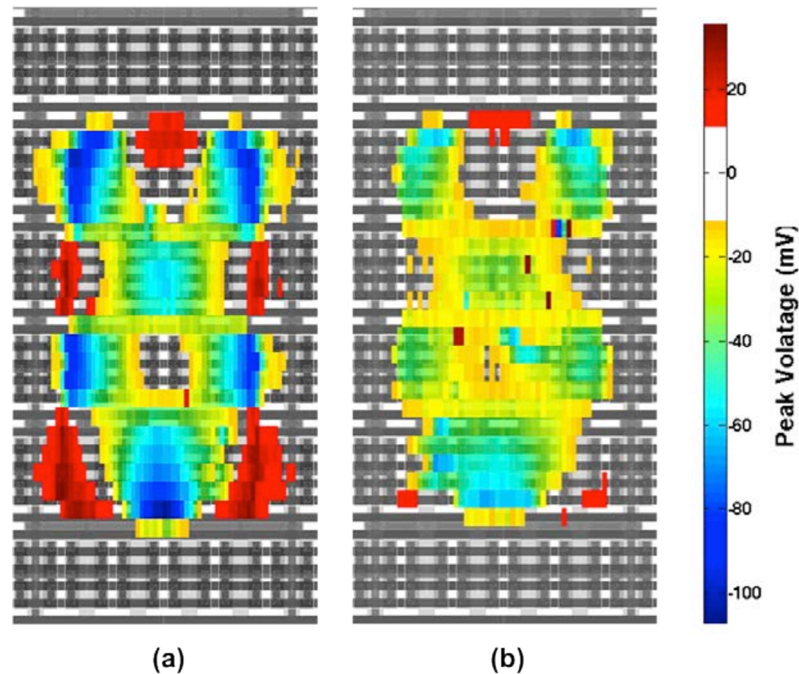


Fig. IV-7 Error map of the maximum perturbation following 5.1 nJ laser strikes to the NMOS input transistors (M4 and M9 in Fig. IV-1) of the short channel design without (a) and with (b) DCC hardening [52].

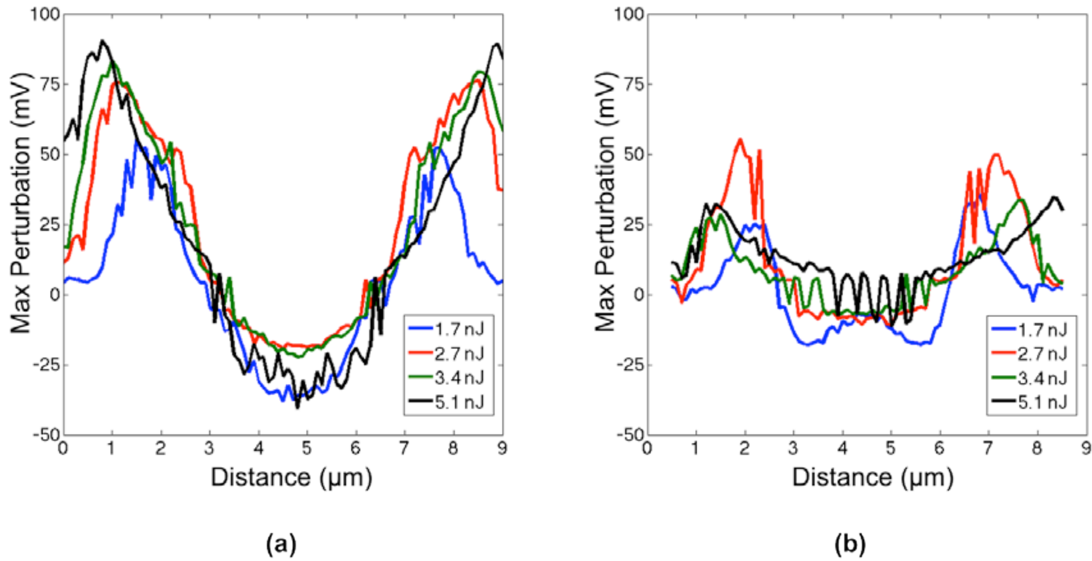


Fig. IV-8 One-dimensional cut across the error map from Fig. IV-6 plotted for various laser energies (a) common centroid layout and (b) DCC layout [52].

Fig. IV-9 is a scatter plot of maximum perturbation versus settling time comparing the entire differential input stage (PMOS and NMOS) of the hardened and unhardened short-channel designs. For this plot, laser strikes with energies of 3.1 nJ were made over all locations in the input pairs. In order to evaluate performance error metrics had to be established, as discussed in the previous chapter. In this case, settling time was defined as the time during which the output exceeded 18 mV. The 18 mV threshold was chosen to correspond to ½ LSB for a 5-bit ADC. Assuming this ADC operates at 2.5 MHz, all the points in the left-hand dotted box represent possible errors, depending on when the strike occurred in the clock cycle. All the points in the right-hand dashed box are definite errors regardless of time dependence, and may even cause multiple errors. Each point in the "definite error" box corresponds to a specific area from the laser scan grid. The full set of points can therefore be summed and correlated to a total sensitive area for each design. Fig. IV-10 is a plot of this sensitive area versus laser

energy squared, where the square of the laser energy is directly proportional to deposited charge. The DCC layout showed zero sensitive area at 5.29 nJ^2, while the common-centroid layout had a sensitive area over 30 μm^2. An effective reduction in sensitive area of more than one order of magnitude was observed for all three tested laser energies.

The error bars for this experiment, as well as all subsequent TPA experimental results are determined using counting statistics, where the error is ± √ (count). Count is the number of transients that exceed a given threshold. Each one of these counted transients is the average of multiple transients (16 for this experiment). This gives us another source of error. The total error for the experiment is the root of sum of the two separate counts squared.

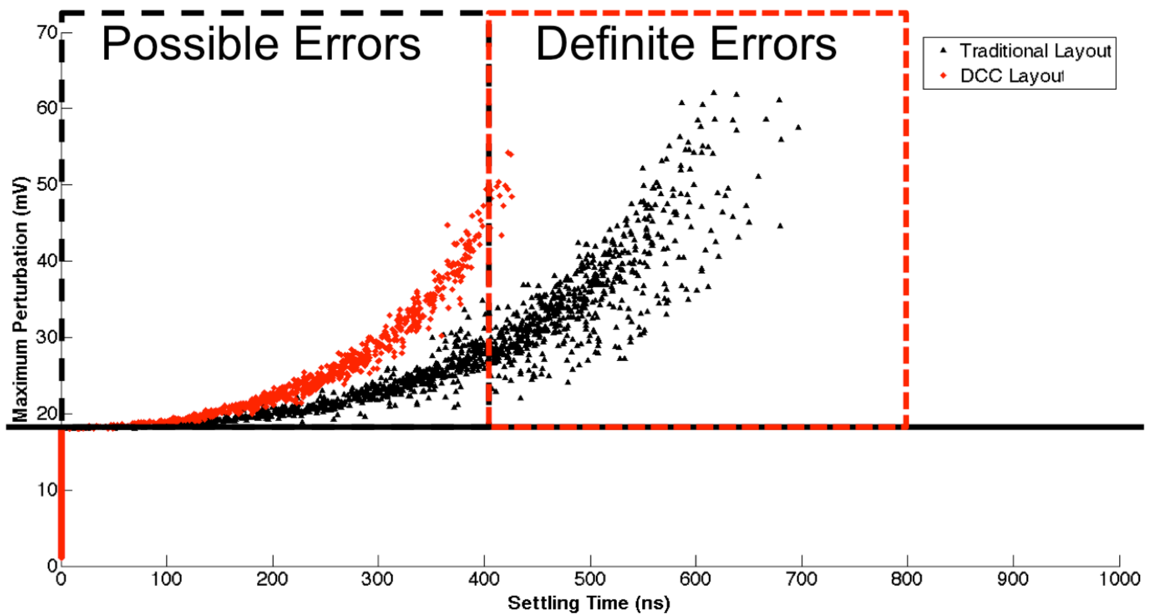


Fig. IV-9 Plot of the maximum perturbation vs. settling time over the entire input stage (PMOS and NMOS) of the short channel design. Error criteria is based off a 5 bit ADC operating at 2.5 MHz [52]

As previously mentioned, long-channel input transistors (with gate lengths > 1 μm) are often used in analog and mixed-signal circuits to improve matching and minimize V_{OS}. Consequently, the spacing between non-adjacent transistors may be much larger compared to transistors with minimum gate lengths, reducing the amount of charge sharing between transistors.

Fig. IV-11 is an error map comparing maximum perturbation between (a) unhardened and (b) DCC-hardened layouts of long-channel (2 μm) PMOS input pairs for a 5.1 nJ laser energy. These devices are laid out in eight rows of eight 8.5 μm width x 2 μm length unit cell devices interleaved in a similar fashion as the short-channel devices (Fig. IV-5). Fig. IV-11 shows that the improved hardening observed with the short-channel design is still significant even for the long-channel design. However, the maximum errors are somewhat larger for the long-channel devices. This is counter-

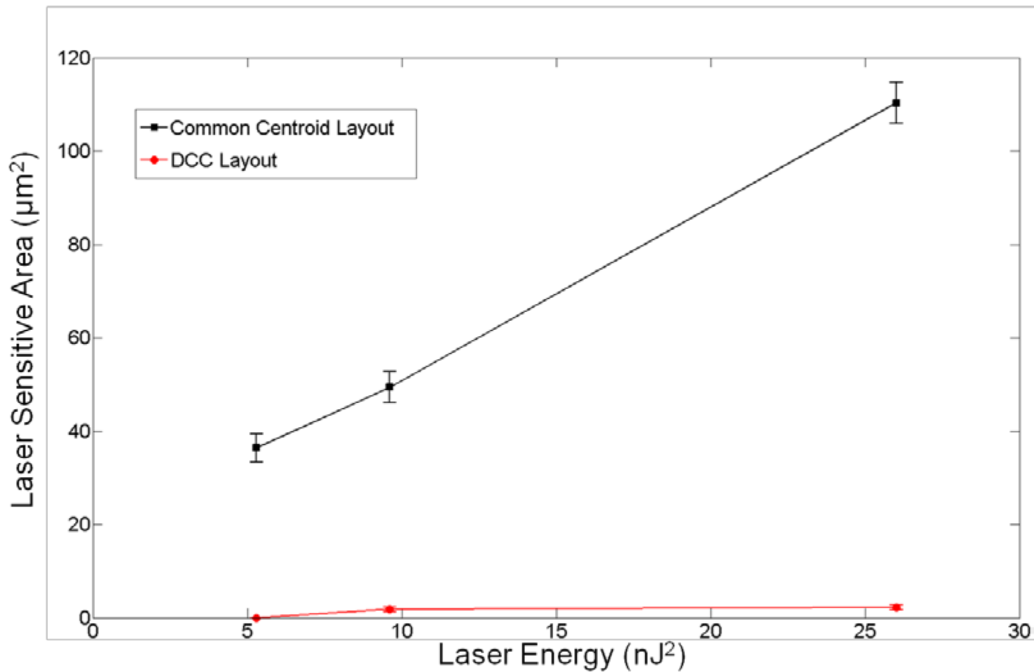


Fig. IV-10 Sensitive area vs. laser energy squared over the entire differential input stage (NMOS and PMOS) of the short channel design [52].

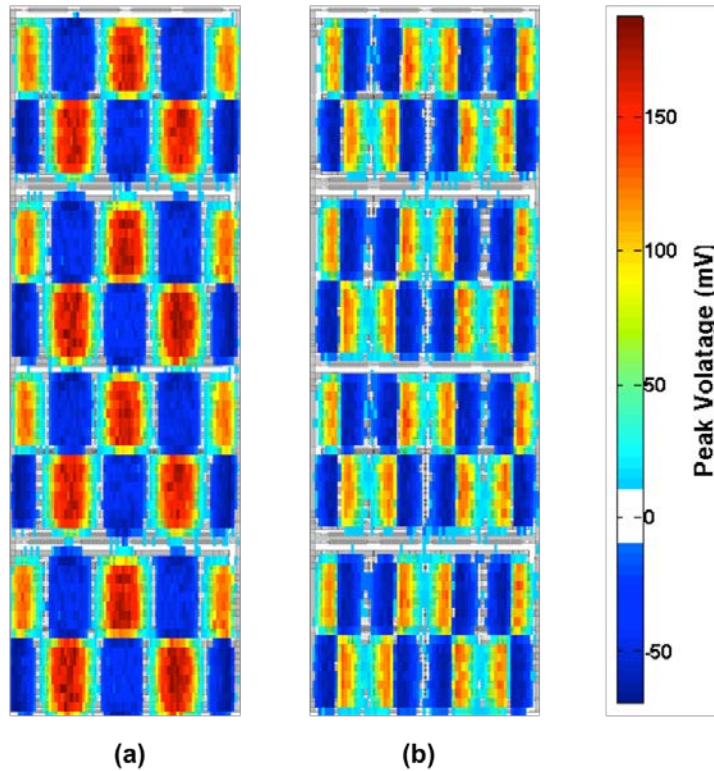


Fig. IV-11 Error map of the maximum perturbation seen follow 5.1 nJ laser strikes to the PMOS input stage of the long channel design without (a) and with (b) DCC hardening [52].

intuitive in the sense that larger transistors will create higher capacitive nodes, but the reduced amount of charge sharing due to the increased spacing makes the transistors more sensitive overall.

Fig. IV-12 is a scatter plot of maximum perturbation versus settling time for the full input stage of the long-channel designs, given a 2.3 nJ laser energy. Using the same error criterion established for the short-channel devices in Fig. IV-9, the sensitive area was plotted for the entire input stage (complementary PMOS and NMOS input pairs) of the hardened and unhardened designs versus laser energy squared. This plot in Fig. IV-13 shows a significant increase in sensitive area in the long-channel design compared to the short-channel design (Fig. 7). This increase is a result of greater physical device area and increased capacitance from the larger transistors [52], which extends the data points

from the “possible” error window in Fig. IV-9 to the “definite” error window as seen in Fig. IV-12. However, the hardened long-channel design still exhibited a 3X reduction in sensitive area at the lowest tested laser energy, and a 2X reduction in sensitive area at the highest energy, when compared to the unhardened layout. The conclusion is that DCC hardening is not as effective for long-channel layouts as it is for short-channel layouts, but still provides a significant (and worthwhile) improvement in single-event hardening.

Differential charge cancellation layout is clearly demonstrated to be an effective mitigation technique in this work for short and long channel single-ended output op amps. The lead up to this experimental verification described in the intro and in [4], demonstrated that this verification was in progress for a significant amount of time. It was also believed to be true prior to experimental proof. There is evidence of this in

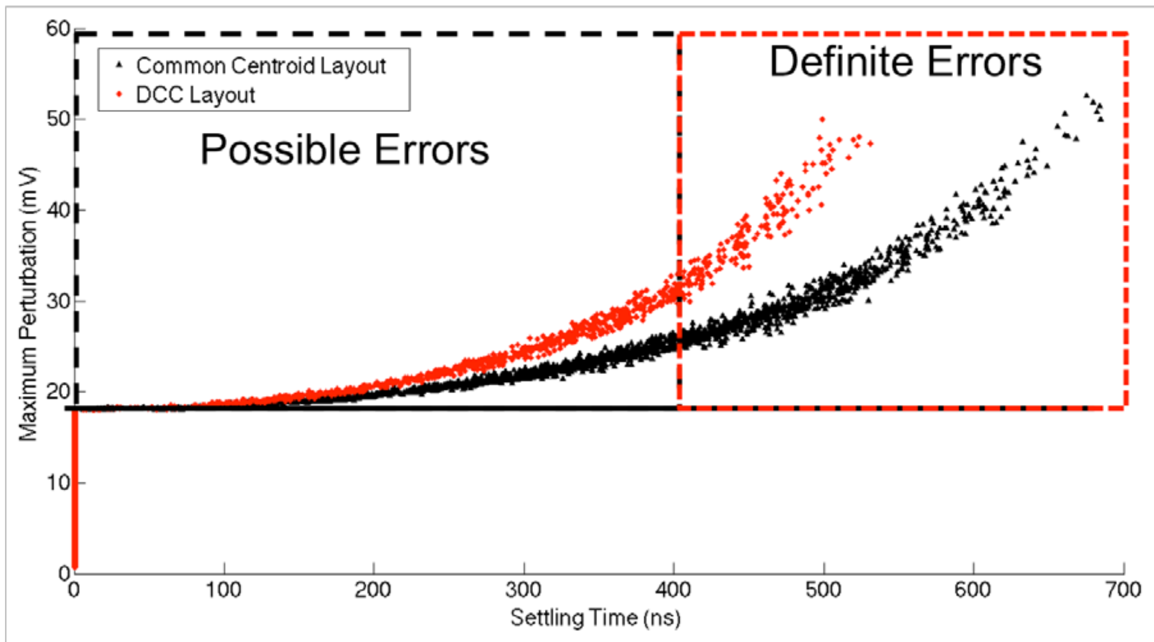


Fig. IV-12 Maximum perturbation vs. settling time over the entire differential input stage (PMOS and NMOS) of the long channel op amp design [52].

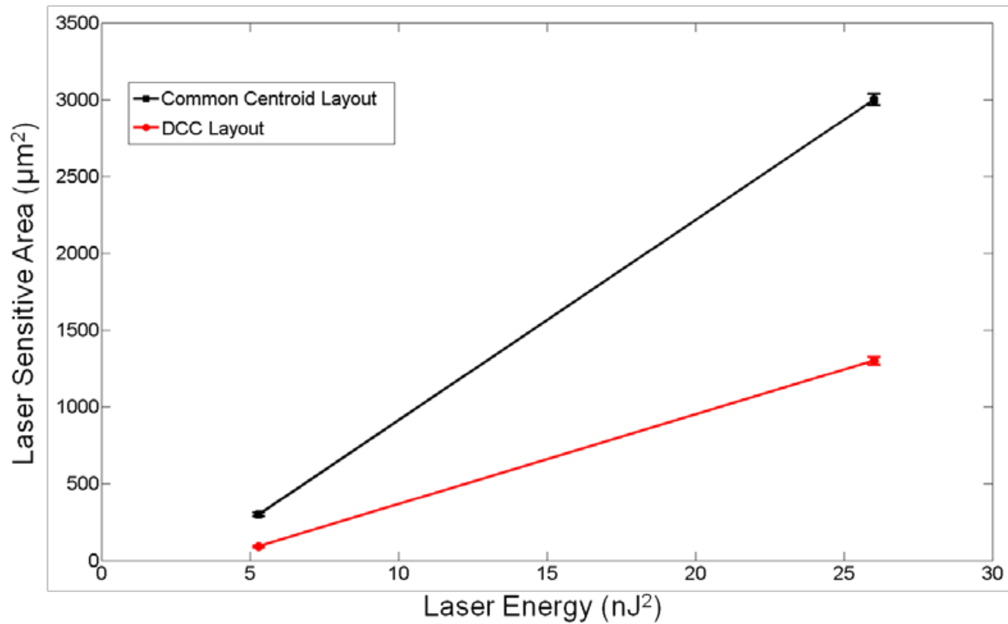


Fig. IV-13 Sensitive area vs. laser energy squared over the entire input stage of the long channel design [52].

industry, such as the Navy's GAP program incorporating DCC as a standard practice for all its differential circuits.

Should DCC be used for all differential circuit as a standard practice? In an attempt to experimentally answer this question, another TPA experiment was conducted on the fully differential op amp in Fig. III-13.The TPA tests were once again conducted at NRL. The op amp was in a closed loop configuration with a gain of 10 V/V using 100 kΩ and 1MΩ resistors in the feedback path. The testing was conducted with the op amp biased at mid-rail (900 mV). Two-dimensional scans of the complementary PMOS and NMOS input transistors as well as the cascode stage were conducted with a resolution of 200 nm in the x-dimension and 500 nm in the y-dimension, primarily. The two primary op amps compared were laid out differently, one with a traditional layout using common-centroid when appropriate and the other using DCC throughout the differential signal path. The experimental set up is shown in Fig. IV-14. The scans were performed at three

different laser energies, 1.1 nJ, 2.6 nJ, and 3.5 nJ. At each point of the scan the positive and negative polarity output terminal were captured and averaged for 25 separate strikes. The output was the recorded as the difference between the positive and negative polarity terminals (V_{out+}-V_{out-}).

Fig. IV-15 is a scatter plot of maximum perturbation versus settling time comparing entire differential input stage (PMOS and NMOS) of the hardened and unhardened circuits. For this plot, laser strikes with energies of 1.1 nJ were made over all locations in the input pairs. In order to evaluate performance, error metrics had to be established, as done with the previous op amp experiment. In this case, because there is not a specific target application settling time was defined as the time during which the output exceeded 10. As with the previous experiments each point on the plot corresponds to an area, in this case .1 μm^2. This area can be summed for different settling time thresholds to determine a total sensitive area for that given metric and then compared across designs.

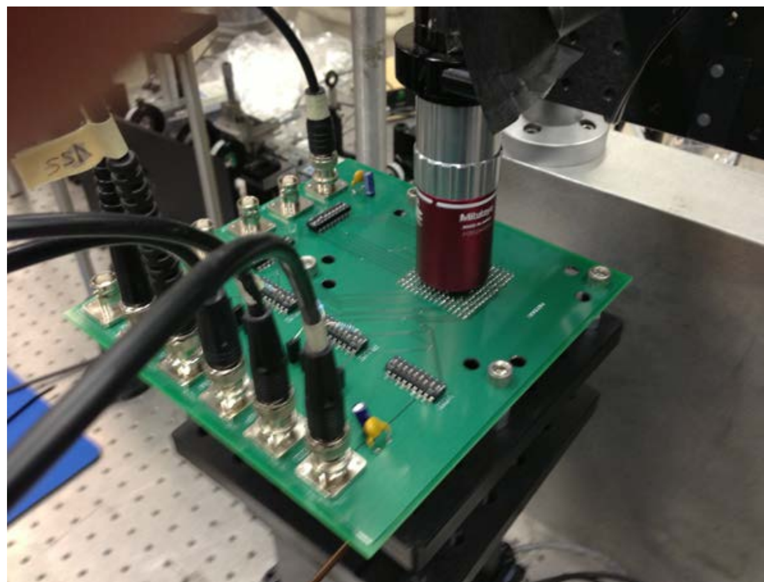


Fig. IV-14 Experimental set up used for testing the op amps at NRL

Fig. IV-16 is a plot of these sensitive areas for different settling time thresholds. In this figure three different settling times are used 800 ns (blue), 1000 ns (red), and 1200 ns (green). For each one of these settling times the baseline sensitive area is plotted as a solid line and the DCC hardened layout's sensitive area is shown as a dashed line for the three different laser energies tested. In all cases the DCC layout significantly lowers the sensitive area. For all three settling time metrics the greatest reduction in sensitive area occurs following strikes of the lowest laser energy, 1.1 nJ. There are two primary things causing the lowest energy to have the greatest reduction. The first and the reason having the smaller impact of the two, is increases charge sharing in the baseline design at higher laser energies. Increased charge sharing allows the baseline's common centroid layout to benefit from the differential charge cancellation as the DCC layout, but to a lesser degree.

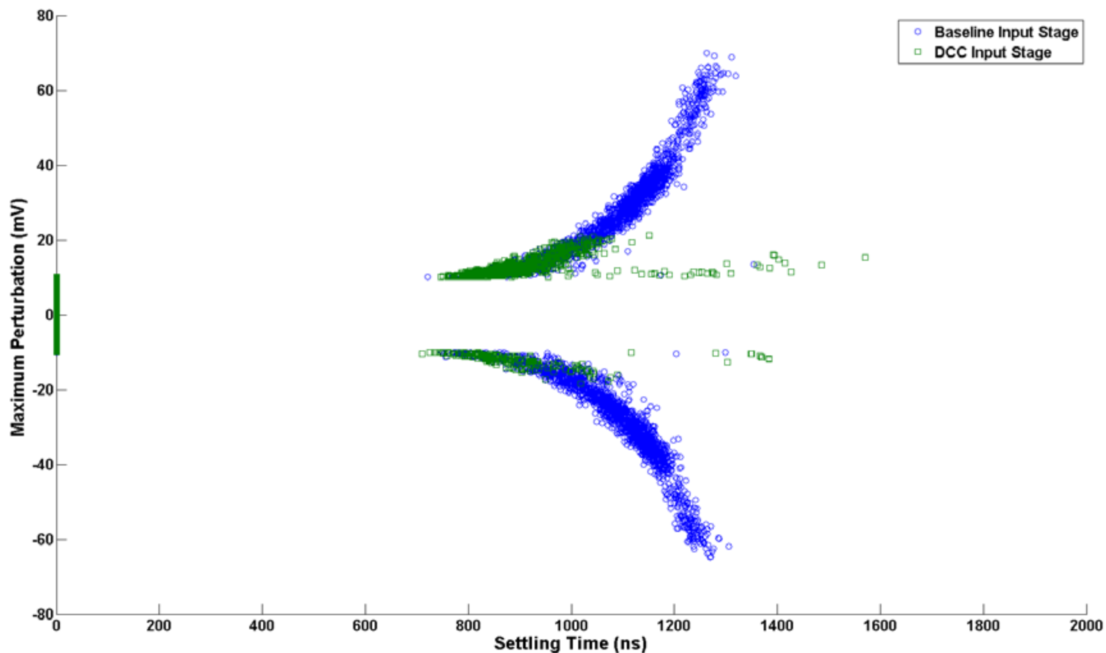


Fig. IV-15 Plot of the maximum perturbation vs. settling time over the entire input stage (PMOS and NMOS) of the baseline (blue circle) and DCC (green square) design

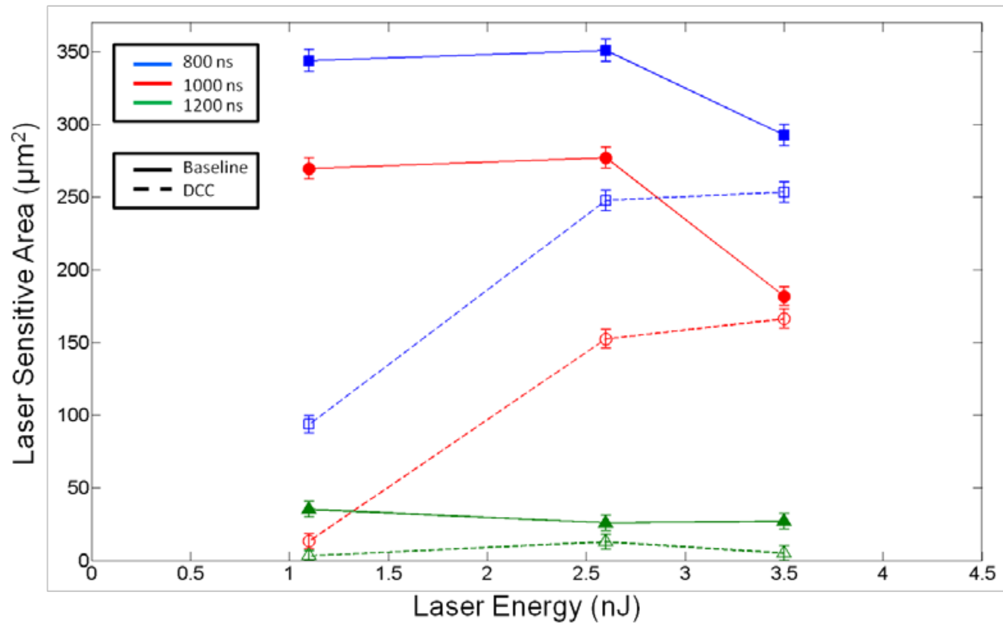


Fig. IV-16 Sensitive area of a fully differential op amp's input stage for various settling time thresholds comparing the baseline (solid) to a DCC layout (dashed)

The second and main reason you see a sharp decrease in sensitive areas for the baseline at higher laser energies is the difference in pulse shapes between the DCC and baseline layouts. The transients following strikes to the baseline input stage grow in magnitude at higher laser energies pretty significantly while maintaining a fairly constant settling time. The DCC layouts tend to not grow as much in magnitude with increasing laser energies, but do increase in settling time. This can be seen when comparing the scatter plot in Fig. IV-15 that uses 1.1 nJ laser energy data and Fig. IV-17 that uses 2.6 nJ laser data. Fig. IV-17 shows that the DCC layout op amp's input stage has very few transients with a magnitude greater the |40 mV| and the baseline op amp has a very significant amount of transients with magnitudes larger than that. The DCC layout produces transients that are smaller in magnitude, but tend to stay outside the 10 mV threshold a little longer, a pseudo dampening effect. This change in pulse shape can make the sensitive area plots misleading if not understood.

As expected, DCC is just as effective at hardening the input stage of a fully differential input stage of an op amp as it is for a single ended one, with a reduction in sensitive area between 73% (800 ns settling time and 1.1 nJ laser energy) and 9% (1000 ns settling time and 3.5 nJ laser energy). The obvious question and primary purpose of the experiment was to see if it was as effective for the rest of the op amp's differential signal path.

Fig. IV-18 is a scatter plot of the maximum perturbation vs. settling time for the entire cascode output stage of the op amp for a traditional baseline design and a design using a DCC layout following strikes with a laser energy of 1.1 nJ. A 10 mV threshold

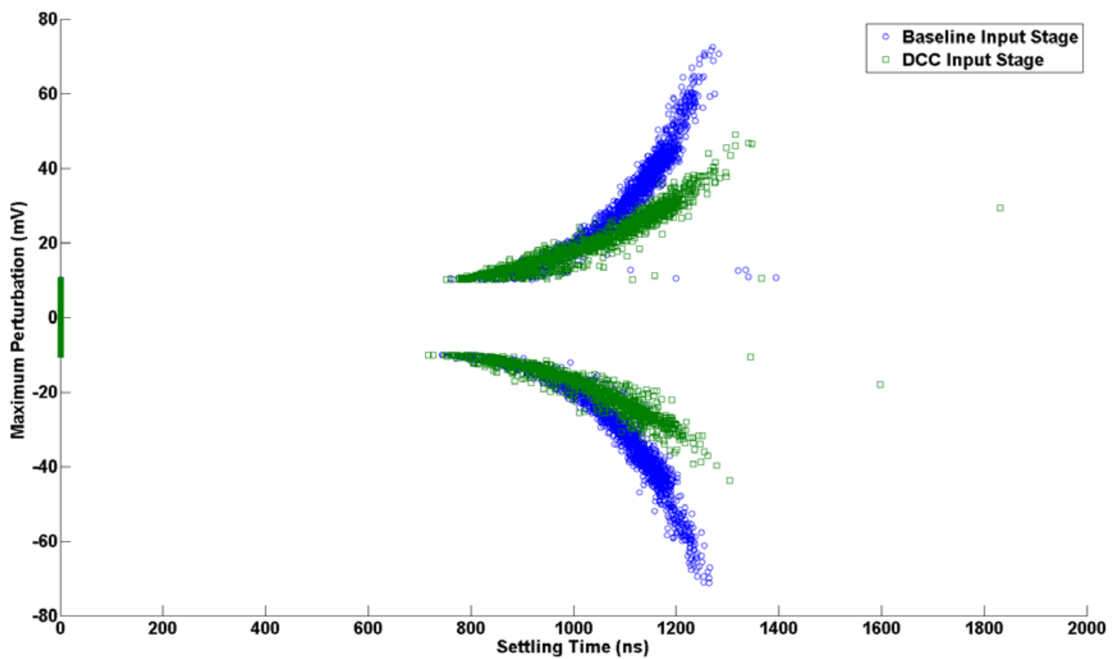


Fig. IV-17 Plot of the maximum perturbation vs. settling time over the entire input stage (PMOS and NMOS) of the baseline (blue circle) and DCC (green square) design for a laser energy of 2.6 nJ.

was used to determine settling time, much like for the input stage. The plot in Fig. IV-18 gives a strong indication that the DCC layout provides a significant reduction in perturbations to the cascode output stage. However, while this plot is informative it only gives a qualitative answer. In order to quantify the effectiveness of the DCC layout an error metric must be established. In this case, the same approach for the output stage is used for the input stage, a 10 mV threshold for three different settling times 800 ns, 1000 ns, and 1200 ns.

The sensitive areas determined using these metrics are shown in Fig. IV-19. In this figure the three different settling times 800 ns, 1000 ns, and 1200 ns are represented by the colors blue, red, and green respectively. The baseline and DCC layouts are then represented by the solid or dashed line respectively. This plot, much like the input stage

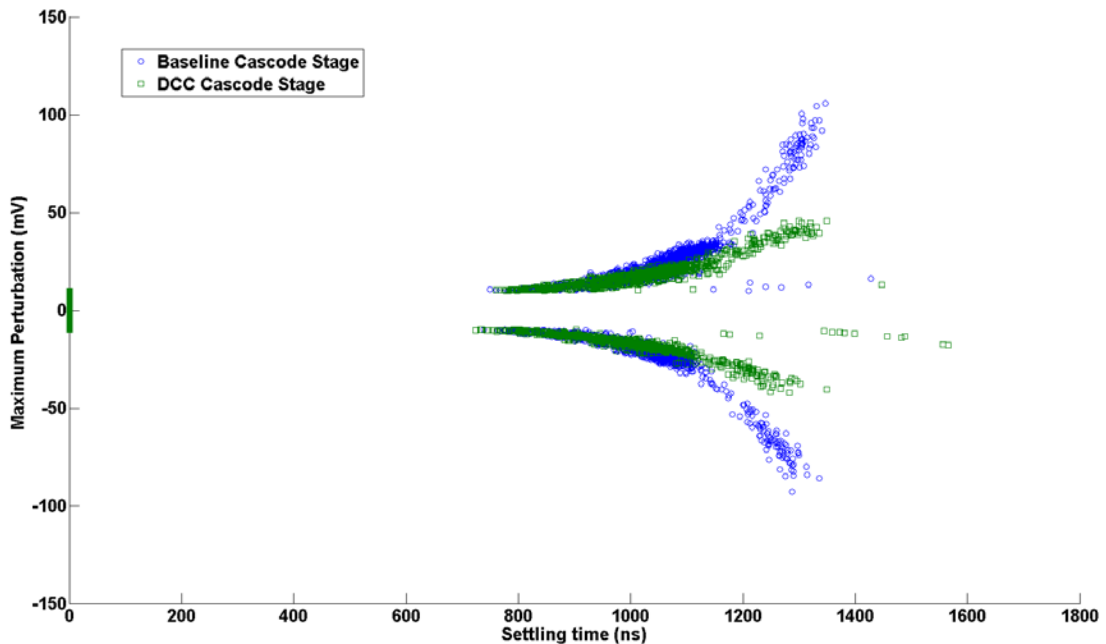


Fig. IV-18 Plot of the maximum perturbation vs. settling time over the entire cascode output stage (PMOS and NMOS) of the baseline (blue circle) and DCC (green square) design for a laser energy of 1.1nJ.

plot shows the DCC mitigates the effect of a SE for all three error criteria and at both tested laser energies (1.1 and 3.5 nJ).

The ranges in sensitive area reduction are from 42% (1000 ns settling time with laser energy 1.1 nJ) to 17% (1200 ns settling time with laser energy 3.5 nJ). DCC in the cascode output stage, much like the input stage appears to become less effective at higher laser energies when examining the sensitive area plots. An examination of the same scatter plot shown in Fig. IV-18 at the higher tested laser energy of 3.5 nJ, shows that this is primarily a function of the chosen metric and not completely representative of what is happening. Fig. IV -20 is the same plot at IV-18, but at the higher energy. It shows that while the baseline design's perturbations tend to grow in magnitude at higher energies, the DCC version's tend to elongate. This elongation makes a metric based on duration skew slightly and a designer with a system that is more vulnerable to maximum perturbation would need to keep this in mind.

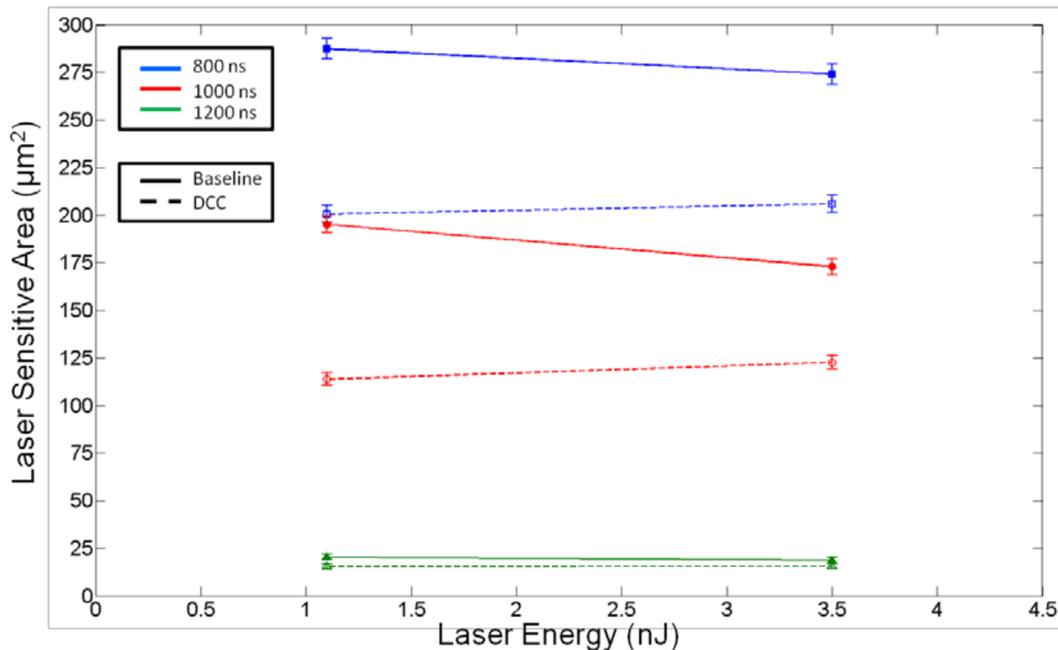


Fig. IV-19 Sensitive area of the fully differential op amp's cascode output stage for various settling time thresholds comparing the baseline (solid) to a DCC layout (dashed)

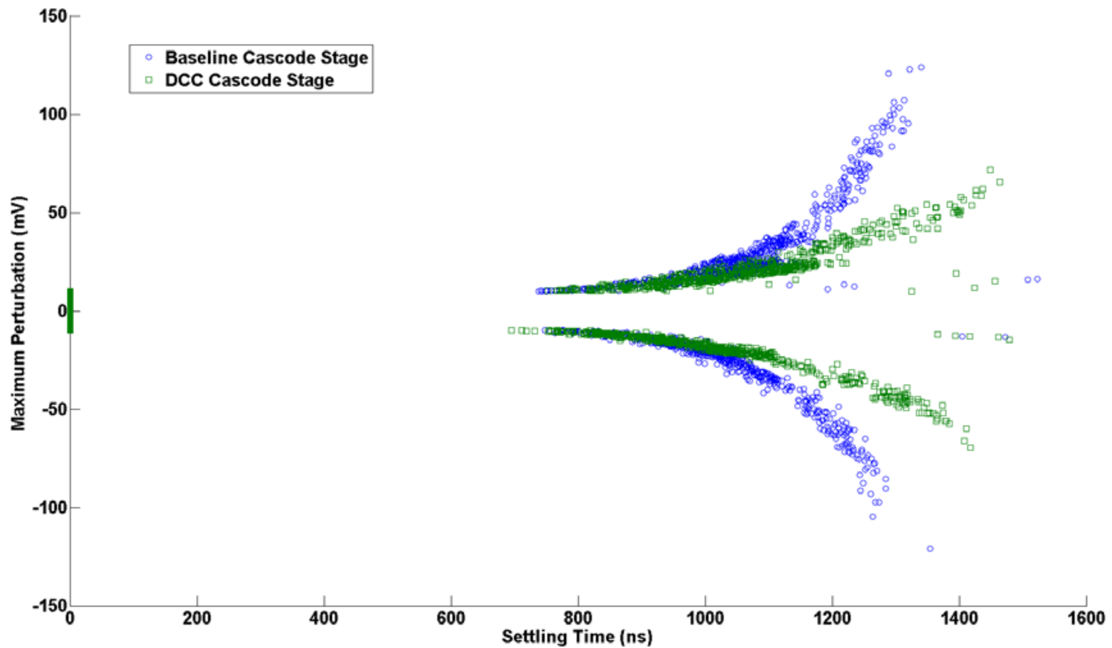


Fig. IV-20 Plot of the maximum perturbation vs. settling time over the entire cascode output stage (PMOS and NMOS) of the baseline (blue circle) and DCC (green square) design for a laser energy of 3.5nJ.

The SE mitigation in the cascode stage of the op amp from a DCC layout, while significant is not quite as strong as the input stage's mitigation. A major reason for this is the difference in the CMRR of the two stages. The CMRR of the input stage (and the entire op amp) is 140 dB. The CMRR of the cascode output stage on the other hand is 93 dB. A CMRR of 93 dB is strong, but a 47 dB difference between the two stages is also enough to make a significant difference in the results.

This dissertation presents the first experimental evidence of a circuit hardened via a DCC layout. However, this experimental verification might not be the most significant impact. The research in this section is also the first to measure and report the circuit ramifications of the layout change, as well as present evidence for increased benefit as technology continues to scale further below 100 nm. The works previous to this work on DCC all cite a chance of increased mismatch and offset as drawbacks of DCC. This

research built more than twenty op amps in two different technologies and found that this was not the case. Op amps with a DCC layout in every case had a measured offset that was the same or in some cases even better than the traditional common-centroid counterparts. A lack of an increase in offset demonstrates that there is no appreciable drawback off using a DCC layout in lieu of the traditional common-centroid.

Sensitive Node Active Charge Cancellation (SNACC)

The second hardening technique presented in this work that falls into the broader hardening via charge sharing category is sensitive node active charge cancellation (SNACC). SNACC and DCC both use charge sharing, but they do so in fundamentally different ways. The SNACC concept (depicted in Fig. IV-21) utilizes charge sharing to detect unwanted current transients (I_{SET}) and quickly remove the excess carriers through current compensation (I_{SNACC}). SNACC uses a DCC layout to deliberately enhance charge sharing and enable a device to serves as a current (charge) detector. It then uses a balanced current mirror topology to remove this current, mitigating the transient effects of SE strikes on the sensitive node. The balanced current mirror topology can be added to the existing circuitry or in special cases already exists inside the circuit's architecture.

The concept of using specialized circuitry to mitigate voltage transients is not new. For example, active decoupling circuits have been used in analog and mixed-signal designs to mitigate crosstalk noise [53-55]. SNACC is similar to these techniques in its basic concept, but is far better suited for single-event mitigation. Active decoupling circuits are typically built around operational amplifiers, resulting in increased quiescent power consumption, increased uncompensated sensitive area, and transient response

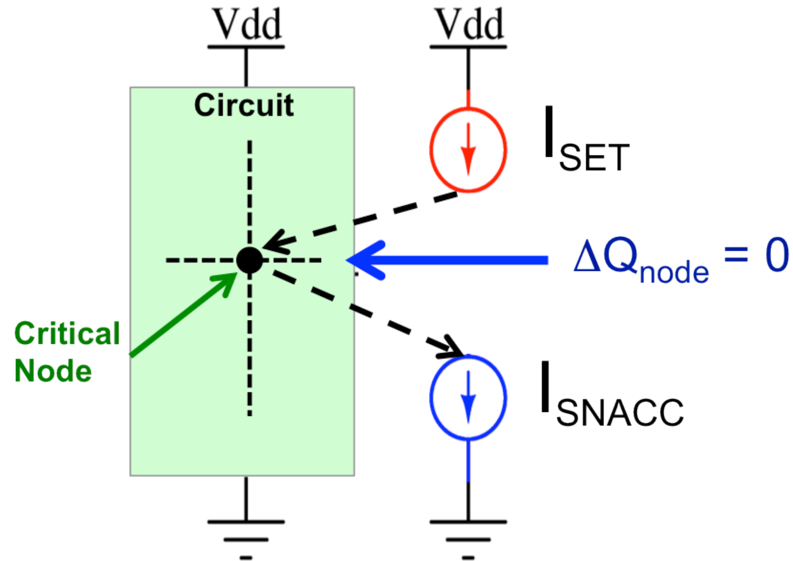


Fig. IV-21 Depiction of SNACC hardening concept, unwanted charge (I_{SET}) is detected and removed via I_{SNACC}

times limited by the frequency response of the feedback amplifier. On the other hand, a SNACC circuit has negligible quiescent power consumption with internally self-compensated sensitive areas, and can respond very quickly to a single-event strike.

The concept of a SNACC circuit has evolved since its first introduction to the community in 2010 [56]. Originally, SNACC was presented as a specific design requiring the addition of six transistors, two of which were twice the size of the device on the protected node. Later work showed that the additional devices could be optimized minimizing their associated area penalty [57]. Adding two more additional devices also allowed this technique to protect multiple sensitive nodes, which was coined multi-node SNACC or M-SNACC [57]. Finally, the SNACC concept's scope was extended even further, demonstrating that it can be applied without adding any devices. This special case of SNACC hardening uses a circuit's base design, but alters the layout to leverage

charge sharing creating the active charge cancellation that is indicative of SNACC hardening [58].

Fig. IV-22 is the original "6 transistor" version of SNACC added to the bias circuit of the 180 nm op amp from Fig. III-11. A preliminary simulation based single-event nodal analysis of the bias circuit shows sensitivity in every node in the circuit. However, the node labeled "Vnp", containing the drains of M28 and M29, is the most sensitive to SE strikes. These two sensitive junctions make this node a prime candidate for the original SNACC hardening technique. Understanding this technique is best accomplished via an example. A SE voltage transient can occur if transistor M27/M28 sources (or M29/M30 sinks) current from a SE strike. In this example only M28 and M29 are of primary concern because they are the most vulnerable and share a node. Following a SE strike on M28 or M29, if device S4 or S3 also collect charge, an equal current will ideally be sourced or sunk through the current mirror of S5 and S6 (or S1 and S2), resulting in no net change at the output node, thus mitigating the transient. Every sensitive junction in the bias circuit is compensated in this manner, including the added SNACC devices. As an example, if an ionizing particle strikes S5 it will sink current creating a voltage transient, however it is laid out to encourage sharing with S3 therefore initiating ideally an equal current to be sourced via S2. Encouraging charge sharing to allow one device to act as a charge detector is critical to the use of SNACC. The DCC layout concept discussed in the previous section is the tool that makes this possible. It is important to note that the SNACC devices S3 and S4 are connected in a zero-bias

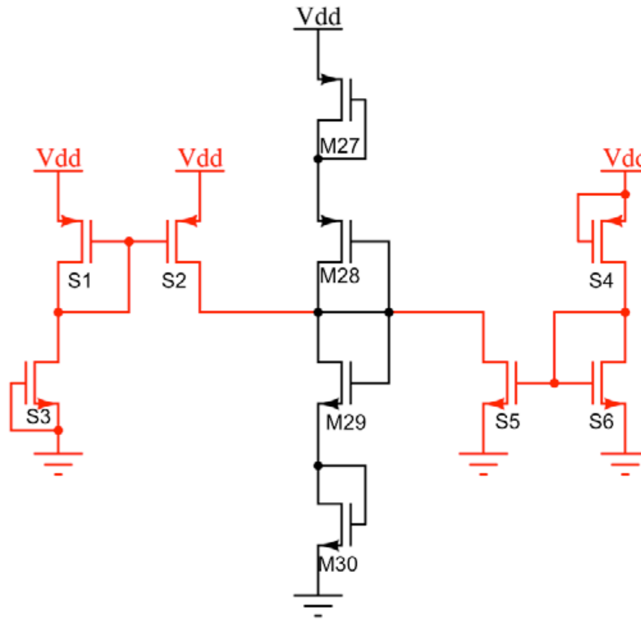


Fig. IV-22 The original six-transistor concept of SNACC applied to the bias circuit of the op amp in Fig. III-11

configuration. During normal operation all SNACC devices are biased "off" and therefore consume negligible additional power.

This particular SNACC application, depicted in Fig. IV-22 was fabricated as a part of the IBM 180 nm CMHV7SF test chip op amps and taken to NRL for TPA laser testing. The operational amplifiers with and without SNACC hardening of their bias circuits were tested in an inverting configuration with a gain of 10 V/V, using resistor values of 1 MΩ and 100 kΩ. The supply voltage VDD was set to 1.8 V, with a 0.9 V common-mode input voltage. Two-dimensional scans of the bias circuit were conducted with a resolution of 200 nm in the x-dimension and 500 nm in the y-dimension. The scans were performed at two different laser energies, 2.3 nJ and 3.1 nJ.

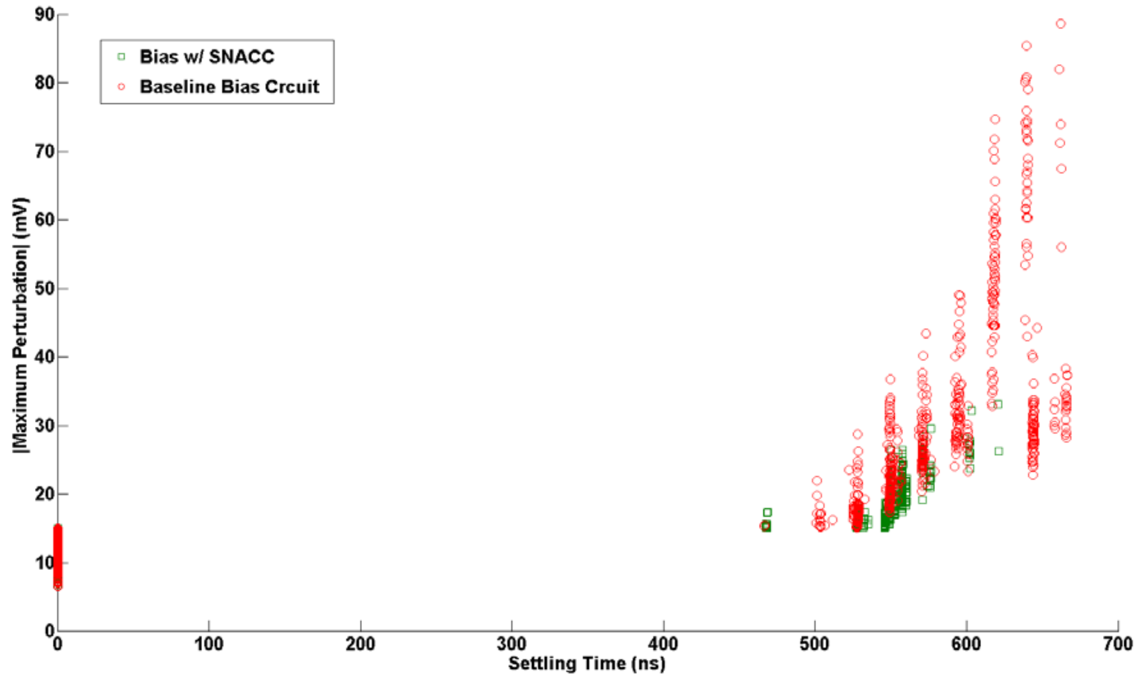


Fig. IV-23 Plot of the maximum perturbation vs. settling time over entire bias circuit (PMOS and NMOS) of the baseline (red circle) and SNACC hardened bias circuit (green square) design for a laser energy of 3.1nJ.

Fig. IV-23 is a scatter plot of the maximum perturbation vs. settling time for a laser energy of 3.1 nJ, obtained from these scans. Fig. IV-23 shows eight clear bands of common settling times. This is puzzling at first because the bias circuit is composed of only four devices. However, each one of these devices is broken into two unit cells connected in parallel leaving eight separate sensitive drain area. Other than the banding phenomenon the other important thing to pull from this figure is the overall smaller perturbations seen from the bias circuit hardened via SNACC. Qualitatively this is very significant evidence of the efficacy of SNACC. SNACC does increase the total area of the bias circuit though, so a more quantitative measure is needed.

In order to determine if the additional sensitive area added by SNACC is justified by increased SE immunity an error metric is needed. The op amp tested in this experiment is the same single-ended design used in the DCC input stages experiments

previously discussed. Therefore, it makes sense to use the same error metric of an 18 mV threshold corresponding to ½ LSB for a 5-bit ADC. Assuming this ADC operates at 2.5 MHz, all the points with setting times less than 400 ns represent possible errors, depending on when the strike occurred in the clock cycle. All the points with settling times grater than 400 ns are definite errors regardless of time dependence, and may even cause multiple errors. Each point in the "definite error" box corresponds to a specific area from the laser scan grid. We can sum these points to get a total sensitive area for various settling times allowing a more robust comparison than the previous use of only 400 ns. This more robust view is necessary because this experiment only has significant data for one laser energy. Two laser energies were tested instead of three due to lab availability time. Unfortunately, the first experiment at the lowest laser energy did not create large enough voltage transients to overcome the added capacitance of the testing set up and be statistically significant.

Fig. IV-24 is a plot of the sensitive area in μm^2 for various settling time thresholds comparing the baseline bias circuit with the bias circuit hardened via SNACC for the 3.1 nJ laser data previously discussed in Fig. IV-23. The SNACC hardening technique reduces the sensitive area for all settling time thresholds. The greatest reduction occurs with a threshold settling time of 600 ns with a reduction of sensitive area from 20.1 μm^2 to 1.1 μm^2. This corresponds to approximately a 96% reduction in sensitive area. The smallest reduction in sensitive area occurs at the 400 ns threshold used in the previous DCC comparisons. The reduction in sensitive area at this point is still very significant at approximately 10 %.

This data set provides significant evidence that SNACC is as effective as the previous simulation papers available in [57] advertised. However, because it is only at a single laser energy it is hard to call it absolutely conclusive. The primary concern with the 6-transistor implementation of the SNACC technique is the additional sensitive area, even though it too is protected via charge cancellation. In this case the physical area of the bias circuit more than doubled, adding a 12% increase in area to the op amp itself. Of that 12% increase in total area only 4% is active area.

A recent simulation study showed that this additional sensitive area could be reduced significantly by using some standard digital design layout tricks [59]. In this work the author was attempting to harden that voltage-summing block of a band gap reference circuit. This circuit along with the proposed added SNACC circuitry is shown in Fig. IV-25 [59]. In this circuit the source of dynamic-threshold MOS transistor

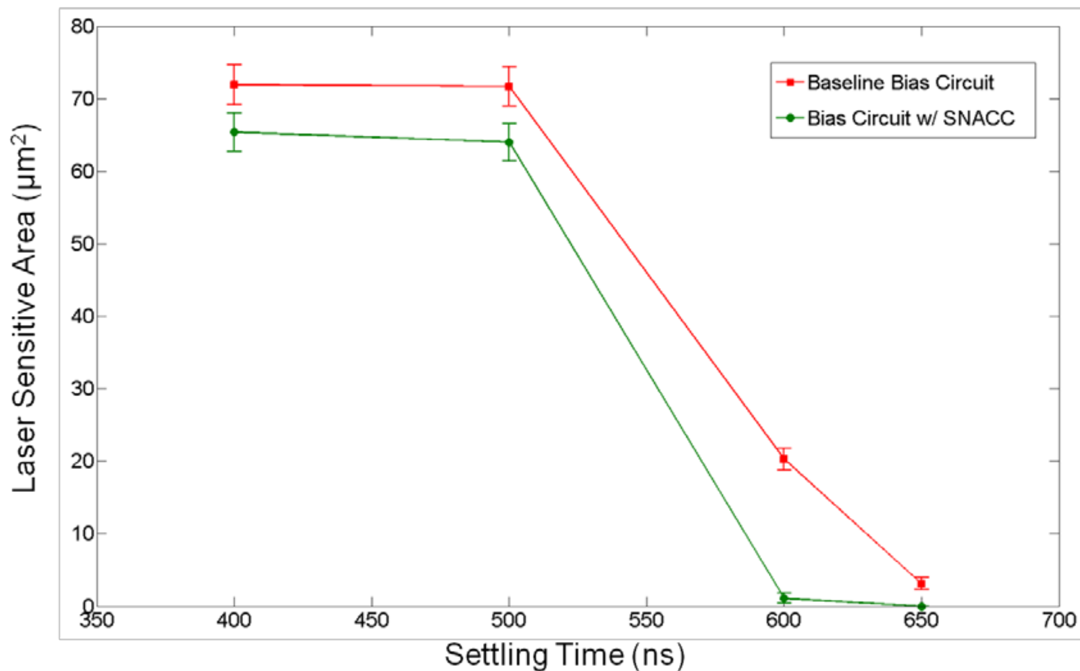


Fig. IV-24 Sensitive area of the baseline bias circuit and bias circuit hardened via SNACC for various setline time thresholds.

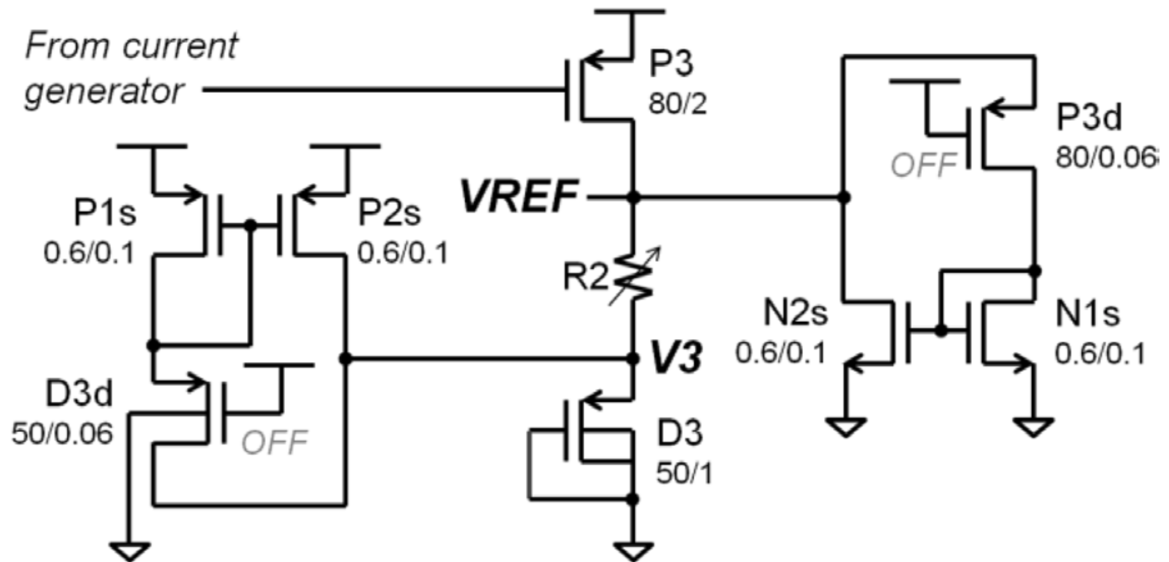


Fig. IV-25 Voltage summing circuit of a band gap reference with SNACC circuitry added, from [59]

(DTMOST) D3 is connected to V_{REF} through R2. The separation from V_{REF} by the resistor makes it less sensitive to SE strikes than V_{REF} node itself, but it still required protection. The protection for this node is provided by the dummy transistor D3d and its corresponding current mirror P1s / P2s, making half of the 6-transistor SNACC circuit. This protection works in the same manner as the previously described SNACC implementations. If D3 and D3d both collect charge following a SE strike, then P1s/P2s will mirror a current onto the protected node cancelling the SE induced current. The true novelty in this approach is the layout of D3d. The author merged the drains of D3d with the sources of D3 and biased the gate is D3d "off" as the schematic shows. This limited the separation between D3 and D3d to just the length of the dummy device channel. This move removes the STI between the two nodes, increasing the charge sharing further while also reducing the area penalty. It is important to note, in all modern technologies

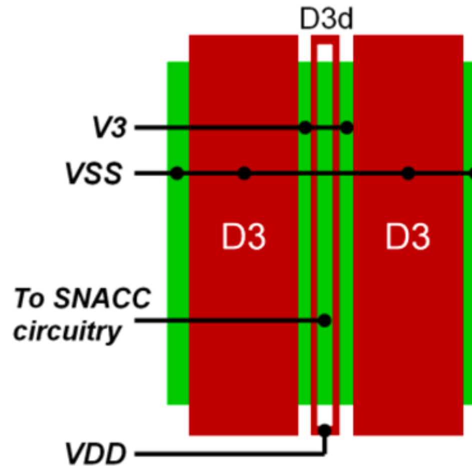


Fig. IV-26 Example layout of two D3 units cells with two D3d cells corresponding to the schematic in Fig. IV-31 [59]

design rules the minimum gate length is less than the active-to-active spacing requirements. This technique for decreasing the spacing between devices has been used in digital latch designs [60], but is novel in its application to SNACC. The author's figure demonstrating this layout technique is shown in Fig. IV-26 [59]. SNACC, as show in Fig. IV-25 using the above layout scheme increases the circuit's layout area by 5.2%.

The key benefits of this new layout technique are that charge sharing is increased making it more effective and the area penalty is reduced. The area penalty reduction was confirmed through layout and measurement. In order to confirm that the increased charge sharing is effective the author performed a simulation study. This simulation study also seeks to answer another important question about this version of the SNACC technique. Is there an optimal percentage of charge sharing to maximize the effectiveness of SNACC?

A simulation study of ion strikes on the circuit depicted in Fig. IV-25, where the ion deposits 200 fC of charge in the vicinity of P3 and P3d was performed. The percentage

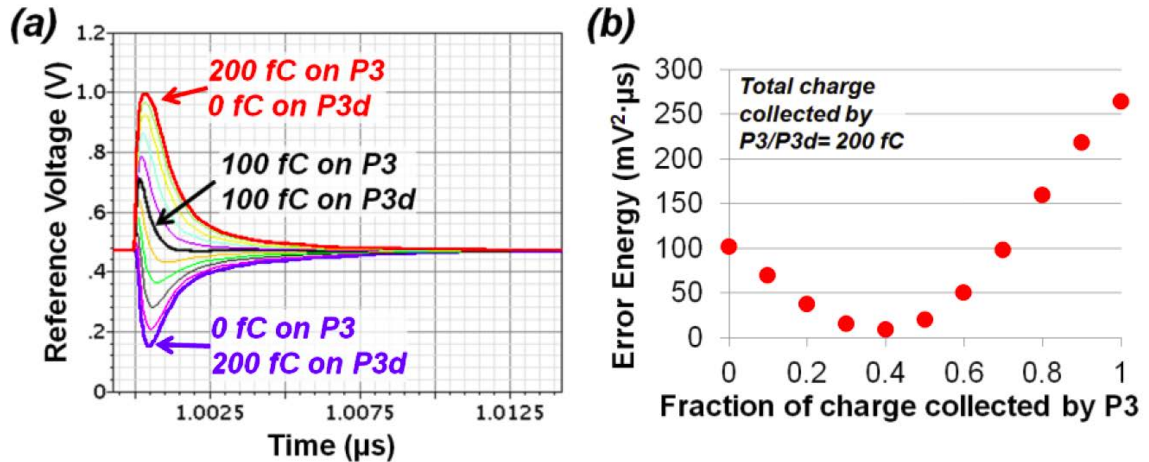


Fig. IV-27 Results of a simulation study on the circuit shown in IV-31, (a) the results ASETs and (b) the resulting error energy as a function of the fraction of charge collected by P3 [59]

of charge collected by each device was varied and the resulting ASETs on the VREF node were measured. Fig. IV-27 is a sample of these results with (a) containing the actual ASETS and (b) showing the error energy as a function of the fraction of charge collected by device P3 [59]. Error energy is a metric that captures both the duration and amplitude of an ASET in a single metric, although at the cost of specificity of both. The error energy is defined as integral of the square of the ASET with respect to time, yielding the units mV^2* µs. This figure shows that the largest transients, positive and negative going, occur when either P3 or P3d collect 100% of the charge respectively. However, there are multiple transients with P3 collecting the majority of the charge that are larger than when P3d collects all the charge. In terms of error energy the optimal point is where the charge collection split is 60-40 between P3d and P3, but anywhere in the 50-50 split is close.

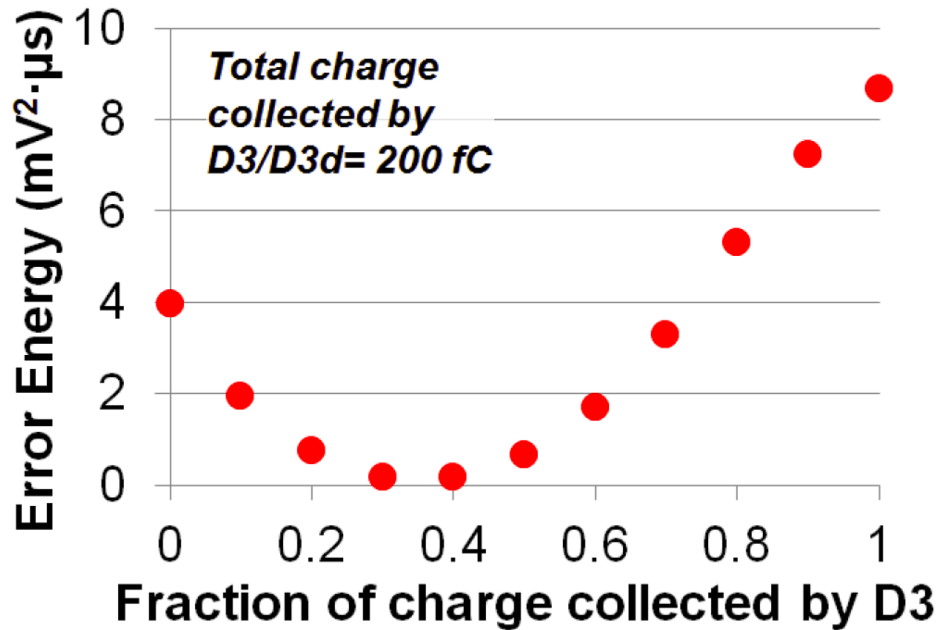


Fig. IV-28 Results of a simulation study on the circuit shown in IV-25, the resulting error energy as a function of the fraction of charge collected by D3 [59]

The author also performed a similar analysis on the other node, labeled V3 in Fig. IV-25 [59]. These results containing the error energy as a function of the fraction of charge collected by D3 are shown in Fig. IV-28. The simulations for strikes in the vicinity of D3 are consistent with P3, indicting the ideal case is when the SNACC device collects slightly more charge (60-40 or even 70-30). This is consistent with the original SNACC work that indicated SNACC was most effective for angled strikes that have a longer track length and therefore deposit more charge through and under the SNACC device [56,57]. Once again though, a 50-50 split is pretty advantageous and likely be the target design point. This layout technique does the best of any to this point in optimizing this sharing ratio.

Reducing the area penalty of SNACC and particularly reducing the added sensitive area are primary concerns with the additional device implementations

previously discussed. However, there are implementations of SNACC that do not require any added circuitry. This type of implementation of SNACC hardening can be used to harden the last block of the op amp shown in Fig. III-11, the cascode output stage. A DCC layout can be used in the stage to exploit the inherent current mirroring behavior to achieve SNACC hardening and SET mitigation [58]. The cascode stage of the op amp in Fig. III-11 is shown again in Fig. IV- 29 to aid in visualization of the SNACC hardening. This technique can best be understood through an example. If an ionizing particle strikes in the vicinity of the cascode stage and only M18 collects the deposited charge, then the SE current will discharge the compensation capacitor and the ASET will propagate to/through the op amp's buffer. However, if a layout can be used to force both M18 and M17 to collect charge, then the SE induced current will run through both M18 and M17.

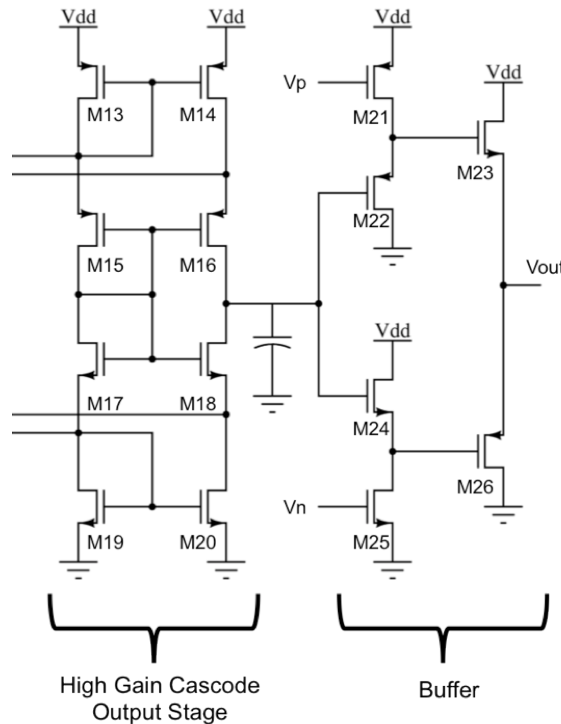


Fig. IV-29 The cascode output stage of the op amp from Fig. III-11, shown again to aid visualization of SNACC hardening

The current in M17 will force M15 to source more current, which is mirrored to M16. Therefore, M16 will also source this current onto the compensation capacitor and actively cancel the charge collected by M18, i.e. SNACC.

In this circuit SNACC hardening is achieved without adding any extra circuitry, it does however require a layout change. The cascode output stage of a single-ended op amp does not typically require a common centroid type layout to maximize matching. The application of SNACC to this circuit requires the use of a DCC layout to maximize charge sharing and therefore will create a small non-sensitive area penalty associated with device spacing.

To test this new application of SNACC, the op amp depicted in Fig. III-11 designed in a bulk 180 nm technology was taken to for TPA testing at NRL. Two-dimensional scans were performed for the cascode output stage of three different designs. At each x-y point in the scan, sixteen laser-induced transients were captured and averaged on an oscilloscope. The operational amplifiers were tested in an inverting configuration with a gain of 10 V/V, using resistor values of 1 MΩ and 100 kΩ. The supply voltage V_{DD} was set to 1.8 V, with a 0.9 V common-mode input voltage. The two-dimensional scans of the cascode output stage transistor were conducted with a resolution of 200 nm in the x-dimension and 500 nm in the y-dimension for the NMOS devices and 200 nm x 1μm for the PMOS devices. The scans were performed at three different laser energies, 2.3 nJ, 3.1 nJ, and 5.1 nJ

Representations of the three different layout designs of the cascode stage are depicted in Fig. IV-30 [58]. The layouts of the devices in the figure labeled N9 and N10 represent any of the four pairs of devices in the cascode stage, M13/M14, M15/M16,

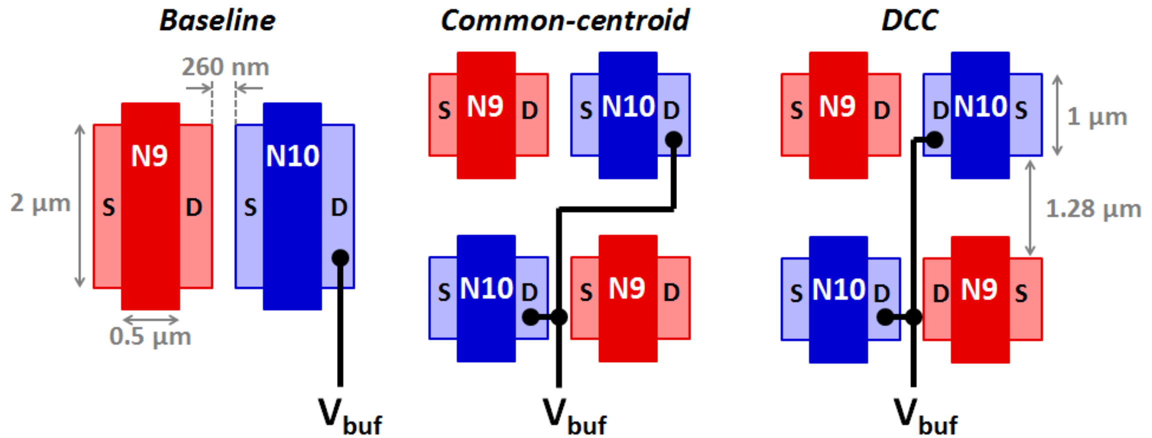


Fig. IV-30 Representations of the three tested layouts of the of the op amp shown in Fig. IV-1's cascode output stage [58]

M17/M18, or M19/M20. The layout labeled baseline is how a designer would typically layout the cascode stage of this circuit, because matching is not critical. The common-centroid layout in the center of the figure is used as an intermediate step, where more charge sharing may be present than the baseline layout. The final layout in the figure is labeled DCC, which will promote the SNACC hardening desired.

The three designs were analyzed using the same SE metrics of maximum perturbation and settling time used in previously discussed experiments. The target application for this op amp, used to establish an upset threshold was an ADC (same as with the input stage and bias circuit experiments) with a ± ½ LSB of 18 mV and a sample rate of 2.5 MS/s. Therefore a definite error is defined as a transient that has a magnitude greater than ± 18 mV and the settling time also exceeds 400 ns. These errors are independent of when the event occurred within the sample period. As with previous discussion, some of the events with settling times less than 400 ns could also produce errors depending on when they occur in the cycle. Fig. IV-31 contains settling time error maps corresponding to the three layout configurations in Fig. IV-30 following laser

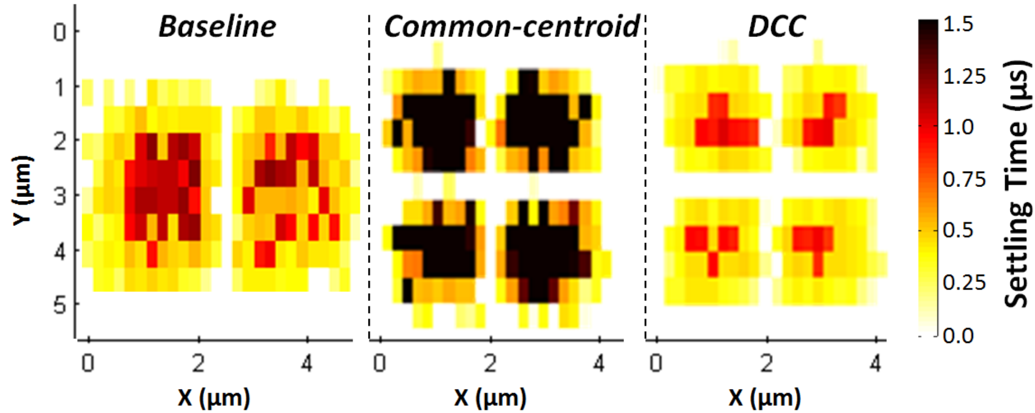


Fig. IV-31 Error maps of settling time of TPA induced SE transients for the three layout type shown in Fig. IV-36 [58]

strikes with a 3.1 nJ energy. The plots in Fig. IV-31 demonstrates the strike location dependence for devices M17 and M18. These devices are shown because the consistently proved to be the most sensitive in the cascode stack throughout the testing process.

These error maps clearly show that the transients with the longest settling time were generated in the baseline and common centroid layouts, as indicated by the black and dark red points. Fig. IV-32 gives a more quantitative view of the difference in the three layouts with a scatter plot of maximum perturbation versus the settling time following 2.3 nJ laser strikes. Fig. IV-32 allows an error metric to be applied, such as our 18 mV and 400 ns ADC error window. However, there are a few data points that get obscured. As an example there are 477 SETs generated in the baseline design that have a magnitude greater than 18 mV, while there are only 196 generated from the DCC layout. This corresponds to a 59% reduction in SETs larger than a ½ LSB. Looking at the maximum perturbations an 88% reduction in perturbations

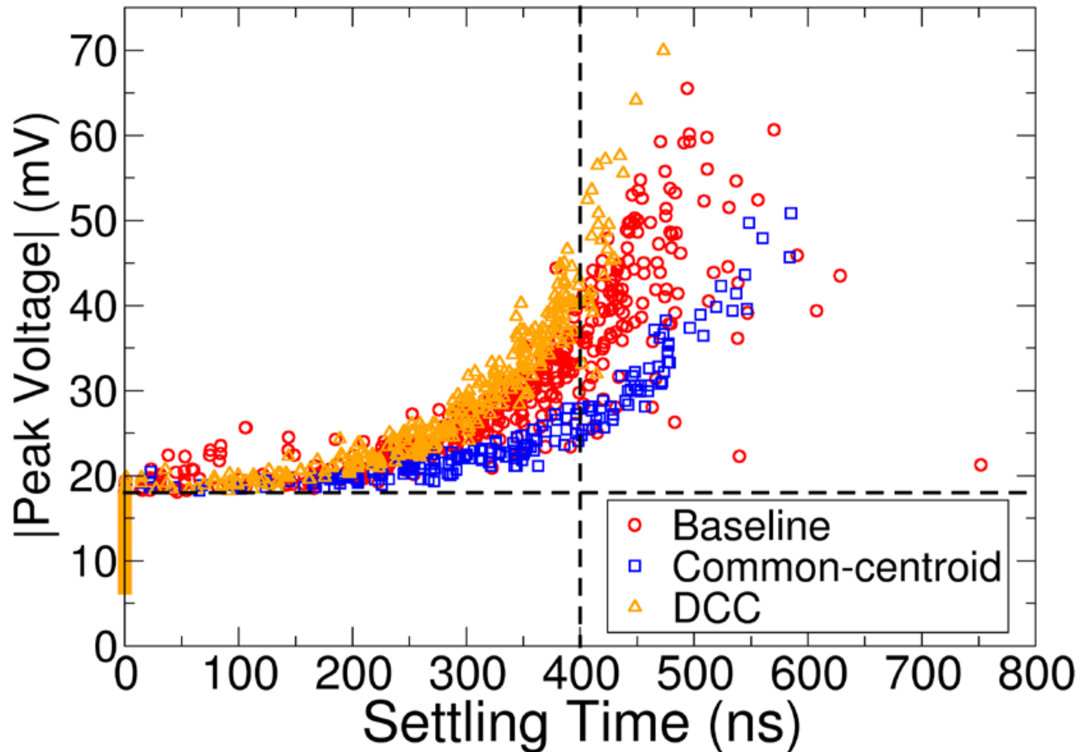


Fig. IV-32 Scatter plot of maximum perturbation vs. settling time for the entire cascode output stage of the op amp in Fig. IV-1 following laser strikes with 2.3 nJ energy[58]

exceeding 50 mV is achieved with a DCC layout reducing the total from 26 with the baseline layout to 3. Using the ADC error criteria and the known raster step size for the experiments a sensitive area can be determined from plots like IV-32. Anything above the horizontal and to the right of the vertical dashed lines in Fig. IV-32 is an error. Summing these points for each design and multiplying them by our raster X and Y step size yields the total sensitive areas for each design, shown in Figs. IV-33 and IV-34. The area grayed out in these plots is the point where the area is equivalent to a single data point. The single data point allows an easy measure of the maximum settling time for each of the three designs. In Fig. IV-33 these maximum points correspond to a settling time of 500 ns, 600ns, and 1.9 μs for the DCC, common centroid, and baseline layouts respectively. If these maximum settling times were used to determine the speed that the ADC could

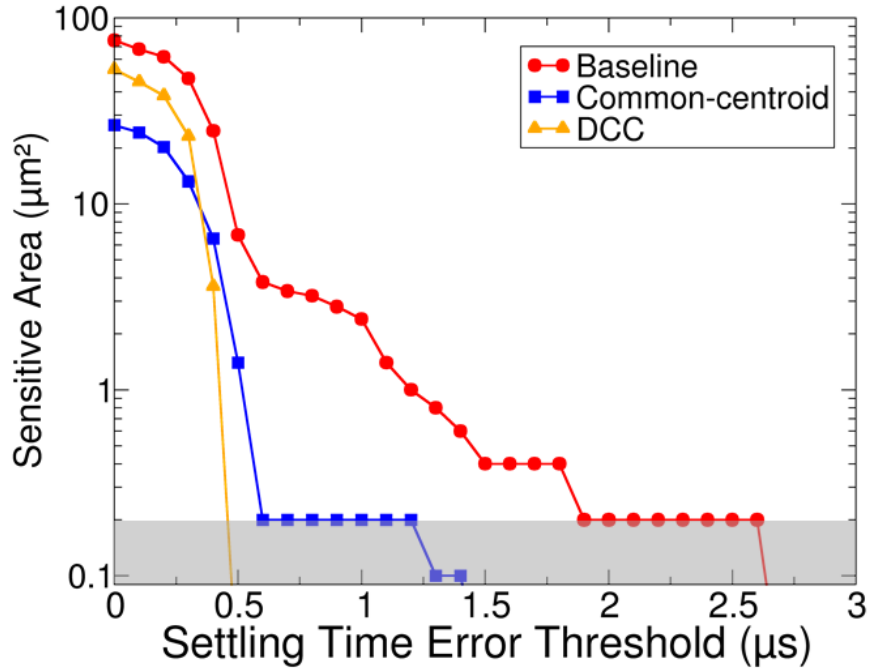


Fig. IV-33 Sensitive area of the three cascode output stage layouts shown in Fig. IV-37 as a function of settling time. The grayed out area corresponds to an area the size of a single data point. This data is for a laser energy of 2.3 nJ [58]

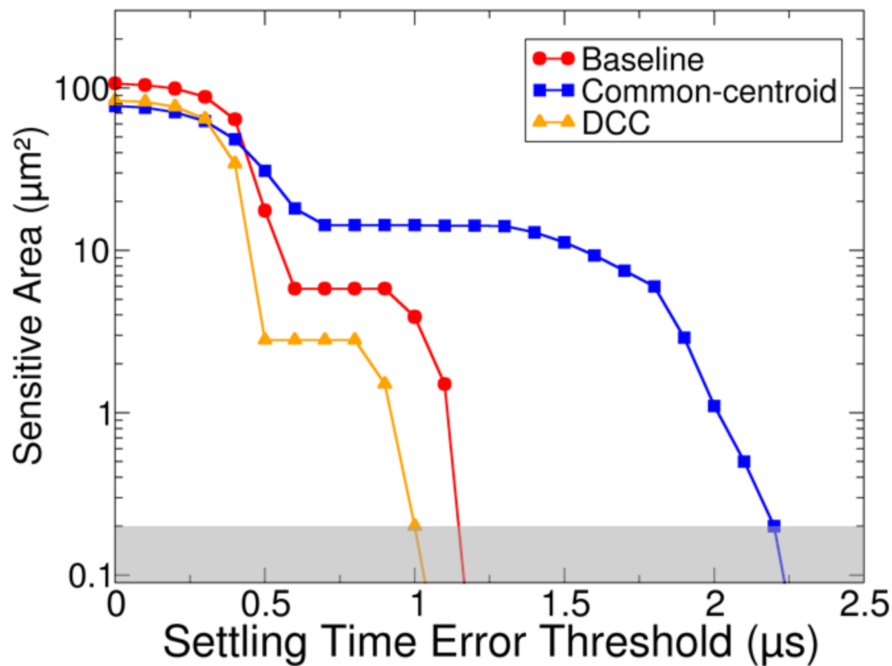


Fig. IV-34 Sensitive area of the three cascode output stage layouts shown in Fig. IV-37 as a function of settling time. The grayed out area corresponds to an area the size of a single data point. This data is for a laser energy of 3.1 nJ [58]

operate without error it would correspond to 2 MS/s for the DCC design and 526 kS/s for the baseline design. This indicates that the simple layout change to the casocde stage of the amplifier would allow it to operate at 4X the speed of the baseline, for this laser energy (2.3 nJ)[58].

A similar comparison to the one just discussed is presented at the higher 3.1 nJ laser energy (Fig. IV-34). At the higher laser energy a DCC layout still consistently provides the smallest sensitive area. However, the common-centroid layout has the largest sensitive area for settling times larger than approximately 500 ns. The common-centroid layout contributed to SETs with the longest duration of the three tested layouts. This is a slightly unexpected result, the common-centroid layout was meant to be a step towards hardness with some charge sharing occurring. Further investigation shows that in all three layouts the longest duration SETs are generated in the NMOS portion of the cascode stack. Examination of Fig. IV-30, indicates that the halved NMOS devices (W= 1 μm) and the laser spot size (1.4 μm) are very close to being the same. The charge deposition profile of the laser nearly encompassed the entire area of each NMOS device in the cascode stack, while only covering half a device in the baseline layout. The error map of the NMOS devices indicates that the longest duration strikes occur when the laser is roughly centered on the device, therefore enveloping it completely. The PMOS devices are significantly larger, so they were not affected in the same manner.

The sizing and spacing of the common-centroid and DCC layout are identical. The only difference between the two layouts is the orientation of the devices. The large reduction in settling times achieved with the DCC layout compared to the common-centroid layout, therefore further demonstrates the power of the layout technique (and its

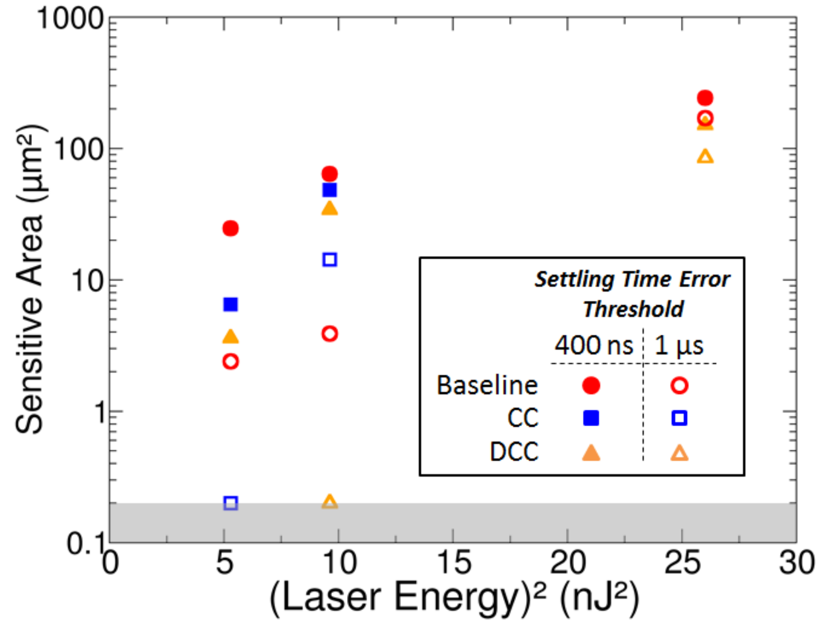


Figure IV-35 Sensitive area of three cascode stage layouts as a function of the square of the laser energy. Two different settling time thresholds were used 400 ns (closed symbols) and 1 μs (open symbols) [58]

importance to SNACC). This large difference also illustrates how important it is for a designer to be cognizant of the layout portion of the design.

Fig. IV-35 is the sensitive area of all three design calculated for two different settling time thresholds, 400 ns (closed symbols) and 1 μs (open symbols). As discussed in the background chapter, charge deposition is proportional to the square of the laser energy, so in this figure that sensitive area is plotted as a function of laser energy squared. In the case of both the time thresholds and across all three laser energies the DCC layout (SNACC hardening) has the lowest sensitive area. Using Fig. IV-35 to quantify the reduction in sensitive area, a 95% and 41% reduction in sensitive area can be achieved at lowest and highest energy tested using the 400 ns threshold with the SNACC hardening technique. Using the 1 μs threshold, a 92% and 50% reduction is seen at the lowest and highest tested energies respectively.

The cascode output stage itself is made up of 8 transistors that have one of two primary functions. The four-cascode transistors (M15-M18) have high output resistance and gain. The other four transistors (M13, M14, M19, M20) are current sources. There are two primary difference of relevance between the cascode output stage and the input stage. The cascode stage is not differential and the cascode transistors in the cascode stage do not have a common mode connection, like their input stage counterparts. Therefore the cascode devices are sensitive to SE strikes on both their source and drains, while the current source devices are only sensitive to SE strikes on their drains (their sources are tied to a power rail).

Figs. IV-36 and IV-37 look at the sensitive area, using a 400 ns threshold, of the cascode devices and the current source devices respectively. The comparison is important, particularly for the cascode devices, because both the source and drains of the devices are sensitive. For the cascode devices (Fig. IV-36), SNACC hardening reduces the sensitive area by 80, 29, and 6% for the three tested energies 5.29 nJ^2, 9.61 nJ^2, and 26.01 nJ^2 respectively. The increase in SE immunity significantly shrinks with increasing laser energy and charge deposition. This is because charge sharing is similar in the baseline to that of the DCC layout at the higher energies. This is due to the fact that both the drains and sources of these devices are sensitive to SEs. The DCC layout is designed to specifically increase the charge sharing between drains, but at a high enough charge level the sources and drains collect charge similarly independent of their orientation[58]. This explains the convergence of the baseline and SNACC hardened designs.

Fig. IV-37 is the same comparison, but for only the current source transistors. For these devices, the sensitive area was reduced by 97% at 5.29 nJ^2 (there is no data point

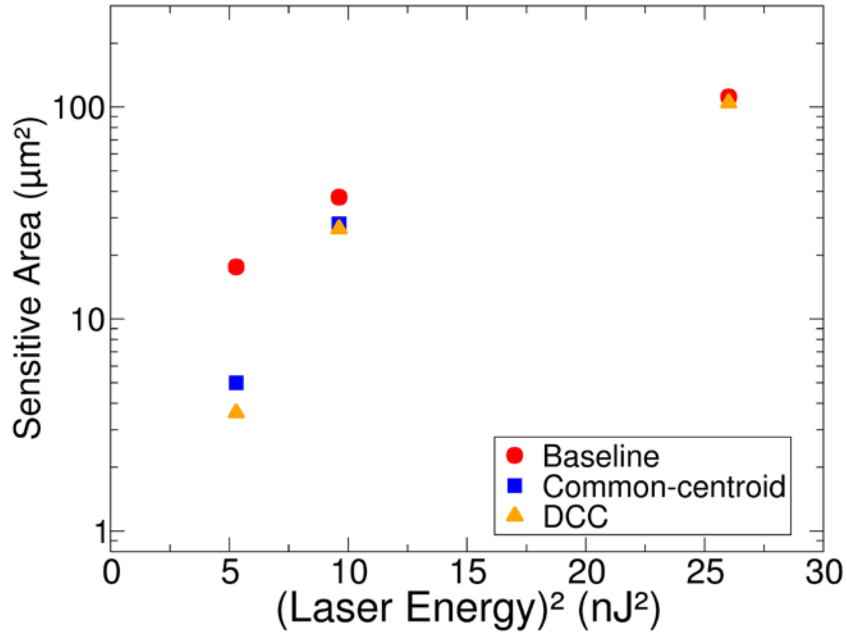


Fig. IV-36 Sensitive area of the cascode devices, (M15, M16, M17,M18) using the three different layouts as a function of the square of the laser energy using a 400 ns settling time threshold [58]

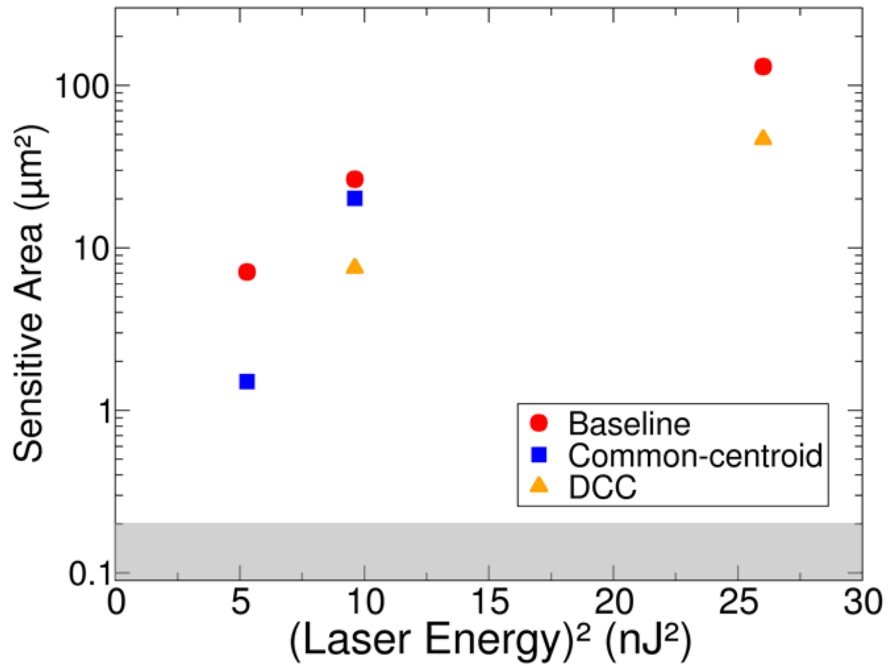


Fig. IV-37 Sensitive area of the cascode devices, (M13, M14, M19, M20) using the three different layouts as a function of the square of the laser energy and a 400 ns settling time threshold [58]

for DCC because it is below the single data point marker), 72% at 9.61 nJ^2, and 64% at 26.01 nJ^2 [58]. The SNACC hardening maintains it effectiveness for these devices across all tested laser energies. This is primarily because these devices only have one sensitive junction (the other junction is tied to a power rail).

The application of SNACC in this experiment requires zero additional active area. However, the additional device spacing required to implement the technique (or the common-centroid layout) creates a silicon area increase of 28%. The cascode output stage is a relatively small sub-circuit of an op amp in terms of area, so the physical area of the op amp increased by less than 1% with this application of SNACC.

The DCC results discussed in the previous section used the same op amp and 400 ns criteria for establishing an error as this SNACC research. The baseline input stage had a sensitive area of 100 μm^2 for a laser energy of 26 nJ^2. The DCC hardening of the input stage reduced its sensitive area to less than 3 μm^2. The sensitive area of the baseline cascode output stage was similar to the input stage's, even though it is a fourth of the actual size. This made the cascode stage by far the most vulnerable to SEs. The novel application of SNACC significantly hardened this most vulnerable stage, with a very small penalty (less than 1% area increase of op amp).

Conclusions

This chapter presented two novel hardening techniques that leverage a phenomenon that typically plagues RHBD circuit designers, (charge sharing) and uses it to significantly increase a circuit's hardness. The first use of charge sharing through a DCC layout was not a completely novel idea. However, its presentation here is the first

experimental verification of its efficacy. This work is also the first to measure its effectiveness, measure the associated penalties, and provide evidence that it will become more effective as technologies scale further below the 180 nm technology used in this work.

The expected increase in SE immunity for the input stage of the single-ended output op amp ranged from complete immunity, to at least an order of magnitude reduction in sensitive area for all tested laser energies. This effectiveness was confirmed through testing the input stage of the fully differential op amp. The fully differential op amp's input stage had a reduction of sensitive are of up to 73%. The differential cascode output stage, partially due to a lower CMRR had a reduction of sensitive area of up to 42%. These reductions in sensitive area came with zero increase in offset voltage or physical layout area.

This work also presents the first experimental verification of hardening via the SNACC technique through two different implementations. One of these techniques requires the addition of six additional devices, adding sensitive area to the design. The other implementation does not add devices or sensitive area, but does increase the designs physical area due to the use of a DCC layout. The "six transistor" version of SNACC applied to the bias circuit of a single-ended op amp yielded a 96% reduction in sensitive area in the bias circuit. The implementation of SNACC that leverages the inherent current mirror topology of the cascode stage of the same op amp reduced the sensitive are by up to 92%.

CHAPTER V

HARDENING VIA NODE SPLITTING

Introduction

The previous chapter described and experimentally validated two extremely powerful techniques that fall into the hardening by charge sharing category, DCC layout and SNACC. While these techniques incur only a minor area penalty, or no penalty at all, they do have limitations in application. The techniques themselves are best used for differential circuits (DCC), static circuits with a single/dominant vulnerable node (SNACC), or a circuit with an inherent current mirror/compensation topology (SNACC). SNACC and DCC also require a technology where charge sharing is prevalent, therefore they are not well suited for silicon-on-insulator (SOI) technologies or any other process that prevents/minimizes charge sharing.

This chapter introduces a new hardening technique that falls into a broader class of hardening techniques called hardening by node splitting. Hardening by node splitting techniques can be applied in any process and work well with any circuit type. The hardening by node splitting concept, depicted in Fig. V-1 is to split a circuit into N pieces or paths [61]. In the process of creating N paths each device is also split into the same N number of unit cells. This process of splitting a device into N pieces means that the active area of the circuit does not increase, but the physical area will increase slightly due to PDK device spacing requirements. During normal operation there is no change to the function or performance of the circuit. However, if a SE occurs in any one path of the

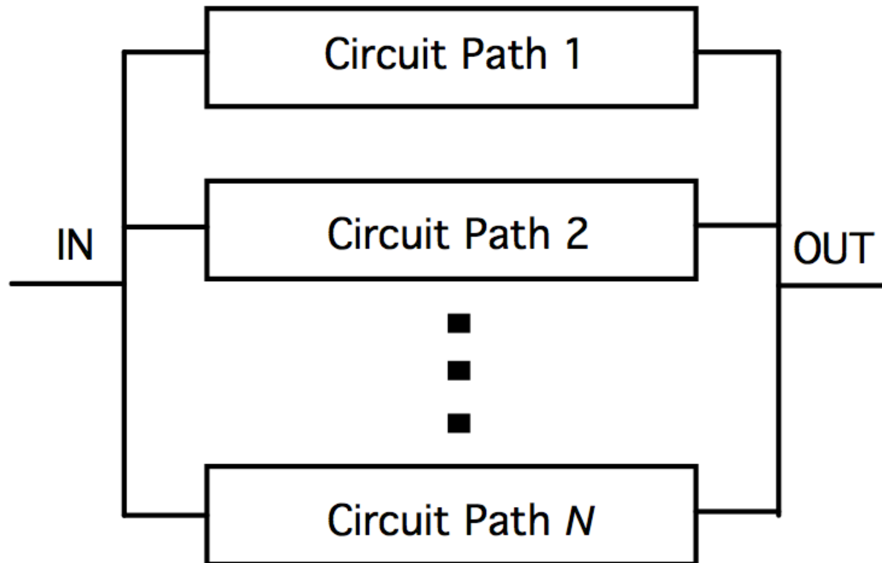


Fig. V-1 The hardening via node splitting concept [61]

circuit, then the remaining paths will maintain signal integrity and hence mitigate the SEEs. In an ideal hardening by node splitting design the circuit path struck by the SE would disable, but this is not always possible [61]. Even without the affected path disabling the entire circuit will see some reduction in perturbation.

The hardened by node splitting concept was first introduced in 2008 [62]. In this work the author sought to harden the switched capacitor sample and hold (S/H) amplifier depicted in Fig. V-2 [62]. A simulation study showed that the floating nodes associated with the capacitors were significantly more vulnerable than the operational transconductance amplifier (OTA). To address this vulnerability the author proposed breaking the capacitors and their associated switches into parallel paths, each half the original size. This concept, depicted in Fig. V-3 is the first use of a node splitting for radiation hardening, termed the dual feedback technique by the author [62]. The author pointed out that for this technique to be effective, switches hooked to the same OTA terminal must not share charge, and therefore should be placed in separate wells.

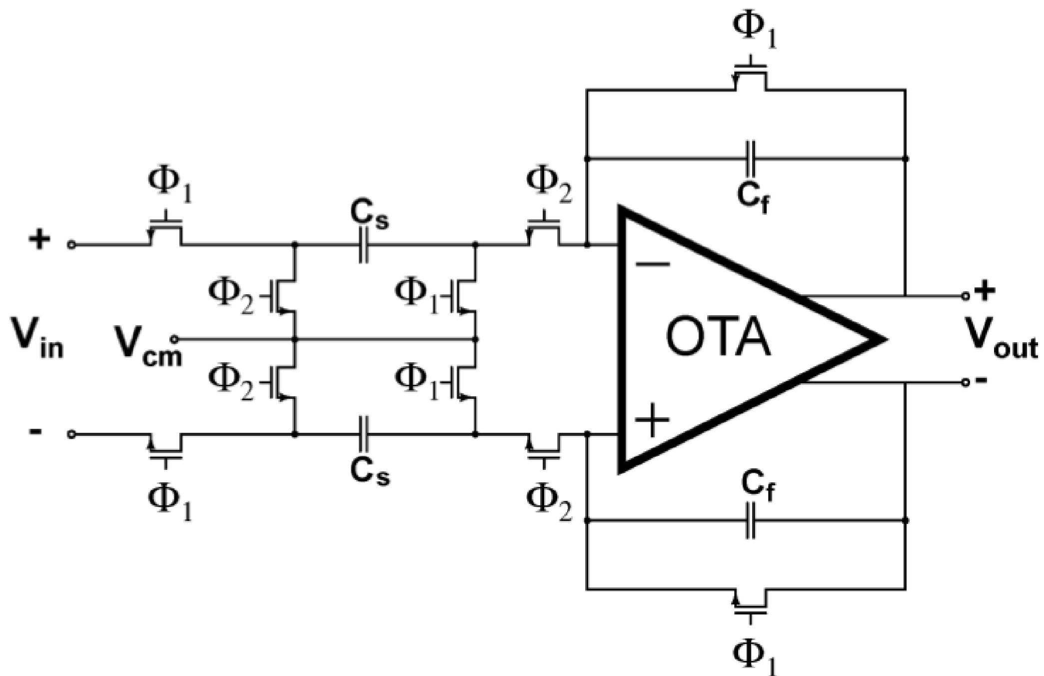


Fig. V-2 Switch capacitor S/H amplifier [62]

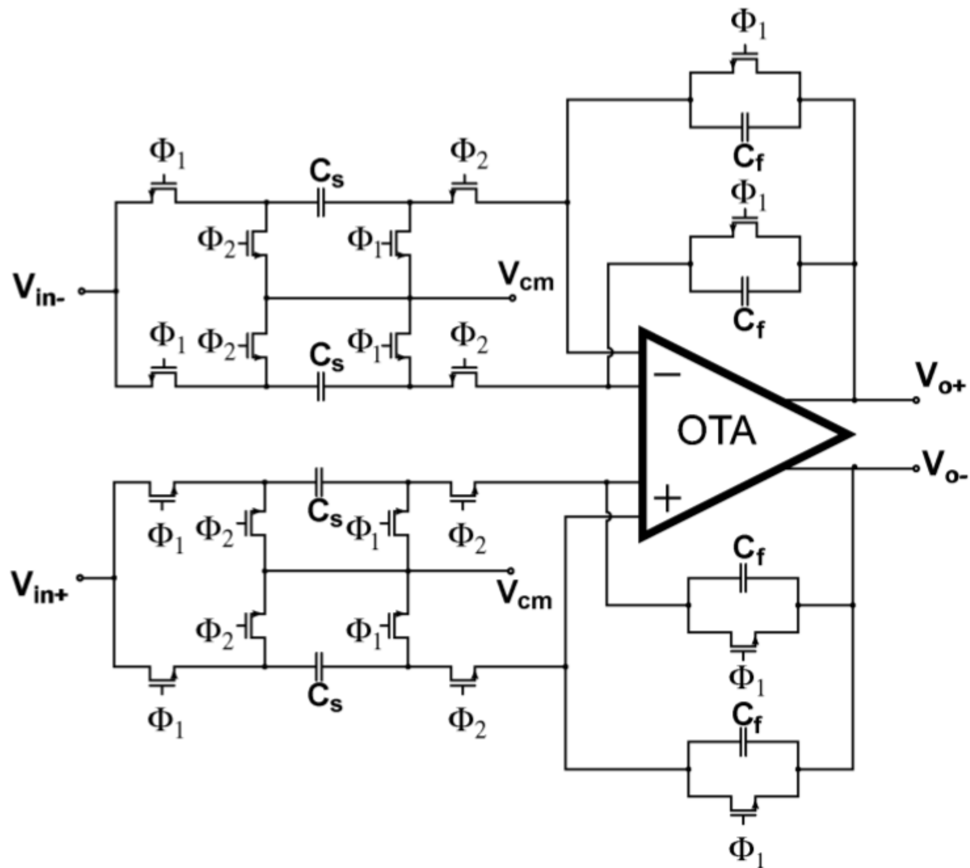


Fig. V-3 RHBD switched capacitor S/H amplifier using node splitting [62]

However, the author recommends interleaving switches from opposite terminals to use a DCC layout and leverage the OTA's common-mode rejection. One of the ways the author chose to convey the performance of this hardening technique was to plot error output voltage vs. deposited charge. A sample of these results is shown in Fig. V-4 [62]. These simulation results show that the maximum error for the baseline design is 1.1 V at a deposited charge of 120 fC. The maximum error in the dual feedback hardened (node split) circuit is 108 mV at a deposited charge of 30 fC. This lowering of the saturation value for errors is related to the halved devices having a lower nodal capacitance and a larger ΔV_{GS} for a lower deposited charge amount [62]. There is very minimal penalty associated with the gain in radiation hardness using this technique. However, it does have a significant limitation. This technique as presented requires the switches to be the same type as the input devices (e.g. NMOS with NMOS). This means that the common-mode input range, which is already critically low in modern CMOS processes, is further limited.

The limitation in common-mode input range was later solved in a 2013 paper that introduced the quad-path hardening technique [63]. The quad path hardening technique is depicted in Fig. V-5 [63]. The quad path technique requires each capacitor and input switch to be split into four parts each a quarter of the size. This split coupled with a fully complementary OTA (like the ones used in this work), where the input device are each split in half creates four signal paths. This proposed advancement to the previously discussed dual feedback technique was created primarily for SE mitigation, but it also has electrical benefits. The most important electrical benefit is that the complementary input devices gives the circuit a full rail-to-rail common-mode input range without the need for

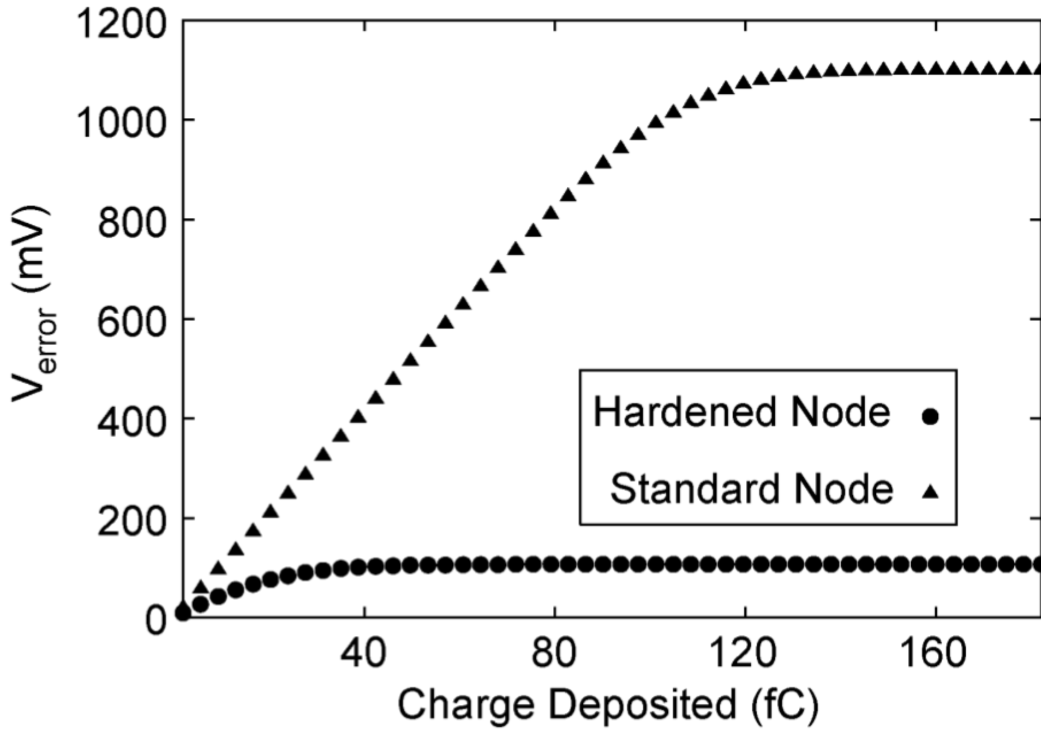


Fig. V-4 Simulation based results for the dual feedback hardening technique as applied in Fig. V-3 [62]

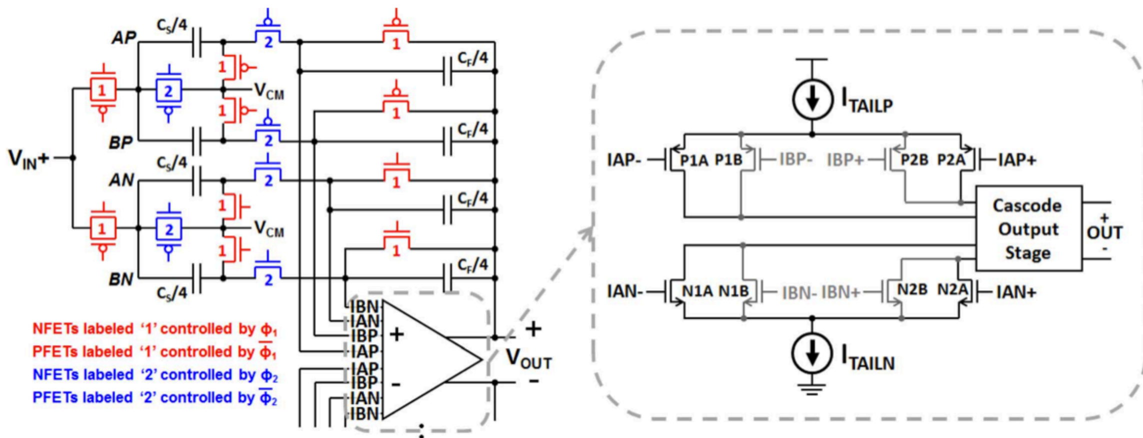


Fig. V-5 Half of the quad path hardening technique (the inverting half is identical) and a simplified schematic of the required modified complementary folded casocde OTA [63]

a charge pump. The author fabricated this quad path design as well as a baseline (similar to Fig. V-2) and a dual path design (similar to Fig. V-3) in a 45 nm SOI technology. These design were then take to NRL for TPA experimental testing.

Results from these TPA experiments are shown in Figs.V-6 and V-7. Fig. V-6 is a plot of the sample errors generated on the most sensitive NMOS device versus the square of various laser energies. There are five different S/H amplifiers being compared, a transmission gate baseline variant (TG Baseline), a transmission gate dual path variant (TG Dual), a quad path variant (Quad), the NMOS baseline (N Baseline), and finally the NMOS dual path variant (N Dual). The device types either NMOS or transmission gate refers to the switches used in the switch capacitor networks. This plot shows that the errors from the TG Baseline, TG Dual, and N Baseline all increase fairly constantly with the square of laser energy. As the previously discussed simulation paper predicted the N Dual significantly reduces the voltage errors and saturates as a much lower value. The quad path technique introduced in the work reduces the errors and saturates at an even lower value. The maximum errors in the baseline exceed 250 mV, while the dual path and quad designs top out at 59 and 25 mV respectively. This is a roughly 90% reduction in maximum error. Fig. V-7 shows the maximum errors following strikes to the PMOS devices, which have the opposite polarity. This time there are only three designs to compare and are labeled the same as the previous plot. The transmission gate based designs both have maximum errors that track with the square of the laser energy. The quad path design saturates at a significantly lower voltage magnitude. There is an 87% reduction in maximum error for PMOS strikes. It is important to note, these reductions in maximum error are achieved while increasing the common-mode input range.

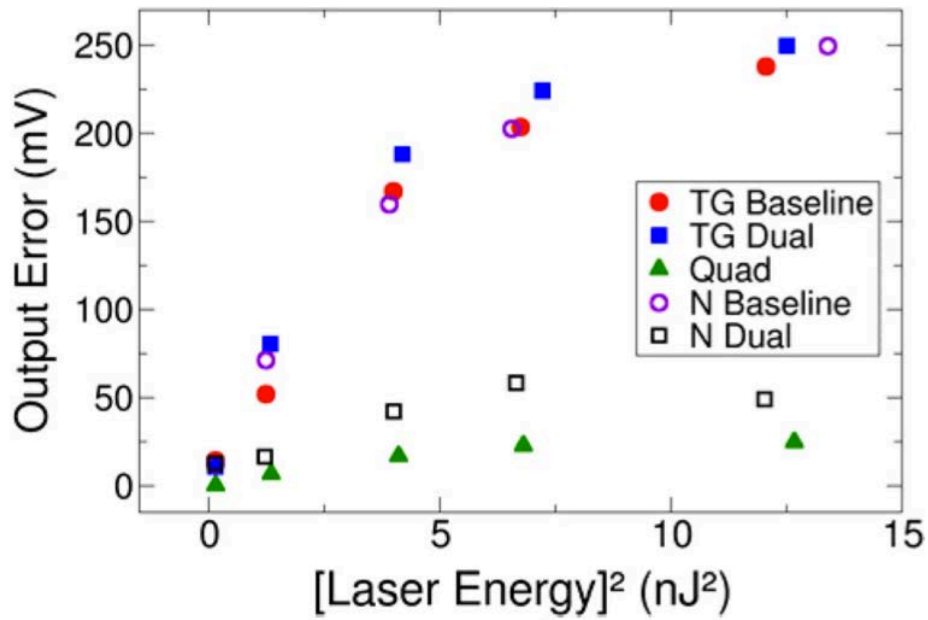


Fig. V-6 The maximum output error of the five different S/H amplifiers tested versus the square of laser energy following strikes to the NMOS switches[63]

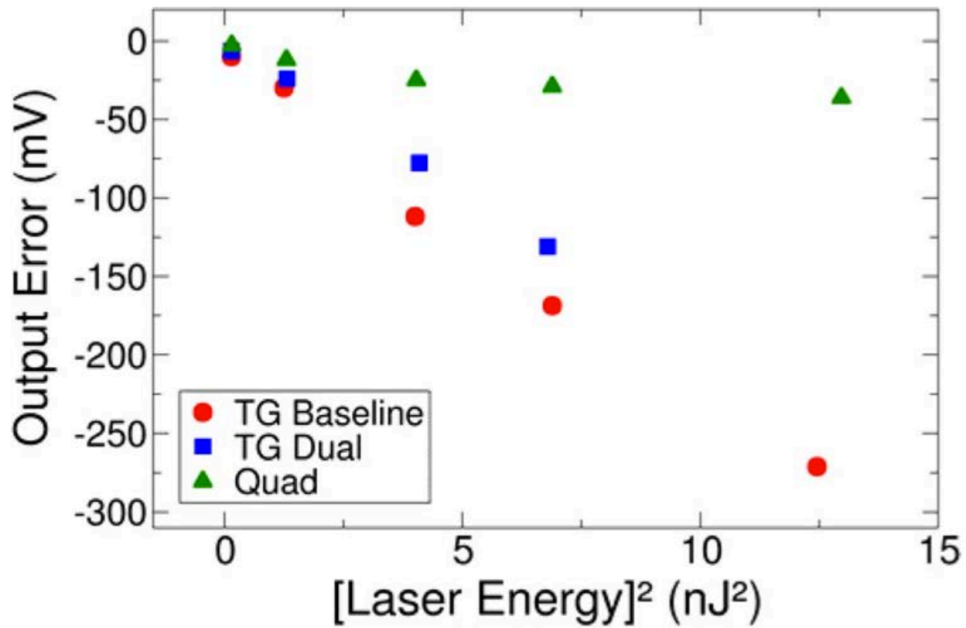


Fig. V-7 The maximum output error of the five different S/H amplifiers tested versus the square of laser energy following strikes to the PMOS switches [63]

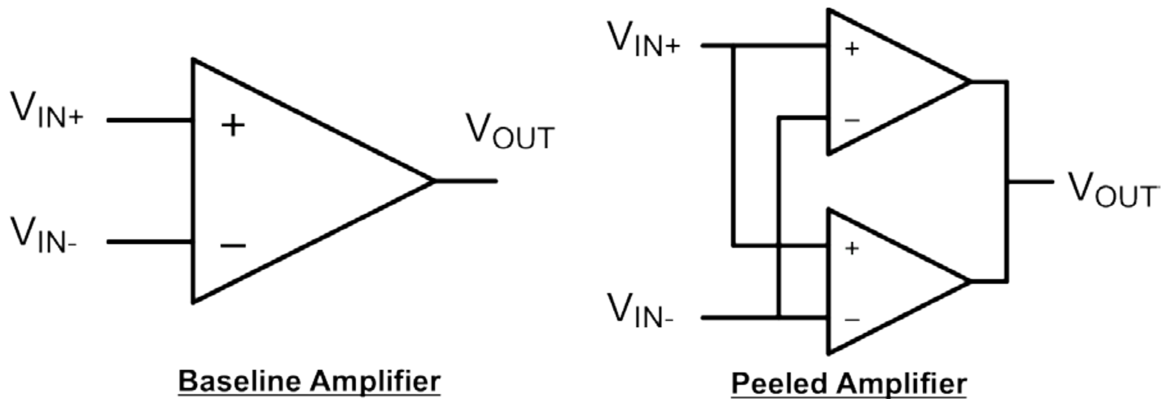


Fig. V-8 Applying the hardening via node splitting concept to a continuous time circuit such as an amplifier in the form of a peeled layout. The baseline amplifier is split into two copies each half the original size.

Peeled Layout

The previously discussed novel hardening techniques both fall into the category of hardening via node splitting. This concept however is not confined to just these discrete time circuits. Continuous time A/MS circuits, such as op amps typically have relatively large transistors in order to achieve high open-loop gains or quiescent currents. In layout form these devices are often broken into unit cells connected in parallel to facilitate matching. With this in mind, an A/MS circuit such as an op amp can be split in half or peeled into two identical copies, each half the size of the original. If the two copies of the amplifier are then connected in parallel, the output sees the same electrical characteristics as the original amplifier. The only difference is an area penalty associated with device and well spacing rules. As with the original concept depicted in Fig. V-1, the circuit can also be split into more than two paths. This technique is shown symbolically in Fig. V-8 and can be applied either to the entire A/MS circuit or to individual stages.

Peeled Layout in an SOI Technology

In order to test this concept and its application to a continuous time A/MS circuit, two different test chips were designed and taken for testing. The first experiment was conducted on the 32 nm SOI folded cascode op amp described in Fig. III-16, shown again in Fig. V-9 for convenience (without the bias circuit). This circuit highlights an important advantage of the hardened by node splitting concept, it can be applied to technologies such as SOI where charge sharing is greatly minimized. In this experiment only the input stage was peeled. Fig. V-10 is the schematic of the peeled op amp with the layouts for the baseline and peeled op amps in Figs. V-11 and V-12 respectively. Fig. V-11 and V-12 illustrate how small of an area penalty is incurred with this technique, 4 %.

The baseline and peeled input stage 32 nm SOI op amps were taken to NRL for TPA testing. During the testing the op amps were biased mid-rail at 450 mV (V_{DD} = 900 mV) with a closed loop gain of 331 V/V using resistors of 3.3 MΩ and 10 k Ω. As discussed in chapter III the larger gain was chosen to maintain the stability of the circuit. Two-dimensional scans of the op amp were performed with a resolution of 0.1 μm in the x dimension (along gate length) and 0.2 μm in the y dimension (along width of the device).

The TPA laser experiments were performed on the baseline and peeled input stage op amps at three different laser energies, 0.839 nJ, 1.19 nJ, and 1.49 nJ. At each point of the scan fifty transients were captured and averaged on the oscilloscope. The captured transients were analyzed for maximum perturbation and settling time. Settling time for this experiment due to the sensitivity of the parts and noise floor of the lab was defined as the time the output exceeded 25 mV. This corresponds to a ½ LSB using the 900 mV of

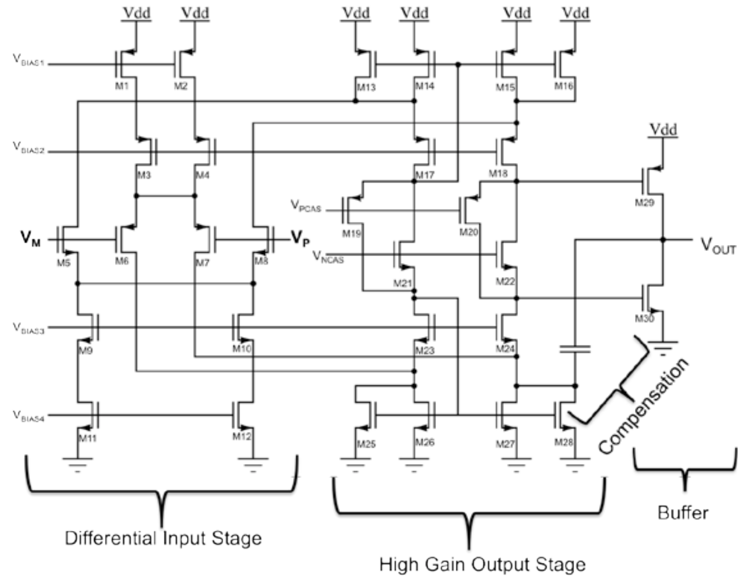


Fig. V-9 The folded cascode op amp designed in a 32 nm SOI technology, used for testing of the peeled layout concept (bias circuit not shown)

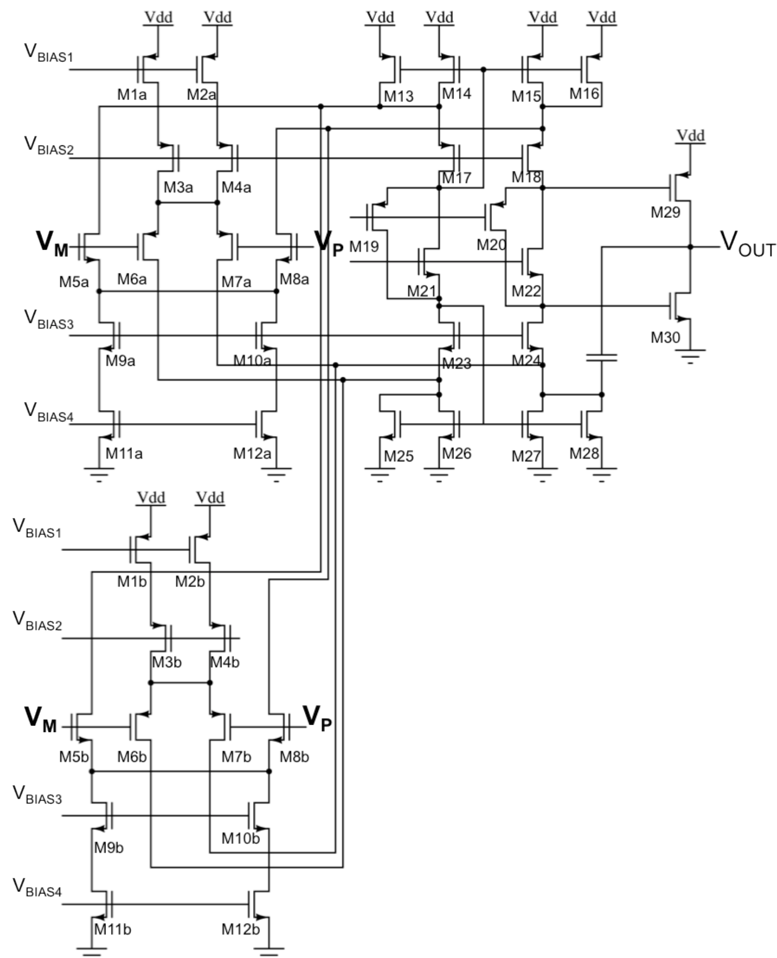


Fig. V-10 Schematic of op amp in Fig. V-9 with a peeled input stage

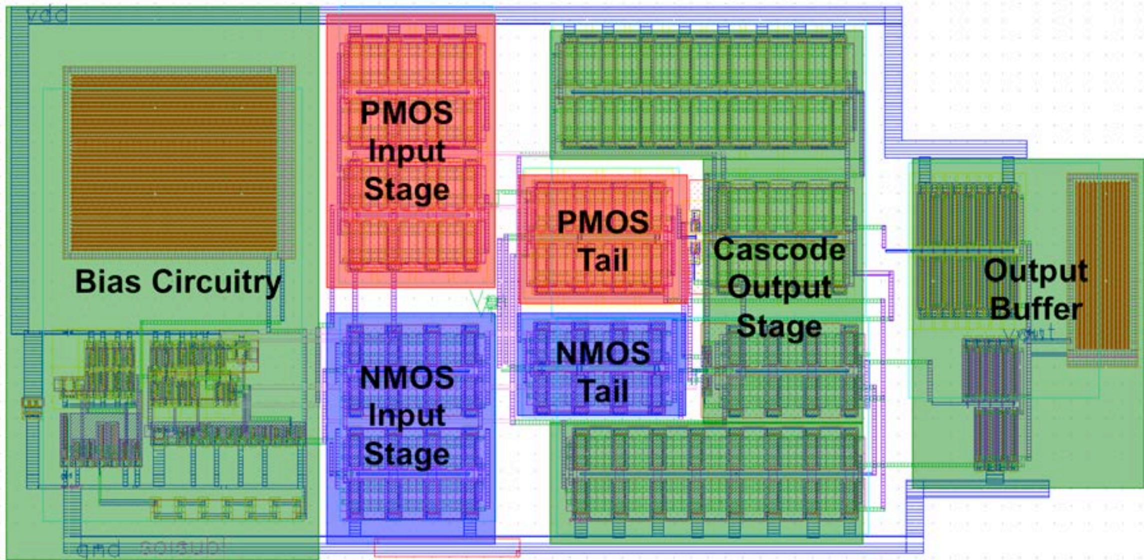


Fig. V-11 Layout of the baseline 32 nm SOI folded cascode op amp shown in Fig. V-9.

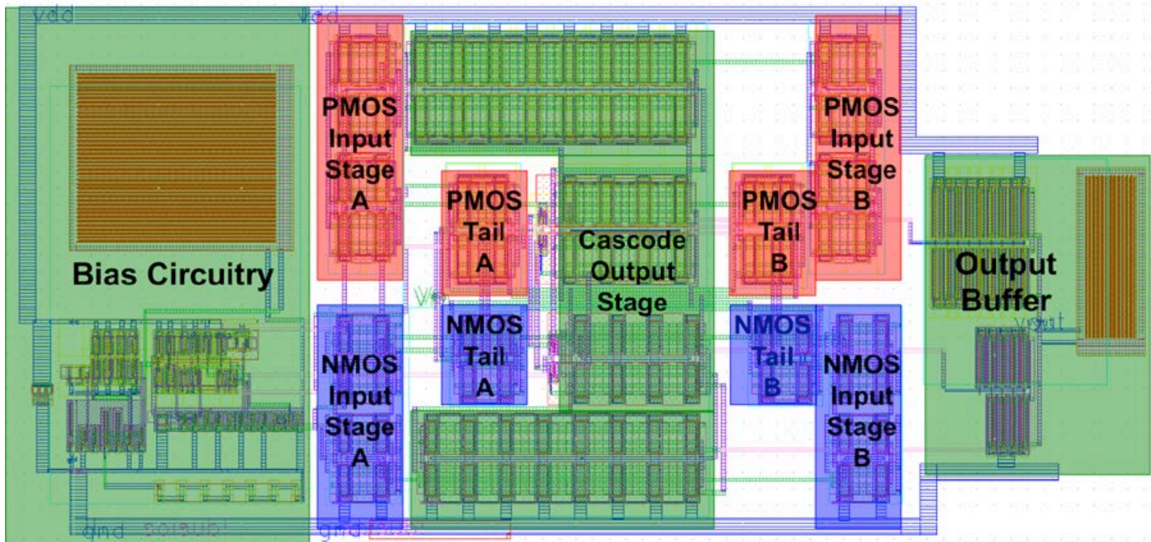


Fig. V-12 Layout of the peeled input stage version of the 32 nm SOI op amp shown schematically in Fig. V-10

headroom available and four bits of resolution.

Fig. V-13 is a scatter plot of the maximum perturbation versus settling time for the complete input stages (NMOS and PMOS) comparing the baseline and peeled layout for a laser energy of 1.49 nJ. This figure clearly shows that the maximum perturbations are smaller in magnitude for the peeled layout, however the perturbations tend to have

longer settling times. The importance of these two observations is directly tied to the intended application. If the intended application is sensitive to settling time and has a particular sampling period, then the number of perturbations with settling times that exceed that sampling period can be summed and multiplied by the raster step sizes to determine a total sensitive area. Fig. V-14 plots sensitive area determined in this manner. Using settling times (or sampling periods) of 10, 20, and 40 ns the sensitive area is reduced for all three-laser energies. The greatest decrease in sensitive area occurs for the lowest laser energy with a reduction of 17, 32.5, and 38.4 percent for each of three sampling periods respectively. The smallest decrease in sensitive area occurs for the highest laser energies with a reduction of less than 1, 2.5, and 10 percent for the respective sampling periods. These numbers give a strong indication that the peeled layout increases the SE immunity of the input stage.

There are fifty-nine long duration pulses (> 180 ns) in the peeled design and two in the baseline design. These transients may be due to laser fluctuation or may be actual errors. Fifty of the fifty-nine pulses occur following laser strikes to the center of the channel of the inverting PMOS device. There is not enough information to rule these pulses out as errors caused by laser fluctuations, so a designer must be aware of the possibility they will occur. These pulses combined, sum to a sensitive area of 1.18 μm^2 and fall within the error bars of the sensitive area calculations.

A different intended application may be more sensitive to higher maximum perturbations. Sensitive areas can be determined for different maximum perturbation thresholds in the same fashion as the sensitive areas determined for the settling times.

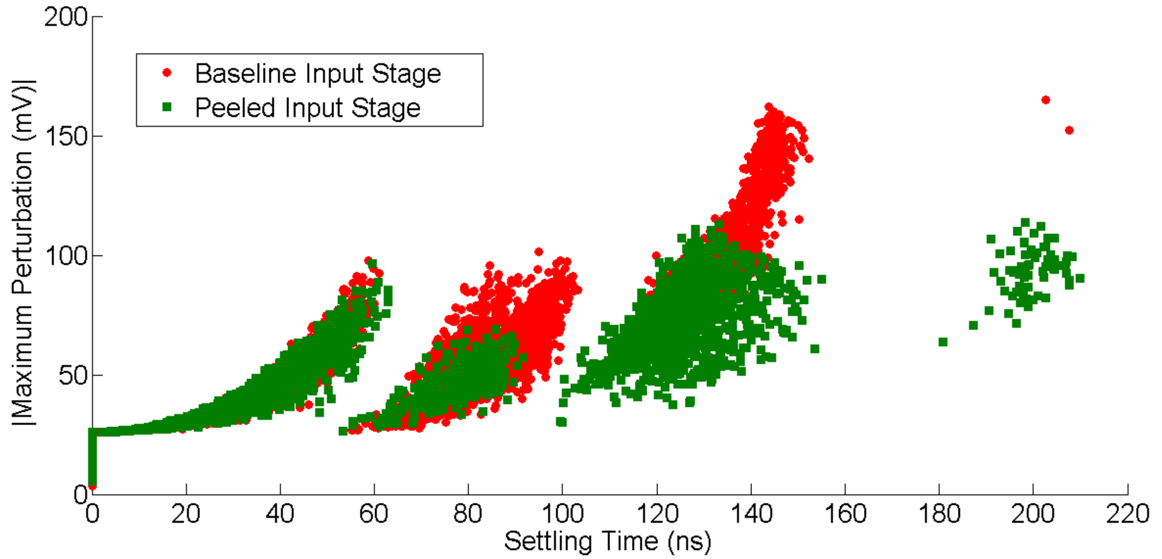


Fig. V-13 Scatter plot of the absolute value of the maximum perturbation versus settling time for the entire input stages of the baseline and peeled input stage op amp, following laser energy strikes of 1.49 nJ

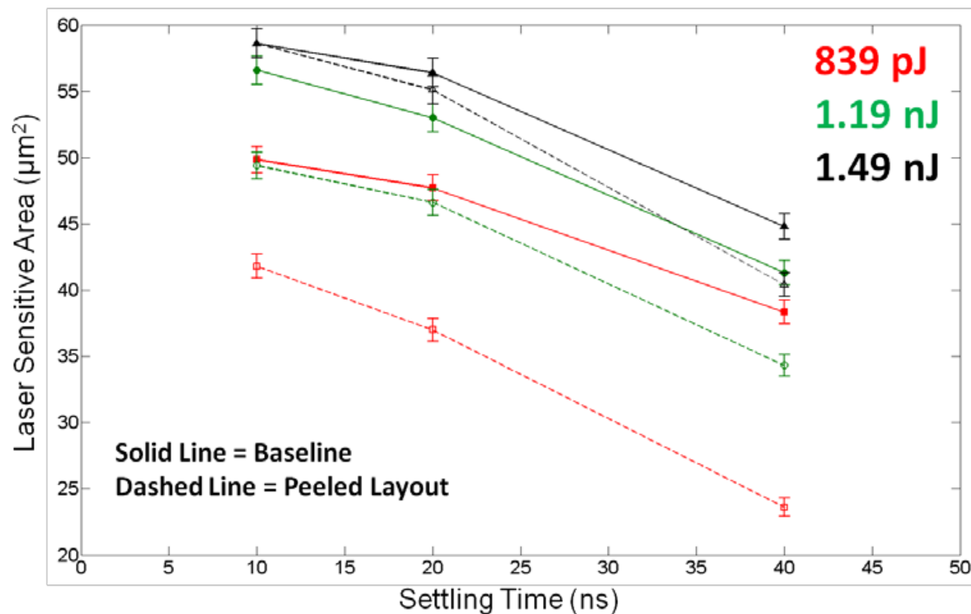


Fig. V-14 Sensitive area as a function of settling time for three different laser energies. The solid line corresponds to the baseline design and the dashed line corresponds to the peeled layout with the colors distinguishing the different energies.

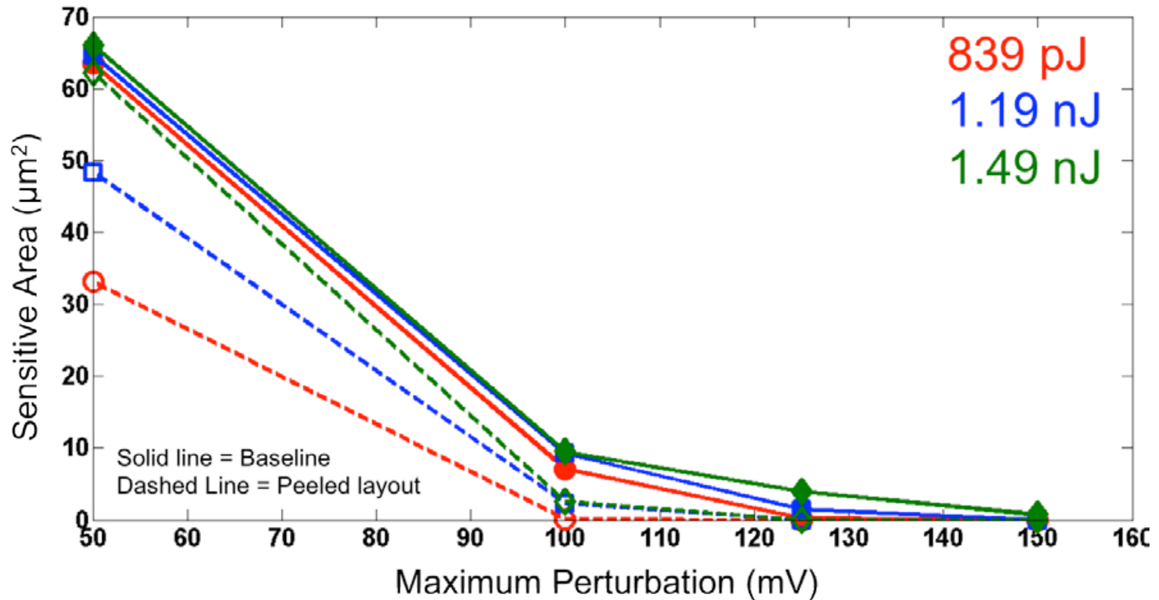


Fig. V-15 Sensitive area as a function of maximum perturbation for the three tested laser energies. The solid lines correspond to the baseline and the dashed lines correspond the peeled layout with the colors distinguishing the energies.

Fig. V-15 is a plot of the sensitive area of the baseline (solid lines) and peeled (dashed lines) input stages for different maximum perturbation thresholds at the three tested laser energies. Once again the peeled layout reduces the sensitive area for all max perturbation thresholds at all tested laser energies and is the most effective at the lowest tested energy. The sensitive areas of the peeled design also all go to zero between 100 and 125 mV, while the baseline designs has none zero sensitive areas out to 150 mV. Fig. V-16 is a different way to visualize this sensitive area; plotting the percent reduction in area achieved for different perturbation thresholds for all three-tested laser energies. Once again the technique is the most effective for the lowest laser energy with reductions of 48, 99, and 100 percent for three of the four thresholds plotted (50, 100, 125). At the lowest energy neither design had any perturbations larger than 150 mV. The technique was the least effective for the highest laser energy with reductions of 4, 72.3, 100, and 100 percent for the four plotted thresholds. As an example the baseline design had 197 points

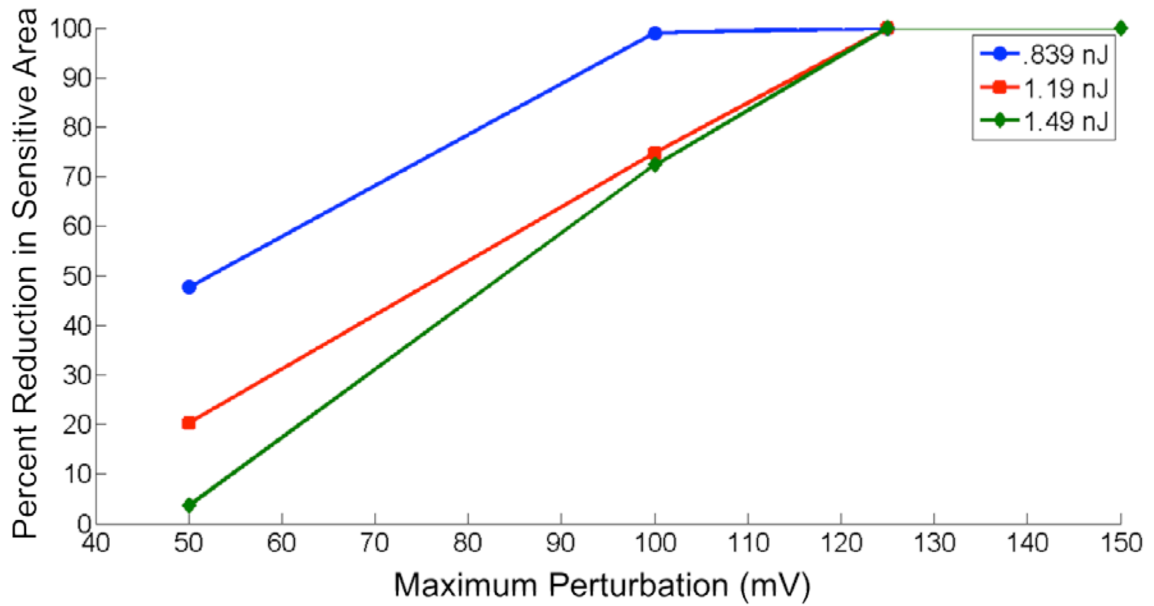


Fig. V-16 A plot of the percentage of reduction in maximum perturbation as a function of maximum perturbation for the three tested laser energies.

and 37 points that created transients with magnitudes larger than 125 and 150 mV respectively. The peeled design had zero points that created transients of either magnitude.

Peeled Layout in a Bulk Technology

A peeled layout was clearly effective in hardening the input stage of an op amp in a 32 nm SOI technology. Those tests indicated that the sensitive area was reduced whether the metric was settling time or maximum perturbation. The tests also indicated that the technique was the most effective for the lowest tested energies, corresponding to the lowest amount of deposited charge. In order to confirm these findings and test the applicability of the technique to a bulk technology a second experiment was performed using the op amp described in Fig. III-13, shown again here in Fig. V-17.

The experiment was performed at NRL using the TPA through-wafer technique. Multiple op amps were tested; the ones of concern for this section were the baseline and peeled input stage designs, similar to the SOI experiment previously discussed. Two-dimensional scans of the input stages of these designs were performed at a resolution of 0.2 in the x-direction (along gate length) and 0.5 in the y-direction (along the device width). The scans were performed at three different laser energies, 1.1 nJ, 2.6 nJ, and 3.5 nJ. At each point of the scan the positive and negative polarity output terminal were captured and averaged for 25 separate strikes. The output was then recorded as the difference between the positive and negative polarity terminals (V_{out+}-V_{out-}). The captured transients were evaluated for maximum perturbation and settling time. In this experiment, just like the previously discussed experiments involving this op amp design, settling time was defined as the time the output exceeded 10 mV.

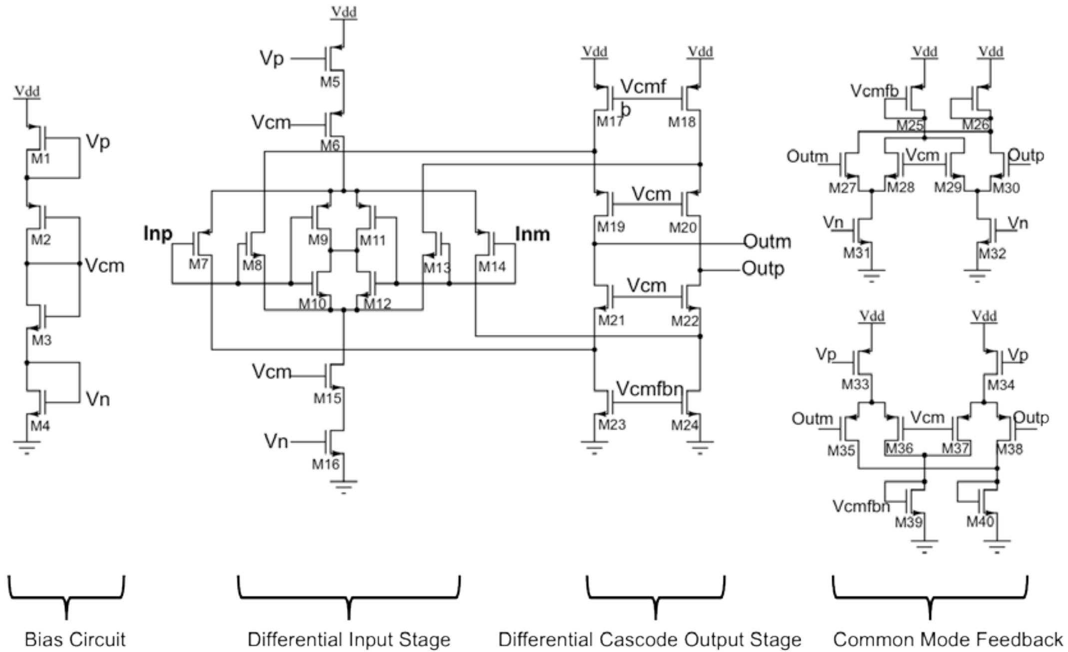


Fig. V-17 The fully differential op amp described in chapter III (Fig. III-13) used to test the applicability of a peeled layout in a bulk technology

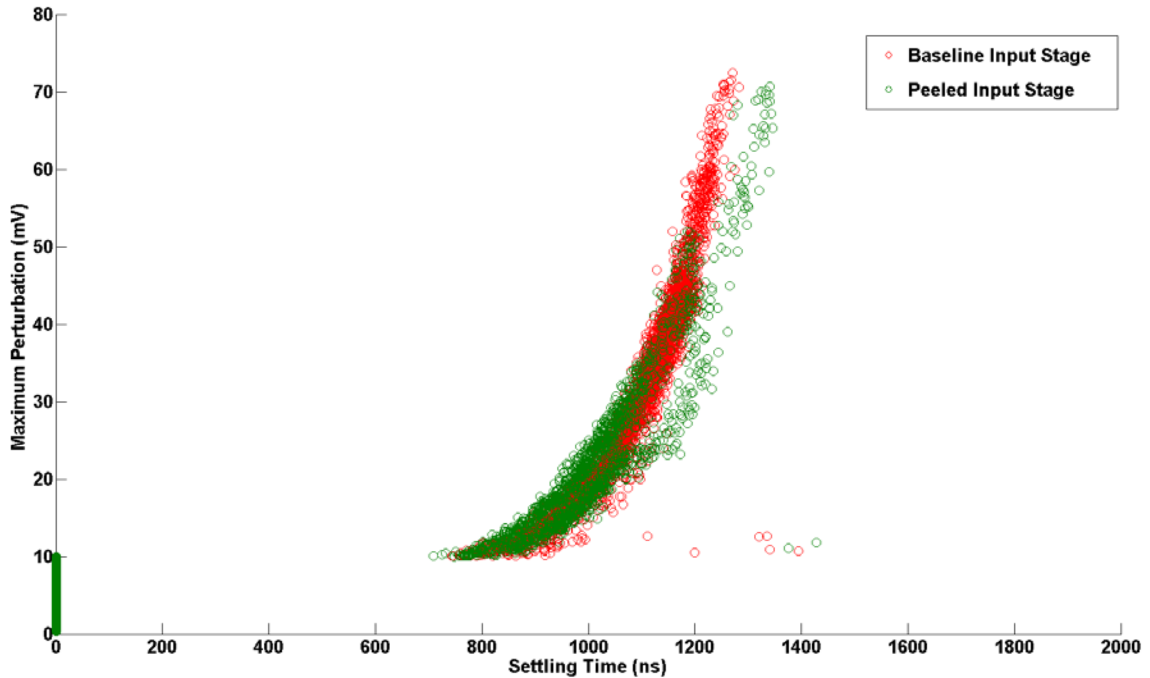


Fig. V-18 Maximum Perturbation versus settling time comparing the baseline input stage with a peeled input stage for a laser energy of 2.6 nJ

Fig. V-18 is a scatter plot of some of the results from this experiment, comparing the baseline and peeled design's settling time versus maximum perturbation using a laser energy of 2.6 nJ. This figure illustrates once again that the peeled layout reduces the number of point above a certain maximum perturbation, while seeming to extend the settling times slightly. The data in Fig. V-18, as well as similar data sets for the other tested energies allow a sensitive area to be calculated for a given settling time threshold. This is accomplished by summing the data points larger than that threshold and multiplying them by the scan grid steps, as was done with the previous data sets presented. Fig. V-19 is a sensitive area plot comparing the baseline and peeled input stages across the three tested laser energies for an error threshold of 800 ns. This plot shows that the sensitive area is reduced for all tested laser energies by using a peeled layout. The greatest reduction in sensitive area occurs at the lowest tested energy (1.1 nJ)

and the smallest reduction occurs at the median energy (2.6 nJ). These reductions are by 91 and 55 % respectively. The dip in sensitive area at the highest tested energy is interesting. The reason for this is most likely charge sharing and a DCC mechanism. This will be discussed in much more detail in the next section.

The choice of a settling time to determine the sensitive area is application dependent and can cloud the overall picture. In order to investigate this, the sensitive areas of the two designs are plotted in Fig. V-20 for various settling time thresholds, using the worse case laser energy (2.6 nJ) from Fig. V-19. A peeled layout reduces the total sensitive area of the input stage for thresholds of 600, 800, 1000, and 1200 ns by 54, 55, 70, and 62% respectively. While the sensitive area is reduced by more than 50% in all cases, a design may be more sensitive to maximum perturbations than settling time.

A peeled layout reduces the number of strike locations that create perturbation magnitudes of different thresholds also. The amount of sensitive area following laser energy strikes of 2.6 nJ that can produce a transient with a maximum greater than 30, 40, or 50 mV is reduced with a peeled layout by 67, 69, and 65% respectively.

Combining a Peeled and DCC Layout

The data in the previous section had a fairly significant lowering of sensitive area at the highest tested laser energy (Fig. V-19). That would be a fairly counterintuitive trend outside the realm of this research. However, the previous chapter already experimentally proved that this exact circuit topology could be significantly hardened via charge sharing. This lowering in sensitive area suggests that there is charge-sharing

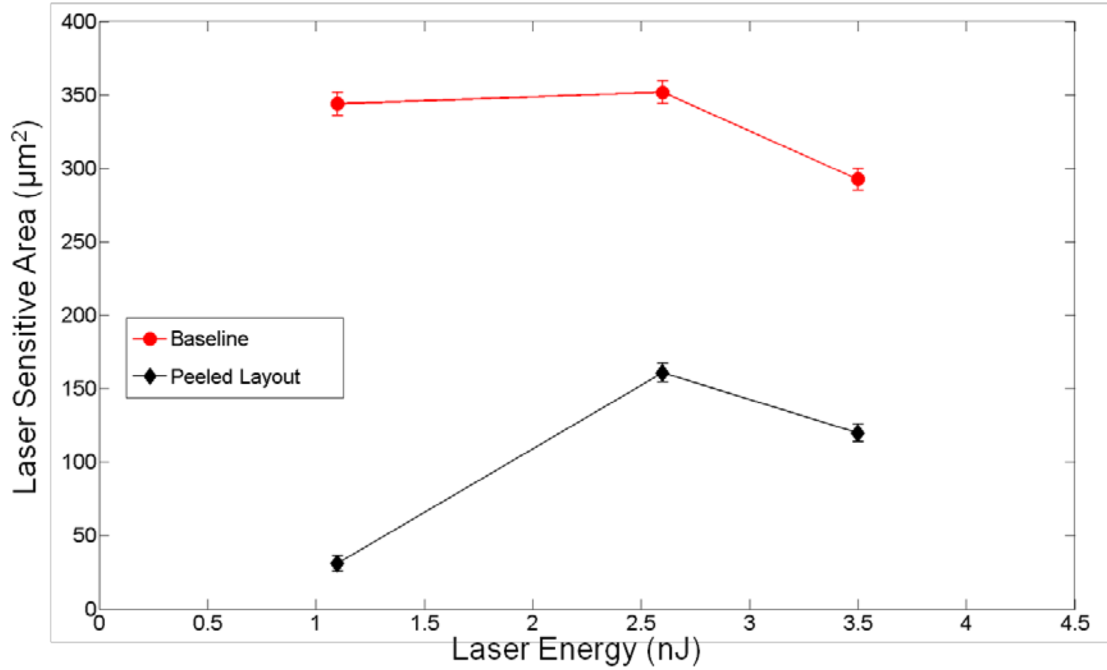


Fig. V-19 Sensitive area versus laser energy of the baseline and peeled input stage using an error threshold settling time of 800 ns.

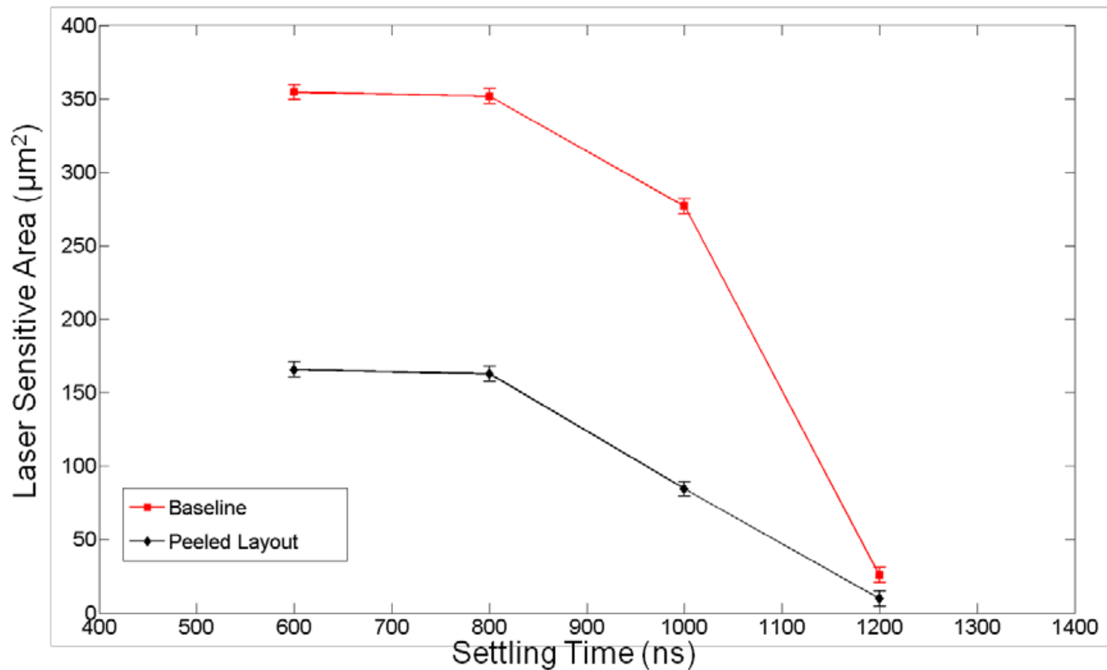


Fig. V-20 Sensitive area versus settling time, comparing the baseline input stage and the peeled input stage for a laser energy of 2.6 nJ

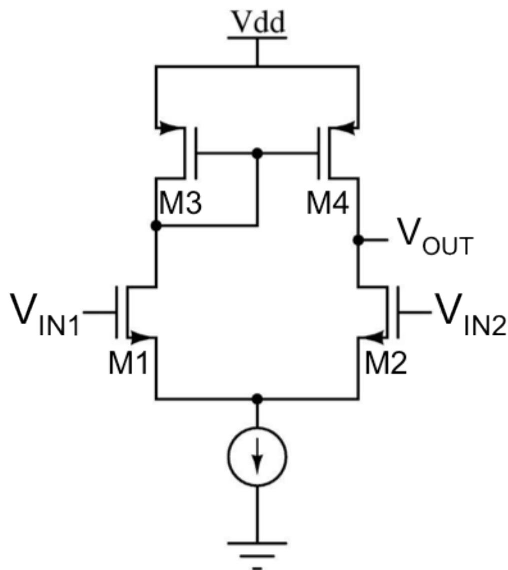


Fig. V-21 Basic differential amplifier, similar to the ones used throughout this work.

occurring in the baseline common-centroid layouts used in both the baseline and peeled op amps The technique of a peeled layout can use this and leverage a DCC layout to enhance the charge sharing and further harden the circuit.

The previous chapter demonstrated a correlation between the CMRR of a circuit and the effectiveness of a DCC layout. This correlation leads to the obvious question of how a peeled layout affects a circuit's or piece of a circuit's CMRR. A search of a basic analog circuits textbook for a differential amplifier (diff amp) similar to the ones used in the op amps of this work (shown in Fig. V-21) yields equation V-1 for CMRR [64]. In the baseline diff amp g_m is given in equation V-2, r_o is given in equation V-3,and R_o is the equivalent resistance of the tail current devices. Substituting those smaller equations into the CMRR equation (V-1) yields equation V-4.

$$CMRR = 20\log\left[g_{m1,2} * (r_{o2}||r_{o4}) * 2g_{m3,4} * R_o\right] \quad \text{V-1}$$

$$g_m = \frac{2I_D}{(V_{GS} - V_T)} \tag{V-2}$$

$$r_o = \frac{1}{\lambda I_{DQ}} \tag{V-3}$$

$$CMRR = 20\log\left[\frac{2I_D}{(V_{GS}-V_T)} * \left(\frac{1}{\lambda I_{DQ}} || \frac{1}{\lambda I_{DQ}} * \frac{4I_D}{(V_{GS}-V_T)} * R_o\right)\right] \tag{V-4}$$

A peeled version of this circuit would have half the W/L ratio of the baseline and therefore half the drain current with a g_m as shown in equation V-5 or simplified in V-6 and the value of r_o becomes equation V-7 or V-8. Finally, the value of R_o doubles, using ohm's law and the fact that the current is halved with the same voltage drop. Substituting these smaller equations into the equation to determine the CMRR of the peeled diff amp yields, equation V-9. Careful inspection of equations V-4 and V-9 proves that peeling the circuit does not change the CMRR.

$$g_m = \frac{2\left(\frac{1}{2}\right)I_D}{(V_{GS} - V_T)} \tag{V-5}$$

$$g_m = \frac{I_D}{(V_{GS} - V_T)} \tag{V-6}$$

$$r_o = \frac{1}{\lambda\left(\frac{1}{2}\right)I_{DQ}} \tag{V-7}$$

$$r_o = \frac{2}{\lambda I_{DQ}} \tag{V-8}$$

$$CMRR = 20\log\left[\frac{I_D}{(V_{GS}-V_T)} * \left(\frac{2}{\lambda I_{DQ}} || \frac{2}{\lambda I_{DQ}}\right) * \frac{2I_D}{(V_{GS}-V_T)} * 2R_o\right] \tag{V-9}$$

If the CMRR of the op amp is unchanged by the peeled layout, then combining the peeled layout technique with a DCC layout should gain further SE immunity. To investigate this theory a third op amp was tested in conjunction with the baseline and peeled input stage op amps discussed in the previous section. The third op amp had a peeled input stage and a DCC layout. Fig. V-22 is a scatter plot comparing the maximum perturbation versus settling time for the baseline input stage and the input stage of the op amp with a peeled DCC layout of the input stage (laser energy = 2.6 nJ). There is such a dramatic difference in Fig. V-22 that it is important to keep in mind that both designs have the same number of data points. There is little doubt that the peeled DCC layout combination hardens the baseline input stage, but an interesting question is how it relates to just the two other hardening techniques used alone (DCC and peeled layout).
Fig. V-23 is a scatter plot of maximum perturbation versus settling time for three hardened op amp input stages following strikes with a laser energy of 2.6 nJ. The three op amp input stages are hardened via a peeled layout, a DCC layout, and a combination of the two. All three data sets have the same number of points and it is clear that the peeled layout has the least amount of points out of the rectangle defined below10 mV and 600 ns. As discussed before, the DCC layout tends to have the longest durations while minimizing the maximums and the peeled layout does the opposite. Summing the number of points based on a criterion as we have done throughout this chapter allows for the calculation of sensitive areas.

Fig. V-24 is a plot of the baseline and the three hardened input stage's sensitive area for various settling times using a laser energy of 2.6 nJ. It is interesting that the effectiveness of the hardening techniques goes from DCC, to peeled, to the combination

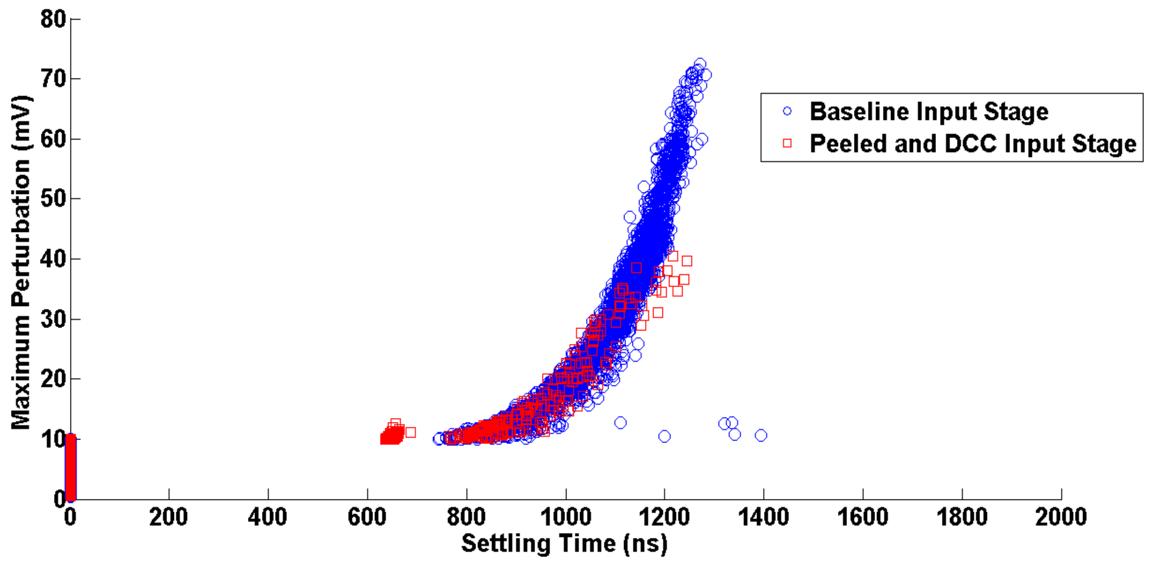


Fig. V-22 Scatter plot of the maximum perturbation versus settling time, comparing the baseline input stage to a peeled input stage with a DCC layout

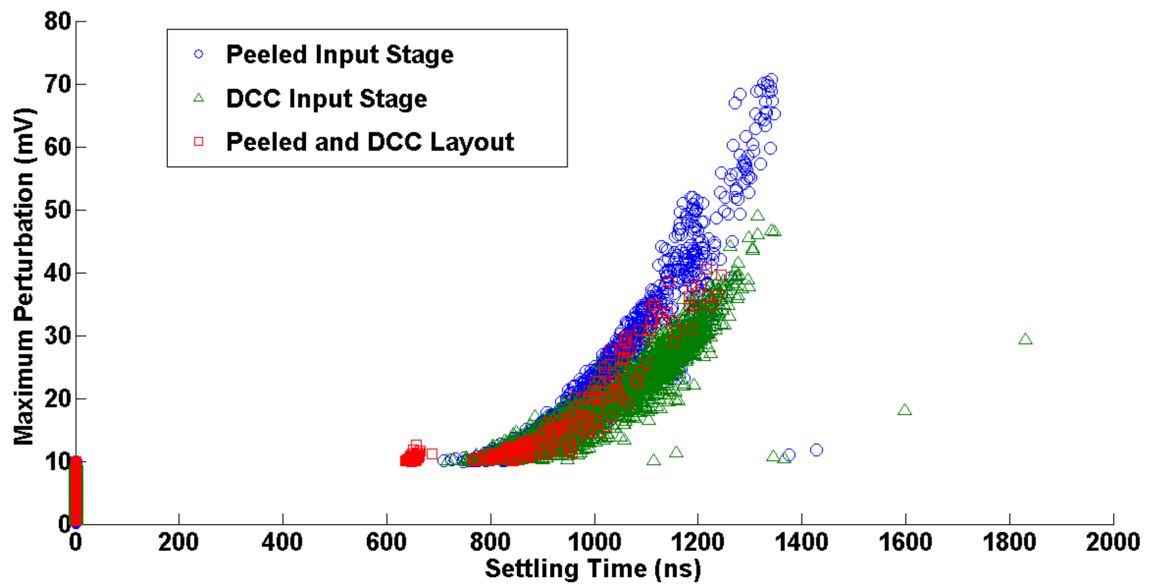


Fig. V-23 Scatter plot of maximum perturbation versus settling time of three hardening techniques, a peeled input stage, an input stage with a DCC layout, and an input stage with both for a 2.6 nJ laser energy

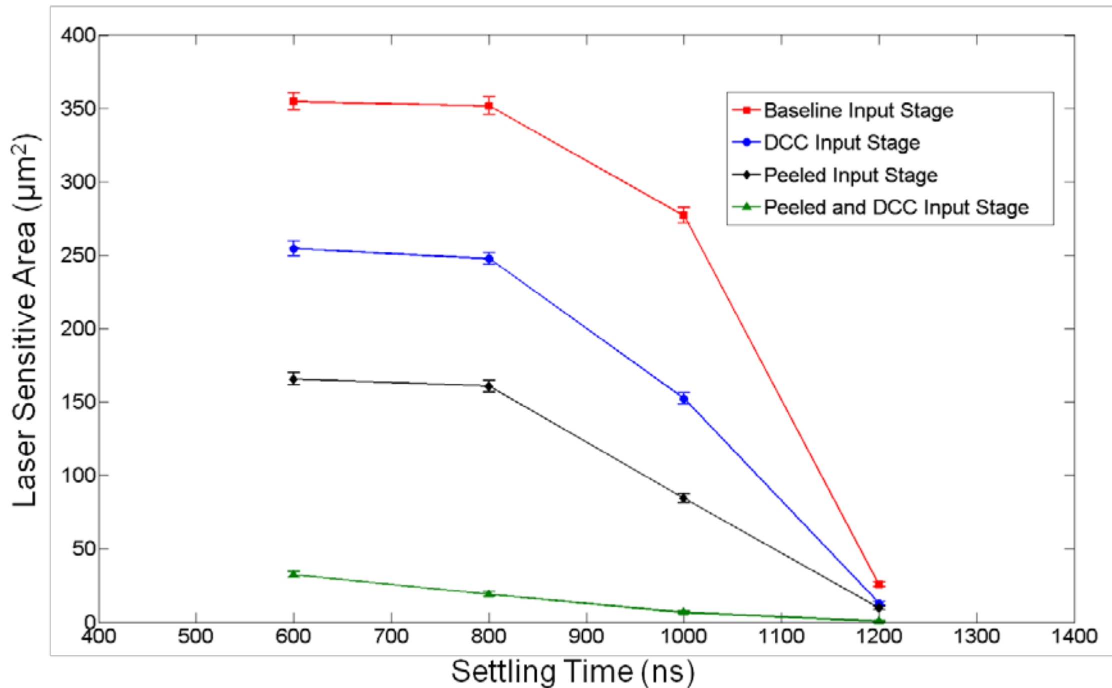


Fig. V-24 Sensitive area of the baseline, DCC layout, Peeled Layout, and Peeled with DCC layout input stages for a laser energy of 2.6 nJ

of the two in that order. All of the hardening techniques significantly reduce the sensitive area of the baseline design for all of the settling time thresholds. The reductions are 29, 54, and 91% for the 600 ns threshold for the DCC, peeled, and combination layouts respectively. Sensitive area is reduced by 30, 55, and 95% at 800 ns threshold for each layout. The reductions are 45, 70, and 98 % at 1000 ns threshold. Finally, the reductions are 50, 62, and 98 % at 1200 ns threshold for the DCC, peeled, and combination layouts respectively.

Previous sections demonstrated that the effectiveness of these hardening techniques vary with laser energy (or deposited charge). In order to investigate this a settling time threshold of 800 ns was chosen from Fig. V-23. This threshold was chosen because it encompasses a significant amount of errors from all of the designs. Fig. V-25 is a plot of sensitive area versus laser energy for this error threshold. The figure illustrates

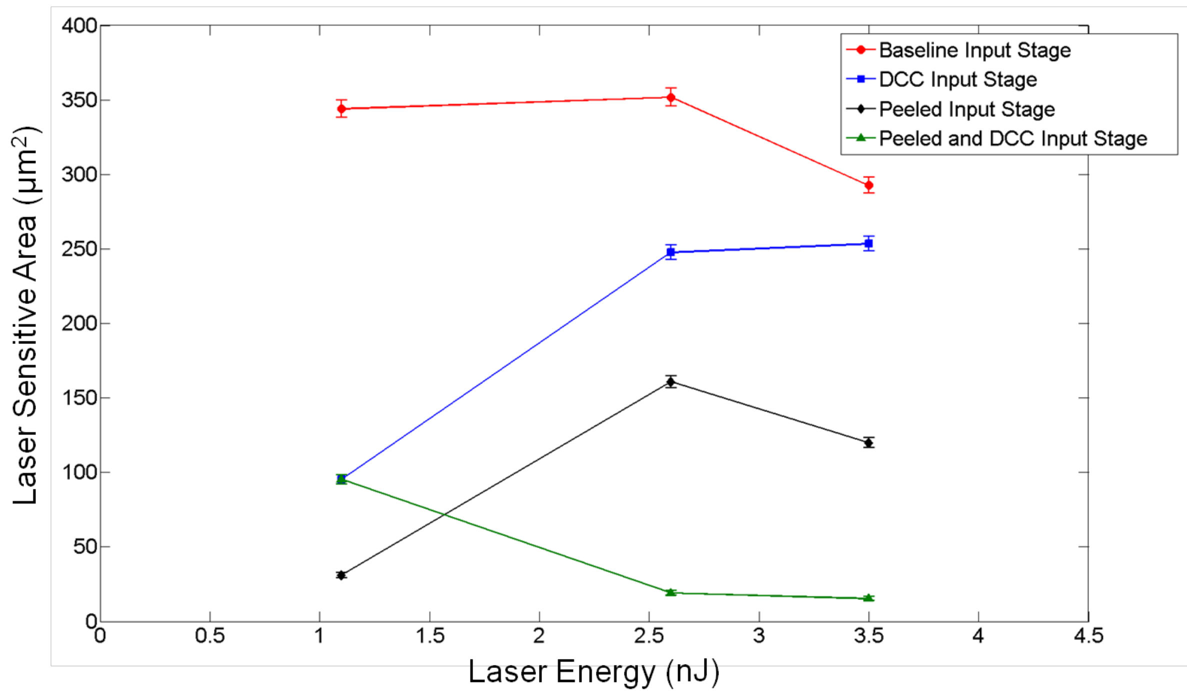


Fig. V-25 Sensitive area versus laser energy for the baseline, DCC, Peeled, and combination layout input stages for an error threshold of 800 ns

that the reduction in sensitive area is significant using any of the three hardening techniques. The combination of the peeled and DCC layout is incredibly effective for all energies. This combination technique reduces the sensitive area by roughly 95% at both the 2.6 and 3.5 nJ laser energies. Even when the combined technique is at its least effective point (laser energy = 1.1 nJ) it reduces the sensitive area of the baseline design by 73%.

A look at the sensitive area of the four different designs calculated as a function of a maximum perturbation threshold is also very informative. This plot of sensitive area for a laser energy of 2.6 nJ is shown in Fig. V-26. For an intended application that has maximum perturbation as its critical error criteria the combination is clearly that best choice. The order of the DCC and peeled input stages has reversed when compared to the sensitive area plot based on settling time. The reduction in sensitive areas for the 20 mV

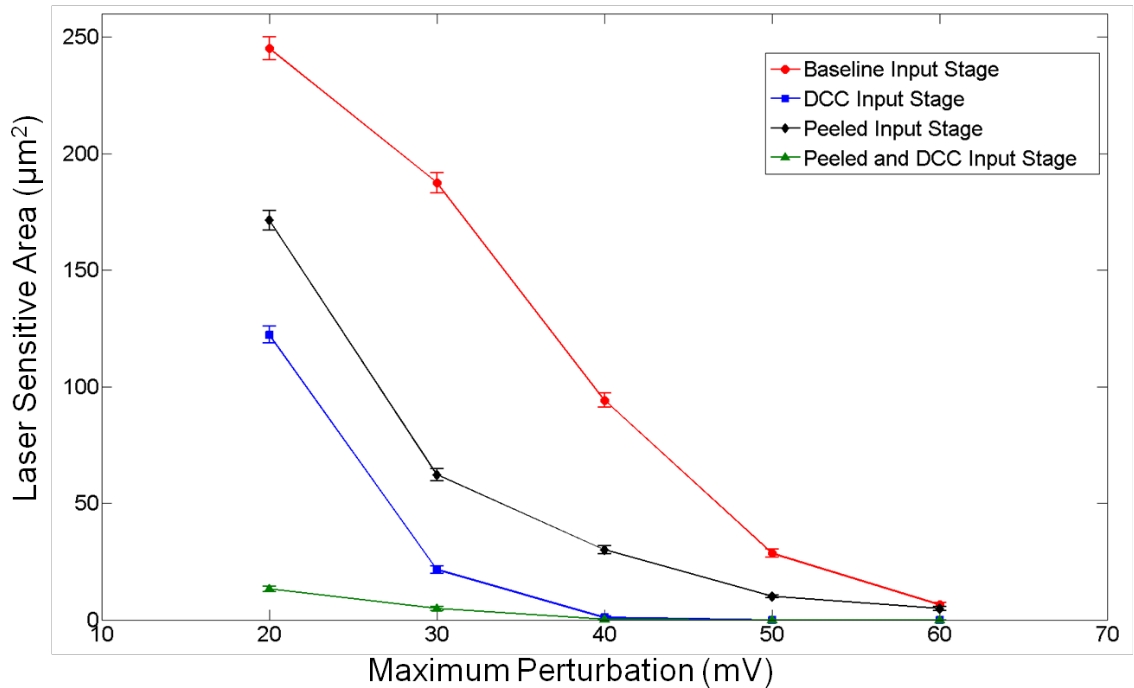


Fig. V-26 Sensitive area versus maximum perturbation threshold plotted for all op amps designs following laser energy strikes of 2.6 nJ

threshold is 36, 54, and 95 % for the peeled, DCC, and combination input stage when compared to the baseline. The reductions in sensitive area for a 30 mV threshold are 67, 89, and 98% for the same designs. The DCC and combination layouts eliminate all sensitive area to thresholds greater than 50 mV and shrink the sensitive area to a 40 mV threshold down to almost negligible amount.

Conclusion

This chapter introduced and experimentally validated a novel SE hardening technique called a peeled layout that falls into a broader RHBD category termed hardened via node splitting. This technique when applied to the input stage of either an SOI or bulk CMOS op amp significantly reduced the circuit's SE vulnerability. The reduction in sensitive area was present for all metrics and typically was greater than 50%.

The larger reductions in SE sensitive area came without electrical penalties and only a minor non-sensitive area penalty. The area penalty in both designs was associated with PDK device and well spacing rules and amounted to less than a 5% increase.

Finally, the peeled layout was combined with a DCC layout. The CMRR of the peeled circuit was proven mathematically to be equivalent to the baseline circuit and then verified experimentally. Combining the two techniques allowed the sensitive area of the baseline design to be reduced by more than 90% versus multiple metrics and for multiple different laser energies.

CHAPTER VI

APPLICATION TO FUNDAMENTAL A/MS CIRCUITS

Introduction

The previous two chapters introduced and experimentally verified SE hardening techniques that can be classified as hardening via charge sharing or node splitting. The hardening techniques of a DCC layout, SNACC, and a peeled layout can be combined as the final experiment in Chapter V illustrated. The previous chapter also demonstrated the versatility of techniques such as a peeled layout in terms of application to target technologies. However, to this point all three of the techniques have been primarily applied to the stages of different op amp designs. A designer has no clear guidance on when to use hardening via charge sharing, node splitting, or both. This chapter will focus on providing this guidance.

An introductory analog circuit course in most universities covers the same group of basic circuits. These basic circuits do not pop up in the curriculums of multiple universities, due to lack of creativity. They are used to teach analog design because of the insight these fundamental circuits can provide. Analog and A/MS circuits in general are often built using a few basic building block circuits. A larger circuit may not be a direct addition of the building blocks, but will almost certainly contain pieces or resemble them.

This concept of understanding the behavior of the basic A/MS building blocks in order to build a solid foundation and intuition on all A/MS circuit will be applied in this chapter. The goal is to analyze these basic circuits in order to determine how they are best

hardened against SEs. The astute reader will then be able to take the guidelines established in this chapter and apply them to harden a much larger array of circuits. The basic building blocks were chosen because they appear in multiple of these introductory type texts and then adapted to fit more modern design, typical of the ones used in the microelectronic circuit industry.

Hardening of A/MS Building Block Circuits

A cascode current sink, depicted in Fig. VI-1, is the first fundamental building block examined. Cascode current sinks are popular in modern A/MS design because of their high output resistance and relative insensitivity to load and transistor-to-transistor parameter variations. The investigation of this circuit and all of the other fundamental building blocks will follow a similar process.

This investigation process used in this chapter will encompass extensive simulations using the Cadence Spectre environment, the IBM CMRF7SF process, and the ISDE bias dependent SE model described in chapter three. Nodal analysis simulations were run for each building block circuit using the bias dependent models for normal incidence strikes with LETs of 10, 20, 30, 40, and 50 MeV-cm^2/mg. The outputs of each building block circuit were set up in order to measure an output voltage. Each circuit's individual set up and specifications were different and will be discussed in detail in the appropriate section.

Cascode Current Sink

The cascode current sink was designed with a PMOS current source (1 µm x 0.5 µm) providing i_{in} and the output current (i_{out}) was running through a resistor to establish

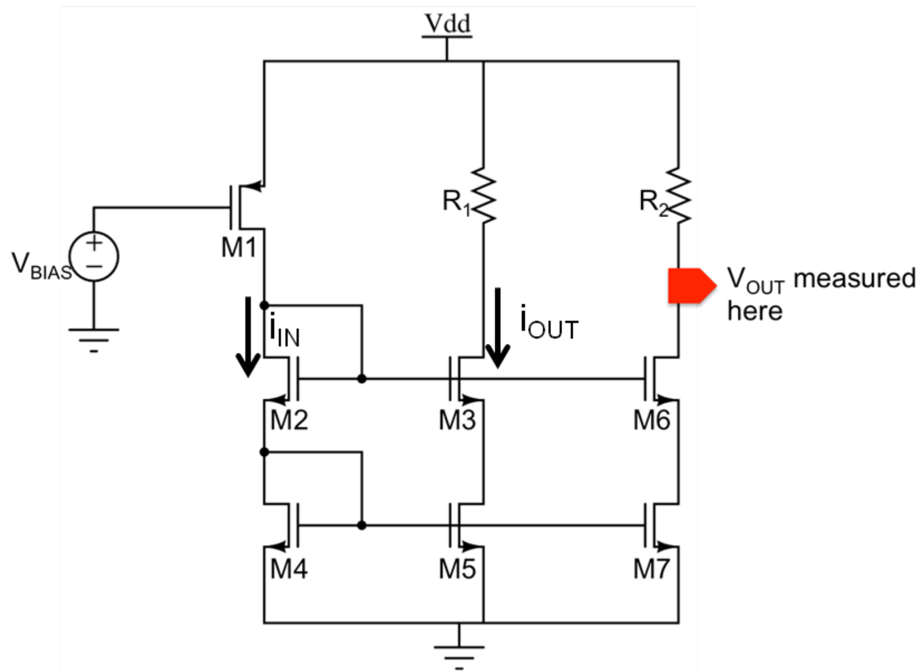


Fig. VI-1 Cascode current sink investigated as a fundamental A/MS building block

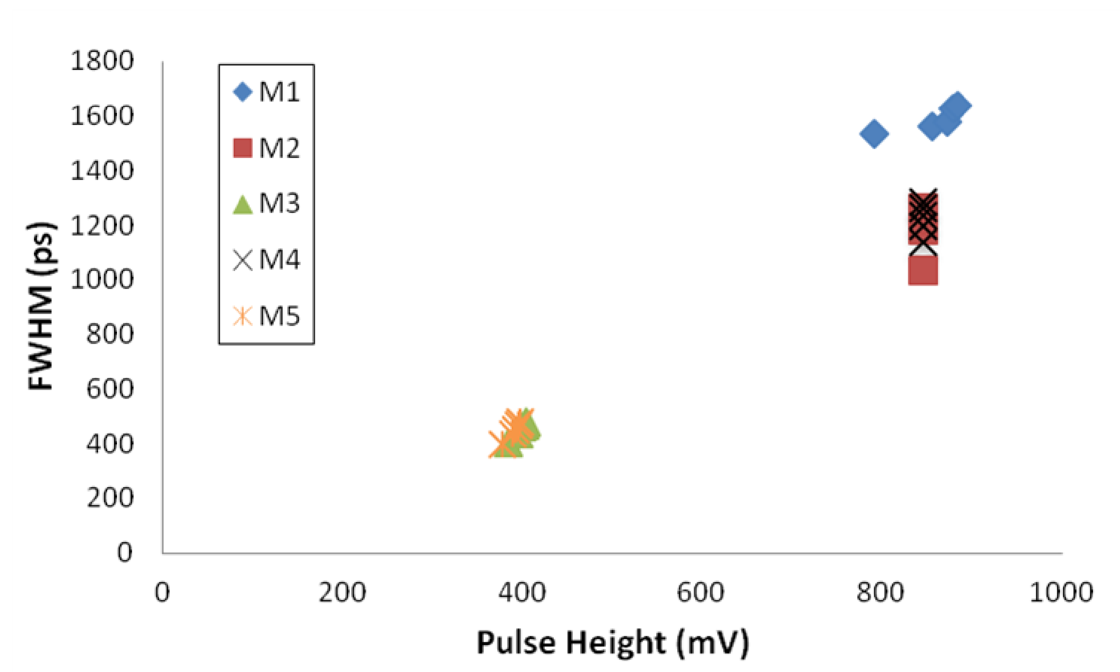


Fig. VI-2 A nodal analysis of the circuit shown in Fig. VI-1 with strikes on every node of 10-50 MeV-cm2/mg in increments of 10

a node voltage. Transistors M2 and M4 were mirrored off to identical devices with a resistor load, to allow the output to be measured on a non-struck node. The NMOS devices have dimensions of 5 µm x 0.5 µm and a quiescent current of 33.8 µA.

Fig. VI-2 contains the results of this nodal analysis plotting pulse height versus the full width half max (FWHM) of the pulse. Each node was struck five times, once for each LET between 10 and 50 MeV-cm^2/mg in increments of ten. This plot depicts all of those data points with pulse height and/or width increasing with LET. The transistors on the left leg of the circuit (M1, M2, and M4) are clearly the most sensitive to SEs. The vertically stacked nature of the data points is due to the transient hitting the voltage rail. This pattern of sensitivity on a fairly static circuit appears to be a good candidate for some form of SNACC hardening.

Fig. VI-3, depicts the basic six-transistor implementation of SNACC hardening added to the current sink in. The idea of this hardening is to protect the current source device, M1 and device M2. If an ionizing particle strikes on or near device M1 and both it and S4 collect charge, then ideally an equal current would be sourced and sunk through M1 and S6 (because of S4) respectively. The current mirror structure would enable S5 to remove the unwanted current sourced by M1 from the node, therefore mitigating the SE. Transistor M2 is protected in the same manner, with the charge sharing required between S3 and M2. The charge sharing is facilitated by a DCC layout between the appropriate devices.

Fig. VI-4 contains the pulse height and FWHM of perturbations created following SE strikes to M1 and M2 with and without the SNACC hardening. Similar to the nodal

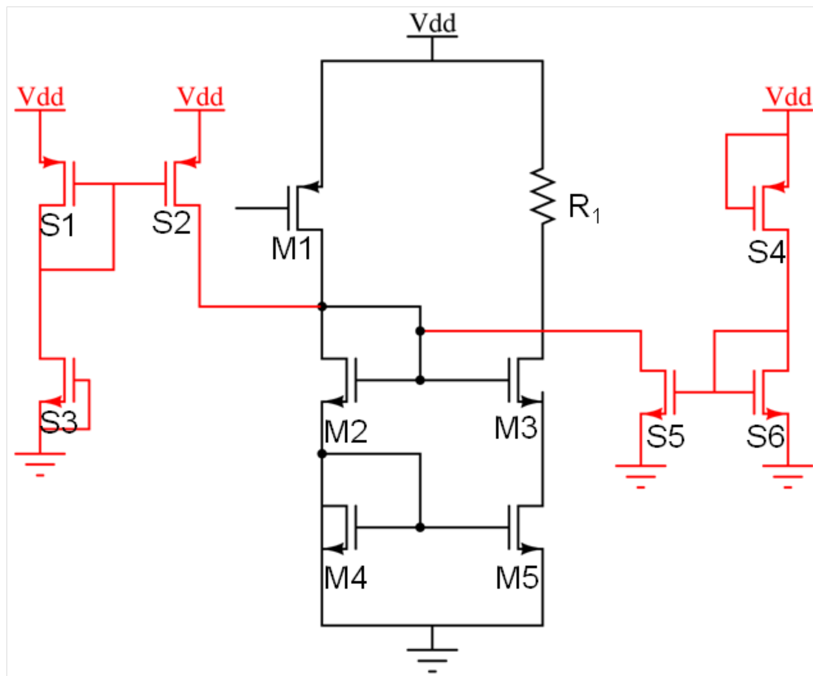


Fig. VI-3 The six-transistor implementation of SNACC applied to protect the drains of M1 and M2.

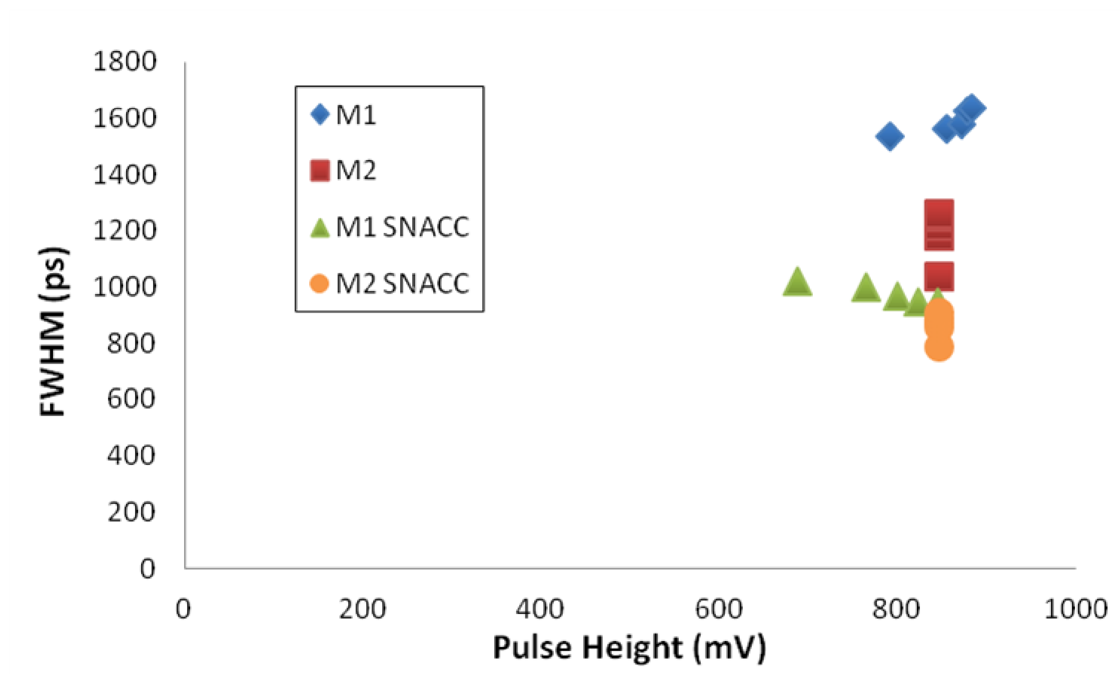


Fig. VI-4 Results of strikes to the drains of devices M1 and M2 with and without SNACC hardening for LETs ranging from 10 to 50 MeV-cm^2/mg in increments of 10

analysis plot there are five points for each node, each corresponding to an LET between 10 and 50 MeV-cm^2/mg in increments of ten. The data in Fig. VI-4 illustrates that the SNACC hardening does a fairly good job reducing the duration of the perturbations, up to an approximate 45% reduction in FWHM following a strike of 50 MeV-cm^2/mg to M1.

While the use of SNACC hardening does produce significant reductions in pulse widths, it does not significantly reduce their magnitudes. When using the six-transistor implementation of SNACC a designer must discern whether or not the added sensitive area is worth the SE mitigation achieved. One way to do this is through a layout aware SE model, such as the one described in [41]. However, in this case before considering the additional area it is a good idea to see if another hardening technique provides better results rendering the layout aware simulations unnecessary.

There is not a differential component to this circuit or an inherent mirror architecture that would imply the DCC or another implementation of SNACC would be beneficial. Simulations were performed to see if charge sharing could be leveraged through a DCC layout and in most cases it made the SE response worse. However, a peeled layout might be useful. The cascode current sink was peeled into two current sinks, each half the original size and summed on the mirrored output node. The electrical performance of this circuit is identical. Fig. VI-5 contains the results of a nodal analysis of the peeled circuit for all five LETs. In this figure, the baseline results are the solid shapes and the peeled results are the same color and shape, but outlines. The data in this figure clearly shows that a peeled layout significantly reduces the FWHM, pulse height, or both of every node in the circuit. The reductions in pulse height for nodes M2 and M4, two of the most sensitive, are on the order of 50%. The peeled circuit significantly

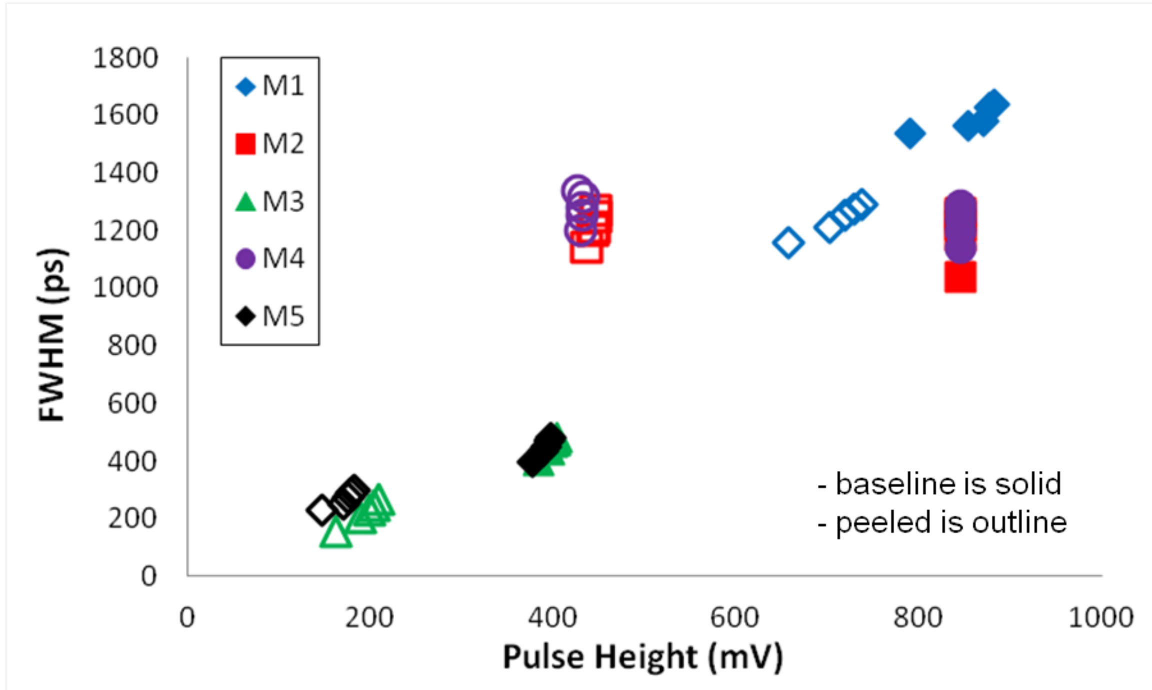


Fig. VI-5 FWHM versus pulse height for the baseline current sink (solid shapes) and the peeled current sink (outline) for all 5 simulated LETs

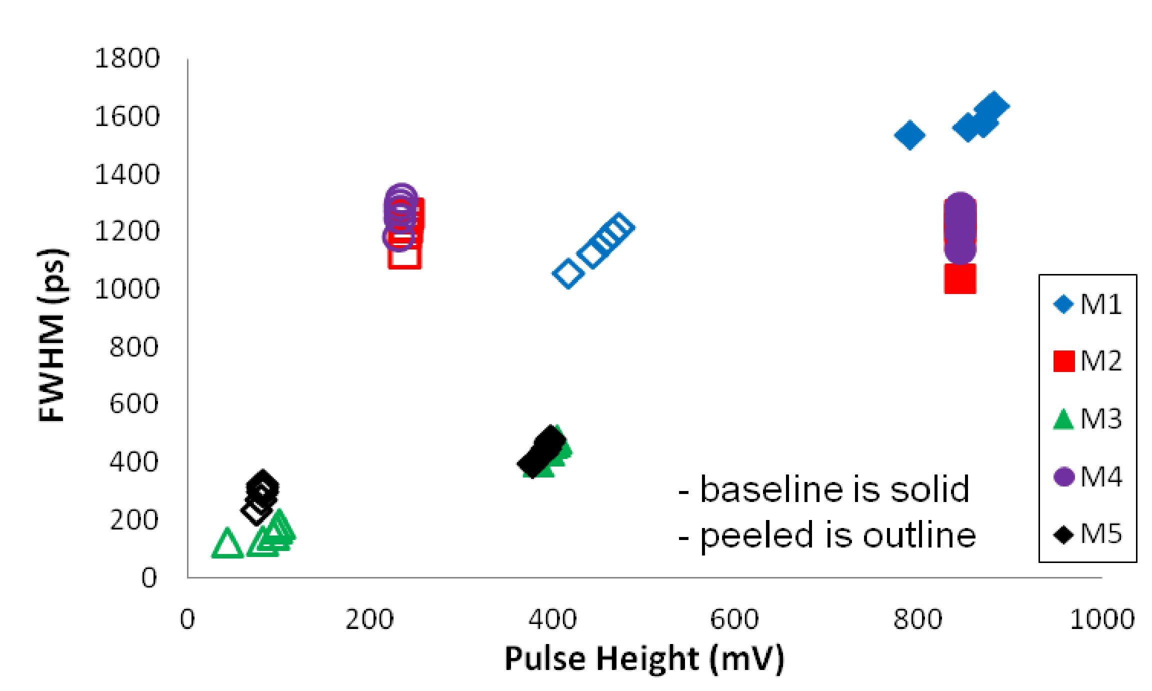


Fig. VI-6 FWHM versus pulse height for the baseline current sink (solid shape) and the current sink peeled into four parallel circuits

reduces the perturbations following strikes of all LETs, to all nodes.

A circuit with large enough devices could possible be peeled into more than two parallel copies. Fig. VI-6 contains the results of simulations of the baseline versus a peeled copy with four parallel paths. Comparing Fig. VI-5 and Fig. VI-6 shows that peeling of the baseline circuit into more than two copies yields even better SE immunity at every node. The reduction in the pulse height of the most sensitive node (M2 and M4) is approximately 75%, when peeled into four parallel paths. The limit on peeling a circuit will be set by the device sizes and PDK limits on sizing of unit cells. The other important parameter is the ability to maintain well potential. If circuits are peeled into multiple small copies additional well contacts may be needed to prevent well collapse.

Figure VI-7 is a comparison of all of the hardening techniques applied to the baseline current sink following strikes to every node with an LET of 30 MeV-cm^2/mg. The baseline (square) is very sensitive, but the DCC layout actually makes the circuit more sensitive in this case. The circuits hardened by SNACC and the twice peeled variant both reduce pulse width, but the peeled version decreases the pulse height and the widths to a much greater degree.

This simulation study showed that up to a 25% reduction in pulse width could be achieved by hardening a cascade current sink with the six-transistor implementation of SNACC. This technique however requires the addition of sensitive area to the circuit and is not the best hardening choice. A peeled layout (4 parallel copies) can reduce the perturbation pulse height by up to 73% without the addition of any sensitive area and is the best choice for this type of circuit. It is important to point out that the output was measure on a mirrored node and not a struck node.

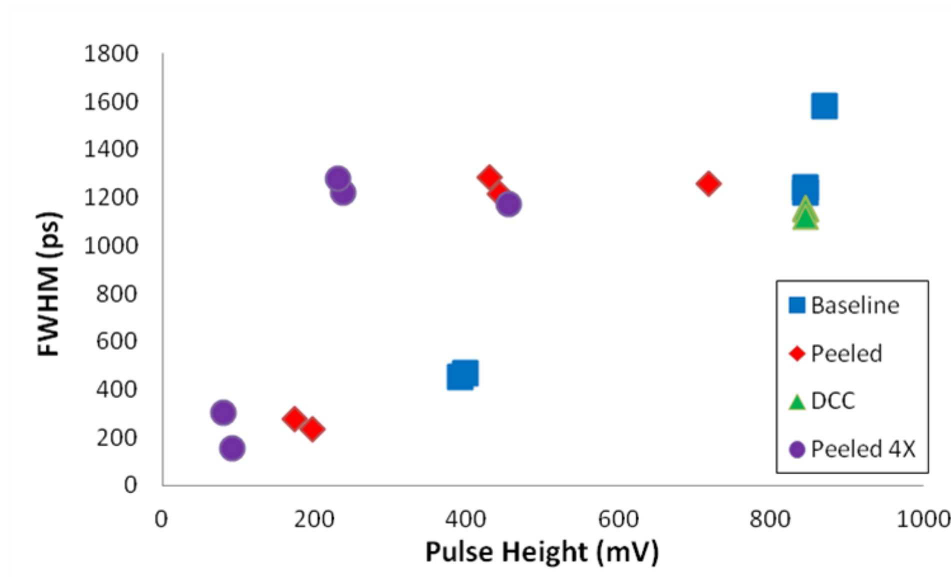


Fig. VI-7 Comparison of the FWHM versus pulse height for the baseline circuit and the circuit hardened with each of the three hardening technique following strikes of 30 MeV-cm^2/mg to every node

Regulated Cascode Current Mirror

The second building block circuit investigated was a regulated cascode current mirror, shown in Fig. VI-8. This circuit makes improvements on other advanced current mirrors, such as the Wilson Current Mirror, by further increasing the output resistance. The current mirror for these simulations was designed with M1 and M2 as 20 by 0.5 µm devices, M3 was 2 by 0.5 µm, the PMOS current source was 2 µm by 0.5 µm with a 20 kΩ resistor, and a quiescent current of 42 µA.

Fig. VI-9 contains the results of a nodal analysis of the baseline circuit. Each node of the regulated cascode current mirror was struck five times with LETs ranging from 10-50 MeV-cm^2/mg in increment of ten. Following the simulated SE strike the output node, marked in Fig. VI-8 was monitored for the perturbation pulse height and width. A significant difference between this circuit and the previously discussed current sink is that the output is being measured on a struck node. Fig. VI-9 indicates that the right leg of the

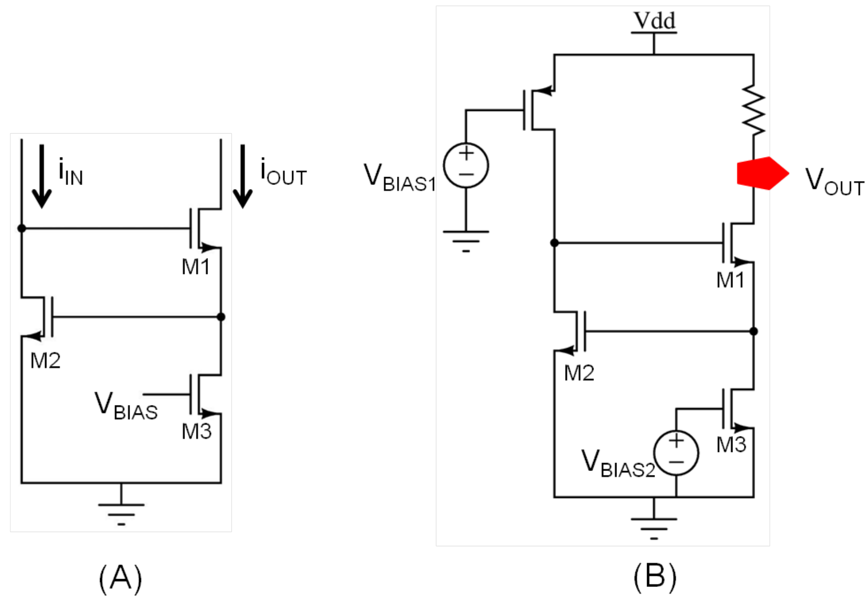


Fig. VI-8 The second A/M building block studies, a regulated cascode current mirror (a) and its simulation configuration in (b)

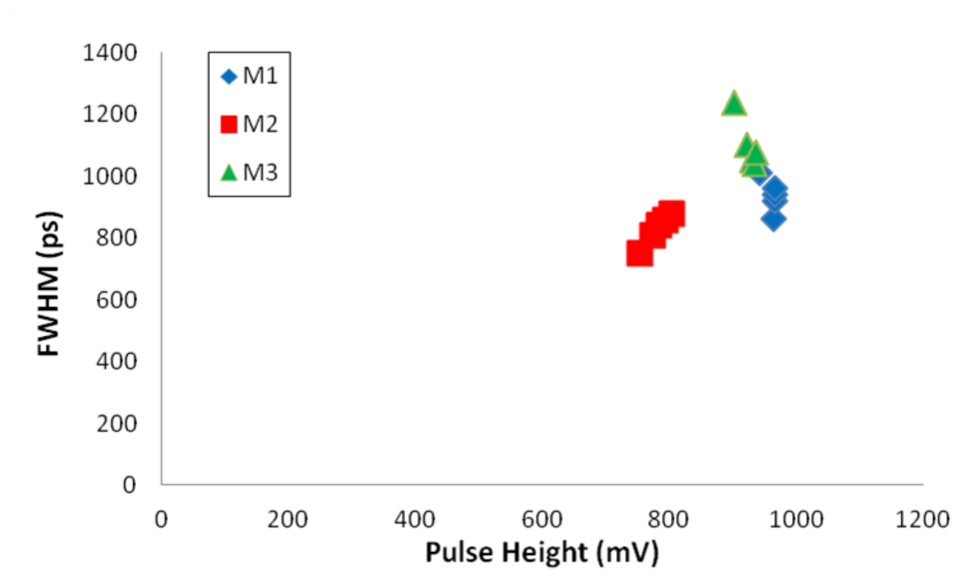


Fig. VI-9 Results of a simulated nodal analysis of the regulated cascode current mirror shown in Fig. VI-8 following simulated strikes to every node for LETs ranging from 10 to 50 MeV-cm^2/mg

circuit (M1 and M3) is slightly more sensitive than M2. This fact and because the circuit is fairly static in nature indicate that it is an ideal candidate for SNACC hardening. However, there is not a clear sensitive junction (all are sensitive) to target with the six-transistor implementation of SNACC. For the purposes of this study SNACC was applied to every junction independently to test its performance. In all cases the six-transistor implementation of SNACC improved the SE performance. Some of the highlights were a decrease in pulse height of approximately 60 mV following strikes to M2, a reduction in pulse width of 200 ps following strikes to M1, and finally close to a 500 ps reduction in pulse width following strikes to M3. These reductions are important, but most likely do not justify the increase in sensitive area to such a small circuit.

The regulated cascode current mirror can be peeled and summed on the node below the resistor. As with the previous circuit the current mirror can be peeled into two parallel copies or more. Fig. VI-10 compares the results of the baseline versus the peeled circuit into two parallel paths (a) and 4 parallel paths (b) for all five simulated LETs. The baseline results are shown as solid shapes and the peeled results as outlines. The peeled layout variants significantly reduce the perturbation heights. The maximum perturbation in the 4x peeled circuit is reduced nearly 600 mV, 200 mV, and 10 mV following 50 MeV-cm^2/mg strikes to nodes M2, M3, and M1 respectively. In a few cases the pulse are elongated. As an example, the 200 mV reduction following 50 MeV-cm^2/mg strikes mentioned above increased the pulse width by 600 ps. This is not overly surprising and relatively consistent with the experimental results presented in the previous chapter. The fact that a peeled layout is not significantly helping the measured node is also something that will become a pattern through the rest of this study.

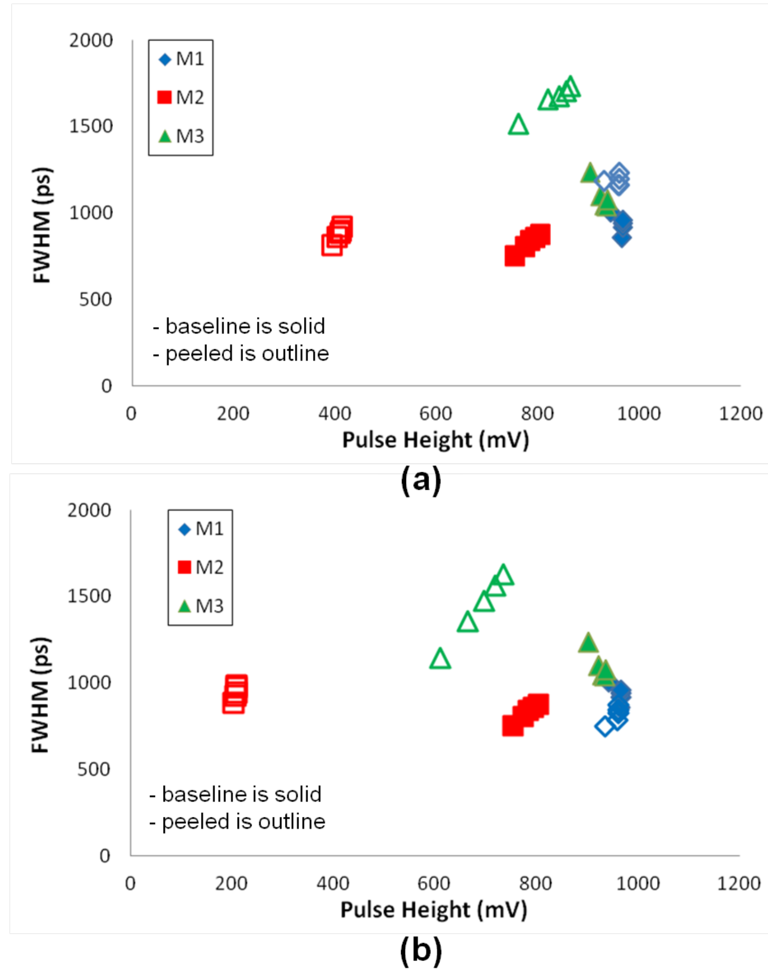


Fig. VI-10 Simulation results comparing a peeled (2x (a) and 4x (b)) versus baseline regulated cascode current mirror following strikes of 10-50 MeV-cm^2/mg

The regulated cascode current mirror does not have a differential component to it, so there is no reason to believe that a differential charge cancellation process will harden the circuit. However, as shown in the discussion of the experimental SNACC results (Chapter IV) charge sharing can be encouraged via a DCC layout to promote other mechanisms. In the case of this circuit a DCC layout between M2 and M3 significantly reduces the error response of M3. Fig. VI-11 illustrates this point. The change in layout does little to the response of strikes to M2, but the durations of perturbations following strikes to M3 are reduced by upwards of 85 % in some cases. The mechanism that

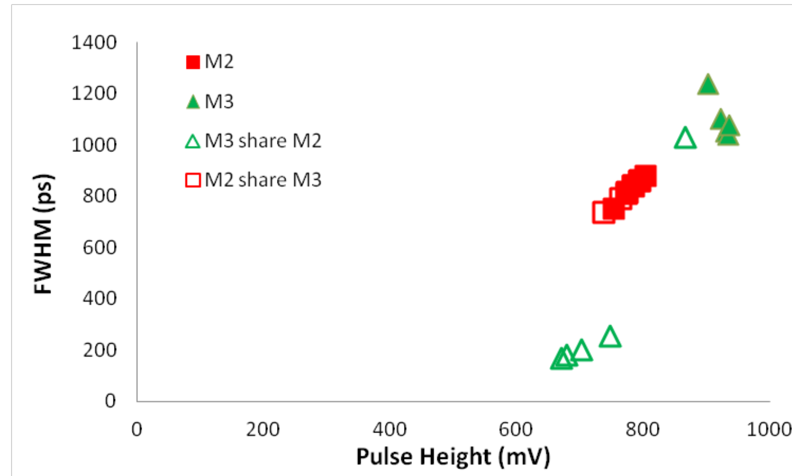


Fig. VI-11 FWHM versus pulse height following strikes of all five simulated LETs comparing the baseline response with the response of a circuit with a DCC layout

causes this is a pseudo differential gain path allowing for a common-mode type rejection. Device M2 creates a non-inverting gain path between the drains of M3 and M1. However, a strike on M2 has an inverting gain path to drain of M1, the output node. If a strike occurs on M3 and it is shared with the drain of M2, then the inverting path to the output node on M1 will help to mitigate the effects caused by M3 sinking the excess current.

In summary, all three hardening techniques work to some extent in hardening the regulated cascode current mirror. SNACC reduces the expected pulse widths by up to 42% for strikes to M1, 51% for M2, and 48% for M3. However, considering the other options these reductions come at to steep a price in terms of additional sensitive area for SNACC to be the best choice. A DCC layout creates a pseudo differential like hardening when applied to devices M2 and M3. This layout change can create up to an expected 5% reduction in pulse height following strikes to M2 and an 85% reduction in pulse duration following strikes to M3 without any major penalty. Finally, a peeled layout can achieve

up to a 10% pulse width reduction following strikes to M1, 65% reduction in pulse height for M2, and 17% reduction in pulse height for M3. The DCC layout and peeled layout can be combined for greater effect and can be achieved with only a marginal non-sensitive area penalty, associated with the peeled layout spacing requirements.

Bootstrap Current Source

A bootstrap current source, sometimes referred to as a V_T referenced current source, is a popular design because to first order its reference current is independent of V_{DD}. In the case of the bootstrap current source studied in this work, shown in Fig. VI-12, the quiescent current is set by the convergence of the voltage drop across R_2 and gate source voltage of device M6. The operating current for the design used in this work was set at 29 μA by making the PMOS devices 75 x 0.5 μm, M5 and M6 5 x 0.5 μm, and setting R_2 to be 15 kΩ.

Fig. VI-13 is a SE nodal analysis of the baseline current source plotting pulse height versus pulse width for LETs ranging from 10-50 MeV-cm^2/mg in increments of 10. This plot shows that M3 and M5, constituting the right leg of the circuit in Fig. VI-12. is much more sensitive than the left. So much so, that the perturbations following SE strikes of 10 MeV-cm^2/mg to the right leg are larger than 50 MeV-cm^2/mg to the left. This fact coupled with previous research on a similar circuit [56], would indicate that this circuit is a perfect candidate for SNACC hardening.

Fig. VI-14 shows a schematic of the six-transistor implementation of SNACC applied to the current source (a) and the results of simulated SE strikes to unprotected and SNACC protected junctions (b). This implementation of SNACC works just like previous applications. If M3 is struck by an ionizing particle and shares charge with S6,

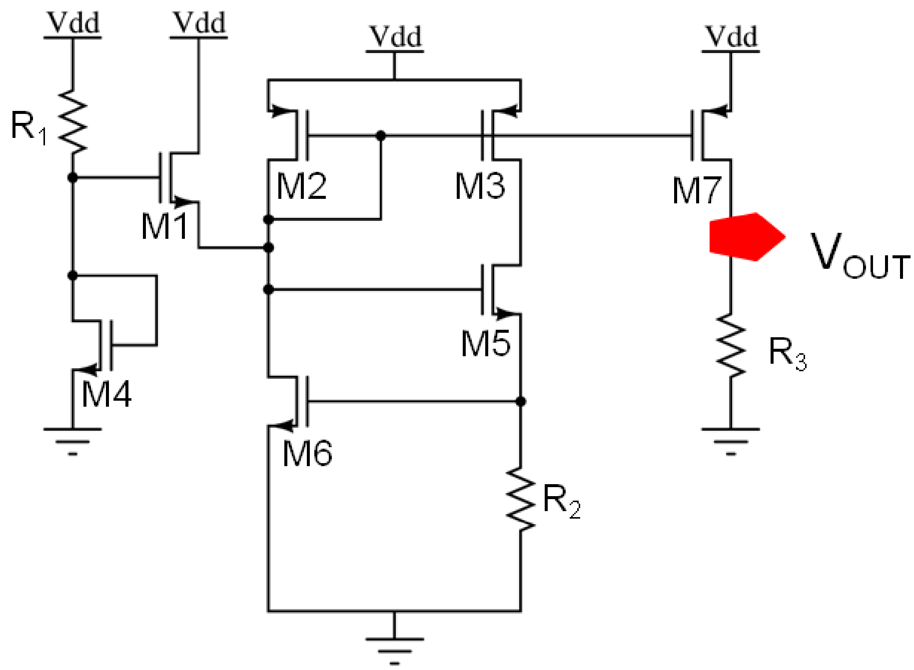


Fig. VI-12 Bootstrap current source studied in this work as one of the fundamental A/MS building blocks

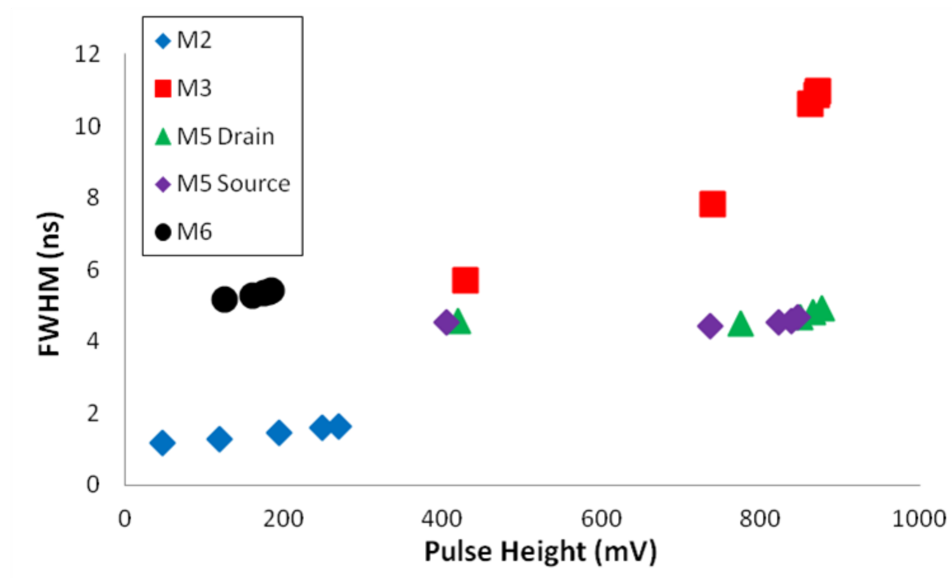
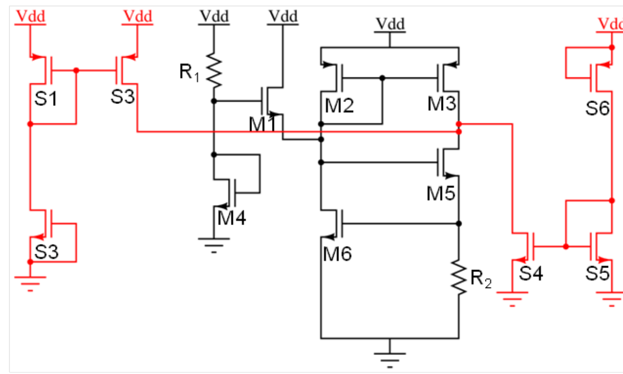
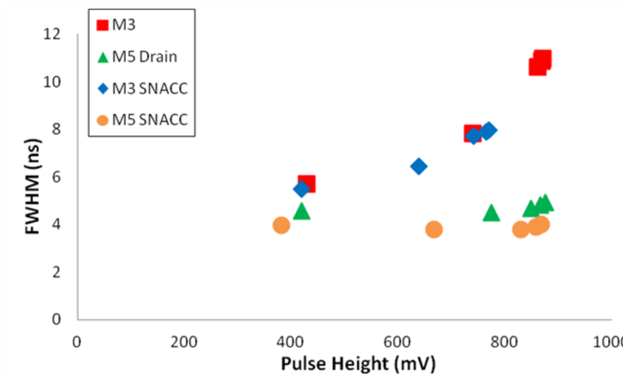


Fig. VI-13 Nodal analysis of the bootstrap current source shown in Fig. VI-11 for all five simulated LETs 10-50 in increments of 10 MeV-cm^2/mg



(a)



(b)

Fig. VI-14 (a) Schematic of the six-transistor implementation of SNACC applied to the bootstrap current source of VI-11 and (b) simulated SE results for all five LETs following strike to the protected and unprotected nodes

then S6 will sink that charge (current) and through the current mirror, S4 will remove the unwanted SE charge from the protected node. The device labeled M5 is protected in the same manner, by sharing charge with device S3. Comparing the results of SE strikes to the baseline M3 and SNACC protected M3 shows that SNACC is fairly effective in reducing both the pulse magnitude and widths. The reduction in error pulse heights, range from 2% for an LET of 10 MeV-cm^2/mg to 15% for an LET of 50 MeV-cm^2/mg. The range of reduction in pulse widths, range from 31% to 30% for the same LETs. These reductions are significant, but as with other versions of the six-transistor implementation of SNACC considered in the simulation portions of this dissertation, it does not account

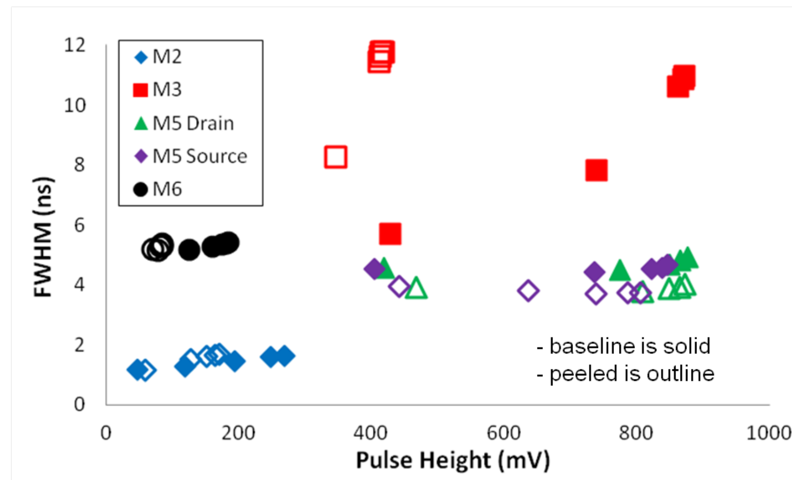


Fig. VI-15 Nodal analysis of the bootstrap current source baseline versus a peeled current course for all five simulated LETs 10-50 in increments of 10 MeV-cm^2/mg

for the additional sensitive area. Before extensive effort is placed into layout aware simulations the other hardening techniques should be explored to determine if SNACC is the best choice for hardening.

Fig. VI-15 contains the simulated SE results from strikes to every node in the baseline and a peeled version of the current source for all 5 LETs. The peeled version is a single peel (two parallel circuits) and is effective at reducing the pulse heights for every node. It is only moderately effective at hardening the two sensitive junctions of device M5. As is the case with other peeled layouts, the pulse width results are mixed, with the peeled layout extending them in some cases. The results for mitigating the perturbation following strikes to M3 are very encouraging, but device M5 still needs to be addressed.

There is not an explicit differential component to this circuit, but this dissertation includes multiple examples of a DCC layout being effective in similar circumstances. In order to determine if a DCC layout could help mitigate the response of device M5 multiple charge sharing simulations were performed for various combinations. A result

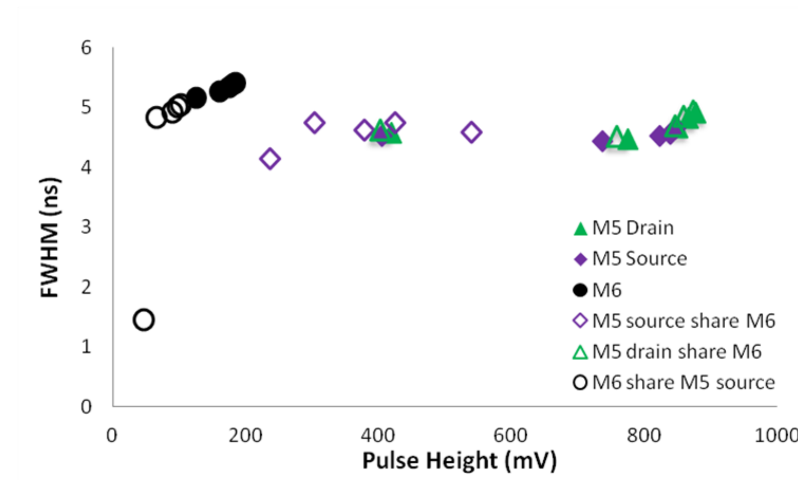


Fig. VI-16 Pulse height versus width results for the baseline bootstrap current source and various charge sharing scenarios involving device M5 and M6 for all 5 simulated LETs

from this simulations study is shown in Fig. VI-16. This result compares the baseline results with various combinations of charge sharing between devices M5 and M6. The figure clearly shows that sharing between the source of M5 and M6 is advantageous to the SE response. Using a DCC layout configuration encouraging charge sharing between the source of M5 and M6 reduces the error pulse height following a normal incidence 50 MeV-cm^2/mg strike to M5 by 73%. The width of the reduced pulse is also 40% shorter than the baseline. These results are outstanding and can be explained in the same manner as the regulated cascode current mirror previously discussed. Careful inspection of the two circuits indicates that same inverting and non-inverting signal paths exist in this circuit. Previously studied circuits also prove that this charge sharing hardening mechanism can be combined with the peeled layout to gain further SE immunity.

Fig. VI-17 is plot of pulse height versus width of the baseline design and a peeled version that has a DCC layout between the source of M5 and M6 for all five simulated LETs. Comparing this result to the results of the peeled layout only in Fig. VI-14

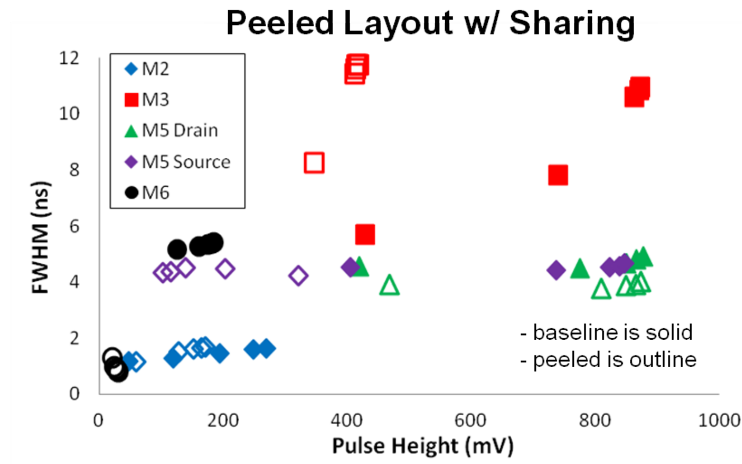


Fig. VI-17 Pulse height versus duration of the baseline current source an the peeled current source that has a DCC layout between the source of M5 and M6 for all five simulated LETs

demonstrates the effectiveness of combining the two hardening techniques. The magnitudes of perturbations following strikes to the source of M5 are reduced by 88% when compared to the baseline. Interestingly enough the DCC layout of the peeled circuit reduces the perturbation of the DCC layout only by more than 50%. Another very important benefit of the combined techniques is the reduction in pulse width following strikes to M6. At an LET of 50 MeV-cm^2/mg the pulse width is reduced by 85%. These increases in SE hardness are achieved with only the addition of a small non-sensitive physical area.

In summary, all three hardening techniques are effective when used on the bootstrap current source. Using SNACC, a designer could expect to see up to a 15 and 30% reduction in pulse width and pulse height following strikes to M3 and a 20% in pulse widths following strikes to the drain of M5. This technique does require the addition of sensitive devices (although also compensated for) and is not the best option. The DCC and Peeled layout techniques are each very effective in mitigating the SE

response of the circuit and are even more effective when combined. Combining these techniques a designer could expect to see a reduction in SE transient pulse height of 37, 56, 1, 85, and 55% following SE strikes to devices M2, M3, the drain of M5, the source of M5, and M6 respectively. The penalty associated with combining these techniques is only a minor non-sensitive area addition due to PDK device spacing rules.

Active Load Inverting Amplifier

Single-stage amplifiers are almost universally one of the first analog circuits that students encounter. There are multiple reasons for this, but mainly because they are often used in practice and can provide insight into more complicated circuits. This is why their SE response is of value to the design community and why they are studied in the next few subsections. The first single-stage amplifier explored is an inverting amplifier with an active load, shown in Fig. VI-18.

The amplifier in this study was designed as a true analog inverter with unity gain. This was accomplished by sizing M1 and M2 as 14 x 0.5 μm and 2.5 x 0.5 μm respectively. The quiescent current of the amplifier was 26.6 μA. A SE nodal analysis of this circuit for LETs ranging from 10 to 50 MeV-cm^2/mg in increments of 10 is shown in Fig. VI-19. This figure demonstrates that both junctions are extremely sensitive and actually hit the voltage rails following SE strikes (600 and 1200 mV).

The six-transistor implementation of SNACC is not an option for circuits that have bandwidth as a critical parameter due to the additional capacitance created by the added devices. The presence of only a single NMOS and PMOS device also precludes the use and investigation of a DCC layout. The only possibly applicable hardening technique of the three is a peeled layout. Investigation of a single peel proved to be ineffective.

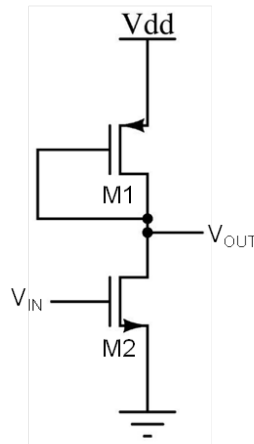


Fig. VI-18 The active-load inverting amplifier investigated as a fundamental A/MS building block

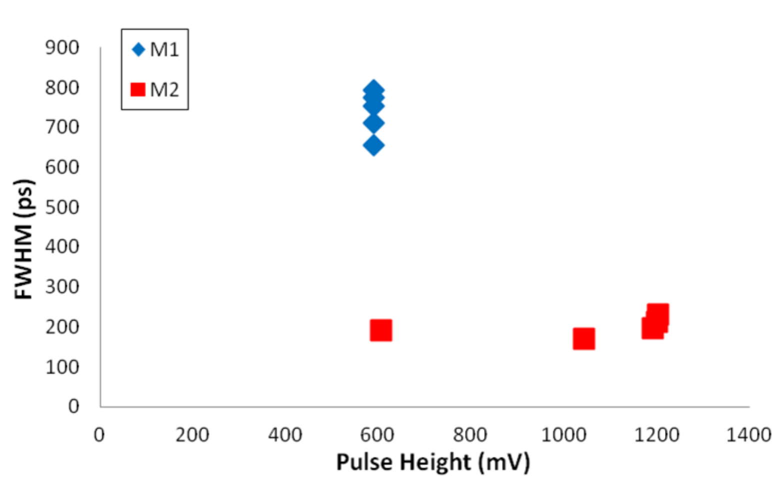


Fig. VI-19 SE nodal analysis of the amplifier depicted in Fig. VI-17 following SE strikes to both junctions of all five simulated LETs

However, this amplifier has fairly large devices and can be peeled into more than two parallel circuits. Fig. VI-20 contains the results of a nodal analysis comparing the response of the baseline amplifier and the amplifier peeled into four parallel paths. These results are not overwhelming, but the peeled layout was able to prevent strikes to M2 causing the output to hit the power rail. There also was a reduction in SE transient pulse height of 6% following strikes to M1.

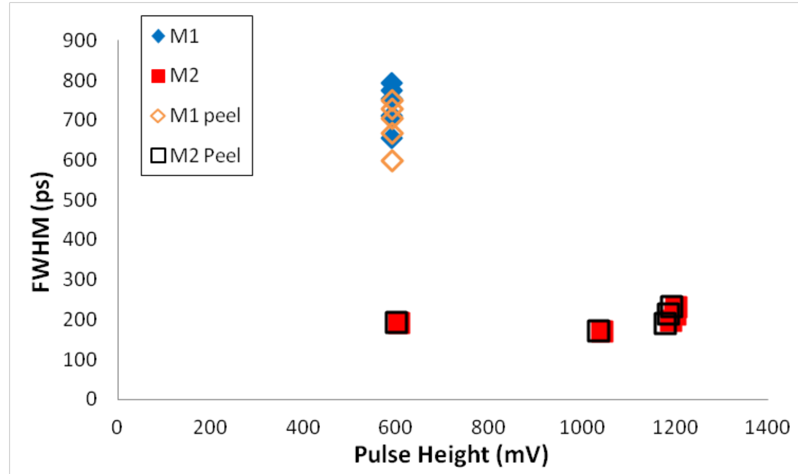


Fig. VI-20 SE nodal analysis of the baseline amplifier and amplifier peeled into four parallel paths for all five simulated LETs

Overall, the hardening of this amplifier was not very effective, but it did improve the response some. The study of the circuits in this dissertation has and will continue to reveal that a peeled layout is least effective in mitigating the response of the measured node. In the case of this circuit, the measured node is of course the only node.

Push-Pull Amplifier

The push-pull amplifier, such as the one depicted in Fig. VI-21 is a common circuit because of its wide output range. These circuits can often be used as buffers, without sacrificing any of the circuit's operating range. The 32 nm op amp described in chapter three of this work had a buffer of this fashion.

The push-pull amplifier studied in this section was designed with a gain of 31 dB and a bandwidth (f_{-3dB}) of 320 MHz. In order to achieve these specifications the devices were sized 14 x 0.5 and 3 x 0.5 μm for the PMOS and NMOS devices respectively. The quiescent current of the amplifier was 179 μA. The results of a nodal analysis of this

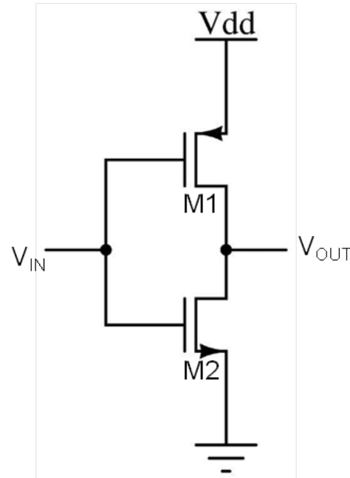


Fig. VI-21 Push-pull amplifier studied in this dissertation as one of the fundamental A/MS building blocks

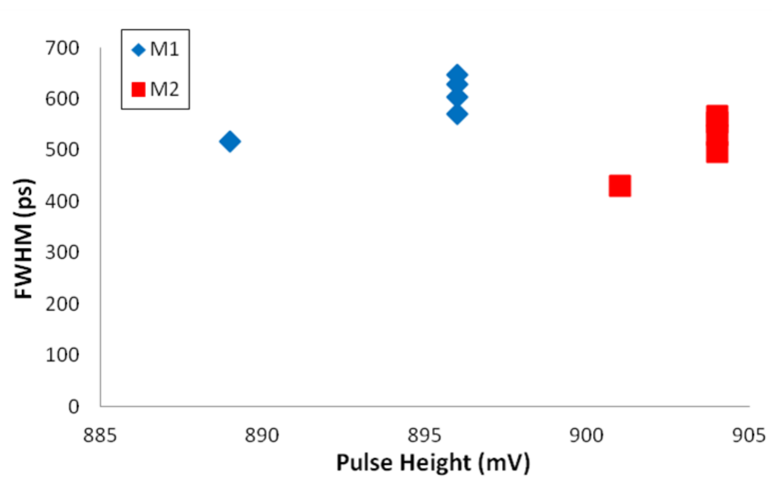
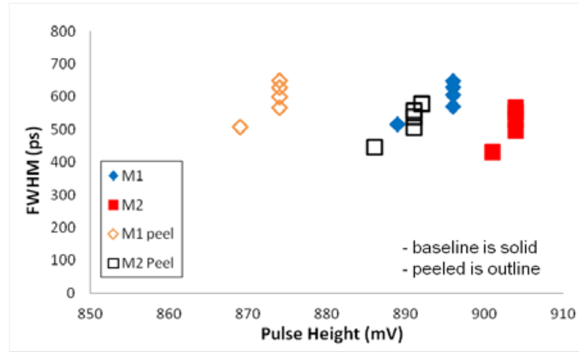


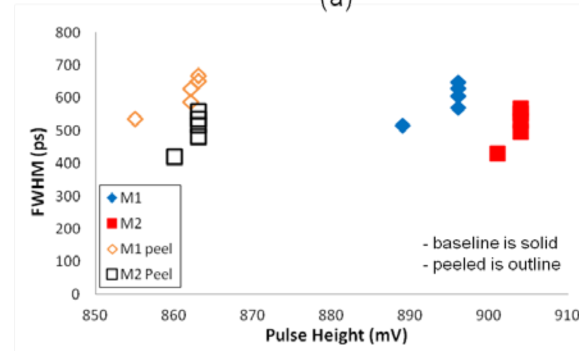
Fig. VI-22 Nodal analysis of the push-pull amplifier displayed in Fig. VI-20 of normal incidence strikes of all five simulated LETs

circuit for all five simulated LETs is shown in Fig. VI-22. Strikes to either device cause the output node to pin to the power rail at LETs larger than 10 MeV-cm^2/mg.

This circuit, like the previous amplifier is not a good candidate for SNACC hardening due to its dynamic nature and bandwidth sensitivity to added capacitance. Also, like the previous amplifier this circuit only has a single NMOS and PMOS transistor, therefore a DCC layout is not possible. These limitations in hardening



(a)



(b)

Fig. VI-23 The SE response of the baseline, peeled (a), and four parallel path (b) version of the push-pull amplifier for all five tested LETs

constrain a designer armed with the tools presented in this dissertation to a peeled layout. This circuit like many A/MS circuits is designed with large devices that can be peeled more than once. Fig. VI-23 contains the simulation results of the baseline versus the peeled amplifier (a) and versus a version with four parallel paths in (b). The peeled layout improves the circuit's SE response in terms of pulse height for both a single peel and the double peel versions. The improvements are modest, but a designer can expect a 4 and 5% reduction in pulse heights following strikes to M1 and M2 respectively using a peeled layout. This improvement in performance comes at the expense of only a small amount of additional non-sensitive area associated with PDK rules for device spacing.

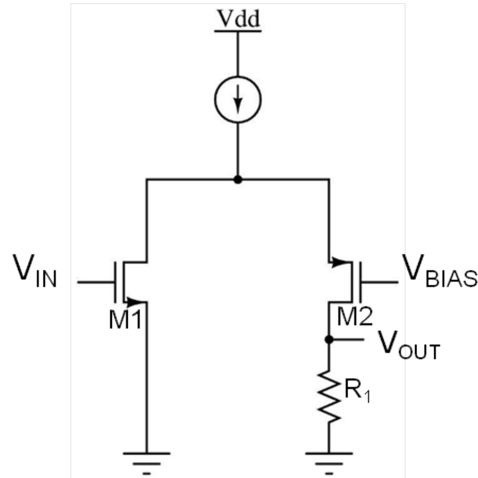


Fig. VI-24 The folded cascode amplifier design studied in this work as one of the A/MS fundamental building blocks

Folded Cascode Amplifier

A cascode amplifier is composed of the combination of two single-stage amplifiers the common source and common gate. These single-stage amplifiers can be of different types (ie. PMOS and NMOS). These amplifiers are combined to maximize the benefits of each of the individual amplifiers and result in an amplifier with a high output resistance and hence gain. The amplifier studied in this work, shown in Fig. VI-24 has a gain of 10 dB and a bandwidth of 1.1 GHz (f_{-3dB}). These specifications are achieved by sizing the devices as 2.5 x 0.5, 14 x 0.5, and 6 x 0.5 μm for M1, M2, and M3 respectively. The quiescent current is 215 μA.

Fig. VI-25 is a nodal analysis of the baseline circuit, plotting transient pulse height versus pulse width following simulated strikes ranging in LET from 10 to 50 MeV-cm^2/mg in increments of 10 to each sensitive junction. Even though this circuit is a low gain high bandwidth design (high current) it is still very sensitive to SEEs with strikes to two of the junctions pinning the output at the power rail for almost all LETs.

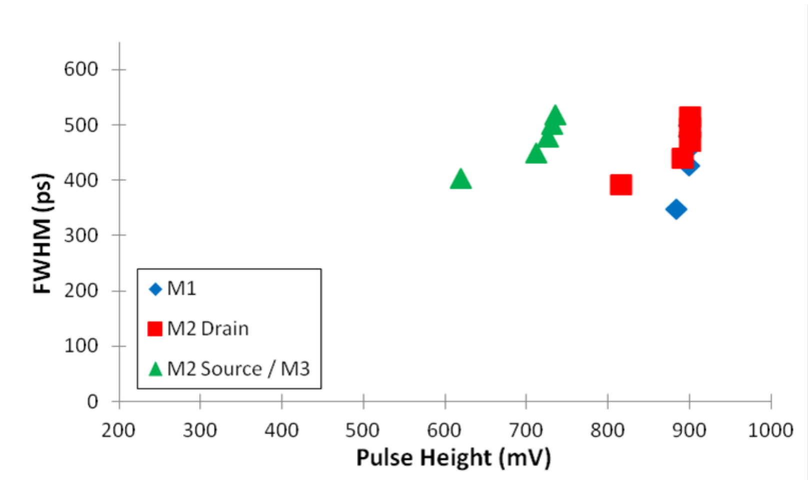
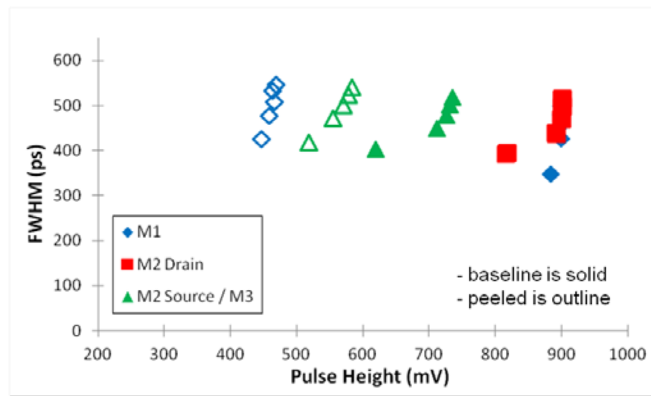


Fig. VI-25 SE nodal analysis of the baseline folded cascode amplifier shown in Fig. VI-22 for all five simulated LETs



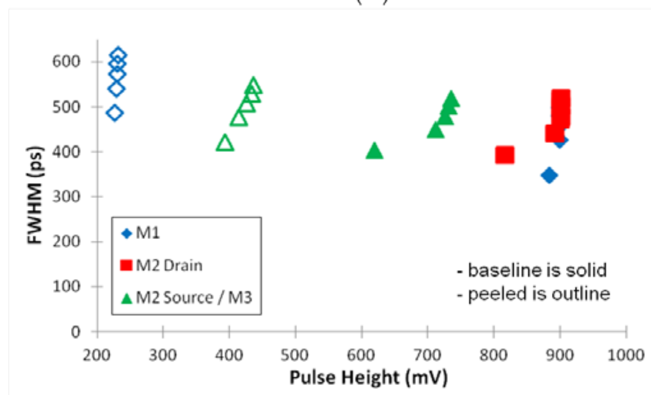


Fig. VI-26 Comparison of the baseline versus peeled (a) and versus the four parallel path (b) peel of the folded cascode amplifier four all five LETs

Similar to the other simple amplifiers discussed to this point, this circuit is not a good candidate for DCC or SNACC, leaving a peeled layout as the primary hardening option.

Fig. IV-26 compares the response of the baseline circuit with that of the single peeled (a) and a double peel version (b) of the hardened circuit. When digesting the results of this circuit with respect to the previous two amplifiers it is important to recognize that the output node of the circuit is not the only node, making a peeled layout more effective. The peeled layout is very effective in mitigate the magnitude of perturbation following strikes to every sensitive junction except the drain of M2, the output node. The reductions in the double peel were better than the single peel with a reduction in pulse height following a 50 MeV-cm^2/mg of 75 and 41% to M1 and the source of M2/ M3. These reductions are significant with only a minor gain of approximately 15% in pulse width in the case of M1 and 7% for the source of M2/M3. The only design penalty associated with the peeled layout is a small non-sensitive area penalty associated with device spacing, like the other peeled layouts.

Cascode Amplifier

The cascode amplifier is a popular choice for A/MS circuit designers due to its high output resistance and shielding of the output node from the input signal. The number of cascode devices often determines the output resistance and therefore the gain, but also consumes valuable voltage headroom. The variation of the cascode amplifier studied in this work is shown in Fig. VI-27. The amplifier has a gain of 12.5 dB and an operating current of 19 μA. These operating parameters are achieved by sizing the PMOS devices as 30 x 0.5 μm and 12.5 x 0.5 μm for the NMOS devices.

Fig. VI-28 contains the simulation results of a nodal analysis of the baseline cascode amplifier for LETs ranging from 10 to 50 MeV-cm^2/mg in increments of ten. This design is similar to the other amplifiers, in that its output node is extremely sensitive to SEs and pins the voltage to the power rails following strikes of most LETs. It also, like the other amplifiers is only able to be hardened via a peeled layout.

Fig. VI-29 contains the results of the nodal analysis of the baseline amplifier and a version peeled into four parallel paths. Similar to the other amplifier the single peel was effective, but the double peel or four-path version is more effective at mitigating the response. The peeling was the most effective mitigating the response of strikes to devices M1 and M4. The hardening does a fairly good job reducing the ASET duration following strikes to M2, but does not prevent the output voltage from being pinned to the rail. Similar to the other amplifiers studies the hardening does little mitigate the response of the struck node, M3 in this case.

Overall, a peeled layout is beneficial to the radiation response of a cascode amplifier. A designer could expect to see up to a 49 and 57% reduction in the ASET pulse height following strikes to M1 and M4. These data points are for a double peel, creating four parallel paths and only incurring the minor non-sensitive area penalty associated with device spacing.

Differential Current Amplifier

Adaptive biasing is a popular technique in A/MS design because it allows a circuit designer to minimize power consumption while increasing the output drive capability. The concept of adaptive biasing is to increase the tail current, in the case of a differential amplifier, when necessary to charge a large capacitance but to nominally keep

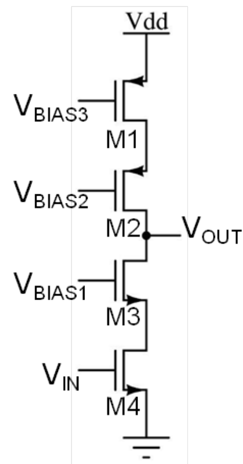


Fig. VI-27 The cascode amplifier designed and studied as a fundamental A/MS building block

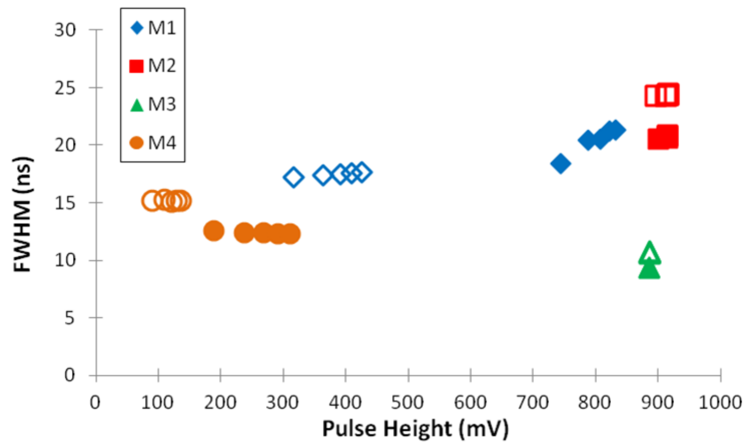


Fig. VI-28 SE nodal analysis of the baseline folded cascode amplifier shown in Fig. VI-22 for all five simulated LETs

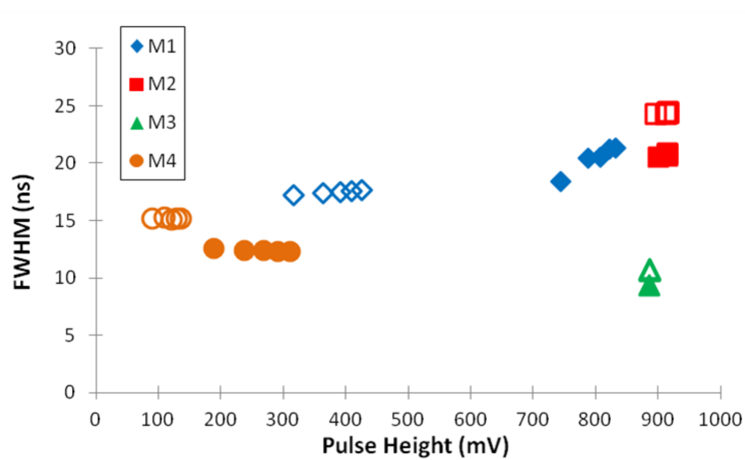


Fig. VI-29 SE nodal analysis of the baseline and twice peeled (four-path) folded cascode amplifier for all five simulated LETs

it at a lower value. A differential current amplifier, such as the one shown in Fig. VI-30 can be used to provide this additional timely tail current [64]. This differential current amplifier compares I_1 and I_2. If I_1 is larger than I_2, then the excess current will go through M3 and will be multiplied by the W/L ratio to sink a current through M4. Circuits like this are often used with a gain (K) of 1 or less when functioning as an adaptive tail current device. The currents I_1 and I_2 are then related to the differential devices currents, allowing for them to turn on when there is a large difference in the input voltages. The simplicity of this design also makes it popular for high-speed circuits that are just primarily concerned with the difference in the two currents.

The circuit design in this work uses 8 µm x 0.5 µm NMOS devices for M1-M4 (K=1). The currents I_1 and I_2 were sourced through PMOS devices with a resistive load attached to M4, creating a mid-rail bias. The quiescent currents were designed at 37.5 and 75 µA for I_1 and I_2 respectively. Fig. VI-31 contains the results of a SE nodal analysis of the baseline circuit design for the 5 simulated LETs (10-50 MeV-cm^2/mg) at normal incidence. These results indicate that three of the four sensitive junctions in the circuit

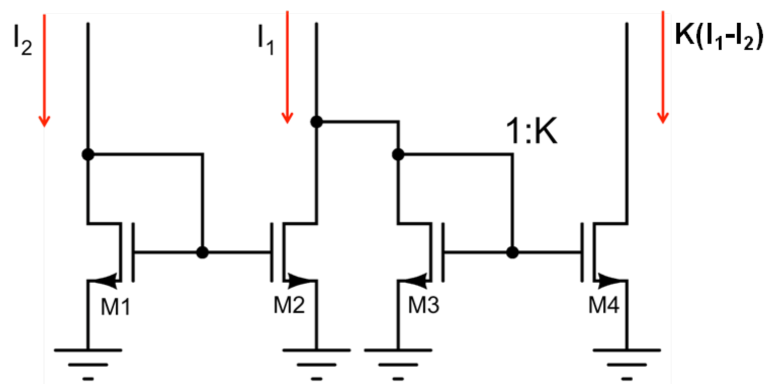


Fig. VI-30 The differential current amplifier studies in this work as one of the A/MS fundamental building blocks

are extremely sensitive to SEs. In fact, SE strikes of all the simulated LETs to devices M2/M3 and M4, caused the output voltage to pin to the power rail. Ideally, M1 would not be sensitive to SEs at all because excess current sunk through it following a SE would be mirrored through M2 and cancelled out, similar to a common mode error. The difference in the timing of charge collection and the circuit's ability to mirror a current prevents this cancellation from fully occurring. A circuit designer attempting to harden this circuit against SEs will want to naturally try a DCC layout due to the differential nature. Fig. VI-32 shows a DCC layout between any set of devices is not very effective or in the case of M1 actually hurts the performance. The DCC layout does reduce the pulse widths of ASETs following strikes to M2/M3 by almost 36%. A peeled layout is much more effective.

Fig. VI-33 contains the results of a SE nodal analysis comparing the baseline circuit (solid shapes) with a double peeled (four path) hardened version (outlines) for the

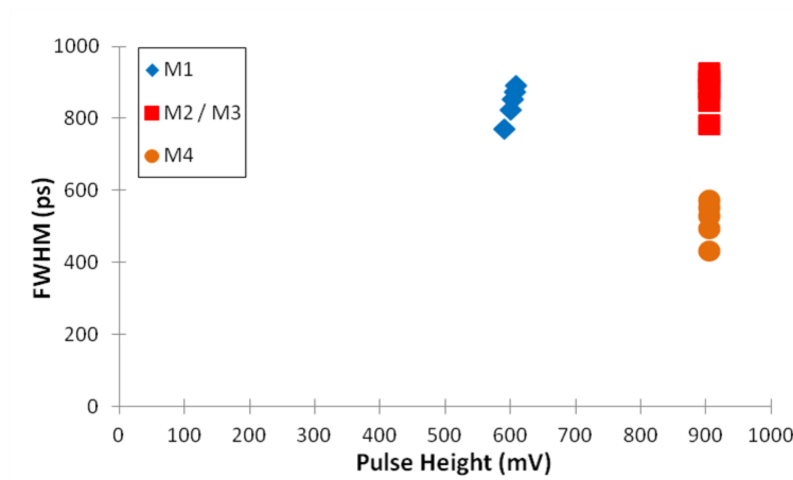


Fig. VI-31 SE nodal analysis simulation results of the baseline differential current amplifier following normal incidence strikes ranging from 10 to 50 MeV-cm^2/mg in increments of 10

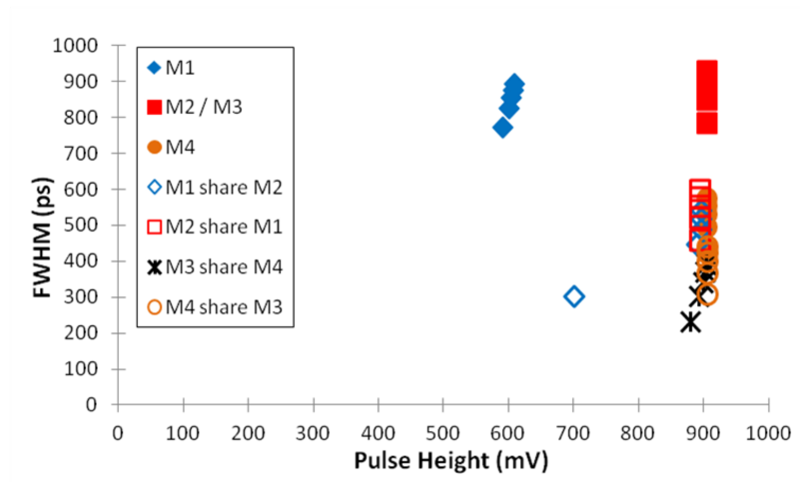


Fig. VI-32 SE nodal analysis of the baseline differential current amplifier exploring various DCC layout combination for all five simulated LETs

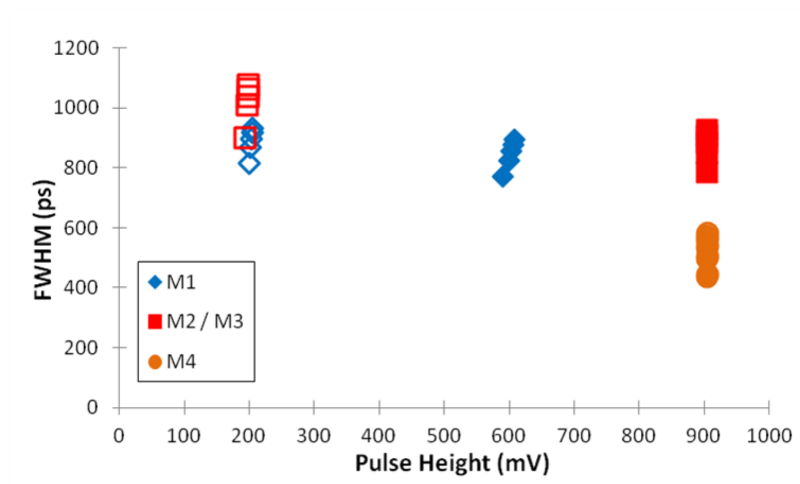


Fig. VI-33 SE nodal analysis of the baseline (solid shapes) and peeled (outline) differential current amplifier for a 2x peel following strikes of all five simulated LETs

five simulated LETs. The single peeled circuit was also effective in mitigating the SE response, but to a lesser extent. The pattern with the peeled layout observed throughout this study of the peeled layout being effective on all nodes except the output node holds true. If a designer peels a circuit similar to this current amplifier he should expect to see

up to a 67 and 79% reduction in ASET pulse height following a SE. The only penalty associated with the peeled layout is once again the non-sensitive area penalty associated with PDK spacing rules.

Differential Amplifier

The differential amplifier (diff amp) is probably the most fundamental of the building blocks explored in this dissertation. Differential amplifiers are everywhere in A/MS design and are critical pieces of other building blocks, such as the op amp discussed in the experimental section of this work. The diff amp studied in this section, shown in Fig. VI-34 is very similar to the one that serves as the input stage of the previously discussed op amps. This diff amp was designed with the current source devices being 25 x 0.5 µm, the input devices 10 x 0.5 µm, and the tail devices were also 10 x 0.5 µm. The amplifier had a gain of 75 dB and a f_{-3dB} of 5 MHz. The common mode rejection ratio (CMRR) was 99.5 dB.

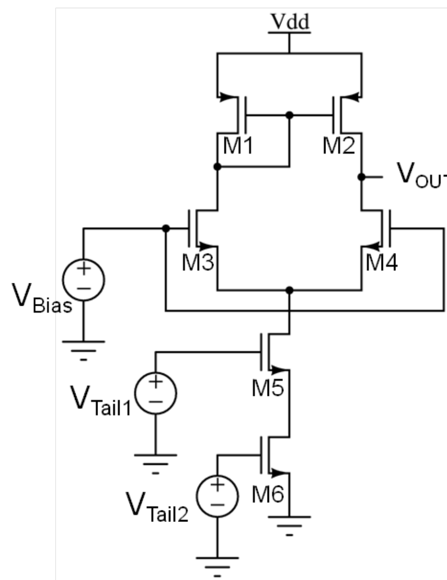


Fig. IV-34 The diff amp studied in this work as one of the fundamental A/MS building blocks

Fig. VI-35 contains the results of a SE nodal analysis of the baseline amplifier for all five of the simulated normal incidence LETs. The results of the tail currents devices are omitted because they were negligible in comparison to the other devices. The hardening results of this type of circuit were experimentally proven, as a sub-circuit of an op amp in chapters four and five. Those chapters showed that a DCC layout, a peeled layout, and the combination of the two were all effective. These cases were simulated to confirm and validate that this information is also true when the diff amp is a stand-alone circuit. Fig. VI-36 depicts the circuit's response following normal incidence SE strikes to the differential input devices (M3 and M4) with and without DCC hardening. As the earlier experiments proved DCC is effective in mitigating the magnitude and duration of perturbation following strikes to a differential pair. Overall there is an average reduction of 15% in pulse height following strikes to the differential input devices when using a DCC layout.

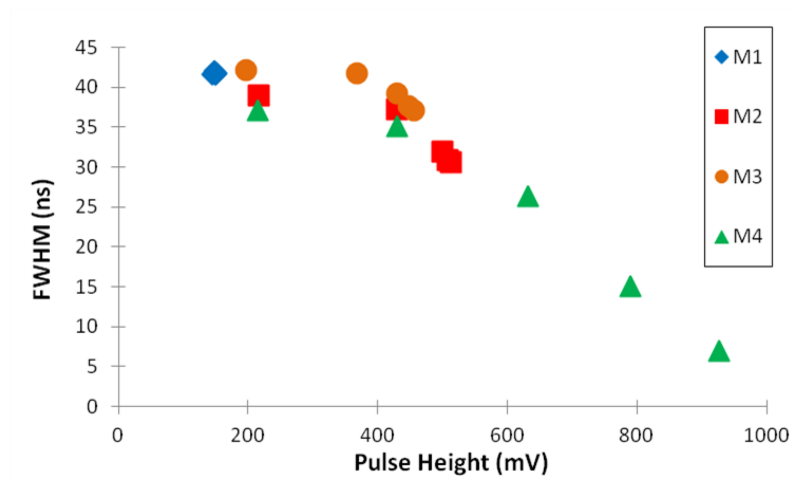


Fig. VI-35 SE simulation results for the baseline diff amp shown in fig. VI-32 for all five simulated LET at normal incidence

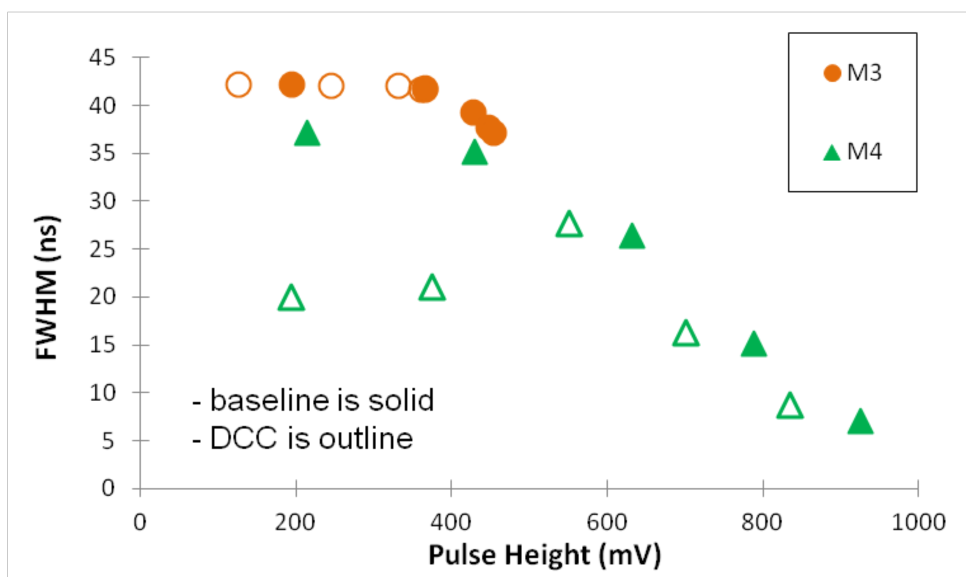


Fig. VI-36 SE simulation results comparing the baseline input stage with an input stage using a DCC layout for all five simulated LETs at normal incidence

Fig. VI-37 plots the simulation results of the baseline versus the twice-peeled input stage (four parallel amplifiers) for all five LETs. The single peel was effective, but the double peel does an even better job, similar to the previous simulations. The peeled layout is very effective in mitigating the error response of devices M1 and M3, but less so for M2 and M4. This is consistent with the other building block simulations that suggest a peeled layout works for every node except the measured/output node. Further evidence that this is a function of M2 and M4 being the output node is how effective the peeled layout was for these same devices in the op amp experimental results presented in chapter V. A peeled layout does have an advantage over a DCC layout in that it also improves the response of the current mirror devices M1 and M2, where a DCC layout actually made it worse.

The previous experiments suggest these mitigation techniques can be combined and Fig. VI-38 shows simulations results supporting that. In this figure M1 and M2 are

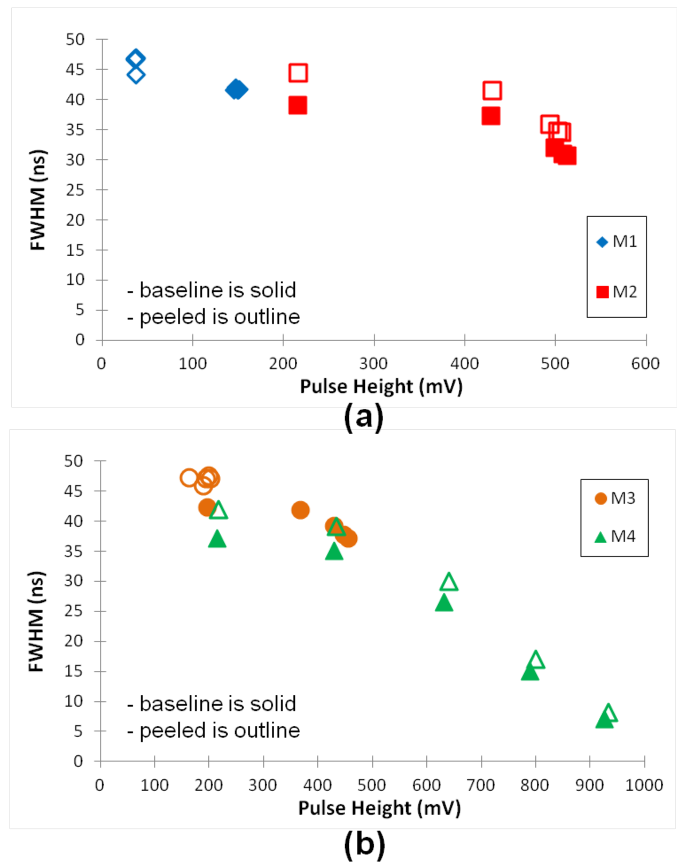


Fig. VI-37 Simulations results comparing the baseline versus the twice peeled (four parallel path) version of a differential amplifier four all five simulated LETs

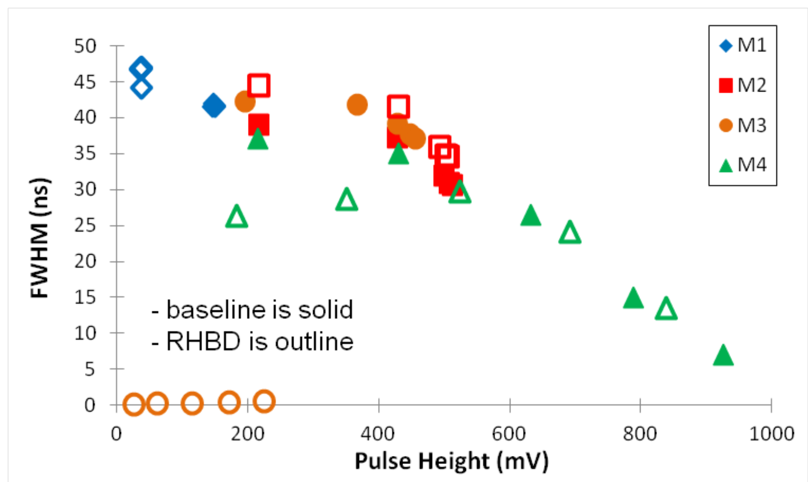


Fig. VI-38 Comparison of the baseline and RHBD diff amp for all five simulated LETs. The RHBD version is peeled twice (four parallel paths) and the input devices have a DCC layout

peeled only and the input devices (M3 and M4) are peeled and have a DCC layout. These results are impressive, particularly for the devices that are not on the measured node such as M3 and M1. The experimental results suggest that all nodes would see such an improvement if this circuit was used as a sub-circuit in a larger system. The overall reduction in pulse height a designer could expect from combining these techniques if 77, 2, and 31% for M1, M2, and the diff pair respectively. Not shown in this analysis because it is less significant, the peeled layout also reduces the average pulse height following strikes to the tail current devices M5 and M6 by more the 50%. These reductions come with only the minor non-sensitive area penalty that accompanies a peeled layout.

Conclusion

The first five chapters laid an extensive groundwork to include experimental verification of three hardening techniques that fall into two larger categories. However, there was not a lot of explanation or suggestion outside of an op amp how these techniques could and should be implemented to harden other A/MS circuits. This chapter followed an approach similar to that of A/MS circuit course and analyzed basic building block circuits to gain insight into how these techniques can apply to a broader set of circuits.

This extensive simulation analysis suggests that every A/MS circuit should be peeled. The small addition of area is less critical in an A/MS system where packing density is often sacrificed for matching and circuit performance anyway and is well worth the gain in SE immunity. The effectiveness of a peeled layout is also minimized when applied to the output node of a circuit.

Differential charge cancellation only appears to occur in traditional differential circuits with a CMRR, like a diff amp. It is not necessarily effective in pseudo differential circuits such as the differential current amplifier studied in this work. A DCC layout however is effective in hardening non-differential circuits by encouraging charge sharing to trigger other mechanisms, such as the internal feedback loops seen in the regulated cascode current mirror and bootstrap current source. Opportunities to leverage this type of circuit behavior should always be sought out and exploited by a circuit designer.

Finally, at least at the 180 nm technology node the 6-transistor implementation of SNACC is not worth the additional sensitive area. The technique is effective, but there are other less costly methods (such as a peeled layout) to achieve the same or better performance. SNACC appears to be most useful when it can be accomplished via the circuit's external circuitry, similar to the cascode output stage of the op amp explored in chapter IV. SNACC hardening should be reconsidered in technologies where charge sharing efficiency approaches 50%, as was discussed in chapter IV.

CHAPTER VII

CONCLUSIONS

This dissertation introduced three novel radiation hardened-by-design techniques that fall into two larger classes of hardening. These broad categories of hardening via charge sharing and hardening by node splitting establish a framework for the radiation effects community. This framework can be used to establish a general hardening concept a circuit designer can later refine for a specific circuit. The hardening specificity that can be added to the general framework varies for each general class. Inside the hardening via node sharing class of techniques the designer can choose between two tools (verified in this dissertation), sensitive-node active charge cancellation and differential charge cancellation layout. These techniques enable the hardening of a vast array of circuits designed in bulk technologies. This dissertation introduced a single hardening technique for the broader hardening via node splitting category, a peeled layout. Significant evidence presented throughout this work established that it is effective in both bulk and SOI technologies.

The operational amplifier was chosen as the test circuit for the experimental portion of this work because of its ubiquitous nature throughout A/MS circuit design. Operational amplifiers are critical circuit components in almost all significant A/MS circuit blocks. Everything from integrators and comparators to data converters and reference circuits use op amps as key components. The primary purpose of the op amps used in the experiments detailed throughout chapters IV and V was to provide a platform

to judge the effectiveness of DCC layouts, SNACC, and a peeled layout. The incredibly powerful added benefit of using the op amp as a test vehicle is a developed framework for exactly how to harden one of the most common and important building blocks in A/MS design.

These experiments demonstrated quite convincingly that all op amps should be peeled, regardless of the technology (bulk or SOI). In the formulation of the experiment a mathematical proof equated the CMRR of a differential amplifier and a single-stage of a peeled op amp. The experiment later verified this and provided another tip to op amp designers. All op amps designed in bulk technologies should have the parts of their peeled signal path that are differential laid out using DCC. The hardening tool that an op amp designer has discretion with is SNACC. This study provided multiple examples of how SNACC can be used by slightly adjusting existing circuit layouts to leverage inherent balancing circuit topologies. It also demonstrated how additional devices can be added to create the SNACC effect. SNACC hardening should always be used when it can be achieved via the circuit's natural topology such as the bulk technology single-ended folded cascode op amp discussed in this work. Experimental evidence also suggests that the additional device implementation of SNACC should be used in a circuit with a large area such as an op amp that is particularly sensitive to strikes to its bias circuit. The TPA SE experiments in this dissertation showed that more than a 90% reduction in SE sensitive area in an op amp could be achieved by combining these techniques. The penalty for this reduction is only a minor addition in area of approximately 5%.

This "how-to" guide for hardening one of the most fundamental blocks in A/MS circuit design (op amp) using novel hardening techniques is a significantly noteworthy

contribution to the scientific community. However, in order to further expand the impact of these novel-hardening techniques a simulation study was performed of simpler A/MS building block circuits. The concept behind this study was similar to the pedagogy used in most electrical engineering curriculums. A thorough understanding of how to harden the building block circuits of A/MS will enable a greater understanding of how to apply those hardening techniques to the majority of A/MS circuits. This methodology coupled with the observation that the majority of A/MS circuits are built using the same topologies and building blocks enables a very broad impact for this work.

The A/MS building blocks simulation study presented in chapter VI of this dissertation, examined in detail nine different circuits. After each circuit was designed using a 180 nm IBM PDK it was subjected to a SE nodal analysis. This nodal analysis included normal incidence strikes of five different LETs ranging from 10 to 50 MeV-cm^2/mg in increments of 10 using a bias-dependent SE model. The circuit was then hardened with each one of the three hardening techniques (and combinations thereof when appropriate) and subjected to another nodal analysis. This process was repeated for each of the nine building block circuits providing a substantial body of data for analysis.

The most significant finding and contribution to the community from this study and the experimental evidence in this dissertation is that all A/MS circuits intended for an ionizing radiation environment should be peeled. This is a very important finding and fundamentally alters the way that circuit designers in this domain operate. The caveat to this statement is that the well potential for each peeled portion must be maintained. This could possibly require the addition of more well contacts and add slightly to the area associated area penalty.

The study also suggests that after every A/MS circuit is peeled, every differential path (for bulk technologies) should use a DCC layout. This coupling of a peeled and DCC layout significantly improves the SE performance of the circuit without any significant additional penalty. Designers also should pay careful attention to recognize internal mechanisms such as the feedback loops in the bootstrap current source and regulated cascode current mirror that can be triggered via charge sharing, encouraged through a DCC layout. Opportunities to exploit hardening via charge sharing in this manner should be sought out by designers because they can be added to a peeled layout to achieve greater SE immunity without any significant additional penalty.

Finally, the study suggests that while the six-transistor implementation of SNACC is effective in certain cases it is not the best choice for hardening at the 180 nm technology node. Greater reduction in SE errors can be achieved via a peeled layout and/or a DCC layout without adding sensitive area. The technology node used primarily in this work (180 nm) is not cutting edge, but preferred in the A/MS design community due to its process maturity and voltage headroom. Evidence was presented that suggests the additional device implementation of SNACC may be more effective at cutting edge technology nodes where the charge share ratio between primary and secondary device approaches 50/50. SNACC behavior, as demonstrated through the TPA SE hardening tests of the output stage of the folded cascode op amp, should always be sought out when achieved through existing compensatory current mirror architectures.

While the research presented in this dissertation does provide significant contribution to the radiation effects circuit design community it also illuminated a substantial limitations in current measurement methodologies that merits future

investigation. In order to measure the radiation response of the integrated circuit op amps presented in this work they had to be discretized. The addition of the parasitics associated with the IC's I/O, the PCB, the cabling, and the measurement device (oscilloscope) fundamentally changed not only the behavior of the circuit, but the circuit design itself. In order for the op amp to be stable and able to drive those parasitics the compensation and buffer had to be altered. This alteration was unavoidable with the current state of the art and previous work (presented in chapter II) allowed for it to be accounted for, but a better method is possible.

The design of an on-chip analog pulse capture circuit is greatly needed and would enable exponential growth in understanding of the SE performance of A/MS circuits. The design of such a circuit would be difficult, primarily due to the pico-second or better time resolution it would require. The measurement and understanding of an A/MS circuit behavior in its intended use (i.e. without unwanted parasitics) would enable further development of hardening techniques and advances in the field.

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