RADIATION-HARDENED-BY-DESIGN (RHBD) DELAY LOCKED LOOPS (DLLs): SINGLE EVENT TRANSIENT ANALYSIS, SIMULATION, AND HARDENING

By

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TABLE OF CONTENTS

APPENDIX

LIST OF FIGURES

Figure Page

LIST OF TABLES

Table Page

TABLE OF ABBREVIATIONS

ABBR.	***DEFINITION***	***ABBR.***	***DEFINITION***
DLL	**Delay-Locked Loop**	**V_CP**	**Voltage-based charge pump**
PLL	**Phase-Locked Loop**	**SET**	**Single-event transient**
VCDL	**Voltage-controlled delay line**	**WR_VCDL**	**VCDL of the WR-DLL**
CP	**Charge pump**	**WR-CP**	**charge pump of WR-DLL**
PD	**Phase detector**	**WR-DLL**	**Wide-range DLL**
PFD	**Phase-frequency detector**	**LET**	**Linear energy transfer**
LPF	**Low pass filter**	**DFF**	**D flip flop**

LIST OF APPENDIXES

Page

CHAPTER I

INTRODUCTION

Delay-locked loops (DLLs) are widely used for clock recovery and on-chip clock distribution in microprocessors, memories, and communication ICs in commercial and space deployed electronics systems. DLLs represent a modification of phase-locked loop (PLL) circuits created specifically for clock distribution and data synchronization applications where frequency multiplication or synthesis is not required. Often, DLLs are preferred in these applications due to their improved stability and better jitter performance over PLLs [1-3]. The DLL is frequently used to eliminate the delay created by a skewed clock signal, which can otherwise limit the maximum data transfer frequency [4].

A single-event (SE) effect occurs when a high-energy ionizing particle, such as a heavy ion, strikes the circuit. As the particle penetrates the semiconductor material, it loses energy through coulombic interactions with the lattice structure and leaves a dense track of electron-hole pairs in the material. These excess carriers can be collected on circuit nodes, resulting in undesirable circuit responses which can vary depending on the circuit topology. One type of effect resulting from SEs in an IC is a single-event transient (SET); SETs are undesirable asynchronous signals that can propagate through signal paths and result in a variety of circuit responses.

Single-event transients (SETs) have been identified as the primary failure mechanism behind several spacecraft malfunctions in recent years. Several techniques have been developed to characterize SETs in integrated circuits. Experimental approaches based on heavy-ion beams,

laser strikes, and ion micro-beams have been used to characterize the effects of SETs in integrated circuits.

The single-event vulnerabilities of DLL and PLL circuits are of particular concern for space-deployed systems, as SETs occurring within a clock distribution system can result in global errors across the entire IC. Since DLLs typically provide better noise rejection and lower jitter than their PLL counterparts when frequency synthesis is not required, the DLL is an excellent candidate for use in spacecraft clock distribution networks. While recent publications have shown that ion-strikes in PLL circuits can result in SETs on the order of several microseconds in length [4, 6], no research to date has analyzed SETs in DLLs specifically. Therefore, it is critical that SETs in DLLs be characterized in order to determine suitable techniques for hardening them against errors due to radiation effects.

This thesis presents the analysis of the SET response of a typical analog DLL and a wide-range DLL circuit in order to determine the response of the overall system, and (where appropriate) compare the response to that of similar sub-circuits in a PLL. The vulnerability of a DLL is shown to vary widely depending on the sub-circuit subjected to the ion strike. SETs in the phase detector or the controlled phase frequency detector sub-circuits have no significant impact on normal DLL operation, while the voltage-controlled delay line (VCDL) sub-circuit is most sensitive to single-events, as measured by output phase displacement and the number of erroneous output pulses. At a sufficiently large LET, a strike within the charge pump (CP) of an analog DLL may also lead to a persistent false lock error, termed an inverted lock error.

In this thesis the RHBD work was focused on mitigating the inverted-lock error, therefore the RHBD effort was directed on the charge pump in conventional DLLs. A voltage based charge pump is used as a RHBD solution to mitigate inverted lock errors in analog DLL, since

this hardening solution had already been successfully used to reduce the impact of SET in PLLs after an ion strike within the CP [6]. SET simulations of the DLL show the efficiency of this technique, as the inverted lock error is mitigated, but also the DLL implementing the voltage based CP exhibit a better SET response in terms of phase displacement than the other DLL topology considered in this work. However, the implementation of the voltage based CP in DLLs should be done carefully since this CP topology is sensitive to power supply fluctuations.

CHAPTER II

THE DELAY-LOCKED LOOP

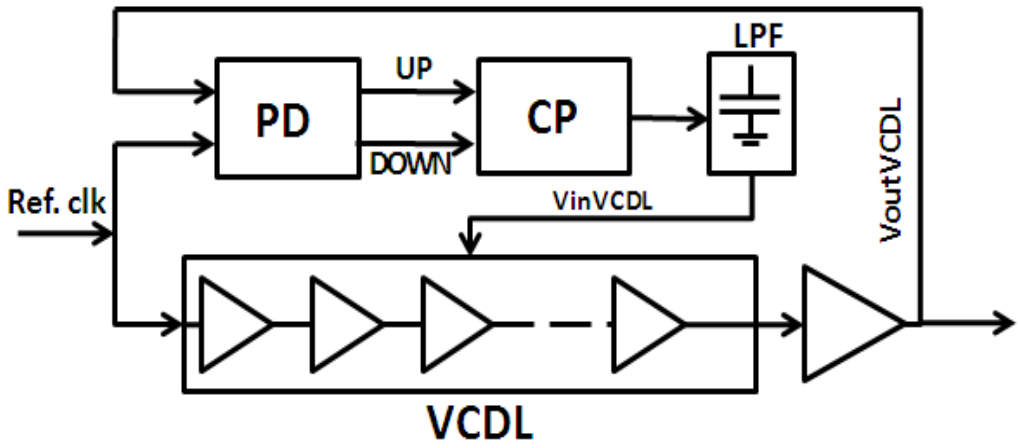
The delay-locked loop (DLL) is widely used for clock generation, clock de-skewing, and data recovery. Compared to phase-locked loops, delay-locked loops are a relatively recent innovation, first found in Dr. Combes' work in the early 1990s, then popularized by Xilinx in their Virtex family of FPGA products. Phase-locked loops (PLLs) and delay-locked loops (DLLs) have been typically employed for the purpose of synchronization. Due to the difference of their configuration, the DLLs are preferred for their unconditional stability and faster locking time than the PLLs. Additionally, a DLL offers better jitter performance than a PLL because noise in the voltage-controlled delay line (VCDL) does not accumulate over many clock cycles.

A. The Conventional Analog Delay-Locked Loop

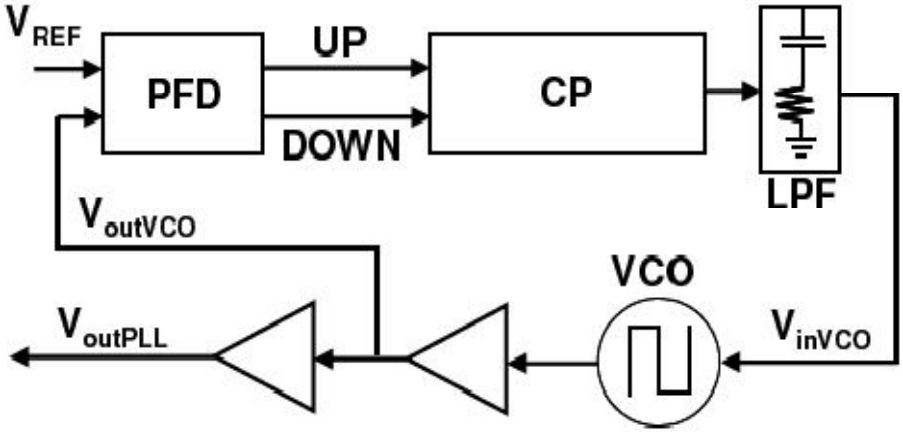
1. *Circuit Topology Description*

The delay-locked loop (DLL) in Fig.I.1 (a) consists of four main sub-circuits: a phase detector (PD), a charge pump (CP), a low-pass filter (LPF), and a voltage-controlled delay line (VCDL). From a topological perspective, DLLs and PLLs are similar in many respects. As shown in Fig. I.1(b), the basic PLL consists of a phase-frequency detector (PFD), a charge-pump (CP), a low-pass-filter (LPF), and a voltage-controlled oscillator (VCO). The main difference is that a PLL uses the VCO to generate an oscillating signal that is synchronized with the reference signal, while the DLL adjusts the phase of a reference signal using the VCDL.

In addition, DLLs are typically single-pole systems with a first-order loop filter (LPF pole), while PLLs are at minimum two-pole (VCO and LPF poles) systems. Consequently, DLLs provide improved stability over PLLs. Furthermore, while PLLs offer a greater phase capture range than the DLL ($\pm 2\pi$ versus $\pm\pi$ radians), DLLs have no phase error accumulation and no self-generated jitter.



(a)



(b)

Fig.II.1 (a). Block diagram of DLL consisting of a phase detector (PD), charge-pump (CP), low-pass filter (LPF), and voltage-controlled delay line (VCDL). **(b).** Block Diagram of PLL consisting of a phase-frequency detector (PFD), charge-pump (CP), low-pass filter (LPF), and voltage-controlled oscillator (VCO) [6].

2. Delay Locked Loop Modules

a) Phase Detector (PD)

A phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the delay-locked loop (DLL). Detailed schematics of the PD component choice and design are presented in CHAPTER V.

When the output of the VCDL ($V_{outVCDL}$) leads the rising edge of the input reference signal (*Ref.clk*), the output DOWN of the PD is active and generates a pulse proportional to the phase difference between the input signals *Ref.clk* and $V_{outVCDL,}$ when the output UP remain ideally null. Conversely, the UP output is active when $V_{outVCDL}$ lags *Ref.clk* in phase, and the output DOWN remains null. When both signals are in phase the outputs of the PD are ideally null values.

When the DLL is close to phase lock, i.e. the phase difference between *Ref.clk* and the output of the DLL ($V_{outVCDL}$) is nearly zero, the digital PD exhibits a region of very low or zero gain, called the dead zone. Ideally, when the phase of the DLL output differs only very slightly from the input signal (*Ref.clk*), the PD should be able to generate a very short pulse to drive the VCDL to an ideal phase difference of zero. Because the PD cannot generate such extremely narrow pulses, the input control voltage (V_{inVCDL}) will fluctuate randomly between the bounds determined by the shortest digital pulses the phase detector is able to generate, which in turn defines the dead zone region for the DLL, as illustrated in Fig. II.3.

As in PLL circuits, DLLs typically utilize a current-based charge pump topology (Fig. B.3) to convert the detected phase error into a proportional current, while also reducing the phase jitter associated with power supply fluctuations [5]. The CP remains idle when both signals are

synchronized. When the PD generates an UP/DOWN signal, the CP sources/sinks current to/from the low pass filter (LPF). The LPF converts the CP current into a voltage (V_{inVCDL}) that is used to adjust the delay of the VCDL. The value of capacitor C in the low pass filter can be calculated using Eqn. I.1 [3]:

$$Tr = \frac{(2.2 * C * Tclock)}{(Kv * 2 * Ipump)} = \#\ clock\ \ cycles\ \ * Tclock \qquad \text{II.1}$$

Where *Tr* is the response time of the DLL in second, *Tclock* is the input signal period in second, *Kv* the gain of the VCDL in second per volts and *Ipump* the CP current in Amperes.

b) The Charge Pump (CP)

The output of the phase detector is combined into a single output for driving the loop filter. There are two methods for doing this. The first method is called a tri-state output (also known as voltage-based charge pump), but this technique is sensitive to power supply fluctuations [3], and the effect is to modulate the VCDL input voltage. The second method is the so-called charge pump (illustrated in APPENDIX B, Fig B.3); in this method, MOS current sources are used, and the modulation of the VCDL input voltage is reduced since the current sources can be made insensitive to power supply fluctuations.

c) The Voltage Controlled Delay Line (VCDL)

The VCDL is based on a current-starved driver topology, composed of several variable-delay elements connected in series as shown in Fig. II.1(a), to provide a controlled delay of the input clock signal. Alternative VCDL topologies, such as a fully differential topology, may also be used for improved noise performance and power supply variation rejection. It is important to

note that a conventional DLL will either fail to lock or go into false lock if the initial delay of the VCDL is shorter than 0.5 Tclk or longer than 1.5 Tclk, where Tclk is the period of the clock signal. Therefore, the initial delay of the VCDL must be in the range 0.5 Tclk to 1.5 Tclk [1-3].

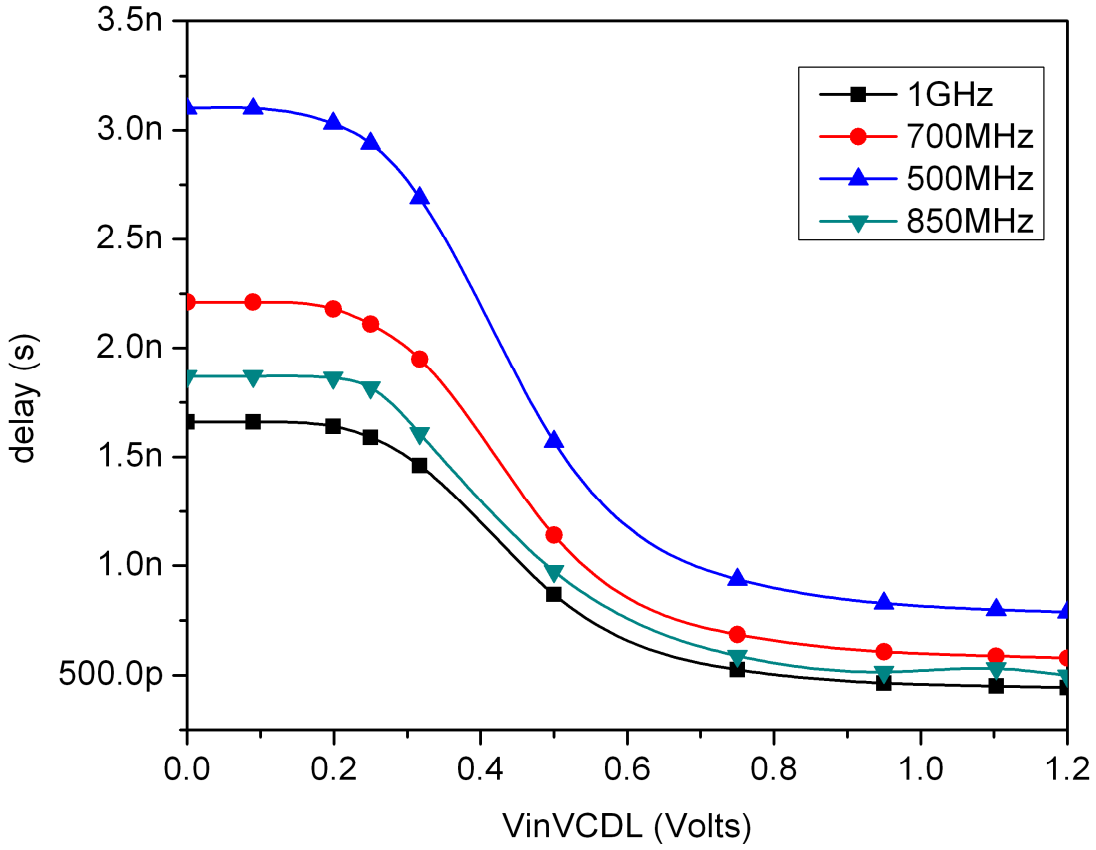


Fig. II.2. VCDL output delay versus control voltage (VinVCL) for analog DLLs operating at 500 MHz, 700MHz, 850 MHz and 1 GHz.

Fig. II.2 shows the VCDL output delay versus input control voltage (V_{inVCDL}) with a delay range of 0.5 Tclk to 1.5 Tclk for typical analog DLLs operating at 500 MHz, 700 MHz, 850 MHz and 1 GHz.

3. DLL Electrical Characteristics

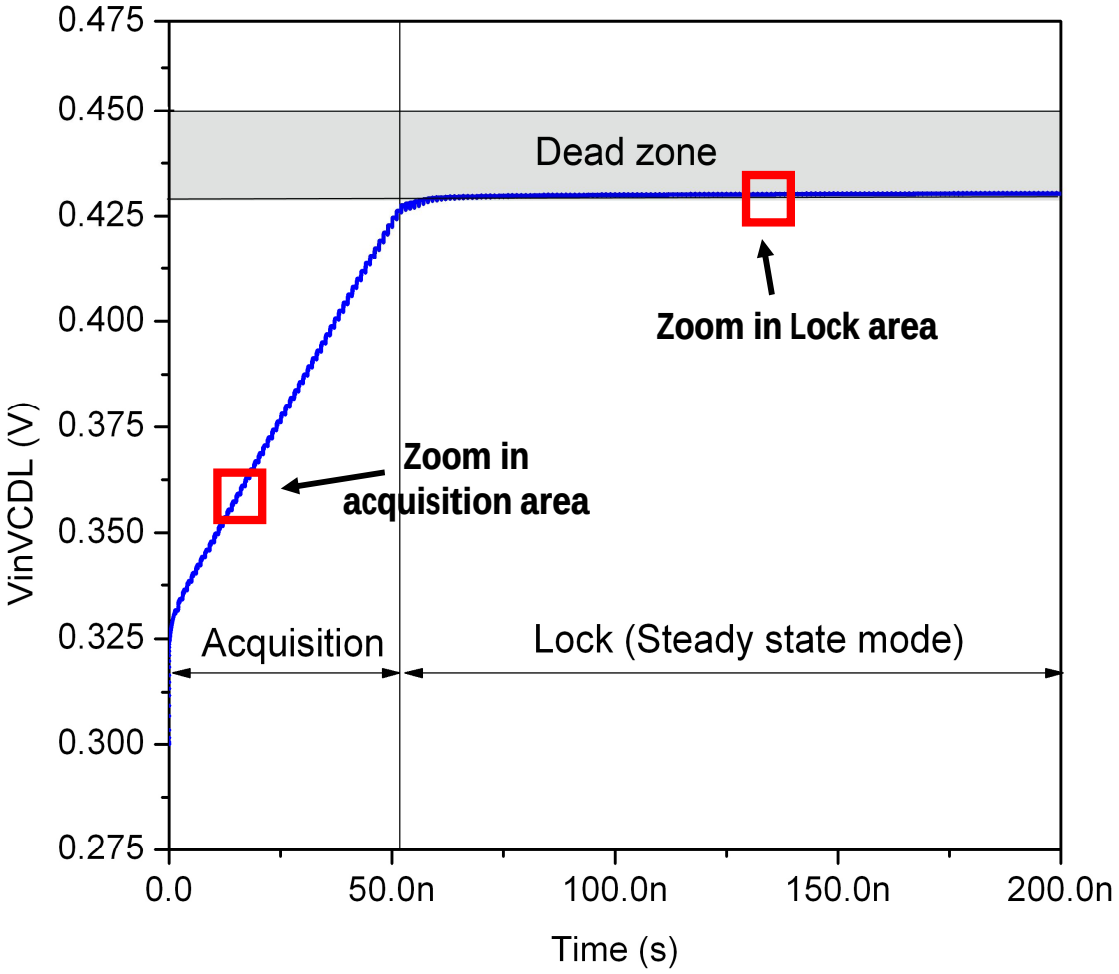


Fig. II.3. DLL acquisition curve for operation at 1 GHz, the dead zone has been measured (≈ 36 ps) and represented by the grey region in terms of VinVCDL.

The basic function of the DLL is to synchronize the delayed output signal ($V_{outVCDL}$) to the reference signal (*Ref.clk*). On startup, the DLL passes through two operating phases: the acquisition phase, and then the lock phase where the phase difference between $V_{outVCDL}$ and

Ref.clk is a constant value of 0 or π radians, depending on the design. Fig. II.3 shows the acquisition curve of a typical DLL that is operating at 1 GHz. The acquisition mode represents the time period where clock signal $V_{outVCDL}$ is lagging in phase compared to the input reference signal, *Ref.clk* (Fig.II.4). During this time the value of V_{inVCDL} changes with every clock cycle as the PD compares the phases of the two signals and the CP sources current to the LPF. Once signals $V_{outVCDL}$ and *Ref.clk* are in phase (or ± π out of phase) as in Fig. II.5, the DLL goes into lock state, where voltage V_{inVCDL} ideally remains constant. The value of V_{inVCDL} in lock mode is determined by the dead zone region.

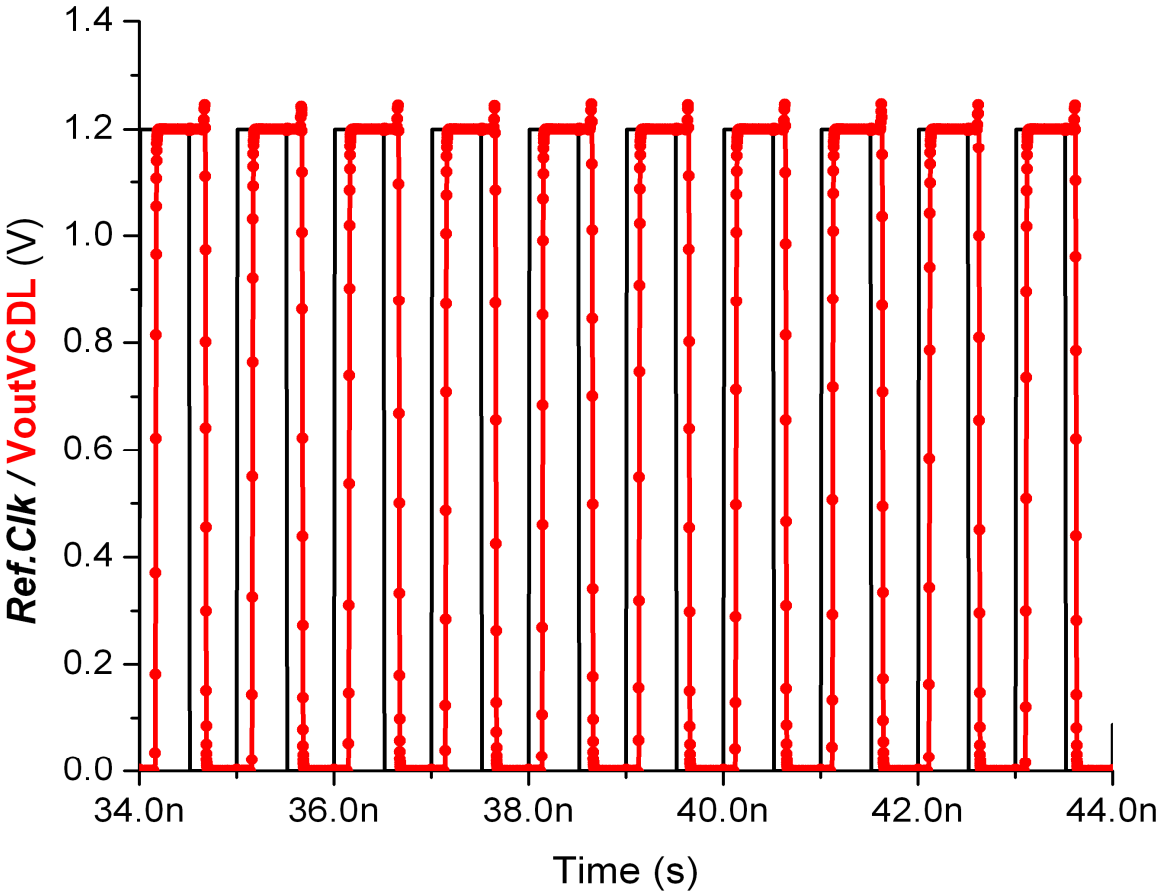


Fig. II.4. Zoom in the acquisition area for an analog DLL operating at 1 GHz.

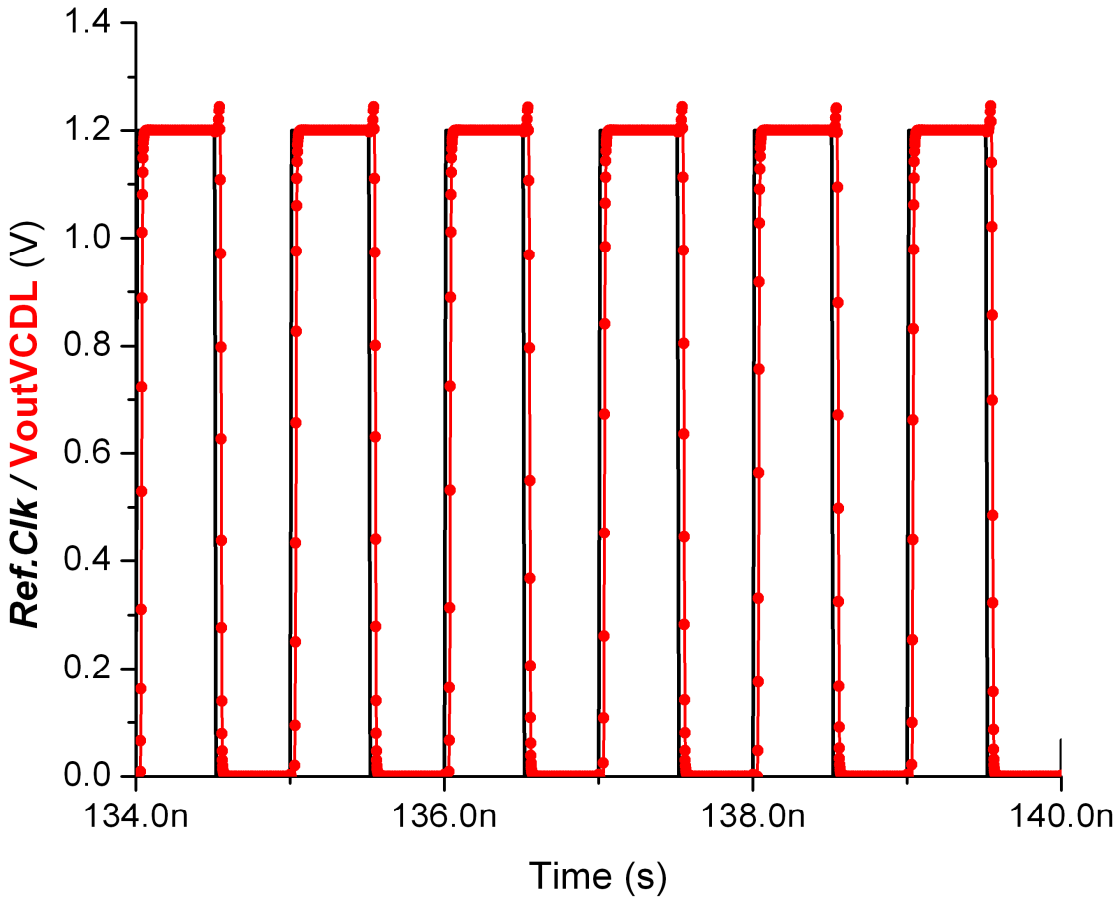


Fig. II.5. Zoom in the lock area for an analog DLL operating at 1 GHz.

B. The Wide-Range Delay-Locked Loop

The conventional analog DLL cannot false lock or harmonic lock to two or more clock cycles *Tclk* of the input reference signal, since the initial delay of the VCDL is designed to be located between 0.5 *Tclk* and 1.5 *Tclk*, regardless of the initial voltage of the loop filter, as shown in (Fig.II.6). Assume that the maximum and the minimum delay of the VCDL are *Tmax* and *Tmin*, respectively. As a result, the period of the input signal should satisfy the following inequality [12]:

$$Max\ (Tmin\ ,\ \frac{2}{3} * Tmax) < Tclk < Min\ (Tmax,\ 2 * Tmin) \qquad \text{II.2}$$

Equation (I.2) shows that the DLL is prone to the false locking problem when process variations are taken into account [12]. Therefore, some solutions, described as follows, were proposed to overcome this problem.

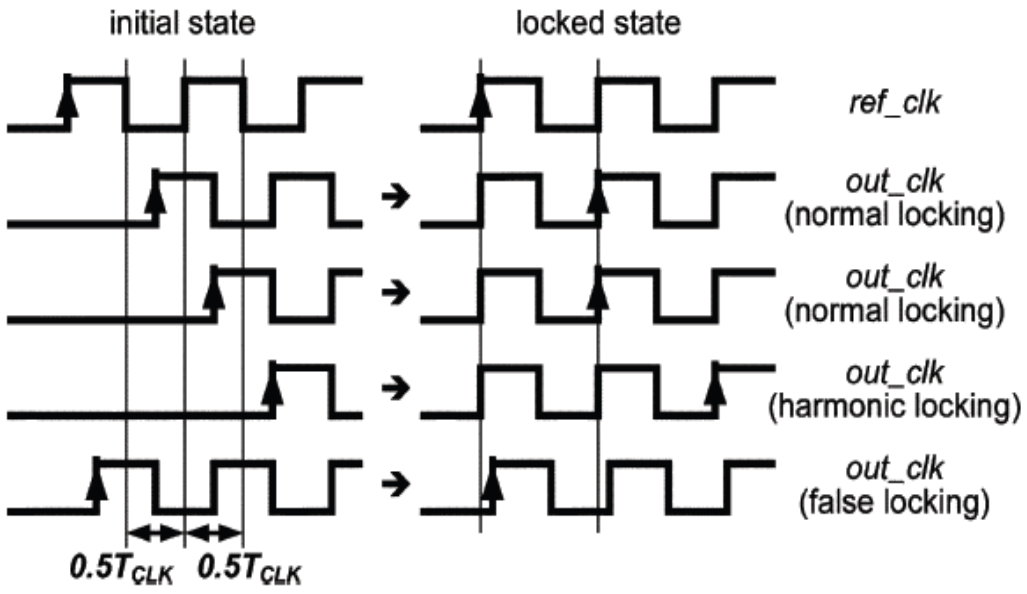


Fig. II.6 . DLL in normal locking, harmonic locking, and false locking conditions

First, the basic idea is to use a phase-frequency detector (PFD) [1], because it has a phase capture range of $\pm 2\pi$ vs. $\pm \pi$ for conventional phase detectors. Therefore, the PFD is a better choice for wide range operation. However, the PFD cannot be used in the DLL alone without any control circuit because the DLL will try to lock at zero delay. A PFD combined with a control circuit is presented in [2]. Nevertheless, in some cases, especially for high-frequency operations, the initial delay between ref_clk and vcdl_clk, as shown in Fig. 1, may be larger than two clock cycles and harmonic locking will occur.

Second, a solution called an all-analog DLL using a replica delay line [12] has been developed to solve the narrow frequency range problem of a conventional DLL. If the delay range of the VCDL satisfies the relation Tmin < 1/7 Tmax, the DLL output delay can be significantly increased. However, because the PD uses an exclusive-NOR in the replica delay line, the input signal duty cycle must exactly equal 50%.

Third, a digital-controlled DLL called the self-correcting DLL is proposed in [11]. The problem of false locking is solved by the addition of a lock-detect circuit and the modified phase detector. Although this self-correcting DLL avoids false locking, based on the circuit design, the outputs of the VCDL are required to have an exact 50% duty cycle, in order to the digital-controlled DLL to work properly.

In this work, a wide-range DLL using a PFD was designed using the IBM 90-nm PDK. This topology is very similar to the conventional analog DLL design and has been used, in some applications, to replace conventional analog DLLs. The PFD topology should also have an advantage in terms of sensitivity of the DLL to single events. Therefore it is also critical that

SETs in wide-range DLLs be characterized in order to determine suitable techniques for hardening them against errors due to radiation effects.

1. Topology Description

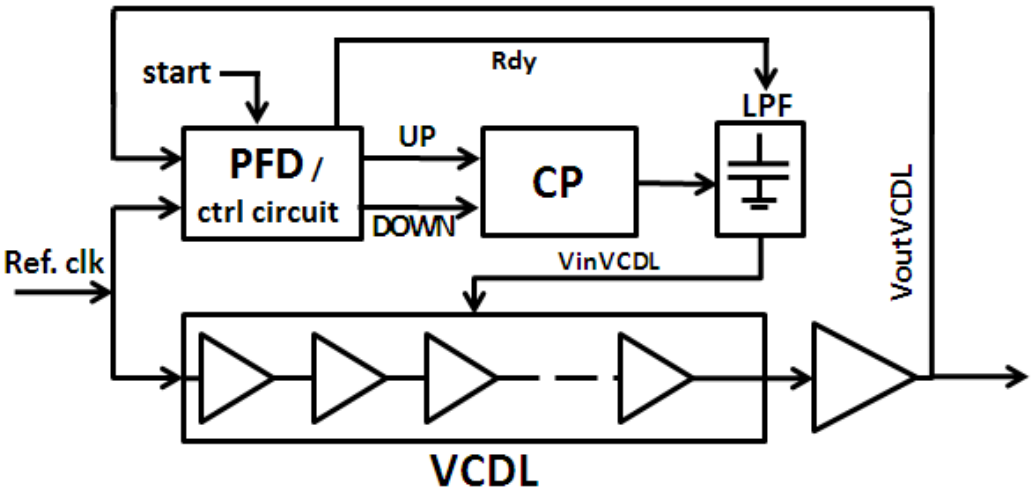


Fig. II.7. Block diagram of a wide-range DLL consisting of a phase-frequency detector (PFD) with control circuit, charge-pump (CP), low-pass filter (LPF), and voltage-controlled delay line (VCDL) .

The wide- range DLL (WR-DLL) presented Fig. II.7 consists of four main sub-circuits: a charge pump (CP), a low-pass filter (LPF), and a voltage-controlled delay line (VCDL), similar in topology to the modules in the analog DLL, and a phase-frequency detector and its control circuit (PDF/ctrl circuit). As in analog DLLs, wide-range DLLs are also single-pole systems with a first-order loop filter (LPF pole), and consequently they also provide improved stability over PLLs.

2. *The Phase-Frequency Detector (PFD) Module and Its Control Circuit*

The main difference between analog and wide-range DLLs is that the conventional phase detector has been replaced by a phase frequency detector; however the PFD needs to be combined with a control circuit is in order to ensure the proper operation of the wide-range DLL. A resettable dynamic D-flip-flop (DFF) based start-controlled PFD (detailed in CHAPTER V, with its timing diagram) was used for the designed wide-range DLL, since this design requires less circuit area and lower power consumption, than the other PFD with controlled circuit topologies. Details about the control circuit and the PFD are presented in the custom design section in CHAPTER V.

Initially, the start signal is set at low to clear the three DFF outputs. Therefore, Rdy is low and pulls the control voltage to Vdd (1.2 V), setting the VCDL delay to its minimum value. In this condition, the two PFD inputs are at a low level. When the start signal switches to high, the Rdy signal also switches to high after the rising edge of ref clk. Thus, the first rising edge of ref-clk can be virtually hidden and neglected during phase comparison. Due to the nature of the negative feedback architecture, the VCDL delay increases until it is equal to one clock cycle of input signal. Since the start-controlled circuit forces the VCDL delay to its minimum value and causes the VCDL delay to increase until its delay equals one clock cycle, and therefore lock. The DLL will not fall into false locking or harmonic locking. Fig. II.8 shows the acquisition curve of a wide-range DLL that is operating at 1 GHz.

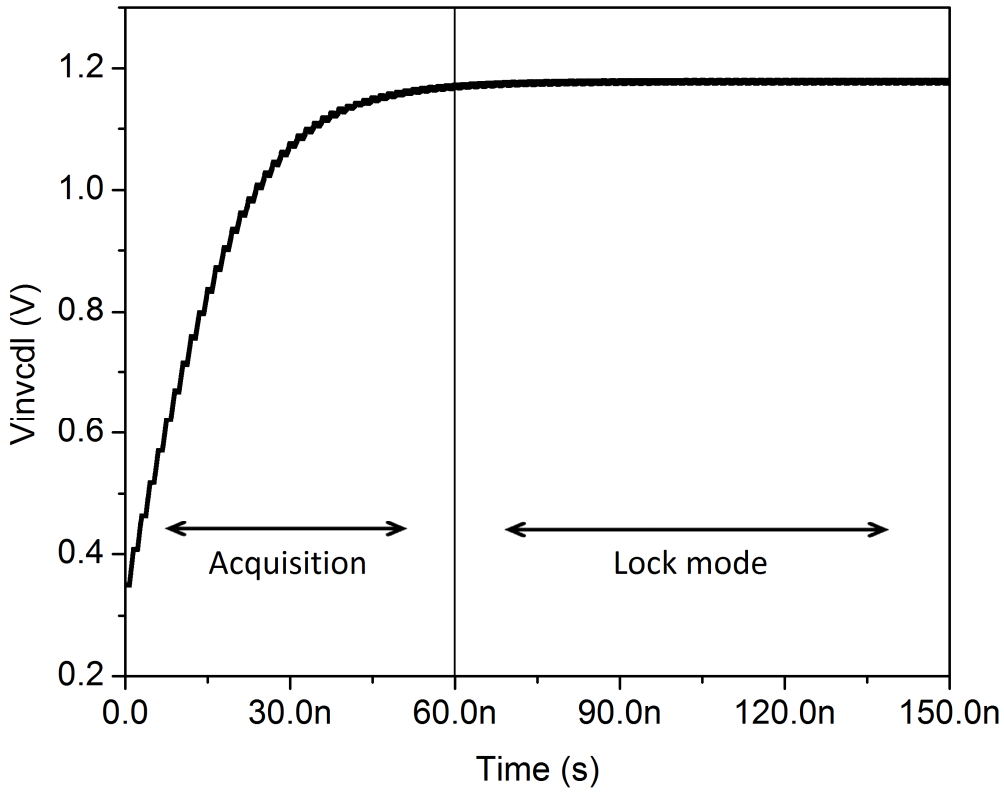


Fig. II.8. Wide-range DLL acquisition curve for operation at 1 GHz

As in the analog DLL, the VCDL is based on a current-starved driver topology, composed of several variable-delay elements connected in series as shown in Fig. II.7, each element controlled by either a voltage or a current. However the initial delay of the wide-range VCDL (WR-VCDL) must be in the range $\pm 2\pi$ of the clock period Tclk. The basic function of the WR-DLL, The low pass filter and the charge pump are similar to the analog DLL topology.

CHAPTER III

SINGLE EVENT RADIATION EFFECT IN MIXED-SIGNAL STRUCTURES

A. Definition of Single-Event effects

Single-event effects (SEE), mostly affecting only digital or mixed-signal devices, are caused by a single, energetic particle. They can be non-destructive, such as soft errors, or destructive like in the case of hard errors. When a high-energy particle travels through a semiconductor, it leaves an ionized track behind. This ionization may cause a highly localized effect such as a transient glitch in an output, a less benign bit flip in memory or a register, or, especially in high-power transistors, a destructive latch-up and burnout. Single event effects have significant importance for electronics in satellites, aircraft, and other both civilian and military aerospace applications. In circuits not involving latches, it is often helpful to introduce RC time constant circuits, slowing down the circuit's reaction time beyond the duration of an SEE. In the space environment, spacecraft designers are concerned with two main causes of single-event effects (SEEs): cosmic rays and high-energy protons. For cosmic rays (energetic particles originating from outer space that impinge on Earth's atmosphere), SEEs are typically caused by its heavy ion component. These heavy ions cause a direct ionization SEE, i.e. if an ion particle passing through a device deposits sufficient charge, an event such as a memory bit flip or transient may occur.

Recent works in PLLs [4, 6-7] show that mixed-signal circuits are particularly sensitive to Single-Event transient. Single-event transient (SET) happens when the charge collected from an ionization event discharges in the form of a spurious signal traveling through the circuit.

B. SEs in Mixed-Signal Circuits: PLLs

As shown in Fig. II.1 (b), the PLL consists of four modules connected in a closed loop to implement a negative feedback action: a phase-frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF) and a voltage-controlled oscillator (VCO). Recent work with computer circuit-level simulation techniques has allow mixed-signal circuit designers, to understand the SET effects in mixed-signal applications such as the digital phase-locked loop [4, 6].

Analyses of the circuit simulations show that the SET response of the PFD module has no significant impact on the overall PLL response, and that this response can be observed for higher operating frequencies [4]. The VCO module exhibits a moderate sensitivity to ion strikes with increasing frequency of oscillation [5], SEs occurring within mixed-signal VCOs generated different undesirable transients, such as output frequency modulation, amplitude modulation, and a temporary loss of oscillation, generating missing or additional pulses so called erroneous pulses [6]. However most importantly, simulations showed that in mixed signal circuit like PLLs, the output stage of the charge pump is the SET vulnerable point in the structure, inducing drastic transient pulses at the voltage node as shown in Fig.III.1. Some of the transients forced the PLL control voltage so low that the input transistors of the VCO module were nearly turned off. With poor current conduction in its biasing transistors, the VCO control voltage changes very abruptly, pulling the analog PLL out of lock and therefore modulating the oscillating frequency of the PLL. Even if the negative feedback progressively corrects the frequency and phase

differences until it reacquires the initial signal, the PLL exhibited a large amount of erroneous pulses (i.e. missing or additional pulses) represented by the maximum phase displacement generated by both the VCO and the CP [5, 6], see Fig III.2.

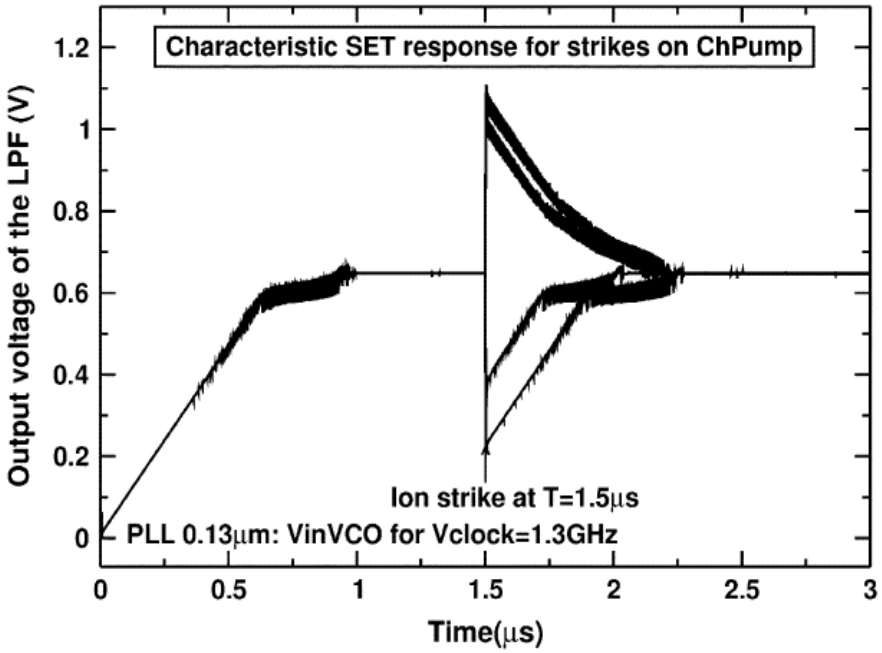


Fig. III.1. SET response of the DPLLs following the ion strikes of the charge pump module: (a) DPLL 0.18 um. (b) DPLL 0.13 um. The current source simulating the ion strike has a total worst case integrated charge of 1 pC [5].

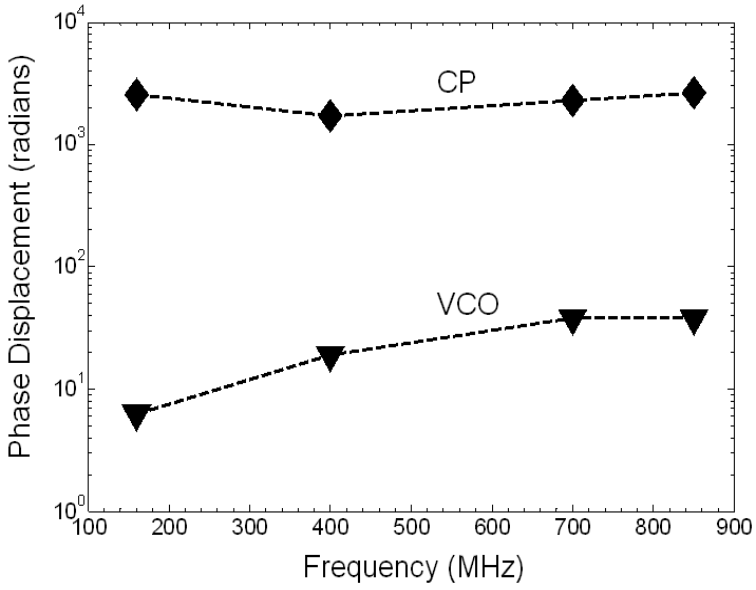


Fig. III.2. Phase locked loop: maximum phase displacement versus operating frequency for charge deposition of 500 fC, where the VCO and the CP both exhibit erroneous pulses [6], and presenting the CP as the most sensitive sub-circuit of the PLL, when compared to the other modules of the circuit [6].

CHAPTER IV

ERRORS SIGNATURE & QUANTIFICATION IN DLLs

Following an ion strike on a DLL sub-circuit, three distinct types of transient errors can occur: erroneous (missing) pulses, inverted lock, and duty-cycle errors. These different errors will be presented by order of relative effect on the reference signal propagation.

A. Error Quantification

All three types of errors can be quantified in terms of phase displacement. Phase displacement and erroneous pulses have been used to characterize the SET response in PLLs [6, 7], and are also useful to analyze the SET vulnerability of the DLL. The phase displacement, Φ_{disp}, represents the time difference between the rising (or falling) edge of $V_{outVCDL}$ and the rising (or falling) edge of the reference signal (*te*), normalized by the period of the reference signal [6]. Additionally, erroneous pulses (missing or additional pulses) can be related to phase displacement by [8]:

$$n = k \ \ for\ 2\pi * k \le \Phi disp \le 2\pi(k+1)\ ,\ k \ge 0 \qquad \text{III.2}$$

Where *n* is the number of erroneous pulses. For example, one erroneous pulse requires at least 2π radians of phase displacement. Additionally, an inverted lock error can be quantified as a multiple of π radians. Fig. IV.1 shows an example of a SET in the output of the DLL following a strike on a PMOS device connected to the output of the VCDL. In this example, the output

phase displacement is equal to 3 ns or 18.8 radians, corresponding to 2 erroneous pulses, for a DLL operating at 1 GHz.

B. Error Signatures

1. *Missing Pulses*

Missing pulses represent the case when one or more pulse(s) are absent from the output. This type of transient error is usually not persistent, but can drastically affect the original signal. The phase displacement Φ_{disp} generated by an ion strike in the DLL can be calculated using the equation [8]:

$$\Phi disp = \frac{(te - Tclk)}{Tclk} * 2\pi \qquad \text{III.1}$$

Where *te* is the time error and *Tclk* the ideal signal period. In Fig. IV.1, a charge deposition of 500 fC (LET ~ 80 MeV-cm^2/mg) in the 1 GHz DLL spreads over 3.5 ns, resulting in 2 missing pulses and a phase displacement of 12.56 radians.

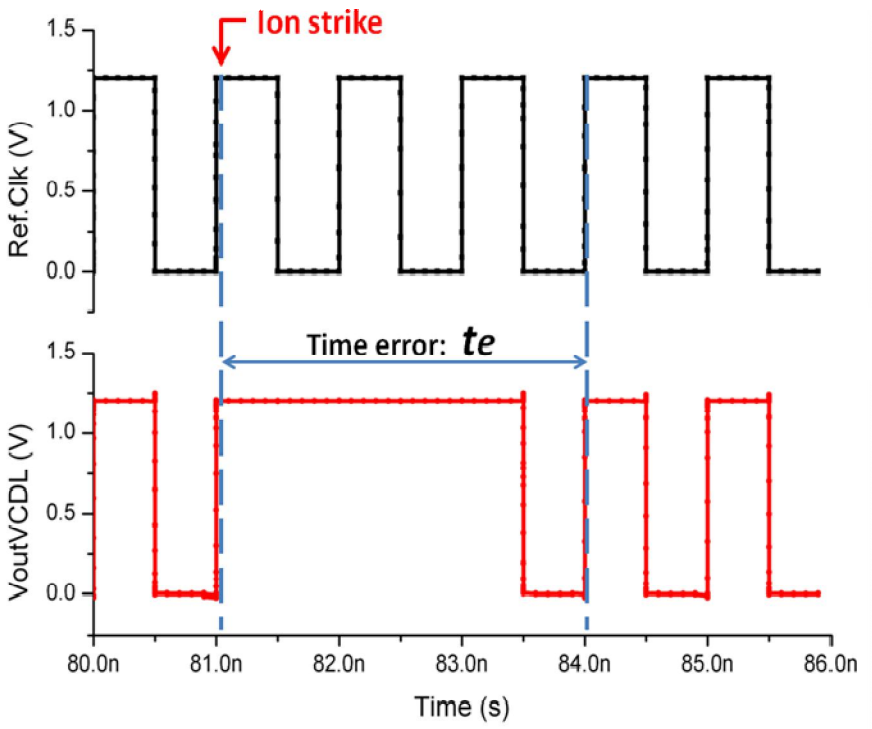


Fig. IV.1. Transient illustrating missing pulses error on DLL at 1 GHz for LET of 10, 20 and 80 MeV-cm^2/mg. The time error *te* is measured to calculate the phase displacement generated by the ion strike.

2. *Inverted Lock Error*

Strikes in the CP may perturb the DLL output in a persistent fashion. This phenomenon can easily be observed using the DLL acquisition curve of Fig. V.4. This figure represents the VCDL input voltage versus time. It is divided into two regions, where the first (grey) region represents the DLL normal operating mode when the system is locked at zero radians of phase difference, (i.e. when *Ref.Clk* and $V_{outVCDL}$ are in phase). This behavior represents the expected response of the DLL. An ion strike in the CP (white region) can force the system out of lock. For a large enough phase perturbation, the DLL may re-acquire the reference signal at π radians rather than 0 radians (due to the phase capture range characteristics of the PD).

This false-lock error is persistent and results in a constant phase displacement of π. Fig. IV.2 shows an example of a transient resulting from a strike in the CP sub-circuit and the resulting false lock. Because the VCDL delay differs in false lock as compared to the original delay, the final control voltage V_{inVCDL} will settle to a new value as seen in Fig. IV.2.

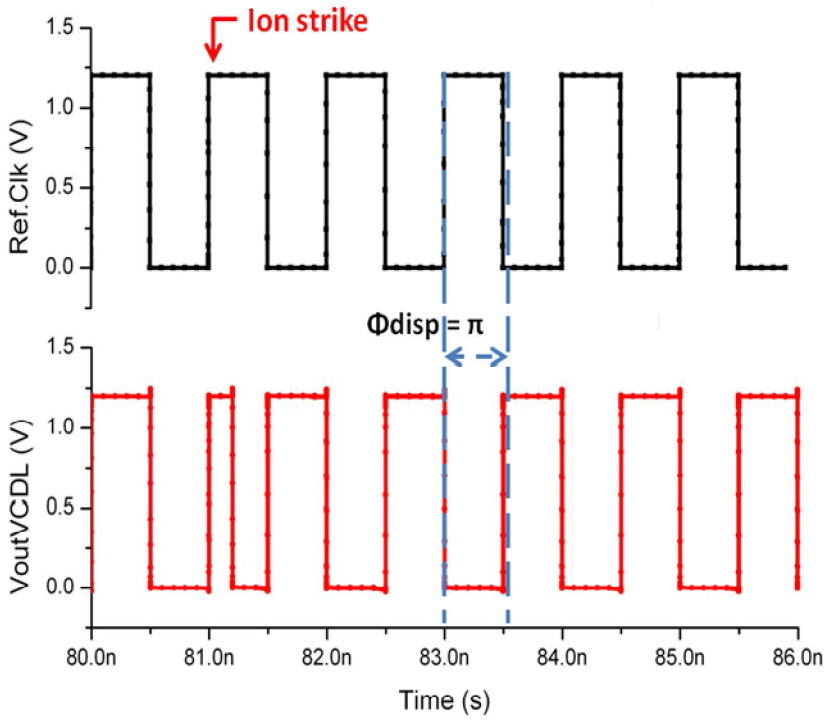


Fig. IV.2. Transient illustrating persistent inverted lock error, on DLL at 1 GHz for LET of 80 MeV-cm^2/mg.

3. Duty-Cycle Errors

Duty-cycle errors represent the specific case where the logic HIGH/LOW pulse widths differ. In general, this type of error will not affect more than two pulses, as larger duty-cycle errors tend to become false lock errors.

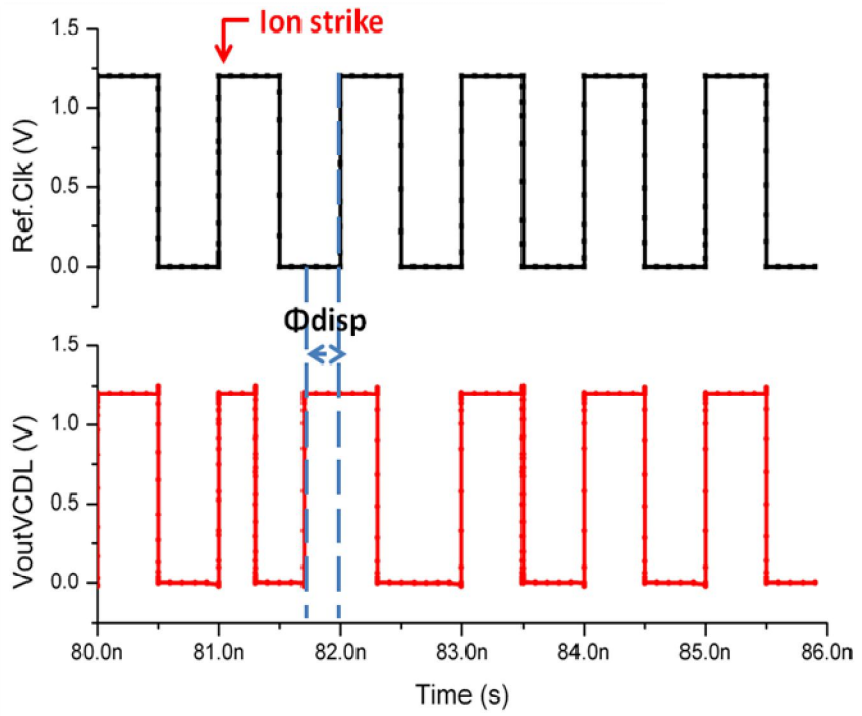


Fig. IV.3. Transient illustrating duty cycle errors on an analog DLL operating at 1 GHz for LET of 10, 20 and 80 MeV-cm^2/mg.

CHAPTER V

CUSTOM ANALOG DLLs DESIGN

A. Design Choices for the Conventional Analog DLL Sub-circuits

1. Phase Detector (PD)

A dynamic PD, illustrated in Fig V.1, with the truth table shown in Table V.1, was chosen as the phase detector due to its reduced phase offset at higher operating frequencies, compared to other phase detector topologies. The dynamic PD design is derived from the frequency detector [10] by removing a feedback path and replacing the feedback input with a Ref.clk or Vout.VCDL signal. Also this topology has been chosen in order to minimize the power consumption of the designed analog DLL, since it uses fewer transistors than other PD design like the Hogge-PD, 16 transistors versus 64 transistors respectively. With a PMOS W/L ratio of 480 nm/ 80 nm and an NMOS W/L ratio of 200 n / 80 nm, the dead zone of the overall DLL can be reduced to 36 ps.

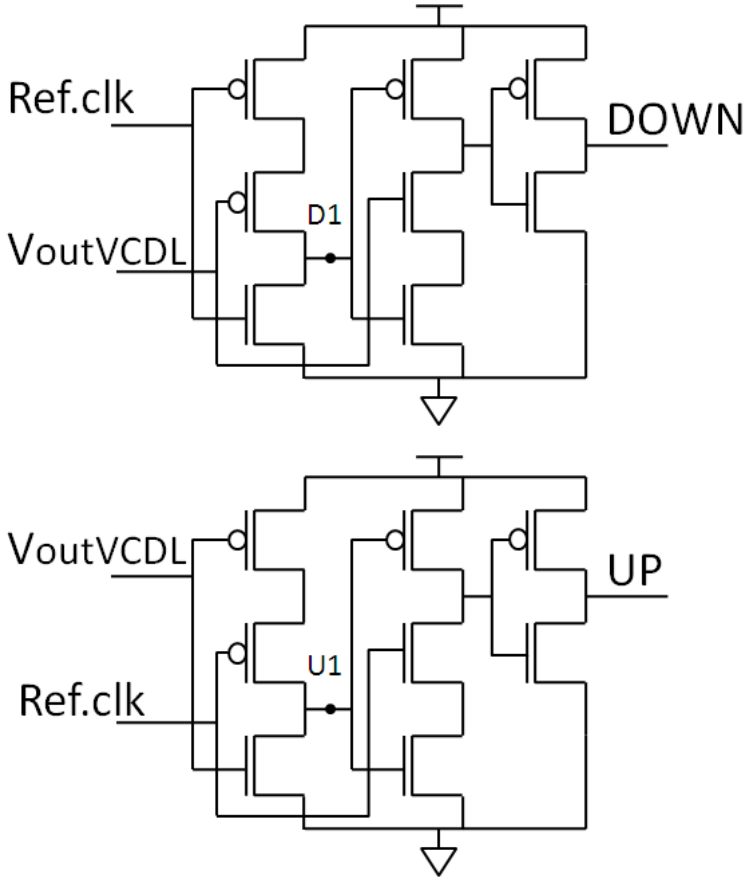


Fig. V.1. Dynamic phase detector schematic.

TABLE V.1: PD truth table.

Ref.clk	VoutVCDL	D1	U1	DOWN	UP	Lock phase
1	**1**	0	0	0	0	0
1	**0**	X	0	X	0	π
0	**1**	0	X	0	X	-π
0	**0**	1	1	X	X	--

Table V.1. Dynamic phase detector truth table: X represents undetermined states where the output of the PD depends on nodes D1 and U1 (Fig. V.1).

2. Voltage-Controlled Delay Line (VCDL)

The VCDL is based on a current-starved driver topology, composed of several variable-delay elements connected in series as shown in Fig. V.2 to provide a variable delay of the input clock signal. To design analog DLLs operating between 500 MHz and 1 GHz, an arbitrary 125 ps delay line was chosen and designed for the VCDL. Approximately 8 stages are needed to design a 1 GHz DLL and 32 stages for a 500 MHz operating frequency. The width-to-length ratio of the biasing transistors MPbias (580 nm / 80 nm), MNbias (340 nm / 80 nm), MNb1 (480 nm / 80 nm), MNb1 (340 nm/ 80 nm), and the inverters MP1 (960 nm/ 80 nm) and MN1 (400 nm / 80 nm) were designed with minimum size to preserve the power consumption.

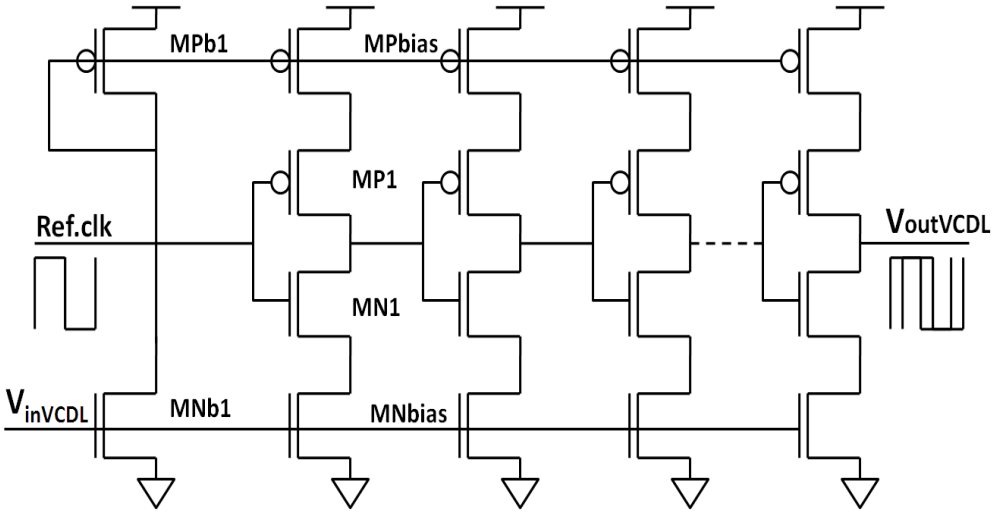


Fig. V.3. Current starved VCDL.

3. *Charge Pump (CP) and Low Pass Filter (LPF)*

The charge pump design used to design the analog DLLs have been chosen based on the charge pump topology used in the digital PLL used in [5, 6], but also because this design was used successfully as a base for the tri-state CP presented in CHAPTER VIII used to harden the conventional analog DLL. The output current of the charge pump is approximately 250 nA, this arbitrary value was chosen in order to minimize the analog DLL power consumption

The value of the capacitor C in the low pass filter was calculated using Eqn. I.1 [3]. The number of clock cycles before locking was arbitrarily set to 50 cycles. Equation A.2 was used to estimate the VCDL gain, and the charge pump current Ipump set to 250 nA. Figure II.4 show the acquisition curve of the conventional analog DLL operating at 1GHz, locking at approximately 50ns, or 50 clock cycles since 1 clock cycle is 1 ns in duration.

The width-to-length (W/L) ratio of the transistors in region 1 (Fig V.4), are 900 nm / 900 nm for the NFET and 3.5 µm / 80 nm for the PFET. In region 2 the W/L ratios are PMOS = 2.74 µm / 160 nm, NMOS = 1.14 µm / 160 nm for the pass gates, and PMOS = 480 nm / 80 nm and NMOS = 200 nm / 80 nm for the inverters. In zone 3 the PMOS W/L ratio is 4.23 µm / 3 µm, and in zone 4 the NMOS W/L ratio is 3.57 µm / 1 µm.

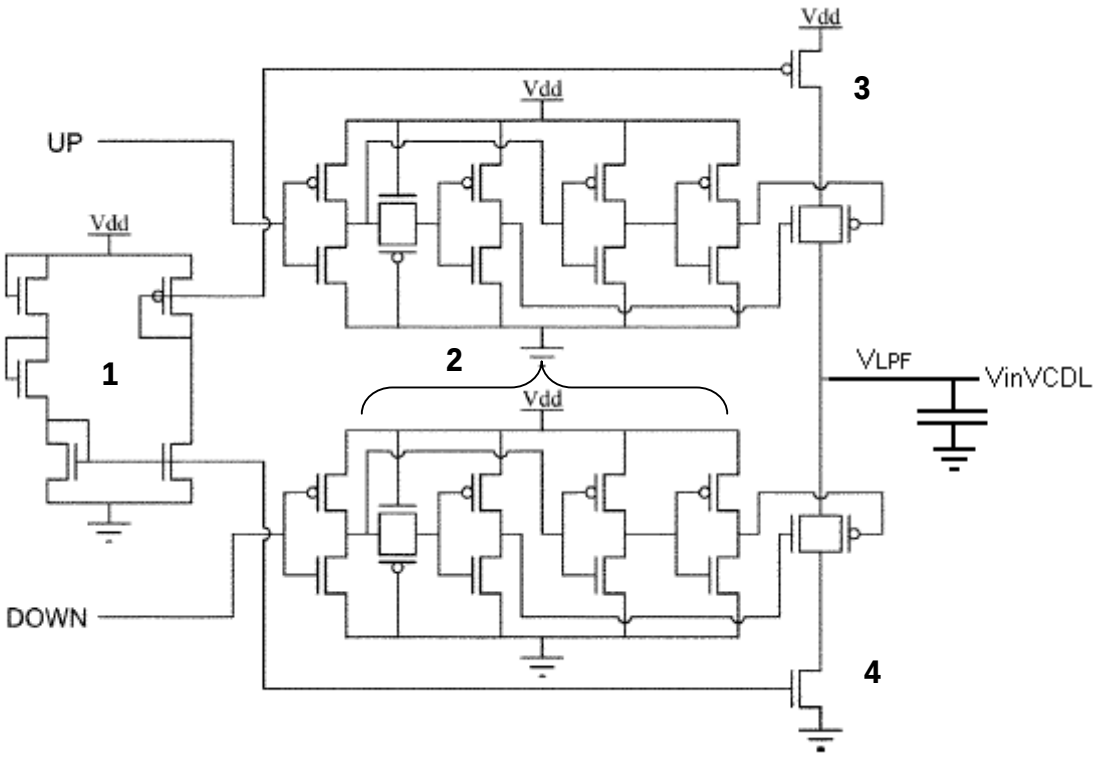


Fig. V.4. Schematic of the charge pump with low pass filter [5].

A. Design Choices for the Wide-Range DLL Sub-circuits

1. *The Start Controlled PFD*

A resettable dynamic D-flip-flop (DFF) based start-controlled PFD [4], as illustrated in Fig V.4, was used for the designed wide-range DLLs. This design requires less circuit area and less power consumption, than the other PFD with controlled circuit topologies. This design requires 52 transistors versus 104 transistors for the start controlled PFD in [1] or 120 transistors in [2]. The control circuit in Fig V.5 is composed by a single resettable D-flip-flop (see APPENDIX B, Fig B.1), the PFD is composed by 2 resettable D-flip-flop and 2 NAND gates.

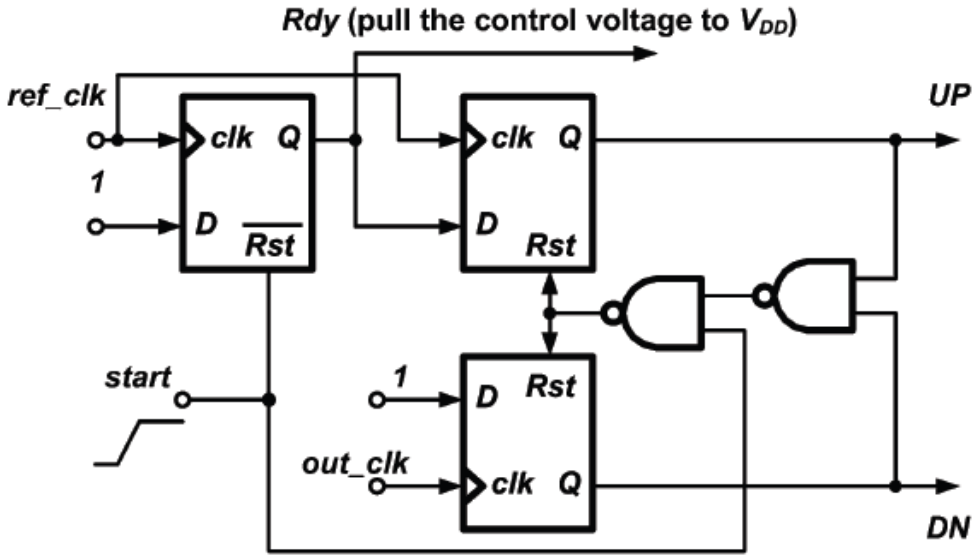


Fig. V.5. Schematic block of the PFD with control circuit [4]

CHAPTER VI

SIMULATION SETUP

Single-event transient (SET) simulations were performed on the DLL sub-circuits using ion-induced current profiles obtained from 3D TCAD models calibrated to the IBM 90-nm CMOS9SF bulk process [11]. Four analog and four wide-range DLL circuits were designed for operating frequencies of 500 MHz, 700 MHz, 850 MHz and 1 GHz, respectively.

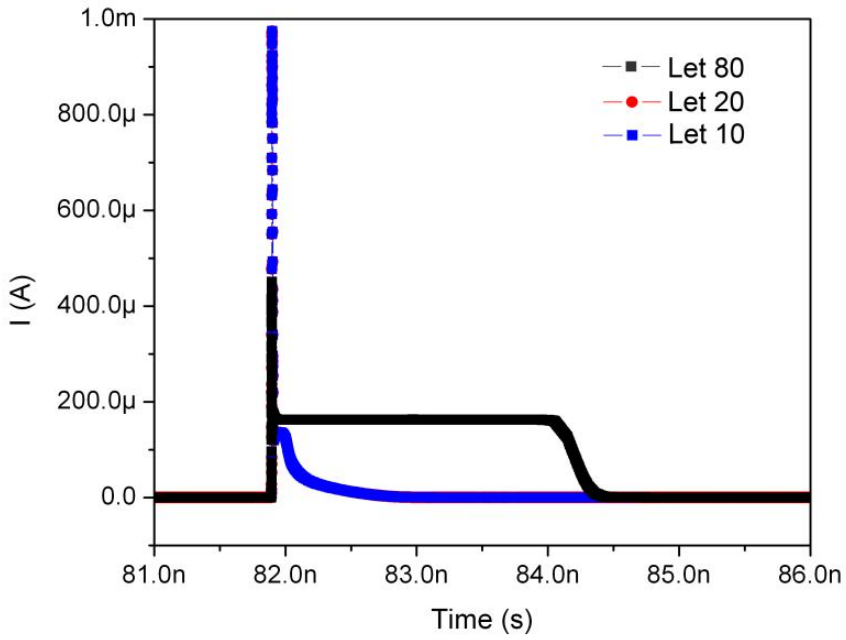


Fig. VI.1. Ion-induced current profiles obtained from 3D TCAD models calibrated to the IBM 90 nm CMOS9SF bulk process, for linear-energy-transfer (LET) values of 10 MeV-cm^2/mg, 20 MeV-cm^2/mg and 80 MeV-cm^2/mg.

The SET response of the DLL was simulated for linear-energy-transfer (LET) values of 10 MeV-cm^2/mg, 20 MeV-cm^2/mg and 80 MeV-cm^2/mg, illustrated Fig VI.1. The ion current profiles were calibrated using inverter with width-length ratio of 480 nm / 80 nm and 200 nm / 80 nm, for respectively the PMOS and NMOS, and were used to simulate the SET response of PLL, using current-starved based VCO. The current starved topology was also used as a base of the VCDL module in analog DLLs. Also this type of simulation approach, utilizing extracted TCAD ion-induced current profiles, has been shown effective through the experimental validation of the SET response of similar mixed-signal topologies and in relatively comparing different RHBD designs [6-7, 9]. The ion-strike current profiles for three different LET values were applied to each of the DLL sub-circuit nodes displayed in Fig. VI.1. Additionally the ion strike profiles were applied at different times in the clock period. The phase displacement, the number of erroneous clock pulses, and the output signal duty cycle errors were measured for all cases.

A. Critical Nodes in DLLs

In the PD module, ion strikes on nodes U1 and D1 (Fig V.1) resulted in the majority of perturbations at the output of the DLL. This result can be explained by considering the PD functionality. In some cases the PD outputs are undetermined as shown by the truth table (Table I), and therefore will depend on the sub-circuit's previous state and on the state of nodes U1/D1.

In the CP, the critical nodes are in the output stage, which consists of two current sources and two transmission gates. The output stage of the CP is connected directly to the capacitor of the LPF, which stores voltage V_{inVCDL}. An SE strike at this node will either deplete or deposit

charge on the LPF capacitor, thus directly affecting voltage V_{inVCDL}. The rate at which this charge error is removed or restored by the CP determines the SE response of the DLL.

Because each VCDL delay stage is identical, with identical sensitivities, the critical nodes consisted of the drains of the current source/sink transistors, and the sources and drains of the current-starved inverter transistors connected between them. Strikes on the PFETs resulted in slightly more variation in the DLL responses as compared to strikes on the NFETs. The VCDL bias circuit was also determined to be sensitive to ion strikes, with strikes creating perturbations in all stages simultaneously.

CHAPTER VII

ANALYSIS OF DLL SET VULNERABILITY

After simulating and quantifying the SET error signatures of the DLL sub-circuits, a strong correlation was found between the sub-circuit exposed to an ion strike and the vulnerability of the DLL to SETs. After each simulated ion strike, the perturbations induced in the steady-state operating conditions of the DLL were measured. Due to the large amount of data produced by the simulations, the analysis was limited to worst-case simulated strikes, i.e. a linear energy transfer of 80 MeV-cm^2/mg.

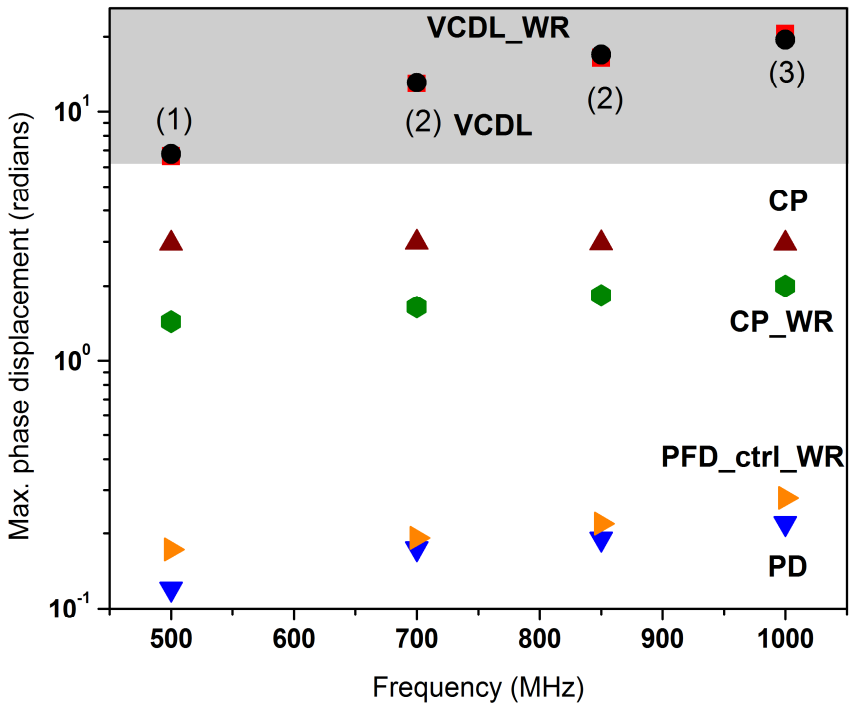


Fig. VII.1. DLL SET response in terms of erroneous pulses/phase displacement vs. operating frequency (500, 700, 850 MHz and 1 GHz) for LET 80 MeV-cm^2/mg. The grey region shows where missing pulses are observed, where no missing pulses are observed in the white region. The numbers in parenthesis are the maximum number of missing pulses observed after an ion strike.

Fig. VII.1 illustrates the phase displacement and number of erroneous pulses, respectively, for four operating frequencies (500 MHz, 700 MHz, 850 MHz and 1 GHz), and for the different DLLs modules, the phase detector (PD), charge pump (CP), the voltage controlled delay line (VCDL) for the conventional DLL, and the start controlled phase frequency detector (PFD_ctrl), the charge pump (CP_WR) and the voltage controlled delay line (VCDL_WR) of the wide range DLL. The figure is divided in two parts, the white parts represents the area where no missing pulses are observed, as the phase displacement error is less that 2π radians. The grey region shows where erroneous pulses were observed with a phase displacement greater than 2π

radians. The numbers in parenthesis are the maximum number of missing pulses for each operating frequency.

A. Analysis of PD and PFD/Control Circuit Vulnerability

The phase detector exhibits a maximum phase displacement approximately two orders of magnitude below that of the VCDL. Additionally, no erroneous pulses or significant phase displacement errors were observed due to strikes in the PD. Therefore, as was previously observed with the PLL PFD sub-circuit [4] and in the wide-range DLL PFD with control circuit module, ion strikes on the DLL phase detector result in no significant errors at the output. This result is a consequence of the continuous signal comparison of the PD or the PFD, reducing the sub-circuit's output signal perturbation duration after an ion strike. The PD or PFD, comparison process is much faster than the DLL response time, which corrects the error before the CP can significantly alter the VCDL input voltage value. The dead zone of the PD is less than 40 ps, and slightly decreases with operating frequency, so the PD phase displacement will increase as the operating frequency increases. The decreasing dead zone effectively increases the PD lock range slightly. Fig. VI.3 illustrates the phenomenon with the PD dead zone, for a strike on the current CP of a 1 GHz DLL with an LET of 20 MeV-cm^2/mg. After the phase perturbation, the value of V_{inVCDL} is different from the original locking value, thus allowing one to identify the dead zone bounds.

B. Analysis of Voltage-Controlled Delay Line Vulnerability

As shown in Fig. VII.1, the VCDL presents the highest sensitivity to irradiation, and is the dominant contributor to the SET vulnerability of both of the DLL topologies. Strikes in the VCDL result in significantly larger phase displacement values over any other DLL sub-circuit, and the phase displacement increases for increasing clock frequency. Also, as illustrated in Fig. VII.1, the VCDL is the only DLL sub-circuit that can create erroneous pulses at the output. The maximum phase displacement and the number of erroneous pulses both increase with increasing operating frequency, and strikes within any stage the VCDL, including the bias circuit, can result in erroneous output pulses and duty cycle errors.

C. Analysis of the Charge Pump Vulnerability

Depending on the topology used the sensitivity to SET of the CP at worst-case SET response varies.

1. SET in the Analog DLL

An ion strike in the charge pump (CP) results in the second highest phase displacement as well as the longest recovery time after irradiation. A maximum recovery time of 295 ns was measured for strikes in the CP at an LET of 80 MeV-cm^2/mg. Similar strikes in the VCDL and PD sub-circuits did not result in persistent errors. Therefore, in terms of recovery time, the strikes in the CP result in the worst-case response. However, as the PD acquisition range ($\pm \pi$ radians) can result in a DLL lock at 0 or π radians out of phase, the DLL is expected to return to a stable locked condition following the ion strike where the input and reference signal are π radians out of phase rather than the initial locked condition of 0 radians. Therefore, regardless of

the operating frequency, the maximum phase displacement for strikes in the CP is π radians, as shown in Fig. VII.2. Consequently, no erroneous clock pulses were measured for any simulated LET values for SE hits on the CP. This is in contrast to previous studies on PLL circuits [2-4] where phase displacement values at least 2 orders of magnitude greater than π radians were observed for hits on CP. Strikes in the CP of a PLL, for example, can generate phase displacement values and erroneous pulses orders of magnitude larger than ion strikes on any other sub-circuit, as these strikes perturb the VCO's control voltage and modify the PLL's output frequency. Because the DLL does not contain an internal oscillator, any changes in the VCDL's control voltage in a DLL result in only phase errors, and cannot modulate the output frequency.

For the worst-case simulated LET strike, the CP was the only sub-circuit exhibiting the inverted lock error. This error is a consequence of the CP/ LPF and PD operating modes. The ion strike forces the VCDL input voltage to change abruptly, thereby drastically changing the DLL output delay and inducing the DLL to leave the lock condition. As the PD acquisition range is ± π, the system will false lock at this phase instead of recovering to 0 phase radians (as can be observed in Fig. VII.3, for a strike within the CP at LET 20 MeV-cm2/mg, leading to a permanent phase error at π radians.

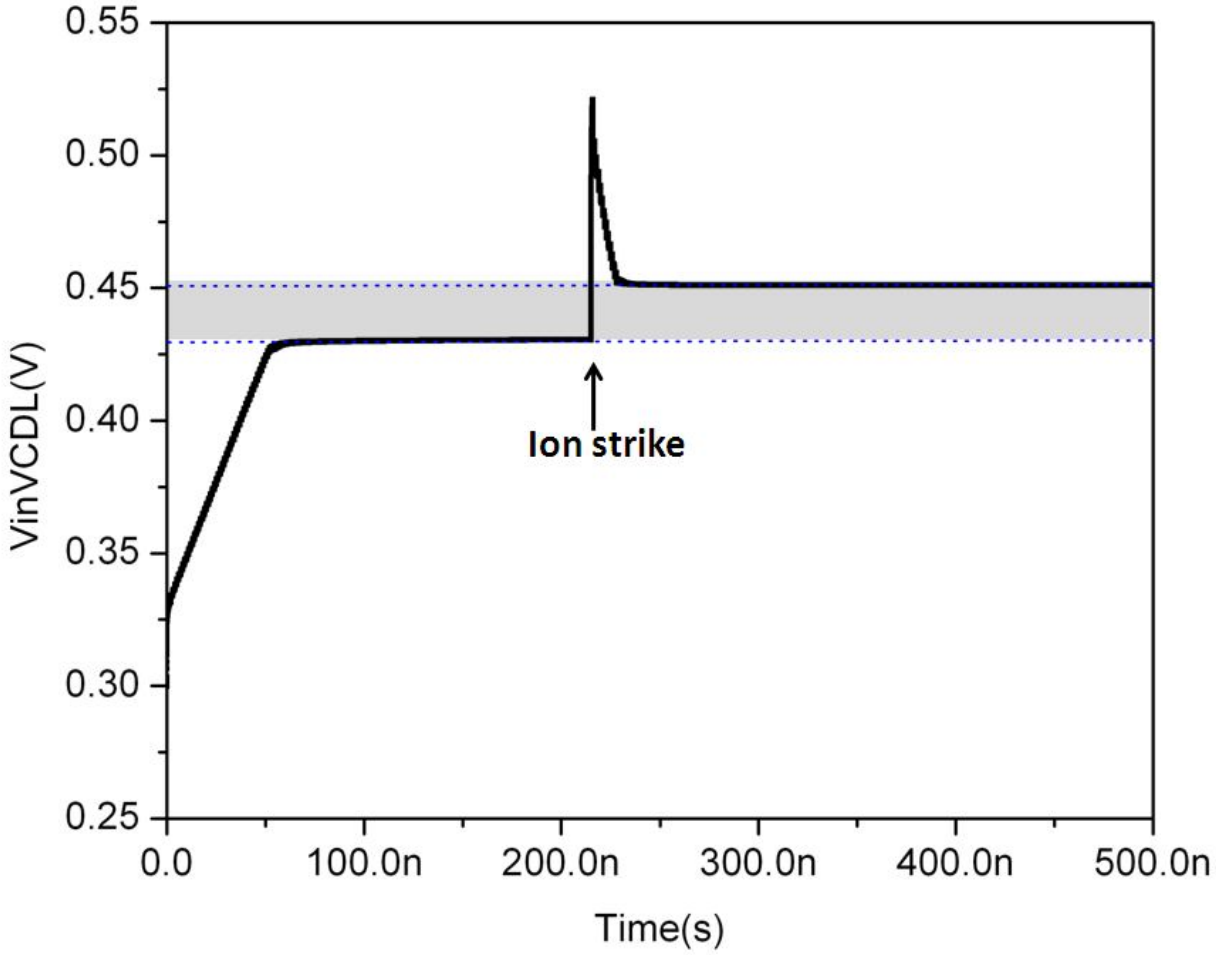


Fig. VII.3. Illustration of the PD dead zone phenomenon for a 1 GHZ DLL acquisition curve with strike on the CP for an LET of 20 MeV-cm^2/mg, generating a significant phase shifts. VCDL input voltage V_{inVCDL} does not regain its original voltage value after the perturbation because of the dead zone (grey region).

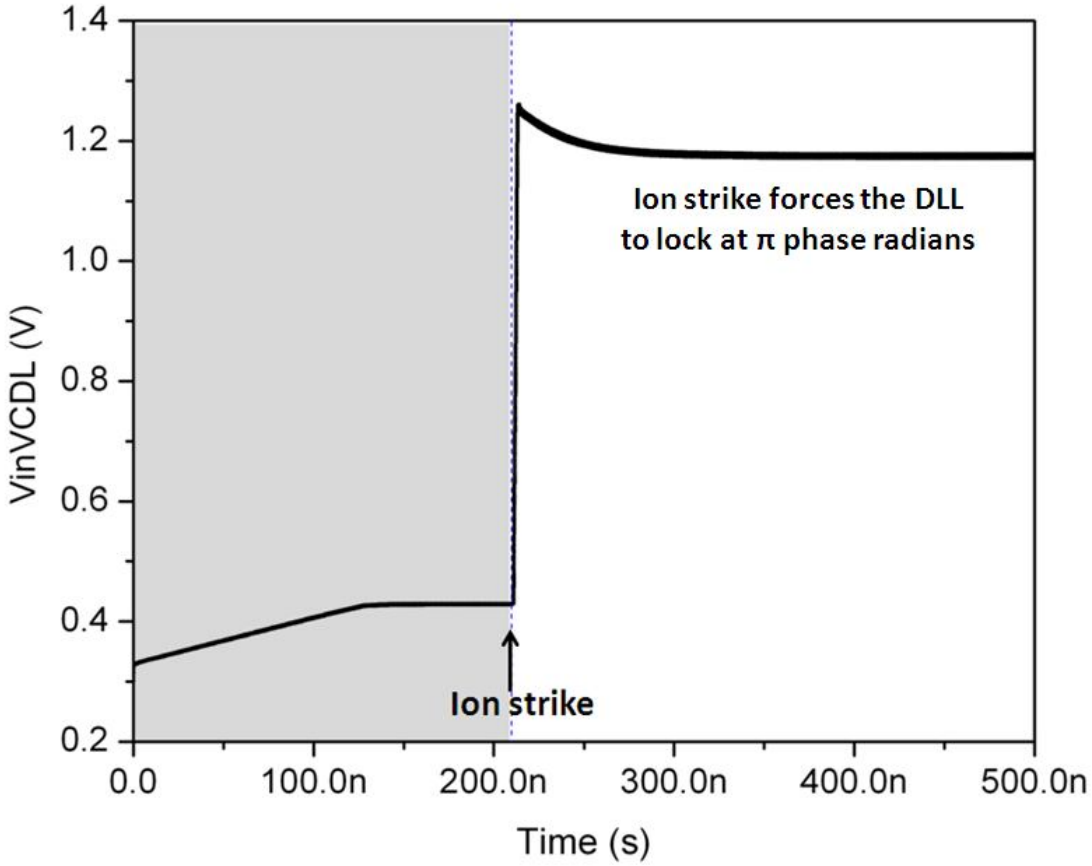


Fig. VII.4. DLL acquisition curve, at 1 GHz for an LET of 80 MeV-cm^2/mg, illustrating the persistent inverted lock error generated by an ion strike in the analog DLL charge pump.

2. SET in the Wide-Range DLL

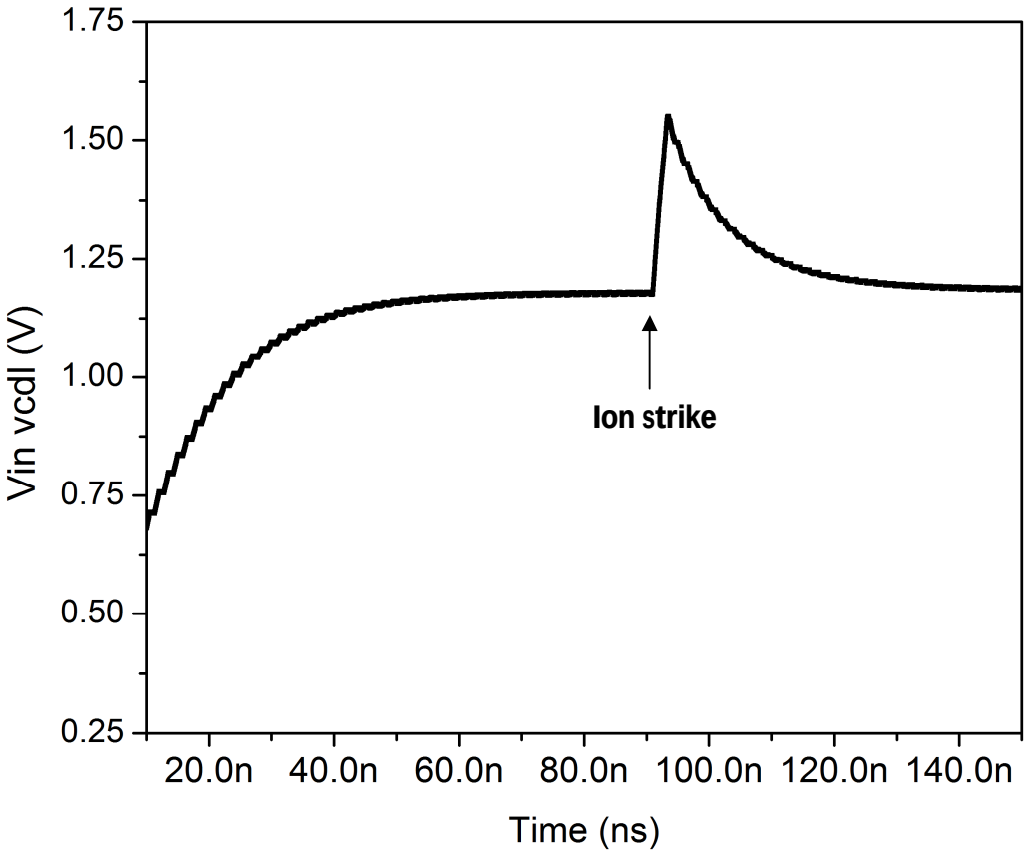


Fig. VII.5. Wide-range DLL acquisition curve operating at 1 GHz, illustrating the SET response of the WR-DLL after an ion strike within the CP.

For the worst-case simulated LET strike, as shown Fig VII.5, the CP in the wide-range DLL exhibit SET response similar to the acquisition curves observed for a strike within the charge pump in digital PLL [2], or for the analog DLL at lower LETs as shown in figure VII.3. As in the analog DLL, the ion strike forces the VCDL input voltage to change abruptly, thereby drastically changing the DLL output delay and inducing the DLL to leave the lock condition. But

since in this case the PFD detector capture range is between ± 2π, the DLL will recover to 0 or ± 2π phase radians at LET 80 MeV-cm2/mg. Therefore, no inverted lock error was recorded for the worst case of SET response, representing an advantage in terms of naturally harder topology when compared to analog DLLs. The SET response in term of phase displacement of the wide-range DLL will be better than for the analog DLL, since this topology will never generate an inverted-lock error after an ion strike within the charge pump.

When comparing both DLLs topologies, the observed SET responses generated by the VCDLs and the phase detector or phase frequency detector / control circuit are very similar. The main difference resides in the CP sensitivity to ion strike, for the analog topology in the worst case the module generated inverted lock error, that can be mitigated using voltage-based charge pump RHBD technique, or using wide-range DLL that presented phase error but no permanent missing pulses error.

The SET responses observed in the DLL for strikes on the VCDL and the CP have different signatures when compared to those of a PLL. In the PLL, the charge pump was the most sensitive sub-circuit, followed by the voltage-controlled oscillator (Fig. III.2). In contrast, the VCDL is the most sensitive sub-circuit of the DLL, as this sub-circuit exhibited the highest phase displacement along with missing pulses. The CP had the second highest phase displacement of the system, but also generated the persistent inverted lock error.

The effects of SETs on a mixed-signal analog and wide-range delay-locked loop have been analyzed, for operating frequencies of 500 MHz, 700 MHz, 850 MHz and 1 GHz. Simulations showed that single-events in the phase detector have little impact on the DLL output signal in lock mode. Strikes in the PD or the start-controlled PFD modules have no significant impact on the DLLs. While strikes in the charge pump resulted in moderate phase displacement values and increased recovery times at the output of the DLL, no erroneous output pulses were observed. However, an ion strike on the CP can generate a false lock (or inverted lock) error, which is the only persistent single-event error observed in the DLL. In terms of phase displacement and erroneous pulses, the VCDL exhibited the highest vulnerability in the DLL, with ion strikes leading to worst-case SET error signatures. This analysis indicates that hardening efforts that are focused on the VCDL and CP will provide the greatest benefit in terms of designing an RHBD delay-locked loop circuit. In the next section a RHBD solution used in PLLs [6] is implemented to mitigate the inverted lock error in analog DLLs.

CHAPTER VIII

RHBD SOLUTIONS for DLL:

INVERTED-LOCK ERROR MITIGATION

A. The Voltage-Based Charge Pump (V_CP)

The inverted-lock error can be considered a worst-case error for many applications, because it will not self-correct in the basic DLL topology. Therefore this error needs to be migrated in analog DLLs.

Most modern charge pumps are current-based since voltage-based (also called tri-state) charge pumps can be significantly affected by power supply fluctuations. As in current based CPs the output stage of the sub-circuit is directly connected to the capacitive node of the LPF. A SE strike in this sector will either deplete or deposit charge on the LPF capacitor, thus directly affecting the VCDL control voltage by abruptly increasing or decreasing the voltage and therefore forcing the DLL to exit the lock mode. When the voltage perturbation reaches, or goes beyond a critical value (900 mV for the 90-nm analog design), the DLL will permanently lock to $\pm \pi$, inducing an inverted-lock error (Ref. Fig. VII.4). The pace at which this deposited charge is removed by the CP determines the maximum voltage perturbation of the VCDL input voltage and therefore the SE response of the DLL. One possible solution to mitigate the inverted-lock error in analog DLLs is to use a tri-state charge pump, also called a voltage-based charge pump, which was successfully applied to an RBHD mixed-signal PLL [6]. Because the inverted lock error is a false lock error, another possible solution is to implement a false lock detection circuit,

like wide-range DLLs, which forces the DLL back into normal lock state and therefore mitigates the error.

In this chapter we implement a voltage-base CP as a RHBD technique to mitigate the permanent inverted-lock error, induced by an ion strike within current based CP in analog DLLs.

1. *Topology Description*

The assumption behind the voltage-based CP (V_CP) and LPF design, (illustrated in Fig. C.1), is to reduce the number of vulnerable nodes present in the CP, by reducing the number of current sources, increase the rate of charge sourcing and sinking and provide a mechanism to isolate the vulnerable nodes from the SE sensitive capacitive nodes of the LPF. The V_CP is implemented using two transmission gates that are controlled by "dead-zone" circuitry to ensure simultaneous switching [6]. In addition, a series resistance, R is used on the output of the module, to separate the voltage based charge pump from the VCDL input voltage (Vin.vcdl) in the LPF.

A voltage-based CP can improve the speed of the acquisition since the current is not limited to a fixed value set by current sources [3], provided an appropriate resistor value for R is chosen. Upon start-up, a large amount of current can flow from the V_CP into the LPF to quickly increase VCDL control voltage. However, as the current magnitude depends strongly on the voltage on the LPF capacitor, a voltage increase on Vin.VCDL will decrease the current flow, resulting in a non-linear response in the acquisition period. This large initial current may cause voltage spikes in the power supply node, and precautions need to be taken when implementing the V_CP, in order to avoid power supply fluctuations. Therefore after an ion strike in the module we can observe a very significant improvement in terms of transient

response of the circuit. As simulation results show in the next section, using the VCP is a good solution to mitigate the inverted lock error generated by the current dependence of the CP since the strike doesn't directly affect the capacitor on the output of the circuit.

B. Implementation of the Voltage Charge Pump in the Analog DLL

1. *Simulation Analysis Setup*

Four analog DLL using voltage based CP were designed for operating frequencies of 500 MHz, 700 MHz, 850 MHz and 1 GHz, respectively, in the IBM 90-nm PDK. The other parameters used to simulate the SET in the DLLs are similar to the ones described in the CHAPTER VI.

2. *Simulation Analysis and Comparison with Wide-Range SET Response*

Figure VIII.1. shows the implementation of the voltage based charge pump RHBD technique in an analog DLL. The simulation for worst-case SET response shows that using a voltage-based charge pump improves the speed of the acquisition since the current is not limited to a fixed value set by current sources. Since in charge pump topology the current magnitude depends on the voltage on the LPF capacitors, a voltage increase on the output resistor of the LPF [3], will decrease the current flow, and therefore the voltage perturbation response in the acquisition period, resulting in a voltage perturbation of the VCDL input voltage, under the critical value for the worst LET value, as shown in Fig.VIII.1.

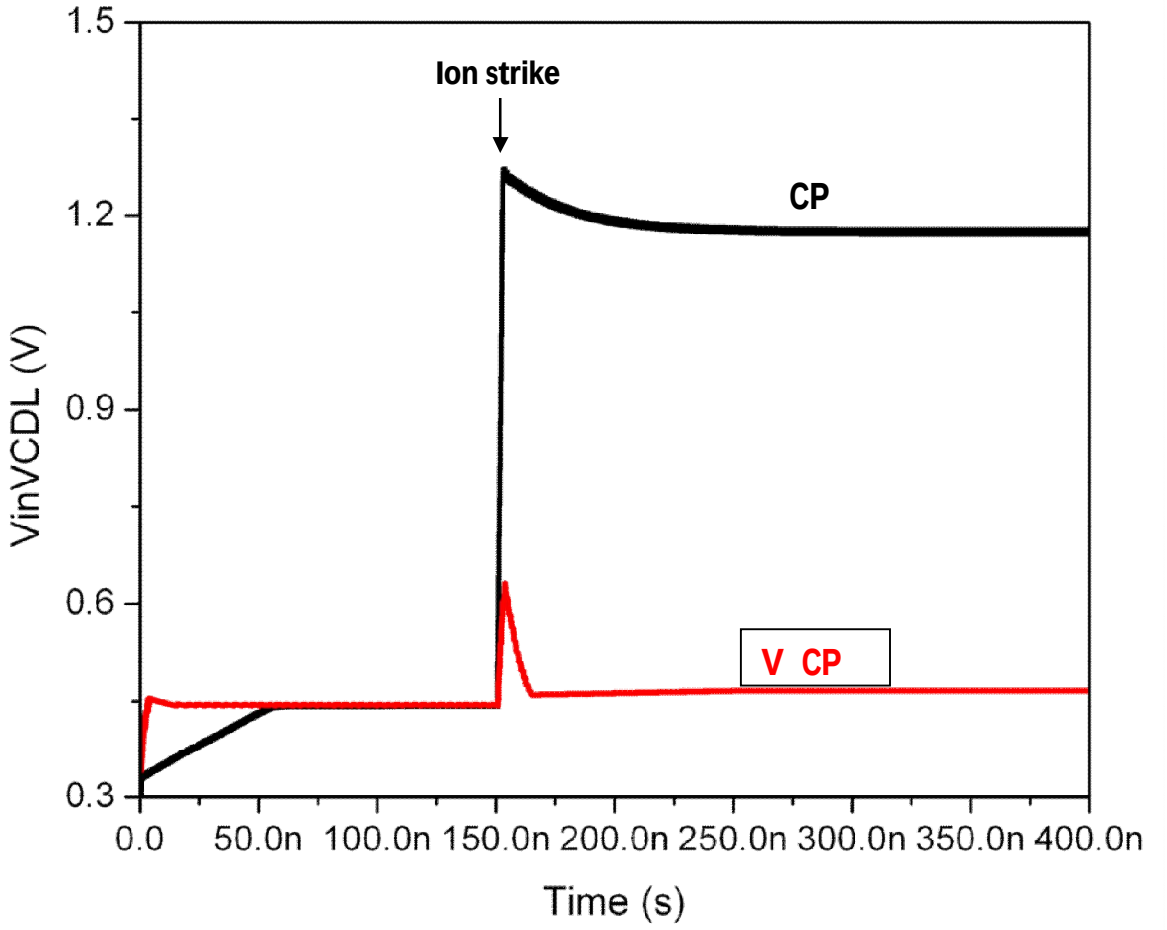


Fig. VIII.1. DLL transient response before (black) and after (red) implementation of the voltage-based charge pump for an LET of 80 MeV-cm^2/mg, the phase error is significantly reduce using the RHBD technique since the VCDL input voltage V_{inVCDL} does not reach the critical value generating (900 mV) generating inverted-lock errors.

The DLLs maximum phase displacement versus the operating frequency, Fig.VIII.2, shows that the voltage-based charge pump (V_CP) dramatically reduces the impact of an ion-strike on the DLL, but also provided better results in terms of reduced sensitivity of the DLL when compared to the wide-range DLL SET response after a strike within the charge pump (CP_WR), as shown in figure VIII.2. However the main problem with voltage-based CP is its

sensitivity to power supply variations that can significantly affect the output voltage. Therefore, in the case where power fluctuations are a concern, a wide-range DLL using a phase frequency detector (PFD) instead of a PD is a better candidate.

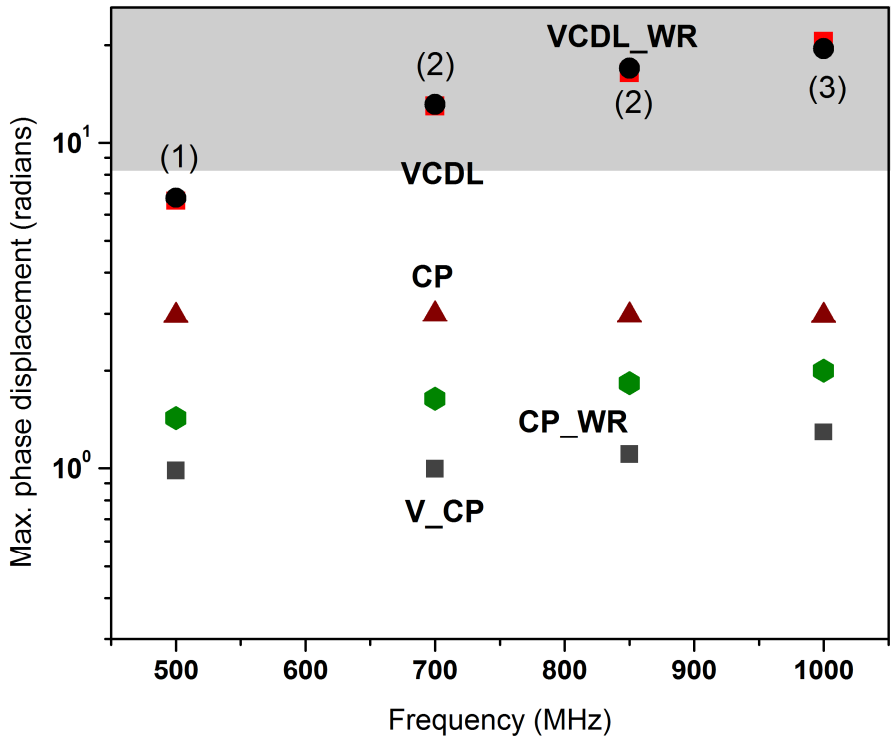


Fig. VIII.2. . DLL SET response in terms of erroneous pulses/phase displacement vs. operating frequency (500, 700, 850 MHz and 1 GHz) for LET 80 MeV-cm^2/mg, with implementation of the voltage-based charge pump in the analog DLL. The grey region shows where missing pulses are observed, where no missing pulses are observed in the white region. The numbers in parenthesis are the maximum number of missing pulses observed after an ion strike.

CONCLUSION

The effects of SETs on a mixed-signal, analog and wide-range delay-locked loop have been analyzed. This analysis was performed for a wide range of LET values (10, 20, and 80 MeV-cm2/mg) and for operating frequencies of 500 MHz, 700 MHz, 850 MHz and 1 GHz. Simulations showed that single-events in the phase detector or the phase frequency detector for wide-range DLL have little impact on the DLL output signal in lock mode. Strikes in the charge pump resulted in moderate phase displacement values and increased recovery times at the output of the DLL, but no missing output pulses were observed. However, an ion strike on the CP can generate a persistent false lock (or inverted lock) error in the analog DLL, when an ion strike within the CP of a wide-range DLL generates no inverted lock error. Simulation results also showed and verified that the implementation of a voltage-based CP in the analog DLL was a very efficient RHBD technique to mitigate inverted-lock errors generated by the CP, and presented better SET response than the wide-range DLL. In terms of phase displacement and erroneous pulses, the VCDL exhibited the highest vulnerability in the DLL for both topologies, with ion strikes leading to worst-case SET error signatures. This analysis indicates that hardening efforts that are focused on the VCDL will provide the greatest benefit in terms of designing an RHBD delay-locked loop circuit.

APPENDIX A

DELAY LOCKED LOOP DESIGN EQUATIONS

The phase output, in radians, is related to the phase of the reference signal the equation:

$$\Phi out = \Phi in + to * \frac{2\pi}{Tclk} \qquad Eq. \quad A.1$$

The delay to can be written in terms of the VCDL gain, K*v*, and the VCDL input voltage Vin.vcdl by the equation,

$$to = Kv * Vin.vcdl \qquad Eq. \quad A.2$$

The output of the DLL loop filter, also the VCDL input voltage Vin.vcdl can be written as a function of the charge pump current Ipump and the low pass filter capacitor C,

$$Vin.vcdl = -\Phi out * \frac{Ipump}{\pi} * \frac{1}{sC} \qquad Eq. \quad A.3$$

The overall transfer functions of the DLL can be written using equation A.1, 2, 3 as,

$$\frac{\Phi out}{\Phi in} = \frac{1}{1 + \frac{Ipump}{\pi} * \frac{1}{sC} * \frac{to}{Vin.vcdl} * \omega clk} \qquad Eq. \quad A.4$$

APPENDIX B

WIDE-RANGE DELAY-LOCKED LOOP MODULES

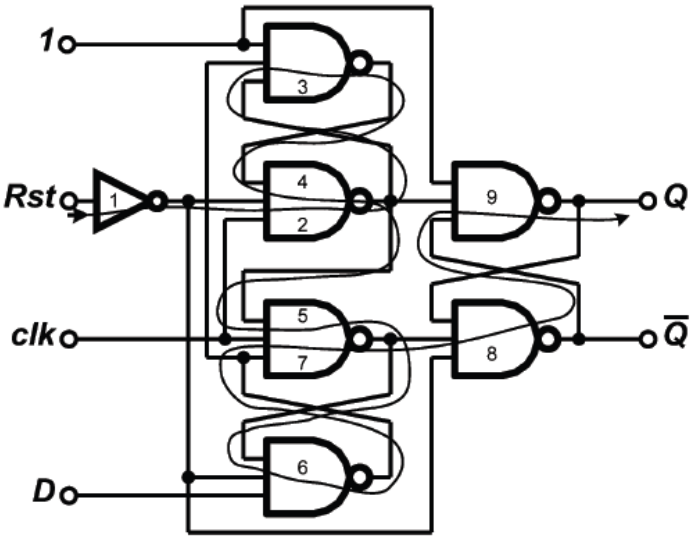


Fig. B.1. Schematic block of resettable DFF used in the start-controlled PFD.

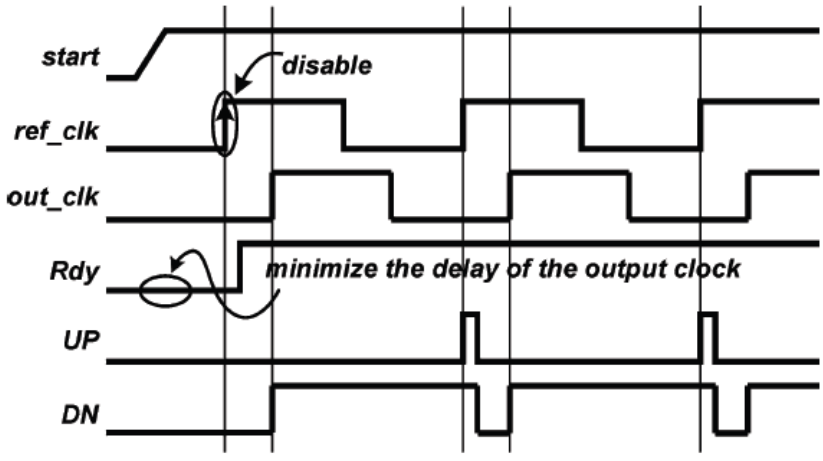


Fig. B.2. Schematic block of the PFD with control circuit.

APPENDIX C

THE VOLTAGE BASED CHARGE PUMP

Schematic of the voltage charge pump implemented in the analog DLL, in order to mitigated the persistent inverted lock error generated by an ion strike within the CP.

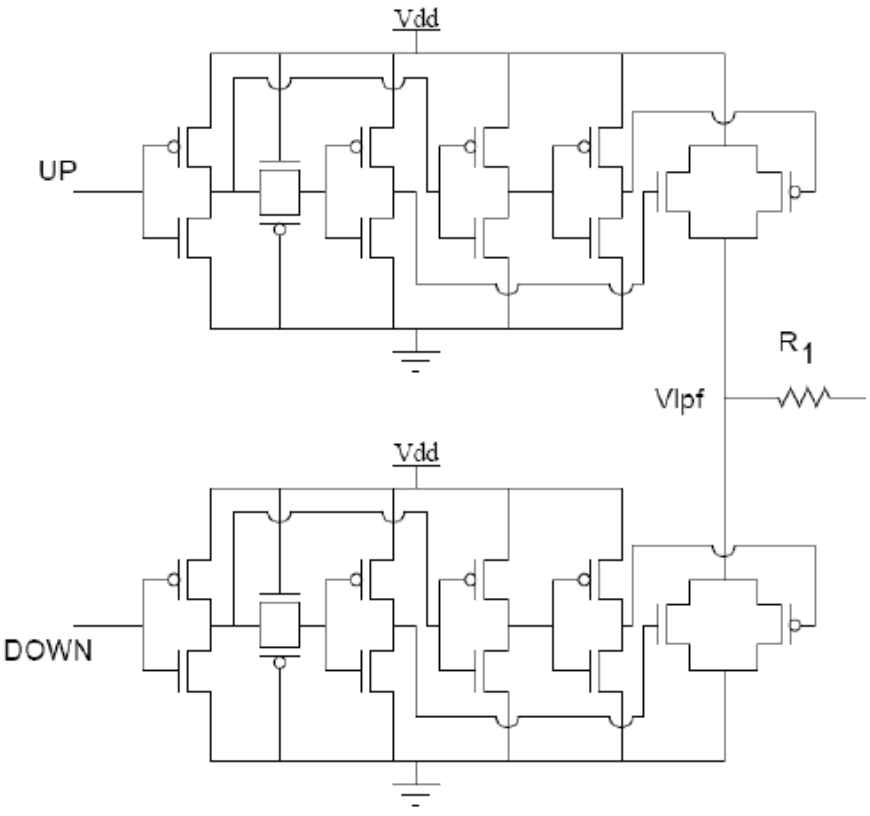


Fig. C.1. Schematic of the voltage based charge pump with low pass filter, used to mitigate inverted lock error in the analog DLL [6].

APPENDIX D

ANALOG DELAY LOCKED LOOP SPICE NETLIST

```
// Generated for: spectre
// Generated on: May 27 13:41:16 2009
// Design library name: DLL_042009
// Design cell name: DLL_1Ghz_cs
// Design view name: schematic
simulator lang=spectre
global 0 Up! Down! Vvcdl! vdd!
parameters stkdelay=210n R=9k wp=960n wpb=580n wnb=340n wn=400n
wpd1=560n \
    lpd1=160n wpd2=280n lpd2=80n wnd1=560n lnd1=160n wnd2=280n
lnd2=80n
include
"/usr/local/isde/PDK/IBM_PDK/cmos9sf/relIBM/Spectre/models/design.scs"
include
"/usr/local/isde/PDK/IBM_PDK/cmos9sf/relIBM/Spectre/models/fixed_corne
r.scs"
include
"/usr/local/isde/PDK/IBM_PDK/cmos9sf/relIBM/Spectre/models/process.scs
"

// Library name: DLL
// Cell name: invX1
// View name: schematic
subckt invX1 in out vdd vss
    T0 (out in vdd vdd!) lvtpfet w=480.0n l=80n par=1 m=1 ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T1 (out in vss 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f as=48.0f
\
        pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends invX1
// End of subcircuit definition.


// Library name: 20060706_90nm_CP_VCP
// Cell name: p_switch_1.2
// View name: schematic
```

```
subckt _sub0 SW0 SW1 in
    I13 (net021 net039 vdd! 0) invX1
    I14 (in net019 vdd! 0) invX1
    I12 (net024 net051 vdd! 0) invX1
    IP1 (net019 net024 vdd! 0) invX1
    T0 (SW0 net051 SW1 vdd!) pfet w=2.74u l=160.0n par=1 m=1 ad=657.6f
\
        as=657.6f pd=5.96u ps=5.96u nf=1 dtemp=0.0 rgatemod=0
sa=260.0n \
        sb=260.0n sd=280.0n panw1=0 panw2=0 panw3=0 panw4=0 panw5=0 \
        panw6=0 panw7=0 panw8=0 panw9=0 panw10=0
    TN2 (net021 0 net019 vdd!) pfet w=1.83u l=80n par=1 m=1 ad=439.2f
\
        as=439.2f pd=4.14u ps=4.14u nf=1 dtemp=0.0 rgatemod=0
sa=140.0n \
        sb=100n sd=280.0n panw1=0 panw2=0 panw3=0 panw4=0 panw5=0
panw6=0 \
        panw7=0 panw8=0 panw9=0 panw10=0
    T3 (SW0 net039 SW1 0) nfet w=1.14u l=160.0n par=1 m=1 ad=273.6f \
        as=273.6f pd=2.76u ps=2.76u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=260.0n sb=260.0n sd=280.0n panw1=0 panw2=0 panw3=0 panw4=0
\
        panw5=0 panw6=0 panw7=0 panw8=0 panw9=0 panw10=0
    TN1 (net021 vdd! net019 0) nfet w=915.00n l=80n par=1 m=1
ad=237.9f \
        as=237.9f pd=2.35u ps=2.35u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=100n sb=140.0n sd=280.0n panw1=0 panw2=0 panw3=0 panw4=0 \
        panw5=0 panw6=0 panw7=0 panw8=0 panw9=0 panw10=0
ends _sub0
// End of subcircuit definition.

//DESCRIPTION OF THE CHARGE PUMP MODULE
// Library name: 20060706_90nm_CP_VCP
// Cell name: CP_250nA_1.2
// View name: schematic
subckt _sub1 ChDown ChUp Vcap
    I0 (net42 Vcap ChUp) _sub0
    I1 (Vcap net27 ChDown) _sub0
    T5 (net27 vnbias 0 0) nfet w=8.57u l=1u par=1 m=1 ad=2.0568p \
        as=2.0568p pd=17.62u ps=17.62u nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=260.0n sb=260.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T2 (vpbias vnbias 0 0) nfet w=3.5u l=80n par=1 m=1 ad=910.0f
as=910.0f \
        pd=7.52u ps=7.52u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
```

```
    T9 (vdd! vdd! n1 0) nfet w=900n l=900n par=1 m=1 ad=234.00f
as=234.00f \
        pd=2.32u ps=2.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=260.0n
\
        sb=260.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T13 (n1 n1 vnbias 0) nfet w=900n l=900n par=1 m=1 ad=234.00f \
        as=234.00f pd=2.32u ps=2.32u nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=260.0n sb=260.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T15 (0 vnbias vnbias 0) nfet w=720.0n l=720.0n par=196349776 m=1 \
        ad=187.2f as=187.2f pd=1.96u ps=1.96u nf=1 ptwell=1 dtemp=0.0
\
        rgatemod=0 sa=260.0n sb=260.0n sd=0 panw1=0p panw2=0p panw3=0p
\
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p
panw10=0p
    T1 (net42 vpbias vdd! vdd!) pfet w=4.23u l=3u par=1 m=1 ad=1.0998p
\
        as=1.0998p pd=8.98u ps=8.98u nf=1 dtemp=0.0 rgatemod=0
sa=260.0n \
        sb=260.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (vpbias vpbias vdd! vdd!) pfet w=3.5u l=80n par=1 m=1 ad=910.0f
\
        as=910.0f pd=7.52u ps=7.52u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends _sub1
// End of subcircuit definition.

//DESCRIPTION OF THE DYNAMIC PASHE DECTECTOR MODULE
// Library name: DLL
// Cell name: Dynamic_PD_lvt
// View name: schematic
subckt Dynamic_PD_lvt Down Up clk data
    T19 (Up net0114 vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1
ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T7 (Down net0125 vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1
ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
```

```
    T11 (net92 clk vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1
ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T17 (net84 data vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1
ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T18 (net0114 up_int vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1 \
        ad=115.2f as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T10 (net0125 down_int vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1
\
        ad=115.2f as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T16 (up_int clk net84 vdd!) lvtpfet w=480.0n l=80n par=1 m=1
ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T12 (down_int data net92 vdd!) lvtpfet w=480.0n l=80n par=1 m=1 \
        ad=115.2f as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T20 (net99 down_int 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f \
        as=48.0f pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T21 (down_int clk 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f \
        as=48.0f pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T14 (up_int data 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f
as=48.0f \
        pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
```

```
    T8 (Down net0125 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f
as=48.0f \
        pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T9 (net0114 clk net95 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f \
        as=48.0f pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T6 (Up net0114 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f
as=48.0f \
        pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T13 (net95 up_int 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f \
        as=48.0f pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T15 (net0125 data net99 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f
\
        as=48.0f pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends Dynamic_PD_lvt
// End of subcircuit definition.

//DESCRIPTION OF THE VCDL BIASING CIRCUIT
// Library name: DLL
// Cell name: vcdl_input_stage_R
// View name: schematic
subckt _sub2 n_in n_out p_out
    R0 (net37 0) resistor r=R
    T1 (n_out p_out vdd! vdd!) lvtpfet w=wpb l=80n par=1 m=1 \
        ad=(wpb*2.4e-07) as=(wpb*2.4e-07) pd=(2*wpb+2*2.4e-07) \
        ps=(2*wpb+2*2.4e-07) nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n \
        sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p \
        panw7=0p panw8=0p panw9=0p panw10=0p
    T14 (p_out p_out vdd! vdd!) lvtpfet w=wpb l=80n par=1 m=1 \
        ad=(wpb*2.4e-07) as=(wpb*2.4e-07) pd=(2*wpb+2*2.4e-07) \
        ps=(2*wpb+2*2.4e-07) nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n \
        sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p \
        panw7=0p panw8=0p panw9=0p panw10=0p
    T3 (n_out n_out 0 0) lvtnfet w=wnb l=80n par=1 m=1 ad=(wnb*2.4e-
07) \
```

```
        as=(wnb*2.4e-07) pd=(2*wnb+2*2.4e-07) ps=(2*wnb+2*2.4e-07)
nf=1 \
        ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n sb=240.0n sd=0
panw1=0p \
        panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p
\
        panw9=0p panw10=0p
    T4 (p_out p_out net37 net37) lvtnfet w=140.0n l=80n par=1 m=1
ad=33.6f \
        as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0 \
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T8 (p_out n_in 0 0) lvtnfet w=wnb l=80n par=1 m=1 ad=(wnb*2.4e-07)
\
        as=(wnb*2.4e-07) pd=(2*wnb+2*2.4e-07) ps=(2*wnb+2*2.4e-07)
nf=1 \
        ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n sb=240.0n sd=0
panw1=0p \
        panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p
\
        panw9=0p panw10=0p
ends _sub2
// End of subcircuit definition.

//DESCRIPTION OF THE OUTPUT BUFFERS
// Library name: DLL
// Cell name: invX8
// View name: schematic
subckt invX8 in out
    T1 (out in 0 0) lvtnfet w=1.6u l=80n par=1 m=1 ad=384.00f
as=384.00f \
        pd=3.68u ps=3.68u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (out in vdd! vdd!) lvtpfet w=3.84u l=80n par=1 m=1 ad=921.6f \
        as=921.6f pd=8.16u ps=8.16u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends invX8
// End of subcircuit definition.

// Library name: DLL
// Cell name: invX4
// View name: schematic
subckt invX4 in out
    T1 (out in 0 0) lvtnfet w=800n l=80n par=1 m=1 ad=192.00f
as=192.00f \
```

```
        pd=2.08u ps=2.08u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (out in vdd! vdd!) lvtpfet w=1.92u l=80n par=1 m=1 ad=460.8f \
        as=460.8f pd=4.32u ps=4.32u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends invX4
// End of subcircuit definition.

// Library name: DLL
// Cell name: invX2
// View name: schematic
subckt invX2 in out
    T1 (out in 0 0) lvtnfet w=400n l=80n par=1 m=1 ad=96.0f as=96.0f \
        pd=1.28u ps=1.28u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (out in vdd! vdd!) lvtpfet w=960.0n l=80n par=1 m=1 ad=230.4f \
        as=230.4f pd=2.4u ps=2.4u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends invX2
// End of subcircuit definition.

// Library name: DLL
// Cell name: invX1
// View name: schematic
subckt invX1_schematic in out
    T1 (out in 0 0) lvtnfet w=200n l=80n par=1 m=1 ad=48.0f as=48.0f \
        pd=880.0n ps=880.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (out in vdd! vdd!) lvtpfet w=480.0n l=80n par=1 m=1 ad=115.2f \
        as=115.2f pd=1.44u ps=1.44u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends invX1_schematic
// End of subcircuit definition.

//DESCRIPTION OF THE VCDL DELAY CELL
// Library name: DLL
// Cell name: vcdl_stage_1GHz
// View name: schematic
subckt _sub3 _net0 n_in out p_in
```

```
    T40 (net050 p_in vdd! vdd!) lvtpfet w=wpb l=80n par=1 m=1 \
        ad=(wpb*1e-07) as=(wpb*2.4e-07) pd=(wpb+2*1e-07) \
        ps=(2*wpb+2*2.4e-07) nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=100n \
        sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p \
        panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (out _net0 net050 vdd!) lvtpfet w=wp l=80n par=1 m=1 ad=(wp*1e-
07) \
        as=(wp*2.4e-07) pd=(wp+2*1e-07) ps=(2*wp+2*2.4e-07) nf=1
dtemp=0.0 \
        rgatemod=0 sa=240.0n sb=100n sd=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p
panw10=0p
    T1 (out _net0 net20 0) lvtnfet w=wn l=80n par=1 m=1 ad=(wn*1e-07)
\
        as=(wn*2.4e-07) pd=(wn+2*1e-07) ps=(2*wn+2*2.4e-07) nf=1
ptwell=1 \
        dtemp=0.0 rgatemod=0 sa=240.0n sb=100n sd=0 panw1=0p panw2=0p
\
        panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p
\
        panw10=0p
    T27 (net20 n_in 0 0) lvtnfet w=wnb l=80n par=1 m=1 ad=(wnb*1e-07)
\
        as=(wnb*2.4e-07) pd=(wnb+2*1e-07) ps=(2*wnb+2*2.4e-07) nf=1 \
        ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n sb=100n sd=0 panw1=0p
\
        panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p
\
        panw9=0p panw10=0p
ends _sub3
// End of subcircuit definition.

//DESCRIPTION OF THE VCDL MODULE
// Library name: DLL
// Cell name: vcdl_1.2_1Ghz_0
// View name: schematic
subckt _sub4 v_out_11 in o1 o2 o4 vcdl_in
    I130 (vcdl_in n_bias p_bias) _sub2
    I125 (o4 v_out_11) invX8
    I124 (o2 o4) invX4
    I123 (o1 o2) invX2
    I121 (net075 o1) invX1_schematic
    I133 (net088 n_bias net092 p_bias) _sub3
    I72 (net104 n_bias net112 p_bias) _sub3
    I103 (net100 n_bias v_out_7 p_bias) _sub3
    I95 (net112 n_bias net96 p_bias) _sub3
    I117 (net049 n_bias net086 p_bias) _sub3
    I109 (net68 n_bias net049 p_bias) _sub3
    I131 (net074 n_bias net078 p_bias) _sub3
    I136 (net092 n_bias net080 p_bias) _sub3
```

```
    I134 (net078 n_bias net088 p_bias) _sub3
    I135 (net080 n_bias net075 p_bias) _sub3
    I137 (net086 n_bias net074 p_bias) _sub3
    I101 (net84 n_bias net68 p_bias) _sub3
    I98 (net108 n_bias net100 p_bias) _sub3
    I97 (net92 n_bias net108 p_bias) _sub3
    I100 (net76 n_bias net84 p_bias) _sub3
    I31 (in n_bias net104 p_bias) _sub3
    I99 (v_out_7 n_bias net76 p_bias) _sub3
    I96 (net96 n_bias net92 p_bias) _sub3
ends _sub4
// End of subcircuit definition.

//DESCRIPTION OF THE ANALOG DLL
// Library name: DLL_042009
// Cell name: DLL_1Ghz_cs
// View name: schematic
I0 (Vvcdl! vdd!) isource \
        file="~/20060809_90nm_IonStrikeCurves/pmoslet20a.txt" type=pwl
\
        delay=stkdelay
I9 (Down! Up! Vvcdl!) _sub1
I13 (Down! Up! in Out) Dynamic_PD_lvt
I12 (Out in o1 o2 o4 Vvcdl!) _sub4
C0 (Vvcdl! 0) capacitor c=426f
include "./_graphical_stimuli.scs"
ic Vvcdl!=0.3
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12
temp=27 \
    tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=500n write="spectre.ic"
writefinal="~/DLL_1GHz_CP_IL.fc" \
    annotate=status maxiters=5
    settings options rawfmt=nutascii
    save in Out Vvcdl!
saveOptions options save=selected
```

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